Frequency Generation for ADPLLs in Automotive FMCW Radar using Nano-Scale CMOS

Von der Fakultät für Elektrotechnik und Informationstechnik
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vorgelegt von

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To you and me, to the future and to life

人生如逆旅，我亦是行人。

- 苏轼

Life is like a guest house; I, too, am but a traveler.

- Su Shi

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It has been such a long yet wonderful journey for me to finally be able to present this work. I come from a small city at an altitude of more than 2,400 m in the Hengduan Mountains of China. A mountain of around 5,600 m locates right at the doorstep of my hometown. Lying in the transitional area from the Yun-Gui Plateau to the Himalayas, despite the fame for its spectacular landscape, my hometown remains till today very remote and non-industrialized. Surrounded by these high mountains, even visiting a county that is merely 100 km away would take more than 4 hours of driving on the twisted mountain road. It wasn't until 2010 that the first railway and, subsequently, in 2013, a motorway connected our town to the outer world. Growing up in such a remote area, being able to research cutting-edge topics in microelectronics alongside some of the brightest minds in the world was beyond anything I could have imagined.

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王澜涛 Lantao Wang
Hamburg, Germany, September 2024

CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

ACC	autonomous cruise control
ADC	analog-to-digital converter
ADPLL	all-digital phase-locked loop
AM	amplitude modulation
ASIC	application-specific integrated circuit
CCNMOS	constantly-conducting NMOS
CI	chirp signal injection
CKV	frequency-variable DCO clock
CMF	carrier mobility fluctuation
CMOS	complementary metal-oxide semiconductor
CNF	carrier number fluctuation
CP	charge pump
DAC	digital-to-analog converter
DCO	digitally-controlled oscillator
DCRO	digitally-controlled ring oscillator
DDS	direct digital synthesizer
DFLL	digital frequency-locked loop
DI	dithered signal injection
DLF	digital loop filter
DSP	digital signal processing
EA	error amplifier
ESR	equivalent series resistance
EVM	error vector magnitude
FCW	frequency control word
FFT	fast Fourier transform
FMCW	frequency-modulated continuous-wave
FoM	figure-of-merit
IF	intermediate frequency
ISF	impulse sensitivity function

LDO	low-dropout regulator
LF	loop filter
LFSR	linear feedback shift register
LNA	low-noise amplifier
LNLDO	low-noise low-dropout regulator
LO	local oscillator
LPF	low-pass filter
LSB	least significant bit
LTI	linear time-invariant
LTV	linear time-variant
MEMS	micro-electro-mechanical systems
MIM	metal-insulator-metal
MIMO	multiple-input and multiple-output
MOM	metal-oxide-metal
MOS	metal-oxide-semiconductor
MSB	most significant bit
NRB	negative resistance boost
OTA	operational transconductance amplifier
PA	power amplifier
PCB	printed circuit board
PFD	phase frequency detector
PHE	phase error
PHR	reference phase
PHV	variable clock phase
PLL	phase-locked loop
PM	phase modulation
PSD	power spectral density
PSR	power supply rejection
PSRR	power supply rejection ratio
PVT	process, voltage and temperature
RA	reference amplifier
radar	radio detection and ranging
RF	radio frequency
RFIC	radio-frequency integrated circuit
RMS	root mean square
RO	ring oscillator

RX receiver
SC switchable capacitor
SNR signal-to-noise ratio
SoC system-on-chip
SPI serial peripheral interface
SSB single-sided band
TDC time-to-digital converter
TR tuning range
TX transmitter
VCO voltage controlled oscillator
VGA variable gain amplifier

LIST OF SYMBOLS

B	bandwidth of a chirp signal
c_0	speed of light
C_{mom}	capacitance of MOM capacitor
C_{off}	off-state capacitance
C_{on}	on-state capacitance
Q_{off}	off-state quality factor
Q_{on}	on-state quality factor
R_{on}	on-state resistance
C_{ox}	capacitance per unit area of the gate oxide
ΔC	difference of on- and off-state capacitance
ESR_{mom}	equivalent series resistance of MOM capacitor
f_0	carrier frequency
f_{beat}	beat frequency in FMCW radar receiver
f_r	range caused frequency shift in the radar echo signal
C_{par}	parasitic capacitance
f_{res}	oscillator tuning resolution
f_T	transit frequency of a transistor
f_v	Doppler effect frequency shift in the radar echo signal
γ	noise coefficient of MOSFET
g_m	transconductance
k_B	Boltzmann constant
R_{pu}	pull-up resistance
T	absolute temperature
T_0	chirp signal period
V_{DD}	power supply voltage
V_{SS}	ground reference voltage
V_{th}	threshold voltage

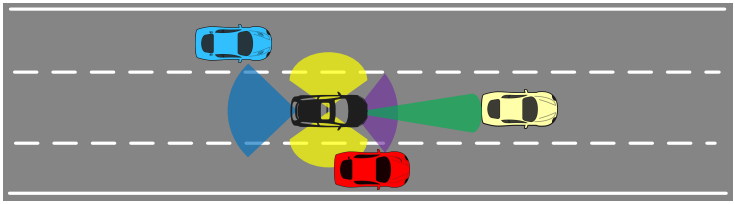
CHAPTER 1

INTRODUCTION

Since the early 1970s, applications of radio detection and ranging (radar) in automobiles have drawn significant attention from both industry and academia, as it is a highly effective method to avoid collisions and reduce the accident rate. However, because of the bulky size, it was very difficult to integrate radar in a commercial product [1]. In 1999, Mercedes-Benz became the first automobile company to equip a radar-based autonomous cruise control (ACC), so-called *DISTRONIC*, in its S-class, and other car companies, such as Nissan and BMW, quickly followed up in 2000 [2, 3]. Since then, radar sensor technology has advanced rapidly, aided by down-scaling technologies that have made these systems more affordable and easier to integrate. Today, automotive radar systems are widely employed across various products and manufacturers. Fig. 1.1 shows the general categories of the automotive radars used in a modern vehicle. Based on their different maximum detectable range, they are classified as long-range radar, medium-range radar and short-range radar, each suited for different driving scenarios [4].

Modern radar systems have undergone a significant shift in operating frequency, moving from the 24/26 GHz band to the 77-81 GHz band. One of the primary reasons for this shift is that antennas operating in the 77 GHz band are considerably smaller compared to those in the 24/26 GHz band, enabling the installation of larger arrays of 77 GHz radar antennas to achieve better angular measurement resolution. Additionally, the 77-81 GHz band offers a wider bandwidth of 4 GHz, which significantly enhances the resolution of distance and velocity measurements, whereas the narrow 24 GHz band provides only a 200 MHz bandwidth. Furthermore, regulatory standards set by the European Telecommunications Standards Institute (ETSI) [5] and the Federal Communications Commission (FCC) [6] have restricted the use of the ultra-wide-band from 21.65-26.65 GHz in both Europe and the U.S. effective 01. January 2022 [7].

However, designing a system in 77-81 GHz is more challenging and has stricter requirement on the technology. Conventionally, automotive semiconductor companies use compound technologies such as GaAs or SiGe BiCMOS



Long Range Radar: ACC, Automatic Emergency Braking, Forward Collision Warning

Short Range Radar: Park Assist, Junction Assist

Medium Range Radar: Cross Traffic Alert

Medium Range Radar: Blind Side Detection, Rear Collision Warning

Figure 1.1: Distance measurement using chirp signal.

to design and fabricate their radar transceivers, e.g. NXP [8] and Infineon [9]. But the cost of fabrication in these technologies is very high and 77 GHz radar could therefore only be equipped in the premium or luxury vehicles. On the other hand, the fabrication cost in a complementary metal-oxide semiconductor (CMOS) technology is much more affordable due to its high yield and a much higher level of integration. Hence, implementing automotive radar systems in a complementary metal-oxide semiconductor (CMOS) technology is of great value in expanding the usage of radars across all traffic participants to reduce casualties in the accident.

However, unlike in a e.g. SiGe technology, when designing in a CMOS technology, designers do not have the luxury to apply high voltage on the devices to obtain high output power. Moreover, the transit frequency of the active devices in a CMOS technology is also relatively lower, limiting the maximum operating frequency. But with the rapid scaling down of processes to the era of 90 nm, researchers have started to report highly integrated 77 GHz radar transceivers, e.g. in [10–12], proving it is a feasible solution. Yet, the radar system design in CMOS has become increasingly complicated with the continuously shrinking technology and the challenges it brings [13], e.g. the supply voltage headroom is becoming much smaller, but the threshold voltage remains unscaled. In addition, in a nano-scale technology, the process, voltage and temperature (PVT) variations are more severe and has much more impact on the performance. Thus only very recently, companies have started

to release such products [14, 15] in an advanced CMOS technology node. Automotive radar design in an advanced CMOS technology hence remains till today a very hot topic both in academia and industry.

In an automotive frequency-modulated continuous-wave (FMCW) radar transceiver, using a phase-locked loop (PLL) to generate the modulated chirp signal whose frequency increases linearly with time, is a common solution to achieve a good linearity. The traditional analog phase-locked loop (PLL), however, has the disadvantage of a larger area occupation due to the analog loop filter constructed by passive devices. Moreover, the loop bandwidth is not adjustable in an analog PLL, making it less flexible to support various functions.

With the continuous down-scaling of the CMOS technology, an all-digital phase-locked loop (ADPLL) is becoming increasingly interesting as it can potentially address the challenges in the conventional analog PLL. Moreover, this type of PLL has better scalability, thus reducing the potential re-design effort. Nevertheless, the strict specifications of automotive radar applications induce harsh requirements on the design of an all-digital phase-locked loop (ADPLL). First, the digitization of the voltage controlled oscillator (VCO), i.e. digitally-controlled oscillator (DCO) in an ADPLL introduces quantization noise, which does not exist in the analog counterpart, which requires a very fine tuning resolution of the digitally-controlled oscillator (DCO). Secondly, at the same time, the tuning range of the DCO must be expansive enough to cover the widening PVT spread inherent in a nano-scale technology and to ensure a large bandwidth for the modulated chirp signal. Furthermore, the shrinking technology, resulting in narrower metal tracks, leads to a decline in the quality factor of passive devices, thereby limiting the phase noise performance of oscillators. These requirements pose design challenges on the implementation of the frequency generation circuits in an ADPLL and call for innovative solutions. The goal of this thesis is thus to explore frequency generation circuit topologies, primarily the DCO and the crystal oscillator, to push the performance limits further.

1.1 Research Contribution

Throughout the work of this thesis, the author proposed several design innovations in the frequency generation circuits with the potential to enhance the overall performance of the ADPLL. Three prototypes were designed and fabricated in a 28 nm CMOS technology. Fig. 1.2 provides the micrographs of

the developed chips. These innovations, validated with silicon measurement results, were also presented by the author in various peer-reviewed papers [16–21].

In the initial prototype, identified as project *PANDA* and taped out in November 2020, whose micrograph is shown in Fig. 1.2(a), the author introduced an innovative switchable capacitor (SC) architecture utilizing constantly-conducting NMOS (CCNMOS) to increase the tuning resolution and improve the transient performance of the oscillator [16]. A class-B DCO was implemented using this novel switchable capacitor (SC) architecture, demonstrating excellent phase noise and frequency tuning performance. With a comparable figure-of-merit (FoM) to the state-of-the-art solutions, the proposed DCO exhibits an inherent frequency tuning and very fine resolution, making it particularly advantageous in the application of ADPLL. Moreover, a low-noise low-dropout regulator (LNLDO) was designed by the author to serve as the power supply for the noise-sensitive RF blocks including the DCO and the time-to-digital converter (TDC) [16, 17, 19, 20, 22]. The author also made significant contributions to the implementation of the digital clock and buffer module of this chip.

The second chip, designated as project *RedPANDA* and taped out in November 2021, as shown in Fig. 1.2(b), featured a crystal oscillator with fast start-up implemented by the author [18]. The DCO on this chip employed a class-C architecture to reduce the area occupation. Furthermore, the SC bank underwent a redesign, aiming to achieve a higher DCO frequency and wider tuning range [19]. Notably, the author took charge of the physical implementation of the retiming module and the top-level integration of this chip.

The contribution of the author to the third chip, named project *Cheetah*, taped out in July 2023 and depicted in Fig. 1.2(c), encompassed the implementation of bias voltage regulation for the class-C DCO and auxiliary circuitry for better measurability of the crystal oscillator.

1.2 Thesis Organization

Chapter 2 starts with a brief review of the fundamentals of FMCW radar and then moves into the system architecture and the requirements of the FMCW transceiver. Subsequently, the demand on the frequency generation circuits and the design challenges are explained in this chapter.

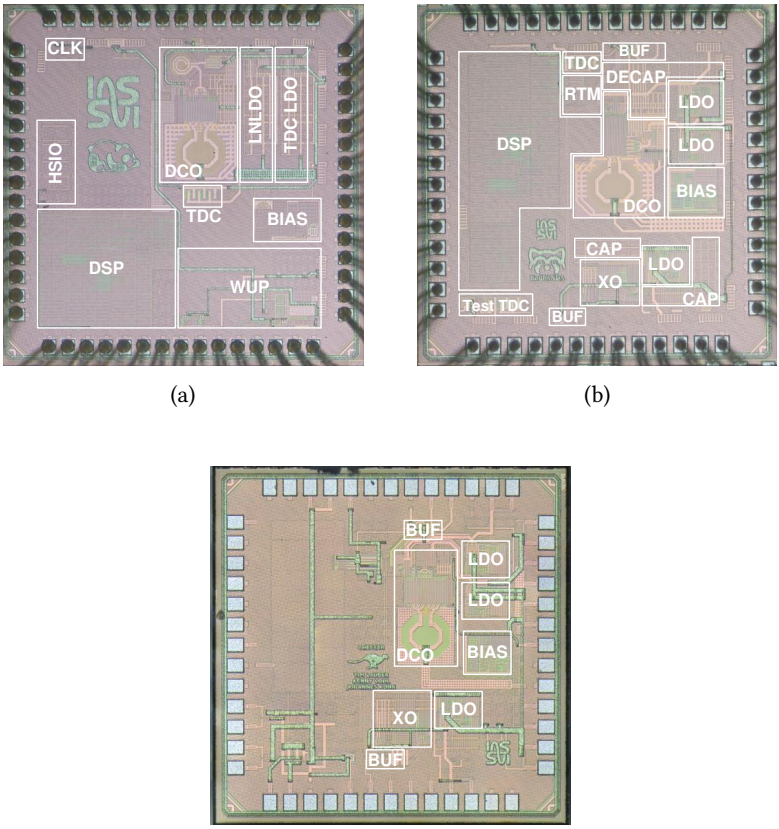


Figure 1.2: Micrographs of the 28 nm chips relevant to this thesis. (a) Project *PANDA*. (b) Project *RedPANDA*. (c) Project *Cheetah*.

The scope of Chapter 3 covers various design aspects of *LC* oscillators. This chapter starts with basics of passive devices, followed by the introduction and comparison of different oscillator core structures. Thereafter, switchable capacitor (SC) architectures are discussed in detail, and this chapter also illustrates the design methodology of the SC array. Lastly, two *LC* oscillators with an innovative SC architecture, fabricated in a 28 nm CMOS technology are presented and the measurement results are compared with the state-of-the-art.

Chapter 4 discusses how the power supply influences the noise performance of the frequency generation circuits. Design and implementation of a low-noise low-dropout regulator (LNLDO) in a 28 nm CMOS technology is then presented and the measurement results demonstrate the necessity to include such a block in the high-demand and noise sensitive application.

Chapter 5 focuses on the design and analysis of crystal oscillators. First, characteristics of quartz crystal and its electrical mode are introduced. Thereafter, structures of crystal oscillators are briefly reviewed. Crystal oscillators featuring two different start-up acceleration schemes are then introduced.

Chapter 6 summarizes the thesis and provides an outlook for future developments.

CHAPTER 2

FUNDAMENTALS AND SYSTEM CONSIDERATION OF FREQUENCY GENERATION CIRCUITS

In this chapter, the basics of automotive radar are briefly introduced. Thereafter, we dive deeper into the architectures of 77-81 GHz radar transceivers and explain the system requirements for the frequency generation blocks.

2.1 Fundamentals of FMCW Radar

2.1.1 Distance Measurement

The distance measurement using FMCW radar is carried out by sending modulated electromagnetic chirp signal ,whose frequency increases from f_0 by a bandwidth of B linearly within the signal period T_0. Fig. 2.1 illustrates the FMCW radar measurement. The chirp signals transmitted from the radar transmitter (TX) are reflected by the vehicle in front and received by the radar receiver (RX).

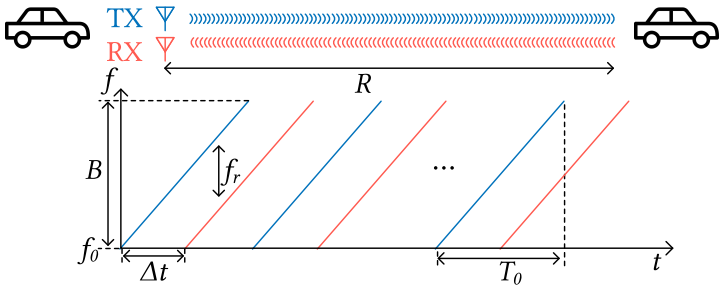


Figure 2.1: Distance measurement using chirp signal.

As the signal traveled a distance of $2R$, a delay Δt is generated by the time

of flight, which can be represented by:

$$\Delta t = \frac{2R}{c_0} \tag{2.1}$$

where c_0 is the speed of light. The frequency difference f_r, introduced by the distance R, is constant at each measure time point as the chirp signal is linear. In practice, f_r can be easily derived by mixing the received signal with the transmitted signal. The frequency of this down-converted signal is also called beat frequency f_beat. In the case of measuring a motionless object, f_beat equals to f_r. The distance information is carried by f_r that can be written as:

$$f_r = \frac{B}{T_0}\Delta t \tag{2.2}$$

The distance R can thus be obtained by

$$\begin{aligned} R &= \frac{c_0}{2}\Delta t \\ &= \frac{c_0}{2}\frac{T_0}{B}f_\mathrm{r} \end{aligned} \tag{2.3}$$

The maximum measurable range is then

$$R_\mathrm{max} = \frac{c_0 T_0 f_{r_\mathrm{max}}}{2B} \tag{2.4}$$

where $f_{\mathrm{r}_\mathrm{max}}$ is limited by the sampling rate of the receiver chain f_s, and according to Nyquist sampling theorem, the following equation holds:

$$f_{r_\mathrm{max}} = \frac{1}{2}f_\mathrm{s} \tag{2.5}$$

The range measurement resolution R_min is determined by the modulation bandwidth B, as in

$$R_\mathrm{min} = \frac{c_0}{2B} \tag{2.6}$$

2.1.2 Velocity Measurement

If the measured object is moving, the reflected chirp signal experiences a frequency change due to the *Doppler effect*. Fig. 2.2 depicts the velocity measurement using a chirp FMCW radar, where f_v is the frequency offset introduced due to Doppler effect. The beat frequency f_beat varies depending

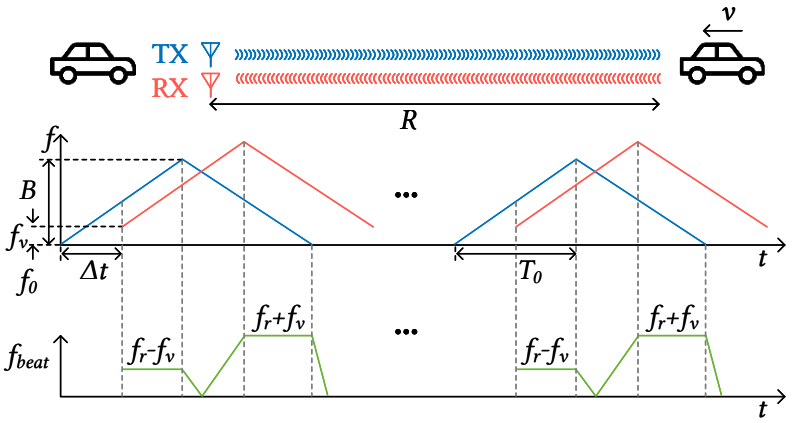


Figure 2.2: Chirp FMCW radar velocity and distance measurement.

on whether the chirped signal is ramping up or down. In the frequency increasing phase, the following equations holds:

$$f_{\text{beat,up}} = f_{\text{r}} - f_{\text{v}} \tag{2.7}$$

and for the frequency decreasing phase:

$$f_{\text{beat,down}} = f_{\text{r}} + f_{\text{v}} \tag{2.8}$$

The distance R and the velocity v can thus be obtained as [23]:

$$\begin{aligned} R &= \left(\frac{c_0 T_0}{4B}\right) \times \left(\frac{f_{\text{beat,up}} + f_{\text{beat,down}}}{2}\right) \\ v &= \left(\frac{c_0}{2f_0}\right) \times \left(\frac{f_{\text{beat,up}} - f_{\text{beat,down}}}{2}\right) \end{aligned} \tag{2.9}$$

Despite its simplicity, the traditional slow-chirp FMCW scheme has several disadvantages. First, if the radar needs detect multiple object, it lacks a definitive solution, i.e. some "ghost objects" will be detected by the receiver. Second, both the range shift frequency f_{r} and the Doppler frequency shift f_{v} are in a range of kilo-hertz, which is susceptible to flicker noise from the devices. This significantly limits the range detection resolution [23]. As a result, fast-chirp FMCW method, first introduced in [24], has become the preferred solution for most automotive radar applications [25–27].

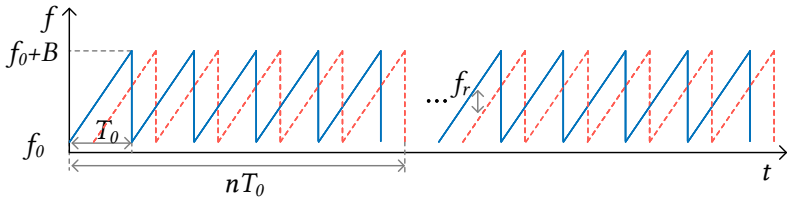


Figure 2.3: Fast chirp FMCW radar waveform.

As shown in Fig. 2.3, fast-chirp FMCW radar utilizes a sawtooth waveform to avoid ambiguity, i.e. the ghost targets problem in traditional chirp radar. The period of the sawtooth signal T_0 is designed to be in a range of several microsecond. From Eq. 2.3, f_r can be written as

$$f_r = \left(\frac{2R}{c_0}\right)\left(\frac{B}{T_0}\right) \tag{2.10}$$

The designed T_0 results in a much larger f_r in comparison to the Doppler frequency shift f_v. As a result, the Doppler frequency shift is neglected and the beat frequency f_beat can be purely used for distance measurement. In fact, in a modern fast chirp FMCW system, the distance is measured by performing a fast Fourier transform (FFT) to the down-converted f_beat. The velocity information, however, is embedded in the phase shift of the received signal, which is extracted by a second-dimension FFT. In this way, the velocity and distance measurement can be separated and f_r is moved away from devices' flicker noise region [23].

2.1.3 Fast-Chirp FMCW Radar Transceiver

Fig. 2.4 depicts the architecture of a commercial 77-81 GHz radar transceiver [28]. In general, the radar is a multiple-input and multiple-output (MIMO) with transceiver array.

In the transmitter path, a digital-to-analog converter (DAC) and chirp frequency synthesizer or the local oscillator (LO) generate the fast-chirp FMCW signal at around 76-81 GHz as discussed in 2.1. The chirp signal is directly connected to a power amplifier (PA), which amplifies the signal for transmission. On the receiver side, the antenna captures the reflected chirp radio frequency (RF) signal, which is then amplified by a low-noise amplifier (LNA). The intermediate frequency (IF) signal is obtained by the mixing the

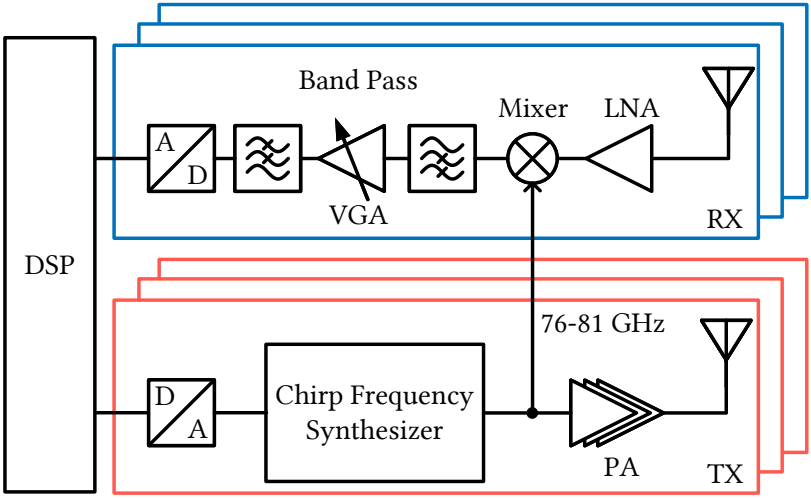


Figure 2.4: Architecture of a commercial fast-chirp FMCW radar transceiver [28].

received RF and the local oscillator (LO) signal. The combination of the band-pass filter and variable gain amplifier (VGA) further amplifies the IF signal for the processing of analog-to-digital converter (ADC).

2.1.4 Frequency Synthesis with Phase-Locked Loops

One of the most critical components in the FMCW radar transceiver is the frequency synthesizer, as it directly determines the noise level of the chirp signal. Despite the existence of several possibilities for frequency synthesis, the indirect frequency synthesizer using a phase-locked loop (PLL) is the most popular solution due to its superior spectral purity and robustness in comparison to direct synthesizers such as direct digital synthesizer (DDS) [29].

Fig. 2.5 shows the structure of the classic charge-pump based analog PLL. This type of PLL uses a phase frequency detector (PFD) to compare the phase and frequency relationship between the voltage controlled oscillator (VCO) frequency f_{LO} and the reference frequency f_{ref}, which is normally derived from a crystal oscillator. The following charge pump translates the signals

from PFD to a signal indicating the phase error between f_{LO} and f_{ref}. A low-pass filter, also called loop filter (LF), is incorporated to smooth the repetitive pulses generated by PFD and charge pump (CP) to eliminate the generation of large sidebands in the f_{LO}. The DC signal after the LF is introduced into a voltage controlled oscillator (VCO), whose output frequency is proportional to the applied voltage. The PLL is a negative feedback system, achieving the phase alignment of the LO clock with the reference clock when locked. This alignment implies equality in the frequencies of the two inputs of the PFD:

$$\begin{aligned} f_{ref} &= f_{LO,div} \\ &= \frac{f_{LO}}{N} \end{aligned} \tag{2.11}$$

Given that the output frequency of the PLL is N times the reference clock frequency, this configuration is commonly referred to as an integer-N PLL. By programming the divider factor N, the $f_{LO} = N \times f_{ref}$ can be synthesized.

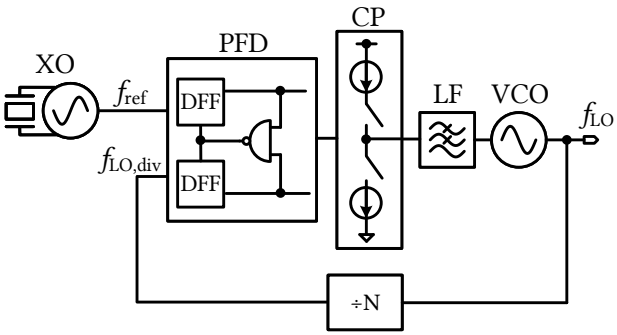


Figure 2.5: Block diagram of an integer-N analog PLL.

Despite its simplicity, the integer-N PLL exhibits several limitations. First, the frequency of the reference clock is limited by the channel spacing because the integer-N PLL can only generate $N \times f_{ref}$. A higher f_{ref} introduces a large quantization step in the chirp, which could affect the phase noise performance. On the other hand, reducing f_{ref} restricts the bandwidth of the LF, resulting in a prolonged PLL settling time and substantial footprint of resistor and capacitor in the LF.

These disadvantages can be mitigated by introducing a fractional divider. Fig. 2.6 shows the architecture of a fractional-N PLL, where the fractional divider is implemented by a ÷N/N+1 divider controlled by a dithered sig-

nal. As long as the frequency of dithered signal considerably surpasses loop bandwidth, the *effective* divide ratio for the PLL becomes an average value between N and N+1. Adjustment of the divide ratio is accomplished by tuning the percentage of time allocated to dividing f_{LO} by N and N+1. To address the generation of spurs in the output spectrum due to periodic signals, a $\Sigma\Delta$ modulator is commonly integrated into a fractional-N PLL to introduce randomness to the dither signal, converting the spurs into noise at higher frequency offsets, which is then regulated by the loop.

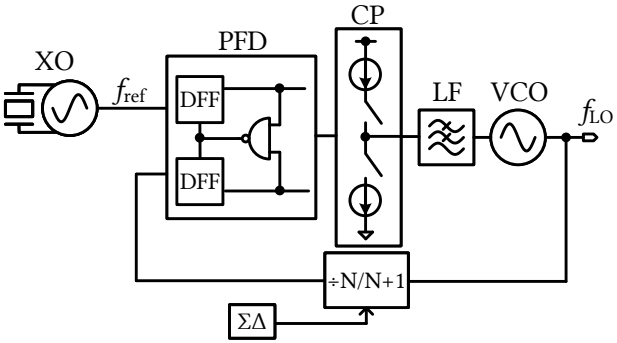


Figure 2.6: Structure of a fractional-N PLL.

The fractional-N PLL is widely used for the frequency band of 77-81 GHz of the FMCW radar application [4, 11, 30]. However, for a monolithic CMOS technology, despite the f_T of the transistors reaching around 200 GHz in an advanced technology, the quality factor of on-chip passive devices, particularly the inductor, often remains suboptimal due to the skin effect. This deteriorates the phase noise performance of the *LC* oscillator, typically serving as the VCO in a noise-critical application. Additionally, at such high frequencies, the oscillation period is on the order of tens of picoseconds, making the design of the PFD very challenging. For the optimal phase noise performance of the synthesizer, a good compromise is to select the operating frequency of the VCO to be multi-gigahertz and subsequently multiply the frequency to reach the FMCW radar band, as shown in works such as [31, 32].

Fig. 2.7 shows the architecture of a commercial RF-CMOS fast-chirp frequency synthesizer. This synthesizer employs a fractional-N PLL with a VCO frequency of 8.45-9 GHz. Following the VCO stage in the PLL loop, a frequency tripler is utilized, resulting in a frequency of 25.3-27 GHz. Subsequently, a second frequency tripler is connected after the PLL, converting the frequency to 76-81 GHz. The tripler can be implemented using a mixer,

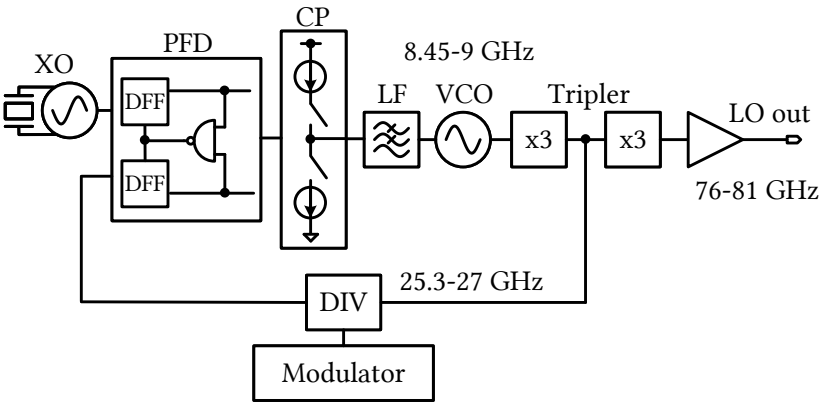


Figure 2.7: System overview of a commercial RF-CMOS fast-chirp frequency synthesizer [33].

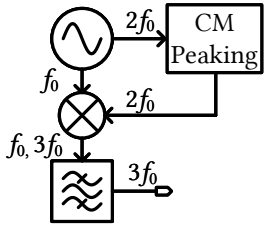


Figure 2.8: Architecture of a self-mixed frequency tripler [34].

as illustrated in Fig. 2.8. In this configuration, the VCO output frequency is mixed with its common-mode voltage, which represents the second harmonic. The output of the mixer contains first and third harmonic components.A band-pass filter is then used to isolate the tripled frequency [34, 35]. Alternative architectures include a frequency selection scheme for the broad-band operation [36], or directly extract the third harmonic from the VCO using a transformer [37–39].

2.2 All-Digital Phase-Locked Loops

Despite the analog PLL's ability to provide good performance and its popularity, it cannot fully exploit the benefits of continuously down-scaling CMOS technology due to the bulky LF. For example, in a typical analog chirp PLL, the LF is implemented using an RC low-pass filter. The resistor in this filter significantly contributes thermal noise to the overall phase noise of the PLL, limiting the value of the resistor. Consequently, the capacitors in the LF need to be very large, typically in the nano-farad range, which is very costly to implement in deep sub-micron technology. Moreover, the shrinking technologies lead to a reduced supply voltage, making it more difficult to design an analog charge pump, which dominates the in-band phase noise of the PLL.

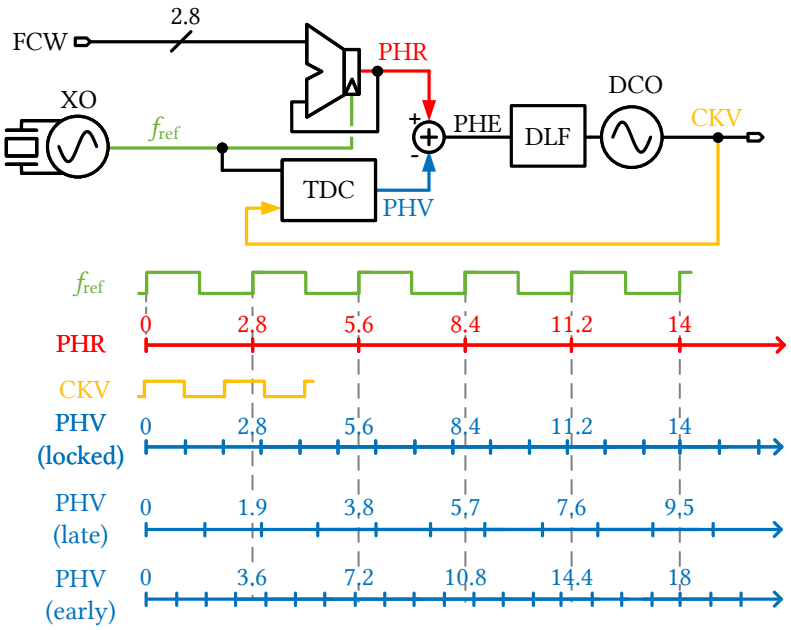


Figure 2.9: Functioning principle of the ADPLL.

On the other hand, digital circuits can perform much more complicated functions at a higher speed, making it advantageous to shift the RF system towards a digital-assisted approach in a nano-scale regime. In addition, the digital designs can scale down further with advancing technologies with less

effort, leading to long-term cost reductions.

To address these issues and better exploit the advantage of down-scaling CMOS technologies, an all-digital phase-locked loop (ADPLL) is introduced. By processing the phase difference between the reference and high-frequency oscillator in the digital domain, the analog LF can be replaced by a digital LF, implemented using logic gates and registers. Fig. 2.9 depicts the structure and illustrates the principles of an ADPLL. The ADPLL consists of a counter, a time-to-digital converter (TDC), a digital LF, and a digitally-controlled oscillator (DCO). The reference clock is provided by a crystal oscillator.

In the example shown in Fig. 2.9, the ADPLL aims at generating a phase-locked signal with the reference clock, where the frequency is 2.8 times higher. The frequency control word (FCW) is thus set to 2.8. At each rising edge of the reference clock, the counter accumulates the FCW into the reference phase (PHR). Meanwhile, the TDC compares the phase difference between the reference clock and the frequency-variable DCO clock (CKV), generating the variable clock phase (PHV). When the DCO frequency (f_{DCO}) equals FCW times the reference frequency (f_{ref}), PHV matches PHR. Consequently, the subtractor generates a phase error (PHE) of 0, indicating that the PLL is locked.

If the DCO frequency is lower than FCW times the reference frequency, the cycle number of CKV between two rising edges of the reference clock is smaller than FCW. In this case, PHV is 1.9 for a slower DCO. The subtractor calculates the difference between PHR and PHV, generating a positive PHE. The digital loop filter (DLF) accumulates the PHE and tunes up the frequency of the DCO. Conversely, when the DCO frequency is higher than FCW times the reference frequency, PHV will be larger than PHR, such as 3.6 in this example, resulting in a negative PHE, which eventually tunes down the frequency of the DCO. The feasibility of the utilizing an ADPLL to generate the chirp signal for a FMCW radar has been demonstrated in e.g. [40]. In comparison to the conventional analog counterpart, these ADPLL-based designs offer enhanced flexibility including improved configurability of loop bandwidth and superior linearity.

The TDC is a device that converts the time difference between the reference signal and CKV into digital codes. Fig. 2.10 illustrates the schematic of a basic delay-line based TDC and its functioning principle. The TDC consists of a chain of delay buffers with the CKV as the input. D-flip-flops are connected to the output of each buffer and sample the state of the outputs with the reference clock. Apparently, the resolution of the TDC is determined by the delay of the buffer for this basic delay-line based TDC. In order to further

increase the resolution, a 2-D structure, i.e. a Vernier TDC is implemented for the ADPLL of this work [22]. The complete schematic of the ADPLL[1] related to this dissertation is demonstrated in Fig. 2.11 [41].

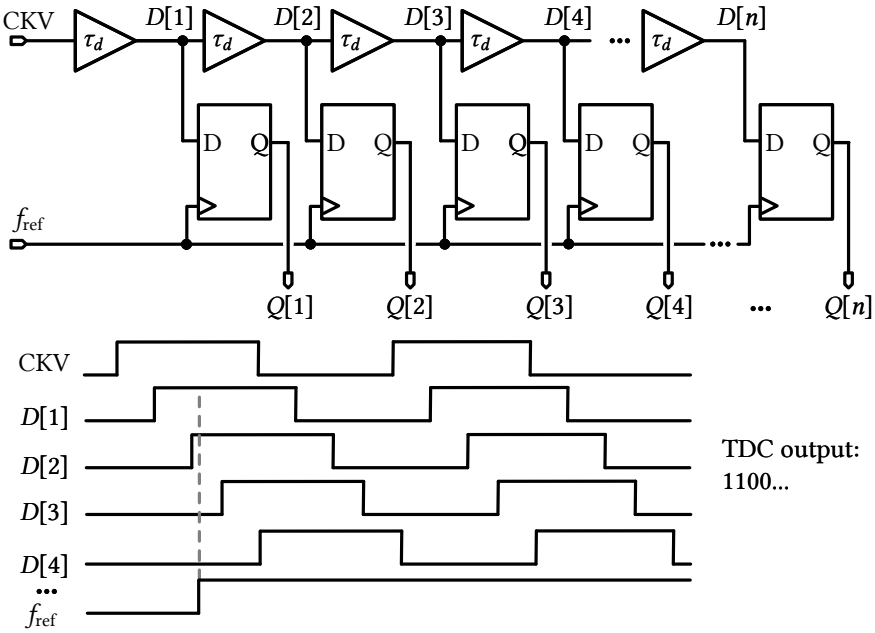


Figure 2.10: Schematic and functioning principle of the TDC.

2.3 Noise

A major performance metric of any RF systems is its noise performance. The signal-to-noise ratio (SNR) is often used to describe the quality of the signal. Due to the random nature of noise, its analysis commonly involves modeling using power spectral density (PSD).

In Fig. 2.12, the thermal noise model of a resistor is depicted. For a resistor with a value of R_0 and at an ambient temperature of T, the noise can be

[1]The system and digital design of the ADPLL was first undertaken by Jonas Meier and the design of the TDC was conducted by Tim Lauber. The author's contribution encompassed the design of XO, DCO and LDO as well as the physical implementation of the retiming circuitry.

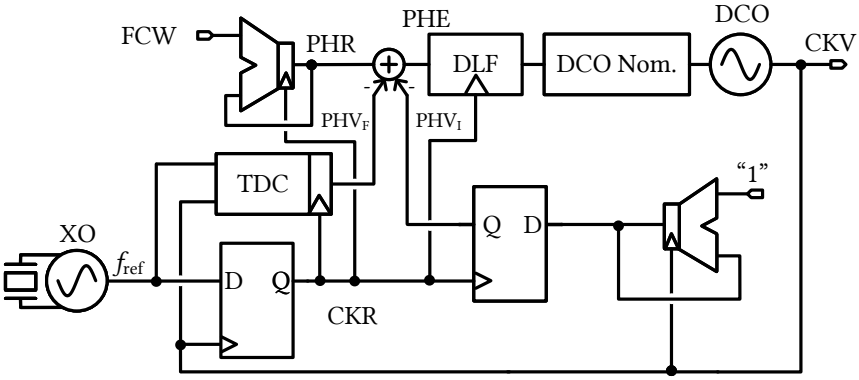


Figure 2.11: Block diagram of the ADPLL implemented in this thesis work.

represented by a voltage source, as shown in Fig. 2.12(a), with the PSD given by

$$\overline{v_n^2} = 4k_B T R_0 \tag{2.12}$$

Alternatively, the noise of a resistor can be modeled by a parallel-connected current source, as illustrated in Fig. 2.12(b). The PSD of the current source is expressed as

$$\overline{i_n^2} = \frac{4k_B T}{R_0} \tag{2.13}$$

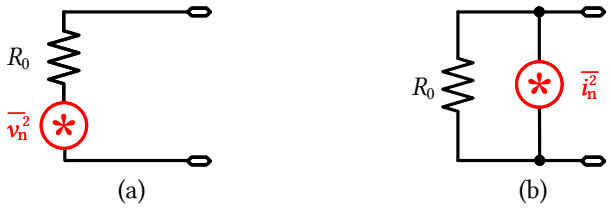


Figure 2.12: Resistor thermal noise modeled by (a) voltage source and (b) current source.

For a MOSFET in saturation, the channel exhibits the characteristic of a resistor, which also generates thermal noise [42]. The noise can be approximately modeled by a current source connected in parallel with the MOSFET

as shown in Fig. 2.13. The PSD of this current source is expressed by

$$\overline{i_n^2} = 4k_B T \gamma g_m \tag{2.14}$$

Here, γ represents the noise coefficient of the MOSFET, a parameter influenced by the process and channel length of the transistor, while g_m denotes the transconductance of the MOSFET in saturation. Determining the specific value of γ often requires experimental measurement [43]. For a long-channel device, γ is typically 2/3 [44, 45], with this value increasing as the channel length decreases. As an example, in a 40 nm CMOS technology, the value is 1 for a MOSFET with the minimum channel length [42].

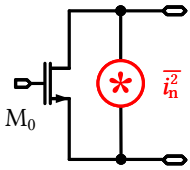


Figure 2.13: Thermal noise model of a MOSFET.

Another type of noise that is generated in MOSFET is the flicker noise. In contrast to thermal noise that is constant over the frequency or *white*, flicker noise exhibits frequency dependence. As the flicker noise's PSD is inversely proportional to frequency, it is also called $1/f$ noise or *pink* noise. The exact mechanism underlying flicker noise generation remains incompletely understood. A widely accepted hypothesis attributes this noise to the random fluctuations of electrons or holes in the channel [46], known as carrier number fluctuation (CNF). These fluctuations arise due to imperfections in the Si-SiO_2 lattice, causing random trapping and releasing of electrons or holes near the Si-SiO_2 interface in the MOSFET. Additionally, changes in charge within the channel can lead to variations in carrier mobility, a phenomenon known as carrier mobility fluctuation (CMF), which also contributes to noise and becomes more significant as technologies scale down [47]. The flicker can be modeled by a voltage source in series with the gate of the MOSFET, whose PSD is written as

$$\overline{v_n^2} = \frac{K}{WLC_{ox}} \frac{1}{f} \tag{2.15}$$

where K denotes a process-dependent constant, C_{ox} represents the capacitance per unit area of the gate oxide, and W and L are the width and length of the transistor, respectively. In CMOS technologies, PMOS transistors in general exhibit a smaller K than compared to NMOS transistors. The reason is that

holes generated in a p-type channel are typically further away from the Si-SiO_2 interface than electrons in an n-type channel [44]. As indicated in Eq. 2.15, increasing the area of the MOSFET proves to be an effective approach to reduce the transistor's flicker noise. The combination of thermal and flicker noise results in the noise profile depicted in Fig. 2.14. A corner frequency in the PSD of MOSFET noise indicates the frequency range where flicker noise predominates the overall noise characteristics of the MOSFET. In advanced CMOS technologies, this corner frequency is typically in the tens to hundreds of megahertz range [44]. Flicker noise from the MOSFET can be up-converted to the oscillator's carrier frequency, becoming one of the major contributors to noise in oscillators.

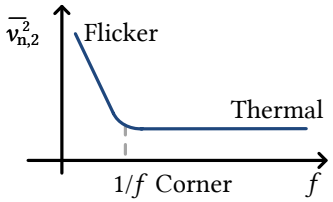


Figure 2.14: Noise profile of a MOSFET.

2.4 Phase Noise

An ideal LO output signal can be represented as

$$v_o(t) = V_{\text{peak}} \cdot \cos(2\pi f_0 t) \tag{2.16}$$

where V_{peak} is the amplitude of the LO signal and f_0 is the carrier frequency. The waveform and spectrum of an ideal LO is depicted in Fig. 2.15(a), where a single pulse at f_0 is present. However, due to the noise from the devices, the instantaneous phase of the LO is affected, as illustrated in the waveform of Fig .2.15 (b). The non-ideal LO output can thus be expressed by:

$$v_o(t) = V_{\text{peak}} \cdot \cos(2\pi f_0 t + \phi_n(t)) \tag{2.17}$$

where $\phi_n(t)$ is the denoted as *phase noise*. Fig .2.15 (b) also shows the spectrum of a noisy LO, where the frequency demonstrates a random fluctuation around f_0. The phase noise of the LO is normally quantified by integrating the power of 1 Hz bandwidth at a frequency Δf, departed from the carrier f_0. This value

is then normalized to the carrier power, resulting in a unit of dB referred to the carrier per hertz, or dBc/Hz as abbreviation.

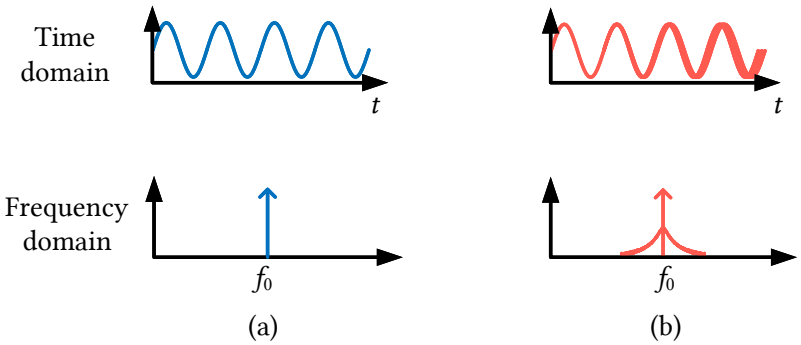


Figure 2.15: Waveform and spectrum of an (a) ideal and (b) realistic LO.

At the transmitter side, phase noise degrades signal quality, which can be quantified by error vector magnitude (EVM). The EVM can be approximately given by:

$$\text{EVM} \approx \sqrt{10^{\text{IQ}} + 10^{\text{LOFT}} + 10^{\text{PN}}} \tag{2.18}$$

where IQ represents I/Q mismatch, LOFT is LO feed-through, and PN denotes phase noise of the LO [42].

At the receiver side, phase noise significantly affects performance through reciprocal mixing, as illustrated in Fig. 2.16. This effect of reciprocal mixing occurs when a strong blocker exists in an adjacent channel, and due to the LO's phase noise, the blocker is down-converted into the signal band, degrading the SNR. The LO's phase noise requirement for the receiver is expressed as:

$$\mathcal{L}(\Delta f) = P_{\text{sig}}|_{\text{dB}} - SNR - P_{\text{B}}|_{\text{dB}} - 20\log(BW) \tag{2.19}$$

Thus, the phase noise of the LO is critical to the overall performance of RF systems. For a typical LO implemented by a PLL, the phase noise profile is shown in Figure 2.17. It has a skirt-like shape with three distinct regions. For offset frequencies lower than the loop bandwidth, the profile is flat, mainly determined by the noise of the reference frequency and PLL loop control units, such as the PFD and CP in an analog PLL, or the TDC in an ADPLL.

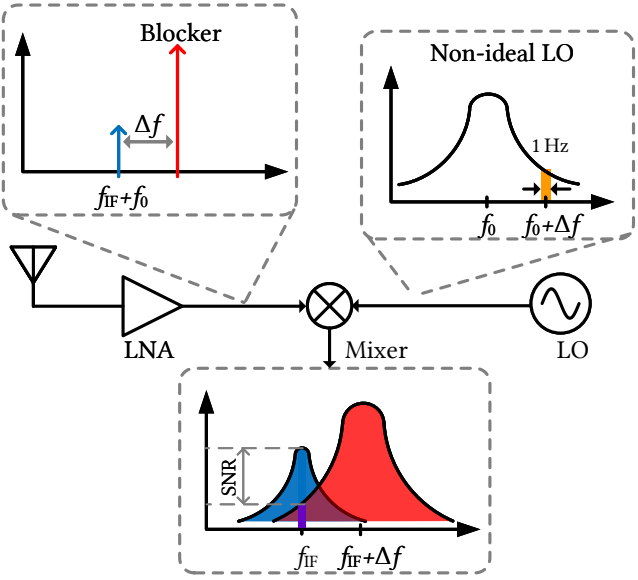


Figure 2.16: Influence of LO phase noise: reciprocal mixing.

Beyond this region, the profile exhibits a slope where the noise decreases by approximately 20 dB/dec. In advanced technologies with a higher flicker noise corner, a region with a slope decreasing by 30 dB/dec may also be observed. In this region, noise performance is primarily determined by the VCO or DCO. In the far-out region from the carrier frequency, the noise floor is set by the divider and buffer in the signal chain. Hence, optimizing the noise performance of frequency generation circuits, such as the crystal oscillator and DCO, is crucial.

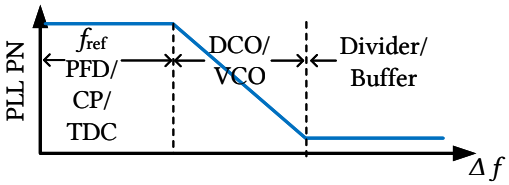


Figure 2.17: Noise profile of a PLL.

CHAPTER 3

LOW-NOISE DIGITALLY CONTROLLED LC OSCILLATORS

The strict performance requirements of the frequency synthesizer in a modern FMCW radar transceiver pose harsh challenges on design of low-noise oscillators. Among various oscillator architectures, LC oscillator have become the *sole* option of radio-frequency integrated circuit (RFIC) designers in many applications because it can achieve a much lower phase noise than other structures such as a ring oscillator, due to the higher frequency selectivity of an LC resonator. In addition, an LC oscillator can operate at a much higher frequency in comparison to e.g. a crystal oscillator, whose frequency is limited by the quartz resonate frequency.

However, LC oscillator also has its drawbacks. First, the integrated inductor occupies a very large area and thus increases the chip fabrication cost. Second, the magnetic coupling and radiation due to the inductor could decreases the noise performance [48] and hence special care has to be taken in isolation and decoupling. In addition, the integrated coil experiences a poorer quality compared to its off-chip counterpart due to the limited metal track width, especially in a nano-scale technology. As a result, LC oscillator designers must study the topologies of LC oscillators intensively to achieve a better phase noise performance [44].

With the trend into digital assisted RF circuits or all-digital RF circuits, such as all-digital phase-locked loop (ADPLL) thanks to the continuous scaling down of CMOS technology, a high-performance digitally-controlled oscillator (DCO) has become of more interest than ever. However, as the DCO utilize a fully discrete frequency tuning, it suffers from more quantization noise than its analog counterpart, i.e. a voltage controlled oscillator (VCO). An intuitive method to mitigate this is to increase the DCO tuning resolution, i.e. minimize the frequency tuning step. In the same time, the large tuning range of a DCO is also preferred due to the requirement on the wider bandwidth of fast chirp signal FMCW to increase the distance measurement resolution, as discussed in 2.1.1. Moreover, the transient behavior of a DCO can greatly

influence the lock time of a ADPLL. These requirements call for innovations in design of DCO.

Because of its the importance and design challenges, this chapter is devoted to study the different aspects and give practical design considerations on digitally controlled LC oscillators in an advanced CMOS technology. Two design examples with measurement results are also demonstrated.

3.1 Passive Devices

The integration of passive devices, e.g. inductor and transformer, is one of the main contributors to the success of modern RF integrated circuits, especially in CMOS technologies. For example, an RF amplifier can achieve a much higher gain at center frequency when using an inductive load stage without spending the supply voltage overhead, which is already very small in an ultra-scaled-down technology.

Despite the fact that on-chip passive devices exhibit worse characteristics than the off-chip ones, e.g. smaller quality factor of an inductor that could lead to a poorer phase noise of an LC oscillator, integrated passive devices have many advantages. First, to use an off-chip passive device, designers must take the parasitic inductance introduced by the long bond wire into consideration. A typical inductance value of a bond wire is in range of 1-2 nH, which is obviously too large for a RF circuit for radar applications that operate in giga-hertz. Second, it is difficult to achieve fully symmetrical structure due to the insufficient control on the bond wire inductance value. Last, the bond wires could have a very strong coupling with other part of the system, degrading the noise performance of the circuit of interest [44].

As integrated passive devices have a very large influence on the performance of LC oscillators, this section discuss the practical considerations on the basics, design and selection of these devices.

3.1.1 Inductor

Monolithic integrated inductors are commonly implemented by metal spiral coils. For the purpose of a high quality factor, the design of inductors typically use top thick metal due to its smaller resistivity. Fig. 3.1 illustrates the 3-D layout of a 1-turn O-shape spiral coil implemented using top thick metals.

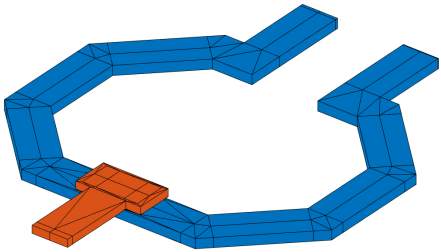


Figure 3.1: 3D illustration of an integrated differential center-tapped O-shape inductor.

Author in [49] gave a mathematical model that can be used to estimate the inductance of an on-chip spiral

$$L \approx 1.37 \times 10^{-7} \times \frac{l_{\text{tot}}^{5/4}}{\left(\frac{l_{\text{tot}}}{4N} + W + (N-1)(W+S)\right)^{1/3} W^{0.083}(W+S)^{0.25}} \tag{3.1}$$

where l_{tot} is the total length of the metal trace, N stands for the number of turns, W is the metal trace width and S is the spacing between trances. Fig. 3.2(a) gives a simple model for the integrated inductor. The series resistance is calculated by

$$R_{\text{s}} = R_{\square} \frac{l_{\text{tot}}}{W} \tag{3.2}$$

where $R_{\square}$ is the square resistance of the used metal and determined by the technology. The quality factor of the inductor can thus be expressed by

$$Q = \frac{\omega_0 L}{R_{\text{s}}} \tag{3.3}$$

The accuracy of the model presented in Eq. 3.1 for inductor characterization is reported to have an error ranging from 10% to 20% according to several references [48–50]. To improve upon this, researchers have explored more advanced inductor modeling techniques as documented in [50–53]. Nevertheless, during practical design processes, it is often necessary to employ specific electromagnetic solvers to accurately characterize integrated spiral inductors. In this thesis, the EMX from Cadence has been chosen for this purpose. Fig. 3.2(b) illustrates a more sophisticated lumped model obtained

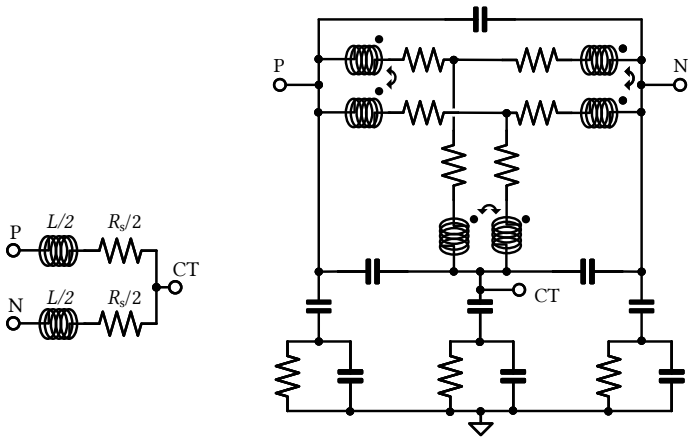


Figure 3.2: Model of a center-tapped inductor. (a) Simple model with series resistors. (b) Lumped model generated by Cadence EMX.

through EMX for a differential center-tapped coil, reflecting the enhanced accuracy achieved through this approach.

In modern transceivers, such as the FMCW radar transceiver depicted in Fig 2.4, it is often desirable to minimize the magnetic coupling between the LC oscillator and other circuits in order to mitigate the pulling effect, particularly from the strong PA. Although the PA operates at a much higher frequency than the oscillator, as shown in Fig. 2.7, the presence of strong harmonics can still negatively impact the performance of both the PA and the oscillator. To address this issue, a simple yet effective solution is to employ an 8-shaped coil, as illustrated in Fig. 3.3. The concept behind the 8-shaped coil is to utilize two symmetrical spirals in the inductor, which results in the cancellation of electromagnetic emissions. This configuration helps to reduce the unwanted magnetic coupling between the LC oscillator and other circuits.

However, when comparing the 8-shaped inductor to its O-shaped counterpart, it is observed that the 8-shaped inductor generally exhibits a relatively lower Q. This decrease in Q is a trade-off for achieving better isolation and reduced magnetic coupling between the LC oscillator and other circuits. In a study conducted by authors in [54], it was reported that the 8-shaped inductor had approximately 30% lower quality factor compared to the O-shaped induc-

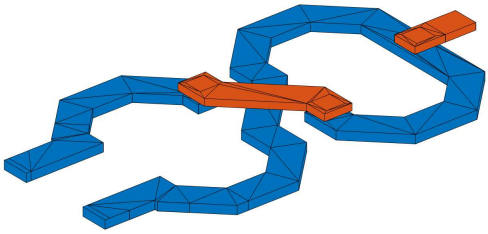


Figure 3.3: Layout of an 8-shape inductor.

tor. However, it is worth noting that in the 90 nm technology used in their research, the achieved Q value was still sufficiently large to not significantly limit the performance of the LC oscillator.

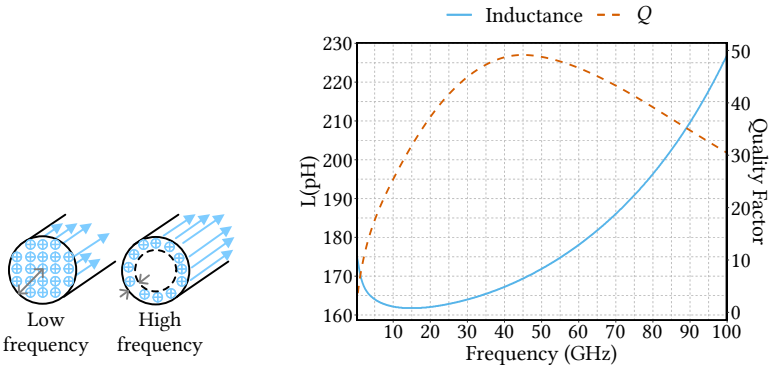


Figure 3.4: Illustration of (a) current distribution due to skin effect and (b) simulated O-shape coil inductance and quality across frequency in room temperature in a 28 nm CMOS using EMX.

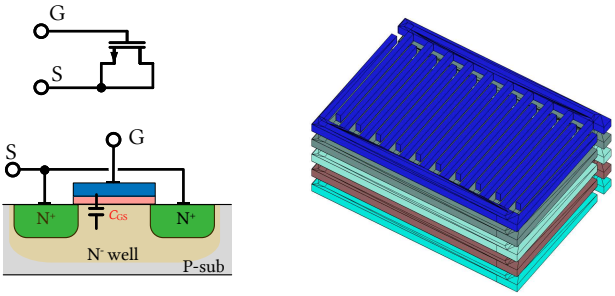
Another important aspect that designers need to account for is the impact of operating frequency on both inductance and quality factor. At very high frequencies, the phenomenon known as the *skin effect* becomes significant. The skin effect refers to the concentration of current towards the surface of the conductor when carrying high-frequency AC current, as depicted in Fig. 3.4(a). This occurrence leads to an effective increase in resistance, resulting in a lower quality factor for the inductor. To illustrate this effect, Fig. 3.4(b) presents the results of EM simulations showing the quality factor and

inductance of an O-shaped integrated inductor implemented using a 28 nm CMOS process at room temperature. The plot demonstrates that beyond a frequency of approximately 45 GHz, the quality factor of the inductor starts to decrease. This behavior is contrary to the linear dependence of the Q on the ω_0 as predicted by Eq. 3.3. This result further emphasizes the necessity of not having the LC oscillator operate at a very high frequency such as the radar band of 77 GHz, as discussed in 2.1.4, for optimal LC tank quality factor, which significantly impacts the phase noise performance.

An integrated inductor can also be used as a variable element to tune the frequency of an LC oscillator, e.g. in [55]. However, a variable inductor is normally associated with special fabrication technology such as micro-electro-mechanical systems (MEMS). As a result, the use of variable inductors is beyond the scope of this thesis.

3.1.2 Capacitor

The capacitor is a crucial component, fulfilling various essential functions in RFICs. Firstly, capacitors play an important role in adjusting the resonance of the LC circuit, enabling the oscillator's frequency tuning. Secondly, capacitors serve as efficient AC couplers, facilitating the interconnection of different RF blocks. Lastly, they can function as the decoupling capacitance between significant nets and ground [44].



(a) (b)

Figure 3.5: (a) Symbol and cross-section of a n-type MOS capacitor. (b) 3-D illustration of a fringe MOM capacitor.

Fig. 3.5 illustrates two commonly utilized capacitor types in CMOS technology. The n-type metal-oxide-semiconductor (MOS) capacitor, shown in

Fig. 3.5(a), consists of an NMOS transistor embedded within a lightly doped N-well. By applying a voltage higher than that of the source to the gate electrode, an electric field is generated, attracting electrons, and establishing a conducting channel beneath the oxide layer, thus forming a capacitor. The MOS capacitor exhibits the advantage of very high density, particularly in nano-scale technologies where the oxide thickness is significantly reduced. However, this capacitor type suffers from certain limitations, such as a relatively small quality factor due to the substantial resistance of the channel. Moreover, achieving large capacitance with MOS capacitors is associated with a considerable oxide area, leading to increased leakage current. These disadvantages make MOS capacitor unsuitable for LC tank or coupler between RF blocks. Nevertheless, these capacitors can serve effectively as decoupling capacitance for the power supply rail.

The fringe metal-oxide-metal (MOM) capacitor, as depicted in Fig. 3.5(b), typically consists of narrow metal lines with small gaps. This design aims to maximize the capacitance density by utilizing the available area efficiently. Similar to a metal-insulator-metal (MIM) capacitor, it employs metal layers as capacitor plates, with an oxide layer serving as the dielectric. However, unlike MIM capacitor, the fringe MOM capacitor does not require specialized fabrication technology, making it a more affordable and generally available option. The primary advantage of fringe MOM capacitors is their relatively high quality factor due to the low resistance of the metal traces compared to that of the channel. However, as all the metal traces are utilized to increase the capacitance, they obstruct routing possibilities for the entire area they occupy.

3.2 Phase Noise in LC Oscillator

3.2.1 Theoretical Analysis of Phase Noise - LTI Approach

The phase noise of an LC oscillator can be analyzed by a linear time-invariant (LTI) approach [56]. The transfer function of an LC oscillator under the assumption that the negative resistance introduced by the g_m stage cancels out the tank resistance R can be straightforward derived by

$$|H(j\omega)|^2 = \left| \frac{\omega L}{1 - \omega^2 LC} \right| \tag{3.4}$$

as also shown in Fig. 3.7.

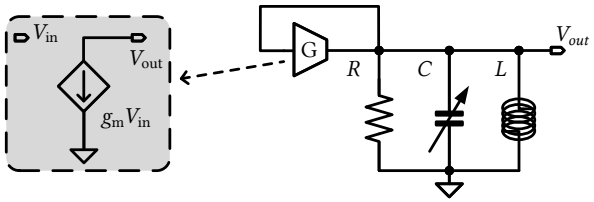


Figure 3.6: General model of an LC oscillator.

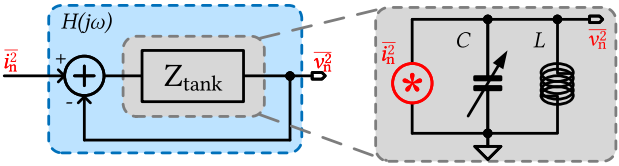


Figure 3.7: Transfer function of an LC oscillator for the noise current.

At the frequency of $\omega_0 \pm \Delta\omega$, where $\Delta\omega << \omega_0$, the expression of noise transfer function holds

$$\begin{aligned} |H(j(\omega_0 + \Delta\omega))|^2 &\approx \left| \frac{1}{2\Delta\omega C} \right|^2 \\ &= \left| \frac{\omega_0^2 L}{2\Delta\omega} \right|^2 = \frac{R^2}{4Q^2} \left(\frac{\omega_0}{\Delta\omega} \right)^2 \end{aligned} \tag{3.5}$$

where Q is the quality factor of the parallel RLC resonator and can be calculated by

$$Q = \frac{R}{L\omega_0} \tag{3.6}$$

The thermal noise current of R injected into the LC resonator can be expressed as follows:

$$\overline{i_n^2} = \frac{4k_B T}{R} \tag{3.7}$$

where k_B is the Boltzmann's constant and T is the temperature. The PSD of the noise voltage due to the injection of $\overline{i_n^2}$, at an offset frequency of $\Delta\omega$ from oscillator carrier frequency ω_0 can hence be written as

$$\overline{v_n^2} = \overline{i_n^2} \, |H(j(\omega_0 + \Delta\omega))|^2 \tag{3.8}$$

Assume that the noise current contributes equally into amplitude modulation (AM) and phase modulation (PM), i.e. 1/2 of the total noise current is up-converted into phase noise. The phase noise is defined as the single-sided band (SSB) voltage spectral density divided by the carrier power, it can be derived by

$$\mathcal{L}(\Delta\omega) = \frac{\overline{v_n^2}}{V_{peak}^2/4} \tag{3.9}$$

The phase noise of the oscillator can thus be predicted by the famous Leeson's equation [56]:

$$\mathcal{L}(\Delta\omega) \approx \frac{k_B T R}{Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 \cdot \frac{1}{V_{peak}^2} \tag{3.10}$$

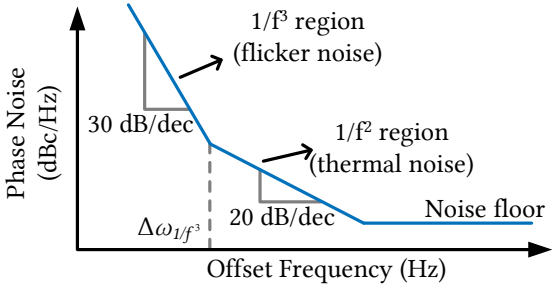


Figure 3.8: LC oscillator phase noise profile.

Leeson's equation successfully predicts that the phase noise of an LC oscillator drops by 20 dB/dec with the offset frequency $\Delta\omega$ under the circumstance that only thermal noise is considered. In the case that flicker noise, i.e. $1/f$ noise, is also taken into consideration, one can intuitively conclude that in a frequency range where flicker noise dominates, the phase noise of an LC oscillator falls by 30 dB/dec with $\Delta\omega$, based on the same LTI analysis. Eq. 3.10 can then empirically be adjusted as discussed in [57]

$$\mathcal{L}(\Delta\omega) \approx \frac{F k_B T R}{V_{peak}^2} \cdot \left(1 + \frac{\omega_0}{Q^2 \Delta\omega}\right)^2 \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{\Delta\omega}\right) \tag{3.11}$$

Fig. 3.8 depicts the LC oscillator phase noise. The introduced parameter

$\Delta\omega_{1/f^3}$ stands for the flicker noise corner, which represents the frequency up to which the phase noise decreases by 30 dB/dec with an offset frequency from the carrier. F is the noise factor of the g_m stage and was assumed to be 1, i.e. noiseless in the previous analysis.

The limitation of this analysis is that the parameter $\Delta\omega_{1/f^3}$ is purely empirical instead of from a rigorous calculation. In addition, the LTI approach is conducted under the assumption that noise of the tank contributes equally to AM and PM noises. Moreover, it fails to explain the noise up-conversion of active devices, which is simply expressed by a noise factor F. However, Leeson's equation still provides a good intuition to oscillator designers on how to optimize the phase noise performance of an oscillator, i.e. to maximize the tank Q as well as the oscillation amplitude.

3.2.2 LTV Approach for Phase Noise Calculation

In order to precisely compute the value of $\Delta\omega_{1/f^3}$, the authors in [58] introduced a methodology that considers the LC oscillator as a linear time-variant (LTV). Fig. 3.9 depicts an intuitive introduction of the idea of the LTV system into oscillator phase noise analysis. Suppose a current impulse is injected into the LC tank at the time Δt, it results in an instant voltage rise Δv across the tank.

Depending on the time when the injection happens in relation to the oscillation period, it causes different effect on the phase variation of the oscillation. In the situation that the current impulse is injection when the output voltage is at the maximum amplitude, the instant rise of voltage Δv causes no phase shift. On the other hand, if the current impulse is injected at the zero crossing, a maximum phase shift is generated as the oscillation stays as sinusoid. One can thus conclude that in terms of phase, the oscillator is a LTV system despite all the devices in the oscillator are time-invariant.

As the LC oscillator reacts differently to the noise current across the oscillation period T, authors in [58] introduces the impulse sensitivity function (ISF) $\Gamma(\omega_0 t)$ to describe this characteristic. $\Gamma(\omega_0 t)$ is normally normalized to be unit-less, independent of frequency and amplitude, and solely determined by the architecture of the oscillator. Moreover, $\Gamma(\omega_0 t)$ has a period of 2π and can thus be written in a Fourier series form as

$$\Gamma(\omega_0 t) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 t + \phi_n) \tag{3.12}$$

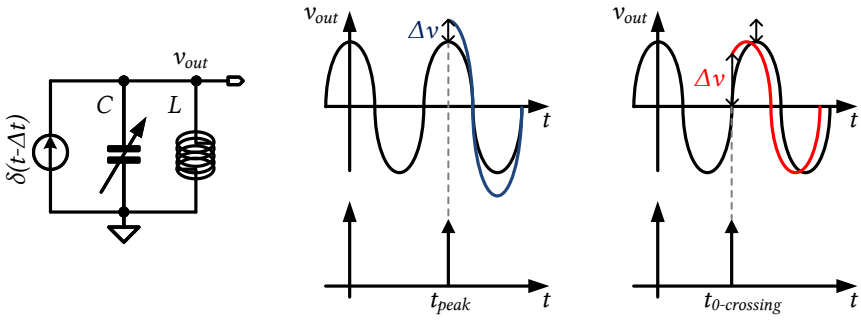


Figure 3.9: Illustration of LC oscillator as a LTV system in terms of phase [58].

For example, as analyzed for the case of Fig. 3.9, the ISF of an LC oscillator is the derivative of the output waveform, which can be expressed as

$$\Gamma(\omega_0 t) = -\sin(\omega_0 t) \tag{3.13}$$

The effective current noise contribution of the tank resistance into the phase noise is thus the product of its noise current and the Γ:

$$\overline{i^2_{\text{n,eff}}} = \overline{i^2_{\text{n}}} \times \Gamma^2_{\text{rms}}(\omega_0 t) \tag{3.14}$$

Where $\Gamma_{\text{rms}}(\omega_0 t)^2 = 1/2$. The phase noise due to the tank resistance can therefore be expressed as:

$$\begin{aligned} \mathcal{L}(\Delta\omega) &= \frac{\overline{i^2_{\text{n,eff}}} \times |H(j(\omega_0 + \Delta\omega))|^2}{V^2_{\text{peak}}/2} \\ &= \frac{\frac{1}{2}\overline{i^2_{\text{n}}} \times \Gamma^2_{\text{rms}}(\omega_0 t) \times \frac{R^2}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2}{V^2_{\text{peak}}/2} \end{aligned} \tag{3.15}$$

Substituting Eq. 3.7 into Eq. 3.15, we obtain

$$\mathcal{L}(\Delta\omega) = \frac{k_{\text{B}}TR}{Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 \cdot \frac{1}{V^2_{\text{peak}}} \tag{3.16}$$

which is the same conclusion with Leeson's equation, i.e. Eq. 3.10. But with this conduction, the assumption of equal contribution of tank loss into AM noise and PM noise is not necessary. Another important aspect of ISF is

the prediction of flicker noise up-conversion. Fig. 3.10 illustrates this in the frequency domain. The noise side band in the different harmonics of the oscillation frequency convolves the ISF. This results in the phase modulation profile of the carrier f_0 and eventually causes phase noise.

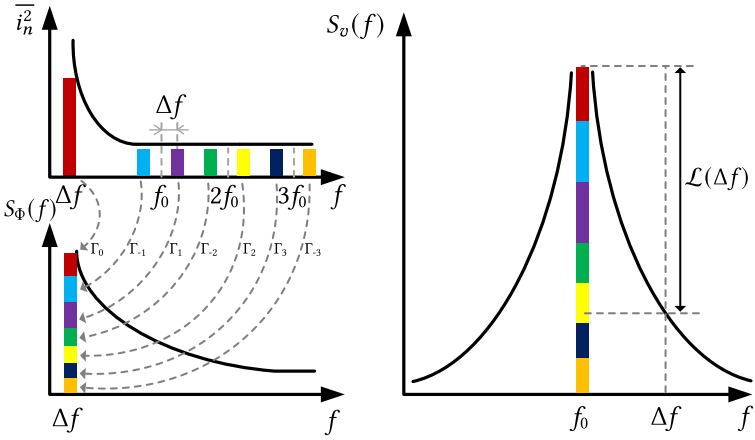


Figure 3.10: Noise up-conversion [57].

For the phase noise contribution from the active devices, authors in [59] utilizes the concept of LTV analysis to calculate it in a case of a cross-coupled class-B LC oscillator. The approach is very similar to that of the noise due to the tank loss. The noise current of the transistor is given by

$$\overline{i_{\mathrm{n}}^2} = 4k_B T\gamma_{\{\mathrm{n,p}\}} g_{\mathrm{m}}(\omega_0 t) \tag{3.17}$$

where $\gamma_{\{n,p\}}$ is the thermal noise excess factor of the n-type and p-type transistor, respectively, and g_{m} stands for the transconductance of the device. The noise of the active devices contributes to the phase noise only during the time when both transistors are conducting, because during the time when one branch is carrying all the tail current, its noise is overwhelmed by the ideal tail current source, and when the transistor is in cut-off, it generates no noise as g_{m} is zero. With this analysis, the phase noise induced by the active devices can be written as

$$\mathcal{L}_{g_{\mathrm{m}}}(\Delta\omega) = \frac{2k_{\mathrm{B}}TR}{Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 \cdot \frac{1+\gamma_{\{\mathrm{n,p}\}}}{V_{\mathrm{peak}}^2} \tag{3.18}$$

Interestingly, this conclusion states that g_m does not have effect on the phase noise. This is because when g_m is increased, although the noise generated by the active devices become larger, the current waveform also becomes steeper, making the time for both transistors are conducting smaller.

Taking this research a step further, a subsequent investigation in [60] employed a phasor-based analysis to provide a rigorous mathematical derivation of phase noise, thereby enhancing our understanding in this area.

3.2.3 Brief Summary of Flicker Noise Upconversion Mechanisms

There are three primary mechanisms, through which the flicker noise of active devices is up-converted into phase noise. Firstly, in LC oscillators with a significantly large amplitude for optimal phase noise performance, the parasitic capacitance of active devices, such as g_m stages and switches in the SC cell, exhibit varactor-like behavior. Since the oscillation amplitude is influenced by the tail current value, it becomes modulated by its 1/f noise. This mechanism, known as AM-to-PM conversion, has been studied in [61] and [62].

The second mechanism, known as the *Groszkowski effect* [63], describes the instantaneous phase fluctuations experienced by the oscillator due to flicker noise originating directly from the g_m stages or the tail current.

The last mechanism involves the up-conversion of 1/f noise to the second harmonic, $2\omega_0$, where its sidebands degrade the phase noise performance at ω_0 [64].

3.3 Structures of Oscillator Core

The need of mitigating the noise up-conversion mechanism have motivated researchers to explore various LC oscillator topologies. Selections of the device type and bias scheme affect the phase noise performance of an *LC* oscillator differently. These design details are discussed in the subsequent sections.

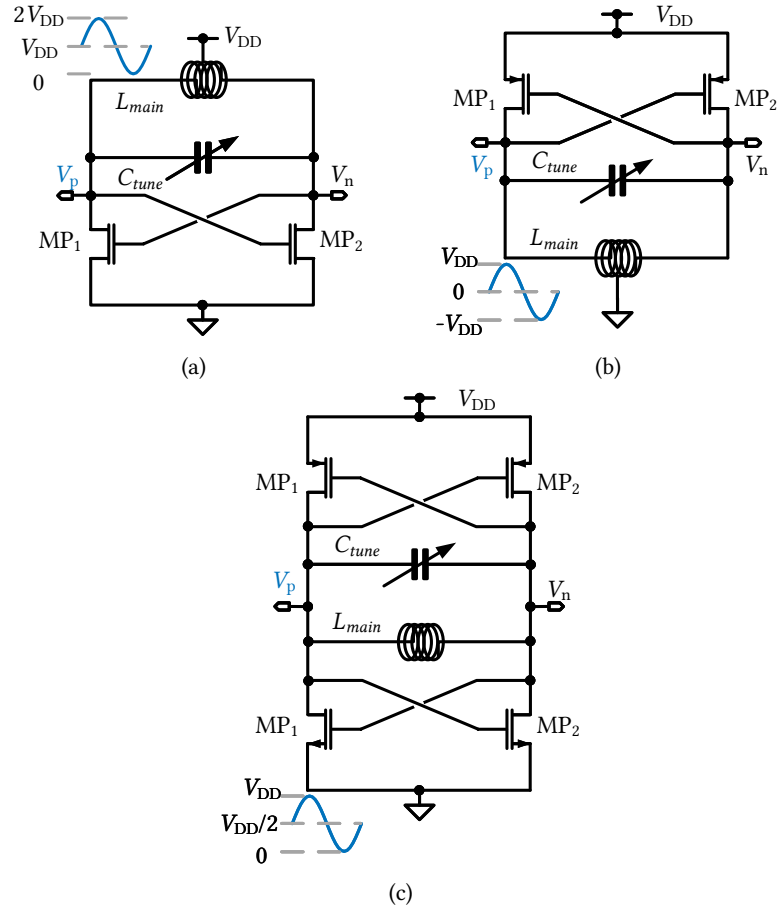


Figure 3.11: Structures of (a) NMOS-only, (b) PMOS-only and (c) CMOS LC oscillator core.

3.3.1 Selection of Active Device Type

The cross-coupled oscillator is the most classic and widely used LC oscillator. As depicted in Fig. 3.11, this type of oscillators feature a direct drain-gate cross-coupled differential MOS pair to generate the necessary negative resistance for sustaining oscillation. The differential configuration can be implemented using NMOS, PMOS, or a combination of both. Fig. 3.11(a) illustrates the schematic of an NMOS cross-coupled oscillator. The DC voltage at the drains of the g_m transistors is biased at V_{DD} through the center tap of the coil, allowing the oscillator to swing between ground and $2V_{DD}$. As the oscillator is symmetrical, the differential output exhibits a very large voltage swing of $2V_{DD}$. According to the calculation from Eq. 3.11, a large amplitude is favorable as it leads to good phase noise performance.

Fig. 3.11(b) illustrates the schematic of a cross-coupled oscillator using PMOS transistors, where the differential amplitude remains the same at $2V_{DD}$. Utilizing PMOS transistors offers the advantage of inherently reduced flicker noise contribution [65]. However, due to the lower carrier mobility in PMOS compared to NMOS, it may be necessary to increase the size of the g_m stage, thereby limiting the maximum oscillation frequency. Nevertheless, in advanced technology nodes, the carrier mobility gap between electrons and holes becomes almost negligible, making PMOS-based LC oscillators an increasingly attractive option for designers [66] [67].

Another alternative is to use a complementary structure, as depicted in Fig. 3.11(c). In this structure, the DC voltage of the LC tank is biased at $V_{DD}/2$. As a result, the single-ended output can swing between V_{DD} and ground. Therefore, the maximum differential amplitude of this structure is only V_{DD}, which is half of the NMOS-only or PMOS-only counterpart. Consequently, the minimum achievable phase noise performance is also limited. However, the advantage of this structure lies in its higher current efficiency. It can generate twice the g_m with the same tail current compared to the NMOS-only or PMOS-only counterpart, which is due to the doubled number of devices used in this configuration. Additionally, a relatively small swing in this structure can be more favorable for reliability considerations, especially in an advanced technology node featuring very thin gate oxide.

3.3.2 Selection of Tail Bias

Biasing the g_m devices within an LC oscillator accurately is crucial for optimizing phase noise performance and managing power consumption. In an

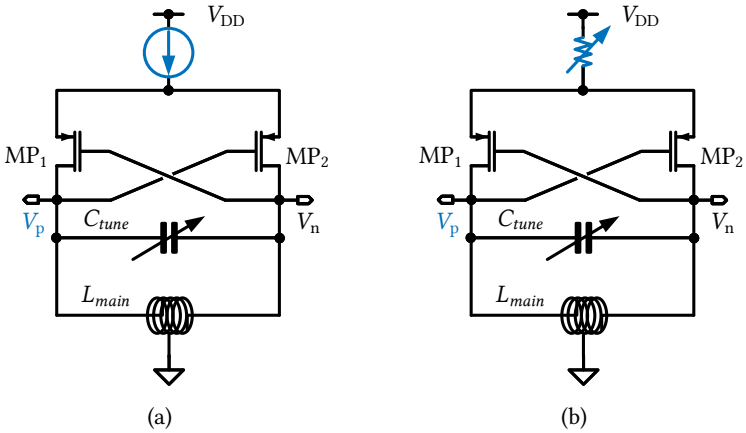


Figure 3.12: (a) Tail current source and (b) tail resistor biased LC oscillators.

ideal scenario, the g_m should compensate the losses in the resonator by providing just enough negative resistance for best current efficiency. However, in reality, designers must safeguard the oscillator's startup across various PVT conditions.

Introducing a tail bias circuit offers an additional degree of freedom in adjusting the g_m value. Fig. 3.12 shows two popular architectures for oscillator biasing. The utilization of a tail current source to bias the oscillator core, depicted in Fig. 3.12(a), is very widely used due to its robustness. This design minimizes power supply ripple and noise interference within the g_m devices due to the inherent characteristics of a current source. Consequently, this architecture often provides good power supply rejection (PSR). However, the current source itself becomes a primary source of flicker noise. It is hence necessary to size the transistor used as the current source very long, e.g. larger than 1 μm even in a 28 nm technology to reduce the flicker noise contribution. Correspondingly, the width of the transistor must be increased to prevent excessive V_{DS} drop, in order not to limit the oscillation amplitude. This need for larger transistors contributes to increased chip area usage. Additionally, the induced large parasitic capacitance at the common source of the g_m devices can push these transistors into the linear region, resulting in a degradation of phase noise performance. Furthermore, designing the bias current source for such noise-sensitive RF blocks necessitates the implementation of an aggressive low-pass filter, further increasing area occupation.

An alternative technique is the tail resistor bias method illustrated in Fig. 3.12(b), where a tunable resistor replaces the current source. This architecture simplifies biasing as it directly biases the g_m transistors by altering the common source voltage. Additionally, the passive poly-resistor used in this architecture does not generate $1/f$ noise, potentially benefiting the overall phase noise performance of the oscillator. However, as the resistor is typically designed to be relatively small, in the range of tens to hundreds of ohms, to avoid excessive voltage headroom occupation, this architecture experiences poor PSR. Consequently, a dedicated low-noise low-dropout regulator (LNLDO) becomes necessary. Moreover, the poly resistor in advanced technologies exhibits a wide spread across PVT, complicating the design. Additionally, in applications requiring precise control of oscillation amplitude, applying all-analog amplitude regulation for the resistor-biased oscillator is more challenging compared to its current-biased counterpart.

3.3.3 Class-B

The oscillator structures depicted in both Fig. 3.11 and Fig. 3.12 fall under the category of class-B oscillators. In these configurations, each branch within the cross-coupled pair conducts the entire tail current for half of the oscillation cycle, while the other branch remains in a cut-off state, resulting in a square-

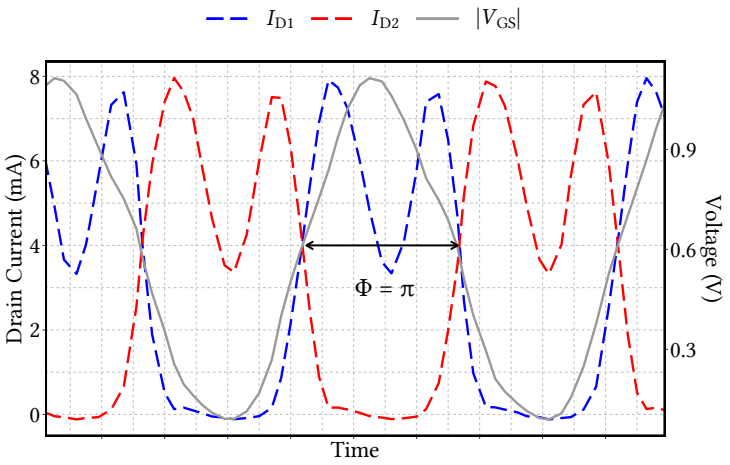


Figure 3.13: Simulated gate-source voltage and drain current of g_m devices in a class-B LC oscillator.

like current waveform. The class-B oscillator, owing to its simplicity and robustness, continues to be highly favored in modern designs.

However, a significant drawback of the class-B LC oscillator is the occurrence of deep-triode region operation of the g_m devices during each oscillation cycle. This happens because the devices alternately carry the tail current with a conducting angle ϕ of π, as depicted in Fig. 3.13. It can be seen from the V_{GS} waveform, at the second harmonic, which is the inherent common-mode oscillation, the g_m devices enter deep-triode region. This operation in the deep-triode region introduces leads to degradation in phase noise performance.

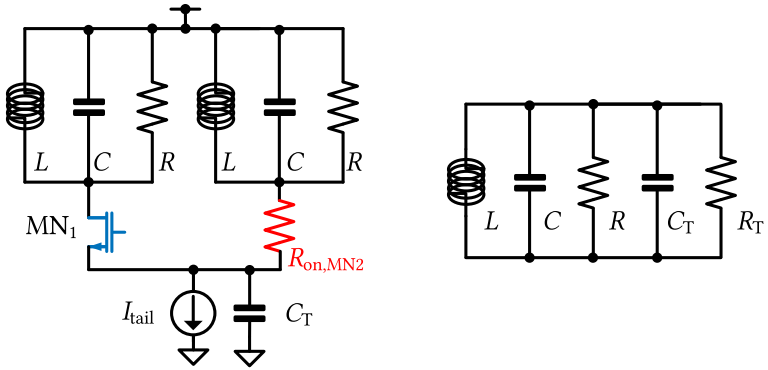


Figure 3.14: (a) Illustration of one g_m transistor entering deep-triode region and (b) the equivalent tank schematic [44].

Fig. 3.14(a) illustrates the scenario when MN_2 enters deep triode, where it is approximated by its on resistance R_{on}. The tank equivalent circuit, depicted in Fig. 3.14(b), presents the parallel equivalent of the RC network formed by R_{on} and C_T, denoted as R_T and C_T respectively. R_T can be expressed as follows:

$$R_T = \frac{1}{R_{on} C_T^2 \omega_0^2} \tag{3.19}$$

In situations where R_T is comparable to R, the operation of the g_m device in deep triode region significantly degrades the tank quality factor according to Eq. 3.6, consequently resulting in deteriorated phase noise performance [44].

As discussed in 3.2.3, the presence of noise at the second harmonic can also

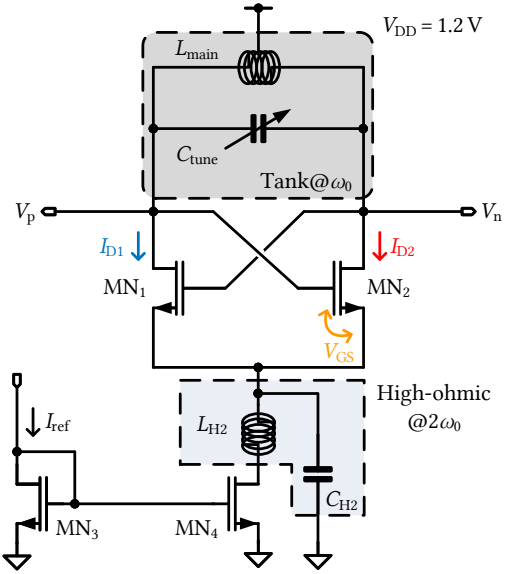


Figure 3.15: Structure of an NMOS class-B LC oscillator with second harmonic tail filter.

affect the phase noise performance of the LC oscillator. Another effect due to the second harmonic is that the common-mode oscillation at the common-source pushes the g_m into triode region because the V_{GS} of the transistors are becoming larger.

A straightforward yet effective solution to address these issues is to employ a tail filter, as illustrated in Fig. 3.15 [64]. The tail inductor L_{H2} is designed to resonate with C_{H2} at $2\omega_0$, effectively compensating for the impact of the second harmonic. The idea is to introduce an higher impedance, rising the common-source voltage at the second harmonic. The g_m devices can thus stay in saturation. However, this configuration has its drawbacks. First and obviously, the additional coil occupies a significant chip area. In the case of using a complementary g_m devices architecture shown in Fig. 3.11(c), two more coils are needed for this technique to be effective, which greatly increases the chip manufacturing cost. Moreover, the configuration is inherently narrowband because it is only effective if the second tank resonates precisely at the second harmonic. One solution for this difficulty is to make the tail filter also tunable, which greatly increases the design complexity on control, routing and calibration, e.g. in [68]. A feasible compromise is to intentionally reduce

the quality factor of the tail filter, making it slightly more wide-band [16].

3.3.4 Class-C

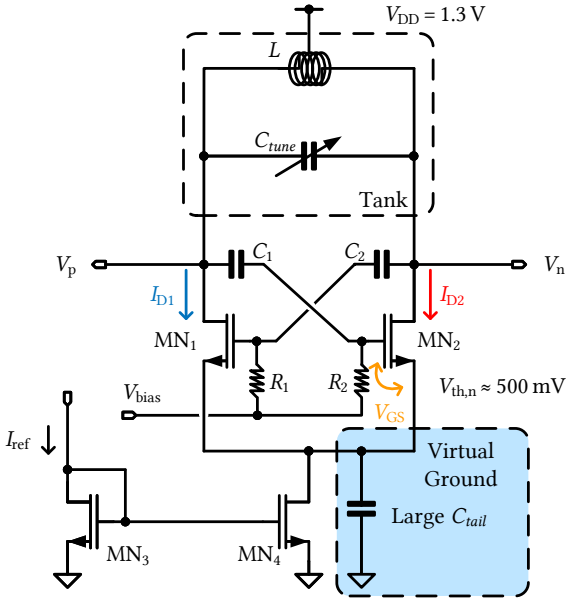


Figure 3.16: Schematic of an RC-biased NMOS class-C LC oscillator.

Introduced first by Mazzanti and Andreani in [69], the class-C oscillator aims to solve the drawbacks of the class-B oscillator discussed in 3.3.3. The idea of the class-C oscillator is to shape the current waveform of the g_m devices into a pulse-like form by deliberately attaching a large C_{tail} onto the common source of the g_m transistors, such that the time when both branches are carry the tail current is reduced. As mentioned in 3.2.2, the noise of the active devices is only up-converted into phase noise during this time. As a result, the phase noise performance of the oscillator can be improved.

In order to prevent the g_m devices from entering linear region to avoid phase noise degradation, as discussed in 3.3.3, class-C oscillator features a AC-coupled feedback. Fig. 3.16 illustrates the schematic of a class-C oscillator biased by a RC network. Coupling capacitors C_1 and C_2 are introduced to provide the feedback path. On the other hand, the DC level of the gates of

g_m stage is set actively to V_{bias} through R_1 and R_2. The bias voltage V_{bias} needs to be large enough so that MN_1 and MN_2 are able to provide enough negative resistance for sustaining the oscillation. The selection of V_{bias} should also consider its role in preventing MN_1 and MN_2 from entering deep-triode operation. Typically, a value around the threshold voltage of the transistors is chosen for V_{bias} to ensure this requirement is met. Fig. 3.17 depicts the simulated waveform of the drain current and the gate-source voltage of the g_m devices. The plot reveals that the conducting angle Φ of the class-C oscillator is reduced to $\frac{2\pi}{3}$, resulting in a distinct pulse-like waveform for the drain current.

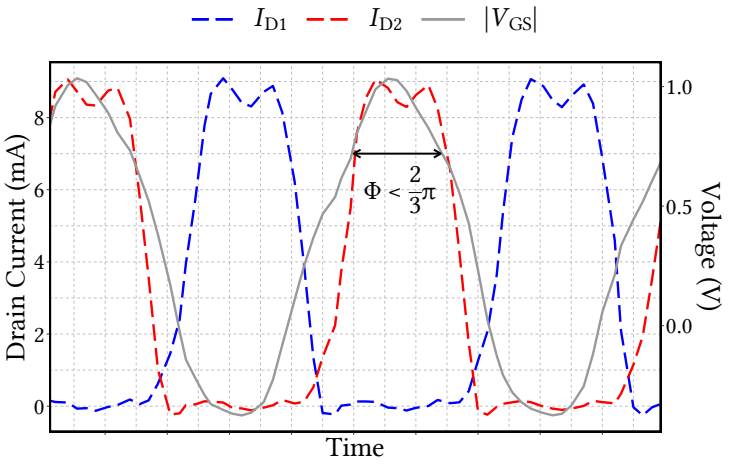


Figure 3.17: Simulated gate-source voltage and drain current of g_m devices in a class-C LC oscillator.

The class-C oscillator offers a notable advantage by enabling the DC operating point of the g_m stage to be finely adjusted close to the threshold voltage. This adjustment allows for optimal allocation of the supply headroom to enhance the oscillation amplitude while ensuring that the active devices remain in saturation. Consequently, this configuration yields a significantly high current efficiency, resulting in an impressive FoM. However, the setup with a low gate DC voltage in the class-C oscillator poses challenges during startup. To address this issue, a regulation loop becomes essential to manage the gate bias. This regulation needs to ensure a higher gate voltage and gradually reduces it to approximately V_{TH}.

Researchers in [70] have proposed a regulation approach based on the

oscillation amplitude. This method allows the oscillator to operate initially in class-A before transitioning into class-C, effectively managing the startup challenges. Alternatively, another strategy to overcome these difficulties involves utilizing a hybrid structure that combines class-B and class-C operation, as proposed in [71].

3.3.5 Class-D

In low-power applications such as Zigbee or Bluetooth, minimizing the power consumption of the LC oscillator is crucial since it typically represents the most power-intensive component in a wireless system. While a class-C oscillator offers higher current efficiency compared to its class-B counterpart, maintaining satisfactory phase noise performance still demands a relatively high V_{DD}. This voltage requirement is not advantageous for low-power applications. In pursuit of further reducing power consumption, researchers introduced the class-D oscillator. This concept was introduced in studies such as [72] and [73], proposing a schematic illustrated in Fig. 3.18.

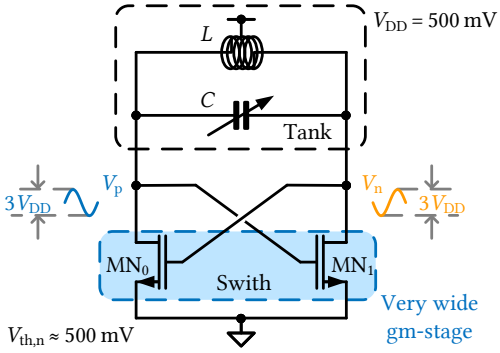


Figure 3.18: Schematic of an NMOS class-D LC oscillator.

At first glance, the class-D oscillator appears to share the same fundamental architecture as the class-B oscillator, with the omission of the tail biasing block. However, the significant distinction lies in the sizing of the g_m devices with very large W/L ratios, causing them to function purely as switches. This design approach aims to ensure that these devices behave like near-ideal switches, minimizing the voltage across the drain and source when they are in the on state.

Theoretically, in the class-D oscillator, when one branch of the oscillator is carrying current, but the transistor has minimal voltage across its terminals due to its switch-like behavior, the majority of the power contribution comes from the *LC* tank itself. This characteristic results in a very high power efficiency. For low-power applications, this becomes particularly advantageous, as the V_{DD} can potentially be as low as the threshold voltage of the g_m devices, significantly reducing power consumption while maintaining operational functionality.

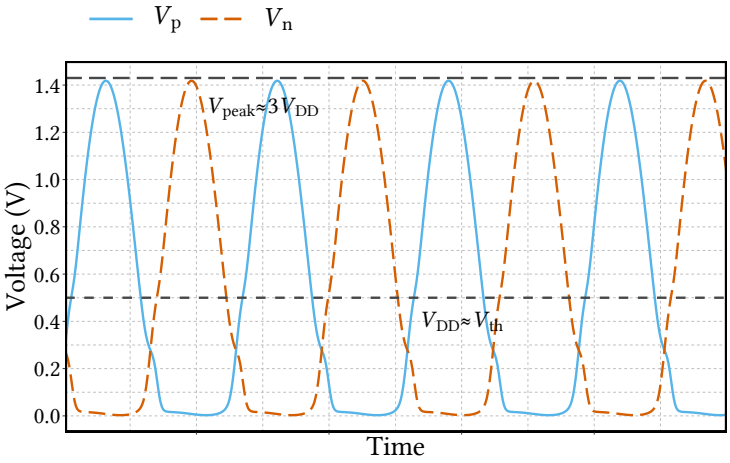


Figure 3.19: Simulated output voltage of a class-D LC oscillator.

Fig. 3.19 depicts the simulated output voltage waveform of a class-D oscillator. As can be seen, the class-D oscillator is able to provide a oscillation amplitude as $3 \times V_{DD}$, with the V_{DD} close to V_{th}. The class-D oscillator is reported to have very low power consumption, e.g. 0.171 mW in [73] with a 225 mV V_{DD} while maintaining a FoM lower than −190 dBc/Hz. However, the PSR of the class-D architecture is apparently low and it is thus necessary to design a low-noise low-dropout regulator (LNLDO). In addition, the start-up condition of the class-D oscillator is also stricter than that of the class-B oscillator.

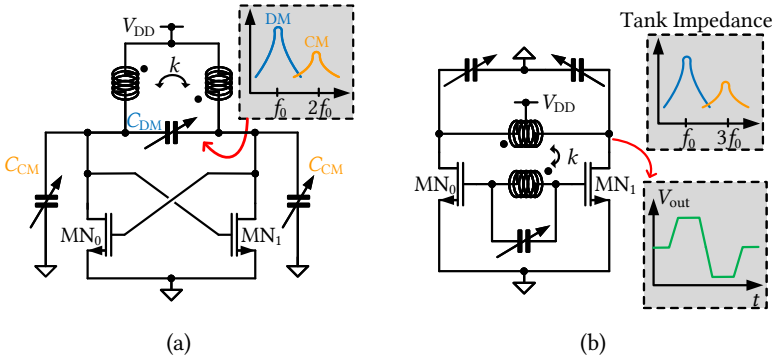


Figure 3.20: Examples of transformer-based LC oscillators. (a) Implicit common-mode resonator [74] and (b) class-F VCO [75].

3.3.6 Transformer-based LC Oscillator

While class-C and class-D oscillators are very attractive, particularly in low-power applications, their phase noise performance and FoM do not surpass those of the class-B oscillator featuring a second harmonic tail filter as shown in Fig. 3.15. However, this class-B architecture suffers from a notable drawback of an extensive footprint due to the inclusion of the second harmonic filter.

Recently, researchers have introduced the utilization of a transformer within an LC oscillator. This approach enables the design of the differential-mode resonant frequency and the common-mode resonant frequency aimed at distinct frequencies using a sole transformer. Consequently, it becomes feasible to attain optimal phase noise performance for the class-B oscillator without the need for a bulky second coil, as demonstrated in works such as [74] and [76]. This pioneering concept, known as the implicit common-mode resonator technique as illustrated in Fig. 3.20(a), employs common-mode tunable capacitors C_{CM} to adjust the common-mode resonant frequency to align with the second harmonic. The design reported in [74], achieved the best FoM among LC oscillators in a 28 nm process.

In another line of innovation, the class-F oscillator as depicted in Fig. 3.20(b), reported in [75] and [39], employs a similar methodology. It enhances the tank impedance at the third harmonic, resulting in an output voltage exhibiting a square-like waveform rather than a sinusoid. This modification yields a steeper zero-crossing in the voltage output, consequently improving phase noise performance. Nevertheless, these topologies require manual

tuning of the common-mode resonant frequency and may potentially restrict the highest attainable operating frequency due to the common-mode capacitors.

Class-C oscillator can also employ a transformer e.g. in [77], where it is used to replace the *RC* feedback network. The advantage of utilizing such combination is that transformer provides several degrees of freedom, such as the coupling coefficient k, and the possibility to tap the DCO output at the gate of the g_m devices to obtain a large signal power.

3.3.7 Multi-Core LC Oscillator

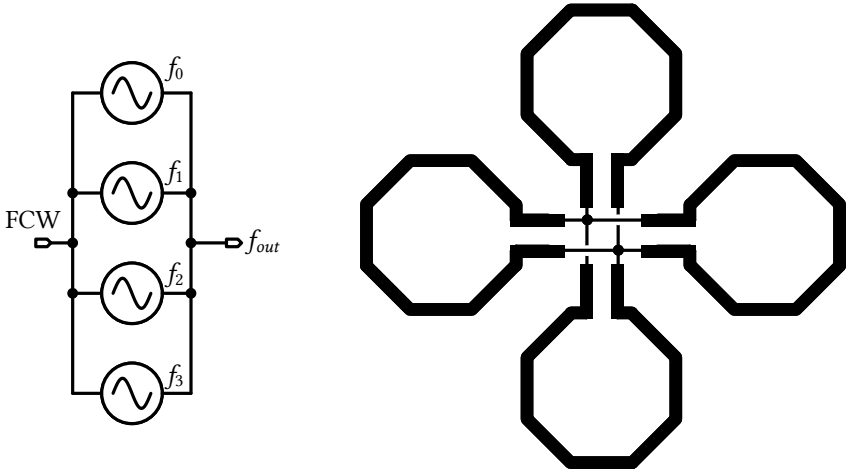


Figure 3.21: (a) Block diagram and (b) simplified layout floor-plan of a quad-core LC oscillator.

The heightened demand for stringent phase noise specifications in LC oscillators necessitates innovative architectural improvements. However, inherent physical limitations within CMOS technology must be acknowledged, as elucidated by Leeson's equation (Eq. 3.10):

$$\mathcal{L}(\Delta\omega) = \frac{k_B T R}{Q^2} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 \cdot \frac{1}{V_{\text{peak}}^2}$$

By substituting the value of the parallel equivalent tank resistor R with $R = \omega_0 LQ$ in Leeson's equation, it can be reformulated as:

$$\mathcal{L}(\Delta\omega) = \frac{k_B T}{Q} \cdot \left(\frac{\omega_0^3}{\Delta\omega^2}\right) \cdot \frac{L}{V_{\text{peak}}^2} \tag{3.20}$$

The implication of Eq. 3.20 is that, for a given oscillation frequency, minimizing the inductance L of the tank at a specific Q and oscillation amplitude is necessary to achieve minimal phase noise. However, practical implementation presents challenges because reducing inductance involves decreasing the inner diameter of the spiral, amplifying magnetic coupling between inner edges and subsequently deteriorating the coil's Q [78].

An alternative approach to enhance phase noise performance involves increasing oscillation amplitude, at the cost of higher power consumption. Nevertheless, in smaller technology nodes, transistor gate-oxide thinness restricts their ability to withstand high voltage stress. Thus, employing a large oscillation amplitude poses reliability challenges. Consequently, the recent shift towards employing a multi-core oscillator has become more appealing. This concept involves coupling N uncorrelated LC oscillator cores to achieve a $10\log(N)$ improvement in phase noise performance. For instance, Fig. 3.21(a) illustrates a quad-core VCO with four cores arranged in a star-like configuration [79]. However, this technique has obvious disadvantages, notably consuming N times more power and area.

3.4 Switchable Capacitors for DCO

One of the most crucial components that influences the overall performance of a DCO is the digitally controlled varactor or switchable capacitor (SC) array, which is responsible for frequency tuning. As the distance measure resolution is limited by the chirp signal bandwidth B as discussed in 2.1.1, which corresponds to the overall tuning range of the oscillator, the SC array is preferred to have a large overall capacitance difference between on and off states. At the same time, a very fine tuning step of the SC needs to be ensured to fulfill the demand of channel selection ability and minimal quantization noise. Furthermore, the SC bank must have sufficient quality factor such that it does not become the bottleneck for the LC oscillator phase noise performance.

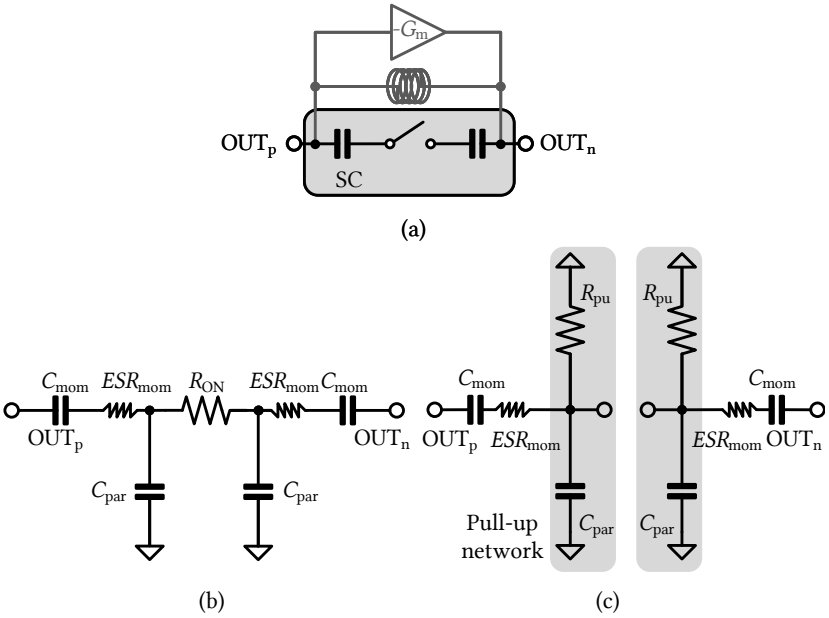


Figure 3.22: Equivalent circuits of (a) a general LC oscillator, and the switchable capacitor in (a) on state and (b) off state.

Fig. 3.22(a) illustrates the equivalent circuits of a general LC oscillator, featuring the use of a SC for frequency tuning. In the on state of the SC, as depicted in Fig. 3.22(b), C_{mom} represents the capacitance of the fringe capacitor, while ESR_{mom} denotes its equivalent series resistance. Additionally, R_{on} represents the on-resistance of the switch, and C_{par} symbolizes the parasitic capacitance introduced by the switch, interconnects, and other biasing circuitries. Conversely, in the off state, shown in Fig. 3.22 (c), the presence of R_{pu} introduces resistance caused by the biasing circuits. In the following analysis, R_{pu} is neglected in the on state since R_{on} is typically much smaller than R_{pu}.

In the on state, the signal path within a differential LC oscillator employing this SC is as follows: It originates from OUT_p, passes through the fringe capacitor on the left side, continues through the NMOS switch R_{on}, proceeds through the fringe capacitor on the right side, and finally reaches OUT_n. Consequently, the equivalent capacitance between OUT_p and OUT_n can be

expressed as:

$$C_{on} = \frac{C_{mom}}{2} \tag{3.21}$$

and the quality factor of the SC in the on state is:

$$Q_{on} = \frac{1}{\omega_0 (R_{on} + 2ESR_{mom}) C_{on}} \tag{3.22}$$

It is obvious that in order to have a larger quality factor at the on state of the SC, the R_{on} needs to be minimized.

Conversely, in the off state, as depicted in Fig. 3.22(c), the capacitive signal path of the SC within a differential LC oscillator follows the route from OUT_P, traversing the left fringe capacitor C_{mom}, the left parasitic capacitor C_{par} towards the ground, then continuing to the parasitic capacitor C_{par} on the right side, the right fringe capacitor C_{mom}, and ultimately reaching OUT_n. Consequently, the equivalent capacitance between OUT_P and OUT_n can be mathematically expressed as:

$$C_{off} = \frac{C_{mom} C_{par}}{2(C_{mom} + C_{par})} \tag{3.23}$$

To understand the quality factor of the SC in the off state, one can regard the SC as a circuit that connects a fringe capacitor and a biasing network in series, whereas the biasing network is a parallel connected RC circuit, with the quality factor expressed as:

$$Q_{pu} = \omega_0 \times R_{pu} \times C_{par} \tag{3.24}$$

As the equivalent circuit is symmetrical, one can look at the half circuit. The parallel RC network can be converted to a series-equivalent RC network. The series-equivalent capacitance $C_{S_{par}}$ and resistance $R_{S_{pu}}$ can be expressed as:

$$\begin{aligned} C_{S_{par}} &= C_{par} \left. \frac{1 + Q_{pu}^2}{Q_{pu}^2} \right|_{Q_{pu}^2 >> 1} \\ &\approx C_{par} \end{aligned} \tag{3.25}$$

and

$$\begin{aligned} R_{S_{pu}} &= R_{pu} \left. \frac{1}{1+Q_{pu}^2} \right|_{Q_{pu}^2>>1} \\ &\approx R_{pu} \frac{1}{Q_{pu}^2} \end{aligned} \tag{3.26}$$

The overall quality factor of the SC can be calculated by the ratio of the reactance $X_{C_{tot}}$ and the resistance R_{tot} of the capacitor. In the off state, it Q_{off} can thus be expressed by:

$$\begin{aligned} Q_{off} &= \frac{X_{C_{tot}}}{R_{tot}} \\ &= \frac{\frac{C_{mom}C_{par}}{\omega_0(C_{mom}+C_{par})}}{ESR_{mom} + \frac{R_{pu}}{Q_{pu}^2}} \end{aligned} \tag{3.27}$$

Substituting Eq. 3.24 into Eq. 3.27, it follows for the off-state quality factor:

$$Q_{off} = \frac{C_{mom}C_{par}}{\omega_0(C_{mom}+C_{par})} \cdot \frac{1}{ESR_{mom} + \frac{1}{\omega_0^2 C_{par}^2 R_{pu}}} \tag{3.28}$$

Eq. 3.28 indicates that in the off state of a SC, a higher R_{pu} value leads to a larger quality factor, which aids in the phase noise performance of the DCO.

For the capacitance difference between on and off state of the SC cell holds:

$$\begin{aligned} \Delta C &= C_{on} - C_{off} \\ &= \frac{C_{mom}^2}{2C_{mom} + C_{par}} \end{aligned} \tag{3.29}$$

Also, the frequency of a LC oscillator is determined by the resonate frequency of the LC tank:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \tag{3.30}$$

Here, L represents the inductance and C indicates the capacitance value of the tank. To obtain the tuning resolution at a specific frequency f_0, one can calculate the first-order derivative of the capacitance with respect to the

tuning parameter as

$$\left.\frac{df_{\text{osc}}}{dC}\right|_{f_{\text{osc}}=f_0} = -\frac{2\pi\sqrt{L}\cdot\frac{1}{2\sqrt{C}}}{4\pi^2LC} = -\frac{f_0}{2\pi C} \tag{3.31}$$

By substituting capacitance with $C = \frac{1}{4\pi^2 L f_0^2}$, Eq. (3.31) can be expressed as

$$df_{\text{osc}} = -2\pi^2 f_0^3 L dC \tag{3.32}$$

The analysis suggests that achieving a high-performance differential SC with substantial ΔC and quality factor is crucial to avoid limiting the highest oscillation frequency and phase noise performance of an LC oscillator. This can be achieved by maximizing the biasing resistance in the off state while minimizing both the parasitic capacitance (C_{par}) and the on-resistance of the SC.

Furthermore, as per Eq. 3.32, it is evident that an increase in the oscillation frequency f_0 leads to a cubic increase in the frequency tuning step of a DCO for a given ΔC. This behavior poses a substantial challenge in designing a fine-tuning bank at the frequency of interest of around 10 GHz. For example, aiming for a frequency resolution of 10 kHz at 10 GHz, considering an inductance of 200 pH, the required change in capacitance is merely 2.5 aF. Such a small change in capacitance approaches the fundamental limitations imposed by the capabilities of a CMOS lithography process.

In the subsequent sections, the characterization setup of the SC using large signal simulation is introduced, followed by an analysis of two conventional SC architectures. Subsequently, an innovative constantly-conducting NMOS (CCNMOS) SC architecture is proposed to alleviate the limitations associated with the conventional designs and address the challenge of designing fine-tuning bank.

SC Characterization Setup

Traditionally, a small-signal AC simulation is commonly used to estimate the ΔC and quality factor of a SC. However, this approach is not accurate for designing LC oscillators, particularly when the SC unit experiences a significant voltage amplitude on its electrodes. In such cases, the voltage

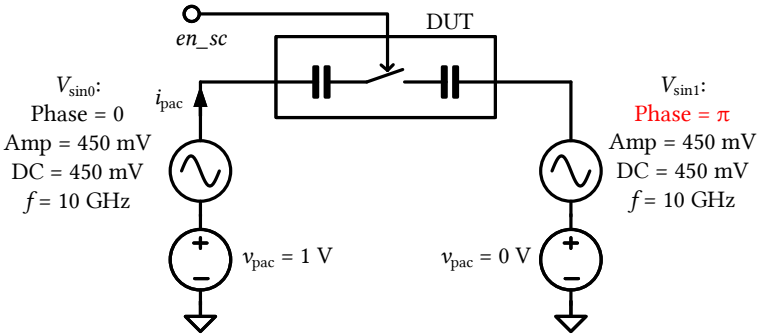


Figure 3.23: Testbench of the switchable capacitor unit cell.

range represents a large-signal operation, and the parasitic capacitance in the SC is influenced by the applied voltage, rendering the small-signal AC simulation inadequate for accurate characterization.

To achieve a more accurate characterization of the switchable capacitor cell in the DCO operation, a dedicated testbench was developed, as depicted in Fig. 3.23 [21]. This testbench involves the application of two sinusoidal voltage sources with a phase difference of π and a voltage swing ranging from 0 to V_{DD} to the differential outputs of the capacitor cell. This setup emulates the steady-state operation of the DCO. Additionally, a periodic AC (PAC) voltage signal of 1 V is introduced. By monitoring the PAC current i_{pac} flowing through the cell, it becomes possible to calculate both the quality factor and the capacitance of the cell using the following relationship:

$$Q = \frac{\mathrm{Im}(i_{pac})}{\mathrm{Re}(i_{pac})} \tag{3.33}$$

$$C_{pac} = \frac{1}{2\pi \times f_0} \times \mathrm{Im}\left(\frac{v_{pac}}{i_{pac}}\right) \tag{3.34}$$

where v_{pac} is 1 V in this setup. Utilizing this characterization setup allows for the consideration of various effects, including instances such as accidental switch-on behavior occurring during the off state of the SC, as well as the variations observed in C_{off} due to the amplitude. This is particularly significant as large signal simulation provides an average quality factor over the oscillation period, enabling a comprehensive evaluation of the system's behavior and performance under more realistic operating conditions.

3.4.1 Resistor-biased SC

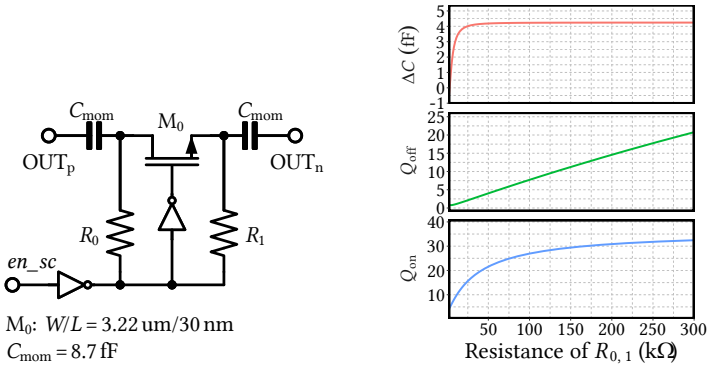


Figure 3.24: (a) The schematic and (b) the simulated ΔC and quality factor of resistor-biased SC over the resistance.

The schematic of a state-of-the-art resistor-biased SC used for the differential *LC* DCO is depicted in Fig. 3.24(a). Furthermore, Fig. 3.24(b) illustrates the simulated values of ΔC and the off-state quality factor as a function of the resistance value. These results were obtained through large-signal simulations using PSS and PAC techniques introduced in 3.4, with a frequency of 10 GHz selected for the analysis. The switch is implemented using an NMOS transistor M_0 with a (W/L) ratio of 4.6 μm/30 nm. The drain and source of M_0 are biased by poly-resistors R_0 and R_1. Additionally, the fringe capacitor C_{mom} has a value of 8.7 fF.

In order to achieve a better Q_{on}, as indicated by Eq. 3.22, it is desirable to have a smaller R_{on}. This can be accomplished by ensuring a large V_{GS} for M_0. Consequently, in the on state, the gate of M_0 is set to V_{DD}, while the drain and source are pulled to V_{SS}. On the other hand, in the off state of the SC, when the gate of M_0 is set to V_{SS}, it is advantageous to pull the drain and source of M_0 to V_{DD}. This serves two purposes: reducing the parasitic depletion capacitance, and consequently C_{off}, and preventing any undesired switched-on behavior of M_0 caused by the large oscillation amplitude.

Eq. 3.28 demonstrates that a higher value of R_{pu} results in a larger off-state quality factor of the SC cell. To ensure an adequate quality factor, the resistors R_0 and R_1 are typically chosen in a range of tens to hundreds of kilo-ohms,

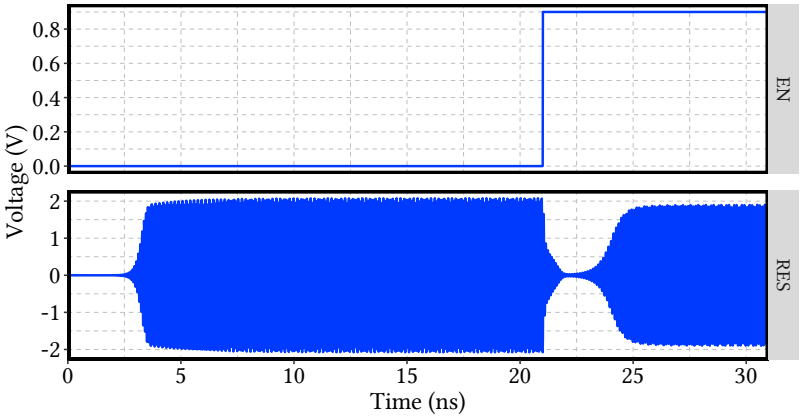


Figure 3.25: Simulated oscillator transient response using resistor biased SC.

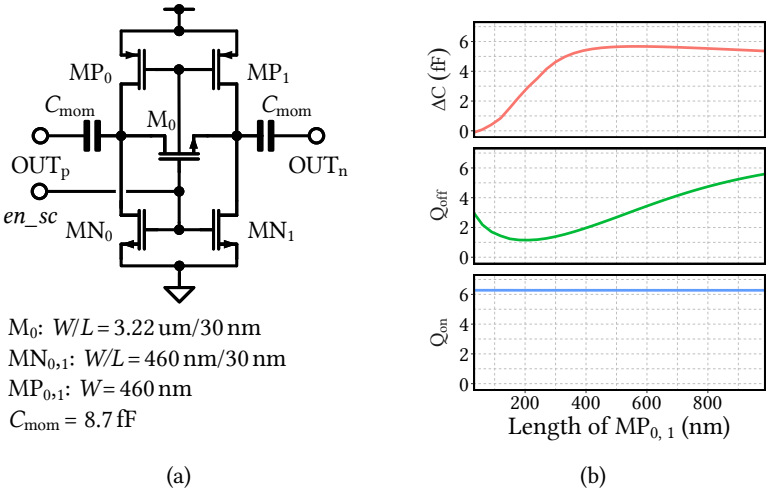
as depicted in Fig. 3.24(b). However, incorporating a large resistor on the drain or source of M_0 introduces a significant time constant, especially for coarse tuning SC cells with a large capacitance C_{mom}. During the transition from the off state to the on state of the SC, the D/S of M_0 remain at V_{DD} for a relatively extended time. Consequently, the g_m devices fail to provide sufficient negative resistance to sustain oscillation until the V_{GS} of M_0 reaches a suitable level.

Fig. 3.25 illustrates the transient response of the DCO when employing resistor-biased SC cells, with R_0 and R_1 set at 250 kΩ and C_{mom} at 8.7 fF. A global enable signal (*EN*) is utilized to activate 256 SC cells at 20 ns. It can be observed that the amplitude decays for approximately 5 ns before recovering. This issue can potentially lead to difficulties in achieving stable locking for PLL system.

In a study conducted by Andreani et al. [54], a method was proposed to address the issue of poor transient behavior observed in resistor-biased SC by decoupling the switch time of the gate and the D/S of M_0. However, this approach entails doubling the number of control signals, which can result in challenges related to signal routing, particularly when employing a large SC bank with numerous unit cells. Moreover, in applications that demand stringent noise performance such as the LC DCO, the use of poly-resistors is generally preferred due to their lower noise contribution. However, in ultra-scaled-down technology nodes, the minimum width of poly-resistors is constrained to a few hundred nanometers to ensure manufacturability,

utilizing a resistor with a value of 250 kΩ is area-intensive and thus has high manufacture cost.

3.4.2 CMOS-biased SC



(a) (b)

Figure 3.26: (a) The schematic and (b) the simulated ΔC and quality factor of CMOS-biased SC over the length of PMOS pull-up transistors.

The CMOS-biased SC circuit, as depicted in Fig. 3.26 and introduced in literature such as [80], is designed to address the inadequate transient performance observed in resistor-biased SC configurations. The schematic in Fig. 3.26(a) illustrates this configuration, where the drain and source of the switch transistor M_0 are biased using complementary MOS pairs. In the off state, MP_0 and MP_1 pull the drain and source of M_0 to the voltage V_{DD}. Consequently, the R_{pu} is determined by the on-resistance of these transistors. In order to have a good quality factor from the SC, MP_0 and MP_1 need to be sized with a large length to provide a large R_{pu}.

Fig. 3.26(b) demonstrates the simulated ΔC and the quality factor. For a SC with a C_{mom} of 8.7 fF, and MP_0 and MP_1 having a width of 460 nm, the lengths of these transistors need to be at least 400 nm to ensure proper switching behavior ($\Delta C \approx \frac{C_{mom}}{2}$). Moreover, for an Q_{off} of 4, MP_0 and MP_1 should be even longer, for instance, 700 nm. However, longer transistors exhibit higher C_{par}, resulting in greater off-state capacitance. This increased capacitance

reduces the overall tuning range, limits the maximum oscillation frequency, and requires more physical space for the entire SC bank.

3.4.3 Constantly-conducting NMOS-biased SC

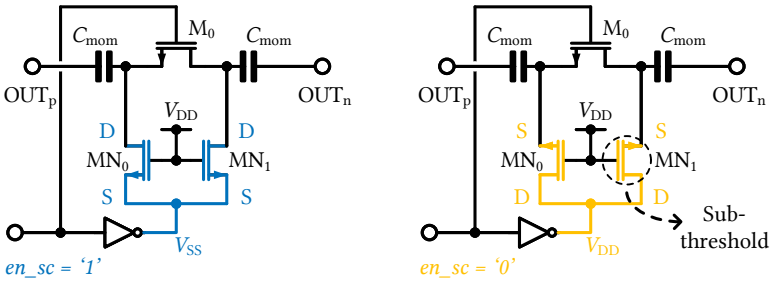


Figure 3.27: Schematic and function principle of the proposed constantly-conducting NMOS (CCNMOS) biased SC. (a) On state and (b) off state.

The structure of the proposed constantly-conducting NMOS (CCNMOS)-biased SC is depicted in Fig. 3.27. In this configuration, M_0 functions as the switch transistor, and its drain and source terminals are biased by MN_0 and MN_1. MN_0 and MN_1 have their gates connected to V_{DD}, ensuring a constantly conducting state for these two transistors. Additionally, the common source of MN_0 and MN_1 is tied to the inverted control signal governing the behavior of the SC.

In the on state, illustrated in Fig. 3.27(a), with the common source pulled to V_{SS}, MN_0 and MN_1 operate in a fully conducting state, serving as low-impedance paths to ground, similar to the behavior observed in the CMOS-biased SC. However, during the off state, as depicted in 3.27(b), the common node of MN_0 and MN_1 is set to V_{DD}. In this state, these two transistors function in drain-source reversal mode, exhibiting behavior similar to that of a source follower. Consequently, the drain-source terminals of M_0 will also be pulled towards approximately V_{DD}, resulting in very low V_{GS} values for MN_0 and MN_1. Operating in the deep sub-threshold region, these transistors can only conduct minimal drain-source leakage current, establishing highly resistive paths for the drain-source of M_0 to V_{DD} such that a very high Q_{off} can be achieved.

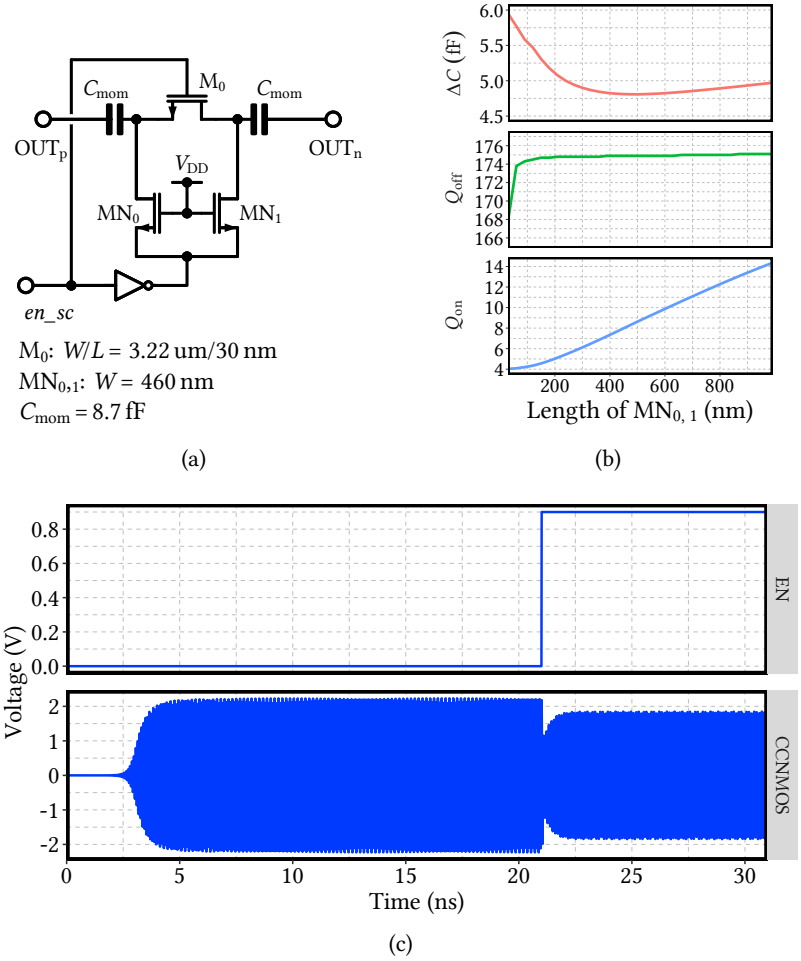


Figure 3.28: (a) The schematic and (b) the simulated ΔC and quality factor of the proposed constantly-conducting NMOS biased SC.

Fig. 3.28(b) depicts the simulated ΔC and quality factor of the proposed CCNMOS-biased SC and the device parameters are given in Fig. 3.28(a). With C_{mom} of 8.7 fF and 460 nm wide MN_0 and MN_1, the CCNMOS-biased SC achieves a Q_{off} of 168 even with the smallest allowed channel length of 30 nm in the 28 nm process.

The proposed CCNMOS-biased SC architecture also mitigates the inadequate transient behavior observed when activating a substantial number of SC cells, which might impede the PLL locking process, as discussed in Sec. 3.4.1. During the off state, MN_0 and MN_1 pull the drain and source of the switch transistor M_0 to V_{DD}. As the SC is switched on, MN_0 and MN_1 retain the capability to conduct high current, facilitating rapid discharge of the drain and source of M_0 due to the substantial V_{GS} of these transistors. Fig. 3.28(c) illustrates the simulated transient response of a 10 GHz DCO employing a CCNMOS-biased SC bank, where a global *EN* signal activates all SC cells in the bank. The analysis shows that the amplitude of the DCO signal barely drops below the transistor threshold and quickly recovers to its maximum value within a timeframe of 1 ns.

3.4.4 CCNMOS-biased SC for fine tuning

While the incorporation of an ADPLL in the FMCW system offers advantages, the finite resolution of the DCO introduces unavoidable quantization noise. This noise can potentially serve as a limiting factor for the out-of-band noise of an ADPLL. At a frequency offset Δf from the oscillation frequency f_0, the introduced quantization error of the DCO can be mathematically expressed using Equation 3.35:

$$\mathcal{L}_{QN}(\Delta f) = \frac{1}{12} \cdot \left(\frac{f_{\text{res}}}{\Delta f}\right)^2 \cdot \frac{1}{f_0} \cdot \text{sinc}^2\left(\frac{\Delta f}{f_0}\right) \tag{3.35}$$

Here, f_{res} represents the tuning resolution [81]. Although the inclusion of a $\Sigma\Delta$ modulator in the ADPLL design can help alleviate the quantization noise, a substantial portion of the noise persists due to bandwidth limitations and finite attenuation [82]. Consequently, achieving an exceptionally fine tuning resolution in the DCO becomes an area of considerable interest.

As per Eq. 3.29, the value of ΔC, crucial in determining the frequency resolution of the DCO, is significantly influenced by the capacitance C_{mom}. In theory, one can directly reduce the size of C_{mom} to achieve a finer resolution. However, practical constraints arise from the limitations imposed by

technology PDK-provided MOM capacitors. These capacitors have specific restrictions on geometric parameters, including minimum metal layers, length, and the number of fingers. To comply with the resolution specifications of the DCO, in this work, customized the C_{mom} is utilized in the fine-tuning bank by employing a smaller number of fingers and metal layers.

However, diminishing the physical dimensions of capacitors within the SC unit cell introduces challenges in meeting strict density design rules in an ultra-deep-submicron technology. To address this issue, in this work, a modification to the CCNMOS-biased SC is proposed by incorporating a large fringe capacitor, C_{L}, connected across the drain and source of the switch transistor M_0, as depicted in Fig. 3.29(a).

The on-state equivalent circuit is illustrated in Fig. 3.29(b). During the on state, the substantial C_{L} is effectively shorted by the small on-resistance of the NMOS switch. Consequently, the on-state differential capacitance C_{on} of the SC equals that of the coarse and intermediate tuning SC, represented as:

$$C_{\text{on}} = \frac{C_{\text{mom}}}{2} \tag{3.36}$$

On the other hand, in the off state, depicted in Fig. 3.29(c), the effective differential capacitance of the SC accounts for the series capacitance of three capacitors, i.e. two C_{mom} and C_{L}, expressed as:

$$\begin{aligned} C_{\text{off}} &= \frac{1}{\frac{1}{\frac{C_{\text{mom}}}{2}} + \frac{1}{C_{\text{L}}}} \\ &= \frac{C_{\text{mom}} C_{\text{L}}}{2C_{\text{L}} + C_{\text{mom}}} \end{aligned} \tag{3.37}$$

Consequently, the capacitance difference between the on and off states is derived as:

$$\begin{aligned} \Delta C_{\text{fine}} &= C_{\text{on}} - C_{\text{off}} \\ &= \frac{C_{\text{mom}}^2}{4C_{\text{L}} + 2C_{\text{mom}}} \end{aligned} \tag{3.38}$$

The enhancement in tuning resolution is facilitated by the relatively large capacitor C_{L}. Additionally, Fig. 3.29(d) displays the layout of the fine-tuning SC, where C_{mom} comprises two fingers using metals 5 and 6. The supplementary capacitor C_L is a 19 fF MOM capacitor employing metals 4 to 6. The transistors within this SC cell are positioned beneath the capacitors and utilize metals 1 to 3 for interconnection. Simulation result with the extracted layout shows this design achieve a the ΔC of around 5 aF.

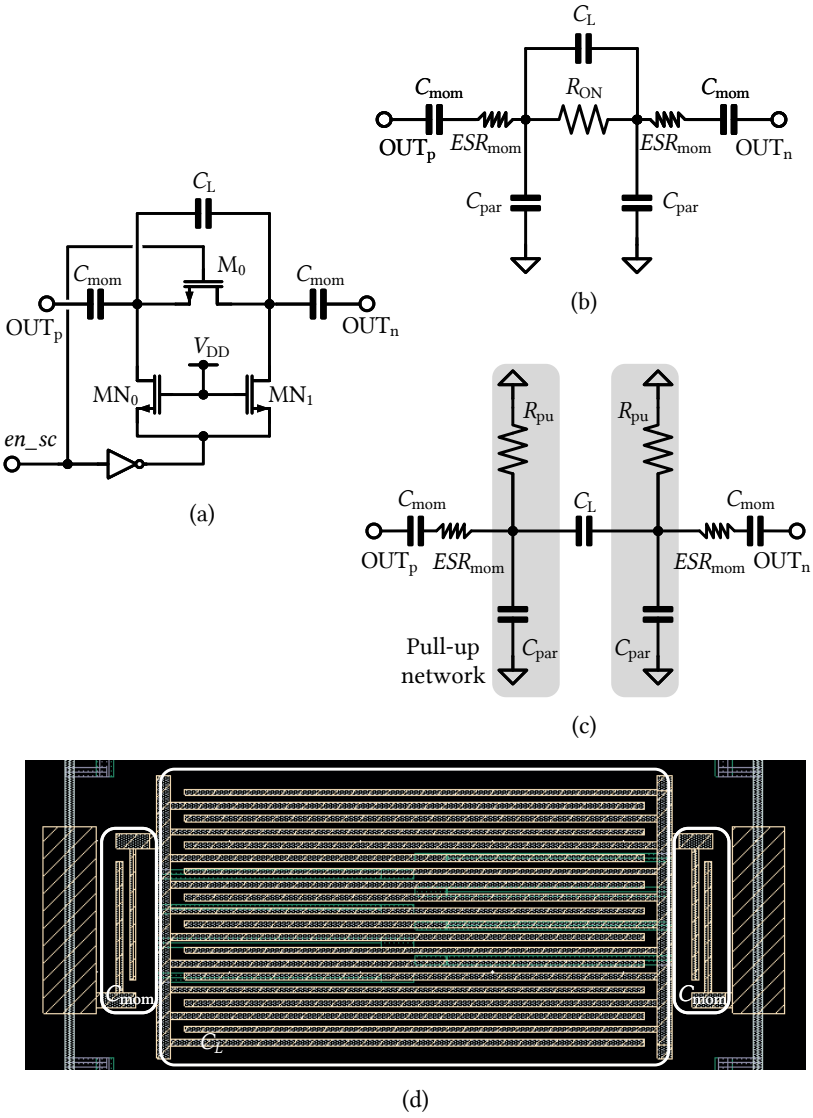
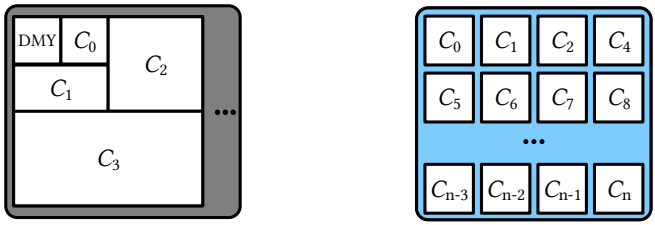


Figure 3.29: (a) Schematic, (b) on-state, (c) off-state equivalent circuits and (d) simplified layout of a fine-tuning SC cell.

3.4.5 Design of SC Array



(a) (b)

Figure 3.30: Illustration of switchable capacitor bank formation schemes. (a) Binary-Weighted. (b) Unitary-weighted.

The SC bank in a DCO is usually partitioned into two or three sub-banks with different tuning step granularity. Fig. 3.30 shows two structures of an SC bank. Conventionally, a binary-weighted scheme, wherein the SC value doubles for every bit from the least significant bit (LSB) to the most significant bit (MSB), as depicted in Fig. 3.30(a), is utilized for the coarse tuning bank due to its fewer control signals and lower total C_{off}. However, managing the parasitic effects caused by interconnections becomes progressively challenging during the continuous down-scaling process. This challenge makes it more difficult for a binary-weighted SC bank to guarantee a monotonic frequency tuning.

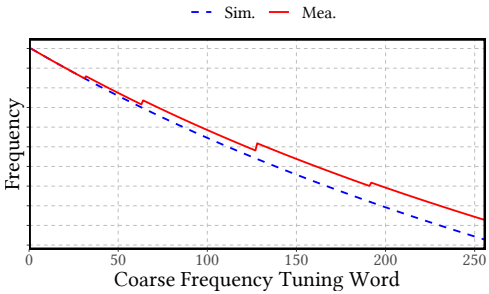


Figure 3.31: Potential non-monotonic frequency tuning behavior of a DCO with a binary-weighted SC array.

Fig. 3.31 demonstrates the potential non-monotonic frequency tuning behavior of the DCO due to PVT variations, particularly noticeable dur-

ing the transition between frequency control words of 2^{n-1} and 2^{n}. This non-monotonicity in the DCO's behavior can significantly disrupt the PLL's locking process, leading the loop to falsely adopt a false FCW.

The SC bank, composed of unitary cells as depicted in Fig. 3.30(b), inherently maintains monotonicity in frequency tuning. However, it tends to accumulate off-state capacitance, notably within the coarse tuning bank, hence limiting the overall tuning range and oscillation frequency. In applications, especially in scenarios demanding robustness of application-specific integrated circuit (ASIC)s such as automotive radar, a scheme utilizing a unitary-weighted SC array is preferred.

Thanks to the introduction of the proposed CCNMOS-biased SC cell, it becomes feasible to minimize the accumulated C_{off} and thus enable the utilization of a unitary-weighted SC array, even at high oscillation frequencies reaching 10 GHz. This innovation facilitates maintaining the desired characteristics within the SC array while reducing the adverse effects of accumulated capacitance in high-frequency operations, meeting the stringent requirements in applications such as automotive radar systems.

3.5 Frequency Divider, Clock Distribution and Measurement Setup

The operation of an ADPLL relies on a digital clock signal featuring a square waveform. However, due to the inherent linearity of the LC oscillator, the resulting signal is sinusoidal in nature. Consequently, a squaring circuit is necessary to convert this sinusoidal signal into a square waveform. While a basic inverter could potentially perform this conversion, it is essential to consider that the DC operating points of the LC oscillator's outputs may differ from those of a simple inverter. For instance, outputs of the oscillator using NMOS structures might operate at a voltage level of V_{DD} for their g_{m} core, while that of PMOS g_{m} cores could operate at V_{SS}. Furthermore, variations in power domains might exist, as the LC oscillator could utilize a V_{DD} that surpasses the voltage level of the core transistors, aiming for improved phase noise performance. Such differences in DC operating points and power domains could result in malfunctions and reliability issues for a DC coupled squarer.

In Figure 3.32, the schematic of the proposed squarer is depicted. The first stage involves an inverter biased by a feedback resistor R_{B}, where the inputs

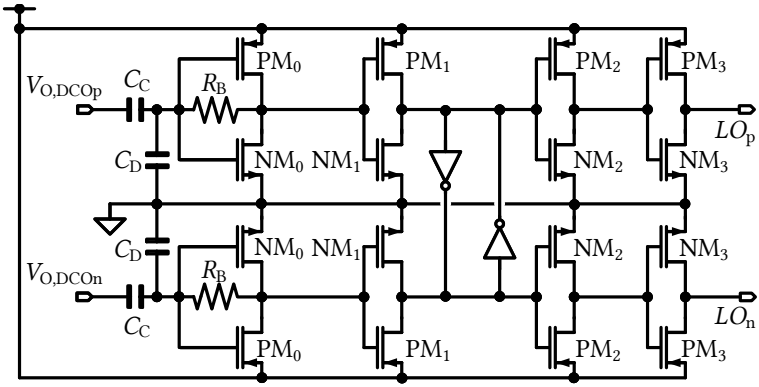


Figure 3.32: Schematic of the squarer.

are AC coupled to the outputs of the DCO using capacitor C_C. Additionally, capacitors C_C and C_D are arranged to form a capacitive divider, reducing the voltage swing at the gates of PM_0 and NM_0. An inverter chain with a ratio of 2 is employed to ensure sufficient drive strength. Following the second stage, two cross-coupled inverters between the positive and negative signal chains are utilized to correct the signal's duty cycle.

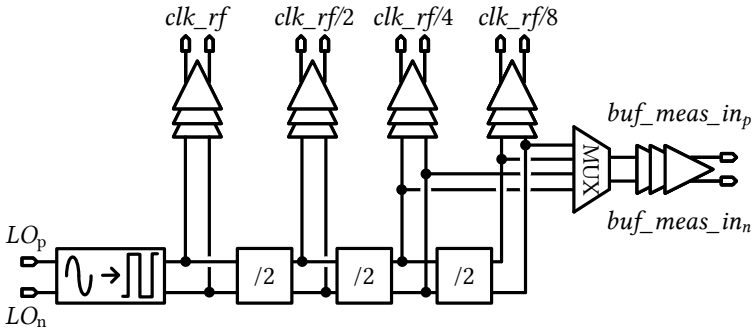


Figure 3.33: Schematic of the on-chip RF clock distribution.

Fig. 3.33 demonstrates the RF clock distribution system directed towards both the TDC and digital signal processing (DSP) units within the ADPLL. This block includes the squarer alongside a series of divide-by-2 frequency dividers designed to generate signals with the frequency of the DCO and its divisions by 2, 4, and 8. A multiplexer is employed to choose the signal for

transmission to the measurement buffer for silicon validation purposes.

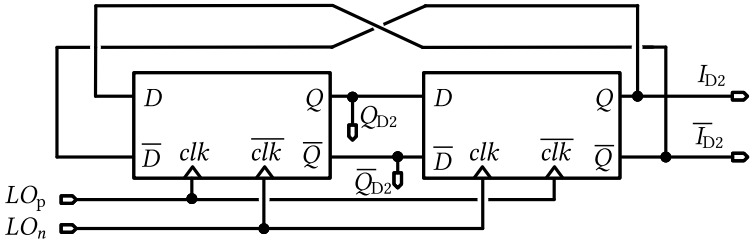


Figure 3.34: Schematic of the divide-by-2 frequency divider.

Ideally, the divide-by-2 divider can be digitally synthesized using standard cells. However, because of the very high oscillation frequency of around 10 GHz from the DCO, a synthesized divider constructed using standard cells may not function reliably. Consequently, the RF divider needs to be manually designed. Fig. 3.34 presents the fundamental concept of the divider employing two differential D-latches. These latches have their inputs connected to the inverse outputs. Consequently, the frequency of the signal at the I and Q inputs is half that of the input.

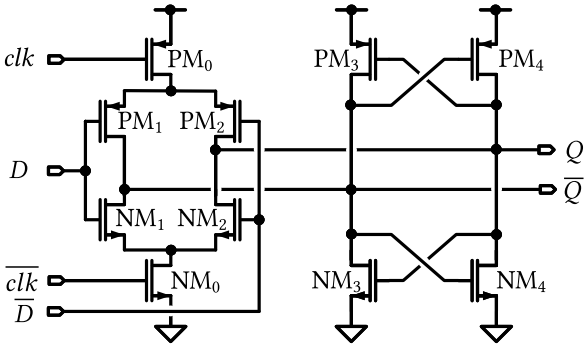


Figure 3.35: Schematic of the differential D-latch.

Fig. 3.35 shows the schematic of the differential D-latch implemented in this work. It consists of a differential gated inverter that drives an inverter latch. Notably, the drive strength of the gated inverters must be higher than that of the inverter latch to ensure the ability to overwrite the state.

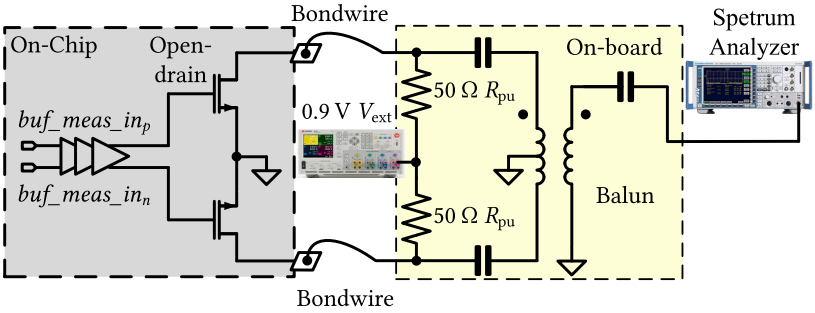


Figure 3.36: Measurement setup with the open-drain buffer.

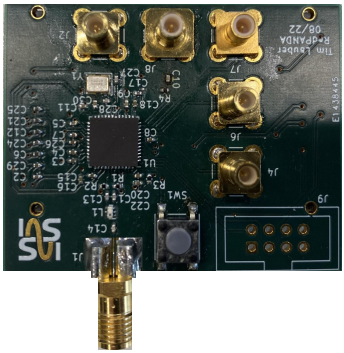


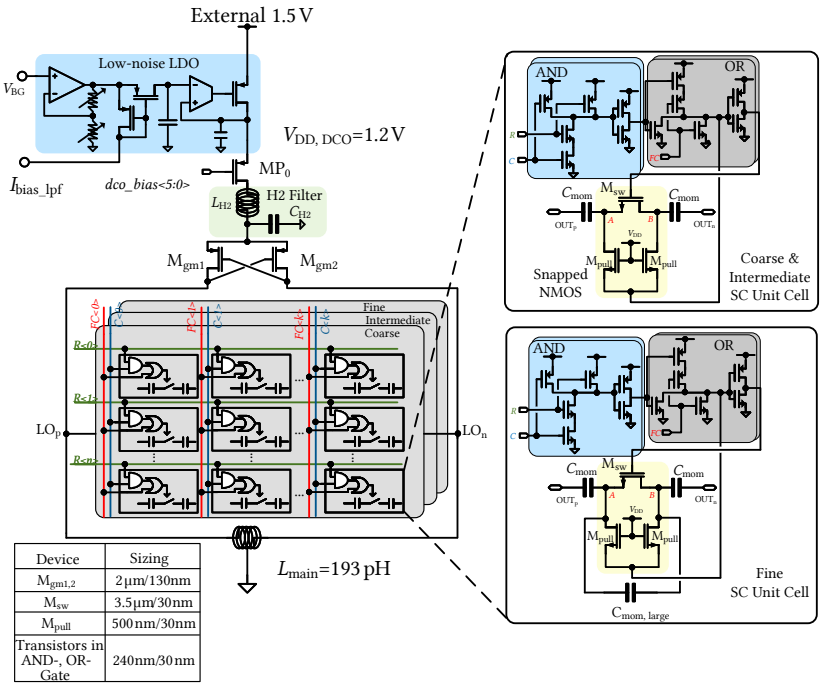
Figure 3.37: Measurement board used in this work.

The illustration of the measurement setup employed for the DCO within this thesis is depicted in Fig. 3.36. The LO output is connected to a pre-buffer, followed by a very strong open-drain measurement buffer, aimed at driving the substantial parasitic capacitance caused by the bond pad and the inductance due to the bond wire. On the measurement board[1], whose photo is shown in Fig. 3.37, two 50-ohm resistors, attached to a clean external V_{DD} provided by Keysight N6705B [83], serve as pull-up resistors, also matching with the input impedance of the spectrum analyzer. A balun is incorporated to convert the differential input into a single-ended signal, facilitating its connection to the spectrum analyzer Rohde & Schwarz FSQ 40 [84].

[1]The implementation of the measurement PCB was conducted by Tim Lauber.

3.6 DCO Prototypes

3.6.1 Class-B DCO with 2nd Harmonic Tail Filter



Device	Sizing
$M_{gm1,2}$	2 µm/130 nm
M_{sw}	3.5 µm/30 nm
M_{pull}	500 nm/30 nm
Transistors in AND-, OR-Gate	240 nm/30 nm

Figure 3.38: Detailed schematic of the proposed class-B DCO using CCNMOS SC bank.

Fig. 3.38 provides the detailed schematic of the proposed class-B DCO integrated with a second harmonic (H2) tail filter. Within this setup, a switch denoted as MP$_0$ is utilized to bias the source voltage of the DCO. In contrast to the conventional method involving a current source-biased LC oscillator, the substitution of the current source with a switch or a switchable poly-resistor can significantly decrease the overall phase noise of the oscillator. This is crucial since the current source typically stands out as one of the primary sources of flicker noise, as highlighted in previous studies [85]. However, this replacement imposes a more stringent output noise requirement for the power supply.

To address this issue, a two-stage LNLDO is employed to alleviate the impact. This LNLDO incorporates a low-pass filter characterized by an extremely low cut-off frequency, effectively filtering the noise stemming from both the bandgap reference and the resistive voltage divider [17]. It is noteworthy that the detailed design specifics of the LNLDO will be discussed in a separate chapter.

In advanced technological nodes, the gap in mobility between p-type and n-type transistors has decreased significantly. Consequently, there is no imperative need to proportionally increase the size of PMOS transistors to achieve equivalent g_m in comparison to NMOS transistors given the same tail current. Opting for PMOS g_m cores is thus favored owing to the inherent lower flicker noise generated by PMOS devices.

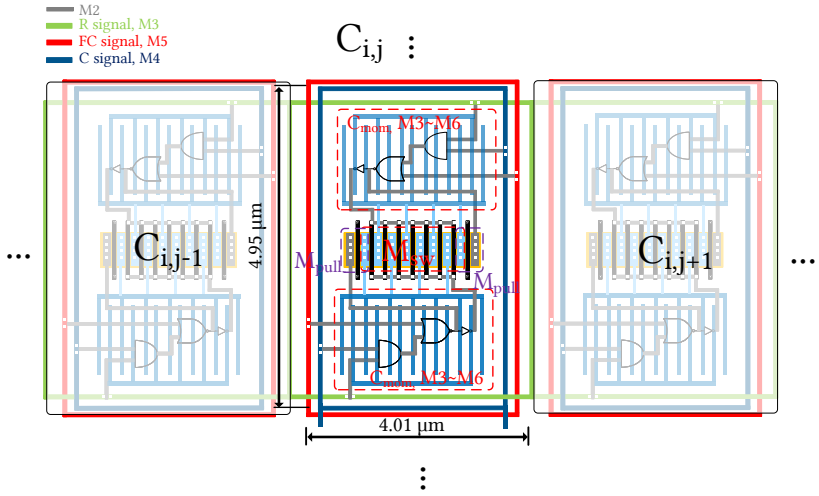


Figure 3.39: Simplified layout of a coarse SC in the tuning bank matrix. Metal 1 and its interconnection are not shown for better visibility.

Furthermore, the N-well structure inherent in PMOS transistors offers uncomplicated and direct substrate isolation. While achieving similar isolation for NMOS transistors is possible by utilizing deep N-well or high-ohmic native layers i.e. the NT_N layer, this approach results in a larger area footprint compared to using only PMOS with N-well for isolation purposes. Additionally, the transistors M_{gm1} and M_{gm2} have been intentionally selected as thick-oxide devices, primarily due to the substantial voltage stress encountered by these transistors resulting from the oscillation amplitude.

The SC cells are organized within a 32-column matrix controlled by address signal, very similar to SRAM design, to alleviate the routing complexities. Each individual SC cell is controlled by both a row (R) and a column (C) signal. Enabling the entire column's SC cells is achieved through the use of full-column (FC) signals. To tune the frequency, the frequency tuning word needs conversion into row and column address signals, which are then transmitted to the SC bank matrix. The address decoder is integrated within each individual SC cell unit. The coarse, intermediate, and fine tuning banks consist of 256 unitary cells across 8 rows, 64 cells distributed in 2 rows, and 128 cells within 4 rows, respectively.

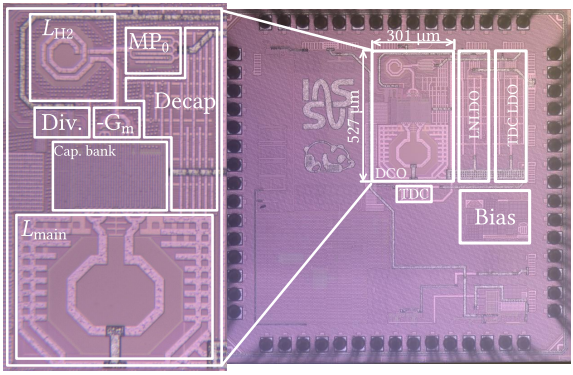


Figure 3.40: Chip micrograph of the class-B DCO prototype, whose active area is 0.13 mm^2.

Fig. 3.39 illustrates the simplified layout of a single SC cell within the coarse bank. To minimize substrate coupling, the fringe capacitors employ metal 3 to metal 6. The area beneath the fringe capacitors, with M1 and M2 available for routing, accommodates the placement of the address decoder. This decoder is duplicated beneath both instances of C_{mom}, ensuring a symmetrical layout. To reduce routing complexity within the bank, address signals (R, C, and FC) are routed around the edge of the unit cell. This design approach enables automatic connection of address buses between adjacent cells by overlapping corresponding metal lines in the layout. The intermediate and fine SC banks adopt a similar arrangement, differing primarily in fringe capacitor sizes to maintain a uniform layout structure.

The DCO design has been implemented and manufactured using a 28 nm technology, whose micrograph is given in Fig. 3.40. The physical footprint of the DCO, encompassing the output frequency dividers and buffers, measures

0.13 mm^2. Operating at a supply voltage of 1.2 V, this DCO shows its frequency tuning capabilities through a series of experiments.

The frequency tuning range measurement of the proposed DCO is accomplished by sweeping the control word of the coarse capacitor bank while keeping the intermediate and fine capacitor banks deactivated. The results, shown in Fig. 3.41, demonstrate the coarse tuning bank's effectiveness in covering an oscillation frequency range of 8.2-10.2 GHz in 256 steps, with an average tuning step of 7.7 MHz.

Further evaluations concentrate on the tuning capacities of the intermediate and fine capacitor banks, specifically around an oscillation frequency of 10 GHz. The intermediate bank, comprising 64 switchable unitary capacitor cells, demonstrates an average tuning step of 370 kHz and a range of 24 MHz, as depicted in Fig. 3.42.

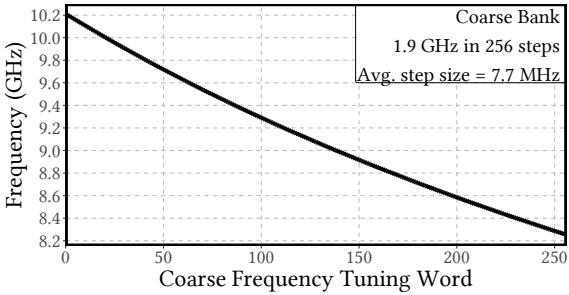


Figure 3.41: Measured coarse bank frequency tuning.

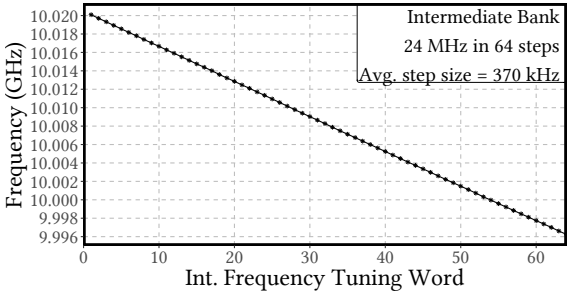


Figure 3.42: Measured intermediate bank frequency tuning around 10 GHz.

Fig. 3.43 demonstrates that the fine bank has a tuning range of 2.24 MHz in 128 steps. Fig. 3.44 shows the frequency tuning step of the fine bank. The

proposed design achieves a resolution of smaller than 60 kHz and an average resolution of 17.5 kHz. The frequency covering range of a smaller capacitor bank is designed to be able to cover the frequency change of at least 2 steps in the larger capacitor bank.

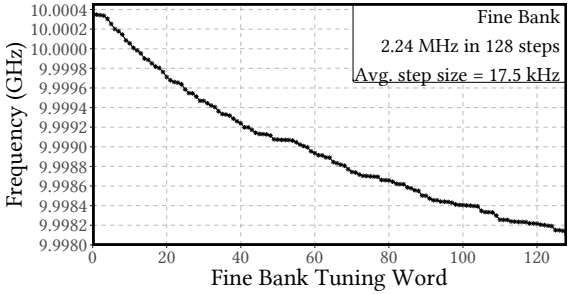


Figure 3.43: Measured fine bank frequency tuning around 10 GHz.

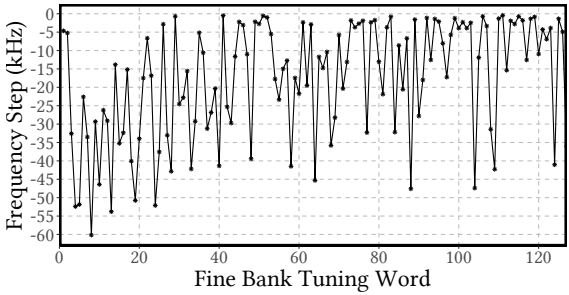
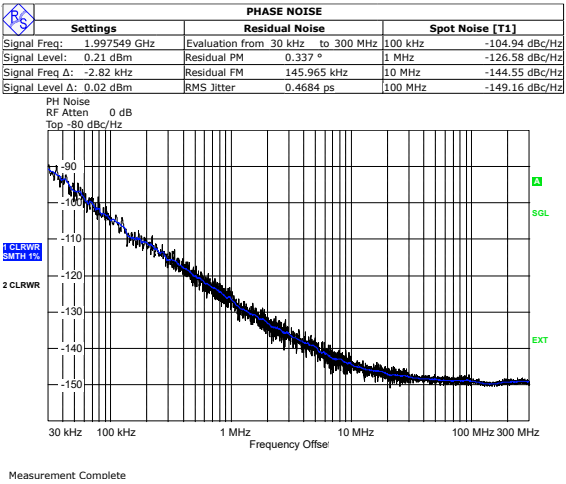
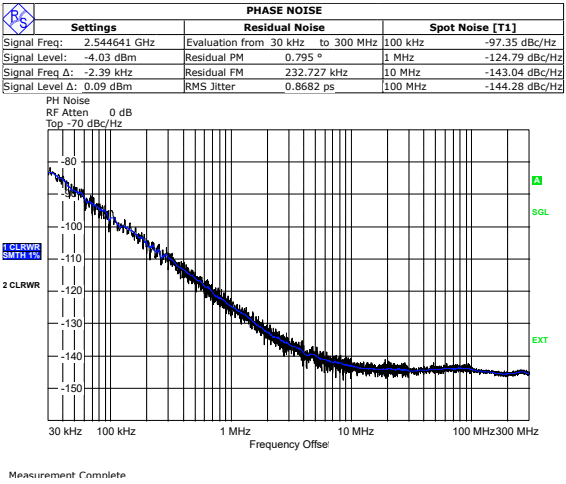


Figure 3.44: Measured fine bank frequency tuning step.

The phase noise performance measured at the maximum and minimum frequencies of the proposed DCO is illustrated in Fig. 3.45. To achieve a better measurability, the DCO's signal is divided by 4 and then measured by the spectrum analyzer. At a frequency of 2 GHz, the DCO exhibits a phase noise of −126.6 dBc/Hz with an offset of 1 MHz, corresponding to −114.6 dBc/Hz at 8 GHz. At the upper frequency limit, with all SC cells deactivated, the DCO demonstrates a phase noise of −124.8 dBc/Hz at 2.55 GHz, which translates to −112.8 dBc/Hz at 10.2 GHz.



(a)



(b)

Figure 3.45: Measured phase noise at carrier frequency of (a) 8 GHz (b) 10.2 GHz, with frequency ÷4 output.

For a fair comparison with the state-of-the-art oscillators design, the figure-of-merit (FoM) is used in publications. The FoM of oscillators is given by

$$\mathrm{FoM} = \mathrm{PN} - 20\log\left(\frac{f_0}{f_{\mathrm{off}}}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1\mathrm{mW}}\right) \tag{3.39}$$

The implementation of the oscillator's SC bank design involves a trade-off between phase noise and tuning range. Consequently, it becomes sensible to include the tuning range (TR) of the oscillator in the comparison. To incorporate this aspect, a figure-of-merit denoted as $\mathrm{FoM_T}$, which integrates TR in percentage, is introduced:

$$\mathrm{FoM_T} = \mathrm{PN} - 20\log\left(\frac{f_0}{f_{\mathrm{off}}} \cdot \frac{TR}{10}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1\mathrm{mW}}\right) \tag{3.40}$$

The proposed DCO with a TR of 24%, operating at a power consumption of 13 mW, achieves a FoM of −183 dBc/Hz and a $\mathrm{FoM_T}$ of −191 dBc/Hz.

Fig. 3.46 represents the phase noise characteristics of the DCO across its tuning range. An observable trend shows a marginal reduction in phase noise as the DCO undergoes tuning from 8.2 to 8.5 GHz at 1 MHz and 10 MHz offset frequencies. This decrease is attributed to the considerably higher off-state quality factor within the proposed Switched Capacitor (SC) compared to its on state counterpart.

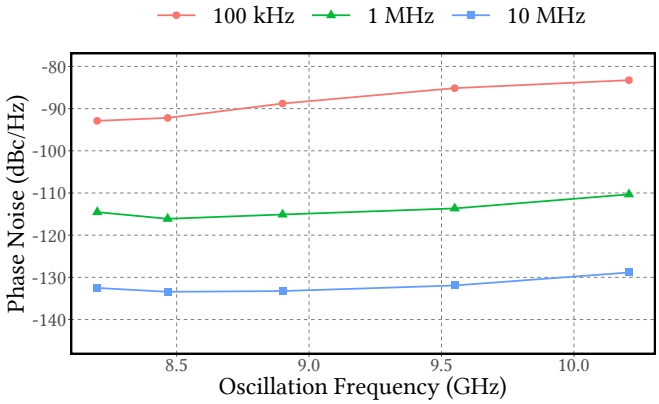


Figure 3.46: Measured phase noise across the oscillator tuning range.

In the operation where most SCs within the coarse bank are in the on state, they are the dominant contributors to the quality factor of the LC tank. However, upon deactivating a certain number of SCs, the inductor begins to take precedence as the primary contributor to the quality factor. Consequently, this shift leads to the anticipated slight rise in phase noise with an increase in the oscillation frequency. This effect can be mitigated by marginally increasing the width of the switch transistors, at the expense of reducing the tuning range.

3.6.2 RC-biased Class-C DCO

Published in [19], a class-C DCO prototype has also been designed in this thesis work. Fig. 3.47 presents the simplified layout of the DCO, illustrating the floorplan of components. Positioned at the center is the CCNMOS SC

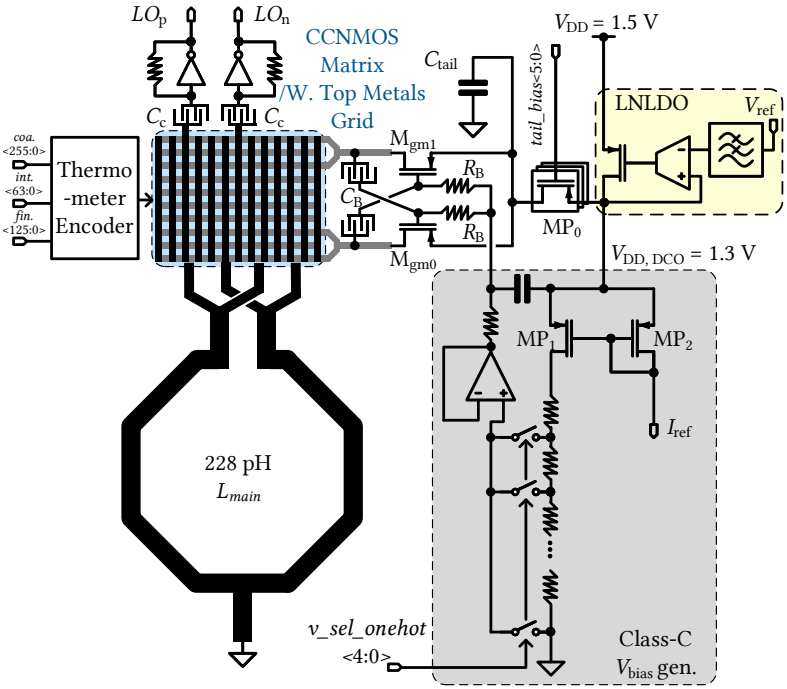


Figure 3.47: Simplified layout of the proposed class-C DCO, showing the blocks floorplan.

matrix. Using the top 2 metal layers, the SC matrix forms a low-ohmic grid for the oscillator's differential output. Below this matrix locates a high-Q inductor in an O-shape with 228 pH. On the upper side of the matrix, the AC-coupled squarer is situated, followed by the RF clock distributor. Adjacent to the matrix's right side lies the g_m stage. Capacitor C_B provides AC-coupled feedback to the gate, while the DC operating point of the gate is biased via a 2 kΩ poly resistor R_B. The common source of the g_m devices is biased through a low-ohmic switch MP_0 and connected to a 5 pF tail capacitor C_{tail} aimed at filtering high-frequency noise and providing AC grounding. Furthermore, a LNLDO supplies a low-noise 1.3 V power source to the DCO core from an external 1.5 V input, offering additional PSR by utilizing a pass transistor with a 200 mV voltage drop to enhance the phase noise performance of the DCO.

The gate's DC bias voltage for the g_m devices is generated by the class-C V_{bias} generator. This circuit essentially constitutes a resistor ladder incorporating one-hot signal-controlled switches. The generated voltage is subsequently buffered and connected to a low-pass filter with an extremely low cut-off frequency to ensure minimal interference from this block's noise into the g_m devices, thereby preserving the phase noise performance.

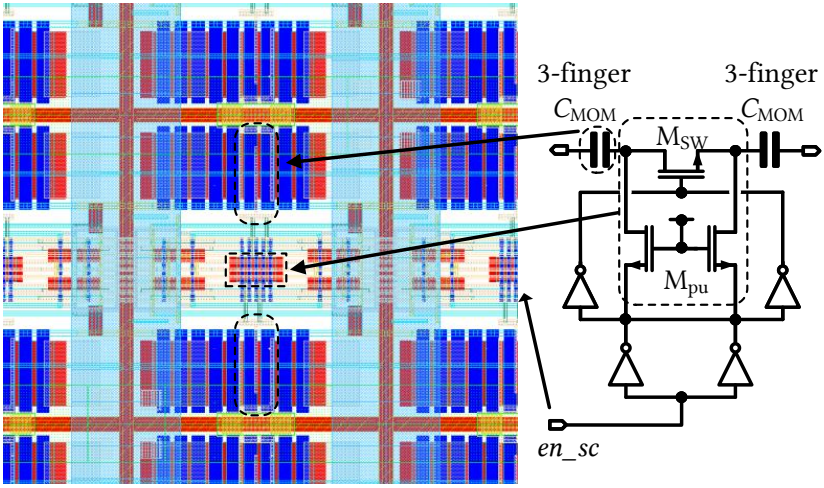


Figure 3.48: Layout of SC cell for fine tuning using customized fringe capacitor.

In contrast to the class-B prototype, the class-C redesign of the CCNMOS SC cell does not integrate an address decoder within it. Instead, the decoder

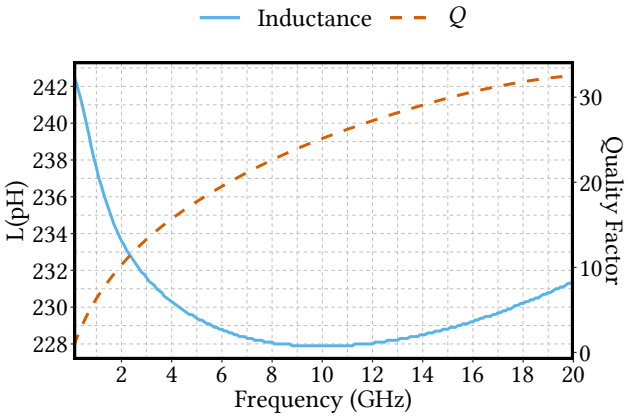


Figure 3.49: Simulated inductance and quality factor of the coil.

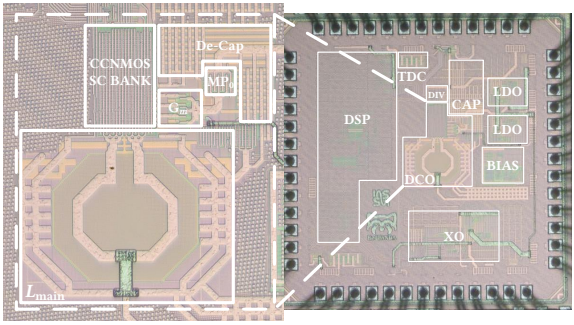


Figure 3.50: Micrograph of the class-C DCO prototype.

is directly generated by the digital synthesizer. While this alteration significantly increases routing complexity for the SC matrix, eliminating the decoder beneath the MOM capacitor offers the advantage of reduced capacitive coupling from the oscillator outputs. Consequently, this configuration enables higher maximum oscillation frequency.

Fig. 3.48 displays the layout of the SC in the fine-tuning bank, featuring a manually crafted C_{mom} with only 3 fingers. Positioned below the C_{mom}, a MOS capacitor ensures compliance with density rules and stabilizes the local V_{DD}. The switches M_{SW} and two M_{pull} share the same active region and are placed in the middle. Inverters are utilized to set up voltage level for the

switch gate and the common source of M_{pull}. These inverters are duplicated to maintain a strictly symmetrical layout. Control signals are routed above the M_{SW} and M_{pull} using metal 4 and 6. For SC cells utilized in coarse and intermediate tuning banks, the same structure is maintained, varying only the finger count of C_{mom}.

In this design, an O-shaped spiral inductor is employed, utilizing an ultra-thick top copper metal with a width of 15 μm to achieve a high quality factor. Fig. 3.49 presents the simulated inductance and quality factor of the coil via Cadence EMX. At the specified frequency of 10 GHz, the coil exhibits an inductance of approximately 228 pH and a quality factor of 25.

The proposed DCO has been implemented in a 28 nm CMOS technology. Fig. 3.50 shows the micrograph of the class-C prototype. The class-C prototype reduces the area to 0.07 mm^2 by 46% due to the removal of the H-2 tail coil in comparison to the class-B prototype discussed in section 3.6.1.

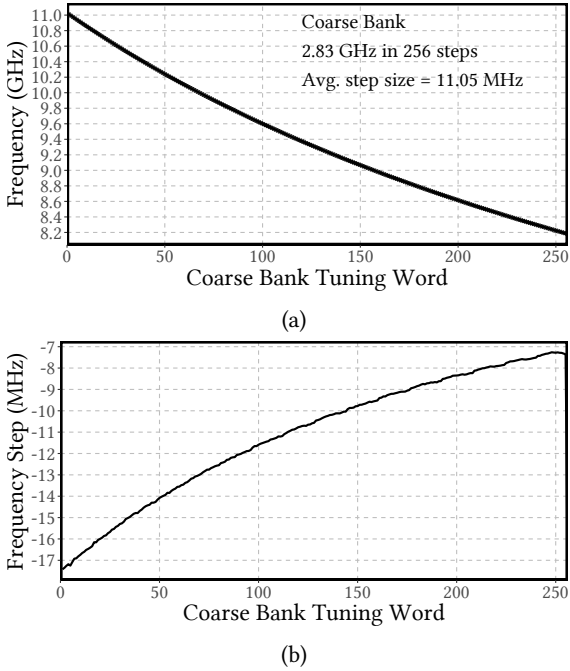


Figure 3.51: Measured class-C DCO prototype coarse frequency tuning. (a) Tuning range. (b) Coarse bank frequency tuning step.

The coarse tuning bank frequency coverage of the class-C DCO is depicted in Fig. 3.51(a), with SCs in intermediate and fine bank switched off. It can be seen that the coarse bank covers 8.2 GHz to 11.1 GHz in 256 steps. Fig. 3.51(b) illustrates the frequency step size over the tuning range and the tuning resolution of the coarse bank ranges from 7 MHz to 17 MHz, according to different oscillation frequencies, with an inherent monotonicity.

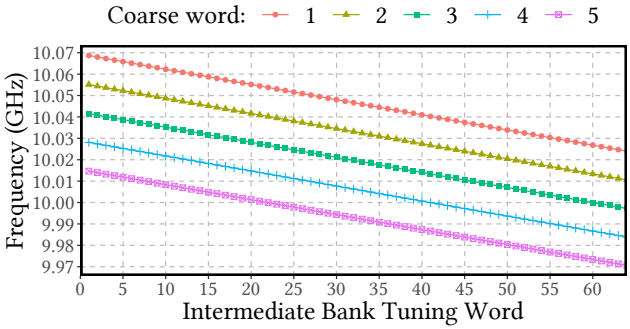


Figure 3.52: Measured DCO intermediate bank tuning around 10 GHz, with 5 consecutive coarse bank steps.

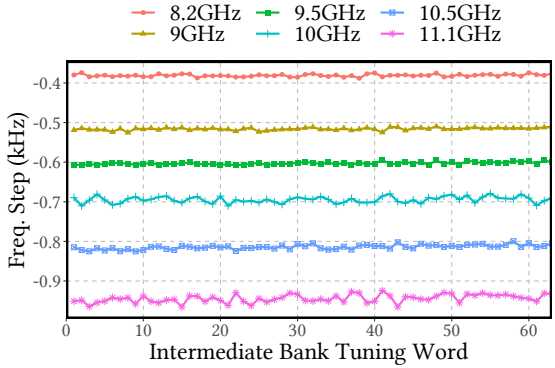


Figure 3.53: Measured intermediate bank tuning resolution across the DCO tuning range.

Fig. 3.52 shows the frequency sweep of the 64-step intermediate bank with 5 consecutive coarse bank steps around 10 GHz. The tuning range of the intermediate bank is able to cover at least two coarse bank steps. Fig. 3.53 depicts the frequency tuning resolution of the intermediate bank over the

oscillator tuning range, and the step size of the intermediate bank is between 380 kHz and 950 kHz.

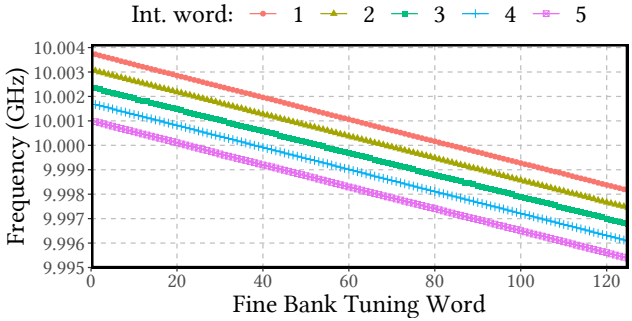


Figure 3.54: Measured DCO fine bank tuning around 10 GHz, with 5 consecutive intermediate bank steps.

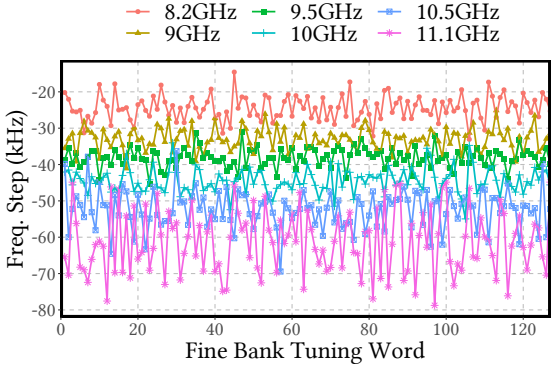


Figure 3.55: Measured fine bank tuning resolution across the DCO tuning range.

In addition, the frequency tuning ability of the 125-step fine bank with 5 intermediate bank steps is demonstrated in Fig. 3.54. The tuning range of the fine bank is designed to cover at least 4 intermediate steps. The tuning step of the fine bank is shown in Fig. 3.55, and the resolution ranges from 20 kHz to 75 kHz, depending on the oscillation frequency. At around 10 GHz, the frequency tuning resolution of the class-C DCO is 40 kHz.

The measured phase noise performance at a 10 GHz carrier frequency

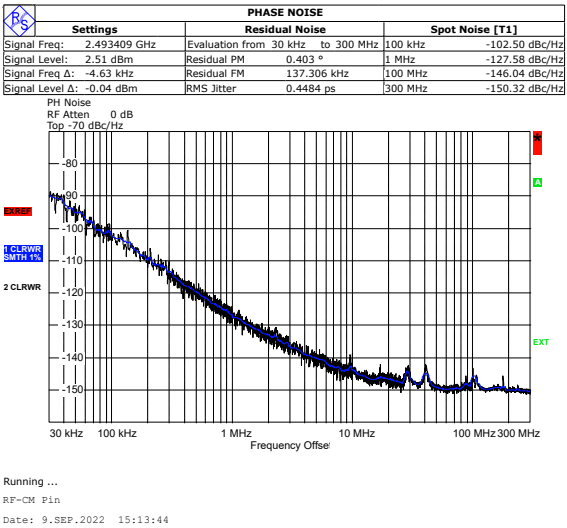


Figure 3.56: Measured class-C DCO phase noise at 10 GHz, with the ÷4 output.

of the class-C prototype is depicted in Fig. 3.56. At 1 MHz offset from the carrier frequency, the class-C DCO achieves a phase noise of −115.5 dBc/Hz with 23 mW power consumption, resulting in a FoM of −182 dBc/Hz. With a tuning range of 30.1%, the proposed class-C DCO achieves a −191.5 dBc/Hz FoM_T at 1 MHz offset. Fig. 3.57 shows the measured DCO phase noise over its tuning range. The phase noise change of the class-C DCO is smaller in comparison to the class-B prototype presented in [16] because our prior published class-B DCO does not have a tunable tail filter to better limit the flicker noise up-conversion, whereas the oscillator in the class-C configuration does not require one.

3.6.3 Summary of Experimental Results

Table 3.1 gives a performance summary of the proposed DCOs and compares it with state-of-the-art multi-GHz DCOs/VCOs. The proposed DCOs provide the advantage of an inherently monotonic frequency tuning and an ultra-fine tuning resolution thanks to the innovative CCNMOS-biased SC structure, which are very helpful in a highly-demanding ADPLL application. The FoM and FoM_T of the proposed DCO align with that of the prior reported designs

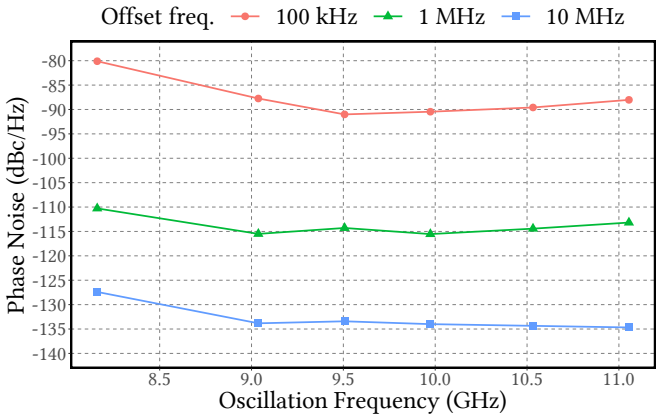


Figure 3.57: Measured phase noise across the class-C oscillator tuning range.

in a similar technology node except for the design using an implicit resonate architecture [74].

However, the class-C technique has the advantage of not requiring an additional tunable common-mode capacitor bank or a secondary tail coil for optimum noise performance over the oscillator tuning range, and thus the area of a class-C oscillator is also smaller in comparison to designs reported in [74], [39] and [16].

Table 3.1
Performance comparison of state-of-the-art multi-gigahertz DCO.

Performance	[86]	[74]	[77]	[39]	PANDA	RedPANDA
Feature	Bottom-pinning SC	Implicit resonate	Class-C	Class-F_{23}	CCNMOS Class-B	CCNMOS Class-C
Tech. (nm)	28	28	28	28	28	28
Freq. (GHz)	12.7	3.75	20.9	31.2	9	10
TR (%)	32	27	12	14	24	30.1
V_{DD} (V)	0.9	0.9	0.9	1	1.2	1.3
Resolution (Hz)	Analog	N.A.	Analog	Analog	60k	40k
Inherent monotonicity	No	No	No	No	Yes	Yes
PN@1MHz (dBc/Hz)	-107	-127.5	-112.3	-106	-115.1	-115.5
FoM*@1MHz (dBc/Hz)	-179	-191	-185	-184	-183	-182
FoM_T**@1MHz (dBc/H	-189	-199	-187	-187	-190.6	-191.5
Power (mW)	8.3	6.6	20.7	13	13	23
Area (mm^2)	0.13	0.15	0.07	0.15	0.13	0.07

*FoM = PN - $20\log(f_{osc}/f_{offset})$ + $10\log(P_{DC}(mW))$
**FoM_T = PN - $20\log((f_{osc}/f_{offset})(TR/10))$ + $10\log(P_{DC}(mW))$

CHAPTER 4

POWER SUPPLY FOR LOW-NOISE RF APPLICATIONS

As discussed in the previous chapter, the phase noise from frequency generation circuits, such as the DCO, constitutes a significant part of the overall noise characteristics of the LO. This factor holds paramount importance in RF systems, notably in applications like FMCW radar. In the context of an LC oscillator, beyond the intrinsic noise attributed to devices, the random variations in the supply voltage, known to as power supply noise, serve as another substantial source contributing to phase noise [87].

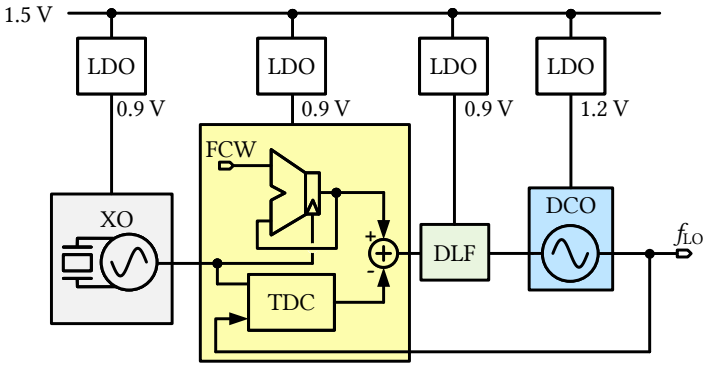


Figure 4.1: Power domain separation of an ADPLL using low-dropout regulator (LDO).

In a nano-scale CMOS technology, the impact of power supply noise becomes increasingly significant due to the decreased power supply voltage, resulting in a reduction in oscillation amplitude. Furthermore, the trend towards higher integration levels in RF-system-on-chip (SoC) designs, wherein RF, analog, and digital circuits are consolidated onto a single chip, is favored because of its compact footprint and long-term cost reduction [88]. However, the switching activity inherent in digital circuits can induce IR-drop on the

supply voltage, contributing to power supply fluctuations. This phenomenon can adversely affect the performance of frequency generation circuits due to power supply coupling. Consequently, power supply noise has become as a limiting factor in the overall noise performance of RF components [89], particularly given the switching activities of digital circuitry operating at frequencies ranging from 10 MHz to 100 MHz [20]. For examples, authors in [90] have observed that supply noise has the most significant influence on the phase noise of an LC oscillator in terms of deterministic noise.

Traditionally, in such applications, a LDO is commonly integrated on-chip to provide a precise and stable power supply. Additionally, it separates the power domains to optimize the overall phase noise performance, due to its capability to offer adequate power supply rejection ratio (PSRR). Fig. 4.1 illustrates the utilization of an LDO to separate the power domains of the sub-blocks within an ADPLL, which aids in spur reduction in the output spectrum. On the other hand, modern communication systems impose even stricter specifications on the phase-noise performance of the LO. As VCO or DCO is the dominant contributor to out-of-band noise in a PLL system, the noise contributors in such oscillator have recently garnered significant attention.

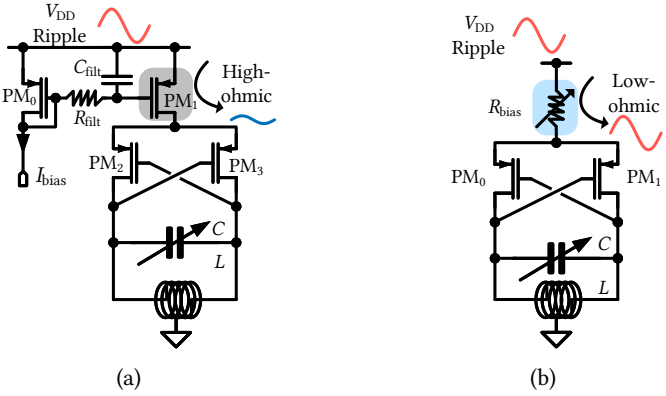


Figure 4.2: (a) The schematic and (b) the simulated ΔC and quality factor of resistor-biased SC over the resistance.

As discussed in chapter 3.3.1, there is a trade-off in selecting the tail current bias architecture in designing the LC oscillator. Fig. 4.2(a) briefly revisits the design of an oscillator biased by a current source, where the current source offers an effective isolation from the power supply, consequently ensuring

a decent PSR. However, since oscillation amplitude is highly correlated to the tail current, the noise generated by the current source PM_1 has the most significant influence on the phase noise of the oscillator.

On the other hand, Fig. 4.2(b) illustrates an alternative architecture employing a low-ohmic switchable poly-resistor [76] or a transistor operating in the linear region [16] for biasing. This configuration eliminates the current source, which is one of the primary sources of flicker noise. However, these low-ohmic bias schemes offer poor PSR because supply noise can more easily intrude the cross-coupled transistors, leading to a degradation in the oscillator's phase noise performance. Fig. 4.3 presents simulated phase noise sources of a well-optimized LC oscillator biased with a low-ohmic tail, demonstrating that despite employing a LNLDO, the V_{DD} noise remains at around 20%.

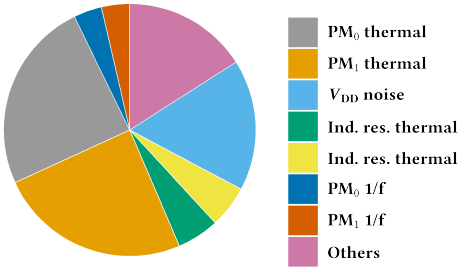


Figure 4.3: Simulated major phase noise contributors in a well-designed tail voltage-biased LC oscillator.

Moreover, as the trend shifts towards all-digital or digitally assisted RF circuits in modern RF-SoCs, particularly in advanced technology nodes, voltage bias is increasingly favored over current bias in high-precision circuits like TDC due to its greater robustness against the PVT variation. Consequently, the low-noise performance of the power supply becomes crucial to ensure the optimal operation of these sensitive blocks. To accommodate the use of these low-ohmic bias schemes, the integration of a low-noise low-dropout regulator (LNLDO) is gaining high interest among RFIC designers. Furthermore, to address the need for reduced PCB area and enhanced portability, meeting the demands for high integration and compact size, a capacitor-less LDO structure holds significant value.

In this chapter, starting from the basics of LDO, the impact of the power supply on the phase noise of the frequency generation circuit is reviewed. Subsequently, a LNLDO implemented in a 28 nm technology is introduced. This LNLDO design was utilized in all three fabricated chips relevant to this thesis work.

4.1 Fundamentals of Low-Dropout Regulator

Fig. 4.4 illustrates the structure of a conventional LDO. When the LDO is stable, i.e. the OTA together with the pass transistor PM_0 is in a negative feedback configuration, the current flowing through the tunable resistor R_1 is expressed as:

$$I_{R_1} = \frac{V_{BG}}{R_1} \tag{4.1}$$

Therefore, the output voltage of the LDO is written as:

$$V_{out} = I_{R1} \cdot (R_0 + R_1) = V_{BG} \cdot \left(1 + \frac{R_0}{R_1}\right) \tag{4.2}$$

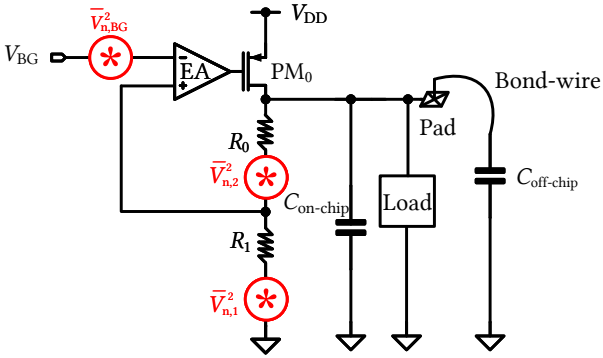


Figure 4.4: Schematic of a traditional LDO including noise sources.

The power supply ripple rejection is expressed as:

$$PSRR = \frac{\Delta V_{in}}{\Delta V_{out}} \tag{4.3}$$

At low frequency, the PSRR is highly influenced by the gain of the error amplifier (EA) A_{EA}, which can be written as

$$\frac{\Delta V_{\mathrm{in}}}{\Delta V_{\mathrm{out}}} \approx \frac{A_{\mathrm{EA}}}{\left(1+\frac{R_0}{R_1}\right)} \tag{4.4}$$

Eq. 4.4 indicates that a large A_{EA} can lead to a better PSRR, which is beneficial for a noise-critical application such as LC oscillators. In addition, for such application, the output noise of the LDO is also a very important performance metric, which can be expressed as

$$\overline{V_{\mathrm{n,out}}^2} = \left(1+\frac{R_0}{R_1}\right)^2 \left(\overline{V_{\mathrm{n,EA}}^2} + \overline{V_{\mathrm{n,BG}}^2} + \overline{V_{\mathrm{n,1}}^2} + \overline{V_{\mathrm{n,2}}^2} + \frac{\overline{V_{\mathrm{n,PM0}}^2}}{A_{\mathrm{EA}}^2}\right) \tag{4.5}$$

where $\overline{V_{\mathrm{n,EA}}^2}$ is the input-referred noise of the EA, $\overline{V_{\mathrm{n,BG}}^2}$ represents the noise of the bandgap reference, $V_{\mathrm{n,PM0}}$ stands for the noise of the pass transistor PM_0, $\overline{V_{\mathrm{n,1}}^2}$ and $\overline{V_{\mathrm{n,1}}^2}$ are the thermal noise induced by the resistive divider. Due to the high voltage gain of the EA, the noise from the pass device in an LDO is usually negligible [87]. The conventional LDO has an obvious disadvantage as the bandgap reference and the resistive divider contribute a significant part to the output noise of the LDO. In order to mitigate this, a two-stage low-noise LDO structure is introduced.

4.2 Low-Noise Linear Regulator

Eq. 4.5 indicates that the noise originating from the bandgap reference significantly contributes to the overall noise of the LDO. One common approach to mitigate this noise is by employing a low-pass filter (LPF) at the V_{BG}, as demonstrated in [91]. However, the thermal noise of the resistive feedback network R_0 and R_1 also degrades the noise performance of the LDO. Hence, a low-noise low-dropout regulator (LNLDO) is proposed to address these challenges by introducing a second feedback loop, as depicted in Fig. 4.5 [20, 92–94].

In comparison to the traditional architecture, this configuration incorporates not only the bandgap reference but also the resistive feedback before the LPF. By designing the LPF to have a very low cut-off frequency, the regulation loop becomes immune to the noises of V_{BG}, R_0, and R_1. Consequently, the EA

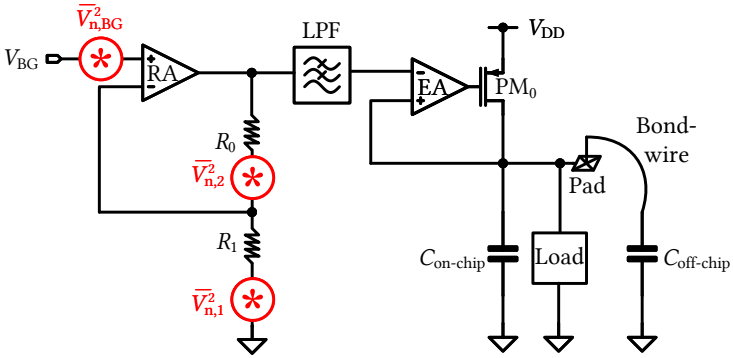


Figure 4.5: Structure of a low-noise LDO.

becomes the sole contributor to the output noise of LDO as the noise of pass transistor PM_0 is attenuated by the large gain of the EA. The introduced secondary amplifier, denoted as reference amplifier (RA), forms a non-inverting operational amplifier configuration with R_0 and R_1, thereby producing a output voltage $V_{BG}\left(1+\frac{R_0}{R_1}\right)$. The output voltage of the LNLDO tracks this reference voltage. In the subsequent sections, a detailed LNLDO implemented in a 28 nm CMOS is presented. Although the architecture bears resemblance to state-of-the-art LNLDO designs reported in [92–94], the proposed design incorporates a on-chip impedance scaler. This feature enables the LNLDO to operate without the need for an external capacitor, exhibiting the advantage of reducing overall system footprint on the printed circuit board (PCB).

4.2.1 Proposed LNLDO with On-chip Impedance Scaler

Fig. 4.6 depicts the top-level schematic of the proposed LNLDO. Contrasted with the LNLDO structure illustrated in Fig. 4.5, the proposed LNLDO incorporates an on-chip capacitance enhancer utilizing the impedance scaler technique introduced in [95] and [96]. This enhancement aims to stabilize the LDO without the assistance of an off-chip capacitor, thereby reducing the overall footprint of the system. The concept of this technique is essentially Miller effect with current amplification. As shown in Fig. 4.6, the current

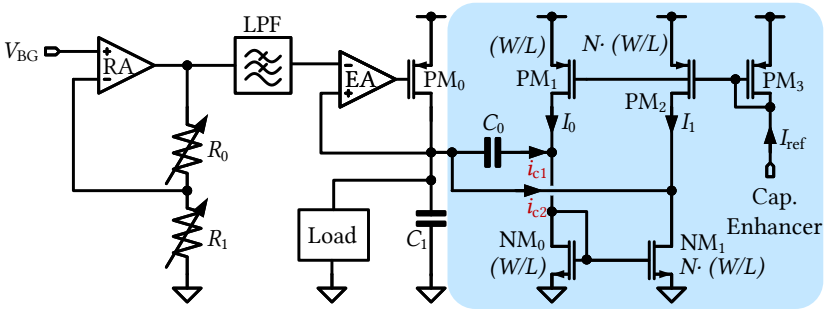


Figure 4.6: Structure of the LNLDO with on-chip capacitance enhancer.

mirror of the capacitance enhancer is sized as

$$\begin{aligned} N \cdot \left(\frac{W}{L}\right)_{PM_1} &= \left(\frac{W}{L}\right)_{PM_2} \\ N \cdot \left(\frac{W}{L}\right)_{NM_0} &= \left(\frac{W}{L}\right)_{NM_1} \end{aligned} \tag{4.6}$$

Thus, the small-signal ac current $i_{c2} = N \cdot i_{c1}$, where i_{c1} and i_{c2} are the ac current flowing in the left and right branches of the capacitor enhancer. The total ac current drawn by the capacitance enhancer is:

$$\begin{aligned} i_{tot} &= i_{c1} + i_{c2} \\ &= (N+1) \times i_{c1} \end{aligned} \tag{4.7}$$

Hence, the impedance seen from the input of the capacitance enhancer is N+1 times smaller than the impedance of the capacitor C_0, i.e. $\frac{1}{sC_0}$. Effectively, the equivalent capacitance of this circuit is:

$$C_{eq} = (N+1) \times C_0 \tag{4.8}$$

By choosing a large current multiplication factor N, the effective capacitance on the LNLDO output can be significantly increased. The capacitance enhancer shifts the dominant pole further to the left, thus aiding in the stability of the LDO. However, this comes at the expense of increased quiescent current consumption.

4.2.2 Output Voltage Level Generator and Low-Pass Filter

Fig. 4.7 depicts the schematic of the circuit responsible for generating output voltage levels, comprising a RA, a resistive divider, and a LPF. The RA is selected as a conventional two-stage operational amplifier employing Miller compensation, chosen for its design simplicity and robustness. The design of the RA has a very relaxed specification on the bandwidth and output noise due to the presence of the LPF. In conjunction with the resistive divider, they establish a non-inverting operational amplifier configuration, facilitating the adjustment of the LDO's output voltage to the desired level.

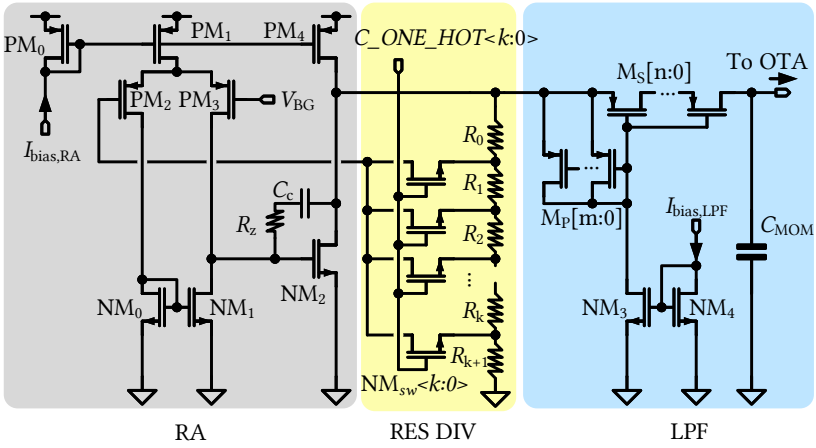


Figure 4.7: Detailed schematic of the LNLDO output voltage level generator and low-pass filter.

The resistive divider, employing k unitary resistors and controlled by a one-hot coded control word $C\_ONE\_HOT[k{:}0]$, ensures monotonic tuning. This tuning method offers an advantage over schemes using switchable resistors, as the output of the RA consistently encounters the highest output load resistance. Thus, the gain of the RA remains unaffected by fluctuations in load resistance. Suppose the i-th transistor in NM_{sw} is activated; the output voltage of the divider can be expressed as:

$$\begin{aligned} V_{out} &= V_{BG} \times \frac{k \cdot R}{(k-i) \cdot R} \\ &= V_{BG} \times \frac{k}{(k-i)} \end{aligned} \tag{4.9}$$

Although theoretically, the output voltage remains independent of the resistance value, ensuring sufficient impedance at the output of the RA is essential due to its lack of an output stage. Consequently, the resistor ladder incorporates unit high-R poly-resistors typically ranging in several kilo-ohms.

To filter out noise from the bandgap reference voltage V_{BG}, the RA and the thermal noise of the resistive divider, a LPF filter is employed. The filter is essentially a *RC* filter where the *R* is implemented by *n* PMOS transistor $M_S[n:0]$ connected in series. The gate bias voltage is established by a reference current of 10 nA. This current is directed out of the *m* diode-connected transistors $M_P[m:0]$ in parallel, thereby generating a bias voltage closely matching their source voltage. Consequently, $M_S[n:0]$ operates in deep sub-threshold region, exhibiting a very resistance typically in the giga-ohm range.

To construct the RC filter with the active resistor, a fringe capacitor C_{MOM} with a capacitance of several tens of picofarads is employed. Despite offering higher capacitance density, thin-oxide MOS capacitors should be avoided in a nano-scale technology to prevent significant voltage drop resulting from gate leakage current at this high-impedance node. With this proposed configuration, the filter achieves an exceptionally low cut-off frequency of below 10 Hz. It is noteworthy that the precise value of the cut-off frequency of the filter is not critical, as long as it remains sufficiently low to effectively filter out noise.

4.2.3 Error Amplifier

Shown in Fig. 4.5, because the EA is at the stage after the LPF, its performance has a significant impact on the overall noise performance of the LNLDO. As analyzed in Eq. 4.4 and 4.5, a higher DC gain of the EA is preferred as it can enhance LDO's PSRR and attenuate the noise contribution of the pass device. Accordingly, a folded-cascode operational transconductance amplifier (OTA) is chosen to serve as the the EA in this LNLDO, with its schematic illustrated in Fig. 4.8. The cascode current sources feature a self-biased structure, offering advantages such as increased voltage overhead and design simplicity.

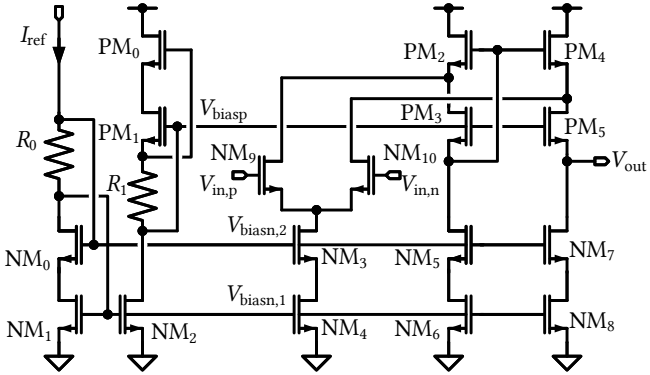


Figure 4.8: Schematic of the LNLDO folded-cascode error amplifier with self biasing.

The noise of the EA can be expressed as

$$\begin{aligned}\overline{V^2_{\mathrm{n,EA}}} = \frac{16k_{\mathrm{B}}T}{3}\left(\frac{1}{g_{m,\mathrm{NM9,10}}} + \frac{g_{\mathrm{m,PM2,4}}}{g^2_{\mathrm{m,NM9,10}}} + \frac{g_{\mathrm{m,NM6,8}}}{g_{\mathrm{m,NM9,10}}}\right) \\ + \frac{2K_{\mathrm{N}}}{C_{\mathrm{ox}}f}\left(\frac{1}{(WL)_{\mathrm{NM9,10}}} + \frac{1}{(WL)_{\mathrm{NM6,8}}}\frac{g^2_{\mathrm{m,NM6,8}}}{g^2_{\mathrm{m,NM9,10}}}\right) \\ + \frac{2K_{\mathrm{P}}}{C_{\mathrm{ox}}f}\left(\frac{1}{(WL)_{\mathrm{PM2,4}}}\frac{g^2_{\mathrm{m,PM2,4}}}{g^2_{\mathrm{m,NM9,10}}}\right)\end{aligned} \tag{4.10}$$

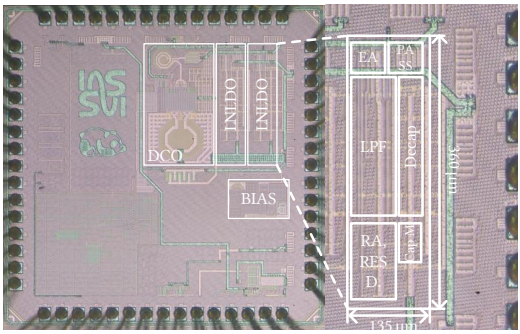
Here, the first term represents thermal noise, while the second and third terms denote the flicker noises of the n-type and p-type devices, respectively. Negligible noise contributions are assumed from the cascode transistors $NM_{5,7}$ and $PM_{3,5}$, as well as the current source of the differential pair $NM_{3,4}$, in the folded-cascode amplifier [97].

Eq. 4.10 indicates that to minimize the output noise of the folded-cascode EA, maximizing the g_{m} of the differential stage is essential. Additionally, it suggests that the g_{m} of the cascode current stage should be kept small with the same bias current, while increasing the area of these devices to reduce their flicker noise. Furthermore, the EA is designed with a relatively narrow bandwidth of 10 kHz in order not to integrate additional thermal noise. The EA achieves a DC gain of more than 60 dB in the typical-typical corner.

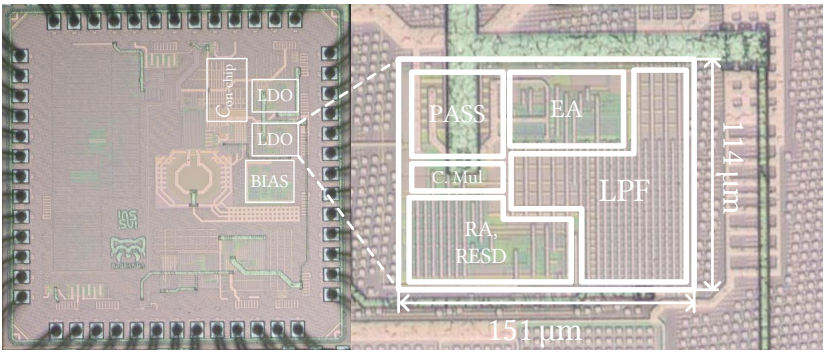
Given that the negative input of the EA directly connects to the output of the LPF, which is characterized by very high impedance, thick-oxide devices are employed for the input differential pair to prevent voltage drop due to gate leakage.

4.3 Experimental Results

The proposed LNLDO was fabricated using a 28 nm CMOS technology. Fig. 4.9 displays two versions of the chip micrographs of the LNLDO utilized in the *PANDA* and *RedPanda* projects, respectively. In comparison to the



(a)



(b)

Figure 4.9: Chip micrographs of the LNLDO prototypes with (a) class-B DCO and (b) class-C DCO.

initial version depicted in Fig. 4.9(a), the revised version shown in Fig. 4.9(b) occupies a much denser area of only 0.017 mm^2. The quiescent current of the LNLDO is 817.4 μA.

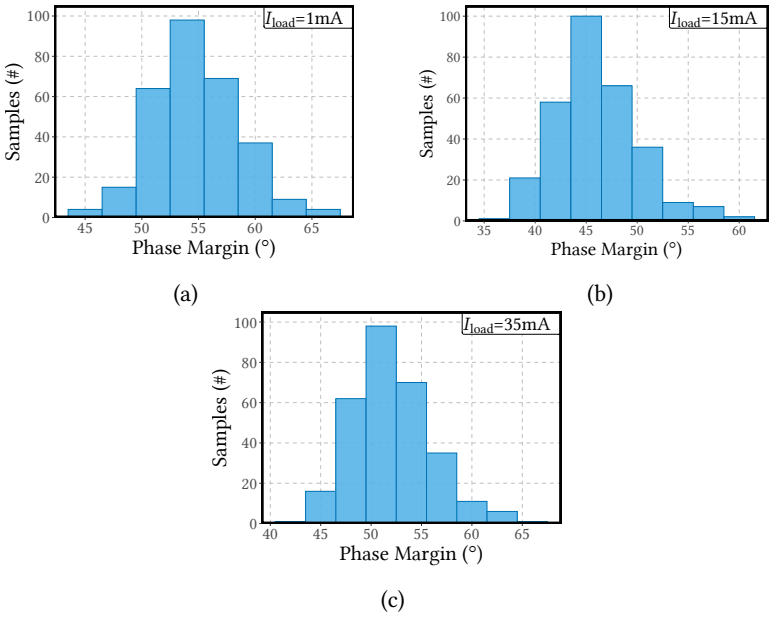


Figure 4.10: Global and local mismatch of the phase margin of OTA-PM$_0$ loop based on simulation using schematic. (a) I_{load}=1 mA. (b) I_{load}=15 mA. (c) I_{load}=35 mA.

The input voltage supplied to the LNLDO is 1.5 V and is obtained from an external power supply. The LNLDO is designed to provide the DCO with an output voltage ranging from 1.2 to 1.3 V, with a current consumption of up to 35 mA. Additionally, it supplies the crystal oscillator and the TDC with a voltage of 0.9 V.

Although successful silicon functionality of the LNLDO has been implicitly proven through DCO and crystal oscillator measurements, due to limitation of access to internal signals and measurement techniques, the assessment of performance of the LNLDO such as PSRR, stability, and output noise is based on simulated results with the extracted layout.

Fig. 4.10 presents the stability characteristics of the EA-PM$_0$ loop in the proposed LNLDO, as determined through Monte-Carlo analysis incorporating

both local and global mismatches. The analysis includes 300 samples across various load current values. The result shows the phase margin of the LNLDO remains above 35° over Monte-Carlo, demonstrating the effectiveness of the capacitance enhancer [17].

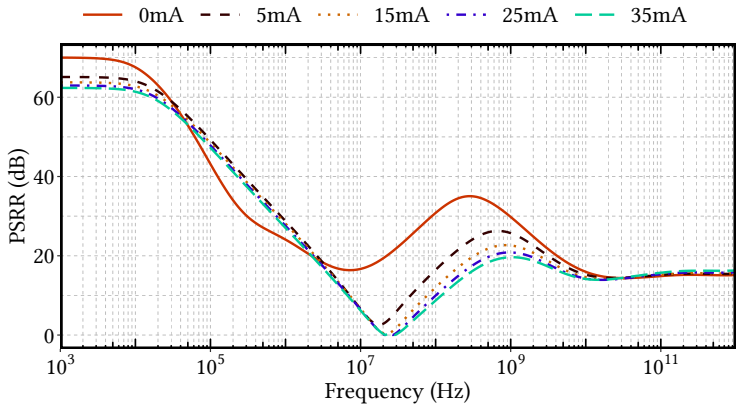


Figure 4.11: Post-layout simulated PSRR with different load current values.

Fig. 4.11 illustrates the simulated PSRR of the proposed LNLDO with the extracted layout. The simulation was conducted with varying load currents and an output voltage of 1.2 V. The proposed LNLDO achieves a PSRR at low frequencies ranging from 63 dB to 70 dB, with the minimum PSRR of the LNLDO remaining above 0 dB across all frequencies.

Notably, for the case when load current is 0 mA, the PSRR is improved at both DC and at frequencies in the several mega-hertz range. This improvement is attributed to the pass device PM_0 being able to operate in saturation due to the relatively small load current, which is only the quiescent current due to the capacitance enhancer, resulting in a increased loop gain. In a potential revision, further enhancement of the LNLDO's PSRR could be achieved by increasing the W/L ratio at the expense of increased area. The effectiveness of the on-chip capacitance enhancer can also be seen from Fig. 4.11, showing its contribution to the PSRR across frequencies spanning approximately from 10 MHz to 1 GHz.

The simulated startup behavior for output voltages of 1.2 V and 0.9 V of the proposed LNLDO, utilizing the extracted layout, is depicted in Fig. 4.12. The presence of a large time constant due to the LPF results in an excessive startup time. To accelerate the startup process, the LPF is temporarily disabled

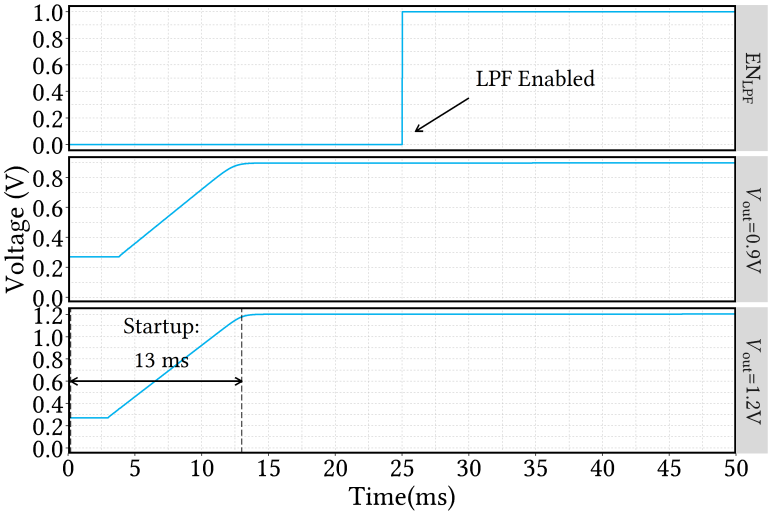


Figure 4.12: Post-layout simulated LNLDO startup behavior.

during the startup phase and subsequently re-enabled after setting the output voltage. The outcome demonstrates that the LNLDO achieves a startup time of 13 ms for an output voltage of 1.2 V. Following the startup phase, the LPF can be activated for low-noise applications.

Table 4.1 demonstrates the output noise performance simulated with the extracted layout of the proposed LNLDO at an output voltage of 1.2 V and various load currents. The root mean square (RMS) noise from 10 Hz to 100 kHz remains below 18 μV across all load scenarios. Specifically, for the typical use case in RFIC applications such as the DCO with a current consumption ranging from 5 mA to 35 mA, the LNLDO achieves an RMS noise level below 15 μV.

Fig. 4.13 illustrates the measured output voltage tuning range of the proposed LNLDO. The LNLDO is capable of delivering a power supply ranging from 0.73V to 1.71V, demonstrating its ability to meet various supply voltage level specifications.

To assess the impact of the LNLDO on silicon, the output spectrum of the DCO is measured and depicted in Fig. 4.14. A comparison is made between the noisy DCO output supplied by an external V_{DD}, i.e. Keysight N6705B [83],

Table 4.1
Post-layout Simulated LNLDO Output Noise.

	Output Noise with Different Load Current ($nV/\sqrt{Hz}$)				
Frequency (MHz)	0	5 mA	15 mA	25 mA	35 mA
0.01	53.01	51.65	51.6	51.59	51.59
0.1	51.91	21.35	21.32	21.31	21.31
1	84.34	14.11	13.77	13.83	13.8
40	2.561	4.366	5.944	6.553	6.614
100	0.735	1.21	1.654	1.886	2.008
V_{RMS} (μV) 10 Hz – 100 kHz	17.67	14.79	14.77	14.77	14.77

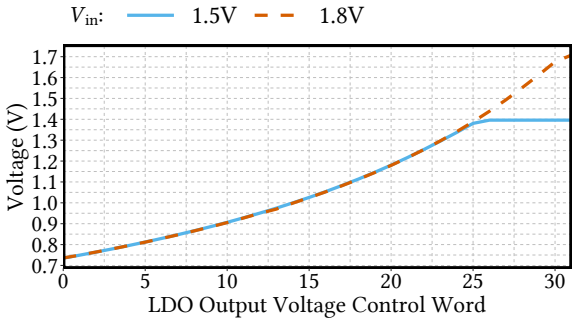


Figure 4.13: Measured output voltage tunning range.

shown in Fig. 4.14(b), and the spectrum with the LNLDO, illustrated in Fig. 4.14(a), which exhibits a significantly cleaner spectrum.

Table 4.2 presents a summary of the performance comparison between the LNLDO and state-of-the-art designs. The quiescent current of the proposed LNLDO is 817.4 μA, primarily attributed to the on-chip capacitor enhancer. This current is largely due to the substantial sizing of the current mirror, necessary for effectively substituting an external capacitor typically in the range of several hundred nano-farads.

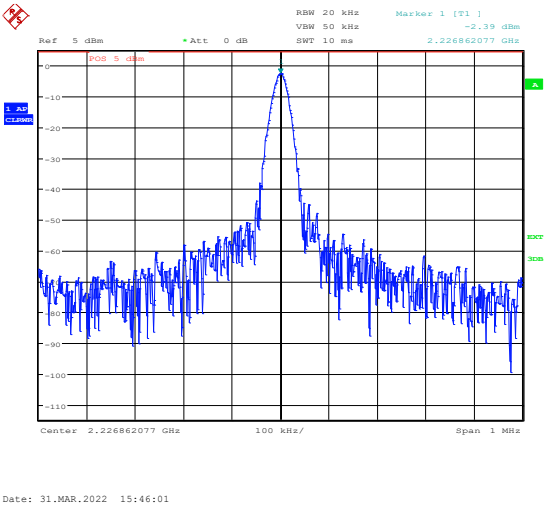
In comparison to reported LNLDO designs that can supply large load currents exceeding 35 mA using larger technology nodes, the proposed LNLDO

Table 4.2
Low-noise LDO performance comparison.

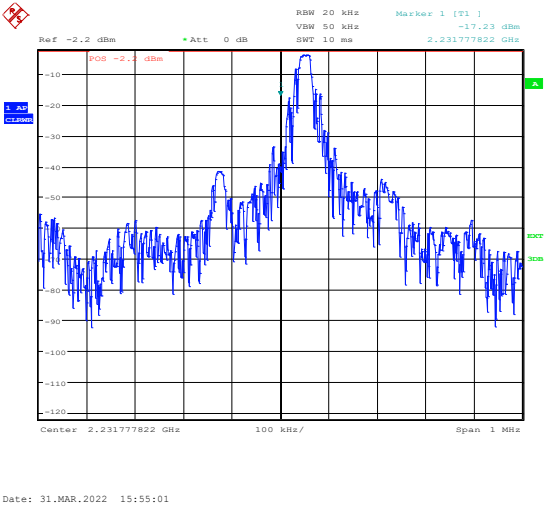
Parameter	[92]	[93]	[94]	This work
Technology	N.A.	350 nm	180 nm	28 nm
V_{BG}	1.2 V	N.A.	N.A.	0.6 V
V_{IN}	N.A.	3.6 V	0.9 - 1.8V	1.5 - 1.8 V
V_{OUT}	2.8 V	2.8 V	0.65 - 1.5 V	0.73 - 1.71 V
Max. I_{load}	100 mA	100 mA	150 mA	35 mA
VN_{RMS}* (μV)	6.6	21.2**	17	17.67
Quiescent current	25 μA	N.A.	24 μA	817.4 μA
Off-chip capacitor	Yes	1 μF	N.A.	No
Area	N.A.	N.A.	0.14 mm^2	0.017 mm^2

*RMS value calculated in range 10 Hz to 100 kHz
** Value measured from 10 kHz to 100 kHz

is optimized for applications requiring load currents typically below 35 mA in 28 nm CMOS, while maintaining a smaller chip footprint. Despite this limitation, the proposed design demonstrates comparable noise performance and offers the unique advantage of operating in a capacitor-less configuration, making it well-suited for targeted applications where these features are prioritized.



(a)



(b)

Figure 4.14: Measured DCO output signal spectrum(a) with the LNLDO and (b) with an external clean power supply.

CHAPTER 5

CRYSTAL OSCILLATOR WITH START-UP ACCELERATION

Crystal oscillators are oscillators that utilize a quartz crystal instead of an LC resonate tank. They offer several advantages over LC tank oscillators, especially in RF applications like frequency synthesis within PLL systems. One key advantage is their exceptional stability, which is crucial for maintaining precise frequency generation. Quartz crystals can also be cut at specific angles to achieve very low temperature coefficients, enhancing frequency stability over varying environmental conditions. Moreover, quartz crystals exhibit an extremely high quality factor, typically in the order of 10^6 [29], providing superior frequency selectivity and minimizing phase noise.

In frequency synthesizers, the crystal oscillator acts as the reference clock, meeting stringent in-band phase noise requirements essential for modern PLL systems used in communication applications. However, evolving communication systems demand advanced crystal oscillator designs, particularly in nano-scale CMOS technologies.

Reducing the start-up time of crystal oscillators is critical for improving overall system response times. This start-up time significantly impacts communication system performance. Additionally, as technology nodes shrink, optimizing the noise performance of crystal oscillators becomes increasingly challenging due to elevated noise levels inherent in MOS devices.

This chapter introduces a low-noise crystal oscillator designed specifically for 28 nm CMOS technology. The discussion begins with an electrical model incorporating a quartz crystal, followed by an exploration of different crystal oscillator topologies. Techniques to accelerate oscillator start-up are then detailed, addressing crucial aspects of crystal oscillator design in the context of advanced CMOS technologies.

5.1 Modeling of the Quartz Crystal

Common electrical parameters of a quartz crystal include output frequency f_0, frequency calibration, shunt capacitance C_0 and load capacitance C_L. The specific parameters for the 54 MHz quartz crystal utilized in this application are detailed in Table 5.1.

Table 5.1
Typical parameters of a 54 MHz quartz crystal.

Parameter	Symbol	min.	nom.	max.	Unit
Resonate freq.	f_0		54		MHz
Freq. calibration		-15		15	ppm
Shunt capacitance	C_0			2	pF
Load capacitance	C_L		8		pF
ESR			40		Ω

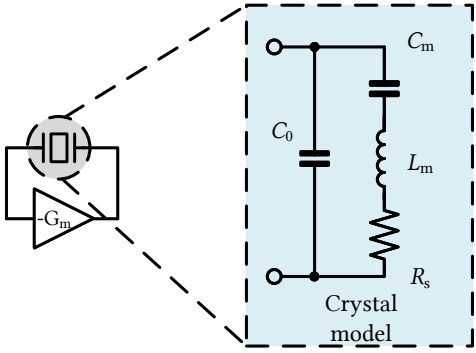


Figure 5.1: Equivalent circuit of a quartz crystal.

To facilitate the design process of a crystal oscillator within a circuit design environment, an equivalent model of the quartz crystal is essential. Typically, an LCR model as depicted in Fig. 5.1 is employed for this purpose. This model includes C_0, representing parallel capacitance between the crystal's electrodes due to interconnect. Additionally, L_m and C_m represent the motional inductance and capacitance, respectively. The resistance R_s is associated with the loss of energy during the transition between kinetic and electrical energy. The value of R_s can be calculated from the crystal's equivalent series resistance

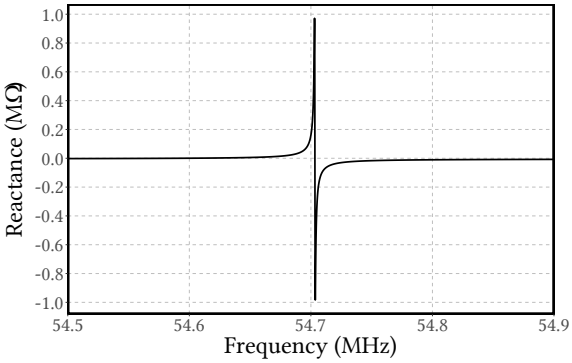


Figure 5.2: Simulated reactance of the equivalent circuit of the crystal.

(ESR) using the formula:

$$R_s = \frac{ESR}{\left(1 + \frac{C_0}{C_L}\right)^2} \tag{5.1}$$

The motional capacitance C_m and inductance L_m are obtained using the series resonate frequency

$$f_s = \frac{1}{2\pi\sqrt{L_m C_m}} \tag{5.2}$$

The quality factor Q of the crystal model can then be expressed by:

$$Q = \frac{\sqrt{\frac{L_m}{C_m}}}{R_s} \tag{5.3}$$

The parallel resonate frequency can be calculated as:

$$f_p = \frac{1}{2\pi\sqrt{L_m \frac{C_m(C_0+C_L)}{C_m+C_0+C_L}}} \tag{5.4}$$

In practical scenarios, the value of C_0 is much larger than C_m, resulting in f_s and f_p being approximately equal. Table. 5.2 presents the model parameter of the quartz crystal used in this work, and Fig. 5.2 illustrates the simulated reactance of the crystal over frequency.

Table 5.2
Model parameters of the used quartz crystal.

	C_m	L_m	R_S	C_0
Value	2.5 fF	3.4 mH	12 Ω	600 fF

5.2 Oscillator Architecture

Despite the high quality factor of quartz crystals, there is inherent energy loss R_S that prevents oscillation from sustaining indefinitely without compensation. Therefore, the oscillator requires active components to counteract this energy loss and maintain oscillation. Two widely recognized crystal oscillator topologies that effectively address this requirement are the Colpitts and Pierce configurations.

5.2.1 Pierce Oscillator

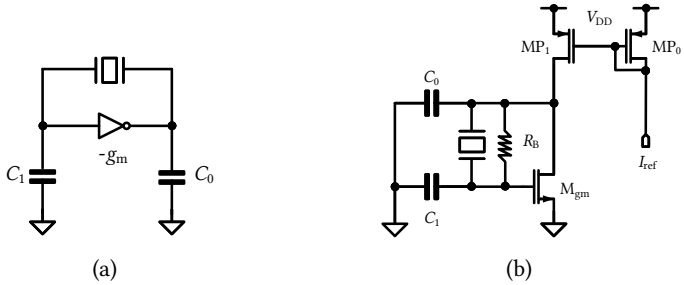


Figure 5.3: Pierce crystal oscillator. (a) General configuration. (b) A detailed schematic.

Fig. 5.3(a) illustrates the general configuration a Pierce crystal oscillator. The g_m-stage within this oscillator provides gain with a −180° phase shift. A more detailed schematic of a possible implementation of a Pierce crystal oscillator in shown in Fig. 5.3(b), employing an NMOS g_m transistor supplied by a current source. A large resistor R_B is utilized to bias the DC level of M_{gm}.

The Pierce crystal oscillator offers simplicity in design and excellent stability. This configuration can achieve a large output swing, leading to favorable

phase noise performance. However, to sustain oscillation, the g_m stage of the Pierce oscillator must deliver substantial gain, necessitating a significant current draw from the power supply. This characteristic makes the Pierce oscillator less suitable for ultra-low power applications.

5.2.2 Colpitts Oscillator

Another commonly used architecture, particularly for low-power crystal oscillators, is the Colpitts oscillator, as depicted in the general configuration shown in Fig. 5.4(a). In comparison to the Pierce oscillator, the Colpitts oscillator exhibits significantly lower current consumption because the g_m stage does not need to provide as high a gain and can therefore be biased out of the linear region. Fig. 5.4(b) illustrates a potential implementation of the Colpitts crystal oscillator, where C_0 and C_1 form a capacitive divider to provide the necessary feedback.

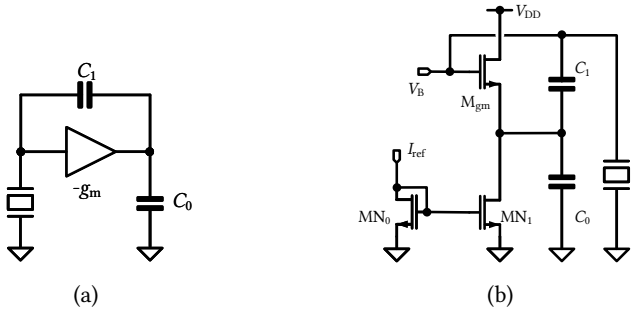


Figure 5.4: Colpitts crystal oscillator. (a) General configuration. (b) A detailed schematic.

Recently published Colpitts crystal oscillator designs, such as those discussed in [98], have achieved power consumption below 10 μW by configuring the g_m stage in the weak-inversion region. However, the Colpitts oscillator poses challenges in achieving good phase noise performance, requiring more intricate design efforts. Additionally, sustaining oscillation in the Colpitts oscillator demands strict device selection for components like C_0 and C_1. Consequently, the capacitive divider is typically integrated into the chip, leading to increased area overhead. In contrast, the load capacitors in Pierce oscillators are typically placed on the PCB, reducing chip area requirements.

5.3 Start-up Acceleration

Due to the low-power requirements of modern wireless communication systems, it is advantageous to operate the transceiver by toggling between active and standby modes. The transceiver is activated only when signal transmission is required, as it consumes significant power. In standby mode, most analog blocks are powered down to minimize energy usage. Consequently, the transceiver's wake-up time critically impacts the system's overall response time. Typical analog blocks—such as the PLL and LDO—exhibit start-up times on the order of 10 μs [44, 99]. However, the crystal oscillator's spontaneous start-up time, limited by its extremely high quality factor, typically exceeds 1 ms, creating a bottleneck for the communication system.

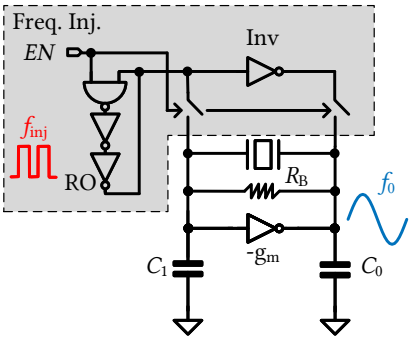


Figure 5.5: Pierce crystal oscillator with constant frequency signal injection.

In order to accelerate the crystal oscillator startup, researchers introduced the signal injection techniques to insert energy into the quartz crystal. For example, authors in [100] and [101] utilize a constant-frequency injection technique to reduce the startup time. Fig. 5.5 illustrates the general concept of this technique, where a ring oscillator (RO) generates a signal with frequency f_{inj} that is then applied to the electrodes of the crystal. This technique has been reported to be effective but only under the condition that f_{inj} matches the resonate frequency of the crystal f_0. However, this requires an accurate and dynamic calibration to compensate the strong frequency drift of a ring oscillator due to temperature and supply voltage variation. To tackle this difficulty, two more sophisticated signal injection schemes, i.e. chirp signal injection and dithered signal injection, have been introduced in recent works.

5.3.1 Chirp Signal Injection

The chirp signal injection (CI) method was originally proposed by authors in [99], as illustrated in Fig. 5.6. Unlike constant frequency signal injection, this method employs a VCO to generate the injection signal, as depicted in Fig. 5.6(a). A ramp voltage signal is then used to drive the VCO, resulting in a signal with a continuously increasing frequency over time, known as a chirp signal. Designers need only to ensure that the tuning range of the VCO encompasses the resonance frequency of the crystal f_0. As f_{inj} is swept continuously, there comes a point in time where f_{inj} precisely matches f_0, allowing energy to be effectively transferred into the crystal. Fig. 5.6(b) illustrates the waveform of the chirp frequency injection.

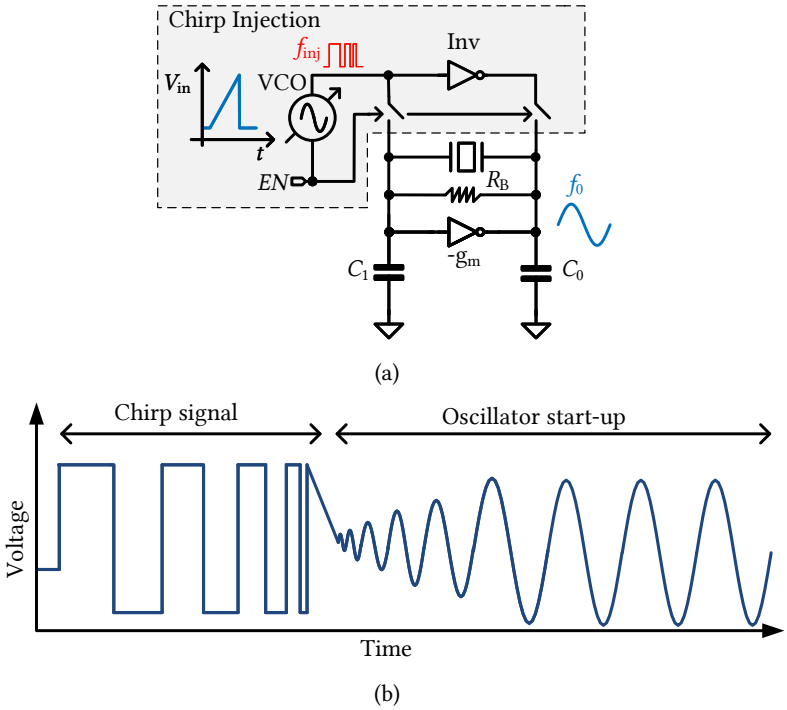


Figure 5.6: (a) General schematic and (b) startup waveform of a Pierce crystal oscillator with Chirp signal injection.

Despite its simplicity, the CI method has certain drawbacks. Much of the power consumed by the VCO is not effectively transferred into the crystal

due to the short duration f_{inj} matches f_0. This inefficiency leads to wasted energy and limited start-up acceleration in comparison to other more sophisticated injection methods. Additionally, in nano-scaled technologies where capacitance and resistance values exhibit large process variations, the VCO must either be calibratable or cover a wide tuning range, increasing startup power consumption.

5.3.2 Dithered Signal Injection

The authors described in [102] a method for startup acceleration utilizing dithered signal injection (DI). As depicted in Fig. 5.7, a DCO is utilized to generate the signal. The tuning range of the DCO needs to encompass f_0. A FCW generation module produces a signal oscillating between the maximum and minimum FCW values. By adjusting the duty cycle of this signal, the frequency of the injected signal can be finely controlled, enabling higher resolution frequency adjustment. Consequently, more energy is introduced into the crystal, facilitating faster startup.

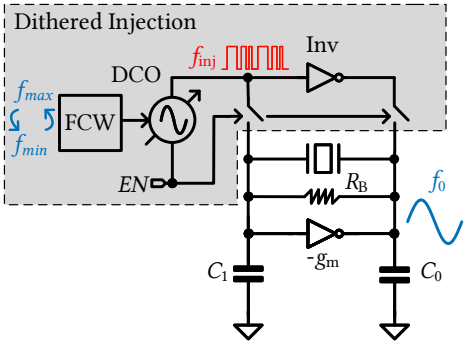


Figure 5.7: General concept of the dithered frequency signal injection.

Authors of [103] advanced the approach by shaping the frequency distribution of the injected signal into a Gaussian profile to minimize the Δf between f_{inj} and f_0. Meanwhile, research detailed in [104] proposed more complex methods aimed at not only reducing Δf but also precisely controlling the period of the injection signal to further accelerate startup.

In subsequent sections, two crystal oscillators employing chirp and dithered injection techniques are presented. The oscillators are implemented using a 28 nm CMOS technology and achieve a phase noise of −133 dBc/Hz at an

offset of 1 kHz from the 54.6 MHz oscillation frequency. The first oscillator employs a simple yet effective ramp-current generation method for chirp injection, achieving a startup time of 300 μs as reported in [18]. The second oscillator, featuring dithered frequency injection, follows a similar design principle to that described in [103] but in a significantly smaller technology node. By combining frequency injection with negative resistance boost, this oscillator achieves a startup time of 30 μs.

5.4 Design Prototypes

5.4.1 Pierce Crystal Oscillator with Chirp Injection

The overview of the proposed crystal oscillator featuring chirp injection is depicted in Fig. 5.8. This oscillator utilizes a Pierce oscillator architecture, with a single transistor M_{gm} supplying the negative resistance. The transistors MP_0 and MP_1 function as a current mirror to bias the Pierce oscillator and enhance the PSR. MP_1 is specifically designed as a thick-oxide, long-channel device to

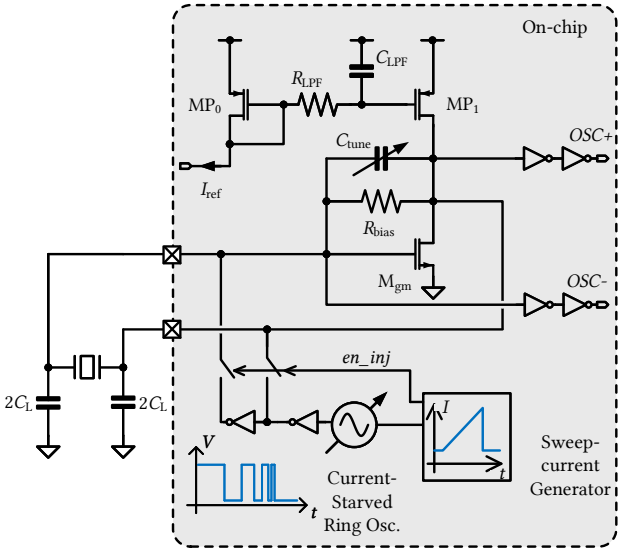


Figure 5.8: Top-level schematic of the proposed Pierce crystal oscillator with chirp signal injection.

minimize short-channel effects and further boost the PSR. Additionally, the width of MP_1 is optimized to ensure sufficient voltage headroom for optimal phase noise performance, benefiting from reduced flicker noise due to the larger transistor area.

To mitigate the influence of reference current noise, a LPF is integrated. This LPF comprises an active resistor, i.e. a transistor biased in the deep sub-threshold region, and an integrated fringe capacitor of 12 pF. It is important to note that a MOS capacitor is avoided due to the gate leakage current issues in 28 nm CMOS technology, which could compromise the bias voltage level.

Furthermore, the inclusion of C_{tune} enables calibration of the oscillator output frequency within a ±20 ppm range, effectively counteracting PVT variations and enhancing frequency accuracy.

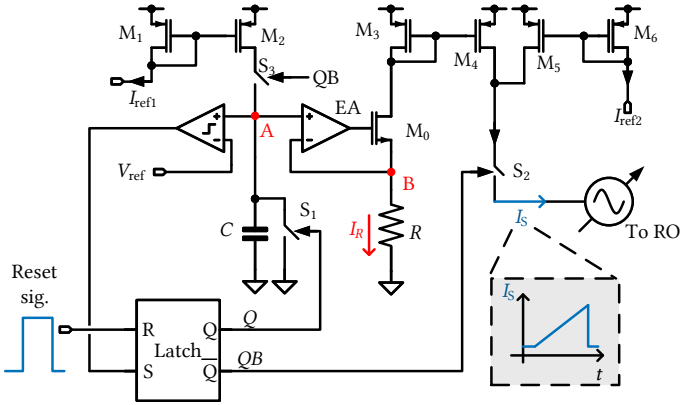


Figure 5.9: Schematic of the sweep-current generator.

The chirp injection circuit comprises a sweep current generator and a current-starved ring oscillator. The schematic of the sweep current generator is depicted in Fig. 5.9, where the entire circuit is biased by two reference currents I_{ref1} and I_{ref2} to transistors M1 and M6, respectively. Initially, at time t_0, the capacitor is discharged with switch S_1 closed.

The start-up sequence of the crystal oscillator is triggered by a 3 μs pulse applied to the reset terminal of an RS latch. When the reset pin of the RS latch is pulled high, the output Q is set to a low level and QB to a high level, opening bypass switch S_1 and closing switches S_2 and S_3. Transistor M2 mirrors the reference current I_{ref1}, charging capacitor C and increasing the

voltage at node A, which can be approximated as:

$$V_A \approx \frac{I_{ref1}}{C}(t - t_0) \tag{5.5}$$

As the error amplifier, EA, and M_0 form a negative feedback loop, the voltage at node B is set to V_A. Consequently, the current through the resistor R can be obtained by:

$$I_R = \frac{V_A}{R} = \frac{I_{ref1}}{RC}(t - t_0) \tag{5.6}$$

This current will then be mirrored by M3 and M4 and then added with I_{ref2}, which is duplicated from M_6 to M_5, resulting in the current I_S that will be fed into the current-starved ring oscillator, whose schematic is illustrated in Fig. 5.10. I_S can hence be expressed as:

$$I_S = I_{ref2} + \frac{I_{ref1}}{RC}(t - t_0) \tag{5.7}$$

For the current-starved RO, its output frequency f_{inj} is proportional to the bias current I_S, and therefore, to the time t.

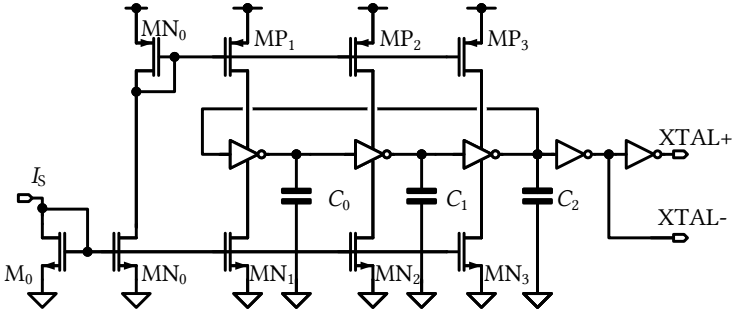


Figure 5.10: Schematic of the current-starved ring oscillator.

Fig. 5.11 shows the simulation result of the oscillation frequency of the CI circuit. As can be observed, the output frequency f_{inj} increases continuously from 30 MHz to 85 MHz, covering the resonate frequency of the quartz crystal f_0.

The simulated phase noise of the crystal oscillator is presented in Fig. 5.12. At the crystal terminals, this oscillator achieves a good phase noise level of −152 dBc/Hz at a 1 kHz offset from the oscillation frequency of 54.6 MHz.

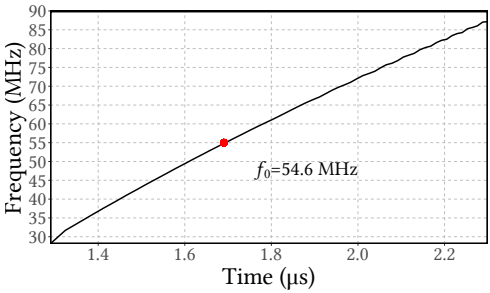
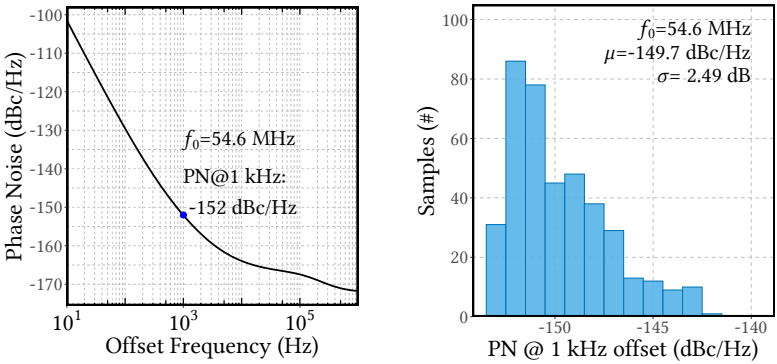


Figure 5.11: Simulated frequency of the current-starved oscillator during injection phase.



(a) (b)

Figure 5.12: Simulated crystal oscillator phase noise (a) at *tt* corner and (b) with global and local mismatch.

Additionally, a Monte-Carlo simulation was conducted to assess the stability and variability of this performance parameter. Fig. 5.12(b) displays the Monte-Carlo simulation result with 400 samples, demonstrating that the crystal oscillator exhibits good stability across variations, as evidenced by a standard deviation of 2.49 dB. This analysis underscores the robustness and reliability of the proposed oscillator design under different operating conditions.

Fig. 5.13 depicts the start-up sequence of the proposed crystal oscillator. The start-up time is defined as the duration from the end of frequency injection until the oscillation amplitude reaches 90% of its maximum value. Initiation

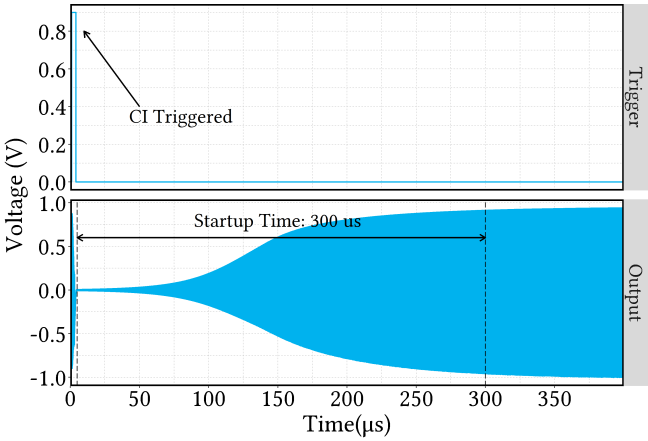


Figure 5.13: Simulated startup acceleration with chirp injection.

is triggered by a 3 μs reset signal. Subsequently, a chirp signal is generated and applied to the oscillator outputs to accelerate start-up. Following this, the reset signal is brought low to terminate the chirp injection. The implemented circuit achieves a start-up time of 300 μs. Simulated start-up energy and static power consumption of the oscillator are 335 nJ and 449.1 μW, respectively.

5.4.2 Crystal Oscillator with Dithered Injection

The top-level schematic of the Pierce crystal oscillator incorporating DI is presented in Fig. 5.14. This oscillator is powered by the same LNLDO regulator detailed in Section 4.3, which serves to enhance PSR and mitigate supply-induced noise.

The oscillator employs a short-channel thin-oxide NMOS transistor (M_{gm}) to provide significant negative resistance for compensating energy losses within the crystal. Transistors MP_0 and MP_1 form a current mirror integrated with a LPF to supply the required current to M_{gm}. A large poly-resistor R_B of 20 kΩ, connected between the gate and drain of M_{gm}, biases this transistor into saturation, thereby facilitating a substantial g_m. The value of R_B should be chosen to be sufficiently large in order to avoid degradation of the overall quality factor of the resonator. However, if R_B is excessively large, it can result in an increased contribution of thermal noise.

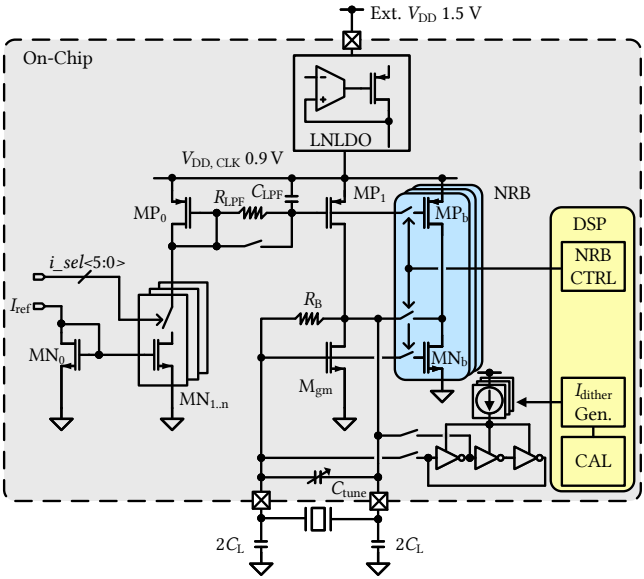


Figure 5.14: Top-level of the proposed Pierce crystal oscillator with shaped dithered injection and negative resistance boost.

$MN_{1..N}$ comprises a digitally controllable array, enabling current trimming on silicon via serial peripheral interface (SPI). Additionally, a tunable capacitor bank C_{tune} is introduced to adjust the oscillator's output frequency within a ±20 ppm range, thereby enhancing the accuracy of transceiver frequency.

Moreover, the proposed crystal oscillator incorporates a negative resistance boost (NRB) function capable of increasing both the bias current and the W/L ratio of M_{gm} during oscillator startup, thereby reducing the startup time.

Gaussian-shaped Dithered Injection

To achieve a more effective start-up acceleration, this work employs a signal injection method featuring a Gaussian-shaped dithered frequency, as originally proposed in [103]. The generation of the DI signal involves a pseudo-random FCW generator and a digitally-controlled ring oscillator (DCRO). The pseudo-random number generator is realized using a linear feedback shift register (LFSR), the configuration of which is illustrated in Fig. 5.15.

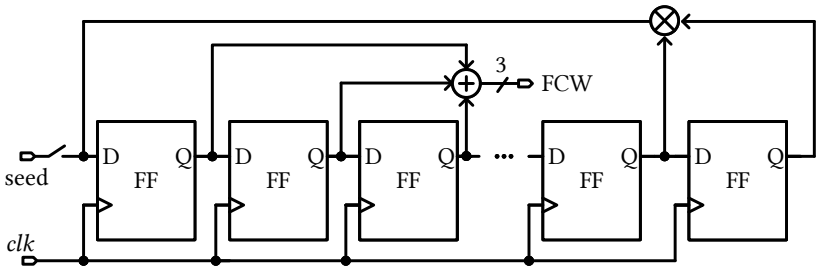


Figure 5.15: Schematic of the Gaussian-shaped pseudo-random control word generator.

The LFSR has a XOR gate with 14^{th} and 15^{th} register values as inputs in the feedback path. The pseudo-random number is generated by the summation of first three consecutive register values. Fig. 5.16 illustrates the output word distribution of the LFSR, where a Gaussian shape can be observed. The DCRO uses the same structure as shown in Fig. 5.10 with digitally controlled MN_0 to change the bias current. The frequency of the injected signal is then a calibrated f_{inj} aim at the resonate frequency of the crystal f_0 with a Gaussian-shaped dither.

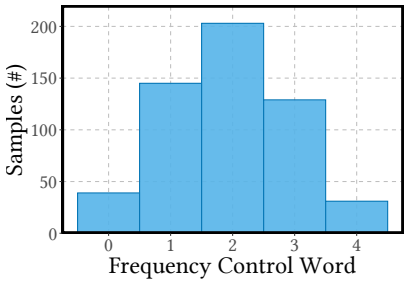


Figure 5.16: Simulated Gaussian-shaped FCW distribution.

Calibration

A factory calibration using a digital frequency-locked loop (DFLL) is designed to calibrate the DCRO with respect to the crystal resonate frequency f_0 as shown in Fig.5.17. The counter based PFD measures the phase error between f_{Inj} and f_0, generating a 10-bit word and then filtered by the digital loop filter

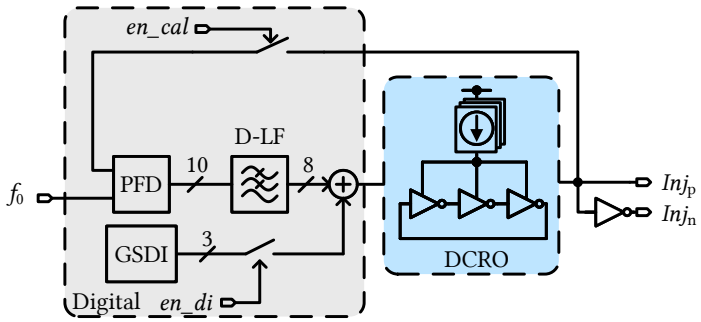


Figure 5.17: Control scheme for the digitally controlled ring oscillator.

(LF), modifying the oscillation frequency of the DCRO. Once the DFLL is locked, f_{Inj} is calibrated to f_0.

The calibration can then be stopped by disabling signal *EN_CAL*. Fig. 5.18 depicts the binary search method of the calibration process. When the DI is enabled, the FCW of the DCRO is a summation of the calibrated value from the DFLL and the Gaussian-shaped pseudo-random word.

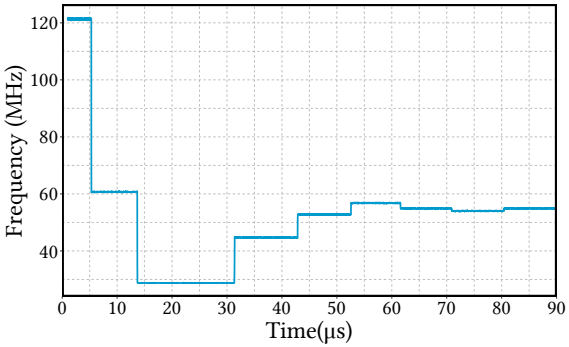


Figure 5.18: Simulated DCRO calibration.

The proposed crystal oscillator is fabricated in a TSMC 28 nm CMOS technology and Fig. 5.19 shows its micrograph. The total area of the clock module is 0.09 mm^2, among which 0.008 mm^2 is the active area of the crystal oscillator. The quartz crystal is an AT-cut crystal in a 3.2 mm×2.5 mm surface mount package.

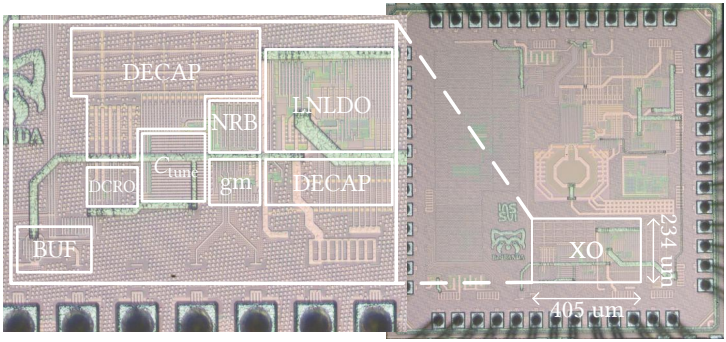


Figure 5.19: Chip micrograph of the proposed crystal oscillator.

Fig. 5.20 illustrates the simulated startup behavior of the proposed crystal oscillator. The DI and NRB are enable at 5 μs. The DI injection time is 3 μs. After the injection is disabled, NRB remains enabled to 38 μs until the amplitude rises to 90% of the steady state amplitude. Thereafter, NRB is disabled and the amplitude of the oscillation drops due to the loss of g_m but reach again the steady state within 30 μs. The start-up time is measured between the time point when NRB is stopped and the oscillation amplitude reaches 90% of the maximum. Thus, the proposed design exhibits a very short startup time of 30 μs. The simulated startup energy of the proposed crystal oscillator is 96.4 nJ.

The measured result also shows that the implemented crystal oscillator has an excellent phase noise performance. Fig. 5.21 shows the measured phase noise of the crystal oscillator at the stage after the measurement buffer. At 1 kHz offset from 54 MHz oscillation frequency, the implemented crystal oscillator achieves a phase noise of 133 dBc/Hz with power consumption of the crystal oscillator is 275 μW.

Tab. 5.3 compares the performance of the proposed crystal oscillator with the state-of-the-art. It can be seen that the crystal oscillator achieves the best start-up time among the prior published works. In addition, despite higher oscillation frequency, the proposed crystal oscillator exhibits a better phase noise performance according to the simulation result. In comparison to the design using the same technology node [106], the proposed implementation has a much lower phase noise and a smaller power consumption, although the design reported in [106] features a fully symmetrical structure that could be advantageous in some application.

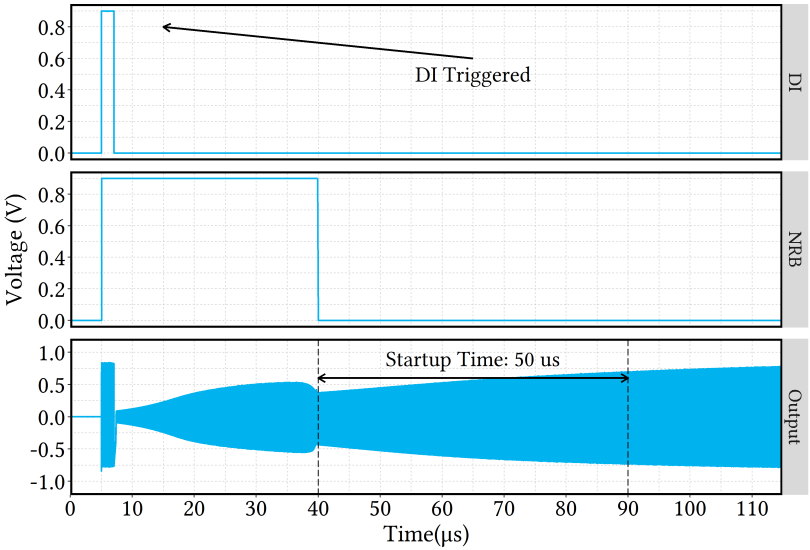


Figure 5.20: Simulated startup behavior of the proposed crystal oscillator with Gaussian-shaped dithered injection and negative resistance boost.

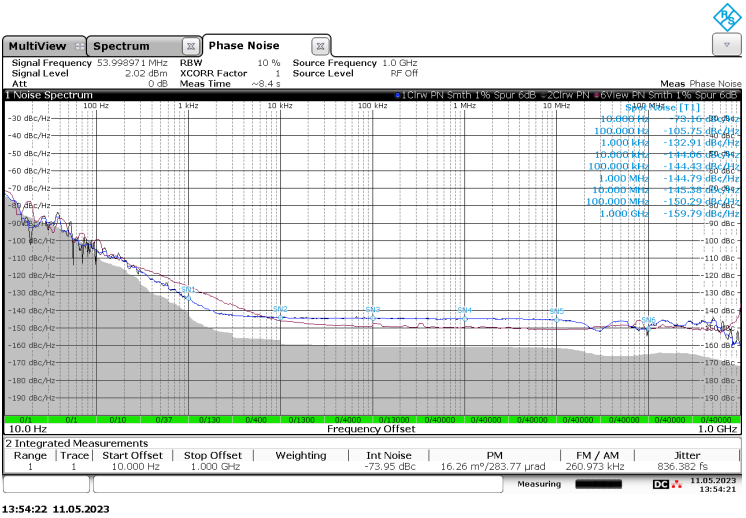


Figure 5.21: Measured crystal oscillator phase noise.

Table 5.3
Performance comparison of state-of-the-art crystal oscillators.

Performance	[105]	[104]	[106]	[99]	[103]	This work
Tech. (nm)	65	65	28	180	130	28
Feature	Stacked g_m	2-step inj.	Diff. g_m stage	CI + NRB	DI + NRB	DI + NRB
Freq. (MHz)	39.25	54	48	39.25	32	54
V_{DD} (V)	3.3	1.0	1.0	1.5	1.2	0.9
PN@1kHz (dBc/Hz)	-139	-139.5	-114.3	-147	N.A.	-133
Startup Time (μs)	3.9	0.019	N.A.	0.158	0.037	0.05*
Startup energy (nJ)	N.A.	34.9	N.A.	349	31.7	96.4*
Power (mW)	0.019	0.198	1.5	0.181	0.181	0.275
Area (mm^2)	0.088	0.069	0.0133	0.12	0.058	0.095**

*Simulated result **Area including a low-noise LDO and non-active decoupling capacitors

CHAPTER 6

CONCLUSION AND OUTLOOKS

6.1 Conclusion

The utilization of FMCW radar in automotive systems has been proven to be an effective method for reducing traffic accident rates. With the continuous shrinking of CMOS technology, the miniaturization of FMCW radar systems has made them more cost-effective and easier to integrate into modern vehicles. However, traditional analog frequency synthesizers are unable to fully exploit the advantages offered by CMOS scaling. Furthermore, the design of analog PLLs faces significant challenges due to the reduced voltage headroom, narrower metal interconnects, and increased flicker noise from active devices. Additionally, the bulky loop filters required by analog PLLs consume substantial silicon area, further increasing costs.

To fully exploit the advantages of CMOS technology scaling, ADPLLs are increasingly employed in these applications. Despite this trend, the design of frequency generation circuits in ADPLLs remains a complex task. For example, digitizing the LC oscillator, i.e., DCO introduces quantization noise, necessitating extremely fine tuning resolution. Simultaneously, a large overall tuning range is essential to ensure the FMCW chirp bandwidth and compensate for PVT variations. This work addresses these challenges by presenting several innovative frequency generation circuit designs using 28 nm CMOS technology, validated by silicon-proven results.

A novel CCNMOS switchable capacitor architecture is proposed to enhance the off-state quality factor of the LC tank and improve the transient behavior of the DCO, which aids in the reduction of locking time of the ADPLL. An 8.2–10.2 GHz class-B DCO was developed, achieving excellent phase noise of −115.1 dBc/Hz at 1 MHz offset, along with FoM of a −183 dBc/Hz and a FoM_T of −190.6 dBc/Hz. A tuning resolution of 60 kHz is achieved, thanks to the customized SC structure.

A class-C prototype operating from 8.2–11.1 GHz, also utilizing the CCN-MOS switchable capacitor structure, was developed with a 30.1% improved tuning range due to its more compact layout. This design exhibited an even finer tuning resolution of approximately 40 kHz, which is the finest reported for DCO in this technology node. The class-C oscillator demonstrated a phase noise of −115.5 dBc/Hz at a 1 MHz offset, with an FoM of −182 dBc/Hz and FoM_T of −191.5 dBc/Hz. Both designs showed phase noise and FoM comparable to state-of-the-art solutions while offering enhanced tuning resolution, superior transient response, and improved inherent monotonic tuning behavior.

Given the significant impact of power supply noise on the performance of frequency generation circuits, a low-noise low-dropout regulator (LNLDO) was implemented. The LNLDO uses a two-stage design with an ultra-low cutoff frequency LPF to effectively filter noise from the bandgap reference and resistive divider. It achieved an RMS noise level of 17.67 μV, with its effectiveness indirectly validated through DCO performance measurements. Additionally, the LNLDO provided a PSRR of greater than 63 dB, ensuring robust supply isolation. Consequently, the LNLDO was also employed for other noise-sensitive blocks within the ADPLL, such as the time-to-digital converter (TDC).

For the reference frequency generation of the ADPLL, a 54 MHz Pierce crystal oscillator was implemented, achieving impressive phase noise of −132.9 dBc/Hz at a 1 kHz offset. Additionally, because the start-up time of the crystal oscillator often limits the overall system response time, methods that accelerate the crystal oscillator start-up were investigated in this work. Chirp frequency and dithered signal injection methods were employed to address this challenge, achieving a start-up time of 50 μs.

6.2 Outlooks

Despite the significant progress made in the innovation of frequency generation circuits, several ideas remain worth exploring in future work, with the goal of further enhancing the performance and robustness of the designs.

6.2.1 Transformer-Based Regulated Class-C DCO

Compared to the class-B LC oscillator, where the gate of the g_m transistors is biased at either V_{DD} or V_{SS}, the g_m devices in a class-C oscillator face a more challenging start-up condition due to a lower initial $|V_{GS}|$. As a result, a regulation loop is required to ensure the reliable operation of the oscillator. In the prototype of project *Cheetah* developed during this thesis, the regulation scheme shown in Fig. 6.1(a) was implemented. An EA is employed to adjust the gate voltage of the g_m devices, PM_2 and PM_3. If the oscillation fails to start, the EA pulls the gate voltage toward V_{SS}, providing a higher $|V_{GS}|$ to ensure safe start-up.

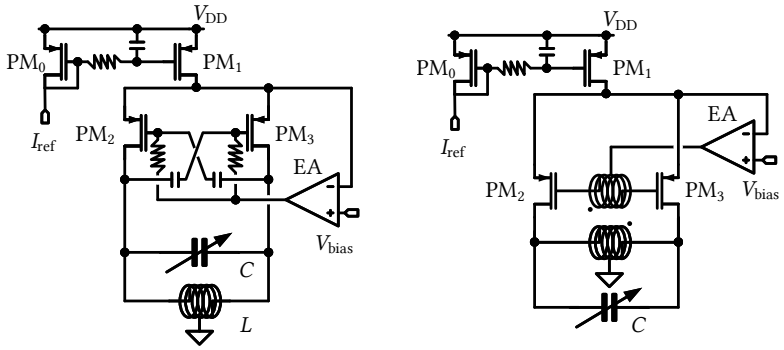


Figure 6.1: Schematic of class-C DCO with regulation using (a) RC feedback and (b) transformer feedback [77].

This operation can also be combined with a transformer, as shown in Fig. 6.1(b) [77]. The use of a transformer introduces additional degrees of freedom in the design, such as tuning the coupling coefficient k and selecting different quality factors for the primary and secondary coils. By incorporating a common-mode LC tank, the transformer also offers the potential to better suppress the influence of second harmonic on the phase noise of the DCO.

6.2.2 Multi-Core DCO

In the previous chapter, it was briefly noted that the amplitude of an oscillator is constrained in CMOS technologies due to limited voltage headroom, unlike

in SiGe or bipolar technologies. To address this, a multi-core DCO is an effective approach for enhancing phase noise performance, at the cost of increased power consumption and chip area. However, employing a direct DC-coupled multi-core architecture introduces undesirable distortions, which can degrade phase noise. A promising solution involves using transformers to achieve AC coupling between cores in a multi-core DCO. Fig. 6.2 illustrates a potential implementation of a quad-core transformer-based DCO [107].

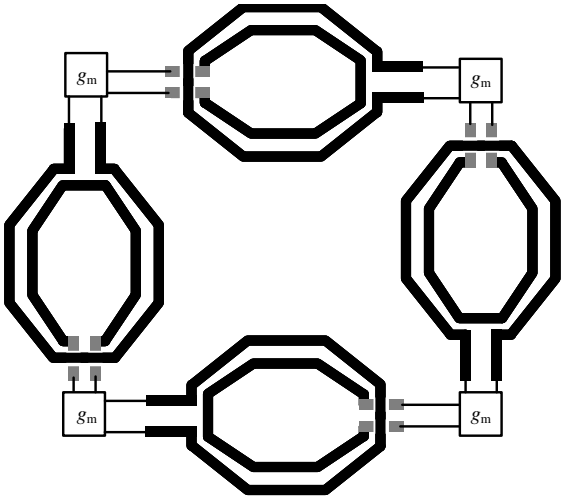


Figure 6.2: A quadcore transformer based DCO [107].

6.2.3 Fully Differential Crystal Oscillator

Although the Pierce crystal oscillator offers good phase noise performance, its asymmetrical nature makes it vulnerable to common-mode distortions. As a result, a symmetrical differential crystal oscillator may be a more suitable option for generating the reference clock in the PLL system. However, unlike the LC oscillator, the crystal resonator does not provide straightforward DC feedback to set the operating point of the g_m devices. This introduces the risk that a differential crystal oscillator could latch due to the high gain at DC, where one pin could be pulled to V_{DD} and the other to V_{SS}, or the circuit may oscillate as an RC oscillator, neglecting the crystal as the resonator, which leads to a poor-quality or absent reference clock. This challenge has prevented

differential crystal oscillators from being widely adopted in the automotive industry, despite their advantage of superior common-mode rejection.

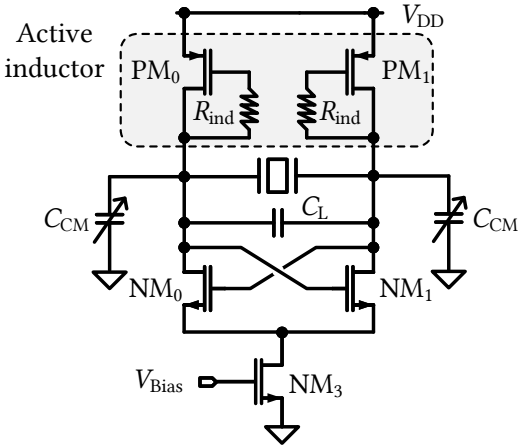


Figure 6.3: A fully differential crystal oscillator using active inductors [106].

A potential solution to address this issue involves the use of an active inductor, as illustrated in Fig. 6.3 [106] [108]. This approach combines a resistor R_{ind} with a PMOS transistor, which exhibits low resistance at DC to prevent the oscillator from latching but presents high impedance at the crystal's resonant frequency, thus achieving high gain only at the target frequency. Additionally, a switched common-mode capacitor C_{CM} is employed to suppress parasitic oscillations.

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APPENDIX A

PUBLICATIONS

A.1 Peer-Reviewed Journal Papers

Tim Lauber, **Lantao Wang**, Johannes Bastl, Kenny Vohl, Ralf Wunderlich, and Stefan Heinen. "A TDC With Integrated Snapshot Circuit and Calibration in 28nm CMOS". in: *IEEE Transactions on Circuits and Systems II: Express Briefs* (2023), pp. 1–1. DOI: 10.1109/TCSII.2023.3343470

Jahnavi Kasturi Rangan, Nasim Pour Aryan, Jens Bargfrede, **Lantao Wang**, Christian Funke, and Helmut Graeb. "Synthesis of DDRO Timing Monitors by Delay-Tracking and Static Timing Analysis". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 67.2 (2020), pp. 401–414. DOI: 10.1109/TCSI.2019.2926149

A.2 Peer-Reviewed Conference Papers

Lantao Wang, Johannes Bastl, Tim Lauber, Kenny Vohl, Jonas Meier, Andreas Köllmann, Ulrich Möhlmann, Michael Hanhart, Ralf Wunderlich, and Stefan Heinen. "A 28 nm 8.2-11.1 GHz Class-C Digitally Controlled Oscillator with 40 kHz Tuning Resolution". In: *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2024, pp. 1–4. DOI: 10.1109/ISCAS58744.2024.10558448

Lantao Wang, Jonas Meier, Johannes Bastl, Tim Lauber, Andreas Köllmann, Ulrich Möhlmann, Michael Hanhart, Alexander Meyer, Christopher Nardi, Ralf Wunderlich, and Stefan Heinen. "An 8.2-10.2 GHz Digitally Controlled Oscillator in 28-nm CMOS Using Constantly-Conducting NMOS Biased Switchable Capacitor". In: *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. 2022, pp. 207–210. DOI: 10.1109/RFIC54546.2022.9863152

Lantao Wang, Running Guo, Johannes Bastl, Jonas Meier, Michael Hanhart, Tim Lauber, Alexander Meyer, Ralf Wunderlich, and Stefan Heinen. "A 0.73-to-1.71 V Capacitor-less Low-Noise Low-Dropout Regulator in 28-nm CMOS". in: *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2022, pp. 1910–1913. DOI: 10.1109/ISCAS48785.2022.9937427

Lantao Wang, Jonas Meier, Ralf Wunderlich, and Stefan Heinen. "A Comparative Study of Switchable Capacitor Structures for LC Oscillators in a 28-nm Technology". In: *2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*. 2021, pp. 1–4. DOI: 10.1109/ICECS53924.2021.9665608

Lantao Wang, Adrian Arnold, Jonas Meier, Markus Scholl, Ralf Wunderlich, and Stefan Heinen. "A 55 MHz Integrated Crystal Oscillator with Chirp Injection Using a 28-nm Technology". In: *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*. 2021, pp. 1–4

Jonas Meier, Florian Menke, **Lantao Wang**, Tim Lauber, Ralf Wunderlich, and Stefan Heinen. "Modeling Power Supply Noise in RF SoCs". In: *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*. 2021, pp. 1–6

Lantao Wang, Marc Fassbender, Markus Scholl, Jonas Meier, Ralf Wunderlich, and Stefan Heinen. "A Low-noise Low-Dropout Regulator Using a 28-nm Technology". In: *2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. 2020, pp. 1–4. DOI: 10.1109/ICECS49266.2020.9294787

Jahnavi Kasturi Rangan, Nasim Pour Aryan, **Lantao Wang**, Jens Bargfrede, Christian Funke, and Helmut Graeb. "Design-dependent Monitors Based on Delay Sensitivity Tracking". In: *2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. 2018, pp. 633–636. DOI: 10.1109/ICECS.2018.8617873

A.3 Talk

Lantao Wang. "Design Considerations for the SC in a DCO for an AD-PLL Application". In: *24. Workshop Analogschaltungen* (2024)

APPENDIX B

CURRICULUM VITAE

25.04.2025	Doctoral Examination for Dr.-Ing.
2023 - Present	RF/PLL Design Engineer NXP Semiconductors, Hamburg, Germany
2019 - 2023	Research Assistant and Doctoral Candidate Integrated Analog Circuits and RF Systems RWTH Aachen University, Aachen, Germany
2018	Master of Science Electrical and Information Technology Technical University of Munich, Munich, Germany
2015	Bachelor of Engineering Electronic Science and Technology Tongji University, Shanghai, China
2010	Chinese University Entrance Qualification (Gaokao) Lijiang No.1 Senior High School Lijiang, Yunnan Province, China