# Carrier mobility in advanced channel materials using alternative gate dielectrics

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# CONTENT

To Edip and Eylül

# Chapter 1

# Introduction

The invention of transistors has led to the development of the integrated electronics era and transistors have become the most widely used devices in modern electronics. The idea of making these electronic devices available throughout the society has yielded to intensive research of microelectronic technology. As a consequence, the need for low cost integration, high speed and low power dissipation has guided Gordon Moore to predict the development of integrated electronic technology and manifest Moore's law, already in 1965 [1]. According to this law, the number of transistors in an integrated circuit roughly doubles every two years. This simple but profound statement has enabled an exponential growth in microelectronic industry over decades.

The root that has been driven by Moore was reinforced by a scaling theory postulated first by Dennard et al. and generalized later by Baccarani et al. [2, 3]. The concept is based on the reduction of the dimensions of the metal-oxide-semiconductor field-effect transistors (MOSFETs) and interconnects of the integrated circuits, such that, gate length L and oxide thickness $t_{ox}$ are reduced by a factor of $1/\alpha$. The electric field may increase by a factor of $\varepsilon$ by reducing the applied voltage by a factor of $1/\lambda$ and increasing the doping concentration by $\alpha^2/\lambda$ in the smaller devices. Hence, higher integration density and faster switching speed are obtained. The gate delay time (inversely proportional to switching speed) as a function of gate length for both, p and n-MOSFETs is shown in Fig. 1.1 [4]. The graph represents the enhanced performance due to the reduced dimensions of the complementary metal-oxide semiconductor (CMOS) transistors.

Another benefit of scaling is the reduction of the power dissipation by a factor of $1/\lambda^2$ due to the reduced voltage and current in each device which results in a power density of $\alpha^2/\lambda^2$. Therefore, the only limitation of the generalized scaling theory is the selection of $\alpha>\lambda$, which results in an increased power density. Nevertheless, now, almost 4 decades after Dennard et al.'s scaling map, the 2011 international technology roadmap of semiconductor (ITRS) has confirmed that since 1974 the MOSFETs has scaled with a factor of 0.7 for every process cycle and 0.5 every two process cycles [5]. This corresponds to device scaling from 3 μm in 1975 to 22 nm in 2012.

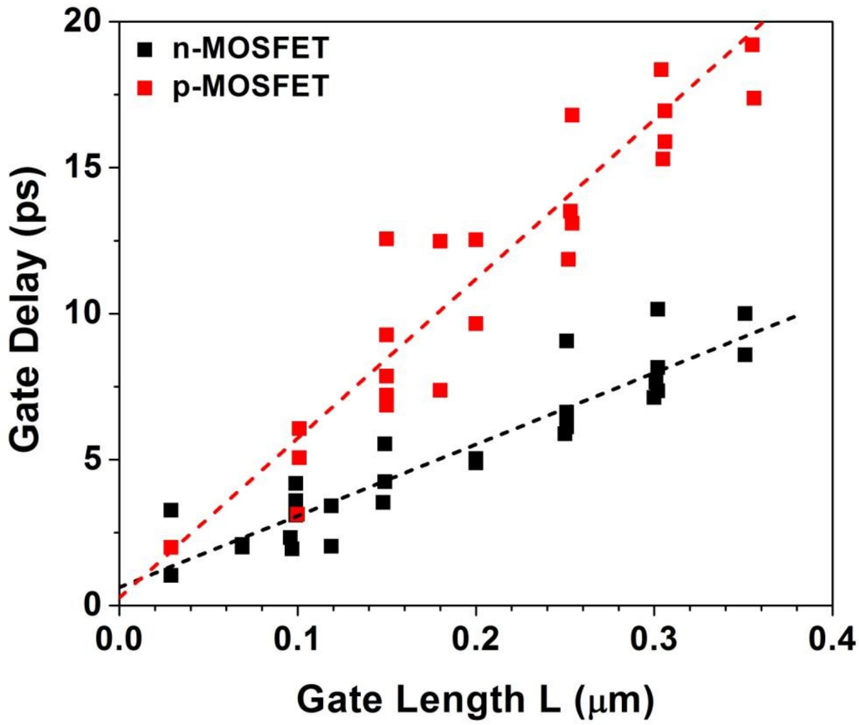


**Figure 1.1:** The gate delay trend as function of gate length for n and p MOSFETs (taken from ref. [4]).

Along the journey in device scaling, to improve the performance, scientists have optimized the source-drain [6, 7, 8], and channel/substrate materials and design [9, 10, 11]. Essentially, the great achievements in the microelectronics and thus the success of down scaling over the last four decades are mainly based on the use of $SiO_2$ as gate oxide, which is a gift of nature. $SiO_2$ provides several advantages for CMOS processing, such as a stable, high quality Si-$SiO_2$ interface with superior electrical isolation properties [12, 13]. Despite its low dielectric constant $\kappa$ =3.9, it has served the industry with a very low defect charge density in the order of $10^{10}$ $cm^{-2}$ and mid gap interface state density in the range of $10^{10}$ $(eVcm^2)^{-1}$, both making $SiO_2$ the best gate oxide. Due to its high band gap of ~9 eV, $SiO_2$ prevents tunneling from the gate to the silicon and acts as a barrier against the diffusion of impurities into the silicon substrate. However, with film thicknesses below 1.5 nm (90 nm technology node and beyond) the devices provided no significant performance improvement and $SiO_2$ does not retain its inherited physical properties. Muller et al. have studied the electronic structure of 0.7-1.5 nm thick $SiO_2$ by electron energy loss spectroscopy (EELS) [14]. They could obtain the full band gap only for two monolayers of $SiO_2$ which sets an absolute minimum thickness of $t_{min}$=0.7 nm for an ideal $SiO_2$ gate oxide. Below two monolayers of $SiO_2$ oxygen atoms do not have the full arrangement of oxygen neighbors and cannot form the full band gap of bulk $SiO_2$. Considering the reactions at both interfaces (top interface with the gate metal and bottom interface with the silicon substrate) and the lower surface roughness the minimum thickness increases to $t_{min}$= 1.2 nm on the practical $SiO_2$ gate oxide. On the other hand, Gou et al. has observed leakage current density higher than 1 $A/cm^2$ on MOS capacitors with $SiO_2$ thickness below 1.5 nm [15]. For MOSFETs with $SiO_2$ thinner than 1.2 nm Timp et al. have observed a reduction in drive current and an increase in leakage current which increases the power consumption and makes further scaling impractical [16, 17]. Thus, 1.2 nm served as a practical limit for the $SiO_2$ thickness. Apart from the leakage problem the reliability and Boron penetration from poly-silicon gate are also big issues for scaled oxides [18, 19, 20].

In order to maintain Moore's law on spite of the problem encountered with scaled $SiO_2$ it has been suggested to use high dielectric constant materials (high-$\kappa$ dielectrics, $\kappa$>3.9). Physically thicker high-$\kappa$ films can be grown providing the same equivalent electrical oxide thickness (EOT), which provides significant gate leakage reduction. There has been a significant improvement in the field of alternative high-$\kappa$ dielectric [21, 22] and the first high-$\kappa$ product was Intel's 45 nm transistor with hafnium (Hf) based gate oxides together with an appropriate metal gate [23]. Recently, Intel has announced the second generation of high-κ gates for 32 nm technology node, where the EOT has been reduced from 1 nm for 45 nm node to 0.9 nm for 32 nm technology node [24]. The leakage current in the 45 nm node decreased by a factor of 5 in the n-MOSFET and 10 in the p-MOSFET as compared to MOSFETs with $SiO_2$. Tomida et al. observed that $Hf_{(1-x)}Si_xO_2$ shows different $\kappa$ values depending on the crystallization phase [25]. They observed that amorphous $Hf_{(1-x)}Si_xO_2$ shows a $\kappa$ value around 20; however, for the monoclinic phase, the $\kappa$ value is 15 and as they increased the temperature and changed the crystallization phase from monoclinic to tetragonal the $\kappa$ value increased to 27. Moreover, Böscke et al. [26] and Migita et al. [27] obtained a $\kappa$ of 36 and an even higher $\kappa$ value for tetragonal and cubic $HfO_2$, respectively. However, the $\kappa$ values of amorphous Hf-based oxides varies around 20 [28, 29].

Although Hf based oxides have replaced $SiO_2$ for high performance MOSFETs, the challenge is to continue scaling for smaller dimensions. On the other hand, it is foreseeable that Hf based oxide will be no long term solution, due to the band gap narrowing (<1.2 nm [30]) that will be faced by the aggressively scaled oxide thickness. This has already been issued by the 2011 ITRS, where EOT scaling below 0.7 nm and higher-$\kappa$ ($\kappa$>30) are referred as a challenge for the next generation technology node (22 nm) [5].

Figure 1.2 shows the optical band gap ($E_g$) versus dielectric constant of possible gate dielectrics thermodynamically stable on silicon [31]. A general trend between the band gap and the $\kappa$ value is obvious: as the $\kappa$ value increases the band gap decreases. Among the materials in the graph, $LaLuO_3$, $LaScO_3$, $SmScO_3$, $GdScO_3$ and $DyScO_3$, which are known as rare-earth based ternary oxides, have higher dielectric constants and a comparable band gap, $E_g$>5 eV, similar to $HfO_2$. Apart from having higher $\kappa$, it is important to have an amorphous phase through out device processing. It has been shown that, $LaLuO_3$ [32], $LaScO_3$ [33] and, within this study, $SmScO_3$ have much higher crystallization temperature ranging between 800-1000 ºC than $HfO_2$ which tends to crystallize at 550 ºC. $TbScO_3$ as a rare-earth based ternary oxide has also proven to have a high dielectric constant with a crystallization temperature over 1000 ºC [34]. Higher κ and crystallization make those materials more attractive for the next generation of high-$\kappa$ gate stacks.

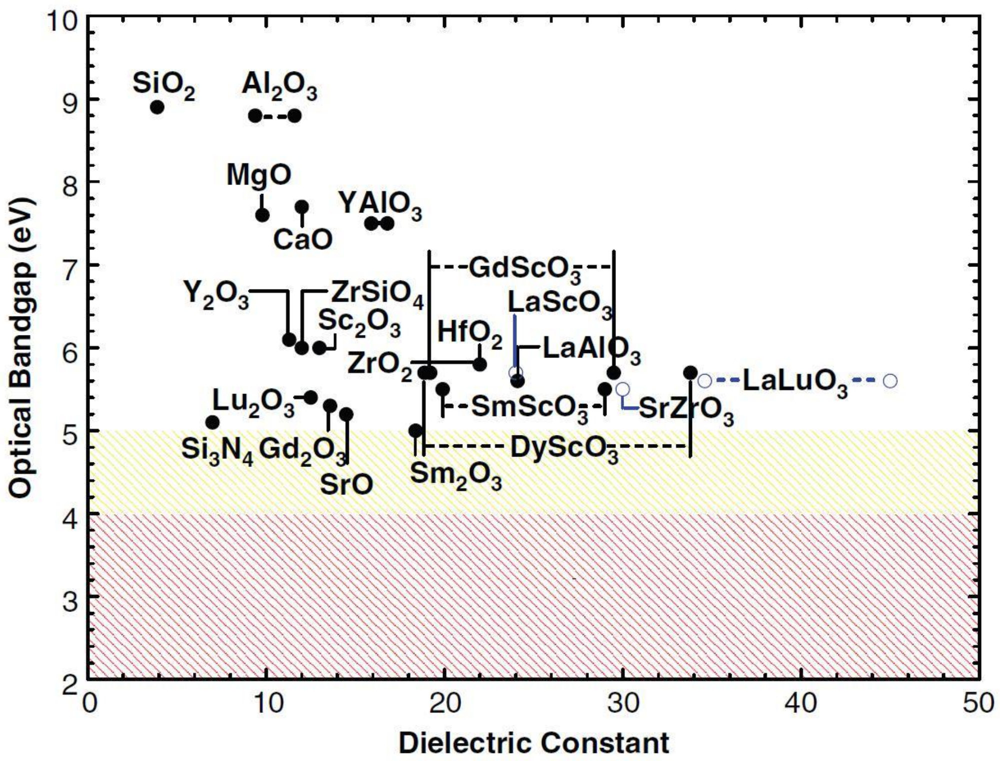


**Figure 1.2:** Plot of optical band gap versus dielectric constant ($\kappa$) for alternative gate dielectric materials (from ref. [30]).

The major problem with the alternative gate dielectrics is the deteriorated interface characteristics which together with the intrinsic properties of the dielectric itself cause reduced channel mobility in high performance devices [35, 36, 37]. Germanium and III-V materials as high channel mobility materials seem to be a possible solution for the mobility reduction caused by the high-$\kappa$ materials. However, this seems also challenging, due to the poorer interface quality for these materials. On the other hand, for the 90 nm technology node, strained silicon was implemented as a substrate with 1.2 nm $SiO_2$ in order to compensate the mobility reduction caused by very thin gate oxide [11]. Research of MOSFETs with $HfO_2$ [38] and $GdScO_3$ [39] on silicon on insulator (SOI) and strained silicon on insulator (sSOI) has shown that, the mobility of sSOI devices is twice as high as for SOI devices. Therefore, integration of the high-$\kappa$ materials with strained silicon in MOSFET devices is a successful technology.

In this thesis, the structural and electrical properties of $LaLuO_3$, $LaScO_3$, $TbScO_3$ and $SmScO_3$ have been investigated. For the first time, their integration, has been achieved for p and n-MOSFET devices using both SOI and sSOI substrates. The experimental work of this thesis was concluded in February 2011.

**Chapter 2:** The principles of the MOS capacitors and MOSFET devices are introduced. The non-ideal properties in a real MOS structure and their effect on the capacitance –voltage (CV) characteristics are explained in detail. Characterization methods used throughout this thesis are also introduced in this chapter. High-$\kappa$ issues with the requirements will be explained.

**Chapter 3:** This chapter is devoted to the structural and electrical investigation of the rare earth based ternary oxides and the results are compared to results with $HfO_2$ gate oxide. The composition and the morphology of the films are studied by Rutherford back-scattering spectrometry (RBS) and X-ray diffraction (XRD), respectively. The possible interfacial layer formation after different annealing conditions is investigated by means of X-ray photoelectron spectroscopy (XPS) and time of flight secondary ion mass spectroscopy (TOF-SIMS). On the base of electrical investigations, an optimization of low temperature annealing is studied. Post deposition annealing (PDA) and post metallization annealing (PMA) in oxygen and forming gas (FG) are investigated. Equivalent oxide thickness (EOT), leakage current density ($J_g$), density of interface trap charges ($D_{it}$) and oxide charge ($N_{ox}$), flatband voltage ($V_{FB}$) shift and effective work function of the metal gate were studied in detail for MOS capacitors with PDA and PMA.

**Chapter 4:** A replacement gate process for the fabrication of MOSFETs has been developed. For the first time n-MOSFETs with $LaLuO_3$, $LaScO_3$, $TbScO_3$ and $SmScO_3$ have been successfully integrated using SOI and sSOI substrates. p-MOSFETs with $LaLuO_3$ and $LaScO_3$, for the first time, have also been integrated using SOI substrates. The key device parameters are extracted using I-V and split C-V measurements and the results are compared with $HfO_2$ devices. The possible reasons for mobility degradation are discussed in this chapter. Gate induced drain leakage (GIDL), which is observed due to the high electric field, caused by very thin oxide layer (or thin high-$\kappa$) at the source-drain overlap region is explained and investigated in detail.

# Chapter 2

# Principles of MOS devices and extraction of their physical parameter

## 2.1 MOS capacitor in ideal case

Metal-Oxide-Semiconductor (MOS) capacitors are the heart of the MOSFETs. The operation and characteristics of the MOSFET strongly depends on the MOS part. Therefore, it is worth first, to understand the MOS structure. Information about MOS capacitors can be found in many books [12, 40, 41]. In order to explain the physics behind, the MOS structure is assumed to be ideal, that means, free of charges and defects. Figure 2.1(a) illustrates the ideal MOS capacitor structure on silicon substrate, where $t_{ox}$ is the oxide thickness and $V_G$ is the applied voltage to the metal gate. The detailed analysis of the MOS capacitor begins with the equilibrium band diagram, when the bias voltage $V_G$=0, which is shown in Fig. 2.1(b). At this condition, the Fermi level in the metal and silicon must be equal and the vacuum level must be continuous. These two requirements determine a unique energy band diagram for the ideal MOS capacitor. The energy barriers presented in the figure prevent the free flow of carriers from the metal to the silicon or vice versa.

Depending on the applied voltage band bending occurs and the basic behavior of the capacitor could be observed. At equilibrium, where $V_G$=0, there is no charge on the silicon surface and no electric field across the oxide layer; the bands are flat. Therefore the work function difference $\phi_{ms}$ is equal to zero and it can be written as

$$\Phi_{ms} = \Phi_m - \Phi_S = \Phi_m - \left(\chi + \frac{E_g}{2q} \pm \Psi_B\right) = 0 \tag{2.1}$$

with

$$\Psi_B = \frac{E_F - E_{Fi}}{q} = \frac{kT}{q}\ln(\frac{N_A}{n_i}) \tag{2.2}$$

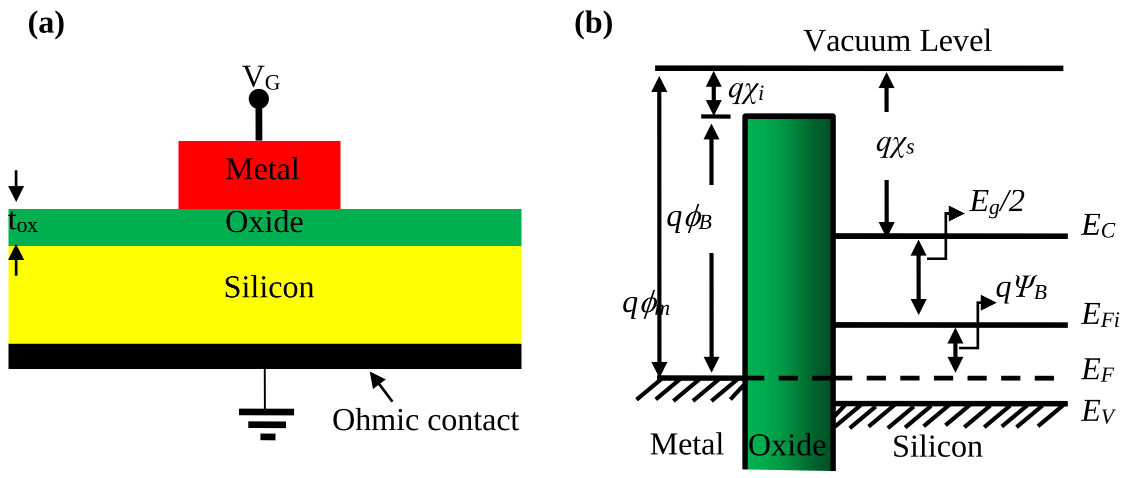


**Figure 2.1:** (a) Schematic illustration of an ideal MOS capacitor. (b) Energy-band diagrams of a p-MOS capacitor at equilibrium. $\phi_m$: metal work function, $\chi_i$: electron affinity of the insulator, $\chi_S$: electron affinity of semiconductor (silicon in this case), $E_g$: energy gap of semiconductor, $\phi_B$: potential difference between the metal Fermi level and conduction band of the insulator, $\Psi_B$ is the potential difference between the intrinsic Fermi level ($E_i$) and Fermi level ($E_F$) inside the bulk, $E_C$: conduction band $E_V$: valance band of the semiconductor.

where $\Phi_S$ is the silicon work function, $N_A$ the acceptor doping concentration and $n_i$ the intrinsic carrier concentration. When $V_G \neq 0$ an electric field will be established in the oxide by the surface charge layer formed in the metal and silicon. The band bending for silicon at any point x in the depletion layer with respect to bulk is defined by $\Psi(x)$ and while in the bulk silicon it is equal to zero (there is no band bending), at the silicon surface it is the surface potential $\Psi_s$, where $\Psi_s$ is the potential difference between $E_{Fi}$ measured at the bulk silicon and $E_{Fi}$ taken at the surface. Depending on the applied voltage, the electron and hole concentration at the silicon surface can be written as

$$p_s = p_{po} \exp(-\beta\Psi) \tag{2.3}$$

$$n_s = n_{po} \exp(\beta\Psi), \tag{2.4}$$

where $p_{po}$ and $n_{po}$ are the equilibrium densities of holes and electrons, respectively, in the bulk of silicon and $\beta = q/kT$. Considering a p type MOS capacitor, mainly five working conditions are present in the silicon.

**Accumulation ($\Psi_s$<0):** When $V_G$<0 is applied to the metal gate, an electric field occurs in the direction from silicon to the metal. The majority carriers, holes, are accumulated at the silicon surface, while the minority carriers, electrons, pushed more inside the bulk. As a result, the hole concentration at the surface will be larger than the one within the bulk. In order to preserve the charge neutrality at the silicon surface the bands bend upward.

**Flat band ($\Psi_s=0$):** As the $V_G$ approaching zero, the holes leave the surface, and at $V_G=0$ the silicon surface becomes neutral. The electron and hole concentration at the surface is equal to their value in the bulk. No band bending occurs, therefore, the bands are flat.

**Depletion ($\Psi_B> \Psi_s>0$):** For a $V_G>0$, due to the created electric field in the direction from metal to silicon, the majority carrier holes are accelerated toward the bulk of silicon and the electron density at the silicon surface is built up. A negative space charge region is created at the silicon and the hole concentration at the surface becomes lower than the one inside the bulk and the bands bend downward.
In a p-type silicon, the electron density is negligible for positive bias, therefore the positive gate charges are balanced not only by electrons, but also by ionized acceptors in the silicon surface depletion layer due to the depleted holes in this region. As gate bias increases, the depletion layer width $x_d$ widens to provide more ionized acceptors (see Fig. 2.2).

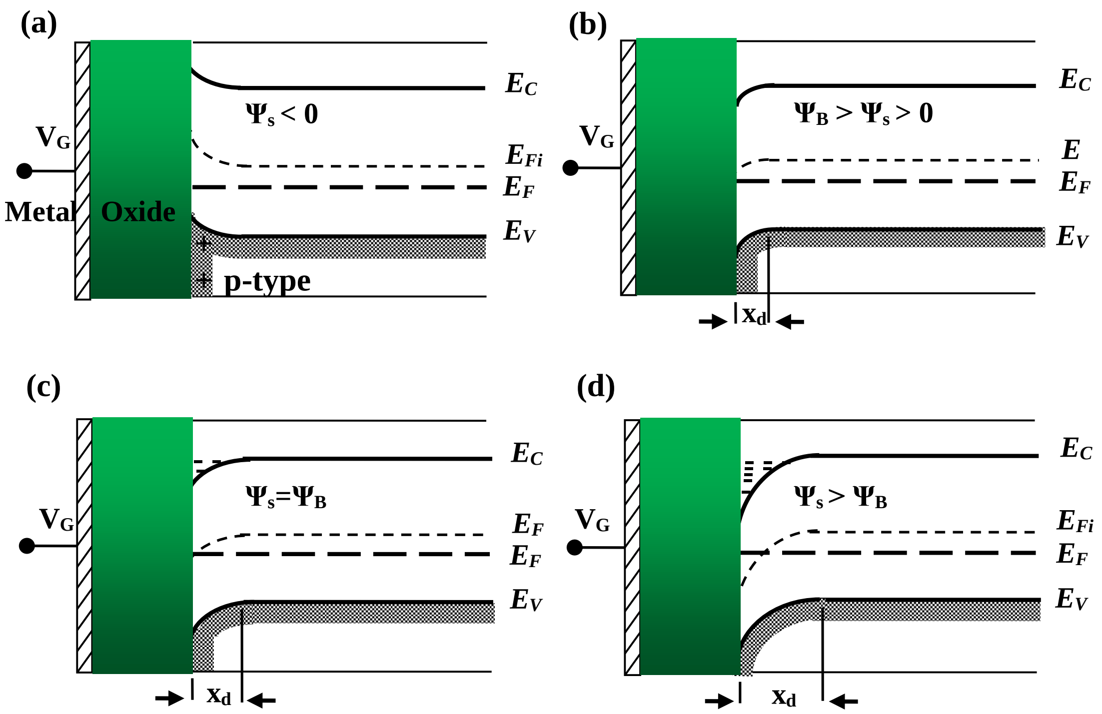


**Figure 2.2:** The energy-band diagram of a MOS capacitor with a p-type substrate for (a) accumulation, (b) depletion, (c) intrinsic point and (d) inversion.

**Intrinsic point ($\Psi_s= \Psi_B$):** Increasing $V_G$ results in a wider depletion region with more band bending. At certain $V_G$, at the silicon surface the electron and the hole concentrations will be equal, hence, $E_{Fi}$ at the surface will be equal to $E_F$. The surface of the silicon becomes intrinsic with $p_s=n_s=n_i$.

**Inversion ($\Psi_s > \Psi_B$):** The $V_G$ is sufficiently high to repel most of the holes from the surface, and electrons appear in the silicon surface in a larger number. In this case, an inversion layer is created with $p_s<n_s$ and the bands continue to bend downward. At the point where $\Psi_s = 2\Psi_B$ strong inversion starts and the $x_d$ reaches its maximum.

### 2.1.1 Theoretical capacitance of ideal MOS structure

For a mathematical expression of the space charge density, $Q_s$, in the depletion region, one has to solve the Poisson equation. Because the silicon surface is represented by the plane at x=0 and the bulk by positive value of x, the Poisson equation should be solved for one dimension. The surface potential as a function of x is the band bending Ψ(x), and is given by the Poisson equation in one dimension as

$$\frac{\partial^2 \Psi(x)}{\partial x^2} = -\frac{\rho(x)}{\varepsilon_S} \tag{2.5}$$

where $\varepsilon_s$ is the permittivity of the silicon and ρ(x) is the total charge density given by

$$\rho(x) = q(N_D^+ - N_A^- + p_p - n_p) \tag{2.6}$$

$N_D^+$ and $N_A^-$ are the densities of ionized donors and acceptors, respectively. Because in bulk silicon the charge neutrality must exist, Ψ(x) and ρ(x) should be equal to zero, therefore,

$$N_D^+ - N_A^- = n_p - p_p \tag{2.7}$$

For any value of *Ψ(x)* according Equations 2.2 and 2.3 the difference between free carriers is

$$p_p - n_p = p_{po}\exp(-\beta\Psi) - n_{po}\exp(\beta\Psi) \tag{2.8}$$

For a p-type silicon $N_A>>N_D$, $p_{po} \approx N_A$ and $n_{po} \simeq n_i^2/N_A$, hence,

$$\rho(x) = q(\frac{n_i^2}{N_A^-} - N_A^- + N_A^- e^{-(\beta\Psi)} - \frac{n_i^2}{N_A^-}\left(e^{(\beta\Psi)}\right)) \tag{2.9}$$

the resulting Poisson equation is obtained as

$$\frac{\partial^2 \psi(x)}{\partial x^2} = -\frac{q}{\varepsilon_S}\left[N_A^-\left(e^{-(\beta\Psi)} - 1\right) - \frac{n_i^2}{N_A^-}\left(e^{(\beta\Psi)} - 1\right)\right] \tag{2.10}$$

The electric field is defined as

$$E_S = -\frac{\partial \Psi(x)}{\partial x}, \qquad \text{hence;} \quad \frac{\partial E_S}{\partial x} = -\frac{\rho(x)}{\varepsilon_S} \tag{2.11}$$

Solving equation 2.10 for 2.11

$$E_S = \pm\frac{\sqrt{2}k_B T}{qL_D}\cdot\sqrt{\left(e^{-(\beta\Psi)} + \beta\Psi - 1\right) + \left(\frac{n_i^2}{N_A^-}\right)^2\left(e^{(\beta\Psi)} - \beta\Psi - 1\right)} \tag{2.12}$$

where

$$L_D = \sqrt{\frac{k_B T \varepsilon_S}{N_A^- q^2}} \tag{2.13}$$

is the Debye length and represents the distance over which the free carriers reduce the potential from the fixed impurity ions. Using the electric field expression in Equation 2.12, the space charge density, $Q_S = -\varepsilon_S E_S$ can be found as follows

$$Q_s = \pm \frac{\sqrt{2}\varepsilon_s k_B T}{q L_D} \cdot \sqrt{\left(e^{-(\beta\Psi)} + \beta\Psi - 1\right) + \left(\frac{n_i^2}{N_A^-}\right)^2 \left(e^{(\beta\Psi)} - \beta\Psi - 1\right)} \tag{2.14}$$

where a positive sign is applied for accumulation and a negative sign for depletion. At the silicon surface, $\Psi(x)\rightarrow\Psi_s$ and at that point $Q_S$ is a function of the surface potential $\Psi_s$. Figure 2.3(a) represents the theoretically calculated space charge density $Q_S$ as a function of the surface potential. The oxide capacitance $C_{ox}$ and the doping concentration $N_A$ are derived from an experimental capacitance-voltage (C-V) measurement. $Q_S$ in the

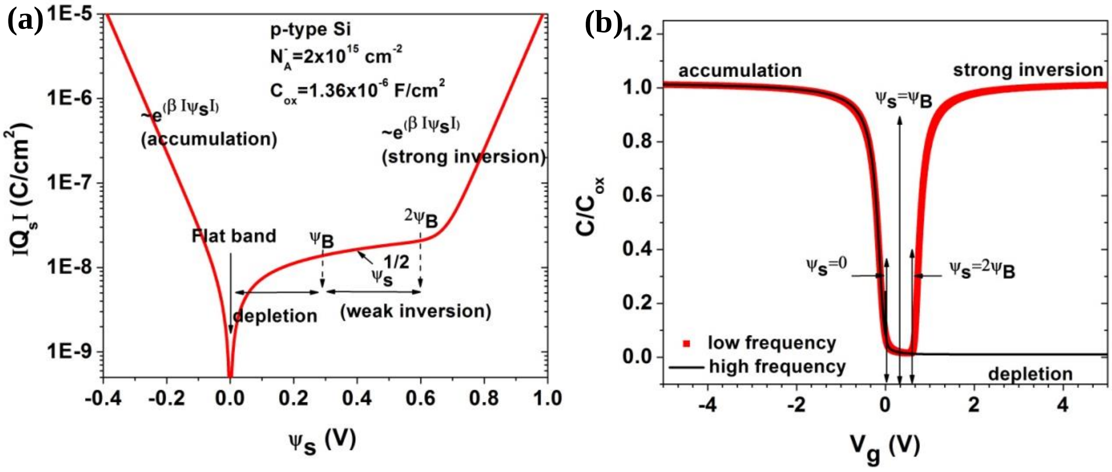


**Figure 2.3:** (a) Variation of the space charge density $Q_s$ as a function of the surface potential $\Psi_s$ for p-type silicon. (b) corresponding normalized ideal capacitance-voltage (C-V) curve. For low frequencies, the curve reaches the strong inversion while for high frequency no inversion layer is observed.

accumulation region is negative and as indicated in the graph, governed by $e^{\beta|\Psi_S|}$ . At flat band $Q_S$ is zero. At depletion and weak inversion it is positive and governed by $\psi_S^{1/2}$, at strong inversion the leading factor is again $e^{\beta|\Psi_S|}$.

At the silicon depletion layer the differential capacitance C is given as

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_D} \tag{2.15}$$

where $C_{ox}$ is the normalized oxide capacitance to the area and $C_D$ is the depletion layer capacitance at the semiconductor surface. $C_{ox}$ and $C_D$ are given as

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad \text{and} \quad C_D = \left|\frac{\partial Q_S}{\partial \Psi_S}\right| \tag{2.16}$$

where $\varepsilon_{ox}$ is the permittivity of the oxide layer while $t_{ox}$ is its thickness. Differentiating Equation 2.14 over $\Psi_s$ yields

$$C_D = \frac{\varepsilon_S}{\sqrt{2}L_D} \cdot \frac{\left[1-e^{-(\beta\Psi_S)}+\left(\frac{n_i^2}{N_A}\right)^2\left(e^{(\beta\Psi_S)}-1\right)\right]}{\sqrt{\left(e^{-(\beta\Psi_S)}+\beta\Psi_S-1\right)+\left(\frac{n_i^2}{N_A}\right)^2\left(e^{(\beta\Psi_S)}-\beta\Psi_S-1\right)}} \tag{2.17}$$

The combination of equations 2.15, 2.16 and 2.17 gives the complete description of the ideal low frequency (LF) MOS capacitor capacitance characteristics. Figure 2.3(b) illustrates the corresponding ideal LF normalized C-V characteristic of the space charge plotted in Fig. 2.3(a), for comparison the ideal high frequency (HF) normalized C-V curve is also added. For the negative applied gate voltage there is an accumulation of holes and because in this case $C_D >> C_{ox}$, $C=C_{ox}$ (from Equation 2.15). As $V_G$ becomes less negative, the hole density at the silicon surface will decrease and $C_D$ will be smaller, therefore the differential capacitance $C$ will be smaller than $C_{ox}$. For positive $V_G$ ($\Psi_s>0$) the holes are repelled from the surface, giving rise to the formation of a depletion layer of ionized acceptors, this region is called as depletion region. If the gate bias turns more positive, the depletion layer widens, making $C_D$ smaller and as a result $C$ decreases. When $\Psi_s= \Psi_B$ is satisfied the hole and electron densities at the surface are both equal $n_i$. Until $\Psi_s= 2\Psi_B$ is satisfied, the ideal LF and HF C-V curves are identical; above this point two possible cases are valid due to the minority carrier response time. The response time $\tau_R$ of the minority carriers in silicon at room temperature is ~0.01-1 sec in strong inversion [12], and they can follow the applied ac voltage as long as $1/\omega >> \tau_R$ , where $\omega$ is the frequency of the applied ac voltage. For low frequency C-V the minority carriers can follow the ac voltage, an inversion layer will be created and $C_D$ is as given in Equation 2.17. However, in case of HF, since the minority carriers are to slow, they cannot follow the rapidly varying ac voltage; therefore, the measured capacitance is still the depletion layer capacitance, $C_D$. Furthermore, because at $\Psi_s= 2\Psi_B$ the depletion layer width reaches its maximum, $x_{d,max}$, $C_D$ reaches its minimum and stays constant for an increased gate voltage. Therefore the depletion layer capacitance where $\Psi_s \geq 2\Psi_B$ is given as [40]

$$C_D = \sqrt{\frac{\varepsilon_S q N_A}{2\Psi_S}} = \frac{\varepsilon_S}{x_{d,max}} \cdot \tag{2.18}$$

## 2.2 Non-ideal properties in real MOS structures and their effect on C-V

In the band bending explanation and calculation of the theoretical capacitance, the MOS structure is assumed to be free of charge, and there is no work function difference between the metal gate and semiconductor substrate. However, in a real capacitor, this is not the case! There exist interface traps, and oxide charge, and the metal work function does not always coincide with the semiconductor one.

### 2.2.1 Interface trap charges

Interface trapped charges $Q_{it}$, or the interface trap density $D_{it}$ play a major role in the operation of MOS devices. They can be produced due to the structural defects, broken bonds, excess oxygen and impurities. They are defects located at the Oxide-Semiconductor interface and have an energy level within the semiconductor band gap. It is accepted that trap energy levels above the mid gap exhibits acceptor-like characteristics and those below midgap has donor-like characteristics [42]. Both kinds of traps could exist at the surface. The net charge is the sum of both types of traps and if they are symmetrically localized around the midgap, the net charge is zero. Depending on the applied voltage, they change occupancy by charge exchanging with the semiconductor, however, their respond to the applied voltage depends on their position; traps close to the mid gap will take longer to respond than those close to the band edges. They can interact with the semiconductor conduction band (valence band) by capturing or emitting electrons (holes). In this way, they can cause severe degradation in majority carrier devices by pinning the Fermi level (at $qD_{it} > C_{ox}$) and disabling the field effect. Even if they are not large enough to pin the Fermi level, they deteriorate the electric field by reducing the surface potential (band bending) which degrades the carrier concentration. Therefore, a larger gate voltage is required to reach the desired carrier concentration at the semiconductor surface, which results in a stretch-out of the C-V measurement.
In order to give an explanation of the possible deteriorations in MOS devices, $D_{it}$ should be extracted. In this study two methods have been used to extract $D_{it}$; a high frequency C-V technique (which is known as Terman's method) and a conductance method.

### 2.2.2 Oxide charges and work function differences:

**Oxide Charges:** Oxide charges include the fixed oxide charge ($Q_f$), the mobile ionic charge ($Q_m$) and the oxide trapped charge ($Q_{ot}$) as shown in Fig. 2.4 (a). Unlike interface trapped charge, these charges are independent of applied gate voltage and cause a parallel shift in the C-V curve as compared to the ideal one (Fig. 2.5 (b)). A negative voltage shift $\Delta V$ indicates the presence of positive oxide charges, while a positive $\Delta V$ occurs due to negative oxide charges. The location of the charges defines the amount of $\Delta V$; the closer to the semiconductor interface the larger $\Delta V$ will be observed.

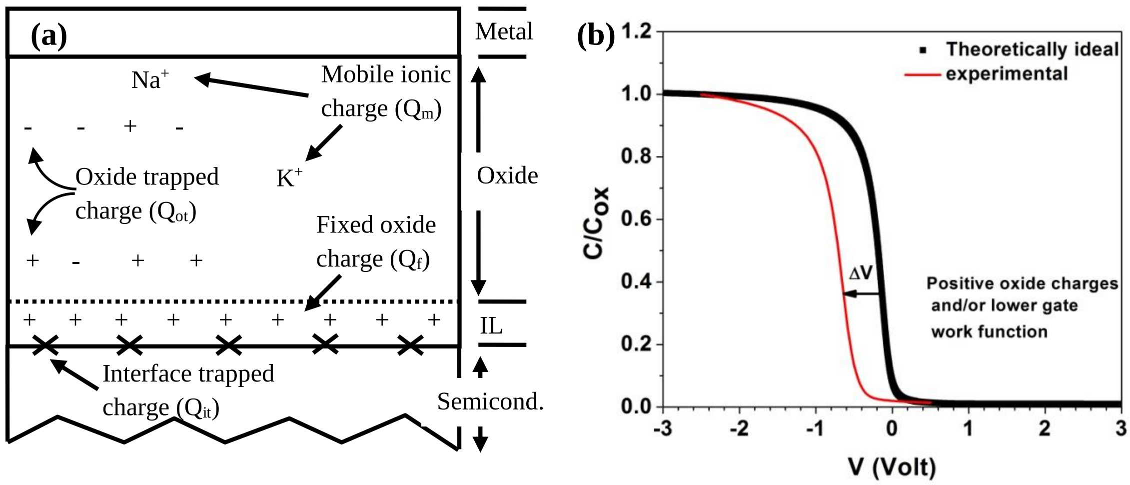


**Figure 2.4:** (a) The oxide charges and interface trapped charge distribution within the oxide and the interface to semiconductor. IL represents the interfacial layer. (b) Normalized theoretically calculated and experimentally measured C-V curves. ΔV voltage shift occurs, due to both, oxide charges and work function differences.

The fixed charges $Q_f$ are located very close to the oxide-semiconductor interface, and are generally positive. These are charges, remaining after interface trap states are annealed out, and hardly affected by the oxide thickness. In electrical measurement, $Q_f$ can be regarded as charge sheet located at the oxide-semiconductor interface and their contribution the ΔV is

$$\Delta V_f = -\frac{Q_f}{C_{ox}} \tag{2.19}$$

The oxide trapped charges $Q_{ot}$ are associated with the defects within the oxide layer. These types of charge are usually initially neutral and are charged by introducing electrons or holes in to the oxide layer via current passing through the oxide. The voltage shift due to $Q_{ot}$ is

$$\Delta V_{ot} = -\frac{Q_{ot}}{C_{ox}} \tag{2.20}$$

The mobile ionic charges $Q_m$ are caused by the presence of ionized metal atoms. These types of charge are located either at the metal-oxide interface or at the oxide semiconductor interface. Depending on the applied voltage, they can move back and forth through the oxide layer and give rise to ΔV. These types of charge are responsible for the hysteresis observed in C-V measurements. They can be positive or negative and their polarity can be investigated by a double sweep C-V measurement. A counter-clockwise hysteresis can be attributed to the existence of positive mobile trapped charges, and clockwise hysteresis indicates the presence of negative mobile trapped charges. Their contribution to ΔV is given as

$$\Delta V_m = -\frac{Q_m}{C_{ox}} \tag{2.21}$$

The total voltage shift due to all the oxide charges is

$$\Delta V = \Delta V_f + \Delta V_{ot} + \Delta V_m = -\frac{Q_f + Q_{ot} + Q_m}{C_{ox}}\,. \tag{2.22}$$

The oxide charges all together, may alter the threshold voltage and reduce the carrier mobility via scattering. Therefore they must be understood for a correct interpretation of a C-V curve measured on a MOS capacitor.

**Work-Function Difference:** The work function difference is given in Equation 2.1 and for an ideal MOS capacitor it is assumed to be zero. However, if $\Phi_{ms} \neq 0$ the experimental C-V curve will be shifted from the theoretical one by the same amount in the gate bias. The polarity of $\Phi_{ms}$ defines the shifting direction. Therefore, the C-V curve will be shifted to a more positive voltage for $\Phi_{ms}>0$ and a negative for $\Phi_{ms}<0$. This shift is in addition to the oxide charges and the net flat band voltage becomes

$$V_{FB} = \Phi_{ms} + \Delta V = \Phi_{ms} - \frac{Q_f + Q_{ot} + Q_m}{C_{ox}}. \tag{2.23}$$

# 2.3 Principles of MOSFET operation

A common MOSFET is a four terminal device that consists of a semiconductor substrate in which opposite polarity source and drain (S/D) region are formed by ion implantation. The basic structure of a MOSFET with p-type Si is shown in Figure 2.5. Shallow $n^+$ junctions connect the S/D to the p-type silicon and the metal gate is separated from the silicon by a thin oxide layer with thickness of $t_{ox}$, where the MOS capacitor is present.

As mentioned in section 2.1, for a MOS capacitor the position of the conduction and valence band relative to the Fermi level is a function of the surface potential, thus the applied gate voltage $V_G$. By applying an appropriate $V_G$ the surface of the semiconductor will be inverted and an induced space charge region will be formed at the semiconductor surface. This space charge region acts as the "heart" of the MOSFET by forming the channel with length L and allowing the current flow between S/D.

In Fig. 2.6, the conduction band $E_C$ diagram variation depending on the applied $V_G$ and $V_D$ is presented. Figure 2.6 (a) represents the condition for an ideal MOSFET, where $V_G=V_D=0$ and the Fermi levels of S/D and channel coincide. In this state the device is in its off-state. Changing the $V_G$ from zero to a value equal to $V_T$ will result in an energy lowering in $E_C$ (also in $E_V$) at the surface of the channel by creating the induced space charge region and inverting the surface from p-type to n-type. In this case the device is in its on-state, but since $V_D$ is zero there will be no charge flow along

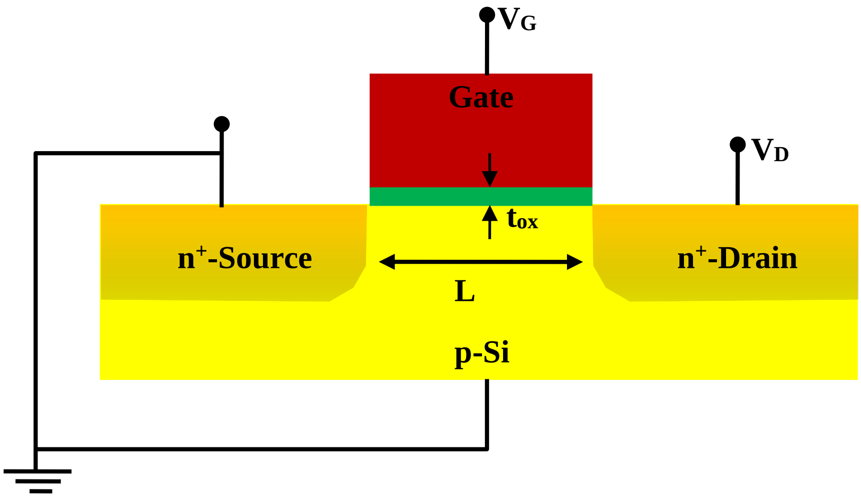


**Figure 2.5:** Schematic illustration of a MOSFET with applied gate voltage $V_G$, drain voltage $V_D$, channel length L and oxide thickness $t_{ox}$.

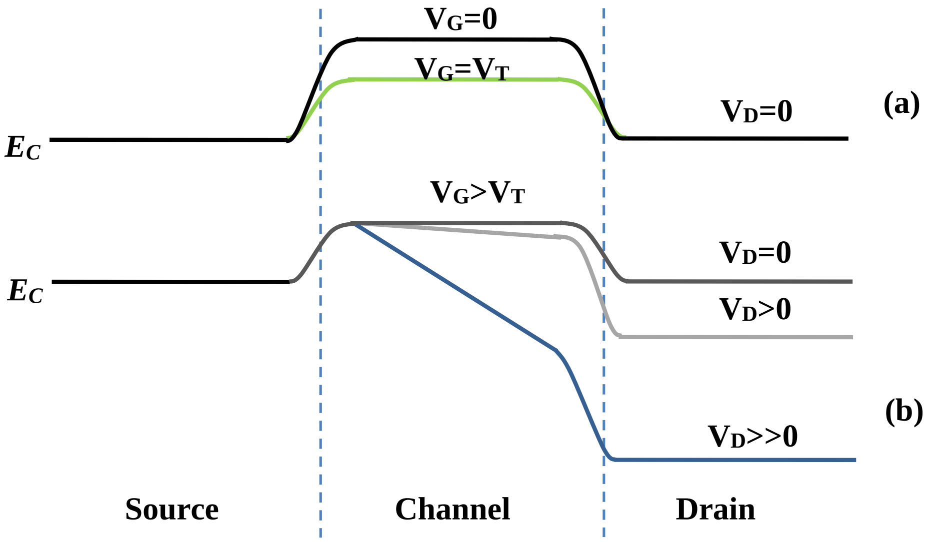


**Figure 2.6:** The Conduction-Band diagram of n-MOSFET for (a) $V_{G}.=V_D=0$ and (b) $V_G>V_T$ and $V_D \geq 0$. $V_D$.

the channel to the drain. This is the equilibrium condition and will be preserved, hence no change in the Fermi level will be observed. On the other hand, the threshold voltage $V_T$ is defined as the minimum voltage needed to create the inversion charge for switching the transistor on. For $V_G>V_T$, the channel is already inverted and when a small positive $V_D$ is applied, the $E_C$ and $E_V$ at the drain side will be lowered (nonequilibrium condition-Fig. 2.6 (b)). In this case, electrons in the inversion layer will flow from the source to the positive drain terminal resulting in a lowered Fermi level in the drain side by an amount of $qV_D$. Increasing $V_D$ to a more positive value will cause a larger band lowering towards the drain side.

## 2.3.1 Determination of current-voltage (I-V) characteristics

According to the charge sheet model, the inversion layer is treated as charge sheet with zero thickness. Based on this model, from the Gauss law, the boundary conditions on both sides of the charge sheet are [40]

$$\mathcal{E}_{ox}\varepsilon_{ox} = \mathcal{E}_{s}\varepsilon_{s} - Q_n \tag{2.24}$$

where $Q_n$ is the inversion charge, $\mathcal{E}_{ox}$ and $\mathcal{E}_s$ are the electric fields across the oxide and silicon channel. For the expression of the $Q_n(y)$ throughout the channel, the surface potential $\Psi_s$ at strong inversion is given as

$$\Psi_S(y) \approx \Delta\Psi_i(y) + 2\Psi_B \tag{2.25}$$

where $\Delta\Psi_i$ is the channel potential with respect to the source end. At the drain end, $\Delta\Psi_i = V_D$. The electric fields can be expressed as

$$\mathcal{E}_{ox} = \frac{V_G - \Psi_S}{t_{ox}} \quad \text{and } \mathcal{E}_S = \sqrt{\frac{2qN_A\Psi_S}{\varepsilon_S}} \tag{2.26}$$

Solving Equation 2.24 for $Q_n(y)$ by using Equation 2.25-26 yields

$$|Q_n(y)| = [V_G - V_{FB} - \Delta\Psi_i(y) - 2\Psi_B]C_{OX} - \sqrt{2\varepsilon_S q N_A[\Delta\Psi_i(y) + 2\Psi_B]}. \tag{2.27}$$

In Equation 2.27 $V_G$ is replaced with $V_G$-$V_{FB}$ in order to compensate the voltage shift due to the oxide charges and work function difference. Now it is possible to define the channel current at any y position along the channel, such that [40],

$$I_D = W|Q_n(y)|v(y) \tag{2.28}$$

where W is the channel width and v(y) is the average carrier velocity. Solving Equation 2.28 using Equation 2.27 results for $I_D$ at the drain edge

$$I_D = \frac{W}{L}\mu_n C_{ox}\left\{\left(V_G - V_{FB} - 2\Psi_B - \frac{V_D}{2}\right)V_D - \frac{2}{3}\frac{\sqrt{2\varepsilon_S q N_A}}{C_{ox}}\left[(V_D + 2\Psi_B)^{3/2} - (2\Psi_B)^{3/2}\right]\right\}. \tag{2.29}$$

where $\mu_n$ is the carrier mobility which is assumed to be constant along the channel. According to Equation 2.29, for a given $V_G$ the drain current increases linearly with drain voltage (linear region), then gradually levels off (non-linear region), reaches a peak point (beginning of the saturation region) and drops with $V_D$. This drop of is the evidence of the vanished inversion layer at the drain side due to the applied $V_D$. Equation 2.29 is valid only for values of $V_D$ for which the inversion layer still exists. Therefore, for a complete explanation of an I-V characteristics it is better to explain the linear and saturation regions with separate equations, such as: for small $V_D$ Equation 2.29 could be linearized which gives explanation for nonsaturation as

$$I_D = \frac{W}{L}\mu_n C_{ox}\left(V_G - V_T - \frac{V_D}{2}\right)V_D \tag{2.30}$$

with the threshold voltage, $V_T$ , given by

$$V_T = V_{FB} + 2\Psi_B + \frac{2\sqrt{\varepsilon_S q N_A \Psi_B}}{C_{ox}} \tag{2.31}$$

For larger $V_D$, that is $V_D > V_D$(saturation), Equation 2.29 describes saturation by

$$I_{Dsat} = \frac{1}{2n}\cdot\frac{W}{L}\mu_n C_{ox}(V_G - V_T)^2 \tag{2.32}$$

where n is the body factor and equal to $1+C_D/C_{ox}$ with $C_D$ depletion layer capacitance which is given in Equation 2.18. Combining Equation 2.30 and 2.32 provides the complete explanation of the I-V characteristics as shown in Fig. 2.7 (a) for variable $V_D$ (output) and (b) for variable $V_G$ (transfer). In both cases, increasing the second variable ($V_G$ for output, and $V_D$ for tranfer) yields to an increase in the drain current $I_D$.

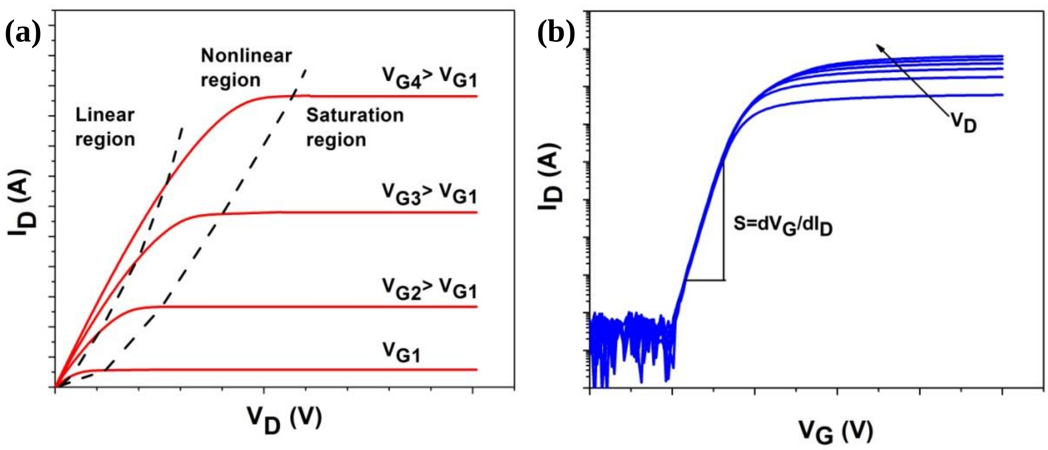


**Figure 2.7:** (a) Current-drain voltage (Output) characteristics of a MOSFET defined with different regions. (b) Current-gate voltage (Transfer) characteristics in a logarithmic scale of a MOSFET.

# 2.4 Electrical characterization

This part is devoted to the explanation of characterization techniques which are needed for the complete analysis of rare-earth based ternary oxide MOS capacitors and MOSFET devices. For the MOS capacitor analysis high frequency C-V measurements are used. The extraction of the equivalent oxide thickness (EOT), κ values, and defect related oxide layer is all carried out from the C-V curves. The I-V curves obtained from MOSFET devices are used to derive the subthreshold slope S, threshold voltage $V_T$ and, together with a split C-V measurement to extract the carrier mobility.

## 2.4.1 MOS Capacitor characterization

**EOT and the dielectric constant κ:**

C-V curves provide all the necessary information about the dielectric material. Once the C-V curves of MOS capacitors formed with different high-κ dielectric thicknesses ($t_{high\text{-}\kappa}$) are obtained, it is possible to calculate the capacitance equivalent thickness CET from the maximum capacitance $C_{acc}$ as

$$CET = \frac{A\varepsilon_o\kappa_{SiO_2}}{C_{acc}} = \frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}} t_{high-\kappa} \tag{2.33}$$

where A is the area of the gate capacitor, $\varepsilon_o$ is the permittivity of the vacuum and $\kappa_{SiO_2}$ and $\kappa_{high-\kappa}$ the dielectric constant of $SiO_2$ and the high-$\kappa$, respectively. CET is the theoretical thickness of $SiO_2$ that is needed to achieve the equivalent capacitance density the high-$\kappa$ capacitor. Due to the reaction with the underlying silicon, there could exist a lower-$\kappa$ interfacial layer (IL) which reduces $C_{acc}$, and therefore, increases CET. Adding this IL to the obtained capacitance will result in

$$CET = \frac{A\varepsilon_o\kappa_{SiO_2}}{C_{acc}} = \frac{\kappa_{SiO_2}}{\kappa_{IL}} t_{IL} + \frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}} t_{high-\kappa} \tag{2.34}$$

where $\kappa_{IL}$ and $t_{IL}$ are the dielectric constant and the thickness of the IL layer, respectively. CET does not contain quantum mechanical and depletion effects from the silicon substrate or the gate. According to Guha et al. [43] this effect causes a reduction of ~ 0.3-0.4 nm of CET which corresponds to the equivalent oxide thickness EOT.
The high-$\kappa$ dielectric constant can be extracted disregarding the contribution of the IL from the plot of EOT (obtained from CET-0.4 nm) as a function of physical oxide thickness. The slope m of the linear fit is related to the $\kappa_{high-\kappa}$ as

$$\kappa_{high-\kappa} = \frac{\kappa_{SiO_2}}{m} \tag{2.35}$$

On the other hand, the intercept of the linear fit on EOT axis represents the electrical thickness of the lower-$\kappa$ IL.

**Extraction of $D_{it}$ from high frequency C-V:**

Due to the consumption of the majority carriers by the interface traps, it takes more charges or applied voltage to accomplish the same $\Psi_s$ as the ideal one. Therefore, the shoulder of the C-V curve is stretched out along the voltage axis. By comparing the theoretically ideal C-$\Psi_s$ curve with an experimentally measured C-V the functional dependence of the surface potential $\Psi_s$ on the gate voltage, V can be found.
For the derivation of the theoretically ideal capacitance, the doping concentration $N_A$ and the oxide capacitance $C_{ox}$ are extracted from the experiment. $C_{ox}$ is the maximum capacitance in the experimental C-V. $N_A$ is derived from the slope of the linear portion of $1/C^2$ (V) curve as [12]

$$N_A = -2 \cdot \left[ q\varepsilon_S \frac{d}{dV_G}\left(\frac{1}{C^2}\right)\right]^{-1} \quad (2.36)$$

Once the $C_{ox}$ and $N_A$ are known, the theoretical capacitance is calculated from Equation 2.15 through 2.17. Figure 2.8 (a) and (b) represents how the $\Psi_s$-V data points are extracted from theoretically calculated normalized C-$\Psi_s$ and experimentally measured normalized C-V curves. These $\Psi_s$-V data points finding is repeated for every $C/C_{ox}$ values on the graphs, and then plotted as $\Psi_s$ vs gate voltage V (not shown).

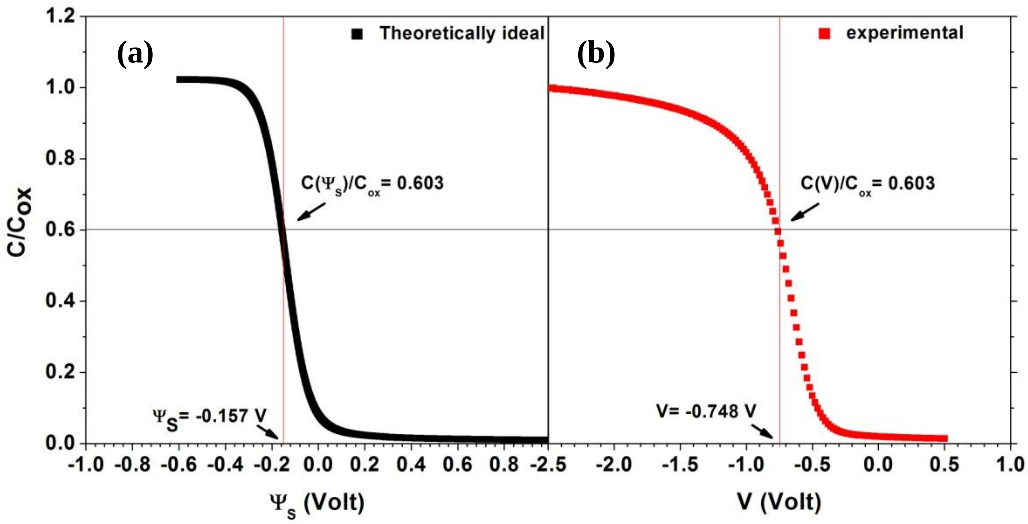


**Figure 2.8:** (a) Theoretically ideal normalized capacitance vs surface potential $\Psi_s$ and (b) experimental high frequency normalized capacitance as a function of voltage. For same capacitances, the corresponding (V,$\Psi_s$) data value are selected.

Finally, using $C_{ox}$, the slope, $\frac{d\Psi_S}{dV}$, and the semiconductor depletion capacitance, $C_{D,}$ for the extracted $\Psi_s$ from the C-V curves (Equation 2.17), the interface trap capacitance $C_{it}$ is calculated as [12]

$$C_{it} = C_{ox}\left[\left(\frac{d\Psi_s}{dV}\right)^{-1} - 1\right] - C_D(\Psi_s) \quad (2.37)$$

and the density of interface states $D_{it}$ is found as [40]

$$D_{it} = \frac{C_{it}(\Psi_s)}{q^2} \quad (2.38)$$

In order to investigate the distribution of the traps over the band-gap, one should define how the band bending, $\Psi_s$, is related to a given position in the semiconductor band-gap. The energy level of the interface trap states $E_T$ above the valence band $E_V$ in a p-type semiconductor is given as

$$\frac{E_T - E_V}{q} = \frac{E_g}{2} + \Psi_S - \Psi_B \tag{2.39}$$

Using the equation given above, the semiconductor band-gap is scanned from $E_T$-$E_V$=0 to $E_T$-$E_V$=$E_g$ by varying $\Psi_S$, where $\Psi_S$ is the surface potential extracted from the C-V curves as a function of applied voltage. Finally, $D_{it}$ as a function of $E_T$-$E_V$ is plotted.

**Extraction of $D_{it}$ from conductance:**

As mentioned above, the interface trap states interact with the semiconductor valence band or conduction band by capturing or emitting majority carriers. Considering, both, p and n-type semiconductor in accumulation, an energy loss occurs when majority carrier holes or electrons at higher average energy are captured by interface trap states at a lower average energy level. On the other hand, in depletion, holes or electrons in filled interface trap states will be in a higher average energy level than those in the semiconductor. As the holes or electrons are emitted by the interface trap states into the semiconductor, they will again lose energy. These energy losses should be supplied by the applied voltage, which is measured as an equivalent parallel conductance $G_p$. For a ω applied frequency, the resultant loss $G_p$ versus gate voltage V curve consists of a peak, which provides $D_{it}$ as [44]

$$D_{it} = \frac{2.5(G_p/\omega)|_{max}}{qA} \tag{2.40}$$

**Extraction of the effective metal gate work function $\Phi_{m,eff}$ and the number density of oxide charge $N_{ox}$:**

The effective work function of the metal gates on high-k dielectrics have been reported to be different from their vacuum level [45]. Therefore, the metal work function calculation is needed for a proper explanation of the flat band and threshold voltage. The extracted new work function is called effective work function.

For the extraction, one needs to know $V_{FB}$, which can be extrapolated from the $1/C^2$ graph as a function of gate voltage. The intercept with the x-axis of a linear fit on the depletion region is the $V_{FB}$ [12]. Taking into account Equation 2.1 and 2.23, by plotting $V_{FB}+\Phi_s$ as a function of CET, a linear behavior is observed. The intercept on the y axis of the linear fit of the curve provides the effective work function of the metal gate, while the slope m of the fit gives the number density $N_{ox}$ of the oxide charge as [46]

$$N_{ox} = \frac{1}{q}\kappa_{sio_2}\varepsilon_o m \tag{2.41}$$

## 2.4.2 MOSFET characterization

**Threshold voltage:**

Because it is the minimum voltage required for switching the device on, the threshold voltage $V_T$ possesses importance in device operation in terms of switching speed. Due to the nonlinear behavior of the $I_D$-$V_G$ curve, it is not possible to make a unique definition for $V_T$. An overview for different $V_T$ measurement techniques is given in REF [41]. In this work a linear extrapolation technique is used for the extraction of $V_T$. According to this technique, for an applied $V_D$, $I_D$ versus $V_G$ curve is extrapolated to $I_D$=0, and the extrapolated $V_G$ value is the $V_T$+$V_D$ determined from the intercept $V_G$ as shown in Fig. 2.9. However, this technique is sensitive to series resistance and mobility degradation. Therefore, it is applied only for $V_D$<<$V_G$ where the series resistance is negligible, and to eliminate the mobility degradation effect the extrapolation is done around a max $I_D$ which is deduced from the maximum peak point in transconductance $g_m$.

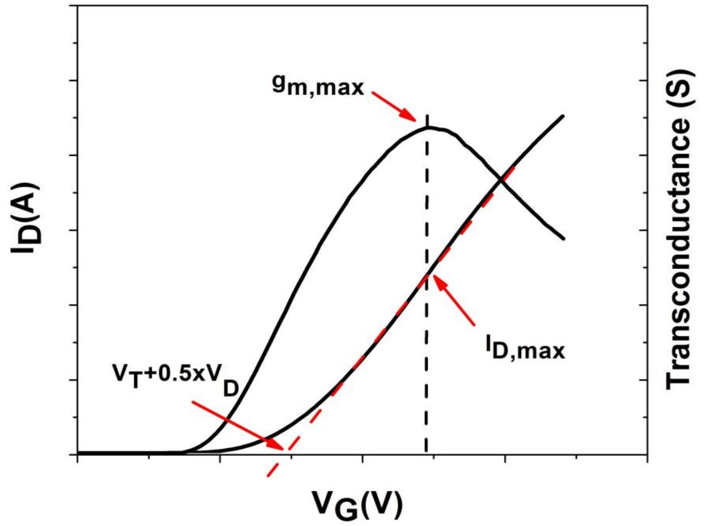


**Figure 2.9:** Threshold voltage $V_T$ determination by the linear extrapolation technique.

**Subthreshold Slope:**

The region below $V_T$ is called subthreshold region and defines how fast the drain current $I_D$ increases with the gate voltage. In this region, the parameter which quantifies the gate voltage induced rapid change in $I_D$ is called the inverse subthreshold slope S. S is the voltage required to increase the current by one order of magnitude and is defined as

$$S = \left(\frac{dlog(I_D)}{dV_G}\right)^{-1} = \ln(10)\frac{k_B T}{q}\left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) \tag{2.42}$$

Figure 2.7 (b) illustrates the determination of S from the logarithmic scale of the $I_D$-$V_G$ characteristic. The minimum theoretical value of S at room temperature is determined to be 60 mV/decade. However S is related to the interface trap density as indicated in Equation 2.42, which requires very small Cit to approach the theoretical value. S provides significant information about the trap states.

**Carrier Mobility:**

An electric field along the channel causes the carriers to drift in the channel with a certain drift velocity υ, which is related to the electric field by a parameter called mobility. Due to the defect charge within the oxide and the impurities within the semiconductor the carriers are involved in collisions. The mobility is given as

$$\mu = \frac{q\tau_m}{m^*} \tag{2.43}$$

where τ is the momentum relaxation time, that is the time between two scattering events, and $m^*$ is the effective mass [47]. It is clear from the Equation 2.43 that, the higher the charge defect or impurities the lower the τ will be, hence, lower mobility. On the other hand, increasing the effective mass $m^*$ will also lower the mobility, which is the reason why electron mobility is higher than the hole mobility. In this work two methods have been used for the extraction of mobility. The first one is the well known split C-V method and the second is the $I_D/\sqrt{g_m}$ [48] method.

**Split C-V technique:** Using Equation 2.30, the effective mobility in a MOSFET can be obtained as

$$\mu_{eff} = \frac{L}{W}\frac{I_D}{Q_{inv}V_D} \tag{2.44}$$

where $Q_{inv}$ is the inversion charge density obtained from the integration of split C-V inversion charge capacitance $C_{gc}$ (gate to channel capacitance) over gate voltage. For a uniform channel charge, $V_D$ is typically~50mV.

Figure 2.10 illustrates the measurement set up for split C-V measurements. The measured capacitance is the sum of the parasitic capacitance $C_p$, overlap capacitance $C_{ov}$ and gate to channel capacitance $C_{gc}$. For the elimination of $C_p$ and $C_{ov}$ a correction suggested in Ref [49] is applied to the measured capacitance as

$$C_{gc}(V_g) = \frac{C_{L_2}-C_{L_1}}{L_2-L_1}L_2 \,, \tag{2.45}$$

where $C_{L2}$ and $C_{L1}$ are the capacitances measured from MOSFETs with different $L_1$ and $L_2$ gate lengths. The effective mobility is then extracted from the corrected C-V after replacing $I_D$ by

$$I_D = 1/(1 - \frac{R_{sd}I_D}{V_D}) \,, \tag{2.46}$$

where $R_{sd}$ is the series resistance extracted according to Ref [41].

***$I_D/\sqrt{g_m}$* technique:** According to the empirical model used in Ref [50], for state of the art MOSFETs operated in linear region, it is suggested to use

$$I_D = \frac{\mu_o}{1+\theta(V_G-V_T-\frac{V_D}{2})}\frac{W}{L}C_{ox}\left(V_G - V_T - \frac{V_D}{2}\right)V_D \tag{2.47}$$

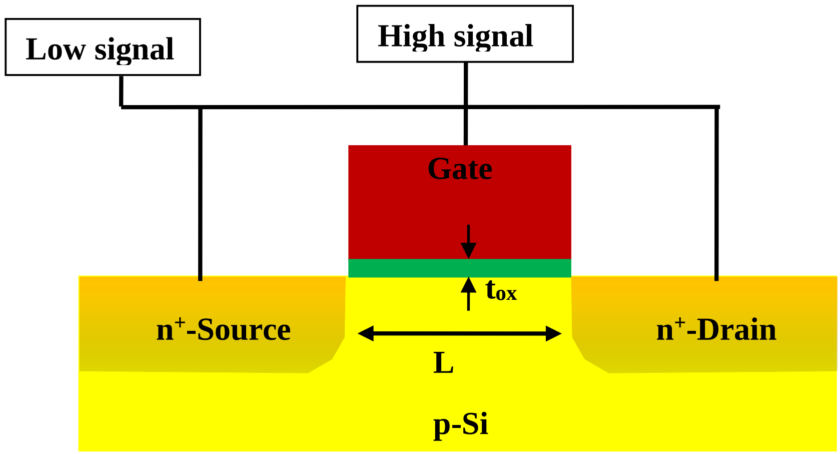


**Figure 2.10:** Measurement set up for inversion charge capacitance $C_{gc}$.

where $\mu_o$ is the low field mobility and $\theta$ the mobility reduction coefficient. The $I_D/\sqrt{g_m}$ technique is based on the combination of $I_D(V_G)$ and $g_m(V_G)$ characteristics and allows to obtain the low field mobility $\mu_o$ without the influence of the series resistance $R_{sd}$ and gate voltage. Plotting $I_D/\sqrt{g_m}$ vs $V_G$ results in a straight line whose intercept to the x axis is $V_T+V_D/2$ (which is known as the charge threshold voltage, and represented with $V_t$) and whose slope A is proportional to $\mu_o$. After the extraction of the whole slopes A for different gate length L, the extracted slope m in the graph of 1/A as function of gate length L is related to $\mu_o$ as

$$\mu_o = \frac{L}{W}\frac{m^2}{C_{ox}V_D} \quad (2.48)$$

It is clear from equation 2.47 that the effective mobility is given as

$$\mu_{eff} = \frac{\mu_o}{1+\theta(V_G-V_t)} \quad (2.49)$$

where $\theta$ is given as [48]

$$\theta = [I_D/(g_m(V_G - V_t)) - 1]/(V_G - V_t) \quad (2.50)$$

A typical variation of $\theta$ as a function of gate voltage $V_G$ is presented in Fig. 2.11. $\theta$ increases with $V_G$ and reaches a saturation only at high voltages, which is the indication of strong inversion. Only this saturation value is used for a correct determination of $\mu_{eff}$. However, since the calculated $\mu_{eff}$ will be voltage dependent, an $R_{sd}$ correction should be done on $I_D$ as indicated in Equation 2.46.

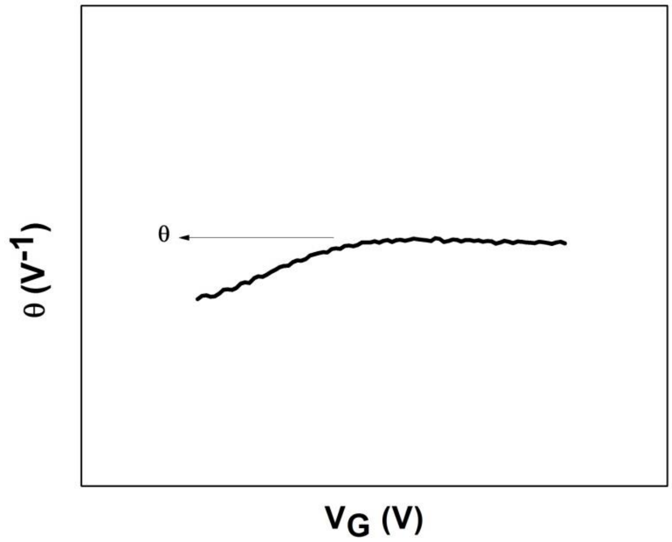


**Figure 2.11:** Typical variation of $[I_D/(g_m(V_G - V_t)) - 1]/(V_G - V_t)$ with gate voltage providing the value of θ.

# 2.5 High-κ dielectrics

Due to the need for low power and high speed application small EOT becomes extremely important. Downscaling of the oxide thickness has shown that it is no longer possible to continue with the ultrathin ~1.3 nm native oxide $SiO_2$. Below this thickness, the key dielectric parameters of $SiO_2$ degrade; boron penetration from the polysilicon gate, gate leakage current and channel mobility becomes critical, all of which shatter the device reliability. Figure 2.12 shows that, as the $SiO_2$ gate oxide thickness is decreased, while the gate leakage constantly increases, however, the drain current first increases and then falls off [16]. This trend, for reduced $SiO_2$ thickness, makes the further progress in CMOS application impossible. The problems encountered in $SiO_2$ below 1.5 nm are listed and reviewed in detail in Ref. [13, 22, 51].

Due to the problem faced with $SiO_2$, it was clear that $SiO_2$ could not survive the challenge of EOT≤1 nm. According to Equation 2.16, where the normalized $C_{ox}$ to the gate area is defined as $\varepsilon_{ox}/t_{ox}$ ($\varepsilon_{ox}=\varepsilon_o\kappa$) , if $SiO_2$ ($\kappa$=3.9) would be replaced with a high-$\kappa$ material, the same $C_{ox}$ could be obtained with a physically thicker oxide and potentially lower leakage as demonstrated by many research groups [22, 52, 53]. However, before the implementation of the new high-$\kappa$ into the CMOS application, the material should satisfy many requirements. These are [13, 31, 52];

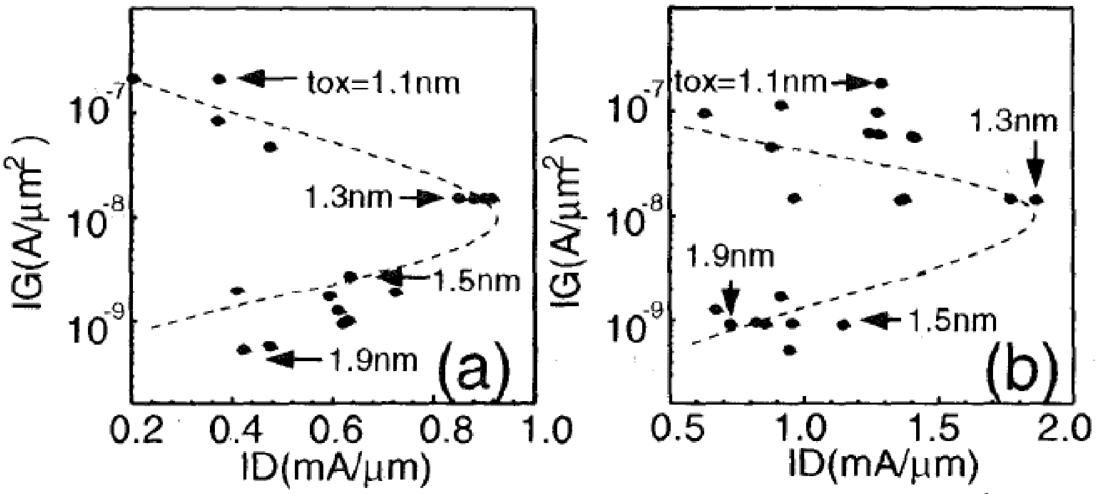


**Figure 2.12:** n-MOSFET gate leakage current vs drain current for (a) $L_g$=140 nm and (b) $L_g$=70 nm (taken from ref [16]).

High dielectric constant and high optical band gap and band offset:
High dielectric constant is needed to provide the same capacitance with a thicker gate oxide. This will not only reduce the tunneling current, but will also allow scaling to lower values of EOT. A large band gap, combined with a large conduction and valence band offset ($\Delta E_C$ and $\Delta E_V$) to silicon is among the requirements in order to prevent the carrier tunneling from Si to the gate or vice versa. This will eliminate the high leakage current and oxide breakdown. $\Delta E_C$>1 and $\Delta E_V$>1 are needed [54]. These criteria restrict the oxides to those of high band gap, such as $E_G \geq 5$ eV. Because the $\kappa$ value tends to vary inversely with the band gap (see Fig. 1.2) the lowest limit of the needed band gap set a limit to the materials candidate with maximum $\kappa$ values around 25 to 35. Materials with higher $\kappa$ value tend to show high leakage current.

Thermodynamic stability in direct contact with Si:
If the high-$\kappa$ is unstable in contact with Si, then a IL would be formed at the high-$\kappa$ Si interface. This undesired interfacial layer has a lower $\kappa$ value and reduces the overall effective dielectric constant, which eventually limits the highest possible gate stack capacitance or equivalently the lowest achievable EOT.

Interface quality:
In a MOSFET device, the carriers are flowing in the channel in direct contact with the IL. Therefore, to ensure high mobility it is important to have a high quality interface in terms of surface roughness and interface charge defects. For the $SiO_2$ the $D_{it}$ is always in the range of $10^{10}$ $(eVcm^2)^{-1}$. However, most of the reported high-$\kappa$ dielectrics show rather high $D_{it}$~$10^{11}$-$10^{12}$ $(eVcm^2)^{-1}$.

Film morphology:
It is preferred to have an amorphous structure after device integration since poly crystalline structure can result in a non-uniform oxide layer and leakage path generation which finally results in an even higher leakage current. Most of the high-$\kappa$ dielectrics are in amorphous state when they are deposited. However, after high temperature treatment they transform into polycrystalline form. Therefore, a high crystallization temperature over 1000 ºC, which is the temperature of device processing, is preferred. Because of their higher-$\kappa$, epitaxial oxides could also be used, but the difficulties encountered during growth and possible lattice mismatch makes these type of oxides unfavorable.

Gate and process compatibility:
For a desired threshold voltage $V_T$, there shouldn't be any reaction between the high-$\kappa$ dielectric and the top gate. That is, the material should be compatible with Si or metal gates. The published results show that, many of the high- $\kappa$ investigated up to now require metal gates.

The deposition process is also important for the determination of the film properties and quality. Although different deposition processes might yield to different results, the process should be CMOS compatible.
According to these requirements, many high-$\kappa$ dielectrics have been experimentally and theoretically investigated for more than two decades [55, 56, 57, 58]. Significant progress has been achieved in terms of the screening and understanding their material and electrical properties. As a result of the intense research hafnium oxide based materials, such as $HfO_2$, $HfSi_xO_y$, $HfSi_xO_yN_z$ were proven to be the leading candidate to replace $SiO_2$. The harvest of this intense work was collected by Intel, in their first 45 nm technology node [23], and later in 32 nm technology node [24], using an appropriate metal gate instead of poly-Si. Replacement of $SiO_2$ with $HfO_2$ based material was a milestone in the development of IC and the researcher are still working on both reducing EOT in $HfO_2$ based materials and alternative gate dielectrics. For a lower EOT, considerable work was done on optimized Si surface preparation [59] and replacing of $SiO_2$ interfacial layer by passivating $HfO_2$ based oxide bottom IL with a metal oxide [60, 61], such as $SrTiO_3$. The aim in capping the bottom IL is to improve the total capacitance by the higher-$\kappa$ metal oxide layer. Another way of achieving lower EOT is, reducing the physical thicknes of IL via remote scavenging effect. In this process, after oxide and metal gate deposition, the metal is doped [60, 62] or just capped [63] with a certain metal, providing that the interface to the high-$\kappa$ is not effected by that metal. An EOT down to 0.42 nm was achieved with these processes however the leakage current is almost equal to 1 $A/cm^2$. This high leakage current could be overcome by using a higher-$\kappa$ dielectrics which could allow long term scaling with lower EOT and leakage current with a thicker oxide layer. It seems that, no scaling is forever, and $HfO_2$ based materials will face an end as $SiO_2$.
According to ITRS potential solutions for thin films are given in Table 1 [5]. It is obvious from the table that deposition tools & methods need continuous improvement and strained Si for high mobility is likely to be used even after 2020. Continuous improvement on Hf

based oxide is obvious till the year of 2017, however; higher-$\kappa$ dielectrics ($\kappa$>30) should also be in full production by the year of 2015. That is, the two years of process qualification and pre-production should be completed before that year.

**Table 1:** Potential solutions roadmap for CMOS (from ref. [5]).

| First year of IC production | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Hf based high-κ (High-κ and interface layer scaling) | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | | | |
| Higher-κ (κ>30, and band offset>1 eV) | Research required | Research required | Development underway | Development underway | Development underway | Qualification/pre-production | Qualification/pre-production / Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement |
| High-κ on non-Si high mobility channels (Si-Ge, III-V) | Research required | Research required | Research required | Development underway | Development underway | Development underway | Development underway / Qualification/pre-production | Qualification/pre-production | Qualification/pre-production | Continuous improvement | Continuous improvement | Continuous improvement |
| Near mid-gap tunable WF electrodes | Research required | Research required | Development underway | Development underway | Development underway | Qualification/pre-production | Qualification/pre-production / Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement |
| Deposition tools and methods | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement |
| Strained Si for high mobility (local strain from contact etch stop, elevated SiGe-SiC S/D, stress memorization, replacement gate) | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement | Continuous improvement |

Research required (black)
Development underway (blue)
Qualification/pre-production (yellow)
Continuous improvement (green)

## 2.5.1 Rare-earth based ternary oxide

Although Hf-based materials have been implemented since the 45 nm technology generation, high leakage current in scaled oxide urge the use of higher-$\kappa$ dielectrics. Many high-$\kappa$ dielectrics have been investigated as potential candidates. However, due to their high dielectric constant and high band gap, which is the evidence of high band offset, rare earth ( RE: Gd, Sc, La..) based ternary oxides ($LaLuO_3$, $DyScO_3$, $TbScO_3$…, see Fig. 1.2) have attracted the highest attention for high-$\kappa$ application. Therefore, in this study, as a member of rare-earth ternary oxide, $LaLuO_3$, and three rare earth scandates ($REScO_3$) $LaScO_3$, $TbScO_3$ and $SmScO_3$ will be investigated as potential high-$\kappa$ dielectrics.

**Lanthanum lutetium oxide as high-*κ* candidate**

Recent results indicated that $LaLuO_3$ is a promising higher-*κ* dielectric with a *κ* value of 32 in the amorphous state [32]. It shows excellent thermodynamic stability on silicon (>1000 ºC) [32]. It fulfills the requirements with large optical band gap (> 5.5 eV), and large conduction and valence band offsets of 2.1 eV [31, 32] . Wang *et al.* [64] achieved, by atomic layer deposition (ALD) high quality $LaLuO_3$ films on Si without a detectable interfacial layer. They obtained an EOT of 0.86 nm, which showed two orders of magnitude lower leakage currents than that of the $SiO_2$ with the same EOT. Following our study, Mitrovic et al. [65] have investigated MBD grown $LaLuO_3$ using TiN/$LaLuO_3$/Si gate stack. They obtained, an EOT of 0.75 nm with a 7 orders of magnitude lower leakage current than that of $SiO_2$ with the same EOT. Using X- ray photo electron spectroscopy (XPS) and electron energy loss spectra (EELS) they observed, however, a dual silicate/$SiO_2$ like IL at the $LaLuO_3$-Si interface. Our study on both $LaLuO_3$ [66] and $HfO_2$ [67] showed that, $LaLuO_3$ provide with smaller leakage current for a comparable EOT. Despite the observed IL, the obtained low EOT and leakage current favor the idea of using this material for the 14-12 nm technology node.

In the meanwhile to this study, $LaLuO_3$ layers, grown by ALD, have been also used for Ge devices, providing good results [68]. On the work done on p-MOSFETs fabricated on sSi/$Si_{0.5}Ge_{0.5}$/sSOI heterostructure, MOSFETs with $LaLuO_3$ show similar mobility characteristics as the one with $HfO_2$ [69].

**Rare-earth scandates**

Starting from 1954 till 1981 many researchers have synthesized and studied the crystallographic structure of many $REScO_3$ [70, 71, 72, 73]. The first synthesizing of the entire series of $REScO_3$ were done by Liferovich et al. [74] . Using powder X-Ray diffraction data, they compared $REScO_3$ crystal chemistry with that of $REFeO_3$ orthoferrite series. They found that, $REScO_3$ are orthorhombic perovskites, adopting space group of Pbnm (#62). On the other hand, due to their narrow diffraction reflections, structural perfection and homogeneity, single crystal $REScO_3$ grown by Czochralski technique are considered to be one of the best substrates for the epitaxial growth of perovskite thin films [75].

The dielectric properties and crystallization behavior of entire $REScO_3$, formed by pulsed laser deposition (PLD) on a $LaAlO_3$ substrate, were investigated by Christen et al [56]. They observed varying crystallization temperature depending on the RE atomic number. The crystallization temperature varies between 650 and 800 for relatively thick films (>200 nm). These investigated dielectrics present band gaps higher than 5.5 eV in the crystalline phase. Another interesting result of their study is these dielectrics show *κ*>30 when they crystallize. They observed the highest *κ* value for $TbScO_3$, *κ*~39, which is followed by $SmScO_3$, *κ*~37.

The electron energy band alignment between Si and several $REScO_3$ ($LaScO_3$, $GdScO_3$ and $DyScO_3$, all in amorphous form) is determined by Afanas'ev et al [76], using internal photoemission and photoconductivity measurement. They observed nearly the same band gap for all investigated dielectrics, ~ 5.6-5.7 eV. The measured conduction and valence band offset at the Si-dielectric interface are 2.0±0.1 and 2.5±0.1, respectively. Similar band gap properties for the same dielectrics were also observed by Heeg et al. [77] and Cicerella et al. [78]

On the work done on thin (≤20nm) $LaScO_3$, $GdScO_3$ and $DyScO_3$,material deposited on Si substrate by PLD, Zhao et al. have found that, while $LaScO_3$ tends to crystallize at 800 ºC, $GdScO_3$ and $DyScO_3$ remains amorphous up to 1000 ºC. The same result were confirmed for molecular beam deposited (MBD) $LaScO_3$ [79] and e-gun evaporated $GdScO_3$ [53], however, ALD grown $GdScO_3$ exhibited slightly lower crystallization temperature (~900 ºC) as compared to the PLD grown one [80].

The electrical characteristics of $LaScO_3$, $GdScO_3$ and $DyScO_3$ were studied by Zhao et al. [81]. They found that these materials have $\kappa$ values of ~22 and they present almost no hysteresis and frequency dispersion in CV curves. Moreover, the observed leakage currents are similar to that of $HfO_2$ for a comparable EOT. $GdScO_3$ was also studied by Wagner et al, and similar results were found [53].

Lopes et al. [82] have investigated the electrical characteristics of MBD grown $LaScO_3$ at 450 ºC and found a $\kappa$ value of 28. However, when they deposited the film at room temperature the $\kappa$ value is 17, and after applying oxygen annealing at 650 ºC the $\kappa$ value increases to 33 [83]. They observed reduced $D_{it}$ (~$5x10^{11}$ $(eVcm^2)^{-1}$) and almost eliminated hysteresis after oxygen annealing. However, the oxygen annealing resulted in an increase in the IL.

Roeckerath et al. [34] have investigated the electrical properties of e-gun evaporated $TbScO_3$ on HF last Si surface. They observed a $\kappa$ value of 26, small $D_{it}$, negligible hysteresis and leakage current. They have done the integration of $GdScO_3$ [39] into the MOSFETs using SOI and sSOI substrates and $TbScO_3$ [34] using SOI substrate. Before the deposition of the high-$\kappa$ dielectrics, they kept the substrates in HF solution for 30 sec to remove the native oxide and provide a hydrogen terminated surface. High $I_{on}/I_{of}$ ratio over $10^7$, steep subthreshold slope down to 66 mV/dec and mobilities comparable to that of $HfO_2$ were observed.

# Chapter 3

# Rare-earth based high dielectric constant materials

This chapter is devoted to structural and electrical properties of the following rare earth based ternary oxides: $LaLuO_3$, $LaScO_3$, $TbScO_3$ and $SmScO_3$. $HfO_2$ is used as a reference since it is the only high-*κ* dielectric which is now in use for CMOS technology. The films were deposited by MBD for $LaLuO_3$ and $LaScO_3$, by electron beam evaporation (e-gun) for $TbScO_3$, PLD for $SmScO_3$ and ALD for $HfO_2$. Analysis of chemical and physical properties such as film composition, chemical bonding, chemical structure of the interface, and thermal stability will be discussed. Various electrical characteristics including capacitance vs. voltage (C-V), hysteresis, work function, interface and oxide charges of the TiN/High-k/Si MOS capacitors will be presented.

## 3.1. Sample preparation

For the sample preparation p-type doped (100) Si with a resistivity of 1-10 Ωcm, which corresponds to a $10^{15}$-$10^{16}$ $cm^{-3}$ Boron concentration, was used as a substrate. Before film deposition, RCA cleaning [84] was carried out in order to clean the Si surface and form an approximately 1 nm chemical $SiO_2$ on its top. Films with various thicknesses were deposited as follow;

$LaLuO_3$: deposited by MBD by co-evaporating lanthanum and lutetium from individual effusion cells in an $O_2$ background atmosphere of ~$10^{-6}$ mbar and at a substrate temperature of 450 °C.

$LaScO_3$: deposited by MBD by co-evaporating La and Sc from individual effusion cells in an $O_2$ background atmosphere of ~$10^{-6}$ mbar and at a substrate temperature of 350 °C.

$TbScO_3$: deposited by e-gun from a stoichiometric ceramic target at a pressure of ~$10^{-6}$ mbar and a substrate temperature of 600 °C.

$SmScO_3$: deposited by PLD from a stoichiometric ceramic target in an $O_2$ background atmosphere of ~$10^{-3}$ mbar and at a substrate temperature of 400 °C.

Reference $HfO_2$: deposited by ALD using liquid Tetrakis (EthylMethylAmido) Hafnium $Hf[N(C_2H_5)CH_3]_4$, (TEMAH) with 99.999% purity as the precursor and dry $O_3/O_2$ as the reactive gases in a pressure of ~0.5 mbar and at a substrate temperature of 300 °C.
After film deposition, some of the samples undergo $O_2$ annealing at 400 °C for 10 min (which will be called as post deposition annealing 1 (PDA1)). In addition, some samples, after $O_2$ annealing at 400 °C for 10 min, were exposed to another annealing in forming gas (FG) (90% $N_2$+10% $H_2$) ambient at 400 °C for 10 min. $O_2$ annealing followed by FG annealing will be abbreviated as PDA2. The results obtained from those samples were compared with the as-deposited samples. These samples were used for XPS and TOF-SIMS analyses, and electrical characterization.

# 3.2. Structural characterization

## 3.2.1 Composition analysis by means of Rutherford backscattering spectrometry (RBS)

Rutherford Backscattering Spectrometry (RBS) is a widely used technique in thin film characterization, in which a target is bombarded with highly energetic (typically 0.5-4 MeV) helium ions (an elastic collision) and the backscattered ions provide information about the composition of the material under test, and depth profiling of the individual element. Detailed information can be found in [85]

In a backscattering spectrum, separate peaks on a number of counts versus energy plot refer to the elements contained in the sample. These elements can be determined from the position of the peaks. The width of the peak provides information about the depth profile. In this work, the composition and the depth profile of the rare-earth scandates and $LaLuO_3$ were investigated using 1.4 MeV $He^+$ ions at a backscattering angle of 170°. Figure 3.1 (a) represents the RBS spectrum (measurement) together with its RUMP simulation for $LaScO_3$ thin film. As expected, among the elements within the sample, since La has the highest mass, it appears in the higher energy part of the spectrum. On the other hand, the high energy edge of the La peak in the spectrum stands for the surface of the film while the low energy edge stands for the interface. Therefore the width of the peak provides information about the depth. Furthermore, the concentration of the elements can be obtained from the height of the peaks. Using the RUMP simulation a compositional ratio of La:Sc:O=1:0.95:2.8, which is very close to the stoichiometric value, was determined. Similar results were also obtained for $LaLuO_3$ [32], $TbScO_3$ [34] and within this work for $SmScO_3$. In order to investigate the reaction after the forming gas (FG, 90 % N + 10% H) annealing, RBS spectra of $TiN/TbScO_3/Si$ system with and without forming gas are plotted in figure 3.1 (b). After the FG a small increase from 2.7 to 2.8 was observed in the ratio of the oxygen. Apart from that, no clear change was observed in the spectrum. This small change might be due to the change at the film interface. However, by using only RBS, it is not possible to investigate such small changes at the interface.

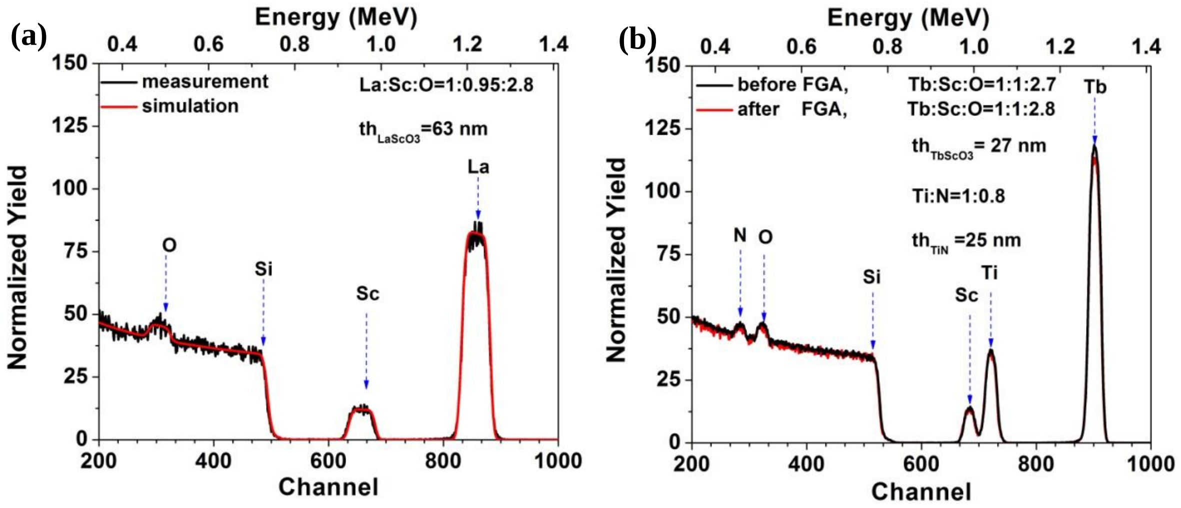


**Figure 3.1:** RBS spectra (a) 63 nm thick $LaScO_3$ films on Si with a RUMP simulation, (b) TiN/$TbScO_3$ on Si before and after a FG annealing.

## 3.2.2 X-ray diffraction (XRD) and X-ray reflection (XRR)

XRR is a non-destructive technique used to investigate density, thickness and surface roughness of thin films, and XRD provides information about the structure of the film. In both of them, depending on which measurement is done, the energetic X-rays can penetrate deep into the film and provide information about the bulk structure without causing any defects. For detailed information see [86].

An example of XRR measurements for four different film thicknesses of $LaLuO_3$ grown on RCA-cleaned Si(100) surface is plotted in Fig. 3.2 (a). After the measurement, the thicknesses of the films were automatically determined via a computer program (X-ray data collector, XRDC) by fitting the XRR curve. The film thickness is proportional to the number of fringes in the XRR curves. This measurement was done for determining the thickness of all high-k films used to form MOS capacitors or MOSFETs.

Because of the possibility of leakage path generation in high-$\kappa$ dielectric application, it is important to keep the film amorphous during device processing. Therefore, the thermal stability of the film is a critical issue. The thermal stabilities of $LaLuO_3$, $LaScO_3$ and $TbScO_3$ were already investigated by ref [32, 34, 81]. It was found that, while $LaLuO_3$ and $TbScO_3$ tend to crystallize at a temperature above 1000 °C -which make these materials very promising for high-$\kappa$ applications- $LaScO_3$ tends to crystallize already at 800 °C. Nevertheless, this temperature is higher than what is observed for $HfO_2$, which fully crystallizes at 550 °C. For $SmScO_3$, the only result about the crystallization temperature of $SmScO_3$ is reported by Christen et al. [56]. They have investigated a very thick film, ≈370 nm, and found a crystallization temperature of 750 °C. However, this might not be valid for thinner films, since the crystallization temperature tends to increase as the film thickness decreases. Therefore, in this work, $SmScO_3$'s thermal stability was investigated for 22 nm thick film by means of XRD. The diffraction pattern is collected by performing a θ/2θ scan. In this case the X-ray source is kept fixed, the sample rotates around θ and the detector moves by 2θ while the scattered intensity I(2θ) is measured. During the measurement, the 2θ was varied from 10° to 80° with step size of 0.02°.

After the film deposition, rapid thermal annealing in ultrapure $N_2$ was performed in atmospheric pressure at different temperatures ranging from 700 °C to 1000 °C for 10 s. Figure 3.2(b) shows the XRD patterns of a 22 nm thick $SmScO_3$ film for different annealing temperatures. The broad peak with low intensity at 30.75° measured for the as-deposited as well as the film annealed at 800 °C samples indicates a fully amorphous

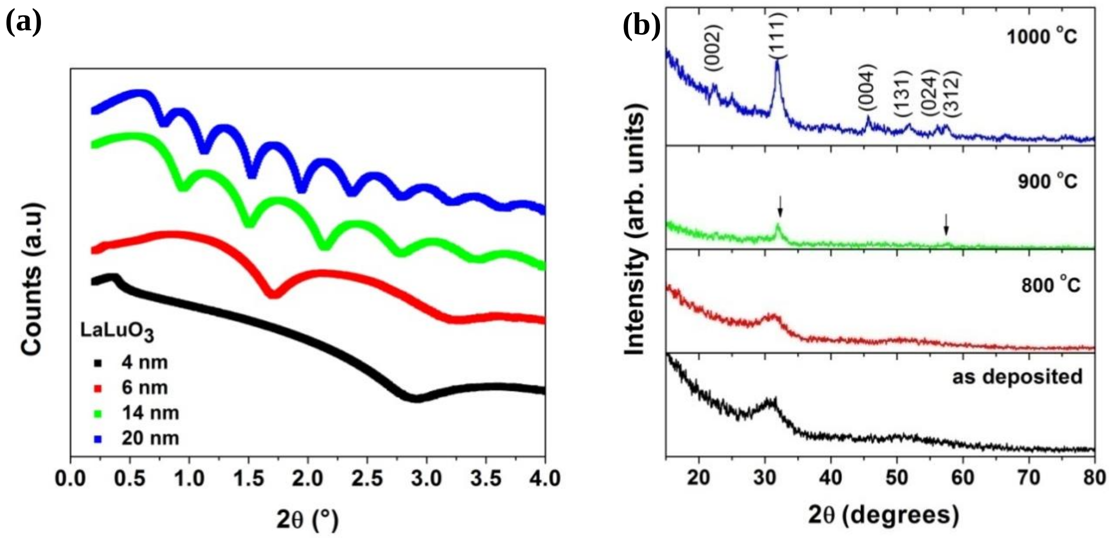


**Figure 3.2:** (a) XRR of $LaLuO_3$ for different thicknesses, (b) XRD patterns of a ~22 nm thick $SmScO_3$ film grown on (100) Si, as-deposited, and after annealing at different temperatures in 1 atm $N_2$ gas for 20 s.

structure. Similar broad peaks were also observed by Roeckerath et al for $TbScO_3$ and $GdScO_3$ [34, 53] and by Adelmann et al for $DyScO_3$ [87]. The origin of this peak is likely to be a short-range order of the atoms in the amorphous solid [86]. The arrangement of the atoms is not fully random and they have a self-volume whose interatomic distances between nearest neighbors compare to those in crystalline structures. Therefore, after the irradiation with monochromatic X-rays a characteristic diffraction pattern would occur.

For films annealed at temperatures above 900 °C the crystallization becomes clear since the sharp Bragg peaks are visible. The peaks seen in the XRD pattern for a film annealed at 1000 °C correspond to the polycrystalline $SmScO_3$ with an orthorhombic structure. No other phases were detected for the investigated annealing temperature. The value for the onset of crystallization is higher than that for $HfO_2$ [88] and comparable to Hf silicates [89].

## 3.2.3 Transmission electron microscope (TEM)

In this study TEM was mainly used to check the amorphous state of the film, investigate the growth of the layers, and study the interfacial layer. The broad peak with low intensity observed in the XRD patterns could also be mixed with the broadening caused by the overlap of neighboring reflections which appear due to very small crystallite size. Then the film would be polycrystalline. To clear up this problem one should investigate the film with an additional technique such as TEM. A cross-sectional TEM image of a 49 nm thick $SmScO_3$ film on Si (100) is shown in Fig. 3.3. It is clearly seen from the inset (also from the main image) that the film is amorphous and smooth. The figure also indicates the existence of an interfacial layer between the silicon and the high-$\kappa$ dielectric with a thickness of 2.5 nm. The growth of the interfacial layer is probably related to the oxidation of the silicon surface during PLD growth.

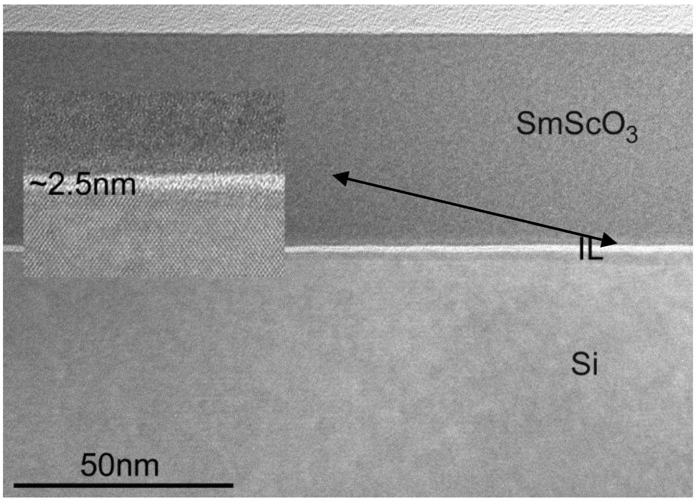


**Figure 3.3:** Cross-sectional TEM micrograph of a 49 nm thick $SmScO_3$ film deposited on (100) Si. The inset shows a close-up of the interlayer, which has a thickness of about

## 3.2.4 Interface investigation by X-ray photoelectron spectroscopy (XPS)

XPS is a powerful analytical method which investigates the surface by irradiating the sample under test with highly energetic photons and analyzing the energy of the ejected electrons emitted from the core levels. Detailed information about XPS could be found in [86].

X-ray photoelectron spectroscopy (XPS 5600, Physical Electronics, USA) were performed using monochromatic AlKα radiation (13kV, 300 Watt). In order to remove any kind of contamination, the surface of the films was cleaned in-situ by $Ar^+$ sputtering at energy of 2kV for 15s before the measurement. Core level spectra of Si2p/Si2s (5.85eV pass energy, 0.025eV per step) were acquired. Core level spectra fitting was done using UNIFIT 2008 after subtraction of a Shirley background and charging correction ($Si^{\pm 0}$ was shifted to 150.7eV depending on substrate composition). Because of the interference of the Si2p core levels with the La4d levels, the Si2s core levels were used to investigate the interfacial layer at $LaLuO_3$ /Si and $LaScO_3$/Si, while Si2p was used for $TbScO_3$/Si samples.
Figure 3.4 shows the Si2s XPS spectra of 3 nm thick as grown and annealed $LaLuO_3$ films deposited on an RCA cleaned Si substrate which contains a thin (~1 nm thick) chemical oxide. For the as deposited sample 4 peaks were observed. The first one at ~150.7 eV is for Si-Si from the Si substrate, the second peak at ~152.5 eV stands for silicate located at the interface of $LaLuO_3$-Si. The third peak at 153.7 eV stands for an oxygen-rich $SiO_x$ and the last peak at 154.8 eV is related to the stoichiometric $SiO_2$. After applying PDA2, no change in the position of the Si and $SiO_2$ is observed, while the peaks related to silicate and $SiO_x$ were shifted by 0.3 and 0.1 eV, respectively, to lower binding energies. This indicates a small oxygen reduction in these layers. Moreover, based on the peaks intensity, it seems that the PDA triggers further reaction between $LaLuO_3$ and Si which results in an increase of the silicate and $SiO_2$ interfacial layer thicknesses. Further detailed XPS analysis on TiN/$LaLuO_3$/Si gate stack has been performed very recently by Nichau et al. [90]. They have found that, homogenously distributed La silicate and Lu silicate at the Si interface are formed during oxide deposition. According to their investigation, the reaction between Si and $LaLuO_3$ is strongly dependent on the annealing duration and temperature. For an annealing temperature of 800 °C they observed a Si rich silicate with a major contribution of La(Lu) silicate, whereas for 1000 °C of annealing temperature a Si rich silicate with a major contribution of oxygen rich compound is observed (eg. $La_2Si_2O_7$). At high temperature transformation of large amount of LuO to Lu silicate and its accumulation at top (with TiN) and bottom (with Si) interfaces is another is also among their observation.
$LaScO_3$ showed a slightly different behavior. While the as-deposited sample showed only silicate formation, after applying PDA2 a combination of both $SiO_2$ and silicate was detected. The observed binding energies for Si and different oxide layers are listed in Table 3.1.

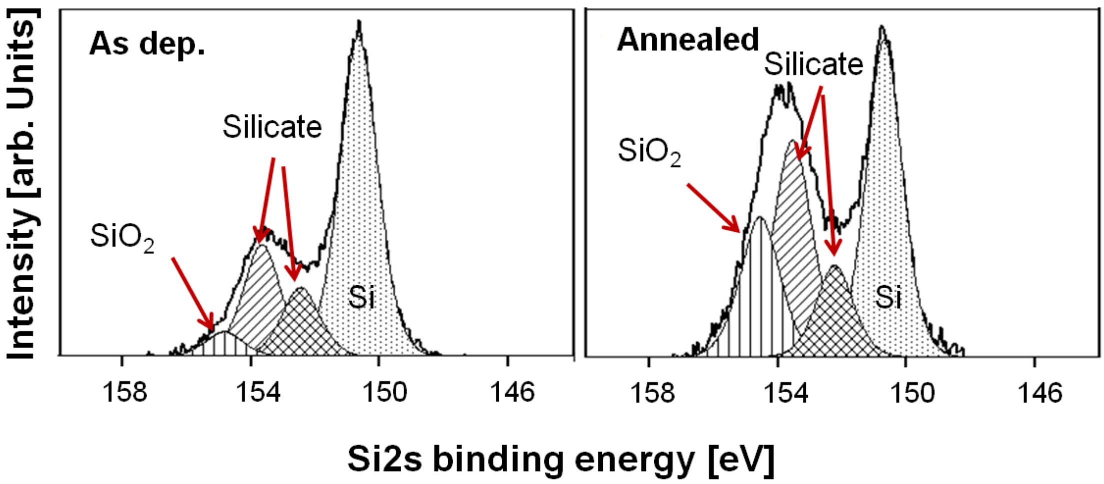


**Figure 3.4:** Fitted core level Si 2s spectra for as deposited and annealed 3 nm thick $LaLuO_3$ films deposited on an RCA last Si surface.

For $TbScO_3$ samples, Si2p core levels were used to investigate the interfacial layer. A 4nm $SiO_2$ thermally grown on Si was used for comparison. In the case of $SiO_2$ on Si, the Si-2p spectra show two peaks which have a shift of 4.3 eV. However, in the case of the as-deposited $TbScO_3$ film, a shift of only 3.2 eV to higher binding energy (BE) relative to Si is observed. This smaller shift suggests the formation of a silicate at the interface. On the other hand, after applying PDA2, the peak is shifted by 3.7 eV to even higher BE, which suggests the existence of an oxygen-richer silicate. However no $SiO_2$ peak was observed. For all oxides, it is noticed that PDA resulted in a growth of interfacial layer.

**Table 3.1:** Binding energy and quantification of the core level compounds

| | **compound** | **$LaLuO_3$/Si as grown** | **$LaLuO_3$/Si PDA2** | **$LaScO_3$/Si as grown** | **$LaScO_3$/Si PDA2** | **TSO/Si as** | **TSO/Si PDA2** |
|---|---|---|---|---|---|---|---|
| Si | $Si^{\pm 0}$ | 150.7 | 150.7 | 150.7 | 150.7 | 99.2 | 99.2 |
| | silicate, $(SiO_3)^{2-}$ | 152.5 | 152.2 | 152.4 | 152.5 | 102.4 | 102.9 |
| | $SiO_x$ | 153.7 | 153.6 | 153.8 | 153.8 | - | - |
| | $SiO_2$ | 154.9 | 154.7 | - | 154.8 | - | - |

A similar study for $LaLuO_3$ was also repeated by Mitrovic et al. [91] where they found exactly the same results. On the other hand, Renault et al. [92] have reported for the $HfO_2$/Si system, where it was mentioned that Hf contributed to form a Si-O-Hf silicate resulting in a peak located at lower BE relative to the $SiO_2$ peak. Furthermore, recently,

Duan et al. [93] have shown that, for $HfO_2/SiO_2/Si$ system, the silicate thickness strongly depends on the $HfO_2$ thickness. For a thicker $HfO_2$, after applying 600 °C annealing, a thicker Hf silicate was observed. It seems that, silicate formation is an unavoidable reaction at the interface. Since silicates of high-κ materials have higher dielectric constant than $SiO_2$, EOT increases less rapidly than with $SiO_2$.
On the other hand, some authors claim that, there is no silicate formation in $HfO_2/Si$ [94]. According to them, the non-stoichiometric $HfO_2$, use the oxygen from the $SiO_2$ to become stoichiometric, instead of forming a silicate. They concluded, even if there is a silicate formation, that the silicate will be decomposed in the non-stoichiometric $Hf_xO_{1-x}$ to form $HfO_2$.

## 3.2.5 Time of flight secondary ion mass spectroscopy (TOF-SIMS)

TOF-SIMS is a surface analytical technique which uses a pulsed ion beam to emit ionized particles (secondary ions) from the surface of the sample and detect them by a mass spectroscope. Comprehensive information could be found in [41].

The TOF-SIMS depth profiling were done in negative secondary ion mode using 1 kV $Cs^+$ primary ions for sputtering and 25 kV $Ga^+$ beam for analysis. 20 nm TiN/6 nm $LaLuO_3/Si$ and 20 nm TiN/6 nm $TbScO_3/Si$ were chosen for TOF-SIMS analyses. For that reason the samples were exposed to different annealing procedures and the reactions taking place at the interface between the layers were studied.

**(a) Analyses of 20 nm TiN/6 nm $LaLuO_3/Si$ gate stacks**

In Fig. 3.5 the depth profiling of $TiN/LaLuO_3/Si$ system for different annealing steps is presented. The depth profiles of La (LaO) and Lu (LuO) are smooth and constant, which indicates that the grown $LaLuO_3$ film has a homogeneous composition. For the as grown film in Fig. 3.3 (a) a strong signal of $SiO_2$ was detected at the interface. This $SiO_2$ signal is likely related to ~1 nm thick $SiO_2$ which is formed as a product of the RCA cleaning. [84]. In addition, a $SiO_2$ signal appearing at the $LaLuO_3$ surface (and which extends into the whole uppermost TiN layer) is also observed. This might be due to Si segregation at the $LaLuO_3$ surface, having as its source Si diffusing either from the $SiO_2$ interfacial layer or from the substrate. Diffusion of Si was also reported by other researchers [62]. However, they also could not identify the detailed mechanisms. On the other hand, the formation of the silicate layer which was observed by XPS is also obvious in TOF-SIMS profile. The two signals coming from LaSiO and LuSiO are located at the interface. Because the LaO and LuO signals starts to decrease before the Si peak position, it seems that the silicate formation occurs due to the reaction with the Si atoms diffusing into the high-$\kappa$ film, rather than by direct reaction with Si substrate. A complementary conclusion was presented by Ono and Katsumata [REF].They have investigated the interfacial reactions between rare-earth metal oxides and silicon substrate and found that, the ionic radii for those oxides could be large enough for the Si to penetrate in, which indeed results in silicate formation. Similar

studies were also done for $Dy_2O_3$, $Sc_2O_3$, $LaAlO_3$, $Al_2O_3$ and $GdScO_3$ where strong Si in-diffusion was observed [87, 95, 96, 97] .
Figure 3.5 (b) shows result for samples with TiN on $LaLuO_3$ with PDA1. After the $O_2$ annealing a shoulder of the LaO and LuO signals on the Si substrate side has appeared (see the arrows indicated with 1 and 2 in the plot). At the same time a similar feature was also observed for the peaks coming from the silicates, $SiO_2$ and left hand shoulder of Si (see the arrows indicated with 3, 4 and 5 in the plot). All this indicates a new reaction between $LaLuO_3$-$SiO_2$ and the diffused Si atoms. At the bottom of the left shoulder of both $SiO_2$ and Si signals (see the arrow indicated with 6 in the plot), peaks with low intensities arise, indicating the accumulation of Si atoms at the interface, which is used for sub-oxide formation. The $SiO_2$ and silicate peaks showed a very small extension, revealing a very small increase in their thicknesses as the Si concentration at $LaLuO_3$ surface raised. This result is also in agreement with the report by Ono and Katsumata [98]. The increase in the interfacial layers thickness is directly correlated with a reduction in the density of interface trap charges, and an increase of the effective oxide thickness (EOT). As the device size shrinks, the traps become more critical since they may degrade the mobility. Therefore, it is important to keep $D_{it}$ below $10^{11}$ $(eVcm^2)^{-1}$.
After applying a FG anneal after PDA1, the $SiO_2$ and silicate peaks in Fig. 3.5 (c) tends to show a much more homogeneous signal, and their widths remained unchanged as compared to PDA1 sample. On the other hand, the $SiO_2$ and Si peaks that were at the bottom of the left shoulder of the $SiO_2$ and Si signals ( arrow indicated with 6 in Fig.3.5 (b)), respectively, as well as the silicates intensities have significantly reduced. This is probably due to the migration of the Si atoms from the interface to the $LaLuO_3$ surface.
Figure 3.5 (d), (e) and (f) show the effect of the post metallization annealing (PMA) on the samples of Figs. 3.5 (a), (b) and (c) respectively. It is clearly seen that, after PMA, the $SiO_2$ signal has descended significantly at the interface, reaching the noise level at the $LaLuO_3$ surface and TiN bulk. This is due to the oxygen scavenging effect of the TiN metal. Ando et al. has used the oxygen-scavenging TiN metal gate in order to scale the EOT via interfacial layer (IL) (scavenging at annealing temperature of 400-600 °C), and to prevent the IL re-growth at higher temperature [62]. Accordingly, the decomposition of the IL proceeds via the following reaction:

$$\frac{1}{2}SiO_2 + V_O \rightarrow \frac{1}{2}Si + O_O \ , \tag{3.1}$$

where $V_O$ is the oxygen vacancy in the $HfO_2$ (the used high-$\kappa$) and $O_O$ is the oxygen atom at the oxygen site of the $HfO_2$. According to this reaction, the oxygen transport from the IL to TiN metal gate is provided by $V_O$, thus, providing the oxygen scavenging. According to their investigation, during the scavenging of the IL, also a small amount of Si from IL has drifted into the bulk high-$\kappa$. As compared to the as grown sample of Fig 3.5 (a), after applying PMA, Fig 3.5 (d), the Si amount in the high-κ has increased during the oxygen drift from $SiO_2$ through $LaLuO_3$ in agreement with Ref. [62]. This actually seems to be a severe problem since it may reduce the effective dielectric constant of the film.

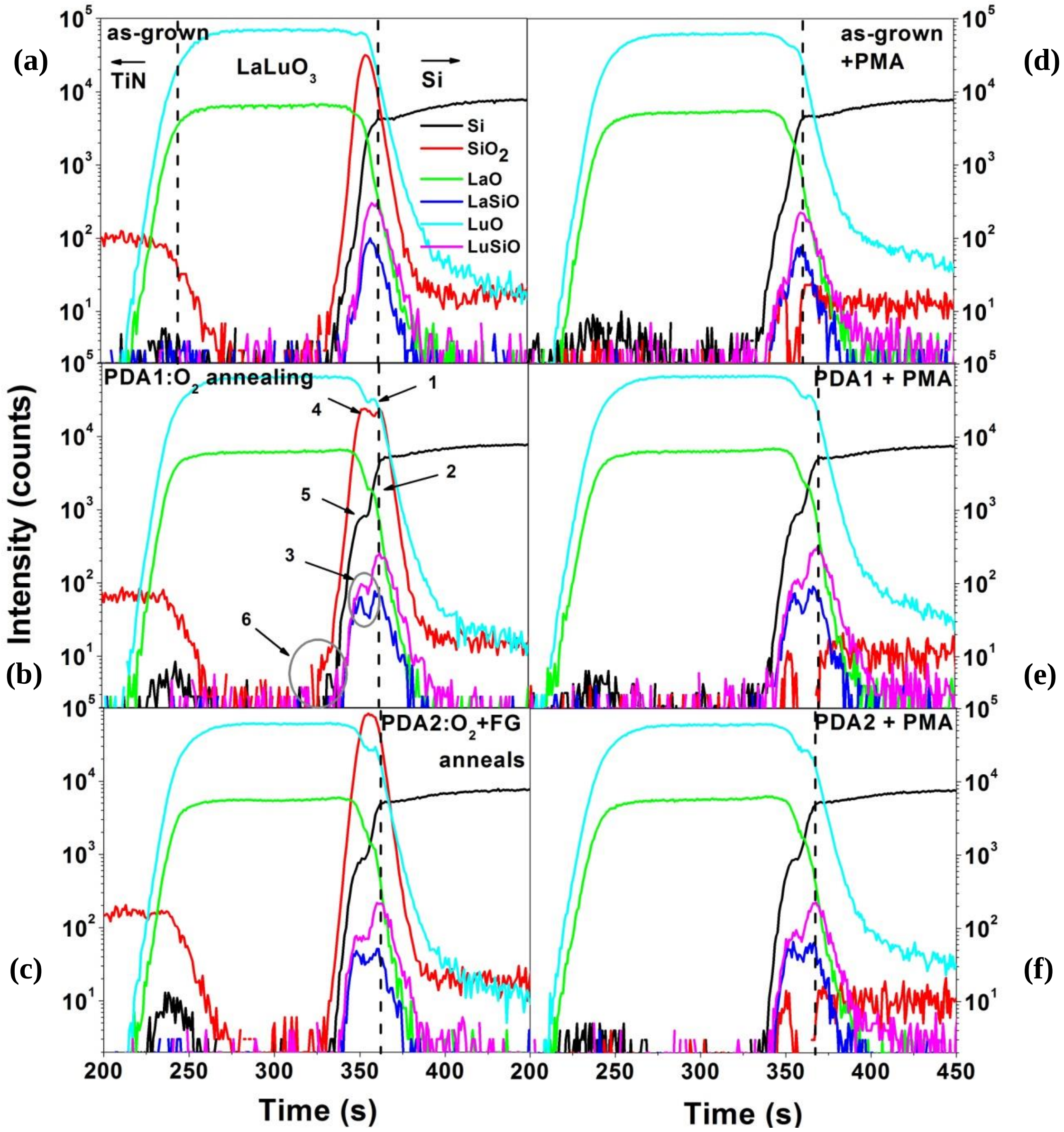


**Figure 3.5:** TOF-SIMS profiles of 20nm TiN/6 nm $LaLuO_3$ on Si, for TiN deposited on a) as grown $LaLuO_3$ film, b) $O_2$ annealed (PDA1) $LaLuO_3$ film, c) $O_2$ annealed and FG annealed (PDA2) $LaLuO_3$ film. (d), (e) and (f) are the results obtained for the same samples of (a), (b) and (c), which were exposed to a FG annealing after the TiN metal deposition (PMA). Vertical dashed lines represent the layer boundaries at high-$\kappa$/TiN interface and high-$\kappa$/Si interface.

Interestingly, an increment in the Si concentration is not observed for the sample with PDA+PMA; on the contrary, it decreased. This occurs probably because there were not

enough oxygen vacancies in these samples, since the previous oxygen annealing has compensated most of them. Here, the $LaLuO_3$ behaves like a barrier for oxygen out-diffusion. Taking a closer look to Fig 3.3 (e) and (f), one can see that, after the PMA, there is broadening of the LuO and LaO signals, not only at the Si interface side (which is the indication of the thickening of the silicate), but also at the TiN interface side. Since the TiN signals remain unchanged after heat treatment (not shown) we conclude that there is no reaction with TiN. Therefore, the broadening cannot be explained by increase of any interfacial layer, but by an increase of areal density of the high-κ itself. The areal density may have increased due to the filled vacancies. In view of mobility, it is a good sign, since the charge traps caused by oxygen vacancies would be eliminated in that way.
Concerning EOT scaling and mobility, it is suggested that the use of an ultra thin ~ 0.5 nm $SiO_2$ IL is beneficial [99]. For the PMA sample, it is clearly seen that the $SiO_2$ is not completely eliminated from the interface. However, as compared to the as-grown sample, which has ~1 nm of $SiO_2$, its thickness has reduced to below 0.5 nm. On the other hand, the formation of silicates instead of $SiO_2$ is desirable since they have higher dielectric constant (~10). Thus, the total capacitance would increase and even lower EOT would be obtained.

**(b) Analyses of 20 nm TiN/6 nm $TbScO_3$/Si gate stacks**

The depth profile of TiN/$TbScO_3$ on Si for different annealing procedures reveals Tb and Sc elements coupled to oxygen. As in the case of $LaLuO_3$, the signals are smooth along the oxide layer, as shown in Fig. 3.6. Fig. 3.6 (a) and (c), show that ScO has piled up at the Si interface, indicating an oversaturation of the silicate layer in terms of ScO. The profiles consistently reveals that, while a TbSc silicate layer is formed at the TbScO-Si interface, a Sc-rich silicate exists at the TbScO-TiN interface (Fig 3.6 (c) and (d)). Sc-rich silicate formation at the top interface was already shown by Adelmann et al. [87] for $DyScO_3$ on Si. On the other hand, on the work that has been done on $TbScO_3$ on Si, Copel et al have also shown the Sc-rich silicate formation at the top surface [100]. Moreover, for an annealing temperature of 950 °C and above, they observed a reaction between $TbScO_3$ layer and underlying $SiO_2$, causing decomposition to a Sc rich oxide on Tb rich silicate. However, for a temperature of ~500 °C the $TbScO_3$ is stable, with no reaction taking place between it and the underlying $SiO_2$.
The as grown sample exhibits $SiO_2$ with a very low intensity. As the film exposed to PDA2, more Si diffused to the interface resulting in an increase in the $SiO_2$ intensity by a factor of three, indicating an increase of the $SiO_2$ thickness. The silicate-related signals have broadened. The intensity reduction in the hump on the right shoulder of the ScO and TbO signals suggests the formation of a Si-rich instead of Sc-rich silicate. Moreover, as the samples are exposed to PDA2 and PMA, Fig. 3.6 (d), the $SiO_2$ intensity is reduced to the initial level, however, showing two peaks. From the positions of these peaks, it can be concluded that the silicate layer consist of two different compositions, and the $SiO_2$ is incorporated into those layers.

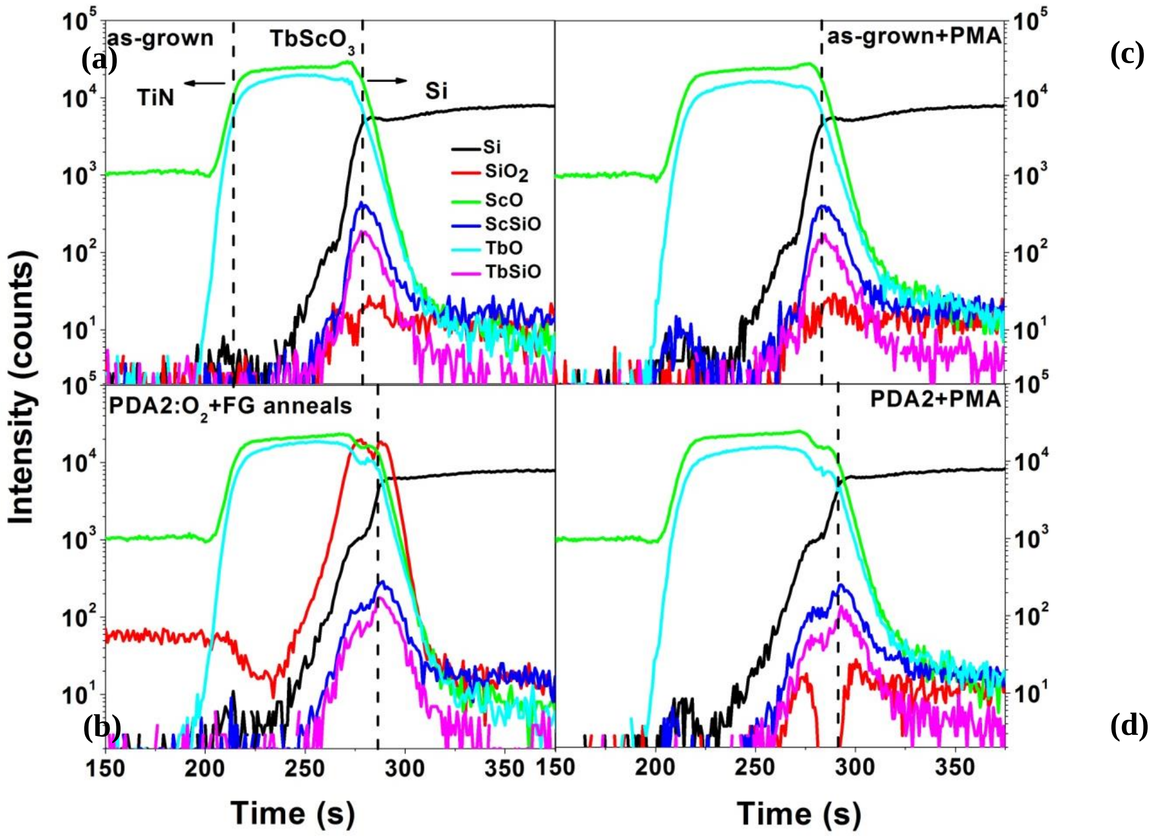


**Figure 3.6:** TOF-SIMS profiles of 20nm TiN/6 nm $TbScO_3$ on Si, for TiN deposited on a) as grown $TbScO_3$, b) $TbScO_3$ film with PDA2. (c) and (d) are the samples of graph (a) and (b), exposed to a FG annealing after the TiN metal deposition (PMA). Vertical dashed lines represent the layer boundaries at high-*κ*/TiN interface and high-*κ*/Si interface.

## 3.3 Electrical characterization

For the electrical characterization e-gun evaporated 70 nm thick Pt or sputtered 20/30 nm thick TiN (by physical vapor deposition, PVD) was used as metal gates. Pt top contacts were realized with a shadow mask, while for patterning TiN top contacts, Al was evaporated via shadow mask and used as a hard mask to protect the TiN during etching back the TiN from the sides by using an $H_2O_2$ solution. During the metal depositions the substrate were kept at room temperature in order to prevent any kind of reaction with the high-*κ* – metal interface.

To obtain an Ohmic contact on the back side of the Si substrate, a ~150 nm thick Al metal was deposited after removing the native $SiO_2$ on the back side of Si in order to provide better electrical contact between Si and Al. Finally, a PMA was carried out in a FG ambient at 400 °C to assure good backside Ohmic contact as well as improve the interface properties. Finaly, the electrical characterization of the capacitor structures was performed using an HP 4192A impedance analyzer for C-V measurements and a Keithley 4200 SCS semiconductor characterization system for leakage current measurements.

## 3.3.1 Effect of PDA1 and PDA2 on C-V and I-V

Figure 3.7 (a) compares the C–V characteristics of the films with and without PDA. The curves were recorded under forward and reverse bias sweeps at a frequency of 100 kHz and a hold time of 3 s for each measuring point. For the sample without PDA, a capacitance equivalent thickness (CET) value of 1.37 nm, which yields to an equivalent oxide thickness (EOT) of ~1nm using CET-0.4 nm = EOT [43] was achieved when taking into account quantum mechanical corrections. However, a large negative flat band voltage, $V_{FB}$, together with a large hysteresis are present in the C–V curve. According to Ref. [45] the main reason of the large negative $V_{FB}$ is the existence of oxygen vacancies.

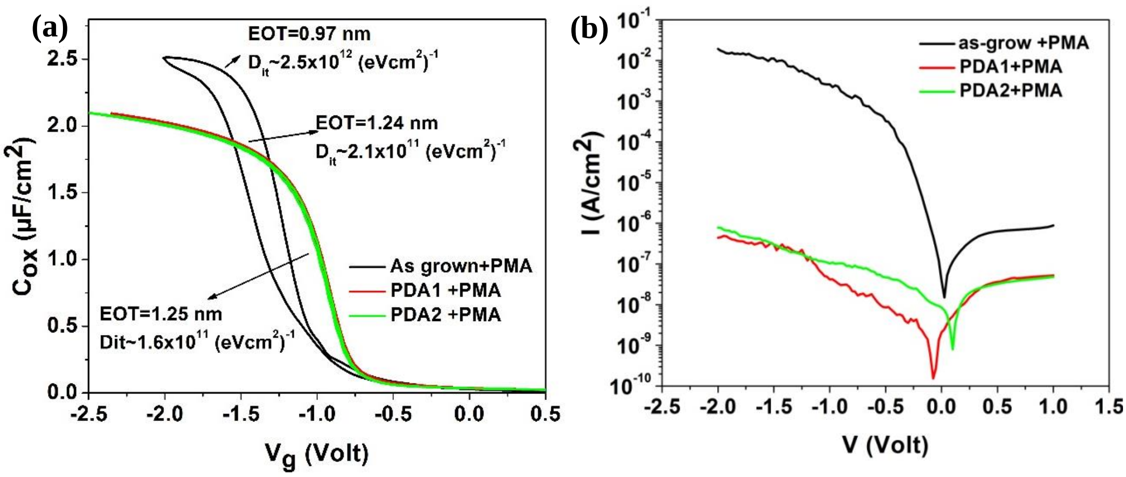


**Figure 3.7:** (a) C-V characteristics of MOS capacitors with Al/TiN/4.5 nm $LaLuO_3$ on Si. The PDA greatly reduces the hysteresis and $D_{it}$. (b) the leakage current density for these capacitors. At $V=V_{fb}-1$, the leakage current density has reduced 4 orders of magnitude after PDA.

It has been reported that the oxygen vacancies give rise to the transfer of two electrons to the metal gate, leaving a +2 charged oxygen vacancy in the oxide layer [45].

$$O_o \rightarrow V_o^{++} + 2e + \frac{1}{2} O_2. \tag{3.2}$$

Thus, positive trap charges created in the the oxide layer results in a shift of $V_{FB}$ to a more negative value. On the other hand, the hysteresis loop occurs due to the oxide trap which are mobile. This type of oxygen vacancies represent charges. The density of interface trap charge, $D_{it}$, calculated by conductance technique, is higher than $10^{12}$ (eV cm$^2$)$^{-1}$. The large

$D_{it}$ could stem from the large hysteresis. Nevertheless, for such a low EOT, it is not so easy to separate the interface traps from the high-$\kappa$ traps. On the other hand, applying PDA1 to the film helps to shift the $V_{fb}$ to a lower value, -0.46 V, completely eliminating the hysteresis, and improving $D_{it}$ to a level of ~$2x10^{11}$ $(eVcm^2)^{-1}$. This is certainly due to a reduced amount of oxygen vacancies and improved interface. However, the annealing increases EOT from 1 nm to 1.25 nm as indicated in Fig. 3.7 (a). The increment in the EOT is due to the thickness increase of the interfacial layer, as shown by TOF-SIMS to be composed of a silicate with a very thin $SiO_2$. The sample with PDA2 shows the same C-V behavior as sample with PDA1. The only difference is the slightly improved $D_{it}$, which is $1.6x10^{11}$ $(eVcm^2)^{-1}$. This is due to the passivating effect of the hydrogen on Si. Fig. 3.7 (b) shows the corresponding leakage current density after these two different treatments. It is clearly seen that at V = $V_{fb}$-1V, PDA results in 4orders of magnitude lower leakage current density, which is almost two orders of magnitude less as compared to $HfO_2$ ($10^{-2}$ $A/cm^2$) with a similar EOT [67].
Similar results were also obtained for TiN/3.5 nm $LaScO_3$ grown on silicon as shown in Fig. 3.8. The obtained EOT for an as-grown sample with PMA has increased from EOT=0.6 nm to EOT=1.05 nm for the sample with PDA2 and PMA due to the increase in the IL thicknes. The hysteresis and $D_{it}$ have improved significantly after the PDA2, inferring that, PDA2 is important in reducing the interface trap and mobile oxide trap charges at the interface to Si, and in the high-$\kappa$. The inset in Fig. 3.8 represents the corresponding leakage current density after these two different treatments. The leakage

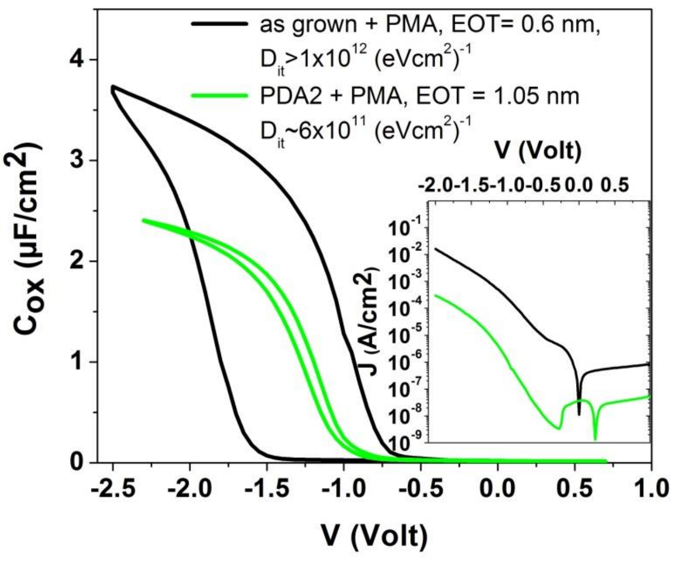


**Figure 3.8:** C–V characteristics of MOS capacitors with TiN/3.5 nm $LaScO_3$ on Si with and without PDA. The PDA greatly reduces the hysteresis. The inset shows the leakage current density for these capacitors, which is reduced by two orders of magnitude after PDA.

current at V = $V_{fb}$-1V, has been reduced by two orders of magnitude after PDA2, which is more than one order of magnitude smaller than measured for $HfO_2$ ($10^{-2}$ A/cm$^2$) films with a similar EOT [67].

## 3.3.2 Electrical properties of the rare-earth based ternary oxides

The C-V characteristics of TiN /$TbScO_3$ grown on p-type silicon with PDA2 and PMA are presented in Fig. 3.9 (a). The $TbScO_3$ film thicknesses range from 7 to 38 nm, as measured by XRR. No hysteresis was observed in the C-V curves, indicating that the high- $\kappa$ films are free of mobile charge traps. In addition, no flat band voltage shift was observed as a function of film thickness, which reveals a negligible effective oxide charge within the films. Roeckerath et al. has already investigated TiN/$TbScO_3$/Si MOS capacitors with PDA2 and PMA. However, due to different metal gate source, a flat band voltage ~ 0 V was observed, and as the film thickness increases, the flat band voltage shifted to more positive voltages. On the other hand, $TbScO_3$ was grown on a so-called HF last surface (after RCA cleaning, just before the film deposition, the samples were dipped in diluted 1% HF in order to remove the chemical oxide and provide a $SiO_2$ free Si surface). Thus, due to the direct interaction with the Si surface, a small hysteresis and a positive flat band voltage shift as a function of film thicknesses were observed. Therefore, as already mentioned in Ref. [99] having a thin $SiO_2$ is important to improve the transport properties. So, during the film deposition, the oxide will react with the $SiO_2$ instead of Si. The good quality of the interface is also confirmed by the very low $D_{it}$ ~8x$10^{10}$ (eVcm$^2$)$^{-1}$. The $D_{it}$ obtained from conductance technique is listed in Table 3.2, for all investigated

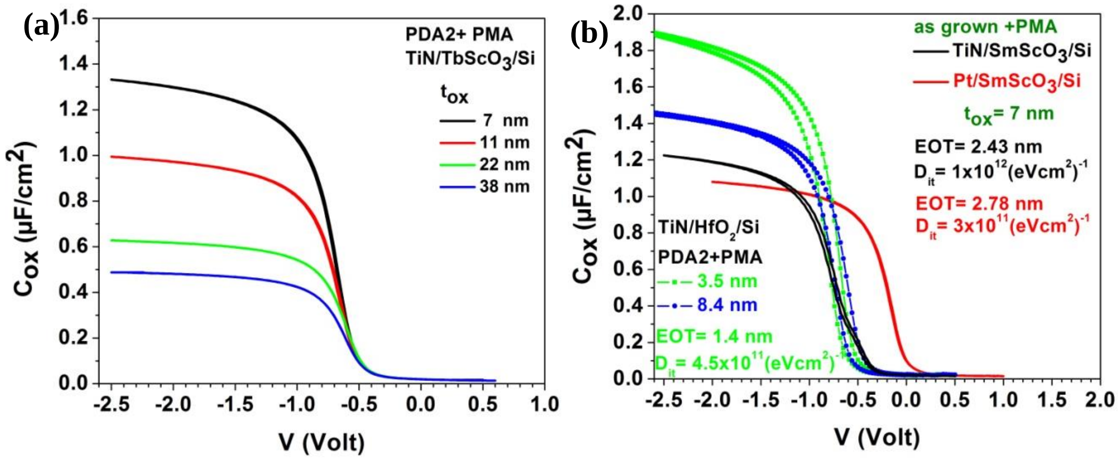


**Figure 3.9:** (a) C-V characteristics of TiN/$TbScO_3$ grown on Si with PDA2, (b) C -V characteristics for TiN/$HfO_2$ grown on Si, with PDA2 and for TiN/$SmScO_3$/Si and Pt/$SmScO_3$/Si structures with 7 nm thick as grown $SmScO_3$. All the samples were exposed to a PMA after preparation.

high-$\kappa$ dielectrics. The films with $SmScO_3$ were not exposed to PDA2 due to the fact that, during the deposition of the film, the $O_2$ partial pressure is equal or even higher than $10^{-3}$ mbar, which is three orders of magnitude higher as compared to the pressure utilized in the other techniques (e.g. MBD, e-gun). This pressure is high enough for Si to react with oxygen and create a thicker $SiO_2$ layer.
Therefore, in order to prevent even thicker IL, no PDA was applied. On the other hand, reported results have shown that, the oxygen pressure during deposition is playing an important role [101] for the C-V characteristics. Lu et al. have investigated the electrical properties of Pt/$LaAlO_3$/Si MOS structures. According to different deposition pressure in $O_2$ ambient, they observed healing in terms of hysteresis and $V_{FB}$ in the C-V curves as the pressure increased from 0.01 Pa to 0.1 Pa and finally to 1 Pa ($10^{-2}$ mbar). They conclude that high vacuum or lower oxygen partial pressure favors the formation of oxide trap charges in the films and accordingly larger hysteresis due to the oxygen vacancies appear.
The C-V characteristics of MOS structures for $SmScO_3$ on Si with Pt and TiN gate metals are presented in Fig. 3.9 (b) together with the C-V curves obtained for TiN/HfO/Si for a 3.5 nm oxide thicknesses. The results obtained from $SmScO_3$ on Si with Pt top contact showed perfect C-V behavior (an example is shown only for 7 nm film thickness). It can be seen that the deposition pressure is enough to suppress the oxygen vacancies and provide a hysteresis-free and smooth C-V curve.

**Table 3.2**: Summary of $\kappa$ values, interfacial layer thickness $d_{IL}$, number density of oxide charge ($N_{ox}$), effective metal work function ($\Phi_{m,eff}$) and density of interface trap charges ($D_{it}$).

| **Material** | $\boldsymbol{\kappa}$ | $\mathbf{d_{IL}}$ | $\mathbf{N_{ox}}$ **x10$^{11}$(cm$^{-2}$)** | $\mathbf{\Phi_{m,eff}}$ **(eV)** | $\mathbf{D_{it\_Cond.}}$ **(eVcm$^2$)$^{-1}$** | $\mathbf{D_{it\_Terman}}$ **(eVcm$^2$)$^{-1}$** |
|---|---|---|---|---|---|---|
| **TiN/ $LaLuO_3$** | 32±1 | 0.95 | -12 | 4.35 | 2x10$^{11}$ | 4x10$^{11}$ |
| **TiN/$LaScO_3$** | 29±1 | 0.65 | -13 | 4.2 | 6x10$^{11}$ | 6x10$^{11}$ |
| **TiN/ $TbScO_3$** | 26±1 | 1.3 | +1.2 | 4.5 | 8x10$^{10}$ | 1x10$^{11}$ |
| **TiN/ $SmScO_3$** | 26±1 | 1.4 | -2 | 4.65 | 9x10$^{11}$ | 1x10$^{12}$ |
| **Pt/ $SmScO_3$** | 28±1 | 2.2 | +3 | 5 | 5x10$^{11}$ | 4x10$^{11}$ |
| **TiN/$HfO_2$** | 22±1 | 0.69 | -12 | 4.54 | 4x10$^{11}$ | 6x10$^{11}$ |

On the other hand, the $V_{FB}$ stands ~0.1 V, which for Pt top contact and Si substrate indicates a negligible density of oxide charges within the oxide. However, as the top gate is replaced by TiN, the $V_{FB}$ shifts to more negative values, -0.5 V, due to the lower work function of TiN. The 40 mV counterclockwise hysteresis indicates the existence of positive mobile charges, which are supposed to be oxygen vacancies, since they are always positive charges. Not only the hysteresis, but also the interface to the Si is deteriorated as visible from the depletion zone which shows a stretch out of the C-V. The $D_{it}$~$9x10^{11}$ $(eVcm^2)^{-1}$ is almost two times higher than the one obtained for samples with Pt. This is most probably due to the scavenging effect of the TiN metal gate; while removing the oxygen from the interface, it leaves behind a non-stoichiometric $SiO_2$ IL with dangling bonds and reduced thickness. According to Guha and Narayanan [102], to induce scavenging, the oxygen vacancies in the oxide layer become mobile and reach a steady state for oxygen transport. This would simply explain the deterioration of the gate stack. Moreover, TiN metal gate provide higher $C_{ox}$, consequently lower EOT due to the reduced $SiO_2$ IL thickness.
The C-V characteristics of TiN/$HfO_2$/Si structures with PDA2+PMA for different film thicknesses are also shown in Fig. 3.9 (b) for comparison. Steep C-V curves with low $D_{it}$~$4x10^{11}$ $(eVcm^2)^{-1}$ is obtained. The thinnest film (3.5 nm) provide EOT =1.4 nm. However, 100 mV of counterclockwise hysteresis indicates the presence of the positive mobile charges within the oxide. As the thickness of the film increases from 3.5 nm to 17.5 nm, the $V_{FB}$ shifts to more positive side. This suggests the presence of negative fixed charge within the oxide. Since the oxygen vacancies are always positive charges, the negative charges are supposed to be related to Al incorporation into the oxide, most probably during the patterning of TiN with $H_2O_2$ solution. During the patterning the Al hard mask is etched with very slow etching rate. This might allow Al to diffuse into the oxide and cause negative fixed charges. In agreement with this result, Bae et al., who investigated Poly-Si/HfAlO/Si gate stacks, observed negative fixed charge due to the Al accumulation at the HfAlO-Si interface [103]. A similar behavior was also investigated in REF [67].
The lowest EOT obtained for $HfO_2$ is 0.34 nm higher than the one obtained for $LaScO_3$ for the same thickness (3.5 nm) and 0.14 nm higher than for $LaLuO_3$, with a 1 nm larger thickness (4.5 nm). This is due to different $\kappa$ values of the films, which is extracted from the slopes of the EOT vs $T_{ox}$ plots shown in Fig. 3.10 (a). The obtained $\kappa$ values are listed in Table 3.2, which are in good agreement with previous results [32, 34, 66, 67]. The intercept of the slopes with the EOT axis represents the electrical thicknesses of the lower-$\kappa$ interfacial layer, $d_{IL}$. These values are also listed in Table 3.2. The highest $d_{IL}$ was observed for PLD grown $SmScO_3$ with Pt top contact. However, by using TiN instead of Pt, $d_{IL}$ reduced significantly by an amount of 0.8 nm. $LaScO_3$ and $HfO_2$ present comparable $d_{IL}$, while ~0.4 nm higher $d_{IL}$ exists for $LaLuO_3$. If the $d_{IL}$ would be reduced for $LaLuO_3$, an even lower EOT value could be achieved.
In order to evaluate the effective work function $\Phi_{m,eff}$ of the TiN and Pt metal gates, $W_{FB}+\Phi_{Si}$ vs. EOT was plotted in Fig. 3.10 (b) for different high-$\kappa$ materials, where $W_{FB}=qV_{FB}$ and $\Phi_{Si}$ is the work function of Si. The intercept of the slopes on $W_{FB}+\Phi_{Si}$ axis gives the $\Phi_{m,eff}$. Extracted $\Phi_{m,eff}$ values are listed in Table 3.2. The 5 eV $\Phi_{m,eff}$ for Pt gate contact satisfies the work function requirement for a p-type MOSFET's. However,

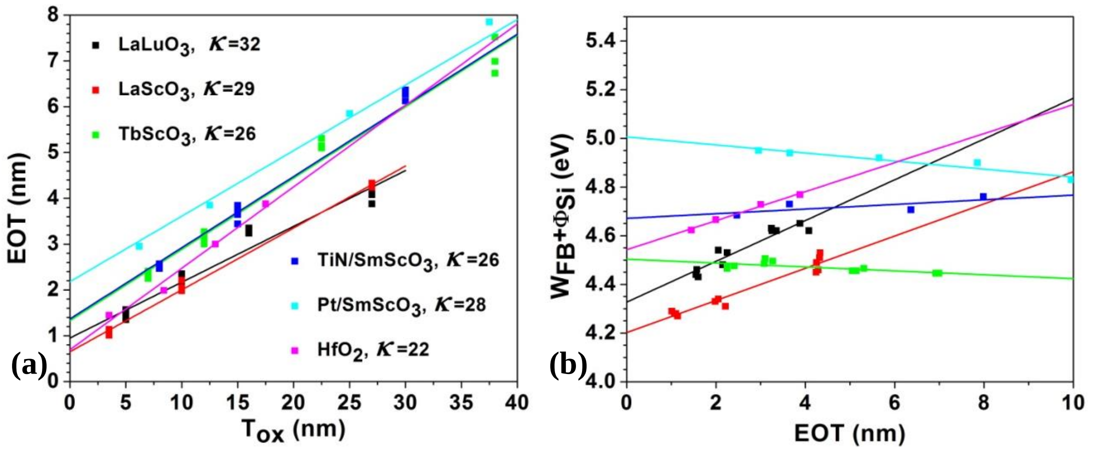


**Figure 3.10:** (a) Calculated EOT vs $t_{ox}$ of different MOS capacitors for various rare earth oxides with TiN as metal gate, except $SmScO_3$ for which Pt was used. The slope of the best-fit line provide the $\kappa$ and its intercept on the EOT axis corresponds to the electrical thickness of the lower-$\kappa$ IL. (b) $qV_{FB} + \Phi_{Si}$ vs EOT for the same capacitors. The intercept of the best-fit line on the $qV_{FB} + \Phi_{Si}$ axis gives $\Phi_{m,eff}$ and the slope, number density of oxide charge, $N_{ox}$.

for TiN metal gate, a work function ranging from 4.2 to 4.65 eV is obtained. On the other hand, by varying the temperature and $O_2$ partial pressure during post deposition annealing with Re, Ru and Pt gatecontact on $HfO_2$ Cartier et al. have observed up to 750 mV $V_{FB}$ shift [45].They attributed the $V_{FB}$ change to the variation in oxygen vacancy concentration. According to Equation 3.2, a charge transfer occurs and a dipole layer would form at the top interface (oxide-metal gate), and change $\Phi_{m,eff}$ and $V_{FB}$. Cartier et al. showed that for a Re gate contact and concluded that $V_{FB}$ can be tuned by increasing the temperature and $O_2$ partial pressure. It seems that the low $\Phi_{m,eff}$ observed for $LaLuO_3$ and $LaScO_3$ is mainly due to the oxygen vacancies, which appears to be the dominant intrinsic defect in the oxide layers.

Another important feature extracted from the $W_{FB}+\Phi_{Si}$ vs. EOT plot is the number density of oxide charges, $N_{ox}$. From the slope of the curves for different high-$\kappa$ dielectrics the polarity and the amount of charge could be obtained. A negative slope indicates the presence of positive oxide charges, while positive slope indicates negative oxide charges. The results are listed in Table 3.2. The observed high negative charge for $LaLuO_3$, $LaScO_3$ and $HfO_2$ is based on the Al incorporation from the etching in $H_2O_2$ solution. This could be eliminated by using dry etching instead of wet etching, which is the case for the MOSFETs processed in this study. For $TbScO_3$ a dry etching process in SF6 plasma was applied. Therefore, negligible oxide charge ~$10^{11}$ $cm^{-2}$ were observed. Interestingly, the best $D_{it}$ obtained from conductance method was also observed for these samples, $D_{it}$~$8x10^{10}$ $(eVcm^2)^{-1}$, indicating the good quality of the oxide. It is assumed that the Al incorporation to the other high-$\kappa$ dielectrics also affect the interface, which result in slightly higher $D_{it}$. Apart from the conductance method, high frequency C-V method was also employed to obtain $D_{it}$, which is known as Terman's method. In Fig. 3.11 the density of interface trap charges, $D_{it}$ as function of energy in the band gap of crystalline silicon is presented. As expected, the curves are U shaped due to the interaction with the silicon conduction band by capturing and emitting electrons. The curves reach their minima, which is the exact value of the $D_{it}$ at the oxide-Si interface, around flat band voltages. The extracted $D_{it\_Terman}$ levels are added to the Table 3.2. Those obtained results are almost the same as the one obtained from the conductance method. The slight change could occur due to the extraction of the interface state capacitance, $C_{it}$ from the measured capacitance, which consist of oxide capacitance, depletion layer capacitance and the interface state capacitance. On the other hand, from the position of the minimum for each curve, it can be concluded that, while for Pt/$SmScO_3$ MOS capacitors, the interface trap charges are located more in the valence band, for the rest, they are close to the mid gap.

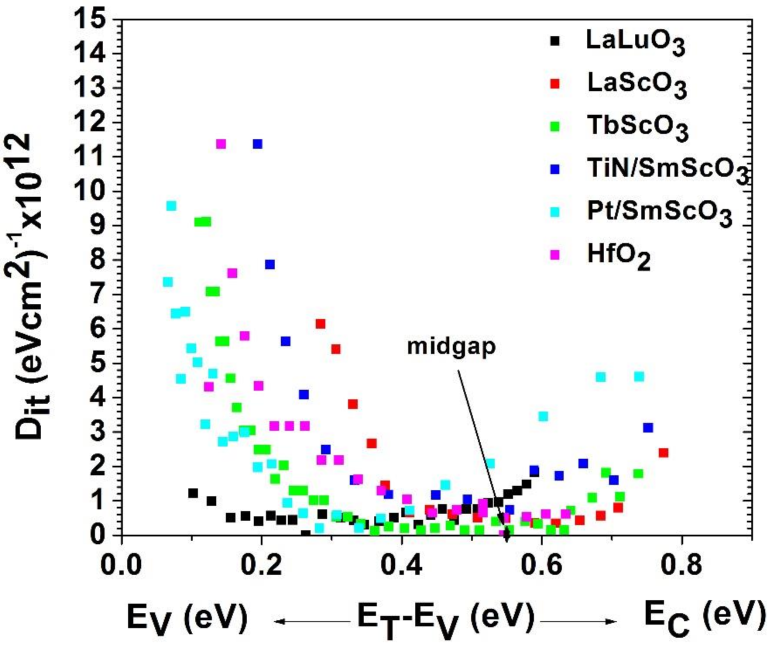


**Figure 3.11:** Density of interface trap obtained from Terman's method (high frequency C-V method) for different high-*κ* dielectrics

Low leakage current density levels are observed for the investigated high-*κ* dielectrics as ilustrated in Fig. 3.12. For the sake of comparison, leakage currents for gate stacks containing $SiO_2$, $HfO_2$ [62], $HfO_2/Al_2O_3$ [67] and $GdScO_3$ [53]as gate dielectrics are also plotted. For EOT≥ 1 nm, all the dielectrics showed comparable and low leakage current density. As compared to $HfO_2$ for an EOT≤ 1 nm, $LaLuO_3$ samples showed 1 order of magnetude lower leakage current density ($1.1x10^{-2}$ A/cm$^2$) while three orders of magnitude lower leakage could be achieved with $LaScO_3$. Therefore, $LaLuO_3$ and $LaScO_3$ seem to be promising in terms of further device scaling, since they provide very low leakage current densities.

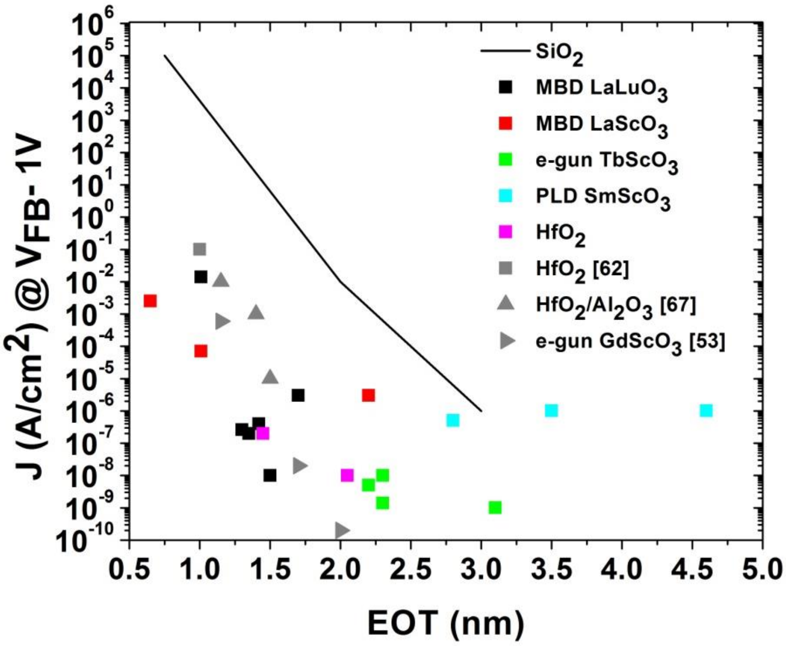


**Figure 3.12:** Leakage current density J vs EOT for different high-κ dielectrics investigated in this work together with $HfO_2$ and $GdScO_3$ references. The plotted values are for $V= V_{FB}+1$ V.

# 3.4 Summary

In the first part of this chapter the structural characteristics of the rare-earth based ternary oxides are described. It is found that the films are stoichiometric and amorphous up to 800 ºC-1000 ºC. The investigation of the effect of oxygen annealing and FG annealing on the structural characteristics of the MOS capacitor has revealed that silicate formation is an inevitable process during film growth. The silicate formation is triggered by oxygen annealing, while it remains unchanged after FG annealing. Another observation is that, TiN metal helps to reduce the $SiO_2$ interfacial layer thickness after FG anneal by scavenging oxygen from the interface, which is useful in terms of EOT scaling.

The second part is devoted to the electrical characteristics of MOS capacitors fabricated with $LaLuO_3$, $LaScO_3$, $TbScO_3$ and $SmScO_3$. C-V characteristics close to ideal could be obtained by applying PDA2+PMA to the as-grown films. The formed silicate-like interface seems to improve the electrical characteristics of the MOS capacitors. The extracted $\kappa$ values range from 26 to 32, distinctly higher than for $HfO_2$. Negligible hysteresis, low interface trap and oxide charges, and for a comparable EOT, at least one order of magnitude lower leakage current as compared to $HfO_2$ is achieved. However, oxygen vacancies are found to be intrinsic dominant defects causing a reduction of the work function of TiN as metal gate facilitated by electron transport from the high-$\kappa$ to the metal.

# Chapter 4

# Integration of rare-earth based oxides into MOSFETs

## 4.1 Introduction

In chapter 3, rare earth based ternary oxides $LaLuO_3$, $LaScO_3$, $TbScO_3$ and $SmScO_3$ were investigated. It was shown that an annealing procedure can improve the oxide properties and also the interface quality of MOS structures with a lower leakage current, less interface trap states and compensated oxide charges. In this chapter, by using the same conditions, the MOSFET characteristics with the same rare-earth based oxide materials will be investigated. One of the main goals is to give a comprehensive understanding of the physical phenomenon in these MOSFETs, especially regarding the mobility degradation which occurs typically for a high-$\kappa$ layer compared to $SiO_2$. Up to now, for these materials, no result has been published regarding the mobility degradation (the mobility obtained for $TbScO_3$ in [34] is the low field mobility, $\mu_o$ and refers to one single point, doesn't give any information about the voltage dependence of the mobility). Therefore, it is important to study the mobility degradation in order to see their possible application for advanced CMOS applications, especially compared to devices with industrial widely used high-$\kappa$ material, $HfO_2$. For the investigation of the MOSFETs with rare earth based oxides, a replacement gate process was developed and both n- and p- MOSFETs were fabricated on conventional SOI and biaxially strained sSOI substrates. Mobility enhancement and on current gain in MOSFETs with $LaLuO_3$, $LaScO_3$ and $TbScO_3$ are investigated and compared to $HfO_2$ based MOSFETs. As compared to SOI devices, a 90 percent improvement is achieved in mobility by using biaxially tensile strained sSOI. We also found that p-MOSFET devices with $LaLuO_3$ and $LaScO_3$ showed a very good performance with a subthreshold slope down to 65 mV/dec and a mobility comparable with $SiO_2$.

## 4.2 Replacement gate process and device fabrication

In Ref [34] and [39], we have used a non-self-aligned transistor process to prepare transistors and to measure the mobility of devices with $GdScO_3$ and $TbScO_3$ as gate dielectric. Since the gate was not self-aligned to the source-drain junction, the mask was designed in such a way that, in all cases the gate overlaps the S/D junctions. However, this caused a drawback with this structure, the gate metal area was too large and therefore the overlap was also large, which caused a large series resistance $R_{sd}$ due to the increase in $R_{sp}$ and $R_{ac}$ (see Fig. 4.1) and a large overlap capacitance. Due to the non-self alignment, the metal gate was not symmetric on S/D part and the correction of the relatively large overlap capacitance for split C-V mobility extraction was not accurate.
On the other hand, the replacement gate process is a self aligned metal gate process which was first demonstrated by Chatterjee et al for a gate last process [104], in order to prevent the metal gate from high temperature exposure during S/D dopant activation. Since it is a self aligned process all possible misalignment problems could be eliminated and the $R_{sp}$ component of the $R_{sd}$ in Fig. 4.1 could be neglected by providing S/D edge to gate edge implantation and $L_{sp}$ approaching zero. In this thesis a gate last process was used, which is a low temperature process for the high-k materials since the gate oxide and the metal gate are not exposed to high temperature S/D activation process. Therefore the main aim of using the replacement gate process is not to protect the metal gate from high temperature but eliminating any possible misalignment and reducing $R_{sd}$, improving the device characteristics for obtaining reliable mobility data.

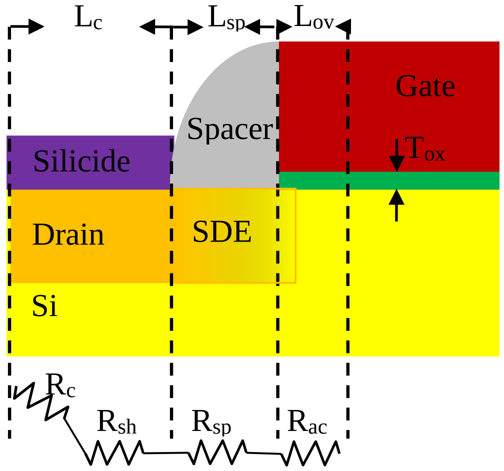


**Figure 4.1:** The S/D series resistance component: contact resistance $R_c$, sheet resistance $R_{sh}$, spreading resistance $R_{sp}$ and accumulation resistance $R_{ac}$. The $L_c$, $L_{sp}$ and $L_{ov}$ are the silicon-silicate contact length, the spacer length (or non-implanted area due to misalignment) and the gate-drain (source) overlap length. The gate is separated from the S/D contact region by the S/D extensions (SDE).

The device fabrication flow with replacement gate process is shown in Fig. 4.2. Lightly p-doped SOI (100) and sSOI (100) wafers with top Si thickness of 88 nm and 70 nm, respectively, were chosen as starting material and cut into 2x2 $cm^2$ sized pieces. The thickness of the buried oxides (BOX) for both, SOI and sSOI is 145 nm. sSOI with a biaxial tensile strain of $\varepsilon_{biax}$ =0.8%, corresponding to a stress of 1.35 GPa, was used.

*1. Thinning down:*

The SOI and sSOI wafers with their thicknesses mentioned above are too thick for fully-depleted (FD) MOSFET application. Therefore, their thicknesses were thinned down by a 2-step oxidation and HF dipping. The SOI thickness was thinned down to 50 nm after the first oxidation and HF dip.

*2. Mesa Definition:*

Before the last oxidation for the final thinning down was performed, the transistors were electrically isolated by patterning the top Si into L/W=84/20 µm size, which is known as mesa isolation. The patterning was carried out using an optical lithography with AZ5214 photoresist (PR) and RIE etching in Ar/$SF_6$ plasma.

3. *Sacrificial gate oxide formation ( Fig. 4.2 (a))*:

After the mesa isolation an RCA cleaning was carried out to keep the surface clean before the sacrificial gate oxide formation which serves as a passivation between the gate-S/D regions. A 22/30 nm sacrificial oxide was formed in a rapid thermal oxidation furnace at 900/950 °C in 55/60 min in oxygen ambient. The final SOI and sSOI thicknesses together with sacrificial gate oxide thicknesses are summarized in table 1.

*4. Sacrificial gate patterning and implantation (Fig. 4.2 (b):*

An AZ5206 PR was used as sacrificial gate. The samples were coated with this PR. After a hard bake of the PR a 100 nm $SiO_2$, which will serve as a hard mask during patterning, was deposited on top by e-gun evaporation. The gate was defined by optical lithography (UV6.06 PR) and RIE etching using $CHF_3$ and $O_2$ plasma. $CHF_3$ plasma etches $SiO_2$ while the $O_2$ plasma is used to etch the photoresist selectively.
The gate definition was followed by arsenic ($As^+$) implantation for n-MOSFETs and boron ($B^+$) implantation for p-MOSFETs with an ion dose of $3x10^{15}$ $cm^{-2}$. Among the n-MOSFETs for devices with 22 nm sacrificial gate oxide an ion energy of 25 keV was used while for the one with 30 nm $SiO_2$ an energy of 35 keV was used. For the p-MOSFETs a 6 keV ion energy was applied. The implantation energy was chosen so that after the annealing for activation of the dopants, the dopants spread to the entire Si layer and result in a carrier depleted channel which is known as fully depleted (FD) condition.

*5. Ti hard mask deposition etching back of the sacrificial gate oxide-removal of Ti (Fig. 4.2 (c), (d), (e,), (f)):*

The S/D implantation was followed by a Ti metal deposition (see Fig. 4.2(c)). This would help even after the removal of the sacrificial gate by lift-off to keep the S/D already defined (see Fig. 4.2(d)). In addition this serves as a hard mask during the etching of the open area with the use of a $CHF_3$ plasma in RIE. By doing so, the channel with a certain length L and width W will be free of the sacrificial gate oxide (see Fig. 4.2(e)).
Finally the Ti layers were removed in a piranha solution ($H_2SO_4/H_2O_2$=4/1). Thus, without the need of a second lithography step, a self aligned gate with a $SiO_2$ passivation layer on S/D could be defined (see figure 4.2(f)).

*6. Dopant activation and high-κ deposition (Fig. 4.2(g)):*

Directly after the piranha cleaning for the removal of the Ti, annealing at 900 °C for 1 min (n-MOSFETs) and 1000 °C for 5 sec (p-MOSFET) were carried out in order to activate the dopants and re-crystallize the implanted S/D. This step was followed by an RCA cleaning to keep the Si surface clean and prevent any kind of contamination before the high-*κ* deposition. The high-*κ* materials used in this work, together with their deposition conditions and the film thicknesses are listed in Table 4.1. After the film deposition, all the samples, except for the one with $SmScO_3$ undergo an $O_2$ anneal at 400 °C for 10 min which was followed by another 10 min anneal in FG atmosphere at 400 °C in order to compensate any possible $O_2$ vacancies within the film and at the interface to silicon and to reduce the interface trap density.

**Table 4.1:** Process parameters for different fabricated samples. $t_{SOI/sSOI}$: Si/strained Si thickness, $t_{SiO2}$: sacrificial gate oxide thickness $t_{ox}$: oxide thickness.

| Material | $t_{SOI/sSOI}$ (nm) (n-MOSFET) | $t_{SOI}$ (nm) (p-MOSFET) | $t_{SiO2}$(nm) (n/p-MOSFETs) | Film dep. | Substrate temp. (°C) | $t_{ox}$(nm) (n/p-MOSFETs |
|---|---|---|---|---|---|---|
| $HfO_2$ | 30/35 | ---- | 30/-- | ALD | 300 | 8/-- |
| $LaLuO_3$ | 30/35 | 30 | 30/30 | MBD | 450 | 7/8 |
| $LaScO_3$ | 36/40 | 30 | 18/30 | MBD | 350 | 7/10 |
| $TbScO_3$ | 36/40 | ---- | 18/-- | e-Gun | 600 | 7/-- |
| $SmScO_3$ | 32/-- | ---- | 30/-- | PLD | 450 | 8/-- |

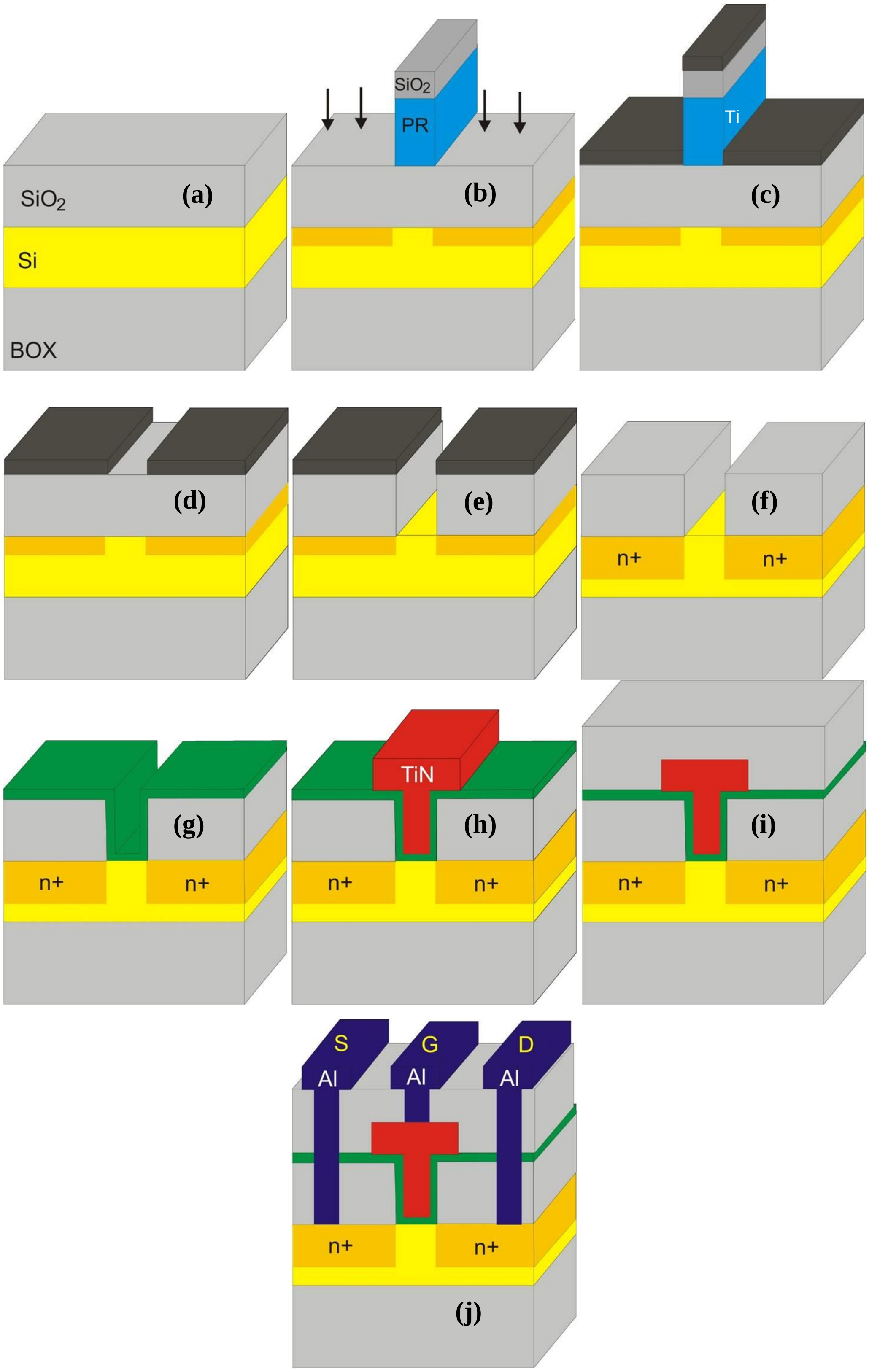


**Figure 4.2:** Replacement gate process flow for fabrication of MOSFETs

7. *Metal gate formation and $SiO_2$ passivation (Fig.4.2(h),(i)):*

A 25 nm thick TiN metal gate was deposited using sputtering. The metal gate was then patterned using optical lithography and RIE (Fig. 4.2(h). $SF_6$ plasma was used to etch TiN, which is highly selective to high-$\kappa$, and the high-$\kappa$ layer was used as an etch stop layer. After that, the samples were capped by 100 nm $SiO_2$ deposited by plasma enhanced chemical vapor deposition in order to passivate the devices (Fig. 4.2(i)).

8. *Contact metallization and final FG annealing (Fig. 4.2(j)):*

The contact windows were realized by optical lithography. With a $CHF_3$ plasma the $SiO_2$ layers were etched down to the Si and TiN surface to form the contact windows. Directly before the 150 nm Al metal contact, first the samples were kept in a buffered HCl (5%) solution for 90 sec to remove the high-$\kappa$ layer from S/D windows. Second, a 30 sec HFdip was done in order to remove any possible remaining $SiO_2$ from the surface and provide a better Ohmic contact. After Al deposition, the contacts were patterned by a lift-off process.

Finally the samples were annealed in a FG ambient for 10 min at 400 °C to provide a reduced contact resistivity and to improve the device characteristics.
Fig. 4.3 shows the top view of the Si mesa after the removal of Ti metal. Along the Si mesa, the bright field shows the source and drain with a $SiO_2$ layer on top, and the dark part the Si channel. The observed side wall roughness is due to the optical lithography and is around 60 nm.

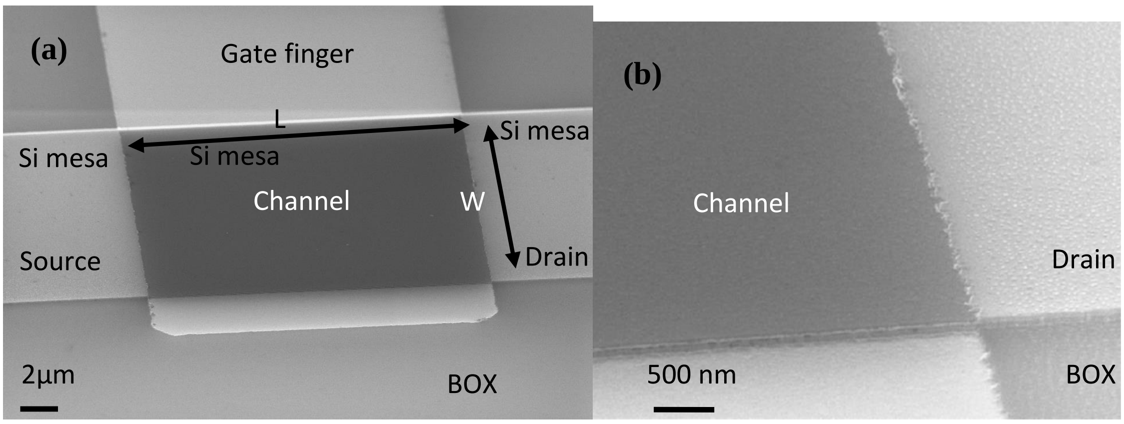


**Figure 4.3:** SEM image of the MOSFET structure with (a) exposed Si channel area and a $SiO_2$ layer on S/D after the removal of Ti, (b) a closer look to the surface and the side wall. The roughness at the side walls is due to optical lithography.

Fig. 4.4 shows a cross sectional TEM image of FD MOSFET with $HfO_2$ and $LaLuO_3$ on SOI. ALD technique is well known for its conformal deposition advantage which is provided for $HfO_2$, the side wall is nicely covered realizing perfect isolation between the gate and S/D and channel areas. However, MBD grown $LaLuO_3$ doesn't show the same characteristics, which finally results in a higher leakage in the on state of the devices due to the fringing effect. MBD grown $LaScO_3$, e-gun evaporated $TbScO_3$ and PLD grown $SmScO_3$ showed the same non-conformal coverage at the side walls.

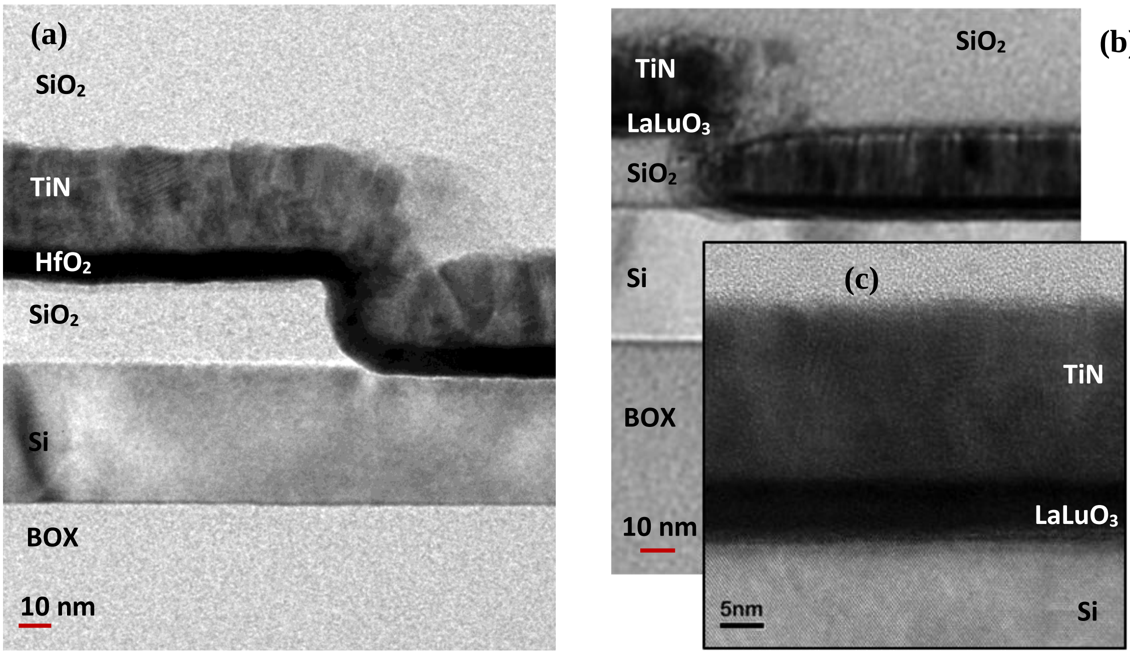


**Figure 4.4:** Cross sectional TEM image of FD MOSFETs with (a) ALD grown 8 nm $HfO_2$, (b) MBD grown 7 nm $LaLuO_3$. A nice conformal deposition is achieved by ALD while MBD technique has a poor conformality. (c) A 7 nm $LaLuO_3$ film after $O_2$ and FG anneals showed ~1 nm of interfacial layer.

# 4.3. Results and discussions

## 4.3.1 n-MOSFETs on SOI

Fig. 4.5(a) shows typical output characteristics of an n- type fully depleted (FD) MOSFET with $LaLuO_3$ gate oxide and TiN metal gate on SOI substrate at $V_g$ ranging from 0 to 2.5 V. The drain current $I_d$ shows a steep linear behavior at low $V_{ds}$ and a good saturation at high $V_{ds}$. According to the explanation of the $I_{d,sat}$, the mobility μ, the oxide capacitance $C_{ox}$ and the series resistance $R_{sd}$ strongly effect the saturation current. The graph in Fig. 4.5 (b) represents the output characteristics of 2 μm gate length devices with various high dielectric constant materials on SOI substrate together with the reference $HfO_2$ transistor at $V_g$=2 V. Among these high-κ materials, $LaLuO_3$, $LaScO_3$ and $TbScO_3$ seem to show the best results. However, although the device with $LaScO_3$ provides the

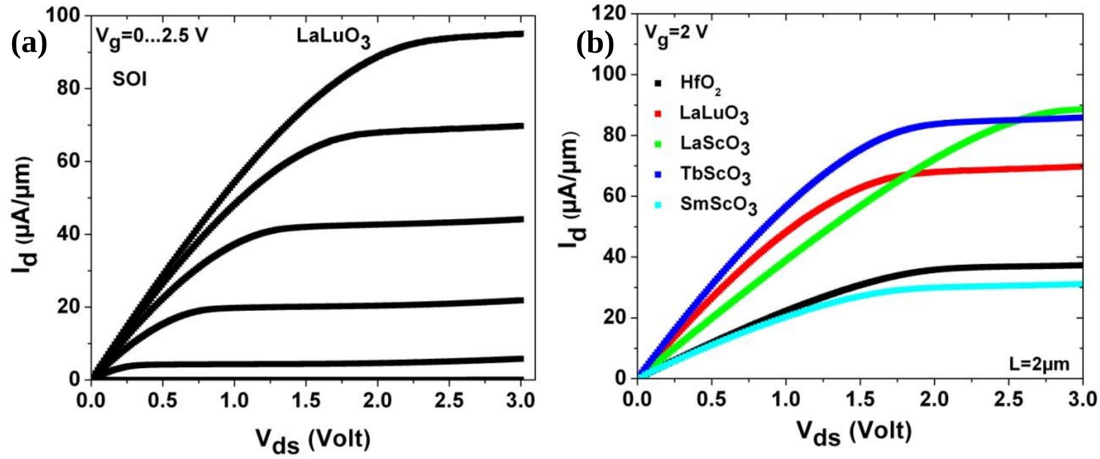


**Figure 4.5:** (a) Output characteristics of an n-type FD MOSFET with $LaLuO_3$, (b) comparison of $I_d$-$V_{ds}$ curves for rare-earth based oxide MOSFETs and the reference $HfO_2$ MOSFET on SOI substrates ($L_g$ =2 µm) at $V_g$-$V_t$ = 2 V.

highest saturation current it suffers from high series $R_{sd}$ which results in an extended linear region. This behavior is also visable for $HfO_2$ and $SmScO_3$ devices. Although $LaLuO_3$ has the highest "*κ*" value, the device did not show the highest on current. This could be explained with the different silicate like interfacial layers (IL) observed by XPS and TOF-SIMS measurements for different high-*κ*. Apart from the oxide charge within the oxide layer, the silicate like IL will cause scattering at the channel resulting in a lowered drain current. That's why a $SiO_2$ IL ~0.5 nm just above Si is needed to prevent the scattering. Unfortunately, for those investigated MOS capacitors or MOSFET devices, although the TOF-SIMS investigation points to a very thin $SiO_2$, much thinner than the silicate layer, the exact $SiO_2$ IL thicknesses is not known. Therefore, an investigation of the effect of the thickness of the IL on the mobility needed.

Fig.4.6 shows the plot of total resistance $R_T$ versus gate length L for different gate voltage $V_g$. To extract the $R_{sd}$ the $R_T$ is extrapolated to zero gate length. The intersection of the fitted line on the y-axis provides the $R_{sd}$. In case of $TbScO_3$ the obtained $R_{sd}$ is 2 kΩµm and the results obtained for all the high-*κ* devices are summarized in Table 4.2. The highest $R_{sd}$ was extracted for $SmScO_3$, which is grown by PLD. Unfortunately, PLD is not an industrial method for high-*κ* deposition due to the limited layer uniformity in large scale. Moreover, the highly energetic pulsed laser beam might cause a degradation of the channel area which finally may affect the device performance. Nevertheless, the obtained $R_{sd}$'s are one and even two orders of magnitude higher than the required $R_{sd}$ stated by the International Technology Roadmap of Semiconductors (ITRS) [5] (200 Ωµm). This huge $R_{sd}$ is not modulated by the gate voltage and introduces a voltage drop on the S/D contacts, which finally reduces the drain conductance and the transconductance. At a voltage $V_g$-$V_T$=2.5 V, as listed in Table 4.2, the $I_{d,sat}$ for $LaScO_3$ is lower than the one obtained from $TbScO_3$ based MOSFET due to the extracted higher $R_{sd}$. The replacement gate process shown in this thesis is not

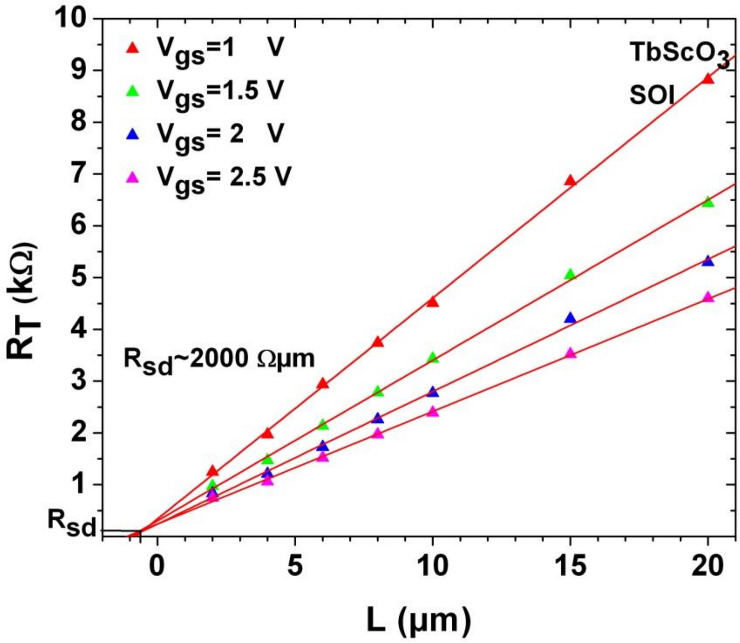


**Figure 4.6:** Total resistance $R_T$ as a function of gate length L for $TbScO_3$ gate oxide on SOI FD MOSFET, for a gate voltage ranging from 1 to 2.5 V. The gate width is W=20 μm.

**Table 4.2:** Parameters extracted from output characteristics together with the $\kappa$ values.

| Material | κ | $I_{on}$ (μA/μm) (@$V_g$-$V_t$=2.5V) | $R_{sd}$ (kΩμm) | $N_A$ ($cm^{-3}$) |
|---|---|---|---|---|
| $HfO_2$ | ~22 | 45 | 16 | 1.23e18 |
| $LaLuO_3$ | ~32 | 95 | 6.0 | 1.34e19 |
| $LaScO_3$ | ~29 | 106 | 18 | 2.67e18 |
| $TbScO_3$ | ~26 | 120 | 2.0 | 4.46e19 |
| $SmScO_3$ | ~26 | 37 | 28 | 1.17e18 |

compatible with industrial application, but it provides a simple method for the characterization of the gate and drain currents as well as the mobility behavior of the new high-$\kappa$ dielectrics. Since no silicided contacts were used and the distance from the channel end to the metal contact is 6 μm the huge portion of the $R_{sd}$ is mainly caused from the spreading resistance. This could be greatly suppressed by using silicided contacts and reduced gate-source and gate-drain metal contact distance. The $R_{sd}$ between the contact trenches is related to the resistivity as follow;

$$R_{sd} = \frac{\rho_s l}{d} \quad , \tag{4.1}$$

where $\rho_s$ is the sheet resistivity, $l$ the distance between contact trenches and d the thickness of the implanted area. From the obtained $R_{sd}$ one can calculate the $\rho_s$. Once the resistivity calculated, it is easy to get the doping concentration according to;

$$\rho_S = \frac{1}{q\mu_n N_A} \quad , \tag{4.2}$$

where $\mu_n$ is the mobility at the S/D (the mobility of the silicon) and $N_A$ the doping concentration. From the extracted $\rho_s$, the corresponding doping concentrations were estimated from the "resistivity vs impurity concentration graph" in REF [40], which used equation 4.2 for the calculation. The extracted results are summarized in Table 2. The obtained $N_A$ values range from $1.17x10^{18}$ to $4.4x10^{19}$ $cm^{-3}$ One of the main reasons for this variation could be the thickness variation of the $SiO_2$ passivation layer. A second reason could be an incomplete activation of the carriers.
Typical transfer and gate leakage characteristics of a FD SOI MOSFET with $LaLuO_3$ gate oxide for a drain voltage ranging from 0.1 to 1.1 V are shown in Fig. 4.7 (a). The devices show an almost ideal subthreshold slope of 72 mV/dec. At low $V_{ds}$ a high $I_{on}/I_{off}$ ratio up to $10^9$ and an off state current $I_{off}$ down to $10^{-8}$ µA/µm were achieved. However as $V_{ds}$ increases $I_{off}$ also increases. As $V_{ds}$ exceeds 0.9 V, the $I_{off}$ exceeds the gate leakage by an order of magnitude. This behavior in the off state can be explained by the gate induced drain leakage (GIDL) which limits achieving low $I_{off}$ with an increased $V_{ds}$ due to the high electric field which occurred at the extended gate to S/D overlap region. Similar GIDL behavior was also observed for the other high-$\kappa$ devices, however due to the conformal deposition provided by atomic layer deposition, $HfO_2$ showed lower degradation in the off state for increased $V_{ds}$. On the other hand, due to the non-conformal deposition the leakage currents at on state for all the devices with rare-earth based scandates are three orders of magnitude higher than the devices with $HfO_2$. Fig. 4.7 (c) and (d) represent the statistical distribution of the threshold voltage $V_T$ for FD MOSFETs with $LaLuO_3$ and $LaScO_3$ gate oxides. $\langle V_T \rangle$ represents the average threshold voltage and $\sigma$ is the standard deviation. In Table 4.3 the $I_{on}/I_{off}$ ratio obtained for $V_{ds}$=0.3 V and the extracted average $V_T$ for devices with different high-$\kappa$ are summarized. A $V_T$ of ±0.2 V is always desired for n/p MOSFETs in order to achieve a reasonable gate overdrive for the desired device performance. Due to the low work function obtained for the TiN metal gate, which is caused by the presence of oxygen vacancies or the non optimized deposition condition of the TiN, the obtained $V_T$ are in an acceptable range. Fig. 4.7 (b) shows the subthreshold characteristics of RE-based oxides. For a direct comparison of the subthreshold slope a $V_T$ correction was applied. Among these materials $LaLuO_3$ and $LaScO_3$ show the steepest subthreshold characteristics. The high subthreshold slope observed for $HfO_2$ and $SmScO_3$ implies that whether the films are too thick or the trap density located at the interface is relatively higher compared to the other oxides.

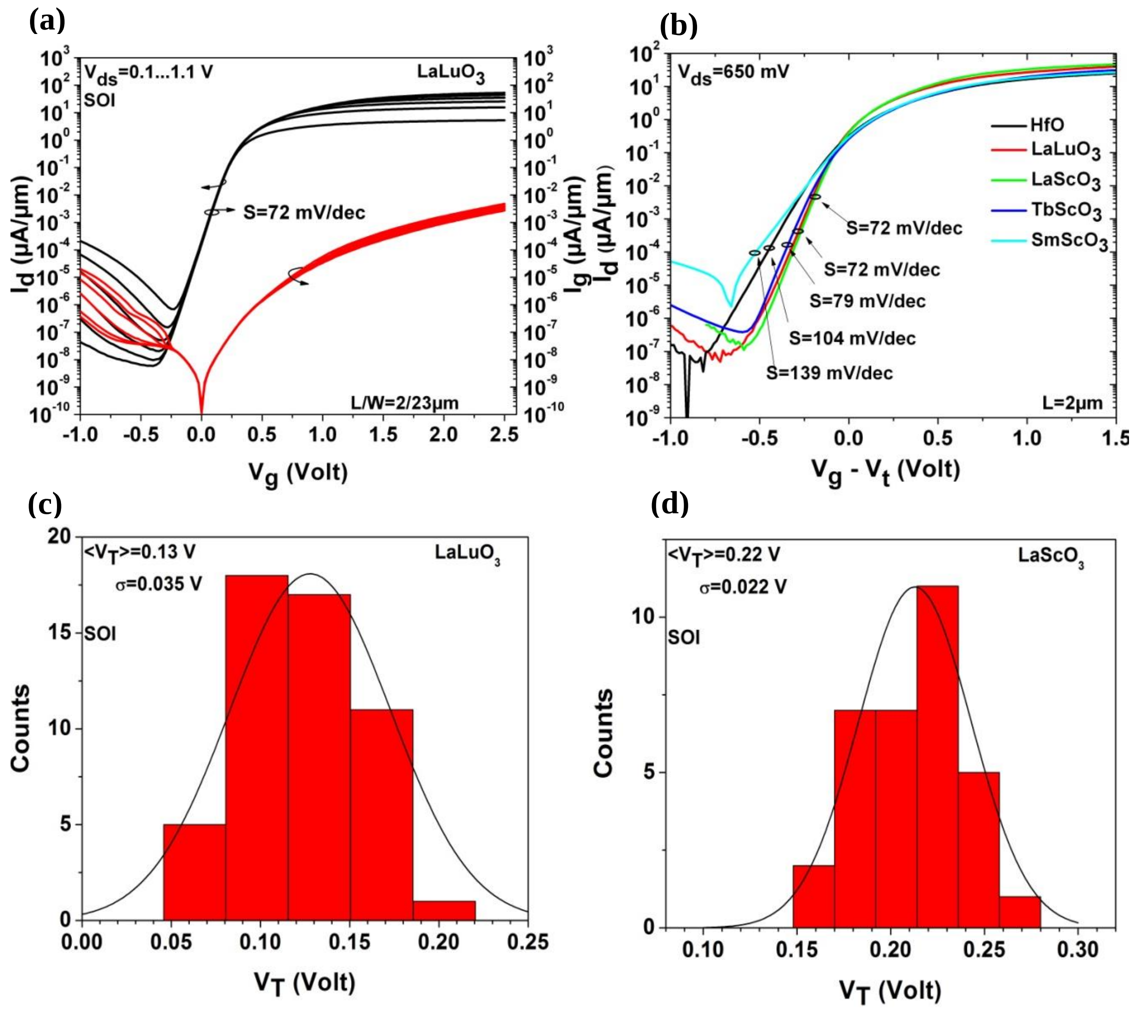


**Figure 4.7:** Transfer characteristics of n-type FD MOSFET with (a) $LaLuO_3$ at $V_{ds}$ from 0.1 to 1.1 V. The gate leakage currents $I_g$ are also presented in the figure. (b) Comparison of subthreshold characteristics of devices with various high-k dielectrics. Steep sub-threshold slopes were obtained for $LaLuO_3$ and $LaScO_3$ devices. (c) and (d) statistical distribution of threshold voltage for MOSFETs with $LaLuO_3$ and $LaScO_3$ gate oxides.

**Table 4.3:** Parameters extracted from transfer characteristics and split C-V measurements.

| Material | $I_{on}/I_{off}$ (@$V_{ds}$=0.3V) | $\langle V_T \rangle$ (V) | S (mV/dec) | EOT (nm) | $D_{it}$ x$10^{11}$ $(eVcm^2)^{-1}$ |
|---|---|---|---|---|---|
| $HfO_2$ | $10^8$ | 0.24 | 104 | 3.0 | ~20 |
| $LaLuO_3$ | $10^9$ | 0.13 | 72 | 1.7 | 2-5 |
| $LaScO_3$ | $10^9$ | 0.22 | 72 | 2.3 | 2-4 |
| $TbScO_3$ | $10^8$ | 0.1 | 79 | 2.7 | 2-6 |
| $SmScO_3$ | $10^6$ | 0.05 | 139 | 3.0 | ~50 |

The inverse subthreshold slopes show a uniform distribution over the gate length as shown in Fig. 4.8 (a) for MOSFETs with $LaLuO_3$. The same behavior was also observed for the rare-earth scandates and $HfO_2$. This is a clear indication of the homogeneity of the interface to silicon and the uniformly grown oxide layer. In Fig. 4.8 (b) the transconductance, $G_m$ of the devices is plotted for a $V_{ds}$=0.65 V by taking the derivative of the drain current over gate voltage. Before taking the derivative of the drain current $R_{sd}$ was corrected in order to remove the effect of the $R_{sd}$ to allow a direct comparison. As compared to $HfO_2$ devices, $LaScO_3$ devices show an improvement of a factor of two, while for $LaLuO_3$, $TbScO_3$ and $SmScO_3$ factors of 1.62, 1.58 and 1.14 of improvement in transconductance, respectively, were obtained. Because of their higher dielectric constant, the rare earth based oxides provide much higher drain currents as compared to $HfO_2$, and even for further scaling much better performance would be achieved. Although $SmScO_3$ has a $\kappa$ value of 26, current gain compared to $HfO_2$ is not that high as compared to the other scandates, which might be due to the damage of the channel of the highly energetic pulsed laser deposition. For all devices the observed degradation in transconductance for high gate voltage is due to the reduced mobility at high electric fields.

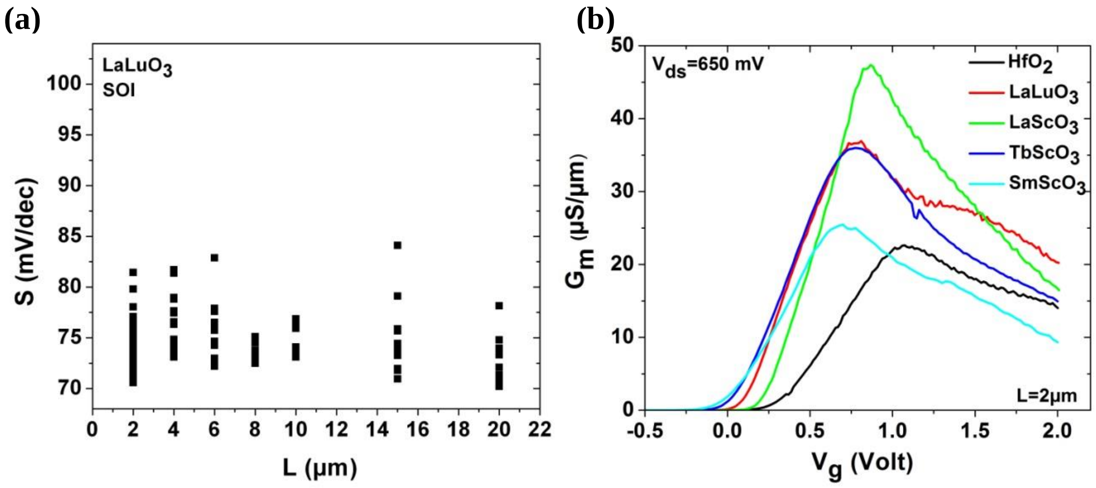


**Figure 4.8:** (a) Subthreshold slopes extracted from different gate length devices, (b) the transconductance extracted from differentiating $I_d$ over $V_g$. The $I_d$ current is corrected for the series resistance.

The gate capacitance, $C_g$, obtained from the split capacitance-voltage (C-V) measurement of different gate length for FD MOSFETs with $LaScO_3$ is plotted in Fig. 4.9 (a). The measured capacitance includes the overlap parasitic capacitance, $C_{ov}$, from the gate to S/D extension. To eliminate the $C_{ov}$ and extract the exact capacitance of the gate to channel, $C_{gc,corr}$ the correction which is mentioned in section 2.4.2 is applied. In Fig. 4.9 (b) the corrected gate to channel capacitance $C_{gc,corr}$ is plotted. The same depletion and almost the same inversion region imply a uniform oxide layer over the sample surface which finally results in an accurate mobility extraction. The maximum capacitance in inversion, $C_{ox}$, gave an

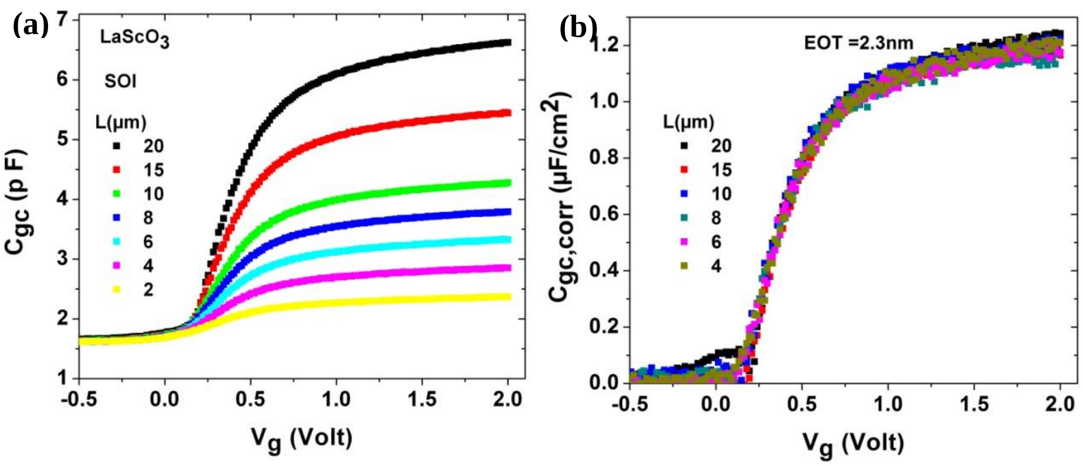


Figure 4.9: (a) split CV capacitance; $C_{gc}$ of FD MOSFET with 7 nm $LaScO_3$ on SOI, (b) corrected $C_{gc}$ yields EOT of 2.3 nm.

equivalent oxide thickness EOT of ~2.3 nm. Knowing the $C_{ox}$ and subthreshold slope helps to extract the density of interface states $D_{it}$ by using Equation 2.42. In table 4.3 the obtained EOT and $D_{it}$ values are listed for different gate oxides. The extracted $D_{it}$ values for $LaLuO_3$ and $LaScO_3$ based MOSFETs are in agreement with the results obtained from their MOS capacitor counterparts as reported in chapter 3, while $HfO_2$ devices show an order of magnitude deterioration as compared to the MOS capacitor with $HfO_2$. Bae et al. [105] have shown that, as the thickness of TiN increases, the stress on the film also increases, resulting in a higher $D_{it}$. On the other hand, according to Reimbold et al. [106] a TiN film behaves as a nitrogen reservoir. Nitrogen diffuses through the high-$\kappa$ layer, and results in a deteriorated interface, therefore, as the TiN thickness increases $D_{it}$ also increases. However both of these claims cannot explain the higher $D_{it}$ obtained for MOSFETs with $HfO_2$ since for both MOS capacitors and MOSFETs the TiN has the same thickness. The same problem is also observed for the $TbScO_3$ and $SmScO_3$ MOSFET system. While 2 times of degradation in $D_{it}$ is observed for $TbScO_3$ MOSFET system, this factor increases to 5 times for $SmScO_3$ system. This is most probably process related damage, since in MOS structures, a planar Si substrate has been used, however for the transistor, a mesa isolated Si layer with thermally grown $SiO_2$ passivated S/D and sidewalls were used. The $D_{it}$ most probably increased due to the stress induced defects caused by the TiN and sidewall passivation at the edges of the channel.

Fig. 4.10 shows the effective electron mobility derived from split C-V measurements for $HfO_2$ devices and different rare-earth based oxide MOSFETs. For an accurate mobility extraction capacitance and $R_{sd}$ correction were carried out as explained in section 2.4.2. The obtained mobilities of all high-$\kappa$ dielectrics are lower than the universal $SiO_2$ mobility curve.

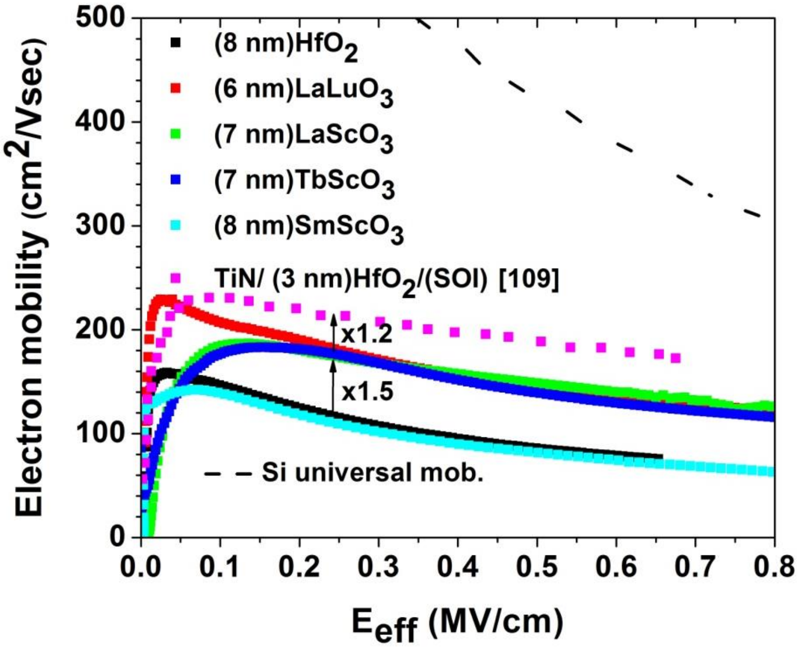


**Figure 4.10:** Effective electron mobility versus the effective field in FD MOSFETs with $HfO_2$ and rare earth based oxides. The universal Si mobility and mobilities extracted from MOSFETs with 3 nm $HfO_2$ are plotted as a comparison.

Although with the recent technologically improved devices and processes, the obtained mobility of devices with high-κ dielectrics is still lower than the universal $SiO_2$ mobility. The degradation of the channel mobility with high-*κ* dielectrics is mainly attributed to three scattering mechanisms. The first is remote Coulomb scattering (RCS), which occurs due to remote electrostatic interaction caused by charged species into the gate dielectric and at the interfaces to metal gate and the Si substrate. This kind of interactions modifies the electrostatic potential seen by electrons traveling in the conduction channel. Among the investigated MOS structures in Chapter 3, positive and negative oxide charges were observed. However, as already mentioned, the high portion of the observed negative charges is attributed to the wet etched Al metal, which is not the case for the MOSFETs. For $TbScO_3$, for example, $N_{ox} \sim 1x10^{11}$ $cm^{-2}$ and the scattering is relatively small, but is not negligible. It is worth indicating that, the observed oxygen vacancies, discussed in Chapter 3, while not causing scattering, they may trigger the transient carrier exchange between the channel and gate dielectric and result in a mobility reduction during a quasi-static measurement [107]. On the other hand, the observed Si diffusion towards the high-*κ* detected by the TOF-SIMS, could be another possible reason for RCS, if they are charged. Also, one should not underlook the Coulomb scattering due to the interface trap charge. Higher $D_{it}$ was observed for $SmScO_3$ and $HfO_2$ which showed 1.5 times lower electron mobility as compared to the other oxides. Moreover, the $D_{it}$ in $SiO_2$ MOSFETs is in the range of $10^{10}$ $(eVcm^2)^{-1}$, which is almost one order of magnitude lower than for MOSFETs with $LaLuO_3$, $LaScO_3$ and $TbScO_3$. The second scattering mechanism is surface roughness scattering which occurs at high applied electric field, and is mainly due to the deposition conditions and processing issues. This type of scattering decreases the mobility strongly at high electric field which is obvious in Fig. 4.10. The third scattering mechanism is the high-$\kappa$ related surface soft optical (SO) phonon scattering. Fischetti et al. have already shown that the large dielectric constant of the high-$\kappa$ materials originates from their strong ionic response which results in low-energy polar-optical phonons within the material [35]. Electrons at the Si channel will scatter from SO phonons via a Fröhlich interaction which has unscreened scattering field amplitude $\Phi_{\omega so}$ at the dielectric interface proportional to

$$\Phi_{\omega so} \sim \hbar\omega_{SO} \left[\frac{1}{\varepsilon_{Si}^{\infty}+\varepsilon_{ox}^{\infty}} - \frac{1}{\varepsilon_{Si}^{\infty}+\varepsilon_{ox}^{0}}\right], \quad (4.3)$$

where ħ is the reduced Planck constant, $\omega_{SO}$ is the frequency of the SO insulator phonon, $\varepsilon_{Si}^{\infty}$ is the optical permittivity of Si and $\varepsilon_{ox}^{\infty}$ and $\varepsilon_{ox}^{0}$ are the optical and the static permittivities of the dielectric, respectively. For the high-$\kappa$ dielectrics, an ionic bonding exists, therefore, there is a large difference between the $\varepsilon_{ox}^{\infty}$ and $\varepsilon_{ox}^{0}$. The first term in the square bracket represents the inverse of the electronic response of the dielectric, which is almost equal for all the dielectric materials. Since ions cannot fully respond at sufficiently high frequency, their optical permittivity (high frequency permittivity) is low and close to the $SiO_2$ one. The second term denotes the inverse of the ionic response. The ionic response is dominant at low frequencies and results in both, the high dielectric constant, ($\kappa = \varepsilon_{ox}^{0}/\varepsilon_{vac}$, where $\varepsilon_{vac}$ is the permittivity of the vacuum) and high scattering contribution due to ionic polarization. Simply, the higher the ionic response, the higher the dielectric constant and scattering contribution become. On the other hand, $\hbar\omega_{SO}$ (the phonon energy) increased with decreased "$\kappa$" value. In case of $SiO_2$ gate oxide, a covalent band exists, therefore the ionic response is small, that's why its "$\kappa$" value is small. Moreover, the Si-O bonds are quiet stiff, hence, they have a large $\hbar\omega_{SO}$, however, the electron in inversion layer cannot interact with too large energy. Therefore, for $SiO_2$ the SO phonon scattering does not really affect the electron mobility. In contrast, for high-$\kappa$ material, the carrier electron in the conductive channel undergoes more collisions with the low energy optical phonon and the mobility degrades. It can be concluded that, for high-$\kappa$ systems, even under ideal conditions, due to the high-$\kappa$ inherited SO phonon scattering, a reduced mobility will always be observed. Due to this fact, a very thin $SiO_2$ IL is suggested between the high-$\kappa$ and Si in order to reduce the scattering effect and improve the mobility [99].

For TiN/$HfO_2$ gate system, Sim et al. [108], showed that the mobility strongly depends on the thickness of the $HfO_2$. According to their assumption, increasing the film thickness results in an increase in oxide charges and dipoles which trigger RCS and SO phonon scattering. To point out their observation, a mobility curve for TiN/3 nm $HfO_2$/SOI system with an EOT of 1.4 nm is also plotted in Fig. 4.10 [109] which shows a 1.2x improvement as compared to our results with $LaLuO_3$, $LaScO_3$ and $TbScO_3$ and 1.8x improvement over the $HfO_2$ mobility measured in this work for an EOT of 3 nm. Surprisingly, although $LaLuO_3$, $LaScO_3$ and $TbScO_3$ have different dielectric permittivities, and in this experiment different EOT values, they show the same electron mobilities. According to XPS and TOF-SIMS measurements, the same mobility could be explained by the observed silicate like interfacial layer for those materials.

For the sake of further confirmation of the extracted split C-V mobilities, the effective electron mobility was also determined from the direct parameter extraction using $I_d(V_g)$ characteristics in strong inversion by applying the $I_d/\sqrt{g_m}(V_g)$ method as explained in section 2.4.2. The plot of 1/A as a function of gate length L is presented in Fig. 4.11(a). With the help of a linear fit, the low field mobility $\mu_o$ is extracted. In this way the effects of mobility reduction with gate voltage and $R_{sd}$ are avoided. For comparable thicknesses, a mobility reduction trend was observed for a decreased EOT in $\mu_o$. For $LaLuO_3$ MOSFET system, a 1.15x improvement in the $\mu_o$ over $LaScO_3$ sample was observed, while MOSFETs with $LaScO_3$ proved a 1.14 times of improvement over $HfO_2$ sample. This trend demonstrates the benefit of $LaLuO_3$ and $LaScO_3$ in terms of mobility. In order to calculate the effective electron mobility from the extracted $\mu_o$, first the mobility reduction coefficient θ is calculated from the $I_d(V_g)$ curve after correcting $R_{sd}$. The obtained results are 1.01 $V^{-1}$, 0.8 $V^{-1}$, and 0.43$V^{-1}$ for $HfO_2$, $LaLuO_3$ and $LaScO_3$ MOSFETs, respectively. The extracted effective electron mobilities from $I_d(V_g)$ are illustrated in fig. 4.11 (b) (solid lines). The intercept on the mobility axes is the low field mobility, $\mu_o$. For comparison, the split C-V mobilities are also added to the graph (solid squares). It is clear from this figure that a very good agreement is achieved between the two approaches. In both cases, the mobility degrades with the applied voltage, due to the further activated scattering mechanisms.

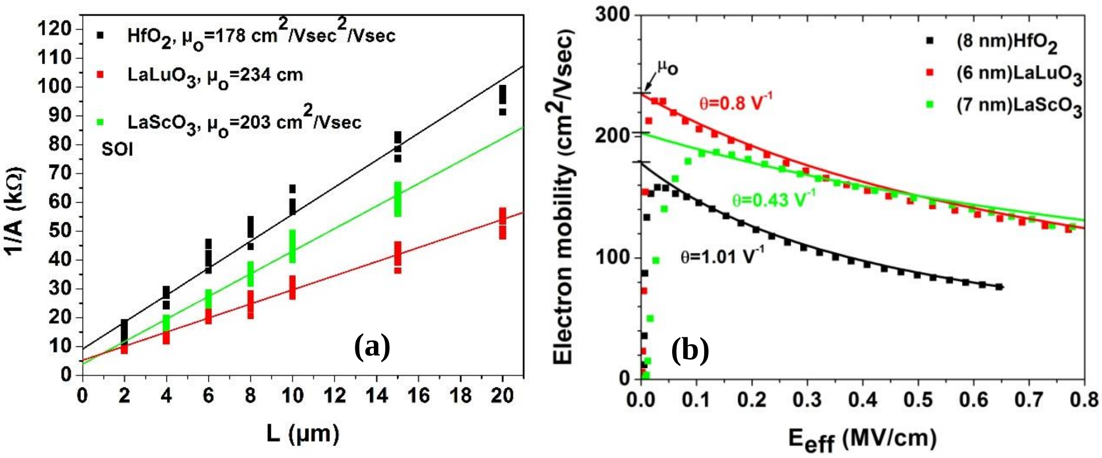


**Figure 4.11:** (a) Plot of the 1/*A* vs. the gate length *L* to extract the low field mobility parameter $\mu_o$ in the transistors with $HfO_2$, $LaLuO_3$ and $LaScO_3$ on SOI substrate. (b) Comparison of the effective electron mobilities obtained from split C-V (solid squares) and static $I_d(V_g)$ curves (solid lines).

## 4.3.2 n-MOSFETs on sSOI

Fig. 4.12 represents the measured output characteristics of MOSFETs with $LaLuO_3$ and $TbScO_3$ gate oxides on SOI and sSOI substrates at gate voltage ranging from 0 to 2.5 V. Devices with $LaLuO_3$ on sSOI substrate showed almost 80% enhancements of saturation currents as compared to SOI devices, which is an expected improvement with sSOI substrate. $TbScO_3$ devices on sSOI showed an enhancement factor over their SOI control device of ~20%. The large series resistance $R_{sd}$ limited the drain current from reaching the saturation at $V_g$=2.5 V. $TbScO_3$ devices on sSOI have lower $R_{sd}$ as compared to $LaLuO_3$ devices on sSOI. Therefore the enhancement factor over their SOI control remains almost the same, ~20%, for every applied gate voltage. The obtained drain current enhancement factor over SOI, the extracted $R_{sd}$ and the doping concentration are summarized in Table 4.4. As also observed for SOI devices, sSOI devices with $LaLuO_3$, $LaScO_3$ and $TbScO_3$ showed over 50% of improvement in maximum achievable drain current as compared to $HfO_2$ reference devices. On the other hand, the $R_{sd}$ still seems not to show a consistent variation among the high-$\kappa$ and even among SOI and sSOI, which is the result of the contact resistance and implantation through thick $SiO_2$ layers.

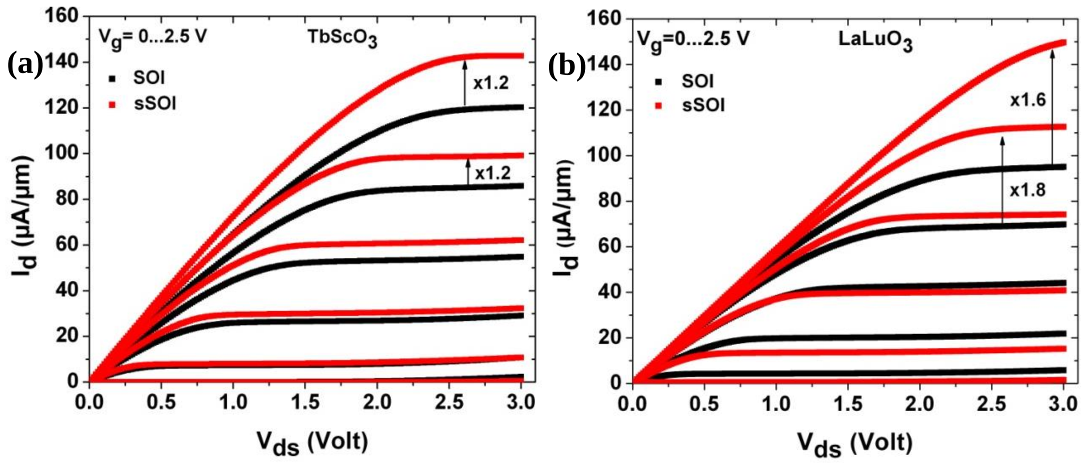


**Figure 4.12:** The output characteristics of FD MOSFET's with (a) $LaLuO_3$, (b) $TbScO_3$ gate oxides on SOI and sSOI substrates. L/W= 2/20 µm.

**Table 4.4:** sSOI drain current enhancement over SOI and the extracted $R_{sd}$.

| Material | $I_d$ Enhancement over SOI (%) | $R_{sd}$ (kΩµm) | $N_d$ ($cm^{-3}$) |
|---|---|---|---|
| $HfO_2$ | 70 | 7.8 | 8.89e18 |
| $LaLuO_3$ | 80 | 13.8 | 3.92e18 |
| $LaScO_3$ | 40 | 3.0 | 2.27e19 |
| $TbScO_3$ | 20 | 7.6 | 7.90e18 |

Fig. 4.13 shows the transfer characteristics of FD MOSFETs with $LaScO_3$ and $TbScO_3$ gate oxides on SOI and sSOI substrates at drain voltages ranging from 50 to 650 mV. For all of the devices no remarkable change was observed in the subthreshold slope(see Fig. 4.14 (a)) and off-currents. GIDL still remains a limiting issue for the off current. Obtaining the same subthreshold slope for sSOI as compared to their SOI control devices implies good oxide properties. The improvement in the on current is an expected consequence of the sSOI

substrate. On the other hand, as already been observed by Lim et al. [110], due to the strain induced band gap-narrowing, the change of the electron affinity and stress induced changes in the density-of-states a threshold voltage shift $\Delta V_T$ was observed in sSOI devices compared to their SOI control transistors. The statistical distribution of the $V_T$ for FD MOSFETs with $LaLuO_3$ on sSOI substrate is plotted in Fig. 4.14 (b) and the obtained $\Delta V_T$ shifts are summarized in Table 4.5. The $\Delta V_T$ variation from one high-$\kappa$ to another stems from both, the different reaction of each high-$\kappa$ with TiN and different interface to SOI and sSOI substrates. However, no $V_T$ shift for $TbScO_3$ devices remains unclear. One possible reason could be that the TiN induced tensile stress on the film. According to Choi et al. [111] as the tensile stress induced by the metal increases, the work function of the metal decreases. As a result devices with $TbScO_3$ on SOI substrate might show a lower threshold voltage, which finally became the same as the one of sSOI devices.

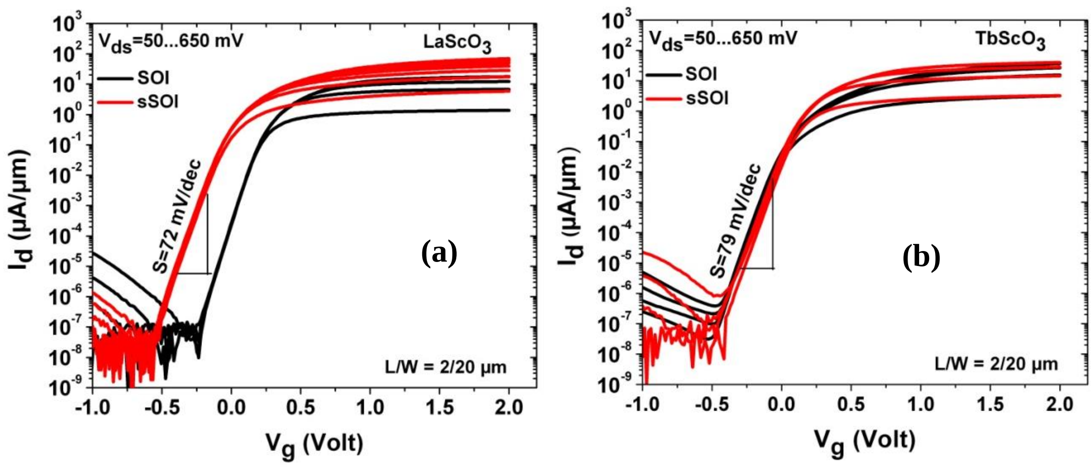


**Figure 4.13:** Transfer characteristics of FD MOSFETs with (a) $LaScO_3$ and (b) $TbScO_3$ gate oxides on SOI and sSOI substrates.

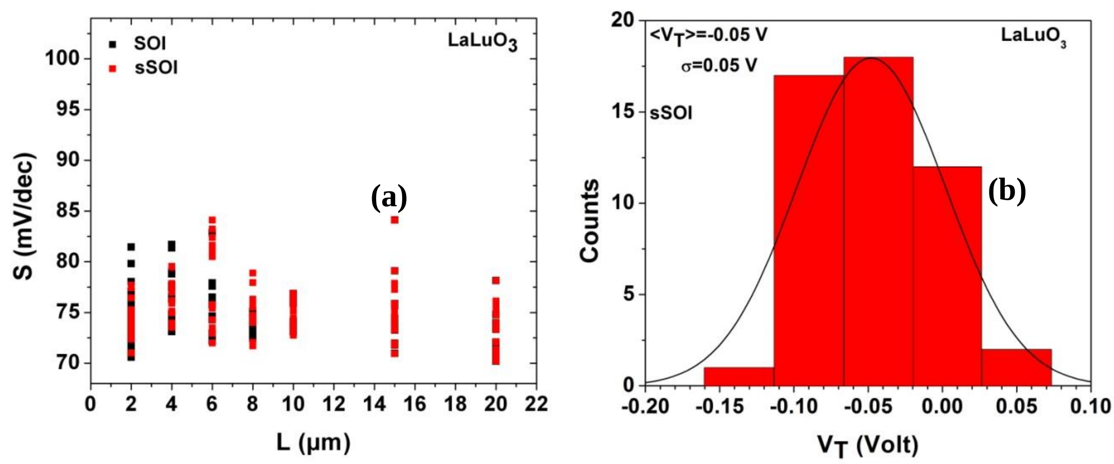


**Figure 4.14:** (a) Subthreshold slope variation over gate length, $L_g$ on SOI and sSOI substrates, (b) statistical distribution of the threshold voltage on for FD MOSFETs with $LaLuO_3$ on sSOI substrates.

**Table 4.5:** sSOI drain saturation current enhancement over SOI and the extracted $R_{sd}$.

| Material | $\Delta V_T$ (mV) | $R_{sd}$ (kΩµm) | EOT (nm) |
|---|---|---|---|
| $HfO_2$ | ~-200 | 7.8 | ------------ |
| $LaLuO_3$ | ~-180 | 13.8 | 1.7 |
| $LaScO_3$ | ~-210 | 3.0 | 2.3 |
| $TbScO_3$ | ~0 | 7.6 | 3.0 |

The transconductance enhancement with the sSOI substrate for a drain voltage of 650 mV is plotted in Fig. 4.15 as a function of gate length. A significant improvement was observed with the strained silicon devices. Since $R_{sd}$ did not vary too much for devices with $TbScO_3$ on SOI and sSOI, the enhancement factor remains the same as observed from the output characteristic. However, for $LaLuO_3$ and $LaScO_3$ the enhancement is slightly higher than that extracted from their output characteristics due to the change in $R_{sd}$.

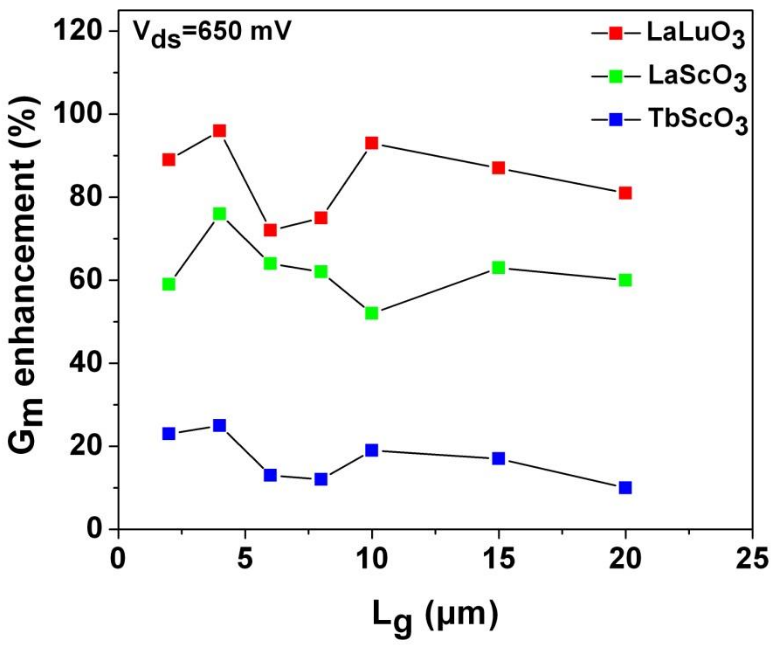


**Figure 4.15:** Transconductance enhancement with sSOI substrate over SOI. The lowest enhancement of ~20% was observed for $TbScO_3$ devices.

The split C-V measurements on sSOI devices yielded similar EOT for $LaLuO_3$ and $LaScO_3$. However a slight increase was observed for $TbScO_3$ most probably due to the oxide growth and oxide reactions on different substrates. This could explain the observed $\Delta V_T$ =0 and lower transconductance enhancement over their SOI control for these devices. The obtained EOT values are included to table 4.5. An example for the corrected split C-V is plotted in fig. 4.16(a). Due to similar subthreshold slopes S and $C_{ox}$, no change was observed on the extracted $D_{it}$ as compared to the SOI ones. The extracted split C-V electron mobilities are plotted in Fig. 4.16(b). For the whole electric field range, $LaLuO_3$, $LaScO_3$ and $TbScO_3$ provide the same electron mobility, similar to the SOI devices shown in Fig.4.10. These dielectrics on SOI substrate provide an electron mobility of 179 $cm^2/Vs$ at an effective field of 0.24 $MV/cm^2$ (Fig. 4.10). A 90% improvement is achieved by using biaxial tensile strained sSOI with a stress of 1.35 GPa. Such an enhancement with sSOI was also observed by Andrieu et al. [112] and Barral et al. [38]. However, the obtained mobilities at high electric field are lower than what they extracted as shown in the Fig. 4.16(b) and only match with universal $SiO_2$ mobilities at high electric field due to SO phonon scattering and RCS. Unfortunately, the deposition conditions and the right metal gate also play an important role in mobility degradation due to different oxide and interface trap charges which may cause stronger SO phonon scattering and RCS.

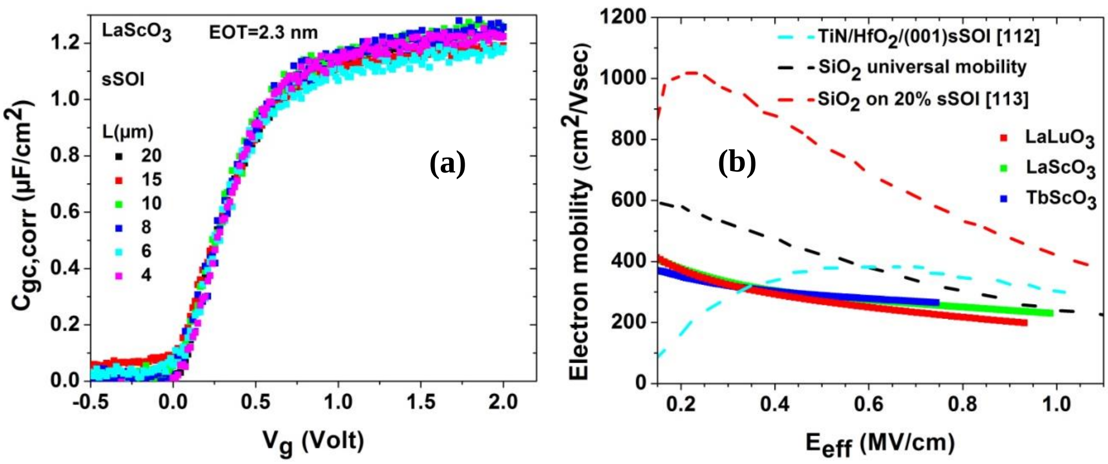


**Figure 4.16:** (a) Corrected split Capacitance-Voltage curve for devices with $LaScO_3$ on sSOI substrate, (b) electron mobility for different rare-earth based oxides and the reference $SiO_2$ universal, $SiO_2$ on sSOI [113] and $HfO_2$ on (001) sSOI substrate.

## 4.3.3 p-MOSFETs on SOI

p-MOSFETs were also fabricated with $LaLuO_3$ and $LaScO_3$. Typical output characteristics of p-MOSFETs are plotted in Fig. 4.17 (a) and (b), at $V_g$-$V_t$ from 0 to 2.5 V. Both type of devices show good on currents, however, there is a slight distortion in the linear part which is extended by the large series resistance. The series resistance $R_{sd}$ derived from output characteristics is plotted in Fig. 4.17(b) and (c) which are as high as the one observed for the n-MOSFETs.

The transfer characteristics and gate leakage of FD p-MOSFETs are shown in Fig. 4.18. Due to the thicker films at least two orders of magnitude lower leakage current is achieved and the gate leakage is not affected by GIDL in the off-state. Both devices show very low off-currents and high $I_{on}/I_{off}$ ratios of $10^{10}$ for $LaLuO_3$ device and $10^{11}$ for $LaScO_3$

MOSFET, respectively. Similar to n-FETs, the GIDL limits the off currents as $V_{ds}$ increases. The devices showed an almost ideal subthreshold slope S, reaching 65 mV/dec, and the slope does not show a strong variation over gate length as shown in Fig. 4.19(a) which refers to a slight change in interface charge traps. On the other hand, the change in interface charge could also be screened by the variation of the threshold voltage, $V_T$. As the subthreshold slope decreased, the threshold voltage also decreased as shown in Fig. 4.18 (b).

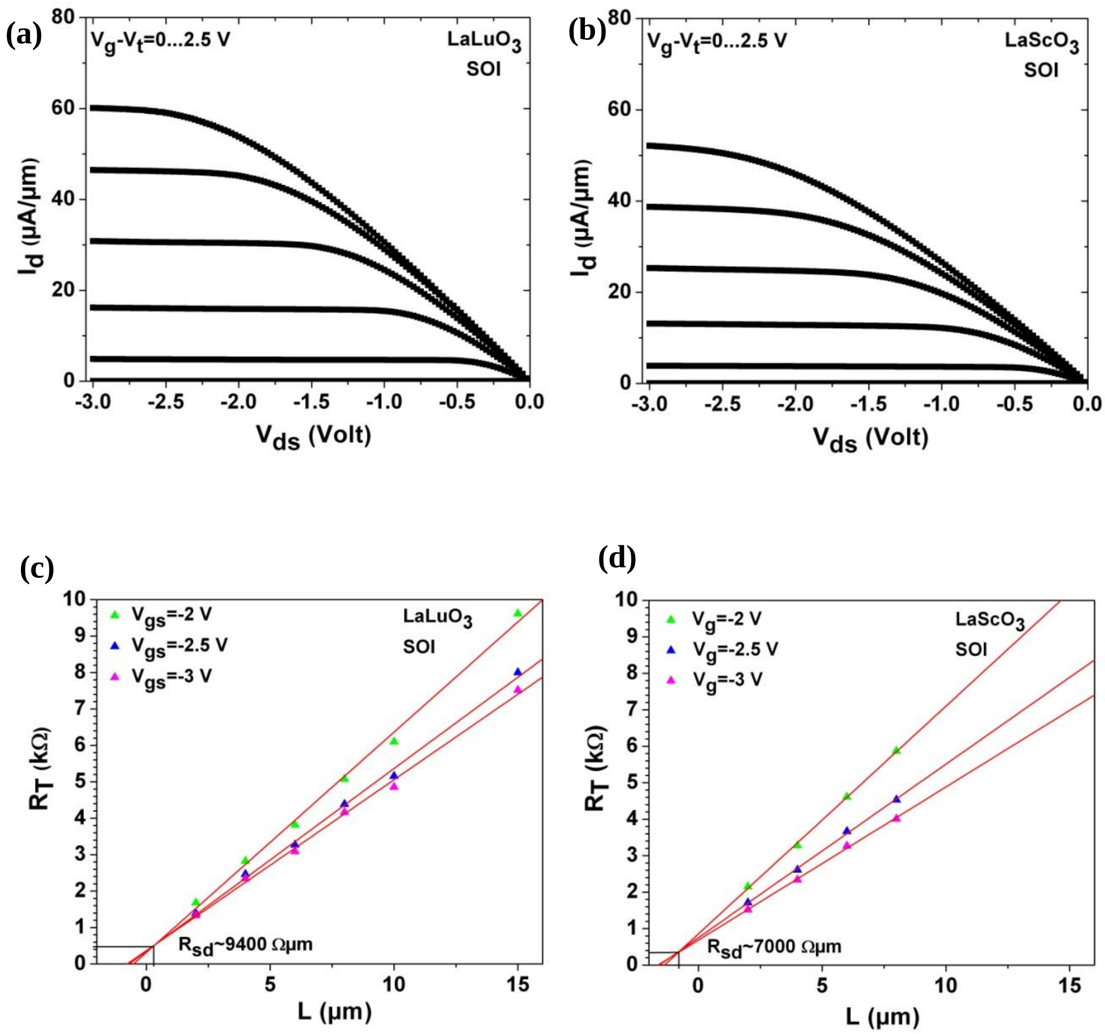


**Figure 4.17:** Output characteristics of FD p-MOSFETs with (a) $LaLuO_3$ and (b) $LaScO_3$ on SOI (L=2 µm). (c) and (d) the total resistance $R_T$ as a function of gate length L for the investigated oxides for gate voltage ranging from -2 to -3 V. The gate width is W=20 µm.

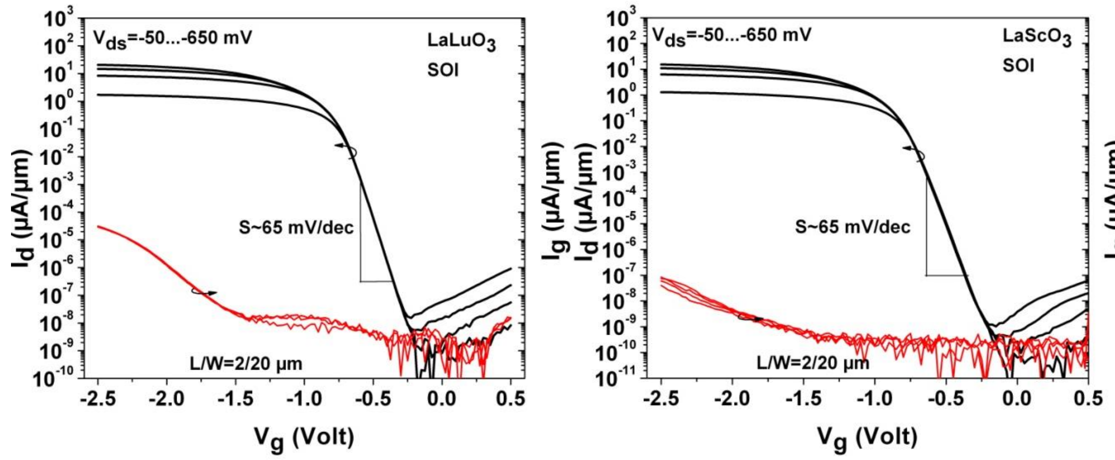


**Figure 4.18:** Transfer and gate leakage characteristics of FD p-MOSFETs with $LaLuO_3$ and $LaScO_3$ on SOI substrate.

The main reason for $V_T$ change is actually the total depletion charge $Q_D$. The interface charges are in parallel to the depletion charge, and any change in their amount easily affects the total $Q_D$. Therefore, depending on their variation the $V_T$ can increase or decrease. In Fig. 4.19 (b) the decrement in subthreshold slope and threshold voltage refers to the less charged interface traps which are already observed by Zhao et al. [114] and Chiang et al. [115]. The statistical distributions of $V_T$ for these devices are shown in Fig. 4.19 (c) and (d) where an average $V_T$ of -0.73 V for $LaLuO_3$ and -0.79 V for $LaScO_3$ was obtained. These obtained results are not symmetric to the n-MOSFETs with the same gate dielectrics which is due to below midgap work function of ~ 4.3eV for TiN.

The split capacitance-voltage measurement of p-MOSFETs with $LaLuO_3$ and $LaScO_3$ shown in Fig. 4.20 yielded EOT values of 2.3 nm and 2.8 nm, respectively. The obtained mobility from the split C-V is shown in Fig. 4.21 with reference $HfO_2$ [38], HfSiON [116] and the universal Si mobility. Devices with $LaLuO_3$ and $LaScO_3$ showed almost the same hole mobility, similar to electron mobility in n-FETs. Their mobilities are comparable to that of HfSiON, and are higher than the ones with $HfO_2$. Although, the hole mobilities in high-$\kappa$ devices remain still below the universal curve, the degradation is not as severe as for the electron mobility. One should note that, the effective hole mobility is always lower than the effective electron mobility due to larger effective mass of hole and the scattering probability of the heavy holes in a high-$\kappa$ based p-MOSFET channel due to the OP phonon scattering or RCS is lower as compared to light electrons in a high-$\kappa$ based n-MOSFET.

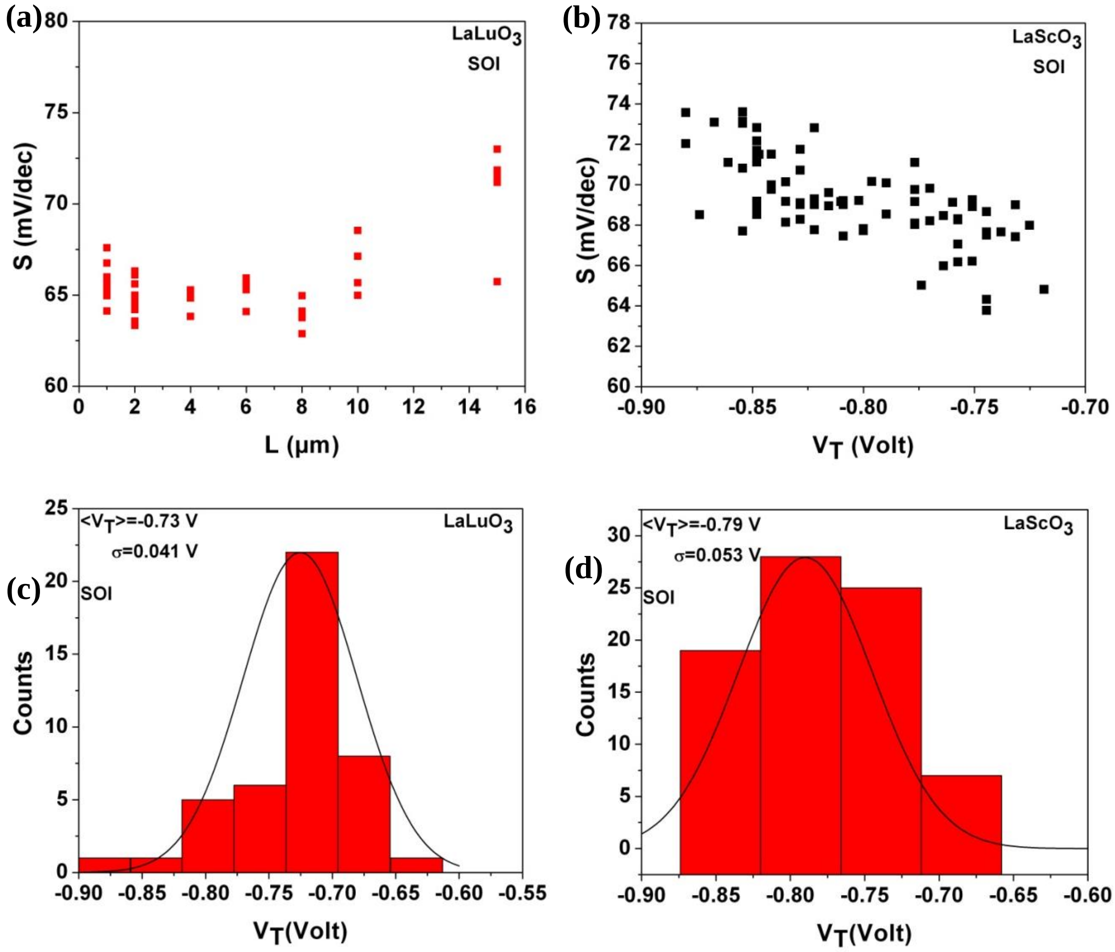


**Figure 4.19:** Subthreshold slope variation over (a) gate length, L, (b) threshold voltage $V_T$ and statistical distribution of threshold voltage in (c) and (d) for FD p-MOSFETs with $LaLuO_3$ and $LaScO_3$ gate oxides.

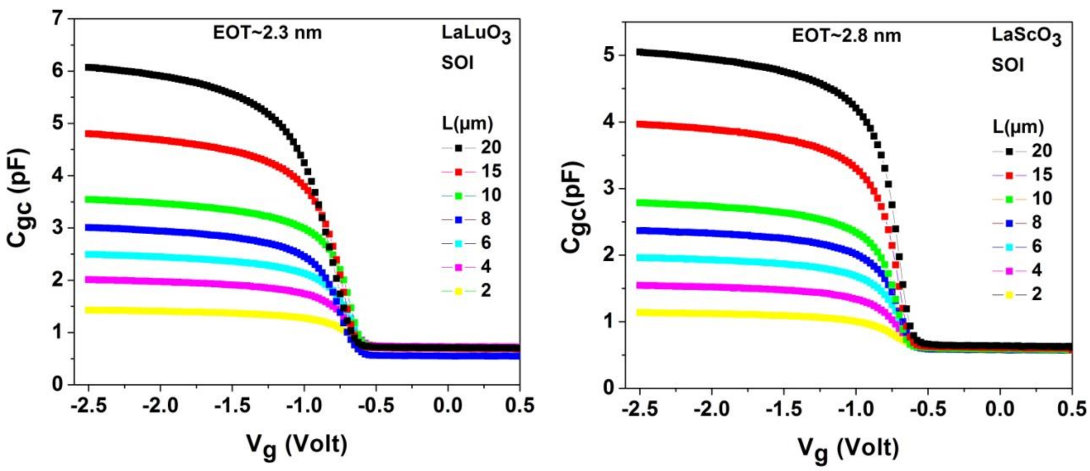


**Figure 4.20:** Split capacitance-voltage measurement of FD p-MOSFETs with $LaLuO_3$ and $LaScO_3$ for different gate length.

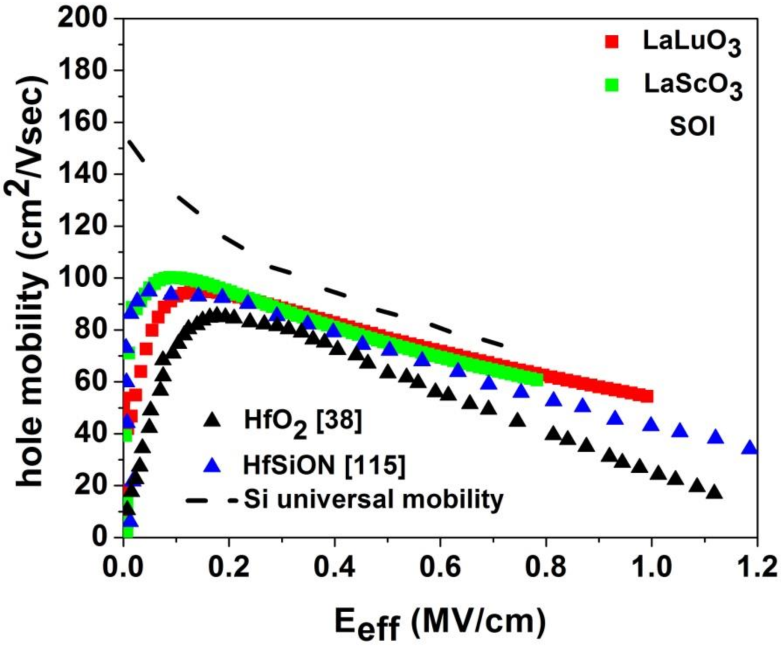


**Figure 4.21:** Hole mobility of devices with $LaLuO_3$ and $LaScO_3$ gate oxides. HfSiON, $HfO_2$ and universal mobilities are also plotted for comparison.

## 4.3.4 Gate induced drain leakage (GIDL)

In accumulation the transistor is in the off-state. When the drain of an n-MOSFET is biased at a positive voltage $V_d$ and the gate is biased with a negative $V_g$ an electric field is created and thus a deep depletion region is formed at the surface of the overlap region between the gate and drain as shown in Fig. 4.22 (a). Gate induced drain leakage (GIDL) is caused by band to band tunneling in the deep depletion region when the band bending is larger than the Si band gap. The band bending exceeds the band gap, electrons in the valence band tunnel to the conduction band giving rise to band to band tunneling (BTBT). Those electrons are swept to the drain due to the lateral electric field giving rise to drain current [117, 118, 119]. In addition, trap assisted tunneling by traps located at an energy level of $E_t$ [120, 121] can also enhance BTBT resulting in larger GIDL. Fig. 4.22(b) shows the trap assisted BTBT, where electrons in the valence band and at the interface tunnel to the conduction band. GIDL can be estimated by the following equation [122]

$$I_{GIDL} = A \cdot \xi_s \cdot exp\left(-\frac{B}{\xi_s}\right) \quad , \tag{4.4}$$

where A is a pre-exponential coefficient, B a constant depending on the barrier height and $\xi_s$ the electric field at the gate to drain overlap region and defined as [118]

$$\xi_s = \frac{\epsilon_{SiO2}}{\epsilon_{si}} \cdot \left(\frac{V_{DG}-\psi_s}{T_{ox}}\right) \ , \tag{4.5}$$

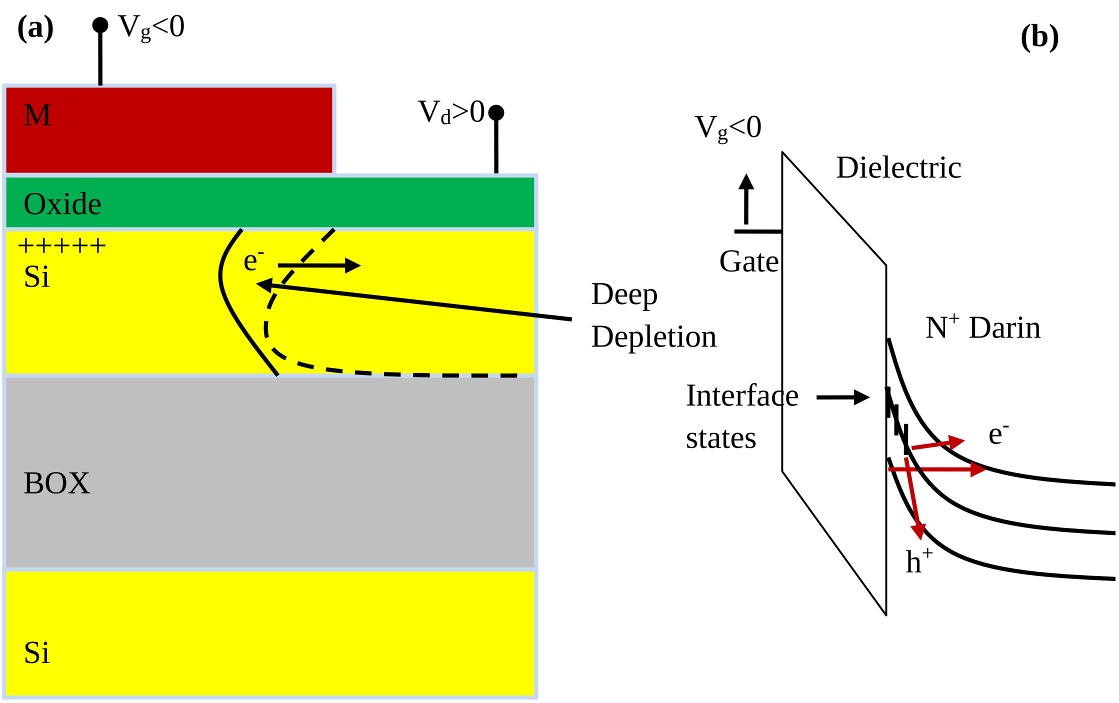


**Figure 4.22:** (a) Schematic current flow under GIDL bias, (b) band diagram of the gate to S/D overlap region.

where $\epsilon_{SiO2}$ and $\epsilon_{si}$ denote the dielectric constant of $SiO_2$ and Si, respectively, $T_{ox}$ the equivalent oxide thickness of the gate dielectric, $V_{DG}$ the potential difference between drain and gate biases and $\psi_s$ is the surface potential and is given by [122]

$$\psi_s = V_{DG} + \frac{T_{ox}^2}{\epsilon_{SiO2}^2} q \cdot N_D \cdot \epsilon_{Si} - \sqrt{(V_{DG} + \frac{T_{ox}^2}{\epsilon_{SiO2}^2} q \cdot N_D \cdot \epsilon_{Si})^2 - V_{DG}^2} \quad , \qquad (4.6)$$

where $N_D$ is the doping concentration. The electric field strongly depends on $V_{DG}$. According to Chen et al [1987], since the band gap of Si is $E_g$=1.12 eV a $\psi_s$=1.2 eV (which is the band bending) is enough to cause BTBT. Therefore $\psi_s$ is chosen to be a constant number equal to 1.2 eV. For the case of indirect tunneling B can be expressed by [122]

$$B = \frac{4 \cdot (2m_r)^{\frac{1}{2}} \cdot E_g^{\frac{3}{2}}}{3q\hbar} \quad , \qquad (4.7)$$

where, $m_r$ is the reduced effective mass of electron, equal to 0.2 times the free electron mass for trap free samples or direct BTBT and $E_g$ denotes the energy gap of silicon. This results in B=36 MV/cm [120]. However, if tunneling is mainly assisted by interface traps located at an energy level $E_t$ relative to the valence band edge, B ranges between 10 to 29 MV/cm and $E_g$ should be replaced by $E_g$-$E_t$, as an effective barrier height for electron tunneling

[120]. After measuring the GIDL current, which is the output current under GIDL bias (negative $V_g$ step for n-MOSFETs, and positive $V_g$ steps for p-MOSFETs) the coefficient B could be extracted from the slope of the linear portion of the $\ln(I_{GIDL}/(V_{dg}-1.2))$ vs. $(1/(V_{dg}-1.2))$ plot as [120]

$$slope = \frac{\epsilon_{Si}}{\epsilon_{siO2}} \cdot B \cdot T_{OX} \,. \tag{4.8}$$

After obtaining the B parameter, one can extract the final barrier height and the energetic position of the interface trap states.
Fig. 4.23 shows the GIDL current under GIDL bias ranging from -1 to -2 V. GIDL can only occur at high electric field. The larger the electric field the higher the tunneling can occur, as also can be seen in the figure. Due to the non-conformal deposition and process related non uniformities, devices with $LaLuO_3$ and $LaScO_3$ on sSOI showed low GIDL current compared to their SOI control samples, however, the opposite behavior was observed for devices with $TbScO_3$.

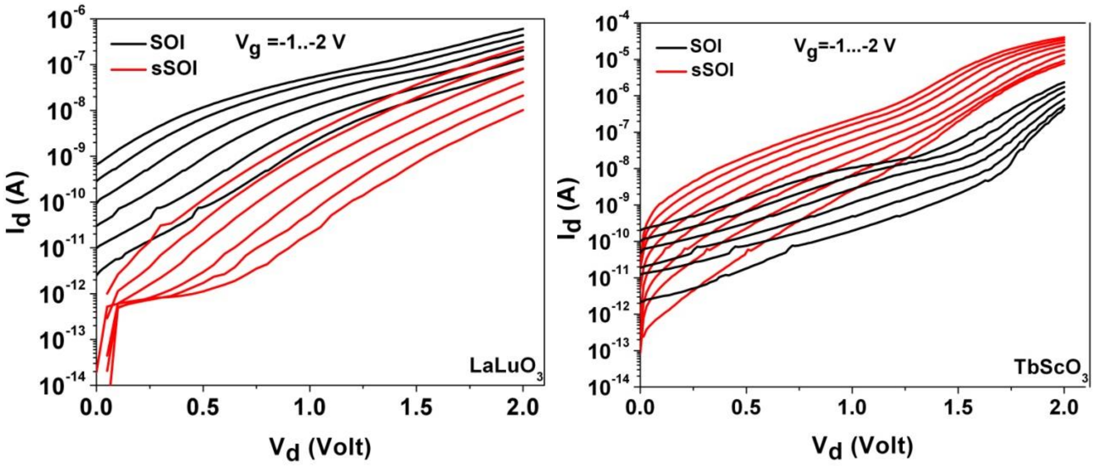


**Figure 4.23:** GIDL current for n-MOSFETs with $LaLuO_3$ and $TbScO_3$ gate oxides on SOI and sSOI substrates under GIDL bias $V_g$.

Fig. 4.24 shows $\ln(I_{GIDL}/(V_{dg}-1.2))$ vs. $(1/(V_{dg}-1.2))$ for the extraction of the B parameter for high-$\kappa$ on different substrates. The extracted B parameters using equation (4.8) are listed in Table 4.6. These calculated values indicate that the main reason for GIDL is trap assisted band-to-band tunneling. $E_t$ values are extracted from the B parameter taking into account $E_g$ = 1.12 eV for SOI and 1.0 eV for sSOI, as calculated in Ref. [123],

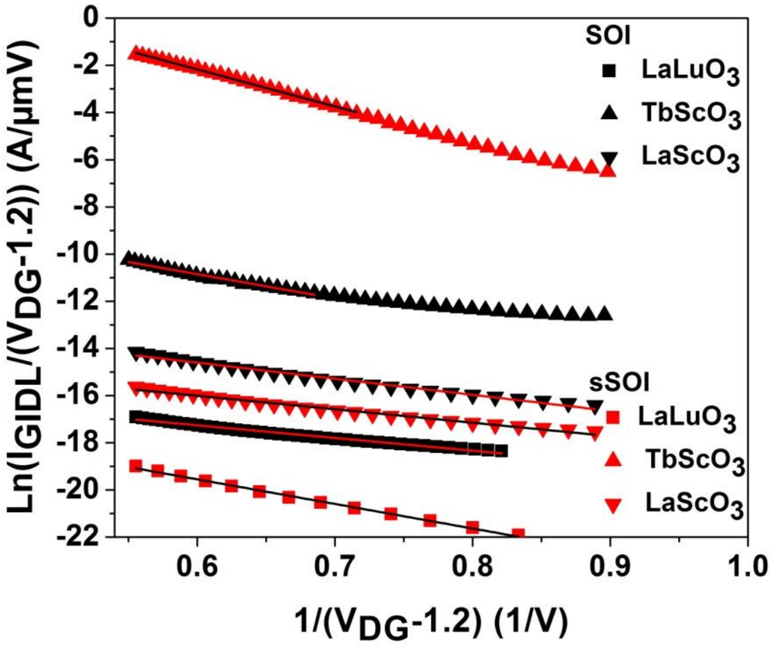


**Figure 4.24:** $\ln(I_d/(V_{DG}-1.2))$ vs $1/(V_{DG}-1.2)$ for the extraction of B parameter.

**Table 4.6:** The extracted B parameters and $E_t$ positions for FD MOSFETs with $LaLuO_3$, $TbScO_3$ and $LaScO_3$

| Material | B (MV/cm) (SOI/sSOI) | $E_t$ (eV) (SOI/sSOI) |
|---|---|---|
| $LaLuO_3$ | 13/17 | 0.55/0.31 |
| $TbScO_3$ | 12/16 | 0.58/0.35 |
| $LaScO_3$ | 11/10 | 0.6/0.51 |

and listed in Table 4.6. Obviously, in all SOI devices the interface states are located around midgap, and due to the strained silicon, their position is shifted more to the valance band edge. The obtained $E_t$ values for SOI devices are supporting the values obtained from high-frequency C-V measurements on bulk Si, which were found to be located around midgap.

## 4.4 Summary

A replacement gate process was used for the fabrication of p- and n-MOSFETs on SOI as well as on sSOI substrates with the alternative gate dielectrics $LaLuO_3$, $LaScO_3$, $TbScO_3$ and $SmScO_3$. Specifically, apart from the MOSFET characteristics, the current gain and the mobility were investigated. $HfO_2$ based MOSFET devices were used for comparison. As a high mobility channel material, sSOI substrates were used for comparison with SOI.
It was found that, despite $R_{sd}$ variations, among the n-MOSFETs with SOI substrate, $LaLuO_3$, $LaScO_3$ and $TbScO_3$ provided superior performance. Much higher on current, con-

sequently higher transconductance, as compared to $SmScO_3$ and $HfO_2$ MOSFETs, was observed. $I_{on}/I_{off}$ ratios over $10^9$ and a subthreshold slopes as low as 72 mV/dec were achieved with these devices. However, due to the high fringing field, also triggered by the non-conformal high-k deposition, actually a requirement for replacement gate process, pronounced GIDL was observed, which prevented even lower lower $I_{off}$ for the devices. The electron mobility extracted from split CV technique or static $I_d(V_g)$ curve amounts to ~179 $cm^2/Vs$ at an effective field of 0.24 $MV/cm^2$, which is 1.5 times higher than the one obtained for $SmScO_3$ or $HfO_2$. However, a degradation in electron mobility for all high-$\kappa$ dielectrics as compared to universal mobility data is observed due to high-k inherited OP phonon scattering and RCS.

Among the results obtained from FD-n-MOSFETs on biaxially strained SOI, $LaLuO_{3,}$ $LaScO_3$ and $TbScO_3$ provides much better performance than the $HfO_2$ reference. As compared to their SOI counterparts, an enhancement of 80%, 40% and 20% was achieved in the on current for $LaLuO_{3,}$ $LaScO_3$ and $TbScO_3$, respectively. The difference in the enhancements is due to the variation in $R_{sd}$ for SOI and sSOI devices. The same subthreshold slopes for sSOI and SOI were achieved. Due to different reactions of each high-$\kappa$ oxide with the TiN metal gate a $<\Delta V_T>$ shift was observed between SOI and sSOI devices. However, due to TiN related stress or, larger EOT, no $\Delta V_T$ was observed for $TbScO_3$ devices. The electron mobility was improved by 90% with sSOI substrates, and even higher mobilities are expected for EOT below 1 nm.

The long channel FD-p-MOSFETs were fabricated on SOI substrates, using $LaLuO_3$ and $LaScO_3$. Good transistor performance was observed. Almost ideal steep subthreshold slopes down to 65 mV/dec and high $I_{on}/I_{off}$ over $10^{10}$ were achieved. Their hole mobility is almost identical, however, slightly lower than the universal reference data but higher than what obtained with $HfO_2$ or HfSiON.

The investigation of GIDL on SOI and sSOI for $LaLuO_{3,}$ $LaScO_3$ and $TbScO_3$ reveals that trap assisted band-to-band tunneling occurs. The position of the traps, $E_t$, associated with tunneling is extracted from the B parameter. While for SOI devices the traps are located around mid-gap, for sSOI devices with $LaLuO_3$ and $TbScO_3$ the level moved more to the valance band edge. Only for $LaScO_3$ on sSOI the trap level remained around mid-gap position. These obtained results for SOI devices are in good agreement with the results obtained from corresponding MOS capacitors.

# Chapter 5

# Summary

Investigation of higher-$\kappa$ dielectric materials is important for scaling down the electronic devices for future nanoelectronics to replace Hf-based oxides that are currently being used. In this thesis, MBD grown $LaLuO_3$ and $LaScO_3$, E-gun deposited $TbScO_3$ and PLD grown $SmScO_3$ have been investigated, both, structurally and electrically. For the first time, their integration into MOSFETs has been successfully achieved using SOI and strained SOI substrates. The composition of the films was studied by means of RBS, while XPS and TEM were used for morphology investigations. TEM together with XPS and TOF-SIMS were used to investigate the interfacial reactions with silicon substrate or top metal gate. Optimization of the annealing was studied on $LaLuO_3$ and $LaScO_3$ gate dielectrics deposited on silicon to achieve the lowest defect states and leakage current density and finally applied to the whole gate dielectrics used in this study. The optimized conditions finally will reduce the amount of the mobility degradation and improve the performance in actual MOSFETs. The main findings and contributions of this work are summarized below.

RBS measurements of $LaScO_3$ and $SmScO_3$ reveal, independently of the deposition technique, a stoichiometry with a ratio close to 1 between the metallic elements, La:Sc and Sm:Sc, respectively, by using appropriate growth conditions. FG annealing at 400 ºC to the MOS capacitor does not change the stoichiometry of the films. These materials have proven to show higher crystallization temperatures as compared to $HfO_2$ which crystallize at 550 ºC. $SmScO_3$ remains amorphous on silicon up to 800 ºC and starts to crystallize at 900 ºC, while $LaScO_3$ crytallizes above 800 ºC. $LaLuO_3$ and $TbScO_3$ stay amorphous up to 1000 ºC. Therefore, possible defect formation caused by the poly-crystalline structure due to elevated process temperatures could be avoided by using these materials.

Detailed XPS and TOF-SIMS investigations of $LaLuO_3$, $LaScO_3$ and $TbScO_3$ reveals silicate formation at the high-k/silicon interface which slightly increases after thermal treatment of the films in oxygen and FG ambient. According to the TOF-SIMS of TiN/$LaLuO_3$ ($TbScO_3$)/$SiO_2$/Si, at first glance, the application of PDA at 400 ºC in oxygen and FG ambient seems to deteriorate the films in terms of the interfacial layer growth. However, as compared to a reference sample with PMA only, those samples after applying

PMA show better interface and oxide quality. PMA results in a reduced $SiO_2$ interfacial layer thickness in the TiN/high-$\kappa$/$SiO_2$/Si system due to the oxygen scavenging effect of the TiN metal gate. Anneals (PDA+PMA) help to increase the areal density of the high-$\kappa$ by the reduced vacancy, during oxygen scavenging from the $SiO_2$ interfacial layer, which results in suppressed silicon diffusion towards the high-$\kappa$ dielectric due to filled vacancies. This minimizes a possible mobility degradation.

A comprehensive investigation of the electrical characteristics carried out on post metal annealed TiN/$LaLuO_3$($LaScO_3$)/Si system showed that it is possible to achieve EOT as small as 0.6 nm with a low leakage current density down to $10^{-3}$ A/cm$^2$. However, in order to improve the electrical properties and reduce the defects present in the oxide and at the oxide-silicon interface, PDA in $O_2$ and FG are needed. PDA combined with PMA improves the interface quality with a lower defect states as low as $8x10^{10}$ (eVcm$^2$)$^{-1}$ and provide up to 4 orders of magnitude reduction in leakage current. Furthermore, the hysteresis is suppressed and flat band voltage $V_{FB}$ shift is reduced, however the EOT increased due to the increase in the interfacial layer thickness. The application of PDA+PMA not only improves the CV characteristics of the films but also does not change the $\kappa$ value. Compared to $HfO_2$, $LaLuO_3$, $LaScO_3$, $TbScO_3$ and $SmScO_3$ offer significant higher $\kappa$ values, ranging from 26 to 32. Due to their higher-$\kappa$, it is possible to achieve smaller EOT with $LaLuO_3$ and $LaScO_3$ as compared to $HfO_2$ with a similar film thickness. However, because of the interfacial layer growth, caused by the deposition techniques, $TbScO_3$ and $SmScO_3$ show poorer EOT scaling. Therefore, for all of the investigated high-$\kappa$ oxides, further investigations on interfacial layer scavenging are needed.

Negligible hysteresis, low interface trap and oxide charges, and for a comparable EOT, up to three orders of magnitude lower leakage current as compared to $HfO_2$ make these materials attractive for next chip generations. However, further work should be carried out in order to suppress the oxygen vacancies in these materials, which are the most effective defects in reducing the metal work function and finally trigger the threshold voltage of the active devices.

A replacement gate process for MOSFET has been developed. The integration of $LaLuO_3$, $LaScO_3$, $TbScO_3$ and $SmScO_3$ has been, for the first time, successfully achieved on fully depleted (FD) n-MOSFETs using SOI and sSOI substrates. $LaLuO_3$, $LaScO_3$ and $TbScO_3$ show very good transistor performance. Steep subthreshold slopes, as small as 72 mV/dec, high $I_{on}/I_{off}$ ratios over $10^8$, and a low density of interface states in the range of $5x10^{11}$ (eVcm$^2$)$^{-1}$ could be achieved. MOSFETs with $TbScO_3$, $LaScO_3$ and $LaLuO_3$ on SOI substrates reveal electron mobilities of 180, 183 and 188 cm$^2$/Vsec, respectively. The sSOI n-MOSFETs show strongly enhanced transconductance and electron mobilities up to a factor of 1.8 compared to SOI reference devices. The mobility and transconductance is enhanced because lifting of the band degeneracy increases the occupancy of the lower mass subband $\Delta_2$ and decreases carrier scattering due to the energy split between the $\Delta_2$ and $\Delta_4$ valleys.

Fully depleted p-MOSFETs with $LaLuO_3$ and $LaScO_3$ have also, for the first time, successfully achieved using SOI substrates. The obtained almost ideal subthreshold slope of 65 mV/dec, high $I_{on}/I_{off}$ ratios over $10^9$ and effective hole mobility comparable with

HfSiON on silicon and slightly better than what could be obtained with $HfO_2$ on SOI make those material much more promising for CMOS applications.
GIDL is observed, in both, p- and n-MOSFETs. High-$\kappa$ layers with EOT<3 nm are used in this work, and since the high-$\kappa$ depositions are not conformal (even thinner oxide at the channel edges), GIDL is an expected issue for such thin oxide layers. In summary the mobility degrades due to the high-$\kappa$ inherent soft optical phonon scattering (SO), remote Coulomb scattering (RCS) and surface roughness. Impurities and metal gate-high-$\kappa$ interface defects can also cause reduction in the mobility. Therefore, careful cleaning and process optimization is needed to minimize these effects. However, it should also be noted that, SO phonon scattering will always be observed due to the intrinsic properties of the high-$\kappa$ materials.
In order to determine the mobility of the rare-earth based ternary oxide, without any short channel effect and leakage problem, long channel devices with thick oxide layer (EOT>1.5 nm) were used. Therefore, as next step short channel devices with EOT<1 nm should be investigated.

# Bibliography

[1] G. E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics,* pp. 114-117, 1965.

[2] R. H. Dennard, F. H. Gaensslen, H-N. Yu, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of solid-state circuits,* Vols. SC-9, no. 5, p. 256258, 1974.

[3] G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to 1/4 micrometer MOSFET design," *IEEE Trans. Electron Devices,* vol. 31, no. 4, pp. 452-462, 1984.

[4] R. Chau, J. Kavalieros, B. Roberds, R. Schenker, D. Lionberger, D. Barlarge, B. Doyle, R. Arghavani, A. Murthy, and G. Dewey, *IEEE Int. Electron Devices Meet. Tech. Dig.,* pp. 45-48, 2000.

[5] International Technology Roadmap for Semiconductors, 2011 Edition, Executive Summary, 2011.

[6] B. Davari, W-H. Chang, K. E. Petrillo, C. Y. Wong, D. Moy, Y. Taur, M. R. Wordeman, J. Y-C. Sun, C. C-H. Hsu, M. R. Polcaria, "A high-performance 0.25-μm CMOS technology: II. Technology," *IEEE Trans. Electron Devices,* vol. 39, no. 4, pp. 967-975, 1992.

[7] T. Hori, "1/4-μm LATID (Large-Tilt-angle Implanted Drain) technology for 3.3-V operation," *IEEE Int.Electron Devices Meet. Tech. Dig.,* pp. 777-780, 1989.

[8] J. W. Chou, C. Y. Chang, K. Joe, "A new surface counter doped LDD (SCD-LDD) structure for deep submicron (0.35 mu m) MOSFETs," *Symp. on VLSI Technology,* pp. 178-181, 1993.

[9] G. G. Shahidi, "A high performance 0.15 μm CMOS," *Symp. on VLSI Technology,* pp. 93-94, 1993.

[10] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. C. Johnson, Kenyon, J. Klaus, B. K. McIntyre, Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, M. Bohr, "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors," *IEEE Int.Electron Devices Meet. Tech. Dig.,* pp. 11.6.1-3, 2003.

[11] S. Thompson, N. Anand, M. Armstrong, C. Auth, B. Arcot, M. Alavi, P. Bai, J. Bielefeld,R. Bigwood, J. Brandenburg, M. Buehler, S. Cea, V. Chikarmane,

C. Choi, R. Frankovic, T. Ghani, G. Glass, W. Han, T. Hoffmann, M. Hussein, P. Jacob, A. Jain et al., "A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low *κ* ILD, and 1 µm2 SRAM cell," *IEEE Int.Electron Devices Meet. Tech. Dig.*, pp. 61-64, 2002.

[12] E. H. Nicollian, and J. R. Brews, MOS ( Metal Oxide Semiconductor) Physics and Technology, New York: John Wiley & Sons, 1982.

[13] R. M. Wallace and G. Wilk, "High-κ gate dielectric materials," *MRS Bull.*, vol. 27, pp. 192-197, 2002.

[14] D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, "The electronic structure at the atomic scale of ultrathin gate oxide," *Nature,* vol. 399, pp. 758-761, 1999.

[15] X. Gou and T. P. Ma, "Tunneling leakage current in oxynitride: dependence on oxygen/nitrogen content," *IEEE Electron Device Letters*, vol. 19, pp. 207-209, 1998.

[16] G. Timp, A. Agarwal, F. H. Baumann, T. Boone, M. Buonanno, R. Cirelli, V. Donnelly, M. Foad, D. Grant, M. Green. H. Gossmann, S. Hillenius, J. Jackson, D. Jacobson, R. Kleiman, A. Kornblit, F. Klemens, J.T-C Lee, W. Mansfield. S. Moccio. A. Murrell, M. O'Malley, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, W.W. Tai, D. Tennant, H. Vuong, B. Weir, "Low leakage, ultra-thin gate oxides for extremely high performance sub-100nm nMOSFETs," *IEEE Int.Electron Devices Meet. Tech. Dig.*, pp. 930-932, 1997.

[17] G. Timp, K. K. Bourdelle, J. E. Bower, F. H. Baumann, T. Boone, R. Cirelli, K. Evans-Lutterodt, J. Garno, A. Ghetti, H. Gossmann, M. L. Green, D. Jacobson, Y. Kim, R. Kleiman, F. Klemens, A. Kornlit, C. Lochstampfor, W. Mansfield. S. Moccio.D. A. Muller, I. E. Ocola, M.I. O'Malley, J. Rosamilia, J. Sapjeta, P. Silverman. T. Sorsch, D.M. Tennant. W. Timp, B.E. Weir, "Progress toward 10nm CMOS Devices," *IEEE Int. Electron Devices Meet. Tech. Dig.*, pp. 615-618, 1998.

[18] B. E. Weir, P. J. Silverman, M. A. Alam, F. Baumann, D. Monroe, A. Ghetti, J. D. Bude, G. L. Timp, A. Hamad, T. M. Oberdick, N. X. Zhao, Y. Ma, M. M. Brown, D.Hwang, T. W. Sorsch, J. Madic, "Gate oxides in 50nm devices: thickness uniformity improves projected reliability," *IEEE Int. Electron Devices Meet. Tech. Dig.*, pp. 437-440, 1999.

[19] R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, and H. E. Maes, "A consistent model for the thickness dependence of intrinsic breakdown in ultra-thin oxides," *IEEE Int. Electron Devices Meet. Tech. Dig.*, pp. 863-866, 1995.

[20] D. Buchanan, "Scaling the gate dielectric: Materials integration, and reliability," *IBM J. Res. Develop.*, vol. 43, pp. 245-264, 1999.

[21] G. D. Wilk, R. M. Wallace and J. M. Anthony, "Hafnium and zirconium silicates for advanced gate dielectrics," *J. Appl. Phys.* , vol. 87, pp. 484-492, 2000.

[22] G. D. Wilk, R. M. Wallace and J. M. Anthony, "High-$\kappa$ gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, pp. 5243-5275, 2001.

[23] M. T. Bohr, R. S. Chau, T. Ghani, and K. Mistry, "The high-$\kappa$ solution," *IEEE Spectrum*, vol. 44, pp. 29-35, 2007.

[24] "Introduction to Intel's 32nm Process Technology," www.intel.com.

[25] K. Tomida, K. Kita, and A. Toriumi, "Dielectric constant enhancement due to Si incorporation into $HfO_2$," *Appl. Phys. Lett*, vol. 89, no. 1, pp. 142902-1-3, 2006.

[26] T. S. Böscke, S. Govindarajan, C. Fachmann, J. Heitmann, A. Avellán, U.Schröder, S. Kudelka, P. D. Kirsch, C. Krug, P. Y. Hung, S. C. Song, B. S. Ju, J. Price, G. Pant, B. E. Gnade, W. Krautschneider, B-E Gnade, W. Krautschneider, B-H. Lee, and R. Jammy, "Tetragonal phase stabilization by doping as an enabler of thermally stable $HfO_2$ based MIM and MIS capacitors for sub 50nm Deep Trench DRAM," *Proceedings of the IEDM,*, pp. 1-4, 2006.

[27] S. Migita, Y. Watanabe, H. Ota, H. Ito, Y. Kamimuta, T. Nabatame, and A. Toriumi, "Design and demonstration of very high-$\kappa$ ($\kappa$ ~50) $HfO_2$ for ultra-scaled Si CMOS," *Symp. on VLSI Technology*, pp. 152-153, 2008.

[28] R. Essary, K. Ramani, V. Craciun, and R. K. Singh, "Improvement in electrical properties and thermal stability of low temperature- processed Hf–Al–O gate dielectrics," *Appl. Phys. Lett.*, vol. 88, pp. 180902-1-3, 2006.

[29] J. L. Roberts, P. A. Marshall, A. C. Jones, P. R. Chalker, J. F. Bickley, P. A. Williams, S. Taylor, L. M. Smith, G. W. Critchlow, M. Schumacher and J. Lindner, "Deposition of hafnium silicate films by liquid injection MOCVD using a single source or dual source approach, " *J. Mater. Chem.*, cilt 14, pp. 391-395, 2004.

[30] L. Wang, P. K. Chu, K. Xue, and J. B. Xu, "In situ characterization of initial growth of HfO2," *Appl. Phys. Lett.*, vol. 94, pp. 032904-1-3, 2009.

[31] D. G. Schlom, S. Guha and S. Datta, "Gate oxides beyond $SiO_2$," *MRS Bulletin*, vol. 33, pp. 1-9, 2008.

[32] J. M. J. Lopes, M. Roeckerath, T. Heeg, E. Rije, J. Schubert, S. Mantl, V. V. Afanasev, S. Shamuilia, A. Stesmans, Y. Jia, and D. G. Schlom, "Amorphous

lanthanum lutetium oxide thin films as an alternative high-$\kappa$ gate dielectric," *Appl. Phys. Lett,* vol. 89, pp. 222902-1-3, 2006.

[33] L. F. Edge, D. G. Schlom, S. Rivillon, Y. J. Chabal, M. P. Agustin, S. Stemmer, T. Lee, M. J. Kim, H. S. Craft, J.-P. Maria, M. E. Hawley, B. Holländer, J. Schubert, and K. Eisenbeiser, "Thermal stability of amorphous $LaScO_3$ films on silicon," *Appl. Phys. Lett.,* vol. 89, pp. 062902-1-3, 2006.

[34] M. Roeckerath, J. M. J. Lopes, E. Durğun Özben, C. Urban, J. Schubert and S. Mantl, "Investigation of terbium scandate as an alternative gate dielectric in fully depleted transistors," *Appl. Phys. Lett,* vol. 96, pp. 013513-1-3, 2010.

[35] M. V. Fischetti, D. A. Neumayer and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal–oxide-semiconductor systems with a high-$\kappa$ insulator: The role of remote phonon scattering," *J. Appl. Phys.,* vol. 90, pp. 4587-4608, 2001.

[36] K. Tatsumura, M. Goto, S. Kawanaka, K. Nakajima, T. Schimizu, T. Ishihara, and M. Koyama, "Clarification of additional mobility components associated with TaC and TiN metal gates in scaled HfSiON MOSFETs down to sub-1.0 nm EOT," *IEEE Int. Electron Devices Meet. Tech. Dig.,* pp. 439-452, 2007.

[37] D. Park, Q. Lu, T-J. King, C. Hu, A. Kalnitsky, S-P. Tay and C-C. Cheng, "SiON/$Ta_2O_5$/TiN Gate-Stack transistor with 1.8nm equivalent $SiO_2$ thickness," *IEEE. Int. Electron Devices Meet. Tech. Dig.,* pp. 381-384, 1998.

[38] V. Barral, T. Poiroux, F. Andrieu, C. Buj-Dufournet, O. Faynot and T. Ernst, "Strained FDSOI CMOS technology scalability down to 2.5 nm film thickness and 18 nm gate length with a TiN/$HfO_2$ gate stack," in *IEEE. Int. Electron Devices Meet.,* Washington, DC, 2007.

[39] M. Roeckerath, J. M. J. Lopes, E. Durğun Özben, C. Sandow , S. Lenk, T. Heeg, J. Schubert, S. Mantl, "Gadolinium scandate as an alternative gate dielectric in field effect transistors on conventional and strained silicon," *Appl. Phys. A,* vol. 94, pp. 521-524, 2009.

[40] S. M. Sze and Kwok K. Ng, Physics of semiconductor devices, Hoboken, New Jersey: John Wiley & Sons, , 2007.

[41] D. K. Schroder, Semiconductor material and device characterization, Hoboken, New Jersey: John Wiley & Sons, 2006.

[42] J. P. Wienke, The impact of interface states on sub-threshold leakage and power menagement in CMOS devices and curcuits, ProQuest, 2008.

[43] S. Guha and V. Narayanan, "High-$\kappa$ / Metal gate science and technology," *Annu. Rev. Mater. Res.,* pp. 181-202, 2009.

[44] E. H. Nicollian and A. Goetzberger, "The Si-$SiO_2$ interface-electrical properties as determined by the metal-insulator-silicon conductance technique," *The Bell system technical journal,* vol. XLVI, pp. 1055-1134, 1967.

[45] E. Cartier, F. R. McFeely, V. Narayanan, P. Jamison, B. P. Linder, M. Copel, V. K. Paruchuri, V. S. Basker, R. Haight, D. Lim, R. Carruthers, T. Shaw, M. Steen, J. Sleight, J. Rubino, H. Deligianni, S. Guha, R. Jammy, G. Shahidi, "Role of oxygen vacancies in VFB/Vt stability of pFET metals on $HfO_2$," *Symp. on VLSI. Tech. Diegest.,* pp. 230-231, 2005.

[46] M. Tapajna, K. Husekova, D. Machajdık, A. P. Kobzev, T. Schram, R. Lupták, L. Harmatha, and K. Frohlich, "Electrical properties and thermal stability of MOCVD grown Ru gate electrodes for advanced CMOS technology," *Microelectron. Eng,* vol. 83, pp. 2412-2416, 2006.

[47] M. S. Lundstrom, J. Guo, Nanoscale Transistors- Device physics, modeling and simulation, New York: Springer Science+Business Media, 2006.

[48] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electronics Letters,* vol. 24, no. 9, pp. 543-545, 1988.

[49] K. Romanjek, F. Andrieu, T. Ernst, G. Ghibaudo, "Characterization of the effective mobility by split C(V) technique in sub 0.1 µm Si and SiGe PMOSFETs," *Solid-State Electronics,* vol. 49, pp. 721-726, 2005.

[50] T-C. Ong, P-K. Ko, C. Hu, "50-A gate-oxide MOSFET's at 77 K," *IEEE Trans. Electron Devices,* vol. 34, no. 10, pp. 2129-2135, 1987.

[51] M. L. Green, E. P. Gusev, R. Degraeve, E. L. Garfunkel, "Ultrathin (<4 nm) $SiO_2$ and Si–O–N gate dielectric layers for silicon microelectronics: Understanding the processing, structure, and physical and electrical limits," *Appl. Phys. Rev.,* vol. 90, pp. 2057-2121, 2001.

[52] J. Robertson, "High dielectric constant gate oxides for metal oxide silicon transistors," *Rep. Prog. Phys.,* vol. 69, pp. 327-396, 2006.

[53] M. Wagner, T. Heeg, J. Schubert, St. Lenk, S. Mantl, C. Zhao, M. Caymax, S. De Gendt, , "Gadolinium scandate thin films as an alternative gate dielectric prepared by electron beam evaporation," *Appl. Phys. Let.,* vol. 88, pp. 172901-3, 2006.

[54] J. Robertson, "Maximizing performance for higher K gate dielectrics," *J. Appl. Phys.,* vol. 104, pp. 12411-1-7, 2008.

[55] E. Durğun Özben, "The effect of prior nitridation process of silicon surface and different metal gates on the capacitance voltage characteristics of metal-$Ta_2O_5$-Si MOS capacitor," MSc thesis, 2007.

[56] H. M. Christen, G. E. Jellison, Jr., I. Ohkubo S. Huang, M. E. Reeves, E. Cicerrella, J. L. Freeouf, Y. Jia and D. G. Schlom , "Dielectric and optical properties of epitaxial rare-earth scandate films and their crystallization behavior," *Appl. Phys. Lett.* , vol. 88, pp. 262906-1-3, 2006.

[57] V. V. Afanas'ev, S. Shamuilia, M. Badylevich, A. Stesmans, L. F. Edge, W. Tian, D. G. Schlom, J. M. J. Lopes, M. Roeckerath, J. Schubert, "Electronic structure of silicon interfaces with amorphous and epitaxial insulating oxides: $Sc_2O_3$, $Lu_2O_3$, $LaLuO_3$," *Microelectronic Engineering* , vol. 84, pp. 2278-2281, 2007.

[58] E. P. Gusev, E. Cartier, D. A. Buchanan, M. Gribelyuk, M. Copel, H. Okorn-Schmidt , C. D'Emic, "Ultrathin high-$\kappa$ metal oxides on silicon: processing, characterization and integration issues," *Microelectronic Engineering* , vol. 59, pp. 341-349, 2001.

[59] M. M. Frank and Y.J. Chabal, "Surface and interface chemistry for gate stacks on silicon," *Springer Series in Materials Science* , vol. 106, pp. 113-168, 2009.

[60] M. M. Frank, T. Ando, K. Choi, C. Choi, J. Bruley, C. Marchiori, J. Fompeyrine, V. Narayanan, "Plenty room at the bottom: Scaling the High-$\kappa$ /Silicon interfacial layer," in *16th Workshop on Dielectrics in Microelectronics*, Bratislava, 2010.

[61] T. Ando, "Ultimate scaling of high-$\kappa$ gate dielectrics: Higher-$\kappa$ or interfacial layer scavenging?," *Materials*, vol. 5, pp. 478-500, 2012.

[62] T. Ando, M. Copel, J. Bruley, M. M. Frank, H. Watanabe and V. Narayanan, "Physical origins of mobility degradation in extremely scaled $SiO_2$/$HfO_2$ gate stacks with La and Al induced dipoles," *Appl. Phys. Lett.* , vol. 96, pp. 132904-1-3, 2010.

[63] A. Nichau, A. Schäfer, L. Knoll, S. Wirths, T. Schram, L.-Å. Ragnarsson, J. Schubert, P. Bernardy, M. Luysberg, A. Besmehn, U. Breuer, D. Buca and S. Mantl, "Reduction of silicon dioxide interfacial layer to 4.6 Å EOT by Al remote scavenging in high- $\kappa$/metal gate stacks on Si," *Microelectronic Engineering*, vol. 109, pp. 109-112, 2013.

[64] H. Wang, J-J. Wang, R. Gordon, J-S. M. Lehn, H. Li, D. H, and D. V. Shenai, "Atomic layer deposition of Lanthanum-based ternary oxides," *Electrochem. Solid-State Lett.*, vol. 12, pp. G13-G-15, 2009.

[65] I. Z. Mitrovic, S. Hall, N. Sedghi, G. Simutis, V. R. Dhanak, P. Bailey, T. C. Q. Noakes, I. Alexandrou, O. Engstrom, J. M. J. Lopes, and J. Schubert, "On the nature of the interfacial layer in ultra-thin TiN/$LaLuO_3$ gate stacks," *J. Appl. Phys.*, vol. 112, pp. 044102-1-7, 2012.

[66] J. M. J. Lopes, E. Durğun Özben, M. Roeckerath, U. Littmark, R. Lupták, St. Lenk, M. Luysberg, A. Besmehn, U. Breuer, J. Schubert, and S. Mantl, "Amorphous

ternary rare-earth gate oxides for future integration in MOSFETs," *Microelectronic Engineering*, vol. 86, pp. 1646-1649, 2009.

[67] R. Lupták, J. M. J. Lopes, St. Lenk, B. Holländer, E. Durğun Özben, A. T. Tiedemann, M. Schnee, J. Schubert, and S. Mantl, "Atomic layer deposition of $HfO_2$ and $Al_2O_3$ films on 300 mm Si wafers for gate stack technology," *J. Vac. Sci. Technol. B 29*, vol. 29, pp. 01A301-1-4, 2011.

[68] J. J. Gu, Y. Q. Liu, M. Xu, G. K. Celler, R. G. Gordon, and P. D. Ye, "High performance atomic-layer-deposited $LaLuO_3$/Ge-on-insulator p-channel metal-oxide-semiconductor field-effect transistor with thermally grown $GeO_2$ as interfacial passivation layer," *Appl. Phys. Lett*, vol. 97, pp. 012106-1-3, 2010.

[69] W. Yu, E. Durğun Özben, B. Zhang, A. Nichau, J. M. J. Lopes, R. Lupták, St. Lenk, J. M. Hartmann, D. Buca, K. K. Bourdelle, J. Schubert, Q. T. Zhao, and S. Mantl, "MOSFETs with high mobility channel materials and higher-$\kappa$/metal gate stack," in *10th IEEE Int. Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Shanghai , 2010.

[70] M. L. Keith and R. Roy, "Structural relations among double oxides of trivalent elements," *Amer. Mineral.*, vol. 39, pp. 1-23, 1954.

[71] S. Geller, "Crystallografic studies of peroskite like compounds. IV. Rare earth scandates, vanidites, galliates, orthochromites," *Acta. Cryst.*, vol. 10, pp. 243-248, 1957.

[72] M. Faucher and P. Caro, "Aff inement de structure et transitions electroniques de $EuScO_3$," *Mate. Res. Bull.*, vol. 10, pp. 1-7, 1975.

[73] J. E. Greedan and K. Seto, "Preparation, cell constants, and some magnetic properties of $CsScO_3$," *Mate. Res. Bull.*, vol. 16, pp. 1479-1485, 1981.

[74] R. P. Liferovich and R. H. Mitchell, "A structural study of ternary lanthanide orthoscandate perovskites," *Journal of Solid State Chemistry* , vol. 177, pp. 2188-2197, 2004.

[75] R. Uecker, B. Velickov, D. Klimm, R. Bertram, M. Bernhagen, M. Rabe, M. Albrecht, R. Fornari, D.G. Schlom, "Properties of rare-earth scandate single crystals (Re= Nd-Dy)," *J. Cryst. Growth* , vol. 310, pp. 2649-2658, 2008.

[76] V. V. Afanas'ev, A. Stesmans, C. Zhao, M. Caymax, T. Heeg, J. Schubert, Y. Jia, D. G. Schlom, G. Lucovsky, "Band alignment between (100)Si and complex rare earth/transition metal oxides," *Appl. Phys. Lett.* , vol. 85, pp. 5917-5919, 2004.

[77] T. Heeg, M. Wagner, J. Schubert, Ch. Buchal, M. Boese, M. Luysberg, E. Cicerrella, J.L. Freeouf, "Rare-earth scandate single- and multi-layer thin films

as alternative gate oxides for microelectronic applications," *Microelectronic Engineering* , vol. 80, pp. 150-153, 2005.

[78] E. Cicerrella, J. L. Freeouf, L. F. Edge, D. G. Schlom, T. Heeg, J. Schubert, S. A. Chambers, "Optical properties of La-based high-$\kappa$ dielectric films," *J. Vac. Sci. Technol. A* , vol. 23, pp. 1676-1680, 2005.

[79] L. F. Edge, D. G. Schlom, S. Rivillon, Y. J. Chabal, M. P. Agustin, S. Stemmer, T. Lee, M. J. Kim, H. S. Craft, J.-P. Maria, M. E. Hawley, B. Holländer, J. Schubert, K. Eisenbeiser, "Thermal stability of amorphous $LaScO_3$ films on silicon," *Appl. Phys. Lett.* , vol. 89, pp. 062902-1-3, 2006.

[80] P. Myllymäki, M. Roeckerath, M. Putkonen, S. Lenk, J. Schubert, L. Niinistö, S. Mantl, "Characterization and electrical properties of high-$\kappa$ GdScO3 thin films grown by atomic layer deposition," *Applied Physics A –Materials Science & Processing,* vol. 88, pp. 633-637, 2007.

[81] C. Zhao, T. Witters, B. Brijs, H. Bender, O. Richard, M. Caymax, T. Heeg, J. Schubert, V. V. Afanas'ev, A. Stesmans and D. G. Schlom, "Ternary rare-earth metal oxide high-$\kappa$ layers on silicon oxide," *Appl. Phys. Lett.* , vol. 86, pp. 132903-1-3, 2005.

[82] J. M. J. Lopes, M. Roeckerath, T. Heeg, U. Littmark, J. Schubert, S. Mantl, Y. Jia and D. G. Schlom, "La-based ternary rare-earth oxides as alternative high-$\kappa$ dielectrics," *Microelectronic Engineering* , vol. 84, pp. 1890-1893, 2007.

[83] J. M. J. Lopes, U. Littmark, M. Roeckerath, St. Lenk, J. Schubert, S. Mantl, A. Beshmen, "Effects of annealing on the electrical and interfacial properties of amorphous lanthanum scandate high-$\kappa$ films prepared by molecular beam deposition," *J. Appl. Phys.* , vol. 101, pp. 104109-1-5, 2007.

[84] W. Kern, "The evolution of silicon wafer cleaning technology," *J. Electrochem. Soc.*, vol. 137, pp. 1887-1892, 1990.

[85] W-K. Chu, J-W. Mayer, M-A. Nicolet, Backscattering spectromety, New York: Academic Pr., 1978.

[86] M. Birkholz, Thin film analysis by X-ray scattering, Weinheim: Wiley-VCH, 2005.

[87] C. Adelmann, S. Van Elshocht, A. Franquet, T. Conard, O. Richard, H. Bender, P. Lehnen, and S. De Gendt, "Thermal stability of dysprosium scandate thin films," *Appl. Phys. Lett.*, vol. 92, p. 112902, 2008.

[88] E. P. Gusev, C. Cabral, Jr., M. Copel, C. D'Emic, and M. Gribelyuk, "Ultrathin $HfO_2$ films grown on silicon by atomic layer deposition for advanced gate dielectrics applications," *Microelectronic Engineering,* vol. 69, pp. 145-151, 2003.

[89] J. Kim and K. Yong, "Characterization of hafnium silicate thin films grown by MOCVD using a new combination of precursors," *J. Cryst. Growth,* vol. 263, pp. 442-446, 2004.

[90] A. Nichau, M. Schnee, J. Schubert, A. Besmehn, J. Rubio-Zuazo, U. Breuer, P. Bernardy, B. Holländer, A. Mücklich, G. R. Castro, J. von Borany, D. Buca and S. Mantl, "Photoemission spectroscopy study of the lanthanum lutetium oxide/silicon interface," *J. Chem. Phys.* , vol. 138, pp. 154709-1-9, 2013.

[91] I. Z. Mitrovic, S. Hall, N. Sedghi, G. Simutis, V. R. Dhanak, P. Bailey, T. C. Q. Noakes, I. Alexandrou, O. Engstrom, J. M. J. Lopes and J. Schubert, "On the nature of the interfacial layer in ultra-thin TiN/$LaLuO_3$ gate stacks," *J. Appl. Phys.,* vol. 112, pp. 044102-1-8, 2012.

[92] O. Renault, D. Samour, J.-F. Damlencourt, D. Blin, F. Martin, S. Marthon, N. T. Barrett, P. Besson, "$HfO_2$/$SiO_2$ interface chemistry studied by synchrotron radiation x-ray photoelectron spectroscopy," *Appl. Phys. Lett.,* vol. 81, pp. 3627-3629, 2002.

[93] T. L. Duan, H. Y. Yu, L. Wu, Z. R. Wang, Y. L. Foo and J. S. Pan, "Investigation of HfO2 high-κ dielectrics electronic structure on $SiO_2$/Si substrate by x-ray photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 99, pp. 012902-1-3, 2011.

[94] S. J. Wang, P . C. Lim, A. C. H. Huan, C. L. Liu, J. W. Chai, S. Y. Chow, J. S. Pan, Q. Li and C. K. Ong, "Reaction of $SiO_2$ with hafnium oxide in low oxygen pressure," *Appl. Phys. Lett.*, vol. 82, pp. 2047-2049, 2003.

[95] A. Besmehn, A. Scholl, E. Rije, U. Breuer, "Surface characterisation and interface studies of high-$\kappa$ materials by XPS and TOF-SIMS," *Appl. Surface Science,* vol. 252, pp. 172-176, 2005.

[96] K. Fröhlich, K. Hušeková, D. Machajdik, J.C. Hooker, N. Perez, M. Fanciulli, S. Ferrari, C. Wiemer, A. Dimoulas, G. Vellianitis, F. Roozeboom, "Ru and $RuO_2$ gate electrodes for advanced CMOS technology," *Materials Science and Engineering B* , vol. 109, pp. 117-121, 2004.

[97] A. Vincze, R. Lupták, K. Hušeková, E. Dobročká, K. Fröhlich, "Thermal stability of $GdScO_3$ and $LaLuO_3$ films prepared by liquid injection MOCVD," *Vacuum 84* , vol. 84, pp. 170-173, 2010.

[98] H. Ono and T. Katsumata, "Interfacial reactions between thin rare-earth-metal oxide films and Si substrates," *Appl. Phys. Lett.,* vol. 78, pp. 1832-1834, 2001.

[99] K. Maitra, M. M. Frank, V. Narayanan, V. Misra, E. A. Cartier, "Impact of metal gates on remote phonon scattering in titanium nitride/hafnium dioxide n-channel

metal–oxide–semiconductor field effect transistors–low temperature electron mobility study," *J. Appl. Phys.*, vol. 102, pp. 114507-1-5, 2007.

[100] M. Copel, N. Bojarczuk, L. F. Edge, and S. Guha, "Stability of terbium scandate on Si(100)," *Appl. Phys. Lett.*, vol. 97, pp. 182901-1-3, 2010.

[101] X. B. Lu, H. B. Lu, J. Y. Dai, Z. H. Chen, M. He, G. Z. Yang, H. L.W. Chan, C. L. Choy, "Oxygen pressure dependence of physical and electrical properties of $LaAlO_3$ gate dielectric," *Microelectronic Engineering*, vol. 77, pp. 399-404, 2005.

[102] S. Guha and V. Narayanan, "Oxygen vacancies in high dielectric constant oxide-semiconductor films," *Physical Review Letters*, vol. 98, pp. 196101-1-4, 2007.

[103] S. H. Bae, C. H. Lee, R. Clark, and D. L. Kwong, "MOS characteristics of ultrathin CVD HfAlO gate dielectrics," *IEEE Electron Device Letters*, vol. 24, pp. 556-558, 2003.

[104] A. Chatterjee, R. A. Chapman, G. Dixit, J. Kuehne, S. Hattangady, H. Yang, G. A. Brown, R. Aggarwal, U. Erdogan, Q. He, M. Hanratty, D. Rogers, S. Murtaza, S. J. Fang, R. Kraft, A. L. P. Rotondaro, J. C. Hu, M. Terry, W. Lee, C. Fernando, A. Konecni, G. Wells , "Sub-100nm Gate length metal gate NMOS transistors fabricated by a replacement gate process," in *IEEE Int. Electron Devices Meet. Tech. Dig.*, Washington, DC, 1997.

[105] S-H. Bae, S-C. Song, K. Choi, G. Bersuker, G. A. Brown, D-L. Kwong, B. H. Lee, "Thickness optimization of the TiN metal gate with polysilicon-capping layer on Hf-based high-$\kappa$ dielectric," *Microelectronic Engineering* , vol. 83, pp. 460-462, 2006.

[106] G. Reimbold, X. Garros, M. Cassé, C. Leroux, F. Martin, and F. Boulanger, "On the key role of nitrogen on reliability and performances of advanced High-$\kappa$ /Metal gate stacks," in *Int. Symposium on Integrated Functionalities ISIF* , San Juan, Puerto Rico., 2010.

[107] G. Hyvert, T. Nguyen, L. Militaru, A. Poncet, C. Plossu, "A study on mobility degradation in nMOSFETs with $HfO_2$ based gate oxide," *Materials Science and Engineering B* , vol. 165, pp. 129-131, 2009.

[108] J. H. Sim, S. C. Song, P. D. Kirsch, C. D. Young, R. Choi, D. L. Kwong, B. H. Lee and G. Bersuker, "Effects of ALD $HfO_2$ thickness on charge trapping and mobility," *Microelectronic Engineering* , vol. 80, pp. 218-221, 2005.

[109] J. Widiez, M. Vinet, B. Guillaumot, T. Poiroux, D. Lafond, P. Holliger, O. Weber, V. Barral, B. Previtali, F. Martin, M. Mouis and S. Deleonibus, "Fully depleted SOI MOSFETs with $WSi_x$, metal gate on $HfO_2$ gate dielectric," in *IEEE Int. SOI Conference*, Niagara Falls, NY, 2006.

[110] J-S. Lim, S. E. Thompson and J. G. Fossum, "Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs," *IEEE Electron Device Letters,* vol. 25, pp. 731-733, 2004.

[111] Y-S. Choi, T. Numata, T. Nishida, R. Harris and S. E. Thompson, "Impact of mechanical stress on gate tunneling currents of germanium and silicon p-type metal-oxide-semiconductor field-effect transistors and metal gate work function," *J. Appl. Phys.* , vol. 103, pp. 064510-1-5, 2008.

[112] F. Andrieu, C. Dupré, F. Rochette, O. Faynot, L. Tosti, C. Buj, E. Rouchouze, M. Cassé, B. Ghyselen, I. Cayrefourcq, L. Brévard, F. Allain, J. C. Barbé, J. Cluzel, A. Vandooren, S. Denorme, T. Ernst, C. Fenouillet-Béranger, C. Jahan, D. Lafond, H. Dansas, B. Previtali, J.P. Colonna, H. Grampeix, P. Gaud, C. Mazuré and S. Deleonibus, "25 nm Short and Narrow Strained FDSOI with TiN/$HfO_2$ Gate Stack," in *IEEE Symposium on VLSI Tech. Dig. of Tech. Papers,* Honolulu, HI , 2006.

[113] I. Lauer, T. A. Langdo, Z-Y. Cheng, J. G. Fiorenza, G. Braithwaite, M. T. Currie, C. W. Leitz, A. Lochtefeld, H. Badawi, M. T. Bulsara, M. Somerville, and D. A. Antoniadis, "Fully depleted n-MOSFETs on supercritical thickness strained SOI," *IEEE Electron Device Letters,* vol. 25, pp. 83-85, 2004.

[114] C. Z. Zhao, M. B. Zahid, J. F. Zhang, G. Groeseneken, R. Degraeve, and S. De Gendt, "Threshold voltage instability of p-channel metal-oxide-semiconductor field effect transistors with hafnium based dielectrics," *Appl. Phys. Lett.,* vol. 90, pp. 143502-1-3, 2007.

[115] T. K. Chiang, Y. H. Wang, M. P. Houng, "Modeling of threshold voltage and subthreshold swing of short-channel SOI MESFET's," *Solid-State Electronics,* vol. 43, pp. 123-129, 1999.

[116] L. Trojman, L. Pantisano, S. Severi, E. San Andres, T. Hoffman, I. Ferain, S. De Gendt, M. Heyns, H. Maes, and G. Groeseneken, "Performance assessment of (110) p-FET high-$\kappa$ /MG: is it mobility or series resistance limited," *Microelectronic Engineering* , vol. 84, pp. 2058-2062, 2007.

[117] E. O. Kane, "Theory of tunneling," *J. App. Phys.,* vol. 32, pp. 83-91, 1961.

[118] J. Chen, T. Y. Chan, I. C. Chen and C. Hu, "Subbreakdown drain leakage current in MOSFET," *IEEE Elecron Device Letters,* Vols. EDL-8, pp. 515-517, 1987.

[119] M. V. Dunga, A. Kumar and V. R. Rao, "Analysis of floating body effects in thin film SOI MOSFETs using the GIDL current technique," in *IEEE, 8th Int. Symposium on Physical and Failure Analysis of Integrated Circuits, IPFA,* 2001.

[120] L. Huang, P. T. Lai , J. P. Xu, Y. C. Cheng, "Mechanism analysis of gate-induced drain leakage in off-state n-MOSFET," *Microelectronics Reliability,* vol. 38, pp. 1425-1431, 1998.

[121] O. Semenov, A. Pradzynski, and M. Sachdev, "Impact of gate induced drain leakage on overall leakage of submicrometer CMOS VLSI circuits," *IEEE Transactions on semiconductor manufacturing,* vol. 15, pp. 9-18, 2002.

[122] L. Lopez, P. Masson, D. Nee, R. Bouchakour, "Temperature and drain voltage dependence of gate-induced drain leakage," *Microelectronic Engineering,* vol. 72, pp. 101-105, 2004.

[123] S. F. Feste, Th. Schäpers, D. Buca, Q. T. Zhao, J. Knoch, M. Bouhassoune, Arno Schindlmayr and S. Mantl, "Measurement of effective electron mass in biaxial tensile strained silicon on insulator," *Appl. Phys. Lett.,* vol. 95, pp. 182101-1-3, 2009.

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# List of Publications

[1] A. Nichau, E. Durğun Özben, M. Schnee, J. M. J. Lopes, A. Besmehn, M. Luysberg, L. Knoll, S. Habicht, V. Mussmann, R. Lupták, St. Lenk, J. Rubio-Zuazo, G. R. Castro, D. Buca, Q. T. Zhao, J. Schubert and S. Mantl, "$LaLuO_3$ higher-$\kappa$ dielectric integration in SOI MOSFETs with gate-first process" *Solid States Elect.* 71 (2012), 19-24. doi:10.1016/j.sse.2011.10.014

[2] E. Durğun Özben, M. Schnee, A. Nichau, V. Mussmann, R. Lupták, J. M. J. Lopes, St. Lenk, K. K. Bourdelle, Q. T. Zhao, J. Schubert, S. Mantl, "$LaScO_3$ as a higher-κ dielectric for p-MOSFETs", *Microelectronic Engineering* 88 (2011), 1323. doi:10.1016/j.mee.2011.03.048

[3] R. A. Minamisawa, M. Schmidt, E. Durğun Özben, J. M. J. Lopes, J. M. Hartmann, K. K. Bourdelle, J. Schubert, Q. T. Zhao, D. Buca, S. Mantl, "High mobility strained $Si_{0.5}Ge_{0.5}$/SSOI short channel field effect transistors with TiN/$GdScO_3$ gate stack", *Microelectronic Engineering* 88 (2011), 2955. doi:10.1016/j.mee.2011.04.030

[4] E. Durğun Özben, J. M. J. Lopes, A. Nichau, R. Lupták, S. Lenk, A. Besmehn, K. K. Bourdelle, Q. T. Zhao, J. Schubert, and S. Mantl, "Rare-Earth scandate/TiN gate stacks in SOI MOSFETs fabricated with a full replacement gate process", *IEEE Trans.on Elect. Devices* 58(3) (2011), 617. doi:10.1109/TED.2010.2096509

[5] A. Nichau, E. Durğun Özben, M. Schnee, J. M. J. Lopes, A. Besmehn, M. Luysberg, L. Knoll, S. Habicht, V. Mussmann, R. Lupták, St. Lenk, J. Rubio-Zuazo, G. R. Castro, D. Buca, Q. T. Zhao, J. Schubert and S. Mantl, " Lanthanum Lutetium oxide integration in a gate-first process on SOI MOSFETs", *Proceedings of the 12th International Conference on Ultimate Integration on Silicon (12th ULIS),* Pages:1-4 (2011). doi:10.1109/ULIS.2011.5757952

[6] E. Durğun Özben, J. M. J. Lopes, A. Nichau, M. Schnee, S. Lenk, A. Besmehn, K. K. Bourdelle, Q. T. Zhao, J. Schubert, and S. Mantl, "Integration of $LaLuO_3$ ($\kappa \sim 30$) as high-$\kappa$ dielectric on strained and unstrained SOI MOSFETs with a replacement gate process", *IEEE Electron Dev. Lett.* 32 (1) (2011), 15. doi:10.1109/LED.2010.2089423

[7] E. Durğun Özben, J. M. J. Lopes, A. Nichau, R. Lupták, S. Lenk, A. Besmehn, K. K. Bourdelle, Q. T. Zhao, J. Schubert, and S. Mantl, "Rare-earth oxide/TiN gate stacks on high mobility strained silicon on insulator for fully depleted metal-oxide-semiconductor fieldeffect transistors", *Journal of Vac. Sci. Technol. B* 29 (2011), 01A903. doi:10.1116/1.3533760

[8] R. Lupták, J. M. J. Lopes, St. Lenk, B. Holländer, E. Durğun Özben, A. T. Tiedemann, M. Schnee, J. Schubert, S. Habicht, S. Feste, S. Mantl, U. Breuer, A. Besmehn, P. K. Baumann, and M. Heuken, "Atomic layer deposition of $HfO_2$ and $Al_2O_3$ layers on 300 mm Si wafers for gate stack technology", *Journal of Vac. Sci. Technol. B* 29 (2011), 01A301. doi:10.1116/1.3521374

[9] J. M. J. Lopes, E. Durğun Özben, M. Schnee, R. Lupták, A. Nichau, A. Tiedemann, W. Yu, Q. T. Zhao, A. Besmehn, U. Breuer, M. Luysberg, St. Lenk, J. Schubert, and S. Mantl, "Electrical and structural properties of ternary rare-earth oxides on Si and higher mobility substrates and their integration as high-$\kappa$ gate dielectrics in MOSFET devices", *Electrochem. Soc. Trans*. 35 (2011), 461. doi:10.1149/1.3572299

[10] C. Radtke, C. Krug, G. V. Soares, I. J. R. Baumvol, J. M. J. Lopes, E. Durğun Özben, A. Nichau, J. Schubert, and S. Mantl, "Physicochemical and electrical properties of $LaLuO_3$/Ge(100) structures submitted to postdeposition annealings", *Electrochem. Solid-State Lett.* 13, G37 (2010), doi:10.1149/1.3322517

[11] M. Roeckerath, J. M. J. Lopes, E. Durğun Özben, C. Urban, J. Schubert, S. Mantl, Y. Jia, and D. G. Schlom, "Investigation of terbium scandate as an alternative gate dielectric in fully depleted transistors", *Applied Physics Letters* 96 (2010), 013513. doi: 10.1063/1.3275731

[12] E. Durğun Özben, A. Nichau, J. M. J. Lopes, St. Lenk, A. Besmehn, K. K. Bourdelle, Q. T. Zhao, J. Schubert, and S. Mantl, "Electrical characterization of $TbScO_3$/TiN gate stacks in MOS capacitors and MOSFETs on strained and unstrained SOI", *Electrochem. Soc. Trans*. 33 (2010), 195. doi:10.1149/1.3481606

[13] J. M. J.Lopes, E. Durgun Özben, M. Roeckerath, U. Littmark, R. Lupták, St. Lenk, M. Luysberg, A. Besmehn, U. Breuer, J. Schubert, and S. Mantl, "Amorphous ternary rare-earth gate oxides for future integration in MOSFETs", *Microelectronic Engineering* 86 (2009), 1646. doi: 10.1016/j.mee.2009.03.065

[14] J. M. J. Lopes, U. Littmark, M. Roeckerath, E. Durğun Özben, S. Lenk, U. Breuer, A. Besmehn, A. Stärk, P.L. Grande, M.A. Sortica, C. Radtke, J. Schubert, S. Mantl, "Isotopic labeling study of oxygen diffusion in amorphous $LaScO_3$ high-$\kappa$ films on Si(100) and its effects on the electrical characteristics", *Applied Physics A-Materials Science & Processing* 96 (2) (2009), 447. doi: 10.1007/s00339-009-5153-y

[15] M. Roeckerath, J. M. J. Lopes, E. Durgun Özben, C. Sandow, S. Lenk, T. Heeg, J. Schubert, S. Mantl, "Gadolinium scandate as an alternative gate dielectric in field effect transistors on conventional and strained silicon", *Applied Physics A-Materials Science & Processing* 94 (2009), 521. doi: 10.1007/s00339-008-4962-8

[16] E. Durğun Özben, J. M. J. Lopes, M. Roeckerath, St. Lenk, B. Holländer, Y. Jia, D. G. Schlom, J. Schubert, S. Mantl, "$SmScO_3$ thin films as an alternative gate dielectric", *Applied Physics Letters* 93 (2008), 052902. doi: 10.1063/1.2968660

# Conference Cotributions


[1] R. A. Minamisawa, J. M. J. Lopes, M. Schmidt, E. Durğun Özben, J. M. Hartmann, D. Buca, J. Schubert, Q. T. Zhao, and S. Mantl, " TiN/$GdScO_3$/strained $Si_{0.5}Ge_{0.5}$/SSOI stack for high mobility short channel *p*-MOSFETs", EUROSOI 2011, Granada, Spain.

[2] A. Nichau, E. Durğun Özben, M. Schnee, J. M. J. Lopes, A. Besmehn, M. Luysberg, L. Knoll, S. Habicht, V. Mussmann, R. Luptak, St. Lenk, J. Rubio-Zuazo, G. R. Castro, D. Buca, Q. T. Zhao, J. Schubert and S. Mantl, " Lanthanum Lutetium oxide integration in a gate-first process on SOI MOSFETs", *12th International Conference on Ultimate Integration on Silicon* ULIS 2011, Cork, Ireland.

[3] E. Durğun Özben, M. Schnee, A. Nichau, V. Mussmann, R. Lupták, J. M. J. Lopes, St. Lenk, K. K. Bourdelle, Q. T. Zhao, J. Schubert, S. Mant, "$LaScO_3$ as a higher-$\kappa$ dielectric for p-MOSFETs", *17th biannual conference of Insulating Films on Semiconductors* INFOS 2011, Grenoble, France.

[4] W. Yu, E. Durğun Özben, B. Zhang, A. Nichau, J. M. J. Lopes, R. Lupták, St. Lenk, J. M. Hartmann, D. Buca, K. K. Bourdelle, J. Schubert, Q. T. Zhao, and S. Mantl, "MOSFETs with high mobility channel materials and higher-$\kappa$/metal gate stack", *Solid-State and Integrated Circuit Technology (*ICSICT), IEEE conference (2010), 875. doi:10.1109/ICSICT.2010.5667458

[5] J. M. J. Lopes , E. Durğun-Özben, R. Luptak, R. A. Minamisawa, S. Feste, D. Buca, J. Schubert, Q. T. Zhao, B. Holländer, A. Tiedemann, J. M. Hartmann, K. Bourdelle, N. Kernevez, P. Baumann, M. Heuken and S. Mantl, "Ternary high-$\kappa$ oxides for nanoscale logic devices" *International Symposium on Integrated Functionalities* ISIF 2010, San Juan, Puerto Rico.

[6] W. Yu, B. Zhang, Q. T. Zhao, J.-M. Hartmann, D. Buca, A. Nichau, E. Durğun Özben, J. M. J. Lopes, J. Schubert, B. Ghyselen and S. Mantl, "Strained-SiGe p-MOSFET with $LaLuO_3$ as high-$\kappa$ gate dielectric and TiN as metal gate", EUROSOI 2010, Grenoble, France.

[7] W. Yu, B. Zhang, E. Durğun Özben, R. A. Minamisawa, R. Luptak, M. Hagedorn, B. Holländer, J. Schubert, J. M. Hartmann, K. K. Bourdelle, Q. T. Zhao, D. Buca, S. Mantl, "High mobility Si-Ge channels and novel high-k materials for nano-MOSFETs", *33rd International Semiconductor Conference* CAS 2010. Sinaia, Romania.

[8] E. Durğun Özben, A. Nichau, J. M. J. Lopes, St. Lenk, A. Besmehn, K. K. Bourdelle, Q. T. Zhao, J. Schubert, and S. Mantl, "Electrical characterization

of $TbScO_3$/TiN gate stacks in MOS capacitors and MOSFETs on strained and unstrained SOI", *218$^{th}$ Electrochemical Society meeting* ECS 2010, Las Vegas, NV, USA.

[9] E. Durğun Özben, J. M. J. Lopes, A. Nichau, R. Lupták, S. Lenk, A. Besmehn, K. K. Bourdelle, Q. T. Zhao, J. Schubert, and S. Mantl, "Rare-earth oxide/TiN gate stacks on high mobility strained silicon on insulator for fully depleted metal-oxide-semiconductor fieldeffect transistors", *16$^{th}$ Workshop on Dielectrics in Microelectronics* WODIM 2010, Bratislava, Slovakia

[10] R. Lupták, J. M. J. Lopes, St. Lenk, B. Holländer, E. Durğun Özben, A. T. Tiedemann, M. Schnee, J. Schubert, S. Habicht, S. Feste, S. Mantl, U. Breuer, A. Besmehn, P. K. Baumann, and M. Heuken, "Atomic layer deposition of $HfO_2$ and $Al_2O_3$ layers on 300 mm Si wafers for gate stack technology", *16$^{th}$ Workshop on Dielectrics in Microelectronics* WODIM 2010, Bratislava, Slovakia

[11] E. Durğun Özben, J. M. J. Lopes, M. Roeckerath, A. Nichau, R. Luptak, St. Lenk, A. Besmehn, B. Ghyselen, Q. T. Zhao, J. Schubert, S. Mantl, "High mobility strained SOI MOSFETs with $LaScO_3$/TiN gate stacks fabricated with a replacement gate process", *11$^{th}$ International Conference on Ultimate Integration on Silicon* ULIS 2010, Glasgow, Scotland.

[12] E. Durğun Özben, J. M. J. Lopes, A. Nichau, R. Luptak, M. Roeckerath, S. Lenk, A. Besmehn, B. Ghyselen, Q. T. Zhao, J. Schubert and S. Mantl, "Rare-earth scandates/TiN gate stack on high mobility strained SOI for fully depleted (FD) MOSFETs" *Electronic Materials Conference* EMC 2010, Notre Dame, Indiana, USA.

[13] J. M. J. Lopes, M. Roeckerath, U. Littmark, E. Durgun Özben, U. Breuer, A. Besmehn, J.M.J.Lopes, E. Durgun-Özben, M. Roeckerath, U. Littmark, R. Lupták, S. Lenk, A. Besmehn, U. Breuer, J. Schubert, and S. Mantl, "Rare-earth based alternative gate dielectrics for future integration in MOSFETs", *10$^{th}$ International Conference on Ultimate Integration on Silicon* ULIS 2009, Aachen, Germany.

[14] P. L. Grande, M. A. Sortica, C. Radtke, J. Schubert, and S. Mantl, "Isotopic labeling investigation of oxygen annealed $LaScO_3$ high-$\kappa$ films grown on Si(100) by molecular beam deposition", *Material Research Society* MRS 2009, San Francisco, USA.

[15] J. M. J. Lopes, E. Durğun Özben, M. Roeckerath, U. Littmark, R. Lupták, St. Lenk, A. Besmehn, U. Breuer, J. Schubert, and S. Mantl, "Rare-earth based alternative gate dielectrics for future integration in MOSFETs" *16th biannual conference of Insulating Films on Semiconductors* INFOS 2009, Cambridge, England.

[16] M. Roeckerath, J. M. J. Lopes, E. Durğun Özben, J. Schubert, S. Mantl, D. G. Schlom, “Terbium scandate as a higher-$\kappa$ dielectric”, *Material Research Society* MRS 2009, San Francisco, USA.

[17] J. M. J. Lopes, M. Roeckerath, E. Durğun Özben, R. Lupták, J. Schubert, and S. Mantl, “Rare-earth based alternative gate-dielectrics for future integration in MOSFETs”, *39th IEEE Semiconductor Interface Specialists Conference* SISC 2008, San Diego, USA.

[18] E. Durğun Özben, J. M. J. Lopes, M. Roeckerath, J. Schubert, St. Lenk, B. Holländer, D. G. Schlom, S. Mantl, “$SmScO_3$ thin films as an alternative gate dielectric”, *15th Workshop on Dielectrics in Microelectronics* WODIM 2008, Bad Saarow (Berlin), Germany.

[19] E. Durğun Özben, E. Atanassova, M. Güneş, “The effects of process conditions on the characteristics of metal-$Ta_2O_5$-Si MOS capacitor”, *Nanoscience & Nanotechnology TR* NanoTr 2007, Ankara, Turkey.

[20] E. Durğun Özben, E. Atanassova, M. Güneş, “The effects of device process conditions on the characteristics of metal-$Ta_2O_5$-Si MOS capacitor”, *14th International School on Condensed Matter Physics* ISCMP 2006, Varna, Bulgaria

# Curriculum Vitae

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## Education

Sep. 2003-Oct. 2007 Master of Science in Physics at İzmir Institute of Technology (IZTECH), Izmir-Turkey

Jen. 2004-Jun. 2006 Master of Science in Physics teaching at Ege University, İzmir, Turkey

Sep. 1998- Jun.2003 Bachelor of Science in Physics at 9 Eylül University, İzmir, Turkey

Sep. 1986- Jen.1997 Scholar education

## Research and professional experience

Oct. 2007- Feb. 2011 Scientific employee with Prof. Dr. S. Mantl at the Peter Grünberg Institute 9, dept. ion technology Forschungszentrum Jülich, Jülich,Germany.

Research Project: Preparation, integration and electrical investigation of rare-earth ternary oxide as alternative high-$\kappa$ gate dielectrics for future CMOS technologies

Nov. 2005-Oct. 2007 Teaching assistant with Prof. Dr. M. Güneş at IZTECH, Izmir, Turkey

Research Project: Investigation of electrical properties of $Ta_2O_5$ insulating layers in MOS capacitors and effects of prior nitridation and metal gate on the oxide and interface properties of MOS capacitors.