Building Blocks
for
Vertical GaN-based Devices

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vorgelegt von
Dipl.-Phys. Wiebke Johanne Witte
aus Aurich

Berichter: Univ.-Prof. Dr.-Ing. Andrei Vescan
Univ.-Prof. Dr. rer. nat. Joachim Knoch

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1. Introduction

The development of power electronics has been driven by two important factors in the recent years. The first factor is the increasing demand for electrical energy [1] which will further rise in the next years due to the rapidly enhanced number of electrical vehicles [2, 3]. The second factor is the increasing generation of renewable energy [4] which demands for more power conversion and switching. Today, about 10% of the generated electrical energy in the US is wasted due to losses [5]. The largest amount of power losses is thereby dissipated in semiconductor devices [6].

So far, the majority of converters and switches is based on silicon (Si) devices. In order to increase their efficiency, the requirements for power electronic devices are approaching the fundamental material limits of Si. As a result of its band gap ($E_g$) of 1.12 eV [7], Si offers only a small critical electric field ($E_{crit}$) limiting the application in high-power devices. Furthermore, the small $E_g$ results in a large intrinsic carrier concentration which will rise exponentially for higher temperatures [8]. Hence, Si-based power electronic applications should not exceed operation temperatures of 200 °C making expensive cooling efforts necessary to avoid intrinsic conduction. Also Si is limited in its switching speed, preventing the further reduction of switching losses. Consequently, the demand for wide-bandgap materials has evolved in the recent years.

Gallium nitride (GaN) has become a very promising candidate for applications in high-power devices. Compared to Si, GaN offers a large $E_g$ of 3.43 eV [7] and thus a lower intrinsic carrier concentration. Therefore, GaN-based devices can be operated at higher temperatures. This reduces cooling efforts and costs. Furthermore, GaN also possesses a much larger $E_{crit}$ than Si which enables the operation at high voltages. Because of the larger $E_{crit}$, the size of the active area can be reduced for a specific breakdown voltage ($V_{BR}$). This also results in a lower on-resistance ($R_{on}$). Additionally, the size of the packaging components is reduced which further saves costs.

The GaN material system profits in particular from the AlGaN/GaN heterostructure. A two-dimensional electron gas (2DEG) is formed at the interface of the two compounds. The 2DEG exhibits a sheet carrier concentration ($n_s$) of $10^{13}$ cm$^{-2}$ and an
electron mobility ($\mu$) of up to 2000 cm$^2$/Vs [9]. These properties allow not only for very high current densities and switching speeds, but also result in a low $R_{on}$.

Up to now, research has mainly focused on lateral GaN-based devices. A lateral heterostructure field effect transistor (HFET) with $V_{BR}$ of 1 kV and $R_{on}$ of 0.39 m$\Omega$cm$^2$ has been presented [10]. However, increasing $V_{BR}$ implies increasing the gate drain separation ($d_{GD}$), with the result of a larger chip size. Concepts to circumvent the increase of $d_{GD}$, such as different means to shape the electrical field e.g. field plates, have been applied leading to more complex processing schemes.

An elegant solution to serve the demand for high $V_{BR}$ is the use of vertical devices. Here, the drain contact is placed on the backside of the device. The separation of gate and drain contact through the devices thickness offers an enhanced $V_{BR}$ without increasing the lateral device size. The region of highest field is buried inside such a structure, which makes the device less sensitive to surface states. Therefore, complex passivation schemes are less important [11]. A further advantage of the vertical configuration is the possibility to deposit large metal backside contacts which serve as a heat sink and reduce the thermal budget. So far, the main challenge, which delays the development of vertical devices is the lack of a sufficient supply of high-quality GaN substrates. The dislocation density on foreign substrates such as sapphire, silicon carbide (SiC), and Si limits $E_{crit}$ [12].

A prominent example for the realization of vertical GaN-based devices is the current aperture vertical electron transistor (CAVET) as proposed by [13]. This device relies on the application of a current blocking layer (CBL) with an aperture. The blocking layer prohibits a short-circuit between source and drain. The aperture is placed underneath the gate and allows for a vertical current flow there.

The objective of this work is the realization of vertical GaN-based devices relying on a CAVET.

Chapter 2 comprises the fundamentals of GaN-based devices. First, the material properties of GaN, in particular polarization effects, are summarized. Next, the AlGaN/GaN heterostructure, leading to the prominent 2DEG, and the HFET are elucidated in more detail. Last, the epitaxial methods to grow GaN-based materials are explained.

Chapter 3 presents the different realizations of vertical GaN-based devices. First, the basic principle and fabrication of the elementary building blocks, such as vertical Schottky and pn diodes are introduced. Then, the more complex vertical transistors, namely the CAVET, the vertical metal oxide semiconductor field effect transistor (VMOSFET) and the vertical trench-gate approaches are presented. Since the CAVET
is the most promising candidate for vertical transistors so far, the processing of such a device will be explained in more detail.

In order to analyze the critical parameters and to deduce design rules, electrical simulations of a CAVET are performed. The results are presented in Chapter 4. First, parameters relating to the growth of the structure, such as the doping and thickness of the drift region and the channel are simulated. In the following, parameters concerning the mask layout are simulated. This comprises the overlap of the gate and the aperture, the aperture length and the geometry of the aperture itself.

The fabrication of a CAVET requires various challenging process steps. Therefore, the process of a CAVET is split into single building blocks which are considered separately from each other in Chapter 5. The building blocks are described in sequence of their occurrence in the process. Due to the use of an insulating sapphire substrate, which prohibits the contacting from the backside, in the first building block the fabrication of a quasi-vertical structure is discussed. Next, the drift region is optimized in terms of $V_{BR}$ and $R_{on}$. Subsequently, the use of a Mg-doped p-GaN layer as CBL is evaluated. The main building blocks are the regrowth on top of the CBL and the aperture. Therefore, the regrowth with metal-organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) is investigated on five different templates: an as-grown GaN surface, a dry-etched GaN surface, a p-GaN layer, a textured and a masked template.

Finally, the results of two complete realizations of a CAVET are presented in Chapter 6. Both devices rely on a MOCVD $n^+/n^-$-GaN template with p-GaN CBL and an etched aperture. For the first device, the AlGaN/GaN regrowth is performed with MOCVD, whereas for the second device MBE is used.

In summary, the challenges of fabricating vertical GaN-based devices will be identified, investigated, and partially solved.
2. Fundamentals

In this work, GaN-based heterostructures are investigated. Therefore, the purpose of the present chapter is to provide an overview over this material system. First, an introduction into the GaN crystal system is given, followed by its physical properties. Here, the advantages of GaN are highlighted with respect to Si and SiC. Next, the inherently existent polarization effects and the resulting 2DEG in a heterostructure are explained. The advantages of a 2DEG are exploited in an AlGaN/GaN HFET, which will be presented thereafter. Also, an introduction into MOCVD and MBE, the main techniques to fabricate GaN-based layer stacks, is provided. At last, the n- and p-type doping of GaN is elucidated.

2.1. Material Properties

GaN and other III-nitride compounds crystallize in a wurtzite structure under ambient conditions (Fig. 2.1). The wurtzite structure consists of a hexagonal unit cell with six atoms of each atom species and is characterized by two lattice constants $a$ and $c$, whereas $c$ in [0001]-direction usually denotes the lattice constant in growth direction. In the case of GaN, Ga and N atoms order in hexagonal-closed-packed (hcp) sublattices, which are shifted by $5/8c$ against each other. The sublattices are stacked in an ABAB sequence. In this structure, each Ga-atom is tetraedically surrounded by four N-atoms. Conversely, all N-atoms are surrounded by four Ga-atoms. Since one special characteristic of the III-N wurtzite structure is the absence of an inversion symmetry along the c-axis, the crystal has two polarities. If the bond from N to Ga points along the [0001]-direction, the crystal is called Ga-polar (Fig. 2.1). For the N-polar crystal, this bond points along the [0001]-direction. In the further course of this work, Ga-polar structures are considered only.

Further important physical properties such as band gap ($E_g$), critical electric field ($E_{crit}$), relative dielectric constant ($\varepsilon_r$), electron mobility ($\mu$) and thermal conductivity ($\kappa$) are summarized in Table 2.1. Here, GaN is compared to Si and SiC, the most
2.1. Material Properties

![Wurtzite structure of a GaN crystal](image)

**Figure 2.1.**: Wurtzite structure of a GaN crystal [14].

<table>
<thead>
<tr>
<th></th>
<th>GaN</th>
<th>Si</th>
<th>4H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{crit}$ [MV/cm]</td>
<td>3.3 [7]</td>
<td>0.3 [7]</td>
<td>2.2 [15]</td>
</tr>
<tr>
<td>$BFOM$</td>
<td>780</td>
<td>1</td>
<td>690</td>
</tr>
</tbody>
</table>

**Table 2.1.**: Comparison of the physical properties of GaN, Si, and 4H-SiC. Baliga’s Figure of Merit ($BFOM$) is normalized to Si [17].

prominent materials GaN has to compete with.

Compared to Si, GaN offers a large $E_g$ of 3.43 eV [7]. This results in several advantages over Si. First, the intrinsic carrier concentration at a given temperature is lower, because more energy is needed to lift an electron from the valence band to the conduction band. Consequently, less cooling has to be applied to GaN devices, which is advantageous in terms of thermal management and thus costs. The second advantage resulting from the large $E_g$ is the high $E_{crit}$ [18, 19]. A larger $E_{crit}$ allows the application of a higher blocking voltage for the same layer thickness, which reduces material and therefore again costs. Furthermore, the estimated maximum bulk mobility for electrons is high in GaN, in the range of 900 cm$^2$/Vs. A higher mobility leads to a lower $R_{on}$, which is favorable in terms of electric losses and energy consumption. Considering the above outlined advantages, the lower thermal conductivity of GaN compared to those
of Si and SiC is of minor importance, since most physical properties are also stable at higher temperatures.

With these parameters, GaN and also SiC seem to be promising candidates for high-power applications, in particular compared to Si. To quantify the advantage of GaN for vertical high power devices, the Baliga’s Figure of Merit (BFOM) \[BFOM = \mu \varepsilon_r \varepsilon_0 E_{crit}^3 = \frac{4V_{BR}^2}{R_{on}} \] is often applied, with permittivity of free space ($\varepsilon_0$), relative dielectric constant ($\varepsilon_r$) and breakdown voltage ($V_{BR}$). With this formula, the minimum achievable $R_{on}$ for a desired $V_{BR}$ can be derived. A vertical, uniformly doped drift region is assumed, in which the space-charge region (scr) is spread entirely over the width of the drift region at $V_{BR}$ and the electrical field decreases linearly. The breakdown occurs, when $E_{crit}$ is reached. $R_{on}$ can be derived for such a designed drift region from the doping concentration ($N_D$), the width of the scr ($w$) and $\mu$ by \[R_{on} = \frac{w}{q\mu N_D} \]

The required material parameters and the resulting Baliga’s Figure of Merit (BFOM) for GaN, SiC and Si are given in Tab. 2.1. Normalized to Si, GaN has a 780 times higher $BFOM$, whereas SiC only has a $BFOM$ 690 times as high as Si. Note that, when calculating $BFOM$ for devices, the factor of four is usually neglected.

Apart from the $BFOM$ for the quantification of high-power devices, further FOM exist, for example the Baliga’s High-frequency Figure of Merit ($BHFO\text{M}$). This quantifies the material for high-frequency applications [20].

2.2. Polarization and AlGaN/GaN heterostructure

Polarization A further special characteristic of III-Nitride materials is the presence of strong polarization. The III-Nitrides exhibit spontaneous polarization ($P_{sp}$) along the c-axis. This effect is caused by two factors: the absence of an inversion center and the strong dipole between Ga and N atoms. Since N exhibits a much larger electronegativity than Ga, the electrons are located closer to the N atom, generating a local dipole for each Ga-N bond. The dipoles in the basal plane cancel each other out. In contrast, a net dipole along the c-direction remains, due to the fact that the
crystal does not offer an inversion symmetry along this direction. The direction of $P_{sp}$ depends on the crystal polarity. For a Ga-polar crystal, $P_{sp}$ points along the [0001], the -c-direction, in the N-polar case, $P_{sp}$ is along the +c-direction. In addition to $P_{sp}$, piezoelectric polarization ($P_{pz}$) appears when the crystal is strained. This may occur in a heterostructure, e.g. for a pseudomorphically grown AlGaN layer on a GaN layer. In this case, the AlGaN crystal is tensile strained, and $P_{pz}$ has a component parallel to $P_{sp}$. The resulting total polarization ($P_{tot}$) of a layer can be calculated by $P_{tot} = P_{sp} + P_{pz}$ [22].

**AlGaN/GaN heterostructure and 2DEG**  

The effects of polarization are exploited in the most common heterostructure: the AlGaN/GaN heterostructure. For this purpose, an Al$_x$Ga$_{1-x}$N barrier layer is pseudomorphically grown on a GaN buffer (Fig. 2.2a). The material parameters, such as the lattice constants a and c and $P_{sp}$, of the two binary components AlN and GaN are summarized in Tab. 2.2.

For a common Al content of $x = 0.25$, the AlGaN barrier layer is tensile-strained which results in a polarization $P_{pz}$. As $P_{sp}$ and $P_{pz}$ point in the same direction, the net polarization $P_{tot}$ increases (Fig. 2.2a). Hence, negative polarization charge at the AlGaN top surface and positive polarization charge at the heterointerface exist. Since the interface charge is only partially compensated by the negative polarization charge from the GaN buffer, a positive sheet charge $\sigma_{int}$ remains (Fig. 2.2b). This positive sheet charge is compensated by electrons, bound in a 2DEG, leading to the band diagram depicted in Fig. 2.2c, where the valence band is drawn beneath the Fermi level ($E_F$) [22].

The sheet carrier concentration ($n_s$) in the 2DEG can be approximated by integrating the electric field in c-direction and taking into account Gauss’s equation at the interfaces, with [16]

$$n_s = \frac{\sigma_{int}}{q} - \frac{\varepsilon_0 \varepsilon_{r,bar}}{t_{bar} \cdot q^2} (\Phi_B - \Delta E_C + \Delta) - \frac{\varepsilon_0 \varepsilon_{r,buf}}{t_{buf} \cdot q^2} E_{C,buf}$$  \hspace{1cm} (2.3)

<table>
<thead>
<tr>
<th>Material</th>
<th>$c$ [nm]</th>
<th>$a$ [nm]</th>
<th>$P_{sp}$ [C/m$^2$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlN</td>
<td>0.4982</td>
<td>0.3112</td>
<td>-0.0898</td>
</tr>
<tr>
<td>GaN</td>
<td>0.5185</td>
<td>0.3189</td>
<td>-0.0339</td>
</tr>
</tbody>
</table>

**Table 2.2:** Lattice constants and $P_{sp}$ of AlN and GaN.
2.2. Polarization and AlGaN/GaN heterostructure

Figure 2.2.: Schematics of structure, polarization charges and band diagram for an AlGaN/GaN heterostructure.

depending on the elementary charge \((q)\), \(\varepsilon_r\) of the barrier and buffer layer \((\varepsilon_{r,\text{bar}}, \varepsilon_{r,\text{buf}})\),
the thickness of the barrier and buffer \((t_{\text{bar}}, t_{\text{buf}})\), the Schottky barrier height \((\Phi_B)\),
the conduction band offset at the heterointerface \((\Delta E_C)\), and the conduction band
minimum \((E_C)\) of the buffer. \(\Delta\) can be attributed to the energy the quantum well is
drawn beneath \(E_F\). It is also a function of \(n_S\)

\[
\Delta = E_0 + \frac{\pi \hbar^2}{m_{\text{GaN}}^*} \cdot n_s
\]  

(2.4)

whereby \(m^*\) denotes the effective electron mass and

\[
E_0 = \left\{ \frac{9\pi \hbar^2}{8\varepsilon_0 \sqrt{8m_{\text{GaN}}^*} \cdot \frac{n_s}{\varepsilon_{r,\text{GaN}}}} \right\}^{2/3}
\]  

(2.5)

is the energy of the lowest subband level of the 2DEG.

To manipulate \(n_S\) in the 2DEG, the Al content in the barrier and the barrier thickness
\((t_{\text{bar}})\) can be varied. A higher Al content will increase \(\sigma_{\text{int}}\) and \(\Delta E_C\). Both are resulting
in a higher \(n_S\). Since the barrier layer is strained, \(t_{\text{bar}}\) can only be increased up to the
critical thickness. Otherwise defects will arise. In addition, a thicker barrier will also
enhance \(n_S\). Further means to increase \(n_S\) are to lower \(\Phi_B\) and to increase \(t_{\text{buf}}\).
2.3. HFET

The HFET, also named high electron mobility transistor (HEMT), is a prominent device that makes use of the above mentioned AlGaN/GaN heterostructure and the generated 2DEG. Electrons, confined in a 2DEG, exhibit very large $\mu$ in the order of 2000 cm$^2$/Vs [9]. With $n_S$ of about $1 \cdot 10^{13}$ cm$^{-2}$ [9], an HFET can operate at very high current densities and switching speeds. A schematic of a processed, lateral device is shown in Fig. 2.3. The layer structure is characterized by the buffer thickness $t_{buf}$ and the barrier thickness $t_{bar}$. Ohmic source and drain contacts and a Schottky gate contact are placed on the surface.

Via the gate-induced electric field, the 2DEG can be modulated. Negative gate source voltage ($V_{GS}$) lift $E_C$. Thus, the 2DEG is depleted. At the threshold voltage ($V_{th}$), at which $E_C$ is pulled above $E_F$, no electrons remain in the channel in the intrinsic region beneath the gate and the transistor is pinched off. $V_{th}$ and $n_S$ are related via [23]

$$V_{th} = -\frac{q \cdot t_{bar}}{\epsilon_0 \epsilon_r} \cdot n_s(V_{gs} = 0 \text{ V})$$

(2.6)

For positive $V_{GS}$, further electrons are accumulated in the 2DEG. Due to the presence of the 2DEG, a current can flow at $V_{GS} = 0$ V, when applying a drain-source voltage ($V_{DS}$). Therefore, such a device is called a „normally-on“ or „depletion mode“ HFET. A critical dimension is the gate length ($L_G$), which influences amongst others the dynamic behavior of the device [24]. Additionally, the source gate separation ($d_{SG}$) and gate drain separation ($d_{GD}$) are important parameters which determine $R_{on}$ and $V_{BR}$, respectively.

![Figure 2.3.: Schematic of a processed lateral HFET.](image-url)
The transistor can be characterized mainly by its transfer, output, and input characteristics.

Output characteristics comprise the measurement of drain current \(I_D\) in dependence of \(V_{DS}\) for different \(V_{GS}\). The output characteristics of the HFET show a linear increase in \(I_D\) up to a \(V_{DS}\) called the knee voltage \((V_{knee})\). At \(V_{knee}\), the current saturates since the electrons reach their saturation velocity [25]. \(R_{on}\) can either be extracted from the slope in the linear region [25, p. 374] or calculated from \(V_{DS}\) at a specified \(I_D\).

The impact of \(V_{GS}\) onto \(I_D\) is evaluated by measuring the transfer characteristics. From the transfer characteristics, \(V_{th}\) can be extracted and the maximum of the derivative displays the maximum transconductance \((g_{m,max})\) [26, p. 222ff]. \(V_{th}\) can be extracted using the linear extrapolation method [26, p. 223]. Here, a tangent to the point of maximum slope (which equals the maximum of transconductance \((g_m)\)) is drawn and then extrapolated to \(I_D = 0\) V.

For the input characteristics, the gate current \((I_G)\) is measured in dependence of \(V_{GS}\). This measurement gives information about the gate Schottky diode.

The breakdown voltage of the transistor can be determined via three-terminal breakdown measurements. Therefore, a \(V_{GS} \leq V_{th}\) is applied and \(V_{DS}\) is increased, either until a specified \(I_D\) (e.g. 1 mA/mm) is reached, or the device is destructed. Thereby, the highest electrical field is located at the gate edge towards the drain. For larger \(d_{GD}\), the field at the gate edge is reduced, thus \(V_{BR}\) is enhanced.

### 2.4. Epitaxial growth

Epitaxy is a Greek word, that consists of the words „\(E\)pi“ which means „above“ and „\(t\)axis“ which means „ordered“ or „aligned“. In general, epitaxial growth denotes the growth of a crystalline layer which adopts the structure of a crystalline substrate. In this work, III-Nitride layers were grown epitaxially on an underlying substrate or layer with MOCVD or MBE.

**Substrates** The main difficulty in growing GaN is the lack of a native substrate. Due to the high vapor pressure of nitrogen \((N_2)\) and the high melting point of GaN, it has not been achieved yet to grow large GaN single-crystals with a Czochralski method [27]. First results of freestanding GaN substrates have been obtained with methods such as hydride vapor phase epitaxy (HVPE) [28] and the AMMONO-Bulk Method [29]. With these techniques, substrates with a dislocation density of \(3\cdot10^6\) cm\(^{-2}\) [30]
2.4.1. MOCVD

and $5\cdot10^3\,\text{cm}^{-2}$ [29] can be realized, respectively. The AMONNO-Bulk Method is very promising, but since this technology is rather new, the availability of freestanding GaN substrates is still insufficient and according to this, prices are still high. Furthermore, only small wafers up to 2" are available.

Therefore, GaN films are grown heteroepitaxially on foreign substrates for most applications. Usually, GaN is deposited on sapphire ($\text{Al}_2\text{O}_3$), SiC or Si with MBE or MOCVD. The large mismatch in lattice constants and thermal expansion coefficients of the GaN film and substrate (Tab. 2.3) lead to defect densities which are much more pronounced compared to homoepitaxially grown GaN. As a result, average defect densities of $10^9\,\text{cm}^{-2}$ are common [31].

The amount of defects plays an important role for the quality of the devices. Electrically active defects, such as dislocations, lead to an increase in leakage currents and therefore reduce $V_{BR}$ [32–34]. The availability of high-quality GaN substrates is crucial, especially for the realization of vertical devices with high $V_{BR}$ [34, 35].

<table>
<thead>
<tr>
<th>Parameter</th>
<th>GaN</th>
<th>$\text{Al}_2\text{O}_3$</th>
<th>6H-SiC</th>
<th>Si (111)</th>
</tr>
</thead>
<tbody>
<tr>
<td>lattice constant a [Å]</td>
<td>3.189</td>
<td>4.759</td>
<td>3.081</td>
<td>5.43</td>
</tr>
<tr>
<td>lattice mismatch to GaN [%]</td>
<td>-</td>
<td>14.8</td>
<td>3.48</td>
<td>-16.99</td>
</tr>
<tr>
<td>thermal expansion coefficient [$10^{-6}/\text{K}$]</td>
<td>5.59</td>
<td>7.5</td>
<td>4.46</td>
<td>2.59</td>
</tr>
</tbody>
</table>

Table 2.3.: Lattice constants and thermal expansion coefficients for GaN and suitable substrate materials [17].

2.4.1. MOCVD

Most samples in this work were grown by MOCVD [36, 37] on sapphire substrates. To grow GaN or AlGaN, metal-organic precursors such as trimethylgallium (TMGa), trimethylaluminium (TMAl) and ammonia (NH$_3$) are injected via a carrier gas (either hydrogen or nitrogen) into the reactor. The susceptor is heated from the bottom with radio frequency (RF) coils. High temperatures around 1050 °C are applied for GaN growth. The substrate is located in the middle of the reactor and it is rotated to obtain a homogeneous layer thickness. The precursors decompose inside the heated reactor and the free Ga, Al or N atoms bond to the substrate. The volatile reaction products are evacuated into the exhaust. The adsorbed atoms diffuse preferably to step edges, where they bind to neighboring atoms. For better process control, the temperature and growth rate can be recorded with a pyrometer and a white-light interferometer.
2.4.3. Doping

To grow n- or p-type GaN, different dopants can be introduced.

**n-type doping** For n-type GaN, the most common dopant is Si, which is provided by silane (SiH$_4$) as precursor during the MOCVD and MBE process [41]. Si is a shallow donor with an activation energy of $w_D = 12$–$17$ meV, depending on the donor concentration ($N_D$) [42]. Due to this small energy, a complete ionization at room temperature ($T_R$) is realized ($kT_R \approx 25$ meV). Thus, $N_D$ corresponds to the electron concentration ($n$). The Si (and electron) concentration can be varied by the silane flow in a wide range from about $5 \cdot 10^{15}$ cm$^{-3}$ to $5 \cdot 10^{19}$ cm$^{-3}$ [41]. Besides Si, germanium can be used as an n-dopant as well [43].

**p-type doping** A p-type dopant for GaN is Mg. Mg is introduced into the gas phase by Cp$_2$Mg for MOCVD and MBE growth [7]. In contrast to n-type doping, p-type doping of GaN is challenging. First, GaN usually exhibits an n-type background doping which has to be compensated [44]. Second, the Mg atoms are passivated by hydrogen atoms, which are provided particularly during MOCVD growth from the carrier gas or the ammonia [45]. The Mg-H bonds can be broken with an annealing step above 600 °C [46]. Third, excessive Mg doping leads to self-compensation [46]. Furthermore, residual carbon impurities have been identified to compensate the Mg doping, leading to highly resistive GaN [47]. This effect occurs predominantly in MOCVD processes and not in...
2.4.3. Doping

the carbon-free MBE growth.
Mg forms a deep acceptor in GaN with an activation energy of $w_A = 160 - 200$ meV [17]. With an optimized annealing procedure and due to the fact that the activation energy is much larger than $kT_R$, a doping efficiency of only 1-5% can be achieved [46]. For an acceptor concentration ($N_A$) of $10^{19}$ cm$^{-3}$, only about $10^{17}$ cm$^{-3}$ holes can be generated. Consequently, a maximum bulk hole concentration ($p$) of only $5 \cdot 10^{17}$ cm$^{-3}$ was reported [41].
3. Vertical devices

GaN, as a wide bandgap material, is an excellent candidate for high-power and high-temperature applications. However, in lateral devices as presented in Sec. 2.3, an enhancement in breakdown voltage is, amongst other means, mainly achieved by an increase of $d_{GD}$ [48, 49]. The device dimensions become larger which implies an increase in chip size and consequently higher costs. Additionally, $R_{on}$ increases, which leads to further losses. To avoid these problems and still access the whole possible voltage range, the interest in vertical devices has evolved over the last years. Here, the drain contact of the device is placed on the backside of the structure. Thus, a separation from the Schottky contact across the thickness is achieved and the lateral dimensions of the device can be kept small. The large metal backside contact can also serve as a heat sink, which enhances the cooling efficiency of the devices.

To judge the devices concerning their suitability for high-power applications, the two important device characteristics $R_{on}$ and $V_{BR}$, which are linked through the $BFOM$ (Eq. 2.1), are evaluated. An overview of the devices realized so far is given in Fig. 3.1. The theoretical predicted limits comprising $R_{on}$ and $V_{BR}$ of Si, SiC, and GaN are plotted according to Eq. 2.1, using the parameters in Tab. 2.1. In this visualization of the $BFOM$, the superior properties of GaN for power applications are again emphasized.

In the graph, characteristic values for GaN-based vertical heterostructure field effect transistors (VHFET) [50–52] and vertical metal oxide semiconductor field effect transistors (VMOSFET) [53] are plotted in comparison to lateral HFET [54, 55]. Recent publications made clear that vertical devices can compete with lateral ones, even though their technology is rather new and thus not matured. Moreover, the values for vertical Schottky diodes (VSD) [35, 56–60] and vertical pn diodes [59, 61–63] are plotted. These approach the theoretical maximum of GaN in terms of $R_{on}$ and $V_{BR}$ and therefore outperform lateral diodes [64, 65].

Depending on the application, either vertical diodes or vertical transistors are of interest. In this chapter, different realizations of vertical diodes will be presented first. Subsequently, the more complex architecture of a vertical transistor is introduced.
3.1. Vertical diodes

In order to replace Si devices in high-power applications, e.g. rectifiers, GaN-based vertical diodes are promising candidates. The large bandgap and therefore high theoretical breakdown field render them not only suitable for high-power but also for high-temperature applications. Vertical Schottky diodes (VSD) and vertical pn diodes have been fabricated so far (Fig. 3.2), which will be elucidated in detail in the following paragraphs. Compared to pn diodes, Schottky diodes offer an additional advantage: due to their unipolar nature, reverse recovery effects are on time constants below 20 ns [66], leading to very high switching speeds.

**Vertical Schottky diodes** A schematic of a VSD is drawn in Fig. 3.2a. It consists of an n⁺-GaN substrate and an n⁻-GaN layer. The Schottky contact is placed on top of the n⁻-GaN layer, the drain contact is placed at the backside of the structure.

The electrical field distribution for reverse-biased VSD at -12 V with different $N_D$ of $8\cdot10^{15}$ cm$^{-3}$ (low) and $6\cdot10^{16}$ cm$^{-3}$ (high) is plotted in Fig. 3.3. A plot of the electrical field along the arrows is depicted in Fig. 3.4. For both $N_D$, a linearly decreasing field profile is observed. The slope and the extension of the field is influenced by the selected
3.1. Vertical diodes

(a) Cross section of a vertical Schottky diode (VSD).

(b) Cross section of a vertical pn diode.

Figure 3.2.: Schematic of vertical diodes on freestanding GaN substrate.

doping concentration. For a higher $N_D$, the field at the Schottky contact is increased and the field decreases with steeper slope. For lower $N_D$, the maximum field at the contact is lower and the field is extended further into the $n^-$-GaN. The expansion $w$ of the electrical field, which corresponds to the expansion of the scr, in dependence of the applied voltage $V$ can be calculated by [8]

$$w(V) = \sqrt{\frac{2\varepsilon_r\varepsilon_0}{q}} \frac{1}{N_D} (V_{Bi} - V)$$  \hspace{1cm} (3.1)

with $V_{Bi}$ as built-in voltage.

As it is visible for both VSD (Fig. 3.3), the maximum field is located at the edge of the Schottky contact at the metal semiconductor junction. The maximum field at the Schottky contact is [8]

$$E_{max} = \sqrt{\frac{2qN_D}{\varepsilon_0\varepsilon_r}} (V_{Bi} - V)$$  \hspace{1cm} (3.2)

If the blocking voltage is enhanced, on the one hand, the maximum field at the contact edge will increase further and on the other hand, the scr will spread over the total thickness until it will reach the underlying $n^+$-GaN. In this case, the maximum field increases much faster towards $E_{crit}$. If $E_{crit}$ is reached at the Schottky contact edge, the device will break down. The exact breakdown mechanisms in GaN are still under discussion [7, 67].

In order to realize a high $V_{BR}$, a small doping concentration and a thick $n^-$-GaN drift
3.1. Vertical diodes

(a) Electrical field in a VSD with low $N_D = 8 \times 10^{15}$ cm$^{-3}$.

(b) Electrical field in a VSD with high $N_D = 6 \times 10^{16}$ cm$^{-3}$.

Figure 3.3.: Electrical field distribution of reverse biased VSD with different $N_D$.

Figure 3.4.: Plot of the electrical field of VSD with different $N_D$.

region should be used. The n$^-$-GaN drift region should be dimensioned in a way that the scr does not reach the n$^-$-GaN for the targeted $V_{BR}$ and that $E_{crit}$ is not exceeded. For example, for $V_{BR} = 600$ V and $N_D = 6 \times 10^{16}$ cm$^{-3}$ an n$^-$-GaN thickness of $\approx 3.7$ $\mu$m is necessary taking into account the width of the scr (Eq. 3.1) and $E_{crit}$ (Eq. 3.2). $R_{on}$ can be derived via $\mu$ and $E_{crit}$ from the $BFOM$ (Eq. 2.1).

The first VSD were fabricated on foreign, mainly insulating substrates, such as sapphire. This implies the fabrication of quasi-vertical devices, only. For a quasi-vertical device, the layer structure is grown on an n$^+$-GaN layer to form the ohmic contact thereon. This is accessed from the top by etching of the overlying layers. For such quasi-vertical devices, breakdown voltages of $V_{BR} = 550$ V and $R_{on} = 8$ m$\Omega$cm$^2$ were achieved [68]. Later diodes were processed directly on GaN substrates without
epitaxy which resulted in $V_{BR} = 630\,\text{V}$ and $R_{on} = 2.2\,\text{m}\Omega\,\text{cm}^2$ [69]. The doping of the layer underneath the Schottky contact mainly dominates $V_{BR}$. To adjust the doping concentration for the drain contact layer and the drift region independently, GaN layers were grown homoepitaxially on GaN substrates. An n$^-$-GaN layer with $N_D = 4\cdot10^{16}\,\text{cm}^{-3}$ below the Schottky contact was used to obtain a minimized $E_{crit}$ at the contact edge and an n$^+$-GaN layer with $N_D = 4\cdot10^{18}\,\text{cm}^{-3}$ as contact layer were used [70]. For VSD, record $V_{BR}$ of 1100 V with $R_{on}$ of 0.71 mΩ cm$^2$ (Fig. 3.1) and an $N_D$ of $8\cdot10^{15}\,\text{cm}^{-3}$ were achieved, resulting in a $B\text{FOM}$ of 1.7 GW/cm$^2$ [35].

**pn diodes** A schematic of a pn diode is drawn in Fig. 3.2b. Here, a p$^+$-GaN layer is grown on top of an n$^-$-GaN layer. Ohmic n- and p-contacts are used to contact both layers.

The electrical field distribution for two reverse biased junctions is drawn in Fig. 3.5. A p-type doping concentration of $N_A = 1.3\cdot10^{19}\,\text{cm}^{-3}$ is employed for both devices. The first device (Fig. 3.5a) has an n-type doping concentration of $N_D = 8\cdot10^{15}\,\text{cm}^{-3}$ (low), whereas for the second device (Fig. 3.5b), $N_D = 6\cdot10^{16}\,\text{cm}^{-3}$ (high) is applied. As Fig. 3.6 shows, in a pn junction the highest field is located at the pn interface inside the structure. A linear decrease of the field is observed in the p$^+$-GaN as well as in the n$^-$-GaN. The field distribution can be influenced by $N_D$ and the offset in $N_D$ and $N_A$. For a large offset, here, a p$^+$n$^-$ diode, the field mainly expands into the n$^-$-GaN. As stated above, the electrical field drops with steeper slope for higher $N_D$ in the n-GaN region. Furthermore, the maximum field at the pn junction is lower. The slope of the electrical field in the p-GaN is equal for both devices due to equal $N_A$. For increasing blocking voltage, the scr will expand primarily in the n$^-$-GaN and the maximum electrical field at the junction will increase further. When $E_{crit}$ is reached at the pn junction, the device will break down. In order to obtain the maximum $V_{BR}$ at $E_{crit}$, a low $N_D$ and a sufficiently thick n$^-$-GaN for the scr should be chosen. The $R_{on}$ is determined by the n$^-$-GaN region by Eq. 2.2.

Much work has been performed on true-vertical pn diodes. They usually offer a higher $V_{BR}$ compared to similarly doped Schottky diodes. For pn diodes, the maximum field is located in the structure at the pn junction. Accordingly, effects from the surface and contacts edges are less pronounced. However, the low mobility of holes in GaN reduces the maximum switching speed of such devices [71].

First, quasi-vertical pin diodes were realized on sapphire substrate [72]. For these, an
3.1. Vertical diodes

(a) Electrical field in a pn diode with $N_D = 8 \times 10^{15} \text{ cm}^{-3}$ and $N_A = 1.3 \times 10^{19} \text{ cm}^{-3}$.

(b) Electrical field in a pn diode with $N_D = 6 \times 10^{16} \text{ cm}^{-3}$ and $N_A = 1.3 \times 10^{19} \text{ cm}^{-3}$.

Figure 3.5.: Electrical field distribution of reverse biased pn diodes with different $N_D$ and equal $N_A$.

Figure 3.6.: Plot of the electrical field of pn diodes with different $N_D$.

The intrinsic layer was introduced between the p-GaN and n-GaN layer, to further decrease $R_{on}$, even though this usually has negative effects on the dynamic characteristics [21]. For this pin diode, a $V_{BR}$ of 490 V was achieved compared to a Schottky diode with $V_{BR}$ of 347 V. The devices started to improve when pn diodes on freestanding GaN substrates were fabricated. These offered about 1.6 times higher $V_{BR}$ [73]. With increasing layer quality, $V_{BR}$ of 1100 V with $R_{on}$ of 0.4 mΩ·cm$^2$ were achieved (Fig. 3.1). Doping levels of $2 \times 10^{16} \text{ cm}^{-3}$ for the n-GaN and $5 \times 10^{17} \text{ cm}^{-3}$ for the p-GaN layer were used for the record diode with a $BFOM$ of 3 GW/cm$^2$ [63].

In summary, the full potential of vertical Schottky and pn diodes could not be exploited, yet. One main problem is still the lack of high-quality GaN substrates which leads to premature breakdown at $E_{crit}$ below the theoretical maximum of 3.3 MV/cm.
Several studies show the dependence of $V_{BR}$ on dislocation density. Due to an increased possibility of a vertical dislocation short-circuiting the two contacts, scaling up to larger device sizes is especially difficult [57, 74]. Furthermore, field crowding at the contact edges was identified as one of the main effects promoting an early breakdown [75, 76]. Guard rings [74], edge termination [58, 77], field-plates and passivation [63] were applied to reduce this effect leading to a higher breakdown voltage. The first commercial suppliers recently started to offer vertical Schottky diodes and pn diodes on freestanding GaN substrates with $V_{BR} = 600$ V and $V_{BR} = 1700$ V, respectively [78].

### 3.1.1. Diode characterization

Usually, diodes are characterized via IV measurements. For Schottky diode, only thermionic emission over the Schottky barrier is assumed and the forward IV curve of an ideal diode can be described as

$$I = AA^* T^2 e^{\frac{\Phi_B}{kT}} (e^{\frac{qV}{nkT}} - 1) = I_s (e^{\frac{qV}{nkT}} - 1)$$

in which $A$ is the diode area, $A^* = 26.4 \text{ A/cm}^2\cdot\text{K}^2$ the Richardson constant [79], $T$ the temperature, $\Phi_B$ the Schottky barrier height, $V$ the applied voltage, and $k$ Boltzmann’s constant. $I_s$ is denoted as saturation current.

The ideal Eq. 3.3 neglects different effects, which occur in a real diode. According to the Schottky effect, the ideal $\Phi_B$ changes with voltage, when $|V| > 3kT$ due to image force barrier lowering [8]. For positive voltages, the barrier height increases, whereas for negative voltage, it decreases. Furthermore, the Richardson constant is voltage-dependent [8]. To include these effects into the theory, the ideality factor $n$ is introduced

$$n = \frac{qA}{kT} \frac{\delta V}{\delta (\ln I)}$$

The current is now described by

$$I = AA^* T^2 e^{\frac{\Phi_B}{kT}} (e^{\frac{qV}{nkT}} - 1) = I_s (e^{\frac{qV}{nkT}} - 1)$$

The ideal barrier height is calculated from $I_s$, which is extrapolated from the semi-
logarithmic I versus V curve to V = 0 V with [26].

$$\Phi_B = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_s}\right)$$ (3.6)

For pn diodes, the ideal approach comprises only diffusion and the forward direction can be applied by [8]

$$I = I_s(e^{\frac{qV}{nkT}} - 1)$$ (3.7)

with

$$I_s = \frac{eD_{p}p_n}{L_p} + \frac{eD_{n}n_p}{L_n}$$ (3.8)

and $p_n$ and $n_p$ as minority carrier concentrations, $D_{p,n}$ as minority carrier diffusion constants and $L_{p,n}$ as minority carrier diffusion lengths.

For a real pn junction, further mechanisms other than diffusion have to be considered. For lower voltages, recombination in the scr is dominant, leading to $n=2$, for higher voltages, high injection is detected, also leading to $n=2$.

Real Schottky and pn diodes also exhibit an $R_{on}$, leading to a deviation from the exponential current to a linear resistor. The resistance can be extracted from the linear slope with

$$R_{on} = \frac{\Delta V}{\Delta I}$$ (3.9)

With capacitance voltage (CV) measurements, the $N_D$ of the material can be determined for Schottky diodes on n-GaN. Furthermore, the $N_D$ in $p^+n^-$ junctions can be measured, given that the scr only reaches into the $n^-$-GaN. For the CV technique, the fact, that the width of the scr depends both, on the applied reverse voltage and the doping concentration, is exploited. Assuming a plane-parallel capacitor, the width ($w$) of a reverse-biased junction can be calculated, in dependence of the measured capacitance (C), with [26]:

$$w = \frac{\varepsilon_r \varepsilon_0 A}{C}$$ (3.10)

with $A$ as the area of the contact.

Corresponding to the width, $N_D$ can be calculated [26]. Later on, this will be denoted as carrier concentration derived by CV measurements ($N_{CV}$):

$$N_{CV}(w) = \frac{2}{q\varepsilon_r \varepsilon_0 A^2 \frac{d(1/C^2)}{dV}}$$ (3.11)
Furthermore, for Schottky diodes, $\Phi_B$ can be extracted from CV from the intercept $V_i$ of the $1/C^2$ curve with the V-axis. With [26]

$$\Phi_B = -V_i + V_0 + kT/q$$  \hspace{1cm} (3.12)

and $V_0 = (kT/q) \ln (N_C/N_D)$ and $N_C$ as effective density of states in the conduction band.

$V_{BR}$ can either by defined as the voltage, at which a specific current (e.g. 1 A/cm$^2$) is reached or as the bias, at which the device suffers from destructive breakdown.

### 3.2. Vertical transistors

High-power switches can particularly profit from vertical heterostructure field effect transistors (VHFET). An exemplary structure of a VHFET based on the CAVET principle is shown in Fig. 3.7. Here, the source and gate electrode are located at the top of the structure and the drain contact is located at the backside.

As stated before, VHFET offer a larger $V_{BR}$, due to the vertical separation of the gate and drain contact. Among this detail, VHFET offer further advantages. As simulations performed with Sentaurus TCAD from Synopsys [80, 81] reveal, the point of highest field in lateral HFET is located in vicinity of the gate towards the drain (Fig. 3.8a). For these devices, the point of highest field is either close to the surface, or for a passivated device, as shown in Fig. 3.8a, at the interface between GaN and SiN passivation. On the contrary, in a VHFET the point of highest field is buried inside the structure.

![Figure 3.7.: Cross section of a vertical heterostructure field effect transistor (VHFET) based on the CAVET principle.](image-url)
3.2. Vertical transistors

The vertical trench gate approach also relies on a 2DEG channel, as the CAVET, but uses a pn junction for the reverse blocking [52, 86] (Fig. 3.9b). An inversion channel with a pn junction for the current blocking [84, 85] (Fig. 3.9a).

The vertical metal oxide semiconductor field effect transistor (VMOSFET) combines state-of-the-art VMOSFET and trench gate transistor is given.

In the following, the most promising concept of the CAVET and its possible realizations are presented in more detail. Subsequently, an overview of the concept and state-of-the-art VMOSFET and trench gate transistor is given.

Figure 3.8.: The electrical field distribution for a lateral HFET and VHFET at pinch-off and large $V_{DS}$. The point of highest field inside the respective structure is highlighted. The scale is valid for both structures.

beneath the gate at the edge of the CBL (Fig. 3.8b). This reduces the influence of surface states, one of the main sources for the current collapse phenomenon [5, 82]. Consequently, complex passivation schemes and field plates will be unnecessary for VHFET [11].

If the VHFET is in on-state, the current flows vertically from the source electrodes to the drain contact. To reduce $R_{on}$ and to obtain a gate-controllable device, as channel, either a 2DEG formed by an AlGaN/GaN heterostructure or an inversion channel are used. In off-state, the channel is depleted by the gate and the transistor is pinched off. To block a high drain voltage, a thick n$^-$-GaN drift layer or a pn junction are employed.

Different realizations of vertical transistors have been presented. The CA VET concept uses a 2DEG as channel, combined with a thick n-GaN drift layer [13, 83] (Fig. 3.7). The vertical metal oxide semiconductor field effect transistor (VMOSFET) combines an inversion channel with a pn junction for the current blocking [84, 85] (Fig. 3.9a). The vertical trench gate approach also relies on a 2DEG channel, as the CA VET, but uses a pn junction for the reverse blocking [52, 86] (Fig. 3.9b).

In the following, the most promising concept of the CAVET and its possible realizations are presented in more detail. Subsequently, an overview of the concept and state-of-the-art VMOSFET and trench gate transistor is given.
3.2. Vertical transistors

Figure 3.9.: Two different realizations of vertical transistors relying on an npn structure.

CAVET The vertical transistor which has yielded the best results in terms of $V_{BR}$ and $R_{on}$ so far, is the CAVET. The concept, process flow and realizations will be elucidated in the following.

Concept: The layer structure of a CAVET is presented in Fig. 3.7. The fully vertical structure consists of an $n^+$-GaN substrate for the backside ohmic contact. Next, it continues with a thick, low doped $n^-$-GaN drift layer, which provides a high $V_{BR}$ in reverse direction. On top, a GaN channel and an AlGaN barrier layer are used for the 2DEG formation. The source and gate contacts are deposited on the surface. In addition, a current blocking layer (CBL) with an aperture is introduced into the structure. This can either be an insulating region or a p-GaN layer. Accordingly, the CBL prohibits a direct vertical current flow from the source contacts via the 2DEG at the AlGaN/GaN heterostructure to the drain without control of the gate.

In on-state, the current flows via the 2DEG through the aperture underneath the gate towards the drain. The resistance of the drift layer and the aperture region should be smaller than that of the 2DEG. This ensures that the device characteristics are dominated by the 2DEG conductivity [83]. To pinch off the device, the 2DEG and the regrown GaN channel are depleted by the gate and the vertical current flow is suppressed. The applied $V_{DS}$ drops over the drift region. The field distribution for such a case is shown in Fig. 3.10a. The plot in Fig. 3.10b shows the field for two different locations in the structure. On the one hand, the distribution far away from the gate in the drift region is plotted (black). Here, a linear decrease of the electrical field in the drift zone is observed. On the other hand, the distribution close to the gate at the aperture edge is shown (red). Here, a steep increase towards the aperture
3.2. Vertical transistors

(a) Electrical field distribution.  
(b) Electrical field along the arrows in (a).

**Figure 3.10.** Electrical field distribution in a CAVET with $V_{GS} \leq V_{th}$ and positive $V_{DS}$.

is observed. As stated in Sec. 3.1, a high $V_{BR}$ is obtained by choosing the doping concentration and thickness of the n$^-$-GaN region in a way, that the scr does not expand to the n$^+$-GaN before $V_{BR}$ is reached.

In a switching application, the CBL should be on a fixed potential to circumvent an uncontrolled charging. One possibility is to connect the CBL with the ground potential of the source.

**Process:** The fabrication of a CAVET is a rather complex process. In particular, the formation of the current aperture and the regrowth of the channel on top were identified as the main challenges [51]. Three different process schemes for a CAVET, which are depicted in Fig. 3.11 are presented. First, a suitable material and process have to be found to create the CBL and the aperture. The CBL should block the current sufficiently, offer temperature stability and should be easy to process. The simplest process comprises the use of implantation to form the CBL. In this case, only a single mask is necessary to protect the aperture opening from implantation (Process 1). One method to render a layer insulating by implantation is defect-induced isolation by either iron (Fe) or aluminum (Al) [5]. However, the temperature stability remains to be a challenge. Especially, the regrowth performed with MOCVD at 1050 °C after implantation will heal out the defects. Another method is to generate p-GaN by Mg implantation [83]. After the implantation procedure, the mask is removed and the AlGaN/GaN heterostructure is regrown on the planar surface.

A more sophisticated process is required, if p-type doping is used to generate the CBL (Process 2, Process 3). For this, mainly Mg doping is applied. In Process 2, the n-
3.2. Vertical transistors

GaN is etched first and then the p-GaN is regrown selectively only at the designated locations for the CBL. Afterwards, the AlGaN/GaN heterostructure is grown. This process comprises two regrowth steps and is therefore rather complicated.

![Diagram of Process 1, Process 2, and Process 3]

**Figure 3.11.:** Three different routes to process a CAVET. In Process 1, Mg implantation is used to form the aperture. In Process 2, the p-doped aperture is created in a selective regrowth step. Process 3 includes the etching of a p-doped aperture.
For Process 3, the p-GaN layer is epitaxially grown homogeneously on the whole wafer. Then, the aperture is formed by etching into the CBL, preferably with a low-damage etch process. Here, the geometry of the aperture and the edge of the CBL can be influenced. In the next step, the AlGaN/GaN regrowth is performed and the aperture is filled. Usually, the aperture region cannot be planarized, most likely leading to further challenges in the following processing sequence [87, 88].

As stated above, a regrowth of an AlGaN/GaN heterostructure has to be performed for all three processes. Hereby, the regrowth on Mg-doped layers was figured out to be challenging since Mg is known to diffuse into overgrown layers [38]. However, not only doped, but also Mg-implanted layers suffer from Mg out-diffusion into the regrown layers. This leads to threshold voltages instabilities and increases $R_{on}$ [51]. The Mg diffusion can be reduced by growing the subsequent layers at lower temperatures for example with MBE [51] or by etching the sample prior to the regrowth to remove the high concentration Mg layer which is typically observed near the surface [38]. To prevent Mg diffusion, also the use of a thin AlN layer was proposed [89].

**Realizations:** Devices which use Mg implantation for the CBL and MBE regrowth showed $V_{BR} = 200$ V with a drift layer thickness of 3 $\mu$m, resulting in $E_{crit} = 0.66$ MV/cm and $R_{on} = 2.2$ m$\Omega$ cm$^2$ [5] (Fig. 3.1). Another device with a Mg-doped CBL and MOCVD regrowth on the etched aperture reached $V_{BR} = 1.5$ kV with a drift region of 15 $\mu$m. From this $E_{crit} = 1$ MV/cm is calculated. However, $R_{on}$ was as low as 2.2 m$\Omega$ cm$^2$, so that $BFOM$ was 1.02 GW/cm$^2$ [50] (Fig. 3.1).

Besides the above mentioned CAVET, this layer design offers the possibility to fabricate a junction field effect transistor (JFET). In this device, the CBL would serve as a p-GaN gate electrode.

**Vertical metal oxide semiconductor field effect transistor (VMOSFET)**

One approach for a vertical transistor is the Vmetal oxide semiconductor field effect transistor (MOSFET). For this device, a layer stack consisting of a thick n$^-$-GaN layer with a p$^-$-GaN layer and an n$^+$-GaN layer on top is grown (Fig. 3.9a). To obtain the MOSFET-typical inversion channel, a trench with a shallow angle is etched and the oxide, usually silicon nitride (SiN) or silicon oxide (SiO$_2$), is deposited thereon. The gate-stack is evaporated on top of the oxide. For positive $V_{GS}$ above $V_{th}$, an inversion channel is generated at the interface of the n$^+$-GaN and the n$^-$-GaN, in which a $\mu$ up to 100 cm$^2$/Vs is achieved [84]. This is much lower compared to the $\mu$ in a 2DEG, thus leading to a higher $R_{on}$. In reverse direction, for $V_{GS}$ below $V_{th}$, the channel is depleted and the pn junction will block the voltage. The challenge of fabricating a VMOSFET...
3.2. Vertical transistors

is the management of the interface between the etched GaN and the oxide material [7]. Interface states will influence the threshold voltage and its stability. However, if adjusted properly, a high positive $V_{th}$ can be obtained [85], as one advantage of the MOSFET approach. A breakdown voltage of 1600 V, with an $R_{on} = 12 \text{mΩ cm}^2$ (Fig. 3.1) and $V_{th} = 7 \text{V}$ was demonstrated [53]. This leads to a $BFOM$ of 0.2 GW/cm.

**Trench Gate Transistor** Trench gate devices use the same layer stack as the VMOSFET. Contrarily to the VMOSFET, the channel in a trench gate device is obtained by a 2DEG. Therefore, an AlGaN/GaN heterostructure is regrown on the etched sidewalls. Subsequently, the gate is deposited on top of the AlGaN in the etched region (Fig. 3.9b). Higher output currents are obtained due to the advantageous high mobility of the 2DEG in contrast to the inversion channel. In on-state, the current can flow via the 2DEG into the drift layer, thus guaranteeing a low $R_{on}$. In off-state, the pn junction will block the electrons and the scr between the n$^-$ and p$^-$-GaN layer induces a high $V_{BR}$ [52, 86]. In addition, the presented devices showed the variation of $n_S$ with the AlGaN barrier thickness [52]. The main challenges for the realization of this concept is the precise etching of the trench gate with shallow angles and the homogeneous regrowth on top of the etched sidewall. Realizations of this concept showed $V_{BR}$ of 672 V and $R_{on}$ of 7.6 mΩ cm$^2$ [52] as depicted in Fig. 3.1. From this, a $BFOM$ of 59 MW/cm$^2$ was calculated.


4. Simulation of a CAVET

Before processing a vertical transistor, understanding the critical dimensions and parameters and their influence onto the device characteristics is of major importance. Therefore, numerical simulations were carried out using Sentaurus TCAD from Synopsys [80, 81, 90]. In the simulations, the device structure is divided into many segments by a user-defined mesh. For each segment, the Poisson equation is solved self-consistently, taking into account the electron and hole continuity equation. Furthermore, the simulations performed in this work apply the drift-diffusion model to allow for different temperatures for the electrons and the lattice [81]. This is necessary especially for large differences in doping concentration. The devices simulated here comprise only electron transport, thus, the hole temperature is neglected in the drift-diffusion model. Additionally, quantization effects, especially for the confinement calculations in the 2DEG, are included. For breakdown simulations, the impact ionization model provided by Sentaurus TCAD is applied.

The purpose of these simulations is to highlight the effects and trends of variations in the device structure onto the electrical characteristics and to deduce design rules. The simulations are based on the structure shown in Fig. 4.1 in cross-section and plain view. The parameters, which were varied, are depicted in bold black. All currents are normalized to the active area. It is defined as the area between the two source electrodes multiplied by the width of the aperture.

![Cross section and plain view of the structure](image)

**Figure 4.1.:** Cross section (left) and plain view (right) of the structure on which the simulations are based. The parameters which are varied are depicted in bold black.
Three parameters related to the growth of the structure were varied in the simulation. First, the doping concentration of the drift region \( (N_{\text{drift}}) \) was modified. This will mainly influence \( R_{\text{on}} \) and \( V_{BR} \). Since these values scale linearly with the thickness of the drift region, it was kept constant. Second, the impact of the doping concentration of the channel region \( (N_c) \) onto \( V_{th} \) and \( g_m \) was evaluated. Third, the channel thickness \( (d_c) \) was changed. Information on its impact on the current and the pinch-off behavior of the transistor can be gained. Besides the growth-related parameters, also the dimensions of the processed device are important, such as the overlap of gate and aperture \( (L_{GA}) \). \( L_{GA} \) accounts as the effective gate length. Also devices with different aperture lengths \( (L_{ap}) \) were simulated. This parameter mainly influences the aperture resistance and consequently \( R_{on} \). At last, the geometry of the aperture was varied. Different opening angles \( (\alpha) \) are simulated to evaluate the influence onto \( E_{crit} \) and \( V_{BR} \).

In Tab. 4.1, an overview of the simulated parameters is provided. The standard parameters are printed in bold. While simulating one, the other parameters were kept constant at their standard value.

<table>
<thead>
<tr>
<th>Standard</th>
<th>( N_{\text{drift}} ) [cm(^{-3})]</th>
<th>( N_c ) [cm(^{-3})]</th>
<th>( d_c ) [nm]</th>
<th>( L_{GA} ) [nm]</th>
<th>( L_{ap} ) [( \mu \text{m} )]</th>
<th>( \alpha ) [°]</th>
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<tbody>
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<td>( 5 \cdot 10^{16} )</td>
<td>200</td>
<td>250</td>
<td>3.0</td>
<td>90</td>
</tr>
<tr>
<td>Variation</td>
<td>( 1 \cdot 10^{16} )</td>
<td>( 1 \cdot 10^{16} )</td>
<td>100</td>
<td>0</td>
<td>1.5</td>
<td>36 - 90</td>
</tr>
<tr>
<td>Variation</td>
<td>( 1 \cdot 10^{16} ) + ( 1 \cdot 10^{17} )</td>
<td>( 1 \cdot 10^{17} )</td>
<td>300</td>
<td>750</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>Variation</td>
<td>( 1 \cdot 10^{17} )</td>
<td></td>
<td>1000</td>
<td></td>
<td>6</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.1.: Parameters for the simulation of the CAVET.

To simplify the simulation, a possible leakage current through the CBL is neglected. Therefore, a 150 nm thick p-GaN layer with a hole concentration of \( 1 \cdot 10^{20} \) cm\(^{-3}\) was used to guarantee a total blocking of vertical leakage currents. No potential was applied to the CBL.

### 4.1. Drift region doping

First, different doping levels of the drift region \( (N_{\text{drift}}) \) were simulated. A doping concentration has to be found which optimizes the competing quantities \( R_{on} \) and \( V_{BR} \). Here, four different values of \( N_{\text{drift}} \), which can be accessed with epitaxial growth [41], were applied: \( 1 \cdot 10^{17} \) cm\(^{-3}\), \( 5 \cdot 10^{16} \) cm\(^{-3}\), \( 1 \cdot 10^{16} \) cm\(^{-3}\) and a two-layer structure with \( N_{\text{drift}} \) of \( 1 \cdot 10^{16} \) cm\(^{-3}\) and an increased doping concentration of \( 1 \cdot 10^{17} \) cm\(^{-3}\) for the
topmost 200 nm of the drift region. This doping is added to reduce the assumed large resistance in the aperture region, which would dominate $R_{on}$ of the complete device. Fig. 4.2a shows the corresponding output characteristics at $V_{GS} = 0$ V. As expected, $R_{on}$ increases from higher to lower doping concentrations from 0.2 mΩ to 1 mΩ. The high $R_{on}$ prevents the saturation of $I_D$ for the two devices with the lowest $N_{drift}$.

As revealed by three-terminal breakdown simulations, depicted in Fig. 4.2b, also $V_{BR}$ is affected by $N_{drift}$, it reduces for increasing doping levels. Please note that a trap-free material was assumed for the breakdown simulations. A plot of $R_{on}$ over $V_{BR}$ is shown in Fig. 4.3 to quantify the optimal value of $N_{drift}$. Therefore, $R_{on}$ is extracted from the linear region of the output characteristic and $V_{BR}$ is taken at a current of 0.2 mA/cm². In addition, the $BFOM$ of GaN is plotted in the graph. The simulated values are below the ideal values, however, the best performance in terms of $R_{on}$ and $V_{BR}$ shows the sample with $N_{drift} = 5 \times 10^{16}$ cm⁻³. Its values are closest to the $BFOM$ curve.

(a) Output characteristics for different $N_{drift}$ at $V_{GS} = 0$ V.

(b) Three terminal breakdown analysis at $V_{GS} = -4$ V.

**Figure 4.2.** Influence of $N_{drift}$ on on- and off-state characteristics.

Figure 4.3.: Extracted $R_{on}$ and $V_{BR}$ for varied $N_{drift}$ in comparison to the $BFOM$ of GaN.
4.2. Channel doping

Next, $N_{\text{drift}}$ was kept constant at $5 \times 10^{16}$ cm$^{-3}$ and the doping concentration ($N_c$) of the 200 nm thick regrown channel was varied. The simulation comprised an unintentionally doped (UID) channel with an assumed n-type doping of $N_c = 1 \times 10^{13}$ cm$^{-3}$ and channels doped with $1 \times 10^{16}$ cm$^{-3}$, $5 \times 10^{16}$ cm$^{-3}$, and $1 \times 10^{17}$ cm$^{-3}$, respectively. $N_c$ will mainly influence the resistance of the vertical current flow and the pinch-off behavior of the transistor. The electrons have to pass through the low-doped channel layer leading to an increase of the series resistance with lower doping concentrations, as depicted in the output characteristics in Fig. 4.4a. Since the channel region is much thinner than the drift region, a change in $N_c$ does not have such a large influence onto $R_{on}$ as $N_{drift}$. From band diagram simulations, the influence of $N_c$ onto $n_S$ in the 2DEG was analyzed. With increasing $N_c$, the quantum well is dragged further below $E_F$ and $n_S$ is increased. An increase in $N_c$ from $1 \times 10^{16}$ cm$^{-3}$ to $1 \times 10^{17}$ cm$^{-3}$ leads to an increase in $n_S$ from $6.6 \times 10^{12}$ cm$^{-2}$ to $7.1 \times 10^{12}$ cm$^{-2}$. To separate the effects from the 2DEG and the underlying n$^-$-GaN channel onto the transistor characteristics, two different measures are introduced: in the following threshold voltage ($V_{th}$) denotes the depletion of the 2DEG ($n_S = 0$) and the pinch-off voltage ($V_p$) the depletion of the underlying n$^-$-GaN channel ($N_c = 0$). The transfer curves in Fig. 4.4b show a shift in $V_{th}$ to more negative values which corresponds perfectly to the higher $n_S$ according to Eq. 2.6. From the transfer characteristics in semi-logarithmic scale (Fig. 4.4b), $V_p$ can be evaluated. The shift in $V_p$ corresponds to the shift in $V_{th}$.

![Simulated output characteristic at $V_{GS} = 0$ V.](image1.png)

![Transfer characteristic in linear and semi-logarithmic scale.](image2.png)

**Figure 4.4.** Influence of different $N_c$ on the output and transfer characteristics.
Three-terminal breakdown simulations for $V_{GS} = -4$ V and $V_{DS}$ up to 800 V reveal an increasing drain leakage current with increasing $N_c$ (Fig. 4.5a). $R_{on}$ and $V_{BR}$ are plotted in Fig. 4.5b in comparison to the BFOM of GaN. The inset shows the values for $N_c = 1 \cdot 10^{17}$ cm$^{-3}$ which exhibited only very low $V_{BR}$. Values closest to the ideal ones exhibit the samples with lowly doped channels, in particular $N_c = 1 \cdot 10^{16}$ cm$^{-3}$.

4.3. Channel thickness

As a third parameter, the thickness of the regrown channel ($d_c$) was varied in the simulations. The values of $N_{drift}$ and $N_c$ were both $5 \cdot 10^{16}$ cm$^{-3}$. The simulation of $d_c$ requires some considerations beforehand. For thin channels, the 2DEG is located very close to the regrowth interface, which will, due to interface scattering, reduce $\mu$. In addition, it has to be taken into account that the channel will be partially depleted by the underlying p-GaN CBL. For a realistic p-type doping concentration of the CBL of $1 \cdot 10^{19}$ cm$^{-3}$ and an $N_c$ of $5 \cdot 10^{16}$ cm$^{-3}$, the ser will extend 250 nm in the channel. On the contrary, a thick channel will lead to a large negative $V_p$ and to additional leakage between source and drain. Consequently, $d_c$ of 100 nm, 200 nm and 300 nm were tested.

To analyze the impact of the underlying p-GaN layer onto the electron density, its distribution in the regrown channel in an unbiased state is plotted in Fig. 4.6a. For the thinnest, 100 nm thick channel, the electron distribution is narrow and the channel is, besides of the 2DEG, depleted. For a 300 nm channel, a broad distribution is
4.3. Channel thickness

(a) Electron density in the channel regions at zero voltage.

(b) Cross section of the structure. The electron density is plotted along the red-dashed line.

Figure 4.6.: Electron density in the n$^-$-GaN channel for different $d_c$.

observed. Furthermore, $n_S$ is increased for thicker channels. These effects are a direct consequence of the depletion from the underlying p-GaN CBL.

As expected, the simulated transfer characteristics (Fig. 4.7a) show a shift of $V_{th}$ to more negative voltages with increasing channel thickness corresponding to the increase in $n_S$ (Eq. 2.6). Also, an increase in $I_D$ is observed, which is accompanied by a reduction of $R_{on}$. From the semi-logarithmic transfer characteristics (Fig. 4.7a), a shift in $V_p$ is observed as well. This can be explained by the above mentioned different electron distributions in the channel. Furthermore, $V_{BR}$ is reduced for thicker channels, as three-terminal breakdown simulations for $V_{GS} = -4$ V show (Fig. 4.7b).

(a) Transfer characteristics in linear and semi-logarithmic scale.

(b) Three terminal breakdown analysis at $V_{GS} = -4$ V.

Figure 4.7.: Transfer and breakdown characteristics of different $d_c$. 

36
4.4. Overlap of gate and aperture

The influence of the length of the overlap between the gate contact and the p-doped CBL ($L_{GA}$) was simulated. Therefore, various $L_{GA}$ of 0 nm, 100 nm, 250 nm, 500 nm, 750 nm, and 1000 nm were applied. $L_{GA}$ is effectively the gate length of the device. The values of $N_{drift}$ and $N_c$ were both $5 \times 10^{16}$ cm$^{-3}$ and $d_c$ was 200 nm.

Transfer characteristics of devices with different $L_{GA}$ and $d_c = 200$ nm at $V_{DS} = 10$ V are depicted exemplary in Fig. 4.8a. With increasing overlap, $V_{th}$ shifts to more positive values, due to a better gate control over the 2DEG. Fig. 4.8b shows the dependence of $V_{th}$ on the overlap for two different $d_c$ of 200 nm and 300 nm and for two different $V_{DS}$ of 10 V and 100 V. $V_{th}$ shifts to more negative values for smaller $L_{GA}$. The shift is even more significant for thicker channels as well as for larger $V_{DS}$. This effect is denoted as the short-channel effect [24]. If the aspect ratio $L_{G}/d_c$ becomes smaller, the drain-induced field dominates over the gate-induced field. Hence, a larger $V_{GS}$ has to be applied to deplete the underlying channel. For these devices, $V_{th}$ starts to shift to negative values at an aspect ratio of $L_{GA}/d_c \geq \frac{250}{200} = 1.25$. In summary, a minimum aspect ratio of 1.25 is necessary to prevent short channel effects.

Furthermore, the application of larger $L_{GA}$ leads to lower off-state leakage currents and an increase in $V_{BR}$, as three-terminal breakdown simulations for $d_c = 200$ nm reveal (Fig. 4.9). Here, an $L_{GA}$ above 500 nm for a 200 nm thick channel is favorable.

![Figure 4.8.](image)

(a) Linear transfer characteristics. (b) $V_{th}$ in dependence of $L_{GA}$ for $d_c = 200$ nm and 300 nm and $V_{DS} = 10$ V and 100 V.

Figure 4.8.: Influence on transfer characteristics and $V_{th}$ of different $L_{GA}$.
4.5. Aperture length

Next, the influence of the aperture length \((L_{ap})\) was simulated. For \(N_{drift}\) and \(N_c\) again a value of \(5 \times 10^{16}\) cm\(^{-3}\) was applied. For \(d_c\) and \(L_{GA}\), 200 nm and 250 nm were employed, respectively.

For a too small aperture length \((L_{ap})\), two parasitic effects become dominant: the horizontal depletion of the aperture induced by the p-GaN and current crowding. Both effects lead to an increase in \(R_{on}\). To find a regime, in which \(L_{ap}\) does not influence the series resistance, \(R_{on}\) extracted from output characteristics is plotted over different \(L_{ap}\) (Fig. 4.10a). If the trend is extrapolated, \(R_{on}\) saturates at an \(L_{ap}\) of around 6 \(\mu m\). In addition, three terminal breakdown simulation show no increase in leakage current or reduced \(V_{BR}\) for larger \(L_{ap}\) (Fig. 4.10b).

Figure 4.10.: Simulations of on- and off-state behavior for different \(L_{ap}\).
4.6. Aperture geometry

Another degree of freedom as sketched in Process 3 (Fig. 3.11, p 27), is the aperture geometry. If the aperture is etched into the p-GaN, the etch angle can be adjusted, leading to either a steep, rectangular shape (as used in the simulations above) or a triangular shape (Fig. 4.11). Since the point of highest field is located at the aperture edge, the angle will influence the breakdown behavior. In this section, aperture geometries with different angles $\alpha$ of 36°, 45°, 50°, 60°, 70°, 80°, and 90° were simulated. Thereby, the aperture opening $L_{ap}$ was kept constant. Furthermore, in these simulations the gate overlapped the planar part of the aperture by a length of 1 $\mu$m. Consequently, $L_{GA}(\alpha)$ can be calculated with $L_{GA}(\alpha) = \frac{150 \text{ nm}}{\tan(\alpha)} + 1 \mu$m. As stated before, no influence from $L_{GA}$ onto leakage currents as well as $V_{BR}$ is expected for these values and a reasonable pinch-off behavior for all angles is ensured.

From the on-state characteristics, a slight decrease in $R_{on}$ and an increase in $I_D$ for smaller angles is deduced (not shown). This is mainly originated in the larger effective area of the channel.

The electrical field for $V_{GS} = -4 \text{ V}$ and $V_{DS} = 900 \text{ V}$ is plotted in Fig. 4.12 for $\alpha = 80^\circ$, 60°, and 10°, respectively. For larger angles, the maximum electrical field ($E_{max}$) is located at the steep edge of the CBL, whereas for angles of about 60° it is equally distributed below the CBL and at the edge. For a small angles of 10°, $E_{max}$ is located beneath the CBL. Furthermore, the maximum electric field is reduced for the latter.

The dependence of $E_{max}$ on the aperture angle is plotted in Fig. 4.13. The same behavior as for a pn-junction with a negative bevel angle is revealed [21], for small angles, a very low electric field is observed, which first increases for larger angles to a maximum and decreases again. The particular shape of the curve is dependent on the doping concentrations and dielectric constant.

From these simulations, an improvement in $V_{BR}$ for smaller angles can be expected.

Figure 4.11.: Triangular (top) and rectangular (bottom) aperture geometry. The aperture length $L_{ap}$ is kept constant.

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As a consequence of the applied breakdown model, the values of $E_{max}$ exceed $E_{crit}$ for GaN.
4.6. Aperture geometry

Figure 4.12.: Simulation of the electrical field for $V_{GS} = -4\, V$ and $V_{DS} = 900\, V$ for different $\alpha$ of $80^\circ$, $60^\circ$ and $10^\circ$.

Figure 4.13.: $E_{\text{max}}$ in dependence of the aperture angle at $V_{GS} = -4\, V$ and $V_{DS} = 900\, V$.

for a sufficiently large $L_{GA}$ which overlaps the major part of the aperture. Otherwise, severe leakage currents will arise.

The comprehensive simulations of growth- and mask-related parameters reveal starting points for the following experiments. With values of $N_{\text{drift}}$ and $N_c$ in the lower $10^{16}\, \text{cm}^{-3}$ range, the best results concerning $BFOM$ were predicted. Furthermore, $d_c$ should be in the order of 200 nm. To prevent short-channel effects, for a 200 nm thick channel, at least an $L_{GA}$ of 250 nm is necessary. Furthermore, $L_{ap}$ should be larger than 6 $\mu$m to obtain optimal $R_{on}$. Shallow aperture angles are preferable, to reduce the maximum electrical field and thus increase $V_{BR}$.

Based on the structure in Fig. 4.1 and with the deduced parameters, devices with
low $R_{on}$ below 0.3 mΩ cm$^2$ and $V_{BR}$ above 800 V are expected. However, particularly for the breakdown behavior, ideal conditions were applied, e.g. trap-free material was assumed. For this reason, lower $V_{BR}$ are expected for real devices. Whereas achieving values of $R_{on}$ below 1 mΩ cm$^2$ is reasonable. In addition, it is expected to reproduce trends such as the influence of $L_{ap}$ and $L_{GA}$ on the on-state and reverse characteristics.
5. Building blocks of a vertical transistor

The fabricating process a VHFET consists of different building blocks, which can be considered and optimized separately from each other. A schematic of the processes, containing the different steps, is depicted in Fig. 3.11 on page 27.

The following steps will be specifically addressed in the course of this chapter:

1. Since insulating sapphire substrates were used for this work, backside ohmic contacts cannot be implemented. Therefore, an etch process of the n$^-$-GaN for the fabrication of quasi-vertical devices is developed.

2. To optimize the competing parameters $V_{BR}$ and $R_{on}$, a suitable vertical drift-zone, consisting of an n$^-$-GaN layer, is designed.

3. To prevent the direct current flow from source to drain, a current blocking layer (CBL) is used. Here, a p-doped layer is applied. Hence, a suitable pn junction for current blocking is developed.

4. In order to form the 2DEG on top of the CBL and the aperture, epitaxial regrowth consisting of AlGaN/GaN has to be performed. Therefore, regrowth with MOCVD and MBE is investigated and optimized. For Process 2 and Process 3 (Fig. 3.11, p. 27), the CBL is either selectively regrown or the aperture is etched into the p-GaN. Consequently, the regrowth on textured and masked templates is investigated.

In the following, both lateral and vertical transistors, as well as diodes are processed and characterized. Methods for surface and topology characterization, such as atomic force microscopy (AFM) [91] and scanning electron microscopy (SEM) [92] were applied. Electrical characterization was amongst other performed by current voltage (IV) and CV measurements [8, 26]. The transistors were characterized via input, output and transfer characteristics [7].
5.1. Quasi-vertical devices

Due to the currently still limited availability of native GaN substrates, sapphire was used as substrate material in this work. Its insulating behavior prohibits contacting the wafer from the backside. For this reason, only quasi-vertical diodes and transistors are processed (Fig. 5.1). The backside ohmic contact is emulated by an n⁺-GaN layer at the bottom of the structure. The access to these layers is achieved by etching the top layers.

ICP etch The large binding energies between Ga and N atoms of 8.92 eV/atom [93] result in a high chemical stability of GaN against bases and acids. Nevertheless, a dry etching process with inductively coupled plasma (ICP) reactive ion etching (RIE) has been proven to be an adequate choice to etch GaN [94, 95]. For a suitable etch process, several requirements have to be fulfilled: mesa structures or deeply etched vertical devices require a reasonably high etch rate, which yields a controllable process. Moreover, a mask material should be available, which offers sufficient selectivity in comparison to the sample material. Finally, the etching process should yield smooth surface and sidewalls. In general, ICP etching fulfills these conditions. The chemical and physical etching components can be adjusted separately, leading to a large flexibility in terms of the etch profiles [94].

Process As a starting point, an etching process with a low RF power of 50 W, corresponding to a dc bias ($V_{dc}$) of -72 V, was used which yielded an etch rate of 200 nm/min [96]. However, only shallow mesa sidewalls with an angle of 70° were achieved and columnar defects remained at the etched surface (Fig. 5.2a). These defects, spread continuously over the sample surface, were partially as high as the etch depth (1-4 µm).

![Figure 5.1: Schematic cross-sectional view of a quasi-VSD.](image)
5.1. Quasi-vertical devices

(Fig. 5.2b) and prohibited the continuation of the process. Most likely, the surface columns arise from dislocations in GaN. During the etch process, impurities from the hardmask, coverplate or etched material preferentially adsorb at these dislocations. This decoration or micro-masking leads to a decreased etch rate [97, 98].

The decorated defects were chemically stable, they could neither be etched with potassium hydroxide (KOH) nor with higher ICP power. Therefore, an etch process with higher $V_{dc}$ and consequently higher physical etch component was developed [99]. Here, $V_{dc}$ is increased from -72 V to -250 V. Further relevant parameters are listed in Tab. 5.1. The higher $V_{dc}$ results in a smoother surface and nearly all defects are etched (Fig. 5.2c). Mesa sidewalls of 4 $\mu$m are realized with an angle of 90° (Fig. 5.2d). As an appropriate mask material, chromium (Cr) was applied. It offers a selectivity of about 1:25 (Cr:GaN) and therefore, a good pattern transfer from the mask to the
5.2. Drift region

In a VSD or VHFET, the drift region is not only responsible for defining $V_{BR}$, but it also contributes to $R_{on}$. The most influential parameter on these two quantities is the donor concentration ($N_D$). With higher doping, $R_{on}$ as well as $V_{BR}$ will decrease (Sec. 4.1). For a targeted $V_{BR}$, the minimum $R_{on}$ is determined by the $BFOM$. To quantify the applied material and to find an optimal layer stack and process, quasi-VSD with different doping levels were processed as test vehicles (Fig. 5.1).

As a starting point, a drift region with a thickness of 4 $\mu$m was used. From Eq. 3.1, a blocking voltage up to 300 V for $N_D$ of $2 \times 10^{16}$ cm$^{-3}$ was derived. This would yield a maximum field of 1.5 MV/cm, still far below $E_{crit}$.

**Process** GaN layers were grown on c-plane sapphire with MOCVD. The growth started with a GaN nucleation layer and a 2 $\mu$m UID GaN buffer layer, followed by a 2 $\mu$m highly doped n$^+$-GaN layer ($N_D = 1 \times 10^{18}$ cm$^{-3}$). This layer will serve as a backside contact layer for the quasi-vertical diode. The growth continued with the drift region. 4 $\mu$m thick n$^-$-GaN layers with varying doping levels ranging from UID to $1.2 \times 10^{17}$ cm$^{-3}$ were deposited (Tab. 5.2). Quasi-vertical diodes were etched as it was described in Sec. 5.1. Ohmic contacts consisting of Ti/Al/Ni/Au (15 nm/1000 nm/40 nm/50 nm) were deposited via e-beam evaporation. Subsequently, the contacts were annealed at 825 °C in N$_2$ atmosphere for 30 s. Ohmic contacts with specific contact resistance ($\rho_C$) of $5 \times 10^{-6}$ $\Omega$cm$^2$ were achieved. On top of the mesa, Ni/Au (50 nm/200 nm) Schottky contacts were evaporated and annealed at 400 °C in air [60].

**Diode Characterization** CV measurements performed at 1 MHz confirm the doping levels (Fig. 5.3a). The $1/C^2$ plot shows a linear dependence on voltage and therefore, a homogeneous doping concentration throughout the profiled depth (Eq. 3.11). The

<table>
<thead>
<tr>
<th>BCl$_3$</th>
<th>Cl$_2$</th>
<th>N$_2$</th>
<th>ICP power</th>
<th>$V_{dc}$</th>
<th>pressure</th>
<th>temperature</th>
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<td>32 sccm</td>
<td>5 sccm</td>
<td>300 W</td>
<td>-250 V</td>
<td>0.5 Pa</td>
<td>12°C</td>
</tr>
</tbody>
</table>

Table 5.1.: ICP-RIE parameters for etching quasi-vertical devices.

etched structure. The full process exhibits an etch rate of 500 nm/min and sidewalls of roughly 90°. Also the surface is sufficiently smooth to deposit the backside ohmic contacts.
capacitance for the sample with the low carrier concentration of \(8.0 \times 10^{15} \text{ cm}^{-3}\) is close to the detection limit of the measurement setup. Accordingly, the \(1/C^2\) curve is rather noisy. The carrier concentration of the UID sample was too low to be determined. For this sample, the \(n^{+}\)-GaN is already depleted at very low reverse voltages. From Eq. 3.12, \(\Phi_B\) is extracted. The values are about 0.81 - 0.86 eV and are summarized in Tab. 5.2.

The impact of the doping concentration is further reflected in the IV characteristics (Fig. 5.3b). From the forward characteristics, the ideality factor \((n)\) is calculated with Eq. 3.4. The three highest intentionally doped samples exhibit \(n\) close to unity, indicating the dominance of thermionic emission and only little voltage dependence of \(\Phi_B\). A slight increase from 1.01 to 1.04 for higher doping levels is detected. The lowest doped sample already shows a decreased forward current and an ideality factor \((n)\) of 1.2, which is possibly due to the inhomogeneous distribution of Schottky barrier heights [100].

<table>
<thead>
<tr>
<th>(N_D) [(\text{cm}^{-3})]</th>
<th>(n)</th>
<th>(\Phi_B) (IV) [eV]</th>
<th>(\Phi_B) (CV) [eV]</th>
<th>(R_{on}) [(\text{m}\Omega \text{cm}^2)]</th>
</tr>
</thead>
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<tr>
<td>(1.2 \times 10^{17})</td>
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<td>0.76</td>
<td>0.81</td>
<td>0.80</td>
</tr>
<tr>
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<td>0.78</td>
<td>0.82</td>
<td>0.87</td>
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<tr>
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<td>0.80</td>
<td>0.86</td>
<td>1.05</td>
</tr>
<tr>
<td>(8.0 \times 10^{15})</td>
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<td>460</td>
</tr>
<tr>
<td>UID</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>985</td>
</tr>
</tbody>
</table>

Table 5.2.: Summary of extracted values of the forward characteristics of VSD with various \(N_D\).
The extracted $\Phi_B$ of 0.8 eV, for the Ni/Au contact is reasonable, it decreases to 0.76 eV for higher $N_D$ (Tab. 5.2). No reasonable values for $n$ and $\Phi_B$ could be extracted for the UID sample. The $\Phi_B$ extracted from CV are systematically about 0.05 eV higher than those extracted from the IV characteristics. The higher values obtained by CV measurements can be explained by the fact that the CV measurement is less sensitive to the contribution of low barrier-height regions, whereas forward current measurements naturally include the leakage contribution of these regions affecting the extracted barrier height more severely.

As $R_{on}$ is inversely dependent on $N_D$ (Eq. 2.2), it decreases with increasing $N_D$. Values of 1 m$\Omega$cm$^2$ for the sample with $N_D = 2.2 \times 10^{16}$ cm$^{-3}$ were obtained. The value slightly decreases with increasing $N_D$. However, the sample with $N_D = 8.0 \times 10^{15}$ cm$^{-3}$ shows a large $R_{on}$ of 460 m$\Omega$cm$^2$, which is further doubled to 985 m$\Omega$cm$^2$ for the UID sample. For these low doped samples, the current is limited by the low concentration of free carriers.

In the reverse direction of the IV characteristic, a steady reduction of the leakage current with decreasing $N_D$ is observed. The reverse leakage current decreases about four orders of magnitude by reducing $N_D$ from $1.2 \times 10^{17}$ cm$^{-3}$ to $8.0 \times 10^{15}$ cm$^{-3}$. The reverse biased diode is characterized further to gain information on the mechanisms generating the leakage currents. Therefore, temperature-dependent IV (IVT) characteristics were measured in a range from $T_R$ to 250 $^\circ$C and the electrical field (E) in reverse direction is evaluated for each temperature. Exemplary, an IVT measurement and the corresponding I/E plot for $N_D = 1.2 \times 10^{17}$ cm$^{-3}$ are shown in Fig. 5.4.

![Figure 5.4: IVT-analysis of VSD with different $N_D$.](image)

(a) Temperature dependent IV characterization.

(b) Analysis of reverse characteristics in a Frenkel-Poole plot.
A linear dependence is observed when plotting $\log(1/E)$ over $E^{0.5}$ (Fig. 5.4b). This is a good indication for a Frenkel-Poole emission \[101\]. For this field-enhanced emission, the following applies:

$$\log(1/E) = \frac{q}{kT} \sqrt{\frac{qE}{\pi \varepsilon_0 \varepsilon_r}} \frac{q\Phi_T}{kT} \frac{1}{b(T)} + \log(C) \quad (5.1)$$

with $\Phi_T$ as barrier height for the emission from the trap state. The trap barrier height in reference to the conduction band can be calculated by plotting the $y$-axis intercept $b(T)$ for each temperature over $1/T$. From the slope, $\Phi_T$ can be extracted. In Fig. 5.5, $b(T)$ is plotted for three different doping concentrations. The slope is similar for all doping concentrations, and $\Phi_T = 0.5 \pm 0.3 \text{eV}$ is extracted. This trap is mainly attributed to a charged impurity, e.g., an N antisite \[102, 103\]. In conclusion, leakage currents are caused by Frenkel-Poole emission from a trap state, e.g., an N antisite, near the metal semiconductor into a continuum of states, probably induced by dislocations \[101, 104\].

![Figure 5.5: Plot of b(T) to analyze the trap barrier height.](image)

**Breakdown** To quantify the influence of $N_D$ onto $V_{BR}$, breakdown measurements were performed (Fig. 5.6a). A systematic increase of breakdown voltage with lower doping concentration is observed (Tab. 5.3). For the sample with $N_D = 2 \cdot 10^{16} \text{cm}^{-3}$, the calculated $V_{BR}$ of 300 V is proven reasonable. The dependence of $V_{BR}$ and $N_D$ is plotted in Fig. 5.6b (rectangles). For the first three samples, the relation of $V_{BR}$ and $N_D$ follows well the dependence

$$V_{Br} \propto \frac{1}{N_D^{3/4}} \quad (5.2)$$

predicted by Trivedi *et al* \[105\], since $V_{BR}$ plotted over $\frac{1}{N_D^{3/4}}$ shows a linear behavior (Fig. 5.6b). However, for the low doped sample, the slope changes and $V_{BR}$ saturates. This can be explained if the width $w$ of the scr at $V_{BR}$ is taken into account, according
to Eq. 3.1, the scr at $V_{BR}$ is [8]:

$$w(V_{BR}) = \sqrt{\frac{2e\varepsilon_0}{qN_D} (V_{BR} + V_{Bi})}$$  \hfill (5.3)

with $V_{Bi}$ as the built-in potential. For the lowest doping concentration, the scr would be 7 $\mu$m which is more than the real thickness of the n$^-$-GaN layer of 4 $\mu$m, causing an early breakdown, due to an enhanced increase in $E_{max}$. Therefore, two thicker samples with 8 $\mu$m of n$^-$-GaN ($N_D = 8 \times 10^{15}$ cm$^{-3}$ and $N_D = 2 \times 10^{15}$ cm$^{-3}$) were fabricated. The higher doped one exhibits a $V_{BR}$ of 500 V, which would result in a scr width of 8.4 $\mu$m. Here, the scr is comparable to the drift region of 8 $\mu$m length. Plotting these results into Fig. 5.6b (star), they fit well with the linear dependence. Since the scr fully extends over the n$^-$-GaN thickness, the lower doped, 8 $\mu$m thick sample also breaks down at around 500 V. Consequently, no improvement in $V_{BR}$ is generated with the lower doping in this case. From $V_{BR}$ and $w$, $E_{crit}$ can be calculated with [106]

$$E_{crit} = \frac{2(V_{BR} + V_{Bi})}{w}$$  \hfill (5.4)

The extracted data in Tab. 5.3 show that $E_{crit}$ is around 1.3 MV/cm to 2.3 MV/cm, still below the theoretical value of 3.3 MV/cm [7]. The UID sample exhibits the highest $E_{crit}$, but this is obtained at the costs of a high $R_{on}$. The extracted data are summarized in Tab. 5.3.

![Graph a](image1.png)

**Figure 5.6.** Analysis of the breakdown characteristics of VSD with drift regions of different $N_D$ and thickness.
5.2 Drift region

Nucleation

Based on the results from the doping series, VSD with two different nucleations were tested to evaluate their influence onto \( V_{BR} \) or precisely \( E_{\text{crit}} \). Instead of a GaN nucleation (as used for the samples above), an AlN nucleation on sapphire was used as a starting layer. Due to oxygen impurity diffusion from the sapphire substrate, GaN layers exhibit an unintentional n-type doping. With an AlN nucleation and buffer, this oxygen reacts with the Al and reduces the oxygen concentration in the upper layers [107]. Hence, the amount of residual oxygen donors in GaN is reduced. Furthermore, an AlN nucleation should reduce the defect density [108].

The IV characteristics of two diodes with GaN and AlN nucleation layer, both with doping levels of about \( 2 \cdot 10^{16} \text{ cm}^{-3} \), show very similar forward characteristics. However, for the AlN nucleation, already a small decrease of reverse leakage current is observed (Fig. 5.7a). This is also reflected in the breakdown characteristics (Fig. 5.7b). Here, samples with AlN nucleation indeed show an improved breakdown behavior compared to a sample with GaN nucleation. The breakdown voltage is enhanced from 130 V to 175 V. But still, a further optimization of the process is required to enhance \( V_{BR} \). For example edge terminations and passivation can be applied [63, 77].

Table 5.3.: Summary of breakdown characteristics for VSD with various drift regions.

<table>
<thead>
<tr>
<th>( N_D ) [cm(^{-3})]</th>
<th>( d ) [( \mu \text{m} )]</th>
<th>( R_{on} ) [m( \Omega \text{cm}^2 )]</th>
<th>( V_{BR} ) [V]</th>
<th>( w ) [( \mu \text{m} )]</th>
<th>( E_{\text{crit}} ) [MV/cm]</th>
<th>BFOM [MW/cm(^2)]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2 ( \cdot ) 10(^{17} )</td>
<td>4</td>
<td>0.80</td>
<td>50</td>
<td>0.638</td>
<td>1.43</td>
<td>2.65</td>
</tr>
<tr>
<td>6.0 ( \cdot ) 10(^{16} )</td>
<td>4</td>
<td>0.87</td>
<td>110</td>
<td>1.278</td>
<td>1.52</td>
<td>9.27</td>
</tr>
<tr>
<td>2.2 ( \cdot ) 10(^{16} )</td>
<td>4</td>
<td>1.05</td>
<td>230</td>
<td>3.439</td>
<td>1.33</td>
<td>50.45</td>
</tr>
<tr>
<td>8.0 ( \cdot ) 10(^{15} )</td>
<td>4</td>
<td>460</td>
<td>350</td>
<td>4.0</td>
<td>1.74</td>
<td>0.26</td>
</tr>
<tr>
<td>8.0 ( \cdot ) 10(^{15} )</td>
<td>8</td>
<td>1590</td>
<td>500</td>
<td>8.0</td>
<td>1.24</td>
<td>0.16</td>
</tr>
<tr>
<td>2.0 ( \cdot ) 10(^{15} )</td>
<td>8</td>
<td>1670</td>
<td>550</td>
<td>8.0</td>
<td>1.37</td>
<td>0.18</td>
</tr>
<tr>
<td>UID</td>
<td>4</td>
<td>985</td>
<td>460</td>
<td>4.0</td>
<td>2.29</td>
<td>0.21</td>
</tr>
</tbody>
</table>

So far, the samples suffer from premature breakdown. This is probably related to the "poor" material quality, which is originated in the growth on sapphire substrates. The best ratio considering \( R_{on} \) and \( V_{BR} \) was reached with a \( N_D \) of 2.2 \( \cdot \) 10\(^{16} \text{ cm}^{-3} \). For this sample, a BFOM of 50 MW/cm\(^2\) was yielded. This result is in good agreement with the simulation in Sec. 4.1, which showed the best performance for \( N_D = 5 \cdot 10^{16} \text{ cm}^{-3} \).

\(^1\)Note that the breakdown voltage for this series was measured in dc mode, therefore the device was stressed for longer times, which leads to increased leakage and reduced \( V_{BR} \) [109].
5.3. Current blocking layer

(a) IV curves of VSD with GaN and AlN nucleation.

(b) Comparison of $V_{BR}$ of samples with GaN and AlN nucleation.

Figure 5.7.: Analysis of the electrical properties of VSD with GaN and AlN nucleation.

<table>
<thead>
<tr>
<th>Nucleation</th>
<th>$R_{on}$ [mΩcm$^2$]</th>
<th>$V_{BR}$ [V]</th>
<th>$w$ [μm]</th>
<th>$E_C$ [MV/cm]</th>
<th>$BFOM$ [MW/cm$^2$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN</td>
<td>1.1</td>
<td>130</td>
<td>2.58</td>
<td>1.0</td>
<td>15.36</td>
</tr>
<tr>
<td>AlN</td>
<td>1.3</td>
<td>175</td>
<td>3.0</td>
<td>1.16</td>
<td>23.56</td>
</tr>
</tbody>
</table>

Table 5.4.: Summary of breakdown characteristics for VSD with GaN and AlN nucleation.

The AlN nucleation yields a higher breakdown field compared to the GaN nucleation. This is most probably related to the reduction of donors and defects. The $BFOM$ of 23 MV/cm$^2$ for the AlN nucleation sample is about 1.5x higher than for the sample with GaN nucleation.

In summary, the following samples with drift region always use an AlN nucleation and a doping concentration of $2.0 \cdot 10^{16}$ cm$^{-3}$, which yielded the highest $BFOM$.

5.3. Current blocking layer

As described in Sec. 3.2, a current blocking layer (CBL) is required to guide the current from the top source contacts towards the bottom drain contact underneath the gate and to prevent a direct current flow from source to drain. One possible realization of a CBL is to employ a buried p-GaN layer and hence, to make use of the reverse operating diode. In a CAVET, ground potential is applied to the p-GaN layer and a positive voltage to the adjacent n-GaN drift layer. Hence, the diode is biased in reverse direction.
The p-GaN layer can either be formed by direct growth of a Mg-doped GaN layer or by Mg implantation. In this work, the use of a p-doped layer is investigated. Therefore, the behavior of a simple pn diode was characterized first. A good insulating behavior of the scr with low leakage currents, resulting in a large $V_{BR}$, is targeted. As stated in Sec. 5.2, a reasonable $N_D$ for an n-GaN drift region concerning $R_{on}$ and $V_{BR}$ is in the lower $10^{16}$ cm$^{-3}$ region. In order to obtain a high $V_{BR}$, an acceptor concentration of $1\cdot10^{19}$ cm$^{-3}$ was targeted for the abrupt p$^+$n$^-$ junction. As mentioned in Sec. 2.4.3, only 1% of the Magnesium is activated, resulting in a required $N_A$ of $1\cdot10^{19}$ cm$^{-3}$. This is close to the maximum $N_A$, which can be reached with MOCVD [41].

In a pn junction, the expansion $d$ at zero bias of the scr into the n- or p-region can be calculated with

$$d_n = \sqrt{\frac{2\varepsilon_r \varepsilon_0 U_D}{q} \frac{N_A/N_D}{N_A + N_D}}$$
and

$$d_p = \sqrt{\frac{2\varepsilon_r \varepsilon_0 U_D}{q} \frac{N_D/N_A}{N_A + N_D}}. \tag{5.5}$$

For $N_D = 5\cdot10^{16}$ cm$^{-3}$ and $N_A = 1\cdot10^{19}$ cm$^{-3}$, the scr reaches approximately 250 nm into the n-GaN and 0.8 nm into the p-GaN. Thus, in further argumentation, the expansion into the p-GaN layer is neglected.

**Process** A diode with these doping levels was processed as depicted in Fig. 5.8. A 700 nm n$^-$-GaN layer was grown on top of an n$^+$-GaN ohmic contact layer. This was followed by a 250 nm thick p-GaN layer. The structure was etched as described in Sec. 5.1 to obtain access to the n$^+$-GaN layer. Ti/Al/Ni/Au n-contacts were deposited and subsequently annealed at 825°C in N$_2$ ambient. Finally, p-contacts consisting of Ni/Au (7 nm/12 nm) were evaporated onto the p-GaN layer on top of the mesa. These were annealed at 495°C in an N$_2$/O$_2$ atmosphere.

![Figure 5.8: Cross section of a pn diode.](image)
5.3. Current blocking layer

**Characterization** First, the hole concentration of the p-GaN layer was verified with Hall measurements, assuming that the space charge region is insulating, and the n-GaN layer underneath does not contribute to the current [26, p. 474]. Here, p-contacts on the top surface were used. As intended, a concentration of $p = 1.3\cdot10^{17}\text{ cm}^{-3}$, which corresponds to $N_A \approx 1.3\cdot10^{19}\text{ cm}^{-3}$ for $w_A = 200\text{ meV}$, was achieved with a mobility of 20 cm$^2$/Vs.

Subsequently, CV measurements on large-area diodes at 1 MHz on a structure as depicted in Fig. 5.8 were performed to obtain the carrier profile of the n-GaN layer (Eq. 3.11). As discussed before, the scr will mainly extend into the n-GaN layer, hence $N_D$ or in the case of Si, $n$ can be extracted. The derived carrier density profile is shown in Fig. 5.9a. $N_{CV}$ increases linearly from $4.8\cdot10^{16}\text{ cm}^{-3}$ to $6\cdot10^{17}\text{ cm}^{-3}$. The extracted space charge region width of 290 nm at 0 V corresponds well to the calculated width from Eq. 5.5.

Next, IV analysis was performed (Fig. 5.9b). Very low reverse leakage currents of $10^{-8}\text{ mA/cm}^2$ are observed. For the on-state, two regions are identified by calculating the ideality factor ($n$). At lower currents, for $n = 2$, the current is dominated by scr recombination. For higher currents, a high-injection (hi) region is detected, also characterized by $n = 2$ [8].

Breakdown measurements of various pn junctions reveal a $V_{BR}$ of 140 V. The theoretical width of the scr for $N_D = 4.8\cdot10^{16}\text{ cm}^{-3}$ is about 1.8 μm at this voltage. If it is assumed that the scr only expands into the lower doped n-GaN region, this width

**Figure 5.9.** Profile of $N_{CV}$ of the n$^-$-GaN layer and IV measurement of the pn diode.
Figure 5.10.: Breakdown characteristics for several pn diodes.

<table>
<thead>
<tr>
<th>$R_{on}$ [mΩcm$^2$]</th>
<th>$V_{BR}$ [V]</th>
<th>$w$ [μm]</th>
<th>$E_C$ [MV/cm]</th>
<th>$BFOM$ [GW/cm$^2$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.4</td>
<td>140</td>
<td>1.8 &gt;0.7</td>
<td>2.0</td>
<td>5.76</td>
</tr>
</tbody>
</table>

Table 5.5.: Summary of the extracted values for the designed pn diode.

would exceed the real thickness of the n-GaN of 700 nm. To calculate the breakdown field only the thickness of the n$^+$-GaN layer of 700 nm is considered, leading to $E_C = 2$ MV/cm.

In conclusion, the use of a pn diode appears suitable for the application as a current blocking layer in a vertical transistor. In a CAVET, for the upper pn junction both, p- and n-, layers will be set to zero volt, leading to a small scr. Whereas, the lower pn junction will be biased in reverse direction, blocking the applied voltage. A single pn diode exhibited leakage currents below $10^{-4}$ A/cm$^2$ up to 40 V and a breakdown voltage of 140 V.

5.4. Regrowth

To realize e.g. a CAVET, selective regrowth of different layers is an essential tool. As shown in Fig. 3.11, various regrowth steps occur in the different process routes of a CAVET. These are summarized in the following

- For Process 1, a full-area regrowth of an AlGaN/GaN heterostructure on a Mg-implanted template is necessary as depicted in Fig. 5.11a.

- For Process 2, a selective regrowth of a p-GaN layer is necessary. Parts of the sample are thereby covered with a mask (Fig. 5.11b).
• For Process 3, the regrowth of AlGaN/GaN on a partly etched and textured template has to be performed as shown in Fig. 5.11c.

For a successful regrowth, several requirements apply: the regrown layer should offer a high crystal quality and a smooth surface. For a selective regrowth, as in Process 2, the material should only grow in the designated regions. Much attention has to be paid to the interface of the regrown layer and the template. A conductive channels caused by defects can affect the device properties, hence, a clean and insulating interface is desired.

To investigate the regrowth comprehensively, in this section, the regrowth on five different templates with MOCVD and MBE is performed. The templates are depicted in Fig. 5.12. First, the MOCVD regrowth on a bare GaN template is investigated to gain information on the influences from the regrowth itself [111]. Second, the MOCVD regrowth on a template with a dry-etched surface is performed. This should simulate the impact of a regrowth on an etched trench sidewall. For both cases, special focus is laid on the characterization of the regrowth interface. Third, the difficulties of a regrowth on p-doped GaN layers are elucidated and different approaches, including growth with MOCVD and MBE, are examined. Fourth, the regrowth of MOCVD and MBE GaN on a textured template is performed. Last, a masked template is used for a selective regrowth.

![Figure 5.11: Three different regrowth steps appearing in the process routes of a CAVET. The regrown layers are depicted in color and enclosed in dotted lines.](image-url)
5.4.1. Regrowth on a GaN template

In order to investigate the influence of the regrowth onto the device properties separately from other effects, at first, the MOCVD regrowth of an AlGaN/GaN heterostructure on an as-grown GaN template is investigated (Fig. 5.12).

**Processing** Two samples were prepared to characterize the properties of a regrown layer (Fig. 5.13): a continuously grown HFET, which serves as a reference sample, was processed, as well as an HFET regrown on a GaN template. Nominally, the structure of both samples is the same: the MOCVD growth was started with an AlN nucleation on sapphire, continued by a 4 $\mu$m thick undoped GaN buffer. For the regrown sample, the growth was interrupted here, and the sample was taken out of the reactor and stored in air for several days. To obtain a clean interface, before regrowth, the sample was dipped in hydrochloric acid (HCl) and buffered oxide etch (BOE) for 1 min each and rinsed in deionized water for 5 min thereafter [112]. The top layers of the continuously grown HFET as well as the regrown layers consisted of a 200 nm thick undoped GaN channel and a 25 nm thick Al$_{0.25}$Ga$_{0.75}$N barrier layer. To extract only the influence of the regrowth interface, the GaN channel is in both cases undoped.

For further characterization, lateral transistors were fabricated. Both samples were processed with the following process: the mesa was etched with a boron trichloride (BCl$_3$)-based ICP process. Subsequently, ohmic contacts of Ti/Al/Ni/Au were deposited via e-beam evaporation and annealed for 30 s at 825 °C in nitrogen atmosphere. The Ni/Au gate contact was deposited thereafter.

**Morphology** To evaluate the influence of the regrowth on the morphology, AFM images (5 $\mu$m x 5 $\mu$m) of the surfaces of the continuously grown HFET and the regrown HFET were compared (Fig. 5.14). Both samples exhibit low root mean square (rms) roughnesses of 0.76 nm and 0.82 nm, respectively, indicating no significant influence
5.4.1. Regrowth on a GaN template

Figure 5.13.: Schematic of the samples for the investigation of regrowth effects. 200 nm undoped GaN and 25 nm AlGaN were regrown.

from the regrowth on the surface morphology.

2DEG Next, the influence of the regrowth on the 2DEG properties was investigated. To gain information about $\mu$ and $n_S$, Hall measurements at room temperature (293 K) and 77 K were performed (Fig. 5.15). The plot shows measurements from several devices on the sample. The continuously grown sample exhibits a $\mu$ of 2000 cm$^2$/Vs at room

Figure 5.14.: Comparison of surface morphology with AFM induced by the regrowth.

(a) AFM image of a continuously grown HFET.

(b) AFM image of a regrown HFET on a GaN buffer.
Figure 5.15.: Hall measurements at room temperature and 77 K.

temperature, in contrast to the regrown sample with a $\mu$ of 1400 cm$^2$/Vs. At 77 K, the mobility is doubled for both samples, however, the trend remains. The reduction of mobility for the regrown sample can be attributed to effects related to the interface, such as different interface roughnesses or scattering at ionized impurities. Other scattering mechanisms are frozen out at 77 K [113, 114]. Even though AFM images did not show an increased roughness of the surface, the regrowth interface may be rougher and charged defects, limiting the electron mobility, could be present. Regarding $n_s$, only a slight difference is detected. This can probably be attributed to a different Al content in the barrier. As expected, no change in $n_s$ from 293 K to 77 K is monitored [114].

**Buffer** To characterize the buffer, which also includes the regrown GaN for the regrown HFET, the current between two isolated mesas was measured. Therefore, the material between two ohmic contacts was etched down by about 80 nm. A schematic of such a mesa-isolation test structure is depicted in Fig. 5.16a. The measurements of several devices on one sample are depicted in Fig. 5.16b. The mesa isolation for the continuously grown HFET is excellent. Only very low currents in the nA-regime up to 100 V are measured. The leakage current of the regrown sample is more inhomogeneously distributed and evidences an increased buffer leakage. This is most likely caused by inferior crystal quality and a possible horizontal leakage path at the regrowth interface which is also indicated in the schematic.
5.4.1. Regrowth on a GaN template

(a) Schematic of a test structure for mesa isolation measurements.

(b) Mesa isolation measurements up to 100 V.

Figure 5.16: Mesa isolation measurements of a continuously grown HFET compared to a regrown HFET.

DC characteristics Transfer characteristics of both samples are depicted in semi-logarithmic scale in Fig 5.17. Measurements of various transistors with $L_C = 1 \mu m$ are plotted. The differences in the off-state leakage currents are most significant. The reference HFET shows pinch-off with currents from the $\mu A/mm$ range down to the nA/mm range, whereas the regrown HFET shows higher leakage currents of 10$\mu A/mm$, but

Figure 5.17: Transfer characteristics of the continuously grown HFET (left) and the regrown HFET (right) for several devices.
also a single device with currents as low as 8 nA/mm. Even though, both transistors exhibit an inhomogeneous off-state leakage distribution, the leakage currents of the regrown sample are mostly larger than for the continuously grown sample. As Fig. 5.17 shows, the gate leakage currents are the main source for the off-state leakage. This allows the conclusion that primarily the quality of the gate-semiconductor interface, and therefore the material quality, is responsible for the increased leakage rather than the leakage of the regrowth interface. Due to higher $n_S$, the reference sample has a more negative $V_{th}$ of -5 V and higher maximum drain current ($I_{D,max}$) of 530 mA/mm than the regrown sample with $V_{th}$ of -3 V and $I_{D,max}$ of 370 mA/mm.

**Dynamic characteristics** The dynamic behavior of the devices was tested with a dynamic IV analysis (DIVA). Both samples were passivated with a SiN passivation layer. Pulsed measurements were performed from a quiescent bias point of $(V_{GS}, V_{DS}) = (0 \, \text{V}, \, 0 \, \text{V})$ (non-stressed), of $( -12 \, \text{V}, \, 0 \, \text{V})$ (gate lag), and of $( -12 \, \text{V}, \, 15 \, \text{V})$ (drain lag). The pulses were 0.2 $\mu$s long and the cycle time was 1 ms.

In Fig. 5.18, the three different pulsed output characteristics are shown with $V_{GS}$ ranging from +1 V to -4 V. The continuously grown sample shows only little gate and drain lag. In contrast, for the regrown sample, a dramatic increase in $R_{on}$ is observed. This is accompanied by a reduction in maximum drain current. The dispersion may be explained by the capture of free carriers in traps either in the regrown GaN.

**Figure 5.18.** Pulsed measurements of the continuously grown HFET (left) and the regrown HFET (right). $(V_{GS}, V_{DS})$ denotes the quiescent point in V.
or located at the regrowth interface. After stress, these captured carriers will not contribute to the current, hence $R_{on}$ is increased and $I_D$ decreased [111].

In summary, the regrowth has a large impact onto the device characteristics. The material quality seems to be reduced due to the regrowth. This is reflected in $\mu$, the gate leakage currents and the increased dispersion. Also, the regrowth interface can be a source for parasitic leakage currents and traps, which influence the DC and dynamic behavior of the sample.

5.4.2. Regrowth on an etched GaN template

Apparently, the crystal quality of the regrown material and the regrowth interface itself play an important role for the electrical properties of the devices. Moreover, a dry-etching process of the template surface will cause an immense modification for the regrowth process. This is especially relevant when the regrowth is performed on an etched aperture (Fig. 5.11c). In order to quantify the effects of this boundary condition separately, the regrowth with MOCVD on a full-area dry-etched sample is investigated (Fig. 5.12).

Processing A GaN template, consisting of a sapphire wafer, an AlN nucleation and a 2 $\mu$m thick GaN buffer was used. In an ICP process, the topmost 20 nm were etched with a digital etch process, which is a low-damage process and leads to a very smooth surface with an rms roughness about 1.2 nm [115]. Afterwards, the sample was dipped in HCl and BOE for one minute each and subsequently rinsed in deionized water for five minutes [112]. The regrown layers consisted of 200 nm UID GaN and 25 nm $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$. The standard process as described in Sec. 5.4.1 was used to process lateral transistors.

2DEG and Buffer Via van der Pauw and the Hall measurements, $n_S$ and $\mu$ were accessed (Fig. 5.19a). In addition to a relatively low $\mu$ of 1100 cm$^2$/Vs, an $n_S$ larger than $10^{13}$ cm$^{-2}$ is detected. At the same time, mesa isolation measurements at a test structure as depicted in Fig. 5.16a reveal high leakage currents up to 100 mA/mm at 20 V (Fig. 5.19b). Both data suggest that extra charges are introduced at the regrowth interface, which will also form a leakage path.

To verify this assumption, CV measurements were performed (Fig. 5.20a) and the
5.4.2. Regrowth on an etched GaN template

![Graphs showing extracted $n_s$ and $\mu$.](image1)

(a) Extracted $n_s$ and $\mu$.  
(b) Mesa isolation measurements up to 40 V.

**Figure 5.19.** Van der Pauw, Hall and mesa isolation measurements of the regrown HFET on an etched surface.

carrier density profile is derived (Fig. 5.20b). $n_s$ is calculated with

$$n_s = \int_{w_{\text{min}}}^{w(V_{th})} N_{CV}(w) \, dw$$  \hspace{1cm} (5.6)

in which $V_{th}$ is defined as the voltage where $C = \frac{C(V=0V)}{2}$. This method reveals an $n_s$ of 4x10^{12} cm^{-2} for the forward sweep, much smaller than $n_s$ measured with Hall measurements. As indicated by the finite capacitance for voltages below -3 V and the derived carrier density profile (Fig. 5.20b), the sample exhibits a large background carrier concentration. This is reflected by the increase in the $N_{CV}$ at 270 nm, which is apparently at the location of the regrowth interface. Most likely, these background

![Graphs showing CV measurement and derived carrier concentration profile.](image2)

(a) CV measurement shows a hysteresis of 1 V.  
(b) Derived carrier concentration profile.

**Figure 5.20.** Buffer characterization with CV measurements of a HFET regrown on an etched GaN surface.
5.4.2. Regrowth on an etched GaN template

carriers have also been detected in the Hall measurements, pretending a larger \( n_S \) in the 2DEG.

In order to evaluate the background carrier concentration \( n_{Bckgrd} \), the results from Hall- and CV measurements can be combined. It has to be taken into account that this structure is a non-uniform layer in terms of \( n_S \) and \( \mu \), due to the presence of 2DEG and background carriers. \( n_S \) and \( \mu \) obtained by the Hall measurements are only the weighted averages. These are composed of the contribution from the 2DEG and the background carriers and can be calculated by [26, p. 474]

\[
\begin{align*}
    n_{s,Hall} &= \left( \frac{n_{2DEG} \mu_{2DEG} + n_{Bckgrd} \mu_{Bckgrd}}{n_{2DEG} \mu_{2DEG}^2 + n_{Bckgrd} \mu_{Bckgrd}^2} \right)^2 \\
    \mu_{Hall} &= \left( \frac{n_{2DEG} \mu_{2DEG}^2 + n_{Bckgrd} \mu_{Bckgrd}^2}{n_{2DEG} \mu_{2DEG} + n_{Bckgrd} \mu_{Bckgrd}} \right)
\end{align*}
\]

where \( n_{s,Hall} \) and \( \mu_{Hall} \) are the measured values. With \( n_{2DEG} = 4\cdot10^{12} \text{ cm}^{-2} \) as revealed from CV measurements and an ideal \( \mu_{2DEG} = 1800 \text{ cm}^2/\text{Vs} \), \( n_{Bckgrd} = 1.4\cdot10^{12} \text{ cm}^{-2} \) and \( \mu_{Bckgrd} = 2907 \text{ cm}^2/\text{Vs} \) are calculated.

Moreover, the CV curve of this sample shows a hysteresis of about 1 V (Fig. 5.20a). \( n_S \) for the backward sweep is calculated to \( 2\cdot10^{12} \text{ cm}^{-2} \), which results in a \( \Delta n_S \) of \( 2\cdot10^{12} \text{ cm}^{-2} \) from the forward to the backward sweep. This confirms the assumption, that traps are present at the interface, which will capture free electrons at negative bias, leading to a shift in \( V_{th} \).

**DC characteristics** Consistent with the previous results, transfer characteristics of this device show large drain leakage currents in the order of 50 mA/mm (Fig. 5.21). However, gate leakage currents are much lower. Thus, the existence of a parasitic channel at the regrowth interface is confirmed.

In conclusion, the regrowth on an etched surface is more difficult compared to the regrowth on an as-grown GaN template. Even though a low-damage etch process has been used, the regrowth interface is a major source for traps and leakage currents. This may also effect the VHFET with a regrowth on an etched aperture, since leakage currents flowing through the aperture may occur.

As pretreatment, to improve the surface, etching with KOH or etching the surface in ammonia atmosphere in the MOCVD directly before regrowth might be possible. In
addition, the process of the first layers of regrowth can be adjusted further.

### 5.4.3. Regrowth on Mg-doped GaN templates

The fabrication of a VHFET requires a regrowth of an AlGaN/GaN heterostructure on top of a p-doped or p-implanted CBL (Fig. 5.11a). As p-dopant, Mg is used. In the following, the expected influence of the buried p-GaN layer on the top layers and especially the 2DEG properties are discussed (Fig. 5.12).

**Mg redistribution mechanisms** The regrowth of undoped or n-type GaN on top of a Mg-doped layer provides some challenges. Mg is known to be incorporated into the upper layer mainly by three effects:

- Mg diffusion
- Mg segregation
- Mg memory effect

The diffusion constant of Mg in GaN with a value of $10^{-15}\text{cm}^{-2}/\text{s}$ at 1150°C is rather high [38, 116]. Furthermore, the diffusion depends exponentially on temperature and is increased with a higher dislocation density [38, 116, 117]. Another effect is the so
called segregation. During growth, a fraction of the Mg atoms are not incorporated into the crystal. They rather stay close to the surface [38, 116]. This Mg reservoir serves as a source of Mg for the regrown layers. The third effect, the Mg memory effect, depends strongly on the epitaxial growth method and the reactor. It is predominantly observed in MOCVD reactors. During growth, Mg adsorbs on the reactor walls. When the Cp₂Mg source is turned off, Mg desorbs into the gas phase and can be incorporated into the top layers of the crystal [38, 118].

If no measures are taken to suppress these effects, a large concentration of Mg nominally undoped or n-doped, layers is observed. Different regimes in the decay tail of Mg have been identified. Close to the Mg-doped layer, a rather fast decay with a rate of 115 nm/dec is observed. This holds for Mg concentrations down to $10^{17}$ cm$^{-3}$. Then, a much slower decay follows with 650-750 nm/dec [38, 119]. In comparison, for Si, decay rates of 15 nm/dec are common [38, 120]. The two regimes mentioned above can be traced back to the different origins of Mg incorporation and therefore, different measures can be taken to overcome this Mg delay. The slow tail converges to a minimum, process-dependent Mg concentration and is mainly influenced by the memory effect. This minimum Mg concentration in the regrown layers can be reduced by a change or thorough cleaning of the reactor equipment before the regrowth process. Furthermore, the memory effect is reduced when growing in an MBE chamber. The faster tail is related to segregation and diffusion. To eliminate the excessive Mg on the surface, an HCl acid dip can be performed prior to regrowth. This dip allows for an etch of the floating layer of metallic Mg [38]. To reduce the diffusion of Mg, a low-temperature AlN interlayer can be introduced into the structure. This interlayer can serve as a diffusion barrier, and in addition, Mg will be incorporated therein [119]. Furthermore, the diffusion coefficient is exponentially dependent on temperature [121]. Hence, for a smaller diffusion constant, low-temperature processes are favorable, e.g. a regrowth using MBE at 750 °C instead of a regrowth in MOCVD at 1050 °C.

**MOCVD regrowth on Mg-doped GaN**

First, the regrowth with MOCVD on a Mg-doped template is performed, to evaluate the above mentioned approaches for the minimization of the Mg concentration in the regrown layers.

**Samples** The template used for this series consists of a GaN buffer on an AlN nucleation on sapphire, followed by a 250 nm p-GaN layer on top (Fig. 5.22). Before regrowth,
5.4.3. Regrowth on Mg-doped GaN templates

The template was dipped in HCl and BOE for 1 minute and subsequently rinsed with deionized water for 5 minutes to eliminate the excessive Mg [38]. To exclude effects from the Mg memory effect for the subsequent regrowth, a clean reactor without Mg-contaminated hardware was used. On top of the template, three different regrowth procedures were performed (A-C) (Fig. 5.22).

(A) For regrowth A, a 300 nm thick $n^-$-GaN layer ($N_D = 2\cdot10^{16}$ cm$^{-3}$) with a 25 nm thick Al$_{0.25}$Ga$_{0.75}$N barrier on top was applied. Both layers were grown at 1105°C.

(B) For regrowth B, 50 nm of $n^-$-GaN were grown at a lower temperature of 970°C. The remaining 250 nm of n-GaN as well as the 25 nm thick Al$_{0.25}$Ga$_{0.75}$N barrier on top were grown at the usual growth temperature of 1050°C.

(C) The third regrowth C started with 2.5 nm low-temperature AlN grown at 1105°C and 2.5 nm high-temperature AlN grown at 1140°C and continued with the growth of 300 nm $n^-$-GaN and a 25 nm thick Al$_{0.25}$Ga$_{0.75}$N barrier at 1050°C.

The samples were processed with the standard process as described in Sec. 5.4.1.

**Surface morphology** First, the surface morphology was examined using light microscopy and AFM. Samples with regrowth A and B showed a smooth surface. AFM measurements reveal an rms roughness below 1 nm, for a $5\mu$m x $5\mu$m scan, indicating no increase in roughness due to the regrowth (Fig. 5.23a, 5.23b). However, the sample with regrowth C shows a 3-dimensional structure on the surface. This is reflected by an increased rms roughness of 2 nm (Fig. 5.23c). The 3D growth for the sample
5.4.3. Regrowth on Mg-doped GaN templates

![AFM images of sample A, B, and C](image)

(a) AFM image of sample A with rms roughness of 0.51 nm.  
(b) AFM image of sample B with rms roughness of 0.93 nm.  
(c) AFM image of sample C with rms roughness of 2 nm.

**Figure 5.23.** AFM images of the different regrowth A, B and C on a Mg-doped template.

![Optical microscopy image](image)

**Figure 5.24.** Optical microscopy image of regrowth C shows 3-dimensional growth.

with regrowth C is also clearly visible in optical microscopy images (Fig. 5.24), even hexagonal clusters emerge. Since the critical thickness of AlN on GaN around 5 nm is nearly exceeded, this is most likely the origin for the 3D growth [89, 122].

**2DEG** The diffusion of Mg and consequently the existence of acceptors close to the 2DEG compensate the carrier density and influence the carrier mobility in the 2DEG. Before regrowth, the sheet resistance ($R_{SH}$) for the template was very high. Values were in the order of 50000 $\Omega$/sq., confirming the insulating behavior of the buffer material. The corresponding results of eddy-current measurements of the templates after regrowth are shown in Tab. 5.6. After regrowth, only sample C with AlN interlayer shows an acceptably low $R_{SH}$. However, even this sample reveals an $R_{SH}$ which is still higher than for a standard HFET with $R_{SH} \approx 450 \Omega$/sq. It was not possible to generate ohmic contacts for samples A and B. Due to this and due to a too high resistance, no further measurements were performed for the other samples A and B. Apparently, neither the HCl/BOE dip nor the low temperature regrowth could prevent a large concentration of Mg in the regrown GaN or even in the AlGaN layer. Only AlN was
Table 5.6: Average $R_{SH}$ obtained with eddy-current measurements after the different regrowths.

<table>
<thead>
<tr>
<th>Regrowth</th>
<th>$R_{SH}$ [$\Omega$/sq.]</th>
</tr>
</thead>
<tbody>
<tr>
<td>A (only BOE/HCl Dip)</td>
<td>5900</td>
</tr>
<tr>
<td>B (LT-GaN)</td>
<td>1200</td>
</tr>
<tr>
<td>C (AlN diffusion barrier)</td>
<td>4400</td>
</tr>
</tbody>
</table>

(a) $n_S$ from Hall and CV measurements. (b) $\mu$ data from Hall measurements.

Figure 5.25: $n_S$ and $\mu$ data for regrowth C in comparison with a standard HFET.

capable of stopping the Mg diffusion or segregation in an appropriate way.

Based on these results, only sample C was characterized in the further course of this section. Van der Pauw and Hall measurements were performed. They show an $n_S$ of $2.2 \times 10^{12}$ cm$^{-3}$ and a $\mu$ of 850 cm$^2$/Vs. Compared, for example with the continuously grown HFET in Sec. 5.4.1 (reference HFET), $n_S$ and $\mu$ are rather low. Most likely, the low $n_S$ can be attributed to the presence of Mg in the GaN layer.

To further quantify $n_S$ and the doping profile, CV measurements were performed (Fig. 5.26a) and $N_{CV}$ was derived (Fig. 5.26b). $n_S$ was determined using Eq. 5.6; $V_{th}$ is drawn exemplary. From the CV measurements of the regrown sample, an $n_S$ of $3 \times 10^{12}$ cm$^{-2}$, was calculated. This value is slightly higher than for the Hall measurements. Probably, the presence of acceptors leads to a lower $n_S$ in the Hall measurements. The CV curve shows a capacitance below $V_{th}$ unequal to zero (Fig. 5.26a). This is also reflected in the $N_{CV}$ profile. Here, in accordance to the doping of the n-GaN, the background concentration is in the range of $1-2 \times 10^{16}$ cm$^{-3}$. The peak at a depth of about 250 nm is attributed to the buried p-GaN layer.

To estimate the Mg concentration in the channel layer, a simulation with a 1D Pois-
5.4.3. Regrowth on Mg-doped GaN templates

(a) CV measurement of sample C.  
(b) The derived carrier density profile.

Figure 5.26.: CV characterization and determination of the carrier density for regrowth C.

son solver was performed [123]. Therefore, the sample was simulated according to the structure of sample C (Fig. 5.22c).

- The p-GaN layer was simulated with a maximum Mg concentration of \(1 \times 10^{19} \text{ cm}^{-3}\), which results in a hole concentration of \(1 \times 10^{17} \text{ cm}^{-3}\).

- This is followed by 5 nm AlN. It is assumed that the AlN layer incorporates Mg up to a peak concentration of \(8 \times 10^{19} \text{ cm}^{-3}\) [119].

- In the following, 300 nm of n-GaN with different decay rates of the Mg concentration based on the decay profiles in [119] were simulated. Furthermore, different residual Mg concentrations after the decay are assumed.

Six different distributions were tested, their parameters are listed in Tab. 5.7. The simulated structure and the Mg profiles are plotted in Fig. 5.27. The respective band diagram and electron concentrations for the Mg decay rates are depicted in Fig. 5.28.

<table>
<thead>
<tr>
<th>residual Mg [cm(^{-3})]</th>
<th>decay length [nm]</th>
<th>decay rate [nm/dec]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (no Mg)</td>
<td>(1 \times 10^{16})</td>
<td>0</td>
</tr>
<tr>
<td>2 (fast)</td>
<td>(1 \times 10^{17})</td>
<td>100</td>
</tr>
<tr>
<td>3 (medium)</td>
<td>(2 \times 10^{17})</td>
<td>200</td>
</tr>
<tr>
<td>4 (slow)</td>
<td>(4 \times 10^{17})</td>
<td>300</td>
</tr>
<tr>
<td>5 (bckg)</td>
<td>(1 \times 10^{18})</td>
<td>300</td>
</tr>
<tr>
<td>6 (AlGaN)</td>
<td>(1 \times 10^{18})</td>
<td>325</td>
</tr>
</tbody>
</table>

Table 5.7.: Parameters for the magnesiuim decay simulations.
5.4.3. Regrowth on Mg-doped GaN templates

![Graph showing Mg concentration vs depth](image)

**Figure 5.27.** Different Mg decay profiles with respect to the sample dimensions.

![Graph showing band diagram and electron concentration](image)

**Figure 5.28.** Band diagram and electron concentration for different Mg decay profiles.

From here, it is seen, that the electron concentration in the 2DEG is reduced and its profile confined with increasing Mg concentration.

The sheet resistance is calculated by taking into account that the $\mu$ of the electrons is $900 \text{ cm}^2/\text{Vs}$ in the channel (as revealed by the Hall measurements), whereas it is
400 cm$^2$/Vs in bulk GaN [124, 125]. The comparison of the calculated data to the measured ones is shown in Fig. 5.29. Only profile 5 (bckg) with a high Mg background doping of $2 \times 10^{18}$ cm$^{-3}$ or profile 6 with Mg in the AlGaN barrier show an $n_S$ similar to the measured $n_S$. The $R_{SH}$ value of profile 6 with the assumed $\mu$ is in agreement to the Hall data. This means that a large concentration of Mg is still present close to the 2DEG or even in the AlGaN, of which both effects reduce the $n_S$. The simulation confirms the data obtained by the Hall measurements and shows that even though an AlN spacer above the CBL can reduce the Mg concentration in the regrown layers compared to approaches without AlN, it cannot prevent the presence of Mg entirely.

![Figure 5.29](image)

**Figure 5.29.** Simulated $R_{SH}$ and $n_S$ in comparison to the experimental data.

With the presented simulations, the Mg distribution can be estimated on the basis of the Hall measurements. More important, expensive and complex analysis methods such as secondary ion mass spectrometry (SIMS) can be avoided in the first place.

**DC characteristics** To determine the DC-behavior of sample C, transfer characteristics of the processed lateral transistor were measured (Fig 5.30a). First, it is noticed that sample C shows an $I_{D_{max}}$ of 230 mA/mm. However, compared to a „standard“ HFET as shown in Sec. 5.4.1 with $I_{D_{max}} = 530$ mA/mm, currents are still rather low, caused by the low $n_S$. $I_G$ and $I_D$ are plotted in semi-logarithmic scale in Fig. 5.30b. The high drain leakage currents in the order of 1 mA/mm at $V_{GS} = -5$ V are originated by the gate leakage current. The gate leakage current is most probably caused by the 3D growth on the surface and therefore the non-ideal Schottky-GaN surface contact.

In brief, the regrowth with MOCVD on Mg-doped GaN layers was performed. The application of an AlN interlayer was capable of reducing the Mg diffusion and thus
5.4.3. Regrowth on Mg-doped GaN templates

![Graphs showing transfer characteristics](image)

(a) Transfer characteristics and corresponding $g_m$ for sample C.

(b) Transfer characteristics in semi-logarithmic scale. $I_D$ and $I_G$ are depicted.

**Figure 5.30.** DC characteristics of sample C, with a buried p-GaN layer.

maintaining a 2DEG at the AlGaN/GaN interface. However, the Mg diffusion could not be prevented in total, as reflected by a low $n_S$ of $2 \cdot 10^{12}$ cm$^{-2}$.

### MBE regrowth on Mg-doped GaN

As stated above, for a regrowth on p-GaN, a low-temperature process is favorable to suppress the Mg diffusion. Consequently, a higher $n_S$ in the 2DEG is expected. Therefore, in this section, a low-temperature regrowth performed with MBE is discussed.

**Samples** For the regrowth on p-doped MOCVD templates, a GaN buffer with 250 nm Mg-doped GaN with $p = 1.3 \cdot 10^{17}$ cm$^{-3}$ on top was used. Furthermore, a reference template consisting of a UID GaN buffer on sapphire was employed. Before regrowth with MBE, the samples were dipped in HCl and BOE for 1 min each and rinsed with deionized water for 5 minutes. Three samples were investigated:

(R.) A reference sample, without p-GaN layer, with a regrowth of 300 nm n$^-$-GaN and 25 nm Al$_{0.25}$Ga$_{0.75}$N (Fig. 5.31a).

(A) 300 nm n$^-$-GaN and 25 nm Al$_{0.25}$Ga$_{0.75}$N were regrown on a Mg-doped template for sample A (Fig. 5.31b).

(B) For sample B, the regrowth consisted of 400 nm n$^-$-GaN and 25 nm Al$_{0.25}$Ga$_{0.75}$N (Fig. 5.31c).

Growth temperatures in the MBE tool were 750 °C [126]. Samples were processed with
5.4.3. Regrowth on Mg-doped GaN templates

Figure 5.31.: Samples for the investigation of MBE regrowth on a Mg-doped template.

the standard process as described in Sec. 5.4.1.

Morphology No increase in surface roughness, neither for the regrowth on the UID template nor the Mg-doped GaN templates could be detected. The rms roughness for 5 $\mu$m x 5 $\mu$m AFM images is in the order of 1 nm.

2DEG To characterize the properties of the 2DEG, first, Hall and van der Pauw measurements were performed. Fig. 5.32a shows the extracted $n_S$. The reference sample exhibits very high $n_S$ of $640 \cdot 10^{12}$ cm$^{-2}$. Also, sample A and sample B show a high $n_S$ of $1.5 \cdot 10^{13}$ cm$^{-2}$ and $1.1 \cdot 10^{13}$ cm$^{-2}$, respectively. Measurements with X-ray diffraction (XRD) confirmed a 25 nm thick AlGaN barrier layer with an Al-content of 25% for all three samples. Consequently, an $n_S$ in the order of $1 \cdot 10^{13}$ cm$^{-2}$ is expected.

To further characterize the 2DEG, in particular for the reference sample, $n_S$ extracted from the Hall measurements ($n_{S,Hall}$) is compared with $n_S$ extracted from CV measurements ($n_{S,CV}$) (Eq. 5.6). The CV curve in Fig. 5.33 shows no hysteresis and according to that, $n_S$ is equal for the forward and backward sweep. For the reference sample, an $n_S$ of $9.8 \cdot 10^{12}$ cm$^{-2}$ is extracted, which is in good agreement with the calculated $n_S$. However, the large difference of the Hall and CV results suggests a high background carrier concentration. With Eq. 5.8 and 5.7 for a multilayer Hall measurement and an assumed 2DEG mobility of 1800 cm$^2$/Vs, an $n_{S,Background}$ of $274 \cdot 10^{12}$ cm$^{-2}$ is calculated. This is equal to a very high doping concentration of $9 \cdot 10^{18}$ cm$^{-3}$.

As Hall results (and CV results for sample B) for sample A and B are in good agreement to the expected $n_S$, calculated on the basis of the XRD data, no large background carrier density is present for these samples. The difference in the background carrier
5.4.3. Regrowth on Mg-doped GaN templates

(a) $n_s$ extracted from Hall and CV measurements.

(b) $\mu$ data from Hall measurements.

Figure 5.32.: Results from Hall and CV measurements for MBE regrowth on a Mg-doped template.

Figure 5.33.: CV measurements of the reference sample and sample B.

density for the reference sample and sample A and B can either be due to a different doping during growth or due to the compensation from the Mg acceptors. One can in addition assume that $n_{S,B\text{bulk}}$ for sample A may be higher than for sample B because of the increased $n_S$, even though the regrown n-GaN is thinner.

The mobilities are plotted in Fig. 5.32b. The reference sample has very low $\mu$ of 79.4 cm$^2$/Vs. This is mainly caused by the low background carrier mobility of 121 cm$^2$/Vs (calculated with Eq. 5.8). Sample A exhibits a $\mu$ of 850 cm$^2$/Vs and sample B of 1500 cm$^2$/Vs. Here, for increasing $n_S$, the 2DEG is located closer to the AlGaN/GaN interface and the mobility decreases due to interface roughness scattering [127].

**DC characteristics** The transistor characteristics of the three samples are evaluated
5.4.3. Regrowth on Mg-doped GaN templates

![Graphs showing transfer characteristics.]

(a) Linear transfer characteristics.  (b) Transfer characteristics in semi-logarithmic scale.

**Figure 5.34.:** Transfer characteristics of devices with MBE regrowth on a Mg-doped template.

(Fig. 5.34). The reference sample shows large currents above 1000 mA/mm and no pinch-off. It is not further characterized in this section. For samples A and B, the pinch-off of the 2DEG at \( V_{th} \) and the pinch-off of the n-GaN channel at \( V_p \) can be distinguished. \( V_{th} \) and \( V_p \) are plotted exemplarily for sample A. From the linear transfer characteristics (Fig. 5.34a), \( V_{th} \) is extracted to -4.2 V for sample A and to -4.0 V for sample B. In this plot, a large drain-leakage current for sample A can already be assumed. This is confirmed by plotting the transfer characteristics in logarithmic scale (Fig. 5.34b). Here, sample A exhibits an \( I_D \) of 4 mA/mm at \( V_{GS} = -8 \) V. \( V_p \) is extracted to -7 V. Sample B shows lower drain leakage currents of \( 10^{-5} \) mA/mm at \( V_{GS} = -8 \) V and a \( V_p \) of -6 V. The higher leakage currents and more negative \( V_p \) for sample A may be caused by the larger background carrier density in the channel.

To conclude, the regrowth of an AlGaN/GaN heterostructure on a Mg-doped GaN template with MBE was successful. This low-temperature process can suppress Mg diffusion effectively. An \( n_S \), well corresponding to the expected \( n_S \) for the AlGaN barrier configuration, of \( 1 \times 10^{13} \) cm\(^{-2} \) was achieved for samples regrown on a p-GaN template. Although the background carriers (or possible doping) may be depleted from the underlying p-GaN, no compensation was detected for the 2DEG.

To sum up, the regrowth with MBE and MOCVD on Mg-doped GaN templates was investigated. In the latter, an AlN interlayer can reduce the Mg diffusion sufficiently that a 2DEG can be detected. Nevertheless, \( n_S \) is still rather low. Only the low-temperature MBE process at 750 °C yielded an \( n_S \) comparable to standard HFET. So
far, an MBE regrowth is preferred over an MOCVD regrowth.

5.4.4. Regrowth on structured templates

Another aspect which has to be considered, is the regrowth on either textured or masked surfaces. The process flow of a VHFET includes on the one hand, the regrowth on or in an etched aperture/trench (Fig. 5.11c) and on the other hand, the selective regrowth of a p-GaN CBL on a masked template (Fig. 5.11b). In this section, the regrowth with MOCVD and MBE on textured and masked templates will be evaluated as shown in Fig. 5.12.

Particularly the planarization of etched trenches is challenging. Usually, material growth will primarily occur on the top surface and on the step edge rather than at the trench bottom [128]. For regrowth with MOCVD at elevated temperatures of 1050 °C, an additional process, the so called mass transport is expected. Hereby, material from the sidewalls and the surface desorbs and adsorbs at the trench bottom [129]. This leads to a wedge-like sidewall profile [130]. On the contrary, for MBE regrowth at lower temperatures of about 750 °C, no mass transport is expected. However, the migration length of the adsorbed atoms is shorter, therefore, a reduced growth in the trench and an enhancement of lateral growth at the step edges is expected.

MOCVD regrowth on a textured template

In the process flow of a VHFET, the aperture opening is etched into the p-GaN CBL and is filled during regrowth of the channel and barrier layer as shown in Fig. 5.11c. Since the gate is located on top of the etched region, it is desired to obtain a planar surface. However, as stated above, a full planarization is not easy to achieve. To investigate the growth behavior on textured surfaces of MOCVD-regrown GaN, 300 nm deep apertures/trenches are etched into a GaN template. The width of an etched trench in this case corresponds to the aperture length \( L_{ap} \) in the device structure. The trenches exhibited \( L_{ap} \) of 1 \( \mu \)m, 2 \( \mu \)m, 6 \( \mu \)m, and 8 \( \mu \)m and a width of 50 \( \mu \)m. The sidewalls have angles of 90°. The regrown GaN layer had a nominal thickness of 350 nm. As structure of such a trench is shown in cross-section and in plain view in Fig. 5.35.
5.4.4. Regrowth on structured templates

**Figure 5.35.** Schematic of a structured template in cross-section (left) and plain view (right).

SEM images of aperture trenches with aperture length ($L_{ap}$) of 1 µm, 6 µm, and 8 µm after the MOCVD regrowth are shown in Fig. 5.36.

**Figure 5.36.** SEM images of aperture trenches with various width after MOCVD regrowth.
A schematic of the trench is inserted in Fig. 5.36a, the trenches are oriented horizontally. The lengths of the apertures as they were before regrowth, are indicated by the white dotted lines. For the aperture with $L_{ap} = 1 \mu m$, a narrow trench is still visible (Fig. 5.36a). For larger apertures, such as 6 $\mu m$ and 8 $\mu m$ (Fig. 5.36b, 5.36c), the trench cannot completely be filled. Furthermore, as shown in the magnified image in Fig. 5.36d, the morphology on the aperture sidewalls is different in comparison to the flat surface and aperture bottom.

AFM images and corresponding height profiles of the trench cross-section are shown in Fig. 5.37. As inset, a schematic of a trench is depicted in Fig. 5.37a, the trenches are oriented vertically. The AFM images confirm the remaining trenches after regrowth. Apertures with increasing $L_{ap}$ show an increased trench depth from about 40 nm for $L_{ap} = 2 \mu m$ to about 170 nm for $L_{ap} = 8 \mu m$ (initial depth 300 nm). In addition, the length of the trench bottom and the trench surface increases for increasing $L_{ap}$. The height profiles show different sidewall slopes for the right and the left side. These are not dependent on the scan direction, but are originated in the growth process. The sidewall angles increase with increasing $L_{ap}$ from about 3° to 7°. Furthermore, the sidewalls show a different morphology compared to the top surface, but no increase in rms roughness.

To quantify the growth, a fill factor (FF) is defined which correlates the volume which "should be filled" with the actually filled volume. Fig. 5.38a, shows the respective volumes. Volume A (striped volume) is the volume which is desired to be filled, whereas volume B (triangle or trapezoid) is the volume of the remaining trench. The Fill factor is then defined as

$$\text{FF} = \frac{A - B}{A}$$

(5.9)

Fill factors increased from 93% for $L_{ap} = 8 \mu m$ and 97% for $L_{ap} = 6 \mu m$ to 98% for $L_{ap} = 1 \mu m$.

A schematic of an MOCVD regrowth in a trench is depicted in Fig. 5.38b. To explain the FF and the morphology, two growth effects and the aspect ratio $\text{AR} = \frac{\text{trench depth}}{L_{ap}}$ of the trench have to be considered. On the one hand, 2D layer growth at the trench bottom and at the surface adjacent to the trench occurs. For larger AR (small $L_{ap}$), all atoms arriving in the trench diffuse to the step edge and nucleate there. For smaller AR (large $L_{ap}$), nucleation in the trench takes place at the step edges as well as in the middle of the trench bottom.
5.4.4. Regrowth on structured templates

(a) Trench with $L_{ap}$ of 2 $\mu$m.

(b) Trench with $L_{ap}$ of 6 $\mu$m.

(c) Trench with $L_{ap}$ of 8 $\mu$m.

(d) Height profiles of trenches after regrowth.

**Figure 5.37.** AFM images and the corresponding profiles of aperture trenches after MOCVD regrowth with various $L_{ap}$.

On the other hand, a redeposition of material from the surface to the trench sidewall is detected. This mass transport leads to more shallow sidewall angles [129] and is also reflected by the differing morphologies of the surface and the sidewall. For smaller apertures, this edge effect due to mass transport is more dominant. Here, for shallow angles of about 3°, the flanks of the two opposite sidewalls overlap, leading to a faster planarization of the trench. Furthermore, the flanks originated from mass transport may contain Mg from the Mg-doped CBL. This is indicated by the red dots in the sidewalls in Fig. 5.38b.
5.4.4. Regrowth on structured templates

MBE regrowth on a textured template

The regrowth on textured templates with MBE is investigated in this section. Again, trenches with $L_{ap}$ of 1 µm, 2 µm, 6 µm, and 8 µm were etched 300 nm deep into the GaN template. Subsequently 350 nm of GaN are regrown with MBE. Since regrowth with MBE is a low-temperature process, only 2D growth is expected and no effects from mass transport from the surface to the sidewalls will occur here [129].

In Fig. 5.39, trenches with three different widths of 1 µm, 2 µm and 6 µm after the MBE regrowth are depicted. The trenches are oriented vertically in these images and the contours of the trenches before regrowth are indicated by the white dotted line. Material growth on the top surface as well as in the aperture trench can be observed. For larger apertures, a layer-by-layer growth in the trench is visible, whereas for the aperture with $L_{ap} = 1$ µm a non-homogeneous, 3D-like growth inside the trench is observed (Fig. 5.39b). To illustrate the growth mechanism, a schematic cross section is shown in Fig. 5.40. Since the migration length of the atoms is shorter in MBE, due to the low temperature [36], the material from the surface most likely sticks to the top edge of the sidewall. Here, the lateral growth is enhanced in comparison to the growth at the trench bottom. This lateral growth leads to the formation of a cusp at the step edge. For smaller apertures, the ratio of lateral growth to trench width is larger, hence, the material transport inside the trench, below the cusp, is hindered. The layer thickness at the bottom is therefore reduced for smaller apertures, and may even lead to the formation of a void in the further growth process. For larger apertures, more material grows in the trench. Consequently, the overlap of the regrown n-GaN on the CBL and in the trench is increasing, providing a thicker channel region for the VHFET.

Figure 5.38.: Schematics of the MOCVD regrowth on a textured sample.
5.4.4. Regrowth on structured templates

(a) Trench with $L_{ap}$ of 1 µm.

(b) Magnification of a trench with $L_{ap}$ of 1 µm.

(c) Trench with $L_{ap}$ of 2 µm.

(d) Trench with $L_{ap}$ of 6 µm.

Figure 5.39.: SEM images of MBE regrowth in trenches with different $L_{ap}$ of 1 µm, 2 µm and 6 µm.

Figure 5.40.: Schematic cross section of MBE regrowth in a trench.
MOCVD regrowth on a masked template

In the previous section, a full-area regrowth on an etched or structured template was performed. However, for Process 2 (Fig. 3.11, p. 27), a selective regrowth of the p-GaN CBL on a defined area is required. Therefore, the n-GaN at the position of the aperture opening has to be masked, thus the growth only occurs at designated openings. Because SiN offers a good growth selectivity to GaN, it was applied as a mask material [131]. In order to investigate the MOCVD regrowth on a masked template, the aperture areas are covered with a 300 nm thick SiN mask. Subsequently, 250 nm of p-GaN were regrown with MOCVD. Fig. 5.41a shows an SEM image of a sample after GaN regrowth. The SiN mask is still on top of the designated aperture and shows the expected selectivity to GaN; no GaN growth is visible thereon. Furthermore, it is visible that the p-GaN adjacent to the SiN mask exhibits an increased growth rate compared to the p-GaN more distant to the mask. A schematic of the sample after regrowth is shown in Fig. 5.41b to illustrate the growth behavior close to the masked area. The increased growth at the mask edges is due to the fact that the Ga and N atoms cannot nucleate an island on the SiN mask. Therefore, they diffuse to the closest GaN surface and incorporate there [132].

In conclusion, a homogeneous regrowth on masked substrates is quite difficult to achieve. Moreover, it leads again to a textured substrate which results in increased complexity of the further growth of the AlGaN/GaN heterostructure. Specific growth processes with adapted growth conditions need to be developed to optimize growth on textured and masked templates.

**Figure 5.41.** Images of GaN regrowth on a template masked with SiN.
5.4.4. Regrowth on structured templates

In summary, both, the regrowth with MOCVD and MBE on textured substrates is challenging. In particular, the full planarization of etched trenches could not be achieved. However, different growth mechanisms have been identified. For MOCVD regrowth, the trench is filled by a combination of mass transport and vertical growth. Whereas, for MBE regrowth, a pronounced lateral growth at the trench edges is observed, limiting the growth in the trench. Furthermore, regrowth on a masked template is challenging, due to an enhanced growth rate in the vicinity of the masked regions. To obtain smooth and homogeneous layers, specific growth processes with new growth conditions need to be developed to optimize growth on textured and masked templates.
6. Realization of a vertical transistor

In this chapter, two realizations of a quasi-vertical VHFET based on the results from the previous chapters are processed. Here, the CBL is formed by an MOCVD p-GaN layer. The aperture is subsequently created by etching into the p-GaN. Next, the regrowth of the n-GaN channel and the AlGaN barrier on top is performed. For the first example, this regrowth is performed with MOCVD. In the second part of the chapter, a device with MBE regrowth is presented.

6.1. Vertical transistor with etched aperture and MOCVD regrowth

First, the process of the all-MOCVD grown VHFET will be described in more detail, also displaying the final structure. Subsequently, the transistor will be electrically characterized, especially emphasizing their DC characteristics and breakdown behavior.

6.1.1. Processing

A schematic of the complete transistor is shown in Fig. 6.1a. The growth was performed on a sapphire substrate. First, a 2 µm thick n⁺-GaN layer on an AlN buffer was grown for the backside ohmic contact; subsequently, a 700 nm thick drift layer was deposited. The doping of the drift region was chosen to 5·10¹⁶ cm⁻³, as it revealed the best $R_{on}$ to $V_{BR}$ ratio (Sec. 5.2). On top, a 250 nm thick p-GaN layer with $N_A = 1·10^{19}$ cm⁻³ was grown. This layer serves as CBL (Sec. 5.3). The VHFET was processed according to Process 3 in Fig. 3.11. Thus apertures with aperture length ($L_{ap}$) of 1 µm to 8 µm and widths of 50 µm were etched into the p-GaN by an ICP-process (Sec. 5.4.2). Before regrowth, the sample was dipped in HCl and BOE for one minute each. Next, a 300 nm thick channel with $N_D = 5·10^{16}$ cm⁻³ was regrown with MOCVD followed by a 25 nm thick Al₀.₂₅Ga₀.₇₅N barrier layer on top.
6.1.2. Characterization

To characterize the 2DEG, Hall measurements were performed. These reveal an electron concentration of $1.6 \times 10^{12} \text{ cm}^{-2}$ and an electron mobility of $750 \text{ cm}^2/\text{Vs}$. These values are in good agreement to the results of Sec. 5.4.3.

Source contact resistance ($R_{c,s}$) and drain contact resistance $R_{d,s}$ were measured via the transfer length method (TLM) and circular transfer length method (CTLM), respectively; $R_{c,s} = 7 \Omega \text{mm}$ and $R_{d,s} = 1.7 \Omega \text{mm}$ were evaluated.

Next, a transistor with a gate length ($L_G$) of $5 \mu\text{m}$, an aperture length ($L_{ap}$) of $1 \mu\text{m}$ and an overlap of gate and aperture ($L_{GA}$) of $2 \mu\text{m}$ is characterized. The currents are normalized to the active area. This area is the distance between the two source electrodes multiplied by the gate length. First, output characteristics of the devices are

Figure 6.1.: Pictures of the processed, fully MOCVD grown VHFET with etched aperture.

After finishing the growth procedure, the mesa was etched, targeting to the $n^+$-GaN layer (Sec. 5.1). Subsequently, the ohmic drain and source contacts consisting of Ti/Al/Ni/Au were deposited via e-beam evaporation and annealed at $825 ^\circ \text{C}$. For the gate contacts, Ni/Au was deposited.

The mask layout comprises vertical devices as well as lateral devices and test structures.

An optical microscopy image of the final device is shown in Fig. 6.1b. In coherence to the findings of Sec: 5.4.4, the aperture is still visible as a thin line.
measured. In this case, $V_{GS}$ was varied from $+2 \text{ V}$ to $-8 \text{ V}$. As depicted in Fig. 6.2a, no saturation can be detected for the drain current up to a $V_{DS}$ of 20 V. This is most likely due to a too large resistance of the aperture ($R_{ap}$) which delays current saturation. Moreover, even for $V_{GS} = -8 \text{ V}$, the transistor does not pinch off. Taking into account the gate current (Fig. 6.2b), it is furthermore obvious that it is rather large compared to $I_D$. Since sources and gate are located on the top of the wafer, the reverse leakage current more easily flows between these contacts. This is furthermore reflected in the source current (not shown). Only, when $V_{DS}$ is large enough, so that the vertical field induced by the drain contact is dominating, the drain current exceeds $I_G$.

Transfer characteristics of the VHFET measured from $V_{GS} = -8 \text{ V}$ to $+4 \text{ V}$ for two different $V_{DS}$ of 10 V and 20 V are shown in Fig. 6.3a. As expected, the transfer characteristics of a depletion mode (d-mode) transistor are recognized. $V_{th}$ was extracted via the linear extrapolation method to $V_{th} = -2.8 \text{ V}$ and $V_{th} = -4.5 \text{ V}$ for $V_{DS} = 10 \text{ V}$ and 20 V, respectively. $I_{D,\text{max}}$ of 0.3 A/cm$^2$ and 1.4 A/cm$^2$ are realized for $V_{DS}$ of 10 V and 20 V, respectively. For $g_m$, values of 0.1 S/cm$^2$ and 0.4 S/cm$^2$ are obtained. These low values indicate again a high $R_{ap}$. Also, the device suffers from high off-state leakage currents, limiting the on/off ratio to 7 and 43 for $V_{DS}$ of 20 V and 10 V, respectively. Further insight into the off-state currents is gained by looking at Fig. 6.3b. Here, it can be seen that the gate leakage currents are in the order of 0.2 to 0.1 A/cm$^2$ at $V_{GS} = -8 \text{ V}$ for both $V_{DS}$. Here, $I_G$ increase for more negative $V_{GS}$ even above $I_D$.

The drain leakage current is in the same order of magnitude as the gate leakage.
6.1.2. Characterization

(a) Linear transfer characteristics. 

(b) $I_D$ and $I_G$ in semi-logarithmic scale.

Figure 6.3.: Linear and logarithmic transfer characteristics of the VHFET with $L_G = 5\, \mu m$, $L_{GA} = 2\, \mu m$ and $L_{ap} = 1\, \mu m$.

Figure 6.4.: Influence of $L_{GA}$ on drain leakage currents for VHFET with $L_G = 6\, \mu m$.

(Fig. 6.3b) and can be attributed to different leakage paths: either along the mesa, through the CBL or through the aperture. Neither mesa leakage has been detected for the VSD in Sec. 5.2, nor severe leakage through the simple pn junction in Sec. 5.3. Hence, the most probable leakage path is through the aperture. This assumption can be confirmed by investigating VHFETs with varying $L_{GA}$. As already predicted by simulations in Sec. 4.4, an increased $L_{GA}$ will enhance the gate control and reduce therefore drain leakage currents. In Fig. 6.4, the transfer characteristics of transistors with $L_{ap} = 6\, \mu m$ and $L_{GA}$ of 1\,\mu m, 3\,\mu m and 4\,\mu m are depicted. The larger the overlap, the more the drain leakage current is reduced. At $V_{GS} = -4\, V$, half an order of magnitude lower currents for $L_{GA}$ of 4\,\mu m compared to $L_{GA}$ of 1\,\mu m are detected, indicating, that the major leakage path is through the regrown GaN-channel and the aperture.
For the gate leakage current, no larger influence can be detected.

Though the transistor shows d-mode characteristics and some trends, such as the influence of $L_{GA}$, can be detected, the currents are rather low. To identify the origin of these low currents, various resistances, which play a role in the device, are quantified. The detailed analysis is described in the Appendix in Sec. A.1. Resultant, $R_{ap}$ is in the order of $10 \, \text{M}\Omega$, whereas the resistance of the 2DEG ($R_{2\text{DEG}}$) and the resistance of the 2DEG in the aperture ($R_{2\text{DEG,ap}}$) are $500 \, \Omega$ and $900 \, \Omega$, respectively. To sum up, the device properties are mainly dominated by the aperture resistance. This can for example be explained by the partial depletion of the aperture opening by the magnesium. The Mg concentration is probably further enhanced by the mass transport from the sidewalls of the CBL. For these reason, current crowding may occur or even a total depletion of the aperture. This would result in an insulating layer.

**Breakdown** In addition to the on-state behavior of the VHFET, three-terminal breakdown measurements were performed. Lateral and vertical transistors on the discussed epitaxial structure were measured with $V_{GS} = -10 \, \text{V}$. The breakdown voltage was defined as the voltage at which $I_D$ exceeds $5 \, \text{A/cm}^2$. The lateral HFET exhibits breakdown voltages of $V_{BR} = 20 \, \text{V}$. In contrast, for the VHFET, values of $V_{BR} = 140 \, \text{V}$ are obtained. For these voltages, the space charge region extends from gate to drain for both devices. With $d_{GD}$ of $2.5 \, \mu\text{m}$ for the lateral HFET and an assumed doping concentration in the AlGaN of $3 \times 10^{15} \, \text{cm}^{-3}$, the critical electrical field is calculated with Eq. 5.4 to $E_{c,\text{lat}} = 0.16 \, \text{MV/cm}$. Even though the vertical HFET has a $d_{GD}$ of only $1 \, \mu\text{m}$, the critical electric field is nearly 20 times larger with $E_{c,\text{vert}} = 3 \, \text{MV/cm}$. Here, an $N_D$ of $2 \times 10^{16} \, \text{cm}^{-3}$ is assumed.

![Graph](image1.png)

(a) Three-terminal breakdown measurements.

![Image](image2.png)

(b) Optical microscopy image of a destructed VHFET.

**Figure 6.5.** Breakdown voltage characterization on lateral and vertical HFET.
6.2.1. Processing

An optical microscope image (Fig. 6.5b) of a VHFET which suffered from destructive breakdown clearly shows that the breakdown takes place underneath the gate contact towards the source. This is most likely attributed to the breakdown at the aperture edge, which is the point, at which the highest field is located (Sec. 4).

In conclusion, a completely MOCVD-grown VHFET has been processed. The on-state characteristics are mainly dominated by the large $R_{ap}$. Thus, only low on-currents and $g_m$ were measured. However, the VHFET shows an excellent breakdown voltage of 150 V, resulting in $E_{crit} = 3$ MV/cm, a value close to the theoretical maximum. To further optimize the VHFET with MOCVD regrowth, the $R_{ap}$, mainly attributed to the Mg-diffusion, has to be reduced. Therefore, a low-temperature MOCVD process would be necessary.

6.2. Vertical transistor with etched aperture and MBE regrowth

The second realization of a vertical transistor is also relying on Process 3 (Fig. 6.6). Equally to the first device, the drift region and the CBL are grown with MOCVD and subsequently, the aperture is etched into the p-GaN. To form the 2DEG at the AlGaN/GaN heterostructure, here, an MBE regrowth is performed. As stated in Sec. 5.4.3, a low-temperature regrowth with MBE is favorable because Mg diffusion is largely suppressed due to a low temperature process.

In this section, first, the processing of the device is elucidated. Subsequently, the DC characterization of the transistors is presented, in particular the dependence of the electrical characteristics on varying $L_{ap}$ and $L_{GA}$.

6.2.1. Processing

For this device, the same structure as in Sec. 6.1.1, consisting of an n$^{+}$-GaN layer, a 700 nm thick n$^{-}$-GaN layer and 250 nm p-GaN on top, was used. The doping concentration of the drift region was $5 \times 10^{16}$ cm$^{-3}$ and the p-type doping of the CBL $1 \times 10^{19}$ cm$^{-3}$. Subsequently, the aperture was etched into the CBL by an ICP process (Sec. 5.4.2). Before regrowth, the sample was dipped in HCl and BOE for one minute each and rinsed in deionized water for five minutes. The regrowth was performed with MBE at 750 °C. 450 nm of n$^{-}$-GaN were grown as channel, before the growth of 25 nm of
6.2.2. Characterization

Figure 6.6.: Schematic of the VHFET with an etched aperture and MBE regrowth.

Al$_{0.25}$Ga$_{0.75}$N barrier. The doping in the channel was targeted to 5·10$^{16}$ cm$^{-3}$.

The identical process as described in Sec. 6.1.1 was used for the fabrication of the devices.

6.2.2. Characterization

First, the 2DEG properties were evaluated. For $n_S$ and $\mu$, the same values as extracted in Sec. 5.4.3 were obtained. Hence, $n_S$ is 7·10$^{12}$ cm$^{-2}$ and $\mu$ is 1500 cm$^2$/Vs. Source and drain contacts were characterized via the TLM and CTLM methods, respectively. For $R_{c,s}=0.4 \, \Omega \, \text{mm}$ and for $R_{c,d}=2.0 \, \Omega \, \text{mm}$ were extracted.

Second, the output characteristics of a transistor with $L_G=12 \, \mu$m, $L_{ap}=8 \, \mu$m and $L_{GA}=2 \, \mu$m were measured. Hereby, $V_{GS}$ was varied from +2 V to -8 V. As depicted in Fig. 6.7a, a linear region and a saturation region are detected. $I_{D,max}$ is in the order of 3000 A/cm$^2$ for $V_{GS}=2$ V. Output characteristics of transistors with different $L_{ap}$ of 8 $\mu$m, 6 $\mu$m and 2 $\mu$m are depicted in Fig. 6.7b. These show a decreasing $R_{on}$ from 15 m$\Omega$cm$^2$ to 2 m$\Omega$cm$^2$ with increasing $L_{ap}$ from 2 $\mu$m to 8 $\mu$m, respectively, as predicted by the simulations in Sec. 4.5. Furthermore, $I_{D,max}$ rises with increasing $L_{ap}$. For smaller $L_{ap}$, the higher $R_{on}$ delays the current saturation, which is particularly visible for $L_{ap}=2 \, \mu$m.

Third, the transfer characteristics of the devices were evaluated. Linear transfer characteristics for the devices with different $L_{ap}$ and $L_{GA}=2 \, \mu$m are shown in Fig. 6.8a. In particular for the sample with $L_{ap}=8 \, \mu$m and $L_{ap}=6 \, \mu$m, the pinch-off of the 2DEG as well as the pinch-off of the channel are detected. These are also reflected in the two
6.2.2. Characterization

(a) Output characteristics for a VHFET with $L_{GA} = 2 \mu m$ and $L_{ap} = 8 \mu m$.

(b) Output characteristics for different $L_{ap}$.

Figure 6.7.: Output characteristics of a VHFET with MBE regrowth.

peaks in the $g_m$ curve.\textsuperscript{1} $V_{th}$ and $V_p$ are -3.8 V and -4.9 V for the sample with $L_{ap} = 8 \mu m$ and -3.5 V and -4.2 V for the sample with $L_{ap} = 6 \mu m$, respectively. Also here, a decrease in $I_{D,max}$ for decreasing $L_{ap}$ is observed. The sample with $L_{ap} = 2 \mu m$ shows a lower $I_D$ of 300 A/cm\textsuperscript{2}, and for this curve only the depletion of the 2DEG can be observed with $V_{th} = -5$ V. However, $I_{D,max}$ in the range from 300 A/cm\textsuperscript{2} to 4000 A/cm\textsuperscript{2}, is still three orders of magnitude higher than for VHFET in Sec. 6.1. The transfer characteristics in logarithmic scale (Fig. 6.8b) demonstrate an increase in drain leakage current with increasing $L_{ap}$. On/off ratios of 61, 300 and 2300 are detected for an $L_{ap}$ of 8 \mu m, 6 \mu m and 2 \mu m, respectively. The above mentioned observations are in good agreement to the results of the growth analysis on textured templates (Sec. 5.4.4). As stated there, the growth in the trench/aperture is enhanced for larger $L_{ap}$. Therefore, an increased overlap between the regrown GaN on the CBL and the regrown GaN in the trench is enabled. This can serve as a leakage path. On the other hand, with increasing $L_{ap}$ also a higher $I_D$ can be realized.

In addition, transfer characteristics on devices with a constant $L_{ap}$ of 6 \mu m and different overlap of gate and aperture ($L_{GA}$) were measured (Fig. 6.9). $L_{GA}$ of 1 \mu m, 3 \mu m and 4 \mu m are applied. According to the simulations in Sec. 4.4, the linear transfer characteristics (Fig. 6.9a) reveal an increasing $g_m$, both, for the depletion of the 2DEG and the channel, with increasing $L_{GA}$. At the same time, $V_{th}$ and $V_p$ shift to more positive values. The enhanced gate control with larger $L_{GA}$ is also reflected in the semi-logarithmic transfer curves. The on/off ratio increases from 66 to 230 when increasing

\textsuperscript{1}For these measurements, only one source electrode was contacted to exclude effects from lithography misalignment.
6.2.2. Characterization

(a) Linear transfer characteristics.  
(b) \( I_D \) and \( I_G \) in semi-logarithmic scale.

Figure 6.8.: Linear and logarithmic transfer characteristics of VHFET with \( L_{GA} = 2 \mu m \) and different \( L_{ap} \).

(a) Linear transfer characteristics.  
(b) Transfer characteristics in semi-logarithmic scale.

Figure 6.9.: Linear and logarithmic transfer characteristics of VHFET with \( L_{ap} = 6 \mu m \) and different \( L_{GA} \).

\( L_{GA} \) from 1 \( \mu \)m to 4 \( \mu \)m.

For the presented devices, high drain leakage currents in the order of 20 A/cm\(^2\) to 50 A/cm\(^2\) were detected. The rather thick channel of 450 nm with \( N_D = 5 \times 10^{16} \text{cm}^{-3} \) prevents a better pinch-off. Hence, three terminal breakdown measurements, with a \( V_{BB} \) defined at \( I_D = 5 \text{A/cm}\(^2\)\), reveal an only very low \( V_{BB} \) of 10 V to 20 V.

To sum up this section, a VHFET with MOCVD-grown p-GaN template and MBE-regrown AlGaN/GaN heterostructure was successfully realized. High on-state currents up to 300 mA/mm and a low \( R_{on} \) in the order of 2 m\( \Omega \)cm\(^2\) were observed.
As expected, with decreasing $L_{ap}$, the resistance increased as well as the leakage currents. For larger $L_{ap}$, the gate control over the 2DEG and the channel could be enhanced, reducing the leakage currents to 10 $\mu$A/mm. In combination with the low $R_{on}$ and the high leakage current, only a very low $V_{BR}$ of 20 V was measured.

In conclusion, two examples of a VHFET based on the evaluated building blocks were presented in this chapter. Both devices are based on an MOCVD template and an etched p-GaN aperture. The device with an MOCVD AlGaN/GaN regrowth exhibited a large $E_{crit}$, but also a large $R_{ap}$. Whereas, the device with MBE regrowth showed reasonable on-state characteristics, but large leakage currents. The most promising approach so far is the use of a low-temperature regrowth process to prevent the diffusion of Mg. The thickness and doping concentration have to be controlled precisely to avoid a conductive channel. Furthermore, large $L_{ap}$ of 8 $\mu$m and a sufficient $L_{GA}$ larger than 4 $\mu$m are favorable to obtain a high on/off ratio.
7. Conclusion and Outlook

The objective of this work was to fabricate vertical GaN-based transistors which rely on the CAVET design. For this purpose, the different building blocks of a CAVET and their challenges were identified, characterized, and various approaches were optimized. Chapter 3 gives an overview of different realizations of vertical diodes and transistors. Thereby, the CAVET design has been identified as the most promising concept for vertical transistors so far. The realization of a CAVET was pursued in the further course of this work.

In order to gain information about the important characteristics of a CAVET, electrical simulations with Sentaurus TCAD of growth and process-related parameters were performed in Chapter 4. The doping of the drift region has been identified as an important parameter, influencing both, $R_{on}$ and $V_{BR}$. A doping concentration of $5 \cdot 10^{16} \text{cm}^{-3}$ exhibited the best performance in terms of the BFOM. Furthermore, the channel parameters were analyzed. The doping concentration and thickness of the channel mainly influence $V_{th}$ and $V_p$. An increase in doping concentration induces an enhanced $n_S$ and a shift of $V_{th}$ to more negative values. Similar to the drift region, a doping concentration of $1 \cdot 10^{16} \text{cm}^{-3}$ in the channel is favorable. An increase in channel thickness reduces the depletion of the 2DEG caused by the p-GaN layer. However, it also induces $V_p$ to shift to more negative values. Balancing the tradeoff between depletion and $V_p$ leads to an optimal thickness of 300 nm. As an important process parameter, the overlap of gate and aperture was simulated. The overlap should be larger than 250 nm to assure a sufficient gate control of the 2DEG and the n$^-$-GaN channel. Moreover, the length of the aperture itself is crucial. Apertures with $L_{ap}$ below 3 $\mu$m exhibit an increased on-resistance due to current crowding. The angle of the aperture can be influenced, as well. Small angles lead to a reduced electrical field at the aperture, which will enhance $V_{BR}$. However, a sufficient $L_{GA}$ has to be ensured.

The complete fabrication of a CAVET comprises various experimental challenges. To solve these challenges separately and successively, the process is divided into four
building blocks. These are elucidated in Chapter 5.

First, a process for the fabrication of quasi-vertical devices was developed. The use of insulating sapphire substrates requires access to the backside ohmic contact from the top. An etch process with $V_{dc}$ of -250 V yielded an etch-rate of 500 nm/min and etch angles of 90°. Also, the surface and sidewalls were sufficiently smooth to deposit the metal stack.

Second, the doping of the drift region was optimized according to the results of the previous simulations. Vertical Schottky diodes with different doping concentrations were characterized with regard to their $R_{on}$ and $V_{BR}$. The highest $BFOM$ was extracted for a doping concentration of $2 \times 10^{16} \text{ cm}^{-3}$ with a $V_{BR}$ of 230 V and $R_{on}$ of 1.05 mΩ cm$^2$. In addition, the use of an AlN nucleation instead of a GaN nucleation was favorable. The AlN nucleation yields $BFOM$ increase of 50%.

Third, the application of a pn junction as current blocking layer was evaluated. A pn junction with $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ and $N_D = 5 \times 10^{16} \text{ cm}^{-3}$ exhibited a breakdown voltage of 140 V and very low leakage currents below $10^{-4} \text{ A/cm}^2$. Hence, such a designed pn junction is capable of blocking the direct current flow between source and drain and furthermore offers a sufficiently high breakdown voltage for an application in a CAVET.

Fourth, the regrowth of the n-GaN channel and the AlGaN barrier on top of the current blocking layer was investigated. The regrowth is one of the main challenges in the process of a CAVET. It determines the interface between the current blocking layer and the channel as well as the interface between the etched aperture and the channel. Regrowth experiments on as-grown GaN buffers confirmed that the influence of the interface is of crucial importance. Pulsed measurement revealed enormous dispersion effects, which were attributed to the regrowth interface. The regrowth is also performed on an etched GaN surface to simulate the regrowth in an etched aperture. It is shown that the regrowth interface is a major source for leakage currents and traps. CV measurements showed a shift in $V_{th}$ which corresponds to a reduction of $n_S$ by $1 \times 10^{12} \text{ cm}^{-2}$ from the backward to the forward sweep. Furthermore, drain leakage currents were as high as 50 mA/mm, whereas gate leakage currents were much lower. A parasitic channel at the regrowth interface was proposed to explain this behavior.

Next, the regrowth on the Mg-doped p-GaN CBL was investigated. Mg is known to diffuse into the adjacent layers resulting in the depletion of the 2DEG. Three different measures to prevent the out-diffusion of Mg were tested for MOCVD regrowth.
In particular, an AlN interlayer successfully reduced the Mg concentration in the regrown layers. As a consequence, an $n_S$ of $2 \times 10^{12}$ cm$^{-2}$ was obtained, still lower than the expected $n_S$ of $9 \times 10^{12}$ cm$^{-2}$ as revealed for a standard lateral HFET. Simulations resulted in a Mg concentration of $1 \times 10^{18}$ cm$^{-3}$ close to the 2DEG. In order to further reduce the Mg concentration, MBE instead of MOCVD regrowth was performed on the CBL. MBE growth takes place at low temperatures of 750 $^\circ$C, in contrast to the high MOCVD temperatures of 1050 $^\circ$C. The lower temperatures more effectively prevent Mg diffusion than the AlN interlayer. Accordingly, an $n_S$ of $7 \times 10^{12}$ cm$^{-2}$ was obtained.

The use of a Mg-doped CBL implies the aperture to be etched into the GaN. Thus, the subsequent regrowth has to be performed on a textured template. A homogeneous growth and a full planarization of the textured aperture area is desired. However, MOCVD regrowth led to only partially filled aperture trenches as a result of mass transport and growth in c-direction. For this process, a larger aspect ratio of the trench is preferable. In contrast, MBE regrowth showed both, lateral growth at the trench edges and vertical growth in and besides the trenches. Here, a smaller aspect ratio is favorable. Also a regrowth on a template partially masked with SiN was investigated. Here, an increased growth rate adjacent to the masked areas was observed. The Ga and N atoms that do not adhere at the mask, diffuse to the closest GaN surface and incorporate there. In conclusion, the standard MOCVD and MBE growth processes on textured or masked templates do not yield the required homogeneous growth mode.

Based on the previous results, two versions of a CAVET were realized. Both used a Mg-doped CBL with an etched aperture. The first design relied on the regrowth of an AlGaN/GaN heterostructure via MOCVD. The high-temperature MOCVD regrowth induced a significant out-diffusion of Mg which depleted the n-GaN. Thus, the aperture resistance was about 10 M$\Omega$ and dominated the on-state characteristics of the device. Hence, low on-state currents of 0.15 mA/mm were obtained. Despite the high on-resistance, the device exhibited excellent breakdown characteristics with a $V_{BR}$ of 150 V. In conjunction with a thickness of 1 $\mu$m, $V_{BR}$ resulted in an $E_{crit}$ of 3 MV/cm. This value is close to the theoretical maximum of 3.3 MV/cm.

The second design was based on AlGaN/GaN regrowth via MBE. Here, less Mg-diffusion is expected. A saturation of the output characteristics and on-currents of 350 mA/mm were observed. At the same time, the device showed drain-leakage currents in the order of mA/mm, reducing the on/off ratio to 2300. These large leakage currents prevented a high breakdown voltage. Furthermore, several trends as predicted by the simulations could be confirmed. On the one hand, a larger $L_{ap}$ led to increased
leakage, but lower $R_{on}$. On the other hand, an enhanced gate control was observed for larger $L_{GA}$.

So far, the presented devices either showed a large $R_{on}$ and excellent $V_{BR}$ or good on-state characteristics and high leakage currents. In a next step, the p-GaN layer should be realized with Mg implantation. This measure would eliminate the regrowth in the aperture trench. Otherwise, a thinner n-GaN regrowth with MBE is promising, which would suppress major leakage currents at the aperture edges.

In conclusion, this work proved the basic concept of vertical GaN-based devices. However, the performance of GaN-based vertical devices is still below its theoretical limits. To further improve the performance, the development and supply of native GaN substrates has to be enhanced to reduce the defects caused by the heteroepitaxial growth which limits $E_{crit}$. In addition, the maximum thickness of the drift region is limited on foreign substrates. In the process of a CAVET, the regrowth on the CBL and in the aperture has to be further improved. In particular, the regrowth on textured substrates requires a fundamental understanding of the basic processes to finally planarize the surface. In switching applications, the concentrations of traps at the regrowth interface and in particular the Mg diffusion has to be controlled. Otherwise, the reliability of a device is questionable. If the above mentioned challenges can be overcome, the substitution of Si by GaN for high-power electronics can be realized by vertical GaN-based devices.
A. Appendix

A.1. Resistances

The fully MOCVD-regrown VHFET in Sec. 6 exhibited only very low on-state currents. To evaluate the origin of these low currents, the resistances in the device are evaluated. An equivalent circuit diagram which comprises the most important resistances is shown in Fig. A.1. It is assumed that no current flows through the p-GaN CBL. The total resistance includes the following seven different resistances:

- the source contact resistance \( R_{c,s} \),
- the resistance of the lateral 2DEG \( R_{2DEG} \),
- the resistance of the 2DEG in the non-planarized area \( R_{2DEG,ap} \),
- the resistance in the aperture \( R_{ap} \),
- the resistance of the n\(^{-}\)-GaN drift region \( R_{n^{-}} \),
- the resistance of the n\(^{+}\)-GaN contact region \( R_{n^{+}} \),
- and the contact resistance of the drain \( R_{c,d} \).

All resistances are calculated for the presented layer stack (Fig. 6.1) and a geometry with a source and aperture width of 50 \( \mu \)m, an aperture-source distance of 5 \( \mu \)m, and an \( L_{ap} \) of 6 \( \mu \)m.

The contact resistances were measured via TLM and were \( R_{c,s} = 7 \Omega \)mm and \( R_{c,d} = 1.7 \Omega \)mm. From Sec. 2.4.3, the resistance of the n\(^{-}\)-GaN region in this geometry can be calculated to \( R_{n^{-}} = 2.6 \Omega \). The resistance of the n\(^{+}\)-region has been determined with CTLM measurements to \( R_{n^{+}} = 7 \text{ m}\Omega \).

To quantify the remaining three resistances, \( R_{2DEG} \), \( R_{2DEG,ap} \) and \( R_{ap} \), IV measurements on different devices were performed (Fig. A.2). First, \( R_{2DEG} \) was determined by
A.1. Resistances

![Diagram of VHFET](image)

**Figure A.1.** Equivalent circuit diagram of a VHFET.

![Setup diagrams](image)

**Figure A.2.** IV measurements performed on different device designs to quantify the resistances.

IV curves measured between source and drain of a lateral transistor. This one is placed on the same wafer as used for the VHFET (Fig. A.2a). Subsequently, $R_{2DEG,ap}$ was quantified via a lateral measurement on an VHFET through the non-planarized gate region from which, by subtraction of $R_{2DEG}$, $R_{2DEG,ap}$ can be extracted (Fig. A.2b). Here, the total resistance is calculated by:

$$R_{tot} = 2R_{2DEG} + 2R_{2DEG,ap} + 2R_{c,s}$$  \hspace{1cm} (A.1)
$$\leftrightarrow R_{2DEG, ap} = \frac{R_{tot} - R_{2DEG} - R_{c,s}}{2}$$ (A.2)

Ultimately, $R_{ap}$ is calculated by measuring the IV curve from source to drain in the VHFET (Fig. A.2c). Here the total resistance is

$$R_{tot, v} = R_{c,s} + R_{2DEG} + R_{2DEG, ap} + R_{ap} + R_{n^-} + R_{n^+} + R_{c,d}$$ (A.3)

$$\leftrightarrow R_{ap} = R_{tot, v} - R_{c,s} - R_{2DEG} - R_{2DEG, ap} - R_{n^-} - R_{n^+} - R_{c,d}$$ (A.4)

IV curves of the three mentioned measurements are shown in Fig. A.3a. On the left-hand side, the measurements of the lateral configurations are shown, whereas the measurement of the vertical configuration is plotted on the right-hand side.

From the IV characteristics and with Eq. A.2 and Eq. A.4, $R_{2DEG}$, $R_{2DEG, ap}$ and $R_{ap}$ are calculated. Fig. A.3b shows the results for several measurements on the sample. $R_{2DEG}$ is in the range of 500 $\Omega$, $R_{2DEG, ap}$ increases to about 900 $\Omega$. The increase in resistance can either be attributed to the angle of the regrown aperture, because the polarization and thus $n_S$ is angle-dependent [133] or to a reduced $n_S$ due to the depletion by the underlying Mg. As already assumed above, the largest resistance in this case is $R_{ap}$; it reaches about 10 M$\Omega$.

(a) IV characteristics for lateral measurement setups (left) and the vertical setup (right). Please note the different scaling.

(b) Depiction of the major resistances.

Figure A.3.: IV measurement and results of the major resistances $R_{2DEG}$, $R_{2DEG, ap}$ and $R_{ap}$.
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List of abbreviations

BFOM
Baliga’s Figure of Merit. 6, 7, 15, 18–20, 28, 29, 33, 35, 40, 46, 51, 52, 55, 95, 96, 117

BH FOM
Baliga’s High-frequency Figure of Merit. 7

E_C
conduction band minimum. 9, 10, 52, 55

E_F
Fermi level. 8–10, 34

E_g
band gap. 1, 5, 6

E_{crit}
critical electric field. 1, 2, 5–7, 17–20, 28, 32, 39, 46, 50, 51, 89, 90, 94, 97, 98

FOM
Figure of Merit. 7

I_{D,max}
maximum drain current. 61, 72, 87, 91, 92

I_D
drain current. 11, 33, 36, 39, 62, 72, 73, 76, 87–89, 92, 93
List of abbreviations

$I_G$

gate current. 11, 72, 73, 87, 88, 93

$I_s$

saturation current. 21

$L_{GA}$

overlap of gate and aperture. 32, 37–41, 86–95, 98, 117, 119, 120

$L_G$

gate length. 10, 37, 60, 86–88, 91, 119

$L_{ap}$

aperture length. 32, 38–41, 77–82, 85–88, 90–95, 97, 99, 117, 119, 120

$N_A$

acceptor concentration. 14, 19, 20, 53, 54, 85, 96, 117

$N_D$

donor concentration. 13, 16–20, 22, 46–51, 53, 54, 67, 85, 89, 93, 96, 117, 118, 121

$N_c$

doping concentration of the channel region. 32, 34, 35, 37, 38, 40, 117

$N_{CV}$

carrier concentration derived by CV measurements. 22, 54, 63, 69, 118

$N_{drift}$

doping concentration of the drift region. 32–35, 37, 38, 40, 117

$P_{pz}$

piezoelectric polarization. 8

$P_{sp}$

spontaneous polarization. 7, 8, 121
List of abbreviations

$P_{tot}$

total polarization. 8

$R_{2DEG,ap}$

resistance of the 2DEG in the aperture. 89, 99–101, 120

$R_{2DEG}$

resistance of the 2DEG. 89, 99–101, 120

$R_{SH}$

sheet resistance. 68, 69, 72, 119, 121

$R_{ap}$

resistance of the aperture. 87, 89, 90, 94, 99–101, 120

$R_{on}$


$T_R$

room temperature. 13, 14, 48, 58

$V_{BR}$

breakdown voltage. 1–3, 7, 10–12, 15–21, 23, 25, 26, 28, 29, 32, 33, 35–41, 43, 46, 49–55, 85, 89, 93–98, 117

$V_{DS}$

drain-source voltage. 10, 11, 24–26, 35, 37, 39, 40, 61, 87, 117, 118

$V_{GS}$

gate source voltage. 10, 11, 26, 28, 33–40, 61, 72, 76, 87–89, 91, 117, 118

$V_{dc}$

dc bias. 44–46, 96, 118
List of abbreviations

$V_{knee}$

knee voltage. 11

$V_p$

pinch-off voltage. 34–36, 76, 92, 95

$V_{th}$

threshold voltage. 10, 11, 26, 28, 29, 32, 34, 36, 37, 61, 63, 64, 69, 76, 87, 92, 95, 96, 117

$\Phi_B$

Schottky barrier height. 9, 21–23, 47, 48

$\kappa$

thermal conductivity. 5, 6

$\mu$

electron mobility. 2, 5–7, 10, 18, 28, 35, 58, 59, 62–64, 69, 71, 72, 75, 91, 119

$\varepsilon_0$

permittivity of free space. 7

$\varepsilon_r$

relative dielectric constant. 5, 7, 9

$d_c$

channel thickness. 32, 35–38, 40, 117

$d_{GD}$

gate drain separation. 2, 10, 11, 15, 89

$d_{SG}$

source gate separation. 10

$g_{m,max}$

maximum transconductance. 11
List of abbreviations

$g_m$
transconductance. 11, 32, 73, 87, 90, 92

$k$
Boltzmann constant. 21

$n_S$
sheet carrier concentration. 1, 8–10, 29, 34, 36, 58, 59, 61–64, 69, 72–76, 91, 95–97, 101, 119

$n$
electron concentration. 13, 54

$n$
ideality factor. 21, 47, 48, 54

$p$
hole concentration. 14, 54

$t_{\text{bar}}$
barrier thickness. 9

$\rho_C$
specific contact resistance. 46

2DEG
two-dimensional electron gas. 1, 2, 5, 8–10, 24, 25, 28, 29, 31, 34, 35, 37, 43, 58, 64, 65, 68, 71–76, 86, 90–92, 94–97, 99

AFM
atomic force microscopy. 43, 57–59, 67, 68, 74, 79, 80, 118, 119

Al
aluminum. 26
List of abbreviations

Au

gold. 48

BCl₃

boron trichloride. 46, 57

BOE

buffered oxide etch. 57, 62, 67, 73, 85, 90

CAVET

current aperture vertical electron transistor. 2, 3, 23–28, 32, 52, 55, 56, 95–98, 117, 118, 121

CBL

current blocking layer. 2, 3, 24–28, 32, 35–37, 39, 43, 52, 56, 65, 72, 77, 80, 81, 83, 85, 88–90, 92, 96–99

Cl₂

dichloride. 46

Cr

cromium. 45

CTLM

circular transfer length method. 86, 91, 99

CV

capacitance voltage. 22, 23, 43, 46–48, 54, 62–64, 69, 70, 74, 75, 96, 118, 119

d-mode

depletion mode. 87, 89

DC

direct current. 85, 90
**List of abbreviations**

**DIVA**

dynamic IV analysis. 61

**Fe**

iron. 26

**HCl**

hydrochloric acid. 57, 62, 66–68, 73, 85, 90

**HEMT**

high electron mobility transistor. 10

**HFET**

heterostructure field effect transistor. 2, 5, 10, 11, 15, 16, 23, 24, 57–61, 63, 65, 68, 69, 72, 76, 89, 97, 117–119

**HVPE**

hydride vapor phase epitaxy. 11

**ICP**

inductively coupled plasma. 44–46, 57, 62, 85, 90, 121

**IV**

current voltage. 21, 43, 47, 48, 51, 54, 99–101, 118, 120

**JFET**

junction field effect transistor. 28

**KOH**

potassium hydroxide. 45

**MBE**

molecular beam epitaxy. 3, 5, 11–14, 28, 43, 56, 66, 73–77, 81, 82, 84, 85, 90–94, 97, 98, 119
List of abbreviations

**Mg**

magnesium. 13, 14, 65–73, 75, 76, 89, 90, 94, 97, 101, 119

**MOCVD**

metal-organic chemical vapor deposition. 3, 5, 11–13, 26, 28, 43, 46, 53, 56, 57, 62, 64, 66, 72, 73, 76–81, 83–87, 90, 93, 94, 96, 97, 99, 119

**MOSFET**

metal oxide semiconductor field effect transistor. 2, 15, 24, 28, 29

**N₂**

nitrogen. 11, 13, 46

**Ni**

nickel. 48

**RF**

radio frequency. 12, 13, 44

**RIE**

reactive ion etching. 44, 46, 121

**rms**

root mean square. 57, 62, 67, 68, 74, 79

**scr**

space-charge region. 7, 17–19, 22, 26, 29, 35, 49, 50, 53–55

**SEM**

canining electron microscopy. 43, 45, 78, 82, 83, 118, 119

**Si**

silicon. 1, 2, 5–7, 12, 13, 15, 16, 66, 98
List of abbreviations

SiC
silicon carbide. 2, 5, 7, 15, 16

SIMS
secondary ion mass spectrometry. 72

SiN
silicon nitride. 28

SiO₂
silicon oxide. 28

TLM
transfer length method. 86, 91

UID
unintentionally doped. 34, 46–48, 50, 62, 73, 74

VHFET
vertical heterostructure field effect transistor. 15, 23, 24, 43, 46, 64, 65, 77, 81, 85–94, 99–101, 117, 119, 120

VSD
vertical Schottky diode. 15–19, 44, 46–48, 50–52, 88, 117, 118, 121

XRD
X-ray diffraction. 74
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