

A Contribution to Continuous-Time Quadrature Bandpass Sigma-Delta Modulators for Low-IF Receivers

Von der Fakultät für Elektrotechnik und Informationstechnik
der Rheinisch-Westfälischen Technischen Hochschule Aachen
zur Erlangung des akademischen Grades eines
Doktors der Ingenieurwissenschaften
genehmigte Dissertation

vorgelegt von

M.Sc.
Song-Bok Kim
aus S. Hamgyong, DPR Korea

Berichter: Univ.- Prof. Dr.-Ing. Stefan Heinen
Univ.- Prof. Dr.-Ing. Maurits Ortmanns

Tag der mündlichen Prüfung: 17. April 2009

Diese Dissertation ist auf den Internetseiten der Hochschulbibliothek
online verfügbar.

to my motherland and my family,

Contents

	iii
1. Introduction	1
1.1. Motivation of This Work	1
1.2. Goal of This Work	2
1.3. Structure of This Work	2
2. Overview of RF Receivers and $\Sigma\Delta$Ms	5
2.1. Integrated Receiver Architectures	5
2.1.1. Superheterodyne Receiver	5
2.1.2. Zero-IF Receiver	6
2.1.3. Low-IF Receiver	7
2.2. CT Sigma-Delta Modulators	9
2.2.1. CT Lowpass $\Sigma\Delta$ M	10
2.2.2. CT Real Bandpass $\Sigma\Delta$ M	11
2.2.3. CT Quadrature Bandpass $\Sigma\Delta$ M	11
3. Design of CT-QBP $\Sigma\Delta$M	15
3.1. Design Methodology	15
3.1.1. Direct Method	17
3.1.1.1. $NTF_{QBP}(z)$ for QBP $\Sigma\Delta$ M	17
3.1.1.2. CT Complex Loop Filter $H_{PPF}(s)$	17
3.1.2. Indirect Method	19
3.1.3. Inverse Method	19
3.1.3.1. Optimization Process	19
3.1.3.2. CT-DT Equivalents	20
3.1.3.3. Estimation of $NTF_{QBP}(z)$	21
3.2. Simulation for CT-QBP $\Sigma\Delta$ M	22
4. CT-QBP $\Sigma\Delta$Ms with CICFF Topology	25
4.1. Overview for Polyphase Filter	25
4.2. Lowpass Filter with CICFF topology	30
4.3. Polyphase Filter with CICFF topology	33
4.4. Implementation of Polyphase Filter	37

5. Analysis of Nonidealities	43
5.1. Finite Gain Bandwidth	43
5.1.1. Stability of the Complex Integrator	44
5.1.2. Deviation from the Center Frequency	48
5.1.3. Polyphase Filter with CIFF and CICFF Topologies	49
5.1.4. Compensation of the Deviation from the Center Frequency . . .	53
5.2. Excess Loop Delay	54
5.2.1. Analysis of Excess Loop Delay	55
5.2.2. Effects of Excess Loop Delay	57
5.2.3. Compensation of Excess Loop Delay	59
5.3. Mismatched Loop Delay	64
5.3.1. Effect of Mismatched Loop Delay	64
5.3.2. Continuous-Discrete Transformation	65
5.3.3. Compensation of Mismatched Loop Delay	72
5.3.3.1. Ratio of Center Frequency to Sampling Frequency . . .	72
5.3.3.2. Compensation Method	73
5.4. Clock Jitter	75
5.4.1. Clock Jitter in CT-QBP $\Sigma\Delta$ M	76
5.4.2. Power Spectral Density of Error Signal by Clock Jitter	79
5.4.3. SNR Estimation of CT-QBP $\Sigma\Delta$ M	81
5.5. Nonlinearity of Multibit DAC	83
5.5.1. Complex Tree-Structured DAC	87
5.5.2. Complex Mismatch Shaper	88
5.5.3. Implementation of Complex Mismatch Shaper	90
6. Application Examples	97
6.1. CT-QBP $\Sigma\Delta$ M for GSM/EDGE Low-IF Receiver	97
6.1.1. Polyphase Filter Design	97
6.1.2. Modulator Design	99
6.1.3. Modulator Nonidealities	100
6.1.3.1. Sensitivity to RC-Product Variation	100
6.1.3.2. Excess Loop Delay	101
6.1.3.3. Clock Jitter	102
6.1.3.4. Finite GBW	102
6.2. CT-QBP $\Sigma\Delta$ M for GPS/Galileo Low-IF Receiver	105
6.2.1. Polyphase Filter Design	106
6.2.2. Modulator Design	108
6.3. Circuit Implementation	110
6.3.1. Integrator Design	110
6.3.2. Quantizer and Feedback DAC	111
6.3.3. Calibration of RC-Product	111
6.4. Chip Implementation	113

7. Measurement Results	115
7.1. Measurement Setup	115
7.2. Dynamic Range and SNDR	116
7.2.1. GSM/EDGE Application	116
7.2.2. GPS/Galileo Application	117
8. Conclusion	123
Bibliography	127
A. Appendix	139
A.1. Abbreviations	139
A.2. Subroutine List	141
A.3. Publications	146
A.4. Acknowledgements	148
A.5. Curriculum Vitae	149

List of Figures

2.1. Superheterodyne receiver architecture	6
2.2. Homodyne receiver architecture	7
2.3. Low-IF receiver architecture	8
2.4. Architecture of CT lowpass $\Sigma\Delta$ M.	10
2.5. Architecture of CT-RBP $\Sigma\Delta$ M.	11
2.6. Architecture of CT-QBP $\Sigma\Delta$ M.	12
2.7. CT-QBP $\Sigma\Delta$ M in low-IF receivers.	12
3.1. Design methodology for CT-QBP $\Sigma\Delta$ M.	16
3.2. Magnitude response and placement of pole ($\times$) and zero (o) of the $NTF_{QBP}(z)$	18
3.3. CT-DT equivalent diagram.	21
4.1. Implementation of the polyphase filter by frequency shifting from the lowpass filter.	25
4.2. Single polyphase filter obtained by two lowpass filters.	26
4.3. Lowpass CT $\Sigma\Delta$ M architecture with CIFB a) and CIFF topology b).	28
4.4. Loop filter with capacitive feedforward structure.	29
4.5. Loop filter with capacitive feedforward structure.	30
4.6. Local feedback loop.	31
4.7. Implementation of capacitive feedforward summation.	32
4.8. Cross-coupling in cascaded local feedback loops.	34
4.9. Compensation cross-couplings in last stage. Here $y_i = y_{I,i} + jy_{Q,i}$	36
4.10. Fourth-order polyphase filter with the CICFF topology.	38
4.11. Amplitude and phase response of fourth-order polyphase filter.	40
4.12. Poles and zeros of the equivalent NTF_{QBP}	41
5.1. Complex integrator with additional voltage sources caused by finite GBW.	43
5.2. The dominant pole locus of the complex integrator with $f_c=5$ MHz. The arrow denotes the increasing direction of GBW. $GBW=\eta \cdot 2\pi f_s$ with $\eta = 1 \sim 10$, and the step size of η is 1.	45
5.3. The dominant pole locus of the complex integrator with $a_i = 0.5 \cdot 2\pi f_s$	45
5.4. The open-loop gain of the equivalent amplifier of the lossy integrator.	46
5.5. Pole placement with $w_{g,i}$. Here, $GBW=4 \cdot 2\pi f_s$, $a_i = 0.5 \cdot 2\pi f_s$	46

5.6. The dominant pole locus of the complex lossy integrator, with $a_i = 0.5 \cdot 2\pi f_s$.	47
5.7. The shifted complex integrator with different GBW, where $a_i = 1.0 \cdot 2\pi f_s$, $f_c = 0.05 \cdot 2\pi f_s$ and $\eta = GBW_i/(2\pi f_s)$.	48
5.8. The relative deviation between $f_{c,r}$ and f_c , where $f_c = 0.05 \cdot 2\pi f_s$.	49
5.9. The second-order polyphase filter with finite GBW.	50
5.10. The amplitude response of the second-order polyphase filter with finite GBW, where $f_c = 0.1 \cdot 2\pi f_s$, $w_{g,1} = 0.01 \cdot a_1$ and $w_{g,2} = 0.01 \cdot a_2$.	51
5.11. The relative deviation in the last stage of CICFF topology, when $f_c = 0.05 \cdot 2\pi f_s$, $a_n = 0.5 \cdot 2\pi f_s$ and $w_{g,n} = 0.02 \cdot a_n$.	51
5.12. The NTF_{QBP} of the second-order CT-QBP $\Sigma\Delta$ with finite GBW.	52
5.13. The compensation by transconductors in the complex integrator inputs.	53
5.14. The reduced relative deviation from f_c , where $f_c = 0.05 \cdot 2\pi f_s$.	54
5.15. CT complex $\Sigma\Delta$ modulator with nonzero-delayed NRZ.	56
5.16. Output spectrum, (up) zero delayed, (down) 50% delayed when $f_c = 2$ MHz.	58
5.17. SNR vs. the excess loop delay τ_d/T_s .	58
5.18. The root-locus of $NTF_{QBP}(z)$ vs. τ_d/T_s , ($= 0.1 - 1.0$) when $f_c = 2$ MHz.	59
5.19. The compensation scheme of excess loop delay.	60
5.20. The second-order CT-QBP $\Sigma\Delta$ with compensation scheme of excess loop delay.	62
5.21. The SNR vs. τ_d/T_s when using the coefficients in Table 5.4.	63
5.22. The output spectrum when $\tau_d/T_s = 0.8$ and $f_c = 2MHz$.	64
5.23. CT second-order complex $\Sigma\Delta$ modulator with nonzero-delayed and mismatched DAC pulses.	65
5.24. Output spectrum of modulator with nonzero delayed- and mismatched-feedback NRZ DAC pulses.	66
5.25. CT-QBP $\Sigma\Delta$ with mismatched loop delay.	66
5.26. DAC pulses in real and imaginary paths.	67
5.27. Mismatched feedback paths (a) in CT-domain, (b) equivalent in DT-domain.	69
5.28. DT-equivalent of CT-complex $\Sigma\Delta$ modulator with nonzero-delayed and mismatched DAC pulses.	70
5.29. Amplitude response of second-order NTF and MTF, when $T_{d,I} = 0.4T_s$, $T_{d,Q} = 0.8T_s$ and $f_s = 64MHz$.	73
5.30. Amplitude response in different center frequencies when $f_s = 64MHz$.	74
5.31. The degradation of SNR vs. mismatched loop delay, in different center frequencies when $f_s = 64MHz$.	74
5.32. CT-QBP $\Sigma\Delta$ with clock jitter.	76
5.33. Simulation model of the CT-QBP $\Sigma\Delta$ with clock jitter.	82
5.34. SNR of the second-order CT-QBP $\Sigma\Delta$ with the jitter-induced noise.	83
5.35. The number of the output bit transitions vs. input level.	84

5.36. The nonlinear error of the SNR vs. input level.	84
5.37. Multibit complex $\Sigma\Delta$ modulator.	85
5.38. Complex DAC bank.	86
5.39. Tree-structured complex DAC.	87
5.40. Complex mismatch shaper.	89
5.41. First-order complex mismatch shaper.	90
5.42. Modified first-order complex mismatch shaper.	93
5.43. First-order shaped power spectrum of layer-1 switching sequence $s_{1,r}$	94
5.44. Output power spectrum of multibit complex $\Sigma\Delta$ modulator.	95
6.1. Polyphase filter for GSM/EDGE ADC.	98
6.2. Frequency response of the designed polyphase filter.	98
6.3. CT-QBP $\Sigma\Delta$ M with CICFF topology.	99
6.4. Placement of the poles and zeros of the NTF.	100
6.5. The equivalent NTF by RC-product variations.	101
6.6. SNDR loss vs. RC-product variations.	102
6.7. The placement of pole and zero vs excess loop delay. The arrow denotes the increasing direction of excess loop delay.	103
6.8. SNDR loss vs. excess loop delay.	103
6.9. SNDR loss vs. clock jitter variance.	104
6.10. The equivalent NTF with finite GBW.	104
6.11. The placement of poles and zeros of the NTF.	105
6.12. SNDR loss vs. finite GBW.	106
6.13. Polyphase filter for GPS/Galileo application.	107
6.14. DT equivalent NTFs for GPS/Galileo application.	109
6.15. OpAmp with continuous-time CMFB.	111
6.16. Single-bit quantizer.	112
6.17. Quantized capacitor array and calibration of RC-product.	112
6.18. Chip micrograph for GSM/EDGE low-IF receiver.	113
6.19. Chip micrograph for GPS/Galileo low-IF receiver.	114
7.1. Measurement setup.	115
7.2. Measured single bit-streams of the I/Q paths for GSM/EDGE.	117
7.3. Measured modulator output spectrum for GSM/EDGE	118
7.4. SNDR vs. input signal level for GSM/EDGE.	119
7.5. Measured modulator output spectrum for GPS/Galileo.	119
7.6. SNDR vs. input signal level for GPS/Galileo.	120

List of Tables

4.1. Component values	40
5.1. The feedback coefficient k_{c0} vs. τ_d	61
5.2. The feedforward coefficient k_{c1} vs. τ_d	61
5.3. The feedforward coefficient k_{c2} vs. τ_d	62
5.4. The approximated k_{c0} , k_{c1} and k_{c2} vs. τ_d	63
6.1. modulator parameter	99
6.2. Component Values for GPS/Galileo	109
7.1. IC Performance for GSM/EDGE	120
7.2. IC Performance for GPS/Galileo	121

1. Introduction

1.1. Motivation of This Work

During the last two decades, there has been no event that would have affected as many people as the cultural changes related to public mobile wireless communications all around the world. For example, GSM (Global System for Mobile communications) is the most popular standard for mobile phones in the world. Its promoter, the GSM Association, estimates that 82% of the global mobile market uses the standard. GSM is used by over 3 billion people across more than 212 countries and territories. With communication technology developing in different parts of the world and powerfully driven trend by different economic interests, a large variety of communication methods and standards have been matured. The numerous standards defined for wireless communication have the different signal bandwidths and a demand of the different dynamic ranges.

Today, mobile terminals such as cellular phones (GSM/UMTS/WCDMA), PDAs and notebooks need to take seamless access to a multitude of available services through a single mobile terminal. This increases the demands of multistandard and multimode architectures. Since the next generation mobile communication (4G) is a collection of wireless standards, the final form of a 4G device will constitute various standards. This can be efficiently realized using software-defined radio (SDR) technology, which is categorized to the area of the radio convergence. The multistandard and multimode radio-frequency (RF) transceivers work in switchable parallel paths or reconfigurable architectures which are embedded on a chip. The switchable parallel architecture can reduce power consumption, but it increases the chip area. On the other hand, the reconfigurable architecture can reduce both power and chip area but increases circuit complexity.

The mobile multimedia communication (MMC) where voice, data and streamed multimedia can be given to users on an "Anytime, Anywhere" basis, brings the requirement of high-speed data processing, and makes demand of wideband signal processing in mobile terminals.

The limited battery life and online access with communication networks need to have reduced power consumption in the mobile terminals. Therefore, the terminals have to be designed with low power architectures and circuit techniques. For the sake of low cost in mobile terminals, off-chip components and highly precise components such as SAW filter should be reduced or replaced into the chip which are produced

by a standard CMOS technology. CMOS circuit techniques with high integration are thus required. With rapid development of CMOS technology, the transistor size continuously scales down, and therefore the supply voltage of mobile terminals will be reduced. This leads the additional design efforts for low supply voltage application.

It is important to choose a feasible transceiver architecture which satisfies above requirements, such as multistandard and multimode, high speed and wideband, high integration, low power, low voltage and deep submicron. Analog-to-digital converter (ADC) and digital-to-analog converter (DAC) provide the interface between analog and digital blocks in RF transceivers. Therefore, ADCs and DACs should also be designed, satisfying the mentioned demands.

1.2. Goal of This Work

Sigma-delta ($\Sigma\Delta$) ADC is a method for encoding high resolution signals into lower resolution signals using pulse-density modulation. This technique has found increasing use in a range of modern electronic components, such as ADCs and DACs, frequency synthesizers, switched mode power supplies and motor controls. One of the earliest and most widespread uses of sigma-delta modulator ($\Sigma\Delta M$) is in data conversion for wireless [HLH⁺02] and wireline [dRdlRPV⁺04] applications as well as audio [FWG01], industrial measurement [BP98] and biosensor read-out [AVG⁺07]. An ADC or DAC circuit which implements this technique can easily achieve very high resolution, using low-cost CMOS processes and digital signal processing techniques. For this reason, even though it was first presented in the early 1960s, it is only in recent years that it has come into widespread use with improvements in silicon technology and the large digital signal processing circuitry. Almost all analog integrated circuit vendors offer sigma delta converters.

In RF receivers, AD conversion can be implemented by using $\Sigma\Delta$ ADCs which have inherently high resolution due to the oversampling and noise shaping techniques. Especially, continuous-time (CT)-quadrature bandpass (QBP) $\Sigma\Delta M$ s are suited in low-IF receivers which have several advantages of wireless architecture.

In this work, we will focus the implementation of CT-QBP $\Sigma\Delta M$ for low-IF receivers. The goal of this work is to design CT-QBP $\Sigma\Delta M$ which is aimed for low power and low voltage.

1.3. Structure of This Work

The outline of this work is as follows:

- Following this introduction, Chapter 2 will give more details on the background of this work. Starting from the consideration concerning with RF integrated receiver architectures, their advantages and disadvantages will be compared. In

next section, $\Sigma\Delta$ M are categorized and estimated, based on previously published literatures. Why CT-QBP $\Sigma\Delta$ M is desired for wireless communication is described in Chapter 2.

- Chapter 3 gives the design methodology for CT-QBP $\Sigma\Delta$ Ms which have started CT optimized loop filter and afterward discrete-time equivalents are obtained and estimated. Finally the simulation method in Matlab is discussed.
- Chapter 4 illustrates the implementation of the polyphase filter by frequency shifting from the lowpass filter. For the sake of low power and low voltage, the polyphase filter with capacitive feedforward summation is proposed. In the last section, the implementation of the fourth-order polyphase filter is listed as example.
- Chapter 5 analyses the effects of nonidealities, such as finite gain bandwidth of the amplifiers, excess loop delay, mismatched loop delay, clock jitter and mismatch in multi-bit DAC bank. Based on theoretical consideration, the methods to compensate and reduce the effects of nonidealities are proposed.
- Chapter 6 presents examples for applications of this work. Wideband CT-QBP $\Sigma\Delta$ M for the reconfigurable multimode GPS/Galileo receiver, and high-resolution medium-band CT-QBP $\Sigma\Delta$ M for GSM/EDGE receiver are designed and illustrated. They contain polyphase filter with capacitive feedforward summation proposed in Chapter 4.
- Chapter 7 shows the measurement results of the test chips which were designed in a $0.25\ \mu\text{m}$ CMOS technology. The measurement results demonstrate the effectiveness of the proposed CT-QBP $\Sigma\Delta$ Ms for low-IF receivers.
- Chapter 8 concludes this thesis with a brief summary of the work.

2. Overview of RF Receivers and $\Sigma\Delta$ Ms

This chapter will first give a brief overview on integrated receiver architectures for wireless communication. Continuous-time sigma-delta modulators which can be applied in wireless receivers will be presented. The problems which should be solved in this work will be finally summarized.

2.1. Integrated Receiver Architectures

In wireless communication, the receiver systems operate typically with carrier frequencies at many hundreds of megahertz to several gigahertz. Directly converting the antenna signals to digital form in an integrated analog-to-digital converter (ADC) would require large sensitivity, selectivity, and very high conversion speed. Therefore, the received radio frequency (RF) signals have to be converted to lower frequencies, for signal processing step like channels selection, amplification and data conversion.

2.1.1. Superheterodyne Receiver

The superheterodyne mode is most commonly employed in current wireless communication and its operating way is very well known [Raz01], [RFP⁺06], [CWW07].

An example is shown in Figure 2.1. The out-of-band blocking signals are suppressed by an off-chip RF bandpass filter placed after the antenna. The signal is then amplified by a low noise amplifier (LNA). The bandpass filter is usually insufficient to attenuate the signal at the image frequency to the system noise level, so a second off-chip image filter is inserted prior to the mixer. The mixer with a tunable local oscillator (LO_1) downconverts the desired signal from the RF to an intermediate frequency (IF).

Once the signal is downconverted to IF, it has to be filtered in order to extract the wanted signal from the neighboring channels. The off-chip high-Q filter is used for channel selection. A second downconversion mixer translates the selected signal to baseband and the signal is filtered further by integrated lowpass channel selection filter. Then, the signal is converted to the digital signal by an ADC. Finally it is demodulated by the digital signal processor (DSP).

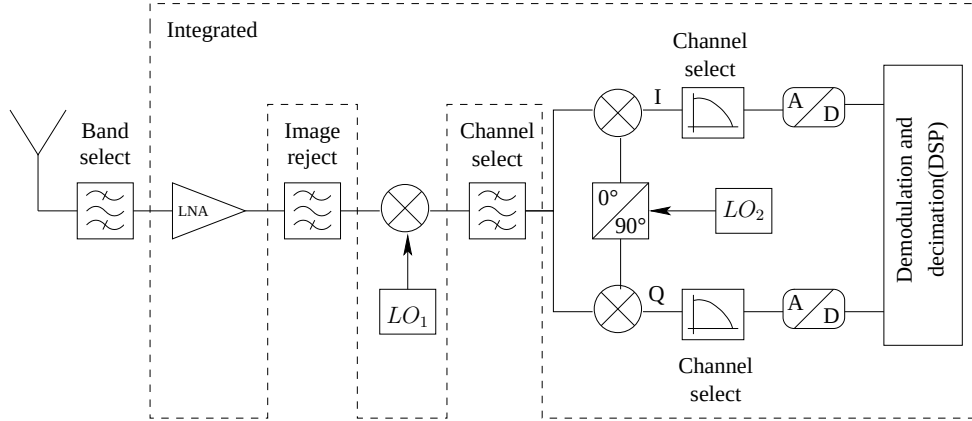


Figure 2.1.: Superheterodyne receiver architecture

In this architecture, even though more analog integrated IF filters were published [AAW⁺04], [ZTJ⁺04], for most applications they are still not good enough. Off-chip passive components provide filters with a high-Q factor. This results in good performance for both sensitivity and selectivity and makes the heterodyne architecture a common choice. However, off-chip filtering comes to the price of extra signal buffering (typically driving 50 Ohm load), increasing complexity, higher power consumption and larger size.

2.1.2. Zero-IF Receiver

In zero-IF (Homodyne) receiver architectures, the wanted signal is directly downconverted to baseband. The IF is chosen to be zero. Because of its simplicity, it appears to offer one of the best opportunities for integrated systems. Some examples of its use in wireless systems do exist today [LLM⁺06],[MLD⁺08], but it is not as simple in practice. Figure 2.2 shows this architecture. An off-chip RF bandpass filter is placed at the input for band selection. The LNA's output is passed to the mixer. The LNA must be able to handle the same dynamic range as for the superheterodyne architecture and it must have enough gain to amplify weak signal above the noise of the mixer. The mixer converts the received signal directly to baseband. Channel selection is done by tuning the frequency of the LO to the center of the desirable channel, making the image equal to the desirable channel. Hence, the problem of images is not present, and the off-chip IF filter can be omitted. The subsequent channel filtering can be carried out by lowpass baseband filter, in order to remove neighboring channels or interferers prior to ADC. Because all channel energy is untreated before channel filtering, this channel filter and ADC have a sharp cutoff profile and high linearity, respectively.

The main issue in zero-IF is the DC offsets which are created during the downconversion [Fau02]. It is mainly a result of the crosstalk between the RF and LO inputs

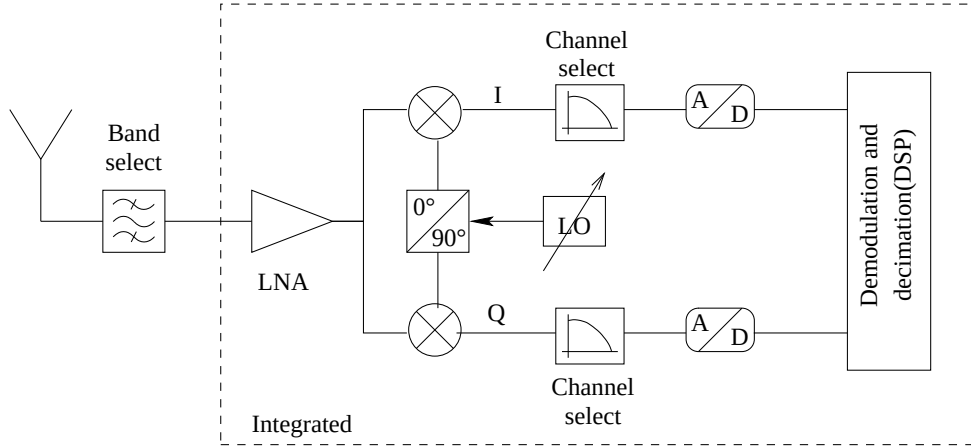


Figure 2.2.: Homodyne receiver architecture

of the mixer. If one of these mixer inputs contains the same signal component as the other, the multiplication gives a DC (or almost DC) signal. Caused by leakage from the local oscillator to the LNA or vice versa, self-mixing will corrupt the baseband signal at DC. Furthermore, the offsets by self-mixing are time-varying-offsets. These offsets need to be compensated. One technique is to disregard a small part of the signal band close to DC and employ a high-pass filter with very sharp cutoff at low corner frequency. This requires large time constants and hence, large capacitor. It is only practical for wide-band applications. For narrow-band applications, it would cause large performance losses. Compensation can be carried out either prior to the ADC or in the digital domain using digital-to analog conversion in a feedback path.

Because of direct conversion to DC, the zero-IF receivers are more susceptible to disturbances arising from I/Q phase mismatches, nonlinearities and flicker noise than heterodyne designs [Fau02],[VS08],[MLD⁺08]. To alleviate the performance loss, additional circuitry and design efforts are required. However, there is no need for image rejection or other off-chip filters. Its monolithic integration capabilities make the zero-IF architecture an attractive alternative for wireless receivers.

2.1.3. Low-IF Receiver

The development of low-IF receiver starts from the perception that it must be possible to realize a receiver which combines the advantages of above both known receiver types [CS98b], [AIO02], [BFC⁺02], [GMPMOG08], [Gro08], [MPJ⁺08]. Figure 2.3 shows the example of the low-IF receiver architecture. An off-chip bandpass filter performs band selection prior to amplification by the LNA. In order to overcome the drawbacks associated with the zero-IF architecture, the RF signal is downconverted to a frequency close to baseband, but not including DC (typically between several 100 kHz and a few megahertz, i.e., one or two times the signal band). Hence the

problem of DC-offset is eliminated, and the effects of flicker noise of MOS transistors and distortion are notably reduced.

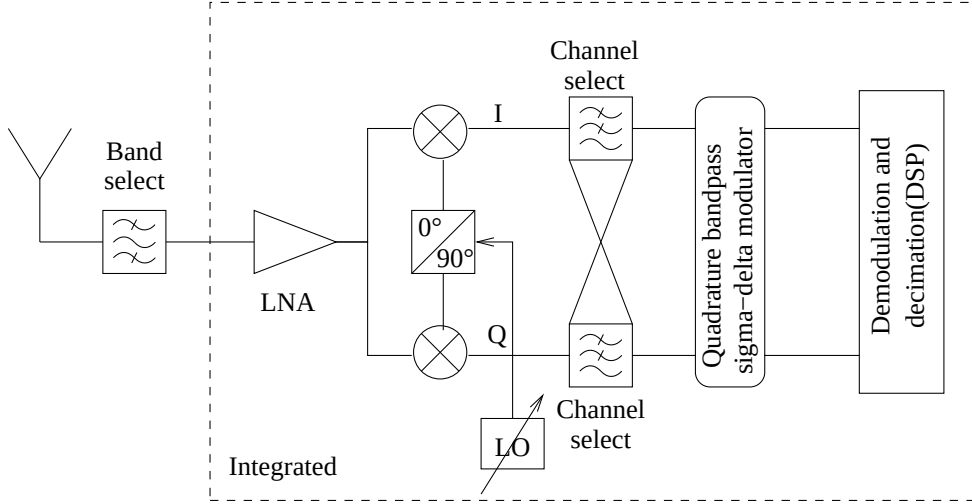


Figure 2.3.: Low-IF receiver architecture

The wanted and mirrored signals are downconverted to the IF, but both signals are not superimposed on each other due to complex combination. If the wanted signal is situated at positive or negative frequencies, the mirrored signal would be inversely situated at negative or positive frequencies. Therefore, the problem of images is not presented as zero-IF architecture. Furthermore, the downconversion is done in a single step and all subsequent filtering can be performed on-chip. This improves integration capabilities. Similar to zero-IF, a tuneable local oscillator selects the desirable RF channel through mixing. However, the image from downconversion is now different from the wanted signal and it has to be taken care of processing after the mixing stage. This can be achieved with an integrated polyphase filter (sometimes called complex filter), or real bandpass filter.

In low-IF receivers using polyphase filter, the mirrored signal is firstly suppressed with the polyphase filter which is centered around IF. After the polyphase filter, the wanted signal is separated from the neighboring channels and is ready for sampling. The required dynamic range (DR) of the ADC is the same as for zero-IF receiver.

On the other hand, in low-IF receiver using a real bandpass filter, the filter is used to separate both the wanted and the mirrored signals from their neighbors. After the bandpass filter, the signal is ready for sampling. In this case, not only the wanted signal, but also the wanted signal together with the mirrored signal, is sampled. The mirrored signal can be 20-30 dB higher than the wanted signal. In high-quality applications, the 4-5 extra bit precision in the ADC DR is required more than polyphase filter. Finally the mirrored signal is removed by lowpass filter in the digital domain.

2.2. CT Sigma-Delta Modulators

The performance of digital signal processing and communication systems is generally limited by the precision of the digital input signal which is achieved at the interface between analog and digital information. The AD conversion technology based on $\Sigma\Delta$ modulation is a cost effective alternative for high resolution (greater than 12 bits) converters which can be ultimately integrated on digital signal processor ICs. A requirement of analog-to-digital interfaces is compatibility with VLSI technology, in order to provide monolithic integration of both the analog and digital sections on a single chip. Since $\Sigma\Delta$ ADCs are based on digital filtering techniques, almost 90% of the chip is implemented in digital circuitry which enhances the prospect of compatibility.

In general, $\Sigma\Delta$ ADCs consist of the modulator and the decimator. The former works in mixed signal domain, while the later works in digital domain. In wireless communication, the decimation of the oversampled digital signal can be implemented by DSP. $\Sigma\Delta$ Ms have two techniques such as oversampling and noise shaping. The oversampling technique effectively reduces floor noise power and noise shaping technique moves the passband noise reduced by oversampling to high frequency. Therefore, $\Sigma\Delta$ ADC is a most effective alternative.

There are two possibilities to design $\Sigma\Delta$ Ms; one is discrete-time (DT) implementation based on switched-capacitor (SC), the other is CT implementation. The earliest implementations of $\Sigma\Delta$ Ms used CT loop filters, but since the advent of SC circuits in 1980s the majority of $\Sigma\Delta$ Ms have been constructed with SC loop filters. SC filters are attractive because they exhibit both good accuracy and good linearity. In addition, the different equations which describe SC circuit are dependent of the clock rate, and hence the transfer function of SC circuits is scaled naturally with the clock frequency.

In contrast to the discrete-time (DT) loop filters, CT filters generally have inferior linearity and accuracy. The RC-products (time-constants) of a CT filter are subjected to large variation and furthermore do not track the clock rate. Despite the above disadvantages, the $\Sigma\Delta$ Ms employing CT elements in their loop filters are appearing frequently in both the literature and the marketplace. Especially, CT $\Sigma\Delta$ Ms are widely used in wireless and wireline communication [Kap03], [YS04], [AKP⁺06], [PDGH⁺04], [SDRP04]. The reasons are as follows:

- In CT architectures, an anti-aliasing filter can be removed because CT loop filter acts as anti-aliasing filter. Thus, it provides a reduced power consumption and chip area.
- Due to the sampled processing in SC techniques, the loop filters need integrators with high gain bandwidth product (GBW)[TMRPW03] and high slew rate for step impulse response. They increase the power consumption of the amplifiers, therefore, total power of the modulator.
- DT $\Sigma\Delta$ Ms are not suited for wideband and high speed application[PDGH⁺04].

Due to the demand of relaxed sampling in CT $\Sigma\Delta$ Ms, it is possible to implement high-speed, wide-band data conversion. In practice, a CT modulator can operate with a clock frequency (and thus achieved wide signal bandwidth) which is 2-4 times faster than the frequency which can be achieved with SC techniques.

- Performance limitations which are introduced by signal swing dependent on-resistance of the switches, glitch-induced noise and the generated digital switching noise can be less problematic [OG06].

Hence, in this overview, the implementation of CT $\Sigma\Delta$ Ms will be focused for the sake of the design of CT quadrature bandpass (CT-QBP) $\Sigma\Delta$ M. There are three kinds of CT $\Sigma\Delta$ Ms, such as the lowpass, the real bandpass and quadrature bandpass $\Sigma\Delta$ Ms.

2.2.1. CT Lowpass $\Sigma\Delta$ M

The design methodology of CT lowpass $\Sigma\Delta$ Ms is well known[NST96],[ST04]. Figure 2.4 shows CT lowpass $\Sigma\Delta$ M. It consists of a CT loop filter $H(s)$, a sampler, a quantizer, and a feedback DAC. The quantization error is suppressed by the feedback loop and removed from the analog bandwidth.

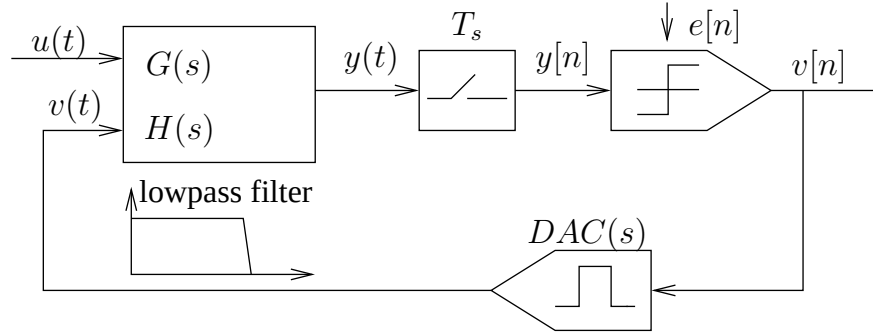


Figure 2.4.: Architecture of CT lowpass $\Sigma\Delta$ M.

In superheterodyne and homodyne receivers, the received signals are down-converted into the baseband by the mixers. Therefore, CT baseband $\Sigma\Delta$ Ms based on the lowpass loop filter are widely used in wireless applications [DKG⁺05], [SDRP04], [BvdZDH00]. CT lowpass $\Sigma\Delta$ Ms have also been employed in wireline applications such as xDSL [PDGH⁺04], [dRdlRPV⁺04], [dlREPV⁺05], as well as, audio application [FWG01], industrial measurement [BP98] and biosensor array readout [AVG⁺07].

Unfortunately, CT lowpass $\Sigma\Delta$ Ms suffer from the baseband noise sources such as $1/f$ noise and DC offset which are introduced by transistors and amplifiers, therefore the performance of modulator can be reduced. Furthermore, for low-IF receivers, the AD conversion by CT lowpass $\Sigma\Delta$ Ms is inadequate.

2.2.2. CT Real Bandpass $\Sigma\Delta$ M

CT real bandpass (CT-RBP) $\Sigma\Delta$ Ms have been used to digitize the IF signal in wireless receivers [GS98], [HK00]. These modulators are based on CT real bandpass filter as shown in Figure 2.5. Compared to CT lowpass $\Sigma\Delta$ Ms, BP $\Sigma\Delta$ Ms have the advantages of being free from interferences such as DC offset, $1/f$ noise and relaxed I/Q mismatch. CT-RBP $\Sigma\Delta$ Ms can be realized by OpAmp-RC, transconductor-C (Gm-C) and inductance-capacitance (LC) filters. In general, the IF signal is centered at $1/4$ of

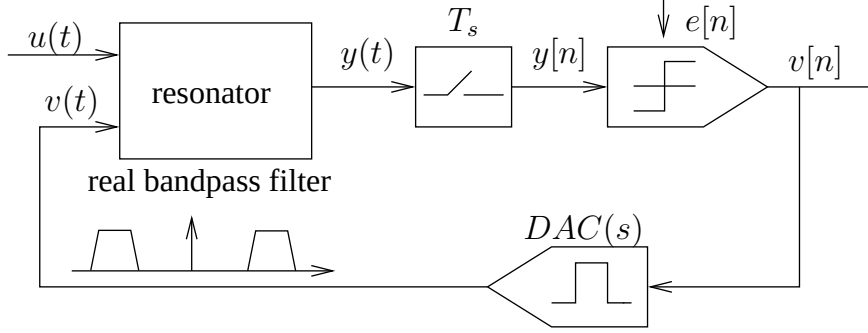


Figure 2.5.: Architecture of CT-RBP $\Sigma\Delta$ M.

the sampling clock f_s . A high resonance quality factor is needed for high resolution CT-RBP $\Sigma\Delta$ Ms. Therefore, the resonators with OpAmp-RC and Gm-C are limited in some applications. Furthermore, in order to obtain the same performance with quadrature bandpass $\Sigma\Delta$ M, the order of CT-RBP $\Sigma\Delta$ M should be increased twice as much as counterpart [CS98b]. LC filter-based converters have generally been relied on off-chip inductors since it is difficult to construct linear high Q LC resonators on chip, increasing the cost.

2.2.3. CT Quadrature Bandpass $\Sigma\Delta$ M

CT quadrature bandpass sigma-delta modulators (CT-QBP $\Sigma\Delta$ Ms) offer the best favorable opportunity for AD conversion implementation in low-IF receivers [HLH⁺02], [EBRB03], [KJZ⁺07]. It is based on polyphase filters as shown in Figure 2.6. There are several advantages as follows:

- An anti-aliasing filter can be removed because CT polyphase filter acts as anti-aliasing filter.
- It is possible to realize high-speed and wideband conversion due to the CT implementation.
- CT-QBP $\Sigma\Delta$ Ms directly perform the AD conversion of quadrature analog I/Q signal within the signal bandwidth around IF. Therefore, they make a freedom from problem of $1/f$ noise and DC offsets.

- AD conversion with programmable bandpass and IF is possible.
- In contrast to RBP $\Sigma\Delta$ Ms, the hardware cost reduces by one-half, with relaxed modulator criterion.

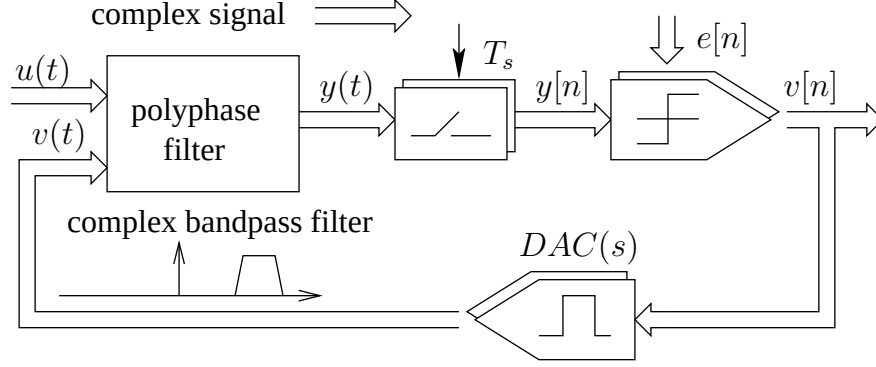


Figure 2.6.: Architecture of CT-QBP $\Sigma\Delta$ M.

Analog polyphase filter can be done with all available implementation techniques for filters, as there are OpAmp-RC [HLH⁺02],[KJZ⁺07], Gm-C [AKP⁺06],[EBRB03], OTA-RC, MOSFET-C, and SC[JMS97]. Which technique is most appropriate depends on specification imposed by the application.

The low-IF receiver architecture is best suited for wireless applications, because it combines the advantages of the other architectures. Especially, CT-QBP $\Sigma\Delta$ Ms are suited in low-IF receivers. In some low-IF applications, the channel selection filter for suppressing neighbors can be removed [HLH⁺02], because the high-Q polyphase filter for CT-QBP $\Sigma\Delta$ Ms can suppress them as shown in Figure 2.7.

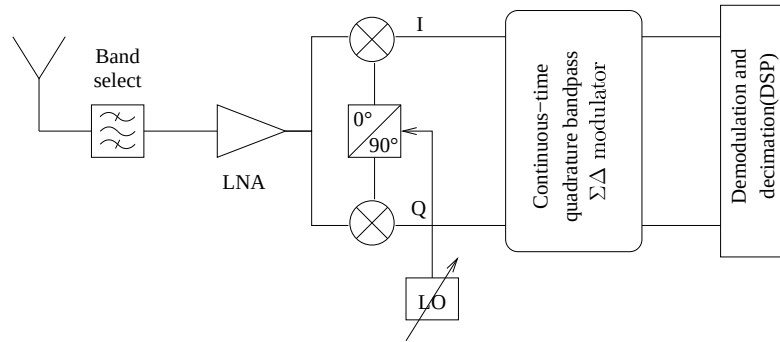


Figure 2.7.: CT-QBP $\Sigma\Delta$ M in low-IF receivers.

Therefore, in this work, we will focus on the implementation of CT-QBP $\Sigma\Delta$ M for low-IF receivers. For this goal, the following problems will be studied:

- The design methodology for CT-QBP $\Sigma\Delta$ M will be theoretically completed as a closed-form. Until now, the design methodology for CT lowpass [Can85], [SZ96], [CS99b], [BAB90], [Hor90] and CT-RBP $\Sigma\Delta$ Ms [AL04],[GS98], [HK00] have been comparatively known to CT-QBP $\Sigma\Delta$ M.
- The simulation method of CT-QBP $\Sigma\Delta$ Ms in Matlab will be presented. In this work, the Delta-Sigma Toolbox [ST04] will be extended into complex signal domain.
- The polyphase filter for low power and low voltage applications will be proposed.
- The nonideal effects of CT-QBP $\Sigma\Delta$ Ms, such as finite gain bandwidth product, excess loop delay and mismatched loop delay, clock jitter and nonlinearity by multibit DAC will be theoretically discussed and the methods for compensation or reducing will be proposed.
- The reconfigurable multimode, wideband CT-QBP $\Sigma\Delta$ M for GPS/Galileo low-IF receiver, and high-resolution medium-band CT-QBP $\Sigma\Delta$ M for GSM/EDGE low-IF receiver will be presented as applications. The measurement results will prove the effectiveness of the proposed CT-QBP $\Sigma\Delta$ Ms for low-IF receivers.

3. Design of CT-QBP $\Sigma\Delta$ M

This chapter illustrates design methods for CT-QBP $\Sigma\Delta$ Ms which are based on impulse invariance transformation. The possible design methods are discussed and compared in order to find out effective design method. In inverse method, starting from CT loop filter that is optimized in the CT-domain, the equivalent DT loop filter and noise shaping transfer function are calculated and estimated by criteria for modulator stability. In addition, simulation method for CT-QBP $\Sigma\Delta$ Ms is presented which are an extension to the Delta-Sigma Toolbox to the complex domain.

3.1. Design Methodology

In this section, the possible design methods will be discussed for CT-QBP $\Sigma\Delta$ M and their advantages are summarized.

There are three possibilities for the design of CT-QBP $\Sigma\Delta$ Ms; a direct method, an indirect method and an inverse method as shown in Figure 3.1. Starting point is the system specification and the final result is generally the CT polyphase filter.

In the first step of these methods, the lowpass noise shaping transfer function $NTF_{LP}(z)$ is calculated for CT-QBP $\Sigma\Delta$ M design. Assuming a center frequency, f_c , equal to zero, the modulator parameters such as modulator order (n), quantizer resolution (B) and oversampling ratio (OSR) are chosen from Equation (3.1) in order to ensure the DR of an targeted modulator,

$$DR^2 = \frac{3}{2} \cdot \frac{2n+1}{\pi^{2n}} \cdot (2^B - 1)^2 \cdot OSR^{2n+1}. \quad (3.1)$$

This equation gives a theoretical limit of achievable DR. However, it should be noted that this equation is more correct for the $NTF_{LP}(z)$ with zeros located at DC, rather than for the $NTF_{LP}(z)$ with the zeros spread over analog bandwidth.

The method reported in [NST96] allows to set $NTF_{LP}(z)$ infinite norm, such that the modulator becomes stable. For single-bit modulators, the following critical limitation may be applied for the $NTF_{LP}(z)$ design,

$$\|NTF_{LP}(z)\|_{\infty} < 1.5. \quad (3.2)$$

but this criterion is only empirical, neither a necessity nor a sufficiency. The above criterion is warranted by pole locations of the $NTF_{LP}(z)$. The poles should be placed

within a unit circle. This criterion is sufficient condition, but not necessary. In addition, the poles of the $NTF_{LP}(z)$ should be selected such that the effects of excess loop delay[HL03] and clock jitter[HWPDG04] are reduced.

From a demand of the analog bandwidth, f_B , of the given system, the zero placement of the $NTF_{LP}(z)$ is determined. For a narrow bandwidth such as audio, industrial measurement and biosensor readout applications, all zeros of the $NTF_{LP}(z)$ can be located at DC. For broad band applications such as multimedia, wireless and wireline an optimized zero placement allows to reduce the in-band noise power. The optimized zero placement with the different modulator order was reported in [NST96].

The CT loop filter can be selected as MASH or single loop architecture. Due to mismatch between the analog and digital coefficients in MASH architectures [dRdlRPV⁺04], [OGM05a] the single loop architecture such as CIFB and CIFF topologies is desirable for the sake of the CT polyphase filter design. The CT loop filter topology is selected from modulator electrical specifications such as power consumption, supply voltage and schematic complexity and chip area.

Based on the chosen modulator order, CT loop filter topology and zero placement of the $NTF_{LP}(z)$, the lowpass filter $H(s; k_1, \dots, k_n)$ is computed. Here, $k_1, \dots, k_n$ are feedback or feedforward coefficients of the CT loop filter which are differently determined in each method. The poles of the CT loop filter corresponds to zeros of the $NTF_{LP}(z)$.

3.1.1. Direct Method

3.1.1.1. $NTF_{QBP}(z)$ for QBP $\Sigma\Delta M$

The noise shaping transfer function $NTF_{QBP}(z)$ for QBP $\Sigma\Delta M$ can be translated from the above $NTF_{LP}(z)$, taking the center frequency, f_c , into account:

$$NTF_{QBP}(z) = NTF_{LP}(z \cdot e^{-j2\pi f_c/f_s}). \quad (3.3)$$

The poles and zeros of the $NTF_{LP}(z)$ are rotated from DC to f_c in the z -plane and the frequency response of $NTF_{LP}(z)$ is shifted to center frequency for the $NTF_{QBP}(z)$ as shown in Figure 3.2. In an ideal case, the translated $NTF_{QBP}(z)$ still maintains the lowpass modulator characteristics such as the DR and the maximum SNR, except for the passband which is centered around f_c .

3.1.1.2. CT Complex Loop Filter $H_{PPF}(s)$

Polyphase filter for CT-QBP $\Sigma\Delta$ modulators is derived by using CT-DT transformation from the DT polyphase filter $HD_{PPF}(z)$ which is defined as follows:

$$HD_{PPF}(z) = \frac{1}{NTF_{QBP}(z)} - 1. \quad (3.4)$$

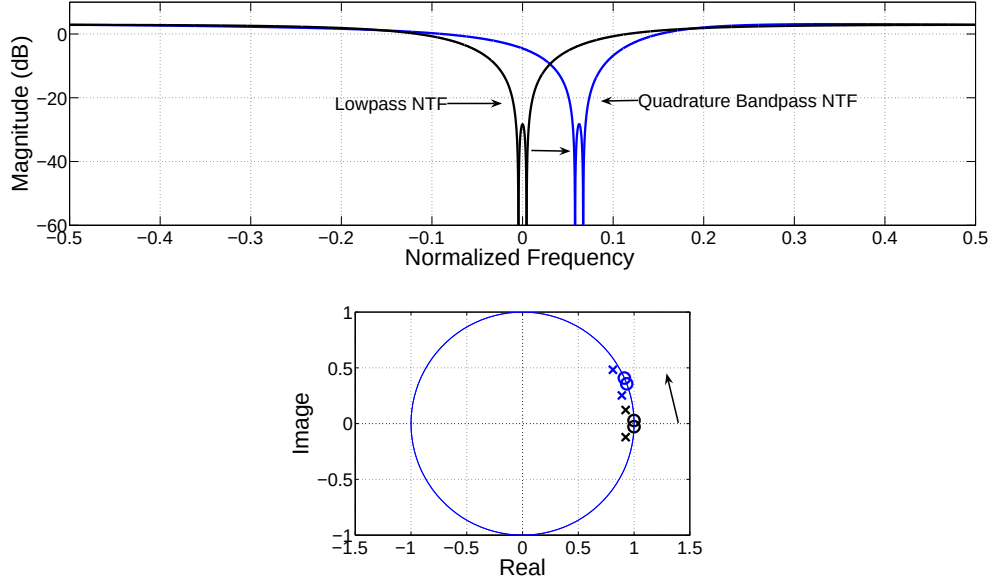


Figure 3.2.: Magnitude response and placement of pole ($\times$) and zero ($\circ$) of the $NTF_{QBP}(z)$.

In order to obtain the CT polyphase filter, the CT loop filter $H(s; k_1, \dots, k_n)$ is translated by jw_c in the s -plane (more detailed in chapter 3), and its result is $H(s - jw_c; k_1, \dots, k_n)$. The feedback or feedforward coefficients $k_1, \dots, k_n$ of the CT loop filter topology are calculated by CT-DT transformation from the DT prototype $HD_{PPF}(z)$.

The purpose of CT-DT transformation is to find the loop filter which implements the NTF designed in DT-domain. Impulse invariance transformation [Can85] based on mapping between impulse responses of two CT and DT equivalent systems, is mainly used in CT lowpass $\Sigma\Delta M$ s. That is because it fits better with the modulator behavior. R. Schreier proposed a methodology based on this transformation in [SZ96]. In this paper the linear blocks of CT $\Sigma\Delta M$ was described using the state space representation. Since then, there have been many publications about CT lowpass $\Sigma\Delta M$ s. Most of them were summarized in [CS99b]. Besides the impulse-invariance transformation, there are bilinear transformation [BAB90] and modified Z-transformation [Hor90], which are also based on equivalent between two systems. The impulse invariance transformation is defined in CT-QBP $\Sigma\Delta M$ as follows:

$$Z^{-1}\{HD_{PPF}(z)\} = L^{-1}\{DAC(s) \cdot H(s - jw_c; k_1, \dots, k_n)\}|_{t=nT_s}. \quad (3.5)$$

where $DAC(s)$ is the feedback DAC analog impulse. Return-to-zero (RZ), half delayed RZ (HRZ) and non-return-to-zero (NRZ) feedback DAC impulses [CS99b] can

be selected and the cosine analog waveform might be chosen to reduce the clock jitter [LL02]. From the above equation, the feedback or feedforward coefficients $k_1, \dots, k_n$ of the loop filter topology, is computed and, hence, the polyphase filter $H_{PPF}(s)$ finally obtained.

The advantage of this design method is that the obtained polyphase filter $H_{PPF}(s)$ is correctly matched with the $NTF_{QBP}(z)$, with no relation to f_c . Unfortunately, the coefficients $k_1, \dots, k_n$ in this design method are complex numbers because the feedback analog pulse $DAC(s)$ is still at DC [RDMRW05]. The complex coefficients are implemented by cross-coupling [HLH⁺02], similar to the complex integrator and it increases the circuit complexity and the chip area.

3.1.2. Indirect Method

In the indirect method, the general procedures [NST96],[ST04],[OG06] for CT lowpass $\Sigma\Delta M$ are applied as shown in Figure 3.1. Starting from the $NTF_{LP}(z)$, through CT-DT transformation the CT lowpass loop filter $\hat{H}_{LP}(s)$ and its coefficients are calculated. Next, the lowpass filter $\hat{H}_{LP}(s)$ is translated by frequency shifting to $\hat{H}_{PPF}(s)$.

The advantage of this design method is that the feedback or feedforward coefficients $k_1, \dots, k_n$ can be obtained as real values, because the coefficient calculation is carried out by means of the lowpass filter with real coefficients. Therefore, hardware complexity in the schematic implementation, is reduced. The main shortcoming of this design method is that, for a higher f_c , the obtained polyphase filter $\hat{H}_{PPF}(s)$ is not matched with ideal $NTF_{QBP}(z)$ anymore, degrading performance and modulator stability.

There is another weakness in the above two design methods. As long as they are based on the DT noise transfer functions and started from DT-domain, the system is usually optimized for DT purposes, without taking care of some effects that inherently occurs on CT domain, such as excess loop delay [CS99b], clock jitter [OGM05b], especially finite gain bandwidth (GBW) [CKE06] and DC gain [JF04] of the CT loop filter.

3.1.3. Inverse Method

The above design procedures can be inversely applied. Firstly, the CT loop filter is properly selected, afterwards by means of impulse invariance transformation, the equivalent DT loop filter $\hat{H}_{DPPF}(z)$ and the $\hat{NTF}_{QBP}(z)$. The integrator scales and loop filter coefficients in optimization step is iteratively modified until the $\hat{NTF}_{QBP}(z)$ is adequate for stability margin.

3.1.3.1. Optimization Process

In the optimization process, the integrator scales and feedback or feedforward coefficients are selected according to the following criteria:

- The spreads of the selected integrator scales and coefficients should be as small as possible, in order to reduce the coefficient mismatch error and chip area.
- The selected coefficients should be real values, not complex, in order to decrease circuit complexity and chip area.
- The phase margin of the CT loop filter $\dot{H}_{LP}(s)$ should be as large as possible, in order to ensure stability and reduce excess loop delay effect.
- The integrator scales should be optimally chosen in order to reduce the effect of finite gain bandwidth and DC gain of active elements (see section 5.1).
- The closed loop system $1/(1 + \dot{H}_{LP}(s))$ should be causal and stable. The stability of the close loop system depends on zero locations of $\dot{H}_{LP}(s)$ and the following conditions are satisfied.

$$\text{Re}[p_i(: \text{pole}) \Leftarrow (1 + \dot{H}_{LP}(s) = 0)] < 0. \quad (3.6)$$

- The infinity norm gives the peak gain of the frequency response and it also affects the stability of the modulator. Therefore, it should be

$$\|1/(1 + \dot{H}_{LP}(s))\|_{\infty} = 1. \quad (3.7)$$

The above described criteria depend on the zero placement of the CT lowpass filter. The zero placement of $\dot{H}_{LP}(s)$ is determined by the integrator scales and the feedback coefficients for the CIFB topology or the feedforward coefficients for the CIFF topology. Note that through the optimization process, the pole placement which is obtained from zero placement of the $NTF_{LP}(z)$ in the z -domain is still preserved in the s -domain. Next, the $\dot{H}_{LP}(s)$ is translated by frequency shifting to the $\dot{H}_{PPF}(s)$ (see chapter 4).

3.1.3.2. CT-DT Equivalents

In this design step, the DT equivalent $\dot{H}D_{PPF}(z)$ is inversely designed from CT prototype $\dot{H}_{PPF}(s)$ rather than usual. Figure 3.3 shows the open loop block diagram which contains the excess delay in loop, T_d . The impulse invariance transformation considered excess loop delay is employed to find out DT equivalent filters as follows:

$$Z^{-1}\{\dot{H}D_{PPF}(z)\} = L^{-1}\{DAC(s) \cdot e^{-T_d \cdot s} \cdot \dot{H}_{PPF}(s)\}|_{nT_s}. \quad (3.8)$$

As a result of transformation, the poles of $\dot{H}D_{PPF}(z)$ are denoted as:

$$z_k = e^{s_k T_s}. \quad (3.9)$$

where s_k is the pole of the CT polyphase filter $\dot{H}_{PPF}(s)$.

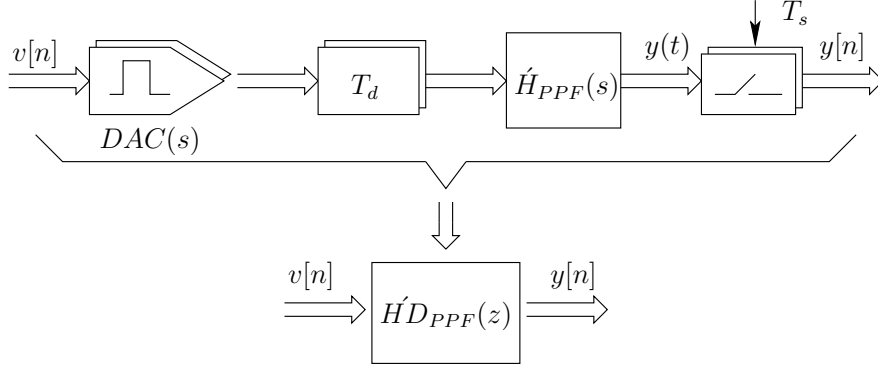


Figure 3.3.: CT-DT equivalent diagram.

3.1.3.3. Estimation of $N\acute{T}F_{QBP}(z)$

The $N\acute{T}F_{QBP}(z)$ is calculated by means of a linear model [RDMRW05].

$$N\acute{T}F_{QBP} = \frac{1}{1 + H'D_{PPF}(z)} \quad (3.10)$$

This linear model guarantees that the zero placement of $N\acute{T}F_{QBP}(z)$ is identical to the pole location of $H'D_{PPF}(z)$. Therefore, all zeros are centered around $e^{j\omega_c T_s}$ in the z -plane. Note that zero placement of the $N\acute{T}F_{QBP}(z)$ is identical to that of $N\acute{T}F_{QBP}(z)$, but the pole placement differs from each other.

The in-band quantization noise power of the modulators mainly depends on the zero placement, otherwise, the stability of the modulator depends on the pole placement. Even though the pole placement differs from that of $N\acute{T}F_{QBP}(z)$, the $N\acute{T}F_{QBP}(z)$ can give the same performance as $N\acute{T}F_{QBP}(z)$, provided that zero placement is equal to each other and the stability of $N\acute{T}F_{QBP}(z)$ is ensured. Therefore, the obtained $N\acute{T}F_{QBP}(z)$ is verified with the following criteria.

$$\|N\acute{T}F_{QBP}(z)\|_{\infty} < 1.5. \quad (3.11)$$

$$|p_k; N\acute{T}F_{QBP}(z)'s \text{ pole}| < 1. \quad (3.12)$$

When the $N\acute{T}F_{QBP}(z)$ deviates from the above established criteria, the integrator scales and/or coefficients of the loop filter, $\acute{H}_{LP}(s)$, should be renewed so that the final $N\acute{T}F_{QBP}(z)$ is desirable.

This method gives lots of allowances for optimized circuit design in CT domain, because it starts from the CT polyphase filter design. Therefore, this design technique might be more accurate and practical for the sake of CT $\Sigma\Delta$ M. However, for a higher center frequency, the obtained $N\acute{T}F_{QBP}(z)$ may not ensure the above criteria anymore,

degrading the performance and modulator stability.

Indirect and inverse methods for CT-QBP $\Sigma\Delta$ M design are well suited if the ratio of the center frequency f_c to sample clock f_s is small, because the CT polyphase filters with only real coefficients can provide desirable modulator performance. In this work, we used the inverse method for CT-QBP $\Sigma\Delta$ M design, because it starts from CT-domain and is optimized in CT-domain.

3.2. Simulation for CT-QBP $\Sigma\Delta$ M

The Delta-Sigma Toolbox [ST04] which has been described by Matlab source code, is widely used in the design of $\Sigma\Delta$ M. But, it is restricted to the generation and simulation of lowpass and real bandpass $\Sigma\Delta$ ADCs whose transfer functions are defined in the real domain. The transfer functions of QBP $\Sigma\Delta$ Ms are defined in complex domain, i.e., polynomials with complex coefficients. Therefore, we propose the simulation methods for CT-QBP $\Sigma\Delta$ M in Matlab [JKH07].

Here, the simulation procedure will follow the inverse design method. As mentioned above, the polyphase filter can be obtained from the optimized lowpass filter. A second-order CT-QBP $\Sigma\Delta$ M which has the center frequency of 2 MHz, the bandwidth of 1 MHz and the sample clock of 64 MHz is shown as simulation example.

```
OSR=64; N = 10000;
fc=2e6; fB=1e6; wc=2*pi*fc; fs=fB*OSR; Ts=1/fs;
nlev=2;          % when nlev=2, single-bit quantizer

%%%% normalization %%%%
fcnorm = ceil(fc/fs*N);
fB = ceil(fB/fs*N);
ftest=fcnorm+(1/3)*fB;
u = 0.5*cos(2*pi*ftest/N*[0:N-1])+j*0.5*sin(2*pi*ftest/N*[0:N-1]);

%%%% CT transfer function %%%%
[HPPF, pnum,pden] =CTpolypassfilter()
BW=0.5*fB;
echo off; figure; clf; hold on;
CTBodeplot(HPPF,BW);
CTBodeplot(1/(1+HPPF),BW);

%%%% DT transfer function %%%%
alpha=0; beta=1;  %\ NRZ feedback DAC pulse
[r, p, k] = residue(pnum,pden);
[ HDT ] = DTFunc( p(1),p(2),r(1),r(2), alpha,beta, Ts);
```

```

%%%% noise shaping transfer function %%%
NTF=1/(1+HDT);
echo off; figure; clf; hold on;
DTBodeplot(HDT,BW,Ts);
DTBodeplot(NTF,BW,Ts);
NTF_PZ(NTF,'b',15,10);

%%%% modulator output bit-streams %%%
GDT=c2d(HPPF, Ts, 'matched');
v = PPFSimulateDSM_RjQ(HDT,GDT,u,N,nlev);

%%%% SNR Estimation form bit-streams %%%
snr=PPFplotdsmsnr(v,u,N,Nftest,Nfc,NfB,OSR);

```

In first step, the simulation parameters are used as input, such as OSR , sample number for calculation (N), center frequency, bandwidth, quantizer level number ($nlev$). After normalization by sample frequency, the polyphase filter is computed by frequency shifting from the lowpass filter. The poles of the lowpass filter are obtained from specifications as shown in the above section. The computed polyphase filter and its closed loop filter are plotted.

Next, the DT polyphase filter is derived by using *DTFunc* from the impulse invariance transformation. The function, *DTFunc* can also be applied to calculation of the transfer function which represents excess loop delay and the different feedback DAC pulses such as NRZ, RZ and HRZ. The equivalent NTF is calculated by linear model from the DT equivalent loop filter, *HDT*. The stability margin is estimated in the z -domain as shown in Equation 3.11 and 3.12. If the obtained NTF is not enough to ensure modulator stability, the CT loop filter should be changed with the feedforward or feedback coefficients so that modulator would be stable, even in case of higher excess loop delay.

After the estimation of the NTF, the modulator output bit-streams are simulated. Based on the state space matrix description, the modulator bit-streams with multibit or single-bit quantizer are calculated by using the complex quantizer. Finally, the ideal SNR is obtained. Here, the output spectrum is plotted by using the Fast Fourier Transformation (FFT) with Hanning window. In order to calculate the SNR, the *rms* of the noise tones within the passband and the input signal tone are estimated in frequency domain.

The above simulation procedure can be applied to any modulator, with no restriction to modulator order, topology, feedback DAC pulse, multi- or single-bit quantizer, center frequency, and bandwidth. The detailed sub-routines are listed in Appendix A

In this chapter, the possible design methodologies have been compared. The inverse method is desirable for the design of CT-QBP $\Sigma\Delta M$. Starting from CT loop filter optimization, the equivalent noise shaping transfer function is finally calculated and

its stability margin is estimated. Because of the optimization in the CT-domain, this method gives to designer lots of flexibilities for circuit design in CT domain. When the ratio of the center frequency to the sampling frequency is not too large, using the feedforward or feedback coefficients with real values, the desirable SNR and stability margin can be obtained, while decreasing circuit complexity and chip area. In order to estimate the targeted modulator performances, the simulation method by Matlab code has been presented in Matlab. This is an extension of the Delta-Sigma Toolbox into the complex domain.

4. CT-QBP $\Sigma\Delta$ Ms with CICFF Topology

This chapter presents a strategy for successful polyphase filter design for CT-QBP $\Sigma\Delta$ Ms. Based on a lowpass filter with a *chain of integrators with weighted capacitive feedforward summation* (CICFF) topology - which is suited for implementation in low power applications - analytical equations are derived [KRJ⁺08]. A new compensation scheme is proposed and implemented by cross-coupling additional resistors, without the necessity of extra active components.

4.1. Overview for Polyphase Filter

A polyphase filter for quadrature bandpass $\Sigma\Delta$ modulators can be obtained by translating a lowpass filter transfer function from DC to the desired intermediate frequency ($w_c = 2\pi f_c$).

$$H_{PPF}(jw) = H_{LP}(jw - jw_c). \quad (4.1)$$

This translation moves all poles and zeros in the s -plane to positions centered around

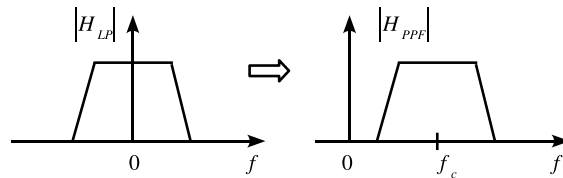


Figure 4.1.: Implementation of the polyphase filter by frequency shifting from the low-pass filter.

the intermediate frequency. Figure 4.1 shows the frequency shifting of the transfer function of the lowpass filter $H_{LP}(s)$. This can be implemented by cross-couplings between the outputs and inputs of the integrators of the two lowpass filters [HLH⁺02],[CS98b]. The implementation of single polyphase filter is shown in Figure 4.2. The single polyphase filter transfer function is

$$H_{PPF}(jw) = \frac{1}{1 + jw/w_0 - jw_c/w_0}. \quad (4.2)$$

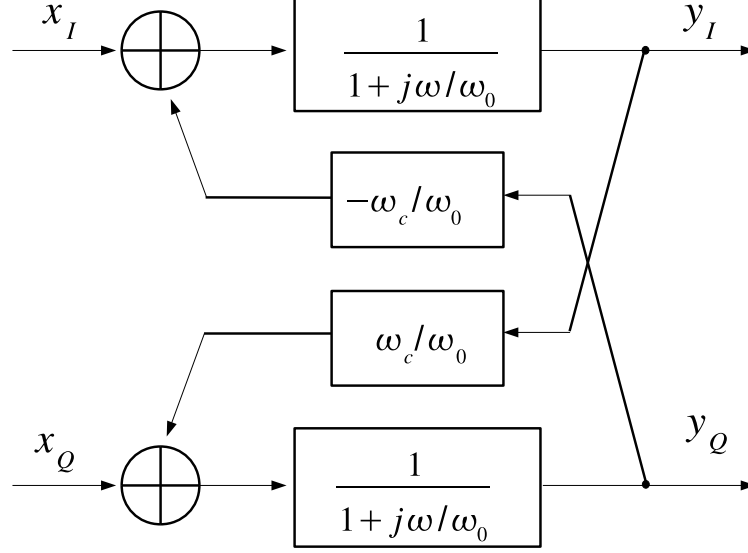


Figure 4.2.: Single polyphase filter obtained by two lowpass filters.

In general, a high order lowpass filter has a filter transfer function with complex conjugated pairs of poles and zeros. This implies that the lowpass filter has a passband at positive and negative frequencies. In contrast to that (since all poles and zeros in a polyphase filter transfer function $H_{PPF}(s)$ are moved by jw_c from original points in s -plane), the polyphase filter has a transfer function with complex, but not conjugated-complex poles and zeros. This leads to a passband only at positive or negative frequencies centered around w_c .

Since the polyphase filter for CT-QBP $\Sigma\Delta$ modulators can be obtained from CT lowpass filter, the characteristics of the lowpass $\Sigma\Delta$ modulators are preserved in QBP $\Sigma\Delta$ as well, except for different center frequency. This implies that the selection of lowpass filter is a main key for design of QBP $\Sigma\Delta$ modulators.

Loop-filter architecture selection is a design step, no matter which is the employed design technique, e.g., direct, indirect or inverse design method. The architecture is chosen according to hardware restrictions, power consumption, distortion and noise consideration. There are two possible architecture for $\Sigma\Delta$ M; one is a MASH architecture and the other is a single loop architecture.

Many $\Sigma\Delta$ Ms have been designed by using MASH architectures [MPVRV99], [OGM05a], [dlREPV⁺05], [MPSS98]. MASH architecture is a cascaded combination with second and/or first-order modulators. Therefore, the whole architecture has several loop filters with second or first-order and quantizers. The quantizer noise generated at each stage is remodulated and shaped by next one. The main advantage of this architecture is the unconditional stability for even large input signal level and any initial condition.

Furthermore, the placement of the multibit DAC at the last stage can reduce the DAC nonlinearity, because the DAC nonlinearity error is shaped with an adequate order which depends on MASH architecture [dRdlRPV⁺04]. But, in CT-QBP $\Sigma\Delta$ designs, the use of MASH architecture has been rarely seen in literatures, because the main drawback of this architecture is a mismatch between analog and digital coefficients and it causes the irrevocable channel mismatch error in CT-QBP $\Sigma\Delta$ s.

In addition, high DC gain amplifiers, typically 90 dB, are required in order to minimize integrator leakage[JF04]. To achieve high DC gain, the amplifiers often require multiple gain stages or gain boosting techniques, which lead to more area and power consumption. With advanced CMOS processes, the size of transistor is scaled down and, therefore, the power supply voltage becomes lower. This makes the design of such amplifiers even more difficult. Thus, MASH architecture might not be a feasible choice for low-power and low-voltage applications.

The single-loop architecture is one of the possible options for $\Sigma\Delta$ s [ST04] [PDGH⁺04], [MPSS98]. To construct a high order $\Sigma\Delta$ s, in the single-loop architecture, the simplest method is to cascade several integrators. Thus, the DC gain of the feedforward path is very high and this architecture does not require high DC gain. Two main single-loop topologies exist as shown in Figure 4.3: a) *the chain of integrators with distributed feedback* (CIFB) and b) *the chain of integrators with weighted feedforward summation* (CIFF).

The drawback of the single loop is instability with the order of the loop. Although stability can be improved by using multibit quantizers and carefully choosing the coefficient values, it is still difficult to design a stable single-loop $\Sigma\Delta$ higher than third order. The most effective solution is to insert the feedforward paths of the input-signal (feedforward path with coefficients l_i in Figure 4.3). Therefore, most of the input signal bypasses rather than the integrator chain. The small residual signal and quantizer error are passed through the integrators, increasing stability[SDRP04]. But, in the opinion of author, it can only be effective in DT $\Sigma\Delta$, because the loop filters in CT $\Sigma\Delta$ s don't act as an anti-aliasing filter, especially not for directly bypassed input signal prior to the quantizer. Therefore, it may require an additional filter for anti-aliasing of the directly feedforward input signal.

In Figure 4.3, a_i is a scale of the i -th integrator and k_i is a feedback coefficient in CIFB and a feedforward coefficient in CIFF topology, which are determined to ensure the modulator stability. The feedback coefficients b_i are used to make local feedback loops, in order to minimize the in-band noise power[NST96]. These make the optimized zeros in the NTF which are spread over modulator bandwidth. In wideband applications, the NTF with the spread zero placement is often used [PDGH⁺04], [KJZ⁺07]. When $b_i = 0$, the zeros are located at zero frequency-DC in case of lowpass NTF. This zero placement is mainly used in narrow bandwidth applications, such as audio. Feedforward coefficients, l_i only have influence on signal transfer function (STF).

The CIFB topology is commonly used in implementation of $\Sigma\Delta$ [HLH⁺02], [CJ06]. The distributed feedback DACs are used to ensure stability of the cascaded integrators

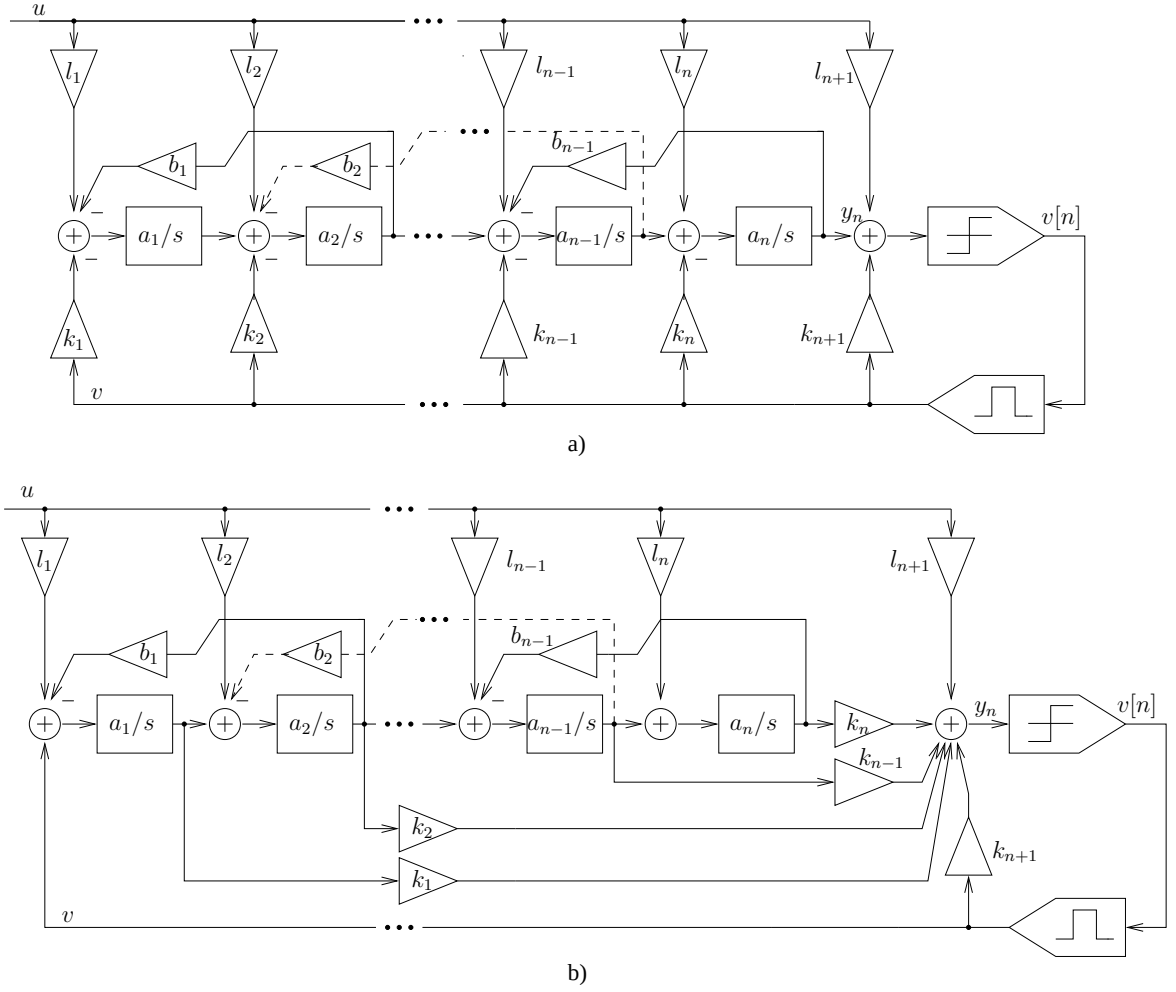


Figure 4.3.: Lowpass CT $\Sigma\Delta$ M architecture with CIFB a) and CIFF topology b).

in feedforward path. The main advantage of the CIFB topology is that it is easy to implement with low sensitivity to component variations. The main disadvantage of this topology is that the signals at the output of the integrators are a function of the input signal, resulting in two effects. First, the signal swing at the output of the integrators is large, making their implementation in low-voltage more difficult. Second, the amplifier nonlinearities generate harmonic distortion that depends on the input-signal.

In the CIFF topology [YS04], [PNR⁺04], in contrast to CIFB, the feedforward paths can be used to establish stability, while requiring one feedback DAC pulse. For the sake of the design of CT-QBP $\Sigma\Delta$ Ms, the CIFF topology has several advantages as follows:

- The swing at the integrator outputs reduces significantly and the output spectrum shows less harmonic distortion.
- The effects of excess loop delay and clock jitter can be reduced, because the CIFF topology has one feedback path and, therefore, has one noise source from excess loop delay and feedback DAC clock uncertainty.
- The demand of slew rate, settling time and finite gain bandwidth product except for the first amplifier can be relaxed, while decreasing power consumption. Especially, the effects by finite GBW can be decreased, because the resistors for feedback DACs can reduce an equivalent input resistor of the integrators and therefore the deviation from the center frequency is increased (see section 5.1).

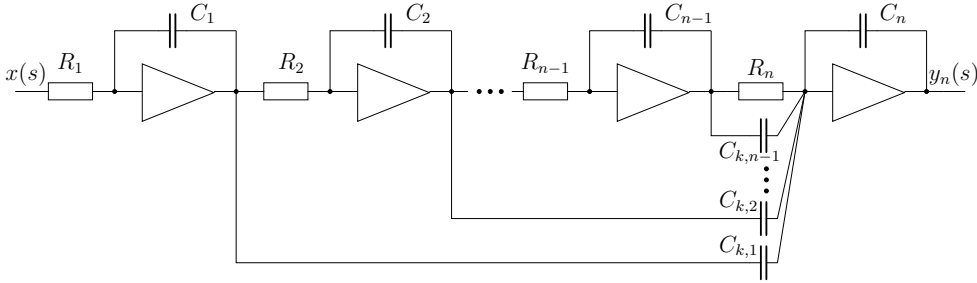


Figure 4.4.: Loop filter with capacitive feedforward structure.

Although CIFF topology has several benefits, it needs extra components for feedforward summation, and thus additional power consumption. This can be overcome by *the chain of integrators with capacitive feedforward summation* (CICFF), which is really CIFF topology, but only difference is in summation [DKG⁺05], [SDRP04]. The main advantage of this structure is the elimination of the feedforward summation amplifier at the output of the loop and hence consumes no additional power in feedforward branches as shown in Figure 4.4. In contrast to the feedforward summation structure with transconductor amplifiers [EBRB03], the feedforward coefficients are inherently

linear. The feedforward coefficients are determined as $k_i = C_{k,i}/C_n$, where $C_{k,i}$ is feedforward capacitor and C_n is the integrating capacitor of the last stage.

The CICFF topology can also be applied to polyphase filter design, but demands careful considerations. In this work, we will focus the implementation of CT-QBP $\Sigma\Delta$ M based on the polyphase filter with CICFF topology, because it is suited for low-power and low-voltage.

4.2. Lowpass Filter with CICFF topology

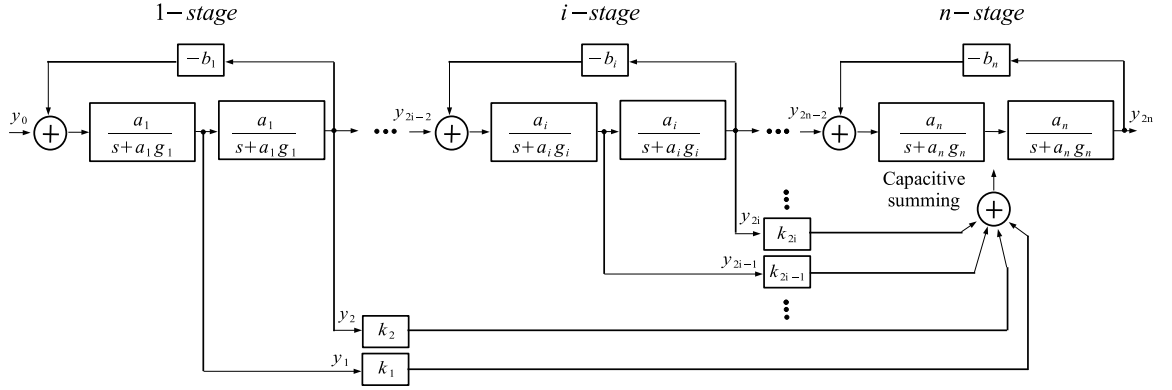


Figure 4.5.: Loop filter with capacitive feedforward structure.

In this section, analytical expressions of a lowpass filter with the CICFF topology are calculated. An even-order lowpass filter with the CICFF topology is shown in Figure 4.5. It consists of a cascade of $(n-1)$ stages with local feedback loops and a final stage with additional capacitive feedforward summation. Each single stage with its local feedback loop corresponds to a second-order lowpass filter. The difference between CIFF and CICFF topology is only in the implementation of the summation. It should be noted that the CICFF topology is an implementation of the CIFF topology. In case of CICFF topologies the summation is implemented by capacitive combinations in the last local feedback loop, in contrast to the summation by additional active components in CIFF topologies. Hence, the output functions of the $(n-1)$ stages are identical in both variants.

Figure 4.6 shows the i^{th} -stage of Figure 4.5, where the input and output of the i^{th} -stage are connections from the output of the previous stage to the input of the following stage. Without loss of generality, a lossy integrator is chosen, according to [HLH⁺02] and [CS98b]. Note that for an ideal integrator, $g_i = 0$, ($i = 1 : n$) in Figure 4.5 or $R_{P,i} = \infty$, ($i = 1 : n$) in Figure 4.6. The output functions of any stage with a

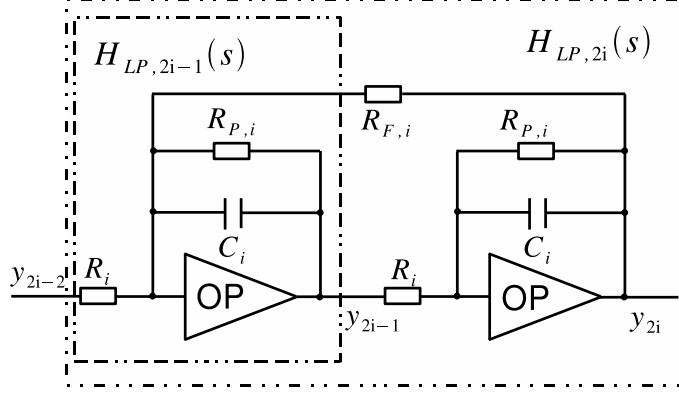


Figure 4.6.: Local feedback loop.

local feedback loop (except the summation stage) can be obtained as follows:

$$y_{2i-1} = H_{LP,2i-1}(s) \cdot y_{2i-2} = \frac{w_{0,i} \sqrt{A_i} (s + \frac{w_{0,i}}{Q_i})}{(s + \frac{w_{0,i}}{Q_i} + jw_{0,i})(s + \frac{w_{0,i}}{Q_i} - jw_{0,i})} \cdot y_{2i-2}, \quad (4.3)$$

$$y_{2i} = H_{LP,2i}(s) \cdot y_{2i-2} = \frac{w_{0,i}^2 A_i}{(s + \frac{w_{0,i}}{Q_i} + jw_{0,i})(s + \frac{w_{0,i}}{Q_i} - jw_{0,i})} \cdot y_{2i-2}, \quad (4.4)$$

$i = 1 : (n - 1)$

with $w_{0,i}^2 = a_i^2 \cdot b_i$, $Q_i = \sqrt{b_i}/g_i$, $A_i = 1/b_i$, $a_i = 1/R_i C_i$, $g_i = R_i/R_{P,i}$ and $b_i = R_i/R_{F,i}$.

The capacitive feedforward summation is implemented by capacitive combinations as shown in Figure 4.7. Except for the output y_{2n-1} , all outputs are connected to capacitors related to the feedforward coefficients. They are summed at the input of the second integrator in the last stage. The summation for the output of y_{2n-1} is realized in front of the final local feedback loop - with the first integrator of the final stage which has y_{2n-2} as input for summation [DKG⁺05]. The local feedback loop with capacitive feedforward summation can be described as

$$\frac{y_{2n-2}(t)}{R_n} + \overbrace{C_{k,2n-1} \frac{dy_{2n-2}}{dt}}^{\text{summation}} = C_n \frac{dy_{2n-1}(t)}{dt} + \frac{y_{2n-1}(t)}{R_{P,n}} + \frac{y_{2n}(t)}{R_{F,n}}, \quad (4.5)$$

$$\frac{y_{2n-1}(t)}{R_n} + \overbrace{\sum_{i=1}^{2n-2} C_{k,i} \frac{dy_i(t)}{dt}}^{\text{summation}} = C_n \frac{dy_{2n}(t)}{dt} + \frac{y_{2n}(t)}{R_{P,n}}. \quad (4.6)$$

In Equation (4.5) and (4.6), the second terms on the left side of these equations are the ones corresponding to summation. Now, applying the Laplace transformation to Equation (4.5) and (4.6), we can obtain the final output function in the s -domain as follows:

$$y_{2n} = H_{LP}(s) \cdot y_0 = H_{LP,n}(s) \cdot y_{2n-2} + H_{LP,s}(s) \cdot \sum_{i=1}^{2n-2} k_i \cdot y_i, \quad (4.7)$$

with $k_i = C_{k,i}/C_n$ ($i = 1 : 2n - 2$). The feedforward coefficients k_i correspond to the ratios of the feedforward capacitor ($C_{k,i}$) to the integrating capacitor (C_n) of the lossy integrator in the last stage. $H_{LP,n}(s)$ and $H_{LP,s}(s)$ are the transfer functions, which are calculated from considerations of the local feedback loop and summation. They can be expressed as follows:

$$H_{LP,n}(s) = \frac{k_{2n-1} \cdot w_{0,n} \sqrt{A_n} s + w_{0,n}^2 A_n}{(s + \frac{w_{0,n}}{Q_n} + jw_{0,n})(s + \frac{w_{0,n}}{Q_n} - jw_{0,n})}, \quad (4.8)$$

$$H_{LP,s}(s) = \frac{s(s + \frac{w_{0,n}}{Q_n})}{(s + \frac{w_{0,n}}{Q_n} + jw_{0,n})(s + \frac{w_{0,n}}{Q_n} - jw_{0,n})}, \quad (4.9)$$

with $k_{2n-1} = C_{k,2n-1}/C_n$ for y_{2n-1} , and $k_{2n} = 1$ for y_{2n} . To avoid resonator damping in the last stage, a distinctive summation for y_{2n-1} is implemented [DKG⁺05].

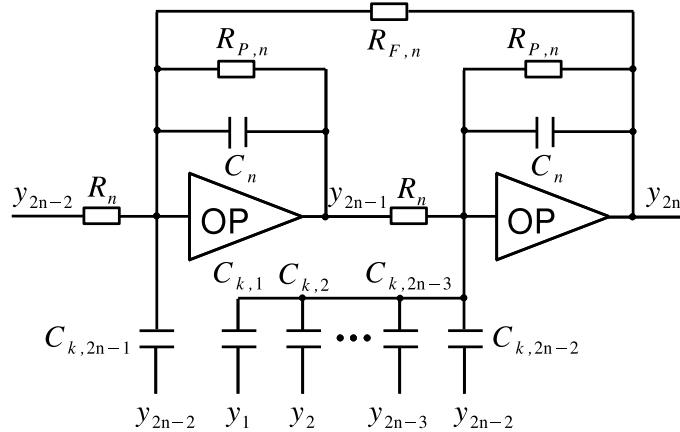


Figure 4.7.: Implementation of capacitive feedforward summation.

The lowpass filter with the CICFF topology can be characterized as recursive combinations by Equation (4.3), (4.5) and (4.7). The order of the numerator of the transfer function $H_{LP}(s)$ is $(2n-1)$, while the order of the denominator $D_{LP}(s)$ is $2n$ as follows:

$$D_{LP}(s) = \prod_{i=1}^n \left[\left(s + \frac{w_{0,i}}{Q_i} + jw_{0,i} \right) \left(s + \frac{w_{0,i}}{Q_i} - jw_{0,i} \right) \right]. \quad (4.10)$$

From the above Equation, we can calculate the poles of the lowpass filter, which only depend upon the circuit components in each local feedback loop and are independent of the feedforward coefficients.

CIFF topologies, that are equivalent to the CICFF, can be obtained by mapping of transfer functions. In CIFF topologies, the summation of all stages which have local feedback loops is implemented by a linear combination of all outputs. The structure of the denominator in both of them are the same as Equation (4.3). Therefore, the coefficients of the polynomial in the numerators need to be identified. For example, in a fourth-order lowpass filter, mapping the coefficients between CIFF and CICFF topologies can be denoted as follows, provided that both local feedback loops have identical circuit parameters.

$$\begin{aligned} k'_1 &= k_1, \\ k'_2 &= k_2 - k_1 g_2 a_2 / a_1, \\ k'_3 &= k_3 - k_2 g_2 - k_1 (g_2^2 + g_1 g_2 + b_2 - 2g_2^2 a_2 / a_1), \\ k'_4 &= 1 - k_3 g_2 - k_2 b_2 - k_1 [(a_2 / a_1 - 1) g_2^3 + \\ &\quad + b_2 (g_1 - g_2 - g_2 a_2 / a_1)], \end{aligned} \quad (4.11)$$

where k'_1, k'_2, k'_3 and k'_4 are the feedforward coefficients of the CIFF topology. They are slightly lower than those of CICFF, except for k'_1 . Using Equation (4.11), a CICFF topology can be simulated using its CIFF equivalent. This mapping relationship can also be applied for polyphase filters with CIFF and CICFF topologies.

Until now, only even order lowpass filter with the CICFF topology have been explained. Fortunately, any odd order lowpass filter with the CICFF topology can be considered by a cascade of one lossy integrator and an even order lowpass filter. Since the transfer function can be easily derived from above analytical description, it is not especially mentioned here.

4.3. Polyphase Filter with CICFF topology

A polyphase filter for quadrature bandpass $\Sigma\Delta$ modulators can be implemented by transforming a lowpass filter from DC to the desired intermediate frequency. This can be implemented by a cross-coupling between the outputs and inputs of the integrators of the lowpass filters [Mar04],[CS98b]. Though the method of cross-coupling quadra-

ture integrators as well as mathematical approaches in order to realize polyphase filter are common, it is practically only possible for CIFB and conventional CIFF topologies. Here, we propose an implementation of a polyphase filter derived from a lowpass filter with CICFF topology.

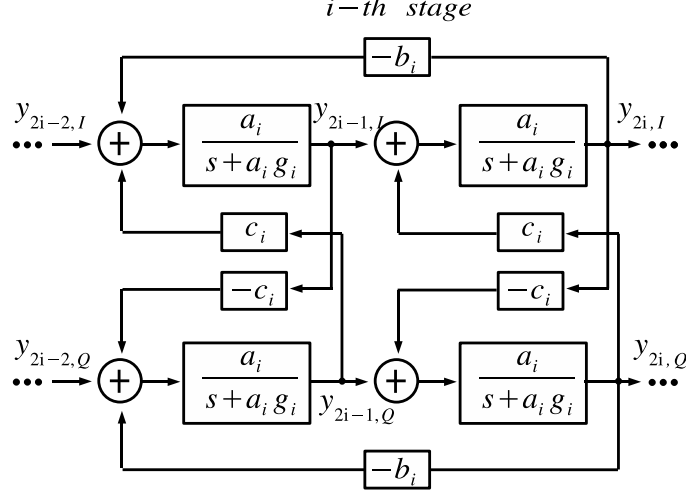


Figure 4.8.: Cross-coupling in cascaded local feedback loops.

As shown in section II, a lowpass filter with the CICFF topology consists of two parts: one is a cascaded combination of the local feedback loops, the other one is a combination of the capacitive feedforward summation scheme and a local feedback loop. In case of the first $(n-1)$ stages with only local feedback loops based on frequency translation of Equation (4.1), the output functions can be obtained from Equations (4.3) and (4.5) as follows:

$$y_{2i-1} = H_{PPF,2i-1}(s) \cdot y_{2i-2} = \frac{w_{0,i} \sqrt{A_i} (s + \frac{w_{0,i}}{Q_i} - jw_c) \cdot y_{2i-2}}{(s + \frac{w_{0,i}}{Q_i} - jw_c + jw_{0,i})(s + \frac{w_{0,i}}{Q_i} - jw_c - jw_{0,i})}, \quad (4.12)$$

$$y_{2i} = H_{PPF,2i}(s) \cdot y_{2i-2} = \frac{w_{0,i}^2 A_i \cdot y_{2i-2}}{(s + \frac{w_{0,i}}{Q_i} - jw_c + jw_{0,i})(s + \frac{w_{0,i}}{Q_i} - jw_c - jw_{0,i})}. \quad (4.13)$$

Note that all outputs of the polyphase filter are complex signals ($y_i = y_{I,i} + jy_{Q,i}$). From Equation (4.12) and (4.13), it can be seen that all poles and zeros of the transfer functions are moved by jw_c in the s -plane. Moving the intermediate frequency w_c can be implemented by using cross-coupling combinations between inputs and outputs in quadrature integrators (in this case, quadrature lossy integrators) like that of CIFF

and CIFB topologies. Figure 4.8 shows the cross-coupling combination in cascaded $(n - 1)$ stages with normal feedback loops, where c_i ($i = 1 : n - 1$) are the cross-coupling coefficients and are described as $R_{C,i}/R_i$. The normal cross-coupling resistors $R_{C,i}$ are chosen to satisfy $w_c = 1/(R_{C,i}C_i)$ ($i = 1 : n - 1$).

In case of the final stage, which comprises the capacitive summation as well as a local feedback loop, careful considerations for the translation to center frequency are necessary. Based on the transformation of Equation 4.1, the final output function, which is moved by jw_c in the s -plane can be obtained from Equations (4.7)-(4.9) as follows:

$$y_{2n} = H_{PPF}(s) \cdot y_0 = H_{PPF,n}(s) \cdot y_{2n-2} + H_{PPF,s}(s) \cdot \sum_{i=1}^{2n-2} k_i y_i, \quad (4.14)$$

$$H_{PPF,n}(s) = \frac{k_{2n-1}w_{0,n}\sqrt{A_n}(s - jw_c) + w_{0,n}^2 A_n}{(s + \frac{w_{0,n}}{Q_n} - jw_c + jw_{0,n})(s + \frac{w_{0,n}}{Q_n} - jw_c - jw_{0,n})}, \quad (4.15)$$

$$H_{PPF,s}(s) = \frac{(s - jw_c)(s + \frac{w_{0,n}}{Q_n} - jw_c)}{(s + \frac{w_{0,n}}{Q_n} - jw_c + jw_{0,n})(s + \frac{w_{0,n}}{Q_n} - jw_c - jw_{0,n})}. \quad (4.16)$$

From Equations (4.14)-(4.16), it can be shown that the poles and zeros of the polyphase filter H_{PPF} with CICFF topology are moved by jw_c in the s -plane. Note that these are results from the direct frequency translation, hence all characteristics of the lowpass filter are preserved in the polyphase filter, except for the new center frequency of the passband. More important is how to realize the full schematic to satisfy Equations (4.14)-(4.16). In consideration of (4.14), the output functions, y_i ($i = 1 : 2n - 2$), of the front stages have already been centered around jw_c by the cross-coupling combinations of the quadrature lossy integrators as shown in Figure 4.8.

An important task is to solve the translation of the transfer functions, $H_{PPF,n}(s)$ and $H_{PPF,s}(s)$. A full schematic for the last stage requires not only cross-couplings for the quadrature lossy integrators within the local feedback loop, but also compensation cross-couplings for the capacitive summation. By conventional cross-coupling applied to the lossy integrators, the poles in $H_{PPF,n}(s)$ and $H_{PPF,s}(s)$ can be moved, but moving the zeros introduced by the capacitive summation is impossible. Hence, the compensation scheme for moving the zeros to center frequency has to provide additional elements to account for the capacitive summation. Recalling the lowpass filter with the CICFF topology, the zeros of $H_{PPF,n}(s)$ and $H_{PPF,s}(s)$ are introduced by the second terms on the left-hand sides in Equations (4.5) and (4.6). It implies that zeros caused by capacitive summation should also be moved by jw_c . Equations (4.5) and

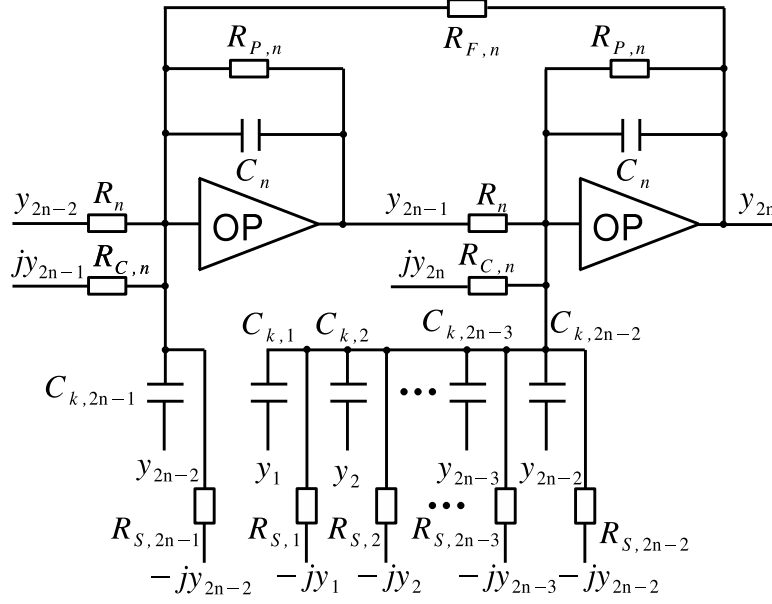


Figure 4.9.: Compensation cross-couplings in last stage. Here $y_i = y_{I,i} + jy_{Q,i}$.

(4.6) have to be replaced by Equations (4.17) and (4.18) for the polyphase filter with CICFF topology. They contain cross-coupling terms for moving the poles in the local feedback loop, as well as for moving the zeros caused by capacitive summation.

$$\begin{aligned} \frac{y_{2n-2}(t)}{R_n} + \overbrace{\left[C_{k,2n-1} \frac{dy_{2n-2}}{dt} - j \frac{y_{2n-2}(t)}{R_{S,2n-1}} \right]}^{\text{summation/compensation}} = \\ C_n \frac{dy_{2n-1}(t)}{dt} - j \frac{y_{2n-1}(t)}{R_{C,n}} + \frac{y_{2n-1}(t)}{R_{P,n}} + \frac{y_{2n}(t)}{R_{F,n}}, \end{aligned} \quad (4.17)$$

$$\begin{aligned} \frac{y_{2n-1}(t)}{R_n} + \overbrace{\left[\sum_{i=1}^{2n-2} \left(C_{k,i} \frac{dy_i(t)}{dt} - j \frac{y_i(t)}{R_{S,i}} \right) \right]}^{\text{summation/compensation}} = \\ C_n \frac{dy_{2n}(t)}{dt} - j \frac{y_{2n}(t)}{R_{C,n}} + \frac{y_{2n}(t)}{R_{P,n}}. \end{aligned} \quad (4.18)$$

The second terms on the right-hand side of Equations (4.17) and (4.18) represent cross-couplings for moving the poles in local feedback loop, which provide for $w_c = 1/(R_{C,n}C_n)$. Since the second terms on the left-hand side are for the summation, the third terms ensation terms on the left-hand side of Equation (4.17) and (4.18) are

inserted for summation. Similar to the above consideration of moving the poles, all of the zeros in the final output function can be moved to jw_c in the s -plane provided that $w_c = 1/(R_{S,i}C_{k,i})$ ($i = 1 : 2n - 1$).

From Equations (4.17) and (4.18), a scheme with compensation cross-couplings as well as normal cross-couplings can be directly obtained. Figure 4.9 shows a compensation cross-coupling scheme in the last stage of a polyphase filter with the CICFF topology. The compensation scheme for moving the zeros to center frequency is implemented by inserting resistors $R_{S,i}$ according to Equations (4.17) and (4.18). Applying the Laplace transformation to Equations (4.17) and (4.18), the same analytical expressions in the s -plane as Equations (4.14)-(4.16) can be obtained. The resistors for cross-coupling compensation are chosen by $R_{S,i} = R_{C,n}/k_i$ ($i = 1 : 2n - 1$).

Finally, by combination of Figures 4.8 and 4.9, all zeros and poles in the lowpass filter with the CICFF topology are placed around the center frequency in the s -plane. Hence, the resulting polyphase filter has a passband only at positive frequencies centered around w_c . Its bandwidth depends on the maximum value of the resonator frequencies, $f_{0,i} = w_{0,i}/2\pi$ ($i = 1 : n$).

Until now, only even-order polyphase filters with capacitive feedforward summation were considered. The shown analytical procedure and the compensation scheme can be adapted to any CICFF topology, regardless of the integrator type (ideal or lossy) and even whether the last stage is a local feedback loop or an integrator alone. Note, that for an ideal integrator, $\frac{w_{0,i}}{Q_i} = 0$ in Equations (4.12)-(4.16).

4.4. Implementation of Polyphase Filter

The fourth-order polyphase filter with the CICFF topology is discussed as a design example. The fourth-order polyphase filter has two local feedback loops and three capacitive summation components. The transfer function can be fully described from Equations (4.12)-(4.16) as follows:

$$\begin{aligned}
 H_{PPF,4}(s) &= N(s)/D(s), \\
 D(s) &= \prod_{i=1}^2 \left[\left(s + \frac{w_{0,i}}{Q_i} - jw_c + jw_{0,i} \right) \cdot \left(s + \frac{w_{0,i}}{Q_i} - jw_c - jw_{0,i} \right) \right], \\
 N(s) &= (s - jw_c) \left(s + \frac{w_{0,2}}{Q_2} - jw_c \right) \cdot [k_1 w_{0,1} \sqrt{A_1} \left(s + \frac{w_{0,1}}{Q_1} - jw_c \right) + k_2 w_{0,1}^2 A_1] + \\
 &\quad + w_0^2 A_1 [k_3 w_{0,2} \sqrt{A_2} (s - jw_c) + w_{0,2}^2 A_2], \tag{4.19}
 \end{aligned}$$

where $w_{0,i}^2 = (R_i/R_{F,i})/(R_i C_i)^2$, $w_c = 1/(R_{C,i} C_i)$, $Q_i = (R_{P,i}/R_i) \sqrt{R_i/R_{F,i}}$, $A_i = R_{F,i}/R_i$, $k_i = C_{k,i}/C_2$. Figure 4.10 shows a full schematic of a fourth-order polyphase filter with the CICFF topology for a fourth-order CT-QBP $\Sigma\Delta$ M, which has three sets of resistors for compensation cross-couplings for the translation of zeros, where the

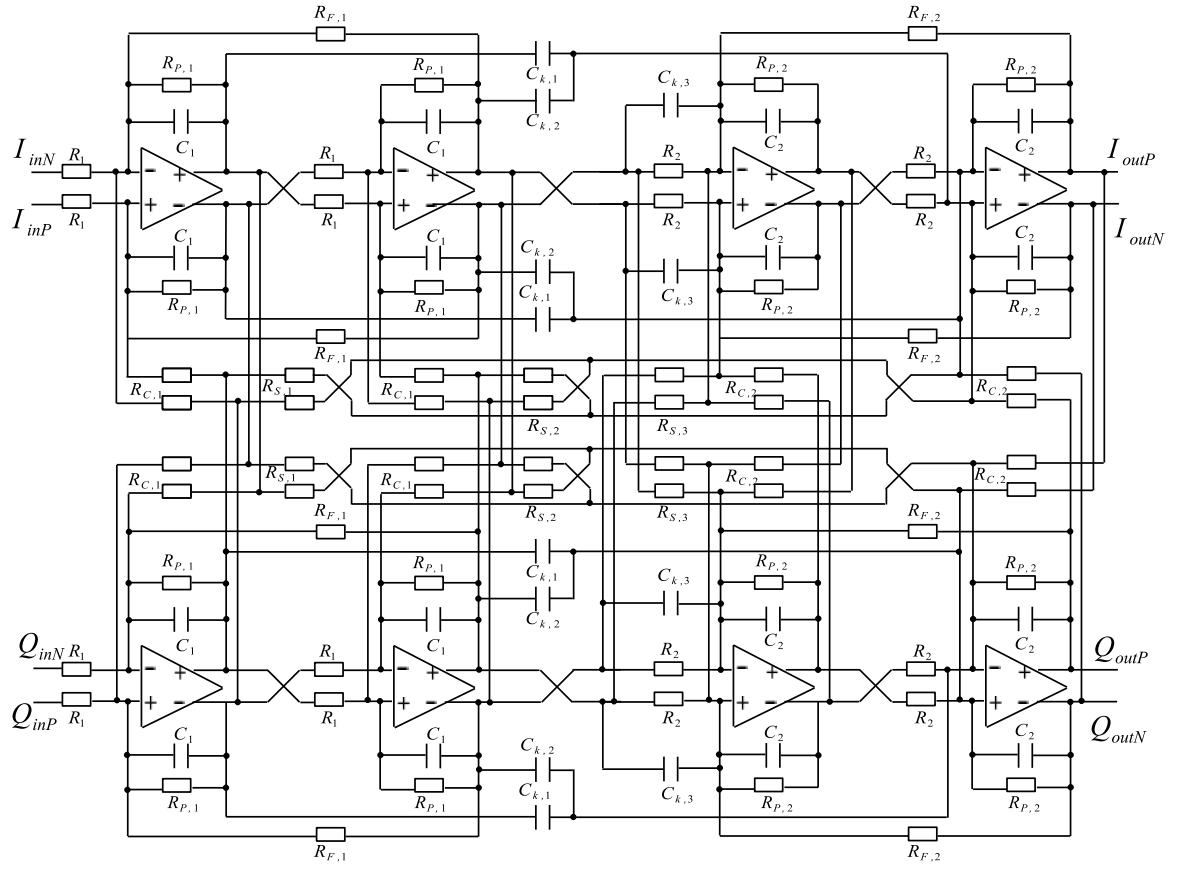


Figure 4.10.: Fourth-order polyphase filter with the CICFF topology.

compensation resistors are $R_{S,i} = R_{C,2}/k_i$ ($i = 1 : 3$).

The resonance frequencies of a fourth-order lowpass filter with the CICFF topology can be obtained from an optimized placement of zeros in the NTF_{LP} as mentioned in Chapter 3. The imaginary part of two conjugated-complex poles which dominate the resonance frequencies in two local feedback loops were chosen as

$$\begin{aligned} w_{0,1,LP} &= \pm 0.74156w_B, \\ w_{0,2,LP} &= \pm 0.42636w_B. \end{aligned} \quad (4.20)$$

The scale values of the integrators a_i and the feedback coefficients b_i can be calculated from the resonance frequencies, within a limitation imposed by the permissible chip design. The feedback coefficients, g_i of the lossy integrators which changes the in-band minimum level and the out-of band maximum of the NTF_{LP} , significantly affect the stability and the quality factor. Especially, it increases the in-band minimum level of the NTF, so that the in-band quantization noise increases. The feedback coefficient g_i is determined from the noise budget and stability margin.

The resonance frequencies of two local feedback loops for the fourth-order polyphase filter are moved to center frequency as follows:

$$\begin{aligned} w_{0,1,PPF} &= \pm 0.74156w_B + w_c, \\ w_{0,2,PPF} &= \pm 0.46236w_B + w_c. \end{aligned} \quad (4.21)$$

The resonator frequency of two local feedback loops are then

$$\begin{aligned} \sqrt{(R_1/R_{F,1})/(R_1C_1)^2} &= 0.74156w_B, \\ \sqrt{(R_2/R_{F,2})/(R_2C_2)^2} &= 0.46236w_B. \end{aligned} \quad (4.22)$$

This placement of the poles in the polyphase filter is not affected by the coefficients k_1, k_2 and k_3 . The placement of the zeros depend differently on the the feedforward coefficients k_1, k_2 and k_3 . For the fourth-order polyphase filter, zeros are three complex values centered around jw_c . In this simulation $k_1 = 1, k_2 = 1$ and $k_3 = 0.8$ were chosen.

The amplitude and phase responses of the transfer function $H_{PPF,4}(s)$ which are shifted from a lowpass filter, are shown in Figure 4.11. The filter has a bandwidth of 1.0 MHz and the center frequency is 2 MHz. At that time, the phase margin of $H(s)$ is 45.9°. The component values used in the design example are listed in Table 4.1.

For the polyphase filter without compensation - only with the cross-couplings of quadrature integrators - the asymmetries in $H_{PPF,4}(s)$ and therefore an equivalent DT NTF_{QBP} are also introduced, which are due to moving the poles to center frequency, but remaining the zeros centered around DC.

Figure 4.12 shows the placement of the poles and zeros of the equivalent NTF_{QBP} from the polyphase filter, which is derived by inverse design method and is defined as

Component list	Values
R_1, C_1	17.176 k Ω , 5 pF
$R_{P,1}, R_{F,1}$	858.80 k Ω , 429.40 k Ω
R_2, C_2	41.327 k Ω , 5 pF
$R_{P,2}, R_{F,2}$	826.54 k Ω , 1.3638 M Ω
$R_{C,1} = R_{C,2} = R_{C,3} = R_{C,4}$	15.915 k Ω
$R_{S,1} = R_{S,2}, C_{k,1} = C_{k,2}$	15.915 k Ω , 5 pF
$R_{S,3}, C_{k,3}$	19.884 k Ω , 4 pF

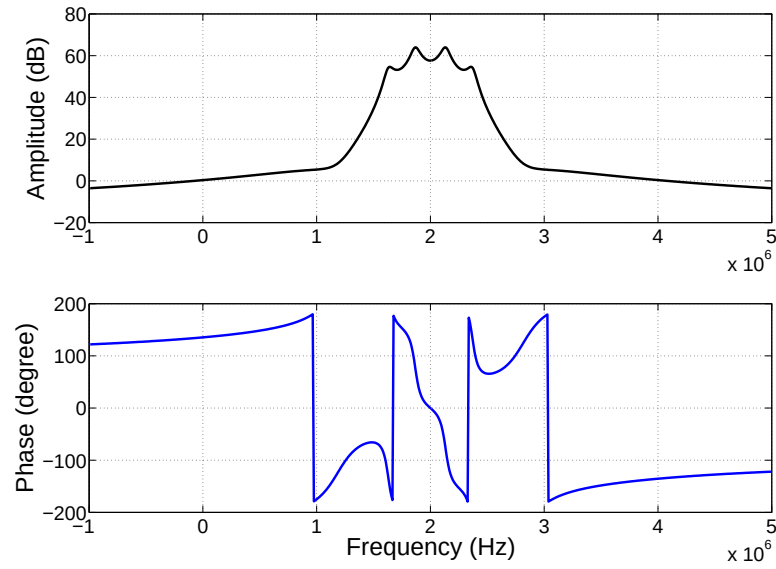
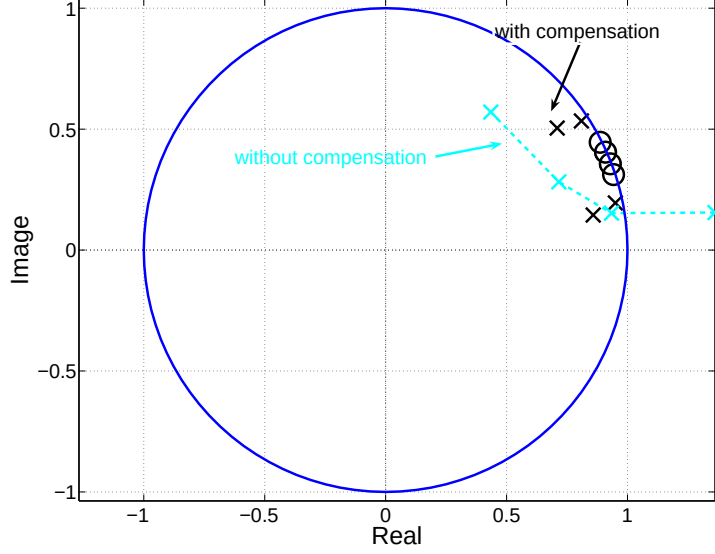


Figure 4.11.: Amplitude and phase response of fourth-order polyphase filter.

Figure 4.12.: Poles and zeros of the equivalent NTF_{QBP} .

a polynomial expression with complex coefficients. When using the proposed compensation cross-couplings, the NTF has complex poles and zeros and is nearly symmetric around the center frequency. All poles and zeros are shifted by $e^{j\omega_c T_s}$ toward the upper half of unit circle in the z-plane. Otherwise, without the compensation cross-couplings, the poles of the NTF_{QBP} are asymmetrically placed around $e^{j\omega_c T_s}$ and thus, the NTF_{QBP} are also asymmetric at the out-of-band. Furthermore, one pole is toward the outside of the unit circle, while introducing an instability. That's why the feed-forward coefficients affect the zero placement of the polyphase filter and therefore the pole locations of the NTF_{QBP} .

It should be noted that without the proposed zero compensation for the capacitive feedforward coefficients, the higher the center frequency, the less is the modulator stability [KJWH08a]. Therefore, in a system with a higher center frequency, the compensation cross-couplings should be absolutely applied for the modulator stability. The compensation cross-couplings caused by the capacitive feedforward do not rarely affect the maximum SNR of the modulator except for second-order modulator (see chapter 6.2), because the in-band noise level depends on local feedback loops and feedback coefficients for lossy integrators.

Until now, in this chapter, starting from the consideration of the lowpass filter, the implementation of the polyphase filter with the CICFF topology have been presented. We can summarize as follows:

- The CICFF topology which is one of the CIFF topologies, is suited for low power and low voltage applications. Feedforward coefficients are implemented as the

ratios of the feedforward capacitors to last integrating capacitor.

- Polyphase filters with the CICFF topology can be obtained by the conventional cross-couplings for moving poles to center frequency and by the proposed compensation cross-couplings for moving zeros caused by capacitive feedforward, without extra active components.
- The compensation cross-couplings affects the modulator stability, especially for a higher center frequency.

5. Analysis of Nonidealities

This chapter presents non-ideal effects of CT-QBP $\Sigma\Delta$ Ms, such as finite gain bandwidth of the amplifiers, excess loop delay, clock jitter, nonlinearity caused by DAC unit element mismatch. The analytical results can be used in predetermining the modulator performance. The compensation or cancellation method can be applied to an optimized CT-loop filter H_{PPF} design and a selection of the modulator parameters.

5.1. Finite Gain Bandwidth

The polyphase filter is implemented by a cascade combination of the complex integrators which is realized by cross-couplings between the input and the output of the real integrators. Thus, the polyphase filter behavior is affected by amplifiers, especially their finite GBW. Finite GBW reduces the whole performance of the modulator. The finite GBW causes a gain error and an additional second pole of the real integrator in CT lowpass $\Sigma\Delta$ modulators[CKE06],[OGM04],[OGM03c]

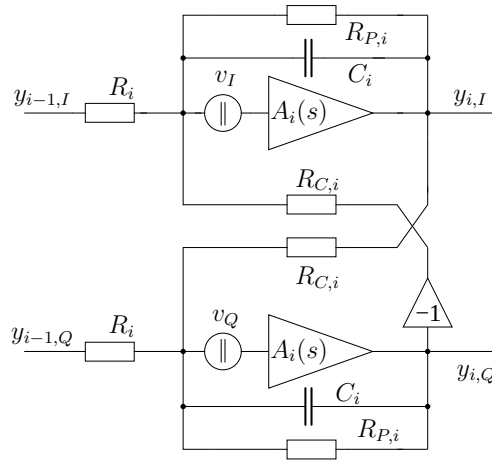


Figure 5.1.: Complex integrator with additional voltage sources caused by finite GBW.

This section presents the effects caused by finite GBW, and gives a practical limitation in design of CT-QBP $\Sigma\Delta$ Ms and compensation method. The complex integrator-single polyphase filter-with finite GBW can be modeled as shown in Figure 5.1. At

the inputs of the amplifiers, the additional voltage sources ($v_I = y_{i,I}/A_i(s)$, and $v_Q = y_{i,Q}/A_i(s)$) are inserted.

5.1.1. Stability of the Complex Integrator

Let's first consider the conventional complex integrator without the feedback resistor for the lossy integrator. The open-loop gain of the single-pole amplifier is

$$A(s) = \frac{A_{DC}}{s/w_p + 1}, \quad GBW = A_{DC} \cdot w_p \text{ (rad/s)}, \quad (5.1)$$

where A_{DC} and w_p are DC gain and a first pole of the single-pole amplifier, respectively. Then, the transfer function of the i -th complex integrator of the polyphase filter is

$$CINT_{i,0}(s) = \frac{a_i}{(s - jw_c) + (1/A_i(s)) \cdot (s + a_i + w_c)}. \quad (5.2)$$

Here, $A_i(s)$ and a_i are the open-loop gain of the amplifier and scale value for the i -th integrator in the cascaded complex integrators, respectively. The transfer function has a dominant pole around w_c and an additional (parasitic) pole. The stability of the complex integrator depends on the placement of the dominant pole and the parasitic pole. The parasitic pole is located in the left-half of the s -plane, within a limitation imposed by the permissible design parameters. The dominant pole might locate at the right-half plane, depending on the selection of the complex integrator parameters. This implies that the complex integrator might become unstable.

The dominant pole locus was simulated with Matlab. The sample clock used in this analysis, is $f_s=100$ MHz and DC gain is $A_{DC}=60$ dB. Figure 5.2 shows the dominant pole locus of the complex integrator. The pole moves toward the left-half plane with increasing GBW and the stability of the complex integrator is hence improved. In addition, it can be seen that the greater the integrator scale a_i is, the more stable is the complex integrator but the deviation from the desired center frequency w_c is increased (see next subsection). Furthermore, when a_i increases, the amplifier has to provide a higher output driven current which increases power consumption.

The pole placement is also effected by the selection of f_c . Figure 5.3 shows the dominant pole locus which is plotted with different center frequencies. It can be seen that the greater the center frequency, i.e. the lower the cross-coupling resistor $R_{C,i}$, the worse is the stability of the complex integrator. This implies that the design of the complex integrator is more critical than that of the lowpass integrator.

Next, the pole of the amplifier at the $w_p = 2\pi f_p$ in Equation (5.1), where f_p is -3 dB frequency, is one of the most important factors for the stability. In order to consider an effect of the w_p , focus is shifted to a lossy integrator, because w_p can be enhanced in this structure without any increase in GBW. In fact, the increment of GBW in amplifiers causes the increment of w_p when A_{DC} is constant. Therefore, it is

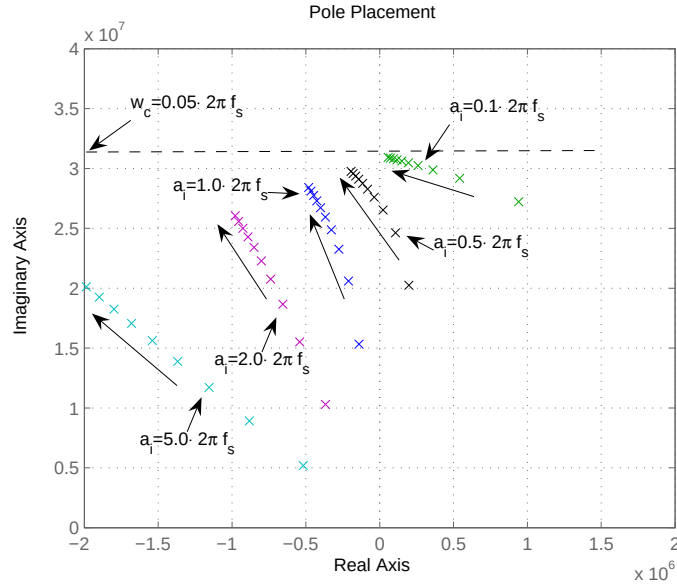


Figure 5.2.: The dominant pole locus of the complex integrator with $f_c=5$ MHz. The arrow denotes the increasing direction of GBW. $\text{GBW}=\eta \cdot 2\pi f_s$ with $\eta = 1 \sim 10$, and the step size of η is 1.

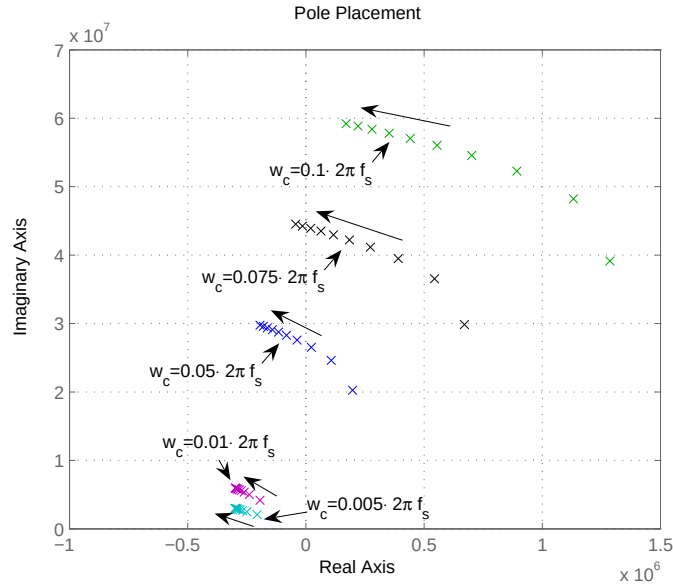


Figure 5.3.: The dominant pole locus of the complex integrator with $a_i = 0.5 \cdot 2\pi f_s$.

difficult to distinguish the effects of GBW and w_p . When using the lossy integrator, its open-loop gain $A'(s)$ of an equivalent amplifier is modified as shown in Figure 5.4 and the transfer function is

$$A'(s) = \frac{K}{K+1} \cdot \frac{GBW}{s + (w_p + GBW/(K+1))}. \quad (5.3)$$

Here, $K = R_2/R_1$. For $A_{DC} \gg K$,

$$\begin{aligned} w'_p &= w_p + GBW/(K+1), \\ A'_{DC} &\approx K, \quad GBW \approx GBW. \end{aligned} \quad (5.4)$$

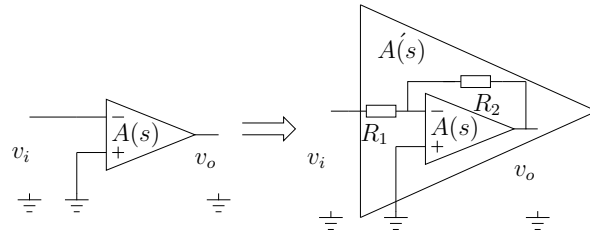


Figure 5.4.: The open-loop gain of the equivalent amplifier of the lossy integrator.

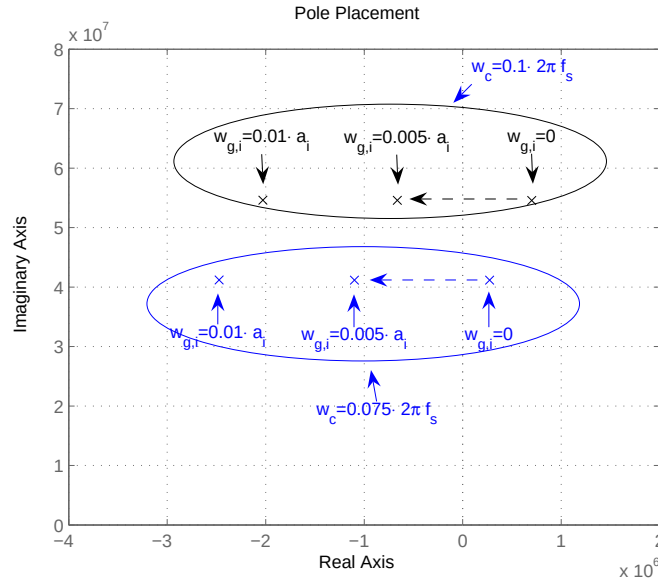


Figure 5.5.: Pole placement with $w_{g,i}$. Here, $GBW = 4 \cdot 2\pi f_s$, $a_i = 0.5 \cdot 2\pi f_s$.

In the lossy integrator, it can be seen that the equivalent pole w_p is shifted from original values w_p without significant change of GBW. The greater the feedback resistor R_2 for the lossy integrator, the greater is the pole w_p , but the lower is the equivalent DC gain A_{DC}' . For the lossy complex integrator, the transfer function is

$$CINT_i(s) = \frac{a_i}{(s + w_{g,i} - jw_c) + (1/A_i(s)) \cdot (s + a_i + w_{g,i} + w_c)}, \quad (5.5)$$

where $w_{g,i} = 1/(R_{P,i}C_i) = a_i g_i$. We can guess that the dominant pole is nearly shifted by $w_{g,i}$ toward the left-half plane in s -domain. This implies that the complex integrator can become more stable, when using the complex lossy integrator. From Figure 5.5, it can be directly seen that the dominant pole can be located in the left-half s -plane when using the lossy complex integrator, even without any GBW enhancement.

Figure 5.6 shows that when finite GBW increases, the complex integrator becomes as stable as the higher feedback resistor $R_{P,i}$ (see Figure 5.1) is chosen. Since $w_{g,i}$ mainly affects the real part of the dominant pole of the lossy complex integrator, the deviation from f_c does not reduce with $w_{g,i}$. It should be noted that when using the lossy integrator, the linearity and the SNDR of the modulator can be reduced because the in-band noise power is increased. Here, an effect of the finite open-loop gain A_{DC} of the amplifier should also be mentioned. It mainly causes a gain error in the passband, similar to the lossy integrator.

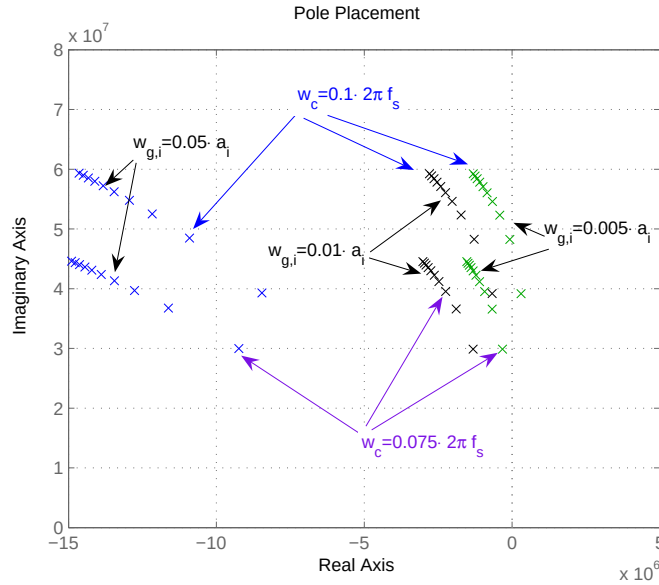


Figure 5.6.: The dominant pole locus of the complex lossy integrator, with $a_i = 0.5 \cdot 2\pi f_s$.

5.1.2. Deviation from the Center Frequency

In an ideal case, the center frequency, f_c , of the complex integrator is uniquely defined by the product of cross-coupling resistor and integrating capacitor. Unfortunately, due to finite GBW, not only stability might be worsened but also the frequency shifting is deviated from ideal f_c . The “real” center frequency, $f_{c,r}$, which is shifted by the complex integrator can seriously deviate from the ideal f_c as shown in Equations (5.2) and (5.5) as well as in Figure 5.7. When the amplifier GBW increases, the real center frequency, $f_{c,r}$, shifts toward the ideal center frequency, f_c . In order to reduce the deviation, the finite GBW of the amplifiers should be as great as possible, satisfying the demand for maximum power consumption of the modulator. This implies that a high amplifier GBW is more critical for CT-QBP $\Sigma\Delta$ Ms than for CT lowpass $\Sigma\Delta$ Ms.

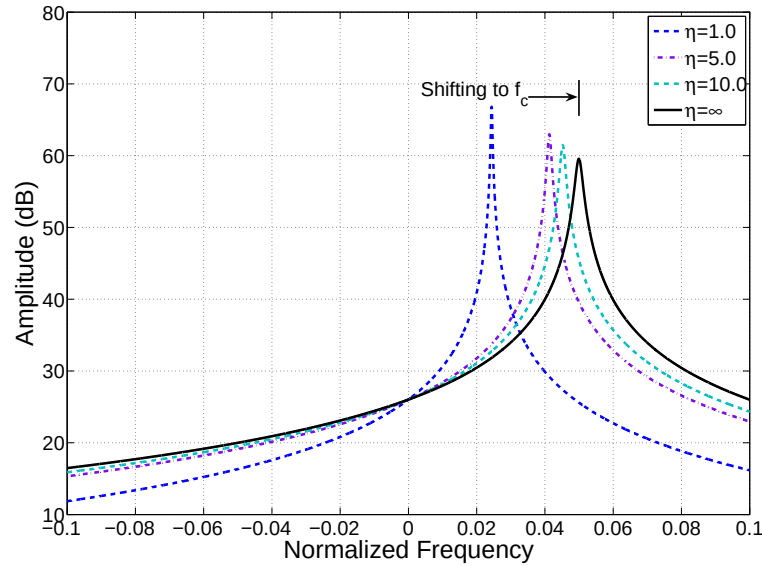


Figure 5.7.: The shifted complex integrator with different GBW, where $a_i = 1.0 \cdot 2\pi f_s$, $f_c = 0.05 \cdot 2\pi f_s$ and $\eta = GBW_i / (2\pi f_s)$.

The integrator scale a_i also severely influences on the deviation from f_c , because the imaginary part of the complex integrators dominant pole seriously varies with a_i as shown in Figure 5.2. Figure 5.8 shows the relative deviation $((f_c - f_{c,r}) \cdot 100 / f_c [\%])$ between the shifted frequency $f_{c,r}$ and ideal center frequency, f_c , vs. GBW, with different integrator scale values. The relative deviation changes notably with the different selections of a_i . The relative deviation is similar to that of Figure 5.8, with no relation to chosen center frequency f_c . This means that the lower the center frequency is, the lower is an absolute deviation from the center frequency. Also, note that if the

ratios of GBW, f_c and a_i relative to any sample frequency, f_s , are kept as constants, their deviations are similar to Figure 5.8.

In order to reduce the deviation from f_c , the integrator scale should be as low as the stability of complex integrator ensures. As shown in the above subsection, a reduced scale impairs the stability. Therefore, it is desirable to employ the lossy complex integrator with a low integrator scale, because it provides the stability of complex integrator, while the deviation from the targeted f_c is reduced.

But, the lossy integrator with certain lower integrating scale suffers from the following problems:

- It can decrease the maximum SNDR and linearity of the modulator because of the reduced integrator scale and feedback coefficient for the lossy integrator.
- The reduced integrator scale needs an increased chip area due to great R_i and C_i . Especially, since the feedback resistor $R_{P,i} = (\text{few } 10 \sim \text{few } 100) \cdot R_i$, sometimes it might be too great to implement on a chip.

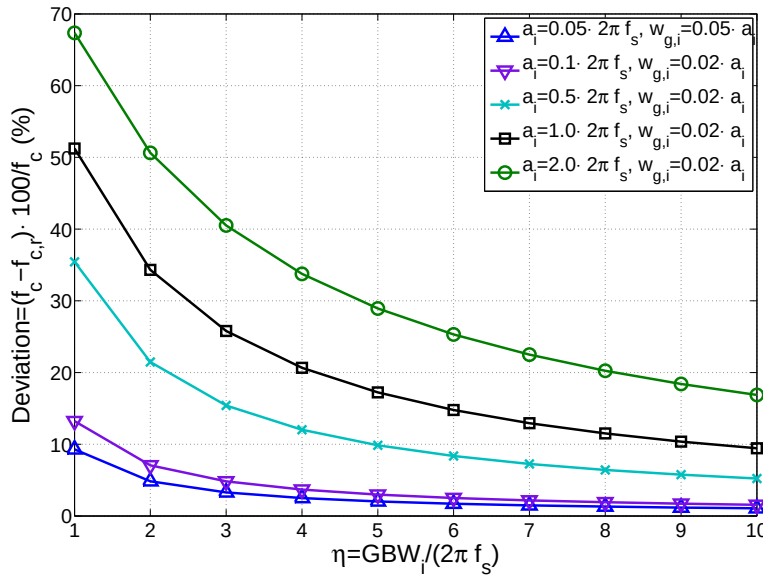


Figure 5.8.: The relative deviation between $f_{c,r}$ and f_c , where $f_c = 0.05 \cdot 2\pi f_s$.

5.1.3. Polyphase Filter with CIFF and CICFF Topologies

Polyphase filters are implemented by a cascade of the complex integrators. Therefore, the whole behavior of the polyphase filter depends on the individual complex integrators and effects the modulator performance.

For the CIFF topology, the transfer functions of all complex integrators in the polyphase filter are identical to Equations (5.2) or (5.5) for the complex lossy integrator. The dependence of every complex integrator on finite GBW might vary. For example, even though the finite GBW of all amplifiers of the polyphase filter are the same, the stability margin of every complex integrator and its deviation from ideal f_c differ due to the choices of the different integrator scales a_i . Especially, the stability margin of the lossy complex integrators significantly depends on its feedback coefficients. Figure 5.9 shows the second-order polyphase filter with CIFF topology whose poles locate at jw_c in s -domain for the ideal case.

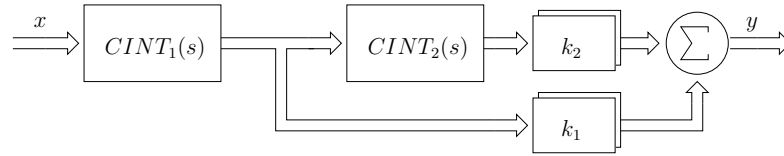


Figure 5.9.: The second-order polyphase filter with finite GBW.

The amplitude response of the second-order polyphase filter with CIFF topology was plotted in Figure 5.10. When scale values a_1 and a_2 of the two complex integrators are the same, the two dominant poles of the polyphase filter locate at point C as shown in Figure 5.10. On the other hand, when $a_1 \neq a_2$, the two poles are separately placed at point A and B. The deviation caused by the complex integrator with greater scale is larger than that of the complex integrator with lower scale.

For the CICFF topology as shown in Chapter 4, all stages except for the last stage with the capacitive summation, are the complex integrators and their transfer functions are the same as Equation (5.2) or (5.5). The last stage has a huge capacitive and resistive load at the input for the capacitive summation. The sum of the feedforward coefficients is

$$M = 1 + \sum_{i=1}^{n-1} k_i. \quad (5.6)$$

The final output y of the last stage is

$$y = \frac{a_n \cdot y_{n-1} + \sum_{i=1}^{n-1} k_i (s - jw_c) \cdot y_i}{(s + w_{g,n} - jw_c) + (1/A_n(s)) \cdot (M(s + w_c) + a_n + w_{g,n})}. \quad (5.7)$$

Figure 5.11 shows the deviation from f_c in the last quadrature integrator which has the capacitive summation. Obviously, when the feedforward capacitors, i.e., the feedforward coefficients increase, the deviation from f_c also increases due to finite GBW of the last amplifier. This implies that the GBW of the last amplifier should be greater than the GBW of the other stages. In general, the higher the GBW is, the greater the power consumption. Thus, it might have a loss of one of the significances of the CICFF topology for low power application.

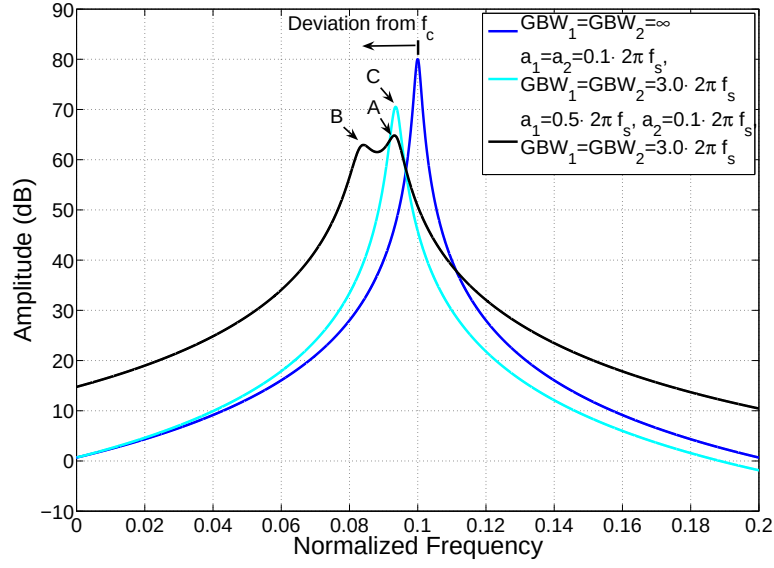


Figure 5.10.: The amplitude response of the second-order polyphase filter with finite GBW, where $f_c = 0.1 \cdot 2\pi f_s$, $w_{g,1} = 0.01 \cdot a_1$ and $w_{g,2} = 0.01 \cdot a_2$.

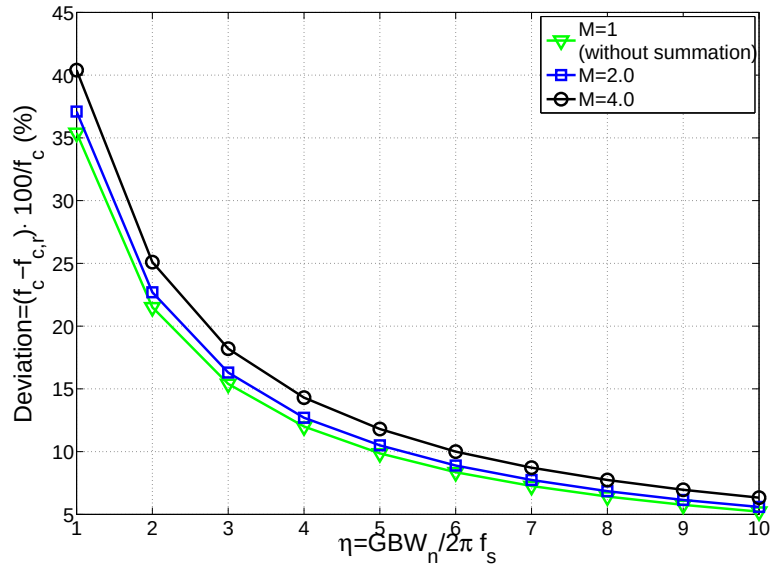


Figure 5.11.: The relative deviation in the last stage of CICFF topology, when $f_c = 0.05 \cdot 2\pi f_s$, $a_n = 0.5 \cdot 2\pi f_s$ and $w_{g,n} = 0.02 \cdot a_n$.

Figure 5.12 shows the NTF_{QBP} of the second-order CT-QBP $\Sigma\Delta$ M with CIFF and CICFF topologies. Here, the notches labeled A and B indicate the deviations from f_c which are caused by the first and the second complex integrator with finite GBW. The deviation from f_c in the NTF_{QBP} increases with reducing the GBW in the CICFF as well as the CIFF topology. But, in the CICFF topology, the notch at point B caused by the last stage with capacitive summation is pushed farther from f_c than the notches at point A and C.

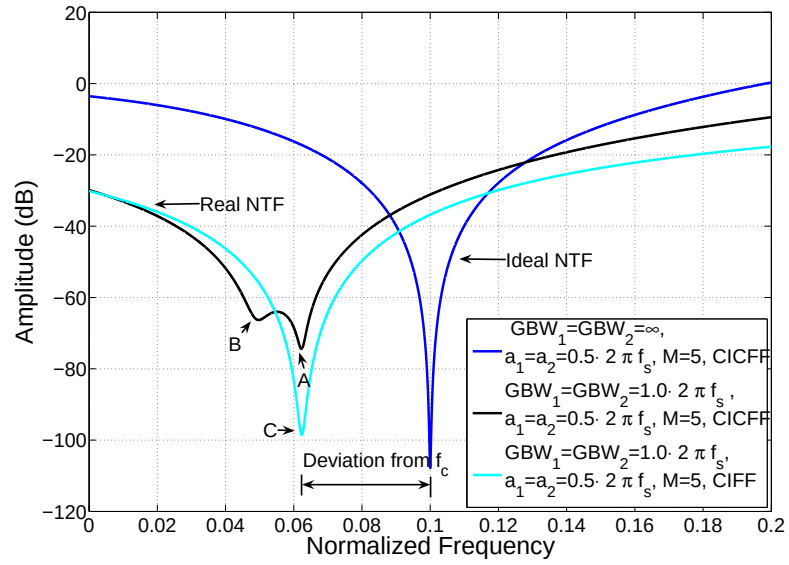


Figure 5.12.: The NTF_{QBP} of the second-order CT-QBP $\Sigma\Delta$ M with finite GBW.

For a lower M and f_c in the CICFF topology, the minimum level of the NTF and the deviation from f_c decreases. The shifted frequency of the CICFF topology approaches to that of the CIFF topology and the notch at point B caused by the last quadrature integrator nearly coincides with the notch at point A. In the analysis of the CIFF topology, it has been assumed that the GBW of an additional active component for the summation is infinite and the feedforward coefficients are linear. Note that the modulator performance might be reduced[TMRPW03], when the summation in the CIFF topology is done with active components exhibiting finite GBW, as shown for the CICFF topology.

Now, we can conclude as follows:

- Finite GBW of all amplifiers in the polyphase filter affects the performances of both the CIFF and the CICFF topology, but the finite GBW of the amplifier in the last stage of the CICFF topology has a more significant effect than that of the others.

- The stability margin of complex integrators and the deviation from the ideal f_c caused by the finite GBW should carefully be considered in the design of CT quadrature bandpass $\Sigma\Delta$ modulators.
- An undesirable deviation which are not permitted from the modulator specification, should be compensated or reduced.

5.1.4. Compensation of the Deviation from the Center Frequency

In order to compensate or reduce the deviation from f_c , let's consider again Equation (5.5). The first term of the denominator is an ideal one and second term is introduced by the finite GBW of the amplifiers. In this non-ideal term, the integrator scale a_i contributes significantly as shown in Figure 5.2, because the input resistor R_i is much less than the feedback resistors and cross-coupling resistors. Therefore, when a_i of the second term of the denominator of Equation (5.5) is reduced or removed, the deviation from f_c would notably be decreased.

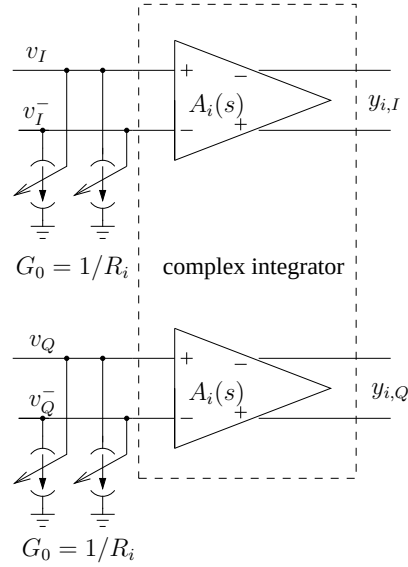


Figure 5.13.: The compensation by transconductors in the complex integrator inputs.

In the Figure 5.1, extra currents v_I/R_i and v_Q/R_i caused by finite GBW introduces the term $a_i/A_i(s)$ in the denominator of Equation (5.5). In order to remove the extra currents v_I/R_i and v_Q/R_i , transconductors with $G_0 = 1/R_i$ can be applied as shown in Figure 5.13. Their output currents are fed into the virtual ground nodes of the fully differential amplifiers. In an ideal case, the contribution of v_I/R_i and v_Q/R_i is canceled by the transconductors with $G_0 = 1/R_i$. Therefore, the term $a_i/A_i(s)$ in the

denominator of Equation (5.5) can be removed. In practice, the perfect matching with $G_0 = 1/R_i$ is difficult in the design of the transconductors. But, the properly matched transconductors can give a desirable compensation effect. After compensating, the transfer function of the complex integrator can be represented with a compensation coefficient γ_i which denotes the mismatch between real and ideal transconductance $G_0 = 1/R_i$.

$$CINT_i(s) = \frac{a_i}{(s + w_{g,i} - jw_c) + (1/A_i(s)) \cdot (s + \gamma_i \cdot a_i + w_{g,i} + w_c)}. \quad (5.8)$$

For the perfect matching, $\gamma_i = 0$. Thus, the effect of the v_I/R_i and v_Q/R_i is completely removed. Figure 5.14 shows the reduced relative deviation from the center frequency when $\gamma_i = 0.1$. It can be seen that the relative deviation from f_c is significantly reduced. Note that the concept can be similarly applied if the impact of $R_{C,i}$ dominates in the second term of the denominator in Equation (5.5). The currents $v_I/R_{C,i}$ and $v_Q/R_{C,i}$ then will be cancelled by means of transconductors $G_C = 1/R_{C,i}$.

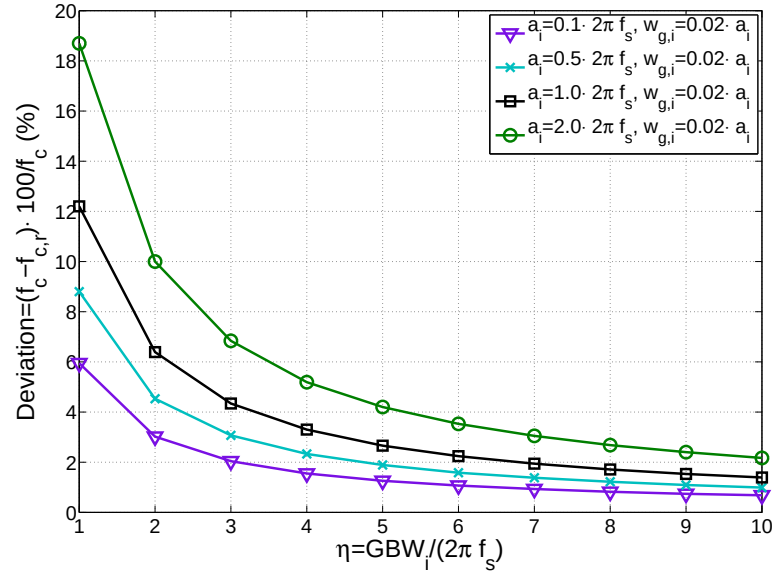


Figure 5.14.: The reduced relative deviation from f_c , where $f_c = 0.05 \cdot 2\pi f_s$.

5.2. Excess Loop Delay

CT $\Sigma\Delta$ Ms seriously suffer from excess loop delay, which can not be seen in discrete-time designs. The excess loop delay is a nonzero delay between the quantizer clock edge and the feedback DAC pulse switching point. It depends on the number of the

transistors in the feedback path, the switching speed and parasitic capacitance. The compensation strategies of excess loop delay in lowpass and real bandpass CT $\Sigma\Delta$ s have been previously proposed in [CS99b],[GSS97],[AL04],[CS98a],[SS04] and [TC05]. Based on the equivalent transformation between CT and DT domain, these used one or more additional feedback DAC pulse with tuned coefficients from the mapping of the transfer function[CS99b],[GSS97]. The disadvantages of this method are high sensitivity to process variation, especially the additional coefficients seriously depend on loop delay. Furthermore, it is impossible to make additional DAC pulse such as HRZ and RZ which are identical delay with NRZ.

The compensation scheme of excess loop delay in the CT-QBP $\Sigma\Delta$ s has not been published, yet. The effects of loop delay in CT-QBP $\Sigma\Delta$ s were firstly introduced in [HL03] and only root-locus in noise shaping transfer function for the stability were considered without compensation on excess loop delay.

This section firstly presents analytical expressions on excess loop delay in the CT-QBP $\Sigma\Delta$ with CIFF topology and the compensation scheme on excess loop delay is proposed [KJH07].

5.2.1. Analysis of Excess Loop Delay

A CT $\Sigma\Delta$ is inherently a DT system since there is a sampler inside the loop as shown in Figure 5.15. The equivalent transfer function $\hat{H}(z)$ in DT domain can be derived from Equation (5.9).

$$Z^{-1}(\hat{H}(z)) = L^{-1}(DAC_{(\alpha,\beta)}(s)\hat{H}(s))|_{t=nT_s}. \quad (5.9)$$

DAC impulse response is $DAC_{(\alpha,\beta)}(t) = 1, (\alpha \leq t/T_s < \beta, \quad 0 \leq \alpha < \beta \leq 1)$ and is zero in other case. After applying Laplace transformation it yields

$$DAC_{(\alpha,\beta)}(s) = \frac{\exp((- \alpha T_s)s) - \exp((- \beta T_s)s)}{s}. \quad (5.10)$$

Figure 5.15 shows a second-order CT-QBP $\Sigma\Delta$ with CIFF topology which has a local feedback loop b_1 for the optimized zero placement of noise-shaping transfer function, feedforward coefficients k_1 and k_2 , and cross-coupling c_1 and c_2 for the translation to center frequency. Without consideration of loop delay, its transfer function in CT domain is derived as follows:

$$\hat{H}(s) = \frac{k_1 w_0 \sqrt{A}(s - jw_c) + k_2 w_0^2 A}{(s - jw_c - jw_0)(s - jw_c + jw_0)}, \quad (5.11)$$

where $w_0^2 = a_1 a_2 b_1$, $w_c = a_1 c_1 = a_2 c_2$ and $A = 1/b_1$.

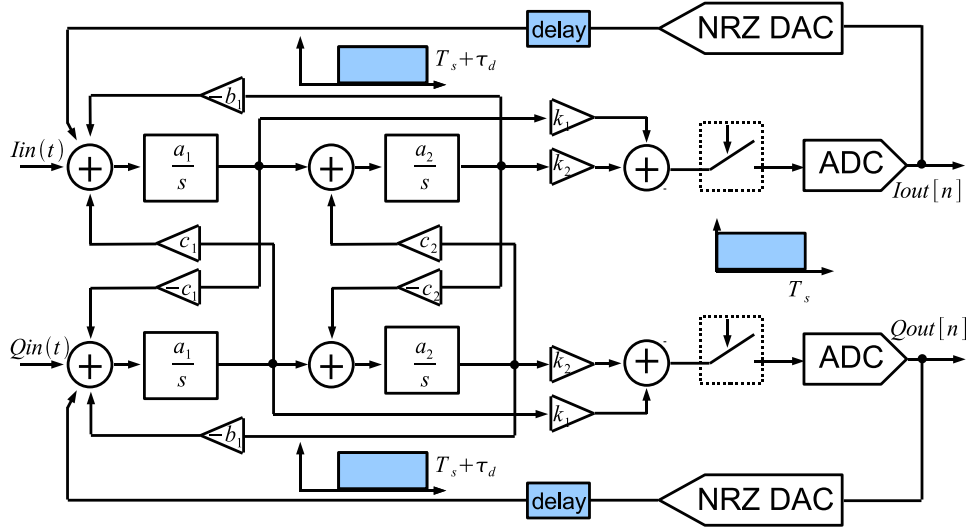


Figure 5.15.: CT complex $\Sigma\Delta$ modulator with nonzero-delayed NRZ..

The above equation can be changed as a partial fraction expansion.

$$\hat{H}(s) = \frac{A_{01}}{(s - jw_c - jw_0)} + \frac{A_{01}^*}{(s - jw_c + jw_0)}, \quad (5.12)$$

where $A_{01} = 0.5w_0(k_1\sqrt{A} - jk_2A)$ and A_{01}^* is a conjugation complex of A_{01} .

Many designers use NRZ DAC output pulse which remains over a full period, because the NRZ DAC pulse are easily made by regenerative latching comparators and has less other nonideal effects than that of RZ and HRZ. Now we can apply the transformation (5.9) to transfer function $\hat{H}(s)$ with zero-delay NRZ DAC pulse. DT loop filter transfer function $\hat{H}(z)$ is derived by using transformation tables in [CS99b]

$$\hat{H}(z) = \frac{A_{01} \cdot (e^{s_1 T_s} - 1)}{s_1(z - e^{s_1 T_s})} + \frac{A_{01}^* \cdot (e^{s_1 T_s} - 1)}{s_2(z - e^{s_2 T_s})}, \quad (5.13)$$

where $s_1 = jw_c + jw_0$, $s_2 = jw_c - jw_0$.

The equivalent transfer function $H(z)$ with nonzero-delayed NRZ pulse is seriously changed and moved away from the desirable DT loop filter transfer function (5.13). Based on the transfer function $\hat{H}(s)$ in CT domain, DT loop filter transfer function with different excess loop delay (τ_d) is calculated according to procedure of [CS99b], and its calculation result depends on the excess loop delay. Therefore, DT loop filter transfer function can be seen as $H_D(z, \tau_d)$ where excess loop delay (τ_d) is considered

as a parameter, and is derived as follows:

$$H_D(z, \tau_d) = \frac{A_{01} \cdot ((e^{s_1 T_s})^{1-\tau_d} - 1)}{s_1(z - e^{s_1 T_s})} + z^{-1} \cdot \frac{A_{01} \cdot (e^{s_1 T_s} - (e^{s_1 T_s})^{1-\tau_d})}{s_1(z - e^{s_1 T_s})} + \frac{A_{01}^* \cdot ((e^{s_2 T_s})^{1-\tau_d} - 1)}{s_2(z - e^{s_2 T_s})} + z^{-1} \cdot \frac{A_{01}^* \cdot (e^{s_2 T_s} - (e^{s_2 T_s})^{1-\tau_d})}{s_2(z - e^{s_2 T_s})} \quad (5.14)$$

From Equation (5.14), it can be seen that the order of the transfer function in case of nonzero-delay is increased by one order compared to an ideal case, and an additional pole appears. For ideal $\Sigma\Delta$ modulator, when $\tau_d = 0$ the Equation (5.14) turns into (5.13). However, $\tau_d \neq 0$, the equivalent DT loop filter transfer function is significantly changed from Equation (5.13).

Above equations based on transformation (5.9) and architecture of Figure 5.15 are fairly effective in implementation and analysis of CT-QBP $\Sigma\Delta$ M for a low center frequency f_c . On the other hand, when higher f_c is, $NTF(z)$ obtained by equivalent DT loop filter has an asymmetric pole placement and some pole may be placed outside a unit circle in a z -domain. This is due to the feedback DAC pulse still centered around DC. Therefore for higher f_c , a cross-coupling for feedback DAC pulse should be added in Figure 5.15, and the term $DAC_{(\alpha,\beta)}(s)$ in Equation (5.9) is replaced by $DAC_{(\alpha,\beta)}(s - jw_c)$. But, it is difficult to realize as shown in Chapter 3.

Here we consider the excess loop delay in CT-QBP $\Sigma\Delta$ with relatively low f_c compared to a sampling frequency, f_s , using the architecture of Figure 5.15 and transformation (5.9). This is because the effect of loop delay is much greater than in the architecture with cross-coupled feedback DAC. Furthermore the architecture without cross-coupled feedback DAC can be used for low-IF receivers.

5.2.2. Effects of Excess Loop Delay

The most important effect of the excess loop delay is to increase the in-band quantization noise power and therefore to introduce the degradation in SNR. Figure 5.16 shows the output spectrum of the CT-QBP $\Sigma\Delta$ modulator with nonzero-delay NRZ DAC pulse ($\tau_d/T_s = 0.5$). It can be seen that the in-band noise power is much greater than in the ideal case and the asymmetry in noise spectrum appears in out-of-band. The SNR degradation due to the excess loop delay is shown in Figure 5.17. For higher center frequency f_c , the SNR degradation is much greater than for lower f_c . As above mentioned, this is because for higher f_c , the $NTF_{QBP}(z)$ becomes easily unstable due to the asymmetric and outward pole placement at the lower loop delay. The parameters used in simulation are $a_1 = a_2 = 9.0e6$, $b_1 = 0.04$, $k_1 = k_2 = 1$, $T_s = 32$ MHz with 1-bit quantizer, and the bandwidth f_B of this modulator is 1 MHz.

The excess loop delay also affects the stability of the CT $\Sigma\Delta$ M. In order to consider this effect, the noise-shaping transfer function is calculated from Equation (5.14). Due to additional pole ($z = 0$), $NTF_{QBP}(z)$ with excess loop delay has one additional zero

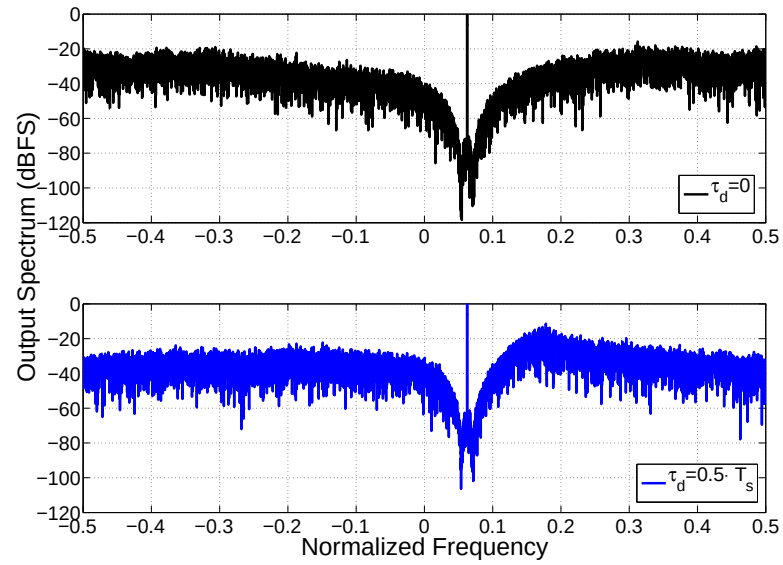


Figure 5.16.: Output spectrum, (up) zero delayed, (down) 50% delayed when $f_c = 2$ MHz.

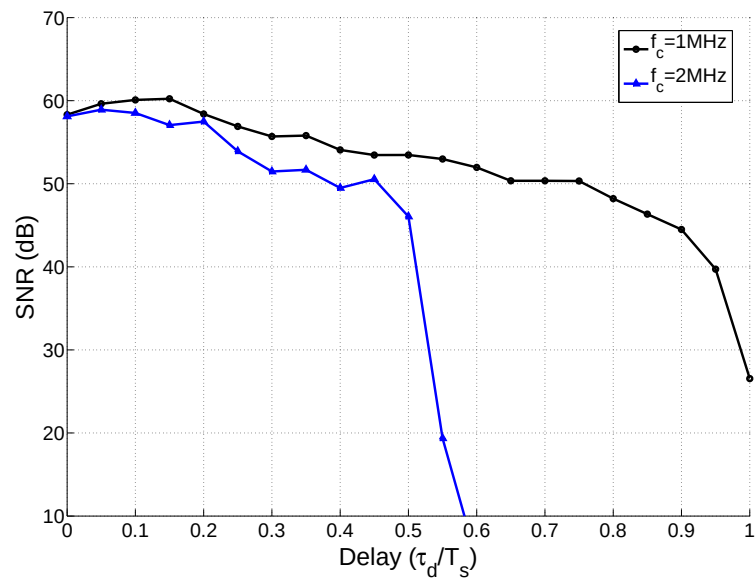


Figure 5.17.: SNR vs. the excess loop delay τ_d/T_s .

and pole, i.e., the order of denominator and numerator of $NTF(z)_{QBP}$ is increased by one. The root-locus of $NTF(z)_{QBP}$ as a function of τ_d is shown on the unit circle in Figure 5.18. The pole of $NTF(z)_{QBP}$ is outside the unit circle when the excess loop delay increases. It implies that the higher excess loop delay can result in an unstable $\Sigma\Delta M$. From Figure 5.18, it can be also seen that the poles of the $NTF_{QBP}(z)$ are asymmetrically located around $e^{j\omega_c T_s}$ which corresponds to $j\omega_c$ in CT domain.

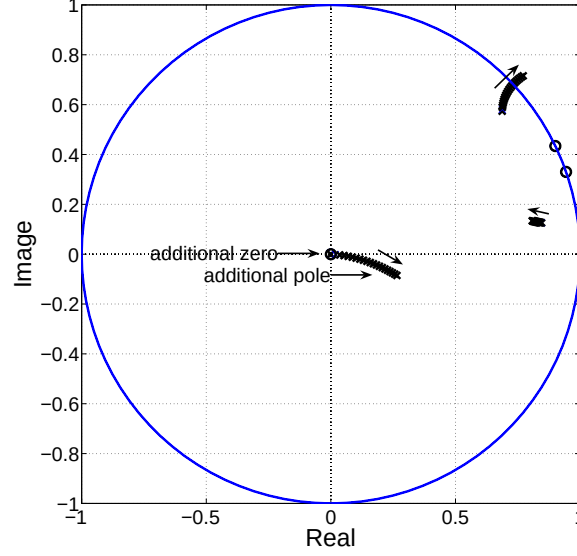


Figure 5.18.: The root-locus of $NTF_{QBP}(z)$ vs. τ_d/T_s , ($= 0.1 - 1.0$) when $f_c = 2$ MHz.

An asymmetric placement of poles also effects the modulator stability. Usually the root-locus gives a sufficient condition but is not a necessary condition. Due to the asymmetric placement, the $NTF_{QBP}(z)$ in DT domain are asymmetrically introduced around center frequency. It can not track input signal and cause the instability. It implies that the CT-QBP $\Sigma\Delta M$ can become unstable more easily than the lowpass $\Sigma\Delta M$ by excess loop delay. Note that the pole of $NTF_{QBP}(z)$ is placed outside the unit circle at lower loop delay, when the center frequency increase.

In addition, excess loop delay is effected to a peak SNDR of the CT-QBP $\Sigma\Delta M$ s. This is due to the reduction of the maximum stable amplitude with the loop delay.

5.2.3. Compensation of Excess Loop Delay

From Equation (5.14), it can be recognized that if the term z^{-1} (which is due to the excess loop delay) is removed, the increased order of $NTF_{QBP}(z)$ is decreased by one. To remove the term z^{-1} , an additional path which has unity delay with complex

coefficient k_{c0} is inserted in front of quantizer as shown in Figure 5.19. Also, the complex feedforward coefficients k_{c1} , k_{c2} is used for mapping to Equation (5.13). The transfer function of Figure 5.19 can be written as follows:

$$H_C(z, \tau_d) = \frac{A_{11} \cdot ((e^{s_1 T_s})^{1-\tau_d} - 1)}{s_1(z - e^{s_1 T_s})} + z^{-1} \cdot \frac{A_{11} \cdot (e^{s_1 T_s} - (e^{s_1 T_s})^{1-\tau_d})}{s_1(z - e^{s_1 T_s})} + \frac{A_{11}^* \cdot ((e^{s_2 T_s})^{1-\tau_d} - 1)}{s_2(z - e^{s_2 T_s})} + z^{-1} \cdot \frac{A_{11}^* \cdot (e^{s_2 T_s} - (e^{s_2 T_s})^{1-\tau_d})}{s_2(z - e^{s_2 T_s})} + k_{c0} \cdot z^{-1}, \quad (5.15)$$

where $A_{11} = 0.5w_0(k_{c1}\sqrt{A} - jk_{c2}A)$ and A_{11}^* is a conjugation complex of A_{11} .

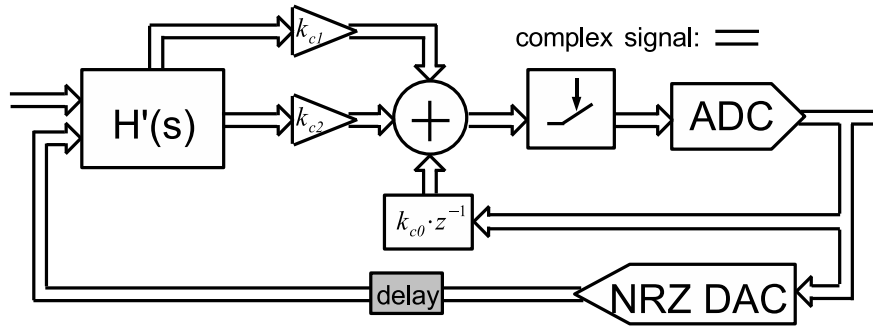


Figure 5.19.: The compensation scheme of excess loop delay.

By the desirable selection of the complex coefficients k_{c0} , k_{c1} and k_{c2} , an additional pole is replaced closed to additional zero (original point in Figure 5.18) in $NTF_{QBP}(z)$, the additional pole and zero are removed and the symmetric placement of poles can be obtained around $e^{jw_c T_s}$ in the unit circle. If $\hat{H}(z) = \hat{H}(z, k_1, k_2)$, this can be expressed for a compensated DT loop filter transfer function as follows:

$$H_C(z, k_{c0}, k_{c1}, k_{c2}, \tau_d) = \hat{H}(z, k_1, k_2) \quad (5.16)$$

Therefore the compensation on the excess loop delay τ_d corresponds to find the complex feedforward coefficients k_{c0} , k_{c1} and k_{c2} which satisfy Equation (5.16) in Figure 5.19, that is,

$$\begin{aligned} k_{c0} &= f(k_1, k_2, \tau_d), \\ k_{c1} &= f(k_1, k_2, \tau_d), \\ k_{c2} &= f(k_1, k_2, \tau_d). \end{aligned} \quad (5.17)$$

If the complex coefficients k_{c0} , k_{c1} and k_{c2} are determined from (5.16) like Equation (5.17), the CT complex $\Sigma\Delta$ modulator of Figure 5.19 can perfectly compensate the effects of excess loop delay. The above compensation method of excess loop delay can be adapted to any CT complex $\Sigma\Delta$ modulator with CIFF topology.

Table 5.1.: The feedback coefficient k_{c0} vs. τ_d

τ_d/T_s	k_{c0}
0.1	$0.028k_1 + j0.000k_1 + 0.000k_2 + j0.000k_2$
0.2	$0.056k_1 + j0.002k_1 + 0.002k_2 + j0.000k_2$
0.3	$0.084k_1 + j0.005k_1 + 0.004k_2 + j0.000k_2$
0.4	$0.112k_1 + j0.009k_1 + 0.006k_2 + j0.000k_2$
0.5	$0.140k_1 + j0.014k_1 + 0.010k_2 + j0.001k_2$
0.6	$0.167k_1 + j0.020k_1 + 0.014k_2 + j0.002k_2$
0.7	$0.194k_1 + j0.027k_1 + 0.019k_2 + j0.003k_2$
0.8	$0.221k_1 + j0.035k_1 + 0.025k_2 + j0.005k_2$
0.9	$0.248k_1 + j0.044k_1 + 0.031k_2 + j0.007k_2$
1.0	$0.274k_1 + j0.054k_1 + 0.038k_2 + j0.010k_2$

Table 5.2.: The feedforward coefficient k_{c1} vs. τ_d

τ_d	k_{c1}
0.1	$0.999k_1 + j0.039k_1 + 0.028k_2 + j0.001k_2$
0.2	$0.996k_1 + j0.078k_1 + 0.056k_2 + j0.004k_2$
0.3	$0.993k_1 + j0.117k_1 + 0.084k_2 + j0.010k_2$
0.4	$0.987k_1 + j0.156k_1 + 0.111k_2 + j0.018k_2$
0.5	$0.980k_1 + j0.195k_1 + 0.138k_2 + j0.027k_2$
0.6	$0.972k_1 + j0.233k_1 + 0.164k_2 + j0.039k_2$
0.7	$0.961k_1 + j0.271k_1 + 0.189k_2 + j0.053k_2$
0.8	$0.950k_1 + j0.309k_1 + 0.214k_2 + j0.069k_2$
0.9	$0.937k_1 + j0.346k_1 + 0.237k_2 + j0.088k_2$
1.0	$0.922k_1 + j0.382k_1 + 0.260k_2 + j0.104k_2$

As an example, the complex coefficients k_{c0} , k_{c1} and k_{c2} of the second-order CT-QBP $\Sigma\Delta$ M with parameters of $a_1 = a_2 = 9e6$, $b_1 = 0.04$, $f_s = 32$ MHz, $f_c = 2$ MHz and $f_B = 1$ MHz, were calculated by using the symbolic math program Maple. The calculated results are shown in Table 5.1, 5.2 and 5.3 as a function of excess loop delay τ_d .

The compensation scheme which satisfy Table 5.1, 5.2 and 5.3 must implement many switches, and it is practically impossible to realize a full schematic for compensation of excess loop delay because of complexity. An approximation can be applied to Table 5.1, 5.2 and 5.3, provided that the spread of feedforward coefficients in Figure 5.15 is not very high (this is possible by using integrator scale value). Note that for an optimized zero placement in the $NTF_{QBP}(z)$, the CT integrator gains are scaled and therefore the spread of feedforward coefficients is low. From Table 5.1, it can be seen that the complex feedback coefficient k_{c0} has a higher dependency on k_1 than other factors. Therefore k_2 and the complex terms jk_1 and jk_2 can be ignored. In Table 5.1

Table 5.3.: The feedforward coefficient k_{c2} vs. τ_d

τ_d	k_{c2}
0.1	$-0.001k_1 - j0.000k_1 + 0.999k_2 + j0.039k_2$
0.2	$-0.002k_1 - j0.000k_1 + 0.996k_2 + j0.078k_2$
0.3	$-0.003k_1 - j0.000k_1 + 0.993k_2 + j0.117k_2$
0.4	$-0.004k_1 - j0.000k_1 + 0.987k_2 + j0.156k_2$
0.5	$-0.006k_1 - j0.001k_1 + 0.980k_2 + j0.195k_2$
0.6	$-0.007k_1 - j0.002k_1 + 0.972k_2 + j0.233k_2$
0.7	$-0.008k_1 - j0.002k_1 + 0.961k_2 + j0.271k_2$
0.8	$-0.009k_1 - j0.003k_1 + 0.950k_2 + j0.309k_2$
0.9	$-0.009k_1 - j0.004k_1 + 0.937k_2 + j0.346k_2$
1.0	$-0.010k_1 - j0.004k_1 + 0.922k_2 + j0.382k_2$

and 5.3, the dependence of k_{c1} on k_1 is identical to that of k_{c2} on k_2 . Therefore, the dependency of k_{c1} on k_{c2} and k_{c2} on k_{c1} can be neglected, too.

In Table 5.1, 5.2 and 5.3, the spread of real and image terms in complex coefficients depends on an original placement of poles in the $NTF(z)_{QBP}$ with excess loop delay (see Figure 5.18). The greater the change of placement of poles introduced by excess loop delay is, the greater is the spread of complex coefficients. After compensation, the original placement of poles in the $NTF(z)_{QBP}$ is nearly symmetric and the additional pole is close to the additional zero placed original point, and therefore is canceled each other.

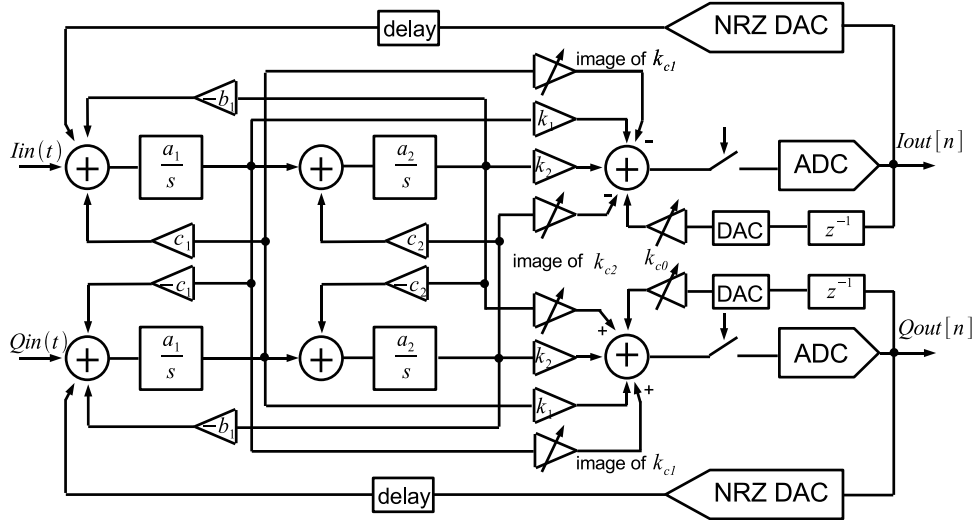
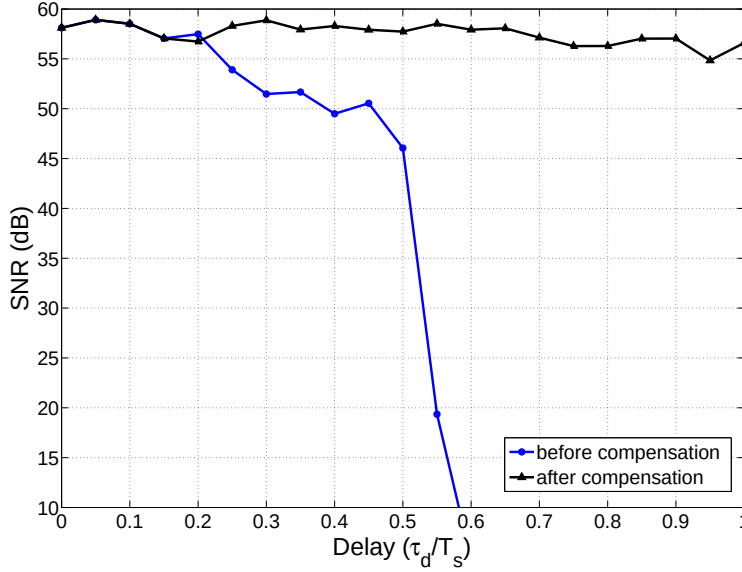


Figure 5.20.: The second-order CT-QBP $\Sigma\Delta M$ with compensation scheme of excess loop delay.

Table 5.4.: The approximated k_{c0} , k_{c1} and k_{c2} vs. τ_d

τ_d	k_{c0}	k_{c1}	k_{c2}
$(0.0 \sim 0.099)T_s$	$0.000k_1$	$k_1 + j0.000k_1$	$k_2 + j0.000k_2$
$(0.1 \sim 0.499)T_s$	$0.100k_1$	$k_1 + j0.150k_1$	$k_2 + j0.150k_2$
$(0.5 \sim 0.799)T_s$	$0.150k_1$	$k_1 + j0.300k_1$	$k_2 + j0.300k_2$
$(0.8 \sim 1.0)T_s$	$0.250k_1$	$k_1 + j0.400k_1$	$k_2 + j0.400k_2$

Finally, the compensation coefficients k_{c0} , k_{c1} and k_{c2} were approximately chosen as shown in Table 5.4. It implies that the compensation of the excess loop delay can be realized by a programmable 2-bit digital word. The full schematic based on the Table 5.4 is shown in Figure 5.20. The simulation results of SNR vs. τ_d/T_s are shown in Figure 5.21. Using a 2-bit digital word, excess loop delay can be handled up to one clock delay. Figure 5.22 show the output spectrum after compensation which is simulated with the approximated coefficients of Table 5.4.

Figure 5.21.: The SNR vs. τ_d/T_s when using the coefficients in Table 5.4.

From Figure 5.20, it can be seen that the feedforward complex coefficients for compensation of excess loop delay are implemented by using extra cross-couplings. This increases the circuit complexity. For a lower ratio of the center frequency to sampling clock, note that if the phase margin of the CT loop filter is large enough, the reduced SNR loss and the desirable stability margin of the modulator can be obtained without any compensation.

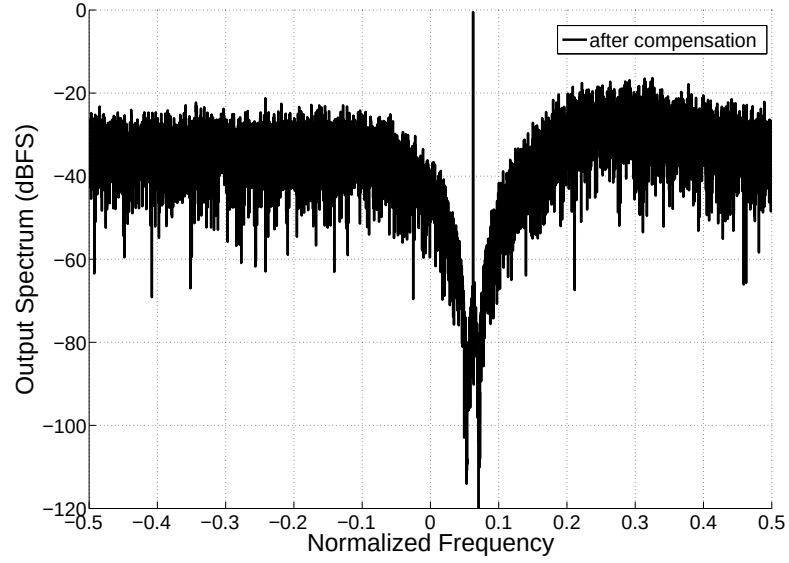


Figure 5.22.: The output spectrum when $\tau_d/T_s = 0.8$ and $f_c = 2MHz$.

5.3. Mismatched Loop Delay

CT-QBP $\Sigma\Delta$ Ms seriously suffer from delay in real and imaginary feedback paths. The mismatched loop delay between real (I) and imaginary (Q) paths reduces the performance of CT-QBP $\Sigma\Delta$ Ms, because they have the cross-couplings between I/Q paths inside CT loop filter.

As shown in the above section, for analytical considerations of excess loop delay which means a matched loop delay, a continuous-discrete transformation, the impulse-invariant transformation, was used as a continuous-discrete transformation, in [CS99b], [HL03]. Unfortunately, this transformation cannot be directly applied for consideration of mismatched loop delay in CT-QBP $\Sigma\Delta$ modulators.

In this section, the effect of mismatch loop delay is demonstrated in a second-order CT-QBP $\Sigma\Delta$ modulator [KWJ⁺08]. We obtain the equivalent discrete-time (DT) transfer functions through a continuous-discrete transformation in the complex signal domain, assuming nonzero delayed- and mismatched-feedback DAC pulses. In the last subsection, a solution for the compensation of its effect is proposed.

5.3.1. Effect of Mismatched Loop Delay

In this subsection, the effect of mismatched loop delay is demonstrated in a CT second-order complex $\Sigma\Delta$ modulator with feedforward topology. Figure 5.23 shows the feedforward second-order modulator with single-bit quantizer and NRZ DAC, which has different loop delay in the feedback I/Q paths, namely, $T_{d,I}$ and $T_{d,Q}$. The CT loop

filter transfer function is

$$H_0(s) = \frac{A_{01}}{s - j(w_c - w_0)} + \frac{A_{01}^*}{s - j(w_c + w_0)}, \quad (5.18)$$

where $w_0^2 = a_1 a_2 b_1$, $w_c = a_1 c_1 = a_2 c_2$ and $A_0 = 1/b_1$, and $A_{01} = 0.5w_0(k_1\sqrt{A_0} - jk_2A_0)$. A_{01}^* is conjugation of A_{01} .

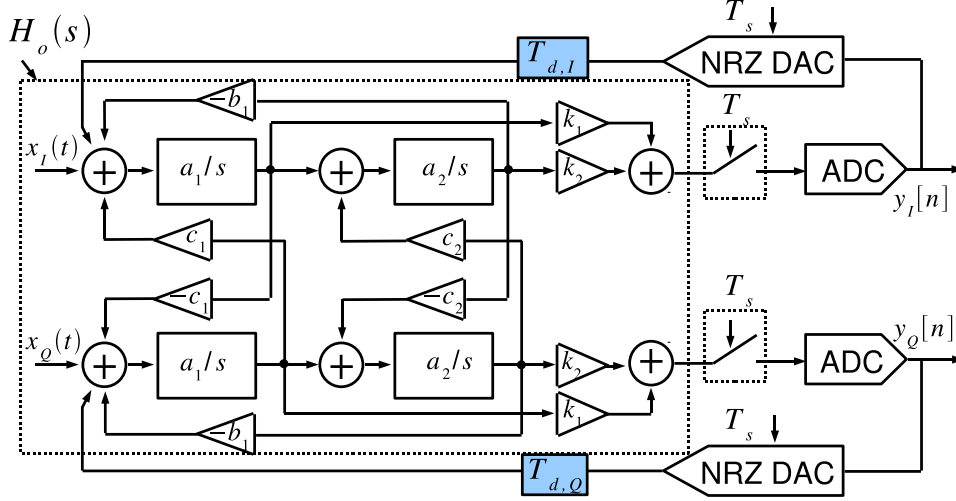


Figure 5.23.: CT second-order complex $\Sigma\Delta$ modulator with non-zero delayed and mismatched DAC pulses.

Figure 5.24 shows the output spectrum of the second-order CT-QBP $\Sigma\Delta$ M with non-zero delayed- and mismatched-feedback NRZ DAC pulses, which are simulated in Matlab simulink. As shown in top and middle of this figure, the degradation in SNR increases with non-zero delayed-feedback loop delay. For the mismatched feedback DAC pulse, as shown in middle and bottom of Figure 5.24, when $T_{d,I} = 0.4T_s$, $T_{d,Q} = 0.8T_s$, the degradation in SNR is increased much more than that of an even higher common loop delay. Also the image signal power in negative frequency appears. The parameters used in the simulation are $a_1 = a_2 = 9.0e6$, $b_1 = 0.04$, $k_1 = k_2 = 1$. The center frequency f_c , the bandwidth f_B , and the sampling frequency f_s of this modulator are 2 MHz, 1 MHz, and 64 MHz, respectively. The input level is -3 dBFS.

5.3.2. Continuous-Discrete Transformation

In general, the loop delay is caused by delay in the quantizer and DAC block. The delay in the quantizer which is called signal dependent delay, depends on the decision time of the comparators and typically increases for small input levels [CS99a]. For CT-QBP $\Sigma\Delta$ Ms, there are two quantizers in I/Q paths and their signal dependent

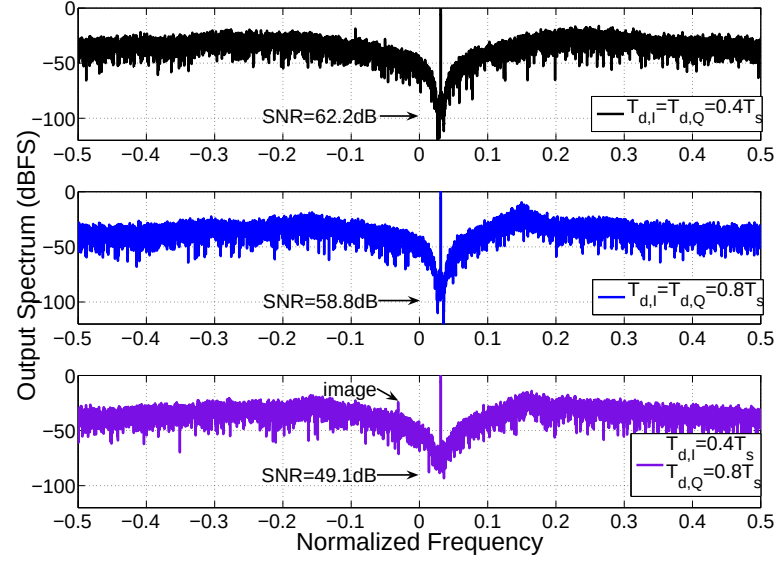


Figure 5.24.: Output spectrum of modulator with nonzero delayed- and mismatched-feedback NRZ DAC pulses.

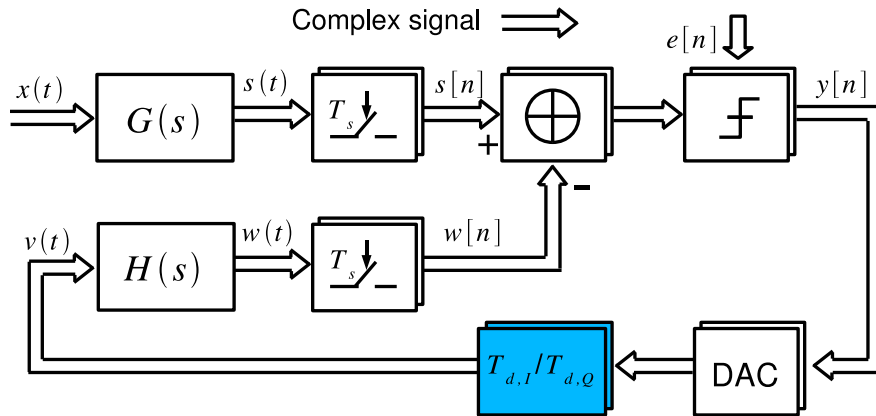


Figure 5.25.: CT-QBP $\Sigma\Delta$ M with mismatched loop delay.

delay typically differs in both paths, due to the different signal at the inputs of two quantizers.

The block diagram of a CT-QBP $\Sigma\Delta$ M with mismatched loop delay is shown in Figure 5.25, where a CT complex modulator can be linearized by two parts-such as feedforward signal path and feedback path for the noise shaping. Also, note that all signals and blocks are divided into real and imaginary parts.

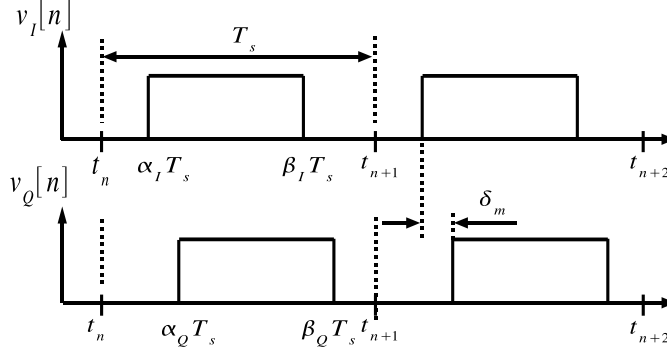


Figure 5.26.: DAC pulses in real and imaginary paths.

As shown in Figure 5.26, the nonzero delayed- and mismatched-feedback DAC pulses can be modeled by the parameters α_I , β_I , α_Q , and β_Q in CT-QBP $\Sigma\Delta$ M. In order to clarify, we use two terms -one is a *common loop delay* (τ_d) which is the lower delay value of both paths (note that the common loop delay is the same as excess loop delay in the above section), the other is a *mismatched loop delay* (δ_m) which is the difference between both paths. With return-to-zero (RZ) feedback DAC pulses which are defined as $(\alpha_I, \beta_I) = (\alpha_Q, \beta_Q) = (0, 0.5)$ (ideal case) in both paths, $\tau_d = \alpha_I$ and $\delta_m = \alpha_Q - \alpha_I$.

From Figure 5.25 and 5.26, using a unit step function $u(t)$, the outputs of the nonzero delayed- and mismatched-feedback DAC analog pulses, are denoted as follows:

$$\begin{aligned} v(t) &= v_I(t) + jv_Q(t), \\ v_I(t) &= \sum_{k=-\infty}^{\infty} y_I[k][u(t - kT_s - \alpha_I T_s) - u(t - kT_s - \beta_I T_s)], \\ v_Q(t) &= \sum_{k=-\infty}^{\infty} y_Q[k][u(t - kT_s - \alpha_Q T_s) - u(t - kT_s - \beta_Q T_s)]. \end{aligned} \quad (5.19)$$

The CT-complex loop filter $H(s)$ can be denoted by a partial-fraction expansion, that is,

$$H(s) = \sum_{k=1}^L \frac{c_k}{s - s_k}, \quad (5.20)$$

where L is the order of the loop filter and c_k is a complex constant. In order to simplify, it is assumed that the complex loop filter has first order poles only which are placed around the center frequency, and the order of the numerator of $H(s)$ does not exceed the order of the denominator (note when an optimized zero placement for minimizing in-band noise power, all poles of $H(s)$ are first order).

In the feedback paths, the output $w(t)$ of the CT complex filter $H(s)$, is the convolution of $v(t)$ and an impulse response $h(t)$ of $H(s)$, that is,

$$w(t) = w_I(t) + jw_Q(t) = h(t) * v(t) \quad (5.21)$$

The impulse response $h(t)$ and the step response $h_u(t)$ of $H(s)$ can be denoted, respectively, as follows:

$$\begin{aligned} h(t) &= h_I(t) + j \cdot h_Q(t), \\ h_u(t) &= h_{u,I}(t) + j \cdot h_{u,Q}(t). \end{aligned} \quad (5.22)$$

For the sake of a simple description, the following functions are defined in our analysis.

$$\begin{aligned} h_{u,I,I}(t) &= h_{u,I}(t - kT_s - \alpha_I T_s) - h_{u,I}(t - kT_s - \beta_I T_s), \\ h_{u,Q,Q}(t) &= h_{u,Q}(t - kT_s - \alpha_Q T_s) - h_{u,Q}(t - kT_s - \beta_Q T_s), \\ h_{u,I,Q}(t) &= h_{u,I}(t - kT_s - \alpha_Q T_s) - h_{u,I}(t - kT_s - \beta_Q T_s), \\ h_{u,Q,I}(t) &= h_{u,Q}(t - kT_s - \alpha_I T_s) - h_{u,Q}(t - kT_s - \beta_I T_s). \end{aligned} \quad (5.23)$$

Then, $w(t)$ is

$$\begin{aligned} w_I(t) &= \sum_{k=-\infty}^{\infty} \{y_I[k]h_{u,I,I}(t) - y_Q[k]h_{u,Q,Q}(t)\}, \\ w_Q(t) &= \sum_{k=-\infty}^{\infty} \{y_Q[k]h_{u,I,Q}(t) + y_I[k]h_{u,Q,I}(t)\}. \end{aligned} \quad (5.24)$$

After the sampling process, $w(t)$ is defined in the DT domain, that is,

$$\begin{aligned} w_I(n) &= y_I[n] * h_{u,I,I}(nT_s; \alpha_I, \beta_I) - y_Q[n] * h_{u,Q,Q}(nT_s; \alpha_Q, \beta_Q), \\ w_Q(n) &= y_Q[n] * h_{u,I,Q}(nT_s; \alpha_Q, \beta_Q) + y_I[n] * h_{u,Q,I}(nT_s; \alpha_I, \beta_I). \end{aligned} \quad (5.25)$$

The z-transformation $W(z)$ of $w(n)$

$$\begin{aligned} W(z) &= H_{u,I,I}(z; \alpha_I, \beta_I)Y_I[z] - H_{u,Q,Q}(z; \alpha_Q, \beta_Q)Y_Q[z] + \\ &+ j \cdot (H_{u,I,Q}(z; \alpha_Q, \beta_Q)Y_Q[z] + H_{u,Q,I}(z; \alpha_I, \beta_I)Y_I[z]). \end{aligned} \quad (5.26)$$

Figure 5.27 shows the DT equivalent scheme with the mismatched loop delay. For the

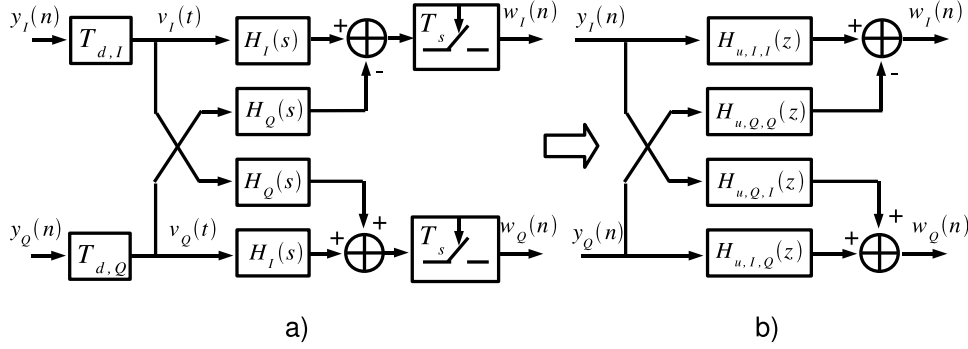


Figure 5.27.: Mismatched feedback paths (a) in CT-domain, (b) equivalent in DT-domain.

mismatched loop delay, $H_{u,I,I}(z; \alpha_I, \beta_I) \neq H_{u,I,Q}(z; \alpha_Q, \beta_Q)$ and $H_{u,Q,Q}(z; \alpha_Q, \beta_Q) \neq H_{u,Q,I}(z; \alpha_I, \beta_I)$. This implies that DT equivalent by the mismatched loop delay is denoted by an identical form like the DT complex filter with the mismatched components in I/Q paths [YS99].

Next, when the CT-complex loop filter $H(s)$ is defined as Equation (5.20), its impulse response is derived through inverse Laplace transformation.

$$\begin{aligned} h_I(t) &= \sum_{k=1}^L 0.5(c_k e^{s_k t} + c_k^* e^{s_k^* t})u(t), \\ j \cdot h_Q(t) &= \sum_{k=1}^L 0.5(c_k e^{s_k t} - c_k^* e^{s_k^* t})u(t). \end{aligned} \quad (5.27)$$

In the above expressions, $\{()\}^*$ denotes the conjugation operator. Considering the relation between step and impulse response- $dh_{u,I}(t)/dt = h_I(t)$, $dh_{u,Q}(t)/dt = h_Q(t)$, and using the derived results in [Gar86], the output which is processed through the CT complex loop filter and the sampler can be denoted in z -domain as follows:

$$W(z) = H_N(z) \cdot Y(z) + H_M(z)Y^*(z), \quad (5.28)$$

where $Y(z) = Y_I(z) + jY_Q(z)$ and

$$H_N(z) = \sum_{k=1}^L \frac{D_{N,k}}{z - z_k}, \quad (5.29)$$

$$H_M(z) = \sum_{k=1}^L \frac{D_{M,k}}{z - z_k}, \quad (5.30)$$

$$D_{N,k} = \frac{c_k}{2s_k} [(z_k^{1-\alpha_I} - z_k^{1-\beta_I}) + (z_k^{1-\alpha_Q} - z_k^{1-\beta_Q})], \quad (5.31)$$

$$D_{M,k} = \frac{c_k}{2s_k} [(z_k^{1-\alpha_I} - z_k^{1-\beta_I}) - (z_k^{1-\alpha_Q} - z_k^{1-\beta_Q})], \quad (5.32)$$

and $z_k = e^{s_k T_s}$, and $Y^*(z)$ is complex conjugation of $Y(z)$.

From the above equations, the DT-equivalent of the CT-complex loop filter due to the nonzero delayed- and mismatched-feedback DAC pulses, is described by two DT-loop filters $H_N(z)$ and $H_M(z)$. Figure 5.28 shows the DT-block diagram including the effects of mismatched loop delay as well as common loop delay. The *loop0* corresponds to DT-loop filter $H_N(z)$ which has α_I , α_Q , β_I and β_Q as parameters and $Y(z)$ as input. It can be seen the *loop0* is a main feedback path for noise shaping. But, the *loop1* is an additional feedback path, introduced by mismatched loop delay. The DT-loop filter, $H_M(z)$ has also α_I , α_Q , β_I and β_Q as parameters but $Y^*(z)$ as input. It can also be seen that when $\alpha_I = \alpha_Q$ and $\beta_I = \beta_Q$, $H_M(z)$ is the same as zero and $H_N(z)$ is identical to the results in above section where they described the DT-equivalent with common loop delay.

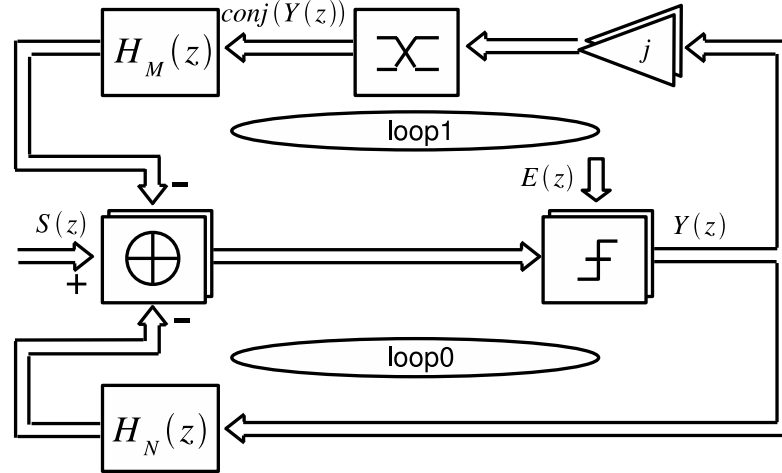


Figure 5.28.: DT-equivalent of CT-complex $\Sigma\Delta$ modulator with nonzero-delayed and mismatched DAC pulses.

The conjugation operator in Equation (5.28) is divided into two parts; one is a multiplication of a complex signal $Y(z)$ with complex constant j , the other is an exchange, which is equal to swapping the sequence of vector components of the complex signal between real and imaginary parts, as shown in Figure 5.28. Note that the first operator preserves the frequency distribution, while swapping is not a linear operator and does not preserve the frequency distribution[CS98b]. Therefore, the relation of $Y(z)$ and $Y^*(z)$ is not linear and the *loop0* and *loop1* are also not linearized feedback loops of each other, as if the two loops of Figure 5.28 were entirely independent.

From Equations (5.28)-(5.32), the ideal DT-equivalent transfer functions of loop filters with the different feedback DAC pulses such as RZ, HRZ and NRZ can be obtained. When $\alpha = \alpha_I = \alpha_Q$, $\beta = \beta_I = \beta_Q$, the DT-equivalent transfer function of CT-complex loop filter is

$$\hat{H}_N(z) = \sum_{k=1}^L \frac{c_k(z_k^{1-\alpha} - z_k^{1-\beta})}{s_k(z - z_k)}, \quad (5.33)$$

and $\hat{H}_M(z) = 0$. Therefore, for NRZ feedback DAC pulse which means that $\alpha = 0$, $\beta = 1$, the DT-transfer function is

$$H_{NRZ}(z) = \sum_{k=1}^L \frac{c_k(z_k - 1)}{s_k(z - z_k)}. \quad (5.34)$$

Note that for the ideal case, the DT equivalent transfer function has the poles and zeros centered around $e^{j\omega_c T_s}$ in z -domain.

We can also calculate the DT equivalent transfer functions, $H_N(z)$ and $H_M(z)$ with nonzero delayed- and mismatched-NRZ DAC pulses in real and imaginary paths. If delay in both paths are $T_{d,I} = \tau_d T_s$ and $T_{d,Q} = (\tau_d + \delta_m) T_s$, respectively, NRZ DAC pulses are denoted as

$$\begin{aligned} DAC_{I,(\tau_d,1+\tau_d)}(t) &= DAC_{I,(\tau_d,1)}(t) + DAC_{I,(0,\tau_d)}(t - T_s), \\ DAC_{Q,(\tau_d+\delta_m,1+\tau_d+\delta_m)}(t) &= DAC_{Q,(\tau_d+\delta_m,1)}(t) + DAC_{Q,(0,\tau_d+\delta_m)}(t - T_s). \end{aligned} \quad (5.35)$$

Therefore its DT-transfer functions of loop filter can be obtained as follows:

$$\begin{aligned} H_{N,NRZ} &= H_N(z)|_{(\alpha_I,\beta_I)=(\tau_d,1),(\alpha_Q,\beta_Q)=(\tau_d+\delta_m,1)} + \\ &+ z^{-1} H_N(z)|_{(\alpha_I,\beta_I)=(0,\tau_d),(\alpha_Q,\beta_Q)=(0,\tau_d+\delta_m)}. \end{aligned} \quad (5.36)$$

$$\begin{aligned} H_{M,NRZ} &= H_M(z)|_{(\alpha_I,\beta_I)=(\tau_d,1),(\alpha_Q,\beta_Q)=(\tau_d+\delta_m,1)} + \\ &+ z^{-1} H_M(z)|_{(\alpha_I,\beta_I)=(0,\tau_d),(\alpha_Q,\beta_Q)=(0,\tau_d+\delta_m)}. \end{aligned} \quad (5.37)$$

Here the term of z^{-1} is introduced by one-sample delayed feedback pulses. Note that in the above two equations, the mismatch in the first term is one in rise time ($\alpha_I \neq \alpha_Q$) and the mismatch in the second term with z^{-1} is one in fall time ($\beta_I \neq \beta_Q$). For mismatched NRZ feedback DAC pulse, it can be seen that two DT-equivalent loop filters have an additional pole in a DC point of the z -domain as well as the poles around $e^{j\omega_c T_s}$. Above analytical procedure can be applied to any topology with RZ and HRZ as well as NRZ DAC pulse.

On the other hand, the input signal is processed by the complex filter $G(s)$ in the feedforward path of Figure 5.25 and its output is defined in DT-domain after the

sampling process. Defining z-transformation of its output $s[n]$ as $S(z)$, the modulator output is obtained as follows:

$$Y(z) = \frac{S(z) + E(z) - H_M(z)Y^*(z)}{1 + H_N(z)}. \quad (5.38)$$

Now we can define the DT-equivalents, such as the noise shaping transfer function (NTF) and the mismatch transfer function (MTF). DT-equivalent transfer functions are

$$NTF(z) = \frac{1}{1 + H_N(z)}, \quad (5.39)$$

$$MTF(z) = \frac{H_M(z)}{1 + H_N(z)}. \quad (5.40)$$

The mismatch transfer function MTF seriously affects the performance of CT-complex $\Sigma\Delta$ modulators. Figure 5.29 shows an amplitude response of NTF and MTF derived from nonzero delayed- and mismatched-feedback NRZ DAC pulses in real and imaginary paths, when $T_{d,I} = 0.4T_s$, $T_{d,Q} = 0.8T_s$. The used parameters are identical to that of second-order CT complex $\Sigma\Delta$ modulator in Figure 5.23 and 5.24.

From Figure 5.29, it can be seen that the MTF makes an increment of the level of in-band noise, because the negative band noise which is shaped by the NTF is again aliased to the positive passband due to the frequency mirroring of the conjugated output $Y^*(z)$. Moreover it can also be shown, that the input signal power is aliased to the negative frequency band as illustrated in Figure 5.29. Therefore, the degradation in SNR increases with mismatched loop delay.

5.3.3. Compensation of Mismatched Loop Delay

As shown above, the degradation in SNR with relation to loop delay is due to the mismatched loop delay δ_m and the common loop delay τ_d . Our task is to find a solution to reduce or compensate the effect of mismatched loop delay, δ_m .

5.3.3.1. Ratio of Center Frequency to Sampling Frequency

For the DT transfer functions, NTF and MTF with nonzero delayed- and mismatched-NRZ DAC pulses, their amplitudes in passband as well as the placement of their poles and zeros depend on the ratio of the center frequency f_c to the sampling frequency f_s as shown in Figure 5.30. When the ratio of f_c to f_s increases, it can be seen that the amplitude of MTF in the positive passband is increased. Therefore the aliased noise into the positive passband by MTF is increased. This implies that for a low ratio of f_c to f_s , the degradation in SNR by the mismatched loop delay is reduced.

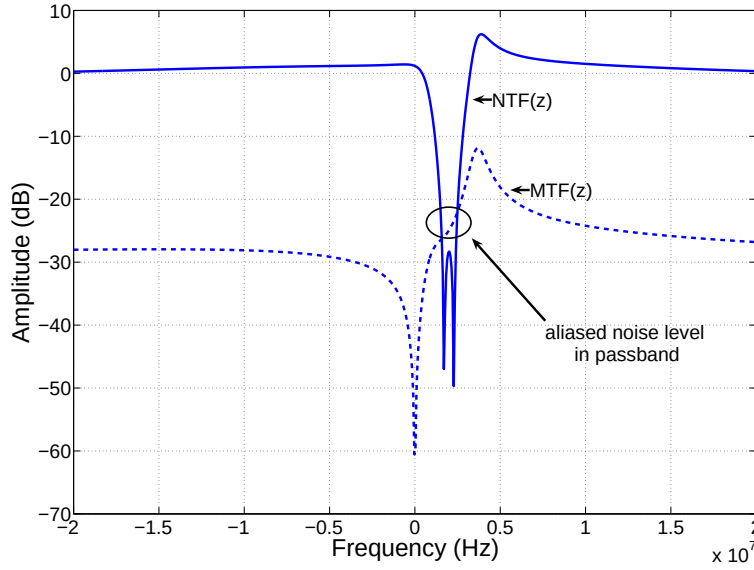


Figure 5.29.: Amplitude response of second-order NTF and MTF, when $T_{d,I} = 0.4T_s$, $T_{d,Q} = 0.8T_s$ and $f_s = 64MHz$.

Figure 5.31 shows the degradation of SNR versus the mismatched loop delay at different common loop delays (for example, $\tau_d = 0$ and $\tau_d = 0.4T_s$) and center frequencies. It can be shown that for lower center frequency, the effect of mismatched loop delay is greatly decreased.

Otherwise, for higher f_c , the obtained NTF has asymmetric placement of poles and zeros, even though $\tau_d = 0$, $\delta_m = 0$. That is why the feedback DAC pulses are still around DC. Therefore, if f_c is relatively lower and/or a new cross-coupling in order to move the feedback DAC pulse to the center frequency is inserted for feedback DAC pulse [RDMRW05], they can provide better results.

5.3.3.2. Compensation Method

Usually, the mismatched feedback DAC pulses are caused by signal dependent delays [CS99a] in the quantizers of real and imaginary paths. As shown in section III, the mismatched loop delay between I/Q paths produces an unwanted MTF through a combination of the cross-couplings and, therefore, reduces the performance of the complex $\Sigma\Delta$ modulator.

In order to compensate the effect of the mismatch loop delay, two steps are necessary; (1) matching the loop delay in the two feedback paths, (2) compensating the matched common loop delay. The use of D-latches following the quantizers in the feedback paths is an effective solution for matching the loop delay. If the signal dependent delay of the

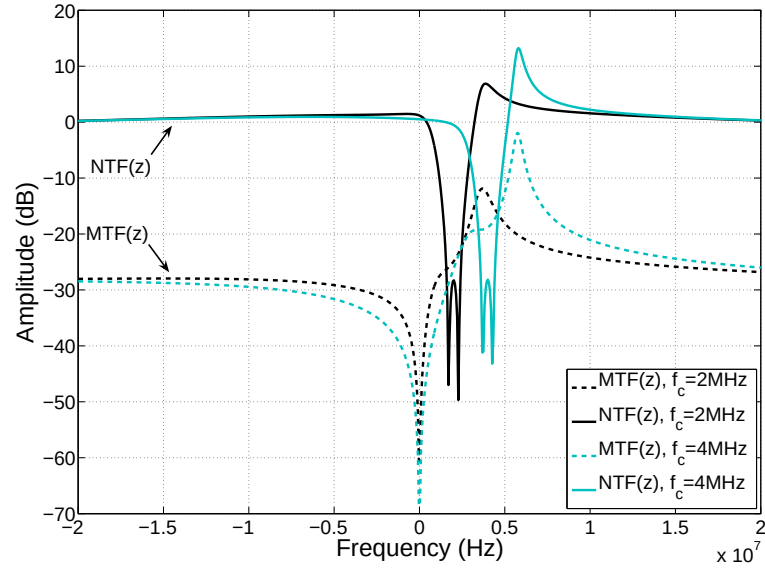


Figure 5.30.: Amplitude response in different center frequencies when $f_s = 64\text{MHz}$.

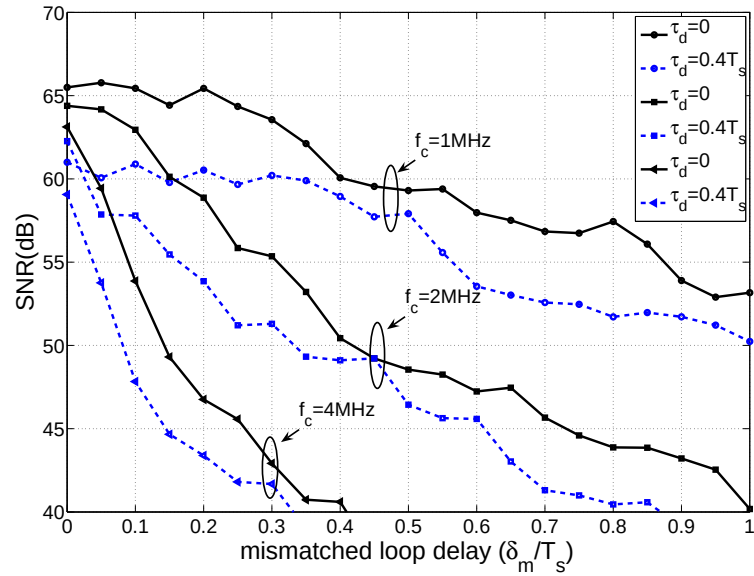


Figure 5.31.: The degradation of SNR vs. mismatched loop delay, in different center frequencies when $f_s = 64\text{MHz}$.

quantizers in both paths is less than a full sampling period, an insertion of D-latches, working at the sampling rate in real and imaginary paths, is desirable. Then, the total loop delay in both paths can be nearly the same as a full sampling period T_s with no relation to the signal dependent delay and therefore the mismatch in the loop delay can be ignored. Here, the delay in DACs for analog step pulse generation was ignored, because it generally depends on the DAC sampling clock and the delay in the feedback DAC is lower than that of quantizers.

By use of D-latches in the feedback paths, though the mismatched loop delay $\delta_m = 0$, the effect of common loop delay still remains ($\tau_d = T_s$) and needs to be compensated. In order to compensate this common loop delay, the compensation scheme in the above section can be used. Therefore, when D-latches and the compensation scheme for the common loop delay are used for the modulator design, the degradation in SNR by mismatched loop delay can be improved. Using a compensation scheme of the common loop delay and D-latches, can provide an ideal SNR of 67.4 dB for a second order CT complex $\Sigma\Delta$ modulator as shown in Figure 5.23.

In this section, the equivalent DT transfer functions with mismatched loop delay was derived from continuous-discrete transformation in the complex signal domain. The analytical results can be applied to consideration of mismatched loop delay, as well as common loop delay (excess loop delay). The mismatched loop delay severely results in a degradation of the SNR. Therefore, the techniques for either reducing or compensating the mismatch in loop delay should be proposed. To reduce the effect of mismatched loop delay in I/Q paths, it is desirable to select a low center frequency compared to the sampling clock. By a combination of D-latches in the feedback paths and the compensation scheme for common loop delay, the effect of mismatched loop delay can be compensated.

5.4. Clock Jitter

In this section, the clock jitter effect on the signal-to-noise ratio in CT-QBP $\Sigma\Delta$ Ms is presented. The clock jitter is a statistical variation of sampling clock, which depends on clock source and chip design. The noise introduced by clock jitter increases the in-band noise power and, therefore, decreases the SNR [OGM03b],[OA98].

The effect of the clock jitter in CT lowpass and real bandpass $\Sigma\Delta$ modulators has been theoretically studied in [OGM06], [Oli03], [Oli01], and [TTK99]. These papers were based on statistical consideration of the clock uncertainties in CT modulators with RZ and NRZ feedback DAC pulses. Most analytical results are applied to CT lowpass and bandpass $\Sigma\Delta$ modulators. For minimal performance degradation by clock jitter, the approaches of an optimized transfer function for reduced jitter effect were presented in [HWPDG04], [RP06]. The methods based on a pulse-shaped cosine feedback DAC [LL02], a SCR DAC [OGM05b], a spectra shaping of clock jitter [HPW06], and a compensation with extra feedback DAC [DvRL02] can also effectively improve

the SNR degradation in the CT lowpass modulators.

In this section, we address the clock jitter effect in CT-QBP $\Sigma\Delta$ Ms with NRZ DAC pulse. This is an extension of [TTK99] to complex signal domain. The closed-form formulas for the output spectrum of noise caused by clock jitter are derived. The derived SNR formula in CT complex $\Sigma\Delta$ modulator is similar to the result in CT lowpass counterparts[CS99a].

5.4.1. Clock Jitter in CT-QBP $\Sigma\Delta$ M

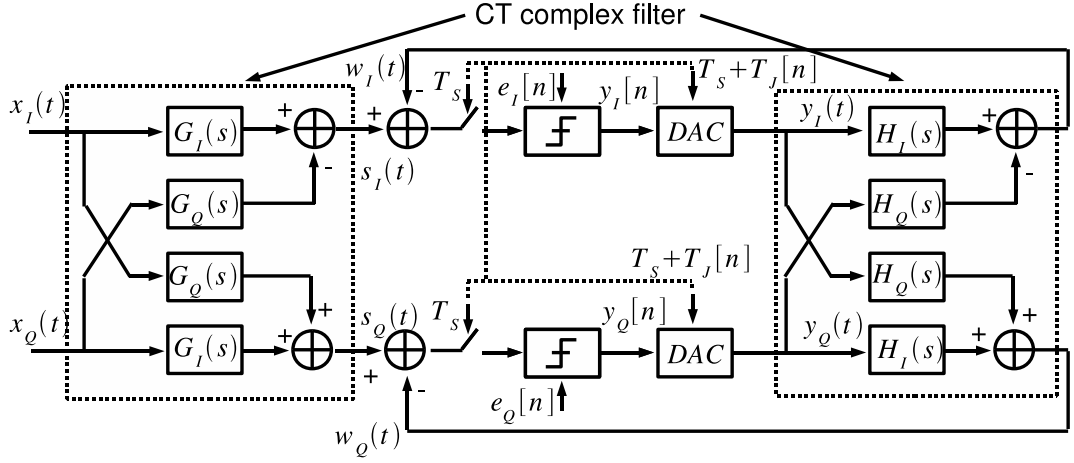


Figure 5.32.: CT-QBP $\Sigma\Delta$ M with clock jitter.

Generally, there are two blocks which require a precise clock signal; the sampler before quantizer and the DAC that generates the feedback pulse. For an ideal case, the sampler and DAC operate with identical and undisturbed sampling clock. Due to several reasons, the clock edge at each instant in sampler and DAC is deviated from exact clock edge.

The clock uncertainties in sampler are generally ignored because the error caused by a sampling clock jitter is shaped by the modulator at maximum noise superpress point. Hence, in our analysis, the effect of clock jitter in feedback DACs with NRZ pulse will be considered.

The equivalent block diagram of a CT-QBP $\Sigma\Delta$ M with clock jitter at the feedback DACs is shown in Figure 5.32 where the complex loop filter $H(s)$ is replicated for the analytical consideration in DT-domain. All signals and blocks are divided into real and image channels.

For jitter free, the identical clock is applied to DACs in real and image channels and

the outputs of DACs are denoted by unity step function for DAC NRZ pulses.

$$\begin{aligned}
 v(t) &= v_I(t) + jv_Q(t), \\
 v_{I,0}(t) &= \sum_{k=-\infty}^{\infty} (y_I[k] - y_I[k-1]) \cdot u(t - kT_s), \\
 v_{Q,0}(t) &= \sum_{k=-\infty}^{\infty} (y_Q[k] - y_Q[k-1]) \cdot u(t - kT_s),
 \end{aligned} \tag{5.41}$$

where $y_I[k]$ and $y_Q[k]$ are k -th outputs in real and imaginary paths. In general, there are two kinds of clock jitter such as a pulse-delay jitter and a pulse-width jitter. For NRZ pulses, both of these are considered at a start of every clock corresponding to the pulse-delay jitter, because the uncertainty at an end corresponding to the pulse-width jitter is also for start of next clock. Therefore the clock uncertainties are inserted into above equation as follows:

$$\begin{aligned}
 v_I(t) &= \sum_{k=-\infty}^{\infty} (y_I[k] - y_I[k-1]) \cdot u(t - kT_s + T_J[k]), \\
 v_Q(t) &= \sum_{k=-\infty}^{\infty} (y_Q[k] - y_Q[k-1]) \cdot u(t - kT_s + T_J[k]),
 \end{aligned} \tag{5.42}$$

where $T_J[k]$ is a clock uncertainty in the feedback DACs which has a statistic distribution. The output of complex filter $H(s)$, $w(t)$ is the convolution of $v(t)$ and an impulse response of complex filter, $h(t)$. The impulse response $h(t)$ and the step response $h_u(t)$ of the complex filter are identical to Equation 5.22 in complex domain. Therefore we get

$$\begin{aligned}
 w(t) &= \sum_{k=-\infty}^{\infty} \{ \Delta y_I[k] \cdot h_{u,I}(t - kT_s + T_J[k]) - \Delta y_Q[k] \cdot h_{u,Q}(t - kT_s + T_J[k]) \} \\
 &+ j \cdot \sum_{k=-\infty}^{\infty} \{ \Delta y_I[k] \cdot h_{u,Q}(t - kT_s + T_J[k]) + \Delta y_Q[k] \cdot h_{u,I}(t - kT_s + T_J[k]) \}.
 \end{aligned} \tag{5.43}$$

Here,

$$\begin{aligned}
 \Delta y[k] &= \Delta y_I[k] + j\Delta y_Q[k], \\
 \Delta y_I[k] &= (y_I[k] - y_I[k-1]), \\
 \Delta y_Q[k] &= (y_Q[k] - y_Q[k-1]).
 \end{aligned} \tag{5.44}$$

Assuming that the clock uncertainty $T_J[k]$ is much smaller than the sampling period T_s , the step response in each channel, $h_{u,I}(t - kT_s + T_J[k])$, $h_{u,Q}(t - kT_s + T_J[k])$ can

be obtained approximately as a first-order Taylor series expanded around $t = t - kT_s$, as follows:

$$\begin{aligned} h_{u,I}(t - kT_s + T_J[k]) &\approx h_{u,I}(t - kT_s) + \frac{d}{dt}h_{u,I}|_{t=t-kT_s} \cdot T_J[k], \\ h_{u,Q}(t - kT_s + T_J[k]) &\approx h_{u,Q}(t - kT_s) + \frac{d}{dt}h_{u,Q}|_{t=t-kT_s} \cdot T_J[k]. \end{aligned} \quad (5.45)$$

For linear time invariant system, we can use the fact that $\frac{d}{dt}h_{u,I}(t) = h_I(t)$, $\frac{d}{dt}h_{u,Q}(t) = h_Q(t)$. The output of feedback, $w(t)$ can be expressed as linear approximation of clock uncertainty.

$$\begin{aligned} w(t) = & \sum_{k=-\infty}^{\infty} \{ \Delta y_I[k](h_{u,I}(t - kT_s) + h_I(t - kT_s)T_J[k]) - \\ & - \Delta y_Q[k](h_{u,Q}(t - kT_s) + h_Q(t - kT_s)T_J[k]) \} \\ & + j \cdot \sum_{k=-\infty}^{\infty} \{ \Delta y_I[k](h_{u,Q}(t - kT_s) + h_Q(t - kT_s)T_J[k]) + \\ & + \Delta y_Q[k](h_{u,I}(t - kT_s) + h_I(t - kT_s)T_J[k]) \}. \end{aligned} \quad (5.46)$$

After sampling process, it is defined in DT domain and denoted as

$$w(n) = \Delta y[n] * h_u(n) + \hat{y}[n] * h(n), \quad (5.47)$$

where

$$\hat{y}[n] = \Delta y[n] \cdot T_J[n]/T_s. \quad (5.48)$$

Expressing the z -transformation of $h(n)$ and $h_u(n)$ as $H(z)$ and $H_u(z)$, we represent them in complex domain.

$$W(z) = (1 - z^{-1})H_u(z)Y(z) + H(z)\hat{Y}(z). \quad (5.49)$$

Then, the output of the modulator is obtained from Figure 4.32 when the z -transformation of $S(n)$ is $S(z)$.

$$Y(z) = \frac{S(z) + E(z) - H(z)\hat{Y}(z)}{1 + (1 - z^{-1})H_u(z)}. \quad (5.50)$$

From the relationship of the step and the impulse response ($h(t) = dh_u(t)/dt$), the

step response in CT-domain is

$$H_u(s) = H(s) \cdot \frac{1}{s} \rightarrow h_u(t) = L^{-1}\{H_u(s)\}, \quad (5.51)$$

then, the step invariant response can be determined by sampling the continuous-time version:

$$h_u(nT_s) = h_u(t) \big|_{t=nT_s}. \quad (5.52)$$

Next, the DT transfer function to step input is derived from the z-transformation, as shown:

$$H_u(z) = Z\{h_u(nT_s)\} = H(z) \cdot \frac{1}{1 - z^{-1}}, \quad (5.53)$$

therefore, we get

$$H(z) = (1 - z^{-1})H_u(z). \quad (5.54)$$

The output of modulator is

$$Y(z) = \frac{S(z) + E(z) - H(z)\hat{Y}(z)}{1 + H(z)}. \quad (5.55)$$

The above equation implies that the error by clock jitter is directly added into the in-band output power spectrum with input signal and quantization error signal.

5.4.2. Power Spectral Density of Error Signal by Clock Jitter

For jitter free case ($T_J[n] = 0$), the output of modulator is

$$Y_0(z) = \frac{S(z) + E_0(z)}{1 + H(z)}. \quad (5.56)$$

Therefore an error signal introduced by clock jitter can be expressed as follows:

$$E_J(z) = Y(z) - Y_0(z) = \frac{(E(z) - E_0(z)) - H(z)\hat{Y}(z)}{1 + H(z)}. \quad (5.57)$$

Here, a term of $(E(z) - E_0(z))$ is ignored due to noise shaping at a maximum noise suppress point. Therefore, the error signal caused by clock jitter is

$$E_J(z) = \frac{-H(z)\hat{Y}(z)}{1 + H(z)} = H_J(z) \cdot \hat{Y}(z). \quad (5.58)$$

From the above equation, it can be seen that the error introduced by clock jitter is filtered by the transfer function, $H_J(z) = H(z)/(1 + H(z))$ which is similar to the input signal in the CIFF topology. Therefore the error signal by clock jitter is directly added to the in-band noise power.

The power spectrum density of error output due to the clock jitter is.

$$S_J(z) = |H_J(z)|^2 S_{\hat{Y}}(z). \quad (5.59)$$

In general, the power spectral density of a signal is obtained from the Fourier transformation of its autocorrelation function. We assume that the clock uncertainty have no correlation with the deviation of output signal $\Delta y[n]$ - statistically independent each other. Hence, the correlation function, $R_{\hat{Y}}[k]$ is

$$\begin{aligned} R_{\hat{Y}}[k] &= E\{\hat{y}^*[n]\hat{y}[n+k]\} \\ &= (1/T_s)^2 E\{\Delta y^*[n]\Delta y[n+k]\} E\{T_J[n]T_J[n+k]\}, \end{aligned} \quad (5.60)$$

where $E\{\cdot\}$ denotes the statistical average operator.

Now, we assume the clock uncertainty sequence $T_J[n]$ is a stationary DT white noise source with the Gaussian distribution and its variance is σ_J . The autocorrelation function of clock uncertainty sequence is

$$R_{T_J}[k] = E\{T_J[n]T_J[n+k]\} = \sigma_J^2 \cdot \delta[k]. \quad (5.61)$$

On the other hand, the autocorrelation of $\Delta y[n]$ is represented by the autocorrelations of the $\Delta y_I[n]$ and $\Delta y_Q[n]$ in the I/Q paths and their crosscorrelations, as shown:

$$E\{\Delta y^*[n]\Delta y[n+k]\} = R_{\Delta Y_I}[k] + R_{\Delta Y_Q}[k] + j(R_{\Delta Y_{I,Q}}[k] - R_{\Delta Y_{Q,I}}[k]), \quad (5.62)$$

where

$$\begin{aligned} R_{\Delta Y_I}[k] &= E\{\Delta y_I[n]\Delta y_I[n+k]\}, \\ R_{\Delta Y_Q}[k] &= E\{\Delta y_Q[n]\Delta y_Q[n+k]\}, \\ R_{\Delta Y_{I,Q}}[k] &= E\{\Delta y_I[n]\Delta y_Q[n+k]\}, \\ R_{\Delta Y_{Q,I}}[k] &= E\{\Delta y_Q[n]\Delta y_I[n+k]\}. \end{aligned}$$

The power spectrum of the $S_{\hat{Y}}(z)$ is identical to a result of the Fourier transform of autocorrelation $R_{\hat{Y}}[k]$, that is,

$$S_{\hat{Y}}(e^{j\omega T_s}) = \sum_{k=-\infty}^{\infty} R_{\hat{Y}}[k] e^{-j\omega k T_s}. \quad (5.63)$$

and is determined as follows:

$$S_{\hat{Y}}(e^{jwT_s}) = [R_{\Delta Y_I}[0] + R_{\Delta Y_Q}[0] + j(R_{\Delta Y_{I,Q}}[0] - R_{\Delta Y_{Q,I}}[0])] \cdot \left(\frac{\sigma_J}{T_s}\right)^2. \quad (5.64)$$

From the definition of the crosscorrelation function,

$$R_{\Delta Y_{I,Q}}[0] = R_{\Delta Y_{Q,I}}[0]. \quad (5.65)$$

The autocorrelations, $R_{\Delta Y_I}[0]$ and $R_{\Delta Y_Q}[0]$ define total powers of the deviation sequences $\Delta y_I[n]$ and $\Delta y_Q[n]$ at I/Q outputs of the CT-QBP $\Sigma\Delta M$.

$$P_{\Delta Y} = R_{\Delta Y_I}[0] + R_{\Delta Y_Q}[0] = P_{\Delta Y_I} + P_{\Delta Y_Q}. \quad (5.66)$$

The total jitter-induced noise of the modulator in the passband centered around w_c can be obtained as

$$P_J = \frac{1}{2\pi f_c} \cdot \int_{w_c-0.5w_B}^{w_c+0.5w_B} |H_J(e^{jwT_s})|^2 \cdot S_{\hat{Y}}(e^{jwT_s}) dw. \quad (5.67)$$

The transfer function $H_J(e^{jwT_s})$ is similar to the signal transfer function of the CIFF topology and the amplitude response in the passband is approximately unity. Therefore, the jitter-induced noise is

$$P_J = \frac{1}{OSR} \cdot \left(\frac{\sigma_J}{T_s}\right)^2 \cdot (P_{\Delta Y_I} + P_{\Delta Y_Q}). \quad (5.68)$$

From the above equation, it can be seen that the noise by clock jitter depends on the powers of the output deviation sequences of the modulator. The jitter-induced noise results in the increased noise power in the passband of the modulator.

5.4.3. SNR Estimation of CT-QBP $\Sigma\Delta M$

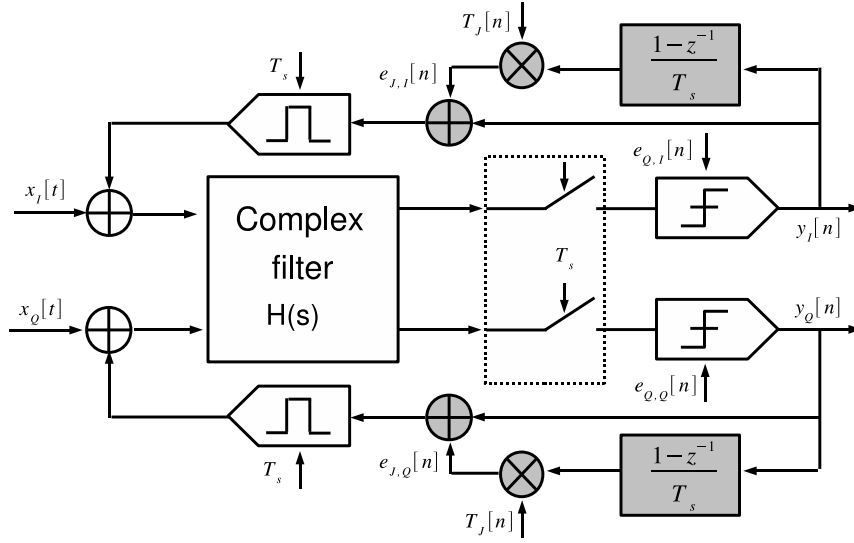
The simulation model is shown in Figure 5.33 which is an extension of the jitter-induced noise source model [HWPDG04] of the CT lowpass modulator to the CT-QBP $\Sigma\Delta M$.

Now we can calculate the SNR_J of the CT-QBP $\Sigma\Delta M$, due to the noise which is caused by clock jitter.

$$SNR_J = 10 \cdot \log_{10} \frac{P_S}{P_J} = 10 \cdot \log_{10} \frac{OSR \cdot V_{in}^2}{\left(\frac{\sigma_J}{T_s}\right)^2 \cdot (P_{\Delta Y_I} + P_{\Delta Y_Q})}, \quad (5.69)$$

where V_{in} is an amplitude of the input signal. The signal power in the CT-QBP $\Sigma\Delta M$ s is two times than that of the lowpass modulators, because the input signal is a complex signal.

The output noise of the modulator is basically caused by the quantization process


 Figure 5.33.: Simulation model of the CT-QBP $\Sigma\Delta$ M with clock jitter.

and clock jitter. When the quantization noise at the modulator output is P_Q , the SNR by two noise sources can be estimated as

$$SNR = 10 \cdot \log_{10} \frac{P_S}{P_Q + P_J}. \quad (5.70)$$

The effect of clock jitter was simulated by using the above model in the second-order CT-QBP $\Sigma\Delta$ M. As shown in Figure 5.34, it can be seen that when σ_J/T_s is lower, the SNR of the modulator is mainly determined by the quantization noise, otherwise, for a higher σ_J/T_s , it depends on the jitter-induced noise. The modulator parameters are $a_1 = a_2 = 9.0e6$, $b_1 = 0.04$ and the feedforward coefficients $k_1 = k_2 = 1$. The center frequency f_c , the bandwidth f_B , and the sampling frequency f_s are 2 MHz, 1 MHz and 64 MHz, respectively. The input signal level is -6 dBFS and the powers of $P_{\Delta Y_I}$ and $P_{\Delta Y_Q}$ are assumed as 2.

The deviation sequences $\Delta y_I[n]$ and $\Delta y_Q[n]$ which take the values of ± 2 and 0 for a single-bit modulator with ± 1 outputs. Their powers are proportional to $\Delta y^2 = (y[n] - y[n-1])^2 = 4$ and the number of bit transitions of quantizer outputs in I/Q paths are as follows [CS99a]:

$$P_{\Delta Y_I} \approx 4N_{\Delta Y_I}/N_t \quad P_{\Delta Y_Q} \approx 4N_{\Delta Y_Q}/N_t \quad (5.71)$$

The number of the transitions is related to the input signal and especially the modulator NTF_{QBP} design. The number of bit transitions in the I-path of the above second-order CT-QBP $\Sigma\Delta$ M is shown in Figure 5.35. In general, the lower the input signal level, the greater the number of bit transitions of quantizer outputs. But, when

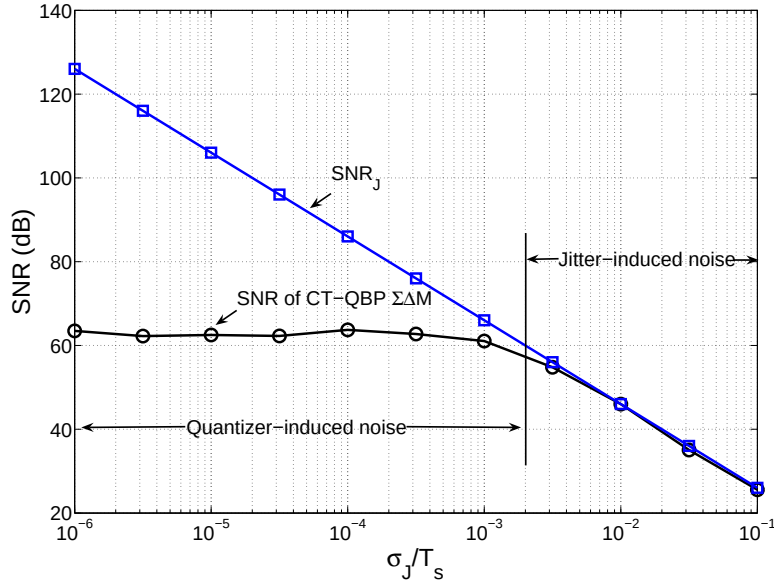


Figure 5.34.: SNR of the second-order CT-QBP $\Sigma\Delta M$ with the jitter-induced noise.

the input level is less than -40 dBFS, the number of bit transitions is nearly constant. Thus, when the input level is greater than -40 dBFS, the jitter-induced noise might result in a nonlinear error of the SNR if σ_J/T_s is greater than a critical value (for example, $\sigma_J/T_s = 2 \cdot 10^{-3}$ in the above second-order CT-QBP $\Sigma\Delta M$) as shown in Figure 5.36. It can be seen that the nonlinear error for $\sigma_J/T_s = 10^{-3}$ is relatively lower than that for $\sigma_J/T_s = 10^{-2}$.

The DT equivalent NTF_{QBP} also affects the number of the output bit transitions [HWPDG04], [RP06]. The number of the bit transitions can be reduced by an optimized NTF_{QBP} , which is carried out by adjusting the zero locations of the loop filter. In this case, a decrease of the area coefficient translates into a smaller power of the jitter-induced noise component and therefore, jitter-induced noise reduces [HWPDG04].

In order for reduced jitter sensitivity, the techniques which have been proposed for the CT lowpass modulators, such as in [OMG02], [OGM03a], [LL02] and [HPW06] can be extended to the design of the CT-QBP $\Sigma\Delta M$ s.

5.5. Nonlinearity of Multibit DAC

Multibit $\Sigma\Delta M$ s are well suited for high resolution because of lower quantizer noise and less sensitivity to feedback DAC clock uncertainties. The overall resolution of multibit modulators is determined by the internal digital-to-analog conversion linearity. The DAC bank contains unit DAC elements with identical weight (LSB) in ideal

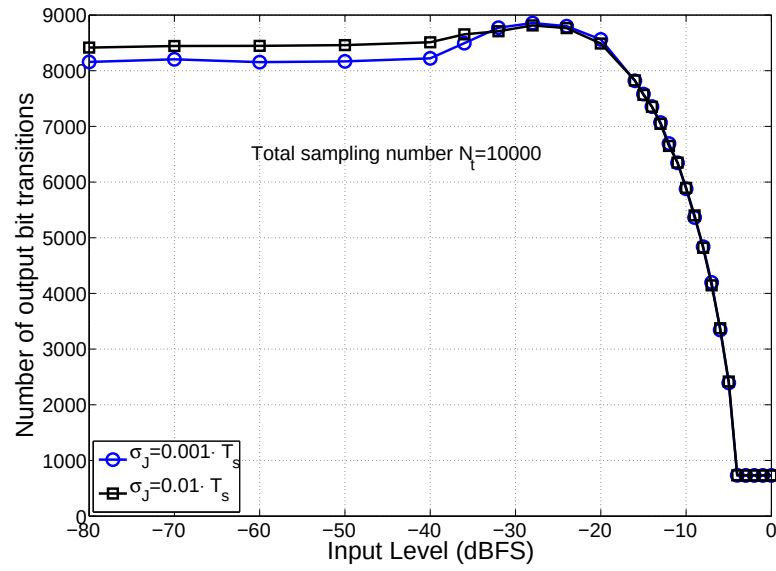


Figure 5.35.: The number of the output bit transitions vs. input level.

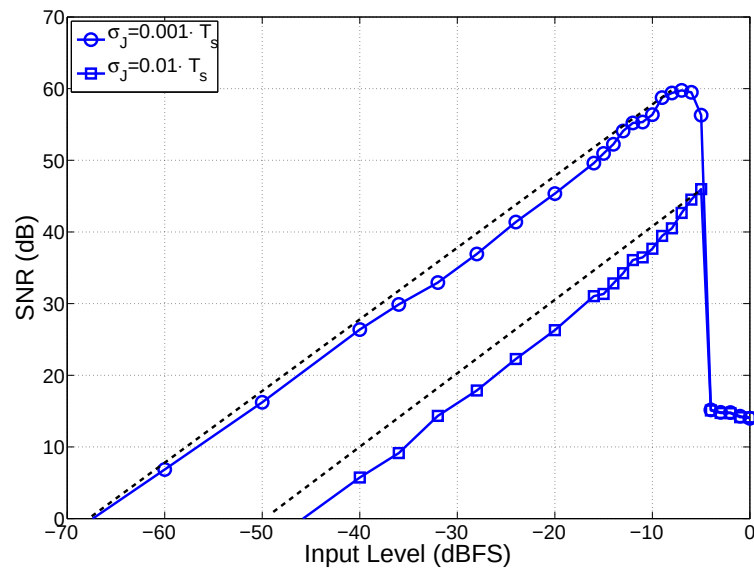


Figure 5.36.: The nonlinear error of the SNR vs. input level.

case. In practice, component mismatch is inevitably introduced during the chip processing. Any error in the feedback DACs is added to the input signal and increases the in-band noise level of the modulator output, and results in a degradation of SNR. In order to reduce the effects of the component mismatch in the DAC bank, the mismatch shaping technique which is based on a noise-shaping, becomes a desirable solution [Gal97], [SSH99], [SZ95]. The mismatch shaping architectures have been developed for the lowpass [FWG01], [HL07] and the real bandpass $\Sigma\Delta$ Ms [Vad04], [MP05]. In general, the first or second-order mismatch shaper is used for the multibit DAC nonlinear error due to its stability [WG02] and hardware complexity [WGF01], [JXC08].

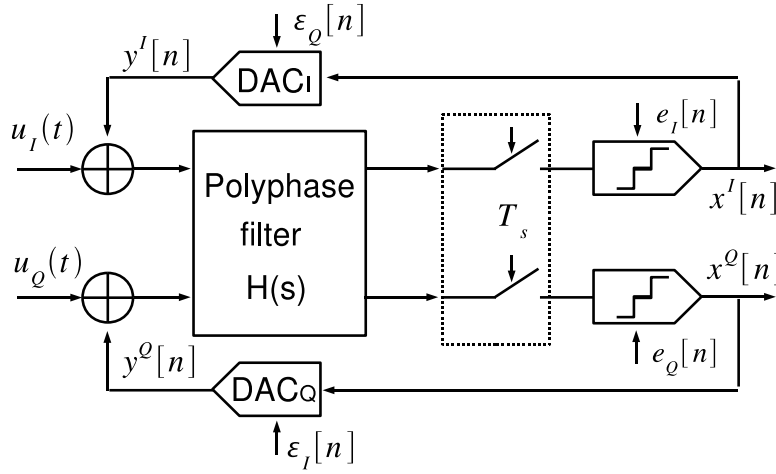


Figure 5.37.: Multibit complex $\Sigma\Delta$ modulator.

As shown in Figure 5.37, the QBP $\Sigma\Delta$ M has two DACs in the I/Q feedback paths. The errors, ε_I and ε_Q by mismatch in the feedback DACs increase the in-band noise-level of the QBP $\Sigma\Delta$ Ms [Sch02], [RCRW06a].

A complex DAC bank was proposed in [RDMRW06], [RCRW06b]. As shown Figure 5.38, two separate DAC banks in Figure 5.37 were merged into one complex DAC structure, which has a bank with $2N$ unit DAC elements. In the complex DAC, the input signal $x[n]$ is defined in the complex domain and its output, $x[i]$ is limited to $\{1, j\}$. When $x_i[n] = 1$, the unit DAC element is selected for I-path and generates a feedback signal to I-path. When $x_i[n] = j$, the unit DAC element is selected for Q-path and gives a feedback signal to Q-path and when $x_i[n] = 0$, the unit DAC element is unselected and generates no feedback. Therefore, it can be denoted as follows:

$$y_i[n] = \begin{cases} (1 + \varepsilon_i) & \text{if } x_i[n] = 1 \\ j(1 + \varepsilon_i) & \text{if } x_i[n] = j \\ 0 & \text{if } x_i[n] = 0 \end{cases} \quad (5.72)$$

where ε_i is the mismatch error of i -th DAC element.

In the complex DAC, the gain error introduced by mismatch between the I and Q-path is canceled[RDMRW06], because selection of the unit DAC elements is addressed in a merged common DAC bank with no relation to the I and Q-path.

$$y[n] = kx[n] + \varepsilon[n] \quad (5.73)$$

The DAC mismatch error $\varepsilon[n] = \varepsilon_I[n] + j\varepsilon_Q[n]$ is a sum of elements mismatch errors of the selected unit DAC elements for the feedback DAC signals of I/Q-paths, respectively. The $\varepsilon[n]$ is added to the input signal and directly presents to the modulator output, and therefore it should be shaped similar to quantizer noise.

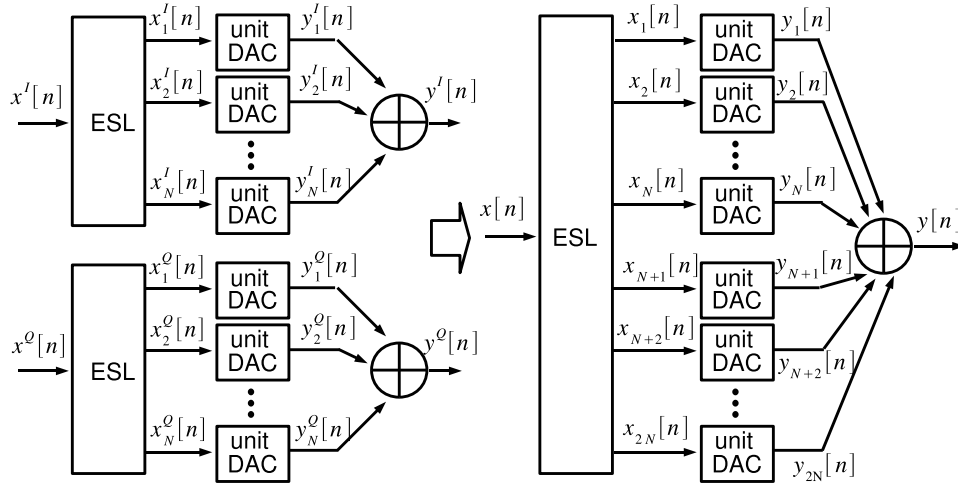


Figure 5.38.: Complex DAC bank.

In order to overcome the drawback of multibit QBP $\Sigma\Delta$ Ms, there are several spectral shaping methods, such as data-weighted average (DWA) based on an element rotation[SKKK04], vector-based spectral shaping[Sch02], butterfly shuffler based on bit-swapping[RCRW06a] and tree-structure[RCRW06b]. Unfortunately, they can only be applied to complex modulators centered around $f_s/4$. The spectral shaping based on butterfly shuffler and tree-structure is a more effective method than the others, because of more randomized selection of unit DAC elements as well as spectral shaping. The butterfly shuffler and the tree-structure are essentially similar to each other, except for bit-level-swapping and register-level-swapping. Furthermore, the hardware complexity for tree-structured DAC is much lower than the butterfly shuffler[RDMRW06].

In this section, the implementation of the tree-structure DAC for multibit QBP $\Sigma\Delta$ modulators centered at any intermediate frequency, will be addressed [KJWH08b]. For the tree-structured DAC, the $2N$ unit DAC elements can be addressed by the element selection logic (ESL). The ESL which gives an assurance of mismatch shaping can be made by the mismatch shaper. A main task for the mismatch spectral shaping, is to find a desirable mismatch shaper in the tree-structured DAC. Therefore, based on the

review of the complex tree-structured DAC, the complex mismatch shaper with any intermediate frequency is proposed and its hardware implementation is discussed. The effectiveness of the proposed mismatch shaper is proved. The proposed shaper can be used in the both of CT- and DT-QBP $\Sigma\Delta$ Ms.

5.5.1. Complex Tree-Structured DAC

Firstly, we review the complex tree-structured DAC. Figure 5.39 shows the tree-structured DAC with eight unit DAC elements, for a 2-bit QBP $\Sigma\Delta$ M, which can be extended into any multibit complex DACs. Every unit DAC element can be addressed by the ESL outputs, for the feedback signal generation of the I/Q-path in every sample period.

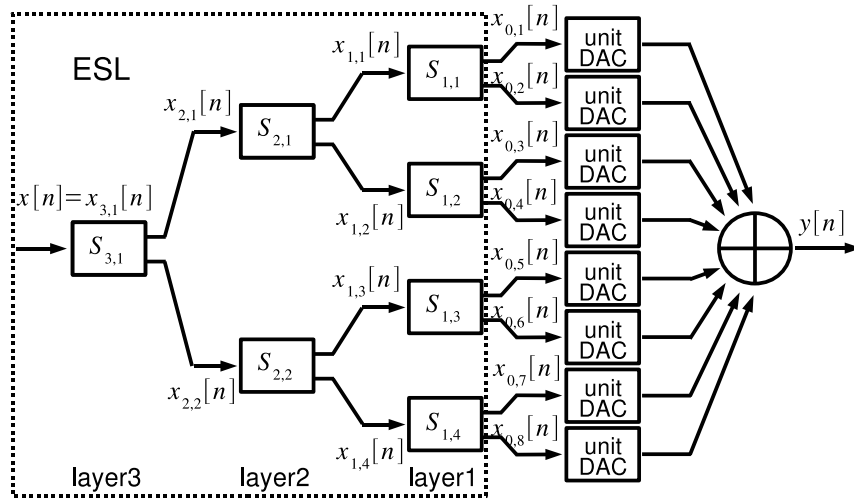


Figure 5.39.: Tree-structured complex DAC.

As shown in Figure 5.39, the ESL consists of $(b + 1)$ layers (b is the bit number of the multibit DAC) of switching blocks $S_{k,r}$, where k and r denote the layer number and the position within the layer, respectively. The switching block $S_{k,r}$ has a single input $x_{k,r}[n]$ and two outputs; one is $x_{k-1,2r-1}[n]$, other is $x_{k-1,2r}[n]$. The sum of two outputs must be equal to the input of the switching block $S_{k,r}$

$$x_{k-1,2r}[n] + x_{k-1,2r-1}[n] = x_{k,r}[n]. \quad (5.74)$$

Also, the input and outputs of the switching block $S_{k,r}$ must satisfy the following

relationship.

$$\begin{aligned} x_{k-1,2r-1}[n] &= \frac{1}{2}(x_{k,r}[n] + s_{k,r}[n]), \\ x_{k-1,2r}[n] &= \frac{1}{2}(x_{k,r}[n] - s_{k,r}[n]), \end{aligned} \quad (5.75)$$

where $s_{k,r}[n]$ is the switching sequence and is defined in the complex domain.

The following constraints for the switching sequences $s_{k,r}[n]$ must also be ensured [RCRW06b]. For layer-1 switching blocks, the switching sequence constraints can be summarized as following:

$$s_{1,r}[n] = \begin{cases} 0 & \text{if } x_{1,r}[n] \text{ is } 0, 2 \text{ or } j, 2 \\ \pm 1 & \text{if } x_{1,r}[n] \text{ is } 1 \\ \pm j & \text{if } x_{1,r}[n] \text{ is } j \\ \pm 1 \mp j & \text{if } x_{1,r}[n] \text{ is } 1+j \end{cases} \quad (5.76)$$

These constraints guarantee that the outputs of the switching blocks within layer-1 are limited to $\{0, 1, j\}$. For all other layers, the above constraints can also be used, but it is rather hardware-complex. Therefore, the following constraints may be used:

$$\begin{aligned} s_{k,r}^I[n] &= \begin{cases} 0 & \text{if } x_{k,r}^I[n] \text{ is even} \\ \pm 1 & \text{if } x_{k,r}^I[n] \text{ is odd} \end{cases} \\ s_{k,r}^Q[n] &= \begin{cases} 0 & \text{if } x_{k,r}^Q[n] \text{ is even} \\ \pm 1 & \text{if } x_{k,r}^Q[n] \text{ is odd} \end{cases} \end{aligned} \quad (5.77)$$

5.5.2. Complex Mismatch Shaper

The DAC mismatch error $\varepsilon[n]$ is a linear combination of the switching sequences $s_{k,r}[n]$ [Gal97]. If the switching sequences are all uncorrelated and share the same K -th shaped sequences, the DAC mismatch error $\varepsilon[n]$ will be a K -th shaped sequence as well. Therefore, a desirable spectral shaping for the $\varepsilon[n]$ conforms to the generated switching sequences $s_{k,r}[n]$.

The switching sequences with complex spectral shaping are obtained from the complex shaper, as shown in Figure 5.40, which was proposed in [RDMRW06]. It consists of a complex loop filter defined in the digital domain with no input signal, and a restricted quantizer. The outputs of the restricted quantizer are forced by the inputs $sv_{k,r}^I[n]$, $sv_{k,r}^Q[n]$ and $x_{k,r}[n]$ to satisfy the constraints (see next subsection). It can be seen that an additional error ($L_{k,r}[n] = L_{k,r}^I[n] + jL_{k,r}^Q[n]$) of the restricted quantizer is shaped by a complex loop filter $H_m(z)$ similar to the quantizer error in the conventional

analog $\Sigma\Delta$ M. Therefore, the switching sequence $s_{k,r}[n]$ is

$$s_{k,r}(z) = \frac{L_{k,r}(z)}{1 + H_m(z)}. \quad (5.78)$$

Now, it can be concluded that the complex spectral shaping of the switching sequence $s_{k,r}[n]$ depends on the complex loop filter $H_m(z)$ for the complex mismatch shaper. The

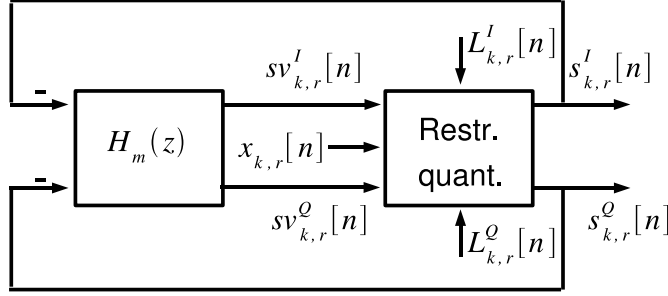


Figure 5.40.: Complex mismatch shaper.

noise introduced by unit DAC element mismatch error, which is zero-mean randomized, has a white noise distribution in frequency domain. The complex mismatch shaper should move the in-band white noise by the mismatch to the out-of-band. Therefore, the loop filter of the complex mismatch shaper should be centered in the passband of the QBP $\Sigma\Delta$ M.

Figure 5.41 shows a first-order complex mismatch shaper which is defined in the digital domain. It has cross-couplings to move from DC to the intermediate frequency. The quantizer is restricted by a parity sequence of the input $x_{k,r}[n]$ and state variables $sv_{k,r}^I[n]$, $sv_{k,r}^Q[n]$. It can be seen that except for no input signal, the complex mismatch shaper behaves like a first-order digital QBP $\Sigma\Delta$ M. The loop filter transfer function of the first-order complex mismatch shaper is

$$H_{1,m}(z) = \frac{(R_1 + jR_2)z^{-1}}{1 - (R_1 + jR_2)z^{-1}}, \quad (5.79)$$

and the additional error $L_{k,r}$ is shaped by the mismatch shaping transfer function. Hence, the output transfer function of the first-order complex mismatch shaper is

$$s_{k,r}(z) = [1 - (R_1 + jR_2)z^{-1}] \cdot L_{k,r}(z). \quad (5.80)$$

Now, if the parameters R_1 , R_2 are properly selected, the complex mismatch shaper can move the mismatch noise power from the in-band to the out-of-band. With the ratio of the intermediate frequency to the sample frequency, $M_0 = f_s/f_c$, the mismatch

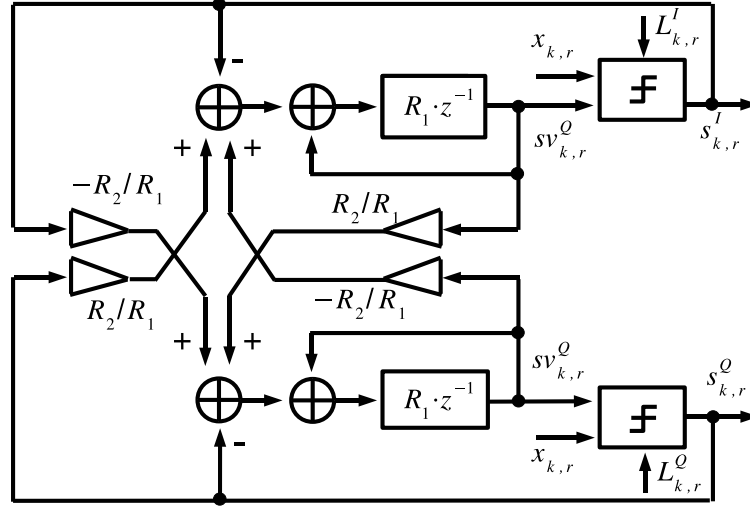


Figure 5.41.: First-order complex mismatch shaper.

shaper parameters are denoted as follows:

$$R_1 = \cos(2\pi/M_0), \quad R_2 = \sin(2\pi/M_0). \quad (5.81)$$

It implies that R_1 decreases but R_2 increases with increasing intermediate frequency. For $f_c = f_s/4$, the transfer function of the complex mismatch shaper is

$$s_{k,r}(z) = [1 - jz^{-1}] \cdot L_{k,r}(z). \quad (5.82)$$

The implementation is considerably easy because of an elimination of multiplier operations. Note that for the b -bit tree-structured DAC, the total number of the required mismatch shapers is the same as the number of switching blocks $S_{k,r}$, is $(2^{b+1} - 1)$.

5.5.3. Implementation of Complex Mismatch Shaper

In the tree-structured DAC, the real and imaginary terms of the input/output signals in the switching block $S_{k,r}$ are always positive integers, because the real and imaginary terms of switching sequence $s_{k,r}$ are limited to $\{0, \pm 1\}$ as shown in Equation (5.76) and (5.77). Therefore, the register operations between the successive switching blocks of the tree-structured DAC obey just as proposed in [Gal97].

In the complex mismatch shaper for the switching blocks $S_{k,r}$, assuming a present state variable $Q_{k,r}^p$ which has one of $\{-1, 1\}$, the switching sequence $s_{k,r}$, i.e., the restricted quantizer output, depends on the parity sequence of $x_{k,r}$ and the state variable $sv_{k,r}$. This part is based on the original scripts which were proposed in [RDMRW06] and they are more detailed here, as follows:

- When both $x_{k,r}^I[n]$ and $x_{k,r}^Q[n]$ are even ($Q_{k,r}^n[n]$ defines next state),

$$s_{k,r}^I[n] = 0, \quad s_{k,r}^Q[n] = 0, \quad Q_{k,r}^n[n] = -Q_{k,r}^p[n]. \quad (5.83)$$

- When $x_{k,r}^I[n]$ is even and $x_{k,r}^Q[n]$ is odd, or the opposite,
if $x_{k,r}^I[n] : \text{even}, \quad s_{k,r}^I[n] = 0.$
if $\text{sign}(sv_{k,r}^Q[n]) = 0,$

$$s_{k,r}^Q[n] = -Q_{k,r}^p[n], \quad Q_{k,r}^n[n] = -Q_{k,r}^p[n]. \quad (5.84)$$

if $\text{sign}(sv_{k,r}^Q[n]) \neq 0,$

$$s_{k,r}^Q[n] = \text{sign}(sv_{k,r}^Q[n]), \quad Q_{k,r}^n[n] = Q_{k,r}^p[n]. \quad (5.85)$$

- When both $x_{k,r}^I[n]$ and $x_{k,r}^Q[n]$ are odd,
if $\text{sign}(sv_{k,r}^I[n]) \neq 0, \text{sign}(sv_{k,r}^Q[n]) \neq 0,$

$$\begin{aligned} s_{k,r}^I[n] &= \text{sign}(sv_{k,r}^I[n]), \quad s_{k,r}^Q[n] = \text{sign}(sv_{k,r}^Q[n]), \\ Q_{k,r}^n[n] &= Q_{k,r}^p[n]. \end{aligned} \quad (5.86)$$

if $\text{sign}(sv_{k,r}^I[n]) = \text{sign}(sv_{k,r}^Q[n]) = 0,$

$$\begin{aligned} s_{k,r}^I[n] &= Q_{k,r}^p[n], \quad s_{k,r}^Q[n] = -s_{k,r}^I[n], \\ Q_{k,r}^n[n] &= -Q_{k,r}^p[n]. \end{aligned} \quad (5.87)$$

if $\text{sign}(sv_{k,r}^I[n]) \neq 0, \text{sign}(sv_{k,r}^Q[n]) = 0,$ or the opposite

$$\begin{aligned} s_{k,r}^I[n] &= \text{sign}(sv_{k,r}^I[n]), \quad s_{k,r}^Q[n] = -s_{k,r}^I[n], \\ Q_{k,r}^n[n] &= -Q_{k,r}^p[n]. \end{aligned} \quad (5.88)$$

The switching sequence constraints (5.77) can be ensured by the above assignment. When both $x_{k,r}^I[n]$ and $x_{k,r}^Q[n]$ are odd, the restricted quantizer is similar to a dithered single-bit quantizer in conventional $\Sigma\Delta$ Ms.

For layer-1 switching blocks, when both $x_{k,r}^I[n]$ and $x_{k,r}^Q[n]$ are odd, that is, $x_{1,r}[n] = 1+j$, a careful consideration needs because $s_{1,r}[n] = \pm 1 \mp j$ from (5.76). This constrain guarantees that $x_{0,2r}[n], x_{0,2r-1}[n]$ can select the other unit DAC elements for the I/Q paths. This constrain can be implemented as follows:

if $\text{sign}(sv_{k,r}^I[n]) \neq \text{sign}(sv_{k,r}^Q[n])$ and both are nonzero,

$$\begin{aligned} s_{k,r}^I[n] &= \text{sign}(sv_{k,r}^I[n]), \quad s_{k,r}^Q[n] = \text{sign}(sv_{k,r}^Q[n]), \\ Q_{k,r}^n[n] &= Q_{k,r}^p[n]. \end{aligned} \quad (5.89)$$

if $\text{sign}(sv_{k,r}^I[n]) = \text{sign}(sv_{k,r}^Q[n])$ and $sv_{k,r}^I[n] \geq sv_{k,r}^Q[n]$,

$$s_{k,r}^I[n] = 1, \quad s_{k,r}^Q[n] = -1, \quad Q_{k,r}^n[n] = Q_{k,r}^p[n]. \quad (5.90)$$

if $\text{sign}(sv_{k,r}^I[n]) = \text{sign}(sv_{k,r}^Q[n])$ and $sv_{k,r}^I[n] < sv_{k,r}^Q[n]$,

$$s_{k,r}^I[n] = -1, \quad s_{k,r}^Q[n] = 1, \quad Q_{k,r}^n[n] = Q_{k,r}^p[n]. \quad (5.91)$$

With the extra cases, they correspond to Equations (5.87) and (5.88). The next state is defined as $Q_{k,r}^p[n+1] = Q_{k,r}^n[n]$, and the above assign of $Q_{k,r}^n[n]$ might avoid spurious tones by zero-crossing.

Until now, we assign the output states for the restricted quantizers of all layers. These can address 2N DAC element with a pseudo-randomized selection which depends on $sv_{k,r}$ and $x_{k,r}$. The randomized selection among the complex DAC bank is effective for DC offset by mismatch error. Note that the above assign for the restricted quantizer might be applied to the complex mismatch shaper with any intermediate frequency, in tree structured DAC.

The complex spectral shaping centered around intermediate frequency results from a combination of cross-couplings and the restricted quantizer. But, the direct combination as shown in Figure 5.41 contains decimal operations in a calculation of the state variable $sv_{k,r}$, needs the addition and the multiplication operations with the floating- or fixed -point decimal operands. It implies that the hardware complexity highly increases, therefore a great significance of the complex mismatch shaping will be loss.

In order to avoid the decimal operations in complex mismatch shaper, we modify the shaper as shown in Figure 5.42. It is equal to Figure 5.41 for B=1. If the mismatch shaper parameters are approached as follows:

$$R_1 \cong \sum_{k=-\infty}^{\infty} R_{1,k} \cdot 2^k, \quad R_2 \cong \sum_{k=-\infty}^{\infty} R_{2,k} \cdot 2^k, \quad (5.92)$$

then the multiplier might be replaced by a few shift and addition operators, where $R_{1,k}$ and $R_{2,k}$ are limited to $\{0, \pm 1\}$. In Figure 5.42, the multiplier after the restricted quantizer is the assign multiplied with 2^{B-1} , but not strictly multiplied. In the following

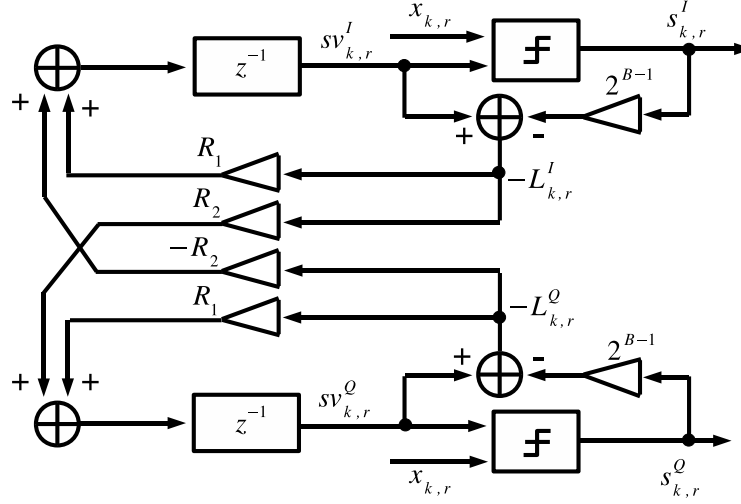


Figure 5.42.: Modified first-order complex mismatch shaper.

approach, that is,

$$\begin{aligned}
 \text{Limiter} &= 2^{B-1}; \\
 L_{k,r}^I[n] &= \text{Limiter} \cdot (-s_{k,r}^I[n]) + sv_{k,r}^I[n]; \\
 L_{k,r}^Q[n] &= \text{Limiter} \cdot (-s_{k,r}^Q[n]) + sv_{k,r}^Q[n]; \\
 sv_{k,r}^I[n+1] &= \text{round}(R_1 \cdot L_{k,r}^I[n] - R_2 \cdot L_{k,r}^Q[n]); \\
 sv_{k,r}^Q[n+1] &= \text{round}(R_1 \cdot L_{k,r}^Q[n] - R_2 \cdot L_{k,r}^I[n]);
 \end{aligned} \tag{5.93}$$

the multiplication of *Limiter* and *round* operation guarantee the integer operations on a $(B+1)$ -bit data structure, including a sign bit.

For the stability of the mismatch shaper, the following bit limitation can be used: if $\text{abs}(sv_{k,r}^I[n+1]) \geq 2 \cdot \text{Limiter} - 1$, or $\text{abs}(sv_{k,r}^Q[n+1]) \geq 2 \cdot \text{Limiter} - 1$,

$$\begin{aligned}
 sv_{k,r}^I[n] &= (2 \cdot \text{Limiter} - 1) \cdot \text{sign}(sv_{k,r}^I[n+1]), \\
 sv_{k,r}^Q[n] &= (2 \cdot \text{Limiter} - 1) \cdot \text{sign}(sv_{k,r}^Q[n+1]).
 \end{aligned} \tag{5.94}$$

It can be recognized that for a higher B , the noise power of $s_{k,r}$ is similar to the ideal noise-shaped spectrum. Figure 5.43 shows the power spectrum of the modified mismatch shaper with a 8-bit data structure, which is centered at $w_c = \pi/6$. The simulation was done with Matlab. For layer-1 switching blocks, the desirable first-order noise shaping clearly appears. The effectiveness of the proposed complex mismatch-shaper for tree-structured DAC was proved by simulation in 3rd-order CT-QBP 3-bit $\Sigma\Delta$ modulator with intermediate frequency $f_c = f_s/12$, bandwidth $f_B = 200$ KHz, and

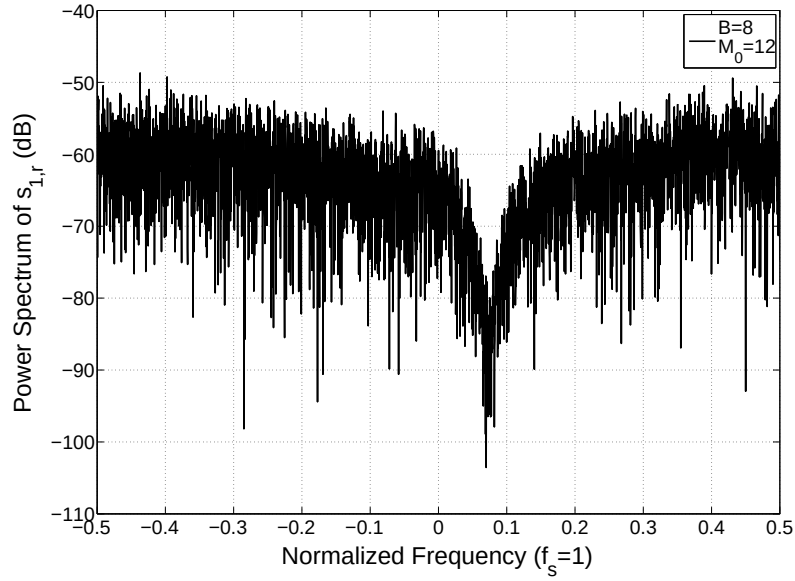


Figure 5.43.: First-order shaped power spectrum of layer-1 switching sequence $s_{1,r}$.

$OSR = 64$. Figure 5.44 shows the output spectrum of the simulated modulator. It can be seen that after the mismatch error is shaped by the proposed first-order shaper, the in-band noise level is notably improved.

In this section, a first-order complex mismatch shaper which is based on a complex noise shaping technique has been presented for the reduction of the mismatch effect in feedback multibit DACs of QBP $\Sigma\Delta$ Ms centered at any center frequency. The proposed complex mismatch shaper can be applied to an ESL design in a tree-structured DAC and is centered at the same intermediate frequency as that of QBP $\Sigma\Delta$ M.

Until now, in this chapter, the nonlinearities of the CT-QBP $\Sigma\Delta$ Ms have been presented. We can summarize as follows:

- Finite GBW of the amplifiers affects the stability and the translation to a wanted center frequency, f_c , of the polyphase filters. The lower GBW of the amplifier, the less is the stability of the complex integrators, and the greater is the deviation from f_c depending on a selection of the integrating scales. Unfortunately, it should be noted that the greater the center frequency, the worse is the stability of the complex integrator. In order to ensure the stability, the use of a lossy complex integrator is desirable. The deviation from the center frequency can be decreased by inserting the transconductors in the virtual ground nodes of the amplifiers.
- Excess loop delay seriously results in reducing the performance of the CT-QBP $\Sigma\Delta$ Ms, such as stability of the modulator and degradation of the SNR. In CT-

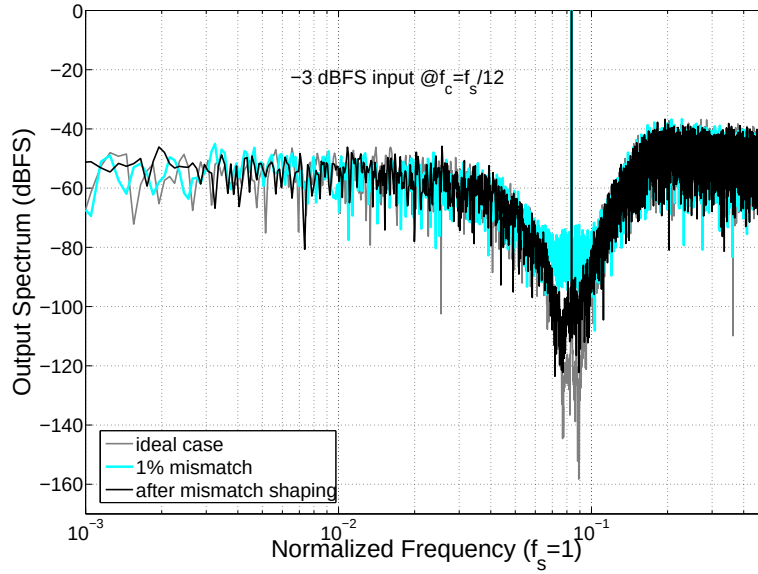


Figure 5.44.: Output power spectrum of multibit complex $\Sigma\Delta$ modulator.

QBP $\Sigma\Delta$ Ms, the effect of the excess loop delay increases with the center frequency. In order to compensate its effect, the additional feedback DAC with unit delay and the feedforward complex compensation coefficient can be used.

- Mismatch loop delay of the I/Q paths makes the additional aliased noise power in a passband, and therefore results in the degradation of the SNR, causing an extra feedback loop. For a lower center frequency, its effect significantly can be reduced. It can be completely compensated by the use of D-latches in the feedback paths and the compensation scheme of excess loop delay.
- Clock jitter severely reduces the modulator performance. The closed-form formula in CT-QBP $\Sigma\Delta$ M with NRZ feedback DAC pulse have been derived. The degradation of the SNR caused by clock jitter depends on the number of the output bit transitions. In order to reduce the jitter-induced noise, an optimized transfer function which decreases the number of the bit transitions and the modified feedback DAC analog waveforms which were applied to lowpass CT modulators.
- The mismatch of the unit elements in the multibit DAC bank causes a nonlinear error of the modulator. In order to reduce the nonlinearity caused by DAC mismatch in QBP $\Sigma\Delta$ Ms, a complex mismatch shaping technique which is based on a noise shaping, can become a desirable solution. A first-order complex mismatch shaper have been proposed which is centered at any center frequency.

6. Application Examples

This chapter describes two application examples; one is high resolution CT-QBP $\Sigma\Delta$ M for GSM/EDGE low-IF receiver, the other is reconfigurable multimode wideband CT-QBP $\Sigma\Delta$ M for GPS/Galileo low-IF receiver. The modulators are designed by the proposed CICFF topology.

6.1. CT-QBP $\Sigma\Delta$ M for GSM/EDGE Low-IF Receiver

This modulator was designed for GSM/EDGE low-IF receiver [KJWH08c], [KJWH08a]. From the GSM/EDGE low-IF receiver system, the frequency characteristics which have been derived for GSM/EDGE ADC are $f_c = 130$ kHz, $f_B = 200$ kHz. The supply voltage is limited to 1.8 V with the chosen standard $0.25\mu\text{m}$ CMOS technology.

6.1.1. Polyphase Filter Design

A 3^{rd} -order polyphase filter for CT-QBP $\Sigma\Delta$ M for GSM/EDGE low-IF receiver was selected. Figure 6.1 shows the polyphase filter with CICFF topology, designed for GSM/EDGE. The polyphase filter includes a local feedback loop for an optimized placement of the zeros in NTF. The optimized placement can minimize the shaped noise spectrum in passband [NST96]. The summation node for the output of second quadrature complex integrator is moved to front of the local feedback loop, in order to avoid resonance damping of the local feedback loop [DKG⁺05]. Note that if the last integrator is not within the local feedback loop, the capacitive summation for all signals should be implemented at the last stage. The polyphase filter transfer function is

$$H_{PPF}(s) = \frac{k_1 a_1 (s - jw_c)^2 + k_2 a_1 a_2 (s - jw_c) + a_1 a_2 a_3}{(s - jw_c)[(s - jw_c)^2 + a_2 a_3 b_f]}, \quad (6.1)$$

where $a_i = 1/(R_i C_i)$, $b_f = R_2/R_f$ and $w_c = 1/(R_{C,i} C_i) = 1/(R_{S,i} C_{k,i})$ in all stages. As shown in Equation (6.1), the feedforward coefficients k_i do not affect the placement of poles in the polyphase filter, therefore there is no change in the optimized placement of zeros in the equivalent NTF. The feedforward coefficients only affect the stability of the modulator, because the poles of the NTF depend on the feedforward coefficients and the scale coefficients of the integrators.

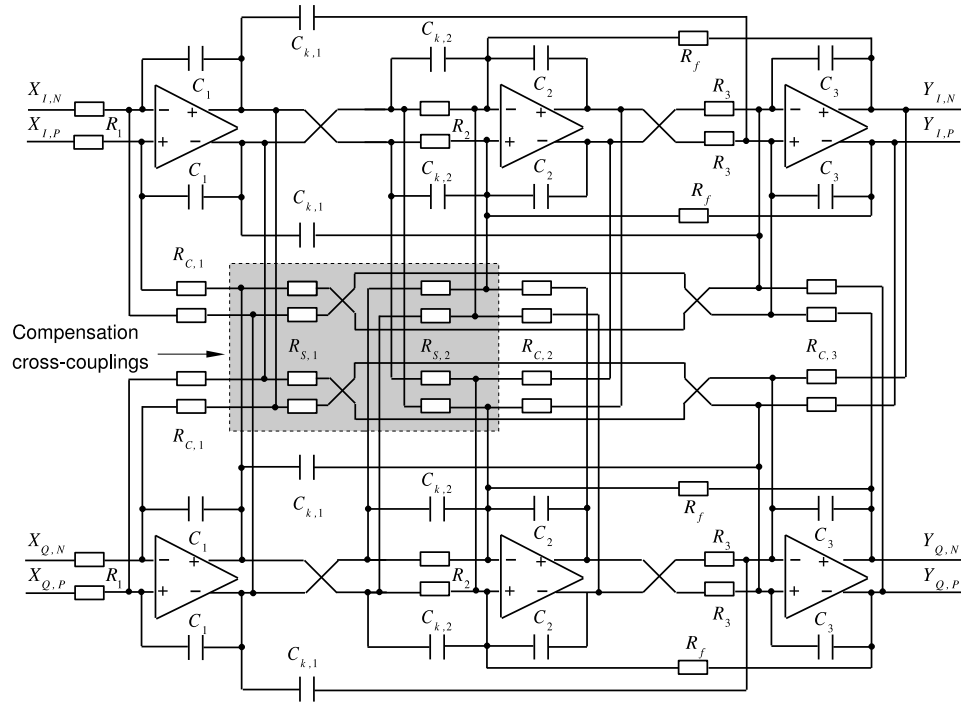


Figure 6.1.: Polyphase filter for GSM/EDGE ADC.

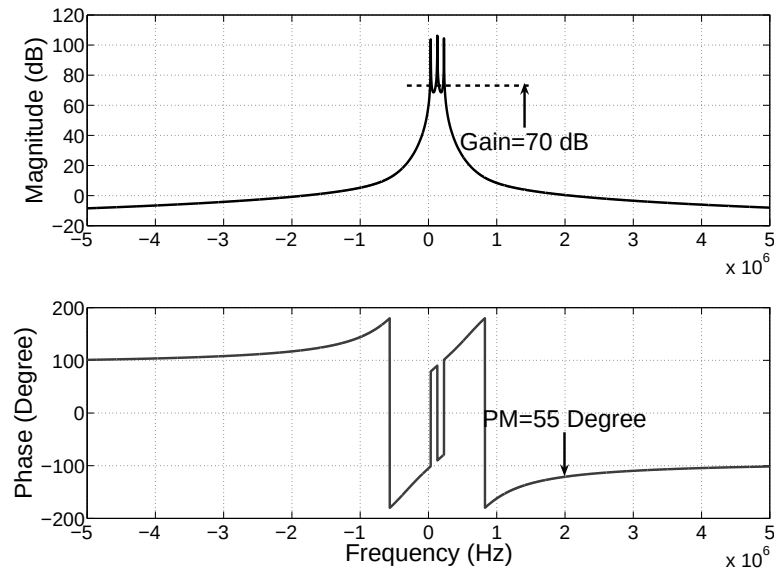


Figure 6.2.: Frequency response of the designed polyphase filter.

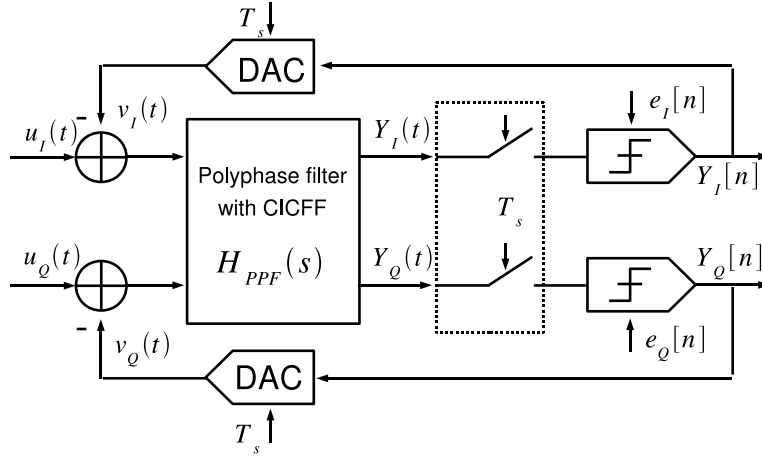
The polyphase filter transfer function is shown in Figure 6.2. The coefficients of the polyphase filter are optimized for a maximum open-loop phase margin, as this improves the modulator stability, allowing a relaxation of the delay requirements on the analogue circuits. The phase margin is around 55° . The polyphase filter gain at in-band is selected as 70 dB to meet the required SNR. The modulator coefficients used in this design are shown in Table 6.1.

Table 6.1.: modulator parameter

coefficients	values
$a_1, a_2 = a_3$	$0.8702/T_s, 0.1142/T_s$
b_f, k_1, k_2	0.04, 0.5, 1.0

6.1.2. Modulator Design

The modulator architecture is shown in Figure 6.3. It consists of the proposed polyphase filter, quantizers at I/Q feedforward paths and DACs at I/Q feedback paths. The feed-


 Figure 6.3.: CT-QBP $\Sigma\Delta$ M with CICFF topology.

back DAC pulse was chosen as NRZ, because it has a lower influence on the clock jitter than other DAC analog pulses.

In this design, the NTF is computed by the inverse method from the proposed polyphase filter and modulator parameters, then its behavior was estimated in z -domain. This method gives an easier feasibility of the optimized circuit design in CT domain, because it starts from the CT polyphase filter design. The out-of-band gain of NTF is kept below 1.5 for stability and all poles of the NTF locate within unit circle at sample clock of $f_s = 26$ MHz as shown in Figure 6.4.

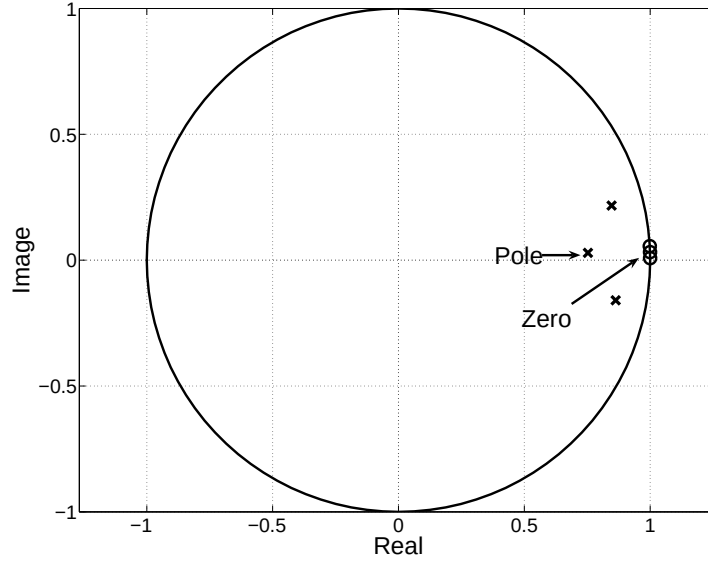


Figure 6.4.: Placement of the poles and zeros of the NTF.

6.1.3. Modulator Nonidealities

In order to satisfy demands for GSM/EDGE applications, the ADC resolution should be in the range of 13-16 bits. In an ideal case, the peak SNDR of the proposed CT quadrature bandpass single-bit $\Sigma\Delta$ modulator is 105.8 dB at the the sampling clock of 26 MHz. Unfortunately, the SNDR of the modulator is reduced by the non-ideal effects, while causing instability.

6.1.3.1. Sensitivity to RC-Product Variation

In DT modulators implemented in SC technique, the integrator scales are computed by sampling clock and capacitor ratios, which are intrinsically precise [OG06]. In contrast, in CT $\Sigma\Delta$ modulators integrator scales are mapped into resistor-capacitor products, which largely vary over chip process and temperature. The process variations of the absolute component values of 10 – 20% might cause the possible variation of the RC-product to more than 35% [PDGH⁺04]. The following equation shows a model for RC-integrator transfer function subject to a tolerance δ_{RC} .

$$INT_i(s) = \frac{1}{s \cdot R_i C_i (1 + \delta_{RC})}, \quad (6.2)$$

The RC-product variation causes the deviation in the optimized zero and the targeted pole locations of the NTF and that from the center frequency. The equivalent

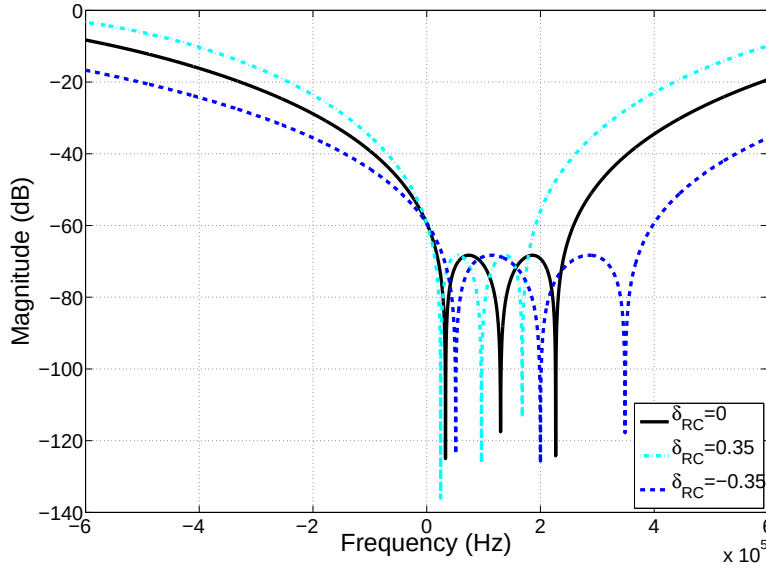


Figure 6.5.: The equivalent NTF by RC-product variations.

NTF was simulated with different RC-tolerances δ_{RC} . It can be seen that the bandwidth as well as the center frequency of the modulator are severely varied as shown in Figure 6.5. Here, all resistive and capacitive ratios such as b_f , k_i were assumed to be preserved.

When $\delta_{RC} < 0$, the modulator becomes unstable due to an aggressive noise shaping, while increasing slightly the SNDR. When $\delta_{RC} > 0$, the degradation of the SNDR results. For $\delta_{RC} = 0.35$, the SNDR loss is around 10 dB as shown in Figure 6.6. Therefore, the RC-product variations should be suppressed or handled. In this application, RC-product variation until 40% is trimmed by extra pins and simple logic scheme.

In addition, the quadrature bandpass $\Sigma\Delta$ modulators are susceptible to a mismatch between the circuit components in the I/Q paths [CS98b], [YS99], [RE02], which leads a severe decrease of the SNR. Since the subsequent stages in polyphase filter suppress the unwanted effects introduced by mismatch, the mismatch in I/Q paths closer to the quantizer is less problematic. The crosstalk depends mainly on the mismatch between the input resistors, and feedback DAC resistors in the first quadrature complex integrator. Therefore, it is necessary to take care in chip design for a good matching in the first stage of the modulator.

6.1.3.2. Excess Loop Delay

Figure 6.7 shows the placement of poles and zeros of the NTF with increasing excess loop delay, in this application. The placement of the zeros of the NTF is not changed, but the placement of the poles has tendency toward the outside of the unit circle with

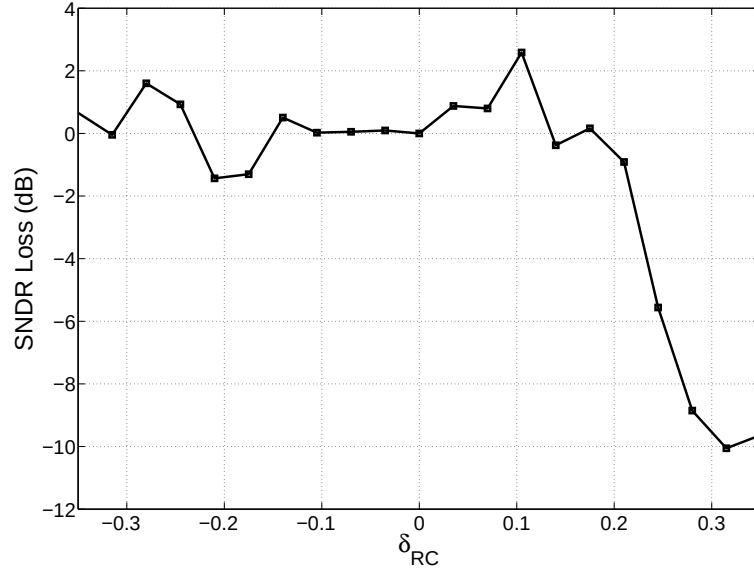


Figure 6.6.: SNDR loss vs. RC-product variations.

increasing excess loop, causing a loss of modulator stability. It can also be seen that an additional pole and zero are introduced by the excess loop delay, increasing the order of the denominator and the numerator of the NTF by one. From simulation results, the designed CT quadrature bandpass $\Sigma\Delta$ modulator was shown that when modulator loop delay is less than 50% of full sample period, the SNDR loss is less than 6 dB as shown in Figure 6.8 and hence there is no need to use an additional compensation scheme. The simulation was done with NRZ feedback DAC pulse in I/Q paths and input signal level of -3 dBFS.

6.1.3.3. Clock Jitter

The effect of clock jitter in NRZ feedback DAC pulse was estimated by using Equation (5.69). In this design application, the variance of the DAC clock uncertainty should be less than 5 ps at sampling clock of 26 MHz as shown in Figure 6.9.

6.1.3.4. Finite GBW

In general, the first amplifier demands higher GBW in CT $\Sigma\Delta$ Ms due to the feedback DAC impulse response. The designed modulator architecture has summation nodes at the inputs of the second and the third integrators as shown in Figure 6.1, demanding higher GBW. Therefore, in this application, all amplifiers have identical structures and sizes - identical GBW and DC gain. The equivalent NTF in z -domain is shown in Figure 6.10.

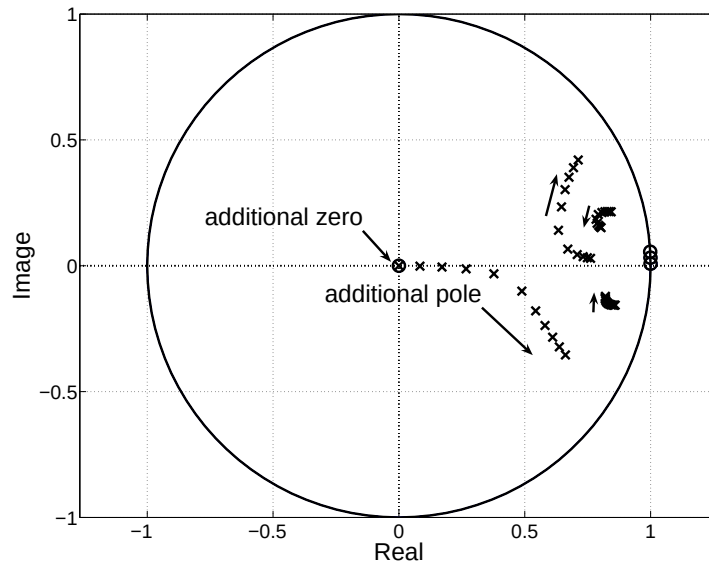


Figure 6.7.: The placement of pole and zero vs excess loop delay. The arrow denotes the increasing direction of excess loop delay.

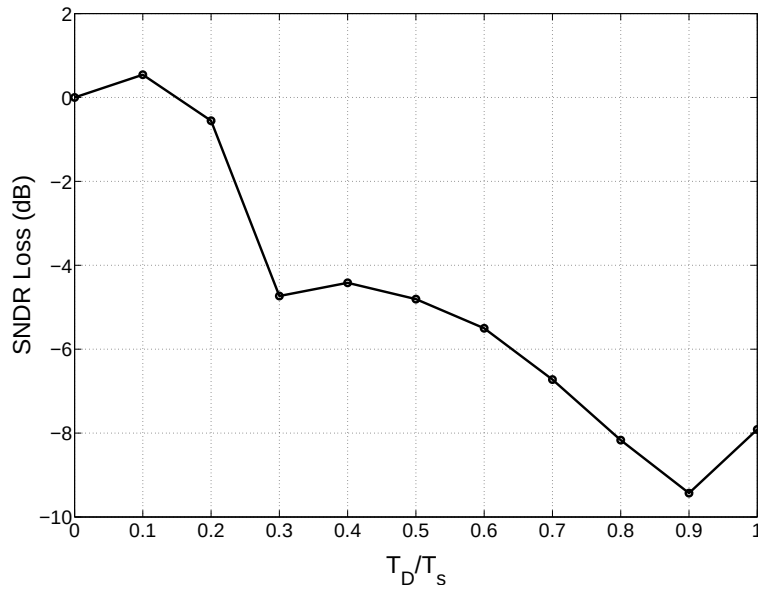


Figure 6.8.: SNDR loss vs. excess loop delay.

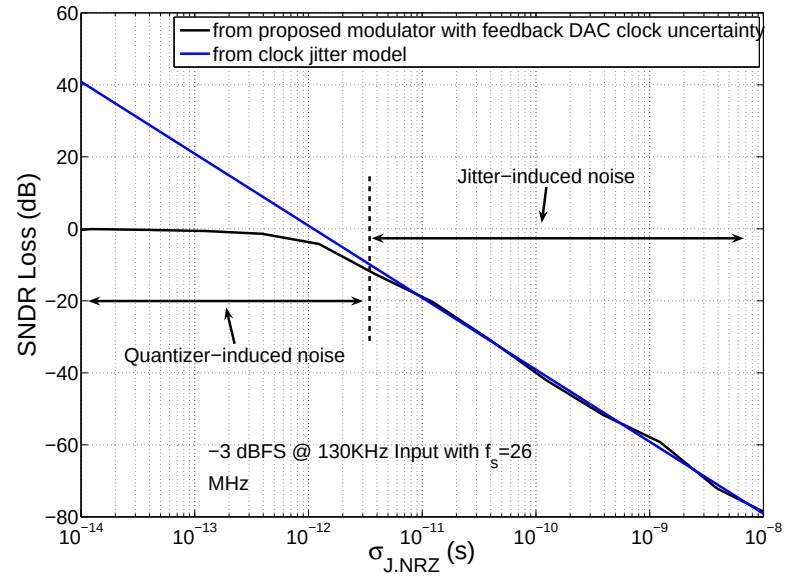


Figure 6.9.: SNDR loss vs. clock jitter variance.

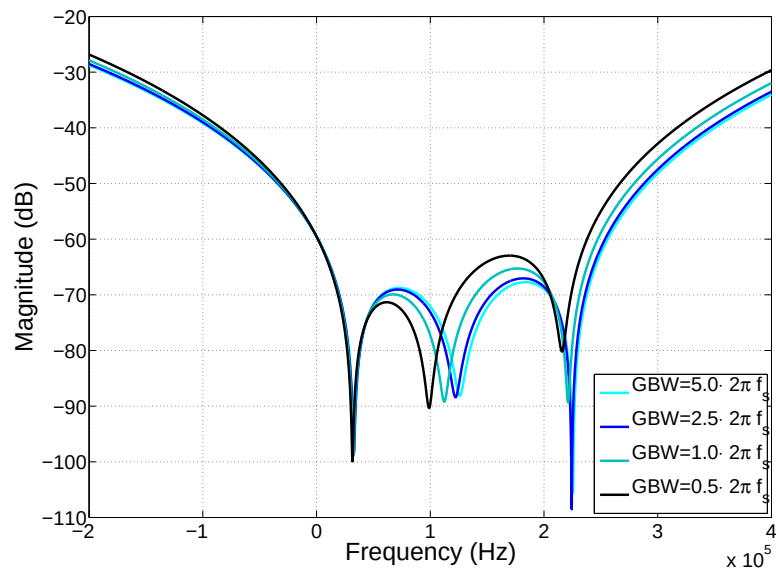


Figure 6.10.: The equivalent NTF with finite GBW.

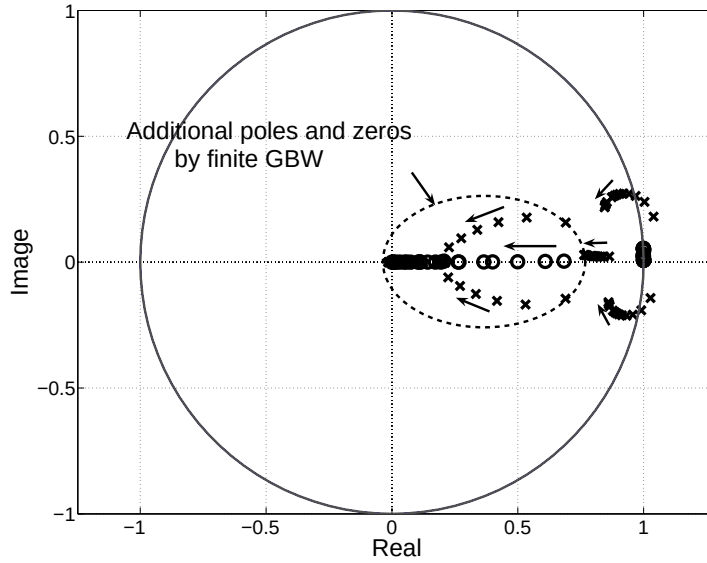


Figure 6.11.: The placement of poles and zeros of the NTF.

Figure 6.11 shows the placement of poles and zeros. It can be seen that additional poles and zeros are placed around the origin in z -plane. With a lower GBW, the poles are placed outside of the unit circle and the additional poles and zeros also affect the modulator performance. On the other hand, for a higher GBW, additional poles and zeros are canceled around the origin and the modulator might give an adequate performance. The SNDR loss by finite GBW is shown in Figure 6.12. It can be shown that in our design consideration, the GBW should be at least as large as $2\pi f_s$.

6.2. CT-QBP $\Sigma\Delta$ M for GPS/Galileo Low-IF Receiver

This modulator was designed for multimode RF receiver which is shared with three satellite navigation systems for GPS, Galileo and Glonass. It consists of shared RF block and two parallel low-IF bands for GPS/Galileo and for Glonass [KJN⁺08]. In this application we only focus the implementation of $\Sigma\Delta$ M for GPS/Galileo [KJZ⁺07].

From the system budget, the frequency characteristics which have been derived for GPS/Galileo ADC are $f_c = 4.092$ MHz, $f_B = 2/4$ MHz (GPS/Galileo). The input DR should be more than 42 dB with an OSR = 64/32 (GPS/Galileo). The supply voltage is limited to 1.8-V with the chosen standard $0.25\mu\text{m}$ CMOS technology. The bandwidth change to switch between GPS and Galileo is implemented by a single logic pin. The center frequency and bandwidth are additionally controlled by digital calibration.

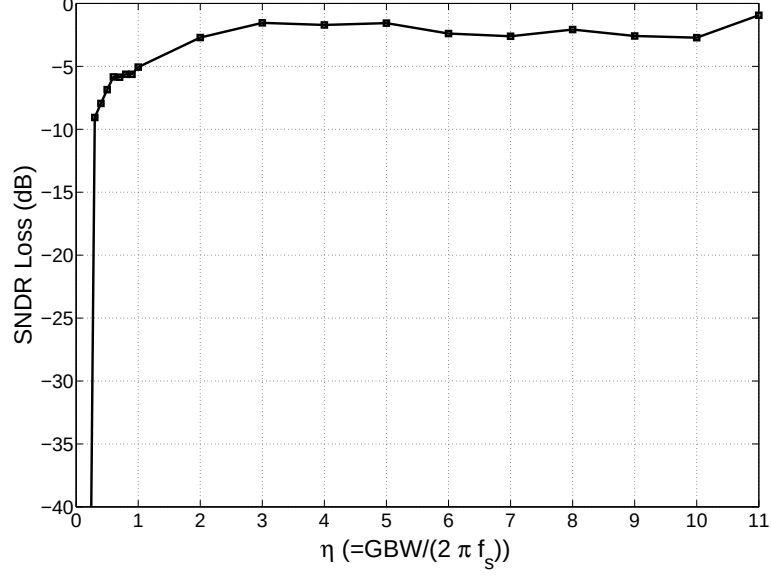


Figure 6.12.: SNDR loss vs. finite GBW.

6.2.1. Polyphase Filter Design

The polyphase filter for the GPS/Galileo CT-QBP $\Sigma\Delta$ M was chosen as 2^{nd} -order capacitive feedforward topology, which is sufficient for the low resolution. A local feedback loop is chosen in order to get an optimized zero placement in a DT equivalent NTF, and to face the demand of a wideband conversion for GPS/Galileo. In order to reduce the effects of excess loop delay and finite GBW, lossy integrators are placed instead of ideal integrators. The selection of a lossy integrator is important to ensure the modulator stability².

In case of a second-order polyphase filter with CICFF topology, the capacitive summation and the compensation cross-couplings for moving the zeros to center frequency are implemented at the input of the local feedback loop. The transfer function of a second order polyphase filter with CICFF topology can be described as

$$H_{PPF,2}(s) = \frac{k_1 w_{0,1} \sqrt{A_1} (s - jw_c) + w_{0,1}^2 A_1}{\left(s + \frac{w_{0,1}}{Q_1} - jw_c + jw_{0,1}\right) \left(s + \frac{w_{0,1}}{Q_1} - jw_c - jw_{0,1}\right)}, \quad (6.3)$$

where $w_{0,1}^2 = (R_1/R_{F,1})/(R_1 C_1)^2$, $w_c = 1/(R_{C,1} C_1)$, $Q_1 = (R_{P,1}/R_1) \sqrt{R_1/R_{F,1}}$, $A_1 = R_{F,1}/R_1$ and $k_1 = C_{k,1}/C_1$. Due to the special structure of the local feedback loop, this implementation is only suitable for stand-alone application of the second-order

²It should be noted that linearity and SNR would be enhanced with an ideal integrator.

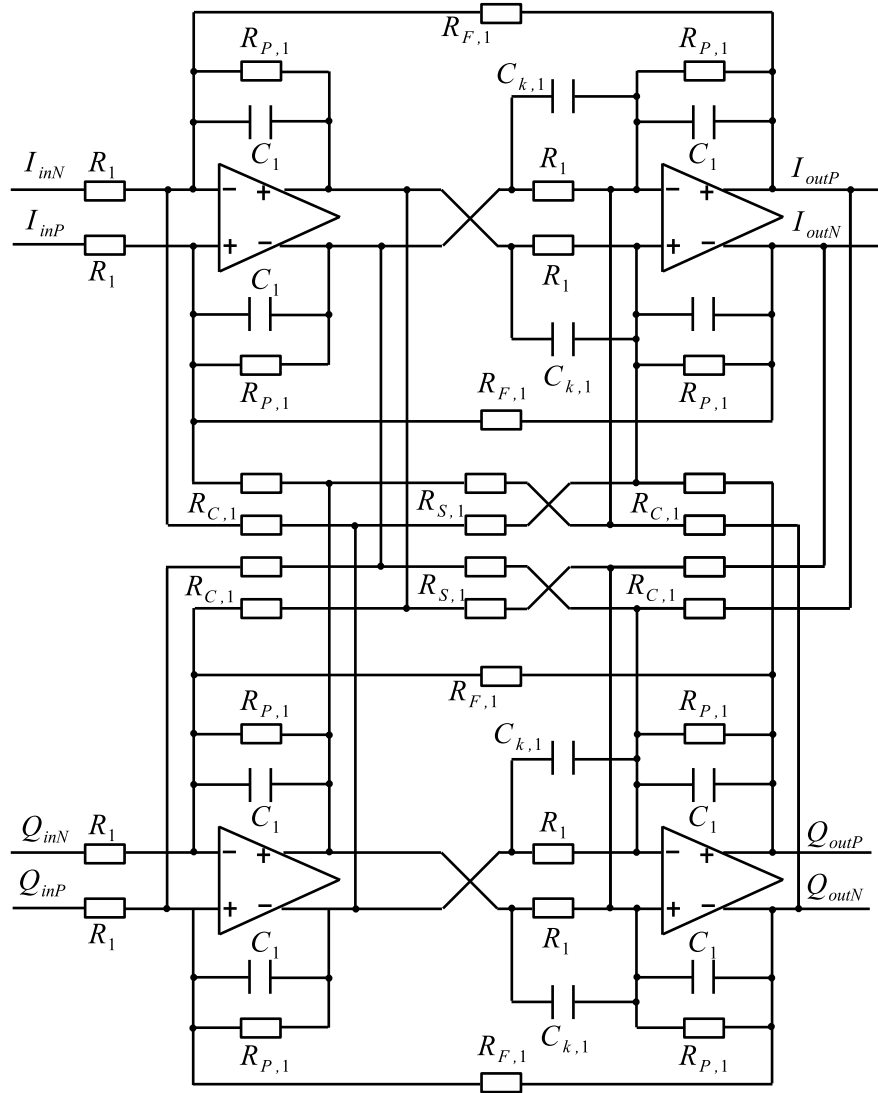


Figure 6.13.: Polyphase filter for GPS/Galileo application.

polyphase filter with capacitive feedforward summation.

For the $\Sigma\Delta$ modulator, a feedback DAC signal as well as the input signal should be summed by the capacitive feedforward summation scheme. This requires extra capacitive summation and separate compensation for the feedback DAC signal in the second-order $\Sigma\Delta$ modulator due to the capacitive summation at the input of the local feedback loop. Thus circuit complexity and chip area would be increased.

The most effective solution is to move the summation node to the input of the second integrator in the local feedback loop. A full schematic of the polyphase filter is shown in Figure 6.13. In this case, it should be noted that the compensation cross-coupling affects moving poles as well as zeros to center frequency, in contrast to higher order polyphase filter than second-order. The values of the compensation resistors are $R_{S,1} = R_{C,1}/k_1$. The polyphase filter transfer function of Figure 6.13 is

$$H_{PPF,m,2}(s) = \frac{k_1 w_{0,1} \sqrt{A_1} (s - jw_c) + w_{0,1}^2 A_1}{\left(s + \frac{w_{0,m}}{Q_m} - jw_c + jw_{0,m}\right) \left(s + \frac{w_{0,m}}{Q_m} - jw_c - jw_{0,m}\right)}, \quad (6.4)$$

$$w_{0,m}^2 = w_{0,1}^2 (1 - k_1 R_1 / R_{P,1} - 0.25 k_1^2 R_1 / R_{F,1}), \quad (6.5)$$

$$Q_m = Q_1 \left(\frac{\sqrt{1 - k_1 R_1 / R_{P,1} - 0.25 k_1^2 R_1 / R_{F,1}}}{1 + 0.5 k_1 R_{P,1} / R_{F,1}} \right). \quad (6.6)$$

When comparing Equations (6.3) to (6.4), the denominator of the transfer functions changes. Hence, only pole positions vary by this modification. From Equation 6.5 and 6.6, it can be seen, that the resonance frequency and the quality factor are lower than that of the previous implementation. Resonant damping is caused by moving the summation node to the input of the second integrator, but it ensures more stability, though the noise level in passband becomes greater for the $\Sigma\Delta$ M. This modification is only applied to the second-order QBP $\Sigma\Delta$ M with the local feedback loop and capacitive feedforward summation.

6.2.2. Modulator Design

The circuit parameters are determined from the system specifications. The resonance frequency of the local feedback loop is determined by the bandwidth w_B and the order of the $\Sigma\Delta$ modulator. The pole placement of the loop filter corresponds to that of the zeros of the NTF of the modulator. The imaginary parts of the poles are chosen to be $(w_c \pm w_0) = (w_c \pm 0.5w_B)$. Therefore, if $w_{0,m} \approx w_0$ in Equation (6.5), this leads to

$$\sqrt{R_1 / R_{F,1}} / (R_1 C_1) = 0.5w_B. \quad (6.7)$$

The conventional cross-coupling and compensation cross-coupling resistors are determined by the center frequency and the feedforward coefficients. The component values used in the design of the polyphase filter are listed in Table 6.2.

Table 6.2.: Component Values for GPS/Galileo

GPS	Galileo
$R_1 = 27.60 \text{ k}\Omega$	$R_1 = 13.80 \text{ k}\Omega$
$C_1 = 2.0 \text{ pF}$	$C_1 = 2.0 \text{ pF}$
$R_{P,1} = 275.96 \text{ k}\Omega$	$R_{P,1} = 137.98 \text{ k}\Omega$
$R_{F,1} = 919.08 \text{ k}\Omega$	$R_{F,1} = 459.54 \text{ k}\Omega$
$R_{C,1} = 19.46 \text{ k}\Omega$	$R_{C,1} = 19.46 \text{ k}\Omega$
$R_{S,1} = 19.46 \text{ k}\Omega$	$R_{S,1} = 19.46 \text{ k}\Omega$
$C_{k,1} = 2.0 \text{ pF}$	$C_{k,1} = 2.0 \text{ pF}$

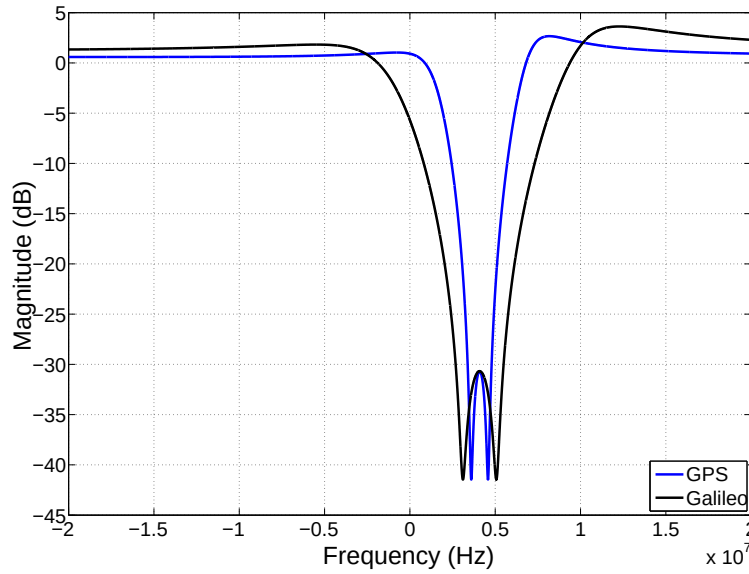


Figure 6.14.: DT equivalent NTFs for GPS/Galileo application.

The modulator architecture for GPS/Galileo low-IF receiver is the same as that of GSM/EDGE application as shown in Figure 6.3. Design procedure follows the inverse method cited in Chapter 3. Figure 6.14 shows the DT equivalent NTFs for GPS/Galileo QBP $\Sigma\Delta M$. In an ideal case, the peak SNR for GPS/Galileo application is 62.3/56.7 dB at the sampling clock of 128 MHz. The SNR of the modulator is reduced by the non-ideal effects, while causing instability, similar to GSM/EDGE application. Fortunately,

the demand on the resolution of $\Sigma\Delta$ ADCs for GPS/Galileo application is not so critical, but the signal bandwidths for GPS/Galileo application are much higher than GSM/EDGE. Therefore, the amplifiers should be designed with higher GBW in order to satisfy the SNDR, DR and stability.

The mode switch between GPS and Galileo applications is implemented by an extra pin. When the pin voltage is High, the modulator indicates GPS mode, and when the pin voltage is Low, it works at Galileo mode.

6.3. Circuit Implementation

The top schematics for chips of the GSM/EDGE and GPS/Galileo CT-QBP $\Sigma\Delta$ s comprise the proposed 3rd-order and 2nd-order polyphase filter with CICFF topology, respectively. In addition, dynamic latched comparators, the feedback NRZ feedback DAC pulse generators, output buffers for measurement, and voltage bias circuits are placed on test chips.

6.3.1. Integrator Design

OpAmp- RC complex integrators are selected for the sake of linearity in low-voltage application. In the design of the integrator, the OpAmp is most important in order to satisfy desirable specifications, because its non-ideality by finite DC gain, GBW and input capacitance affect the modulator directly. In detail, the finite DC gain, GBW and input parasitic capacitance makes an error of the integrator gain and a parasitic pole.

For GSM/EDGE application, from the sampling clock of 26 MHz, OpAmps are designed with GBW higher than 150 MHz, with phase margin of 56.5° under load capacitance of 0.2 pF. On the other hand, for GPS/Galileo application, from broad bandwidth, the OpAmps are designed with GBW higher than 500 MHz with phase margin of 52.5° under load capacitance of 0.5 pF. The DC gain of the designed OpAmps is higher than 60 dB in two applications. In order to accommodate the low supply voltage, fully differential two stage Miller OpAmps were chosen, where a continuous-time common mode feedback circuit is attached as shown in Figure 6.15. The simulated DC power consumptions of the OpAmps are about 170 μ A for GSM/EDGE and about 2 mA for GSM/EDGE application, respectively. Because of a potentially large deviation of the RC-product due to process variations, quantized arrays of switchable capacitors are included. The capacitance value for the test chip is manually controlled by external pins and sample logic block until tolerance δ_{RC} of 40%.

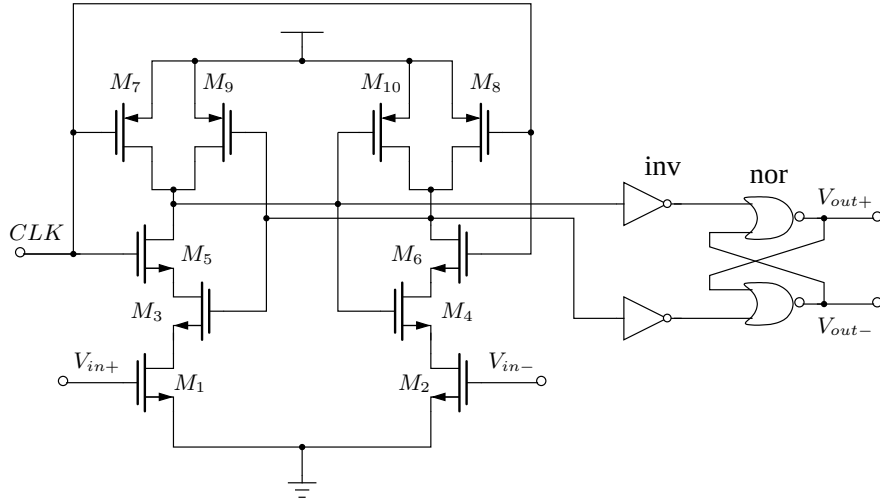


Figure 6.16.: Single-bit quantizer.

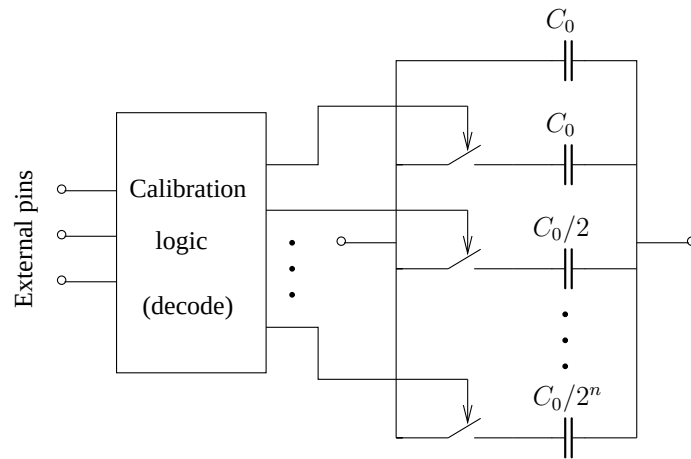


Figure 6.17.: Quantized capacitor array and calibration of RC-product.

6.4. Chip Implementation

For GSM/EDGE and GPS/Galileo applications, the test chips were designed in a $0.25\mu\text{m}$ CMOS technology based on the following rules:

- All analog blocks were clearly separated from the digital blocks on chip in order to prevent a crosstalk from digital circuits.
- All cross-couplings of the quadrature complex integrators and all compensation cross-coupling resistors are symmetrically placed between real and imaginary channels in order to reduce the mismatch. Especially, the integrating, cross-coupling and feedback DAC resistors of the first quadrature complex integrator were carefully designed with larger width.
- The pads of the positive and negative reference voltages were placed far away from the pads of the signal input and digital output. The pads for the sample clock were placed as near as possible to quantizers.

Figure 6.18 and Figure 6.19 show chip micrographs of designed 3rd-order CT-QBP $\Sigma\Delta\text{M}$ for GSM/EDGE low-IF receiver and 2nd-order CT-QBP $\Sigma\Delta\text{M}$ for GPS/Galileo low-IF receiver, respectively.

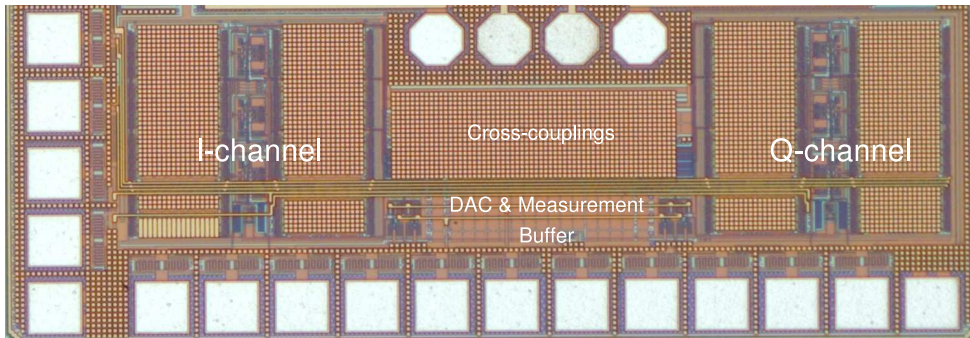


Figure 6.18.: Chip micrograph for GSM/EDGE low-IF receiver.

In this chapter, two design prototypes have been shown as examples; one is high resolution, medium bandwidth CT-QBP $\Sigma\Delta\text{M}$ for GSM/EDGE low-IF receiver, and the other is reconfigurable multimode wideband CT-QBP $\Sigma\Delta\text{M}$ for GPS/Galileo low-IF receiver. The modulator prototypes were designed by the CICFF topology proposed in Chapter 4 and design procedures conform to the inverse method proposed in Chapter 3. In order to ensure the proposed polyphase filters with CICFF topology and design methodology, the test chips were designed in a $0.25\mu\text{m}$ CMOS technology.

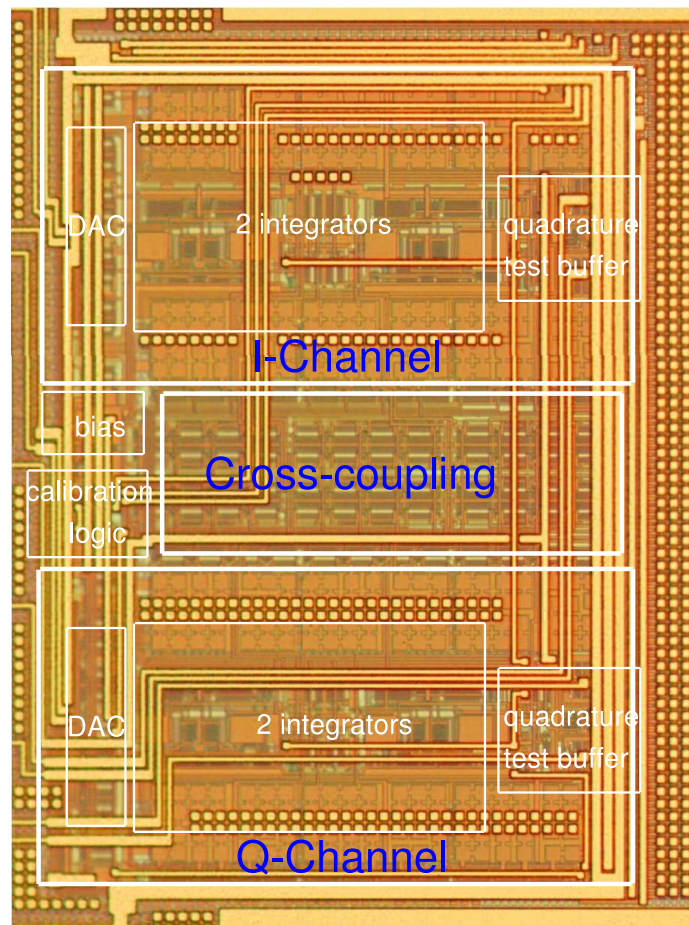


Figure 6.19.: Chip micrograph for GPS/Galileo low-IF receiver.

7. Measurement Results

This chapter presents measurement results of the test chips which were designed in $0.25\ \mu\text{m}$ CMOS technology for GSM/EDGE and GPS/Galileo applications. The measurement results demonstrate the effectiveness of the proposed CT-QBP $\Sigma\Delta$ Ms for low-IF receivers. .

7.1. Measurement Setup

Figure 7.1 shows the measurement setup used for CT-QBP $\Sigma\Delta$ modulator chip. A signal generator provides the quadrature input signals with common mode DC level and permissive minimum channel mismatch. The clock generator supplies sampling clocks of 26 MHz for GSM/EDGE and 125 MHz for GPS/Galileo with clock jitter variance of 5 ps. The quadrature single-bit-streams are transformed to the frequency domain by using the Fast Fourier Transformation (FFT) in the signal analyzer. The shaped noise spectrum is observed.

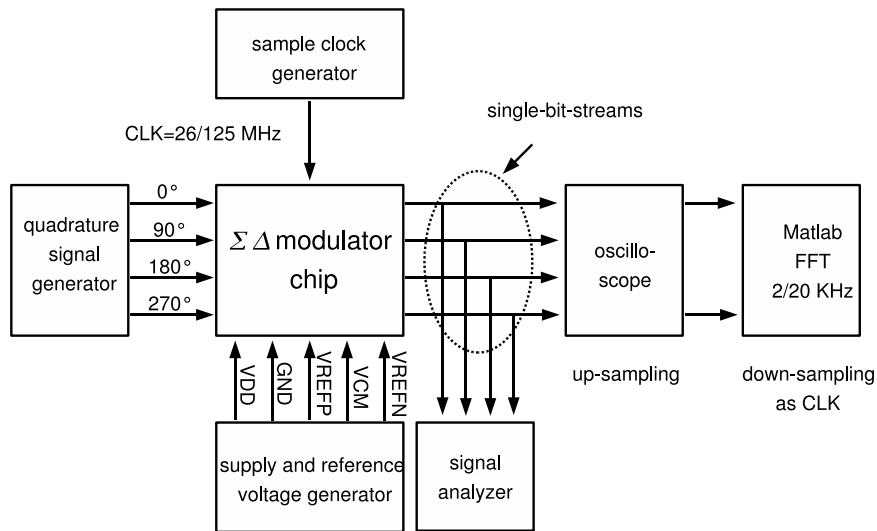


Figure 7.1.: Measurement setup.

The bit-streams of I/Q paths were upsampled on oscilloscope as $f_{ds} = 0.5\ \text{GSamples/s}$ in GSM/EDGE application and as $f_{ds} = 2.5\ \text{GSamples/s}$ in GPS/Galileo appli-

cation. The bit-streams of both I/Q paths are fed through the oscilloscope to a Matlab workstation in order to estimate the SNDR and input DR.

In Matlab, the input bit-streams which are upsampled in oscilloscope should be downsampled to sampling rate of $\Sigma\Delta$ modulator chip. Therefore downsample ratio is f_{ds}/f_s and the FFT resolutions on Matlab workstation are 2 kHz for GSM/EDGE and 20 kHz for GPS/Galileo. The process of bit-streams in Matlab workstation are as follows:

- Bit-streams of I/Q paths in oscilloscope is given as the input of workspace of Matlab.
- Levels of digital bit-streams valued between VDD and GND are shifted into +1 and -1. This implies that the shifted bit-stream has no DC value in FFT by introduced common mode DC level. But it should be noted that DC level in FFT always exists due to DC offset.
- Downsampling of the shifted bit-streams.
- Estimation in time domain. If the downsampled bit-streams of I/Q paths are different to the oscilloscope, by the use of a downsample calibration, the downsample processing is repeated until the downsampled bit-streams are the same as the oscilloscope.
- Transformation from downsampled bit-streams to complex bit-stream.
- FFT process of complex bit-stream in Hanning window.
- SNDR calculation.

7.2. Dynamic Range and SNDR

7.2.1. GSM/EDGE Application

The downsampled single bit-streams of the I/Q paths are shown in Figure 7.2 which were downsampled on Matlab workstation. They are similar to pulse-width modulator outputs of two signals with phase difference of 90 degree. The total number of the digital data which are downsampled with modulator sampling clock rate is 12500.

In order to ensure that second and third harmonic tones fall within the signal bandwidth of 200 kHz centered around 130 kHz, a quadrature sinusoid at 70 kHz with -3 dBFS was selected. Measurement results demonstrate a SFDR of 96.0 dB and an image rejection (IR) of 75.8 dB as shown in Figure 7.3. The SNDR of the designed chip was measured under the above conditions. These data demonstrate that input DR of 90.3 dB was achieved with a peak SNDR of 86.8 dB as shown Figure 7.4.

The measured power dissipation is less than 2.7 mW at 1.8 V supply voltage. In Table 7.1, the measured results are summarized.

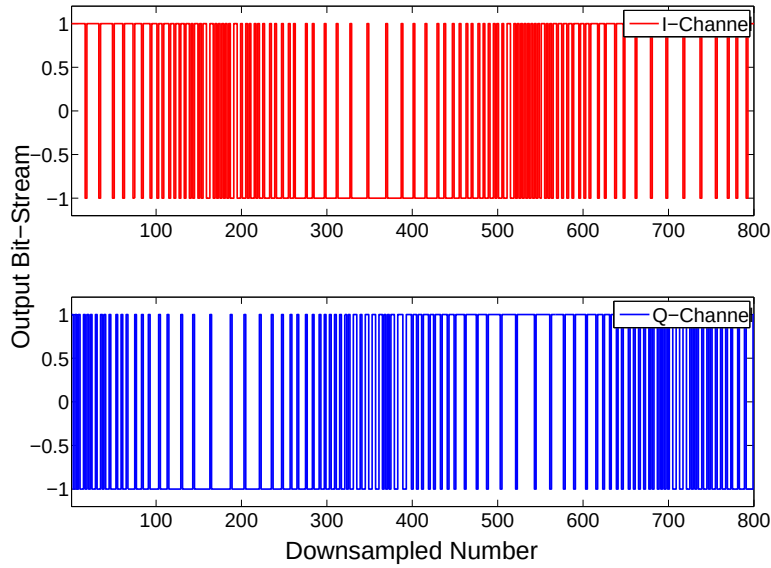
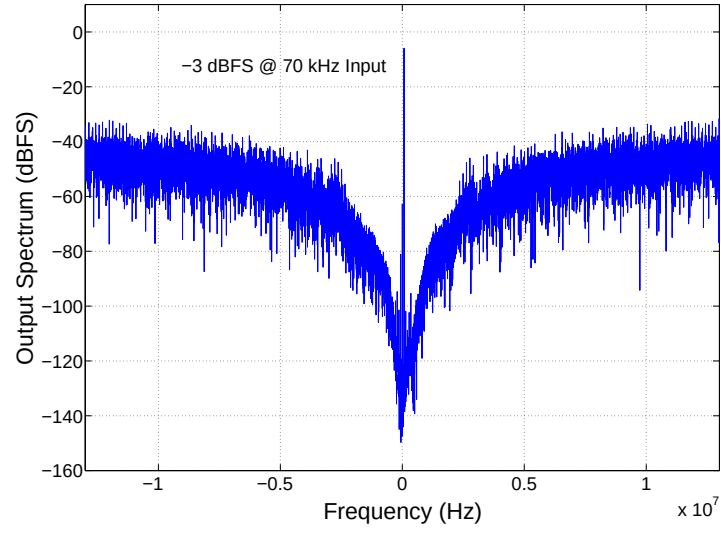


Figure 7.2.: Measured single bit-streams of the I/Q paths for GSM/EDGE.

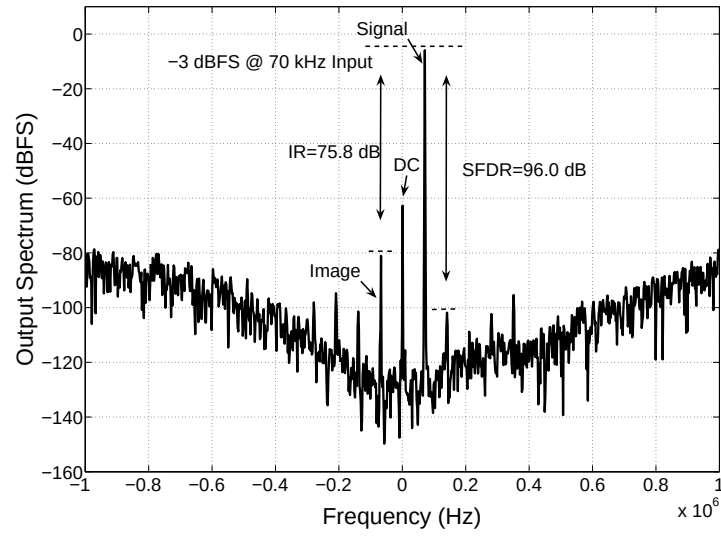
7.2.2. GPS/Galileo Application

All measurements were done in GPS and Galileo mode. In each mode, quadrature input signals with -3 dBFS at 4 MHz were applied to the chip. The sampling clock frequency was chosen to be 125 MHz. The bandwidth switch for GPS/Galileo is realized by integrating resistor and feedback resistors in the local feedback loop and the lossy integrators, as shown in Table 6.2. The bandwidth is tuned by switchable integrating capacitors and feedforward capacitors. The center frequency is tuned by switching the conventional cross-coupling and compensation cross-coupling resistor arrays, using digital calibration logic and external pins.

The single-bit I/Q channel output bit-streams are captured and upsampled by the oscilloscope. The bit-streams fed to the Matlab workstation are down-sampled by the sampling clock and analyzed using a 20 kHz FFT with a Hanning window. Figure 7.5 shows the output spectrum of the measured $\Sigma\Delta$ modulator for GPS/Galileo receiver. The measurement SNDR versus input level is shown in Figure 7.6. The designed modulator achieves a peak SNDR of 52.9dB for GPS and 48.4 dB for Galileo. It has a relatively high input dynamic range because the maximum stable input level increases due to the use of the lossy integrators. In Table 7.2, the measured results are summarized.



(a) $-0.5f_s \sim 0.5f_s$



(b) around passband

Figure 7.3.: Measured modulator output spectrum for GSM/EDGE

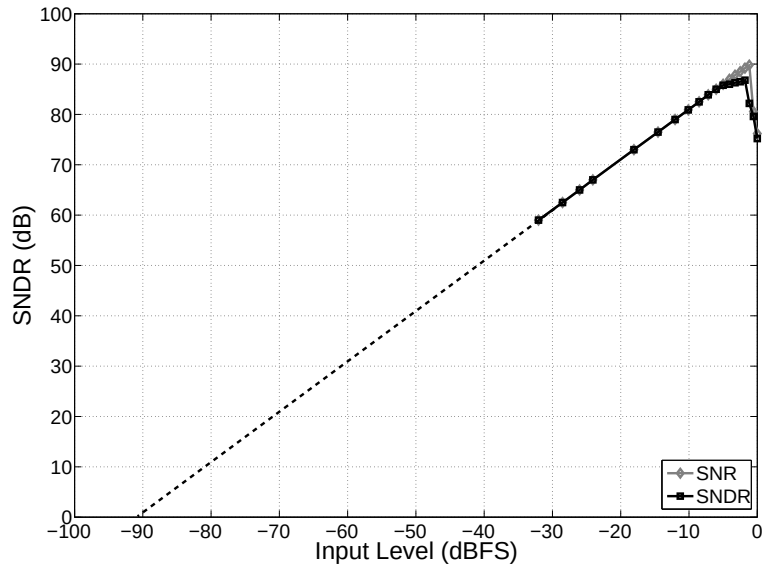


Figure 7.4.: SNDR vs. input signal level for GSM/EDGE.

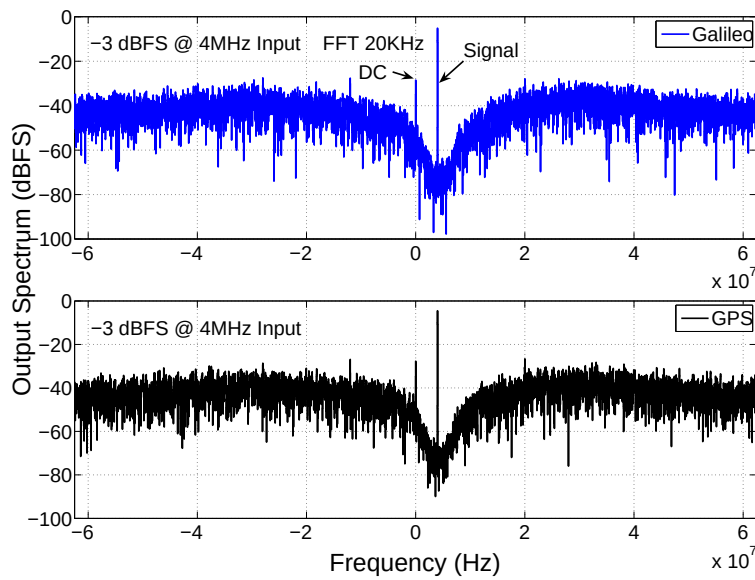


Figure 7.5.: Measured modulator output spectrum for GPS/Galileo.

Table 7.1.: IC Performance for GSM/EDGE

Parameters	Esfahani'03[EBRB03]	This work
Input IF/Bandwidth	-100 kHz/270 kHz	130 kHz/200 kHz
Peak SNDR	78.4 dB	86.8 dB
input DR	82.0 dB	90.3 dB
Image Rejection	57 dB @ mean	76 dB @ 70 kHz
Input Range	$2 V_{pp}$	$1.8 V_{pp}$
Power Dissipation	4.6 mW @ 2 V	2.7 mW @ 1.8 V
Technology	$0.25\mu m$ CMOS	$0.25\mu m$ CMOS
Chip area	$0.66 \times 0.59 mm^2$	$0.5 \times 1.4 mm^2$ (inc.pad)
FOM [EBRB03]	9.3×10^{15}	7.4×10^{16}

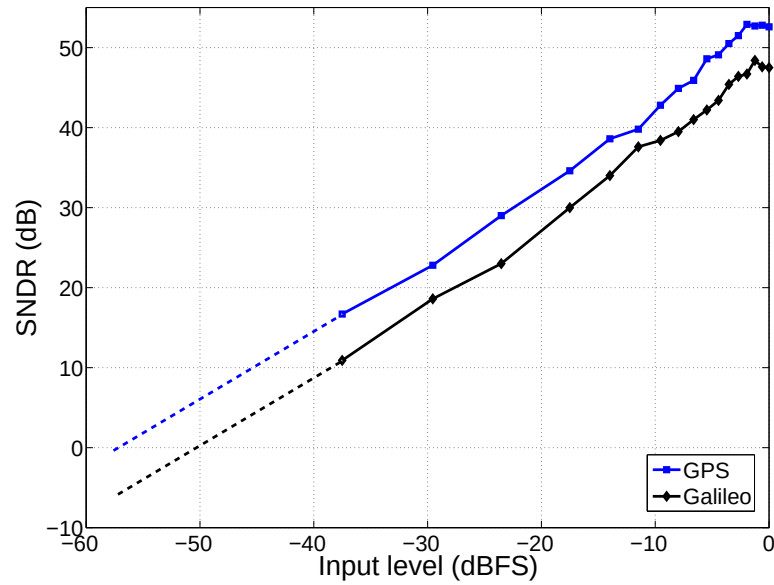


Figure 7.6.: SNDR vs. input signal level for GPS/Galileo.

Table 7.2.: IC Performance for GPS/Galileo

	Henkel'02	This design
Input IF	1 MHz	4.092 MHz
Bandwidth	1 MHz	2/4 MHz (GPS/Galileo)
Peak SNDR	56.7 dB@100 MHz	52.9/48.4 dB@125 MHz
input DR	63.8 dB@100 MHz	57.5/50.2 dB@125 MHz
Max.Input Signal	$2 V_{pp}$	$1.8 V_{pp}$
Image Rejection	≥ 40 dB	
Power Dissipation	21.8 mW @ 2.7 V	20.5 mW @ 1.8 V
Technology	$0.65\mu m$ BiCMOS	$0.25\mu m$ CMOS
Chip area	$2.1 \times 2.9 mm^2$ (inc.pad)	$0.37 \times 0.54 mm^2$ (core)

8. Conclusion

This work presents the implementation of the CT-QBP $\Sigma\Delta$ Ms for low-IF receivers. There are several integrated receiver architectures such as superheterodyne, zero-IF (Homodyne) and low-IF receiver. Superheterodyne architecture needs off-chip passive components which provide filters with a high- Q factor, increasing the cost and power consumption due to the extra signal buffering with off-chip components. The main weakness in zero-IF receiver is the DC offsets which are created during the downconversion. Because of this reason, the zero-IF receivers are more susceptible to disturbances arising from I/Q phase mismatches, nonlinearities and flicker noise than heterodyne designs. Low-IF receiver architecture is best suited in the wireless applications, because it is a technique which combines the advantages of the other two architectures. In the low-IF receiver using polyphase filter, the mirrored signal can be suppressed with the polyphase filter which is centered around IF. AD conversion based on RBP $\Sigma\Delta$ M or QBP $\Sigma\Delta$ M can be applied, but the 4-5 extra bit precision in case of RBP $\Sigma\Delta$ ADC is required more than that of QBP $\Sigma\Delta$ M.

Otherwise, CT $\Sigma\Delta$ Ms have become very popular in telecommunication applications over the last years, mainly due to some significant advantages over discrete-time implementations. They do not need anti-aliasing filters and enable high speed implementations due to relaxed sampling demands.

Therefore, in this work, the implementation of CT-QBP $\Sigma\Delta$ M have been focused. CT-QBP $\Sigma\Delta$ M is well suited for the use in low-IF receivers. It directly performs the AD conversion of complex analog I/Q signals in the signal band around IF and, therefore, reduces the problem of $1/f$ noise and DC offsets. In this case, a lower sampling frequency or a lower $\Sigma\Delta$ modulator order can be implemented resulting in lower power consumption and smaller chip area for the analog part.

In this work, firstly, the possible design methodologies have been defined and compared. The inverse method is desirable for the design of CT-QBP $\Sigma\Delta$ M. Starting from CT loop filter optimization, the equivalent noise shaping transfer function is finally calculated and its stability margin is estimated. Because of the optimization in the CT-domain, this method gives to designer lots of flexibilities for circuit design in the CT domain. When the ratio of the center frequency to the sampling frequency is not too much, using the real feedforward or feedback coefficients, the desirable SNR and stability margin can be obtained, while decreasing circuit complexity and chip area. In order to estimate the targeted modulator performances, the simulation method by Matlab code has been presented in Matlab. This is an extension of the Delta-Sigma Toolbox into the complex domain.

Next, the polyphase filter with CICFF topology have been proposed, starting from the consideration of the lowpass filter. CT-QBP $\Sigma\Delta$ M with the CICFF topology which is one of the CIFF topologies, is suited for low power and low voltage applications. Feedforward coefficients are implemented as the ratios of the feedforward capacitors to last integrating capacitor. The polyphase filters with the CICFF topology can be obtained by the conventional cross-couplings for moving poles to center frequency, and by the proposed compensation cross-couplings for moving zeros caused by capacitive feedforward, without extra active components. The compensation cross-couplings affects the modulator stability, especially for a higher center frequency.

The performance of CT-QBP $\Sigma\Delta$ Ms can be limited due to non-ideal effects such as finite GBW and DC gain, excess loop delay and mismatched loop delay, clock jitter, and DAC nonlinearity. In this work, the influence of the non-idealities have been summarized and their compensation or reduction solutions have been proposed.

Finite GBW of the amplifiers affect stability and translation (frequency shifting) to a wanted center frequency f_c of the polyphase filters. The lower GBW of the amplifier, the less is the stability of the complex integrators and the greater is the deviation from f_c depending on a selection of the integrating scales. It should be noted that the greater the center frequency, the less is the stability of the complex integrator. In order to ensure the stability, the use of a lossy complex integrator is desirable. The deviation from the center frequency can be decreased by inserting the transconductors in the virtual ground nodes of the amplifiers.

Excess loop delay seriously results in reducing the performance of the CT-QBP $\Sigma\Delta$ Ms, such as stability of the modulator and degradation of the SNR. In CT-QBP $\Sigma\Delta$ Ms, the effect of the excess loop delay increases with the center frequency. In order to compensate its effect, the additional feedback DAC with unit delay and the feedforward complex compensation coefficient can be used. Mismatch loop delay of the I/Q paths makes an aliased noise power in a passband and therefore results in SNR degradation, causing an extra feedback loop. For a lower center frequency, its effect significantly can be reduced. It can be completely compensated by using D-latches in the feedback paths and the compensation scheme for excess loop delay.

Clock jitter severely reduces the modulator performance. The closed-form formulas in CT-QBP $\Sigma\Delta$ M with NRZ feedback DAC pulse have been derived. The degradation of the SNR caused by clock jitter depends on the number of the output bit transitions. In order to reduce the jitter-induced noise, an optimized noise shaping transfer function which decreases the number of the bit transitions, and the modified feedback DAC analog waveforms were used to lowpass CT modulators can be applied.

The mismatch of the unit elements in the multibit DAC bank causes a nonlinear error of the modulator. In order to reduce the nonlinearity caused by DAC mismatch in QBP $\Sigma\Delta$ Ms, a complex mismatch shaping technique which is based on noise shaping can become a desirable solution. A first-order complex mismatch shaper have been proposed which is centered at any center frequency.

Two design prototypes have been shown as examples; one is high resolution, medium

bandwidth CT-QBP $\Sigma\Delta$ M for GSM/EDGE low-IF receiver, and the other is reconfigurable multimode wideband CT-QBP $\Sigma\Delta$ M for GPS/Galileo low-IF receiver. The modulator prototypes were designed by the CICFF topology and design procedures conform to the inverse method. The test chips were designed in a $0.25\mu\text{m}$ CMOS technology. For GSM/EDGE application, the measurement results demonstrate a SFDR of 96.0 dB and an image rejection (IR) of 75.8 dB at 70 kHz and -3 dBFS input signal. The DR of 90.3 dB was achieved with a peak SNDR of 86.8 dB. The measured power dissipation is less than 2.7 mW at 1.8 V supply voltage. For GPS/Galileo application, the designed modulator achieved a peak SNDR of 52.9dB for GPS and 48.4 dB for Galileo.

Bibliography

- [AAW⁺04] R. Ahola, A. Aktas, J. Wilson, K.R. Rao, F. Jonsson, I. Hyyrylainen, A. Brolin, T. Hakala, A. Friman, T. Makiniemi, J. Hanze, M. Sanden, D. Wallner, Yuxin Guo, T. Lagerstam, L. Noguer, T. Knuuttila, P. Olofsson, and M. Ismail. “A single-chip CMOS transceiver for 802.11a/b/g wireless LANs”. *Solid-State Circuits, IEEE Journal of*, 39(12):2250–2258, December 2004.
- [AIO02] Adiseno, M. Ismail, and H. Olsson. “A wide-band RF front-end for multiband multistandard high-linearity low-IF wireless receivers”. *Solid-State Circuits, IEEE Journal of*, 37(9):1162–1168, September 2002.
- [AKP⁺06] J. Arias, P. Kiss, V. Prodanov, V. Boccuzzi, M. Banu, D. Bisbal, J. S. Pablo, L. Quintanilla, and J. Barbolla. “A 32-mW 320-MHz continuous-time complex delta-sigma ADC for multi-mode wireless-LAN receivers”. *Solid-State Circuits, IEEE Journal of*, 41(2):339–351, February 2006.
- [AL04] H. Aboushady and M.-M. Louerat. “Loop delay compensation in band-pass continuous-time $\Sigma\Delta$ modulators without additional feedback coefficients”. In *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on, vol-1*, pages 1124–1127, May 2004.
- [AVG⁺07] A. Agah, K. Vleugels, P.B. Griffin, M. Ronaghi, J.D. Plummer, and B.A. Wooley. “A High-Resolution Low-Power Oversampling ADC with Extended-Range for Bio-Sensor Arrays”. In *VLSI Circuits, 2007 IEEE Symposium on*, pages 244–245, June 2007.
- [BAB90] J.E.C. Brown, M. Alexander, and D.F Bowers. “Mixed-mode simulation of a continuous-time $\Sigma\Delta$ ADC”. In *Circuits and Systems, 1990. ISCAS 1990. IEEE International Symposium on, vol-3*, pages 1915–1918, May 1990.
- [BFC⁺02] F. Behbahani, H. Firouzkouhi, R. Chokkalingam, S. Delshadpour, A. Kheirkhahi, M. Nariman, M. Conta, and S. Bhatia. “A fully integrated low-IF CMOS GPS radio with on-chip analog image rejection”.

- Solid-State Circuits, IEEE Journal of*, 37(12):1721–1727, December 2002.
- [BP98] A. Baccigalupi and M. Piscopo. “A variable sampling rate third order MASH $\Sigma\Delta$ modulator for measurement applications”. In *Instrumentation and Measurement Technology Conference, 1998. IMTC/98. Conference Proceedings. IEEE*, pages 1207–1210 vol.2, May 1998.
- [BvdZDH00] L.J. Breems, E.J. van de Zwan, E.C. Dijkmans, and J.H. Huijsing. “A 1.8 mW CMOS $\Sigma\Delta$ modulator with integrated mixer for A/D conversion of IF signals”. *Solid-State Circuits, IEEE Journal of*, 35(4):468–475, April 2000.
- [Can85] J. Candy. “A Use of Double Integration in Sigma Delta Modulation”. *Communications, IEEE Transactions on*, 33(3):249–258, March 1985.
- [CJ06] T.C. Caldwell and D.A. Johns. “A time-interleaved continuous-time $\Delta\Sigma$ modulator with 20-MHz signal bandwidth”. *Solid-State Circuits, IEEE Journal of*, 41(7):1578–1588, July 2006.
- [CKE06] F. Chen, T. Kuendiger, and S. Erfani. “Compensation of Finite GBW Induced Performance Loss on a Fifth-order Continuous-time Sigma-Delta Modulator”. In *Electrical and Computer Engineering, 2006. CCECE '06. Canadian Conference on*, pages 533–536, May 2006.
- [CS98a] J.A. Cherry and W.M. Snelgrove. “Loop delay and jitter in continuous-time delta sigma modulators”. In *Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 International Symposium on, vol-1*, pages 596–599, May 1998.
- [CS98b] J. Crols and M.S.J. Steyaert. “Low-IF topologies for high-performance analog front ends of fully integrated receivers”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 45(3):269–282, March 1998.
- [CS99a] J.A. Cherry and W.M. Snelgrove. “Clock jitter and quantizer metastability in continuous-time delta-sigma modulators”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 46(6):661–676, June 1999.
- [CS99b] J.A. Cherry and W.M. Snelgrove. “Excess loop delay in continuous-time delta-sigma modulators”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 46(4):376–389, April 1999.

- [CWW07] Baoyong Chi, Zhihua Wang, and S.S. Wong. “A Superheterodyne Receiver Front-End With On-Chip Automatically Q-Tuned Notch Filters”. In *Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE*, pages 21–24, June 2007.
- [DKG⁺05] L. Dörrer, F. Kuttner, P. Greco, P. Torta, and T. Hartig. “A 3-mW 74-dB SNR 2-MHz continuous-time delta-sigma ADC with a tracking ADC quantizer in 0.13- μ m CMOS”. *Solid-State Circuits, IEEE Journal of*, 40(12):2416–2427, December 2005.
- [dlREPV⁺05] J.M. de la Rosa, S. Escalera, B. Pérez-Verdú, F. Medeiro, O. Guerra, R. del Río, and A. Rodríguez-Vázquez. “A CMOS 110-dB@40-kS/s programmable-gain chopper-stabilized third-order 2-1 cascade sigma-delta Modulator for low-power high-linearity automotive sensor ASICs”. *Solid-State Circuits, IEEE Journal of*, 40(11):2246–2264, November 2005.
- [dRdlRPV⁺04] R. del Río, J.M. de la Rosa, B. Pérez-Verdú, M. Delgado-Restituto, R. Domínguez-Castro, F. Medeiro, and A. Rodríguez-Vázquez. “Highly linear 2.5-V CMOS $\Sigma\Delta$ modulator for ADSL+”. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 51(1):47–62, January 2004.
- [DvRL02] K. Doris, A. van Roermund, and D. Leenaerts. “DAC compensation for continuous-time delta-sigma modulators”. In *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on, vol-1*, pages 117–120, May 2002.
- [EBRB03] F. Esfahani, P. Basedau, R. Ryter, and R. Becker. “A fourth-order continuous-time complex sigma-delta ADC for low-IF GSM and EDGE receivers”. In *VLSI Circuits, 2003. Digest of Technical Papers. 2003 Symposium on*, pages 75–78, June 2003.
- [Fau02] M. Faulkner. “DC offset and IM2 removal. in. direct conversion. receivers”. *Communications, IEE Proceedings on*, 149(3):179–184, June 2002.
- [FWG01] E. Fogelman, J. Welz, and I. Galton. “An audio ADC Delta-Sigma modulator with 100-dB peak SINAD and 102-dB DR using a second-order mismatch-shaping DAC”. *Solid-State Circuits, IEEE Journal of*, 36(3):339–348, March 2001.
- [Gal97] I. Galton. “Spectral shaping of circuit errors in digital-to-analog converters”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 44(10):808–817, October 1997.

- [Gar86] F Gardner. “A Transformation for Digital Simulation of Analog Filters”. *Communications, IEEE Transactions on*, 34(7):676–680, July 1986.
- [GMPMOG08] A. Gimeno-Martin, J.M. Pardo-Martin, and F.J. Ortega-Gonzalez. “Adaptive algorithm for increasing image rejection ratio in low-IF receivers”. *Electronics Letters*, 44(6):447–448, March 2008.
- [Gro08] J. Groe. “A Multimode Cellular Radio”. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 55(3):269–273, March 2008.
- [GS98] W. Gao and W.M. Snelgrove. “A 950-MHz IF second-order integrated LC bandpass delta-sigma modulator”. *Solid-State Circuits, IEEE Journal of*, 33(5):723–732, May 1998.
- [GSS97] W. Gao, O. Shoaie, and W.M. Snelgrove. “Excess loop delay effects in continuous-time delta-sigma modulator and the compensation solution”. In *Circuits and Systems, 1997. IEEE International symposium on, vol-1*, pages 65–68, June 1997.
- [HK00] A.I. Hussein and W.B. Kuhn. “Bandpass $\Sigma\Delta$ modulator employing undersampling of RF signals for wireless communication”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 47(7):614–620, July 2000.
- [HL03] F. Henkel and U. Langmann. “Excess loop delay effects in continuous-time quadrature bandpass sigma-delta modulators”. In *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on, vol-1*, pages 1029–1032, May 2003.
- [HL07] H.-Y. Hsieh and L. Lin. “A First-Order Tree-Structured DAC With Reduced Signal-Band Noise”. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 54(5):392–396, May 2007.
- [HLH⁺02] F. Henkel, U. Langmann, A. Hanke, S. Heinen, and E. Wagner. “A 1-MHz-bandwidth second-order continuous-time quadrature bandpass sigma-delta modulator for low-IF radio receivers”. *Solid-State Circuits, IEEE Journal of*, 37(12):1628–1635, December 2002.
- [Hor90] U. Horbach. “Design of a 20 bit sigma-delta A/D-converter for audio applications”. In *Circuits and Systems, 1990. ISCAS 1990. IEEE International Symposium on, vol-1.4*, pages 2789–2792, May 1990.
- [HPW06] L. Hernández, S. Patón, and A. Wiesbauer. “Spectral shaping of clock jitter errors for continuous time sigma-delta modulators”. In *Circuits*

- and Systems, 2006. ISCAS 2006. The 2006 IEEE International Symposium on*, pages 2013–2016, May 2006.
- [HWPDG04] L. Hernández, A. Wiesbauer, S. Patón, and A. Di Giandomencio. “Modelling and optimization of low pass continuous-time sigma delta modulators for clock jitter noise reduction”. In *Circuits and Systems, 2004. ISCAS 2004. IEEE International Symposium on, vol-1*, pages 1072–1075, May 2004.
- [JF04] Ruoxin Jiang and T.S. Fiez. “A 14-bit delta-sigma ADC with $8\times$ OSR and 4-MHz conversion bandwidth in a $0.18\text{-}\mu\text{m}$ CMOS process”. *Solid-State Circuits, IEEE Journal of*, 39(1):63–74, January 2004.
- [JKH07] S. Joeres, Song-Bok Kim, and S. Heinen. “Simulation of quadrature-bandpass Sigma-Delta analog to digital converters using state space descriptions”. In *Circuit Theory and Design, 2007. ECCTD 2007. 18th European Conference on*, pages 886–889, August 2007.
- [JMS97] S.A. Jantzi, K.W. Martin, and A.S. Sedra. “Quadrature bandpass $\Sigma\Delta$ modulation for digital radio”. *Solid-State Circuits, IEEE Journal of*, 32(12):1935–1950, December 1997.
- [JXC08] Heng-Yu Jian, Zhiwei Xu, and M.-C.F. Chang. “Delta-Sigma D/A Converter Using Binary- Weighted Digital-to-Analog Differentiator for Second-Order Mismatch Shaping”. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 55(1):6–10, January 2008.
- [Kap03] M. S. Kappes. “A 2.2-mW CMOS bandpass continuous-time multibit $\Sigma\Delta$ with 68 dB of dynamic range and 1-MHz-bandwidth for wireless applications”. *Solid-State Circuits, IEEE Journal of*, 38(7):1098–1104, July 2003.
- [KJH07] Song-Bok Kim, S. Joeres, and S. Heinen. “A compensation method of the excess loop delay in continuous-time complex sigma-delta modulators”. In *Circuit Theory and Design, 2007. ECCTD 2007. 18th European Conference on*, pages 140–143, August 2007.
- [KJN⁺08] A. Kruth, S. Joeres, A. Neryer, M. Robens, H. Erkens, Song-Bok Kim, D. Bormann, T. D. Werth, R. Zimmermann, N. Wunderlich, and S. Heinen. “A Multimode Shared RF Low-Power Receiver Front-End Architecture for Satellite Based Navigation in 90 nm CMOS”. *Workshop Analog’08*, pages 19–24, April 2008.
- [KJWH08a] Song-Bok Kim, S. Joeres, R. Wunderlich, and S. Heinen. “A 2.7-mW, 90.3-dB DR Continuous-Time Quadrature Bandpass Sigma-Delta

- Modulator for GSM/EDGE Low-IF Receiver in 0.25- μ m CMOS”. *Solid-State Circuits, IEEE Journal of*, accepted, 2008.
- [KJWH08b] Song-Bok Kim, S. Joeres, R. Wunderlich, and S. Heinen. “Complex Mismatch Shaper for Tree-Structured DAC in Multi-Bit Complex Sigma-Delta Modulators”. In *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on*, pages 328–331, August 2008.
- [KJWH08c] Song-Bok Kim, S. Joeres, R. Wunderlich, and S. Heinen. “Continuous-Time Quadrature Bandpass Sigma-Delta Modulator with Capacitive Feedforward Summation for GSM/EDGE Low-IF Receiver”. In *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on*, pages 438–441, August 2008.
- [KJZ+07] Song-Bok Kim, S. Joeres, N. Zimmermann, M. Robens, R. Wunderlich, and S. Heinen. “Continuous-time quadrature bandpass sigma-delta modulator for GPS/Galileo low-IF receiver”. In *Radio-Frequency Integration Technology, 2007. RFIT 2007. IEEE International Workshop on*, pages 127–130, December 2007.
- [KRJ+08] Song-Bok Kim, M. Robens, S. Joeres, R. Wunderlich, and S. Heinen. “A Polyphase Filter Design for Continuous-Time Quadrature Bandpass Sigma-Delta Modulators”. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 55(11):3457–3468, November 2008.
- [KWJ+08] Song-Bok Kim, T. D. Werth, S. Joeres, R. Wunderlich, and S. Heinen. “Effect of Mismatched Loop Delay in Continuous-Time Complex Sigma-Delta Modulators”. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 55(10):996–1000, October 2008.
- [LL02] S. Luschas and Hae-Seung Lee. “High-speed $\Sigma\Delta$ modulators with reduced timing jitter sensitivity”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 49(11):712–720, November 2002.
- [LLM+06] K. Lim, S.-H. Lee, S. Min, S. Ock, M.-W. Hwang, C.-H. Lee, K.-L. Kim, and S. Han. “A Fully Integrated Direct-Conversion Receiver for CDMA and GPS Applications”. *Solid-State Circuits, IEEE Journal of*, 41(11):2408–2416, November 2006.
- [Mar04] K.W. Martin. “Complex signal processing is not complex”. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 51(9):1823–1836, September 2004.

-
- [MLD⁺08] P. Martel, G. Lossois, C. Danchesi, D. Brunel, and L. Noel. “Experimental investigations on BER degradations due to analogue channel filtering in zero-IF receivers for FDD WCDMA”. *Electronics Letters*, 44(2):138–139, January 2008.
- [MP05] R. Maurino and C. Papavassiliou. “Quadrature $\Sigma\Delta$ modulators with a dynamic element matching scheme”. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 52(11):771–775, November 2005.
- [MPJ⁺08] A. Maxim, R. Poorfard, R. Johnson, P. Crawley, J. Kao, Z. Dong, M. Chennam, D. Trager, and M. Reid. “A single-chip digitally enhanced radio receiver for DBS satellite TV applications”. In *Radio and Wireless Symposium, 2008 IEEE*, pages 787–790, January 2008.
- [MPSS98] A. Marques, V. Peluso, M.S. Steyaert, and W.M. Sansen. “Optimal parameters for $\Sigma\Delta$ modulator topologies”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 45(9):1232–1241, September 1998.
- [MPVRV99] F. Medeiro, B. Pérez-Verdú, and A. Rodríguez-Vázquez. “A 13-bit, 2.2-MS/s, 55-mW multibit cascade $\Sigma\Delta$ modulator in CMOS 0.7- μ m single-poly technology”. *Solid-State Circuits, IEEE Journal of*, 34(6):748–760, June 1999.
- [NST96] S. R. Norsworthy, R. Schreier, and G. C. Temes. *Delta-Sigma Data Converters: Theory, Design and Simulation*. Wiley-IEEE Press, New York, 1996.
- [OA98] O. Oliaei and H. Aboushady. “Jitter effects in continuous-time $\Sigma\Delta$ modulators with delayed return-to-zero feedback”. In *Electronics, Circuits and Systems, 1998 IEEE International Conference on, vol.1*, pages 351–354, September 1998.
- [OG06] M. Ortmans and F. Gerfers. *Continuous-time Sigma-Delta A/D Conversion: Fundamentals, Performance Limits and Robust Implementations*. Springer, Berlin Heidelberg, 2006.
- [OGM03a] M. Ortmanns, F. Gerfers, and Y. Manoli. “A continuous-time sigma-delta modulator with switched capacitor controlled current mode feedback”. In *Solid-State Circuits Conference, 2003. ESSCIRC 2003. Proceedings of the 29th European*, pages 249–252, September 2003.
- [OGM03b] M. Ortmanns, F. Gerfers, and Y. Manoli. “Fundamental limits of jitter insensitivity in discrete and continuous-time sigma delta modulators”.

- In *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol.1, pages 1037–1040, September 2003.
- [OGM03c] M. Ortmanns, F. Gerfers, and Y. Manoli. “Influence of finite integrator gain bandwidth on continuous-time sigma delta modulators”. In *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol.1, pages 925–928, May 2003.
- [OGM04] M. Ortmanns, F. Gerfers, and Y. Manoli. “Compensation of finite gain-bandwidth induced errors in continuous-time sigma-delta modulators”. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 51(6):1088–1099, June 2004.
- [OGM05a] M. Ortmanns, F. Gerfers, and Y. Manoli. ‘A Case Study on a 2-1-1 Cascaded Continuous-Time Sigma-Delta Modulator’. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 52(8):1515–1525, August 2005.
- [OGM05b] M. Ortmanns, F. Gerfers, and Y. Manoli. “A continuous-time $\Sigma\Delta$ modulator with reduced sensitivity to clock jitter through SCR feedback”. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 52(5):875–884, May 2005.
- [OGM06] M. Ortmanns, F. Gerfers, and Y. Manoli. “Clock jitter insensitive continuous-time $\Sigma\Delta$ modulators”. In *Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE International Conference on*, vol-2, pages 1049–1052, September 2006.
- [Oli01] O. Oliaei. “Continuous-time sigma-delta modulator with an arbitrary feedback waveform”. In *Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on*, vol.1, pages 292–295, May 2001.
- [Oli03] O. Oliaei. “State-space analysis of clock jitter in continuous-time oversampling data converters”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 50(1):31–37, January 2003.
- [OMG02] M. Ortmanns, Y. Manoli, and F. Gerfers. “A continuous-time $\Sigma\Delta$ modulator with reduced jitter sensitivity”. In *Solid-State Circuits Conference, 2002. ESSCIRC 2002. Proceedings of the 28th European*, pages 287–290, September 2002.
- [PDGH⁺04] S. Patón, A. Di Giandomenico, L. Hernández, A. Wiesbauer, T. Pötscher, and M. Clara. “A 70-mW 300-MHz CMOS continuous-time $\Sigma\Delta$ ADC with 15-MHz bandwidth and 11 bits of resolution”.

-
- Solid-State Circuits, IEEE Journal of*, 39(7):1056–1063, September 2004.
- [PNR⁺04] K. Philips, P.A.C.M. Nuijten, R.L.J. Roovers, A.H.M. van Roermund, F.M. Chavero, M.T. Pallares, and A. Torralba. “A continuous-time $\Sigma\Delta$ ADC with increased immunity to interferers”. *Solid-State Circuits, IEEE Journal of*, 39(12):2170–2178, December 2004.
- [Raz01] B. Razavi. “A 5.2-GHz CMOS receiver with 62-dB image rejection”. *Solid-State Circuits, IEEE Journal of*, 36(5):810–815, May 2001.
- [RCRW06a] S. Reekmans, B. Catteau, P. Rombouts, and L. Weyten. “Quadrature Mismatch Shaping with a Complex, Data Directed Swapper”. In *Electronics, Circuits and Systems, 2006. ICECS '06. 13th IEEE International Conference on*, pages 46–49, December 2006.
- [RCRW06b] S. Reekmans, B. Catteau, P. Rombouts, and L. Weyten. “Quadrature mismatch shaping with a complex, tree structured DAC”. In *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, pages 2969–2972, May 2006.
- [RDMRW05] S. Reekmans, J. De Maeyer, P. Rombouts, and L. Weyten. “Improved design method for continuous-time quadrature bandpass $\Sigma\Delta$ ADCs”. *Electronics Letters*, 41(8):461–463, April 2005.
- [RDMRW06] S. Reekmans, J. De Maeyer, P. Rombouts, and L. Weyten. “Quadrature Mismatch Shaping for Digital-to-Analog Converters”. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 53(12):2529–2538, December 2006.
- [RE02] J. Riches and N. Erdol. “Mismatch cancellation in quadrature bandpass $\Delta\Sigma$ modulators using an error shaping technique”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 49(2):73–85, February 2002.
- [RFP⁺06] S. K. Reynolds, B. A. Floyd, U. R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer. “A Silicon 60-GHz Receiver and Transmitter Chipset for Broadband Communications”. *Solid-State Circuits, IEEE Journal of*, 41(12):2820–2831, December 2006.
- [RP06] K. Reddy and S. Pavan. “Fundamental limitations of continuous-time delta-sigma modulators due to clock jitter”. In *Circuits and Systems, 2006. ISCAS 2006. IEEE International Symposium on*, pages 2021–2024, May 2006.

- [Sch02] R. Schreier. “Quadrature mismatch-shaping”. In *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on, vol.4*, pages 675–678, May 2002.
- [SDRP04] M. Schimper, L. Dörrer, E. Riccio, and G. Panov. “A 3mW continuous-time $\Sigma\Delta$ -modulator for EDGE/GSM with high adjacent channel tolerance”. In *Solid-State Circuits Conference, 2004. ESSCIRC 2004. Proceeding of the 30th European*, pages 183–186, September 2004.
- [SKKK04] H. San, H. Kobayashi, S. Kawakami, and N. Kuroiwa. “An element rotation algorithm for multi-bit DAC nonlinearities in complex band-pass $\Sigma\Delta$ AD modulators”. In *VLSI Design, 2004. Proceedings. 17th International Conference on*, pages 151–156, January 2004.
- [SS04] H. Shamsi and O. Shoaie. “Return to-zero feedback insertion in a continuous time Delta-Sigma modulator for excess loop delay compensation”. *IEICE Electronics Express*, 1(18):568–574, December 2004.
- [SSH99] Tao Shui, R. Schreier, and F. Hudson. “Mismatch shaping for a current-mode multibit delta-sigma DAC”. *Solid-State Circuits, IEEE Journal of*, 34(3):331–338, March 1999.
- [ST04] R. Schreier and G. C. Temes. *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, New York, 2004.
- [SZ95] R. Schreier and B. Zhang. “Noise-shaped multibit D/A convertor employing unit elements”. *Electronics Letters*, 31(20):1712–1713, September 1995.
- [SZ96] R. Schreier and B. Zhang. “Delta-sigma modulators employing continuous-time circuitry”. *Circuits and Systems I: Fundamental Theory and Application, IEEE Transactions on*, 43(4):324–332, April 1996.
- [TC05] Kei-Tee Tiew and Yuan Chen. “DAC compensation for continuous-time delta-sigma modulators”. In *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on, vol.4*, pages 3680–3683, May 2005.
- [TMRPW03] B.K. Thandri, J.S. Martinez, J.M. Rocha-Perez, and J. Wang. “A 92MHz, 80dB peak SNR SC bandpass $\Sigma\Delta$ modulator based on a high GBW OTA with no Miller capacitors in 0.35/ μ m CMOS technology”. In *Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003*, pages 21–24, September 2003.

- [TTK99] Hai Tao, L. Tóth, and J.M. Khoury. “Analysis of timing jitter in bandpass sigma-delta modulators”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 46(8):991–1001, August 1999.
- [Vad04] M. Vadipour. “A bandpass mismatch noise-shaping technique for $\Sigma\Delta$ modulators”. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 51(3):130–135, March 2004.
- [VS08] M. B. Vahidfar and O. Shoaie. “A High IIP2 Mixer Enhanced by a New Calibration Technique for Zero-IF Receivers”. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 55(3):219–223, March 2008.
- [WG02] J. Welz and I. Galton. “Necessary and sufficient conditions for mismatch shaping in a general class of multibit DACs”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 49(12):748–759, December 2002.
- [WGF01] J. Welz, I. Galton, and E. Fogleman. “Simplified logic for first-order and second-order mismatch-shaping digital-to-analog converters”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 48(11):1014–1027, November 2001.
- [YS99] L. Yu and W.M. Snelgrove. “A novel adaptive mismatch cancellation system for quadrature IF radio receivers”. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 46(6):789–800, June 1999.
- [YS04] S. Yan and E. S. Sinencio. “A continuous-time $\Sigma\Delta$ modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth”. *Solid-State Circuits, IEEE Journal of*, 39(1):75–86, January 2004.
- [ZTJ⁺04] M. Zargari, M. Terrovitis, S.H.-M. Jen, B.J. Kaczynski, MeeLan Lee, M.P. Mack, S.S. Mehta, S. Mendis, K. Onodera, H. Samavati, W.W. Si, K. Singh, A. Tabatabaei, D. Weber, D.K. Su, and B.A. Woolley. “A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/g wireless LAN”. *Solid-State Circuits, IEEE Journal of*, 39(12):2239–2249, December 2004.

A. Appendix

A.1. Abbreviations

Abbreviation	Meaning
4G	Fourth generation of mobile communication
AC	Alternating Current
ADC	Analog-to-Digital Converter
CICFF	Chain of Integrators with Capacitive FeedForward summation
CIFB	Chain of Integrators with distributed FeedBack
CIFF	Chain of Integrators with weighted FeedForward summation
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous Time
DAC	Digital-to-Analog Converter
DC	Direct Current
DR	Dynamic Range
DSP	Digital Signal Processor
DT	Discrete Time
DWA	Data-Weighted Average
EDGE	Enhanced Data for Global Evolution
ESL	Element Selection Logic
FFT	Fast Fourier Transformation
f_B	Bandwidth
f_c	Center Frequency (Intermediate Frequency)
f_s	Sampling Frequency
GBW	Gain BandWidth product
GPS	Global Positioning System
GSM	Global System for Mobile communication
HRZ	Half delayed RZ
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
MASH	Multi-stage noise SHaping

MMC	Mobile Multimedia Communication
MOSFET	Metal oxide semiconductor field effect transistor
MTF	Mismatch Transfer Function
NRZ	Non-Return-to-Zero
NTF	Noise shaping Transfer Function
OSR	OverSampling Ratio
OpAmp	Operational Amplifier
PDA	Personal Digital Assistant
PWM	Pulse-Width Modulation
QBP	Quadrature BandPass
RBP	Real BandPass
RF	Radio Frequency
RZ	Return-to-Zero
SAW	Surface Acoustic Wave
$\Sigma\Delta$ M	Sigma-Delta Modulator
SC	Switched Capacitor
SNDR	Signal-to-Noise plus Distortion Ratio
SNR	Signal-to-Noise Ratio
SFDR	Spurious Free Dynamic Range
STF	Signal Transfer Function
UMTS	Universal Mobile Telecommunications System
WCDMA	Wideband Code Division Multiple Access

A.2. Subroutine List

```

-----
function [ HPPF, pnum,pden] = CTpolypassfilter()
%%%%% modulator parameters %%%%%%%%%%%%%%
a1=9.0e6; a2=9.0e6; %/ integrator scales
k1=1;k2=1;          %/ feedforward coefficients
b1=0.04;            %/ feedback coefficient for optimized zero
%%%%% Transfer function %%%%%%%%%%%%%%
pnum=[k1*a1 -j*wc*k1*a1+k2*a1*a2];
pden=[1 -2*j*wc -wc^2+a1*a2*b1];
HPPF=tf(pnum,pden);
-----

```

```

-----
function [ HDT ] = DTFunc( sk1,sk2, A1,A2, alpha,beta, Ts)
zk1 = exp(sk1*Ts);
zk2 = exp(sk2*Ts);
y01=zk1^(1-alpha)-zk1^(1-beta);
y02=zk2^(1-alpha)-zk2^(1-beta);
P1= A1*y01*(1/sk1);
P2= A2*y02*(1/sk2);
numer=[0 P1+P2 -(P1*zk2+P2*zk1)];
denom=[1 -(zk1+zk2) (-zk1)*(-zk2)];
HDT=tf(numer, denom, 0.1);
-----

```

```

-----
function CTBodeplot(TF,BW)
f = linspace(-BW, BW,10000);
om=2*pi*f;
s = sqrt(-1)*om;
[b,a]=tfdata(TF,'v');
hs = (polyval((b),s)./polyval((a),s));
subplot(2,1,1);
plot(f, dBV(hs),'g');
ylabel('Magnitude (dB)')
hold on;
subplot(2,1,2);
plot(f, 180/pi*angle(hs),'b');
xlabel('Frequency (Hz)')
ylabel('Phase')
hold on;
-----

```

```

-----
function DTBodeplot(TF,BW,Ts)
f = linspace(-BW, BW,100000);

```

```

om=2*pi*f;
s = sqrt(-1)*om;
[b,a]=tfdata(TF,'v');
z = exp(s*Ts);
hs = (polyval((b),z)./polyval((a),z));
subplot(2,1,1);
plot(f, dBV(hs),'g');
plot(f, (hs),'g');
ylabel('Magnitude (dB)')
hold on;
subplot(2,1,2);
plot(f, 180/pi*angle(hs),'b');
xlabel('Frequency (Hz)')
ylabel('Phase')
hold on;
-----
function NTF_PZ(H,color,markersize,list)
if nargin < 4
    list = 0;
    if nargin < 3
markersize = 5;
if nargin < 2
    color = 'b';
end
end
end
if iscell(color)
    pole_fmt = [color{1} 'x'];
    zero_fmt = [color{end} 'o'];
else
    pole_fmt = [color 'x'];
    zero_fmt = [color 'o'];
end
pp = plot(real(p),imag(p),pole_fmt);
set(pp,'markersize',markersize);
if ~isempty(z)
    hold_status = ishold;
    if ~hold_status; hold on; end;
    zz = plot(real(z),imag(z),zero_fmt);
    set(zz,'markersize',markersize);
    if ~hold_status; hold on; end;
end
end

```

```
% Draw unit circle, real axis and imag axis
hold_status = ishold;
hold on
plot(exp(j*2*pi*(0:0.01:1)));
axis('equal');
set(gcf,'NumberTitle','off');
set(gcf,'Name','PZ');
set(gca,'FontSize', 11);
set(gca, 'Box', 'on');
limits = axis;
plot([0 0],limits(3:4),'k:',limits(1:2),[0 0],'k:')
xlabel('Real')
ylabel('Image')
-----

function [v] = PPFsimulateDSM_RjQ(H,G,u,N,nlev)
% simulates a closed loop Sigma Delta Modulator
% with the transfer function noise shaping H, G
%  $Y(z)=[G(z)*X(z)+E(z)]/(1+Hppf(z)$ 
[HNum,HDen]=tfdata(H,'v'); % split into numerator and denominator
[GNum,GDen]=tfdata(G,'v'); % split into numerator and denominator
[HNum,HDen]=eqtflength(HNum,HDen);
[GNum,GDen]=eqtflength(GNum,GDen);
[A,B,C,D]=tf2ss(HNum,HDen); % create complex ABCD Matrix
[GA,GB,GC,GD]=tf2ss(GNum,GDen); % create complex ABCD Matrix
order=length(A);
nx=zeros(order,1); % initialize state vectors for speedup
order=length(GA);
sx=zeros(order,1); % initialize state vectors for speedup
v(1:N)=0;
for i=1:N
    sy=GC*sx + GD*u(i);
    ny=C*nx + D*v(i);
    y=sy - ny;
    [v(i)] = PPFds_quantize_complex(y,nlev);
    nx = A * nx + B * v(i);
    sx = GA * sx + GB * u(i);
end
-----

function [v] = PPFds_quantize_complex(y,n)
if nargin<2
    n=2;
end
```

```

yre=real(y); yim=imag(y);

if rem(n,2)==0 % mid-rise quantizer
    vre = 2*floor(0.5*yre)+1;
    vim = 2*floor(0.5*yim)+1;
else % mid-tread quantizer
    vre = 2*floor(0.5*(yre+1));
    vim = 2*floor(0.5*(yim+1));
end
% Limit the output
L = n-1;
i = vre>L;
if any(i)
    vre(i) = L(ones(size(vre(i)))));
end
i = vre<-L;
if any(i)
    vre(i) = -L(ones(size(vre(i)))));
end
L = n-1;
i = vim>L;
if any(i)
    vim(i) = L(ones(size(vim(i)))));
end
i = vim<-L;
if any(i)
    vim(i) = -L(ones(size(vim(i)))));
end
v=vre+j*vim; % return complex output
-----
function snr = PPFplotdsmsnr(v,u,N,fctest,fcnorm,fB,R)
t = 0:200;
figure(10); clf; hold on;
subplot(3,1,1);
stairs(t,u(t+1),'r');
subplot(3,1,2);
plot(t,real(v(t+1)),'b');
axis([0 200 -1.2 1.2]);
subplot(3,1,3);
plot(t,imag(v(t+1)),'g');
axis([0 200 -1.2 1.2]);

```

```
f = linspace(-0.5,0.5,N);
echo on
spec(1,:) = fft(v.*hann(N)')/(N/4);
spec2=fftshift(spec);
echo off; figure; clf; hold on;
plot( f, dbv(spec2(1,1:N)), 'b')
axis([-0.5 0.5 -160 0]);
xlabel('Normalized Frequency')
ylabel('Output Spectrum (dBFS)')
snr = calculateSNR(spec(1,ceil(fcnorm-fB/2):ceil(fcnorm+fB/2)),
ceil(fctest-fcnorm+fB/2),10);
-----

function snr = calculateSNR(hwfft,f,nsig)
if nargin<3
    nsig = 1;
end
signalBins = [f-nsig+1:f+nsig+1];
signalBins = signalBins(signalBins>0);
signalBins = signalBins(signalBins<=length(hwfft));
s = norm(hwfft(signalBins));
noiseBins = 1:length(hwfft);
noiseBins(signalBins) = [];
n = norm(hwfft(noiseBins));
if n==0
    snr = Inf;
else
    snr = dbv(s/n);
end
-----
```

A.3. Publications

- Song-Bok Kim, S. Joeres, and S. Heinen, “A compensation method of the excess loop delay in continuous-time complex sigma-delta modulators”, 18th European Conference on Circuit Theory and Design, 2007 (ECCTD07), pp.140-143.
- S. Joeres, Song-Bok Kim, and S. Heinen, “Simulation of quadrature-bandpass Sigma-Delta analog to digital converters using state space descriptions”, 18th European Conference on Circuit Theory and Design, 2007 (ECCTD07), pp.886-889.
- Song-Bok Kim, S. Joeres, N. Zimmermann, M. Robens, R. Wunderlich, and S. Heinen, “Continuous-Time Quadrature Bandpass Sigma-Delta Modulator for GPS/Galileo Low-IF Receiver”, IEEE International Workshop on Radio-Frequency Integration Technology, 2007 (RFIT07), pp 127-130.
- Song-Bok Kim, S. Joeres, and S. Heinen, “The Design of Continuous-Time Quadrature Bandpass Sigma-Delta modulators for Low-IF Receivers”, Workshop Analog’07 in Freiburg, 2007.
- Song-Bok Kim, T. D. Werth, S. Joeres, R. Wunderlich, and S. Heinen, “Effect of Mismatched Loop Delay in Continuous-Time Complex Sigma-Delta Modulators”, IEEE Transactions on Circuits and Systems II: Vol.55, No.10, pp.996-1000, 2008.
- Song-Bok Kim, S. Joeres, R. Wunderlich, and S. Heinen, “Complex Mismatch Shaper for Tree-Structured DAC in Multi-Bit Complex Sigma-Delta Modulators” 15th IEEE International Conference on Electronics, Circuits and Systems, 2008 (ICECS08), pp.328-331.
- Song-Bok Kim, S. Joeres, R. Wunderlich, and S. Heinen, “Continuous-Time Quadrature Bandpass Sigma-Delta Modulator with Capacitive Feedforward Summation for GSM/EDGE Low-IF Receiver” 15th IEEE International Conference on Electronics, Circuits and Systems, 2008 (ICECS08), pp.438-441.
- Song-Bok Kim, S. Joeres, R. Wunderlich, and S. Heinen, “Third-Order Continuous-Time Quadrature Bandpass Sigma-Delta Modulator for GSM/EDGE Low-IF Receiver”, Workshop Analog’08 in Berlin, 2008.
- A. Kruth, S. Joeres, A. Neyer, M. Robens, H. Erkens, Song-Bok Kim, D. Bormann, T. D. Werth, N. Zimmermann, R. Wunderlich and S. Heinen, “A Multi-mode Shared RF Low-Power Receiver Front-End Architecture for Satellite Based Navigation in 90 nm CMOS”, Workshop Analog’08 in Siegen, pp.19-24, 2008.

- Song-Bok Kim, M. Robens, S. Joeres, R. Wunderlich and S. Heinen, “A Polyphase Filter Design for Continuous-Time Quadrature Bandpass Sigma-Delta Modulators”, *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol.55, No.11, pp.3457-3468, Dec.2008.
- Song-Bok Kim, S. Joeres, R. Wunderlich, and S. Heinen, “A 2.7-mW, 90.3-dB DR Continuous-Time Quadrature Bandpass Sigma-Delta Modulator for GSM/EDGE Low-IF Receiver in 0.25- μ m CMOS”, *IEEE Journal of Solid-State Circuits*, Vol.55, No.3, pp.891-900, Mar.2009.
- Song-Bok Kim, Yifan Wang, and S. Heinen, “Analysis of Clock Jitter in Continuous-Time Quadrature Bandpass Sigma-Delta Modulators with NRZ Pulses”, 5th International Conference on Ph.D. Research in Microelectronics & Electronics, 2009 (PRIME09), Cork, Ireland, accepted.
- Song-Bok Kim, M. Robens, R. Wunderlich and S. Heinen, “Performance Limitation by Finite GBW in Continuous-Time Quadrature Bandpass Sigma-Delta Modulators”, *International Symposium on Signals, Circuits and Systems*, 2009, (ISSCS09), Iasi Romania, accepted.
- Song-Bok Kim, R. Wunderlich and S. Heinen, “A Contribution on design methods for Continuous-Time Quadrature Bandpass Sigma-Delta Modulators”, *Semiconductor Conference Dresden*, 2009, (SCD09), accepted.

A.4. Acknowledgements

First of all, author would like to thank the Gottlieb Daimler-und Karl Benz-stiftung for the financial support of this thesis.

I am thankful to my supervisor Prof. Dr.-Ing. Stefan Heinen. He gave me the opportunity to carry out the presented studies and provide kind guidance. I appreciate his supervision, encouragement and advice in process of last few years. He gave me lots of opportunities to present my research results in Conferences and Workshops.

Specially, I would like to say to thank my second supervisor, Prof. Dr.-Ing. Maurits Ortmanns who is a header of Institute of Microelectronics, Ulm University. We have discussed lots of scientific topics and techniques in CT Sigma-Delta modulators.

I am also thankful to Dr.-Ing. Ralf Wunderlich who has discussed issues concerning with published papers and Ph.D dissertation and provide me the help in the tape-out and measurement for test chips.

Of course, I appreciate Dr.-Ing. Stefan Joeres who provided an extended complex sigma-delta Matlab source code and has discussed lots of things as co-worker.

Thanks for the support of the crew here at the Chair of Integrated Analogue Circuits. Thanks for endless discussions.

Undoubtedly, I am indebted to my family and IC design and Microelectronics Center (ICD & MC), the State Academy of Sciences, Pyongyang, DPR Korea for continued support and encouragement, due to my absence from my motherland throughout few years of my studies.

A.5. Curriculum Vitae

Song-Bok Kim

born May, 2nd, 1976

in South Hamgyong, DPR Korea

- 09.1981 - 08.1985 Primary School, DPR Korea
- 09.1985 - 08.1991 Middle School, DPR Korea
- 09.1991 - 08.1992 Preliminary Course, University of Sciences, Pyongyang, DPR Korea
- 09.1992 - 04.1998 **Student, Department of Microelectronics, in Electronics and Automation, University of Sciences, Pyongyang, DPR Korea**
BSc.paper: "Readout Circuit from Chemical Sensor Array-ISFETs"
- 05.1998 - 10.2000 **MSc. Course, Department of Microelectronics, in Electronics and Automation, University of Sciences, Pyongyang, DPR Korea**
MSc.paper: "Nonlinearities and Cancellation in Dual-Slop Integrating Analog-to-Digital Converter"
- 10.2000 - 5.2006 **IC Design and Microelectronics Center, State Academy of Sciences, Pyongyang, DPR Korea**
Design and tape-out of low power and low supply voltage mixed-signal ICs for portable applications
Design and tape-out of $3\frac{3}{4}$ dual-slope integrating analog-to-digital converter which is controlled by embedded micro-processor
Design of pipeline analog-to-digital converter with 2Msamples/s, 10bit resolution
Study on discrete-time lowpass sigma-delta modulator for audio application
- 6.2006 - present **Ph.D. Student, Chair of Integrated Analog Circuits, RWTH Aachen University, Germany**
Design and tape-out of continuous-time quadrature band-pass sigma-delta modulators for GSM/EDGE and GPS/-Galileo applications