Low Power Design for Integrated Energy Harvesting Systems

Von der Fakultät für Elektrotechnik und Informationstechnik der Rheinisch-Westfälischen Technischen Hochschule Aachen zur Erlangung des akademischen Grades eines Doktors der Ingenieurwissenschaften genehmigte Dissertation

dargestellt von

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Thanks to my kids Ruqia and Hayder.

Thanks to my parents and brothers.

Thanks to my friends.
To my parents, Ayad Al-Shebanee and Layla Yousif
To my wife, Shamim
To my Kids, Ruqia and Hayder
Contents

List of Figures xi
List of Tables xv
List of Listings xvii
List of Abbreviations xvii
List of Symbols xix

1 Introduction 1
1.1 Motivation ......................... 1
1.2 Aim of the Thesis .................. 2
1.3 Thesis Structure .................. 2

2 Fundamentals of Conversion Circuits in Energy Harvesting Systems 5
2.1 General Architecture of Harvesting System .................. 5
2.2 Methods of Energy Harvesters .......................... 5
  2.2.1 RF Energy Harvesting ................. 6
  2.2.2 Thermal Energy Harvesting ............ 11
  2.2.3 Piezoelectric Energy Harvesting ........ 13
  2.2.4 Solar Energy Harvesting ................ 16
2.3 Low Voltage Low Power CMOS Circuits .................. 17
  2.3.1 Electrical Characteristics of CMOS Transistor in Sub-threshold Region ........................ 17
  2.3.2 Low Voltage Current Reference Circuit ........... 19
  2.3.3 Reference Voltage Circuit with Low Supply Voltage ........ 23
  2.3.4 Low Voltage Amplifier Circuits ........... 25
2.4 Power Managements Circuit ................... 27
  2.4.1 Rectifier conversion Circuits .............. 27
  2.4.2 DC-DC Up-Conversion Circuits ............ 35
  2.4.3 Power Losses in Conversion Circuits .......... 41
2.5 The Proposed System Aspects ................... 43
  2.5.1 Harvested Power Conditions and Targeted Energy Sources 43
  2.5.2 Sensitivity Enhancement .................. 44
3 RF Energy Harvesting System using Low-Power Charge Pump

3.1 Circuit Model of RF Energy Harvester

3.2 Passive Amplification of Input RF Voltage

3.2.1 High Radiation Resistance

3.2.2 Input Impedance With High Quality

3.3 Proposed CMOS RF Energy Harvesting System

3.4 Low Power RF Rectifier

3.4.1 Design of Differential Cross-Coupled RF Rectifier

3.5 Low-Power Charge Pump

3.5.1 Design of Cross-Coupled Charge Pump

3.5.2 Driving Clock Generator

3.6 System Implementation

3.7 Experimental Results Using RF Power Source

3.7.1 Test Procedure

3.7.2 Measurement Results of Charge Pump

3.7.3 Sensitivity Measurements of RF Energy Harvester

3.8 Design of PCB Antenna for RF energy harvesting

3.8.1 Antenna Characteristics

3.8.2 Antenna Types

3.8.3 Dipole Antenna Implementation

3.9 Experimental Results Using The Dipole Antenna

3.9.1 Test Procedure

3.9.2 Measurements of The S_{11} Parameters

3.9.3 Sensitivity Measurement Using Dipole Antenna

4 Low Input Voltage Boost Converter For Thermal Energy Harvesting

4.1 Thermoelectric Generator

4.1.1 Thermal and Electrical Model of the TEG

4.1.2 Choosing TEG Module For Thermal Energy Harvesting

4.2 Proposed DC-DC UP-Converter for Thermal Energy Harvester

4.2.1 Transformer Reuse Self Start-Up Technique

4.3 Design of Self Start-UP Oscillator

4.3.1 Self Start-Up Techniques

4.3.2 LC Based Start-Up Oscillator

4.3.3 Transformer Based Start-Up Oscillator

4.3.4 Negative Voltage Rectifier

4.4 Design of Low Power Inductor Based Boost Circuit

4.4.1 Ring Oscillator Circuit

4.4.2 Pulse Signal Generation

4.5 Control Circuit

4.5.1 Low Power Comparator Circuit

4.5.2 Driving Multiplexer Circuit
4.5.3 Simulation Results of The Control Circuit . . . . . . . . . 102
4.6 System Implementation . . . . . . . . . . . . . . . . . . . . . 103
4.7 Experimental Results . . . . . . . . . . . . . . . . . . . . . . . 107
   4.7.1 Test Procedure . . . . . . . . . . . . . . . . . . . . . . . . 108
   4.7.2 Measurements of Minimum Start-Up Input Voltage . . . . 109
   4.7.3 Measurements of The Converter In The Inductor-Based
       Boost phase . . . . . . . . . . . . . . . . . . . . . . . . . . . . 110

5 Conclusions and Outlook 113
   5.1 Conclusions . . . . . . . . . . . . . . . . . . . . . . . . . . . . 113
   5.2 Outlook . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 115
# List of Figures

2.1 Energy harvesting system. ............................................. 6  
2.2 RF power sources are everywhere. ................................. 7  
2.3 Floor plan (first floor) of the laboratory building showing the locations of measurements of WLAN signal path loss. .......... 9  
2.4 Example of desktop scanning window by inSSIDer software [2]. 9  
2.5 Path losses of RF signal of WLAN router RF in open space. .... 10  
2.6 Path losses of RF signal of WLAN router RF across two walls. 10  
2.7 Thermal energy sources with thermoelectric generator TEG. ... 12  
2.8 The output electrical power of typical TEG with size of 30 mm². 13  
2.9 Vibrational energy harvesting systems. .......................... 15  
2.10 Structure of photovoltaic arrays. .................................. 17  
2.11 Structure of an N-channel CMOS transistor. ..................... 18  
2.12 Basic supply independent current reference circuit. .......... 20  
2.13 Cascode current mirror with chain of transistors proposed instead of $R_{series}$. .................................................. 21  
2.14 Simulation results of $I_{out}$ with supply voltage using NMOS transistors chain instead of large $R_{series}$. .................. 22  
2.15 Low power circuit suggested to reduce the temperature influence on $I_{out}$. ....................................................... 23  
2.16 The impact of the suggested temperature adaptive current compensating circuit. ............................................. 24  
2.17 Reference voltage generation using the suggested current biasing circuit in sec. 2.3.2. ............................................. 25  
2.18 Low-power voltage reference circuit using NMOS with low $V_{gs}$. 26  
2.19 Reference voltage generation using reverse biased NMOS transistors. ............................................................. 27  
2.20 Implementations of inverter amplifier with low supply voltage. 28  
2.21 PMOS differential pair amplifier. .................................. 28  
2.22 Voltage doubler circuit. ............................................. 29  
2.23 Dickson RF voltage multiplier. ..................................... 30  
2.24 Greinacher charge pump. ............................................ 30  
2.25 Output voltage and efficiency of single stage rectifier using HSMS2860 diode. ..................................................... 31  
2.26 Three-levels threshold voltage compensation method. .......... 32  
2.27 Adaptive threshold-voltage compensation method. ............. 33
2.28 Elimination of the forward voltage $V_{th}$ using cross connection technique. .................................................. 34
2.29 Multistage differential input cross connected rectifier. ............ 34
2.30 Basic structure of single stage charge pump circuit. ............... 35
2.31 Multistage dickson charge circuit. .................................. 36
2.32 Three-stage charge pump with static switch biasing. .............. 37
2.33 Two-stage charge pump with dynamic switch biasing. ............. 38
2.34 Multistage cross coupled charge pump. ............................... 39
2.35 Magnetic-based DC-DC up-conversion circuit principle .......... 40
2.36 Inductor voltage waveform during the switching time $T_s$. ....... 41
2.37 Magnetic based boost converter circuit and its parasitic elements. 42
2.38 Cycled power management strategy by micro-controller in low power WSN. ............................................. 45

3.1 Circuit model of RF energy harvesting system. ...................... 48
3.2 $V_A$ vs the radiation resistance for $(R_r = R_{rec})$. .............. 49
3.3 Impact of high $X_{in}$ on $V_{rec}$. ...................................... 50
3.4 Variation in voltage gain with frequency for $f_c = 850$ MHz. ....... 51
3.5 The proposed CMOS integrated RF energy harvesting system. .... 52
3.6 Equivalent circuits of pad and package connections including parasitic components. ..................................... 54
3.7 Total power efficiency vs received power at a frequency of 850 MHz and typical 50$\Omega$ RF power source. ................. 55
3.8 Output DC voltage at maximum output power vs received power at a frequency of 850 MHz and typical 50$\Omega$ RF power source. . 56
3.9 Cross-coupled charge pump using reverse bulk biasing. .......... 58
3.10 Reference voltage $V_{ref1}$ vs $V_{rec,DC}$. ............................ 60
3.11 Block diagram of the charge pump based DC-DC up-converter. .. 61
3.12 Clock signal with peak-peak equal to $V_{rec,DC}$. .................. 62
3.13 Oscillation frequency stabilization with $V_{rec,DC}$. ............... 62
3.14 Chip micro graph of the RF energy harvesting system within a tape-out using UMC 0.13$\mu$m technology and total area of $(1.6x1.6)mm^2$. .................................................. 63
3.15 Layout of the proposed energy harvesting. .......................... 63
3.16 Matching network based on the charge-pump model coupled to rectifier. ..................................................... 65
3.17 Sensitivity measurements using RF4 PCB and RF source. ..... 66
3.18 Charge pump and sensitivity measurement setup. ................. 67
3.19 Measurements of the output voltage and drawn current of the charge pump. ............................................. 67
3.20 Measurement of $S_{11}$ parameter using of BoardI with the extracted matching network (Section. 3.7.1). ..................... 68
3.21 System sensitivity measurement with center frequency of 850 MHz. 68
3.22 Measurements of frequency influence on the sensitivity. . . . . 69
3.23 Comparison of radiation pattern between isotropic emitter and directional antenna. .................................................. 70
3.24 Typical structure of PCB patch antenna. .......................... 72
3.25 PCB square loop antenna. ........................................... 72
3.26 Dipole antenna realizations. ........................................ 73
3.27 Design of PCB dipole antenna. ..................................... 75
3.28 Main board measurement Board2 of RF energy harvesting system. 76
3.29 Dipole Antenna realization using FR4 substrate. ............... 76
3.30 Simulated and measured $S_{11}$ parameter of dipole antenna. . 77
3.31 Measurements of RF energy harvester in Board2 at 1 m distance from the transmitter. ................................. 78
3.32 Measurements of RF energy harvester at a distance of 1 m from the transmitter and ($P_t = 6.5$ dBm). ......................... 79
3.33 Measurements of RF energy harvester using Board2 at 9.2 m distance from the transmitter. ................................. 79

4.1 The Seebeck effect principle. ......................................... 81
4.2 Thermal and electrical modeling of the thermal energy harvester. 83
4.3 The power delivered from the TEG to the load as a functions to the input resistance. ................................................... 85
4.4 The available DC voltage from the TEG to the load as a functions to the input resistance. ................................................... 85
4.5 System operation phases. ................................................ 87
4.6 Cross-coupled $LC$ tank based self start up oscillator. ......... 88
4.7 Cross-coupled oscillator loaded with voltage multiplier circuit. 90
4.8 Transformer based self start up oscillator. ......................... 91
4.9 Simulation results of the self start up oscillator with $V_{oc} = 10$ mV. 93
4.10 Negative voltage rectifier using PMOS transistors. ............. 93
4.11 Driving circuit of the inductor based boost. ....................... 95
4.12 Clock signal generator circuit. ....................................... 96
4.13 Simulation results of the biased oscillator circuit for supply voltage change with time. ................................................ 96
4.14 Simulation results of the $f_s$ for supply voltage change with time. 97
4.15 Pulse signal generator circuit. ....................................... 98
4.16 The output signal of the high pass filter for an input clock signal of 10 kHz. ......................................................... 99
4.17 The pulse signal generated for input clock signal of 10 kHz. .... 99
4.18 Bulk input differential amplifier given in [27]. ................. 100
4.19 Amplifier circuit with differential signals generation circuits. .. 101
4.20 Output stage of the comparator. ..................................... 102
List of Tables

2.1 Losses of walls inside buildings. ........................................ 8
2.2 Input frequency and acceleration of some common vibration
sources [33]. ................................................................. 14
2.3 Producible power with various optical energy conditions [28, p.274]. 16
2.4 Conversion efficiency of photovoltaic junction according to the
used technology [28, p.275]. ............................................. 18

3.1 Additional RF multiplying stages vs charge pump ................ 53
3.2 Characteristics of the substrate used for antenna fabrication. . 74

4.1 Commercial Off-The-Shelf TEG modules with part numbers and
manufacturers [34]. .......................................................... 84
4.2 Characteristics of the current sense transformer used for the boost
converter. ................................................................. 91

5.1 Performance comparison to the state-of-the-art of RF energy
harvesting systems. ........................................................ 114
5.2 Performance comparison to the state-of-the-art of low input volt-
age boost circuits. ....................................................... 116
**List of Abbreviations**

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>AC-DC</td>
<td>AC to DC conversion</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DC-DC</td>
<td>DC to DC conversion</td>
</tr>
<tr>
<td>EM</td>
<td>Electro-Magnetic</td>
</tr>
<tr>
<td>GSM</td>
<td>Global System for Mobile Communications</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal-Insulator-Metal</td>
</tr>
<tr>
<td>MPPT</td>
<td>Maximum Power Point Tracking</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor (MOS) Field Effect Transistor (FET)</td>
</tr>
<tr>
<td>NMOS</td>
<td>N-type Metal Oxide Semiconductor (MOS) Field Effect Transistor (FET)</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PMOS</td>
<td>P-type Metal Oxide Semiconductor (MOS) Field Effect Transistor (FET)</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RF-EH</td>
<td>RF Energy Harvester</td>
</tr>
<tr>
<td>µC</td>
<td>Microcontroller</td>
</tr>
<tr>
<td>(TE)</td>
<td>Thermal Energy</td>
</tr>
<tr>
<td>TE-H</td>
<td>Thermal Energy Harvesting</td>
</tr>
<tr>
<td>TEG</td>
<td>Thermo-Electric Generator</td>
</tr>
<tr>
<td><strong>WLAN</strong></td>
<td>Wireless Local Area Network</td>
</tr>
<tr>
<td>----------</td>
<td>-----------------------------</td>
</tr>
<tr>
<td><strong>WSN</strong></td>
<td>Wireless Sensor Network</td>
</tr>
</tbody>
</table>
# List of Symbols

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k_f$</td>
<td>Number of penetrated floors</td>
</tr>
<tr>
<td>$k_w$</td>
<td>Number of wall types</td>
</tr>
<tr>
<td>$k_{wi}$</td>
<td>Number for walls of $i$th type</td>
</tr>
<tr>
<td>$L_{wi}$</td>
<td>[dB] The loss for walls of $i$th type</td>
</tr>
<tr>
<td>$L_f$</td>
<td>[dB] The loss between adjacent floors</td>
</tr>
<tr>
<td>$L_{o,dB}$</td>
<td>[dB] The free space path loss at reference distance of 1 m</td>
</tr>
<tr>
<td>$f$</td>
<td>[Hz] The frequency of the RF signals</td>
</tr>
<tr>
<td>$c$</td>
<td>The speed of light</td>
</tr>
<tr>
<td>$\Delta T$</td>
<td>[°C] The temperature difference</td>
</tr>
<tr>
<td>$\Delta T_{TEG}$</td>
<td>[°C] The actual temperature difference across the TEG module</td>
</tr>
<tr>
<td>$T_h$</td>
<td>[°C] The temperature of the hot side of the TEG module</td>
</tr>
<tr>
<td>$T_c$</td>
<td>[°C] The temperature of the cold side of the TEG module</td>
</tr>
<tr>
<td>$P_{TEG}$</td>
<td>[W] The DC available power from the TEG module</td>
</tr>
<tr>
<td>$y(t)$</td>
<td>The displacement of the system housing in vibrational system</td>
</tr>
<tr>
<td>$m$</td>
<td>The mass of the suspended seismic body in vibrational system</td>
</tr>
<tr>
<td>$Y$</td>
<td>The displacement magnitude of input vibrations in vibrational system</td>
</tr>
<tr>
<td>$\zeta_e$</td>
<td>The electrical damping ratio in vibrational system</td>
</tr>
<tr>
<td>$\zeta_m$</td>
<td>The mechanical damping ratio in vibrational system</td>
</tr>
<tr>
<td>$\omega$</td>
<td>The input frequency in vibrational system</td>
</tr>
<tr>
<td>$\omega_n$</td>
<td>The natural frequency of spring mass system</td>
</tr>
<tr>
<td>$a$</td>
<td>The acceleration magnitude of input vibrations in vibrational system</td>
</tr>
<tr>
<td>$n$</td>
<td>The nonideality factor in CMOS transistors</td>
</tr>
<tr>
<td>$V_T$</td>
<td>The thermal voltage</td>
</tr>
<tr>
<td>$I_o$</td>
<td>The residual drain current in saturation for $V_g = V_s = 0$</td>
</tr>
<tr>
<td>$V_{th}$</td>
<td>[V] The threshold voltage</td>
</tr>
<tr>
<td>Parameters</td>
<td>Description</td>
</tr>
<tr>
<td>--------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>$V_{th0}$</td>
<td>The threshold voltage when $V_{sb} = 0$</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>The body effect coefficient</td>
</tr>
<tr>
<td>$\Phi$</td>
<td>The Fermi potential</td>
</tr>
<tr>
<td>$I_d$</td>
<td>The drain current</td>
</tr>
<tr>
<td>$\mu_n$</td>
<td>$[\text{cm}^2\text{V}^{-1}\text{s}]$ The electron mobility</td>
</tr>
<tr>
<td>$I_{out}$</td>
<td>The output current in current reference circuit</td>
</tr>
<tr>
<td>$I_{ref}$</td>
<td>The reference current in current reference circuit</td>
</tr>
<tr>
<td>$V_{ref}$</td>
<td>The reference voltage in voltage reference circuit</td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td>The biasing current</td>
</tr>
<tr>
<td>$g_m$</td>
<td>The transconductance of the CMOS transistors</td>
</tr>
<tr>
<td>$\lambda_{CMOS}$</td>
<td>Channel length modulation</td>
</tr>
<tr>
<td>$P_{in}$</td>
<td>$[\text{W},\text{dBm}]$ Input power</td>
</tr>
<tr>
<td>$I_{Leakage}$</td>
<td>Leakage current in CMOS transistors</td>
</tr>
<tr>
<td>$I_{do}$</td>
<td>The drain current when $(V_{gs} - V_{th}) = 0$</td>
</tr>
<tr>
<td>$f_s$</td>
<td>$[\text{Hz}]$ The switching frequency of the boost converter</td>
</tr>
<tr>
<td>$V_{N\text{drop}}$</td>
<td>The voltage drop across the NMOS transistor</td>
</tr>
<tr>
<td>$V_{P\text{drop}}$</td>
<td>The voltage drop across the PMOS transistor</td>
</tr>
<tr>
<td>$N$</td>
<td>The number of stages in the charge pump</td>
</tr>
<tr>
<td>$P_{dyn}$</td>
<td>$[\text{W}]$ The dynamic losses</td>
</tr>
<tr>
<td>$P_{res,dc}$</td>
<td>The conduction losses due to the $I_{L,\text{average}}$</td>
</tr>
<tr>
<td>$P_{res,ac}$</td>
<td>The conduction losses due to the $\Delta I_L$</td>
</tr>
<tr>
<td>$\eta_{PCE}$</td>
<td>$[%]$ The power conversion efficiency</td>
</tr>
<tr>
<td>$P_{outDC}$</td>
<td>$[\text{W}]$ The DC output power</td>
</tr>
<tr>
<td>$T_s$</td>
<td>$[\text{s}]$ The time period of the switching signal in the boost converter</td>
</tr>
<tr>
<td>$Z_A$</td>
<td>Antenna impedance</td>
</tr>
<tr>
<td>$R_{loss}$</td>
<td>$[\Omega]$ Loss resistance of the antenna</td>
</tr>
<tr>
<td>$R_r$</td>
<td>$[\Omega]$ Radiation resistance of the antenna</td>
</tr>
<tr>
<td>$X_A$</td>
<td>Imaginary part of the antenna impedance</td>
</tr>
<tr>
<td>$Z_{in}$</td>
<td>Input impedance</td>
</tr>
<tr>
<td>$R_{in}$</td>
<td>$[\Omega]$ Real part of the input impedance</td>
</tr>
<tr>
<td>$X_{in}$</td>
<td>Imaginary part of the input impedance</td>
</tr>
<tr>
<td>$P_{av}$</td>
<td>Available power from the antenna</td>
</tr>
<tr>
<td>$X_{\text{match}}$</td>
<td>The matching inductance component</td>
</tr>
<tr>
<td>$A_{v\text{match}}$</td>
<td>The gain in RF voltage by resonance</td>
</tr>
</tbody>
</table>
### Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q$</td>
<td>The quality factor</td>
</tr>
<tr>
<td>$f_c$ [Hz]</td>
<td>The center frequency of bandwidth of RF signals</td>
</tr>
<tr>
<td>$I_{in,\text{rms}}$ [A]</td>
<td>The R.M.S. value of the input current to the boost converter</td>
</tr>
<tr>
<td>$W_p$</td>
<td>PMOS transistor width</td>
</tr>
<tr>
<td>$W_n$</td>
<td>NMOS transistor width</td>
</tr>
<tr>
<td>$I_{\text{load}}$ [A]</td>
<td>The output load current</td>
</tr>
<tr>
<td>$R_{\text{voltmeter}}$ [Ω]</td>
<td>The voltmeter impedance</td>
</tr>
<tr>
<td>$R_{\text{series},\text{meas}}$ [Ω]</td>
<td>The series resistance in measurements of RF energy harvester</td>
</tr>
<tr>
<td>$R_{\text{series}}$ [Ω]</td>
<td>The series resistance in reference circuits</td>
</tr>
<tr>
<td>$S$</td>
<td>The radiation density</td>
</tr>
<tr>
<td>$r$ [m]</td>
<td>The distance from transmitter to the harvester</td>
</tr>
<tr>
<td>$P_{E\text{IRP}}$</td>
<td>The Effective Isotropic Radiation RF Power</td>
</tr>
<tr>
<td>$G_i$</td>
<td>The antenna gain</td>
</tr>
<tr>
<td>$P_t$ [dBm]</td>
<td>The transmitter RF power</td>
</tr>
<tr>
<td>$D$</td>
<td>The antenna directivity</td>
</tr>
<tr>
<td>$\eta_{\text{antenna}}$</td>
<td>The antenna efficiency</td>
</tr>
<tr>
<td>$A_e$</td>
<td>The effective aperture of antenna</td>
</tr>
<tr>
<td>$\varepsilon$</td>
<td>The dielectric constant of the PCB substrate</td>
</tr>
<tr>
<td>$\varepsilon_{\text{eff}}$</td>
<td>The effective dielectric constant of the PCB substrate</td>
</tr>
<tr>
<td>$W_{\text{dipole}}$</td>
<td>The width of the copper track</td>
</tr>
<tr>
<td>$d_{\text{substrate}}$</td>
<td>The thickness of the PCB substrate</td>
</tr>
<tr>
<td>$L_{\text{dipole}}$</td>
<td>The length of the dipole antenna</td>
</tr>
<tr>
<td>$\alpha_S$ [°C/Ω]</td>
<td>Seebeck coefficient</td>
</tr>
<tr>
<td>$k$</td>
<td>Number of thermocouples in the TEG module</td>
</tr>
<tr>
<td>$R_c$</td>
<td>Thermal resistance of the heat sink on the cold side</td>
</tr>
<tr>
<td>$R_h$</td>
<td>Thermal resistance of the heat sink on the hot side</td>
</tr>
<tr>
<td>$R_{\text{th.TEG}}$</td>
<td>Thermal resistance of the TEG module</td>
</tr>
<tr>
<td>$R_{\text{in,boost}}$ [Ω]</td>
<td>The input resistance of the boost converter</td>
</tr>
<tr>
<td>$R_s$ [Ω]</td>
<td>The source resistance</td>
</tr>
</tbody>
</table>
## Parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{osc}$</td>
<td>[Hz]</td>
<td>The start up oscillation frequency of the boost converter</td>
</tr>
<tr>
<td>$R_{L,esr}$</td>
<td>[Ω]</td>
<td>The equivalent series resistance of the inductor</td>
</tr>
<tr>
<td>$R_p$</td>
<td>[Ω]</td>
<td>The modeled parallel resistance of $R_{L,esr}$</td>
</tr>
<tr>
<td>$R_{C,esr}$</td>
<td>[Ω]</td>
<td>The equivalent series resistance of the capacitor</td>
</tr>
<tr>
<td>$C_{mv}$</td>
<td>[F]</td>
<td>The parasitic capacitance of the low frequency voltage multiplier</td>
</tr>
<tr>
<td>$N_{prm}$</td>
<td></td>
<td>The transformation ratio of the SMT transformer</td>
</tr>
<tr>
<td>$C_p$</td>
<td></td>
<td>The parasitic capacitance of the CMOS transistors in the start up oscillator</td>
</tr>
<tr>
<td>$L_{sec}$</td>
<td>[H]</td>
<td>Inductance of the secondary winding of the SMT transformer</td>
</tr>
<tr>
<td>$C_{se}$</td>
<td>[F]</td>
<td>The self capacitance of the secondary winding of the SMT transformer</td>
</tr>
<tr>
<td>$R_g$</td>
<td></td>
<td>The gate resistance</td>
</tr>
<tr>
<td>$D_1$</td>
<td></td>
<td>The pulse width of the pulse signal in boost converter</td>
</tr>
<tr>
<td>$R_{load}$</td>
<td>[Ω]</td>
<td>Load resistance</td>
</tr>
<tr>
<td>$P_{out}$</td>
<td>[W]</td>
<td>The DC output power</td>
</tr>
<tr>
<td>Analog signals</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>--------------------------------</td>
<td>-----------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>$V_{ds}$</td>
<td>The drain-source voltage</td>
<td></td>
</tr>
<tr>
<td>$V_{gs}$</td>
<td>The gate-source voltage</td>
<td></td>
</tr>
<tr>
<td>$V_{bias}$</td>
<td>The biasing voltage</td>
<td></td>
</tr>
<tr>
<td>$V_{ref}$</td>
<td>The reference voltage in voltage reference circuit</td>
<td></td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>The DC input voltage to the DC-DC boost converter</td>
<td></td>
</tr>
<tr>
<td>$V_{RF}$</td>
<td>RF signal voltage</td>
<td></td>
</tr>
<tr>
<td>$V_{CLK}$</td>
<td>Clock signal</td>
<td></td>
</tr>
<tr>
<td>$V_L(t)$</td>
<td>The inductor voltage</td>
<td></td>
</tr>
<tr>
<td>$I_C$</td>
<td>The capacitor current</td>
<td></td>
</tr>
<tr>
<td>$I_L$</td>
<td>The inductor current</td>
<td></td>
</tr>
<tr>
<td>$\Delta I_L$</td>
<td>The ripple component in the inductor current</td>
<td></td>
</tr>
<tr>
<td>$I_{L,average}$</td>
<td>The average inductor current in the boost converter</td>
<td></td>
</tr>
<tr>
<td>$V_{amp}$</td>
<td>Amplitude of the RF sinusoidal signal</td>
<td></td>
</tr>
<tr>
<td>$V_{rec}$</td>
<td>The RF input voltage to the rectifier</td>
<td></td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>The DC output voltage</td>
<td></td>
</tr>
<tr>
<td>$V_{ac}$</td>
<td>The open circuit voltage of the TEG module</td>
<td></td>
</tr>
<tr>
<td>$V_{ant}$</td>
<td>The RF induced at antenna</td>
<td></td>
</tr>
<tr>
<td>$V_{rec,DC}$</td>
<td>The DC rectified voltage from rectifier</td>
<td></td>
</tr>
<tr>
<td>$V_{prm}$</td>
<td>The primary voltage at the primary inductor</td>
<td></td>
</tr>
<tr>
<td>$V_{sec}$</td>
<td>The secondary voltage at the secondary inductor</td>
<td></td>
</tr>
<tr>
<td>$V_{osc}$</td>
<td>The oscillation voltage</td>
<td></td>
</tr>
<tr>
<td>$V_{pulse}$</td>
<td>The pulse signal of the boost converter</td>
<td></td>
</tr>
<tr>
<td>$V_{filter}$</td>
<td>The output signal of the high pass filter</td>
<td></td>
</tr>
<tr>
<td>$V_{comp,1}, V_{comp,2}$</td>
<td>The control signals of the boost converter</td>
<td></td>
</tr>
<tr>
<td>$V_{boost}$</td>
<td>The voltage required to drive the boost circuits</td>
<td></td>
</tr>
<tr>
<td>$V_{out.div.}, V_{ref,low}$</td>
<td>The input differential signals of the comparator</td>
<td></td>
</tr>
<tr>
<td>$V_{neg.}$</td>
<td>The output voltage of the negative voltage rectifier</td>
<td></td>
</tr>
<tr>
<td>$V_{mux}$</td>
<td>The output signal of the driving multiplexer circuit</td>
<td></td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

1.1 Motivation

Wireless Sensor Network (WSN) are widely used in different applications nowadays. These sensors are necessary for monitoring some important physical parameters like temperature, humidity and mechanical stress etc. In the near future, it is expected that trillions of WSNs will be employed in various applications in order to process tremendous amounts of data, which promote the human life to a better quality. Driving these wireless sensor circuits by regular power supply such as a battery limits the places in which these sensors can be installed. Energy harvesting gives the solution to operate the WSN nodes in various places and environments. This is because battery-less electronics eliminate the need for power wires, maintenance and labor cost required for battery replacement and toxic waste for environment. The energy harvesting is defined as a process by which the energy available from various sources is transformed to electrical power. This principle has recently attracted a considerable interest in the academic and the industrial fields. The expected low power available from the harvester became usable because of the drastic reduction in power consumption of electronic circuits in recent years.

A variety of energy sources in the ambient environment can be utilized to generate the electrical power. Such energy sources can be light, motion, radio frequency (RF) radiation and thermal energy sources. Solar cells are one of the most widely used energy harvesting realizations. Here, the optical energy is utilized to generate the electrical power with wide range of sizes and power levels. The temperature difference in different applications is applied on the thermoelectric generator (TEG) module giving the electrical power as an example of the thermal energy harvesting. For a certain temperature difference, the generated power level is determined according to the size and physical characteristics of the TEG module used. The RF signals are exist with different frequencies while the radiation strength is related to the transmitted signal power. The ambient RF radiation in different frequencies can be captured by a receiving antenna giving an electrical signal. The vibration energy which is given by some mechanical excitations can be transformed into usable electrical power by the mechanical energy harvesting. Piezoelectric transducers are widely used for such purposes.
Chapter 1 Introduction

The output voltage given by the harvesting transducer is less than supply voltage level required for the typical sensor circuits. Therefore, voltage conversion circuits are required to reach an acceptable output DC voltage. As the voltage given by the micro harvesting generator is low, a high conversion ratio is needed. However, such high voltage conversion circuits are associated with high power losses contradicting with their use in low power applications. Consequently, low power conversion circuit designs are necessary to be suitable to the low power produced by the harvester.

1.2 Aim of the Thesis

The thesis concentrates on the energy harvesting systems within ultra low power range. The aim of the thesis is to recondition the harvested energy in order to reach the requirements of the sensor circuits used in energy harvesting applications. In addition to the low input power, more obstacles are expected that make the circuit design more challenging. Most of these obstacles are related to the nature of the energy source and the employed transducer such as the high frequency RF input signal in RF energy harvesting and the quite low DC input signal in thermal energy harvesting. The main purpose of the suggested circuit designs is to overcome these constraints with strict low power budget. Moreover, it is important that economic solutions are preferable so that the harvesting systems can be realized feasibly.

1.3 Thesis Structure

Chapter 2 starts with describing briefly the architecture of the energy harvesting system, where the power management circuit position in the system is illustrated. The circuit designs are based on the energy sources and the electrical signal produced from the transducer. Therefore, the most known energy harvesting methods are given including the related application and the power density expected in every method. As mentioned in Section 1.2, the thesis focuses particularly on energy harvesting systems within low power range. Therefore, the principles of low-power low-voltage CMOS circuits are reviewed including the biasing circuits, reference generators and amplifiers. The voltage conversion circuits are explained in detail with regard to both AC-DC rectifiers and DC-DC boost converters. Furthermore, the power losses associated with these circuits are demonstrated as well. Once the fundamentals of low-power voltage conversion circuits are given, it is possible to define the system aspects which are within the scope of this thesis. This includes the chosen energy harvesting methods, the conditions of input power level and input voltage and the targeted output results accordingly.

Chapter 3 is assigned for the design of the CMOS RF energy harvesting
system. The general circuit model of the harvester is given with regard to the impedance of the main parts of the harvester: antenna, CMOS RF rectifier and the matching network. According to the given circuit model, the principles of passively maximizing the RF input voltage is detailed. With the fundamentals of voltage conversion circuits given in Chapter 2, it will be possible to clarify the proposed system for RF energy harvesting. The proposed concept is presented with the explanation of the suggested methodology to increase the sensitivity of the CMOS RF energy harvesting system. The suggested CMOS system is composed mainly of an RF rectifier and a charge pump. The design of cross-coupled differential RF rectifier is detailed with simulation results. Moreover, the design of a cross coupled charge pump is illustrated including the design of the driving circuits and the related simulation results. The layout of the proposed CMOS harvesting system is given in addition to the trade-offs of sizing the capacitors and switches in the RF rectifier and charge pump. The chip is tested using both an RF signal generator and a dipole antenna using two different measurement boards. The measurement results using both test boards are shown and discussed.

Chapter 4 is assigned for the design of low input voltage boost converter for thermal energy harvesting. The circuit model of the thermal energy harvesting system is described according to the electrical model of the thermoelectric generator (TEG). The suggested circuit design of the boost converter is given including the proposed methodology of the transformer reuse technique. The converter is operated in two phases: the self-start-up phase and inductor based boost. The self-start-up oscillator circuit is explained with simulation results. The circuit of the inductor based boost is given as well including the driving pulse signal generation circuit. Furthermore, the control circuit which decides the operation phase of the converter is clarified with regard to the low power comparator and the driving multiplexer circuit. Similar to the RF energy harvesting system (chapter 3), the layout of the CMOS converter circuit is illustrated along with the size limitations and trade-offs regarding the wide switches and capacitors. The measurements results are demonstrated and discussed. It is important to notice that the test boards are the same as the ones used to measure the RF energy harvesting system.

Chapter 5 gives a summary for the accomplished research in this thesis. The conclusions regarding the achieved work and its experimental results are discussed in addition to a brief comparison with previous works found in literature. The outlook for future works are presented in order to discuss the possibilities for improving the performance of the implemented circuits.
Chapter 2

Fundamentals of Conversion Circuits in Energy Harvesting Systems

Since the research in this thesis concentrates on low power energy harvesting systems, this chapter reviews the main fundamentals of low power CMOS circuits. The power management circuits are designed for the source energy. Therefore, the most known energy harvesting methodologies are clarified along with the nature of the generated electrical signal. The basics of low power circuits as well as the power conversion circuits are inspected including those which are proposed to be used in this work.

2.1 General Architecture of Harvesting System

Energy can be found in different forms in ambient nature while the electrical energy is a common human need. Various transducers are used to convert different kinds of energy into electrical energy, Fig. 2.1 shows the general architecture of energy harvesting system. The main challenge in this application is the sufficiently wide gap between the produced voltage from the harvester and the minimum required voltage for the load. Therefore, voltage conversion is needed to boost the voltage up to the desired level. These power conditioning circuits can limit the system performance. The power management circuits are based on the characteristics of the transducers and the nature of their produced electrical signals. According to the energy source, the harvested voltage can be AC or DC with low or high level while the conversion circuit in the harvesting system can be AC-DC rectifier or DC-DC up-converter.

2.2 Methods of Energy Harvesters

The energy sources available for harvesting can exist in four main forms: light, radio frequency (RF) electromagnetic radiation, thermal gradients, and piezoelectric and motion. Every energy kind has its related applications, requirements, transducers and power management circuits. Therefore, it is needed to explore the harvesting methodology accompanied with every kind of energy source in order to optimize the conversion circuits accordingly.
2.2.1 RF Energy Harvesting

RF energy harvesting is a process where the emitted EM radiation from nearby ambient RF sources is linked to a receiving antenna to be converted into usable DC voltage. The main advantage in RF energy harvesting is the availability of power sources everywhere and in various conditions. Radio waves with different frequencies are transmitted from many types of devices such as cell phones, WLAN routers, GSM towers and TV towers. On contact with a conductor such as an antenna, these EM waves induce electrical current on the conductor's surface [42].

Sensor nodes in applications of temperature and moisture monitoring remain in deep sleep mode for long time while it is charged up by the transmitted RF power. In a later step, it is activated at a certain voltage level. Similarly, the sensors in irrigation systems can be active during the water delivery and sleep again [24]. Many applications are optimum within short distances from RF power transmitters like the sensors of temperature, motion, position, water and smoke in hotel rooms. RF energy harvesters using large antenna size can be useful to drive pollution sensors in zones which are crowded with pedestrians [24]. It is possible to realize these applications as practical systems available commercially. Powercast and Microchip produced RF energy harvesting kit for a battery-less wireless powered applications [3]. This given system is a combination of RF energy harvester by Powercast from and an ultra low power MicroController µC.

RF Power Density

The transmitted power reduces strongly because of the losses in transmission media in outdoor and indoor environments. In indoor areas, the transmitted power from WLAN routers can be taken as an example. The losses can be determined using the path loss propagation model given in [6] which is a suitable
Fig. 2.2: RF power sources are everywhere.
Table 2.1: Losses of walls inside buildings.

<table>
<thead>
<tr>
<th>Wall description</th>
<th>Loss [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>plasterboard or light concrete wall of 10 cm</td>
<td>3.4</td>
</tr>
<tr>
<td>Thick concrete or brick wall of 10 cm</td>
<td>6.9</td>
</tr>
</tbody>
</table>

model for initial WLAN planning. The path loss in dB is given by

\[
L_{dB} = L_{o,dB} + 20 \log_{10} d + k_f \left[ \frac{k_f + 2}{k_f + 1} \right]^{-b} L_f + \sum_{i=1}^{k_w} k_{wi} L_{wi},
\]

where \( k_f \) denotes the number of penetrated floors. The parameter \( b \) is used to fit empirically the nonlinear effects of the number of floors on the path loss. \( L_f \) denotes the loss between adjacent floors. The integer \( k_w \) is the number of wall types, \( k_{wi} \) and \( L_{wi} \) denote the number and loss for walls of \( ith \) type, respectively [6]. \( L_{o,dB} \) is the free space path loss at reference distance of 1 m and it is calculated as

\[
L_{o,dB} = 20 \log_{10} \frac{4\pi f}{c},
\]

where \( f \) is the frequency and \( c \) is the speed of light [16]. In order to calculate the losses of walls, Table 2.1 which is given by [6] gives loss approximation of two types of most known walls inside buildings. As a verification of the path losses, rough measurements have been done at the Integrated Analog Circuits and RF Systems Laboratory at RWTH Aachen University using the WLAN router as transmitter and the antenna of notebook as receiver (Fig. 2.3). The losses in RF power transmission were calibrated across open space and brick walls in the building with a transmitted power of 20 dBm peak according to the router datasheet. On the notebook side, the inSSIDer software which is a Wi-Fi network scanner application for Microsoft Windows and Apple OS X was used [1], [2]. Fig. 2.5 and Fig. 2.6 show the measurement results and theoretical calculations for the path losses versus distance across open space and walls respectively. The thickness of the walls is about 15 cm.

It is not possible to compensate the massive path losses by increasing the transmitted power because of health precaution and regulations. The RF exposure is of concern for many European researches which concentrate on the effects of GSM non ionizing radiation like Biomedical Effects of Electromagnetic Fields [7]. These studies can be helpful to estimate the power density on moderate distances from GSM base stations [46]. It was found by [46] that RF power...
2.2 Methods of Energy Harvesters

Fig. 2.3: Floor plan (first floor) of the laboratory building showing the locations of measurements of WLAN signal path loss.

Fig. 2.4: Example of desktop scanning window by inSSIDer software [2].
Fig. 2.5: Path losses of RF signal of WLAN router RF in open space.

Fig. 2.6: Path losses of RF signal of WLAN router RF across two walls.
densities of $10^{-5}$ mW/cm$^2$ to $10^{-4}$ mW/cm$^2$ are expected at distances between 25 m to 100 m from a GSM-900 base stations in indoor or outdoor on an elevated level.

### 2.2 Methods of Energy Harvesters

#### 2.2.2 Thermal Energy Harvesting

Thermal energy (TE) is another form of energy freely available in the ambient environment. It can provide sufficient electrical power able to drive WSN systems in various conditions. Thermal Energy Harvesting TE-H takes the advantage thermoelectric effect to produce electrical power using what is known as Thermo-Electric Generator TEG (see Section. 4.1). Simply, the thermal energy generated from the heat source at certain higher temperature is channeled through the enclosed TEG while the residual heat is then released to the surrounding ambient air at lower temperature [44].

The thermal energy harvester is based on temperature difference $\Delta T$ between hot side of $T_h$ and cold side of $T_c$. The efficiency of conversion from thermal energy to electrical energy relates directly to $\Delta T$ as given in Carnot’s formula

\[
\eta_{\text{carnot}} = \frac{(T_h - T_c)}{T_h}.
\]

(2.3)

This temperature gradient can be found in various applications when there is a heat source at higher temperature than that of ambient environment [36]. The $\Delta T$ can reach 10 °C between the human body skin and ambient temperature of 25 °C while the chest, head and the wrist are suitable body parts for energy harvesting. Sensors for preventive health-care, monitoring chronic deceases and vital body signs are related applications for such heat sources. Another example of heat sources is the waste heat from the daily used machines with $T_h$ higher than that in human body. Moreover, the waste heat from the internal combustion engine exhaust can give $\Delta T$ of several hundreds degrees by the exhaust gases themselves [36]. More related examples can be in the refrigeration systems and other heat pump cycles while the supplied sensors exist in automation systems and industrial applications.

The heat source availability is not the only advantage in thermal energy harvesting. The thermal energy harvesters are featured by their small size giving flexibility to fit with different work environments. Moreover, TE-H systems work autonomously while they can provide power continuously. Especially, with human, animal and other natural heat sources. The energy conversion process in TE-H is not accompanied by any remnants considered as pollutants. The available electrical power from the TEG depends on the temperature gradient $\Delta T$ and the characteristics of the TEG and the heat sink used. Not far from the commercial thermoelectric generators that are used for energy harvesting applications, Fig. 2.8 shows the open circuit voltage, $V_{oc}$, and the available power
Fig. 2.7: Thermal energy sources with thermoelectric generator TEG.
2.2 Methods of Energy Harvesters

Fig. 2.8: The output electrical power of typical TEG with size of 30 mm².

from the TEG, $P_{TEG}$, for typical TEG with electrical resistance of $2 \Omega$ and size of 30 mm² [34]. It is possible to obtain higher electrical power with higher temperature difference $\Delta T$ and larger TEG devices. However, this is limited with cost, size and other operating conditions.

2.2.3 Piezoelectric Energy Harvesting

It is possible to utilize the mechanical vibrations in various applications to produce electrical power. The vibrational energy sources can be high level vibrations from the large industrial equipments or low level vibrations which commonly occur in the ambient environment. Fig. 2.9(a) shows the equivalent model of a general vibrational system proposed in [49]. If the system housing is vibrated with a displacement of $y(t)$, the suspended seismic mass $m$ is vibrated in contrast with a displacement of $z(t)$, the differential equation that describes this relative motion is

$$m \ddot{z}(t) + d \dot{z}(t) + k z(t) = -m \ddot{y}(t),$$

(2.4)

where $k$ is the spring constant and $d$ is the damping constant. The magnitude of output power according to [33] is given as

$$|P| = \frac{m \zeta_e \omega_n \omega^2 \left( \frac{\omega}{\omega_n} \right)^3 Y^2}{\left( 2 \zeta_e + \zeta_m \left( \frac{\omega}{\omega_n} \right) \right) + \left( 1 - \left( \frac{\omega}{\omega_n} \right)^2 \right)^2},$$

(2.5)
Chapter 2 Fundamentals of Conversion Circuits in Energy Harvesting Systems

Table 2.2: Input frequency and acceleration of some common vibration sources [33].

<table>
<thead>
<tr>
<th>Vibration source</th>
<th>( a , (m/s^2) )</th>
<th>FH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Car engine compartment</td>
<td>12</td>
<td>200</td>
</tr>
<tr>
<td>Blender casing</td>
<td>6.4</td>
<td>121</td>
</tr>
<tr>
<td>Clothes dryer</td>
<td>3.5</td>
<td>121</td>
</tr>
<tr>
<td>Nervously tapped heel</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>Small microwave oven</td>
<td>2.5</td>
<td>121</td>
</tr>
<tr>
<td>Windows next to a busy road</td>
<td>0.7</td>
<td>100</td>
</tr>
<tr>
<td>CD on notebook computer</td>
<td>0.6</td>
<td>75</td>
</tr>
<tr>
<td>Second story floor of busy office</td>
<td>0.2</td>
<td>100</td>
</tr>
</tbody>
</table>

where \( Y \) is the displacement magnitude of input vibrations, \( \zeta_e \) is the electrical damping ratio, \( \zeta_m \) is the mechanical damping ratio, \( \omega \) is the input frequency and \( \omega_n \) is the natural frequency of spring mass system. For \( \omega = \omega_n \), the output power is maximum and Eq. 2.5 can be simplified as

\[
|P| = \frac{m \zeta_e \omega^3 Y^2}{4 (\zeta_e + \zeta_m)^2} = \frac{m \zeta_e a^2}{4 \omega (\zeta_e + \zeta_m)^2},
\]  

(2.6)

where \( a \) is the acceleration magnitude of input vibrations. The output power is directly related to the acceleration and inversely related to the input frequency used. Table 2.2 gives the input frequency and acceleration of some common vibration sources [33].

There are three conversion mechanisms to generate electrical power from such energy sources [28, p.276]:

- **Inductive systems**: An AC electrical current is induced in a coil due to a relative motion between a magnet and the coil (Fig. 2.9(b)).

- **Capacitive systems**: A mechanically variable capacitance results in changing the energy stored in the capacitor. For constant charge, the voltage increases as the capacitance decreases. On the other hand, for constant voltage, charge will be drained out of the capacitor as the capacitance decreases [33]. In both cases, the mechanical energy is converted to electrical energy (Fig. 2.9(c)).

- **Piezoelectric converters**: When a mechanical stress is applied on a piezoelectric material, a surface charge appears across the material layer giving an open circuit voltage (Fig. 2.9(d)). Moreover, if an oscillating mechanical load is placed on such materials, AC electrical power is generated.
2.2 Methods of Energy Harvesters

(a) Equivalent model of vibrational system.

(b) Inductive mechanism of vibrational to electrical energy conversion.

(c) Capacitive mechanism of vibrational to electrical energy conversion.

(d) Piezoelectric bimorph for vibrational to electrical energy conversion.

Fig. 2.9: Vibrational energy harvesting systems.
Table 2.3: Producible power with various optical energy conditions [28, p.274].

<table>
<thead>
<tr>
<th>Lighting condition</th>
<th>Incident power density (mW/cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sunny sky (day time)</td>
<td>100</td>
</tr>
<tr>
<td>Cloudy sky</td>
<td>5</td>
</tr>
<tr>
<td>10 ft from an incandescent bulb</td>
<td>10</td>
</tr>
<tr>
<td>10 ft from a CFL bulb</td>
<td>1</td>
</tr>
</tbody>
</table>

2.2.4 Solar Energy Harvesting

Solar energy is one of the most promising energy sources that can substitute the expensive power sources used nowadays. The harvesting process from light sources is strongly desired because it is free, clean and it is has no pollutant products that can harm the nature. Applications of solar energy harvesting can be seen in various environments of residential, vehicular, space and naval applications. In comparison with other energy sources, the solar energy is much abundant. The energy supplied from the sun to the earth for one day is sufficient to power the total energy needs of the planet for one year [18, p.1].

Solar power harvesting systems convert sunlight and other photonic energy sources to electrical power. These harvesting systems based on photovoltaic cells or what is also called as solar cells that utilize the photovoltaic effect will be explained in sec. 2.2.4. The harvested power from light sources depends on the lighting conditions and area of photovoltaic cells. Table. 2.3 give some examples of the incident power according to the lighting conditions.

Photovoltaic cells

The photonic energy is converted to electrical energy via a physical process called photovoltaic effect. The photovoltaic cell consists of two layers of semiconductor materials, N-type material with majority of electrons and p-type material with majority of holes (Fig. 2.10). A part of the incident photons on the solar cell are absorbed so that the electrons are energized and move from the N-type layer to the P-type layer across the junction between them. Consequently, positive charges are built along the N-type side of the PN junction and negative charges are built along the P-type side. An electric field (DC) is generated at the PN junction giving the force to move the electrons from the semiconductor toward the negative side passing to the load. In contrast, the holes move in the opposite direction toward the positive side [18, p.1]. Multiple photovoltaic cells can be arranged in series and parallel within arrays in order to raise the output voltage and output power as shown in Fig. 2.10. The conversion efficiency from photonic
2.3 Low Voltage Low Power CMOS Circuits

2.3.1 Electrical Characteristics of CMOS Transistor in Sub-threshold Region

The complementary metal oxide semiconductor transistors abbreviated as CMOS transistors are used in various integrated circuits known nowadays. These devices are referred as NMOS or PMOS when the current flow is due to electrons or holes respectively. Fig. 2.11 shows the structure of NMOS transistor fabricated on a P-type substrate which is also called the bulk or body. The device has four terminals referred as the gate \( G \), source \( S \), drain \( D \) and body \( B \) respectively. The gate terminal is a polysilicon region insulated from the substrate via a silicon dioxide \( SiO_2 \); the source and drain terminals are formed by heavily doped \( N \) regions in the \( P \)-type silicon bulk.

Assuming that the source and substrate are grounded, when a positive voltage is applied to the gate of the NMOS transistor, the holes in the channel are repelled away from the surface and a depleted layer of negative ions (inverted charges) is created underneath the silicon surface. As the gate voltage increases, an electron current flows from the drain \( D \) to the source \( S \) due to diffusion. This effect is...
Table 2.4: Conversion efficiency of photovoltaic junction according to the used technology [28, p.275].

<table>
<thead>
<tr>
<th>Technology</th>
<th>Efficiency %</th>
</tr>
</thead>
<tbody>
<tr>
<td>a-Si</td>
<td>11</td>
</tr>
<tr>
<td>p-Si</td>
<td>18</td>
</tr>
<tr>
<td>SC-Si</td>
<td>25</td>
</tr>
<tr>
<td>Organic</td>
<td>5</td>
</tr>
<tr>
<td>Organic</td>
<td>5</td>
</tr>
<tr>
<td>CIGS</td>
<td>19</td>
</tr>
<tr>
<td>Multi-gap</td>
<td>35</td>
</tr>
</tbody>
</table>

Fig. 2.11: Structure of an N-channel CMOS transistor.
called subthreshold conduction and the transistor operates in weak inversion region or subthreshold region. The current in this region is finite but it relates exponentially to the gate-source voltage as [29, p.27]

\[ I_d = I_o \exp\left(\frac{V_{gs}}{nV_T}\right), \quad (2.7) \]

where \( n > 1 \) is nonideality factor and \( V_T = (kt)/q \) is the thermal voltage, \( I_o \) is the residual drain current in saturation for \( V_g = V_s = 0 \) [47, p.58]. The weak inversion operating region is preferable with low supply voltage for low power applications because the currents are small. On the other hand, it is accompanied with drawbacks of high noise, limited speed and it is hard to achieve good linearity.

At a sufficient positive voltage value the electrons moves from the source to the drain forming a channel of charge carriers and the transistor is turned on. The value of the gate voltage at which this occurs is called the forward voltage or the threshold voltage \( V_{th} \). Similarly, PMOS transistor is turned on according to a similar principle to that of NMOS but with reserved polarities. The inversion layer is formed from holes in N-substrate in the PMOS transistor when a negative gate-source voltage \( V_{gs} \) is applied.

When \( |V_{gs}| \geq |V_{th}| \), the drain current referred as \( I_d \) is related to the gate-source voltage \( V_{gs} \) and drain-source voltage \( V_{ds} \) [29, p.20] as

\[ I_d = \mu_n C_{ox} \frac{W}{L} \left[ (V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2 \right], \quad (2.8) \]

where \( \mu_n \) is the electron mobility \( \left( \frac{cm^2}{V.s} \right) \), \( \frac{W}{L} \) is the aspect ratio and \( V_{gs} - V_{th} \) is the overdrive voltage. The drain current \( I_d \) reach maximum when \( V_{ds} = V_{gs} - V_{th} \). For further increasing \( V_{ds} \), the transistor channel is pinched off and the drain current will not follow the Eq. 2.8. According to this condition, the transistor operates in the saturation region and the drain current becomes relatively constant versus the drain-source voltage as

\[ I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2. \quad (2.9) \]

For \( V_{ds} < V_{gs} - V_{th} \) the transistor operates in triode region and the drain current relates linearly to the drain source voltage.

### 2.3.2 Low Voltage Current Reference Circuit

The weak inversion region is advantageous by the minimum drain-source voltage required for saturation. The drain current can be constant with a voltage \( V_{ds} \) applied to the transistor of \( 4V_T \) to \( 6V_T \). This makes such an operating region
suitable for low voltage current mirror circuits. It is possible to build low voltage current biasing circuits or amplifiers with supply voltage of less than $8V_T$ to $12V_T$. However, the drawbacks accompanied with subthreshold effect mentioned in Section 2.3.1 should be taken into account.

The regular current reference circuit shown in Fig. 2.12 can be used with low supply voltage while the gate-source voltage of the biasing transistors are less than the threshold voltage. The output current $I_{out}$ is independent from the supply voltage when the reference current $I_{ref}$ is derived from $I_{out}$. The PMOS transistors $M_1$ and $M_2$ are sized equally so that $I_{out} = I_{ref}$. The source resistor $R_{series}$ reduces the gate-source voltage of the NMOS transistor $M_4$ in comparison to that of the transistor $M_3$, thus, the size of the transistor $M_4$ is scaled up by a factor of ($K$) to compensate its drain current so that

$$\left(\frac{W}{L}\right)_{M_3} = K \left(\frac{W}{L}\right)_{M_4}, K > 1.$$  

(2.10)

The circuit performance can be enhanced by adding cascode NMOS transistors.

![Fig. 2.12: Basic supply independent current reference circuit.](image)

The cascode current mirror is used to improve copying the reference current $I_{ref}$ passing in the transistor $M_3$ to the output current $I_{out}$ passing in the transistor $M_4$. Additionally, the cascode NMOS transistors are useful for further stabilizing the output current $I_{out}$ with high supply voltage as well as reducing both $I_{ref}$ and $I_{out}$ currents.

In order to obtain $I_{out}$ less than $100\,\text{nA}$ for example, it is needed to use undesired large resistor $R_{series}$ of more than $1\,\text{M}\Omega$. Alternatively, a chain of NMOS transistors can be used while the gate terminals are connected to the ground in order
to increase their equivalent resistance (Fig. 2.13). Thus, the current $I_{out}$ passing through the transistors $M_{s1}$ to $M_{sn}$ is decreased drastically. This is helpful to eliminate the size required for integrated large resistor, especially when ultra low output current is desired. The total resistance of these NMOS transistors referred as $Z_s$ is determined by the source voltage of the transistor $M_{cas.2}$ to the output current $I_{out}$. The circuit shown in Fig. 2.13 has been simulated with supply voltage change for different temperature degrees. Eight series NMOS transistors have been used with ($W/L = 20\, \mu m/5\, \mu m$) giving high equivalent series resistance $Z_s$, while the other biasing transistors has been optimized to guarantee low reference current with minimum possible supply voltage. The output current given by the circuit is 13 nA. Fig. 2.14 show the simulation results of $I_{out}$ with supply voltage change for different temperatures. It can be seen that the circuit can start-up with 350 mV while the output current is close to be

![Fig. 2.13: Cascode current mirror with chain of transistors proposed instead of $R_{series}$.](image-url)
independent from the supply voltage. Conversely, it is strongly affected by the temperature change. As mentioned before, the drain current is strongly affected by the temperature change when \( V_{gs} < V_{th} \) according to Eq. 2.7. Therefore, it is needed to find a low power solution to decrease the temperature dependency of \( I_{out} \). As the temperature rises, the reference and output currents are increasing while the gate voltage of the transistors \( M_{cas.1} \) and \( M_{cas.2} \) is decreasing. If the resistance \( Z_s \) is increased, the \( I_{out} \) will decrease and vice versa. This principle can be used to eliminate the temperature dependency of the drawn currents as shown in Fig. 2.15. The series connected NMOS transistors can be used as an active load so that their gate voltages referred as \( V_{\text{activeload}} \) are related to the gate voltage of the transistors \( M_{cas.1} \) and \( M_{cas.2} \). Thus, when the temperature increases, the biasing voltage \( V_{\text{activeload}} \) changes inversely while the resistance \( Z_s \) is increased reducing the output current. The biasing voltage \( V_{\text{activeload}} \) can be defined by a voltage divider circuit consisting of series of diode connected NMOS transistors.

The circuit shown in Fig. 2.15 has been simulated with temperature changes for different supply voltages. The simulation results show that \( I_{out} \) changes slightly for wide range of temperature variations using the suggested temperature adaptive current compensating circuit as shown in Fig. 2.16. The output current at 27°C is higher than given in the previous circuit (Fig. 2.13) because the gate terminals of the series transistors are biased with the \( V_{\text{activeload}} \) instead of connecting them to ground giving lower equivalent resistance \( Z_s \).
2.3 Low Voltage Low Power CMOS Circuits

Fig. 2.15: Low power circuit suggested to reduce the temperature influence on $I_{out}$.

### 2.3.3 Reference Voltage Circuit with Low Supply Voltage

It is possible to generate a voltage reference circuit (Fig. 2.17) based on the proposed current reference circuit in sec. 2.3.2. An additional branch is used containing a biasing PMOS transistor and diode connected NMOS transistor. The voltage across the transistor $M_{ref}$ represents the output reference voltage referred as $V_{ref}$. The gate-source voltage of the transistor $M_{ref}$ is equal to the drain-source voltage and according to Eq. 2.9, the output reference voltage can be determined as $V_{ref}$

$$V_{ref} = V_{ds} = \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} + V_{th}, \quad (2.11)$$

where $I_D = I_{bias}$ is the biasing current controlled by the width $W$ of the PMOS biasing transistor $M_{bias}$. The reference voltage $V_{ref}$ is related directly to the square root of the length of the transistor $M_{ref}$ and the drain current $I_D$. The supply voltage range is the same as that of the current reference circuit. However, the minimum supply voltage is constrained with the threshold voltage $V_{th}$ of the transistor and the drain-source voltage of the biasing transistor $M_{bias}$.

The advantage of a low saturation drain-source voltage when $V_{gs} < V_{th}$ can be further utilized to generate a reference current and voltage. Fig. 2.18(a) shows a simple low voltage reference circuit built by an NMOS transistor and resistor.
Fig. 2.16: The impact of the suggested temperature adaptive current compensating circuit.

The gate terminal has been grounded in order to achieve minimum gate-source voltage giving minimum saturation drain-source voltage. At a certain $V_{DD}$ value, the drain current passing through the resistor reaches saturation giving a constant reference voltage referred as $V_{ref}$. High drain current or high resistance result in high $V_{ref}$ level and vice versa. The drain current is expected to be ultra low because of the extremely low gate-source voltage of the transistor $M_{bias}$. Consequently, high resistance $R_{series}$ is necessary to generate moderate reference voltage value and to reduce the power consumption of the circuit.

The resistor $R_{series}$ can be replaced by multiple PMOS transistors ($M_{p1}...M_{pn}$) connected in series while the source terminal of the transistor $M_{p1}$ is connected to the drain terminal of the transistor $M_{bias}$ and the gate terminals of the PMOS transistors are connected to ground (Fig. 2.18(b)). As the supply voltage increases, the drain current increases and reaches the saturation while the output voltage is equal to the defined reference voltage. Using long PMOS transistors enhance the equivalent resistance of the connected transistors and reduce the drawing current needed to reach the desired $V_{ref}$.

**Low power Low-Voltage Reference Circuit**

Not far from the principle used in sec. 2.3.3, the circuit proposed in Fig. 2.19 can be used to generate the reference voltage. The circuit consists of two NMOS transistors ($M_{n1}, M_{n2}$) that are!.reverse biased while the voltage across the transistor $M_{n2}$ represents the reference voltage $V_{ref}$. The gate-source voltage of the transistor $M_{n1}$ is negative minimum ($V_{gs,n1} = -V_{DD}$) giving higher off
2.3 Low Voltage Low Power CMOS Circuits

Fig. 2.17: Reference voltage generation using the suggested current biasing circuit in sec. 2.3.2.

resistance than that of the transistor $M_{n2}$ which has higher gate-source voltage ($V_{gs,n2} = -(V_{DD} - V_{ds,n1})$). Therefore, as the flowing current reaches saturation, the reference voltage is expected to be low. This circuit is advantageous for ultra-low power consumption.

2.3.4 Low Voltage Amplifier Circuits

The CMOS transistors can give acceptable gain even with low supply voltage by utilizing the advantage of minimum saturation voltage due to the subthreshold effect. High transconductance $g_m$ can be obtained by increasing the width while the drain current remains constant. Low drain current is expected as $V_{gs} < V_{th}$ leading to further an increased transconductance. The exponential relation of the drain current to the gate-source voltage (Eq. 2.7) encourages to use the CMOS transistors in subthreshold region in amplifier circuits. However, using wide devices with low drain current can limit the circuit’s speed as mentioned before.

Inverter Amplifier

The inverter circuit shown in Fig. 2.20(a) is a simple form of inverter amplifiers used in oscillators, buffers, gain stages and digital circuits. Assuming that the size of the PMOS transistor is chosen to keep charge mobility close to that in the NMOS transistor, the signal gain increases with supply voltage. However, the aspect ratio $\frac{W}{L}$ of the used devices is further optimized according to the circuit purpose. In ring oscillators, the frequency is determined by the number of inverter stages and signal delay across every stage controlled by the device size.
Fig. 2.18: Low-power voltage reference circuit using NMOS with low $V_{gs}$.

For driving buffers supplying heavy loads like the charge pumps, wider devices are desired for low on-resistances.

A common source amplifier (Fig. 2.20(b)) is another form of inverter amplifier while the current source load is used to maximize the gain. The transistor $M_{bias}$ can be biased by a current reference circuit giving constant current $I_{bias}$. The voltage gain is [29, p.58]

$$A_v = -g_m r_{out},$$

where $r_{out}$ is the output impedance seen at the output node and it is calculated as

$$R_{out} = R_{o,n} \ || \ R_{o,bias}, \ \text{with} \ R_o = \frac{1}{I_D \lambda_{CMOS}},$$

where $\lambda_{CMOS}$ is the channel length modulation which improves with long transistors. The voltage gain of the amplifier relates proportionally to the channel length of the transistors $M_n$ and $M_{bias}$ and, reversely, to the biasing current $I_{bias}$.

It is possible to combine the CMOS inverter with a biasing PMOS transistor giving an analog amplifier as in Fig. 2.20(c). This amplifier circuit can be used as a low-power high gain amplifier so that it gives an output signal with peak-peak amplitude equal to $V_{DD}$ even when the input signal has low amplitude. This technique is helpful to raise the input signal amplitude so that it can be equal to supply voltage with minimum possible power consumption.
2.4 Power Managements Circuit

Fig. 2.19: Reference voltage generation using reverse biased NMOS transistors.

**Differential Pair**

The differential pair amplifiers (Fig. 2.21) are widely used in monolithic analog circuits. The main advantage in using such circuit is the high rejection of the common mode signals in both inputs. These signals are eliminated due to the coupled drain or source terminals of the input transistors. In subthreshold region, high transconductance minimizes the difference of the gate voltages of the transistor pair required to compensate their mismatch. However, the drawback in using differential pair is its limited linearity.

2.4 Power Managements Circuit

As the electrical power is produced from the harvesting transducer, it is necessary to process the incoming electrical signal giving the desired load conditions. Voltage conversion circuits are used for power conditioning purposes. According to the harvester electrical signal, the conversion circuit can be AC-DC rectifier concerning input AC signals or DC-DC up-conversion circuits regarding input DC signals. Moreover, the power management circuit can contain both conversion circuits.

2.4.1 Rectifier conversion Circuits

**Diode Based Rectifier**

Several stages of the voltage doubler shown in Fig. 2.22 can be used to build a conventional RF rectifier using CMOS diode connected transistors as rectifier diodes. The shown circuit consist of a rectifier consisting of \( D_1 \) and \( C_2 \) and a voltage clamp consisting of \( D_2 \) and \( C_1 \). During the negative phase of the RF
Fig. 2.20: Implementations of inverter amplifier with low supply voltage.

Fig. 2.21: PMOS differential pair amplifier.
input voltage, $D_1$ is off and $D_2$ is on. The current pass through $D_2$ with voltage drop equal to $V_{th1}$ to charge $C_1$ up to $V_{amp} - V_{th}$, where $V_{amp}$ is the amplitude of input sinusoidal signal. In the positive phase, $D_2$ is off and $D_1$ is on. The current passes through $D_1$ to charge $C_2$ similarly up to $V_{amp} - V_{th2}$ in addition to the stored energy in $C_1$ during the negative phase so that the output DC voltage is

$$V_{out} = 2V_{amp} - V_{th1} - V_{th2}.$$  \hspace{1cm} (2.14)

The voltage doubler circuit is the fundamental building block for many conventional CMOS voltage multipliers like the Dickson charge pump and the Greinacher voltage multiplier as shown in Fig. 2.23 and Fig. 2.24 respectively.

The main draw back in diode connected rectifiers is the voltage drop across every rectifying diode, which decrease the output voltage massively. The rectifier cannot work with an input voltage of less than a threshold voltage, when the diode is in the dead zone or cut-off region. This kind of rectifier is not suitable for low input power, where the input voltage is expected to be ultra low. High input power applications on the other hand require less stages of voltage doubling circuit for better efficiency and prefer rectifying devices of high power capability like Schottky diodes rather than CMOS transistors.

In order to evaluate the diode connected rectifier for low power RF energy harvesting, single-stage doubler rectifier has been simulated using HSM/S2860 Schottky diodes with an input power range of $-16$ dBm to 0 dBm at a frequency of 0.85 GHz. The rectifier has been matched to an ideal RF power source of 50 $\Omega$ for an input power of $-16$ dBm using single series inductor. Fig. 2.25 shows the simulation results for DC output voltage and efficiency versus input power. The efficiency can reach up to 72% with a DC output voltage of 2.6 V for an input power of 0 dBm. The efficiency and output voltage decrease in strict way for low input power, when the input RF voltage $V_{rec}$ is less than the forward voltage $V_{th}$ of the diode. The output power and voltage can be higher when the matching network is optimized for higher input power because the efficiency changes.
Chapter 2 Fundamentals of Conversion Circuits in Energy Harvesting Systems

Fig. 2.23: Dickson RF voltage multiplier.

Fig. 2.24: Greinacher charge pump.
### Threshold Compensating Rectifier

As it was shown by a diode based rectifier that the threshold voltage drops across every rectifying diode, it decreases the efficiency significantly. The situation can be worse when the input voltage is less than threshold voltage so that the rectifier cannot be powered up to produce noticeable DC voltage. For low forward voltage $V_{th}$ devices, the rectifier is enabled to give high DC voltage with low input power.

In order to reduce the threshold voltage drop of the device, many alternative passive and active techniques have been discussed in literature. Methods of using external power sources are inconsistent with the autarkic operation concept targeted in this thesis. Contrarily, passive techniques require auxiliary circuits consuming additional power.

The threshold voltage technique can be simply realized in multistage rectifier when the gate of an *N MOS* transistor is connected to the next adjacent source of the following transistor instead of the traditional diode connected structure giving a biasing gate-source voltage equivalent to the incremental voltage across each stage. In case that a *PMOS* rectifying device is used, the gate terminal is connected to the previous source of last stage. According to the same principle,
the bias gate-source voltage can be increased by extending the gate connection to further next or previous stages.

Fig. 2.26 shows a hybrid method of 3 stage compensation reported by [14]. During the positive cycle of the input RF voltage, the PMOS transistor $M_i$ is forward biased because the gate terminal is connected to the source of the third previous transistor giving a negative gate-source voltage. During the negative phase, the gate-source voltage of the transistor $M_i$ is still negative increasing the leakage current of the reverse biased transistor.

Most of the reported threshold compensation methods give the priority to reduce the threshold voltage drop while neglect the power losses by the reverse leakage current when the CMOS transistor is reverse biased. The leakage current referred by $I_{Leakage}$ is expressed as

$$I_{Leakage} = I_{Do} \frac{W}{L} e^{\exp\left(\frac{(V_{gs} - V_{th})}{nV_T}\right)},$$  \hspace{1cm} (2.15)

where $I_{do}$ is the drain current when $(V_{gs} - V_{th}) = 0$, $V_T$ is the thermal voltage and $\frac{W}{L}$ is the device aspect ratio. In the threshold compensation technique, the gate-source voltage contains a DC component is given constantly from the next nodes even when the rectifying diode is reverse biased. This will increase the power losses due to the leakage current. Consequently, using higher level of threshold voltage compensation is limited with the resulting leakage current.

An adaptive method was presented by [15] according to this principle using auxiliary circuits shown in Fig. 2.27. During the negative input phase, the PMOS auxiliary transistor $M_{ib}$ is switched off because its gate-source voltage is less than the forward voltage $V_{th}$ while the diode connected PMOS transistor $M_{ia}$

Fig. 2.26: Three-levels threshold voltage compensation method.
is on. Thus, the rectifying PMOS transistor \( M_i \) is back compensated from the previous node so that its gate-source voltage is negative and it is forward biased. During the positive input phase, the source voltage of the auxiliary transistor \( M_{ib} \) is higher than its gate voltage so that it is switched on while the transistor \( M_{ia} \) is off. Thus, the transistor \( M_i \) is front compensated from the next node and its reverse biased. The leakage current is reduced as well.

The solutions given by threshold compensation rectifiers can enable the harvester to work with lower input power in comparison to the conventional diode based rectifiers. However, the auxiliary circuits increase the power budget of the conversion circuit giving that the usefulness of compensation technique is noticeable only when a relatively sufficient power is available. The rectifier circuit design should focus on the challenge of ultra low power received in environments of RF energy harvesting.

**Cross Connected Differential Rectifier**

It is possible to utilize differential RF signals rather than single input to switch the PMOS and NMOS devices to on and off states giving a self-driven synchronous rectifier as shown in Fig. 2.28. When \( V_{RF} \) is high and \( \bar{V}_{RF} \) is low, \( M_1 \) and \( M_4 \) turn on while \( M_2 \) and \( M_3 \) are off. Current flows to the node \( V_{DCH} \) through \( M_4 \) and out of the node \( V_{DCL} \) through \( M_1 \). During the opposite input voltages, \( M_1 \) and \( M_4 \) turn off while \( M_2 \) and \( M_3 \) are on. Thus, the current still in the same direction giving a DC voltage across the load connected between nodes \( V_{DCL} \) and \( V_{DCH} \). The output voltage can be calculated as

\[
V_{outDC} = V_{DCH} - V_{DCL} = 2|V_{RF}| - V_{Ndrop} - V_{Pdrop}, \quad (2.16)
\]
where $V_{N\text{drop}}$ and $V_{P\text{drop}}$ are the voltage drops due to the on-resistance of NMOS and PMOS devices, respectively.

In order to achieve higher output voltage, multistage rectifier can be constructed by cascading multiple rectifying cells. The input differential RF signals are applied in parallel to the rectifying stages across the coupling capacitors as shown in Fig. 2.29. When the input voltage $V_{\text{rec}}$ is high and $V_{\text{rec}}$ is low, current flows through transistor $M_1$ while the coupling capacitor $C_{\text{upper}}$ in the first stage is charged up to $|V_{\text{rec}}| - (V_{N\text{drop}} + V_{P\text{drop}})/2$. When the input voltage $V_{\text{rec}}$ is low and $V_{\text{rec}}$ is high, the current flows throw the transistor $M_3$ of the first stage and the transistor $M_2$ in the second stage to charge the capacitor $C_{\text{lower}}$ of the second stage similarly up to $|V_{\text{rec}}| - (V_{N\text{drop}} + V_{P\text{drop}})/2$ in addition to the charge stored from $C_{\text{upper}}$ in the first stage. The charge flow passes in parallel.
through the transistors $M_4$ of the first stage and the transistor $M_1$ of the second stage charging the capacitor $C_{upper}$ in the second stage to be discharged into the capacitor $C_{lower}$ in the following stage and so on. Consequently, the charge will be added at every stage and the DC voltage is boosted up. The last stage is connected without coupling capacitor to direct the DC current into the output capacitor.

### 2.4.2 DC-DC Up-Conversion Circuits

The DC-DC up-converters are needed to step-up the low DC voltage available from the harvester reaching the desired level. There are two categories of such conversion circuits, the charge pump and the inductor based boost. The charge pump uses capacitors for charge transfer and energy storage while the inductor based boost use inductors for energy transfer and capacitor for energy storage.

#### Low Power Charge Pump Circuits

The charge pump is switched capacitor based circuit used to generate higher voltage than the supply voltage for which the circuit is working. The basic strategy in boosting charge pumps can be illustrated in the circuit shown in Fig. 2.30. The circuit consists of single capacitor $C_{stage}$ used for boosting and three switches $S_1$, $S_2$ and $S_3$ used to control charge transfer. When the switches $S_1$ and $S_2$ are closed while the switch $S_3$ is open, the capacitor $C_{stage}$ is charged to the input voltage $V_{in}$. When the switches $S_1$ and $S_2$ are opened while the switch $S_3$ is closed so that the capacitor $C_{stage}$ behave as a voltage source connected in series with $V_{in}$. Since the capacitor maintains its previously stored charge ($Q = C V_{in}$), the output voltage rises to be twice the input voltage. It is possible to cascade multiple stages of the circuit given in Fig. 2.30 so that the output voltage

$$V_{in} = (N + 1) V_{in},$$

where the $N$ is the number of stages. The charge transfer switches can be realized using CMOS transistors driven by two anti-phase clocks. The clock

![Fig. 2.30: Basic structure of single stage charge pump circuit.](image-url)
voltage is usually limited with the input voltage, therefore, the minimum input voltage required to power up the charge pump is constrained with the forward voltage $V_{th}$ of the CMOS switch. Another challenge facing the charge pumps working with low input voltage is the voltage drop across the used switches which can be dominant with respect to the input voltage. Many circuit topologies have been given in literature to enhance the charge pump performance with low input voltage. In this section, some of these circuits are reviewed including the operation principle, advantages and disadvantages.

**Dickson Charge Pump**

The Dickson charge pump circuit given by John F. Dickson [25] (Fig. 2.31) is considered as a principle circuit for many known charge pump designs. The diode connected NMOS transistors work as switches while two out-of-phase clocks $V_{CLK}$ and $\overline{V}_{CLK}$ are capacitively coupled to the consecutive nodes between the switches. When the clock signal $V_{CLK}$ is low and $\overline{V}_{CLK}$ is high, the transistor $M_1$ is on while the transistor $M_2$ is off. The voltage at the first node $V_1$ is settled to $V_{in} - V_{th}$. When the clock signal $V_{CLK}$ is high and $\overline{V}_{CLK}$ is low, assuming that $V_{CLK} = V_{in}$, the voltage $V_1$ is calculated as

$$ V_1 = V_{in} + (V_{CLK} - V_{th}) \cdot (2.18) $$

At the same time, the transistor $M_2$ is on leading to the voltage at the second node is $(V_1 - V_{th})$. When the cycle is repeated, the clock signal $V_{CLK}$ is low and $\overline{V}_{CLK}$ is high so that the transistor $M_1$ is off while the transistor $M_2$ is on, the voltage $V_2$ becomes

$$ V_2 = V_{in} + 2 \left( V_{CLK} - V_{th} \right) \cdot (2.19) $$

By using multiple stages, the voltage at the node $N$ will be $(V_N = V_{in} + N \left( V_{CLK} - V_{th} \right))$. The last transistor $M_{N+1}$ works as an isolating diode while the output voltage is [25]

$$ V_{out} = V_{in} + N \left( V_{CLK} - V_{th} \right) - V_{th} \cdot (2.20) $$

Fig. 2.31: Multistage dickson charge circuit.
2.4 Power Managements Circuit

The parasitic capacitances of the MOSFET devices influence the coupled clock voltage amplitude at each node referred as \( V'_{CLK} \). This effect can be eliminated by using large coupling capacitor or minimizing the parasitic capacitance as \([22]\)

\[
V'_{CLK} = \frac{C_{stage}}{C_{stage} + C_{parasitic}},
\]

where \( C_{parasitic} \) is parasitic capacitance. It is clear that the voltage gain in every stage is reduced due to the forward voltage drop across the CMOS switch. Moreover, the voltage drop increases with the current supplied to the load. The output voltage can be expressed taking into account the voltage fluctuation caused by the load current referred as \( V_l \) as well as influence of the parasitic capacitance as

\[
V_{out} = V_{in} + N \left( V'_{CLK} - V_{th} - V_l \right) - V_{th}.
\]

**Charge Pump with Static Switches Biasing**

The voltage drop across every switch due to the forward voltage \( V_{th} \) are highly effective when the input voltage is low. Another charge pump design was given in \([53]\) and \([52]\) (Fig. 2.33) in order to overcome the reduction of the voltage gain caused by the threshold voltage drop. The gate terminals of the main NMOS switches referred as \( M_1 \ldots M_4 \) are connected to the nodes of the following stages utilizing the high potential of these nodes so that the mentioned transistors are forward biased. The diode connected NMOS transistors are connected in parallel to the main switches to start-up the charge pump. The main NMOS switches still forward biased even when the clock signal coupled to their drain terminals

![Fig. 2.32: Three-stage charge pump with static switch biasing.](image-url)
are low. Thus, part of the charge stored in the stage capacitors can be pumped reversely to the previous stages instead of the next stages decreasing the circuit performance.

**Charge Pump with Dynamic Switches Biasing**

The drawback of leakage current caused by static switch biasing can be solved if the main switches are turned on and off when the clock signal coupled to their drain terminals are high and low, respectively. Such solution has been given in [8] using inverter circuits to bias the gate terminals of the main switches $M_1 \ldots M_3$ dynamically as shown in Fig. 2.33. The inverter which drives the switch $M_2$ is

controlled by the node voltage $V_2$ while the source terminals of the PMOS and NMOS transistors of the inverter are connected to the node voltages $V_3$ and $V_1$ respectively. When the clock signal $V_{CLK}$ is high while $\overline{V_{CLK}}$ is low, the node voltage $V_1 > V_2$ so that the output signal of the inverter goes high to turn the transistor $M_1$ on. When the clock signal $V_{CLK}$ is low while $\overline{V_{CLK}}$ is high, the node voltage $V_2 < V_1$ so that the output signal of the inverter is low to turn the transistor $M_1$ off.

**Cross Coupled Charge Pump**

Another method to bias the charge transfer switches dynamically is given in [26] without the need for inverter circuits, Fig. 2.34. Every stage consists of two parallel paths used for charge transfer and controlled by two out of phase
signal clocks $V_{CLK}$ and $\overline{V_{CLK}}$. Each path consist of NMOS transistor and PMOS transistor while the clock signal is coupled through the stage capacitor which is connected to the drain terminals of the mentioned transistor. When the clock signal $V_{CLK}$ is low and $\overline{V_{CLK}}$ is high, the transistor $M_{nu}$ is on charging the stage capacitor $C_u$ of the first stage to the input voltage $V_{in}$. At the same time, the transistors $M_{pu}$ in the first stage and $M_{nu}$ in the following stage are off so that the reverse current is eliminated. When the clock signal $V_{CLK}$ is high and $\overline{V_{CLK}}$ is low, the transistors $M_{pu}$ in the first stage and $M_{nu}$ in the second stage are on so that the coupling capacitor in the second stage is charged up to $2V_{in}$. During the next duty cycles, the output voltage is raised according to the number of stages to reach maximally $(N+1)V_{in}$ as mentioned in Eq. 2.17. The same operation principle is applied in the opposite path, but in complementary fashion so that one coupling capacitor is charging while the coupling capacitor in the opposite path is pumping the charge to the output side.

**Inductor Based Boost**

The magnetic based DC-DC converters can give a voltage step-up conversion mechanism using quasi-lossless inductor for energy transfer from the power source to the output. The principle of the inductor based boost is based on energizing and de-energizing the inductor $L$ from the input voltage $V_{in}$ to the output voltage $V_{out}$ in two alternating phases, (Fig. 2.35). During the energizing
phase, the switch $M_n$ is on and the diode is off so that the energy is built up in the inductor by the input voltage ($V_L(t) = V_{in}$) while the output capacitor $C_{out}$ supplies the load with current $\left( I_C(t) = -\frac{V_{out}}{R_{load}} \right)$. During the de-energizing phase, the switch $M_n$ is off and the diode $M_p$ is on and the inductor voltage is reversed to be ($V_L(t) = V_{in} - V_{out}$) while the output capacitor $C_{out}$ is charged up to $\left( I_{L,average} - \frac{V_{out}}{R_{load}} \right)$, where $I_{L,average}$ is the average inductor current. The net inductor voltage for the whole switching period $T_s$ according to the principle of inductor volt-second balance is given by

$$V_{pulse} = V_{in} - V_{out} \cdot M_{switch} \text{ is on}$$

$$\frac{V_{out}}{V_{in}} = 1 \left( \frac{1 - D_1}{2} \right)$$

Conversely, the average capacitor current $I_C$ for the switching period $T_s$ is zero according to the principle of capacitor ampere-second balance resulting in

$$\frac{-V_{out}}{R_{load}} \cdot D_1 \cdot T_s + \left( I_{L,average} - \frac{V_{out}}{R_{load}} \right) \cdot D_2 \cdot T_s \Rightarrow I_{L,average} = \frac{V_{in}}{D_2} = \frac{V_{in}}{(1 - D_1)^2}$$

**Fig. 2.35: Magnetic-based DC-DC up-conversion circuit principle**.
2.4 Power Managements Circuit

2.4.3 Power Losses in Conversion Circuits

Generally, the available power from the transducer is almost low. Therefore, the power losses of the conditioning circuits can be dominant in comparison to the harvested power. This motivates to understand the losses accompanied with the conversion circuits and in opposite, the solutions on the circuit design and optimization are given. The main source of the aforementioned losses are the parasitic resistance, capacitance and inductance associated with the lumped capacitors and inductors and the CMOS switches as well as the driving and control CMOS circuits.

The power losses are classified mainly into two categories, conduction losses and dynamic losses. Conduction losses refers to the power dissipated in the parasitic resistors of the lumped elements and switches. Dynamic losses concerns the power lost by the parasitic capacitances of the switches during the incoming control clock signals. The reverse returned current from the output capacitor is referred also as dynamic losses. In this section, power losses are briefly reviewed with their causes and related expressions. The inductor-based boost circuit shown in Fig. 2.37 can be taken as a typical example of power conversion circuits.

Conduction Losses

The power conduction flow through the resistive elements is associated with conduction losses. These elements include the on-resistances of the PMOS and NMOS switches referred as $R_{on,p}$ and $R_{on,n}$, respectively, the equivalent series resistance of lumped inductor $L_1$ referred $R_{L,esr}$ and lumped output capacitor $C_{out}$ referred as $R_{C,esr}$. For simplicity, the on-resistances of the CMOS switches are assumed to be equal so that $R_{on,p} = R_{on,n} = R_{on}$. The inductor current $I_L$ consists of the DC component $I_{L,average}$ and the AC component $\Delta I_L$. The resistive losses due to the DC current $I_{load}$ is

$$P_{res,dc} = I_{L,average}^2 R_{L,esr} + I_{L,average}^2 R_{on} (D_1 + D_2) = I_{L,average}^2 (R_{L,esr} + R_{on}).$$

(2.25)
Moreover, the AC part of the inductor current $\Delta I_L$ flows through the resistors given in Eq. 2.25 and the equivalent series resistance of the output capacitor $R_{C.esr}$. The $\Delta I_L$ is determined as

$$\Delta I_L = \frac{dI_L(t)}{dt} = \frac{V_L(t)}{L} = \frac{V_{in} - V_{out}}{L} = \frac{V_{in}}{L}D_1T_s.$$  \hspace{1cm} (2.26)

The resistive losses due to the AC component of the inductor current is

$$P_{res.ac} = (\Delta I_L)^2_{rms} \left( R_{L.esr} + R_{on} + R_{C.esr} \right).$$  \hspace{1cm} (2.27)

For $(\Delta I_L)_{rms} = \frac{I_L}{\sqrt{12}}$ (R.M.S. of a triangle ripple current) and by substituting the $\Delta I_L$ from Eq. 2.26 into Eq. 2.27, the $P_{res.ac}$ is given as

$$P_{res.ac} = \frac{(\Delta I_L)^2_{rms}}{12} \left( R_{L.esr} + R_{on} + R_{C.esr} \right).$$  \hspace{1cm} (2.28)

The DC and AC resistive losses are decreased by using high quality lumped elements, wider switches for less on-resistance and using higher switching frequency for less $(\Delta I_L)_{rms}$. However, wider devices and higher switching frequency increase the dynamic losses as will be explained later.

**Dynamic Losses**

The dynamic losses include the gate drive losses, the bidirectional losses and the quiescent current losses when both NMOS and PMOS switches are on. *Gate drive losses* refer to the energy lost due to charging and discharging of the parasitic capacitors of the switch gates $C_{gs}$ and $C_{gd}$. This switching gate-driving
losses are directly related to the switching frequency \( f_s \), the input voltage \( V_{in} \) and the gate parasitic capacitors (device size) as

\[
P_{dyn} = f_s (C_{gs} + C_{gd}) V_{in}^2.
\]

\[ (2.29) \]

Bidirectional losses are caused due to light average inductor current and large ripple current \( \Delta I_L \) during the de-energizing phase so that the inductor current \( I_L(t) \) is reversed being negative. In order to avoid this kind of power losses, the following condition is provided

\[
I_{L,average} > \frac{1}{2} \Delta I_L \Rightarrow \frac{V_{in}}{D_2^2 R_{load}} > \frac{V_{in}}{L} D_1 T_s \Rightarrow \frac{2 L}{R_{load} T_s} > D_1 (1 - D)^2.
\]

\[ (2.30) \]

Another solution can eliminate the bidirectional losses by changing to discontinuous mode \( DCM \) where an additional operation phase of disconnecting inductor from the output capacitor \( C_o \) and \( R_{load} \) to avoid reversing the inductor current. Quiescent current losses is caused when both PMOS and NMOS switches being on so that high current peaks are drained to the ground. This power loss happens twice during the switching cycle and is proportional to the time duration when both transistors are on.

### 2.5 The Proposed System Aspects

The energy harvesting system can be proposed in accordance to the conditions associated with targeted energy sources on one side and the fundamentals given in this chapter regarding the conversion circuits on the other side. This section will summarize the main targets of this work and define the main principles of the proposed circuits for energy harvesting.

#### 2.5.1 Harvested Power Conditions and Targeted Energy Sources

The advantages of RF energy harvesting that have been listed in Section 2.2.1 give the motivation to present a complementary conversion circuit for such energy harvesting method. It has been explained that the RF power density is strongly reduced with distance from the transmitter (see Section 2.2.1). Therefore, the operation condition of ultra low input power is the main challenge to the conversion circuit proposed for RF energy harvesting. Thermal energy harvesting as another kind of energy harvesting methods has been discussed including its feature in Section 2.2.2. The available power from the typical TEG modules (off the shelf TEG modules) is higher than harvested from RF energy harvesting. On the other hand, the DC voltage of the TEG is expected to be quite low (10 mV/K to 50 mV/K). Therefore, this gives another example of the harvested power conditions which require different conversion
circuit design rather than should be designed for RF energy harvesting. The main purpose of this work is to present various CMOS circuit solutions for low-power low-voltage available from the harvester. Thermal and RF energy harvesting methods are associated with such harvested power conditions and require different power conversion circuits, thus, fitting optimally with scope of the work.

### 2.5.2 Sensitivity Enhancement

The input voltage and current are reproduced using the power conversion circuit in order to supply the needs of the loading application. Literature refers to the power conversion efficiency of the conversion circuit as its principal figure of merit. Power conversion efficiency $\eta_{PCE}$ can be calculated as

$$\eta_{PCE} = \frac{P_{outDC}}{P_{in}}, \quad (2.31)$$

where $P_{in}$ is the input electrical power to the conversion circuit and $P_{outDC}$ is the output DC power supplied to the load calculated as

$$P_{outDC} = \frac{V_{out}^2}{R_{load}}, \quad (2.32)$$

where $V_{out}$ is the output DC voltage applied to the load resistance $R_{load}$. Optimizing the conversion circuit for high efficiency requires using wider CMOS devices and less voltage boosting stages in order to supply highest possible DC power to the load with lowest voltage drop due to the on-resistance. As was explained in Section 2.4.3 wider devices can increase the switching power losses. Moreover, additional circuit might be necessary to enhance the efficiency. This, however, can increase power consumption of the power conditioner like the forward voltage $V_{th}$ compensation circuits or the MPPT circuits.

The energy sources in the surrounding environment can be considered as boundless reservoir of energy utilized by the harvester, but its main drawback is low power density. It is expected that output power from the harvester is low and does not fit to the regular power hungry loads like the transmitting power amplifiers which can tolerate conversion circuits with high power consumption. The energy source is not able to supply such power dumps. Therefore, solutions have been given in literature to extend the operational life of energy harvesting applications.

The development in semiconductor technology and IC design have contributed effectively in reducing the power consumption of the sensor node. Simply, a WSN node consists of low power micro-controller to process data from the application and low power RF transceiver for information transmission [20]. Recent studies proposed a duty-cycled power management strategy is divided to sleep phase
2.5 The Proposed System Aspects

The sensor system is going in sleep or stand by mode while the storage capacitor of energy harvester is charged up. At a defined voltage level, the power management unit switches the system to the active mode and the main circuits are activated utilizing the stored energy.

Duty-cycled operation is desired in energy harvesting applications because it gives the opportunity to prolong the sleeping time $T_{sleep}$ and reduce the average drawn current by the sensor node. Fig. 2.38 shows the power consumption scheme during a typical duty cycle managed by an ultra-low power microcontroller $\mu$C.

The total power consumption over the whole cycle time can be calculated as

$$\text{Average Power consumption} = \frac{\text{Active mode power} + \text{sleep mode power}}{T_{sleep} + T_{active}}$$  \hspace{1cm} (2.33)
This kind of energy conditioning strategy is useful to provide high energy at the output when only low power is available from the source. The minimum input power or input voltage required to produce a desired output DC voltage with sufficient energy stored in the output capacitor is referred as the sensitivity. As the energy harvesting system has high sensitivity, it is able to work with challenging operation conditions similar to that given in Section 2.5.1. Improving the system sensitivity is proposed in this work rather than maximizing the efficiency because it fits optimally to the expected conditions of power density.
Chapter 3

RF Energy Harvesting System using Low-Power Charge Pump

This chapter presents a proposed methodology to enhance the sensitivity of the RF energy harvesting systems by amplifying the input RF voltage and supporting the rectifier by a DC-DC up-converter. The rectifier is based on keeping a high input reactance to maximize the quality factor of input impedance giving high voltage gain via matching network. On the other hand, an ultra-low power charge pump is connected to the rectifier in order to boost the DC voltage. The harvesting system has been realized in 130 nm CMOS technology. The design has been proven by an RF source and dipole antenna as well. The sensitivity of the harvester is taken at the input power, where the unloaded output reaches 1 V. The measurements show a sensitivity of $-25$ dBm over the frequency range from 800 MHz to 870 MHz using RF power source. Dipole antenna has been designed and fabricated using economical FR4 substrate. The measurements show that the sensitivity using the dipole antenna is $-25$ dBm over the frequency range from 810 MHz to 830 MHz.

3.1 Circuit Model of RF Energy Harvester

The RF energy harvester (RF-EH) consists basically of an antenna, a matching network and an RF to DC conversion circuit as shown in Fig. 3.1. The RF power is transmitted as a radiation of EM waves to be picked up by the receiving antenna giving an AC electrical power. The conversion circuit referred as RF rectifier converts the input AC signal to DC signal while the harvested electrical energy is stored in the output capacitor. Fig. 3.1 shows a simple model of the circuit of RF-EH. The antenna can be modeled as an RF power source with complex impedance, $Z_A$, composed of effective loss resistance, $R_{loss}$, effective radiation resistance, $R_r$, and imaginary part, $X_A$, which is mostly inductive reactance

$$Z_A = R_r + R_{loss} + jX_A.$$  \hspace{1cm} (3.1)

With regard to the antenna impedance, power is converted into heat by the ohmic resistance, $R_{loss}$, while RF power is emitted from the antenna into space.
in the form of EM waves by the radiation resistance, $R_r$. On the other side, the impedance of RF rectifier is almost capacitive and it consists of real part, $R_{in}$, and imaginary part, $X_{in}$. In regular CMOS rectifiers, the input impedance is nonlinear but it can be assumed to be constant with low input power [21]. The antenna impedance should be equal to the rectifier impedance in order to ensure maximum power transfer from the source to the rectifier, therefore, a matching network is necessary. The antenna and the CMOS harvesting system are optimized according to the RF frequency band, the expected power received and the minimum output DC voltage required by the load.

### 3.2 Passive Amplification of Input RF Voltage

Typically, high efficiency rectification circuits require a minimum input RF voltage of more than the forward voltage, $V_{th}$, of the rectifying device. This can be guaranteed only with sufficient input power. Therefore, low input power is the main obstacle to any system concept since it limits the performance of power conversion circuits. Using Schottky diodes or CMOS rectifying transistors with low threshold voltage can enable the system to work with relatively low input power as will be shown later. In this section, the main scope is to maximize the available RF voltage from antenna in order to overcome the barrier of the forward voltage, $V_{th}$, of the rectifier.

#### 3.2.1 High Radiation Resistance

The induced RF voltage, $V_A$, at the receiving antenna is related to the available power, $P_{av}$, and the radiation resistance, $R_r$, as

$$V_A = \sqrt{8 P_{av} R_r}.$$  \hspace{1cm} (3.2)
3.2 Passive Amplification of Input RF Voltage

![Graph showing V_A vs input power for different radiation resistances](image)

Fig. 3.2: $V_A$ vs the radiation resistance for $(R_r = R_{rec})$.

It can be seen from Eq. 3.2 that the induced voltage at the antenna, $V_A$, increases with, $R_r$, even when the available power, $P_{av}$, is low. Assuming that the ohmic resistance $R_{loss}$ in the antenna is negligible and the input reactance, $X_{in}$, of the rectifier is quite small value and equal to $(X_A + X_{match})$, the input RF voltage to the rectifier, $V_{rec}$, can be calculated as

$$V_{rec} \approx V_A \frac{R_{in}}{R_{in} + R_r}.$$  \hspace{1cm} (3.3)

The input RF voltage, $V_{rec}$, can be maximized with the conditions of high $R_r$ and $(R_{in} = R_r)$, Fig. 3.2 shows how $V_{rec}$ increases with high radiation resistance.

### 3.2.2 Input Impedance With High Quality

In looking to Fig. 3.1, taking into account the influence of the inductance in the antenna ($X_A$) and the matching network ($X_{match}$) on one side and the capacitance in the input impedance of the rectifier ($X_{in}$) on the other side, it is possible to amplify the input RF voltage effectively using high quality $LC$ combination. The voltage gain in input voltage referred as, $Av_{match}$, can be calculated from [41]

$$Av_{match} = \frac{V_{rec}}{V_A} = \frac{X_{in} + R_{in}}{(X_A + R_{loss} + R_r) + (X_{match}) + (X_{in} + R_{in})}.$$  \hspace{1cm} (3.4)
Chapter 3 RF Energy Harvesting System using Low-Power Charge Pump

The induced voltage at antenna, $V_A$, in Eq. 3.2 can be substituted in Eq. 3.4 as well leading to $V_{rec}$ is related to the available RF power, $P_{av}$, as

$$V_{rec} = \frac{\sqrt{8 R_r P_{av}} \cdot (X_{in} + R_{in})}{(X_A + R_{loss} + R_r) + (X_{match}) + (X_{in} + R_{in})}. \tag{3.5}$$

For ($X_{in} = X_A + X_{match}$ and assuming that the ohmic resistance is neglected ($R_{loss} \approx 0$), Eq. 3.5 can be simplified to

$$V_{rec} = \frac{\sqrt{8 R_r P_{av}} \cdot (X_{in} + R_{in})}{R_r + R_{in}}. \tag{3.6}$$

The impact of high input reactance $X_{in}$ on the input RF voltage $V_{rec}$ has been examined with different radiation resistance $R_r$ values as shown in Fig. 3.3 assuming that $R_{in} = R_r$ and $R_{loss} = 0$ and the received RF power $-25$ dBm. It can be noticed from the shown results that high radiation resistance can eliminate the desired advantage of high input reactance.

Increasing the quality factor of input impedance extremely would make the voltage gain very sensitive to the frequency because of the impedance mismatch. The model shown in Fig. 3.1 has been simulated to examine the variation of voltage gain of $V_{rec}$ versus frequency with different quality factor $Q$ values. The simulation based on using ideal RF power source with center frequency of 850 MHz and frequency range from 800 MHz to 900 MHz while ($R_{in} = R_r$), Fig. 3.4 shows the simulation results.

It can be seen that the voltage gain $A_{v_{match}}$ is maximum at center frequency with high quality input impedance, but the frequency bandwidth is narrow.
The voltage gain decreases sharply when the operating frequency deviates from the center frequency so that the advantage of high quality input impedance fades away. On the other side, the mismatch influence of the low quality LC resonator is less affected by the frequency. Within some limits, it is possible to calm the response of the RF voltage gain to the frequency by using moderate input resistance and radiation resistance values. Therefore, there is an optimum trade-off between using RF rectifier with high input reactance $X_{in}$ and using antenna with high radiation resistance in order to get sufficient input RF $V_{rec}$ with low input power and wide frequency range.

### 3.3 Proposed CMOS RF Energy Harvesting System

Various RF energy harvesting systems are previously presented in literature in order to obtain an accepted DC output voltage from low input power. RF energy harvester has been given to utilize a high input impedance of the rectifier to maximize the RF input voltage and improve the sensitivity [41]. Despite of its high sensitivity, the system needs for an off-chip control loop circuit to provide an adaptive matching network. Furthermore, the given sensitivity of $-27$ dBm is reached at singly frequency of 868 MHz. High efficiency RF rectifier has been presented in [15] is based on threshold voltage compensation technique. The rectifier efficiency reaches to 32% at $-15$ dBm with a sensitivity of $-20.5$ dBm for the frequency range from 902 MHz to 928 MHz. However, it is difficult to receive such high power levels from RF ambient sources as explained in Section. 2.2.1. A boost converter circuit can be connected to the rectifier in order to increase the
output voltage as proposed in [35]. High sensitivity of $-25.5$ dBm was reached at a single frequency of 2.2 GHz. Off-chip coupling capacitors were needed for the charge pump. A similar concept was adopted by [31] but with a fully integrated system. The achieved sensitivity was relatively low at $-17.5$ dBm for a single frequency of 900 MHz.

In this work, a CMOS RF energy harvester is proposed that can work with ultra-low input power giving highest possible output DC voltage. Moreover, the intended system aims to show smooth response vs frequency within the chosen bandwidth. The RF rectifier is preferable to work with familiar antenna type of typical $50\,\Omega$ impedance. On one hand, such antennas can be available commercially at an economical cost with desired characteristics. On the other hand, as mentioned in Section 3.2.2, the source resistance should not be large because this would decrease the desired RF voltage gain by resonance, and it should not be small because this would make the voltage gain by resonance becoming sensitive to the frequency. Therefore, a resistance with $50\,\Omega$ is a moderate desirable value.

Furthermore, it is suggested to support the RF rectifier by additional charge pump based DC-DC up converter giving higher output DC voltage for less input power. The CMOS RF energy harvesting system consist simply of two main blocks, RF rectifier and the DC-DC up converter as shown in Fig. 3.5.

In order to investigate the feasibility of the proposed solution, a comparison has been made between adding further RF voltage multiplying stages and adding a multistage charge pump as shown in Table 3.1.

The charge pump advantages are: lower power losses and higher voltage up-conversion gain in comparison with RF rectifier. On the opposite side, the RF rectifier is advantageous by smaller coupling capacitors and no driving circuits needed. The coupling capacitors in the charge pump are related directly to load current and inversely to the clock frequency so that the size can be reduced with low load current as expected in this application. The DC-DC up converter can
Table 3.1: Additional RF multiplying stages vs charge pump

<table>
<thead>
<tr>
<th>RF multiplying stages</th>
<th>charge pump stages</th>
</tr>
</thead>
<tbody>
<tr>
<td>High switching losses due to higher operating RF frequency</td>
<td>Less switching losses because the driving clock frequency is low</td>
</tr>
<tr>
<td>Lower efficiency with $V_{gs} \leq V_{th}$</td>
<td>Higher efficiency with $V_{gs} \geq V_{th}$</td>
</tr>
<tr>
<td>Less added DC voltage for added stages because $V_{rec}$ is low</td>
<td>Higher added DC voltage for additional stages because $V_{in}$ is relatively high</td>
</tr>
<tr>
<td>No driving circuit needed to operate the rectifier</td>
<td>Driving circuit is necessary for the charge pump consuming additional power</td>
</tr>
<tr>
<td>Small coupling capacitors with high RF frequency</td>
<td>Large coupling capacitors with low driving clock frequency</td>
</tr>
</tbody>
</table>

be helpful rather than too many stages in RF rectifiers only when the power consumption of the charge pump is minimized. The minimum required input voltage of the charge pump is an essential parameter because it affects its design and the architecture of the RF rectifier. As the charge pump can be powered up with low input voltage, a minimum rectified DC voltage is needed and a minimum input RF power is sufficient. Design methodology, circuit topology and optimization of both RF rectifier and charge pump including the driving circuit will be explained in the following sections. The charge pump is designed to boost the rectified DC voltage $V_{rec,DC}$ up to maximum possible output voltage with minimum $I_{in,rms}$ drawn by the charge pump. For low input RF power, it is required from the rectifier to provide sufficient DC power able to start up the charge pump. In summary, a highly sensitive RF energy harvesting system is enabled to work with a wide frequency bandwidth.

3.4 Low Power RF Rectifier

RF rectifier is the main power conversion circuit in RF energy harvesters which convert RF power to DC power. It can be constructed using low threshold Schottky diodes or CMOS devices. The AC-DC rectifier in general has to deal with several challenges like the switching losses and the conduction losses which have been detailed in Section 2.4.3. Moreover, the RF low input voltage (less than $V_{TH}$) and the leakage current which is dominant in subthreshold region are additional obstacles face the rectifier. Such problems would decrease the output DC voltage. The RF rectifier in this application is preferable as it has high $X_{in}$.
Chapter 3 RF Energy Harvesting System using Low-Power Charge Pump

![Equivalent circuits of pad and package connections including parasitic components.](image)

Fig. 3.6: Equivalent circuits of pad and package connections including parasitic components.

for high input RF voltage $V_{\text{rec}}$ as explained before. The parasitic capacitances of the pads, package and $ESD$ diodes, shown in Fig. 3.6, decrease the quality factor of the input impedance, especially with high frequency. The circuit principles and topologies of the most used AC-DC rectifier types have been discussed in Section 2.4.1.

### 3.4.1 Design of Differential Cross-Coupled RF Rectifier

The circuit of a multistage differential input cross-coupled rectifier is shown in Fig. 2.34. The cross connection of the four transistors in every stage gives a simple solution to eliminate the threshold voltage drop without using additional power consuming circuits. Additionally, the symmetrical property of the rectifier circuit topology is useful to cancel all even order harmonic currents and suppress the power losses caused by them. Another advantage of the differential rectifier is its high input reactance $X_{\text{in}}$. The signals $V_{\text{rec}}$ and $V_{\text{RF}}$ are added at the differential input pads of the rectifier leading to the parasitic capacitance of pads, package and $ESD$ diodes will be halved and $X_{\text{in}}$ is doubled. In comparison with the reviewed RF rectifier types, the cross connected differential rectifier can perform better to overcome the given challenges of RF energy harvesting. Thus, it has been chosen to be implemented in this work with some optimizations.

Since the circuit topology of RF rectifier has been decided, the following step is to optimize the transistor sizes, number of rectifying stages and coupling capacitors giving an accepted performance. Higher efficiency is obtained with wide transistors because this will decrease the losses in $R_{\text{on}}$ resistance, but this will decrease the input impedance and influence the resonance. The number of
3.4 Low Power RF Rectifier

Fig. 3.7: Total power efficiency vs received power at a frequency of 850 MHz and typical 50 Ω RF power source.

stages is chosen as a trade-off between being high for higher output DC voltage and low for high RF voltage gain by resonance. For every number of stages, there is an appropriate device size enabling the rectifier to produce highest output DC power. In order to find the optimum number of stages, the rectifier circuit shown in Fig. 2.29 has been simulated with different numbers of stages and different device sizes using 0.13 um CMOS technology. Low-threshold devices were used while PMOS transistor width $W_p$ is two times larger than that of an NMOS $W_n$ to compensate the lower mobility of holes. A 50 Ω RF power source was used with power range of $-30$ dBm to $-16$ dBm given as received power. Fig. 3.7 and Fig. 3.8 show the simulation results of efficiency with the DC rectified voltage at maximum output power vs input power respectively, for every number of stages with its suitable transistor width.

It can be seen that using few number of stages, small device size is optimum to enhance the quality factor of input impedance giving highest RF voltage gain $A_{v_{match}}$. The achieved efficiency is low because of the high on-resistance of CMOS transistors while low DC voltage because of low number of stages used. On the opposite side, using large number of stages require wider devices giving higher output DC voltage, but, wider devices decrease the RF voltage gain $A_{v_{match}}$ and increase the switching losses so that efficiency is low. Efficiency is increased using four stages and moderate device size to reach 42% with output DC voltage of 0.72 V. This represents a solution for the trade off between enhancing the quality factor of the input impedance and reducing the ohmic
losses across the rectifying transistors. The DC voltage is further increased using six stages with a slight decrease in efficiency to 40%. The six-stage rectifier was chosen as an optimum for high efficiency and acceptable output DC voltage.

3.5 Low-Power Charge Pump

The circuit topologies of charge pumps have been detailed in the previous chapter including the advantages and disadvantages of every topology and its relevance to the application of low-power DC-DC up conversion with low input voltage. The most appropriate design is the cross-coupled charge pump and it has been chosen in this work because of several reasons as will be discussed in this section in addition to the circuit design optimization and added modifications.

3.5.1 Design of Cross-Coupled Charge Pump

The circuit of the cross-coupled charge pumps and their operational concept have been given in Section 2.4.2. The cross-coupled charge pump gives a simple method to cancel the $V_{th}$ drop across the PMOS and NMOS switches without using auxiliary circuits [51]. Elimination of the auxiliary circuits would avoid the charge sharing between the coupling stage capacitors and parasitic capacitors in these circuits used to bias the charge transfer switches. Besides that, the switching signal passes directly to the gates of the switches without additional control devices which can add time delay and increase the reverse current. The
3.5 Low-Power Charge Pump

risks of applying high potentials across low voltage devices and gate over-stress are avoided also in this topology because the voltage difference between the switches is equal to the input voltage $V_{rec,DC}$ [50].

Several modifications and optimizations have to be applied to the typical structure of the cross-coupled charge pump to fit optimally for the application in this work. The following sections discuss these added adjustments including the proposed driving circuits.

**Reverse Bulk Biasing**

It is important to notice that the main challenge in this topology and other topologies of low input voltage is the bulk biasing which increase the $V_{th}$ of NMOS devices in the last stages when the bulk terminal is connected to ground. Therefore, a triple-well process is necessary in order to avoid the negative influence of body biasing. It is possible to take advantage of the bulk biasing to alter the $V_{th}$ of the charge transfer switch according to its on or off states. The CMOS transistor can work as an efficient switch when the drain current $I_d$ is maximum during the on state and leakage current $I_{leakage}$ is minimum during the off state. In order to decrease the leakage current, it is preferable to decrease the threshold voltage of the device when it is on and increase it when it is off because leakage current relates inversely to the forward voltage $V_{th}$. The bulk terminal voltage affect the threshold voltage $V_{th}$ according to following equation

$$V_{TH} = V_{THo} + \gamma \left( \sqrt{|2\Phi + V_{sb}|} - \sqrt{|2\Phi|} \right), \quad (3.7)$$

where $V_{tho}$ is the threshold voltage when the source-bulk voltage $V_{sb}$ is zero, $\gamma$ is the body effect coefficient and $\Phi$ is the Fermi potential.

Forward body biasing refers for negative $V_{sb}$ in NMOS device or positive $V_{sb}$ in PMOS device, $V_{th}$ is decreased and this is referred as forward body biasing which is useful during on state to increase the $I_d$. The same principle is applied inversely by positive $V_{sb}$ in NMOS device or negative $V_{sb}$ in PMOS device so that $V_{th}$ is increased and this is referred as reverse body biasing which is needed to eliminate the leakage current as given in Eq. 2.15.

Suppressing the leakage current is very important to reduce the power consumption of charge pump, reverse bulk body biasing have been utilized in cross-connected charge pump as shown in Fig. 3.9. The bulk of every PMOS device is connected to the capacitor of next stage to give a positive $V_{sb}$ and higher $V_{th}$ when the device is off. Similarly, the bulk of every NMOS device is connected to the capacitor of the previous device to give a negative $V_{sb}$ when it is off.
Chapter 3 RF Energy Harvesting System using Low-Power Charge Pump

Charge Pump Optimization

The charge pump is adjusted including the charge transfer switches sizes, number of stages, size of coupling capacitors and clock frequency according to the desired conditions. Minimum $V_{\text{rec,DC}}$ and R.M.S. drawn current $I_{\text{in,\text{rms}}}$ are aimed when start up the charge pump which has to boost up the output voltage as high as possible across a capacitive load. Wide device size is desirable for higher $I_{\text{load}}$, but it increases the switching losses and $I_{\text{Leakage}}$. Similarly, high clock frequency is desirable for higher $I_{\text{load}}$ and small stage capacitor, but it causes higher switching losses as well. It is expected in this application to supply the output voltage to a capacitive load as mentioned before so that it is not needed to consider high load current requirements.

The structure shown in Fig. 3.9 was simulated using low threshold 0.13 $\mu$m CMOS devices and ideal pulse voltage sources connected to the stage capacitors to reach optimum design parameters. Transistor sizes have been minimized to 150 nm to reduce the power losses. For the same reason, a low frequency of 200 kHz was chosen while the stage capacitors can be kept small as 2.5 pF. Using a lower frequency would necessitate large capacitors and decrease the output voltage. The charge pump was built with 7 stages as trade-off between higher output voltage and high $I_{\text{in,\text{rms}}}$.

It is not helpful to scale up the switch sizes of the initial stages because leakage current losses increase dominantly especially with low input voltage.

Fig. 3.9: Cross-coupled charge pump using reverse bulk biasing.
3.5.2 Driving Clock Generator

The cross coupled charge pump run with two out-of-phase clocks that are applied oppositely to every stage. The ring oscillator consisting of an odd number of inverters can generate the clock signal while the oscillation frequency is defined by the signal delay across every inverter stage and number of inverters. Low supply voltage is the key challenge to design a low power ring oscillator because of the given reasons before. Using long devices is helpful in such application to reduce the power consumption of the oscillator while it is beneficial to give low frequency signal rather than adding extremely large number of inverters.

The second challenge to the design of low power ring oscillator is that the frequency increases strongly with the supply voltage. Consequently, the power losses increase heavily for small raise in $V_{rec,DC}$. It is possible to stabilize the clock frequency with supply voltage by a current biasing circuit. However, these types of circuits require high supply voltage and consume high power in comparison to the rectified DC power from RF rectifier. In this work, it is proposed to supply the oscillator by a low power reference voltage circuit instead of $V_{rec,DC}$. This would keep low oscillation frequency and maintain low switching losses for high $V_{rec,DC}$.

The proposed reference circuit topology shown in Fig. 2.18(b) and explained in Section. 2.3.3 can be utilized in this application to generate a constant voltage reference for slightly higher supply voltage. This reference circuit is advantageous by its simplicity and the ability to give multiple reference values with horizontal and vertical cascading. The output voltage of the reference circuit $V_{out,ref}$ is related to the supply voltage as

$$V_{out,ref} = \begin{cases} V_{rec,DC} & \text{for } V_{rec,DC} < V_{ref} \\ V_{ref} & \text{for } V_{rec,DC} \geq V_{ref} \end{cases} \quad (3.8)$$

This circuit consumes not more than few nano watts for low $V_{DD}$ while it does not require high supply voltage. The circuit shown in Fig. 2.18(b) was simulated using standard CMOS devices in a single column with one NMOS transistor and 9 PMOS transistors. The devices have been sized to generate a voltage reference of 250 mV. The simulation results given in Fig. 3.10 show that the output voltage being close to the defined level when $V_{rec,DC}$ is higher. It is possible to reduce the drawn current but the circuit was optimized to be able to supply power to the oscillator circuit in this application or other reference circuits as will be discussed later. However, this reference circuit has low performance with regard to the temperature variation.

The clock signal will have maximum peak-peak voltage equal to $V_{ref}$ since the oscillator is supplied by the reference circuit. Therefore, additional circuit is required to have a peak-peak voltage equal to the input $V_{rec,DC}$ of the charge pump. As mentioned before, the reference circuit can be cascaded vertically.
and horizontally giving higher reference voltage values. This principle can be utilized to generate higher reference voltage by using a similar reference circuit while the drain of last PMOS transistor is connected to the output terminal of lower $V_{\text{ref}}$. The higher $V_{\text{ref}}$ circuit was optimized to reach 350 mV supplied to an inverter following the oscillator giving a clock signal with higher peak-peak voltage. The latter signal would be able to drive an inverter supplied directly from $V_{\text{rec,DC}}$ of the charge pump. Additional driving inverters enlarged sequentially are connected to be able to charge up the stage capacitors in charge pump. Fig. 3.11 shows the block diagram of the driving clock generator connected to the charge pump.

![Fig. 3.10: Reference voltage $V_{\text{ref1}}$ vs $V_{\text{rec,DC}}$.](image)

The charge pump based DC-DC up-converter has been simulated with input DC voltage range of 0 mV to 800 mV according to the proposed driving circuit. The input voltage increase with time as expected when the input RF power increases and the rectified DC voltage getting raised as well. The simulation results shows that the output peak-peak clock signal is equal to the input voltage of charge pump as shown in Fig. 3.12. The oscillation frequency starts increasing when $V_{\text{rec,DC}}$ is less than $V_{\text{ref1}}$ and it is stabilized on 200 kHz for higher input voltage. The simulations show that the charge pump is able to give more than 1 V when $V_{\text{rec,DC}}$ is 200 mV at a power consumption of 90 nW. Impediments of power consuming driving circuits have been solved by low power solutions. In comparison with high number of stages in RF multiplier, the sensitivity can be improved using such DC-DC up-converter.
3.6 System Implementation

The Tape-out of the suggested system has been achieved using CMOS UMC 0.13 µm technology. Low threshold devices were used in RF rectifier for low \( V_{rec} \) as expected. Low threshold devices have also been used in the charge pump in order to enable start-up of the DC-DC up-converter with low input voltage while triple-well NMOS transistors were required in order to avoid the substrate biasing. In the ring oscillator, standard devices were utilized in order to guarantee low frequency and low drawing current. MIM capacitors have been used with 1 pF in RF rectifier and 2.5 pF in the charge pump. The rectifier output store capacitor was chosen to be 10 pF. The sizes of capacitors were optimized in trade-off between optimum performance and area considerations. ESD protection diodes were used with typical pads according to the chosen technology in input and output pins. The layout area of the system is \( (0.5 \times 0.5) \text{ mm}^2 \) (Fig. 3.15) within a total area of \( (1.6 \times 1.6) \text{ mm}^2 \) for multiple systems chip as shown in Fig. 3.14. The chip is packaged in a 48-pin QFN package with 0.5 mm pin pitch.
Chapter 3 RF Energy Harvesting System using Low-Power Charge Pump

Fig. 3.12: Clock signal with peak-peak equal to $V_{rec,DC}$.

Fig. 3.13: Oscillation frequency stabilization with $V_{rec,DC}$. 
Fig. 3.14: Chip micro graph of the RF energy harvesting system within a tape-out using UMC 0.13um technology and total area of (1.6x1.6)mm².

Fig. 3.15: Layout of the proposed energy harvesting.
3.7 Experimental Results Using RF Power Source

In order to test the fabricated CMOS RF energy harvester, a Printed Circuit Board (PCB) referred as Board1 has been designed to measure the system functionality as well as the performance of each circuit block. The board was fabricated using FR4 substrate with two layers and a thickness of 1.55 mm with area of \((5 \times 5) \text{ cm}^2\). The board is connected to the power source with 50 \(\Omega\) via an SMA connector so that the chip is supplied by the input RF power with the targeted bandwidth 800 MHz to 900 MHz. The designed rectifier has differential inputs so that balun is needed with 50 \(\Omega\) impedance for balanced and unbalanced ports. Off-chip SMD inductors were used for matching the source to the input impedance of the rectifier. The harvested energy is stored in external capacitor where the output DC voltage is measured. Fig. 3.17 shows the test PCB with the chip placed in the center surrounded with other mentioned components.

3.7.1 Test Procedure

The test setup is based on measuring the system sensitivity to produce 1 V across unloaded capacitor with frequency range of 800 MHz to 900 MHz. It is necessary to define matching network between the source impedance and the input impedance of the rectifier. The charge pump is coupled to RF rectifier and influences its input impedance. For simplification, the charge pump is modeled as a resistor determined by measuring the drawn \(I_{\text{in},rms}\) with minimum required \(V_{\text{rec,DC}}\) to produce 1 V across the output capacitor. The resistor value is compensated back in a simulation test bench shown in Fig. 3.16. Other parasitic capacitors and inductors of pads, package and ESD diodes are taken into account to find the required inductance value in matching network.

3.7.2 Measurement Results of Charge Pump

Fig. 3.19 shows the output voltage of the DC-DC up-converter and the drawn \(I_{\text{in},rms}\) versus input voltage applied from DC power supply. The maximum impedance of voltmeter \(R_{\text{voltmeter}}\) is about 10 M\(\Omega\) while it is intended to measure the voltage with a capacitive load. Therefore, a series resistance of 90 M\(\Omega\) is connected in series to the voltmeter (Fig. 3.18) so that the output voltage is measured by the voltage reading with a multiplication factor according to

\[
V_{\text{out}} = V_{\text{voltmeter}} \cdot \frac{R_{\text{s,meas}} + R_{\text{voltmeter}}}{R_{\text{voltmeter}}},
\]

where \(R_{\text{s,meas}}\) is the added series resistance, \(R_{\text{voltmeter}}\) and \(V_{\text{voltmeter}}\) are the voltmeter impedance and readings, respectively. This factor can be calibrated by applying 1 V across the total impedance and measuring the \(V_{\text{voltmeter}}\). The
3.7 Experimental Results Using RF Power Source

charge pump is able to produce more than 1 V for input DC voltage of 0.2 V with a power consumption of less than 100 nW. It is important to notice that the charge pump is switched off for input voltage of more than 1.3 V. This voltage is high enough for the driving inverters to show continuous state since the maximum peak-peak input clock signal is limited by $V_{ref2} = 0.35$ V as was shown in Fig. 3.11. However, this is helpful as a protection for the charge pump against extremely high input DC voltage.

3.7.3 Sensitivity Measurements of RF Energy Harvester

Once the matching network is defined in a procedure explained in Section 3.7.1, it is possible to measure the system sensitivity using an RF power source and balun with the mentioned frequency range. An off-chip balun from *HHM series* was used with an insertion loss of 1.4 dB according to the data sheet. Fig. 3.21 shows the measurements results of $V_{out}$ vs input RF power at the center frequency of 850 MHz. The output voltage can be more than 1 V for input power of $-23.5$ dBm. Taking into account the balun and cable losses, the system sensitivity for 1 V across the output capacitor can be defined to be better than $-25$ dBm. It is clear from the measurement results that the output voltage is related directly to the input power and increases to reach more than 5 V for input power of $-9$ dBm. The charge pump would switch off with higher input power when $V_{rec, DC}$ reaches 1.3 V as mentioned in the previous section.

In order to test frequency influence on the sensitivity, the output voltage was measured with frequency range of 800 MHz to 900 MHz and input power of
Fig. 3.17: Sensitivity measurements using RF4 PCB and RF source.
3.7 Experimental Results Using RF Power Source

RF source
50Ω

Balun

DC decoupling

Matching

RF Rectifier

C. P.

DC Power supply

V_{rec,DC}

Fig. 3.18: Charge pump and sensitivity measurement setup.

Fig. 3.19: Measurements of the output voltage and drawn current of the charge pump.
Fig. 3.20: Measurement of $S_{11}$ parameter using of Board1 with the extracted matching network (Section. 3.7.1).

Fig. 3.21: System sensitivity measurement with center frequency of 850 MHz.
3.8 Design of PCB Antenna for RF energy harvesting

Fig. 3.22: Measurements of frequency influence on the sensitivity.

−23.5 dBm as shown in Fig. 3.22. The CMOS RF energy harvester keeps giving more than 1 V with frequency range 800 MHz to 870 MHz and decreases smoothly with higher frequencies. The input impedance of the RF rectifier with moderate $R_{\text{in}}$ value and sufficient quality factor enable the system to show stable response for wide frequency bandwidth.

3.8 Design of PCB Antenna for RF energy harvesting

The antenna is a component in which the radiation or reception of EM waves has been optimized for certain frequency ranges by fine tuning of design properties [13, p.118]. The electromagnetic wave is generated by the transmitting antenna to be propagated in far-field environment. In opposite, the receiving antenna resonates at the same frequency of the radiated EM to induce an electrical RF signal. The antenna is considered as a major complementary element to RF-EH as it collects the incoming RF signals of various frequencies and converts them to electrical power. In this work, it is intended to prove the ability of the given CMOS RF-EH which has been designed and fabricated to perform successfully in normal environment of wireless power transfer using a proposed PCB antenna. Therefore, general information for antenna characteristics and types would be given briefly in this section as well as the designed and fabricated antenna.

3.8.1 Antenna Characteristics

Definitions of the most known parameters of antenna:
Chapter 3 RF Energy Harvesting System using Low-Power Charge Pump

Directivity and Gain

For an isotropic emitter, the energy is radiated uniformly in all directions. At distance of $r$, the radiation density $S$ can be calculated as \[S = \frac{P_{EIRP}}{4\pi r^2},\] (3.10)
where $P_{EIRP}$ is the Effective Isotropic Radiation Power. For a real antenna, the radiation density is greater in the preferred direction of the antenna. Fig. 3.23 shows the difference between radiation patterns of directional antennas and isotropic emitter. It can be seen that the radiation density is focused in one direction to be more than that of isotropic emitter by a certain factor. This factor is referred to as the gain of the antenna $G_i$. The radiation density can be taken into account via the gain effect as \[S = \frac{P_t G_i}{4\pi r^2},\] (3.11)
where $P_t$ is the given power to the antenna. The antenna design may include reflectors in order to increase the directivity, $D$, which defines the ability of the antenna to radiate in a specific direction. The $G_i$ is related to $D$ and efficiency of antenna $\eta_{antenna}$ as [23]:
\[G_i = D \eta_{antenna}.\] (3.12)

The $\eta_{antenna}$ depends mainly on the loss tangent of the substrate and the resistive losses of the metal. Furthermore, both $\eta_{antenna}$ and $D$ are strongly frequency dependent.
Effective Aperture

The maximum power received by antenna referred as, $P_{inRF}$, is related to the power density, $S$, and effective aperture, $A_e$, of antenna [13, p.119]

$$P_{inRF} = A_e.S.$$ \hspace{1cm} (3.13)

The $A_e$ is identified according to the antenna design and it determines also the RF power absorbed and transferred to the connected terminating impedance $Z_{in}$. The $A_e$ is related to the gain of antenna as [23]

$$A_e = \frac{\lambda^2}{4\pi} G_i.$$ \hspace{1cm} (3.14)

Antenna Impedance and Radiation Resistance

The antenna impedance has been modeled in Section 3.1 as a complex impedance consisting of $R_r$, $R_{loss}$ and $X_A$. At the resonant frequency of the antenna, $X_A$ tends toward zero. For an ideal antenna when $R_{loss} = 0$, $R_r$ represents the antenna impedance at its operating frequency. $R_r$ is highly important as it affects efficiency of antenna and $V_A$. With the matching condition of $R_r = R_{in}$, the voltage gain at resonance is influenced by $R_r$ in relation to $X_{in}$ as was shown in Fig. 3.3. The value of $R_r$ depends on the antenna type and design as will be explained in the following section.

3.8.2 Antenna Types

Patch Antenna

Patch antenna (Fig. 3.24) consist of a typical PCB substrate metalized on both sides while the bottom side is continuous plate and the top side is a patch rectangle fed via a microstrip [13, p.125]. Large directivity can be obtained due to the ground plane which acts as a reflector. This explains also how the radiation pattern is in semihemispherical form. A patch antenna is advantageous by its miniaturized size and circular polarization, but it is not optimal for this work because it has a single port rather than differential ports needed for the defined RF-EH in this work.

Loop Antenna

Loop antenna is a metallic conductor bent into a closed curve of various shapes like circular, square (Fig. 3.25), elliptical with a gap in this curve to form differential terminals. The main advantage in loop antenna is its small size compared with the wavelength in free space. It is used in different communication applications as a receiving antenna where the signal to noise ratio is mostly
considered rather than efficiency. The loop antenna efficiency is lower than other antenna types because $R_{loss}$ is higher than the radiation resistance $R_r$. However, this low $R_r$ value makes loop antenna not desirable in this work as it is preferable to have moderate $R_r$ value. The loop antenna is not optimum for wide frequency bandwidth performance because the quality factor is quite high (large inductance).

**Dipole Antenna**

In its most basic forms, the dipole antenna is composed of a piece of copper wire with a defined length of $\left(\frac{\lambda}{2}\right)$. The dipole is fed at the halfway along the antenna. The PCB dipole antenna can be realized on a PCB substrate as two rectangular arms hatched on the top layer without bottom ground layer. The
3.8 Design of PCB Antenna for RF energy harvesting

Fig. 3.26: Dipole antenna realizations.

The total length of the antenna is affected since the wavelength calculation is affected by the effective dielectric constant of the substrate $\varepsilon_{\text{eff}}$ of the PCB. The effective dielectric constant is calculated as

$$\varepsilon_{\text{eff}} = \frac{\varepsilon + 1}{2} + \frac{\varepsilon - 1}{2} \left( \frac{1}{\sqrt{1 + \left( \frac{12d_{\text{substrate}}}{W_{\text{dipole}}} \right)^2}} \right), \quad (3.15)$$

where $\varepsilon$ is the dielectric constant of the substrate material, the width of the copper track $W_{\text{dipole}}$ and the substrate thickness $d_{\text{substrate}}$. The length of the dipole antenna, $L_{\text{dipole}}$, is determined as

$$L_{\text{dipole}} = \frac{\lambda}{2} = \frac{C}{2f\sqrt{\varepsilon_{\text{eff}}}}, \quad (3.16)$$

where $\lambda$ is the wavelength, $C$ is the light speed and $f$ is the frequency. However, factors like the gap between the microstrip arms of the dipole has to be taken into account.

For regular dipole realization, the radiation resistance $R_r$ is less than 73 $\Omega$ [13, p.122]. Therefore, it is easy to optimize the width $W_{\text{dipole}}$ and the length $L_{\text{dipole}}$ in order to set the antenna impedance to 50 $\Omega$ at the resonance frequency. It is possible to increase the radiation resistance using the 2-wire folded dipole and 3-wire folded dipole, Fig. 3.26 shows the mentioned dipole realizations. The bandwidth of the antenna relate inversely to the quality factor. Increasing the conductor width would decrease the inductance and quality factor consequently giving wider bandwidth.

### 3.8.3 Dipole Antenna Implementation

It has been found by the extracted layout simulation that the real part of the input impedance of the chip is 35 $\Omega$ with input power of sensitivity. Consequently,
Table 3.2: Characteristics of the substrate used for antenna fabrication.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate type</td>
<td>FR4, two layers</td>
</tr>
<tr>
<td>Substrate thickness</td>
<td>1.55 mm</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>4.1</td>
</tr>
<tr>
<td>Copper thickness</td>
<td>35 um</td>
</tr>
<tr>
<td>Loss tangent</td>
<td>0.013</td>
</tr>
</tbody>
</table>

The radiation resistance of the antenna should not be too low as in the loop antenna or too high as in the folded dipole antenna. The radiation resistance of the standard dipole is sufficient regarding the input impedance of the chip. Moreover, it is possible to enhance the frequency bandwidth of the antenna with increasing the $W_{\text{dipole}}$. In order to make the measurements feasible with the power source on one side and the spectrum analyzer on the other side, the antenna impedance is preferable to be settled to 50 $\Omega$. It is possible to fabricate the dipole antenna using an economic FR4 substrate with acceptable efficiency and gain. Therefore, standard dipole has been chosen to be implemented in this work.

The antenna has been fabricated using typical FR4 substrate with the characteristics listed in Table 3.2. The copper track width has been chosen to be 10 mm in order to increase the bandwidth. It is intended to use single board for measuring both the RF and thermal energy harvesting systems. For center frequency $f_c$ of 850 MHz, the antenna length is quite long which leads to combining the antenna with the required lumped elements of both systems will make the size of the PCB to be extremely large. Instead of straight rectangular arms, the dipole terminals have been bent to reduce the board length. The bending arcs have been enlarged to eliminate the influence of the track bend. The antenna has been designed for 50 $\Omega$ impedance at center frequency of 850 MHz. Fig. 3.27 shows the layout and radiation pattern of the designed antenna.

### 3.9 Experimental Results Using The Dipole Antenna

The main board *Board2* used for measurements is shown in Fig. 3.28 with size of $(106 \times 105.3)$ mm$^2$. It contains mainly the antenna, harvesting chip, matching inductors and the output capacitor. The differential port of the antenna is connected to the input pins of the chip using matching inductors. Another board (*Dipole*) has been fabricated with exactly similar dipole antenna and the SMA connector only as shown in Fig. 3.29. This board is needed to measure the power received at the harvester point.
3.9 Experimental Results Using The Dipole Antenna

(a) Layout of the designed dipole antenna.

(b) Radiation pattern of the designed dipole.

Fig. 3.27: Design of PCB dipole antenna.
Fig. 3.28: Main board measurement Board2 of RF energy harvesting system.

Fig. 3.29: Dipole Antenna realization using FR4 substrate.
3.9 Experimental Results Using The Dipole Antenna

3.9.1 Test Procedure

In order to determine the matching inductance, it is necessary to calibrate the antenna impedance while the input impedance of the chip is tested from the simulation. Once the matching network is given, the (Board2) is ready to measure the sensitivity of the system using the dipole antenna. The power is transmitted from the power source via the transmitting antenna (Dipole) to be received by (Board2) at a certain distance. The output voltage is measured across the output capacitor at a certain distance from the transmitter and the transmitted power $P_t$. In order to measure the system sensitivity, the received RF power $P_{in}$ is measured using two (Dipole) boards.

3.9.2 Measurements of The $S_{11}$ Parameters

Fig. 3.30 shows a comparison of $S_{11}$ parameters between the simulations and measurements. The measurement results are close to that of the simulation with slight difference in the center frequency of the fabricated antenna of 820 MHz while the center frequency of the simulated design is 840 MHz.

3.9.3 Sensitivity Measurement Using Dipole Antenna

Fig. 3.32 shows the received power $P_r$ and the output voltage $V_{out}$ versus frequency at a distance of 1 m for a transmitted power, $P_t$, of 6.5 dBm. The maximum power received is around $-21.5$ dBm with an output DC voltage, $V_{out}$, of 2.6 V at 820 MHz which is close to the frequency at which minimum $S_{11}$
parameters have been measured (Fig. 3.30). The matching is strongly altered with frequency leading to the input RF voltage, $V_{\text{rec}}$, changes with frequency as well. This explains the sharp fluctuations in the output voltage. One more cause for this wobbling in the power received is the effects of indoor measurement environment (laboratory room). The RF energy harvester in \textit{(Board2)} has been measured at distance of 9.2 m from the transmitting antenna in indoor long corridor (Fig. 3.33). The output DC voltage reaches 2.4 V with power received of $-23 \text{ dBm}$ and frequency of 850 MHz while the transmitted power is ($P_t = 20 \text{ dBm}$).
3.9 Experimental Results Using The Dipole Antenna

Fig. 3.32: Measurements of RF energy harvester at a distance of 1 m from the transmitter and ($P_t = 6.5$ dBm).

Fig. 3.33: Measurements of RF energy harvester using Board2 at 9.2 m distance from the transmitter.
Chapter 4

Low Input Voltage Boost Converter For Thermal Energy Harvesting

4.1 Thermoelectric Generator

The thermoelectric effect has two main effects within: the Seebeck effect, Peltier effect. In 1821, Thomas Johan Seebeck found that a temperature difference between hot and cold junctions of different electrical conductors produces a voltage difference across them as shown in Fig. 4.1. This voltage difference relates directly to the $\Delta T$ between the junctions while the coefficient of a material or device to generate a voltage per unit of temperature is known as its Seebeck coefficient, $\alpha_S$, with a unit of $V/C$. In 1834, Jean Charles Peltier discover the reverse effect. He found out that passing an electric current through a junction of two different conductors could cause it to act as a heater or a cooler depending on the direction of the current. However, the solid state devices used according to Peltier effect can be used in temperature control applications. These devices are called Peltier devices, while same devices can work reversely according to Seebeck effect and used nowadays in TE-H applications. The TEG is composed of a number of $k$ semiconductor thermocouples are organized to create a series electrical connection and thermal parallel connection as shown in Fig. 2.7. The top and bottom of TEG is made of a material that can give an electrical insulation and thermal conductivity simultaneously. When a TEG is attached to the heat source, a heat sink is necessary to be added to the cold side in order to keep the temperature difference between hot and cold sides, otherwise, the entire
Chapter 4 Low Input Voltage Boost Converter For Thermal Energy Harvesting

TEG would heat up to nearly same of $T_h$ temperature erasing the temperature gradient [34].

4.1.1 Thermal and Electrical Model of the TEG

The thermal and electrical characteristics of the TE-H can be used to predict and simulate its behavior for a certain $\Delta T$. It is possible to build simple circuits for this purpose based on the TEG and the attached heat sink. In this section, the thermal and electric circuit models are reviewed briefly according to the literature showing the effects of the related parameters on the produced power DC.

Thermal Resistance Model

In reality, the actual $\Delta T$ across the TEG junctions is lower than the total temperature gradient because of the thermal resistances of heat sinks residing on the cold and the hot sides of the TEG represented by $R_c$ and $R_h$, respectively. The thermal resistance is a measure of the temperature gradient by which an object resist the heat flow. When a heat energy given to different materials attached to each other, the biggest share of energy is utilized by material of higher thermal resistance. Fig. 4.2(a) shows that the thermal resistance of heat sink and TEG determine which portion of the total $\Delta T$ is concentrated across the TEG [34]. The actual temperature difference across the TEG sides is referred as $\Delta T_{\text{TEG}}$ to differentiate it from the total $\Delta T$ and it is calculated as

$$\Delta T_{\text{TEG}} = \Delta T \frac{R_{\text{th.TEG}}}{R_{\text{th.TEG}} + R_h + R_c}, \quad (4.1)$$

where $R_{\text{th.TEG}}$ is the thermal resistance of the thermoelectric generator. In order to minimize the temperature drop across the heat sinks and thermal contacts, the TEG thermal resistance $R_{\text{th.TEG}}$ should be as high as possible in comparison with $R_c$ and $R_h$.

Electrical Model

The electrical behavior of TE-H can be simulated according to the Seebeck effect. The open-circuit voltage $V_{oc}$ across the terminals of the TEG is related to the Seebeck coefficient $\alpha_S$, number of thermocouples in the TEG used and $\Delta T_{\text{TEG}}$ as

$$V_{oc} = n \alpha_S \Delta T_{\text{TEG}} = n \alpha_S (T_h - T_c). \quad (4.2)$$

When the TEG is connected to an input resistance $R_{\text{in,boost}}$ as shown in Fig. 4.2(b), electrical current passes through the circuit and it is determined as

$$I_{\text{in,rms}} = \frac{V_{oc}}{(R_{\text{in,boost}} + R_s)}, \quad (4.3)$$
4.1 Thermoelectric Generator

where \( R_s \) is the TEG internal electrical resistance based on the current-voltage characteristic. The DC power delivered to the connected load \( P_{TEG} \) can be calculated as

\[
P_{TEG} = I_{in}^2 R_{in,boost} = \left( \frac{V_{oc}}{R_{in,boost} + R_s} \right)^2 R_{in,boost} . \tag{4.4}
\]

4.1.2 Choosing TEG Module For Thermal Energy Harvesting

The commercial off-the-shelf TEG modules vary significantly regarding the produced electrical power with \( \Delta T_{TEG} \). The produced DC voltage from the module for a certain \( \Delta T_{TEG} \) depends mainly on the Seebeck coefficient of the TEG. It is possible to increase the open-circuit voltage \( V_{oc} \) by increasing the number of the thermocouples but, this will increase the source resistance \( R_s \) resulting in higher voltage drop when the TEG is loaded. Such a trade-off is noticed in the size of the module, i.e. larger harvester can give higher output voltage for a certain \( \Delta T_{TEG} \) but its \( R_s \) is relatively large. Table 4.1 lists some of the commercially available and recommended by [34]. The \( V_{oc} \) of these modules is 10 mV/K to 50 mV/K with typical source resistances \( R_s \) of 0.5 Ω to 5 Ω according to the TEG size.
Chapter 4 Low Input Voltage Boost Converter For Thermal Energy Harvesting

Table 4.1: Commercial Off-The-Shelf TEG modules with part numbers and manufacturers [34].

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>15 mm²</th>
<th>30 mm²</th>
<th>40 mm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>CUI INC (Distributor)</td>
<td>CP60133</td>
<td>CP60333</td>
<td>CP85438</td>
</tr>
<tr>
<td>FERROTEC</td>
<td>9501/031/030 B</td>
<td>9500/097/090 B</td>
<td>9500/127/100 B</td>
</tr>
<tr>
<td>FUJITAKA</td>
<td>FPH13106NC</td>
<td>FPH17108AC</td>
<td>FPH112708AC</td>
</tr>
<tr>
<td>MARLOW INDUSTRIES</td>
<td></td>
<td>RC6-6-01</td>
<td>RC12-8-01LS</td>
</tr>
<tr>
<td>TELLUREX</td>
<td>C2-15-0405</td>
<td>C2-30-1505</td>
<td>C2-40-1509</td>
</tr>
<tr>
<td>TE TECHNOLOGY</td>
<td>TE-31-1.0-1.3</td>
<td>TE-71-1.4-1.15</td>
<td>TE-127-1.4-1.05</td>
</tr>
</tbody>
</table>

The maximum power supplied from the TEG is reached when the input resistance is equal to the electrical resistance of the TEG. The circuit shown in Fig. 4.2(b) has been simulated with sweeping the input resistance, $R_{in,boost}$, using a constant open-circuit voltage, $V_{oc}$, of 10 mV for different TEG resistances, $R_s$. It is clear by the simulation results (Fig. 4.3) that maximum power is delivered when $R_{in,boost} = R_s$. In opposite, it can be noticed that the input voltage, $V_{in}$, is higher with higher input resistance, $R_{in,boost}$. However, higher input impedance is associated with less input power.

4.2 Proposed DC-DC UP-Converter for Thermal Energy Harvester

As it has been illustrated in the second chapter, the power conversion circuit is necessary because the voltage produced from the harvester (TEG) is less than the supply voltage required to be applied to the load (sensor node). The output signal from the TEG is a DC signal leading to that DC-DC up-converter is needed as a power conditioning circuit. The principles of DC-DC boost circuit design has been explained in details in Section 2.4.2.

Several solutions have been presented in literature to start up the converter system with minimum possible input voltage. The boost converter given by [19] is based on a self start up oscillator with the help of an SMT transformer to work with low input voltage. The system was able to start up with an open circuit voltage of 20 mV. Moreover, maximum efficiency is reached of 40% for an open-circuit voltage of 55 mV. Similar principle has been adopted for start up the boost circuit in [17]. In later step, the system reuse the transformer
4.2 Proposed DC-DC UP-Converter for Thermal Energy Harvester

Fig. 4.3: The power delivered from the TEG to the load as a functions to the input resistance.

Fig. 4.4: The available DC voltage from the TEG to the load as a functions to the input resistance.
as an inductor based boost when the input voltage is high. Despite of higher efficiency reported of 60% at open circuit voltage of 300 mV, the minimum start up voltage is 40 mV. The converter system presented by [45] is based on using coupled inductors of 1:1 turn ratio instead of using SMT transformer with high transformation ratio. This was helpful to minimize the switching losses due to the transformer parasitic capacitance. This circuit was able to start up with minimum open circuit voltage of 21 mV while maximum efficiency was 75% at an input power of 2 mW. However, the maximum DC output voltage was limited to 1 V.

The circuit is chosen and optimized according to the input voltage, $V_{in}$, which is expected to be as low as the available power from the TEG ($P_{TEG}$) as mentioned in Section 2.5.1. The input resistance, $R_{in, boost}$, of the boost circuit might be preferable to be close to $R_s$ in order to extract maximum power from the thermoelectric generator. However, this condition is not optimum for low open circuit voltage $V_{oc}$. This is because the input voltage to the boost will be half of $V_{oc}$ giving that it will be challenging to start up the converter. Therefore, it is proposed to optimize the boost circuit to keep the $R_{in, boost}$ is relatively higher than $R_s$ to obtain an accepted input voltage. This condition is only possible with minimum input current, $I_{in, rms}$, drawn into the converter circuit.

### 4.2.1 Transformer Reuse Self Start-Up Technique

The input voltage is unlikely to start up a regular boost converter. This is because of the limitation of the minimum supply voltage required for the driving signal circuit. Consequently, the DC-DC work in two phases, the self start-up phase and inductor based boost phase. The circuits associated with both operation phases will be explained in details in Section 4.3 and Section 4.4. The self start-up phase based on using a current sense SMT transformer to generate an oscillated AC signal spontaneously. The generated AC voltage is rectified by a rectifying diode giving DC output voltage as shown in Fig. 4.5(a). In the second phase, the circuit is switched to inductor based boost phase using the secondary inductor of the transformer as shown in Fig. 4.5(b).

The self start-up phase is necessary to initiate the circuit. However, it is associated with high power losses in comparison to the inductor based boost phase (as will be discussed later in this chapter). During self start-up phase, when the input voltage, $V_{in}$, is high, the secondary voltage would be extremely high because of the high transformation ratio given by the transformer. Thus, the circuits connected to the secondary inductor might be damaged due to the extra high voltage. On the other hand, it is possible to optimize the inductor based boost to give voltage conversion ratio higher than that given by self start up oscillator. Therefore, it is preferable to switch the operation phase to the inductor based boost phase once the output DC voltage is high enough to run its related driving
4.3 Design of Self Start-UP Oscillator

4.3.1 Self Start-Up Techniques

The self start up oscillator circuit is needed when the input voltage is extremely low so that it is not able to power the DC-DC up converter. Instead of using charge pump or inductor based boost converters, simple oscillator is used to generate an AC voltage which can be further processed via a rectifier or a voltage multiplier circuit. In this section, the self start up oscillator circuit topologies are reviewed including the advantages and drawbacks of every circuit.
Chapter 4 Low Input Voltage Boost Converter For Thermal Energy Harvesting

4.3.2 LC Based Start-Up Oscillator

This low voltage starter circuit is based on using LC tank oscillator. The circuit shown in Fig. 4.6 illustrate an LC oscillator with cross coupled NMOS transistors. Simply, the LC tank resonates at a frequency, \( f_{osc} \), given as

\[
f_{osc} = \frac{1}{2\pi \sqrt{L_s C_{osc}}}. \tag{4.5}
\]

In reality, the inductor is associated with series ohmic resistance, \( R_{L, esr} \), determine its quality factor, \( Q \). The series resistance is modeled as a parallel resistor, \( R_p \), calculated at resonance as [29, p.497]

\[
R_p \approx \frac{L^2 \omega^2}{R_{L, esr}} \approx \frac{L_s}{R_{L, esr} C_{osc}} \text{ with } L_p \approx L_s. \tag{4.6}
\]

In order to minimize the \( VDD \) voltage required for oscillator, low threshold voltage or native NMOS transistors can used. The oscillation start up condition is given in [48] as

\[
VDD > \frac{4}{R_p g_{m,n}} + V_{th,n} \Rightarrow VDD > \frac{4L_s}{R_{L, esr} (C_{osc} + C_p) g_{m,n}} + V_{th,n}, \tag{4.7}
\]

where the \( C_p \) is the parasitic capacitance of the native NMOS transistors. The series resistance, \( R_{L, esr} \), is small leading to the DC level of \( V_{osc} \) is close to the
supply voltage, therefore, the peak point of the oscillation voltage exceeds \( V_{DD} \). The circuit can be optimized properly to give peak to peak voltage swing larger than \( V_{DD} \).

Since the output voltage from the oscillator is still low, it needs a further voltage multiplying circuit in order to produce an accepted DC voltage as shown in Fig. 4.7. Such a conversion circuit is loaded to the oscillator while its input capacitance and resistance will affect the oscillation frequency as well as the conditional start up voltage. The voltage multiplying circuit can be optimized so that wider devices are needed with large number of stages in order to avoid increasing the load resistance of the oscillator. Moreover, the parasitic capacitance can be effective, especially, when the NMOS transistors are enlarged to increase the \( g_m \). Eq. 4.7 can be rewritten as

\[
V_{DD} > \frac{4L_s}{R_{L,esr} (C_{osc} + C_p + C_{mv}) g_{m,n}} + V_{th,n}.
\]  

(4.8)

where \( C_{mv} \) is the input capacitance of the voltage multiplier circuit. The sizes of coupling capacitors are reversely related to the oscillation frequency. High frequency is also relatively desired to decrease the minimum supply voltage needed to start up the oscillator. High frequency on the other hand leads to high dynamic losses as mentioned in Section 2.4.3. The main drawback in this method is the need for conversion circuit associated with typical power losses. Another drawback in using \( LC \) self start up oscillator is that it has low voltage conversion ratio even with large number of voltage multiplier stages being added. For an input voltage of 50 mV, the output AC signal can be ranges from 100 mV to 150 mV with proper design, but, this will need large number of voltage multiplier stages to reach an accepted output voltage.

### 4.3.3 Transformer Based Start-Up Oscillator

The transformer based oscillator consists basically of a common source amplifier loaded by an \( SMT \) transformer with a transformation ratio of \( N_{SMT} \) as shown in Fig. 4.8(a). The polarity between the primary and the secondary transformer windings can be used with the inverter amplifier to compose a positive feedback loop. The noise signal generated at the gate of the NMOS transistor, \( S_{osc} \), is translated into a drain current passing through the primary inductor of the transformer. Consequently, a primary voltage of \( V_{prm} \) is given across the primary side of the transformer leads to a secondary voltage of \( V_{sec} = N_{SMT} V_{prm} \) across the secondary side. The \( V_{sec} \) is fed back positively to the \( S_{osc} \) giving higher drain current and higher \( V_{prm} \) so that the generated AC voltage is maximized by resonance. The oscillation frequency \( f_{osc} \) is determined by

\[
f_{osc} = \frac{1}{2 \pi \sqrt{L_{sec} (C_{se} + C_{gs} + C_d)}}.
\]  

(4.9)
where $L_{sec}$ is the secondary inductance of the transformer and $C_{sc}$ is the self capacitance of the secondary winding. The main condition to start up the oscillation is

$$\text{Positive feedback loop gain} > 1 \Rightarrow \frac{g_m (R_p || R_g)}{N} > 1,$$

where $R_p$ is calculated from the $R_{L, esr}$ of the secondary inductor in similar way to that given in Eq. 4.6 and $R_g$ is the resistive part of the input impedance of the transistor $S_{osc}$. The $R_g$ can be effective for extremely wide transistors so that it can influence the loop gain. On the other hand, the transconductance increases with the transistor width and the gate source voltage $V_{gs}$. There is a trade off with wider devices between high transconductance on one hand and low quality factor ($f_{osc} \propto \frac{1}{C_{gs}}$) and relatively low loop gain on the other hand.

In comparison with LC based start up oscillator, the transformer based oscillator is advantageous by higher voltage conversion ratio and less power losses. The transformer based self start up technique given in Section 4.3.3 is chosen to be used in this work to start up the DC-DC converter. As mentioned before, the $SMT$ transformer is reused for inductor based boost once the output voltage reach a defined level. In order to reach the switching point with minimum $V_{in}$ possible, it is preferable to use a transformer with high transformation ratio in order to obtain high output voltage in consequent. An $SMT$ transformer has been chosen with characteristics listed in table 4.8.

As it was given in Eq. 4.10, high $g_m$ is necessary to minimize the start up input voltage. Thus, the transistor, $S_{osc}$, has to be wide enough in order to
4.3 Design of Self Start-UP Oscillator

(a) Oscillator circuit.  
(b) Equivalent model LC combination with parasitic components.

Fig. 4.8: Transformer based self start up oscillator.

Table 4.2: Characteristics of the current sense transformer used for the boost converter.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer, MFG P/N</td>
<td>Pulse electronics, P8208NL</td>
</tr>
<tr>
<td>Turns ratio</td>
<td>1 : 100</td>
</tr>
<tr>
<td>Secondary Inductance $L_{sec}$</td>
<td>2 mH</td>
</tr>
<tr>
<td>DC resistance of $L_{sec}$</td>
<td>5.5 $\Omega$</td>
</tr>
<tr>
<td>Parasitic capacitance $C_{se}$</td>
<td>$\approx 46$ pF</td>
</tr>
</tbody>
</table>
obtain high transconductance. Native NMOS transistor is not desirable because it has long channel length. It is associated with extreme large $C_{gs}$ getting less $Q$. The leakage current is dominant in native devices, especially, with quite wide devices. Low threshold NMOS transistor is an alternative solution since it is advantageous by less parasitic gate-source capacitance and less leakage current in comparison to the native transistor. When the converter switches to the inductor based boost phase, the transistor $S_{osc}$ has to be turned off, otherwise, high power losses are wasted via current passing through the primary inductor. Therefore, additional circuit is necessary to control the NMOS transistor $S_{osc}$ according to the operation phase. Low threshold PMOS transistor is proposed in this work to build a positive feedback loop as shown in Fig. 4.5(a). The PMOS transistor is turned off automatically once the converter switches to inductor based boost so that no control circuit is needed. The bulk terminal can be connected to the output voltage increasing the threshold voltage and reducing the leakage current. The transformer based self start up oscillator has been designed using CMOS UMC 0.13 um technology. Wide low threshold PMOS transistor has been used with minimum channel length. Diode connected standard PMOS transistor has been used for rectifying the generated AC signal. In order to simulate the oscillator circuit, the TEG is modeled as DC voltage source connected with series resistance of ($R_s = 2.5 \, \Omega$) as an average of the source resistances of the typical commercial TEG modules. A Large capacitor of 100 uF is connected across the input terminal of the converter. The big capacitor serves as an RF bypass to ground and supply a smooth input voltage to the converter. The simulation results shows that the oscillator can start up with an oscillation frequency of 434 MHz for open circuit voltage $V_{oc}$ of 10 mV.

### 4.3.4 Negative Voltage Rectifier

The boost switch, $S_{boost}$, is preferable to be wide enough to draw high current into the boost converter and to obtain an accepted power transfer from the source to the load. Even when the gate voltage of the boost switch is grounded, the leakage current is still dominant. This is because the device is quite large with wide width. The leakage current influence the oscillation start up negatively, especially, with low input voltage. It is proposed to bias the boost switch with a negative voltage during the self start up phase. Voltage rectifier is fed by the secondary voltage $V_{sec}$ in order to obtain a negative DC voltage. The rectifier consists of two stages voltage doubler circuit built with standard PMOS devices as shown in Fig. 4.10.
4.3 Design of Self Start-UP Oscillator

![Simulation results of the self start up oscillator with $V_{oc} = 10$ mV.](image)

*Fig. 4.9: Simulation results of the self start up oscillator with $V_{oc} = 10$ mV.*

![Negative voltage rectifier using PMOS transistors.](image)

*Fig. 4.10: Negative voltage rectifier using PMOS transistors.*
4.4 Design of Low Power Inductor Based Boost Circuit

The inductor based boost is optimized so that the power consumption of the driving circuits is minimum. This will enable a switched operation mode with minimal input voltage. For the same purpose, the boost circuit is designed to give high voltage conversion ratio. According to Eq. 2.23, \( T_s = (1 - D_1) T_s \) has to be quite narrow. However, such a condition is possible only with low switching frequency. The pulse generating circuit and its following buffer circuits will suffer from undesired high power losses with high \( f_s \) as given in Section. 2.4.3.

For an open circuit voltage of around 30 mV, the boost can be optimized to obtain a high conversion ratio \( V_{out} / V_{in} \approx 100 \Rightarrow D_1 = 0.99 \). The output voltage can reach 2 V taking into account effects of the parasitic components given in Section. 2.4.3. Low switching frequency with low \( I_{L,average} \) lead to bidirectional losses unless high inductance is used as given in Eq. 2.30. The principle of the SMT transformer reuse technique is based on reusing secondary winding in the inductor based boost circuit. The \( L_{sec} \) is 2 mH as given in table. 4.2. Assuming the load resistance, \( R_{load} \), is high in the range of 100 k\( \Omega \), the switching frequency \( f_s \) required to avoid bidirectional losses is

\[
f_s > \frac{D_1 (1 - D_1)^2 R_{load}}{2 L_{sec}} = \frac{0.99 \times 0.01^2 \times 100 \times 10^3}{2 \times 2 \times 10^{-3}} \Rightarrow f_s > 8 \text{ kHz}.
\]

The switching frequency \( f_s \) is chosen to be 10 kHz. The boost driving circuit consists of the secondary inductor of the transformer, the boost switch \( S_{boost} \), oscillator, pulse signal generator and its following driving inverters as shown in Fig. 4.11.

4.4.1 Ring Oscillator Circuit

The driving clock signal can be produced using ring oscillator. The switching frequency has been given (10 KHz). In comparison with the ring oscillator given in Section. 3.5.2, the switching frequency is quite low. More inverter stages with longer CMOS devices is needed to obtain low \( f_s \). Instead of biasing the oscillator using low voltage reference generator, the proposed oscillator for the boost converter is biased using low power current reference circuit shown in Fig. 2.15. This current reference circuit is optimum for the proposed boost because the supply voltage \( V_{out} \) is expected to reach high voltage levels of 3 V. Standard CMOS devices has been optimized to be extremely long \( (L = 25 \text{ um}) \) in order to decrease the oscillation frequency while 17 stages are used for the same reason. The peak-peak voltage of the produced clock signal from the biased oscillator \( V_{clk, low} \) is low in the range of 250 mV. Therefore, another biased inverter \( (Inv._{clk}) \) is used as an amplifier following the oscillator, as shown in Fig. 4.12, in order to give the clock signal \( V_{clk} \) with peak-peak voltage equal to the supply
4.4 Design of Low Power Inductor Based Boost Circuit

Fig. 4.11: Driving circuit of the inductor based boost.

voltage. The NMOS transistor in the inverter $Inv_{clk}$ has been sized equal to the PMOS transistor because of the low voltage of the input signal $V_{clk,low}$. The principle of the biasing circuit is explained including simulation results in Section 2.3.2. It keeps the oscillation frequency constant with supply voltage while the current drawn by the oscillator and $(Inv_{clk,1})$ is kept constantly low as well. Fig. 4.13 and Fig. 4.14 shows the simulation results of the peak-peak voltage of the clock signal and the $f_s$, respectively, with the supply voltage increasing. The clock signal is equal to the supply voltage while the clock frequency start with 9.5 KHz at 0.21 V and reaches 10.2 KHz at 3.3 V.

4.4.2 Pulse Signal Generation

The boost switch $S_{boost}$ is driven by the pulse signal $V_{pulse}$. It has been proposed to generate the pulse signal by passing the clock signal through a passive high pass filter as shown in Fig. 4.15. It is possible to optimize the resistance, $R_{filter}$, and the capacitance, $C_{filter}$, in this simple filter circuit to control the duration of the pulse signal. The resistor is designed to a high value of around 0.5 MΩ (integrated resistor) to reduce the power consumed in the resistor. Thus, the pulse width is determined by the value of $C_{filter}$. For a switching frequency of 10 kHz and a voltage conversion ratio of $(\frac{V_2}{V_1} \geq 100)$, the duration of $D_2 = 0.01T_s \approx 1\text{us}$ is needed. A metal-insulator-metal MIM capacitor has been used with size of $(C_{filter} = 1\text{pF})$. The high pass filter is followed by three inverters so that the given signal by the filter is reproduced giving a pulse signal with the desired
Chapter 4 Low Input Voltage Boost Converter For Thermal Energy Harvesting

Fig. 4.12: Clock signal generator circuit.

Fig. 4.13: Simulation results of the biased oscillator circuit for supply voltage change with time.
4.5 Control Circuit

As has been mentioned in Section 4.2 that a comparator circuit is needed to determine if the converter operates in start up phase or inductor based boost phase. In addition to the comparator circuit, the control circuit includes the interface circuit needed to control the boost switch $S_{boost}$. The designs of theses circuit are explained in details in this section includes the simulation results.

4.5.1 Low Power Comparator Circuit

Low power comparator circuit is needed to measure the output voltage $V_{out}$ giving the control signals $V_{comp,1}$ and $V_{comp,2}$ accordingly. When the voltage $V_{out}$ is less than a reference level referred as $V_{boost}$, the signals $V_{comp,1}$ and $V_{comp,2}$ states are low and high, respectively. When the output voltage becomes higher than the defined reference level, the signals $V_{comp,1}$ and $V_{comp,2}$ change to high and low respectively. The voltage $V_{boost}$ is determined so that the inductor is able to increase concurrent output voltage. It has been found by simulation that minimum supply voltage required for such condition is around 0.7 V.

Fig. 4.14: Simulation results of the $f_s$ for supply voltage change with time.

duty cycle. Fig. 4.16 and Fig. 4.17 shows the simulation results of the produced signal by the filter $V_{filter}$ and the pulse signal $V_{pulse}$ for supply voltage of 2 V.
Differential Amplifier Circuit

The output voltage of the converter, \( V_{out} \), is compared with a reference voltage \( V_{boost} = 0.7 \) V using a differential amplifier. The main obstacle to the design of differential amplifier in this application is that the supply voltage is one of the differential input signals to the differential PMOS transistors. Consequently, the connected PMOS transistor to the supply voltage (\( V_{out} \)) is switched off. There are some solutions have been presented for such problems like the differential amplifier circuit given in [27] and shown in Fig. 4.18. In this circuit, the differential input signals are fed to the bulk terminals of the PMOS transistors pair. When the supply voltage exceeds the defined reference voltage, the output signal switches from low to high. However, this circuit is not suitable for high supply voltages and relatively low reference voltage levels. This is because the bulk biasing of the PMOS transistor will decrease the threshold voltage as given in Eq. 3.7 and increase the drain current and power consumption dominantly.

Instead of measuring the output voltage directly, it is proposed to scale it down by a certain factor to be compared with a reference voltage. In comparison to the reference voltage \( V_{boost} = 0.7 \) V, low reference voltage, \( V_{ref,\text{low}} \), for the proposed amplifier is used. Therefore, it will be possible to use typical differential amplifier using differential PMOS transistors, \( M_{p.in1} \), and, \( M_{p.in2} \), as shown in Fig. 4.19(b). The amplifier circuit is biased using the biasing circuit given in Fig. 2.15 to ensure stable performance with supply voltage. The biasing PMOS transistor is biased in subthreshold region and its drain-source voltage is high so that the source voltages of the input transistors pair is low. Thus, the input
4.5 Control Circuit

Fig. 4.16: The output signal of the high pass filter for an input clock signal of 10 kHz.

Fig. 4.17: The pulse signal generated for input clock signal of 10 kHz.

differential signals should be low in order to avoid switching PMOS transistors, \( M_{p.in1} \), and, \( M_{p.in2} \), off.

**Generation of Differential Signals**

A division of the output voltage referred as, \( V_{out.div.} \), is extracted using ultra low power voltage divider circuit. This circuit is built by a series of diode connected standard PMOS transistors. The \( V_{out.div.} \) is measured across the the last diode giving quite low voltage. This reduces the sensitivity to the process variations as the voltage will be affected by a single diode rather than multiple diodes. For the same reason, the \( V_{out.div.} \), is less affected by the current-voltage nonlinear behavior of the CMOS devices.

Low reference voltage, \( V_{ref.low} \), is given in contrast to \( V_{out.div.} \). The principles of low power reference circuits have been given in Section. 2.3.3. The circuit given in Fig. 2.19 can be used to generate \( V_{ref.low} \) because it is sufficient to produce low reference voltage.
The scale factor in the voltage divider circuit and the reference voltage are defined so that the output signal of the amplifier referred as $V_{amp.}$ gets down at supply voltage of 0.7 V. The voltage divider circuit has been built by 12 diodes $M_{p,d1}...M_{p,d10}$ optimized so that $(V_{out.div} \approx (V_{out}/10))$. On the other hand, the NMOS transistors $M_{n1}$ and $M_{n2}$ has been optimized to produce a reference voltage of 25 mV.

For $V_{out.div} > V_{ref.low}$, the converter switches to the inductor based boost phase. The boost takes a while to work properly while the output voltage decreases slightly to be less than the defined, $V_{boost}$, during this time duration. Consequently, the output signal from the comparator oscillates as well as the operation phase of the converter and the output voltage stopped at $V_{out} = V_{boost} \approx 0.7$ V. In order to avoid this oscillation, an adaptive reference circuit is suggested so that the reference voltage, $V_{ref.low}$, becomes lower after switching while the control signals, $V_{comp,1}$, and, $V_{comp,2}$, are kept unchanged. Fig. 4.19(c) shows the suggested reference voltage circuit. When the control signal, $V_{comp,1}$, changes to high state, the transistor $M_{n,adaptive}$ is switched off and the drawn current into the transistor $M_{n2}$ and the reference voltage are both decreased (see Fig. 4.19(c)).

**Output Stage Circuit**

When the supply voltage exceeds the $V_{boost}$ level, the output signal of the differential amplifier $V_{amp.}$ changes from low state to high state but, it is still less than $V_{DD}$ and not sharply skewed as desired. The output stage is needed in order to generate a nearly digital control signals. The output stage consists of biased inverter amplifier followed by two inverters $Inv.1_{comp}$ and $Inv.2_{comp}$ as shown in Fig. 4.20. The biased inverter circuit will amplify its input signal $V_{amp.}$ while the control signals $V_{comp,1}$ and $V_{comp,2}$ are given by the inverters $Inv.1_{comp}$
and \( I_{\text{inv},2_{\text{comp}}} \) respectively. Additional \( RC \) circuit is placed between theses two mentioned inverters in order to absorb any undesired signals generated from the supply voltage when the inductor based boost starts working. This will eliminate the influence of such undesired signals on the control signal \( V_{\text{comp},2} \).

### 4.5.2 Driving Multiplexer Circuit

As has been explained in Section 4.3.4, in order to minimize the leakage current drawn into the boost switch, \( S_{\text{boost}} \), during start up phase, the gate terminal of this NMOS switch is biased by the negative voltage, \( V_{\text{neg}} \), generated from the negative voltage rectifier. During the inductor based boost, the \( S_{\text{boost}} \) is driven by the pulse signal generated from the pulse signal generator. This requires a driving multiplexer circuit to interchange the gate connection according to the operation phase. Fig. 4.21 shows the proposed \((2 \times 1)\) multiplexer circuit controlled by the the signal, \( V_{\text{comp},2} \), generated from the comparator.

The negative voltage is given through the NMOS switch \( S_{\text{neg}} \) controlled by the signal \( V_{\text{comp},2} \). The pulse signal, on the other hand, is given through the PMOS switch \( S_{\text{p,pulse}} \) controlled by the control signal \( V_{\text{comp},2} \) and the NMOS switch \( S_{\text{n,pulse}} \) controlled by the signal \( V_{\text{inv,cont}} \) which is given by the inverter \( I_{\text{inv,cont}} \). When the signal \( V_{\text{comp},2} \) is high, the switch \( S_{\text{neg}} \) is turned on and the negative
Chapter 4 Low Input Voltage Boost Converter For Thermal Energy Harvesting

![Fig. 4.20: Output stage of the comparator.](image)

... voltage is applied to the $S_{boost}$. The PMOS switch $S_{p,pulse}$ is turned off with the $V_{comp,2}$ is high. The source terminal of the NMOS device in the inverter $Inv_{cont}$ is connected to the source terminals of the switch, $S_{neg}$, so that the output signal ($V_{inv,cont} = V_{neg}$) and the switch $S_{n,pulse}$ is turned off. Thus, the converter is operated in the start up phase. When the signal $V_{comp,2}$ is low, the switch $S_{neg}$ is turned off while the PMOS switch $S_{p,pulse}$ is turned on. The signal $V_{inv,cont}$ goes high so that the NMOS switch $S_{n,pulse}$ is turned on. Consequently, the driving pulse signal $V_{pulse}$ is applied to the boost and the converter is operated in the inductor based boost. The block diagram of the whole boost converter circuit including the control circuit is shown is in Fig. 4.22.

4.5.3 Simulation Results of The Control Circuit

The DC-DC up converter circuit has been simulated with open circuit voltage ($V_{oc} = 30$ mV and source resistance of ($R_s = 2.5 \Omega$)) in order to evaluate the circuit behavior and control signals during the start up and the inductor based boost phases. The Figures:(Fig. 4.24, Fig. 4.25 and Fig. 4.26) show the simulation results of the signals given by the comparator circuit: $V_{out.div}$, $V_{ref.low}$, $V_{amp.}$, $V_{comp,1}$ and $V_{comp,2}$. These signals are generated in response to the output voltage (Fig. 4.23) as has been explained in Section. 4.5.1. It can be seen that the control signals $V_{comp,1}$ and $V_{comp,2}$ are reversed at ($V_{out} = 0.72$ V) and the converter switches to the inductor based boost. The output voltage is slightly decreased until the boost works properly. Once the signal $V_{comp,1}$ goes high, the reference voltage $V_{ref.low}$ decrease from 25 mV to 15 mV so that the output signals of the comparator are kept unchanged. Simulation results of the output signal of the driving multiplexer circuit $V_{mux}$ is
4.6 System Implementation

The proposed boost converter circuit has been taped out using CMOS UMC 0.13um technology. Various CMOS devices types have been used in the converter circuits like the standard transistors, high threshold transistors, low threshold transistors and triple well NMOS transistors. The low threshold PMOS transistor $S_{osc}$ has been sized to be quite wide (3 mm) in order to guarantee the oscillation start up with low input voltage. However, increasing the size of this switch is limited by the available chip area. On the other hand, increasing the width of the transistor $S_{osc}$ will increase the drawn current into the converter $I_{in,\text{rms}}$ and decreases the input impedance $R_{in,\text{boost}}$. As explained in Section 4.2, the input impedance is proposed to be higher than the source impedance in order to keep the input voltage within an accepted range. On the other hand, the size of the NMOS switch $S_{boost}$ is also limited with the available chip area. The size of the MIM capacitor used in the negative voltage rectifier have been

shown in Fig. 4.28. The driving pulse signal is applied to the switch $S_{boost}$ when the control signal $V_{comp,2}$ changes from high state to low state. The negative DC voltage produced from the negative voltage rectifier is shown in Fig. 4.27. It can be seen that the rectified negative DC voltage contains large ripple voltage. This is because the output capacitor of the negative voltage rectifier is quite small.

![Diagram of multiplexer circuit](image)

Fig. 4.21: The suggested multiplexer circuit to drive the switch $S_{boost}$.
Chapter 4 Low Input Voltage Boost Converter For Thermal Energy Harvesting

![Block diagram of the proposed boost converter circuit.](image)

**Fig. 4.22**: Block diagram of the proposed boost converter circuit.

![Output voltage for an open circuit voltage of 30 mV.](image)

**Fig. 4.23**: The output voltage for an open circuit voltage of 30 mV.
4.6 System Implementation

Fig. 4.24: The differential input signals to the amplifier circuit.

Fig. 4.25: The output signal of the differential amplifier circuit.

Fig. 4.26: The output signals of the comparator circuit.
Fig. 4.27: The negative DC voltage generated from the negative voltage rectifier.

Fig. 4.28: The output signal of the driving multiplexer circuit.
Fig. 4.29: Micro-graph of multiple block chip with a total area of $1.6 \times 1.6 \text{mm}^2$ containing the boost converter system.

minimized to 0.5 pF. Despite of the large ripple voltage in the rectified negative DC voltage, $V_{\text{neg}}$, it is sufficient to eliminate the leakage current of the boost switch $S_{\text{boost}}$ during the start up phase. The sizes of the capacitor used in the high pass filter in signals generation circuit and and low pass filter in the comparator circuit have been optimized according to the desired signals characteristics like low power consumption and the duty cycle of the pulse signal $D_1$. On the other hand, the capacitor $C_{\text{LPF}}$ in the low pass filter inside the comparator circuit have been optimized to 1 pF to absorb the noise signals coming from the supply voltage. The layout area of the proposed converter is shown in Fig. 4.30, the occupied area is $(270 \times 270) \text{mm}^2$ within total area of $(1.6 \times 1.6) \text{mm}^2$ multiple blocks including the RF energy harvesting system given the third chapter. As mentioned in Section. 3.6, the chip chip is packaged in a 48-pin QFN package with 0.5 mm pin pitch.

4.7 Experimental Results

The PCB boards Board1 and Board2 mentioned in Section. 3.7 and Section. 3.9, respectively, has been used to test the low input voltage boost converter. The input power is supplied to the chip from DC power supply connected in series to a resistor of 2.5 Ω in order to model the thermoelectric generator TEG (See Section. 4.3). Large capacitor of 100 uF is placed in parallel to the input pin
of the on chip converter in order to construct in combination with the source resistance $R_s$ a low pass filter. This filter absorbs the undesirable ripple in the input voltage $V_{in}$. On the output side, the SMD capacitor $C_{out}$ (100 nF) is connected to the output pin of the converter. Fig. 4.31 shows the test board containing the fabricated chip, SMT transformer and other SMD mentioned components.

### 4.7.1 Test Procedure

The chip verification is composed of two parts: start up phase and inductor based boost phase. The open circuit voltage $V_{oc}$ is increased from 0 V in order to reach minimum $V_{oc}$ required to start up the converter. As the DC source voltage supplied by the DC power supply is further increased, the output voltage increases as well until reaching the switching point $V_{out} = V_{boost} \approx 0.7$ V. At this point, the converter is operated in inductor based boost phase. The output capacitor is connected to a variable load resistance $R_{load}$ in order to measure the output power, efficiency and the output voltage according to the given source voltage.

The board has been connected to a small TEG module from CUI INC with size of $(15 \times 15 \text{ mm}^2)$ in order to proof the ability of the presented converter to work properly in a practical application. The test bench used to measure the
4.7 Experimental Results

The test board of the CMOS boost converter is shown in Fig. 4.31.

### 4.7.2 Measurements of Minimum Start-Up Input Voltage

The hot side of the thermoelectric generator module has been attached to a heating plate which is used as heat source. The residual heat is radiated via a heat sink with low thermal resistance. As the temperature of the heating plate is increased, the open circuit voltage is increased as well until reaching the minimum source voltage required to start up the converter. The measurements show that the minimum open circuit voltage given by the TEG module to start up the converter is less than 10 mV. Fig. 4.33 show the measurements of open circuit voltage before connecting the TEG to the chip and the rectified output DC voltage from the boost converter. The chip has been measured with DC power supply and an equivalent source resistance of 2.5 Ω in order to proof the system ability to work with a wide range of the TEG modules which are commercially available.

The measurements show that the converter can start up with minimum source voltage of 12 mV giving an output DC voltage of 0.48 V (see Fig. 4.34). The measured drawn current $I_{in,rms}$ at the start up voltage is less than 0.5 mA while
the input voltage $V_{in}$ is 11 mV. The input impedance is quite higher than the equivalent $R_s$.

### 4.7.3 Measurements of The Converter In The Inductor-Based Boost phase

As the source voltage is increased, the output voltage $V_{out}$ increases until reaching the switching point. The measurements results show that the converter switches from the start up phase to the inductor based boost phase at $V_{out} = 0.75 \text{ V}$ with source voltage $V_{oc} = 30 \text{ mV}$. The measurement shows that the oscillation frequency during the start up phase is 440 kHz close to that found by simulation with 434 kHz. Both simulation and measurement results are given while the input impedance of oscilloscope (15 pF $\parallel$ 1 MΩ) is connected to the secondary inductor (see Fig. 4.32).

Once the switching occurs, the output voltage becomes 2.7 V for the same source voltage of 30 mV. Maximum output power can be obtained by varying the load resistor $R_{load}$. Fig. 4.35 shows the maximum power conversion efficiency achieved and the associated output DC voltage with the source voltage ranging from 30 mV to 100 mV. The maximum achieved efficiency is 35% at source voltage of 35 mV while the associated output voltage is 1.9 V. This matches with the scope of this project to achieve best characteristics with low input power.
Fig. 4.33: Measurement of start-up voltage of the converter connected to the TEG.

Fig. 4.34: Measurements of output voltage of the converter.
Fig. 4.35: Measurements results of output power and efficiency.
Chapter 5
Conclusions and Outlook

5.1 Conclusions

The aim of the achieved research in this thesis is to present CMOS circuit designs that enable energy harvesting in challenging conditions like low power available from the harvester as well as low input voltage. In this work, a highly sensitive RF energy harvesting system and low input voltage DC-DC boost converter for thermal energy harvesting have been presented.

The RF energy harvesting system consists of differential input cross coupled rectifier and low power charge pump. The rectifier has been designed with high input reactance in order to maximize the RF input voltage by resonance. Moreover, the rectifier has been optimized to be able to drive the charge pump. The suggested circuits of the low-voltage oscillator and the low-voltage reference generator contributed effectively to minimize the power consumption and the start-up voltage of the charge pump. Consequently, the rectifier is able to drive the charge pump even when the RF input power is low.

The measurement results show that the calibrated system sensitivity to produce more than 1 V for a capacitive load is $-25\,\text{dBm}$ within a frequency range of 800 MHz to 870 MHz. Furthermore, a dipole antenna using an economical FR4 substrate has been fabricated in order to prove the design concept with a real antenna rather than using an RF power source. The best sensitivity of the RF energy harvesting system is $-25\,\text{dBm}$ at 820 MHz using the dipole antenna. It can be concluded by the measurement results that using the charge pump is helpful to maximize the DC output voltage for low RF input power with wide bandwidth.

The performance of the presented RF energy harvesting system in this thesis is sufficiently acceptable in comparison with literature as shown in Table. 5.1. The sensitivity measurement is slightly less than that given in [41] and [35]. In opposite, the presented design is able to work with wider frequency bandwidth. Furthermore, the harvesting systems in [35] and [41] require off chip control loop (to control the input impedance) and off chip capacitors (for low frequency charge pump). In contrast, the power conversion system presented here is fully integrated.

Low input voltage CMOS boost converter consists of self start-up oscillator,
Table 5.1: Performance comparison to the state-of-the-art of RF energy harvesting systems.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>UMC 130 nm</td>
<td>TSMC 90 nm</td>
<td>IBM 130 nm</td>
<td>IBM 130 nm</td>
</tr>
<tr>
<td>Die area</td>
<td>0.25 mm$^2$</td>
<td>0.029 mm$^2$</td>
<td>0.25 mm$^2$</td>
<td>Na</td>
</tr>
<tr>
<td>Frequency</td>
<td>(800 to 870) MHz</td>
<td>-</td>
<td>(902 to 928) MHz</td>
<td>2.2 GHz</td>
</tr>
<tr>
<td>Frequency using antenna</td>
<td>810 to 830) MHz</td>
<td>868 MHz</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Requirement</td>
<td>Deep n-well</td>
<td>Off chip control loop</td>
<td>-</td>
<td>Off chip capacitor</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>$-25$ dBm, $R_{load} \approx \infty$</td>
<td>$-27$ dBm, $R_{load} \approx \infty$</td>
<td>$-20.5$ dBm, $R_{load} = 1, \text{M}\Omega$</td>
<td>$-25.5$ dBm, $R_{load} \approx \infty$</td>
</tr>
<tr>
<td>max. $V_{out}$</td>
<td>5 V at $P_{in} = -9$ dBm</td>
<td>3 V at $P_{in} = -15$ dBm</td>
<td>5 V at $P_{in} = -5.8$ dBm</td>
<td>1.5 V at $P_{in} = -23.5$ dBm</td>
</tr>
<tr>
<td>Efficiency</td>
<td>-</td>
<td>40% at $P_{in} = -17$ dBm</td>
<td>32% at $P_{in} = -15$ dBm</td>
<td>-</td>
</tr>
</tbody>
</table>
inductor-based boost and control circuit. The self start-up oscillator has been designed to be able to start up with minimum possible voltage and maximum possible input impedance. The measurements show that the boost can start up with an open circuit voltage of less than 10 mV using typical TEG module giving a DC output voltage of 0.48 V. The inductor based boost has been optimized to give high voltage conversion ratio while its driving circuits are driven by low supply voltage. The suggested pulse signal generation circuit minimized the required supply voltage and the power consumption. For control circuit, low power circuits like low current biasing, the adaptive reference generator, the low power comparator and the driving multiplexer circuit have been presented. These circuits contributed successfully to control the converter operation with minimum power consumption.

It has been found by measurements that the converter can start up for an open circuit voltage of 12 mV with source resistance of 2.5 Ω as an average for the source resistances of the commercially available TEG modules. Besides, when the inductor based boost circuit is activated, the output voltage is raised from 2 V to 2.9 V for open circuit voltage range of 30 mV to 100 mV with an average efficiency of 31 %. It can be seen from the measurements that the proposed converter design is optimum for thermal energy harvesting applications of low input voltage.

Table 5.2 shows a comparison with the state-of-the-art regarding the low input voltage boost converter. The minimum input voltage of the achieved design in this work is less than those reported in literature. The produced output voltage is higher than those given in the mentioned designs. Furthermore, the measured efficiency with an input voltage range of 30 mV to 100 mV is acceptable in comparison to the previously published converters.

The power management circuits which have been designed in this thesis match with aim of work to provide successful energy conditioning with minimum possible power losses. The presented designs gave solutions to overcome the challenging conditions of low power available from the harvester as well as low input voltage. Consequently, the electrical power produced from the harvester can be usable even when the distance between the RF transmitter antenna and the harvesting system is long (in RF energy harvesting), or when the temperature difference across the TEG module is quite low (in thermal energy harvesting).

5.2 Outlook

The measurement results of the presented designs match the targets of the thesis, yet, it is still possible to make these designs more efficient for wide range of input power. Mainly, the given solutions concentrates on working with low power while it was found that performance is not increasing with high input power.
Table 5.2: Performance comparison to the state-of-the-art of low input voltage boost circuits.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>This work</th>
<th>LTC3108 - 2010 [19], Industrial application</th>
<th>Jong-Pil Im - 2012 [17]</th>
<th>Teh - 2014 [45]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>UMC 130 nm</td>
<td>na</td>
<td>130 nm</td>
<td>130 nm</td>
</tr>
<tr>
<td>Minimum $V_{oc}$</td>
<td>10 mV</td>
<td>20 mV</td>
<td>40 mV</td>
<td>21 mV</td>
</tr>
<tr>
<td>Max. $V_{out}$</td>
<td>2.9 V</td>
<td>2.35 V, 5 V</td>
<td>2 V</td>
<td>1 V</td>
</tr>
<tr>
<td>Peak efficiency</td>
<td>31% at $V_{oc} = 30$ mV to $100$ mV</td>
<td>40% at $V_{oc} = 55$ mV</td>
<td>61% at $V_{oc} = 300$ mV</td>
<td>74% for $P_{in} = 2$ mW</td>
</tr>
<tr>
<td>Max. $P_{out}$</td>
<td>130 uW at $V_{oc} = 100$ mV</td>
<td>600 uW at $V_{oc} = 500$ mV</td>
<td>2.7 mW at $V_{oc} = 300$ mV</td>
<td>1.5 mW at $V_{oc} = 1$ V</td>
</tr>
<tr>
<td>MPPT</td>
<td>no</td>
<td>no</td>
<td>yes</td>
<td>yes</td>
</tr>
</tbody>
</table>

For the RF energy harvesting system, the parasitic capacitance of the pads decreases the input reactance massively and decreases the RF voltage gain by resonance. The sensitivity can be improved by using smaller pads. When the RF input power increases, the rectified voltage from the rectifier can be higher than 1 V. Consequently, the rectifier output terminal can be connected directly to the output capacitor instead of the charge pump based boost converter. This gives the possibility to obtain high efficiency with high input power. This can be managed using low power comparator with two switches as shown in Fig. 5.1. The comparator is optimized so that its output signal is switched from high to low at certain input power level when the rectified voltage $V_{rec,DC}$ is higher than 1 V. Furthermore, since the the input impedance is varying with input power, an adaptive matching network will be helpful to guarantee maximum power matching for wide range of RF input power. The adaptive matching network can be realized using variable capacitor or switched capacitors that are connected in parallel to the input terminals.

For the boost converter design, it is possible to increase the output voltage during the start-up phase using multistage rectifier instead of single diode. The rectifier can be switched off when the converter changes to inductor based boost. Off chip capacitors might be needed for this suggestion because the oscillation frequency is low so that large capacitors will be required.
Furthermore, additional maximum power point tracking (MPPT) circuit will be
helpful to increase the efficiency and guarantees maximum power transfer from the source to the converter. The duty cycle of the driving pulse signal can be changed by changing the capacitance of the high pass filter. Switched capacitors are suggested to be controlled by the MPPT circuit according to the input voltage. It is possible to increase the output power during the inductor-based boost phase by increasing the width of the boost switch. A rectifying diode with wider width is preferable to decrease the conduction losses.

Fig. 5.1: Suggested RF energy harvesting system for future works.
References


5.2 Outlook


Chapter 5 Conclusions and Outlook


5.2 Outlook


Curriculum Vitae

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