Ultra Thin Silicon Nitride Interface Engineering

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Chapter 1

Introduction

The on-going scaling of the metal-oxide-semiconductor-field-effect transistor (MOSFET) based on silicon is now coming to an era of a new semiconductor material. The 10nm node is going to be the final application of silicon as a channel material starting with the 7nm SiGe node next year by Intel and AMD [1, 2]. Nevertheless, the market for application-specific integrated circuits (ASIC, custom chips) grows owing to arising fields for instance the internet of things, which is one crucial key element of the fourth industrial revolution 4.0 [3–8]. The internet of things is composed of sensors, micro- and nano-electromechanical systems, discrete power devices and integrated circuits, which do not need a state-of-the-art machine processor unit (MPU). For instance, the costs of ultra modern MPUs is in the range of almost all automotive semiconductor components in one vehicle combined [9]. Hence, in principal the mainstream fabrication is several technology nodes behind [10] so that the end of silicon as a semiconductor material is not expected to come in the next three decades.

A cost reduction of the fabrication procedure is a promising impulse to postpone the transition to a new semiconductor material processes. One cost-intensive process is the doping of silicon. If metal is in contact with silicon, a Schottky-barrier is formed, which increases the contact resistance. Here, ohmic contacts are commonly realized by highly doped source-drain regions. If local doping profiles are intended, an incorporation by ion implantation is the commonly used approach nowadays. However, this technique has several drawbacks: It does not provide a simultaneous batch processing. A subsequent annealing is indispensable to electrically activate and recrystallize the doped area and the elevated acquisition and maintenance costs [11]. Furthermore, the annealing results in a diffusion of dopants, which deteriorates the control of the geometry of ultimately scaled FETs. In addition, the random distribution and discreteness of dopants leads to a variation of the device performance. Several approaches have been introduced to master the above mentioned issues such as junctionless transistors to avoid P-N junctions as well as Laser or flash lamp activation annealing procedures or ultra-low-energy implantation [12–17]. All these approaches aim to improve the contact of the metal silicon junction. The immense technological expenditure to tackle the Schottky-barrier of metal-silicon interfaces
is one present reason to look for alternative solutions. Hence, a reduction of the Schottky-barrier was one intensive research topic in the last two decades [18–21]. A minimizing of the Schottky-barrier impact was achieved, however, the presence of the Schottky-barrier yields so-called ambipolar transistors that show electron and hole transport depending on the voltage bias. While this might appear as a benefit, ambipolar conduction actually leads to leakage currents in the off-state, particularly in ultimately scaled transistors. Additionally, the Schottky-barrier region exhibits strong carrier recombination owing to the high interface state density [22,23]. Recent work demonstrated that a silicon nitride layer between metal and silicon suppresses the Fermi level pinning and improves the N-type device characteristics [24–27]. Connelly and Ghoneim et al. demonstrated clearly that despite the additional tunneling resistance the contact resistance is reduced. Moreover, the leakage P-type branch of the ambipolar behavior was suppressed by several orders of magnitude owing to the unipolar N-type device behavior. A second and even more relevant aspect of the incorporation of an ultra thin insulator is the formation of a depletion layer at the surface of silicon depending on work function of metal. In spite of the tunneling insulator carriers from metal owing to the huge free carrier concentration in metal are injected into the semiconductor to form an equilibrium state between the two different Fermi-levels. One aim of this thesis is to setup a framework for ultra thin silicon nitride interface engineering including the fabrication, characterization of several silicon nitride based device concepts. The basic fundamentals in chapter 2 start with an introduction of the formation of an ohmic tunneling junction at the metal-silicon nitride-silicon stack. Afterwards, a brief review of p-n-junctions and Schottky diodes is presented to highlight the main differences of silicon nitride based depletion junctions. A second application is the Metal-Insulator-Silicon (MIS) solar cell because the built-in potential of the junction inside the solar cell is the essential component. This section deals with main differences and benefits of silicon nitride in contrast to silicon oxide concepts for passivated contacts. Next, the basics of resonant tunneling diodes fabricated out of a silicon nitride-amorphous silicon-silicon nitride-stack are introduced. Chapter 2 ends with the impact of an incorporated silicon nitride layer providing an improved energy selective contact concept and a brief introduction of MOSFETs and. Three optical analysis techniques are described in chapter 3 consisting of ellipsometry, Fourier transform infrared spectroscopy (FTIR) and Terahertz-Time-Resolved-Spectroscopy. Chapter 4 silicon nitride layers regarding their growth, element composition, temperature effects, insulating property and density are discussed. Subsequently, chapter 5 gives a broad overview of the fabrication of the earlier stated devices. Moreover, one key element of this chapter deals with the development and manufacturing of micro-and nanostencil masks, which are of great importance to exclude any possible contamination on top of the silicon nitride layers. Chapter 6 is the final part of this thesis presenting and characterizing MOSFETs, diodes, solar cells and resonant tunneling diodes. A summary and an outlook finalize this work.
Chapter 2

Fundamentals

Taking into account all successful applications of silicon as Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET), bipolar junction transistor, solar cell it turns out that in principle silicon’s economical success is based on the rectifying nature of P-N junctions. Since all these devices are in focus of the presented work, the basics start with the P-N junction, from which the connection to each device type are presented to broaden the perspective of the impact of the studied dopant-free-approach. One part of the present chapter deals with fundamentals is a comparison between conventional P-N junctions, Schottky diodes and the new silicon nitride-based diodes. The latter ones are incorporated into a new metal insulator semiconductor solar cell concept. Afterwards, resonant tunneling diodes are presented owing to the importance of the resonant states to increase further the performance of solar cells by energy selective contacts. Finally, this chapter is closed by silicon on insulator (SOI) MOSFETs, where the ohmic tunneling insulator nature is a prerequisite to establish normally-off unipolar P-type or N-type devices.

2.1 Ohmic Tunneling Junction

A considerable amount of process engineering is needed to reduce the parasitic resistance of silicon metal contacts, which is caused by a Schottky Barrier at the interface of the junction. All known silicon metal junctions do not naturally exhibit ohmic contacts. A Schottky Barrier (SB) originates from a high interface density, which consists of two main parts [28, 29]:

- Dangling Bonds and
- Metal Induced Gap States (MIGS).

The first component consists of unpaired states at the silicon surface. If a metal comes in contact with silicon, electrons are injected into the band gap of silicon, which decay in an evanescent manner once entering the energy gap of silicon (see Fig. 2.1a). Electrons (holes) with energies close to the conduction band (valence band)
propagate further into the band gap. These states are separated into conduction-like and valence-like states (see Fig. 2.1 b). These MIGS reflect the wave nature of electrons.

Considering the dangling bonds, these lead to a significant interface state density. As a result, the Fermi level is pinned and less sensitive to the work function of the corresponding metal causing a Schottky barrier $\phi_b$ (see Fig. 2.1 c).

In this context, silicon nitride is a promising interface engineering approach because it directly aims at removing the associated Fermi level pinning (FLP). On the one hand the incorporation of an ultra-thin insulator has to saturate dangling bonds and on the other hand the MIGS should be blocked by this tunneling barrier to ensure a depinning of the Fermi level (see Fig. 2.1 d).

However, a trade-off situation between blocking the current and reducing the MIGS occurs. Keep in mind, that energetically lower lying electrons are stronger suppressed in comparison to electrons which are injected into the conduction band. The transmission of carriers through the silicon nitride layer should be as high as possible but the injection of metal gap states as low as possible. Fig. 2.1 e shows the transmission coefficients on a semi-logarithmic scale for SiN layers with different thicknesses (0.8 nm, 1 nm and 3 nm) to emphasize the impact on the transmission of carriers. The trans-
mission coefficient is calculated by a spectral function based approach [30]. The spectral function is determined by the solutions of the Schrödinger equation so-called wave functions which contain the quantum mechanical nature of the carriers. A thicker (e.g. 3 nm) silicon nitride layer reduces the transmission of carriers and causes a Metal Oxide Semiconductor (MOS) capacitor situation whereas thinner silicon nitride layers exhibit much higher transmissions. It is evident that for MIGS the transmission into the band gap is much smaller due to a higher effective energy barrier ($\phi_e < \phi_{MIGS}$) leading to an increased reduction of MIGS (see Fig. 2.1 d and e).

Connelly and Ghoneim et al. demonstrated clearly that in spite of a tunneling barrier the overall injection of carriers into the conduction band is enhanced so that the parasitic contact resistance for electrons is diminished [24–27]. It is worth mentioning that a tunneling barrier is essential to remove the FLP. Even if it was possible to achieve a depinned interface without any nitride (or doping), ambipolar behavior would appear due to the fact that the metal causes a metal-like density of states in the band gap at the silicon interface. This aspect is presented in detail in section 2.6.

The optimum between blocking MIGS and suppressing carrier transport is the ideal solution to handle this trade-off. However, an appropriate ultra-thin silicon nitride layer depins the silicon-metal interface of the FLP, which has a severe consequence and is explained in detail in the upcoming sections.

2.2 P-N Junctions, Schottky and Schottky-Mott Diodes

Diodes were one of the first successful semiconductor devices due to their rectifying nature. Therefore, the basics of the P-N-junction and Schottky diodes are introduced to give a better understanding of similarities and differences to the silicon nitride based diodes in the last subsection.

2.2.1 P-N Junction

In principle, P-N junctions are made of two P-type and N-type doping regions. Choosing silicon as an elemental semiconductor from group IV, P-type dopants are located in the group III (for instance boron) while N-type dopants are part of group V (e.g. phosphorus). A dopant contributes either a free electron (donator) or collects an electron (acceptor) and leaves behind a localized charged ion compensating the free charge. If a P- and N-type region are in contact free electrons (holes) diffuse into the P-type (or N-type) region and recombine leaving behind a localized space charge (see Fig. 2.2 a and b). However, the recombination leads to a depletion of carriers which yields to an electrical field between acceptor and donator regions. The electrical field $\xi$ inside the P-N junction depends on the concentration of dopants
Figure 2.2: a) Conduction, valence band and a sketch of a P-N junction is illustrated, squared and circle symbols correspond to localized space charge and free carriers, b) local carrier density of the depletion region, c) local electrical field inside the depletion region, d) local electrical potential showing the built-in voltage $V_{bi}$.

as (see Fig. 2.2 c):

$$\frac{d \xi}{dx} = -\frac{\rho(x)}{\varepsilon_{Si}} = -\frac{qN_i}{\varepsilon_{Si}} \begin{cases} N_i = N_a & \text{if } -w_a < x < 0 \\ N_i = N_d & \text{if } 0 < x < w_d. \end{cases} \quad (2.1)$$

where $\rho$, $q$, $N_a$, $N_d$, $w_a$, $w_d$ and $\varepsilon_{Si}$ are charge density, elementary charge, the acceptor- and donator concentrations, the P-type and N-type boundary widths and the dielectric constant of silicon. Relying on the relation between the electrical potential and the electrical field

$$\frac{d\phi(x)}{dx} = -\xi(x), \quad (2.2)$$

the electric field is replaced, which yields to the Poisson equation

$$\frac{d^2\phi(x)}{dx^2} = \frac{\rho(x)}{\varepsilon_{Si}} = \frac{qN_i}{\varepsilon_{Si}} \begin{cases} N_i = N_a & \text{if } -w_a < x < 0 \\ N_i = N_d & \text{if } 0 < x < w_d. \end{cases} \quad (2.3)$$

Fig. 2.2 d shows the solution of the Poisson equation including the built-in voltage, which is closely related to the forward voltage $V_f$ of a diode and characteristic values are between 0.7-0.9 V. The built-in voltage depends on the intrinsic carrier

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2.2. P-N Junctions, Schottky and Schottky-Mott Diodes

The forward voltage is one figure of merit of diodes and states the voltage up to which the transport of carriers through the P-N junction is blocked. The forward voltage is the voltage drop across the diode at a certain current density. The diffusion current still rises, which consists of electrons from the N-type reservoir injected into the P-type region. The same holds true for holes from the P-type reservoir, but these propagate into the N-type region until they recombine with majorities. So, injected majority carriers are now minorities. This minority carrier injection is responsible for the overall current through the P-N junction:

\[ I = I_0 (e^{\frac{qV}{nkT}} - 1), \quad \text{with} \quad I_0 = AqN_i^2 \left( \frac{D_p}{L_p N_d} + \frac{D_n}{L_n N_a} \right), \]  

(2.5)

where \( n, A, D_p, D_n, L_p \) and \( L_n \) are the ideality factor, area, diffusion coefficients and diffusion length for holes and electrons, respectively. If the diode is reverse biased, the external electrical field expands the depletion region so that the reverse current stems from purely generation and recombination process, which saturates for higher voltages. For the sake of completeness, the breakdown voltage \( V_{BR} \) of P-N junctions is based on either avalanche or Zener phenomena [31–34]. Fig. 2.3

**Figure 2.3:** IV characteristic of an ideal diode exhibiting forward, reverse and breakdown regimes is illustrated.
2. Fundamentals

summarizes graphically the three characteristic regimes of a diode: Forward, reverse and the breakdown regimes. Usually, the breakdown voltage is above 100 V for impurity concentrations below $5 \cdot 10^{16} \, \text{cm}^{-3}$ and a drift zone thickness of 5 $\mu\text{m}$ [32,35], making a P-N junction a perfect rectifying device.

2.2.2 Schottky Diodes

In contrast to P-N junctions Schottky-Diodes are majority based diodes. To simplify matters, the majority carriers are considered to be electrons (depicted in Fig. 2.4). At the metal silicon interface electrons have to overcome the Schottky barrier either by thermal emission (TE), thermally assisted field emission (TFE) or field emission (FE) [36]. Recombination and deep level tunneling phenomena are neglected here [37–39], because these two components do not contribute to the understanding of dopant free diodes and Schottky diodes. The Schottky barrier band bending causes a depleting region of majority carriers, similar to a P-N junction. However, the current through this depletion region is a completely majority based flux. Therefore, Schottky diodes are applicable for much higher frequency ranges compared to doped P-N junctions at the cost of much lower forward voltages (typically < 0.4V) [35]. In practice, Schottky diodes beat any other technology in terms of fabrication simplicity and costs apart from point contact diodes [40,41].

![Figure 2.4: Band structure of a metal-silicon interface with FLP is depicted leading to a Schottky-barrier.](image)

2.2.3 Schottky-Mott Diodes

In section 2.1 one missing consequence of silicon nitride was left out. If the FLP is no longer present at the interface, the work function of metal becomes a crucial
2.2. P-N Junctions, Schottky and Schottky-Mott Diodes

part of interface engineering. The metal induces carriers into the silicon surface to equalize the imbalance of the silicon and its own Fermi level (see Fig. 2.5a). Giving an example, aluminum is chosen to be in contact with an ultra silicon nitride layer on top of silicon. Aluminum exhibits approximately a work function of 4.1 eV, which is close to the electron affinity of silicon 4.05 eV [35, 42, 43]. Furthermore, the silicon should be low doped \(10^{15} \text{cm}^{-3}\) or in a best-case scenario undoped. The electrons of aluminum propagate through the highly transparent tunneling barrier into the silicon resulting in a higher electron concentration at the silicon surface, which is depicted by the band bending downwards (see Fig. 2.5b). For the sake of simplicity, a band bending at the metal surface is not shown here on the basis of high carrier concentration and a small screening length. In addition, the shape of the conduction and valence bands at the interface can be assigned to a depletion region similar to the Schottky diodes, but it provides ohmic contacts in place of a real Schottky-barrier.

Schottky and Mott predicted the impact of metals on the silicon surface but the FLP reduces significantly this dependency [28, 29, 44–46]. The work function of metal bends the surface of silicon without any additional impurities due to the suppressed FLP (as illustrated in Fig. 2.5b)

![Figure 2.5: Band structure with silicon nitride layers between metal and silicon prior to contact and in contact are presented: a) silicon with Si\(_3\)N\(_4\) prior to metalization is illustrated. The blue line corresponds to the ultra-thin insulator, the arrows indicate the Fermi energy of the metals. b) Low and high work function metals bend the surface of silicon silicon’s surface, which causes an either convex or concave band bending and leaves behind one junction on each contact.

where a low work function metal bends the silicon surface downwards and a high work function metal upwards. A closer look at the transport reveals a similar carrier behavior as in Schottky diodes.
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Figure 2.6: Band structures of a Schottky-Mott diode in forward-bias and reverse-bias are depicted: a) forward-bias Schottky-Mott diode, the applied forward bias $V_{ds}$ leads to a reduction of both junction widths and built-in voltages at the silicon increasing the electron and hole currents. b) Reverse-bias Schottky-Mott diode, owing to the reverse bias the built-in voltages are increased at both interfaces. However, the unconventionally high built-in voltages ($\phi_{SB}$) reduce the injection of carriers.

Each metal-silicon contact blocks either electrons or holes. The band bending at the interface is increased in contrast to real metal-silicon contacts with their FLP (see Fig. 2.6 a). Hence, these Schottky-Mott diodes (SM) benefit from elevated $\phi_{SB}$, when biased in reverse mode. Despite the fact, that the SB thickness is reduced by the reverse bias, the band bending is sufficiently strong to block carriers from tunneling (see Fig. 2.6 b) leading to a much smaller reverse current. In addition, it has to be taken into account that both contacts are in reverse mode. Summarizing, Schottky-Mott diodes provide several advantages compared to P-N junctions and Schottky diodes

- dopant free approach,
- high built-in voltage,
- smaller reverse current,
- completely majority based current,
- cost-effective fabrication method.

2.3 Metal Insulator Semiconductor Solar Cell

A solar cell can also benefit from a sophisticated interface engineering by optimizing the electrical properties of the surface of silicon. On the one hand, an ohmic
tunneling insulators offers an ohmic contact, on the other hand it can reduce the recombination of excess carriers at the silicon surface. If a solar cell is not illuminated, they exhibit conventional diode characteristics, as already introduced in section 2.2.1, while under illumination excess carriers are generated leading to a short-circuit current. The reader is referred to section 6.3, where a detailed overview of the IV characteristics of solar cell is given.

A standard silicon solar cell architecture is depicted in Fig. 2.7. If light shines on the surface of silicon, excess carriers are generated. However, these excess carriers are not stable due to the non-equilibrium state, which was excited by the absorption of light. The solar cell displayed here consists of a P-type substrate (base) so that holes are majority carriers while electrons are minority ones. Therefore, the existence of these excess carriers is limited by a lifetime due to recombination, which is divided into three basic types [47–50]:

- Radiative recombination (substantial part for direct band gap semiconductors)
- Shockley-Read-Hall recombination (present in materials with defects)
- Auger recombination (relevant in highly doped materials or high level injection).

The question arises what happens with generated excess carriers close to a P-N junction? Following the law of mass action the free electron concentration rises by doping the active silicon surface (emitter) with N-type atoms.

\[ n_0p_0 = n_i^2, \quad (2.6) \]

**Figure 2.7:** Standard solar cell with P-type Si substrate (base), Aluminum metallization, emitter (front surface field), back surface field and ARC is illustrated.

A higher electron concentration reduces the amount of holes in this N-type doped region given by the law of mass action
where \( n_0, p_0 \) and \( n_i \) are electron-, hole and intrinsic carrier concentrations (\( n_i \sim 10^{10} \text{cm}^{-3} \) at room temperature). The generated holes inside the N-type region are ideally extracted into the base by the electrical field of the P-N junction \([51]\). Hence, a depletion region at the backside results into a rise of the lifetime of the majority carriers \([52]\). It is the electrical field of the junction, which pushes the generated holes (electrons) to the P-type (N-type) region. An ideal passivation layer reduces the surface recombination of minority carriers and additionally introduces a surface field (front surface or back surface field). But these surface depletion regions do not provide emitter dopant depths of hundreds of nanometers owing to small screening lengths \([53]\). Furthermore, an antireflecting coating (ARC) or even double layer of ARC are deposited to reduce the reflected light at the silicon surface. This so far is only a small excerpt from the operating and improvement principles of a solar cell, several other optimization concepts and even solar cell architectures coexist to increase the efficiency \([54–57]\). Another passivation measure deals with the surface recombination (e.g. dangling bonds, high interface state density). To lower the surface recombination the surface is oxidized to saturate dangling bonds and to reduce the interface state density \([58]\). However, this oxide in the contact areas needs to be removed or an ultra-thin thickness is essential to obtain a very low contact resistance and to attain low total power losses.

Nevertheless, the first metal insulator semiconductor solar cell design took advantage of an ultra-thin oxide layer on the complete front silicon surface, even between metal and silicon (see Fig. 2.8) \([59–65]\). A Low contact resistance is commonly achieved with thicknesses below 2nm. Notwithstanding, silicon oxide has several disadvantages in contrast to silicon nitride \([66–71]\):

- Higher band gap of approximately 9eV (\( Si_3N_4 \): 5eV)

![Figure 2.8: MIS-Solar cell consisting of a P-type Si substrate (base), ultra-thin silicon nitride layers, an Aluminum front-, a Gold backside-metallization, an anti reflective coating and a front surface field is demonstrated.](image)
2.4 Resonant Tunneling Diode

- Smaller density of silicon oxide layers (SiO$_2$:Si$_3$N$_4$): $2 - 2.65 \frac{g}{cm^3} : 3.0 - 3.4 \frac{g}{cm^3}$
- Degradation of the tunneling oxide by post-processing steps
- Lower dielectric constant, $\epsilon_{SiO_2} \approx 3.9$
- No sophisticated fabrication approach below or even close to 1nm established.

The higher density of silicon nitrides ensures much smaller insulator thicknesses below 1nm offering theoretically lower contact resistances, which is not feasible for silicon oxide interface engineering [72]. Moreover, the smaller band gap allows thicker silicon nitride layers (see section 2.1). In addition, the Schottky-Mott behavior at the interface is extremely attractive because of an extra field-effect passivation leading to less recombination. The electric field of the Schottky-Mott junction supports the separation of generated carriers, which is applied in Schottky-barrier solar cell concepts [73, 74]. However, Schottky-barrier solar cell concepts exhibit small open-circuit voltages associated to the increased recombination at the surface of silicon. The incorporation of silicon nitride layer reduces the interface state density and increases the minority carrier lifetime which both contribute to the open-circuit voltage. Up to now, an ultra-thin silicon oxide technology is the only insulator technology of MIS solar cells.

2.4 Resonant Tunneling Diode

The Esaki tunneling diode in 1957 paved the way for the resonant tunneling diode (RTD) [75]. While the transport in tunneling diodes takes place between two bands (usually conduction and valence band) of a material, the RTD exhibits defined eigenenergies for transport. Both device concepts do have in common a unique negative differential resistance (NDR). In contrast to other diodes, both approaches exhibit quantum mechanical phenomena:

- Tunneling through potential barriers and
- Quantum mechanical confinement of states (bounded states only in RTD present).

Resonant tunneling diodes work as energy filters due to the eigenstates. The confinement inside the semiconductor allows the injection from one contact to the other by well-defined energy channels, which is called resonant tunneling (see Fig. 2.9 I and III, eigenenergy $E_1$). Nevertheless, the transmission of carriers above and beneath an eigenenergy level is reduced but not completely blocked, so that less carriers contribute to the current, which is displayed in Fig. 2.9 II and IV. In the case of energies above an eigenenergy the differential resistance becomes negative and a peak-to-valley ratio appears. The Peak-to-Valley-Current Ratio (PVCR) is a figure of merit of tunneling and resonant tunneling diodes, where a high Q-factor is desired for oscillator applications [76, 77].
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Figure 2.9: Current Voltage characteristic of a RTD is illustrated, exhibiting resonant tunneling transport (I+II) and transport blocking (II+IV) leading to peak-to-valley phenomena.

2.5 Silicon Nitride based-Resonant Tunneling Diodes

Three general concepts of tunneling diodes are well known. A sandwich of alternating highly doped layers separated by an abrupt and thin intrinsic layer forming a PIN structure is the most common one for tunneling diodes. Secondly, resonant interband tunneling diodes are the first devices exhibiting a negative differential resistance at room temperature [78–80]. However, these two ideas are conventionally implemented by molecular beam epitaxy (MBE). The third idea of manufacturing tunneling diodes relies on insulator semiconductor insulator semiconductor sandwiches where the confined semiconductor region is encapsulated by two insulators and not by a high band gap semiconductor [81].

In contrast to MBE-grown devices it is difficult to fabricate tunneling diodes or RTDs by chemical vapor deposition, implantation and annealing techniques. In principle, a tunneling diode realized by externally introduced dopants fails due to several issues namely scattering events (implantation), diffusion process (activation of dopants) and high doping (crystal defects) [82–84].
A more promising concept is depicted in Fig. 2.10. As a starting point the surface of a crystalline substrate is nitrided, subsequently an ultra-thin amorphous silicon (a-Si) layer is deposited and once again nitrided. The growth of the second insulator on the deposited amorphous silicon surface closes the surface and reduces the interface state density. Additionally, prior to the second nitridation step the in-situ crystallization of the amorphous silicon (a-Si - c-Si) layer begins during heating in inert atmosphere. While a deposition of a higher band gap material for the tunneling barriers requires a highly sophisticated process, the growth of potential barriers has several advantages:

- Completely closed and homogenous layer of insulators
- Thermally driven diffusion process
- Lower interface state densities
- In-situ crystallization during heating prior to second nitridation step
- One part of the a-Si thickness is consumed during second nitridation requiring thicker initial a-Si layers
- Scalability of the ultra-thin nitride layer offers a metal tuning\energy selective contacts.

The smaller band gap and higher density of silicon nitride are promising features for RTDs with thin insulators. The crystallization of the amorphous layer is affected
by two interfaces. On the one hand, the nucleation depends on the amorphous-crystalline interface, on the other hand the dielectric-crystalline interface influences the formation of the nanocrystals. Keeping in mind that the amorphous layer is encased on two sides by a silicon nitride layer, the transition temperature of phase change from amorphous to crystalline nature rises owing to the capping in combination with a small silicon thickness [85]. Zacharias and Streitenberger derived a first principle theory of a crystallization model based on an exponential dependency between silicon thickness and crystallization temperature [86]. In their work, an effective crystalline-dielectric interface energy $\gamma_{\text{eff}}$ consists of amorphous-crystalline and crystalline-dielectric interface energies $\gamma_{\text{ac}}$, $\gamma_{\text{cd}}$, which are connected as follows:

$$\gamma_{\text{eff}} = \gamma_{\text{ac}} + (\gamma_{\text{cd}} - \gamma_{\text{ac}}) e^{-\frac{l}{l_0}}.$$  \hspace{1cm} (2.7)

The exponential function takes into account the thickness-dependent phase change temperature, where $l$ reflects the residual distance between crystal nuclei and dielectric and $l_0$ is a characteristic screening length. The latter one is attributed to the interatomic force. However, this approach is based on cylindrically shaped nuclei. Recent work of Chen et al. considers a spherically shaped crystallization [85]. Hence, both approaches assume a symmetrical expansion despite the fact that silicon is not confined in the longitudinal direction. The concept in Fig. 2.10 takes advantage of having only one silicon nitride-amorphous silicon interface, while the nitridation of the top surface of the amorphous layers starts after heating up in inert atmosphere. During this heating period the crystallization of the amorphous layers takes place. Hence, the total interface energy is reduced offering lower crystallization temperature. Moreover, it is worth mentioning that the impact of thickness is more or less independent of the type of deposition procedure [87-92]. A sophisticated amorphous silicon-silicon nitride fabrication procedure for RTD is not established yet and is studied in this thesis.

### 2.6 Metal Oxide Semiconductor Field Effect Transistors

The fabrication of Metal Oxide Semiconductor Field effect transistors (MOSFET) is the heart of the semiconductor industry. While silicon as a channel material will be most likely replaced by germanium and InGaAs starting with the upcoming 10 nm node or at the latest when the 7nm node is introduced [93] (IBM has already successfully demonstrated a 7nm SiGe FinFET chip in 2015 [2]), silicon will keep its relevance the next two decades due to the high risk investments for technology concepts. In the context of cost effectiveness, the operation of MOSFETs is introduced and the impact of the silicon nitride is given for a dopant free approach.

#### 2.6.1 Complementary MOSFETs

Two kinds of transistor concepts for silicon exist: The bipolar junction transistor (BJT) and the MOSFET, which are used in a variety of applications (thyristor,
2.6. Metal Oxide Semiconductor Field Effect Transistors

Figure 2.11: a) Sketch of a N-type MOSFET is depicted; source, drain and gate terminals are at the top of the MOSFET, beneath the metals highly N-type doped regions are illustrated, b) and structure of a MOS capacitor for the flat band case, c) band structure of a MOS capacitor in inversion mode, d) conduction band of an N-type MOSFET for different $V_{gs}$ is displayed, red arrow in a) shows the conduction band along the source drain region.

Insulated-gate bipolar transistor, amplification, Power MOSFET, integrated circuits) [94]. Fig. 2.11a illustrates a N-type MOSFET, which consists of source, drain and a gate terminal. The bulk terminal is not part of the sketch because a silicon-on-insulator (SOI) technology is assumed. The channel region lies directly beneath the oxide. While a BJT is based on an injection of carriers into the base to switch the current between emitter and collector, ideal MOSFETs take advantage of the field-effect to accumulate, deplete or invert the channel region. In Fig. 2.11b a MOS gate capacitor is depicted for the flat band case. Let us assume that a positive charge is at the gate, the induced field attracts electrons to the surface of the semiconductor. Therefore, a band bending occurs at the surface, which is shown in Fig. 2.11c. In principle, the potential barrier, which results from the already introduced built-in voltage (NPN, see Fig. 2.11d), blocks the transport of electrons from the left to the right hand side. Thus, a potential barrier leads to the off-state, while no barrier results in the on-state of the MOSFET. The sketch in Fig. 2.11d illustrates the relation between the drain current of a MOSFET and the potential barrier in
the channel region. Moreover, the transfer characteristic provides several important information about the features of the MOSFET, this includes for instance:

- On-off ratio,
- Inverse subthreshold slope $S$
- Leakage current of unipolar devices
- Leakage current due to ambipolar nature.

The on-off ratio and subthreshold swing are figures of merit. A rule of thumb for the performance of a "good" MOSFET, is an on-off ratio of at least 6 decades and an inverse subthreshold slope close to the limit of thermionic emission $[$95$]$:

$$S \approx \ln(10) \frac{kT}{q} = 60 \frac{mV}{dec} \quad at \quad T = 300 \text{ K}.$$  

(2.8)

Simply speaking, the subthreshold swing states how much voltage is required to switch one decade of current. To switch the claimed 6 decades at least 360 mV are necessary, which is the ideal limit of the operation voltage of conventional MOSFETs concepts. The output characteristic of FETs describes the relation between drain current and the drain-source voltage, which is divided into three regimes:

- Linear / ohmic regime
- Saturation regime
- Punch-through.

Assuming an inversion layer in the channel the drain current linearly rises for small biases ($V_{ds} < V_{gs} - V_{th}$). Once the drain source voltage exceeds $V_{gs} - V_{th}$ the current starts to saturate originated from the depletion region at the channel drain junction $[$96$]$. The drain current of the ohmic and saturation regime is described by the equation:

$$I = \mu_{n,p} C_{ox} \frac{W}{L} \left[ (V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2} \right],$$

(2.9)

where $\mu_{n,p}$, $C_{ox}$, $W$ and $L$ are the carrier mobility for electrons or holes, gate capacitance, width and channel length of the MOSFET. If the voltage is kept increasing the punch-through regime occurs which results from the avalanche breakthrough (see section 2.2.1).

As already mentioned in the introduction, the key component of the success of the semiconductor industry is the complementary technology making it possible to build up logic gates for Boolean functions ("1", "0", "high", "low"). Therefore, MOSFETs are divided into either N-type or P-type devices. However, a transport blocking potential barrier is required for ideal N-type as well as P-type MOSFETs, which exhibit unipolar characteristics (Fig. 2.12 a). The simplest rudimentary logic gate
2.6. Metal Oxide Semiconductor Field Effect Transistors

Figure 2.12: a) Inverter composed of P-type (right) and N-type (left) MOSFETs is depicted, transfer characteristic of each individual MOSFET is illustrated below, dashed and solid lines correspond to off and on state of the respective FET, b) ambipolar transfer characteristic of SB-MOSFET is demonstrated, c) output characteristic of an ohmic (darkblue) and SB (red) MOSFET are sketched.

is the inverter made of P-type and N-type MOSFETs. Considering a “good” inverter static losses are not present, because N-type as well as P-type MOSFETs are in the off-state once they have driven the output to $V_{dd}$ ("High", Pull up) or $V_{ss}$ ("Low", Pull down). Therefore, dynamic losses switching from “High” to “Low” or vice versa account for the biggest part, which in a first approximation depends on:

$$P_{dyn} \propto V_{dd}^2 C f_{clock},$$

(2.10)

where $V_{dd}$, $C$ and $f_{clock}$ are the maximum voltage, load capacitance and clock frequency.

As depicted in Fig. 2.12a the metal silicon contacts have a highly doped region to ensure ohmic contacts. If the Schottky contact is not tackled by an interface engineering approach the Schottky-barrier causes an additional parasitic resistance. However, the present FLP at the interface and huge density of states in the band gap of silicon at the surface leads to an ambipolar behavior which is demonstrated in Fig. 2.12b by the transfer characteristic of a SB-MOSFET. As a consequence, a small voltage range is left to switch off the device making a complementary concept ad absurdum. Considering an inverter composed of SB-MOSFETs larger dynamic dissipation, smaller $V_{ss} - V_{dd}$ ranges, threshold voltage adjustment and half of the
on-off ratio have to be taken into account. Furthermore, the linear regime is replaced by an exponential rise and reduced current due to the additional contact resistance (Fig. 2.12c). Therefore, it is essential to achieve defined P- and N-type contacts on silicon which provide sufficiently low density of states in the band gap of silicon to suppress ambipolar behavior.

2.6.2 Dopant-Free CMOS-FET

In principle, all semiconductors are capable of providing either electron (N-type) or hole (P-type) carrier transport. The type of dopant at the contacts or even only the silicon-metal-interface determines the dominant carrier transport, although the interface accounts for a small part of the full device.

The incorporation of an ultra-thin silicon nitride tunneling barrier between metal and silicon offers a tunable coupling of metal into the silicon. Connelly et al. demonstrated that low work function metals with a silicon nitride layer in between reduce the parasitic resistance considerably [24, 25]. However, Ghoneim et al. proved with a thicker silicon nitride layer of approximately 0.8 nm (in contrast to the estimated 0.25 nm of Connelly) that the tunneling barrier leads to ohmic N-type MOSFETs.
and unipolar behavior [26,27]. It is worth mentioning that in the case of a Fermi level depinned interface without a tunneling barrier the metal would completely transform the silicon contact regions into metal-like contacts (Fig. 2.13a). In the first instance, this situation enables ohmic contacts but at the price of an ambipolar behavior of the MOSFET, which results once more in additional leakage current. The incorporation of an ultra-thin tunneling barrier provides a stronger band bending at the interface so that the injection of holes into the valence band is strongly reduced by the artificially higher potential barrier (Fig. 2.13b) while in the on-state the electron injection is less blocked leading to a trade-off situation of choosing the right silicon nitride thickness as illustrated in the Fig. 2.13c.
From Ultraviolet to Terahertz

This section deals with a detailed introduction of the optical characterization techniques ranging from ultraviolet (UV) to terahertz (THz). This spectrum offers insights into the band structure, composition of silicon nitride and its impact on silicon surface. The thickness of ultra-thin insulators requires a detailed understanding of ellipsometry, Fourier transform infrared spectroscopy (FTIR) and THz time domain spectroscopy.

3.1 Ellipsometry

Ellipsometry is a non-destructive method to determine the impact of a material on light, which is reflected on the surface. A defined polarized wave is targeted on the surface of a sample and the response is measured so that the change of amplitude and phase is associated to a characteristic behavior of the material. A polarizer and compensator (retarder) are responsible for the defined state of the incident light. Next, the light is focused on the surface of the sample under a specified angle. The reflected light is characterized by an analyzer. Assuming isotropic materials the reflection leads to a complex reflectance ratio:

\[ \bar{\rho} = \tan \psi e^{i\delta}, \]  

where \( \tan \psi \) is the ratio of changed amplitude and \( \delta \) denotes the relative phase shift of propagated light through the material. Ellipsometry measurements consist indispensably on existing models of the material so that no reference measurements are required.

In this work the ellipsometry characterization is based on nulling ellipsometry, which consists of a polarizer, compensator, sample and analyzer (PCSA) setup (Fig. 3.1 a). Linearly polarized light is generally transferred into an elliptical polarized state by the interaction with the sample surface [98, 99]. So, it is possible to find an elliptic polarized state of the light, which transposes into a linearly polarized state once it has interacted with the surface. The detection of this polarized state is performed by an analyzer. This analyzer is a polarizer with the crucial point that it detects the polarized state shifted by 90° in position to find the minimum signal (searching
3. FROM ULTRAVIOLET TO TERAHERTZ

Figure 3.1: a) Chain of PCSA is illustrated: Linearly polarized light (P) is compensated (C) to create an elliptical polarized light. Interaction with the sample (S) leads to linearly polarized light. Analyzer (A) searches the perpendicular polarized light (minimum), reprint permitted by Accurion GmbH, b) EP4 Accurion nulling ellipsometry composed of light source, polarizer, compensator, sample objective, analyzer and CCD chip is depicted.

for the “null”). Fig. 3.1a shows the applied nulling ellipsometer EP4 of Accurion. Consequently, the complex reflection depends on the angles of the PCSA $A_0$, $C_0$ and $P_0$ as follows:

$$\rho = \frac{\tan(A_0) \tan C_0 + \tau_c \tan(P_0 - C_0)}{\tau_c \tan(P_0 - C_0) - 1},$$  \hspace{1cm} (3.2)

where $\tau_c$ is the complex transmittance of the compensator. For the sake of completeness, it is mentioned here that this equation 3.2 is only valid for isotropic materials. A general approach consists of a reflection matrix [99]. Moreover, this method offers systematic error reduction by a four-zone null average owing to the 4 redundant PCA combinations [100, 101]:

$C_0 = +45^\circ$ \begin{align*}
\text{zone 2 with } P_0 \text{ and } A_0, \\
\text{zone 4 with } -P_0 \text{ and } -A_0,
\end{align*}  \hspace{1cm} (3.3)

$C_0 = -45^\circ$ \begin{align*}
\text{zone 1 with } P_0 \text{ and } A_0, \\
\text{zone 3 with } -P_0 \text{ and } -A_0.
\end{align*}  \hspace{1cm} (3.4)

This characterization procedure is suitable for ultra-thin layers due to the nature of an angle based probing technique in contrast to light-flux measurements, which requires permanently stable intensities during the analysis procedure. Fig. 3.2 illustrates $\psi$ and $\delta$ versus wave number for three different silicon nitrid layers grown at different temperatures. While $\psi$ (Fig. 3.2a) does not exhibit a difference between these layers, $\delta$ depends on these various ultra-thin layers highlighting the
3.2. Fourier Transform Infrared Spectroscopy

The first infrared spectroscopy analysis of materials was already done in 1882 [102]. Infrared spectroscopy provides a direct and simple measurement technique of the bonding between different atoms. Furthermore, this approach is even not restricted to the state of the material, it can be either in solid, liquid or gaseous states as long as the material is not a complete infrared absorber.

The infrared absorption by a molecule causes a multitude of displacements. Fig. 3.3 demonstrates scissor, wagging, twisting, symmetrical stretching, asymmetrical stretching and rocking modes of vibration. In principal, in solid state matter these vibrational modes are also existent, but do not exhibit rotational vibrational modes. Furthermore, these modes are affected by either additional bonded atoms or the density of the material itself [103].

Infrared spectroscopy based on a Fourier transformation routine is a fast method to measure a large spectrum in a short period of time (10 kHz). While in the beginning of the spectroscopy each wave number had to be setup individually, a major breakthrough was the introduction of a Michelson interferometer in combination with a fully automatic moving stage module. Whereas the interferometer features a high resolution, the highly accurate stage enables a rapid positioning of the interferometer leading to an interferometer spectrum (Connes’ advantage), which is Fourier-transformed into a wave number dependent intensity. Additionally, the light of an infrared source is subdivided into pieces by a monochromator featuring a...

Figure 3.2: a) Relative amplitude of three silicon nitride layers is shown grown at various temperatures 450°C, 850°C and 1100°C: None exact distinction, b) Relative phase of three silicon nitride layers is demonstrated grown at various temperatures 450°C (0.8 nm), 850°C (1.7 nm) and 1100°C (2.5 nm): The phase is directly related to the thickness of the material.

benefit of nulling ellipsometry (Fig. 3.2 b). It is quite remarkable that the thickness lies between 0.8 nm and up to 2.5 nm and the nulling ellipsometry provides three substantially different values for δ.

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Figure 3.3: Several displacements are illustrated: Moving atom (red), fixed particle and bonding (blue); six common types of vibrational modes: Rocking, scissor, wagging, twisting, symmetrical- and antisymmetrical stretching mode, huge red balls indicate out of plane vibration.

higher signal to noise ratio (SNR), which is described by Fellgett’s and Jacquinot’s advantages [104]. Depending on the electron number of the two types of atoms a particular quantum of infrared photon energy is absorbed which excites the bonding into a higher energy state. While the lifetime of the excited state is very short a negligible amount of reemission is part of the incident infrared spectrum (emission in all direction) leaving behind a fingerprint of the sample. To overcome the impact of the background absorption a reference measurement of the beam path without the particular sample is done. It accounts for the gases as CO₂, H₂O and even water in liquid phase. However, most of the studies require an analysis of a thin material on top of a substrate leading to an additional absorption due impurities inside of the substrate. For instance, Czochralski (CZ) substrates exhibit a considerable amount of impurities such as carbon and oxygen or even dopant-related bonds. At first glance, it is not straightforward to take into account these additional bondings owing to the small concentrations of approximately \(10^{13}\)...\(10^{17}\) cm\(^{-3}\) [105, 106], depending on the substrate thickness, simplification becomes a crucial key component.
to simplify the analysis. Substrate thicknesses in this work are 525±25 \( \mu \text{m} \) (4-inch wafer) and 625±25 \( \mu \text{m} \) (6-inch wafer). Keeping in mind that ultra-thin nitrides with thicknesses below 4nm are to be characterized and the conventional density of Si-N bonds is in the range of \( 10^{21} \text{ to } 10^{22} \text{ cm}^{-3} \) contaminants and dopant concentrations can be related to a ratio of doses:

\[
H = \frac{\{10^{15} \text{ cm}^{-3} \ldots 10^{17} \text{ cm}^{-3}\} \{525 \text{ \( \mu \text{m} \ldots 625 \text{ \( \mu \text{m}\}\} \}}{\{10^{21} \text{ cm}^{-3} \ldots 10^{22} \text{ cm}^{-3}\} \{0.8 \text{ nm} \ldots 4 \text{ nm}\}}
\]

which leads to a dose ratio

\[
H = \frac{5.25 \cdot 10^{13} \text{ cm}^{-2} \ldots 6.25 \cdot 10^{15} \text{ cm}^{-2}}{8 \cdot 10^{13} \text{ cm}^{-2} \ldots 4 \cdot 10^{15} \text{ cm}^{-2}}.
\]

Therefore, it is obviously mandatory to cancel out the absorption of the corresponding substrate to enhance the SNR. Indeed, a low resistivity Float Zone (FZ) material would bypass this circumstance. Furthermore, the measurement of a blank reference substrate requires a native oxide free surface but is relevant to provide a clear silicon nitride related response.

While the latter paragraph deals with reducing the background noise, the upcoming part describes the analysis of the corresponding vibrational modes. Several molecular vibrations modes exist where a proportional relation between concentration of bonds and absorption is observed as for instance the Si-H mode at 640 cm\(^{-1}\) (rocking/wagging mode) \[107\]. From the complex refractive index

\[
\bar{n}(\omega) = n(\omega) + ik(\omega),
\]

which consists of the refractive \( n(\omega) \) and the absorption (or sometimes attenuation) index \( k(\omega) \), the imaginary component depends on the absorption coefficient \( \alpha(\omega) \) as follows \[104\]:

\[
k(\omega) = \frac{\alpha(\omega)}{4\pi\omega}.
\]

The analysis of the absorbance of the silicon nitride layers provides the coefficient of absorption. Next, the integration over the absorption coefficient multiplied by the proportional factor \( C_{X\ldots Y} \) denotes the concentration of the molecular vibrational mode:

\[
N_{X\ldots Y} = C_{X\ldots Y} \int \frac{\alpha(\omega)}{\omega} d\omega.
\]

A direct and simple measurement of hydrogen is a crucial advantage of FTIR in contrast to X-ray photoelectron spectroscopy (XPS) \[108\]. For the sake of completeness, the reflectance has to be taken into consideration if the material has a high refractive index. For instance, the refractive index of 1.5 leads to reflectance of approximately 4\%, while a refractive index of 4 causes a reflection of 36\%.

Taking all these conditions into account the FTIR is an excellent technique which allows to obtain knowledge about the composition of ultra-thin materials, especially of ultra-thin silicon nitride layers, which is in detail characterized in section 4.3.
3. From Ultraviolet to Terahertz

3.3 Terahertz-Time-Resolved-Spectroscopy

The Terahertz (THz)-time-resolved-spectroscopy became more and more relevant for free charge carrier analyses in the early 90’s owing to new sophisticated sources and detectors to address this regime at that time. Two attributes of THz spectrum contributed to the huge success: First of all the corresponding energies (e.g. 1 THz: 4.1 meV) of the the electromagnetic fields do not harm matter at all, secondly, it propagates through a multitude of materials providing an elegant method to screen objects.

The generation of THz pulses has two main sources: Photogeneration of carriers $J_{\text{photocurrent}}$ and/or by a change of polarization $P(t)$. A simple expression of the radiated field $E_{\text{rad}}$ is based on Fraunhofer-approximation for the far-field by [110]:

$$E_{rad} \approx \mu_n S A 4\pi z \left\{ \frac{\partial J_{\text{photocurrent}}}{\partial t} + \frac{\partial^2}{\partial t^2} P(t) \right\},$$

(3.10)

where $\mu_n$, $S$, $A$, $z$ are the electron mobility, surface of the incident beam and distance between source and sample.

For instance, the characterization of the silicon-Si$_3$N$_4$-metal junction relies on the photogeneration of carriers. Therefore, an ultra-fast pump pulse (120 fs, 1 MW) is beamed towards the surface of the silicon to create electron-hole pairs. If no band bending of the silicon is present only the Dember-effect appears, where the currents consisting of holes and electrons differ due to the various mobilities. This effect is in general observed for semiconductors with much higher mobilities in contrast to silicon (e.g. InP, InAs) [111]. However, once a band bending is present generated carriers are accelerated by the electrical field of the junction, recombine and a characteristic THz pulse is emitted.

The detection of the THz pulse is achieved by either electro-optic detectors or photoconductive antennas. The former takes advantage of the Pockels-effect, where the larger THz pulse causes a polarization of the medium, which itself interacts with the probe pulse so that birefringence occurs. The detection pulse of the birefringence is closely related to the strength of the electrical THz field. The photoconductive antenna (Austin switch) requires an electric field between two terminals. The THz pulse leads to a current, which is amplified in a femtosecond resolved time domain. The amplitude of the current is directly related to the strength of the THz field.

Two other components are part of the THz setup. First of all, a dual phase lock-in boosts the signal-to-noise ratio, where a chopper reduces the Johnson-Nyquist noise owing to the bandwidth filtering [112]. The pump-laser pulse is half-split into so that the generated THz pulse is referred to the pump-laser pulse by a tunable delay stage enabling a time resolved spectroscopy.

While the characterization of Schottky junctions by THz emission is a known application, a band bending by ultra-thin ohmic tunneling barriers is a new area of silicon surface bending for THz emission (see Fig. 3.4). The THz characterization is done without biasing the junction. Hence, this technique provides a maximum field analysis, while electrical characterization approaches detect exclusively an averaged electric field owing to voids and defects in the ultra-thin silicon nitride layer.
Figure 3.4: THz pulse generation by the electrical field of the metal silicon interfaces and photogenerated carriers is depicted.

The Schottky-Mott diodes introduced in section 2.2.3 require a small spacing between both metals to increase the electrical field in the junction as high as possible. In section 5.7 the fabrication is described to produce metal spacings in the range of 20-30 nm. The reader is referred that a THz framework for tunneling barrier contacts provides an excellent tool to examine tunneling diodes, which is elucidated in detail in section 6.2.6.
Chapter 4

Silicon Nitride

Stoichiometric silicon nitride Si₃N₄ exhibits three crystalline phases, specified as α, β and γ [113–115]. The first two phases are the most common ones, while the γ phase is only established under high vacuum [116]. These crystal phases are basically formed above melting temperature of silicon [117]. However, in contrast to the variety of applications as ceramic based material [118], amorphous silicon nitride has gained interest in the semiconductor industry due to a multitude of applications e.g. anti-reflective coating, field-effect passivation, insulator, hard mask for etching, deoxyribonucleic acid (DNA) separation, extreme ultraviolet (EUV) masks, background for scanning electron microscope (SEM) as well as transmission electron microscope (TEM) analysis [119–133]. Amorphous silicon nitride layers can either be deposited or be grown on silicon. Several different processes are established either by using plasma enhanced-, low pressure chemical vapor-, physical vapor- or atomic layer deposition procedures and molecular beam epitaxy (PECVD, LPCVD, MBE, ALD) [134–139]. The growth of an insulator has particular benefits in contrast to deposition as will be demonstrated in the upcoming sections.

4.1 Growth of Silicon Nitride

At first glance, molecular nitrogen would be expected as a preferred reactant similar to a dry oxidation procedure with molecular oxygen [140], but the triple bond of molecular nitrogen requires either high temperatures (>1200 K) or a plasma assisted dissociation procedure [141–149]. Ammonia offers an attractive source of nitrogen, where nitrogen is bonded to three hydrogen atoms at an angle of 106,67° [150]. The nitrogen-hydrogen bonding energy is almost two and a half times smaller than the triple bond of N₂ (N-H: 386 kJ/mol, N-N: 942 kJ/mol) [151, 152]. Therefore, temperatures close to 100 K are sufficient to ensure a surface reaction between silicon substrate and ammonia [153]. It was proven that on dimerized silicon surfaces (100)- (2x1) dissociation of ammonia takes place at these low temperatures. Silicon dimers crack ammonia into N-H₂ and hydrogen. The latter one saturates a dangling bond of neighboring silicon atoms [154, 155]. Furthermore, it was demonstrated that even one atomic layer of SiNH₂ and Si-H at the surface exists at low temperatures [156].
4. Silicon Nitride

However, these experiments rely on MBE grown silicon layers, which exhibit an excellent surface smoothness. Silicon nitride grown on CZ and FZ substrates do not reveal these smooth features. Nevertheless, X-ray reflectivity (XRR) measurements of approximately 3.7 nm thick grown nitrides show a small roughness of 3.2 Å. While high temperature ammonia based silicon nitrides are well known since 1970s [147, 149], nitrides formed in the temperature range of 350°C-800°C were not in detail studied investigated.

4.2 Rapid Thermal Nitridation

Rapid thermal nitridation (RTN) combines a fast and cost-efficient processing owing to the small chamber with a high vacuum pumping systems, which is depicted in Fig. 4.1. An array of halogen lamps heats up quickly (∼75 K/s) the wafer in an ammonia atmosphere.

As already mentioned before, silicon nitrides grown at higher temperatures are well described in literature [144, 149]. Ludsteck et al. have demonstrated that excellent insulators are fabricated by a rapid thermal procedure [145, 146]. As a starting point, a high nitridation temperature of 1060°C was chosen to establish a reliable and mature process of stochiometric silicon nitride layers. Squared samples of a 1.5 cm size are nitrided on a 6-inch wafer, which has a thick silicon nitride layer to exclude an ammonia consumption during the annealing.

Increasing the flux of ammonia from 100 sccm to 300 sccm reduces the variation of the thickness as depicted in Fig. 4.2 left hand side. Moreover, a short duration

![Figure 4.1: Rapid thermal processing machine is depicted with an open chamber, Anneal-Sys has permitted the reprint.](image-url)
<60 s and a small flux of 100 sccm is not sufficient to ensure a homogenous ammonia atmosphere in the chamber causing huge thickness deviation and native oxidation outside the chamber (see Fig. 4.2). It turns out that small fluxes of NH₃ do not provide a reliable fabrication procedure owing to the single-side inlet of ammonia inside the cold wall reactor. Thus, the position of the samples on top of the carrier wafer affects strongly the nitride thickness, which is confirmed by the results obtained with 100 sccm (shown in Fig. 4.2 middle part). Obviously, a prolongation of the annealing process solves this. The time dependent thickness confirms that the nitridation process does not grow logarithmically. A larger flux (here 300 sccm) solves this issue and enables small variations of thicknesses (right hand side) less than 0.1 nm from sample to sample and run to run. The best reproducible and reliable nitrides are formed by an argon/ammonia flux ratio of 1000/300 sccm confirmed by the process at 900 °C and a flow for 60 s (see Fig. 4.2). The thickness of silicon nitrides grown at 300 sccm, 300 s at 1060 °C were confirmed by three different ellipsometry systems verifying the thicknesses (see appendix B). The deviation is approximately 0.1 nm, which underlines the highly sophisticated silicon nitride layer (even for 4-inch wafers).

Figure 4.2: Silicon nitride thickness is demonstrated for various process conditions; Left hand side: fixed duration at 1060 °C for three different ammonia currents, 100 sccm, 200 sccm, 300 sccm, middle region: fixed current at 1060 °C for various annealing times: 10 s, 60 s, 90 s, 120 s and 180 s, right hand side: exhibits small variation for 60 s with a flux of 300 sccm at 900 °C; two types of symbols for each process setup imply two individual nitridation runs.
4. Silicon Nitride

4.3 Characterization of ultra thin Silicon Nitride Layers

Whereas $\text{Si}_3\text{N}_4$ thickness above 1nm are rather suitable for an insulator technology, which was the original idea behind the development of silicon nitride layers [145, 146, 157], the interface engineering nitride has to be thinner to avoid a MOS-capacitor contact behavior. It turns out that a reduced duration of nitridation down to 60s still produces similar thicknesses if an ammonia flux of 300sccm is considered. Thus, different thicknesses of the nitride layer are realized with various growth temperatures.

Fig. 4.3 shows the silicon nitride thickness as function of temperature. The small activation energy of $E_a = 0.061 \text{eV}$ determined by the slope emphasizes that according to Wu et al. the growth of silicon nitride occurs in the logarithmic regime, where the thickness $t_{\text{Si}_3\text{N}_4}$ depends on time as follows [147]:

$$t_{\text{Si}_3\text{N}_4}(\tau) = L_{\text{NH}_3} \log(\alpha_a \tau + 1),$$  \hspace{1cm} (4.1)

$L_{\text{NH}_3}$ is the diffusion length of the ammonia related species and $\alpha_a$ a constant. The logarithmic behavior is often attributed to the higher density of silicon nitride in contrast to silicon dioxide [66, 67]. XRR measurements verified the high density of $\approx 3.4 \frac{g}{cm^3}$.

However, decreasing the temperature changes the dissociation of the ammonia.

![Figure 4.3](image-url)
4.3. Characterization of ultra thin Silicon Nitride Layers

Hence, FTIR measurements were carried out for three nitridation temperatures 450°C, 600°C and 1100°C displayed in Fig. 4.4. Owing to the ultra-thin silicon nitride layers, hydrogen or nitrogen-hydrogen bonds, which are apparent at higher wave numbers, are not observed. Thus, the FTIR spectra are reduced to a wave number range of 500-1200 cm\(^{-1}\).

Hydrogen is mainly incorporated at either broken bonds (tetravacancies) at 618 cm\(^{-1}\) (cf. the close-up displayed in Fig. 4.5a) or is present as a Si-H wagging mode at 650 cm\(^{-1}\) (see Fig. 4.5b) [158,159]. The wagging mode is related to the hydrogen concentration \(N_H\) of the silicon nitride (see section 3.2) so silicon nitride layers which are grown at 450°C exhibit a hydrogen concentration of approximately 13-15 % [160–163]. It is well known that this rather large amount of hydrogen deteriorates the insulating properties of nitrides as demonstrated by Parsons and Brown [164,165]. Nevertheless, it is likely that the high hydrogen concentration contributes positively by efficiently saturating the dangling bonds. Hence, one part of the interface state density is reduced. At a nitridation temperature of 1100°C, the Si-H mode at 618 cm\(^{-1}\) is not observed indicating that such a high temperature results in the formation of further silicon nitrogen bonds due to the complete decomposition of ammonia [166]. Accordingly, the hydrogen concentration is below 5 % based on the wagging mode. Moreover, Larsson et al. demonstrated that the hydrogen is released from silicon at 1100 K [154].

**Figure 4.4:** FTIR spectra of three nitridation temperatures are depicted: 450°C, 600°C, 1100°C.
In contrast, the intensity of the silicon nitrogen tetrahedra mode at 685 cm\(^{-1}\) does not vary with nitridation temperature (cf. Fig. 4.4). However, the Si-N asymmetric stretching mode is now observed at a broad, symmetric and intense peak centered around 875 cm\(^{-1}\) indicating a stoichiometric nitride (Fig. 4.5c). For lower nitridation temperatures, an asymmetric Si-N stretching mode at 849 cm\(^{-1}\) and a Si-N-H\(_2\) mode at 891 cm\(^{-1}\) exist\(^{[167–169]}\). These two peaks are often also attributed to the Si-H bond bending doublet Si-H\(_2\) wagging and scissor mode\(^{[170]}\), demonstrating the change of a hydrogen to a nitrogen bond at higher temperatures. Particularly the dissociation of N-H\(_2\) at 800 K need to be clarified if these bonds are inside the silicon nitride layer or at the surface\(^{[154]}\). In addition, a new mode at 964 cm\(^{-1}\) appears (see Fig. 4.5d) which is associated to planar silicon nitride formation\(^{[171,172]}\). Stretching modes of Si-H and N-H for wave numbers above 2000 cm\(^{-1}\) were not observed due to the lack of thickness for ultra-thin nitrides.

![Figure 4.5](image)

**Figure 4.5:** Characteristic vibrational modes of SiN-H are demonstrated: (a) 618 cm\(^{-1}\) Si-H, (b) 875 cm\(^{-1}\) Si-N, (c) 649 cm\(^{-1}\) Si-H wagging mode, (d) 964 cm\(^{-1}\) Si-N mode occurs only at high temperatures.
According to Giorgis et al., N-H reacts exothermically with silicon to form Si-N and Si-H bonds justified by N-H concentrations less than 5% [173]. Table 4.1 gives an overview of the vibrational modes of the ultra-thin silicon nitride layers presented here.

The results of the FTIR study verify the presence of hydrogen in the SiN_x layers. A high hydrogen fraction deteriorates the insulating properties of the silicon nitride layers which will be further discussed in chapter 6. Nevertheless, the advantage of hydrogen is the saturation of dangling bonds either from nitrogen or silicon, so that the passivated dangling bonds do not contribute to the gap states [150]. It is also evident that at higher nitridation temperatures additional silicon nitrogen bonds are created consistent with a strong temperature dependent silicon nitride growth mechanism (see Fig. 4.3).

<table>
<thead>
<tr>
<th>wavenumber [cm⁻¹]</th>
<th>Si-X bond</th>
<th>Vibrational mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>618</td>
<td>Si-H</td>
<td>broken bond (tetravacancies)</td>
</tr>
<tr>
<td>649</td>
<td>Si-H</td>
<td>wagging mode</td>
</tr>
<tr>
<td>667-669</td>
<td>Si-B</td>
<td>related to substrate doping</td>
</tr>
<tr>
<td>849</td>
<td>Si-N</td>
<td>asymmetric stretching mode</td>
</tr>
<tr>
<td>875</td>
<td>Si-N</td>
<td>asymmetric stretching mode</td>
</tr>
<tr>
<td>891</td>
<td>Si-N-H₂</td>
<td>nitrogen-hydrogen vibrational mode</td>
</tr>
<tr>
<td>964</td>
<td>Si-N</td>
<td>of a planar silicon nitride formation</td>
</tr>
<tr>
<td>1108</td>
<td>Si-O-Si</td>
<td>of the interstitial oxygen</td>
</tr>
</tbody>
</table>

Table 4.1: Vibrational modes in ultra-thin silicon nitride layers are listed grown at 450°C, 600°C and 1100°C on CZ-P-type doped silicon substrates.

4.4 Post Annealing Characterization

The impact of temperature treatments on silicon nitride layers grown at different temperatures in a defined atmosphere is of main interest, when further processing steps are taken into account. In Table 4.2 several post annealing procedures including the untreated nitrides are listed. The refractive index is close to 2.0 at 633 nm known in literature [173–175]. However, it is well known from ultra-thin silicon dioxide that the refractive index rises with decreasing thickness owing to the more or less gradual transition from stoichiometric SiO_2 to Si-Si, which was never observed for any nitridation temperature [176]. Nonetheless, the higher density in contrast to SiO_2 could explain the absence of an increased refractive index [177,178]. Moreover, the ellipsometry measurements are based on a model that uses thick stoichiometric silicon nitride of Philipp [179], which was also applied by Ghoneim et al. but was never studied for ultra-thin tunneling nitrides [26,27]. An annealing step in a mixture of nitrogen and hydrogen effects neither the thickness nor the refractive index verifying a sufficient amount of already passivated silicon dangling bonds. A post annealing in argon at 850°C decreases the refractive index caused by a reduction of hydrogen (Fig. 4.5a) in accordance with literature [175]. Nitrides, which were
4. Silicon Nitride

annealed at 850°C, are thicker due to residual ammonia inside the rapid thermal processing (RTP) chamber because the chamber was not flushed with inert gases prior to HTT. The outgasing of hydrogen is verified by an additional second annealing in N\textsubscript{2}\textbackslash H\textsubscript{2} causing a rise of the refractive index closer to the value of the initial silicon nitride layer. In principle, this is the first ellipsometry study of ultra-thin tunneling barriers for thicknesses between 0.8 nm up to 1.7 nm.

<table>
<thead>
<tr>
<th>process</th>
<th>thickness [nm]</th>
<th>refractive index n</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st: Original state</td>
<td>0.8</td>
<td>1.958</td>
</tr>
<tr>
<td>2nd: Original state</td>
<td>0.8</td>
<td>1.963</td>
</tr>
<tr>
<td>1st: OS + hydrogen annealing</td>
<td>0.8</td>
<td>1.959</td>
</tr>
<tr>
<td>2nd: OS + hydrogen annealing</td>
<td>0.8</td>
<td>1.962</td>
</tr>
<tr>
<td>1st: OS + high temperature treatment</td>
<td>1.3</td>
<td>1.894</td>
</tr>
<tr>
<td>2nd: OS + high temperature treatment</td>
<td>1.3</td>
<td>1.899</td>
</tr>
<tr>
<td>1st: OS + HTT + HA</td>
<td>1.3</td>
<td>1.939</td>
</tr>
<tr>
<td>2nd: OS + HTT + HA</td>
<td>1.3</td>
<td>1.924</td>
</tr>
</tbody>
</table>

Table 4.2: Table summarizes the impact of post annealing steps on thickness and the refractive index: Original state (OS) at 450°C, 300 sccm, 60 s, 1000 mbar; hydrogen annealing (HA) N\textsubscript{2}\textbackslash H\textsubscript{2} at 400°C, 5 min, 1000 mbar; high temperature treatment (HTT) at 850°C, 300 sccm, 60 s, 1000 mbar.

The impact of the nitride on the silicon surface is investigated by quasi-steady-state photo conductance (QSSPC) measurements [180]. First of all, virgin silicon CZ wafers directly measured with native oxide exhibit the smallest observed lifetime of approximately 3 µs attributed to the absent chemical and field-effect passivation of the surface (see Fig. 4.6). However, the CZ wafers show very low bulk lifetimes. Therefore, an oxide of approximately 90 nm is grown to ensure a perfect chemically passivated surface, QSSPC measurements confirm a lifetime of close to 50 µs. If the wafer is dipped in 1 %-HF and immediately measured afterwards, the wafers exhibit a lifetime of close to 25 µs caused by hydrogen passivation at the surface, which decays with time owing to the native oxidation [181]. If this wafer is nitrided at 450°C a lifetime of 12 µs is observed. Wafers, which were not RCA cleaned prior to the HF Dip, but are directly dipped after taking out of the box have the highest lifetime of about 16 µs. Moreover, it turns out that even a two-time RCA clean procedure lowers the lifetime owing to the wet chemical process. In addition, a hydrogen annealing directly in the chamber does not increase the lifetime at all indicating an already substantial amount of incorporated hydrogen, while an annealing at 850°C in argon atmosphere reduces the lifetime to 8 µs of the silicon proving the loss of hydrogen. A lifetime of approximately 32 µs is achieved for a nitridation temperature of 250°C, which is slightly higher than for the 1 %-HF dipped samples owing to the growth of silicon nitride, whereas the hydrogen fluoride etchant saturates solely the dangling bonds by an atomic layer of hydrogen. Similar to the 1 %-HF dip the lifetime decreases indicating an outgasing or even an oxidation of the nitride grown at 250°C. After 36 hours a lifetime of approximately 7 µs is obtained. If only one
4.5 Ultra Thin Silicon Nitride Insulator

The functionality of ohmic tunneling barriers requires an excellent insulator property with no trap assisted tunneling. While a capacitance analysis of nitrides grown at 450°C is not feasible owing to the ultra-thin dimensions, thicker nitrides, which are applicable for capacitors, are suitable to be characterized by CV measurements. An aluminum layer of 100 nm thickness is deposited on top of silicon nitride layer and patterned by a lift-off process; the backside of the substrate is covered completely with aluminum. Fig. 4.7a shows the high frequency CV measurements of two different nitrides (1.7 nm grown at 850°C and 2.3 nm grown at 1100°C), indicating a strong variation of the full depletion voltage for a higher nitridation temperature.

Figure 4.6: QSSPC lifetime results for various processing treatments are shown; capped by native oxide, thermally grown SiO$_2$, dipped in 1%-HF (declining over time), nitridation at 450°C, high thermal treatment in Ar at 850°C, arrows stand for the degradation (outgasing of hydrogen) of the nitrided surface.

or two monolayers of nitride with a substantial amount of hydrogen exist the native oxidation starts at the saturated Si atoms causing a reduction of the carrier lifetime (see section 4.1). In order to reduce the impact of the equipment consisting of sample holder, tweezer and beakers are cleaned following the recipe presented in the appendix H. Hydrogen inside the silicon nitride and the CMOS clean high vacuum process provide a sophisticated technology of ultra-thin passivation layers.
While the nitride grown at 850 °C exhibits an excellent slope, no humps and even no hysteresis is apparent (the backward curve is completely covered by the forward graph). Secondly, a hysteresis is observed demonstrated by a voltage shift of approximately 115mV (Fig. 4.7 b). However, a post-metal-annealing (PMA, 400 °C) step of the final MOSCap in N₂\H₂ atmosphere improves the silicon-silicon nitride stack. For instance, the hysteresis is completely gone and the capacitance in fully accumulated state is increased. Moreover, the slope of the hydrogen annealed capacitors increases. However, due to the higher total capacitance value the range of the applied bias to switch from accumulation to fully depletion is unchanged highlighting that dangling bonds of silicon and nitrogen are passivated [145, 146, 182–184]. This passivation is directly observed for low frequency measurements exhibiting a small inversion, which does not appear without a PMA (Fig. 4.7 c). Nevertheless, a small hump is observed, if the fully depletion state is reached, which is attributed to frequency dependent interface traps [185–187]. Despite the fact of a greater capacity (Fig. 4.7 c) and vanished hysteresis, these additional interface states originate from the PMA. Here, a detailed study of the impact of metal evaporation process on the silicon nitride can give further insights.

**Figure 4.7:** CV-characteristics of ultra-thin silicon nitride layers are shown: a) CV-measurements of nitrides grown at 850 °C and 1100 °C at 100 kHz, b) hysteresis of nitrides grown at 1100 °C, c) reference samples and samples with PMA (Post Metal Annealing), d) plasma nitride grown in an Inductively Coupled Plasma Chemical Vapour Deposition chamber on N-type silicon substrates; Nitridation, 1 min, RF power 30 W, ICP 100 W, 100 mTorr at 280 °C.
An alternative growth of ultra-thin nitrides is performed by dissociation of either nitrogen or ammonia due in a RF plasma chamber \cite{142, 143}. A CV plasma silicon nitride is given in Fig. 4.7 d, which is manufactured on top of a low doped N-type silicon substrate. Here, no interface traps are present. However, also a hysteresis loop appears assisting the previously demonstrated nitrides thermally grown in ammonia atmosphere at high temperatures. Nevertheless, nitrides grown at lower annealing temperatures show an excellent performance (see Fig. 4.7 a).

### 4.6 Low Stress Diffusion Barrier

The high density of silicon nitride promises to produce excellent ultra-thin diffusion barriers. Murarka et al. demonstrated that the diffusion of oxygen is significantly hampered \cite{149}. To confirm the outstanding density of silicon nitride several nitride layers are grown at 1200 °C, 850 °C and 450 °C. The thickness of 3.5 nm (1200 °C) is determined by ellipsometry and XRR measurements (see Fig. 4.8 black curve), while the nitrides grown at lower temperatures are only characterized by ellipsometry owing to the ultra-thin thickness for XRR analysis (Fig. 4.8 red curve). Nevertheless, the higher density of silicon nitride in contrast to silicon oxides offers a diffusion barrier analysis, where ultra-thin silicon nitride layers lower the diffusion of molecular oxygen. Oxidation is done in a 600 hPa O$_2$ atmosphere at 1000 °C for 30 min.

![Figure 4.8: X-ray reflectivity results of nitrides are depicted grown at 1200 °C and 1000 °C on P-type silicon substrates (5-10 Ωcm)](image-url)
4. Silicon Nitride

Reference samples were standard cleaned and the wet chemically grown oxide by HCl:H$_2$O$_2$:H$_2$O (Standard Clean, SC2) is applied as a defined initial layer for oxidation. After 30 minutes of oxidation an oxide thickness of approximately 30.1 nm is monitored (Fig. 4.9a). The oxygen diffusion is strongly reduced by the thickest silicon nitride (grown at 1200 °C) as it can be seen from the SEM images (Fig. 4.9b), where only a very small oxide layer is barely observed. If it comes to thinner nitrides (850 °C and 450 °C), the presence of oxides of approximately 9 nm or 20 nm is clearly observed by SEM (Fig. 4.9c) and Fig. 4.9d) verifying the higher density even for low temperature grown nitrides in contrast to a silicon oxide SC2-layer (Fig. 4.9a).

However, replacing the native oxide or ultra-thin silicon dioxide layer by a defined interfacial layer of Si$_3$N$_4$ allows one to reduce the overall thickness of the interfacial layer below 1 nm. Thus, high-K gate stacks and post annealing procedures become attractive. For instance, on top of 0.7 nm thick grown SiN$_x$ titanium is evaporated, which is afterwards annealed in oxygen up to a temperature of 800 °C to fabricate the high-K TiO$_2$. Titanium oxide is a high-K material and is an excellent passivation layer for transition metal dichalcogenide which pushes superconducting states in transition metal dichalcogenide (TMD) to bypass ionic liquids [188–193]. A cross-section SEM image does not exhibit any silicide formation highlighting the excellent diffusion barrier (Fig. 4.10a).

The silicon nitride diffusion barrier offers new application, if it comes to silicide based technologies. The high density and smaller bandgap in contrast to SiO$_2$ is a door opener for superconductor insulator superconductor (SIS) sandwiches by taking advantage of silicon based superconductors (CoSi$_2$, V$_3$Si, PtSi). Pioneering this is the first time that thermally grown insulators and silicide superconductors can be fabricated. First of all, it is well known that cobalt diffuses into silicon as well as silicon diffuses into cobalt as depicted in Fig. 4.10b. The illustrated edge of the cobalt lift-off is demonstrated by a red line and a lateral diffusion is observed. Moreover, the silicidation by CoSi$_2$ does not increase the roughness of the polished surface indicating a smooth process. It is worth mentioning that this silicon nitride has a thickness of 0.8 nm, which has to be thicker when a Josephson-junction concept is considered. Nevertheless, it is pioneering work that an insulator and superconductor are grown out of the same crystalline substrate.

Low stress of silicon nitride layer is a crucial attribute for MOSFET and membrane application. Hence, to verify a low stress material, nanowires with <111> silicon planes are formed by TMAH\IPA (tetramethylammonium hydroxide\isopropyl alcohol) etching and nitrided at 1100 °C (Fig. 4.10c). The SEM images do not exhibit any bending of the suspended wires (compare parallel red dashed lines). A detailed process overview is added to the appendix D.
Figure 4.9: Diffusion barrier tests of silicon nitride layers are done in oxygen atmosphere (600 hPa) at 1000 °C for 30 min: a) Initial SC2 oxide, ~32 nm, b) at 1200 °C grown nitride diffusion barrier <10 nm, c) at 850 °C grown nitride diffusion barrier ~10 nm, d) At 450 °C grown nitride diffusion barrier 20.1 nm.
Figure 4.10: a) Titanium completely oxidized by RTP, silicide is not present, b) cobalt diffuses into silicon, where on the surface a low temperature (450 °C) grown nitride is apparent, c) suspended silicon wires, which are capped on the top faces by a thick silicon nitride layer to examine the stress induced relaxation, red parallel and dashed lines demonstrate no relaxation.
4.7 Ultra Thin Hard Mask for Anisotropic Etching

Silicon nitride layers grown at temperatures below $< 1200^\circ C$ exhibit thicknesses less than 3 nm, which offer an excellent hard mask material for anisotropic etching processes in spite of small thicknesses. Maintaining a CMOS process anisotropic etching is restricted to tetramethylammonium hydroxide (TMAH). Therefore, a silicon sample was nitrided at $1100^\circ C$ and patterned by an optical lithography step and a subsequent plasma etching in $SF_6\cdot O_2$. Fig. 4.11a shows the Secondary electron microscope (SEM) image of this TMAH etched silicon nitride sample at $65^\circ C$ with a small portion of isopropyl alcohol to lower the surface roughness. The cross-section image of silicon surface confirms that the ultra-thin silicon nitride mask is still present. A few smaller grooves at the silicon surface are observed due to the hydrogen fluoride dip, which harms the nitride seriously in contrast to TMAH. For instance, 20 s in 1 %-HF etches several pinholes into the material (SEM-Fig. 4.11 b). However, in principle silicon nitride layers can sustain up to 10 s in 1 % HF without loosing their closed form (see SEM-Fig. 4.11 c). A native oxide removal step by HF can be replaced by immediately etching in TMAH directly after dismounting of the reactive ion etching chamber. Even the thinnest nitrides grown at $450^\circ C$ show a promising hard mask property for anisotropic etching (not shown here) which can withstand at least five minutes in TMAH leading to an overall small etching rate similar to nitrides deposited by LPCVD [194].

Taking advantage of this outstanding TMAH etching resistance low stress (see section 4.6) ultra-thin silicon nitride membranes are formed out of a silicon on insulator substrate. A detailed description of the manufacturing procedure is given in section 5.3.
Figure 4.11: Ultra-thin silicon nitride hard mask functionality for TMAH etching are demonstrated: a) low temperature nitride$_{450\,\degree C}$ mask for TMAH etching of 2.55 µm depth, pinholes at the surfaces confirm the HF-impact, b) SEM image of a groove, which exhibits a huge amount of unintended grooves/pinholes attributed to the HF-Dip, c) SEM image of a 10s 1%-HF-Dip process verifying the excellent etching resistance of TMAH.
4.8 Summary

In principle, the characterization of ultra-thin nitride layers demonstrates that excellent insulators are fabricated by RTN. Nitrides fabricated at temperatures below 1100°C exhibit excellent insulating characteristics. Furthermore, despite the fact that a large amount of hydrogen is present in silicon nitride layers grown at 450°C, this hydrogen increases the excess minority carrier lifetime by passivating the silicon surface if a thickness of less than 1 nm is considered. These excellent insulating and passivating properties are of great importance, for instance, MIS-solar cell concepts.
Chapter 5

Device Fabrication

Before the fabrication of the MOSFETs, Schottky-Mott diodes and resonant tunneling diodes is described in detail the relevant elements of the the micro- and nanostencil mask construction are introduced. While the microstencil masks are key for a successful implementation of the Schottky-Mott diodes, the nanostencil mask offers an interesting tool to check the impact of metal contaminants during processing because the silicon nitride is completely exposed to contamination in the ambient. The nanostencil mask has several additional process steps in contrast to the microstencil lithography. Between these two processes one section deals with the fabrication of crystalline silicon-oxide membranes, which offer a variety of applications such as sophisticated silicon nitride based bipolar junctions. The flow of processes of the silicon nitride based diodes is specified. Afterwards, the technology of complementary MOSFETs by a silicon nitride interface engineering is demonstrated, where the technological issues of the P-type MOSFETs are tackled. Finally, the fabrication of the resonant tunneling diodes are given.

5.1 Microstencil

Evaporation of atoms, reactive ions or dopants are stopped or passed through by a pattern in the stencil mask offering a non contact lithography to avoid any surface damage by contact. In principle, microstencil lithography is a resist-less, straightforward and parallel fabrication technique, speeding up the manufacturing procedure, if two major challenges namely clogging and blurring are taken into account. Considering the conventional photolithography a stencil based approach has raised the overall yield of successfully manufactured diodes avoiding photolithography related issues based on an increased complexity of manufacturing, sticking issues on the surface for high work function metals (lift-off) and particle deposition. The stencil masks for dopant-free diodes are made of Czochralski- silicon substrates. At a first glance, it appears to be an elegant solution to etch straight through the silicon for instance by an established BOSCH-process [195]. However, it has several drawbacks such as massive carrier wafer etching, thicker resist thicknesses (>5 µm) and a reactive ion etching (RIE) machine with a BOSCH process functionality.
5. Device Fabrication

Figure 5.1: Fabrication procedure of groove microstencil masks is illustrated: a) substrate is sealed by a LPCVD layer on the polished and rough surfaces. The backside is not polished illustrated by an undulating surface, b) LPCVD is patterned either by wet chemical etching or RIE, c) anisotropic backside etching by potassium hydroxide at 96 °C.

Thus, an anisotropic wet chemical etching of silicon offers an affordable process with predetermined angles depending on crystal facets of silicon. Etching of <100> silicon stops almost on silicon <111> crystal facets owing to the much lower etching rates. Furthermore, these different crystal facets lead to grooves which offer a simple way of various depositions without shifting the mask or sample just by tilting the sample-mask stack.

In order to manufacture the stencil mask the silicon substrate is covered by a closed silicon nitride layer (Fig. 5.1 a). Next, the material is patterned either by an RIE or wet chemical H$_3$PO$_4$ etching step as depicted in Fig. 5.1 b. It is worth mentioning that AZ15nxt survives the nitride etching despite the fact that the wet chemical etching is carried out at 165 °C. Silicon nitride is an excellent material as a hard mask to withstand potassium hydroxide etching (KOH) at high temperatures temperatures (>90 °C) in contrast to silicon dioxide. Once the silicon nitride layer has openings the samples are immersed into potassium hydroxide after removal of the native oxide by hydrofluoric acid (Fig. 5.1 c). Several challenges are identified in small beakers, a list of issues and corresponding solutions is given in appendix G. Most of the etching is carried out at 96 °C in order to increase the etching rate of the <100> silicon facets owing to the thick substrate (CZ-Si substrates 525 µm), which takes approximately four hours of etching. One promising PECVD (T: 475 °C, RF-P: 30 W, SiH$_4$: 40 sccm, NH$_3$: 45 sccm, He: 300 sccm, P: 15 mTorr, thickness approximately 220 nm) and one LPCVD (T: 770 °C, 27 min, 280 mTorr, NH$_3$: 450 sccm, SiH$_2$Cl$_2$: 74 sccm, 100 nm, thickness approximately 200 nm) silicon nitrides were under investigation. However, it turned out that the PECVD layers are not suitable for harsh anisotropic etching conditions. After two hours of etching in potassium hydroxide the silicon nitride layers exhibit a largely damaged surface attributed to a silicon- and hydrogen rich and low dense composition (Fig. 5.2 a). It is obvious that even the initial size of the pattern increased from 1mm up to 1.3 mm. The inset shows the cross section of one groove verifying an insufficient masking by sil-
5.1. Microstencil

icon nitride. Even the aforesaid LPCVD nitride failed after three hours of etching stressing the need of an excellently developed silicon nitride layer. Increased etching resistance is associated with a smaller amount of hydrogen and a higher density. An excellent LPCVD silicon nitride material is offered by Hahn-Schickard-Gesellschaft-Institut für Mikro- und Informationstechnik (HSG-IMIT). This material does not suffer from low density or hydrogen, which is confirmed by FTIR measurements (see appendix K).

This particular nitride perfectly seals the complete samples during KOH etching as depicted in Fig. 5.2b, which shows a silicon nitride membrane etched from the rear side of the silicon substrate. Furthermore, a small misalignment of 2° is observed which is attributed to the optical lithography step or dicing alignment. The increased width and length of the membranes is associated with the etching of the <111> planes, which gives an underetching of 13 μm depicted in the SEM image (Fig. 5.2b) leading to an etching ratio of

\[ V(96{°}C) = \frac{V_{100}}{V_{111}} \approx 48.1. \]  

(5.1)

Owing to the excellent etching resistance of the LPCVD nitride the initial thickness of the SiN layer can be further reduced. 20 nm of nitride are etched by harsh KOH etching (Fig. 5.2c), which allows to reduce the silicon nitride thickness by at least a factor of four to simplify the preceding process steps. The final step consists of the removal of silicon nitride, which is fully etched by phosphoric acid at 165 °C.

A complete process overview of the steps and associated parameters is attached in appendix I.

Stencil lithography has two disadvantages: Clogging and blurring issues [196–205]. Clogging shrinks the feature size due to the deposition of material inside and on top of the apertures. However, most of the deposited materials are easily removed without harming the silicon aperture pattern due to the high etching selectivity between silicon and metals. By cleaning the mask the initial state is always established ensuring reproducible and reliable repetition of the deposition process through the stencil. Blurring, however, becomes a challenge (see Fig. 5.3) if two requirements are not fulfilled:

- Large distance \( D \) between evaporation source and stencil mask
- Small gap \( G \) between mask and substrate.

Taking into account these specifications and assuming that the diameter \( D_S \) of the evaporation source is much larger than the aperture size \( A_S \) a simple expression for the blurring \( B \) is given by:

\[ B \approx A_S + \frac{D_S \cdot G}{D}. \]  

(5.2)

Fig. 5.4a shows an image of three deposited pads, where the gap is approximately 114 μm indicating a tremendous amount of blurring. If the stencil mask is in direct
Figure 5.2: SEM-images demonstrate the damage caused by etching, the underetching and the remaining excellent LPCVD SiN hardmask: a) SEM image of a PECVD silicon nitride hard mask demonstrates the insufficient etching resistance after two hours of KOH etching, intense surface etching damage, inset: cross-section SEM image exhibits only a smooth groove bottom, b) LPCVD sealed Si substrate shows an established silicon nitride membrane, underetching associated to mask misalignment, c) cross-section image of the rear side confirms the high etching resistance of LPCVD-nitride, 170.2 nm remained of initial 210 nm silicon nitride after 4 hours of KOH etching.
contact, the edge of the pad becomes sharp confirming a substantial reduction of blurring as displayed in Fig. 5.4b by the evaporated aluminum area. The deposited gold is cut at the top of the image attributed to the angle of 60° during deposition which is larger than 54.7°. It is an attractive approach to reduce the contact area in one dimension without fabricating a new mask with smaller openings. However, a closer look at the surface of the substrates reveals a very thin deposited layer of metal surrounding the pattern (see inset Fig. 5.4a und b), which is called halo in literature [196]. The halo effect is recognized by the green glimmer around the evaporated gold area (see Fig. 5.4 bottom). The big advantage is that tilting the sample-mask stack simplifies the deposition of various metals (see Fig. 5.3). Several metals can be simply evaporated by rotating horizontally the sample by ±90° and 180° in combination with different angles. In order to realize sharp edges by stencil lithography a direct contact between mask and substrate and a cooling system of the chuck are required to reduce diffusion of the metal (halo). However, MIS-silicon nitride solar cells take advantage of the halo phenomenon to introduce a front surface field (see section 6.3.3). The stencil lithography offers a sophisticated, favorable and rapid technology to increase the overall yield of working Schottky-Mott diodes due to a resist-free method if clogging and blurring are taken into consideration.

**Figure 5.3:** The blurring in combination with a tilted mask-sample is illustrated.
5.2 Crystalline Silicon-Silicon Oxide Membranes

One principal process of fabricating crystalline silicon membranes consists of doping the silicon surface with P-type dopants (e.g. boron). However, the high doping concentration causes an additional crystal damage and Coulomb scattering of charge carriers. Moreover, this process is limited to P-type doping. A more sophisticated approach is based on silicon on insulator substrates. Here, the procedures relies on the buried oxide (BOX) beneath the top silicon layer (device layer). Appendix A gives an overview of a fabrication procedure for bipolar junction transistor based on an ultra-thin silicon nitride approach. Furthermore, this method offers fabrication scheme for silicon based Josephson junctions controlled by backside gate.

This process is equal to the one explained in the previous section (Fig. 5.5 a). Nevertheless, it turns out that the buried oxide is not an adequate etch stop for the potassium hydroxide at a temperature of 96 °C so that the device layer is easily etched if no etching control is present [206,207]. Therefore, the fabrication procedure is slightly changed to reduce the attack of the buried oxide to maintain the dielectric.

Considering a squared area of 1 mm² a membrane window of 110 µm is expected taking into account the SOI substrate thickness of 625 µm ± 25 µm. This information...
allows to control the etching depth without harming the buried oxide layer. A closer look at the remaining 10 $\mu$m of backside silicon reveals a rough frame near to the buried oxide confirmed by the SEM image in Fig. 5.5 b. Thus, once the frame occurs a “softer” potassium hydroxide recipe at 60 °C is chosen to reduce strongly the etching rate of the BOX (see appendix A). Several tests have shown that the BOX is more or less not attacked if the etching time is increased to ensure a complete removal of the silicon on the BOX surface. The etching depth is determined by either laser microscope or stylus profilometry. It is also apparent that particular faces appear (see Fig. 5.5 c). These are very well known from literature [208–210], which start to appear once the interface of the handle wafer-BOX is exposed. Keeping in mind that the SOI and silicon substrate is capped by a silicon nitride layer the silicon nitride is removed by phosphoric acid leaving behind a crystalline silicon-silicon oxide membrane of approximately 110 $\mu$m squared shapes (top view depicted in appendix A).

**Figure 5.5:** Backside etching of the handle wafer is demonstrated by illustration and images taken from the backside: a) schematic cross-section of the c-Si-BOX membrane is illustrated here, b) SEM image of <111> sidewall exhibits a huge roughness close to the buried oxide layer, c) microscope image of the backside of the handle wafer shows predefined silicon facets, once the surface of the buried oxide is reached.
5.3 Nanostencil - ultra thin Silicon Nitride Membranes

The fabrication procedure of the nanostencil masks is based on a process of the ultra-thin silicon nitride membrane, which is presented in this section. Owing to the small difference in the fabrication procedure and new applications enabled by the ultra-thin silicon nitride membrane both tools are introduced here. Silicon nitride membranes are widely accepted as a proper background material for SEM and TEM imaging due to the high signal to noise ratio and high density (see chapter 4). Ultra-thin silicon insulator membranes with thicknesses smaller than 2 nm fabricated by thermally driven process promise to open new applications if superconductors and insulators grown out of a crystalline layer are considered. All thermally grown silicon based insulators are restricted to superconductor-insulator-silicon approaches (asymmetrical Josephson junctions). Therefore, a membrane based technique overcomes most of the issues and challenges of the processing. Exposed and free-standing insulators can be deposited by superconducting material on both sides (symmetrical Josephson junctions). Silicon oxide and silicon nitride are high quality materials grown out of silicon. Silicon nitride outperforms the silicon oxide for small thicknesses and a smaller band gap because the higher band gap of silicon oxide would require even thinner membranes. On the other hand the fabrication procedure of

Figure 5.6: a) The ultra-thin silicon nitride membrane by nitridation of the SOI-backside is illustrated, b) SEM image of a 10 s 1%-HF TMAH etched 3 nm silicon nitride membrane shows the top view. One SEM carbon contamination dot is hold by the silicon nitride membrane, c) AFM scan of a membrane exhibiting a huge surface roughness in contrast to the very smooth $<111>$ sidewalls, AFM-imaging: AFM-tip caused a falling of the underetched top Si$_3$N$_4$ layer, which is observed in b) by the white frame above the TMAH groove.
5.3. Nanostencil - ultra thin Silicon Nitride Membranes

Ultra-thin silicon nitride membranes offer a sophisticated approach to manufacture nanostencil lithography masks, which exhibit promising results owing to the silicon edge smoothness. It is a major advantage in contrast to focused ion beam (FIB) or RIE based nanostencil masks. Therefore, the nanostencil masks are a perfect tool to test the impact of metal contaminants on the complementary metal area.

Starting from the last section with silicon-silicon oxide layers the BOX is removed by a buffered oxide etch. While the thinnest silicon nitride membranes have a thickness of 3 nm \[211\], a deposition of silicon nitride by LPCVD below this thickness becomes quite a challenge. Here, thermally grown nitrides are more promising owing to the closed and dense nature of the material in contrast to deposited nitrides.

After removing the BOX the silicon device layer is exposed to the environment on the front and back side. The silicon nitride membrane is formed by double side nitridation of the top-silicon layer as illustrated in Fig. 5.6a (Silicon nitrides grown at 850°C, 1000°C, 1100°C exhibit thicknesses of 1.7 nm, 2 nm and 2.4 nm) followed by an ebeam lithography to open the top silicon nitride with a RIE step.

The polymethyl methacrylate (PMMA) resist is removed and the backside is covered by an optical resist, to avoid an attacking by the 1%-HF prior to the TMAH etching of silicon. TMAH etching immediately after dry etching does not require an HF dipping or resist coating on the backside. The silicon nitride layer exhibit small TMAH-etching rates, even the thinnest nitrides grown at 450°C (thickness 0.6-0.8 nm) can withstand TMAH (60°C) etching of several micrometers of silicon (see section 4.7). Fig. 5.6b demonstrates a 3.3 nm thick silicon nitride membrane. To prove the existence of this membrane a carbon contamination dot is deposited by the ebeam induced current deposition during SEM-imaging. However, it is worth mentioning that the insulating property of nitride in combination with high electron beam currents during imaging leads to breaking of the membranes (appendix J).

It is quite remarkable that the presence of nitrogen could be verified by energy dispersive X-ray spectroscopy (EDX) due to a reduced silicon-nitrogen ratio inside the nano-groove depicted in Fig. 5.6. Despite the fact that the entire top silicon layer (size of 110x110 µm²) forms a free-standing membrane, nitrogen is not observed by EDX outside the groove. If the beam of the SEM is centered inside a membrane nitrogen is measurable by EDX owing to the reduced silicon volume (appendix C).

With this fabrication procedure silicon nitride membranes with thicknesses of 1.7 nm grown at 850°C were achieved (appendix J). Additionally, from the SEM image depicted in Fig. 5.6b a clear undercut is observed due to TMAH etching. Even the diagonal elements of the groove shimmer through the silicon nitride confirming the low background signal of ultra-thin silicon nitride layers. Outside the groove the surface exhibits a substantial roughness, which is related to the phosphoric etching of the residual thick LPCVD silicon nitride layer (see section 5.1). Atomic force microscope (AFM) confirms that the TMAH etched faces reveal an excellent smoothness in contrast to the surface (Fig. 5.6c, inset). The inset displays an AFM image of a broken piece of the undercut nitride layer on the TMAH etched silicon. The broken piece is relaxed exhibiting less surface roughness in contrast to the silicon nitride layer on top of the silicon surface which originates from the
removal of the LPCVD SiN by the hot phosphoric acid process step (section 5.2). In addition, even the membrane shows a rough surface. However, this is attributed to the SMART CUT™ technology associated with the bonding procedure [212]. The very low roughness of the silicon surface due to the TMAH/IPA etching is a major benefit of the here presented fabrication procedure for nanostencil masks. If the silicon nitride membrane is etched by HF, BOE and H₃PO₄ the silicon is not harmed at all leaving behind a perfectly shaped silicon frame for nanostencils.

First thick layers of vanadium are deposited as displayed in Fig. 5.7a. The nanostencil mask exhibits squared openings rising from 80 nm up to 300 nm, which is illustrated by the AFM image in Fig. 5.7b. The sample is in hard contact with the mask so that the feature size is in excellent accordance with the deposited pattern confirmed by the lateral resolution (inset Fig. 5.7b). Furthermore, the clogging is obviously taking place demonstrated by the conic dot shape owing to the small feature size with a vanadium thickness of 80 nm [213]. The rounding is attributed to either a deposition of vanadium on the nanostencil window or a small gap between mask and surface [214]. However, the blurring phenomenon is not observed owing to a small gap.

As already mentioned in the beginning vanadium is easily removed by etching without harming the silicon nanostencil mask or even the nitride membrane. The nanostencil mask is a perfect match to test the impact of contaminants by avoiding any contact related issues for Schottky-Mott-diodes based on ultra-thin silicon nitride layers. This study is presented in section 6.2.
5.4 Diodes

All ultra-thin nitride based applications require an excellent handling of the surface. Considering dopant related approaches, the crucial junction region is conventionally not close to the surface of the silicon dealing with much less surface related issues. Secondly, it is worth mentioning that a complete nitrided surface over the entire sample or even a 4-inch wafer (or larger) does not exhibit a definitely homogenous silicon nitride layer. Several runs of fabrication indicated that the contact area need to be reduced due to minor imperfections inside the silicon nitride layer (see section 6). It is in this context, that two simple technologies are demonstrated to lower risks of possible defects and contamination and to increase the yield: Vertical and planar Schottky-Mott diodes depicted in Fig. 5.8 a and b.

Figure 5.7: a) Laser Microscope image at 150x magnification shows the matrix of squared deposited vanadium spots on a Si substrate, area: \((80 \text{ nm})^2\) up to \((300 \text{ nm})^2\), on the right hand side an inverted part of the left image is given confirming the existence of the 80 nm sized vanadium spots, b) rounded vanadium spots with conic dot shape are observed via AFM scan, which exhibit 80 nm of diameter (right hand side).
Vertical diodes benefit from a completely metalized backside. This configuration is suitable for highly doped (below degenerate state) substrates because one junction governs completely the IV characteristics. Moreover, surface related issues have less impact on the backside due to a wide contact area and a low contact resistance, which leads to a single side Schottky-Mott junction concept. The top contacts are patterned by a metal lift-off procedure. However, this vertical configuration suffers from simultaneously handling of the front surface as well as the back surface. A planar diode configuration does not have this challenge by applying microstencil lithography (see section 5.1). The microstencil mask is brought in hard contact or a small gap of 100 \( \mu \)m is added between sample and shadow mask. After first metallization either the mask is moved or the mask-sample stack is tilted. These diodes can be monolithically connected into a series of P-N junction to increase the overall blocking voltage.

### 5.5 Ultra Thin-Silicon-Nitride-Solar Cells

#### 5.5.1 Standard Cell

The standard cell concept is based on a highly doped emitter with a depth of approximately 750 nm and a doping concentration of \( 8 \cdot 10^{18} \text{cm}^{-3} \). The doped region is produced by a phosphoryl chloride (POCl\(_3\)) process, where in Fig. 5.9 I the doped N-type region is depicted. The silicon surface is nitrided at 450°C (see Fig. 5.9 II.) and aluminum (gold) is evaporated on the front (rear) surface (see Fig. 5.9 III. and IV.). Reference solar cells are not nitrided so that the Schottky barrier formed between aluminum and low P-type doped substrate provides a simple approach to achieve a P-type contact on the backside. A detailed overview of the process steps and parameters is listed in the appendix E.
5.5. Ultra Thin-Silicon-Nitride-Solar Cells

Figure 5.9: A Solar cell with a POCl$_3$ FSF and a silicon nitride process is illustrated: I. POCl$_3$ process, II. standard Clean and RTN at 450°C, III. Al-lift-off on the front side and IV. backside Au metallization, reference samples have an aluminum backside metallization taking advantage of the Schottky-Barrier and its electrical field for the P-type contact.

5.5.2 Metal-Insulator-Solar Cells

MIS-solar cells are fabricated without any additional dopant processes. The carrier life time measurements (see section 4.4) indicated that only HF-dipped wafer without any RCA cleaning procedure prior to the mounting exhibit higher carrier life times. Hence, 4-inch wafers directly out of the box with P-type doping (5-10Ω·cm) are dipped and introduced into the RTP and heated up to 450°C. After capping the wafers by a protective resist samples are cut by a diamond scribe into squared 4 cm$^2$ to avoid saw damages. Next, the front surface of silicon is patterned by an aluminum-lift-off for busbar and lines. Before the lift-off is started the rear side is deposited with gold. Here especially, a careful handling of the surface of the sample is highly relevant. To prevent resist related issues two shadow masks for both metallizations are applied, which lowers the risk of damage of the ultra-thin silicon nitride layer. An overview of the process is given in Fig. 5.10. The process steps are described in detail in appendix E.
5. Device Fabrication

Figure 5.10: MIS-solar cell fabrication process is depicted: I. Standard clean and RTN, II. Al-lift-off on the front side and III. Backside Au metallization.

5.6 MOSFETs

Taking advantage of silicon on insulator (SOI) technology rudimentary PSEUDO-MOSFETs are fabricated, where the buried oxide (BOX) serves as a back gate oxide for first principle investigations (see Fig. 5.11). The top silicon layer is called device layer owing to the fact that the top layer will be the active part of the device. SOI material offers an elegant approach to bypass isolation step of electrical components either by a local oxidation or a shallow trench isolation process [215]. Hence, PSEUDO-MOSFETs provide a quick and straightforward characterization of the active silicon layer with respect to ohmic-, Schottky contact formation, ambipolar, unipolar behavior, electron and hole mobility and sub threshold voltage swing.

In Fig. 5.12 the process for N-type and P-type MOSFETs is illustrated. While for N-type devices the mesa etching is done by RIE (SF₆/O₂) prior to metallization, P-type devices receive immediately a metallization layer after RTN (450-850°C) owing to the insufficient adhesion between high work function metals on silicon nitrides. The low adhesion after metallization lift-off leads to a very low yield of devices.

Figure 5.11: SEM cross section image of SOI-BOX-handle wafer stack sketches a PSEUDO-MOSFET with N-type doped contact regions and aluminum pads.
5.6. MOSFETs

Figure 5.12: Process flows of N-type (top process flowchart, a)) and P-type (bottom process flowchart, b)) MOSFETs are illustrated: a) I. Mesa-lithography, II. Mesa-RIE etching and resist removal, III. Standard cleaning and RTN, IV. Metal lithography, V. Lift-off of Al or V, VI. Backside metallization Al or Ti/Au, b) standard cleaning and RTN, II. Metal lithography, III. Pt or Ni Lift-off, IV. Mesa-lithography, V. Mesa-RIE etching and resist removal, VI. Backside metallization Al or Ti/Au.
It turns out that the adhesion is strongly negatively impacted by previous process steps. Aggravated by a thick metal layer (>50 nm) the adhesion becomes even more complicated. The evaporation of thin metals avoids most of the issues, although the characterization requires a more careful handling to avoid damaging the metal layer and the silicon nitride layer by bringing the contact needle in contact with the silicon nitride. Nevertheless, high yields of up to 100 percentage are achieved if the mesa etching is shifted to the end of the processing, which leads to a RTN directly at the beginning of the process order in contrast to N-type MOSFETs (see Fig. 5.12 a), I. and b), IV). It is worth mentioning that the evaporation procedure can increase further the adherence [216].

![Figure 5.13: PSEUDO-MOSFETs are captured by the Laser-Microscope scanning from the top view: a) lateral design of PSEUDO-N-type MOSFETs, b) circularly shaped PSEUDO-P-type MOSFETs.](image)

The design of the N-type MOSFET is depicted in Fig. 5.13 a. The length of the mesa is set to 200 µm. The width is changed from 20 µm up to 50 µm. Source and drain regions are separated by 140 µm distance and a contact length of 30 µm. For P-type MOSFETs circularly shaped source and drain regions are more suitable to increase the adhesion. Short Ultra sonic cleaning steps do not cause a lift-off of the high work function metals. A top-view image of the P-type MOSFETs is depicted in Fig. 5.13 b and Tab. 5.1 gives an overview of the geometry dimensions. The width is determined by [217]:

\[ W = \frac{2\pi L}{\ln\left(\frac{d_o}{d_i}\right)} \]

(5.3)

where \( L \), \( d_o \) and \( d_i \) are the outer and inner diameter. The unequal contact areas of source and drain have to be taken into consideration, if the devices are characterized. The complete process for both MOSFETs is listed in the appendix F.
<table>
<thead>
<tr>
<th>device No.</th>
<th>( d_i ) [µm]</th>
<th>( d_o ) [µm]</th>
<th>L [µm]</th>
<th>W [µm]</th>
<th>ratio of areas ( \frac{A_o}{A_i} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st</td>
<td>600</td>
<td>6692</td>
<td>3046</td>
<td>18263</td>
<td>10.90</td>
</tr>
<tr>
<td>2nd</td>
<td>600</td>
<td>2550</td>
<td>975</td>
<td>9744</td>
<td>4</td>
</tr>
<tr>
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<td>1690</td>
<td>545</td>
<td>7610</td>
<td>2.57</td>
</tr>
<tr>
<td>4th</td>
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<td>5791</td>
<td>2105.5</td>
<td>23440</td>
<td>1.36</td>
</tr>
<tr>
<td>5th</td>
<td>1580</td>
<td>3590</td>
<td>1005</td>
<td>17707</td>
<td>0.83</td>
</tr>
<tr>
<td>6th</td>
<td>400</td>
<td>3590</td>
<td>1595</td>
<td>10510</td>
<td>12.90</td>
</tr>
<tr>
<td>7th</td>
<td>574</td>
<td>1940</td>
<td>683</td>
<td>8110</td>
<td>3.26</td>
</tr>
<tr>
<td>8th</td>
<td>390</td>
<td>1940</td>
<td>775</td>
<td>6985</td>
<td>7.06</td>
</tr>
<tr>
<td>9th</td>
<td>200</td>
<td>1940</td>
<td>870</td>
<td>5537</td>
<td>26.85</td>
</tr>
</tbody>
</table>

Table 5.1: Feature sizes of the various circular P-type PSEUDO-MOSFETs are listed, inner diameter \( d_i \), outer diameter \( d_o \), channel length L, width W, outer contact area \( A_o \) and inner contact area \( A_i \), the annulus has a width of 150 µm.
5. Device Fabrication

5.7 Resonant Tunneling Diode

Resonant tunneling diodes based on silicon nitride insulators are fabricated by PECVD and RTP processes for the first time [90,218–222]. The approach pursued in this thesis takes advantage of the closed and uniform thermally grown layers. Silicon nitride is grown at 1050°C on top of CZ silicon substrate, which yields a thickness of 2.4 nm determined by ellipsometry. As a next step amorphous silicon of 7 nm is deposited by inductively coupled plasma (ICP)-PECVD and the sample is immediately mounted into the RTN chamber to prevent a native oxidation of the silicon amorphous silicon layer. The RTN process consists of two steps: A heating step in inert atmosphere and the nitridation at 1050°C, which causes several effects: Outgasing of hydrogen, thinning of a-Si, densification and nucleation of a-Si. The first aspect is verified by FTIR measurements in Fig. 5.14. The infrared spectrum reveals only the asymmetric Si-N stretching mode at approximately 850 cm⁻¹, no hydrogen related bond is detected by FTIR.

![FTIR spectrum of Si₃N₄|nanocrystalline-Si \ Si₃N₄ stack on a low doped substrate (5-10 Ωcm) nitrided at 1050°C is shown.](image)

The nucleation of amorphous silicon is proven by Raman analysis. A reference sample is fabricated by sealing the amorphous silicon with a nitride layer grown at 850°C to prevent a nucleation formation. On one half of the sample the stack of Si₃N₄\a-Si\Si₃N₄ is completely etched by a SF₆\O₂ RIE process providing a clean background signal of the silicon substrate. For the sample nitrided at 1050°C the
5.7. Resonant Tunneling Diode

same procedure is applied. Fig. 5.15 a and b depicts the Raman spectra of the samples nitrided at 850 °C and 1050 °C. In logarithmic scale the signal of the RTD stack (see Fig. 5.15 a, red curve) at approximately 470 cm$^{-1}$ exhibits a much higher intensity than from the silicon surface in the range of the characteristic amorphous silicon modes [223]. In this regime the response of the amorphous layer governs almost the overall spectra, which is not observed if an annealing temperature at 1050 °C is chosen indicating a phase transition of the amorphous layer. The intensity difference between the silicon surface and stack Raman spectra are displayed in Fig. 5.15 c and d. In the case of 850 °C the longitudinal acoustic (LA) mode at 301 cm$^{-1}$ and the longitudinal optical (LO) mode at 380 cm$^{-1}$ are barely observed. A more intense peak appears at approximately 470 cm$^{-1}$.

![Raman spectra](image)

Figure 5.15: Raman spectra of a crystalline and an amorphous stack are demonstrated: a) 5 nm amorphous silicon layer is nitrided at 850 °C to avoid nucleation, b) initial 7 nm amorphous silicon layer is nitrided at 1050 °C for nucleation and capping, c) difference of spectra shown in a) are demonstrated in the particular surrounding of the amorphous silicon peak at 480 cm$^{-1}$, d) difference of spectra depicted in b) at 1050 °C.

Mercaldo et al. attributed these peaks to a double mode consisting of a Si-N mode at 465 cm$^{-1}$ and the transverse optical (TO) mode of amorphous silicon located at 480 cm$^{-1}$ [224]. However, Park et al. examined a shift of the TO mode associated to the compressive strain of their PECVD-SiN$_x$ [225]. Unfortunately, the crystalline
phonon band at 520 cm\(^{-1}\) overlaps the amorphous silicon band and the silicon nitride mode, which is displayed in Fig. 5.15c by the increased rise of the intensity close to 500 cm\(^{-1}\) owing to the higher c-Si peak of the crystalline silicon surface. Nevertheless, in the case of the 1050°C sample also both modes at 465 cm\(^{-1}\) and 480 cm\(^{-1}\) are observed in Fig. 5.15d, even a rise starting at a wave number of approximately 486 cm\(^{-1}\) appears, which is attributed to the nanocrystalline nature of the initial amorphous silicon layer [226]. However, the crystalline peak of the silicon substrate overlaps the complete characteristic regime allowing only qualitatively interpretation. Taking advantage of the ultra-thin silicon nitride membranes introduced in section 5.3 a deposition of the amorphous silicon layer on the membranes and a second nitridation of the amorphous silicon offers an excellent free-standing resonant tunneling diode concept.

![Figure 5.16: Angle shadow evaporation technique is illustrated, 1st metal layer causes a gap by shadowing which depends on the thickness of the first layer and the angle between evaporation source and sample on top of the resonant tunneling barrier stack.](image)

The first silicon nitride based RTD was fabricated on low doped silicon substrates (P-type, 5-10\(\Omega\)cm, CZ). The lowly doped samples "as will become clearer in section 6.4 exhibit resonant tunneling phenomena". Due to the high series resistance and lowly doped substrate owing to dopant freeze out it is mandatory to lower the distance between front and rear terminals [227–229]. The shadow evaporation technique is a simple approach to realize sub 100nm spacings between metal layers based on microstructuring technology. The patterning of the metal contacts is splitted into a two step lithography process. After the first lift-off (1st metal layer) the second
lithography takes advantage of an overlap between the 1st metal layer and the open areas of the second resist prior to metal deposition. The first metal layer shadows the vapor flow causing a sub micrometer gap, if the sample is tilted relative to the evaporation source (see Fig. 5.17). As a first approximation the gap \( l \) depends on the tilt \( \alpha \) and the thickness of the first metal \( h \):

\[
l = \frac{h}{\tan(\alpha)}.
\]  

(5.4)

However, the relation is affected by the substrate temperature during evaporation and the growth of the metal layer.

**Figure 5.17:** SEM-image of an aluminum spacing with a tilt angle \( \alpha=45^\circ \) and \( h=100 \text{ nm} \) of aluminum is depicted; inset exhibits 200 nm (2 \( \cdot h \)) thick aluminum layers leading to bigger distance \( l \).

After the metallization of the first contact pads, the mask is tilted by 45° and the samples are evaporated in order to ensure a small spacing of 70 nm (Fig. 5.17). The inset of Fig. 5.17 depicts a bigger spacing of approximately 160 nm if the thickness of the aluminum layer is increased to 200 nm. In principle, even spacings of 30 nm are easily fabricated by this method, if the thickness of the aluminum is further reduced despite the fact of a microstructure lithography process 6.2.
Chapter 6

Device Characterization

6.1 Dopant-Free MOSFET

6.1.1 N-Type MOSFET

Aluminum Schottky barrier MOSFETs exhibit ambipolar behavior (Fig. 6.1a) if the MOSFETs are fabricated from low doped silicon substrates. For positive gate voltages the transport is governed by the source Schottky barrier, while for negative gate voltages the hole transport is controlled by the SB of the channel drain junction. The output characteristic of a SB-MOSFET is depicted in Fig. 6.1b exhibiting first an unexpected linear regime. However, the first derivative of the output characteristic proves a linear slope associated to a superlinear for small voltages (Fig. 6.1c).

Incorporating an ultra-thin silicon nitride layer between metal and silicon causes a Fermi level depinning, which is demonstrated by the p-branch suppression of 6 decades (Fig. 6.1d). Hence, the ultra-thin silicon nitride layer causes an N-type unipolar behavior. Connelly and Ghoneim et al. have successfully demonstrated that silicon nitride increases the conductance for various metals such as Yb, Er, Mg, and Al [24, 26]. These metals offer work functions $W_f$ (2.7 eV, 3.2 eV, 3.7 eV and 4.3 eV) close or even much smaller than silicon electron affinity $\chi$ 4.05 eV [35, 230] and are promising materials to inject into the conduction band of silicon, if the metal is depinned of the charge neutrality level. However, the results depicted in Fig. 6.1d do not exhibit an increase of the on-current. The absent performance boost is attributed to the incorporated hydrogen during the growth of the nitride at lower annealing temperatures (<600 °C) and the requirement of a high quality clean fabrication procedure which is addressed in section 6.2. First of all, Connelly and Ghoneim et al. took advantage of a plasma assisted nitridation, which leads to much smaller hydrogen proportion due to an intense decomposition state of the ammonia-nitrogen mixture. But exclusively the Ghoneim group demonstrated additionally unipolar behavior of aluminum based N-type MOSFETs. Connelly et al. considered that the overlap of its field oxide caused a dramatic recombination current. However, the band bending due to the metal at the silicon surface was underestimated. The current flow between two similar low work function metals on medium P-type doped substrates causes a rectifying nature owing to the
6. Device Characterization

Figure 6.1: IV characteristics of N-type MOSFETs with a channel length of 395 µm are depicted: a) Transfer characteristic of a Al-SB MOSFET exhibiting ambipolar behavior (width 50 µm), b) output characteristic of a Al-SB-MOSFET, c) first derivative of the output characteristic demonstrating rise of the drain current for small voltages, d) transfer characteristic of an ultra-thin silicon nitride MOSFET grown at 450 °C (0.7 nm) incorporated between silicon and aluminum demonstrating on-off ratio of 6 decades, e) comparison of transfer characteristics for silicon nitrides grown at various temperatures 600 °C (1 nm), 800 °C (1.7 nm), 1000 °C (2.4 nm) and 1200 °C (3 nm), f) output characteristic of a nitride layer annealed at 450 °C (0.7 nm) showing a clear linear regime and saturation of the drain current (width 20 µm).
present Schottky-Mott junction. Moreover, the ultra-thin thickness of silicon nitride could cause a metal-like contact formation, which would again lead to an ambipolar behavior (see section 2.1). A larger hydrogen portion deteriorates the insulating properties of the silicon nitride layers, as it was demonstrated by Parsons and Brown et al. [164,165]. Nitrides which were grown at higher temperatures, can be applied as dielectric materials revealing excellent insulating properties as demonstrated in section 4.5 [145,231]. Thicker nitrides lead to a very large tunneling resistance and reduce the current (Fig. 6.1 e). The current of the pFET branch starts to increase owing to the smaller impact of the metal on the silicon surface, which leads to a smaller SB for holes (see section 2.2.3). Furthermore, the threshold voltage is shifted to negative voltages associated to a generation of oxygen-vacancy-related defects in the SOI-BOX interface [232]. The thickest nitride grown at 1200°C exhibits an almost completely flat line of the transfer characteristic in this voltage range due to a huge shift of the threshold voltage close to -44 V exhibiting an increased impact on the buried oxide owing to the high annealing temperature (see inset of Fig. 6.1 e) [233]. The output characteristic of an ultra-thin layer (450°C) demonstrates clear ohmic and saturation regimes depicted in Fig. 6.1 f.

The tunneling through thicker silicon nitride layers is observed by an exponential rise of the current in the output characteristics associated to the tunneling phenomenon through an insulator, which is depicted in Fig. 6.2 a, b and c for 550°C, 700°C and 800°C. However, lowering the nitridation temperature leads to a reduction of the contact resistance confirmed by the rise of current (Fig. 6.2 a, b and c). Vanadium has a higher work function of approximately 4.1-4.65 eV [234,235]. The vanadium SB MOSFET exhibits a reduced PFET branch (see Fig. 6.2 d), which is attributed to the higher $\phi_{SB}^h$ for holes in relation to electrons $\phi_{SB}^e$ of 0.55 eV for P-type Si substrate [236]. In contrast to the aluminium silicon nitride-MOSFETs a nitridation at 450°C leads to a small increase of the NFET branch (Fig. 6.2 e) proving the benefit of the tunneling insulator between metal and silicon. However, the blocking of the ambipolar behavior is very weak, which causes an on-off ratio of less than 4 orders of magnitude. Taking a closer look at the inverse subthreshold voltage vanadium based MOSFETs outperform aluminium based MOSFETs (compare Fig. 6.1 d and 6.2 e). For vanadium the subthreshold swing is in the range of 140-160 mV/dec in contrast to aluminium with 300-400 mV/dec. Furthermore, it is expected to obtain much smaller $S$, if a top gate approach is considered owing to the rather non-ideal buried oxide, which is confirmed by CV measurements depicted in the inset of Fig. 6.2 e. The high frequency part of the CV-measurement reveals a less steep slope close to the threshold voltage attributed to an increased interface density. For positive voltages a rise of the capacitance is apparent. Moreover, the drain current is clearly separated into a linear and saturation regime (Fig. 6.2 f). The hump in the output characteristic is attributed to a local early breakdown and turn-on behavior of the device, which appears in the range of the transfer characteristic from -8 V to -2 V [237].
Figure 6.2: Output characteristics of silicon nitride N-type MOSFETs (width 50 µm) are depicted grown at a) 550 °C (0.8 nm), b) 700 °C (1.2 nm), and c) 800 °C (1.7 nm); Contact width 50 µm, d) Schottky Barrier MOSFET transfer characteristic of vanadium contacts, e) vanadium-silicon nitride-MOSFET transfer characteristic, f) output characteristic of vanadium-silicon nitride-MOSFET.
Shadow Mask Evaporated MOSFETs

The conventional MOSFET metallization process is based on a lift-off procedure. However, from the results of the SM-diodes and solar cells (see following sections) it is confirmed that the metallization via lift-off impairs the ohmic tunneling junction. A possible solution is therefore a microstencil lithography process in order to ensure a high quality and pure metal-silicon nitride-contact which is confirmed by the fact that the aluminum nitride based N-type MOSFETs exhibit to some extent a large inverse subthreshold slope. Hence, after nitridation a direct evaporation of aluminum through a shadow mask is performed. After metallization the mesa is etched into the SOI layer. The transfer characteristic of the MOSFET fabricated with shadow mask exhibits unipolar N-type behavior as depicted in Fig. 6.3a. Studying the subthreshold swing a smooth shape of $S$ is apparent in contrast to the Al-silicon nitride-MOSFET fabricated by lift-off (compare Fig. 6.1 b and 6.3 c). The latter

![Graphs showing IV characteristics of silicon nitride N-type MOSFETs](image)

**Figure 6.3**: IV characteristics of silicon nitride N-type MOSFETs grown at 450°C are depicted with a microstencil based metallization process: a) Unipolar transfer characteristic of a shadow evaporated aluminum-silicon nitride-MOSFET, channel length 950 μm and width 50 μm, b) inverse subthreshold swing versus gate voltage, exhibiting a rather smooth transition from on-off switching, minimum inverse subthreshold voltage 358 mV/dec, c) inverse subthreshold swing of the MOSFET from Fig. 6.1 fabricated by a lift-off process, minimum inverse subthreshold voltage 380 mV/dec, d) output characteristic of the shadow-mask evaporated aluminum-silicon nitride-MOSFET.
Figure 6.4: Two types of metallization procedures are illustrated: a) lift-off metallization, b) after microstencil metallization mesa etching.

process exhibits a noisy signal, which could be improved by rising the integration time. In addition, the slope is reduced from 380 mV to 358 mV (compare 6.3 band c). Keep in mind that the lift-off fabrication technique covers the mesa on all three silicon sides (see Fig. 6.4a), which should give much smaller $S$. The deposited metal via shadow mask is only in contact with the front surface of silicon leading to a less efficient gate control (see Fig. 6.4b). A shadow evaporation of aluminum after mesa etching and nitridation is expected to decrease the inverse subthreshold swing. Schottky-Mott diodes fabricated in the next section confirmed that a lift-off process lowers the electric field at the metal-nitride-silicon junction. Furthermore, section 6.2.4 demonstrates the large impact of a small contaminated area on the specific resistance indicating a silicon surface related issue. All these experiments point to the depletion region of the Schottky-Mott contact but an explicit identification of this cause is not presented in this thesis. An analysis of the lift-off steps is necessary to clarify the circumstance of any residual materials or contaminants causing a rise of the contact resistance. Here, a contact resistivity study by transmission line method is an appropriate approach to analyze in detail the junction resistance [238].

The results of the vanadium based nitride MOSFET indicate that a clean and pure metal evaporation fabrication process is crucial for a low subthreshold swing. For instance, the grain size of the evaporated material determines the specific resistance [239]. SEM images of in-house evaporated aluminum and vanadium and externally deposited aluminum layer show different grain sizes. While vanadium exhibits an excellent smoothness and no small grain formation (see Fig. 6.5a), the aluminum layers have much smaller grain sizes (see Fig. 6.5 b and c). Especially the in-house evaporated aluminum has even smaller fragments, which is confirmed by the huge surface roughness. This might be an indication for various work functions and a detailed study of the evaporated metal should take this into account.
Figure 6.5: Cross-section SEM images are depicted of a) 100 nm evaporated vanadium, b) approximately 145 nm of in-house evaporated aluminum, c) 165 nm externally evaporated aluminum.
6. Device Characterization

6.1.2 P-Type MOSFET

Nickel with a work function of 5.15 eV is initially selected as a suitable candidate to ensure P-type contacts [35]. SB MOSFETs with Nickel are shown in Fig. 6.6a demonstrating ambipolar behavior. However, similar to the SB MOSFETs with vanadium and aluminum contacts the output characteristic exhibits a clear linear regime at the first glance owing to the large contact areas (Fig. 6.6b). A closer look at the first derivative of the drain currents \(I_{ds}\) reveals a rise of the slope for small voltages too, which verifies the presence of a non linear contact formation (Fig. 6.6c). In contrast to aluminum, nickel displays a small current increase with an incorporated silicon nitride layer (Fig. 6.6d), although, the N-type branch of the drain current is merely reduced by a factor of 10. Increasing the temperature up to 800 °C results more or less the same on current, even a small rise is apparent indicating an insufficient blocking of MIGS at low temperatures (Fig. 6.6e). Moreover, the inverse subthreshold slope deteriorates with an embedded ultra-thin silicon nitride layer as obviously demonstrated in Fig. 6.6f. The NFET branch is reduced by approximately 2.5 decades and an ohmic behavior is observed in contrast to the reference Ni-Si samples (Fig. 6.6f). While the output characteristic of the silicon nitride grown at 450 °C exhibits clearly an ohmic behavior, the MOSFET nitrided at 800 °C shows a linear regime as well (see Fig. 6.7a and b). The derivatives of the output characteristics do not show a super linear rise, even in the case of the thicker nitride, where an exponential increase is expected owing to the tunneling through a thicker insulator (Fig. 6.7c and d).

In contrast to nickel, platinum is a noble metal and has a much higher work function of 5.65 eV complementary to magnesium and erbium for electron transport [35]. The transfer characteristic of a platinum SB MOSFET reference sample is presented in Fig. 6.8a. If a nitride layer grown at 450 °C is incorporated, the NFET branch is more than two decades suppressed (Fig. 6.8b) and enables an on-off ratio of more than 6 decades. Since these devices are circular Pseudo-MOSFETs this on-off ratio is even higher owing to the asymmetrical contact areas (see section 5.6). The contact area of the outer ring is approximately 7 times larger. In comparison to the reference sample a small improvement of the subthreshold swing of 10 mV is determined attributed to the ohmic contacts, which leads to an inverse subthreshold slope of 330 mV.

A substantial improvement of the on-off switching performance is expected if a top gate approach is considered, where the source and drain regions overlap with the gate oxide as it was demonstrated already in the case of vanadium based MOSFETs in section 6.1.1, where the silicon is covered by vanadium on all three sides leading to a direct gate control of the vanadium-silicon nitride-silicon interface.
Figure 6.6: Nickel-SB MOSFET characteristics of a device with \( r_i = 790 \, \mu m \) and \( r_o = 1645 \, \mu m \) feature sizes are demonstrated: Channel length 1005 \( \mu m \) a) Ambipolar transfer characteristic with nickel contacts, b) output characteristic with nickel contacts, c) first derivative of the output characteristic confirming the superlinear Schottky rise in the linear regime; Nickel-silicon nitride-MOSFET \( (r_i = 790 \, \mu m \) and \( r_o = 1645 \, \mu m) \) transfer characteristics of various nitridation temperatures: d) 450\(^\circ\)C, e) 800\(^\circ\)C, f) comparison of transfer behavior for various annealing temperatures and the SB reference sample.
6. Device Characterization

![Graphs](image)

**Figure 6.7:** Nickel-silicon nitride-MOSFET output characteristics and the first derivative \((r_1=790 \, \mu m \text{ and } r_0 = 1645 \, \mu m)\) are depicted: a) grown at 450°C, b) grown at 800°C, c) first derivative of the 450°C output characteristic, d) first derivative of the 800°C output characteristic.

It is very well known in literature that the thickness of the device layer and the gate oxide have a crucial impact on the subthreshold voltage confirmed by \([35,240]\):

\[
S = \ln(10) \frac{kT}{q} (1 + \frac{C_{\text{depl}}}{C_{\text{ox}}}),
\]

where \(C_{\text{depl}}\) and \(C_{\text{ox}}\) are the depletion and oxide capacitances, respectively. This relation holds true as long as the \(C_{\text{depl}}\) is the dominating part in the top of the barrier model. The oxide capacitance is a geometry and material dependent quantity, whereas the depletion capacitance depends on the applied voltage and the width of the depletion layer owing to the not completely depleted SOI layer. Hence, a better performance is expected for SOI thicknesses below 100 nm. In addition, a current enhancement is not observed, which is again associated to the hydrogen content inside the silicon nitride layer.

In principle, platinum based nitride FETs exhibit an equal thickness relation as it was demonstrated for aluminum before (Fig. 6.1 d and Fig. 6.9 a). An increasing thickness reduces the injection of carriers from the metal on the surface of silicon \([59]\), which yields to a smaller Schottky-Mott barrier at the surface of silicon.

Contrary to nickel MOSFETs, platinum based devices show much smaller source drain resistances \(R_{DS}\) (Fig. 6.6 vs. Fig. 6.8 b). The output characteristics of the
Figure 6.8: Transfer characteristics of P-type MOSFETs with platinum contacts: a) Transfer characteristic of an ambipolar platinum-SB-MOSFET, $r_i=287\,\mu m$ and $r_o=820\,\mu m$, b) transfer characteristic of platinum-silicon nitride $450^\circ C$, $r_i=287\,\mu m$ and $r_o=820\,\mu m$.

The presented platinum $Si_3N_4$ MOSFET is depicted in Fig. 6.9 b. A second MOSFET with a slightly longer channel length confirms the channel dependence (Fig. 6.9 c). Each of them demonstrates clearly a linear and a saturation regime. The first derivative of the device from Fig. 6.9 a underlines the ohmic contacts established by an ultra-thin tunneling insulator (Fig. 6.9 d).

An appropriate contact resistance study of Schottky-Mott contact requires a perfect matching between the work function of metal and silicon substrate doping. Assuming high work function metals and a N-type silicon substrate are applied, a diode behavior is obtained due to the formation of a Schottky-Mott-junction, which is experimentally demonstrated in section 6.2.4. However, a low P-type silicon substrate (5-10 $\Omega$cm) exhibits a Fermi energy close to the valence band ($\Delta E_v \approx 240\,mV$) forming a Schottky-Mott junction at the metal-silicon nitride-silicon contact. An applied bias lowers the potential barrier but hampers the determination of the contact resistance. Replacing the metal by a lower work function material does not solve the issue at all, while an appropriate metal with no Schottky-Mott junction offers a promising analysis of the tunnel contact. However, this approach requires a fine tuning between doping concentration and metal work function. On the other hand, if the doping concentration is increased, the Fermi level is shifted closer to the high work function metal. The Schottky-Mott potential barrier is further decreased. Nonetheless, only metals with a work function close or higher are suitable for this method. It is obvious that the doping concentration reduces the amount of suitable metals for a contact resistance study. In this context, the characterization of Schottky-Mott diodes in the next section contribute to a better understanding of the relation between silicon substrate doping concentration and the work function of the metal.
Figure 6.9: IV characteristics of P-type MOSFETs with platinum contacts are depicted: a) Transfer characteristic for different nitridation temperatures, b) output characteristics of platinum-silicon nitride-MOSFETs, $R_{DS} = 4.7 \, \text{kΩ}$, $r_i = 287 \, \mu\text{m}$ and $r_o = 820 \, \mu\text{m}$, c) output characteristic of a MOSFET with $R_{DS} = 5.2 \, \text{kΩ}$, $R_i = 195 \, \mu\text{m}$ and $r_o = 820 \, \mu\text{m}$, d) first derivative of the drain current output characteristic of device from a).
6.2 Rectifying Nature of Schottky-Mott Junctions

6.2.1 Schottky-Mott Diodes

In the preceding section the unipolar behavior of low work function and high work function metal is demonstrated. Building a device out of low and high work function metal on a nitrided silicon substrate a rectifying behavior is expected. If not stated otherwise the silicon nitride is grown at 450°C. Fig. 6.10 shows the metal Schottky-Mott diode setup, which is basis of the results demonstrated in this section. For the P-type contact the high work function metal platinum is applied, while for the N-type energy selective contact aluminum is chosen. Both metals are deposited in a two step lift-off procedure. The platinum evaporation is done first to ensure an excellent adhesion. On four individual samples (two separate lots), each of them has 20 diodes, most of the diodes revealed a diode characteristic with a very high reverse currents and very small forward voltages, which is shown in Fig. 6.11 a. Only one device revealed a promising rectifying nature, which is presented in Fig. 6.11 b. However, the high forward voltage originates from a large series resistance, which is demonstrated in logarithmic scale by the square root rise of the forward current depicted in the inset of Fig. 6.11 b [35]. Moreover, an increasingly high reverse current is observed. Gold-aluminum diodes manufactured by lift-off exhibit much more promising results as confirmed by two diodes demonstrated in Fig. 6.12 a. Although a very small forward voltage of approximately 450 mV is obtained, the reverse current does not rise as in the case of platinum diodes. Furthermore, no large impact of the series resistance is apparent confirmed by the almost linear rise of the forward current once the forward voltage is exceeded.

Figure 6.10: Schottky-Mott diodes for various metal configurations in this section are illustrated; N-type contact is grounded, while the P-type contact has a negative (positive) potential for the reverse (forward) mode of the diode.
6. Device Characterization

The series resistance starts to impact the forward current observed by the reduced slope at voltages smaller than -1V. The small forward voltage is also present for nickel (see Fig. 6.12 b) and cobalt (see Fig. 6.13 a) P-type contacts indicating a rather aluminum related small forward voltage issue. Considering the low boron doping concentration \( \sim 10^{15} \text{ cm}^{-3} \), which corresponds to a Fermi level of 240 mV close to the valence band so that the dominant Schottky-Mott junction is located at the N-type contact interface. Assuming Boltzmann statistic and extrinsic region at 300 K: the Fermi level is determined by the \( E_V - E_F = kT \ln \left( \frac{N_V}{p} \right) \) relation, where \( N_V \) and \( p \) are the effective density of states in the valence band and the hole density \([35]\). As a second step, planar diodes are fabricated by microstencil lithography where smaller contact areas for both junctions are realized. Furthermore, a planar diode

\[ a \]

**Figure 6.11:** IV characteristics of vertical diodes (see section 5.4) with platinum and aluminum contacts are depicted: a) Pt-Al-Si\(_3\)N\(_4\) Schottky-Mott diodes fabricated by a lift-off process, width 75 \( \mu \text{m} \), length 1000 \( \mu \text{m} \), gap 200 \( \mu \text{m} \), b) best performance of the Pt-Al-silicon nitride Schottky-Mott diodes, same feature sizes as in a).

\[ b \]

**Figure 6.12:** IV characteristics of vertical diodes (see section 5.4) with gold, nickel and aluminum contacts are depicted: a) Au-Al-Si\(_3\)N\(_4\) Schottky-Mott diodes fabricated by a lift-off process, squared 200 \( \mu \text{m} \) sized contact pads, gap 200 \( \mu \text{m} \), b) Ni-Al-Si\(_3\)N\(_4\) Schottky-Mott diodes fabricated by a lift-off process, squared 200 \( \mu \text{m} \) sized contact pad, gap 525 \( \mu \text{m} \).
6.2. Rectifying Nature of Schottky-Mott Junctions

Figure 6.13: IV characteristics of **vertical diodes** (see section 5.4) with cobalt, nickel and aluminum contacts are depicted: a) Co-Al-Si$_3$N$_4$ Schottky-Mott diodes fabricated by a lift-off process, squared 200 µm sized contact pad, gap 525 µm, b) Ag-Al-Si$_3$N$_4$ Schottky-Mott diodes fabricated by a lift-off process, squared 200 µm sized contact pad, gap 525 µm.

process takes advantage of only one nitrided surface of the substrate shared by both SM-junctions. Consequently, similar to the shadow evaporated MOSFETs the key to ensure N-type contacts is a sophisticated aluminum evaporation process. For instance, applying the aluminum Al$_{\text{ext}}$ evaporation of the Juelich Forschungszentrum much higher forward voltages are achieved. Ag-Al$_{\text{ext}}$ based diodes exhibit a forward voltage of approximately 0.75 V depicted in Fig. 6.13 b. For the sake of completeness, the reverse current is in the order of 100 nA attributed to the large background contact area (vertical diodes). Since the N-type contact governs almost the rectifying nature low work function metals require the smaller contact area (here, top metal layer of the vertical diode concept, section 5.4) if P-type doped substrates are selected.

Figure 6.14: IV characteristics of **planar diodes** (see section 5.4) with gold, aluminum and magnesium contacts are depicted: a) Au-Al-Si$_3$N$_4$ Schottky-Mott diodes fabricated by shadow evaporation (mask shifted not tilted), squared 110 µm sized contact pad, gap 300 µm, b) Au-Mg-Si$_3$N$_4$ Schottky-Mott diodes fabricated by shadow evaporation, squared 110 µm sized contact pad, gap 300 µm.
6. Device Characterization

Contrary to vertical diodes, planar diodes consisting of gold and aluminum exhibit a forward voltage of approximately 1 V (see Fig. 6.14a). The current starts to saturate at voltages higher than 0.5 V attributed to the series resistance once more. Planar diodes exhibit much smaller reverse currents in the range of $10^{-9} \ldots 10^{-10}$ A owing to the smaller contact areas of both contacts. However, taking a look at the forward current, two slopes appear, where the slope in the voltage range of -1 V to -0.4 V is attributed to high injection effects [241]. The emission of carriers is governed by thermal excitation, therefore the inverse subthreshold slope is an appropriate tool to examine the injection of carriers. From the fundamentals of MOSFETs (see section 2.6) it is a well-known fact that $60 \, \text{mV/dec}$ is the limit at room temperature. The doubling of the subthreshold swing is a characteristic attribute of the high injection as depicted in the logarithmic scale. Replacing aluminum by magnesium the high injection effect is shifted to higher voltage (see Fig. 6.14b).

However, the origin of the high injection state is a low forward voltage. Considering an ideal diode the high injection state is active as long as the depletion layer dominates the flow of carriers. The corresponding samples of Fig. 6.14 are not fabricated with the tilted stencil mask approach presented in section 5.1. After the first metal deposition the mask was shifted at atmosphere to set up a new area for the second shadow metallization. These samples exhibit increased reverse currents originated from the shift of the stencil mask, which led to a large amount of particle emission on the unprotected second metal regions. These results confirm the benefit of a tilt function (see section 5.4), if an automatic stage controller is not an option of the evaporation machine. Henceforth, all upcoming Schottky-Mott diode in this section are manufactured by a microstencil deposition, where the second metal layer is fabricated by tilting the microstencil-sample assembly.

Fig. 6.15a exhibits a gold aluminum Schottky-Mott diode with a promising high forward voltage of approximately 1V and a very small reverse current below 100 pA. The distance of 250 $\mu$m between the low and causes still a substantial series resistance contribution so that much more promising results are expected if the gap between the contacts is reduced. However, smaller spacings require a stencil mask, which is in direct contact or has a little gap between the sample and mask to prevent blurring and halo formation. Furthermore, the mask needs to be shifted in x and y direction manually or by a x-y stage controller due to a smaller gap. A closer look at the inverse subthreshold slope reveals a suspicious behavior.

Fig. 6.16 displays the inverse subthreshold slope of two diodes from Fig. 6.15a and b. First of all, a clearly defined plateau of an almost constant inverse subthreshold voltage is obtained. Secondly, two extrema are apparent in this range. A maximum of $98 \, \text{mV/dec}$ is located at approximately 250 mV and a minimum of $90 \, \text{mV/dec}$ is assigned close to 485 mV. This minimum could be even smaller and more left-shifted to more negative voltages if the series resistance is further reduced. As mentioned earlier the low P-type doped substrate leads to asymmetric Schottky-Mott junctions at the silicon-silicon nitride-metal interfaces. The Schottky-Mott junction at the low work function metal governs almost the entire rectifying behavior. For small negative bias voltages, most of the voltage drop occurs over the aluminum junction. Lowering the bias voltage the electrical field of this depletion layer is reduced until the electrical
6.2. Rectifying Nature of Schottky-Mott Junctions

Figure 6.15: Planar diodes are fabricated by shadow evaporation (tilted microstencil) (see section 5.4): a) Au-Al-Si₃N₄ Schottky-Mott diode, squared 110 µm sized contact pads, gap 250 µm, planar diodes, b) Second Au-Al-Si₃N₄ Schottky-Mott diode with a smaller forward voltage, squared 110 µm sized contact pads, gap 250 µm.

Fields at the aluminum and gold junctions become equivalent so that both junctions determine simultaneously the transport of carriers. This phenomenon will not occur for symmetrically shaped energy selective contacts assuming an equivalent contribution of both junctions. Furthermore, this behavior is predicted for two Schottky barriers at the interfaces. The electric field of the Schottky-Barrier needs to point in the same direction of the field of the P-N depletion layer. Rajasekharan et al. have applied a different fabrication procedure for a double SB device [242]. They have directly formed Schottky-barriers with erbium (low work function) and palladium (high work function) and backgated the channel (three terminal device). The backgating ensures an additional band bending so that the field of the depletion layers at the metal silicon interfaces points in the same direction. A minimum of the current swing was observed for -20 V but Rajasekharan et al. have not paid attention to this particular behavior. In principal, this phenomenon offers a promising approach to examine metal-nitride-contact formation of asymmetric design. Once a metal contact is well characterized, the second one can be studied by the inverse subthreshold slope. Also, the ultra-thin device layer of 20 nm SOI thickness reveals excellent subthreshold swings, which are close to the limit by thermionic emission. In addition, the subthreshold swing provides a simple determination of the ideality factor [243]. Focusing on the minimum $S_{min}$ the subthreshold voltage depends on the ideality factor $n$ as follows:

$$S \approx nkTln(10).$$

This relation is only valid, if the reverse bias saturation current can be neglected (see equation 2.5, section 2.2.1). The reverse bias saturation current is 850 pA at 2.5 V and is sufficiently smaller in relation to the forward current of 6 µA at 485 mV, which results in an ideality factor of 1.5. Three major reasons contribute to an increase of the ideality factor: Trap-assisted tunneling, native oxide pinholes as well
as the presence of a large interface state density results into a degradation of the ideality factor [244–247]. The substantial hydrogen content inside the ultra-thin silicon nitride layers (<1 nm) may lead to a band gap lowering as already discussed in chapter 4 so that the interface state density is increased. Here, a further study of the interface state density is required. An optimization of the silicon nitride growth process by an atomic layer growth procedure might be possible to reduce the amount of hydrogen by nitriding at lower temperatures (~250°C) and outgasing of hydrogen at higher temperatures (~800°C) and repeating it until a thickness of approximately 0.7 nm is established. Moreover, the silicon nitride-silicon interface can benefit of a post metal annealing study to ensure a hydrogen passivation of dangling bonds. Nevertheless, in literature even higher ideality factors are usually observed confirming the need of an excellent tunneling insulator [248, 249].

6.2.2 Metal-Silicon Nitride-Silicon-Field Effect

In section 6.1 the impact of the thickness of the nitride on the current was demonstrated. Here, the impact of the silicon nitride thickness on the surface of silicon is studied. Therefore, three nitridation runs at 450°C, 600°C and 850°C are performed. The thickness of nitrides is determined by ellipsometry measurements corresponding to 0.8 nm, 1.1 nm and 1.7 nm. Owing to the large tunneling resistance of thicker nitrides the IV-curves are normalized to compare the impact on the for-
Rectifying Nature of Schottky-Mott Junctions

6.2. Rectifying Nature of Schottky-Mott Junctions

Figure 6.17: Forward current normalized by the linear slope $G_s = \frac{1}{R_s}$ of Au-Al Schottky-Mott diodes for various nitrides grown at 450°C, 600°C and 800°C is shown.

Forward voltage (see Fig. 6.17). Hence, the thicker nitrides exhibit higher resistances, which leads to a higher $I \cdot R_s$ product. It is apparent that thicker nitrides cause less band bending so that the Schottky-Mott barriers decrease. The forward voltage versus thickness is depicted in the inset of Fig. 6.17 and a clear exponential decay is observed, which confirms the potential barrier related dependence of the transmission.

Furthermore, this correlation is manifested by a THz analysis. On nitrided samples at various annealing temperatures 450°C, 600°C and 1100°C and native oxide reference samples lines and spaces of metal are deposited by a lift-off process. The thickness of platinum is about 25 nm, while the second layer of 25 nm aluminum is evaporated at an angle of 60° leading to Pt-Al gaps in the range of 25-35 nm (see section 5.7). First of all, all samples show the characteristic THz response illustrated in Fig. 6.18, which is explained in section 3.3. The highest signal is obtained for the thinnest nitrides grown at 450°C. Increasing the thickness causes a reduction of the THz signal, keeping in mind that the THz response is directly related to the field of the Schottky-Mott depletion layer. The THz amplitude of the thickest nitride grown at 1100°C is reduced by a factor of two. Moreover, the reference sample with native oxide between metal and silicon exhibits the minimal signal associated to the smaller dielectric permittivity in contrast to silicon nitride layers (see section 2.3). However, if the intensity is plotted against thickness, a clear exponential dependence
6. Device Characterization

Figure 6.18: THz response of Pt-Al lines with a feature gap sizes between 25-35 nm on various nitrides grown at 450°C, 600°C and 800°C is depicted, inset: Peak intensity of the THz response versus thickness.

is observed in the inset of Fig. 6.18. The decay of the intensity is less intense as in the case of the IV characteristic shown in the inset of Fig. 6.17. The THz response is completely governed by the strongest field along the silicon nitride-silicon interface in contrast to the IV measurement, where more or less an average field is detected because local defects might have an impact on the interface. Therefore, the decay of the intensity versus thickness is weakened.
6.2.3 Breakdown of Schottky-Mott Junctions

For vertical diodes, owing to the thick substrate of 525 µm, no breakdown effect is observed below 100 V, which is the maximum possible applied bias by the HP4156A semiconductor parameter analyzer. Therefore, planar Schottky-Mott diodes are fabricated to reduce the gap between both metal layers. The silicon surface is nitrided at 450 °C prior to a gold and aluminum microstencil evaporation. Fig. 6.19a displays the reverse current as a function of the reverse voltage of diodes with 200 µm separated pads. First, the reverse current rises very slowly owing to the rectifying nature of the SM diode. Close to 100 V the current starts to increase but no breakdown is observed indicating a breakdown voltage outside the voltage range. Nevertheless, two additional runs into breakdown afterwards do not confirm a damage of the diode, even a smaller current is obtained at 100 V. A second sample exhibits a clear breakdown at approximately 90 V despite the fact of an equal distance (Fig. 6.19b). But this time, the breakdown has some severe impact on the diode, which is confirmed by two subsequent measurements. The reverse current

![Graphs showing reverse current vs. reverse voltage](image)

**Figure 6.19:** Breakdown behavior of planar diodes are presented: a) Reverse current in logarithmic scale of a Au-Al-Schottky-Mott diode, 180 µm squared pads approximately 200 µm apart, b) reverse current in semi-logarithmic scale of a second Au-Al-Schottky-Mott diode, 180µm squared pads approximately 200 µm apart, c) reverse current of a Co-Al-Schottky-Mott diode, 180 µm squared pads approximately 110 µm apart, d) reverse current in semi-logarithmic scale of the Co-Al-Schottky-Mott diode from c).
is more or less a factor of 100 larger and rises much stronger with applied bias. Reducing the distance leads to an expected lowered breakdown voltage. However, if the gold contact is replaced by a cobalt layer and the separation is reduced to a distance of 110 µm, the breakdown voltage appears at almost 85 V (Fig. 6.19c) despite the fact that the distance is approximately halved. The current is limited by the compliance of 20 mA. The sweep backward exhibits a clear exponential rise of the current at a bias of 40 V. In logarithmic scale the breakdown is observed at 78 V (Fig. 6.19d). The exponential rise of the current starts already at lower voltages. The stronger resistance for breakdown in Co-Al-SM diodes is attributed to the non-noble metal cobalt. The spacing is effectively cut by the cobalt (as well as for gold) halo frame across the pads (see section 5.1) In addition, the native oxidation of these non-noble metal halo regions strengths the resistance for breakdown. A passivation of the surface by an oxide deposition or oxidation prior to nitridation is going to enhance the reliability and the increase the breakdown voltage of the diodes [250,251].
6.2. Rectifying Nature of Schottky-Mott Junctions

6.2.4 Contamination by Nanostencil Lithography

A nanostencil mask offers a simple method to test the impact of evaporated contaminants on the ultra-thin silicon nitride layer. Therefore, a double layer of shadow masks is applied so that the metal pad layer is close to the silicon nitride sample (see Fig. 6.20a), while the nanostencil mask is oriented with respect to the top of the first shadow mask. The orientation requires a matching of the nanostencil region to the contact pad area. On a low P-type doped silicon substrate the nitride is grown at 450 °C. Prior to the gold layer evaporation a 3 nm aluminum layer is deposited (see Fig. 6.20b and 5.7). Fig. 6.21a shows the reference IV curve of a device consisting of two gold contacts on the silicon nitride layer without any aluminum contaminants (black curve). A clear ohmic rise of the current is observed, while in the case of the nanostencil contaminated area the aluminum causes a super linear rise attributed to the impact of the aluminum. The depletion layer of an Al-silicon nitride-Schottky-Mott junction on a P-type substrate is much more dominant in contrast to the gold silicon nitride-low P-type silicon junction. Therefore, this large impact of a tiny layer has a severe impact (see semi-logarithmic scale in Fig. 6.21b).

Figure 6.20: The contamination through the nanostencil mask is illustrated: a) stack of stencil masks for a 3 nm aluminum evaporation, the nanostencil masked is aligned on top of the microstencil layer to one open contact pad region, b) after evaporation one contact pad is artificially “contaminated” by the 3 nm aluminum layer.
6. Device Characterization

Figure 6.21: IV characteristic of Fig. 6.20 is depicted: a) Current-voltage characteristic between two gold pads on a nitrided low P-type doped silicon substrate, silicon nitride is grown at 450 °C, 3 nm of aluminum evaporated through a nanostencil mask prior to the gold evaporation (red line), b) semi-logarithmic scale of the current depicted in a).

6.2.5 Reverse Capacitance

Since Schottky-Mott junctions are majority based devices similar to Schottky diodes rather small reverse capacitance are expected. In Fig. 6.22a the total reverse capacitance of a Au-Al-nitride450 °C-Schottky-Mott diode versus reverse voltage is depicted at 1Mhz. First of all, a very small capacitance at zero bias is observed, taking into account the large contact area of 140 µm times 140 µm, values of below 1 pF are expected comparing it with industrial products (below 50 µm) [252–254]. Secondly, the capacitance does not strongly increase close to zero bias, which is attributed to the high built-in voltage of the Schottky-Mott junction in contrast to conventional Schottky diodes. Since a low doped P-type substrate (5-10 Ωcm, boron) is the bulk material of the SM diodes, the design is similar to conventional Schottky devices, where one contact exhibits more or less an ohmic behavior, while the second one provides the Schottky barrier. The gold metal layer on the nitrided silicon surface acts as an ohmic contact, while the aluminum area provides the rectifying nature.

Furthermore, a capacitance voltage analysis provides a method to calculate the built-in voltage of diodes. The depletion layer capacitance depends on the built-in voltage as follows [35]:

$$C_{depl}(V) = \sqrt{\frac{q\varepsilon Si N_a}{2(V_{bi} - V - \frac{2kT}{q})}}. \tag{6.3}$$

The equation 6.3 is solved for the extrapolation at V=0 V, which gives the built-in voltage:

$$\frac{1}{C_{depl}^2} = \frac{2(V_{bi} - \frac{2kT}{q})}{q\varepsilon Si N_a}. \tag{6.4}$$
6.2. Rectifying Nature of Schottky-Mott Junctions

Figure 6.22: CV characteristics of a Schottky-Mott diode are presented: a) Reverse capacitance versus reverse voltage of a Au-Al-Schottky-Mott diode, $300 \mu m$ gap, $140 \mu m$ squared pads, b) inverse capacitance versus voltage for a Au-Al-Schottky-Mott diode, $300 \mu m$ gap, $140 \mu m$ squared pads.

Fig. 6.22 b demonstrates the linear behavior of a Schottky-Mott diode. Taking advantage of Eqn. 6.3 the extrapolation results in a built in voltage of approximately $1.1 \text{V}$. Moreover, from the slope of the $C_2$ a substrate doping concentration of $1.94 \cdot 10^{15} \text{cm}^{-3}$ is determined, which is close to the real one of $1.7 \cdot 10^{15} \text{cm}^{-3}$. Considering the silicon band gap energy $E_g$ of 1.12 eV the CV-result confirms the presence of a substantial electrical field present at the silicon surface.

6.2.6 Highly Doped Schottky-Mott Junctions

The doping concentration of the substrate results in a shift of the Fermi level either close to the N-type or P-type contact. Hence, only one dominant Schottky-Mott junction is present. High doping concentrations ensure an ohmic contact formation for Schottky junctions owing to the decreasingly small width of the Schottky barrier, which is also valid in the case of low (high) work function metals in contact to silicon nitride on a highly N-type (P-type) doped silicon.

Fig. 6.23 a shows the IV characteristic between two aluminum pads on a highly doped N-type (As)substrate. The resistivity of the arsenic doped substrate is $0.005 \Omega \text{cm}$ corresponding to a doping concentration of approximately $10^{19} \text{cm}^{-3}$ and a Fermi energy of 20 meV below the conduction band edge [255, 256]. First of all, a symmetric rise of the current for negative as well as for positive bias is observed, however, a small exponential rise is attributed to the evaporated aluminum on the large contact areas ($500 \mu m \times 500 \mu m$) and the small barrier of ~20 meV originated from the Fermi-level of the highly doped substrate. Furthermore, the current is limited by the compliance at 100 mA. If now the current is determined of a device consisting of two gold contacts a superlinear rise is observed (Fig. 6.23 b), demonstrated in semi-logarithmic scale (see inset of Fig. 6.23 b). The current between aluminum and gold exhibits a rectifying nature as depicted in the Fig. 6.23 c. Also, the series resistance is reduced by a factor of at least 1000 in comparison to the low doped diodes in the preceding section, which is demonstrated by the extended thermionic
6. Device Characterization

emission regime of the Schottky-Mott diode in forward bias \((V \approx 0.9 \text{ V}, \text{ inset of Fig. 6.23 c})\). On a linear scale a very large reverse current is present attributed to the very thin width of the Schottky-Mott depletion layer, which is also observed in semi-logarithmic scale. On highly P-type doped substrates \((0.01-0.02 \Omega \text{ cm})\) with a doping concentration of almost \(4.73 \cdot 10^{18} \text{ cm}^{-3} (E_F\sim 30 \text{ meV})\) a rectifying behavior is also confirmed (Fig. 6.23 d). However, a smaller built-in voltage is observed, which originates from the large series resistance \((300 \mu \text{ m distance in contrast to } 200 \mu \text{ m sized As Schottky-Mott diodes})\) observed by the impact in the semi-logarithmic scale (inverse subthreshold slope starts to rise below 500 mV) in contrast to arsenic doped substrates.

\[
\begin{align*}
\text{a)} & \quad \text{b)} \\
\begin{array}{c}
\text{c)} \\
\text{d)}
\end{array}
\end{align*}
\]

Figure 6.23: IV characteristics of planar Schottky-Mott diodes made out of highly doped substrates are depicted: a) current-voltage measurement of arsenic doped \((0.005 \Omega \text{ cm})\) \(\text{Al Si}_3\text{N}_4\)-\(\text{Si (As)}\)-\(\text{Si}_3\text{N}_4\)-\(\text{Al}\) sandwich, b) current-voltage measurement of arsenic doped \((0.005 \Omega \text{ cm})\) \(\text{Au Si}_3\text{N}_4\)-\(\text{Si (As)}\)-\(\text{Si}_3\text{N}_4\)-\(\text{Au}\) sandwich, c) highly arsenic doped \((0.005 \Omega \text{ cm})\) \(\text{Au-AI}\) Schottky-Mott diode IV characteristic, inset: semi-logarithmic scale of the current, contact pad size \(140 \mu \text{m}, \text{ gap } 250 \mu \text{m}\), d) highly boron doped \((0.01-0.02 \Omega \text{ cm})\) \(\text{Au-Al}\) Schottky-Mott diode IV characteristic, inset: semi-logarithmic scale of the current, contact pad size \(300 \mu \text{m}, \text{ gap } 250 \mu \text{m}\).
6.2.7 Temperature-dependent Characteristics of Schottky-Mott Junctions

The impact of the process temperature during nitridation temperature and the thickness of the nitriding temperature was demonstrated by IV measurements and THz time domain spectroscopy in section 6.2.2. In addition, the impact of the temperature on the forward voltage is presented here in order to compare with a P-N junction and its nearly linear temperature coefficient of $-2 \text{ mV/K}$. Samples nitrided at 450°C are examined at 200 K, 250 K and 300 K. The temperature coefficient is determined by definition at a constant current, here approximately 55 $\mu$A. Owing to the destruction of the metal-silicon nitride-silicon contact by the harsh positioning of the probe needles several series of Schottky-Mott diodes were destroyed by scratching, which leads to Schottky characteristics (the metal probe needle governs the Schottky contact once the needle is in direct contact to silicon). Therefore, only Schottky-Mott diodes with small voltages were left for a temperature study. Fig. 6.24a displays the temperature-dependent forward voltage. Decreasing the temperature increases the forward voltage. Plotting the forward voltage as a function of the temperature and adding the established temperature coefficient of a P-N junction into the graph reveals an almost equivalent performance (see Fig. 6.24b).

![Figure 6.24: Temperature behavior of the forward current voltage of Schottky-Mott diodes are depicted: a) Forward current-voltage characteristic of Au-Al-Si$_3$N$_4$ Schottky-Mott diodes at 200 K, 250 K and 300 K for 55 $\mu$A, 200 $\mu$m squared contact pads b) forward voltage plotted versus temperature, red line corresponds to the conventional P-N junction temperature coefficient $-2 \text{ mV/K}$ assuming 400 mV forward voltage at 300 K.](image-url)
Beyond Freeze Out

Low doped materials suffer from Freeze Out at very low temperatures (<50 K), while very large scale integration (VLSI) approaches for cryogenic applications suffer from the variability of dopants. Most low temperature characteristics are governed by the Schottky-barrier leading to an additional contact resistance \[^{257}\]. Taking advantage of a low doped silicon substrate the Fermi energy is located between the ionization energy of the dopant (boron, \(\sim 45\) meV \[^{258}\]) and the edge of the valence band or conduction band, respectively. This has a substantial impact on Schottky-Mott junctions, if, for instance, gold or platinum as high work function materials with a P-type (boron) low doped and at 450 °C nitrided silicon are used, the built-in voltage is in the range of \(-22.5-45\) meV for low temperatures causing very small barriers to overcome. Fig. 6.25a demonstrates low temperature dependent IV characteristics between two gold pads (200 \(\mu\)m squared) laterally separated by 300 \(\mu\)m in the range from 8.5 K to 65 K. The lowest reachable temperature of the cryogenic setup is 8.5 K. The lowering of the temperature reduces the current due to the higher silicon band gap energy for lower temperatures \[^{259}\]. Secondly, two regimes are present. For higher temperatures (>250 K) the ionization degree is still quite high, e.g. \(-0.7\) for \(1.5 \cdot 10^{15} \text{cm}^{-3}\) at 65 K \[^{260}\], which results in a barrier of approximately 36 meV. A thermionic emission is strongly reduced for low temperatures. The thermal voltage is in the range of 0.73 meV (8.5 K) and up to 5.6 meV (65 K). The large noise at 8.5 K is attributed to an insufficient contact between needle and pad, which never appeared for higher temperatures. At lower temperatures \(<25\) K the ionization degree is close to zero leaving behind a barrier originating from the ionization energy of the dopant. However, the applied bias reduces the barrier so that holes are injected, which is demonstrated by the current step below 1 V. The semi-logarithmic scale reveals a sharp transition in the range of 220 mV up to 370 mV (see Fig. 6.25 b). Smaller voltages lead to not measurable currents due to the noise level.

![Figure 6.25](image-url)

Figure 6.25: IV characteristics of P-type contacts on low P-type dopde substrate are shown at low temperature: a) Low temperature current voltage characteristics between two 300 \(\mu\)m distant golden regions on a low doped silicon substrate nitrided at 450 °C, b) semi-logarithmic scale of the low P-type temperature current voltage characteristics of a).
It is quite remarkable that a transport of hole carriers is observed over a distance of 300 µm in spite of dopant Freeze Out, although, high mobilities for holes are expected owing to the low doping concentration.

6.3 Ultra Thin Silicon Nitride-Solar Cell

6.3.1 Standard-Solar Cell

One rudimentary silicon solar cell design was introduced in the fabrication section 2.3. Fig. 6.26a demonstrates the IV curves of various illumination states of a 4 cm² solar cell consisting of a highly doped emitter (−8·10¹⁸ cm⁻³). At 1 sun an open-circuit voltage V_OC of 500 mV and a short-circuit current density J_SC of 15.95 mA cm⁻² is observed.

Owing to the large series resistance the solar cell exhibits a low fill factor FF of 0.284 attributed to the Schottky contact on the backside and the thin metallization layer of 100 nm aluminum. However, if the silicon surface is nitrided at 450°C prior to metallization, the aluminum-silicon nitride-silicon interfaces (front and rear side of the substrate) lead to back to back diode configuration, which is demonstrated by the double rectifying nature and a shift of the open-circuit voltage. A closer look at the open circuit voltage operation point confirms the impact of the Schottky-Mott junction at the backside. In addition, a low intensity of the incident light causes a higher open circuit voltage. The reverse state of the backside junction introduces an extra parallel resistance (see low illuminated state which is confirmed by the differential resistance at V=0 V. The standard cell exhibits an approximately 1.56 times smaller value (see Fig. 6.27a), while the series resistance is smaller associated to the larger current. However, the increased parallel resistance as well as the increased open-circuit voltage V_OC lead to a much higher maximum power demonstrated in Fig. 6.27b. Hence, the fill factor rises from 0.385 up to 0.402.

Figure 6.26: IV characteristics of a standard solar cell are depicted, where the emitter is doped by POCl₃ process: a) IV characteristic of a reference sample without nitridation b) POCl₃ doped substrate is nitrided at 450°C, aluminum layer is deposited on the front and rear side.
Figure 6.27: IV characteristics of a standard solar cell and a solar cell with silicon nitride are compared: a) low intensity at 0.085 suns of the solar cells from Fig. 6.26a and 6.26b, b) power versus voltage of solar cells at low intensity 0.085 suns.

Increasing the intensity causes a reduction of the parallel resistance of the Schottky-Mott diode so that the open-circuit voltage decreases. The Schottky-Mott junction on the backside is less dominant associated to the substrate thickness of 525 µm, which excess electrons need to propagate without recombination. The rather small minority bulk life of 50 µs exacerbates the propagation of carriers (see section 4.4). Furthermore, the electrical field of the emitter-base junction attracts the generated electrons into the emitter region. It is remarkable that the open-circuit voltage drops with rising intensity.

Nevertheless, the positive impact of a Schottky-Mott junction for a solar application is demonstrated by changing the backside metal. Replacing the backside aluminum layer with a gold capping, which provides the required P-type contact, a clear improvement of the standard solar cell is obtained as depicted in Fig. 6.28a and b. The short-circuit current $I_{SC}$ is increased by approximately 12 mA, which is attributed to the formation of ohmic contacts by the ultra-thin silicon nitride layer on both sides.

Figure 6.28: IV characteristics of POCl₃ doped and at 450°C nitrided solar cell are depicted: a) IV characteristics, aluminum (gold) is evaporated on the front (rear) side, b) semilogaritmic scale of the IV curves in a).
6.3. Ultra Thin Silicon Nitride-Solar Cell

Figure 6.29: IV characteristics of MIS solar cell with an ultra-thin silicon nitride layer are depicted: a) IV characteristics of a solar cell, nitrided at 450 °C, aluminum (gold) is evaporated on the front (rear) side, b) semi-logarithmic scale of the IV curves depicted in a).

Even the open circuit voltage is increased by almost 50mV. Both improved figure of merits cause a rise of the fill factor FF from 0.28 up to 0.354. Additionally, from the semi-logarithmic scale in Fig. 6.28b it can be expected that a rise of the parallel resistance should enhance the key properties of the solar cell.

6.3.2 Silicon Nitride-MIS Solar Cell

In the preceding section the impact of the ultra-thin silicon nitride on the performance of solar cells was presented. It is even a bigger challenge to introduce a complete dopant free solar cell or at least out of low doped substrates. Considering a P-type doped substrate without a doped (e.g. POCl₃) emitter, silicon nitride is grown at 450 °C and an aluminum (front) and gold (rear) metallization are done. The IV curve (see Fig. 6.29) of the first-time ultra-thin silicon nitride MIS-solar cells exhibit an exponential rise in contrast to the previous ones in the former section which are depicted in Fig. 6.28a. The inset displays a clear concave rise. It is well known in literature that the lack of a field passivation layer or doped emitter on the surface increases the series resistance dramatically, which leads to a Schottky-formation [261]. Therefore, most of the MIS-solar cell designs contain a field effect passivation layer to ensure a complete depletion layer of the entire surface not only beneath the contact regions.

Furthermore, an increased reverse current is observed, which is one major disadvantage owing to the large impact of the contamination during lift-off process on the ultra-thin silicon nitride surface. Here, section 6.2.4 already showed the impact of 3nm aluminum halo evaporation on a gold-silicon nitride Schottky-Mott junction. Owing to the lack of an appropriate field effect passivation layer a new approach is considered. The evaporation of a 3nm aluminum halo layer offers two promising features:

- Metal field effect evaporation concept (field passivation is done after metal-
6. Device Characterization

Figure 6.30: IV characteristic of a MIS solar cell with halo passivation layer are depicted: a) IV characteristics of a Al-Au-silicon nitride $450^\circ C$ solar cell with a 3 nm aluminum halo layer, b) semi-logarithmic scale of the IV curves demonstrated in a).

- Halo formation and native oxide of non-noble metals reveal a much higher resistance (see section 6.2.3).

Measurements of the reflection for various thick metal field layers (appendix L) exhibit a small additional reflectance of the incident light. Fig. 6.30a demonstrates the best solar cell of this thesis on a 4 cm$^2$ sample with a 3 nm-Al halo layer. The concave rise of the current does not any longer appear owing to the introduced 3 nm-Al halo layer, which leads to a FSF and a reduced series resistance. However, the current is sufficiently lower in contrast to the emitter doping by POCl$_3$ demonstrated in the preceding section (see Fig. 6.28).

 Imperfections inside the silicon nitride layer over the entire surface are one reason for small open circuit voltages. It is well known from literature that voids present in the insulating layer reduce the total open circuit voltage [262]. Voids result into a local oxidation of the silicon surface. The void density might be increased in this fabrication process due to a wet native oxide removal step prior to nitridation in a RTP chamber. If the native oxide is directly removed in a high vacuum system, for instance by a hydrogen annealing [263,264], an improved performance is expected. Moreover, a sophisticated field effect passivation will enhance the emitter conductivity. Additionally, the fill factor FF is improved in relation to the reference samples of approximately 0.147 depicted in Fig. 6.29a. Furthermore, the semi-logarithmic scale of the IV curves in Fig. 6.30b demonstrates a substantial rise of the reverse current, which is attributed to contaminants caused by the metal lift-off process.

6.3.3 Planar Schottky-Mott diode and MIS-Solar Cell

MIS-solar cells fabricated in cm dimensions require a perfect clean fabrication process, a sophisticated shadow evaporation in combination with an excellent field effect
passivation concept. Supported by the fact that a halo layer provides a promising field-effect passivation Co-Al-Schottky-Mott junctions are fabricated by shadow evaporation for the purpose of a top solar cell design depicted in Fig. 6.31 a, b and c). Fig. 6.32 shows the IV curves of the illuminated and dark states of the Co-Al-Schottky-Mott diode. Despite the fact of a small forward voltage the minimized solar cell exhibits very promising characteristics. First of all, it shows the highest measured fill factor FF of 0.744 in this work, which is not the end of optimization owing to the high series resistance (see Fig. 6.32 a and b at voltages below -0.5 V). A reduction of the series resistance would even further enhance the fill factor FF. Second, in semi-logarithmic scale the forward current as well as the reverse current reveal excellent behavior. In addition, the open-circuit voltage $V_{OC}$ is also affected by the shading of the probe needles due to the small pad size of 180 $\mu$m and a pad distance of 300 $\mu$m. Furthermore, the small open-circuit voltage $V_{OC}$ is attributed to the contamination of the carbon crucible during the ebeam evaporation.
Figure 6.32: IV characteristics of a planar Schottky-Mott diode are depicted, which is illustrated in Fig. 6.31 c: a) IV characteristics of a Co-Al-silicon nitride\(_{450}^{\circ}C\)-Schottky-Mott diode illuminated by two various light sources, 0.1 suns and 1 suns, 180 \(\mu\)m pad feature size, 300 \(\mu\)m gap between pads, b) semi-logarithmic scale of the IV curves shown in a).
6.4 Resonant Tunneling Diodes

6.4.1 IV Characteristics of Silicon Nitride based Resonant Tunneling Diodes

Room Temperature Characteristics

The fabrication of the resonant tunneling diodes is described in section 5.7. Here, the current-voltage characteristics of these diodes are presented. Fig. 6.33a shows the current voltage of three diodes, which exhibit plateaus at approximately 1.8 V and −1.85 V verified by the extrema of the first derivative of the current (see inset of Fig. 6.33a). The small deviation of the plateau position for negative voltages is attributed to the small difference in contact areas owing to the tilted second mask (explained in section 5.7). In semi-logarithmic scale these clear steps are also observed in Fig. 6.33b. 16 diodes of four individual samples were characterized and each of them demonstrated a clear plateau (see appendix M). Replacing the aluminum layer by gold results in an exponential rise of the current and less pronounced plateaus as shown in Fig. 6.34a. The smaller current hints at a much higher series resistance so that the plateaus are shifted to higher voltages. In semi-logarithmic scale the appearance of the plateaus is not strongly pronounced (see Fig. 6.34b). But the differential conductivity confirms the existence of a plateau displayed in the inset of Fig. 6.34a. However, the resonant tunneling diodes exhibit small hystereses at short integration times of 640 µs (see inset of Fig. 6.34b). It is expected that the hysteresis shrinks for longer integration times. Furthermore, reference samples fabricated by a PECVD process (appendix N), where a plasma nitridation of the silicon substrate surface is performed and subsequently, an approximately 5.5 nm
6. Device Characterization

Figure 6.34: IV characteristics of RTD with gold contacts are depicted: a) IV characteristics at room temperature of three golden resonant tunneling diodes, inset shows the differential conductivity of the third RTD revealing a minimum of the slope proving the existence of a plateau, b) semi-logarithmic scale of the three diodes demonstrated in a), inset demonstrates a small hysteresis for short integration times, here 640 µs; The first two letters stand for the metal layer (Al, Au), the third letter separates the silicon nitride processes (R = RTP nitridation, P = Plasma nitridation) and the number corresponds to the device.

A thick amorphous silicon layer is deposited. Finally, the amorphous silicon layer is again nitrided. These samples allow to consider only a-Si related transport phenomena. First of all, these reference sample exhibit much smaller currents (see Fig. 6.35 a). However, an exponential rise is observed and no plateaus occur. In

Figure 6.35: IV characteristics of the reference samples without a nanocrystalline layer are depicted: a) IV characteristic of a plasma nitride-amorphous silicon-plasma nitride stack exhibiting a strong exponential rise, b) semi-logarithmic scale of the stack shown in a) demonstrates an almost constant rise of the current; voltages above 1.5 V caused a breakdown of the nitride sandwich, thus the regime was set to a maximum voltage of 1 V; The first two letters stand for the metal layer (Al, Au), the third letter separates the silicon nitride processes (R = RTP nitridation, P = Plasma nitridation) and the number corresponds to the device.
semi-logarithmic scale the exponential rise of the current is confirmed by the linear behavior displayed in Fig. 6.35b. In addition, the slope of the current rise is increased and more or less constant over the entire voltage range in contrast to the resonant tunneling diodes introduced in Fig. 6.33b. The latter ones exhibit a current increase of three decades from zero up to 1 V, while the plasma nitride stack reveals a subthreshold swing of approximately $250 \text{ mV/dec}$, which is attributed to the low annealing temperature of 350$^\circ$C during nitridation so that the plasma nitrides are less insulating.

**Low Temperature Current Voltage Characteristics**

The temperature limit of 8 K of the cryogenic system could not be reached owing to the low doped substrate and its freeze-out. Furthermore, the lowest temperature of a observable current was 65 K. The temperature range was set from 65 K up to 135 K depicted in Fig. 6.36a. First of all, two clear peak-valley regions appear at approximately 1.18 V and 2.1 V for 65 K. Taking a closer look at the current below the first peak in semi-logarithmic scale no particular appearance is observed (see Fig. 6.36b). Increasing the temperature reduces the current noise and increases the current. Furthermore, the low doped channel of the double barrier resonant tunneling diode has a large impact on the total resistance of the device, which is demonstrated by the shift of the peak position if the temperature is raised. Fig. 6.36c displays the position of the peaks as a function of temperature. The shift reveals a more or less quadratic rise. Schindler et al. have introduced a method to determine the resistivity of a doped substrate by a modified mobility model [255, 256]. This method is used to calculate the resistivity for the applied temperature range and illustrated in Fig. 6.36c. The curve demonstrates also a quadratic increase verifying the impact of the phonon-scattering in the low doped channel, while at lower temperatures the mobility is rather constant. Hence, at room temperature considering the specified resistivity of 7-10$\Omega$cm the temperature shifts the plateau to a voltage of 1.8-1.85 V demonstrated in Fig. 6.33a. Nevertheless, it is the first time that a resonant tunneling diode made of silicon nitride insulators is successfully fabricated by RTP and PECVD. Moreover, these sandwiches exhibit two resonant peaks. The peak-to-valley ratio of 1.31 is remarkably high, which is the first time that a deposition and a post-annealing process provides these high PVCRs. However, replacing the low doped substrate by a highly doped silicon bulk material a further reduction of the temperature will increase the PVCR. Fig. 6.36d shows the temperature-dependent PVCR of both resonant states. Considering a highly doped substrate the series resistance of the bulk material is reduced by several orders of magnitude. In addition, the complete covered metal surface of the RTD stack contributes to the overall current in contrast to this design fabricated by shadow evaporation, which has the drawback of a large variation of locally arranged crystalline clusters (explained in section 5.7).
6. Device Characterization

6.4.2 Capacitance-Voltage Characteristics

For the purpose of a capacitance analysis the samples are completely metalized by a Ti/Au layer stack on the backside to ensure a low contact resistance. Fig. 6.37a shows the capacitance-voltage characteristic of three individual stacks. First of all, for negative voltages below $-1.25 \text{ V}$ the substrate is accumulated by carriers. Increasing the voltage, a broad capacitance peak appears, which is attributed to the amorphous-nanocrystalline silicon layer. In section 6.4.1 reference samples made of a plasma-nitride-amorphous-silicon-plasma nitride stack were introduced. Comparing the capacitance-voltage characteristics of both material stacks (see Fig. 6.37b) an almost equivalent behavior is observed. Hence, the capacitance peak originates from the residual non-crystallized amorphous silicon of the RTP nitrided stack. The higher capacitance at $V=0 \text{ V}$ in contrast to the plasma nitridation stack (5.5 nm) results from the much initially thicker amorphous silicon layer (7 nm). Furthermore, the second nitridation step at 1050°C causes a large outgasing of hydrogen leaving behind unsaturated dangling bonds. A post metal annealing in a hydrogen/nitrogen atmosphere should improve the performance, which is not part of the analysis here.
A frequency-dependent analysis of the peak gives insights on the time range of the states present in the plasma nitridation or in the RTP nitridation stacks. The relation of a frequency-dependent capacitance can be expressed by a rudimentary approach of various time-dependent responses, which can be attributed to different transport phenomena:

$$\frac{C(f)}{C(0)} = \frac{1}{\sqrt{1 + (2\pi \tau f)^2}},$$  \hspace{1cm} (6.5)

where \( \tau \) is the time constant. The peak capacitance is normalized to the maximum value at the lowest frequency of 400 Hz. The capacitance-frequency measurement is depicted in Fig. 6.37c by the dark symbols. The red curves correspond to a \( \tau \) of approximately 10\( \mu \)s. The time constants differs from the work of Berghoff, where a time constant of 0.2\( \mu \)s was determined [90]. He has attributed this time constant to the loading and unloading of the nanocrystalline cluster. However, taking a closer look at the reference sample a similar shift of the peak to higher voltages is observed, which Berghoff associated to the impact of the nanocrystalline cluster. Silicon nitride resonant tunneling diodes exhibit a completely different behavior. The peak position is more or less stable and even goes to smaller voltages (see Fig. 6.37c, blue symbols), if high frequencies are considered. This is further underlined by the fact that the reference without any crystalline structures exhibits a distinct shift of the peak to higher voltages (see Fig. 6.37d) as also demonstrated in the work of Berghoff. Nevertheless, the peak capacitance of the amorphous layer decreases already at lower frequencies even below 500 Hz, while the resonant diodes reveal an almost constant frequency dependency. Considering one capacitance for the nanocrystals and the residual amorphous portion, respectively, the total capacitance is more or less governed by series and parallel composition of capacitances:

$$C_{tot} = \frac{2(C_{a-Si} + C_{c-Si})C_{Si_3N_4}}{C_{Si_3N_4} + 2C_{a-Si} + 2C_{c-Si}},$$  \hspace{1cm} (6.6)

where \( C_{a-Si} \), \( C_{c-Si} \) and \( C_{Si_3N_4} \) are the capacitance of the residual amorphous layer, the nanocrystalline cluster and the silicon nitride insulators. Here, the knowledge of the portion of crystalline nature inside the amorphous layer could increase the understanding of the impact of both capacitances on the time constant of the resonant tunneling diode.
Figure 6.37: CV characteristic of the nanocrystalline (RTP-process) RTDs and the amorphous reference samples are demonstrated: a) Capacitance versus voltage characteristics at 100 kHz of three individual resonant tunneling diodes fabricated by thermal nitridation, pads are circularly shaped with a diameter of 150 µm, b) Comparison of stacks of either thermal (RTP) and plasma (PECVD) nitrided stack, latter ones do not have nanocrystalline clusters due to the low annealing temperature of 290°C, c) Left axis: Normalized peak capacitance (dark symbols) versus frequency in semi-logarithmic scale, red lines correspond to simulated C(f) characteristic for time constants 7 µs and 15 µs, respectively, right axis: Voltage peak position versus frequency, d) left axis: Normalized peak capacitance of the PECVD stack versus frequency in semi-logarithmic scale, right axis: Voltage peak position against frequency of the PECVD stack.
Chapter 7

Conclusion

More than 60 years have passed without any potential competitor to the doping at the silicon interface [265–267]. Here, a silicon nitride interface engineering approach can significantly contribute to manage the Fermi level pinning. The fabrication procedure can be easily extended into a batch process owing to the self limiting nature of silicon nitride growth. Supportively, the acquisition and maintenance costs are lower than the doping counterpart. This work presented a framework of the fabrication of thermally grown ultra thin silicon nitrides in an ammonia atmosphere. Silicon nitride reveals high densities approved by oxygen diffusion and XRR measurements even for the thickness of 0.8 nm. Ultra thin silicon nitride layers exhibit excellent etching resistance, e.g. to TMAH. The high density of the silicon nitride enables thicknesses close to 0.6 nm. Nitrides with this small feature size show a huge amount of hydrogen, which is specified to be in the range of 10-15 %. The hydrogen concentration is reduced if a post annealing step at temperatures above 750 °C is performed. Nitridation temperatures close to 250 °C exhibit a huge amount of hydrogen and start to decompose or oxidize at atmosphere, which was confirmed by the subsequent decrease of the minority carrier lifetime in contrast to layers grown at 450 °C. Moreover, ellipsometry measurements of the thickness range from 0.6 nm up to 3.7 nm are in good agreement with capacitance-voltage analysis indicating excellent insulating behavior at thicknesses above 1.7 nm. The outstanding silicon nitride properties were also confirmed by the thinnest ever manufactured silicon nitride membranes of 1.7 nm, which appears to be a critical thickness range even for high quality silicon nitrides deposited by LPCVD [211].

Incorporating an ultra thin silicon nitride layer between metal and silicon provides unipolar transfer characteristics for N-type as well as for P-type MOSFETs. Aluminum and platinum MOSFETs showed on-off ratios of at least 6 decades. The P-type unipolar MOSFETs without any dopants were achieved for the first time. Vanadium with the excellent covering demonstrated subthreshold swings in the order of 140-160 mV/dec. Nickel P-type MOSFETs have not revealed this massive suppression of the ambipolar nature, which is attributed to a potential carbon contamination by the crucible. The impact of a 3 nm aluminum halo layer filtered by a nanostencil mask exhibited a huge impact on the ohmic contact formation by an occurrence of
7. Conclusion

a superlinear rise in the current-voltage behavior. Therefore, the evaporation through the here in this thesis developed microstencil masks with incorporated grooves provided a clean and pure fabrication technique to achieve ohmic tunneling junction. In addition, a tilt of the sample-microstencil mask-stack enables a multitude of deposition of metals reducing the risks of contaminants. Magnesium and aluminum for the N-type and gold for the P-type contact revealed forward voltages of approximately 1 V. Capacitance-voltage measurements confirmed very low reverse capacitance of $<5 \, \text{pF}$, which will be even lower owing to the in practice smaller contact areas of Schottky diodes [252–254]. However, the huge resistivity of the low doped substrate (5-10Ωcm) governs most of the forward current at higher forward voltages. Here, a reduction of the bulk resistance by a highly doped substrate provides a rudimentary approach to lower the series resistance and still ensures high forward voltages of almost 1 V. On the other hand, high doping leads to a single-sided dominant Schottky-Mott depletion layer, which exhibit a small depletion layer width so that a huge reverse current is observed. In addition, the rise of the reverse current is similar to a Schottky-diode, where the reverse voltage reduces the width of the depletion layer enhancing the transmission of carriers through the barrier by tunneling. A first principal investigation of the breakdown revealed that non-noble metals exhibit much stronger breakdown voltages, which is attributed to the halo formation around the pad. A direct contact evaporation or cooling of the sample is expected to bypass this halo formation resulting into much higher breakdown voltages.

Additionally, the impact of the thickness on the depletion layer was studied. Current-voltage measurements confirmed the decrease of the built-in voltage with rising silicon nitride thickness. Moreover, this is further verified by THz measurements approving a rise of the electrical field of the depletion layer with decreasing thickness. Furthermore, temperature-dependent current voltage characteristics showed a linear temperature coefficient of $-2 \, \text{mV/K}$. In addition, a current in a low boron doped substrate (5-10Ωcm) between two 300 μm spaced gold contacts was observed at even 8 K once the residual potential barrier is decomposed by the applied bias.

The existence of the depletion layer is further proven by a nitrided solar cell, where the front and rear side are metalized by aluminum. Due to the Schottky-Mott depletion layer on the backside the open-circuit voltage exhibit the highest open circuit voltage at smallest light intensity and reduces if the flux density increases. The standard solar cell was improved if a nitridation of the surfaces was performed and a gold (Al) metallization on the backside (front) is considered. Furthermore, metal halo frames were applied to prove field passivation layer impact which results in a high fill factor of approximately 0.74.

Finally, this thesis is closed by the resonant tunneling diodes fabricated out of excellent silicon nitride layers. Two clear resonant peaks in the current-voltage characteristics were observed. The first peak exhibited a PVCR of 1.3 already at 65 K, which is the first time that a PVCR ratio of >1 was achieved for nano-silicon crystals capped in silicon nitride insulators grown by RTP. Additionally, capacitance-voltage measurements could specifically demonstrate that the occurring peak is a mixture of the residual amorphous parts and nanocrystalline clusters.
What is the big picture behind this mix of results in this work? First, silicon nitride interface engineering is not bounded to any special implementation due to the omnipresent metal silicon junction. Despite the fact that in this work dopant free complementary MOSFETs in microscale dimensions are demonstrated this interface engineering becomes especially promising for nanoscale dimensions. Here, a contact dopant technology is not any longer considered due to dopant-related drawbacks bringing junctionless transistors into play [268]. On the other hand, silicon nitride interface engineering has proven that new applications are possible as Schottky-Mott diodes or silicon nitride based MIS-solar cells. Latter ones can even further improved if energy selective contacts are taken into account confirmed by the resonant tunneling diodes. What is the big picture behind this mix of results in this work? First, silicon nitride interface engineering is not bounded to any special implementation due to the omnipresent metal silicon junction. Despite the fact that in this work dopant free complementary MOSFETs in microscale dimensions are demonstrated this interface engineering becomes especially promising for nanoscale dimensions. Here, a contact dopant technology is not any longer considered due to dopant-related drawbacks bringing junctionless transistors into play [268]. On the other hand, silicon nitride interface engineering has proven that new applications are possible as Schottky-Mott diodes or silicon nitride based MIS-solar cells. Latter ones can even further improved if energy selective contacts are taken into account confirmed by the resonant tunneling diodes.
Chapter 8

Outlook

First of all, the silicon nitride fabrication procedure can be further improved by an optimized native oxide removal step. The here applied 1% HF step to strip off and to passivate the surfaces is a rather rudimentary concept. The minority carrier lifetime measurements verified the direct start of the native oxidation. The level of contamination, roughness and the oxidation by water is reduced if a HF/ethanol mixture is applied which was studied in detail by Garrido et al. [269]. The removal of the native oxide directly in the chamber/oven prior to a nitridation promises to be the best solution to avoid completely any contamination by a wet chemical treatment of the surface. A native oxide removal procedure inside a high-vacuum system is explained in literature [263,264].

The subthreshold swing of the MOSFETs can further improved if a top-gate approach and a thinner SOI device layer is considered expanding the depletion of the Schottky-Mott junction over the entire silicon depth. Furthermore, the impact of a sophisticated post metal annealing in a forming gas atmosphere could further reduce the interface density and boost the overall performance of the device.

The Schottky-Mott junctions need several revisions to increase the performance. First, the series resistance has to be lowered by minimizing the distance between contacts which would also enhance the performance of the miniaturized silicon nitride MIS solar cell with halo frames. Secondly, a prevention of a halo formation by a direct contact evaporation through the microstencil mask should increase the overall breakdown resistance. Furthermore, the open silicon nitride surface, which is not capped by metals, need to be sealed by an insulator to increase the breakdown resistance and the reliability of the devices [250,251].

The resonant tunneling diodes could benefit of a completely encapsulated vacuum system preventing any contact with the air and taking advantage of the hydrogen removal step prior to the first nitridation. Taking a glance at the crystallization process, it is expected that the crystallization starts already during heating owing to the reduced interface energy, which is a huge advantage in contrast to fully encapsulated amorphous layer prior to the crystallization annealing step. The here applied order of process steps starts with the injection of ammonia once the final annealing temperature is reached so that the amorphous silicon has a time slot to
Figure 8.1: The field effect in the channel causes band bending (red dashed lines) downwards, which opens up a tunneling path illustrated by the arrow.

form crystalline clusters once the ammonia starts to be dissociated and interact with the silicon surface. In addition, the thermal budget and silicon nitride thickness could be significantly lowered if a nanocrystalline deposition of the silicon layer by PECVD is considered [270].

Having a broader perspective regarding the impact of the silicon nitride applications the interface engineering approach becomes quite appealing for superconducting silicon based Josephson junctions where the Schottky barriers at the silicon surface require high doping concentrations at degenerate state canceling any gate modulation of the silicon channel. Here, a lower doping concentration in combination with the silicon nitride provides a sophisticated concept. Moreover, the ohmic contacts are promising if the random dopant distribution becomes a limiting factor. Cryogenic MOSFETs try to bypass the integration of dopants, which results into Schottky-barrier MOSFET transfer characteristics [257]. A second field of interest is the incorporation of the silicon nitride for Tunnel-FETs. The huge advantage of a highly doped substrate in combination with a Schottky-Mott junction (see Fig. 8.1) does not require any implantation or electrostatic side gates. Silicon nitride is not the only promising interface engineering material. Keeping in mind that germanium will play a greater role in the semiconductor industry, first steps on germanium nitride as a Fermi level depinning tool have been already performed [271]. Whereas, plasma nitridation assisted by thermal annealing of germanium is more intense studied, a thermal nitridation in ammonia atmosphere was not investigated yet [272,273]. Hexagonal boron nitride with an excellent crystalline nature and passivation skills could be the key of encapsulating 2D materials, especially for emerging research materials [274].
# Chapter 9

## List of Abbreviations and Symbols

### Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AFM</td>
<td>Atomic force microscope</td>
</tr>
<tr>
<td>ALD</td>
<td>Atomic layer deposition</td>
</tr>
<tr>
<td>ARC</td>
<td>Antireflecting coating</td>
</tr>
<tr>
<td>a-Si</td>
<td>Amorphous silicon</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar junction transistor</td>
</tr>
<tr>
<td>BOE</td>
<td>Buffered oxide etch</td>
</tr>
<tr>
<td>BOX</td>
<td>Buried oxide</td>
</tr>
<tr>
<td>CCD</td>
<td>Charge-couple-device</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary MOS</td>
</tr>
<tr>
<td>c-Si</td>
<td>Crystalline silicon</td>
</tr>
<tr>
<td>CV</td>
<td>Current voltage</td>
</tr>
<tr>
<td>CZ</td>
<td>Czochralski</td>
</tr>
<tr>
<td>DNA</td>
<td>Deoxyribonucleic acid</td>
</tr>
<tr>
<td>EDX</td>
<td>Energy-dispersive X-ray spectroscopy</td>
</tr>
<tr>
<td>EUV</td>
<td>Extreme ultraviolet</td>
</tr>
<tr>
<td>FE</td>
<td>Field emission</td>
</tr>
<tr>
<td>FIB</td>
<td>Focused ion beam</td>
</tr>
<tr>
<td>FLP</td>
<td>Fermi-level-pinning</td>
</tr>
<tr>
<td>FTIR</td>
<td>Fourier transform infrared spectroscopy</td>
</tr>
<tr>
<td>FSF</td>
<td>Front surface field</td>
</tr>
<tr>
<td>FZ</td>
<td>Floating zone</td>
</tr>
<tr>
<td>HA</td>
<td>Hydrogen annealing</td>
</tr>
<tr>
<td>HF</td>
<td>Hydrogen fluoride</td>
</tr>
<tr>
<td>HSG-IMIT</td>
<td>Hahn-Schickard-Gesellschaft Institut für Mikro- und Informationstechnik</td>
</tr>
</tbody>
</table>
9. List of Abbreviations and Symbols

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>HTT</td>
<td>High temperature treatment</td>
</tr>
<tr>
<td>ICP</td>
<td>Inductively coupled plasma</td>
</tr>
<tr>
<td>IPA</td>
<td>Isopropyl alcohol</td>
</tr>
<tr>
<td>KOH</td>
<td>Potassium hydroxide</td>
</tr>
<tr>
<td>LA</td>
<td>Longitudinal acoustic</td>
</tr>
<tr>
<td>LO</td>
<td>Longitudinal optical</td>
</tr>
<tr>
<td>LPCVD</td>
<td>Low pressure chemical vapor deposition</td>
</tr>
<tr>
<td>NDR</td>
<td>Negative differential resistance</td>
</tr>
<tr>
<td>MBE</td>
<td>Molecular beam epitaxy</td>
</tr>
<tr>
<td>MIGS</td>
<td>Metal induced gap states</td>
</tr>
<tr>
<td>MIS</td>
<td>Metal insulator semiconductor</td>
</tr>
<tr>
<td>MOSCap</td>
<td>MOS capacitance</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-oxide-semiconductor-field-effect-transistor</td>
</tr>
<tr>
<td>OS</td>
<td>Original state</td>
</tr>
<tr>
<td>PCA</td>
<td>Polarizer-compensator-analyzer</td>
</tr>
<tr>
<td>PCSA</td>
<td>Polarizer-compensator-sample-analyzer</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma enhanced chemical vapor deposition</td>
</tr>
<tr>
<td>PMA</td>
<td>Post metal annealing</td>
</tr>
<tr>
<td>PMMA</td>
<td>Polymethyl methacrylate</td>
</tr>
<tr>
<td>POCl</td>
<td>Phosphoryl chloride</td>
</tr>
<tr>
<td>PVCR</td>
<td>Peak-valley-to-current-ratio</td>
</tr>
<tr>
<td>QSSPC</td>
<td>Quasi-steady-state photo conductance</td>
</tr>
<tr>
<td>RCA</td>
<td>Radio Cooperation of America</td>
</tr>
<tr>
<td>RIE</td>
<td>Reactive ion etching</td>
</tr>
<tr>
<td>RTD</td>
<td>Resonant tunneling diode</td>
</tr>
<tr>
<td>RTN</td>
<td>Rapid thermal nitridation</td>
</tr>
<tr>
<td>RTP</td>
<td>Rapid thermal processing</td>
</tr>
<tr>
<td>SB</td>
<td>Schottky-barrier</td>
</tr>
<tr>
<td>SC2</td>
<td>Standard Clean 2</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning electron microscope</td>
</tr>
<tr>
<td>SIS</td>
<td>Superconductor insulator superconductor</td>
</tr>
<tr>
<td>SM</td>
<td>Schottky-Mott</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-noise-ratio</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon on insulator</td>
</tr>
<tr>
<td>TE</td>
<td>Thermal emission</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission electron microscope</td>
</tr>
<tr>
<td>TFE</td>
<td>Thermally assisted field emission</td>
</tr>
<tr>
<td>THz</td>
<td>Terahertz</td>
</tr>
<tr>
<td>TMAH</td>
<td>Tetramethylammonium hydroxide</td>
</tr>
<tr>
<td>TMD</td>
<td>Transition metal dichalcogenide</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>TO</td>
<td>Transverse optical</td>
</tr>
<tr>
<td>UV</td>
<td>Ultraviolet</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very large scale integration</td>
</tr>
<tr>
<td>XPS</td>
<td>X-ray photospectroscopy</td>
</tr>
<tr>
<td>XRR</td>
<td>X-ray reflectivity</td>
</tr>
</tbody>
</table>
9. List of Abbreviations and Symbols

Symbols

\( E_c \)  Conduction band edge
\( E_{CNL} \)  Charge neutrality level
\( E_v \)  Valence band edge
\( D_d \)  Interface density of states
\( E_F \)  Fermi energy
\( \phi_b \)  Electron Schottky-barrier
\( \phi_e \)  Electron-Si\(_3\)N\(_4\)-barrier
\( \phi_{MIGS} \)  MIGS-barrier
\( q \)  Elementary charge
\( \phi \)  Local electrical potential
\( \xi \)  Electrical field
\( V_{bh} \)  Built-in voltage
\( \rho \)  Carrier density
\( N_a \)  Acceptor concentration
\( N_d \)  Donator concentration
\( w_a \)  P-type boundary width
\( w_d \)  N-Type boundary width
\( k \)  Boltzmann constant
\( T \)  Temperature
\( n_i \)  Intrinsic carrier concentration
\( \epsilon_{Si} \)  Dielectric constant of silicon
\( V_f \)  Forward voltage
\( n_i \)  Intrinsic carrier concentration
\( n \)  Ideality factor
\( A \)  Area
\( D_p \)  Diffusion coefficient of holes
\( D_n \)  Diffusion coefficient of electrons
\( L_p \)  Diffusion length of holes
\( L_n \)  Diffusion length of electrons
\( V \)  Voltage
\( V_{BR} \)  Breakdown voltage
\( \phi_{SB} \)  Schottky-barrier
\( E_{vac} \)  Vacuum level
\( W_F \)  Work function
\( \chi_{Si} \)  Electron affinity of silicon
\( W_F^h \)  High work function
\( W_F^l \)  Low work function
\( V_{ds} \)  Drain-source voltage
$e^-$  Electron
$h^+$  Hole
$n_0$  Electron carrier concentration
$p_0$  Hole carrier concentration
$\epsilon_{SiO_2}$  Dielectric constant of silicon dioxide
$E_1$  First eigenenergy
$E_2$  Second eigenenergy
$\gamma^{eff}$  Effective crystalline-dielectric interface energy
$\gamma_{ac}$  Amorphous-crystalline interface energy
$\gamma_{cd}$  Crystalline-dielectric interface energy
$l$  Distance
$l_0$  Characteristic screening length
$V_{gs}$  Gate-source voltage
$S$  Subthreshold slope
$V_{th}$  Threshold voltage
$\mu_n$  Electron carrier mobility
$\mu_p$  Hole carrier mobility
$C_{ox}$  Oxide capacitance
$W$  Width
$L$  Channel length
$V_{dd}$  Drain potential
$V_{ss}$  Source potential
$V_{in}$  Input voltage
$V_{out}$  Output voltage
$P_{dyn}$  Dynamic power losses
$a$  Activity constant
$C$  Capacitance
$f_{clock}$  Clock frequency
$\bar{\rho}$  Complex reflection value
$tan\psi$  Ratio of changed amplitude
$\Delta$  Relative phase shift
$A_0$  Angle of analyzer
$C_0$  Angle of compensator
$P_0$  Angle of polarizer
$\tau_c$  Acquainted complex transmittance
$\delta$  Relative phase
$\psi$  Ratio of changed amplitude
$D_{substrate}$  Dose of the carbon and oxygen contaminant in the substrate material
$D_{material}$  Atomic concentration of the material times the thickness
$\bar{n}$  Complex refractive index
9. List of Abbreviations and Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\omega$</td>
<td>Wave number</td>
</tr>
<tr>
<td>$n(\omega)$</td>
<td>Real value of refractive index at $\omega$</td>
</tr>
<tr>
<td>$i$</td>
<td>Imaginary unit</td>
</tr>
<tr>
<td>$k(\omega)$</td>
<td>Absorption index at $\omega$</td>
</tr>
<tr>
<td>$\alpha(\omega)$</td>
<td>Absorption coefficient at $\omega$</td>
</tr>
<tr>
<td>$N_{X-Y}$</td>
<td>Concentration of the vibrational mode</td>
</tr>
<tr>
<td>$C_{X-Y}$</td>
<td>Proportional factor</td>
</tr>
<tr>
<td>$J_{\text{photocurrent}}$</td>
<td>Photogeneration of carriers</td>
</tr>
<tr>
<td>$P(t)$</td>
<td>Polarization</td>
</tr>
<tr>
<td>$E_{\text{rad}}$</td>
<td>Radiated field</td>
</tr>
<tr>
<td>$\mu_e$</td>
<td>Electron carrier mobility</td>
</tr>
<tr>
<td>$S_A$</td>
<td>Surface of the incident beam</td>
</tr>
<tr>
<td>$z$</td>
<td>Distance between source and sample</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>First crystalline structure</td>
</tr>
<tr>
<td>$\beta$</td>
<td>Second crystalline structure</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>Third crystalline structure</td>
</tr>
<tr>
<td>$E_a$</td>
<td>Activation energy</td>
</tr>
<tr>
<td>$t_{\text{Si}_3\text{N}_4}$</td>
<td>Thickness of silicon nitride</td>
</tr>
<tr>
<td>$L_{\text{NH}_3}$</td>
<td>Diffusion length of ammonia</td>
</tr>
<tr>
<td>$\alpha_n$</td>
<td>Constant of logarithmic growth</td>
</tr>
<tr>
<td>$N_H$</td>
<td>Hydrogen concentration</td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>Flat band voltage</td>
</tr>
<tr>
<td>$P$</td>
<td>Power</td>
</tr>
<tr>
<td>$V(...)$</td>
<td>Etching selectivity</td>
</tr>
<tr>
<td>$V_{100}$</td>
<td>Etching rate of the $&lt;100&gt;$ plane</td>
</tr>
<tr>
<td>$V_{111}$</td>
<td>Etching rate of the $&lt;111&gt;$ plane</td>
</tr>
<tr>
<td>$D$</td>
<td>Distance between evaporation source and sample</td>
</tr>
<tr>
<td>$G$</td>
<td>Gap</td>
</tr>
<tr>
<td>$D_S$</td>
<td>Diameter of the evaporation source</td>
</tr>
<tr>
<td>$A_S$</td>
<td>Aperture size</td>
</tr>
<tr>
<td>$d_o$</td>
<td>Outer diameter</td>
</tr>
<tr>
<td>$d_i$</td>
<td>Inner diameter</td>
</tr>
<tr>
<td>$r_i$</td>
<td>Inner radius</td>
</tr>
<tr>
<td>$r_o$</td>
<td>Outer radius</td>
</tr>
<tr>
<td>$A_o$</td>
<td>Outer contact area</td>
</tr>
<tr>
<td>$A_i$</td>
<td>Inner contact area</td>
</tr>
<tr>
<td>$\phi_{SB}^h$</td>
<td>Sb for holes</td>
</tr>
<tr>
<td>$\phi_{SB}^e$</td>
<td>Sb for electrons</td>
</tr>
<tr>
<td>$I_{ds}$</td>
<td>Drain current</td>
</tr>
<tr>
<td>$R_i$</td>
<td>Contact resistance of the inner area</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
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</tr>
<tr>
<td>$R_o$</td>
<td>Contact resistance of the outer area</td>
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<tr>
<td>$C_{depl}$</td>
<td>Depletion capacitance</td>
</tr>
<tr>
<td>$R_{DS}$</td>
<td>Source-drain resistance</td>
</tr>
<tr>
<td>$k_d$</td>
<td>Exponential constant</td>
</tr>
<tr>
<td>$V_r$</td>
<td>Reverse voltage</td>
</tr>
<tr>
<td>$\Delta E_v$</td>
<td>Energy difference between Fermi level and valence band edge</td>
</tr>
<tr>
<td>$N_v$</td>
<td>Effective density of states</td>
</tr>
<tr>
<td>$G_s$</td>
<td>Conductance of the linear rise of the diode</td>
</tr>
<tr>
<td>$R_s$</td>
<td>Resistance $\frac{1}{\tau_c}$</td>
</tr>
<tr>
<td>$N_{sub}$</td>
<td>Substrate doping concentration</td>
</tr>
<tr>
<td>$g$</td>
<td>Differential conductivity</td>
</tr>
<tr>
<td>$\tau$</td>
<td>Time constant of frequency response for RTD</td>
</tr>
<tr>
<td>$C_{tot}$</td>
<td>Total capacitance</td>
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<tr>
<td>$C_{a-Si}$</td>
<td>Capacitance of the amorphous layer</td>
</tr>
<tr>
<td>$C_{c-Si}$</td>
<td>Capacitance of the nanocrystalline clusters</td>
</tr>
<tr>
<td>$C_{Si_3N_4}$</td>
<td>Capacitance of one silicon nitride layer</td>
</tr>
</tbody>
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Appendices
Appendix A

Fabrication of Bipolarjunction Transistor

![Schottky-Mott bipolar transistor design](image)

**Figure A.1:** The Schottky-Mott bipolar transistor design is illustrated for a PNP (dark letters) and NPN (white letters) configuration. An ultra-thin silicon layer (<20 nm) is nitrided on both sides to enable Schottky-Mott junctions by the selection of either low work function (Er, Mg, Nd, Sc and Al) or high work function materials (Pt, Au, Pd, Co, Ni and Se). The Schottky-Mott junctions either P-type or N-type contacts dominate the ultra-thin silicon layer causing N-type or P-type behavior in the device layer. Ohmic contact formation without high doping concentration inside the silicon layer is achieved. A low background doping concentration of the silicon layer causes less Coulomb scattering and increases the mobility of carriers.

This process continues after the backside etching of the handle wafer of the SOI substrate given in the appendix H.

- Decontamination of the samples: a) 10 min in 60°C HNO$_3$:H$_2$O:1:1, b) 10 min in 60°C HCl:H$_2$O$_2$:H$_2$O:1:1:1 (attention boiling!!!)

- Thinning of the LPCVD-silicon nitride after backside groove etching down to 10-20 nm, either with a) 165°C hot H$_3$PO$_4$ acid, etching rate ~2-4 nm/min
A. Fabrication of Bipolarjunction Transistor

(depending on amount of samples), b) \( \text{SF}_6 = 8 \text{ sccm}, \quad \text{O}_2 = 4 \text{ sccm}, \quad P = 13 \text{ mTorr} \)  
\((2.5 \times 10^{-2} \text{ mbar}), \quad P_{\text{in}} = 55 \text{ W}, \quad P_{\text{refl}} = 1 \text{ W}, \quad V_{\text{bias}} = -160 \text{ V}, \quad \text{etching rate} \ 20-24 \text{ nm/min}

- RCA clean after thinning, 10 min in acetone, 10 min in IPA, 10 min in H\(_2\)SO\(_4\):H\(_2\)O\(_2\), 10 min in NH\(_4\):H\(_2\)O\(_2\):H\(_2\)O, 10 min in HCl:H\(_2\)O\(_2\):H\(_2\)O

- PMMA double layer spin coating: 1st) 50k PMMA at 5000 rpm, 2nd) 200k PMMA at 4000 rpm, soft bake after each run for 1min at 180°C

- Ebeam parameter: 30 kV, 330 \( \mu \text{C/cm}^2 \), rectangular grooves

- Development: 1 min slowly rotating (0.5 rpm) the sample holder, 1 min stopping with DI-water

- \( \text{SF}_6 = 8 \text{ sccm}, \quad \text{O}_2 = 4 \text{ sccm}, \quad P = 13 \text{ mTorr} \)  
\((25 \mu \text{bar}), \quad P_{\text{in}} = 55 \text{ W}, \quad P_{\text{refl}} = 1 \text{ W}, \quad V_{\text{bias}} = -160 \text{ V}, \quad \text{etching rate} \ 20-24 \text{ nm/min}, \quad \text{duration approximately} \ 30 \text{ s up to} \ 2 \text{ min depending on the silicon nitride thickness}

- PMMA is removed in 10 min acetone and subsequently 10 min IPA

- TMAH\/IPA (9:1) etching of the opened silicon surface, at 60°C 1-2min, etching rate of silicon ~1.5 nm

- Removing of silicon nitride in 165°C hot H\(_3\)PO\(_4\) acid, etching rate ~2-4 nm/min (depends on amount of samples)

- HSQ spin coating at 4000 rpm, soft bake at 165°C for 5 min

- Ebeam parameter: 10 kV, 180 \( \mu \text{C/cm}^2 \), MESA pattern through the rectangular grooves.

- Development: 1min in TMAH, stopping in DI-water (1 min of rinsing)

- HSQ-Hardening for wet chemical etching: Hotplate, 1 h at 300°C or 15 min in Ar atmosphere at 550°C (RTP).

- MESA etching with TMAH\/IPA (9:1) at 60°C for 2min, prior to MESA etching: Native oxide removal step by 5s in 1% HF

- Removing of HSQ with 1% HF, 2 min.

- PMMA double layer spin coating: 1st) 50k PMMA at 5000 rpm, 2nd) 200k PMMA at 4000 rpm, soft bake after each run for 1 min at 180°C

- Ebeam parameter: 30 kV, 330 \( \mu \text{C/cm}^2 \), opening small windows to completely remove the oxide on the backside

- Development: 1 min slowly rotating (0.5 rpm) the sample holder, 1min stopping with DI-water

- Buffered oxide etch (BOE): DI-Water (1:9), 5 min
• RCA clean after opening the SOI from the backside, 10 min in acetone, 10 min in IPA, 10 min in H₂SO₄:H₂O₂, 10 min in NH₄OH:H₂O₂:H₂O, 10 min in HCl:H₂O₂:H₂O.

• Nitridation at 450 °C in NH₃\Ar atmosphere (300 sccm\1000 sccm) for at least 60 s.
Figure A.2: Lasermicroscope image of a silicon-oxide-patterned SOI membrane, the membrane window has a lateral size of approximately $110 \mu m$. The star shape offers a stabilization of the buried oxide layer. The BOX layer breaks once the top-silicon layer is removed. The huge stress inside the oxide layer is observed by the strong birefringence.
Appendix B

Verification of Si$_3$N$_4$ Thicknesses via various Ellipsometry Tools

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Y$_1$</td>
<td>2.1± 0.05</td>
<td>2.12±0.05</td>
<td>2.1±0.1</td>
</tr>
<tr>
<td>Y$_2$</td>
<td>2.12± 0.03</td>
<td>2.12±0.01</td>
<td>2.1±0.1</td>
</tr>
<tr>
<td>Y$_3$</td>
<td>1.88± 0.025</td>
<td>1.96±0.01</td>
<td>2±0.1</td>
</tr>
<tr>
<td>Y$_4$</td>
<td>1.87± 0.01</td>
<td>1.97±0.01</td>
<td>1.9±0.1</td>
</tr>
<tr>
<td>Y$_6$</td>
<td>1.95± 0.05</td>
<td>2.01±0.01</td>
<td>2±0.1</td>
</tr>
</tbody>
</table>

Table B.1: Two various nitridation runs were investigated: 950°C for 20 min (Y$_1$ and Y$_2$), and 60 s (Y$_3$-Y$_6$), the thickness was determined at three complete different ellipsometry measurement units demonstrating the excellent and highly accurate examination of ultra thin silicon nitride layers; J.A. Woollam was provided by IMS of TU Dortmund, Sentech SE800 was provided by JAülich Forschungszentrum.
Appendix C

Approval of a Silicon Nitride Membrane by EDX

<table>
<thead>
<tr>
<th></th>
<th>K percent by weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.739 99.11</td>
</tr>
<tr>
<td>N</td>
<td>0.392 0.89</td>
</tr>
</tbody>
</table>

Table C.1: EDX results of the silicon nitride membrane shown in Figure C.1 are demonstrated, K-alpha emission lines of silicon and nitrogen listed.

Volume of nitrogen of the corresponding area is expressed as follows:

\[ V_N = \left( 2 \cdot ((Z)^2 - (A - \text{undercut})^2) \cdot (t_{Si_3N_4}) \right)^{\frac{4}{7}}, \quad (C.1) \]

where \( Z, A, \text{undercut} \) and \( t_{Si_3N_4} \) are the elements depicted in figure C.1 and the thickness of the silicon nitride layer. Volume of silicon is given by:

\[ V_{Si} = (Z^2 - \frac{1}{3}(A^2 + A \cdot a + a^2)) \cdot h + V_N \cdot \frac{3}{4}, \quad (C.2) \]

where \( a \) is illustrated in figure C.1 and \( h \) is the SOI thickness.

The ratio of both volumes is determined by:

\[ \text{ratio} = \frac{V_{Si}}{V_N}. \quad (C.3) \]
Figure C.1: Silicon nitride membrane and the corresponding elements are demonstrated: 
Z is the window of the EDX scan region, A is the width (length) of the 
groove at the top surface and a is the width (length) of the free-standing 
silicon nitride membrane
Appendix D

Process of $<111>$ nitrided suspended Silicon Wires

- HSQ spin coating at 4000 rpm, softbake at 165°C for 5 min
- Ebeam parameter: 10 kV, 180 $\mu$C/cm$^2$, MESA pattern
- Development: 1 min in TMAH, stopping in DI-water (1min of rinsing)
- HSQ-Hardening for wet chemical etching: Hotplate for 1h at 300°C or 15min in Ar atmosphere at 550°C (RTP)
- MESA etching with TMAH/IPA (9:1) at 60°C for 2min, prior to MESA etching native oxide is removed by 5s in 1% HF
- Removing of HSQ with 1% HF, 2 min
- RCA clean, 10 min in acetone, 10 min in IPA, 10 min in H$_2$SO$_4$:H$_2$O$_2$, 10 min in NH$_4$OH:H$_2$O$_2$:H$_2$O, 10 min in HCl:H$_2$O$_2$:H$_2$O
- Nitridation at 1100°C for 5 min in NH$_3$:Ar atmosphere (300 sccm):1000 sccm)
- HSQ spin coating at 4000 rpm, softbake at 165°C for 5 min
- Ebeam parameter: 10 kV, 180 $\mu$C/cm$^2$, capping of silicon nitride surface by a HSQ layer
- Development: 1 min in TMAH, stopping in DI-water (1 min of rinsing)
- HSQ-Hardening for wet chemical etching: Hotplate for 1h at 300°C or 15 min in Ar atmosphere at 550°C (RTP)
- Removing of HSQ and the BOX underneath the device layer with 1% HF, 2 min
Appendix E

Fabrication of Silicon Nitride Tunneling Solar Cells

E.1 Standard Silicon Solar Cell

- 4in wafer 10 min in acetone, 10 min in IPA, 10 min in H₂SO₄:H₂O₂, 10 min in NH₄OH:H₂O₂:H₂O, 10 min in HCl:H₂O₂:H₂O
- POCl-doping at 875°C, approximately 0.85 µm thick phosphorus doped emitter, 8·10¹⁸ cm⁻³ doping concentration
- Removing of the glass on the surface of the substrate by buffered oxide etch (BOE): DI-Water (1:9), 5 min
- 4in wafer 10 min in acetone, 10 min in IPA, 10 min in H₂SO₄:H₂O₂, 10 min in NH₄OH:H₂O₂:H₂O, 10 min in HCl:H₂O₂:H₂O
- 4in wafer is nitrided at 450°C at least for 5 min in NH₃\Ar atmosphere (300 sccm\1000 sccm)
- Take new carrier wafers (or your own) for the hotplate, cap the chuck of the mask aligner with dicing tape, decontaminate the beakers, wafer holder and tweezer for development (appendix H)
- Pre bake out at 120°C for at least 5 min
- AZ5214E (no Ti-primer!!!) at 3500 rpm, softbake: 1 min 30 s at 95°C
- 405 nm (15 mW\cm²) for 3 s (front aluminum layer), image reverse bake: 2 min at 110°C
- Flood exposure: 10 s at 405 nm (15 mW\cm²)
- developing in AZ726MIF for 35 s (moving wafer holder)
- Gold evaporation of the backside
E. Fabrication of Silicon Nitride Tunneling Solar Cells

- Turn around the wafer for aluminum front side evaporation
- Decontaminate lift-off beakers, tweezer and wafer holder prior to the lift-off procedure
- At least 4 hours of lift-off in Dimethyl sulfoxide (front side of the solar cell is upside down to reduce particle contamination on the front side, beaker is sealed by a parafilm to reduce further particle emission), recommendation: approximately 12 hours, no ultrasonic cleaning!!!

E.2 Silicon Nitride based MIS-Solar Cell

- 4 in wafer 10 min in acetone, 10 min in IPA, 10 min in H$_2$SO$_4$-H$_2$O$_2$, 10 min in NH$_4$OH-H$_2$O$_2$:H$_2$O, 10 min in HCl-H$_2$O$_2$:H$_2$O
- 4 in wafer is nitrided at 450°C at least for 5 min in NH$_3$\Ar atmosphere (300 sccm\1000 sccm)
- Take new carrier wafers (or your own) for the hotplate, cap the chuck of the mask aligner with dicing tape, decontaminate the beakers, wafer holder and tweezer for development (appendix H)
- Pre bake out at 120°C for at least 5 min
- AZ5214E (no Ti-primer!!!) at 3500 rpm, softbake: 1 min 30 s at 95°C
- 405 nm (15 mW\cm$^2$) for 3 s (front aluminum layer), image reverse bake: 2 min at 110°C
- Flood exposure: 10 s at 405 nm (15mW\cm$^2$)
- developing in AZ726MIF for 35 s (moving wafer holder)
- Gold evaporation of the backside
- Turn around the wafer for aluminum front side evaporation
- Decontaminate lift-off beakers, tweezer and wafer holder prior to the lift-off procedure
- At least 4 hours of lift-off in Dimethyl sulfoxide (front side of the solar cell is upside down to reduce particle contamination on the front side, beaker is sealed by a parafilm to reduce further particle emission), recommendation: approximately 12 hours, no ultrasonic cleaning!!!
Appendix F

Fabrication of PSEUDO MOSFETs

F.0.1 N-type MOSFET

- RCA cleaning of SOI samples, 10 min in acetone, 10 min in IPA, 10 min in H₂SO₄:H₂O₂, 10 min in NH₄OH:H₂O₂:H₂O, 10 min in HCl:H₂O₂:H₂O
- Pre bake out at 120°C for at least 5 min
- AZ5214E (!!! no Ti-primer!!!) at 3500 rpm, softbake: 1 min 30 s at 95°C
- 405 nm (15 mW\m²) for 6 s (Mesa pattern).
- Developing in AZ726MIF for 50 s (moving sample holder)
- SF₆ = 30 sccm, O₂ = 4.6 sccm, P = 20 mTorr, Pₐₖ = 55 W, Pₐₑᵣₜ = 1 W, V_{bias} = -160 V, etching rate approximately 50 nm/min, 200 nm SOI results into 4 min of etching
- RCA cleaning of SOI samples, 10 min in acetone, 10 min in IPA, 10 min in H₂SO₄:H₂O₂, 10 min in NH₄OH:H₂O₂:H₂O, 10 min in HCl:H₂O₂:H₂O
- Nitridation at the 450°C at least for 60 s in NH₃\Ar atmosphere (300 sccm\1000 sccm)
- Take new carrier wafers (or your own) for the hotplate, cap the chuck of the mask aligner with dicing tape, decontaminate the beakers, wafer holder and tweezers for development (appendix H)
- Pre bake out at 120°C for at least 5 min
- AZ5214E (!!! no Ti-primer!!!) at 3500 rpm, softbake: 1 min 30 s at 95°C
- 405 nm (15 mW\m²) for 3 s (front metal layer), image reverse bake: 2 min at 110°C
- Flood exposure: 10 s at 405 nm (15 mW\m²)
F. Fabrication of PSEUDO MOSFETs

- Develop in AZ726MIF for 35 s (moving sample holder)
- Evaporation of metal on the front surface
- Decontaminate lift-off beakers, tweezer and wafer holder prior to the lift-off procedure
- At least 4 hours of Lift-off in dimethyl sulfoxide (beaker is sealed by a parafilm to reduce further the particle emission), recommendation: approximately 12 hours, no ultrasonic cleaning
- Safety resist spincoating for the frontside for backside metallization
- Pre bake out at 120 °C for at least 5 min
- AZ520D (no Ti-primer) at 3500 rpm, softbake: 2 min at 110 °C
- 1 % HF Dip approximately 10 s prior to mounting of the sample into the evaporation chamber
- Decontaminate resist removal beakers, tweezer and wafer holder prior to the lift-off procedure (rudimentary removal step of resist just by acetone and IPA wash bottles, less particles)

F.0.2 P-type MOSFET

- RCA cleaning of SOI samples, 10 min in acetone, 10 min in IPA, 10 min in H₂SO₄:H₂O₂, 10 min in NH₄OH:H₂O₂:H₂O, 10 min in HCl:H₂O₂:H₂O
- Nitridation at the 450 °C at least for 60 s in NH₃\Ar atmosphere (300 sccm\1000 sccm)
- Take new carrier wafers (or your own) for the hotplate, cap the chuck of the mask aligner with dicing tape, decontaminate the beakers, wafer holder and tweezer for development (appendix H)
- Pre bake out at 120 °C for at least 5 min
- AZ5214E (no Ti-primer!!!) at 3500 rpm, softbake: 1 min 30 s at 95 °C
- 405 nm (15 mW\cm²) for 3 s (front metal layer), image reverse bake: 2 min at 110 °C
- Flood exposure: 10 s at 405 nm (15 mW\cm²)
- Developing in AZ726MIF for 35 s (moving wafer holder)
- Evaporation of metal
- Decontaminate lift-off beakers, tweezer and wafer holder prior to the lift-off procedure

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• At least 4 hours of Lift-off in dimethyl sulfoxide (beaker is sealed by a parafilm to reduce further particle emission), recommendation: approximately 12 hours, no ultrasonic cleaning!!!

• Take new carrier wafers (or your own) for the hotplate, cap the chuck of the mask aligner with dicing tape, decontaminate the beakers, wafer holder and tweezer for development (appendix H)

• Pre bake out at 120°C for at least 5min

• AZ5214E (!!! no Ti-primer!!!) at 3500 rpm, softbake: 1 min 30 s at 95°C

• 405 nm (15 mW/cm²) for 6 s (Mesa pattern)

• developing in AZ726MIF for 50 s (moving sample holder)

• SF₆ = 30 sccm, O₂ = 4.6 sccm, P = 20 mTorr, P₁ = 55 W, P₂ = 1 W, V_{bias} = -160 V, etching rate approximately 50 nm/min, 200 nm SOI results into 4 min of etching

• Decontaminate resist removal beakers, tweezer and wafer holder for metal contaminated samples

• 10 min in acetone and 10 min in IPA for resist removal

• Safety resist spincoating for the frontside for backside metallization

• Pre bake out at 120°C for at least 5min

• AZ520D (!!! no Ti-primer!!!) at 3500 rpm, softbake: 2 min at 110°C

• 1 % HF Dip approximately 10 s prior to mounting of the sample into the evaporation chamber

• Decontaminate resist removal beakers, tweezer and wafer holder prior to the lift-off procedure (rudimentary removal step of resist just by acetone and IPA wash bottles, less particles)
Appendix G

Beaker-KOH Etching-Issues

• Thermal gradient from the center of the beaker to the outer shell can be minimized if the beaker is shielded to the ambient by a thick thermal insulator, for instance, several aluminum foils.

• The etching temperature of 96°C causes a huge amount of water evaporation. A burette ensures a constant water level.

• Stirring causes a second gradient due to a constant angular velocity. Samples need to be repositioned after 30 minutes to ensure a homogenous etching over the entire batch.

• The sample holder has an impact on the etching rate of the grooves. Hence, the samples have to be rotated to reduce the inhomogeneous etching.

• The sample holder needs to be aligned to the center part of the magnetic stirrer to avoid an asymmetric etching.
Appendix H

Cleaning Procedure for
Decontamination of Equipment

- Tweezers and sampler holders have to be put into the beakers. During the procedure the entire equipment has to be immersed by the acids.

- 10 min in 60°C hot HNO₃:H₂O:1:1

- 10 min of rinsing in DI-water, the heads of the tweezer and sample holder should be cleaned with water too.

- 10 min in 60°C HCl:H₂O₂:H₂O:1:1:1 (!!!attention boiling!!)

- 10 min of rinsing in DI-water, the heads of the tweezer and sample holder should be cleaned with water too.

- These recipe is not tackling noble contaminants as gold or platinum, here, an aqua regia mixture is a more promising wet chemical composition.
Appendix I

Microstencil Process

- RCA cleaning of 6in wafers prior to silicon nitride deposition, 10 min in acetone, 10 min in IPA, 10 min in H₂SO₄:H₂O₂, 10 min in NH₄OH:H₂O₂:H₂O, 10 min in HCl:H₂O₂:H₂O
- Deposition of a KOH-hardmask silicon nitride layer (LPCVD silicon nitride was deposited by HSG-IMIT) on all surfaces of the substrate
- Pre bake out at 120 °C for at least 5 min
- Spin coating of AZ15nxt at 7000 rpm
- Soft bake at 110 °C for 3 min
- 405 nm (15 mW/cm²) for 26.67 s (windows of the grooves)
- Post exposure bake at 120 °C for 1 min
- Develop in AZ726MIF for 40 s (move the sample holder)
- Etching of the silicon nitride either by a) 165 °C hot H₃PO₄ acid, etching rate ~2-4 nm/min (depending on amount of the samples, AZ15nxt is hardened associated to the high temperature) or b) SF₆ = 8 sccm O₂ = 4 sccm, P=13 mTorr (2.5*10⁻² mbar), P_in=55 W, P_ref=1 W, V_bias=-160 V, etching rate 20-24 nm/min
- 1 % HF Dip approximately 10 s prior to KOH etching.
- KOH (26.7 %, 88 g KOH pellets are solved in 200 ml DI-water) etching at 96 °C, approximately 4 hours (resist do not need to be removed prior KOH etching)
- Recommendation: Each half hour repositioning of samples in the sample holder to improve the homogenous etching and for etching depth control
- Decontamination by the following recipe given in appendix H
- Silicon nitride removal step by wet chemical etching: 165 °C hot H₃PO₄ acid, etching rate ~2-4 nm/min
Appendix J

SEM Impact on 1.7 nm thick Ultra Thin Si$_3$N$_4$ Membranes

Figure J.1: Silicon nitride membrane demonstrated which is blasted by the huge ebeam current, 30µm aperture.
Figure J.2: Top view SEM image of the silicon nitride membrane is depicted showing two carbon contamination dots produced intentionally by the beam current of the SEM, silicon nitride membrane thickness 1.7 nm.
Appendix K

FTIR Spectrum of a high-quality grown Si$_3$N$_4$ Hard Mask

\begin{figure}
\centering
\includegraphics[width=0.8\textwidth]{ftir_spectrum.png}
\caption{FTIR spectrum of the 210 nm thick HSG-IMIT-LPCVD silicon nitride layer is depicted, Si-N stretching mode at 845 cm$^{-1}$, small amount of oxygen is present at 1105 cm$^{-1}$.}
\end{figure}
Appendix L

Reflectance Measurement of an Aluminum Halo Capping

Figure L.1: Reflectance measurements of various halo thicknesses are shown: Conventional polished surface (reference); 2 nm, 3 nm and 4 nm halo aluminum layer.
Appendix M

Current-Voltage Characteristics of Resonant Tunneling Diodes

Figure M.1: IV characteristics of 4 various samples are demonstrated: a) Current-voltage characteristic of 4 various samples, b) semilogarithmic scale of the IV curves given in a).
Appendix N

Growth of amorphous Silicon Layer

- 1% HF Dip approximately 10 s prior to mounting into the PECVD chamber (4-inch silicon wafer)
- Nitridation, 1 min, RF power 30 W, ICP 100 W, 100 mTorr at 280 °C
- Deposition of amorphous silicon, 3-5 min, RF power 30 W, ICP 100 W, 100 mTorr
- Nitridation, 1 min, RF power 30 W, ICP 100 W, 100 mTorr at 280 °C
Appendix O

Acknowledgement

I would like to express my deepest gratitude to Professor Joachim Knoch for his support, the chance to work in a highly-flexible cleanroom environment and the opportunity to gain a multitude of cleanroom experiences. He offered always a sympathetic ear and gave very helpful suggestions to manage this Ph.D. thesis. Furthermore, I would like to thank professor Andrei Vescan being my assessor for this Ph.D. thesis. His critical examination was a huge contribution to this work. Also, my great appreciation goes to Gia Vinh Luong for his very beneficial help at the Forschungszentrum Juelich. Moreover, I would like to thank all colleagues of the institute of semiconductor electronics: Starting with Birgit Hadam for the endless evaporation runs and electron beam lithography work, Horst Windgassen with his wide solar cell experience managing MIS-solar cells with silicon nitride, Gerd Esser for his good and quick advices when dealing with the Rapid Thermal Processing machine.

Furthermore, I am very grateful for the support of the IWE2 institute, especially, Sergej Starschich for the X-ray reflectivity measurements and Ms. Gisela Wasse for the EDX measurements proving the existence of nitrogen in the ultra thin silicon nitride membranes. Moreover, I would like to thank Dr. Klaus Kallis and the intelligent Microsystems institute for the access to the ellipsometry at the technical university of Dortmund verifying once more silicon nitride thicknesses below one nanometer.

In addition, it was a great pleasure working with Hauke Ingolf Kremer spending a lot of time to understand the impact of the silicon nitride in the ohmic tunneling junctions, also, Mehrnoosh Mazhar Sarmadi for her perseverance measuring hundreds of Schottky-Mott junctions. Finally, I would like to thank the colleagues which I have been daily in contact, Noel Wilck for the support in the cleanroom and the fruitful discussions; Felix Riederer, Thomas Grap and Tobias Finge for the exciting and joint time.

Last but not the least, I would like to thank my wife for supporting me in this eventful time.
Appendix P

Curriculum Vitae

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