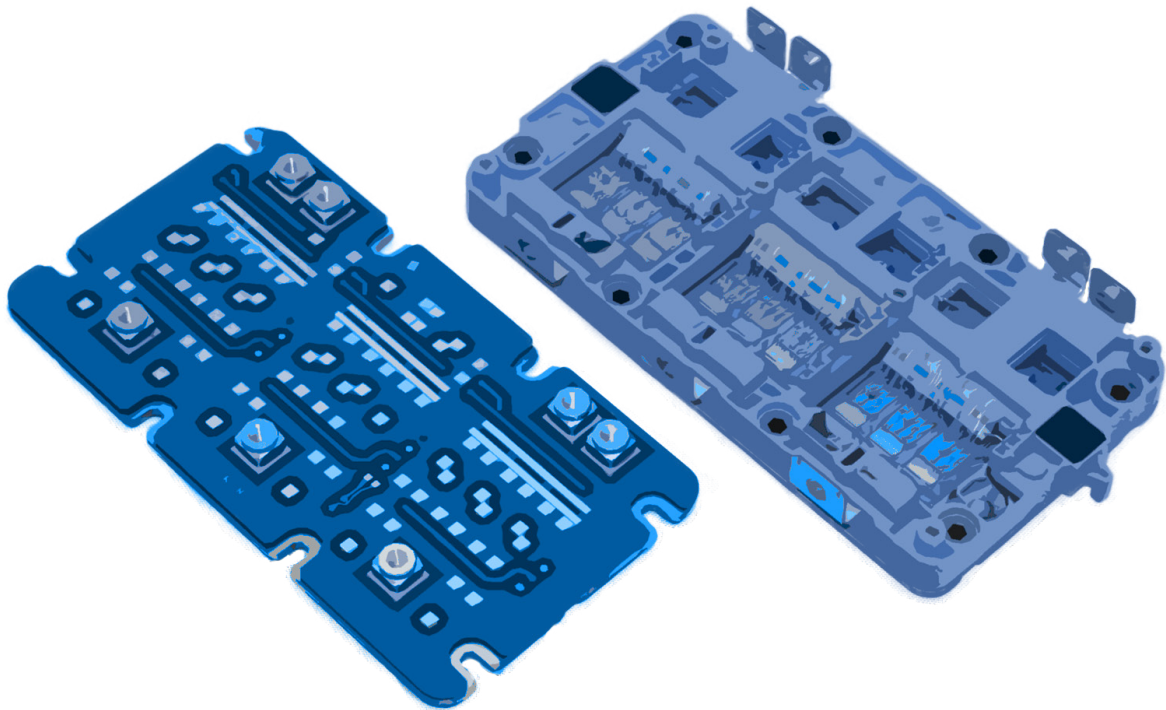


Christoph Neeb

Packaging Technologies for Power Electronics in Automotive Applications



Packaging Technologies for Power Electronics in Automotive Applications

Von der Fakultät für Elektrotechnik und Informationstechnik
der Rheinisch-Westfälischen Technischen Hochschule Aachen
zur Erlangung des akademischen Grades eines Doktors der
Ingenieurwissenschaften genehmigte Dissertation

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Vorwort

In den Jahren 2010 bis 2014 war ich am Institut für Stromrichtertechnik und Elektrische Antriebe (ISEA) der RWTH Aachen als wissenschaftlicher Mitarbeiter beschäftigt. Die im Rahmen der Projekte e performance und HI-LEVEL entstandenen Leistungsmodule mit alternativer Aufbau- und Verbindungstechnik bilden die Grundlage dieser Arbeit.

Ich bedanke mich herzlich bei meinem Doktorvater und Institutsleiter Prof. Dr. Doncker für das entgegengebrachte Vertrauen sowie die gewährten Freiheiten bei meinen Tätigkeiten im Bereich Aufbau- und Verbindungstechnik und für die Betreuung dieser Arbeit. Prof. Knoch danke ich für die freundliche Übernahme des Koreferats.

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Haan im Februar 2018

Christoph Neeb

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1 Introduction

At the beginning of the 20th century, mass mobility with automobiles started in North America. Until the second world war almost 50 million cars were registered. Today, an exponential growth led to an estimated number of registered cars worldwide of around one billion [1][2] with 90 million new cars sold per year [3]. It is to be expected that this strong rate of growth will continue as people living in large emerging markets, e.g. China, India and Brazil, seek for individual freedom and mobility.

The increasing number of automobiles causes serious problems for environment and human health. Combustion engines of conventional cars significantly contribute to the rising CO₂-concentration in the atmosphere. In Germany the share of the transport sector in the total CO₂-emissions was 18 % in 2014 of which 95 % were caused by road traffic [4]. Moreover, the combustion process is never complete and clean so that many additional pollutants are generated. The expected climate warming and health issues are discussed extensively in public during the last years.

Fossil fuels are rapidly depleted by the large demand from power plants and engines which led to a significant price increase of crude oil since the 1970s (Fig. 1.1). After the worldwide financial crisis in 2008 and by the exploitation of new gas fields, e.g. by fracking, after 2014 this development was stopped for the time being [5]. However, it is expected that there will be a shortage of petroleum resources in the near future even though it is not possible to exactly forecast peak oil [1]. Both environmental and economical aspects demand for alternative drive mechanisms for mass mobility. In the 1970s the development of such alternatives started leading to the introduction of cars powered with greener fuels, such as liquid petrol gas and natural gas.

The impact of emissions from automobiles on the human health became a subject of public discussions in the USA during the 1970s. The outcome were strict emission laws that forced the vehicle manufacturer to develop techniques for cleaner exhaust gases where the state of California led the way. In fact, California issued a regulation for zero emission vehicles (ZEV) that established a local electric vehicle boom during 1996-2003. In 2003, the ZEV-regulations were replaced by a partial zero emission vehicle (PZEV) standard that also allowed hybrid electric vehicles (HEV). Toyota that already had introduced the Prius in 1997 highly benefited from this and dominated the HEV market for a long time.

The trend towards electromobility, initiated by the short Californian electric vehicle boom and placed on a broad basis by HEV from Toyota and also Honda, spread to Europe when the EU Commission started to regulate the CO₂-emissions of automobiles in 1995. Since then, more and more activities on developing EV and

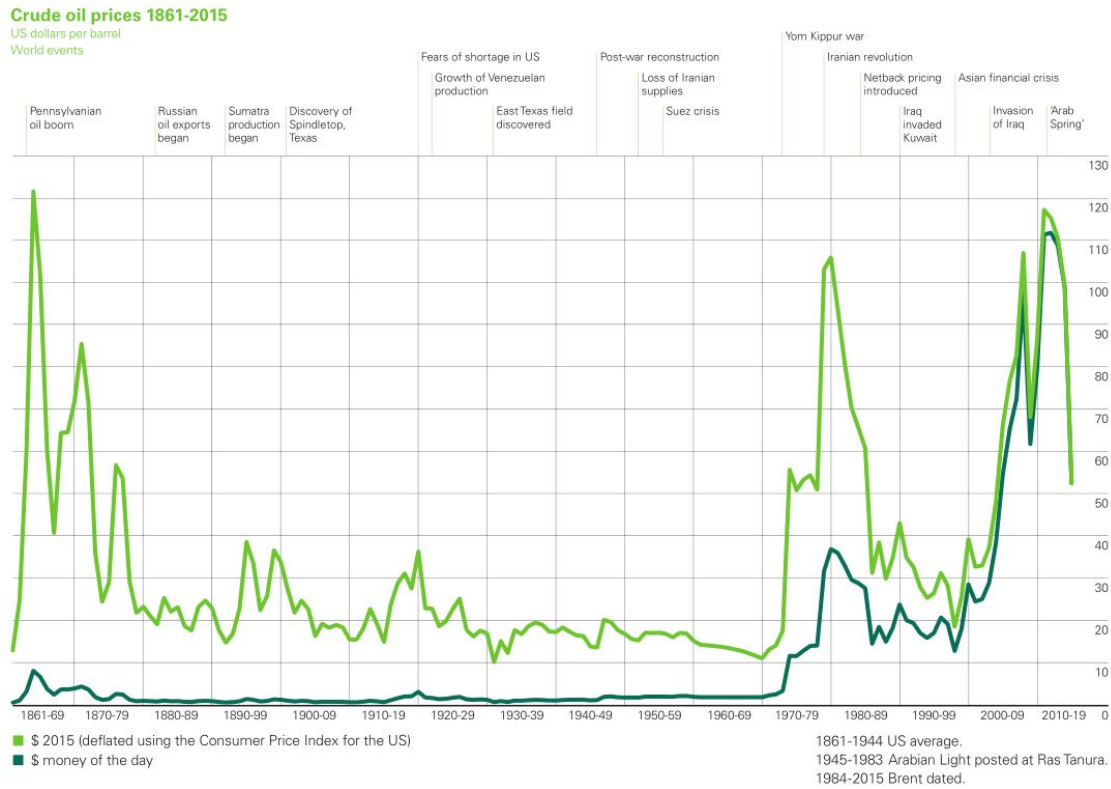


Figure 1.1: Oil price from 1861 to 2015, from [5]

HEV are ongoing. HEV combine combustion engine and electric motor and optimize the load sharing. Additionally, auxiliary power units are driven electrically. By this, HEV and plug-in HEV (PHEV) are currently the most fuel-efficient cars.

Electrical loads in automotive systems initially evolved from lighting and battery charging towards infotainment, sensors and safety. All these loads can be supplied from the 12 V voltage level. In modern HEV auxiliary power units, such as generator/starter, electric climate compressor, electric roll stabilization, steer-by-wire, electric pumps, etc, have an electrical demand in the kW range. This makes the 12 V voltage level too low due to the high currents that would flow. Therefore, the 48 V voltage level was introduced. For HEV with a strong electric traction motor and, of course, for pure electric vehicles this voltage level would require again current levels well above 500 A. Instead, these types of vehicles are usually built with battery systems up to around 400 V. Recently, Porsche announced to introduce 350 kW chargers at 800 V to significantly decrease the charging time of EV [6].

The ongoing electrification of more and more power units in a rising number of automobiles comes along with a higher demand for power electronics. Power electronics is necessary to convert electric energy from one form into another with the means of power semiconductor switches. In an EV or HEV this comprises the conversion from AC to DC (e.g. on-board charger), from DC to DC (e.g. transfer of energy from one voltage level to another) and from DC to AC (e.g. power

an electric motor from the battery). At power ratings of several kW and higher, semiconductor switches packaged in power modules are predominantly used. In particular, MOSFET (metal-oxide-semiconductor field-effect transistor) and IGBT (insulated gate bipolar transistor) are the preferred types of power semiconductors. For low voltages MOSFETs are advantageous due to their low on-resistance and fast switching characteristics. Above some hundreds of volts IGBTs are usually used because they can realize high blocking capability while maintaining comparatively good conduction performance.

Power modules were originally developed for industrial applications. However, in the automotive sector the environmental conditions, size and weight requirements are much more severe. Vibration, dust, humidity, extreme absolute temperatures and large temperature cycles are challenging factors affecting the reliability of power modules for automotive applications. Moreover, limited space within the HEV engine compartment and, consequently, size reduction of all components leads to an increasing power density, which finally results in even higher temperatures.

The reliability requirements that arouse from automotive environmental conditions cannot be fulfilled with the standard packaging technologies of industrial power modules. Hence, alternative solutions have to be found for building reliable power modules for automotive applications.

1.1 Objective of the work

The trend towards electromobility is forcing automobile manufacturers as well as suppliers of power modules to develop new packaging technologies to fulfill the increased reliability, space and low-weight requirements. A variety of approaches is under development and testing, but until now there is no standard automotive power module concept. This work focuses on two of these approaches of which one is the use of high-current printed circuit boards (PCB) as an embedding platform for power semiconductor chips. Chip embedding technologies are well-established in low power applications and are approaching a maturity level that makes them a possible candidate for automotive power electronics. The second approach is the press-pack technology that has been used for many years in high-power applications. The superior reliability of its form-locking chip contact is a promising property to meet the automotive requirements.

A press-pack power module and several versions of PCB based power modules are investigated and compared to a state-of-the-art power module in multiple domains to evaluate the suitability of the new power module concepts for automotive applications. Prototypes of some of the power modules were available for measurements to create a database for the comparison and to validate simulation results. Special focus is on the use of the RC-IGBT (reverse-conducting-IGBT) within the different types of power modules. This new device offers some advantages compared to a standard IGBT and it is elaborated to what extent the different packaging technologies can make use of these advantages.

1.2 Outline

This section gives an overview of the individual chapters.

Chapter 2: Fundamentals

The understanding of power electronics packaging requires a fundamental knowledge about heat transfer mechanism. Besides this, two common models for reliability calculations are introduced, as well as the RC-IGBT. Finally, the influence of parasitics in power modules on the transient behavior of power semiconductors is explained.

Chapter 3: Power Electronics Packaging

Chapter 3 gives an overview of the main well-established packaging technologies. The evolution of power modules from the first power module to the state-of-the-art is outlined together with its impact on the lifetime of power modules. The chapter continues with a review of chip embedding technologies which are new in the field of power electronics. It concludes with the requirements in automotive applications that are relevant for power electronics packaging.

Chapter 4: Power Module Concepts for Automotive Applications

This chapter starts with a presentation of the power module concepts that are investigated in this work. The thermal behavior of these concepts is studied by simulations. Prototypes of three of the module concepts allow to verify the simulation results by thermal impedance measurements. A main goal of using chip embedding technologies for power modules is to realize a very low dc-link stray inductance. During the design phase of the prototype this was addressed by electrical simulation and optimization of the geometry. The electrical behavior of the available module prototypes is characterized in detail by doing extensive double pulse tests and measuring the EMC performance.

Chapter 5: System Level Implications

The thermal and electrical characteristics of the module concepts that were obtained in chapter 4 are used for a comparison on system level. Two typical topologies of automotive converters are simulated to examine the respective transient junction temperature characteristics and to deduce the maximum power density that can be achieved with each module concept. Special focus is on the discussion of the benefits when using RC-IGBT against the conventional configuration with separated IGBT and diode chips.

2 Fundamentals

2.1 Heat transfer

Heat transfer describes the exchange of thermal energy between physical systems. The thermal energy is transported in form of a heat flow from a region of high temperature to another region of lower temperature. The three fundamental mechanisms of heat transfer are conduction, convection and radiation.

2.1.1 Conduction

Heat transfer by conduction is the transportation of energy from particles with a higher energy to particles of less energy by vibrating against one another. In solids, conduction is the most dominant mechanism of heat transfer. In steady-state, conduction is described by Fourier's law which is the analogue of the Ohm's law in electricity. Fourier's law in integral form is

$$\dot{Q}_{\text{cond}} = -\lambda \cdot \oint_S \nabla T \cdot \vec{dA} \quad (2.1)$$

where

$\dot{Q}_{\text{cond}}$ = amount of heat transferred per unit time in W
 λ = materials thermal conductivity in W/mK
 ∇T = temperature gradient in K/m
 $\vec{dA}$ = oriented surface area element in m²

Integrating the above differential equation, gives the heat flow for a 1-D geometry as depicted in Fig. 2.1

$$\dot{Q}_{\text{cond}} = -\lambda \cdot A \cdot \frac{\Delta T}{\Delta x} \quad (2.2)$$

where

A = cross-sectional surface area in m²
 $\Delta T = T_1 - T_2$ temperature difference between the ends in K
 Δx = distance between the ends in m

When the temperature of an object changes as a function of time, Fourier's law is not valid anymore. The analysis of such systems is more complex and is usually done with FEM (finite element method) simulation tools. The heat transfer from chip to heat sink in a power module is a conductive effect.

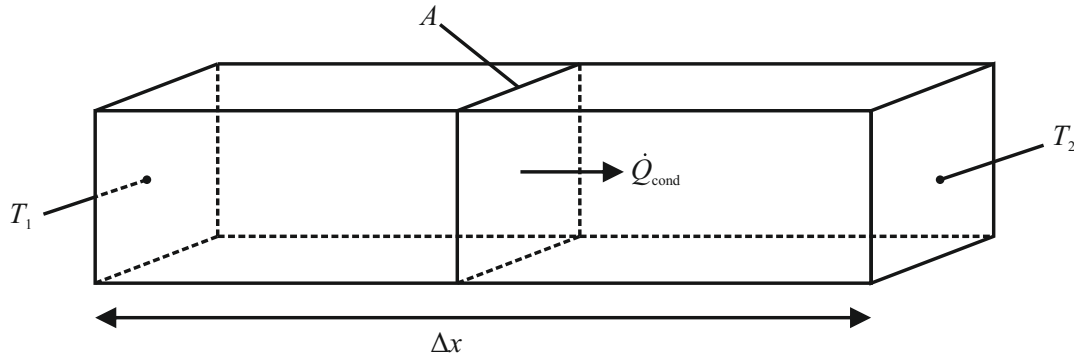


Figure 2.1: One-dimensional heat transfer by conduction through a solid

2.1.2 Convection

Convection is a combination of conduction and heat transfer by moving a gas or a fluid. Convective heat transfer is distinguished into:

- Free, or natural, convection: fluid motion is caused by buoyancy forces resulting from density variations due to variations of temperature in the fluid
- Forced convection: fluid motion is created externally by a pump or a fan

The equation that describes the heat flow from surface A to ambient is similar to the conductive heat transfer equation (Eq. 2.2). However, it is a surface effect so that no geometric thickness is contained:

$$\dot{Q}_{\text{conv}} = -\alpha \cdot A \cdot \Delta T \quad (2.3)$$

where

$\dot{Q}_{\text{conv}}$ = amount of heat transferred per unit time (in W)

α = heat transfer coefficient in $\text{W}/\text{m}^2\text{K}$

A = surface area in m^2

ΔT = temperature difference between surface and ambient in K

The heat transfer from a power-modules heat sink to ambient is a convective effect. The heat transfer coefficient α depends on the type of fluid, fluid velocity, surface geometry, temperature difference, etc. Typical values of forced convection with fluids range from 50 – 20000 $\text{W}/\text{m}^2\text{K}$ [7].

2.1.3 Radiation

Heat transfer in a power module is almost completely described by conduction and convection. Thermal radiation can usually be omitted. For the sake of completeness it is briefly explained, though. Thermal radiation is energy emitted in form of electromagnetic waves. It occurs in a vacuum or any transparent medium. The

radiated heat $\dot{Q}_{\text{rad}}$ from a body with surface A and emissivity ϵ is calculated by the Stefan-Boltzmann law:

$$\dot{Q}_{\text{rad}} = \epsilon \cdot A \cdot \sigma \cdot T^4 \quad (2.4)$$

where

T = absolute temperature of the body in K
 σ = Stefan-Boltzmann constant ($5.67 \cdot 10^{-8} \text{ W/m}^2\text{K}^4$)

Based on this the radiative heat transfer from one surface A_1 to another surface A_2 can be calculated by:

$$\dot{Q}_{\text{rad}} = \epsilon_{\text{eff}} \cdot A_1 \cdot \sigma \cdot (T_1^4 - T_2^4) \text{ with } \epsilon_{\text{eff}} = \frac{1}{\frac{1}{\epsilon_1} + \frac{A_1}{A_2} \cdot (\frac{1}{\epsilon_2} - 1)} \quad (2.5)$$

2.1.4 Thermal equivalent circuits

The physics of heat transfer by thermal conduction is very similar to that of electrical engineering. For example, heat sources in thermal engineering are just like current sources in electrical engineering and a temperature difference corresponds to an electrical voltage. The basic analogies are listed in table 2.1.

Table 2.1: Analogies between thermal and electrical parameters

Electrical parameter	Thermal parameter
Potential difference (= voltage) V in V	Temperature difference ΔT in K
Current I in A	Heat flow $\dot{Q}$ in W
Electrical resistance R_{el} in V/A	Thermal resistance R_{th} in K/W
Electrical conductivity σ_{el} in S/m	Thermal conductivity λ in W/mK
Electrical capacitance C_{el} in As/V	Thermal capacity C_{th} in Ws/K

The thermal resistance of a homogeneous body with uniform cross section can be derived from the conductive heat transfer equation (2.2)

$$R_{\text{th}} = \frac{\Delta T}{\dot{Q}_{\text{cond}}} = \frac{1}{\lambda} \cdot \frac{\Delta x}{A} \quad (2.6)$$

In steady-state all systems can be described by means of a thermal network that consists of thermal resistances. However, transient effects cannot be modeled by thermal resistances only. Changing temperatures inside a solid require the use of thermal capacities. A thermal capacity functions as an energy storage. It describes the amount of thermal energy Q stored upon each change in temperature:

$$C_{\text{th}} = \frac{\Delta Q}{\Delta T} \quad (2.7)$$

The thermal model of an arbitrary solid body can be created by replacing lumped geometric elements with their corresponding thermal resistance and capacity. With this approach a 3-D equivalent circuit of the body is built. As power modules are usually constructed by a layer stack of different materials, a 1-D model is often sufficient to describe the module with satisfactory accuracy. This model can either be a Foster or a Cauer model. The 1-D Cauer model can be derived by replacing each layer by one corresponding RC-element and connecting them in series as shown in Fig. 2.2. The voltage source T_a stands for the ambient temperature which can, for example, be the cooling fluid temperature. T_j is the temperature of the heat source which in a power module is usually the chip that generates the losses P_{loss} . Due to this physically correct approach using geometry and material data, the Cauer model is able to simulate not only the chip temperature but also temperatures of the intermediate layers [8].

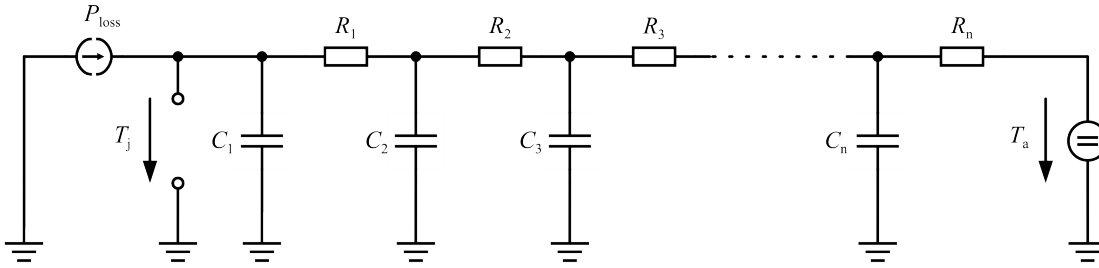


Figure 2.2: Thermal equivalent element circuit (Cauer model)

The Foster thermal equivalent network is shown in Fig. 2.3. It represents a partial fractional division of the thermal transfer function of a system. Its mathematical representation as a thermal impedance Z_{th} , depending on the time t , is very simple and can be described in a closed form (Eq. 2.8). This makes it easy to determine the equivalent elements by means of numeric fitting tools.

$$Z_{\text{th}}(t) = \sum_{i=1}^n R_i \cdot \left(1 - e^{-\frac{t}{R_i \cdot C_i}}\right) \quad (2.8)$$

In contrast to Cauer networks, the internal structure of Foster networks is never related to the real physical structure. Therefore, the internal nodes cannot be used to describe the temperatures of intermediate layers. Furthermore, Foster networks cannot be extended, e.g. to add a heat sink model to the thermal model of a power module [9]. When deriving Foster models it is always mandatory to measure the thermal transfer function of the complete system.

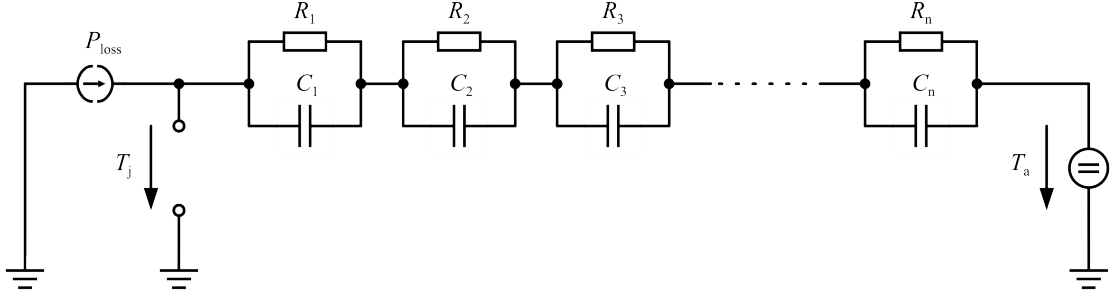


Figure 2.3: Thermal equivalent element circuit (Foster model)

2.2 Reliability

Thermal cycles, caused by varying load and environmental operating conditions, induce high mechanical stress in the interconnection layers of power modules due to the different coefficients of thermal expansion (CTE), leading to fatigue and growth of micro-cracks in the bonding materials. The occurring stress and strain can be described by the van-Mises-stress (equivalent tensile stress) which is a scalar stress value that can be computed from a three-dimensional stress tensor [10]. As a result of the stress, the lifetime of power modules can be severely limited in practical applications. Due to this, lifetime tests are done to evaluate the durability of new packaging technologies and to validate the expected lifetime of power modules before entering series production. Usually it is required to reduce the testing time significantly compared to the product lifetime. Therefore, accelerated tests at elevated temperatures and increased temperature cycles are done. The acceleration factor A_T can be calculated using the Arrhenius or the Coffin-Manson law depending on the accelerating effect.

2.2.1 Arrhenius model

The Arrhenius model is based on the molecular motion within chemical reactions. Reaction rates increase at increasing temperatures and decreasing activation energy. This correlation was first found by J. H. van't Hoff in 1884 [11] and interpreted by S. Arrhenius in 1889 [12]. The Arrhenius model is applicable if elevated temperature is the accelerating stress and potential failures depend on molecular activity. Using the Arrhenius model, the acceleration factor is [13]

$$A_T = e^{\frac{E_A}{k} \cdot \left(\frac{1}{T_u} - \frac{1}{T_A} \right)} = \frac{L_{Tu}}{L_{TA}} \quad (2.9)$$

where

- A_T = thermal acceleration factor (dimensionless)
- L_{Tu} = lifetime under normal operation temperature in hours
- L_{TA} = lifetime at elevated test temperature in hours
- T_u = normal operation temperature in K

T_A = test temperature in K
 E_A = activation energy for the particular failure in eV
 k = Boltzmann's constant ($8.623 \cdot 10^{-5}$ eV/K)

The activation energy for different classes of failures can be found in comprehensive tables [14]. A good general activation energy for many classes of failures is 0.6 eV, which corresponds to the rule of thumb that every 10 K temperature rise cuts lifetime into half.

2.2.2 Coffin-Manson model

A correlation between the number of cycles to failure and the magnitude of induced stress was found independently by L. F. Coffin Jr. in 1954 [15] and S. S. Manson in 1953 [16]:

$$N_f \cdot (\Delta\epsilon_p)^2 = C_1 \quad (2.10)$$

where

N_f = Number of cycles to failure
 $\Delta\epsilon_p$ = Plastic strain
 C_1 = Proportionality constant of the respective material

Since the plastic strain $\Delta\epsilon_p$ is proportional to the magnitude of the temperature cycle, Eq. 2.10 can be rewritten as:

$$N_f \cdot (\Delta T)^2 = C_2 \quad (2.11)$$

where

N_f = Number of cycles to failure
 ΔT = Magnitude of the thermal cycles
 C_2 = Proportionality constant of the respective material

By increasing the magnitude of thermal cycles compared to normal operation the acceleration factor A_{CM} is

$$A_{CM} = \left(\frac{\Delta T_A}{\Delta T_u} \right)^2 = \frac{\Delta N_{fu}}{\Delta N_{fA}} \quad (2.12)$$

where

A_{CM} = acceleration factor for number of cycles (dimensionless)
 N_{fu} = number of cycles to failure under normal operation temperature (dimensionless)
 N_{fA} = number of cycles to failure at increased thermal cycling (dimensionless)

ΔT_A = magnitude of thermal cycles during test in K

ΔT_u = magnitude of thermal cycles during normal operation in K

E_A = activation energy for the particular failure in eV

2.3 Reverse conducting IGBT

In voltage source converter topologies IGBTs can only be used with an anti-parallel diode to provide a free-wheeling path for the inductive currents. But it is also possible to integrate the diode monolithically into the IGBT structure by building n^+ -zones into the p -layer on the collector side (Fig. 2.4). This n^+ -zone establishes a diode together with the p -body, consequently, enabling reverse conduction of the IGBT (RC-IGBT).

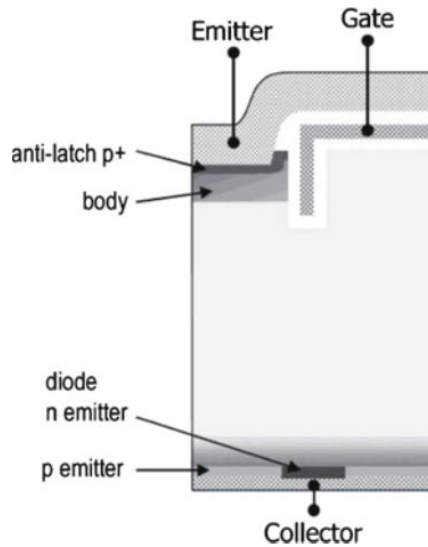


Figure 2.4: Semiconductor structure of an RC-IGBT with trench gate [17]

The main advantage of an RC-IGBT is the possible reduction of silicon area. Thermal calculations of a three-phase inverter show that the RC-IGBT requires approximately the same chip size as a normal IGBT [17]. Hence, the silicon area of the free-wheeling diodes (FWD) can be saved. The advantage of the RC-IGBT regarding chip size is even more significant in a bi-directional dc-dc converter. During operation in buck mode, only the high-side IGBT and the low-side diode are used. Whereas, in boost mode the complementary elements are active. Hence, only 50 % of the silicon area is used for cooling. Against this, the RC-IGBT also uses the chip area of the non-active elements as an additional cooling path to reduce the thermal impedance as shown in Fig. 2.5.

RC-IGBT were initially applied in lamp ballast applications with ratings of 600 V and 1 A because of the low requirements on the diode [18]. For common hard-switched converters the turn-off characteristic of the diode has to be optimized.

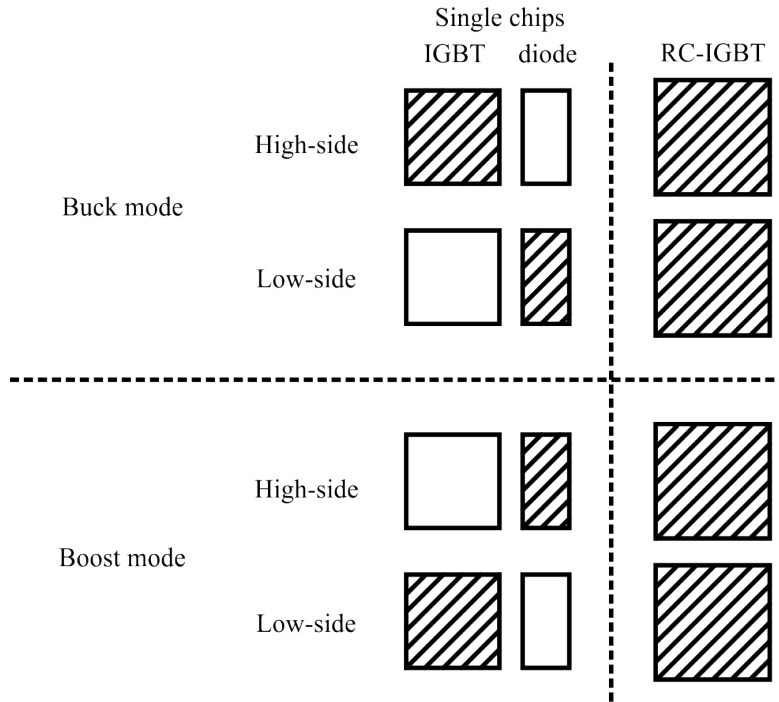


Figure 2.5: Chip area used for cooling in dc-dc converter (buck mode)

The challenge regarding this is that the highly doped p^+ -region of the IGBT leads to a snappy diode characteristic. Still, the doping can not be reduced because a high doping is mandatory for the short-circuit capability of the IGBT [17]. A concept to overcome this issue is introduced in [19], [20]. It is shown that by using several means both devices can profit from the integration of the other. Further improvements are made by developing a Bi-mode insulated gate transistor (BIGT) where a part of the chip is processed with a continuous p-collector zone [19]. A 1,200 V class IGBT was developed by Fuji showing the same performance compared to their present generation of conventional IGBT and FWD [21].

2.4 Electrical parasitics in power modules

The flow of energy in a power electronics circuit is controlled by power semiconductors that turn current on and off. Voltage source inverters (VSI) work with inductive loads that sustain the current after being turned off by the power semiconductor. The current has to commute to an alternative path which is offered by the so-called free-wheeling diode (FWD). When the power semiconductor turns on again the current commutates back. During the switching transition, the current in the commutation cell changes so that the parasitic inductance of the commutation cell has to be magnetized and demagnetized, respectively. The effects of this inductance on the switching characteristics are:

- a voltage dip across the IGBT during turn-on

- a voltage spike across the FWD when the current goes back to zero after reaching the reverse-recovery peak
- a voltage spike across the IGBT during turn-off
- oscillations between the parasitic inductance and parasitic capacitances or the dc-link capacitance

All these are unwanted effects that can even destroy the power semiconductors in case of voltage spikes that exceed the blocking capability of the device. Moreover, not only the voltage shape but also the current shape is influenced by the parasitic inductance. Bayerer reports of an IGBT that changes to much higher $\frac{di}{dt}$ when introduced into a circuit with larger parasitic inductance [22]. The higher voltage spike applied to the IGBT during turn-off leads to an earlier removal of charges from the device. Consequently, the tail current disappears. To maintain a soft switching behavior under these circumstances the IGBT has to be equipped with more stored charges causing higher losses.

This is why one main goal of power circuit design is the minimization of the parasitic commutation cell inductance, which is also called dc-link inductance. When power modules are used, this means a minimization of the inductance of the power module itself as well as a low-inductive connection of the dc-link capacitor. Papers dealing with the minimization of the inductance of wire-bond power modules show that there is room for improvement by re-arranging the chips on the DCB (direct copper bonded) [23], changing the geometry of Cu tracks and terminal leads [24][25] and integrating gate resistors and clamping capacitors into the package [26]. One of the most successful wire-bond module designs in terms of low-inductivity realized a dc-link stray inductance of below 4 nH with 75 V MOSFETs and a current rating of 750 A by paralleling seven chips. These measures can significantly reduce parasitic inductances but for high speed switching devices using wide-bandgap materials a more drastic reduction is necessary which is not possible using wire-bond power modules.

A well-known approach to reduce circuit inductance is the use of strip-line type interconnections. The inductance of a strip-line depends on its width w , length l and the distance d between the conductors [27], [28], [29] as depicted in Fig. 2.6 where H is the magnetic field strength and j is the electric current density. It is calculated according to Eq. 2.13 [22] using the permeability of vacuum μ_0 . Laminated busbars are typically used in power electronics to realize strip-line interconnections of the dc-link capacitors. However, the strip-line concept is violated at capacitor terminals as well as module terminals and inside modules. In case of screw type (or similar) interconnections the inductance can be piece-wisely calculated according to the equation of a two-wire assembly (Fig. 2.7 and Eq. 2.14). Two-wire segments have very high inductance per length compared to a strip-line. Hence, the interconnections that break the strip-line easily dominate the circuits overall inductance.

$$L_\sigma = \mu_0 \cdot \frac{d}{w} \cdot l \quad (2.13)$$

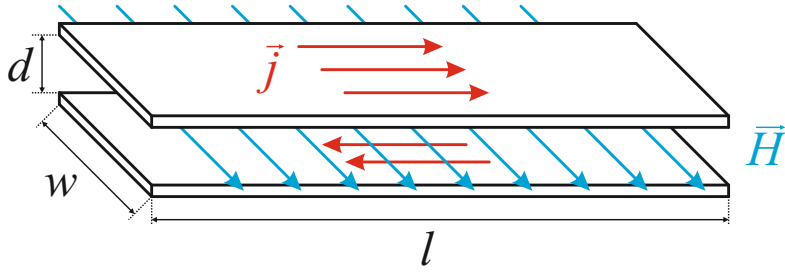


Figure 2.6: Inductance of a strip line configuration

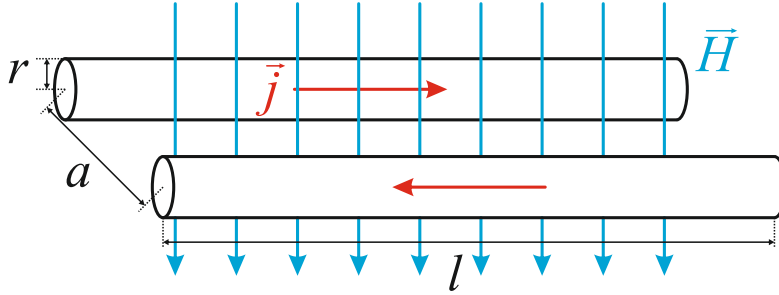


Figure 2.7: Inductance of a two-wire configuration

$$L_{\sigma} = \frac{\mu_0}{\pi} \cdot l \cdot \left(\ln \left(\frac{a}{r} \right) + \frac{1}{2} \right) \quad (2.14)$$

A consequent strip-line design with wide and short conductors is necessary for a low-inductive commutation cell design. In [30] a planar module is simulated and built by using a substrate-chip-substrate sandwich. Indeed, the realized inductance of the module is much lower than of a comparable bond-wire module. However, it is not possible to connect the dc-link capacitor via strip-lines to this module. Consequently, the overall dc-link inductance will still be relatively high.

Alternative module design concepts are the ThinPak Technology from Silicon Power [31], the Power Overlay Technology from General Electric [32] and the Metal Post Interconnect Parallel Structure (MPIPPS) [33], Embedded Power [34], Flip Chip [35] and Dimple Array Interconnect Technology [36] from the Center for Power Electronic Systems (CEPS) at Virginia Tech University, Blacksburg, VA. Chip embedding based on printed circuit board technologies are described in Chapter 3 but it is worth stating already here that with chip embedding technologies dc-link inductances of around 1 nH can be reached [37][38].

In integrated microelectronic circuits the parasitic behavior of conductors is dominated by capacitive effects [39]. In contrast to this, only parasitic inductances and resistances play a significant role in power electronics modules and circuits, as long as no interactions with the environment, e.g. EMC compliance, are considered [40].

3 Power Electronics Packaging

This chapter starts with a brief description of the tasks of power electronics packaging and today's main driver in its development. The connection technologies which are classically used for semiconductor packaging are described with emphasis on power modules. Afterwards, the evolution of power modules over the last 40 years is outlined. It will be shown how the introduction of new packaging technologies affected the reliability and power density of power modules.

3.1 Definition of power electronics packaging

The main tasks of power electronics packaging are [41][42][43]:

- to connect one or more semiconductor chips with the electric circuit they are used in (electrical task)
- to dissipate the heat generated inside the semiconductors due to switching and conduction losses with a very high heat flux density (thermal task)
- to protect the semiconductor from environmental influences that could damage or destroy it (mechanical task)

Based on this, several general trends in the development of new packaging technologies can be identified [41]:

- Optimization of the heat dissipation and the thermal cycling capability
- Minimization of the inductances inside the module as well as in the leads
- Flexible packaging technologies and easy handling/mounting by the user
- Integration of power modules (e.g. into the electric machine, ...)
- Integration of sensing, protection and driver functions into the power module

3.2 Electrical bonding technology

Electrical bonding technology can be distinguished into internal and external. All connections to the semiconductor are referred to as internal bonding technology, whereas external bonding technology refers to all electrical connections from a component, e.g. a power module, to its environment. This work focuses on internal bonding technology for IGBT chips with a vertical structure. Such chips have at

least three connection terminals: The gate and the main emitter are located on the top side of the chip. The collector terminal is at the bottom. IGBT chips with enhanced functionality, such as on-chip temperature or current measurement have additional terminals located on the top side surface.

3.2.1 Soldering

Soldering is used for connecting the IGBT chips electrically and thermally to the substrate, e.g. a DCB (direct copper bonded) or IMS (insulated metal substrate). During a soldering process two metal surfaces are connected by a liquid metal or a liquid metal alloy. Single atoms of the solder diffuse into the metal surfaces such that a thin composition layer of solder and metal is built. To ensure a void-free interconnection, the soldering process is carried out in a vacuum. Otherwise, the insufficient linking increases the thermal resistance between chip and substrate and would inevitably lead to a later failure of the IGBT.

Joining the DCB substrate to a baseplate can also be done by soldering. However, large-area soldering connections of materials with extensive CTE (coefficient of thermal expansion) mismatch are critical regarding lifetime. The bi-metal effect during temperature swings leads to solder fatigue or failure.

3.2.2 Ultrasonic bonding

Ultrasonic bonding is the most common bonding method to contact the top side of power electronic chips. Aluminum wires are micro-welded at room temperature to a contact pad with the exclusive use of ultrasound. While applying a bonding force of 0.3–0.6 N, the ultrasound movement of the wire (amplitude of 1–2 μm at $\approx 60\text{ kHz}$) generates friction that removes the oxide layer of the contact surface, which can be aluminum, copper or gold. Thereby, the wire is attached tightly to the chip. The sequence of the ultrasonic bonding process is shown in Fig. 3.1. After exact positioning of the wire (I) the first bond is made to the die (II). The wire is positioned at the next bonding location and the second bond is made (III). Optionally, between step II and III additional bonds to the die can be made (stitching). After bonding to the package, the excess wire is broken (IV). While thin-wire bonding uses a wire gauge of 17 μm to 100 μm , thick-wire bonding comprises wire gauges from 100 μm to 500 μm . The latter is typically used in IGBT power modules. The technology is very flexible and cheap, making it today's dominant type of top surface connection technology.

Since bond wire crack or lift-off is one of the main failure mechanisms in power modules, manufacturers more and more try to improve this technology. One approach is to optimize the geometry of the bond wires, i.e., the wire thickness and the height to width ratio [44]. Another trend is the usage of copper as bond wire material. Either aluminum wires with copper coating or solid copper wires are bonded to copper surfaces. Copper bonding provides an enhanced reliability and a higher current capability compared to aluminum bond wires [45]).

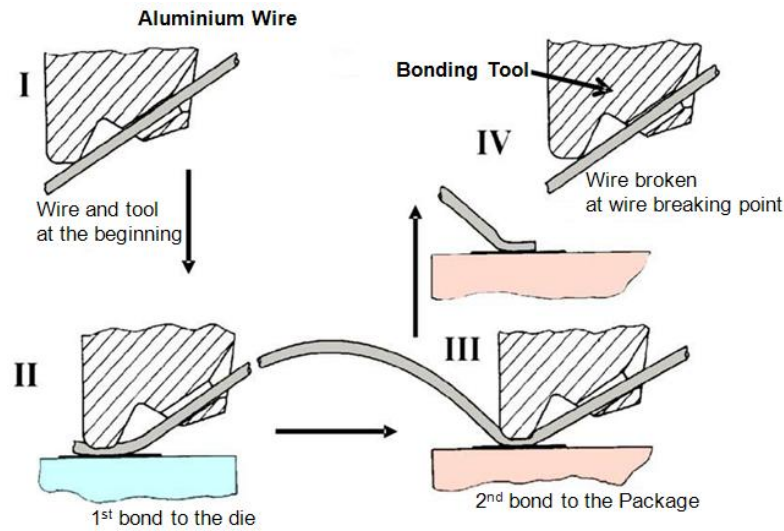


Figure 3.1: Ultrasonic bonding process

3.2.3 Sintering

During a soldering process the solder melts at temperatures of around 250 °C, building an alloy with the metal surface and solidifies again. This results in the disadvantageous fact that the solder layer, which is used for the die attach in power modules, is operated at temperatures that are close to the melting temperature of the solder material. This can be avoided when using a low temperature diffusion sintering process: Similar to reflow soldering, a paste, now containing a fine silver powder, is applied between two metal surfaces. The silver powder is sintered under high pressure and at a temperature of around 250 °C. The liquid component of the paste diffuses out and the silver connects the surfaces by building a thin layer of low porosity (Fig. 3.2). Contrary to the solder particles in a reflow solder process, the silver powder stays far away from its melting temperature. The advantage that arises from this fact can be well illustrated by having a look on the principle of the homologous temperature which is defined by the relation between operating and melting temperature with both related to the absolute temperature scale [46].

$$\text{Homologous temperature in \%} = \frac{\text{Operating temperature in K}}{\text{Melting temperature in K}} \cdot 100 \% \quad (3.1)$$

Below 40 % materials are only little stressed. This is also the range where the silver used for diffusion sintering is operated. Between 40 and 60 % the material starts to creep and is sensitive against mechanical stress. Above 60 %, and this is where typical solder materials are operated, materials are usually not suitable for reliable connections anymore.

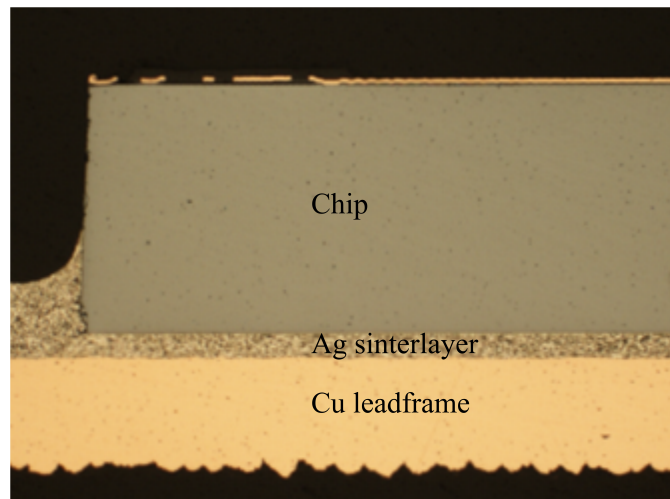


Figure 3.2: Cross section of sintered IGBT die

3.2.4 Pressure contact

Contrary to bonded connections, like soldering, sintering and bond wires, the pressure contact is a form-locking connection. This means that the contact partners can slide on each other which leads to drastically reduced thermal stresses that would otherwise arise from different CTE's. Accordingly, the reliability of pressure contacts is very high. In power electronics packaging there are large and small area pressure contacts. An example for a small area pressure contact are spiral springs for the control terminals of power modules. Large area pressure contacts are used to establish the contact of power modules to a cooler, or in press-pack disc housings for high power diodes or thyristors. In the latter application a buffer material adjust the CTE values to minimize the sliding during temperature cycles. In the 1980s structured copper, many thin Cu filaments put in parallel, was tested for this purpose [47]. Today, molybdenum discs are usually applied.

In high-voltage applications, such as high-voltage, direct current (HVDC) transmission and power quality management, dozens of semiconductor press-pack modules are connected in series to handle dc-link voltages up to 600 kV [48]. Due to the high number of modules the mean-time between failures (MTBF) is quite low. Therefore, redundant modules are used such that in case a failed module the surviving modules are still able to block the voltage. To carry the load current the failed module has to provide a stable short circuit condition. In press-pack IGBT modules ABB uses special platelets that melt in case of a chip failure and form an alloy together with the silicon chip [49]. High current rating of the press-pack IGBT is achieved by paralleling lots of chips. Each chip is contacted with an individual mechanical spring to ensure uniform contact pressure even when connecting a high number of modules in series [50][51]. Contrary to the non-hermetic ABB design, Fuji offers a hermetic shielded press-pack IGBT package [52].

3.3 Evolution of power modules

The development from the first power module to the state-of-the-art is described in the following sections. Afterwards, an alternative power module design is presented that uses chip embedding technology on the basis of high-current printed circuit boards (PCB).

3.3.1 Advancement of technology

DCB ceramic substrates were invented at the General Electric Research Labs, Schenectady, NY in the early 1970's [53][54] and made it possible for the first time to build semiconductor packages that allowed the insulation between the electrical circuit and the cooling system while maintaining a good heat extraction [55]. This kind of package is known today as the classical power module and was introduced to the market by SEMIKRON in 1975. The chips are soldered to the DCB substrate and the top side connection is established using ultrasonic wire bonding. Afterwards, the DCB is soldered to a base plate and the load terminals as well as control connectors are attached to the DCB using soldering [56]. Since then, lots of innovations were made to successively improve the thermal, electrical and mechanical performance of power modules. The main targets of the technology improvements are the enhancement of the heat dissipation, the thermal cycling capability and the feasibility to operate at elevated junction temperatures. Higher temperatures enable system size and weight reduction and are of great interest especially for the use of wide bandgap materials like SiC and GaN because these materials leverage their material characteristics particularly at higher temperatures.

3.3.1.1 DCB

The ceramic of the first power module was made of BeO. Today, Al_2O_3 is the most common material for the DCB even though its thermal conductivity of 24 W/mK is quite poor compared to BeO with more than 300 W/mK [57]. However, BeO is relatively expensive and, moreover, highly toxic. This is why it is only used in special applications today. If high thermal conductivity is mandatory, an alternative for Al_2O_3 is AlN (180 W/mK). The disadvantage of AlN is again a high price. The use of AlN especially makes sense for modules with high requirements regarding insulation voltage as well as cooling performance.

The trend is to improve the thermal performance as well as mechanically strengthen the substrate. This has already been done by reducing the Alumina thickness from 0.63 mm to 0.38 mm. With Zirconium doped Alumina a thickness of 0.32 mm can be realized [58]. With silicon nitride (0.32 mm) it is possible to increase the Cu metallization from 0.3 mm to 0.6 mm due to its high mechanical strength [59].

3.3.1.2 Baseplate

In 1992 SEMIKRON introduced the SKiiP®-technology that left out the baseplate, which was conventionally used to establish the connection between DCB and cooler. Instead, the DCB was pressed onto the cooler using a thin layer of grease as thermal interface material. This solution provides several advantages:

- The elimination of the solder layer between DCB and baseplate ensures a better thermal cycling capability.
- The flexibility of the baseplate-less DCB allows the use of thinner thermal grease layer (only $20 \dots 30 \mu\text{m}$ compared to $70 \dots 120 \mu\text{m}$ for a module with baseplate). Thereby, the static thermal resistance can be significantly reduced.
- Leaving out the baseplate allows for a significant reduction of weight
- Larger DCB's can be used, because they do not have to be soldered anymore. Thereby, no interconnections between separate DCB's are necessary.

The disadvantages of a baseplate-less module are:

- Higher thermal impedance in the range of 1 s due to the missing baseplate, that otherwise provides a high thermal capacity.
- Smaller chip size requires more parallel elements.

In high power modules ($>1,000 \text{ A}$) with AlN ceramics the material of the baseplate has to be changed due to the large CTE mismatch of Cu (CTE = 17 ppm) and AlN (5.7 ppm). Therefore, AlSiC was introduced that has a CTE of 7 ppm [41].

3.3.1.3 Die attach

The demand for increasing power density inevitably led to higher chip temperatures. Consequently, the homologous temperature of the solder layer between chip and DCB more and more increased. This enforced new die attach concepts to retain acceptable reliability of this interconnection. Silver sintering was developed and implemented in the late 1980s by SIEMENS for large area interconnection in high-power press-pack designs. In the 1990s it was demonstrated for the first time that it can also be used to replace solder interconnection in classical power modules [60]. Based on this, SEMIKRON developed a suitable series production process [61] and introduced the first series production modules in 2007. In combination with pressure contact technology and spring connectors the first power module without solder interfaces could be built [62]. The diffusion sintering interconnection technology can replace soldering in many cases and has proven to be far superior to soldering with respect to thermal cycles. Therefore, sintering technology will meet the requirements of most applications in terms of long-term reliability [63]. Despite its superior technical characteristics, this connection method seems to be of limited use for high-volume power module manufacturing due to the slow production process.

3.3.1.4 Top side connection

Multiple improvements like the sintering process replacing the traditional soldering of the chips have enabled to raise the maximum junction temperature from 125°C to 175°C while upgrading the reliability of power modules. But particularly wire-bonding, which is the major connection method for the chip topside, has remained a bottleneck in this development. Even though wire-bonding has been used for many years now it is still not a satisfying contact solution due to its limited reliability. Furthermore, bond wires do not allow for double-sided cooling and add stray inductance, which causes overvoltages and ringing effects. Where reliability is of concern, for example in converters for HVDC applications, switches with press-pack housings are commonly used. Compared to bond wires, a press-pack contact guarantees a predefined fault state (short-circuit) in case of failure, whereas switches with bond wires can either fail into a shorted or open circuit.

In automotive applications where higher switching frequencies and higher power densities are of major concern, there is a great need for replacing the bond wires. As a result, packaging engineers recently increased the focus of their work on finding alternative solutions for the chip topside connection. For high-power automotive applications MITSUBISHI offers a module where the bondwires are replaced by a soldered connection on top of the chip. MITSUBISHI claims to have a significantly higher lifetime compared to industrial modules in their transfer molded power module J-series T-PM [64]. Similarly, TOYOTA equips the converters of their HEV's with power semiconductors soldered from both sides and use double sided cooling [65] which reduces the thermal resistance by up to 40 % [66]. Another new interconnection technology is the replacement of wire bonds by ribbon bonds [67].

One of the latest approaches for the replacement of bond wires is SEMIKRON's SKiN technology [63]. Here, the top metallization of the chips is connected to a flexible circuit board by diffusion sintering. FUJI ELECTRIC COMPANY announced a high-temperature package for SiC devices that uses short copper studs pressing on the emitter and gate contacts [68].

An overview of packaging technologies that are used in specific electric vehicles gives Aranzabal et al. [69].

3.3.2 Lifetime of power modules

The lifetime of power modules is limited due to their operation at elevated temperatures and thermal cycles that are caused by varying load and environmental operating conditions. Elevated temperatures accelerate aging processes caused by molecular activities which can be described by the Arrhenius law (see 2.2.1). Thermal cycles induce high mechanical stress in the interconnection layers of the power module due to the different coefficients of thermal expansion (CTE), leading to fatigue and growth of micro-cracks in the bonding materials following the Coffin-Manson law (see 2.2.2).

In the 1990s the influence of the junction temperature swing and the medium temperature on power cycling results was investigated within the LESIT project [70]. It was found that the number of cycles to failure (N_f) follows the Coffin-Manson law, where the influence of the medium junction temperature T_m is modeled by an additional Arrhenius factor:

$$N_f = B \cdot \Delta T_j^a \cdot \exp\left(\frac{E_A}{k \cdot T_m}\right) \quad (3.2)$$

where

$$\begin{aligned} R &= \text{universal gas constant (8.314 J/(mol} \cdot \text{K))} \\ T_m &= \text{medium junction temperature in K} \\ B &= 640 \\ a &= -5 \\ E_A &= 0.8 \text{ eV} \end{aligned}$$

From Eq. 3.2 it can be seen, that an increase of the temperature swing ΔT_j by a factor of 2 leads to a reduction in lifetime of $2^{-a} = 32$. An increase of the absolute temperature of the module T_m by 10 K leads to a reduction in lifetime by a factor of about two in the temperature range around 100 °C. The found results are only valid for the examined module technology and in the parameter range which was tested.

A more sophisticated model was developed in 2008 which takes into account the influence of several additional parameters [71], namely power-on-time, blocking voltage of the chip, diameter of the bonding wire and current per bond wire. It can especially be used for the estimation of power cycling capability of 1200V-IGBT4 modules. However, even this model is not able to indicate how different failure modes depend on the respective parameters and how they possibly interact with each other. In 2012 SEMIKRON presented a study [72] in which bond-wire failures and such from solder fatigue could be tested separately. This offers the possibility to investigate the influence of different test parameters on the two power cycling failure modes. Nevertheless, the authors conclude that “more investigations have to be performed to get a clear picture of the physics of failure in power cycling tests”.

Since new packaging technologies influence the failure mechanisms of power modules, the lifetime models have to be adapted to the advancement in technology. An example for this is the further development of the lifetime model from [71] which was adapted to modules with silver sintering die attach, copper wire bonding top-side interconnection, ultrasonic welding for power terminals and an advanced solder alloy for the substrate-to-baseplate joint [73]. Some effects were found to not apply anymore for such kind of modules which simplified the lifetime model. For baseplate-free modules and modules with baseplate different failure mechanisms are dominant so that different lifetime model have to be used.

In the majority of cases, it is not possible to make a fair comparison of power cycling tests results because there are no standardized test conditions. One reason for this

is the ongoing increase in power cycling capability that forces manufacturers to test at higher temperatures and with larger magnitudes of thermal cycles in order to limit testing time to a reasonable extent. A comparison for corresponding test conditions was made by Scheuermann when introducing the SKiN technology [46]. At that time, state-of-the-art industrial power modules exceeded the power cycling capability of the classical base plate modules that were used in the LESIT project by a factor of 5. Modules with sintered chips and improved wire bond geometry increase the lifetime limit to a factor of 40. The SKiN technology with sintered top side connection of the chips enhance the power cycling capability by a factor of almost 200 compared to the classical module design.

3.4 Chip embedding for power electronics

An alternative solution for building highly reliable and compact power modules, with an improved thermal management at low costs, is the use of high-current PCB's (printed circuit boards) as an integration platform with embedded power semiconductor chips. The first step into this direction was done in the late 1980's at GENERAL ELECTRIC COMPANY. The development of the High Density Interconnect (HDI) technology made it possible to build packages with embedded semiconductor chips [74]. Different embedding technologies were developed for various applications since that time, finally leading to PCB based power modules with embedded semiconductors.

3.4.1 Embedding technology

The laminate based embedding technology combines standard printed circuit board processing with the addition of high accuracy component placement and handling. Basically, there are two approaches for the embedding of silicon dies: The face up method, i.e. with the contact pads upside, or face down like a flip chip. The resulting structures are comparable, but differ in their suitability for various applications. An exemplary face up embedding process is outlined in Fig. 3.3. Starting with the die attach on a Cu foil or substrate (a), the embedding is done by laminating an epoxy laminate material (b). After the laser drilling of micro-vias (c), the top side connections are done by galvanization followed by structuring of the created top layer (d). More details regarding the different die attach materials, process steps and laminate materials can be found in [75], [76].

Laminate based embedding of power components offers the possibility of 3D packaging, which enables the realization of multi-die or multi-component systems with very low inductances and with EMI (electromagnetic interference) shielding. Most power components are bulk type semiconductors in which current flows vertically through the device. Consequently, these components have contacts on top and bottom of the die. The work done for the embedding of power components like MOSFETs (metal-oxide-semiconductor field-effect transistor), IGBTs, thyristors, diodes etc. is based on the face up embedding method to provide direct access to

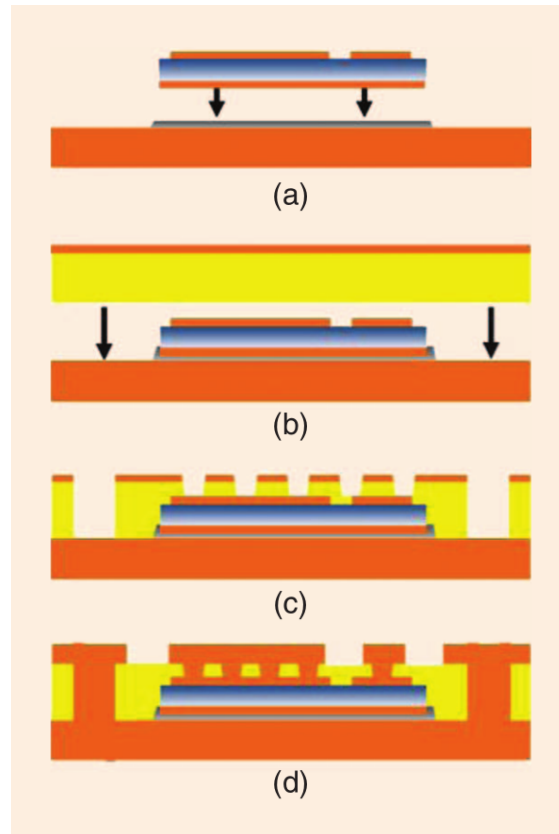


Figure 3.3: The process sequence of power component embedding: (a) conductive chip attach, (b) embedding by lamination, (c) via drilling chip and substrate, and (d) Cu plating and structuring [75]

the chip back. Thereby, an ideal electrical and thermal connection to the die is established without the need of additional via connections. For the back contact the standard metallization for die attach is silver. Copper back metallization is also already partially available. Both materials are compatible with the face-up embedding technology.

For the base substrate typically a copper foil or thick copper substrate is used. To achieve the best possible electrical and thermal connection to the power chip, different die attach materials were tested. The application of conductive adhesives, which can be done by printing, dispensing or jetting, provides a good method to realize a void free and uniform die attach layer. However, this approach has limitations in electrical and thermal conductivity. A new approach is a low temperature and low pressure sintering process (compare Section 3.2.3). This process is currently under continuous development [77].

3.4.2 Application examples for power packages

Since the early 2000s, laminate based chip-embedding has made a huge step towards industrialization. Meanwhile, different products in the low- and medium-power

application, e.g. mobile communication or high-end server applications, are commercially available [78][79][80] (Fig. 3.4). Higher power levels until now have only been addressed within several prototyping studies, e.g. HIDING DIES in 2006 and [81]. Within these studies reliability qualifications have been fully passed. One of the studies is the HI-LEVEL project [82]

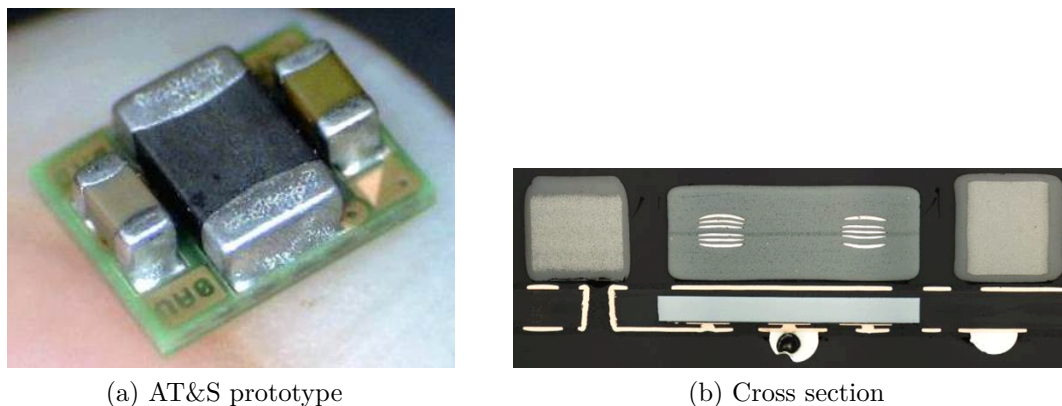


Figure 3.4: Dc-dc converter with embedded power chip [78]

3.4.3 The HI-LEVEL project

In the HI-LEVEL (german acronym of "Integration of Power Electronics in High Current Pcb's for Electric Vehicle Application") project [83], running from 2012 to 2014, partners from industry (automotive manufacturer, automotive supplier, semiconductor and material supplier, PCB manufacturer) and research (circuit design and packaging) teamed up to develop and refine the technology, components and materials to realize laminate based chip embedding for high power automotive application. The goal was the realization of a 50 kW inverter for the electric motor of an upper class HEV. In a conventional version, i.e. using DCBs and wire bonds, this inverter was already in manufacturing. In the following, the manufacturing process of the final 50 kW prototype is described. The characterization of this power module is subject of Chapter 4.

For the prototype a five layer stack is constructed. Three layers are used for the electrical interconnections. One more layer is necessary to provide an insulated Cu surface for the cooler attach. The fifth layer is only needed to retain a symmetric layer construction which is advantageous regarding mechanical stability (bending effects). The manufacturing process starts with the core of the module which is the so called leadframe. This is a copper sheet with a thickness of 600 μm . First of all, the leadframe is structured by milling (Fig. 3.5a.i). Afterwards, 140 μm deep cavities are milled on the top side to later take up the chips. The die attach inside the cavities is done by a sintering process. Due to the cavities, it is not possible to print the sinter paste. Instead the sinter paste is printed onto a separate foil and is predried. Afterwards these preforms can be transferred into the cavities at

moderate pressure and temperature. Now the chips can be placed onto the preforms and the sintering process is carried out (Fig. 3.5a.ii). In the following embedding process, a prepreg layer is laminated onto the leadframe (Fig. 3.5a.iii). In the next step, vias through the prepreg are drilled by a laser (Fig. 3.5a.iv). The vias are filled in a galvanization process that also builds a continuous copper layer on the top side (Fig. 3.6a.v and Fig. 3.6). The copper layer can now be structured and an additional prepreg and a copper layer are laminated on top and bottom (Fig. 3.5a.vi).

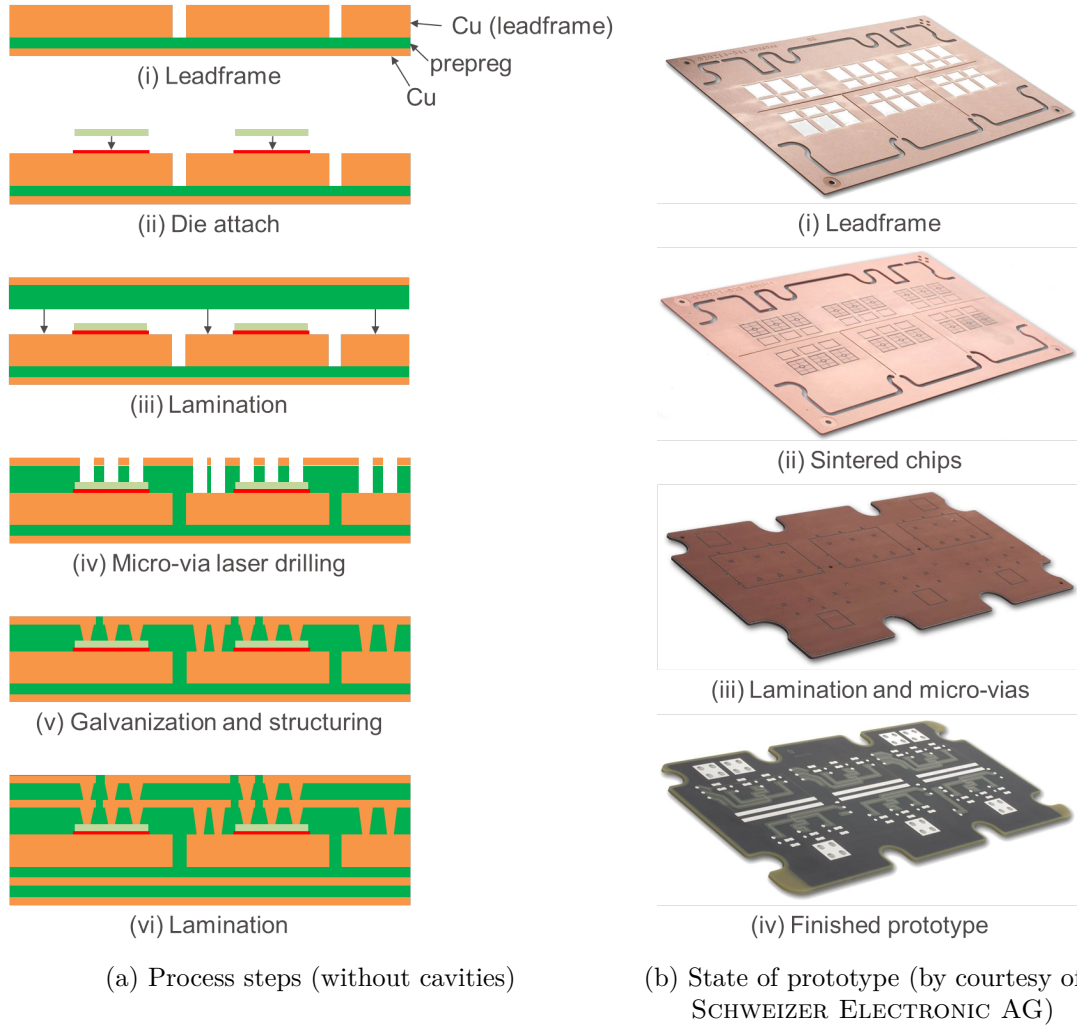


Figure 3.5: Power component embedding for HI-LEVEL project [75]

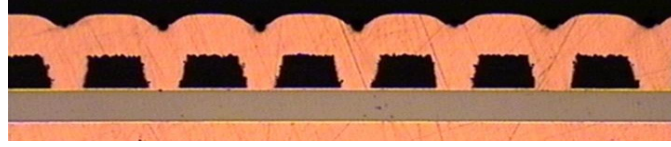


Figure 3.6: Embedded IGBT die with micro-via top side interconnections (by courtesy of SCHWEIZER ELECTRONIC AG)

3.5 Requirements in automotive applications

The installation of power electronics components within the engine compartment of HEVs brings up very challenging environmental conditions in terms of ambient temperature, thermal cycling capability and vibration. Even though each manufacturer defines its own specification for different positions in the vehicle, the requirements are similar and the most common conditions are described here with focus on the harsher conditions for HEV compared to the conditions in purely electric vehicles (EV).

In EVs the ambient temperature is in the range of -40°C to 105°C . In HEV the presence of the combustion engine increases the maximum temperature up to $125\ldots 135^{\circ}\text{C}$ while the temperature of the cooling circuit goes up to 105°C during normal operation and up to 120°C with power derating.

The complete lifetime of automobiles is 15 years of which only 10,000 h are operational time [84]. With an average velocity of 30 km/h this corresponds to a mileage of 300,000 km. Mission profiles specify the duration of operation within a certain ambient temperature range. During a cold start the coolant is heated up from $T_{\text{low}} = 5^{\circ}\text{C}$ to $T_{\text{high}} = 105^{\circ}\text{C}$ and later cooled down again. With two cold starts per day, the number of passive temperature cycles N_{passive} during the complete lifetime is

$$N_{\text{passive}} = 15 \text{ years} \cdot 365 \frac{\text{days}}{\text{year}} \cdot 2 \frac{1}{\text{day}} \approx 10000 \quad (3.3)$$

each stressing the power electronics components with temperature cycles ΔT of

$$\Delta T = T_{\text{high}} - T_{\text{low}} = 100 \text{ K} \quad (3.4)$$

Additionally to the passive cycles, there are also active cycles caused by acceleration and braking. Depending on the driving cycle approximately 3,000,000 active power cycles with 40 K can be assumed.

4 Power Module Concepts for Automotive Applications

In this chapter several new power-module concepts for automotive drive train application are discussed. Indeed, the concepts are based on known packaging technologies, but have not been used in this specific power range (around 50 kW) until now. Moreover, the implications of using RC-IGBT chips in combination with the new module concepts are investigated.

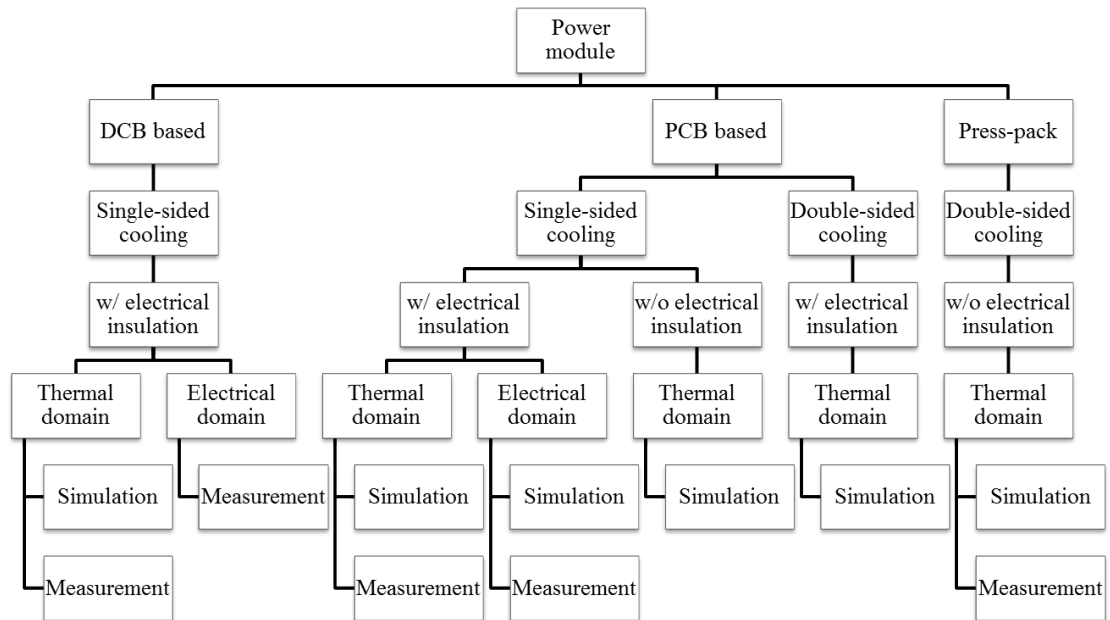


Figure 4.1: Overview: Power modules concepts

Fig. 4.1 gives an overview of the examined modules. In total, five modules are evaluated. Three of them are available as samples to do comparative measurements. The state-of-the-art is a conventional DCB based power module from CONTINENTAL, which has been in series production for several years now (Fig. 4.2a). The first alternative packaging concept uses a high current PCB as an integration platform for the power semiconductors. The IGBTs are embedded into the PCB as described in section 5.1. Besides the constructed prototype with single-sided cooling (Fig. 4.2b), two more variants are analyzed theoretically: A double-sided cooling configuration

and a single-sided cooling configuration that leaves out the electrical insulation layer to optimize heat dissipation.

The second alternative is a press-pack power module, that was designed and constructed within the e performance project [85]. The scope of this project was to build an EV by designing a completely new vehicle concept instead of just replacing the gasoline tank by a battery and the combustion engine by an electric machine. Following this holistic approach all components were optimized for the operation in a full-electric car in order to realize a high range and low costs. To meet the challenging lifetime requirements under harsh environmental conditions in automotive applications (compare section 3.5), the press-pack concept was chosen as packaging technology for the power semiconductors. It is constructed without an electrical insulation between chips and heatsink, comparable to the theoretically investigated module in [86]. The prototype of this module (Fig. 4.2c) consists of five milled aluminum blocks that are bolt together. The semiconductor chips are located on slightly elevated surfaces between the blocks to contact them electrically and thermally. The required pressure is applied by the bolts. The project report [85] describes how the aluminum surfaces have to be prepared and which pressure is needed for best thermal performance.

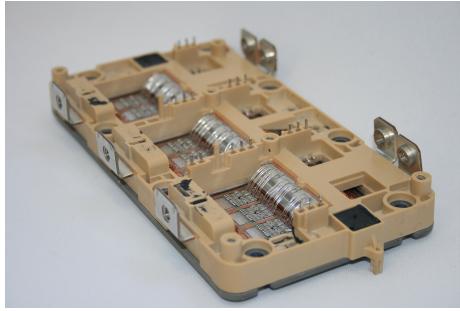
In the following, the different module concepts are denoted as

- Type 1: DCB based power module (illustrated in Fig. 4.2a)
- Type 2: PCB based power module, single-sided cooling **with** electrical insulation (illustrated in Fig. 4.2b)
- Type 3: PCB based power module, single-sided cooling **without** electrical insulation (not shown in Fig. 4.2)
- Type 4: PCB based power module, double-sided cooling with electrical insulation (not shown in Fig. 4.2)
- Type 5: Press-pack power module (illustrated in Fig. 4.2c)

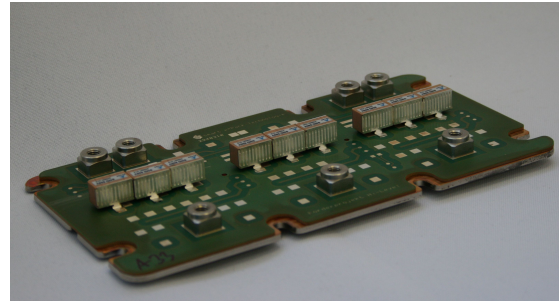
For all five modules, the thermal performance is simulated with an FEM tool. A verification of the simulation is done with Type 1 and Type 2 by thermal impedance measurements. A thermal impedance measurement is also done with Type 5. However, the module construction of the prototype geometrically differs from the simulation data. Hence, no direct comparison is possible. At least, the measurement can be used to parameterize the simulation model, especially the thermal resistance of the pressure contact.

Beyond thermal simulation and measurement, the electrical properties of Type 1 and Type 2 are analyzed in detail. This comprises

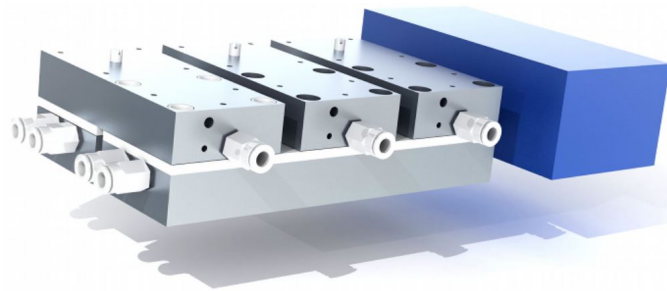
- simulation of the dc-link inductance during the design phase (only Type 2)
- measurement of the dc-link inductance



(a) Type 1: DCB based power module from CONTINENTAL



(b) Type 2: PCB based power module from HI-LEVEL project



(c) Type 5: Press-pack power module from e performance project

Figure 4.2: Examined power module prototypes

- measurement of the conduction losses (output characteristic)
- measurement of the switching losses

4.1 Thermal simulation

The thermal performance of a power module is described by the thermal impedance. In signal theory, the thermal impedance corresponds to the step response. Therefore, it contains the full thermal description of the module. To simulate the thermal impedance, 3D models of all five examined power modules are set up. Since the spatial distribution of the chips is almost equal for Type 1 and Type 2, this configuration is used for all types of modules. Due to symmetry reasons, only one pair of IGBT and FWD is modeled. Exemplary, this section is shown for Type 1 by the red box in Fig. 4.3. To deliver comparable results the simulation also uses the same cooler for all modules. Only the layer construction differs.

4.1.1 Simulation setup

Each type of module has its unique layer construction that determines the thermal impedance. The respective layer arrangement is described here together with the methodology used to extract the thermal impedance from the simulation. The

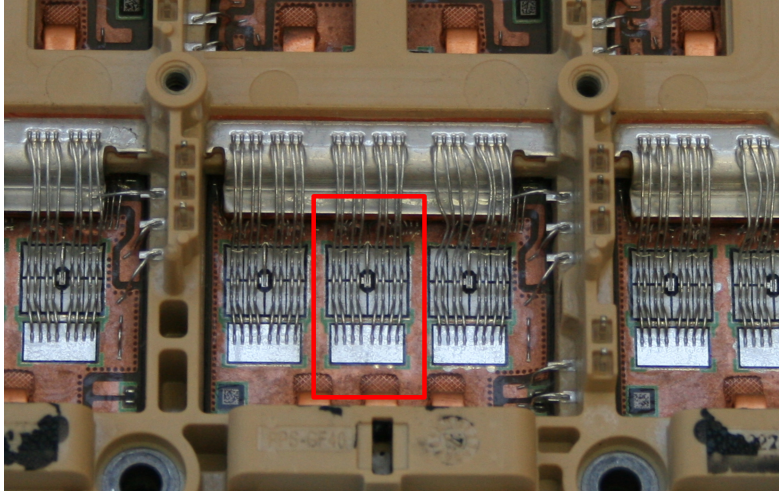


Figure 4.3: Simulated section of the power modules

thermal and electrical properties of the used materials are listed in Table A.1 and A.2.

4.1.1.1 Type 1

The layer construction of the DCB based module corresponds to the CONTINENTAL EPF2-3 module (Fig. 4.2a). The chips are sintered to the DCB substrate which is a sandwich of a $600\text{ }\mu\text{m}$ Al_2O_3 ceramic layer enclosed by $300\text{ }\mu\text{m}$ copper layers. Finally, the DCB substrate is soldered onto the pin fin cooler. The bond wire top side connections are not considered here because they marginally influence the thermal behavior of the module.

4.1.1.2 Type 2

The layer construction of the PCB based module with single sided cooling equals the prototype that was built during the HI-LEVEL project (section 3.4.3). The chips are sintered to the leadframe which is a $550\text{ }\mu\text{m}$ copper layer. The leadframe is combined with another copper layer ($185\text{ }\mu\text{m}$) via a $140\text{ }\mu\text{m}$ thermally conductive prepreg that fulfills the function of electrical insulation. The whole PCB is finally sintered onto the same pin fin cooler as the DCB based module. The upper layers are omitted in the thermal simulation because they only have marginal impact on the thermal impedance.

4.1.1.3 Type 3

Leaving out the electrical insulating layer, the leadframe is directly attached to the cooler. Of course, this induces challenges regarding the electrical insulation of the different potentials of the inverter (DC+, DC-, potential of the phase connections). However, this is not discussed here. Instead, focus is on the thermal characteristic of such a module.

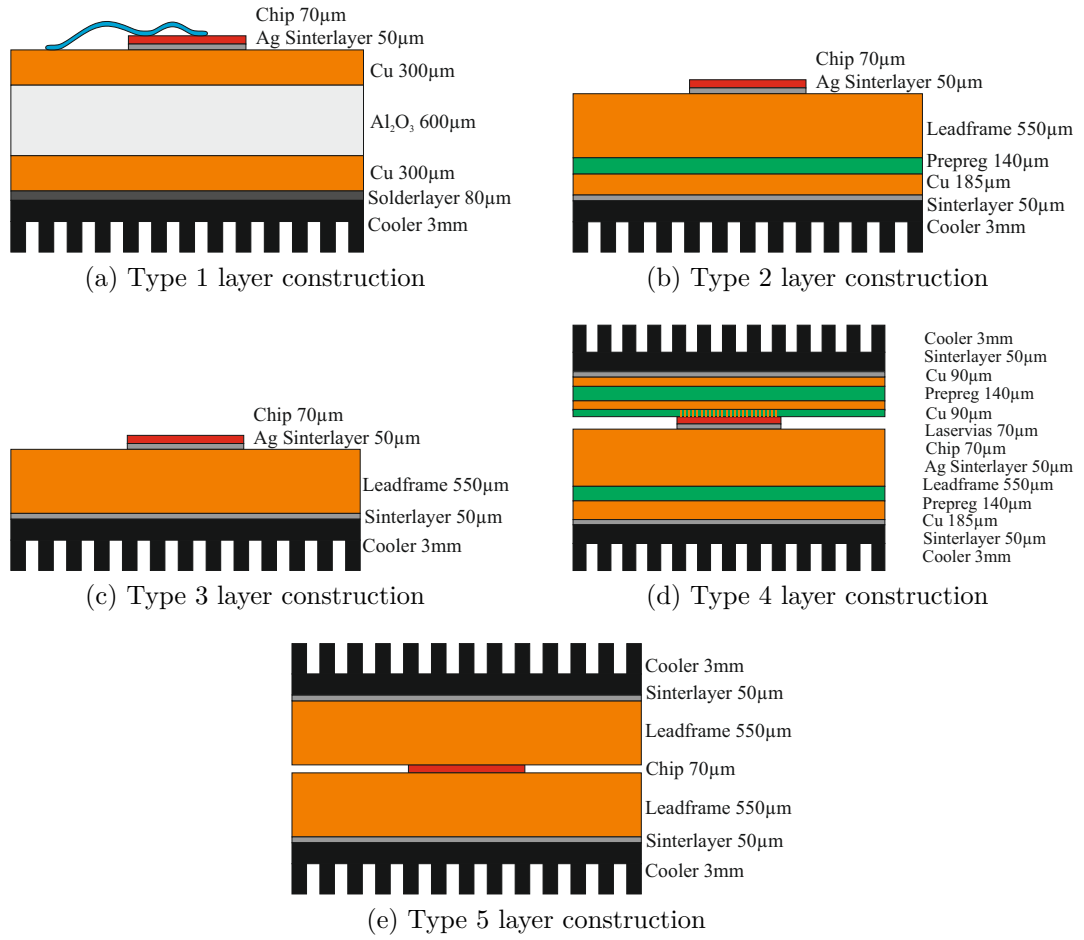


Figure 4.4: Power module layer construction for simulation

4.1.1.4 Type 4

The layer construction is basically the same as for Type 2. However, the top side of the pcb is now also connected to a cooler with a sinter layer.

4.1.1.5 Type 5

The layer construction of the press-pack IGBT module is oriented at the PCB based module without electrical insulation. The sinter joint between chip and leadframe is replaced by a pressure contact and the module is built symmetrically to enable double-sided cooling. The thermal resistance of the pressure contact ($25.7 \text{ kW/m}^2 \cdot \text{K}$) was determined in [87].

4.1.2 Thermal impedance extraction

As shown in Figure 4.3, each IGBT and each diode is built by three parallel chips. Homogeneously distributed static losses (8.93 W/mm^3) are inserted into all three IGBT chips when simulating the thermal impedance of the IGBT. During this, there are no losses in the diode, which means that the thermal impedances of IGBT and diode are simulated independently. In reality, there is a mutual interference between both elements. However, to be comparable with the thermal impedance measurements no interference is considered in the simulation. Moreover, it is shown later that the thermal coupling is negligibly small.

A time dependent study is executed to obtain the time dependent temperature distribution in the module. The thermal impedance from junction to heat sink and from junction to ambient $Z_{\text{th,ja}}$ can then be calculated for the respective device:

$$Z_{\text{th,js}}(t) = \frac{T_j(t) - T_s(t)}{P_{\text{device}}} \quad (4.1)$$

$$Z_{\text{th,ja}}(t) = \frac{T_j(t) - T_a(t)}{P_{\text{device}}} \quad (4.2)$$

$$(4.3)$$

where

T_j = average junction temperature in the respective device

T_s = heat sink temperature 1.5 mm below the respective device (centered position)

T_a = temperature of the cooling fluid

P_{IGBT} = heat dissipation in IGBT (here set at 187.5 W)

P_{diode} = heat dissipation in diode (here set at 84.375 W)

4.1.3 Simulation results

The simulated thermal impedance of each module type is shown in Fig. 4.5 (IGBT), B.1 (diode) and B.5 (RC-IGBT). The differences between the modules are explained with the help of the IGBT diagram without loss of generality: Type 1 and Type 2 show a very similar characteristic. For $t < 3 \cdot 10^{-2} \text{ s}$ Type 2 has a smaller impedance because of its thicker Cu layer nearby the chips (leadframe). However, for greater times $3 \cdot 10^{-2} \text{ s} < t < \infty$ the thermal impedance becomes larger which is due to the worse thermal conductivity of the insulating material.

The thermal resistance ($t \rightarrow \infty$) of Type 4 is less than 60 % of Type 2 due to double-sided cooling. However, for $t < 10^{-1} \text{ s}$ the deviation is much less because the micro-via top side interconnection feature significantly lower thermal capacity compared to the solid leadframe on the chips bottom side.

Type 3 has the lowest thermal impedance for $t < 2$ s because the chips are directly sintered onto the cooler which has a very high thermal capacity. The thermal resistance is a bit worse compared to Type 4 and Type 5 due to the fact that Type 3 only uses single-sided cooling.

The pressure contact of the chips in the Type 5 module is a form-locking interconnection and, thereby, induces a comparatively high thermal resistance nearby the chips. In combination with the small thermal capacity of the chips themselves, this leads to a very high thermal impedance for $t < 10^{-1}$ s. At larger times ($t > 2$ s), the thermal advantages of this module type (double-sided cooling and no electrical insulation layer) appear and lead to a thermal resistance which is as low as Type 4.

4.1.3.1 Thermal equivalent circuits

The simulated thermal impedance is translated to a thermal equivalent circuit from junction to cooling fluid. The Foster networks were obtained by a numerical fitting using the MATLAB CURVE FITTING TOOLBOX. An approach with four RC-elements leads to very accurate fitting results as shown in Fig. 4.5. The fitting parameters for the IGBTs are listed exemplary in Table 4.1 (IGBT). Further fitting parameters are given in Appendix B for the diodes (Table B.1) and the RC-IGBTs (Table B.2).

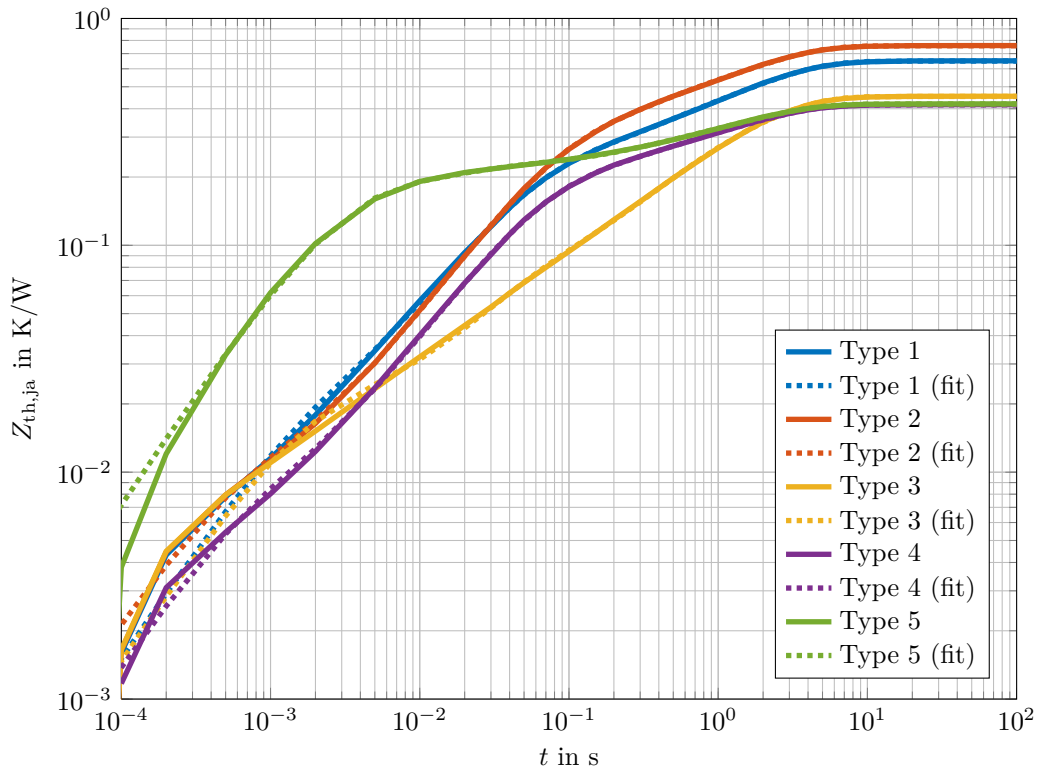


Figure 4.5: IGBT thermal impedance simulation results (Foster fitting)

Table 4.1: Fitting parameter of IGBT thermal impedance curves (Foster model)

	i	1	2	3	4
Type 1	R_i in Ω	$3.31 \cdot 10^{-1}$	$1.98 \cdot 10^{-1}$	$1.17 \cdot 10^{-2}$	$1.09 \cdot 10^{-1}$
	τ_i in s	$2.16 \cdot 10^0$	$4.50 \cdot 10^{-2}$	$1.10 \cdot 10^{-3}$	$3.40 \cdot 10^{-1}$
Type 2	R_i in Ω	$1.51 \cdot 10^{-1}$	$7.55 \cdot 10^{-3}$	$3.52 \cdot 10^{-1}$	$2.48 \cdot 10^{-1}$
	τ_i in s	$3.01 \cdot 10^{-1}$	$4.04 \cdot 10^{-4}$	$2.05 \cdot 10^0$	$6.14 \cdot 10^{-2}$
Type 3	R_i in Ω	$9.60 \cdot 10^{-2}$	$1.73 \cdot 10^{-2}$	$2.95 \cdot 10^{-1}$	$4.53 \cdot 10^{-2}$
	τ_i in s	$4.05 \cdot 10^{-1}$	$1.27 \cdot 10^{-3}$	$1.93 \cdot 10^0$	$3.88 \cdot 10^{-2}$
Type 4	R_i in Ω	$1.71 \cdot 10^{-1}$	$7.13 \cdot 10^{-2}$	$1.69 \cdot 10^{-1}$	$5.47 \cdot 10^{-3}$
	τ_i in s	$1.88 \cdot 10^0$	$2.74 \cdot 10^{-1}$	$4.98 \cdot 10^{-2}$	$4.93 \cdot 10^{-4}$
Type 5	R_i in Ω	$4.69 \cdot 10^{-2}$	$4.90 \cdot 10^{-2}$	$1.55 \cdot 10^{-1}$	$1.69 \cdot 10^{-1}$
	τ_i in s	$2.96 \cdot 10^{-1}$	$1.61 \cdot 10^{-2}$	$1.85 \cdot 10^0$	$2.42 \cdot 10^{-3}$

When using the thermal equivalent circuit for thermo-electrical simulations of power electronics circuits (inverter, dc-dc-converter, ...) the models of the IGBT and the diode have to be combined to account for the fact that they share the same cooler. However, the Foster models are only valid for the specific system for which they were fitted. Modifications lead to significant inaccuracies [8][9]. The only possibility to combine the thermal equivalent circuits of IGBT and diode is the use of Cauer models, because they represent the physical construction of the modules. The derivation of the Cauer models was done by using one RC-element for each physical layer of the respective module. The value of each element was chosen according to its material properties and the layer geometry. The step response of the resulting circuit was simulated in PLECS and compared to the thermal impedance from the thermal FEM simulation. One or two elements still had to be tuned to obtain good fitting results because the starting element values did not account for effects like heat spreading. The Cauer models were **not** built for Type 3 and 4 as they were not used for the thermal-electric system simulations in chapter 5.

The fitting curves in Fig. 4.6 and Fig. B.2 show that the physical approach leads to less accurate fitting results compared to the numerical method. However, it can be used for system simulations because larger deviation are only present in the range $10^{-4} \text{ s} < t < 10^{-3} \text{ s}$.

The resulting thermal equivalent circuits can be found in Fig. 4.7 (Type 1 with single chips for IGBT and diode) and Fig. 4.8 (Type 1 with RC-IGBT). In Appendix B the Cauer circuit models are given for Type 2 with single chips (Fig. B.6), Type 2 with RC-IGBT (Fig. B.7), Type 5 with single chips (Fig. B.8) and Type 5 with RC-IGBT (Fig. B.9).

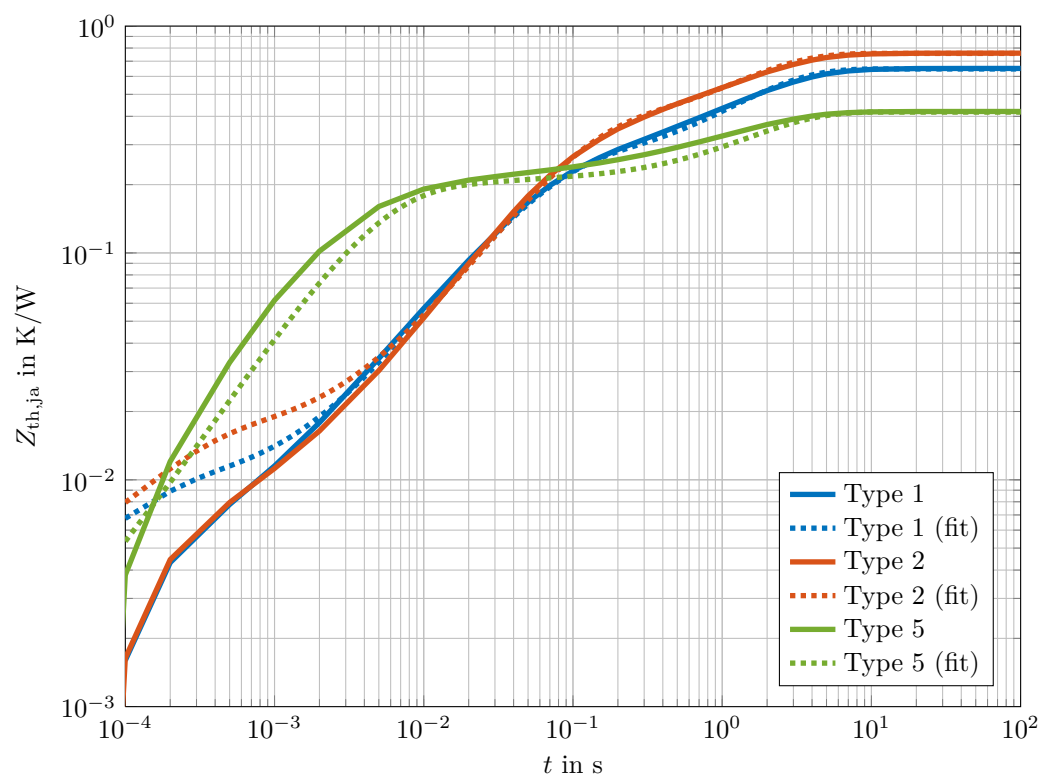


Figure 4.6: IGBT thermal impedance simulation results (Cauer fitting)

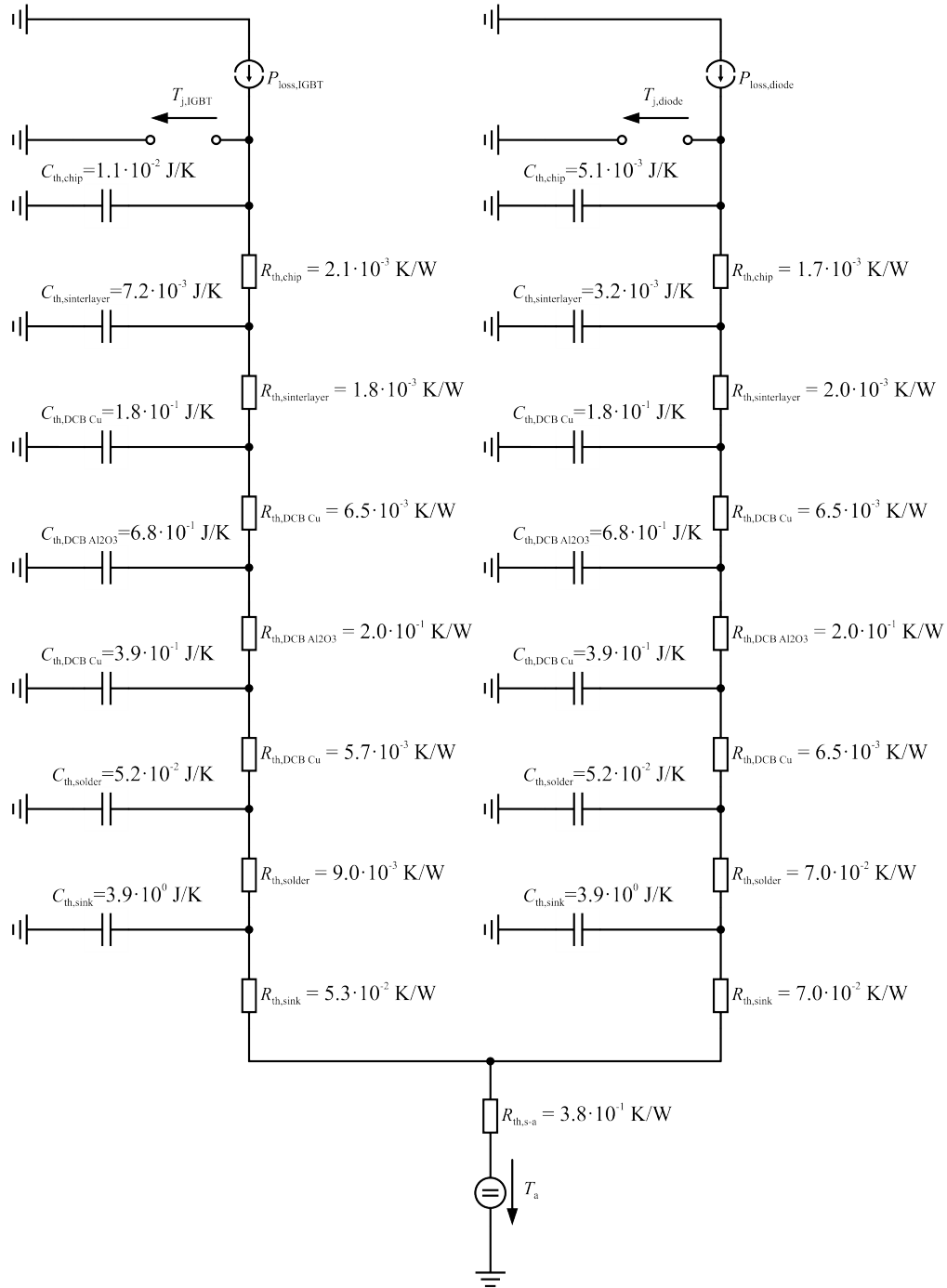


Figure 4.7: Cauer thermal equivalent circuit for Type 1 module

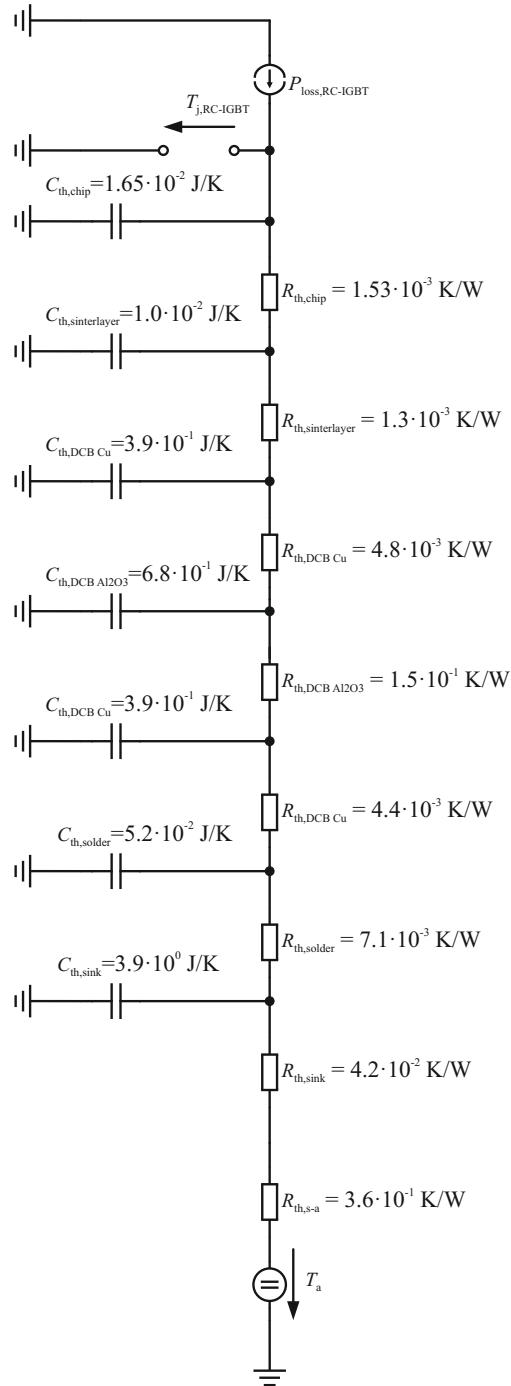


Figure 4.8: Cauer thermal equivalent circuit for Type 1 module with (RC-IGBT)

4.1.3.2 Heat spreading

Heat spreading describes the effect of lateral heat flow within the layers of a power module. It particularly occurs if a layer of high thermal conductivity is followed by a layer of low thermal conductivity. In the highly conductive layer the heat is forced to flow planar, thus, increasing the effective area A for the heat flow (compare Fig. 2.1). This leads to a reduced thermal resistance of the system. The heat spreading capability of a certain layer can either be improved by increasing the lateral thermal conductivity or by increasing the thickness of the highly conductive material. At first sight, the latter contradicts Eq. 2.2 but this equation is only valid for one-dimensional geometries. The heat spreading capability of the different module types can be analyzed by simulating the thermal resistance with varying module area. Only the area of the die and the die attach are kept constant. Fig. 4.9 shows that up to a width of approximately 50 mm the thermal resistance of all modules is decreased. A further increase does not improve the thermal resistance further. To compare the heat spreading capability of the module types the heat spreading index (HSI) is introduced. It is defined as the ratio between thermal resistance without heat spreading $R_{th,ja,0}$ and thermal resistance with maximum heat spreading $R_{th,ja,min}$.

$$HSI = \frac{R_{th,ja,0}}{R_{th,ja,min}} \quad (4.4)$$

Fig. 4.10 gives an overview of the HSI's. Obviously, Type 3 features the best heat spreading capability. The reason for this is the absence of a low-conductive insulation layer which allows the heat to spread efficiently within the thick cooler, whereas, Type 1, 2 and 4 mainly use the relatively thin Cu layer above the insulator for heat spreading. The poor heat spreading performance of Type 5 is due to the fact that a high portion of the thermal resistance is defined by the pressure contact die attach. This part of the thermal resistance is not improved when increasing the modules area because the chip size is kept constant.

The effect of increasing the thickness of the highly conductive material is investigated in Fig. 4.11. Here, the thermal resistance of a Type 2 module with varying leadframe thickness is shown. At the lowest width the thermal resistance increases with higher leadframe thickness because here the heat flow can be considered to be one-dimensional. Up to 20 mm the heat spreading does not depend on the leadframe thickness even though the thermal resistance is already reduced by a factor of 2 at this point. Only at higher width the thicker leadframe results in an improved heat spreading which can also be seen in Fig. 4.12.

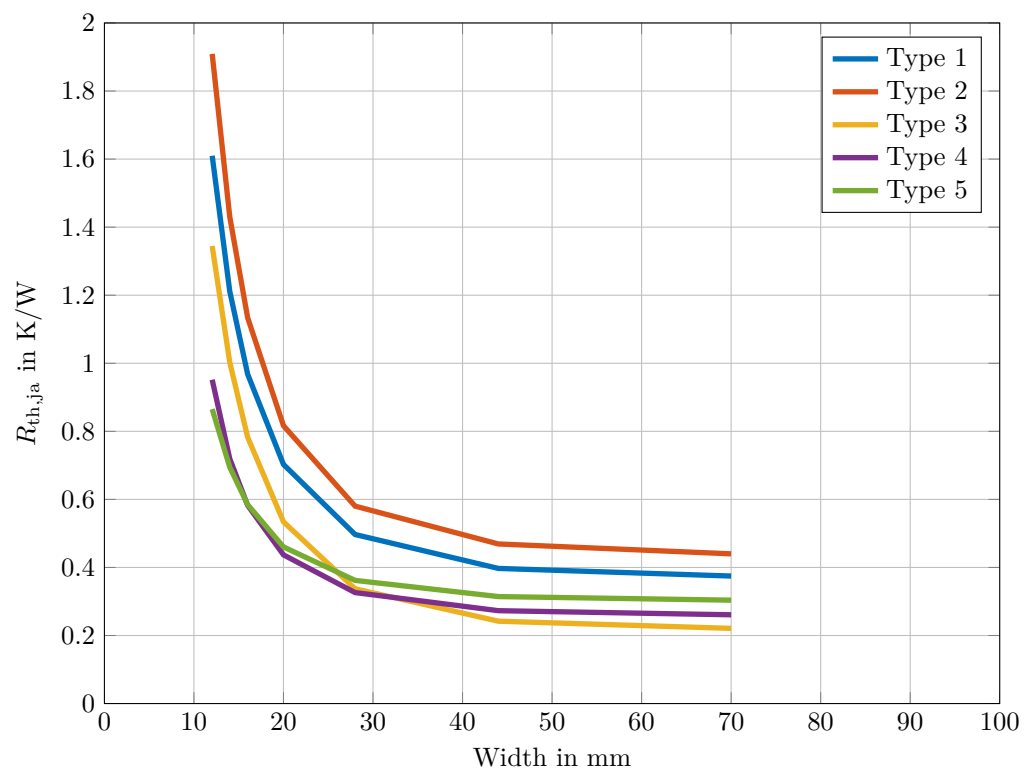


Figure 4.9: Heat spreading capability of different types of modules

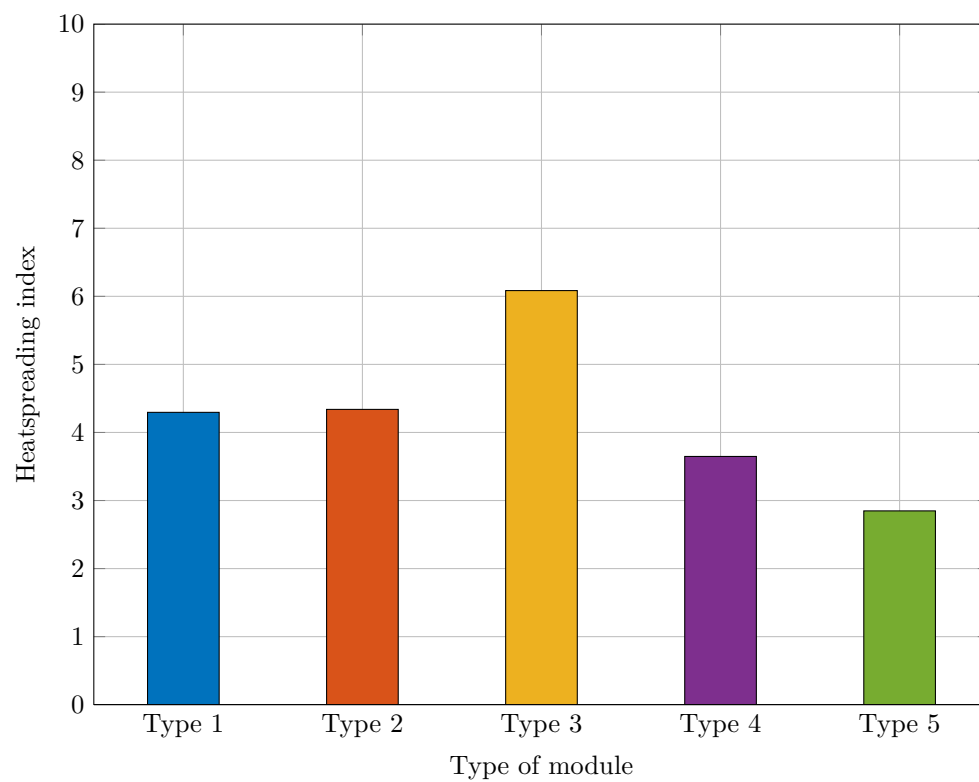


Figure 4.10: Heat spreading index of different types of modules

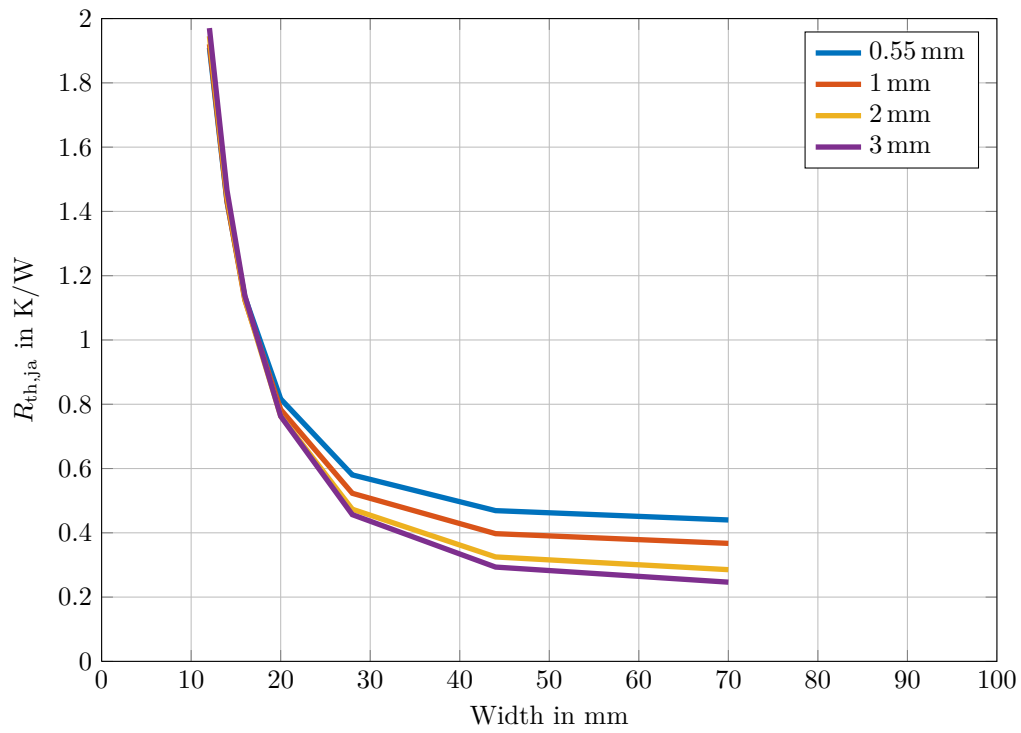


Figure 4.11: Heat spreading capability of Type 2 module with different leadframe thickness

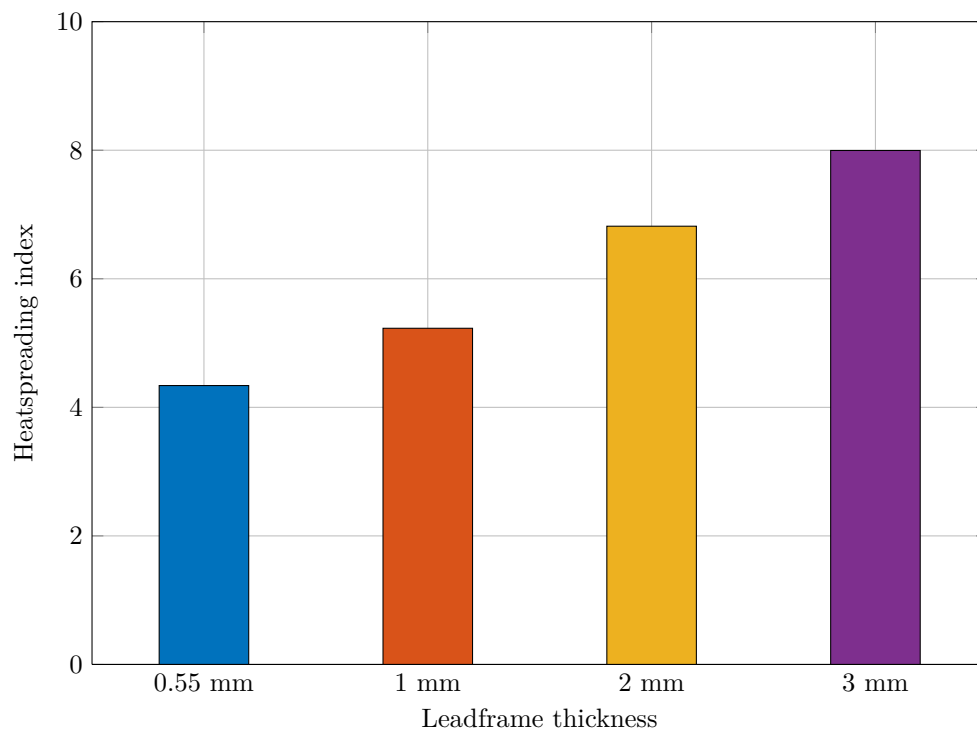


Figure 4.12: Heat spreading index of Type 2 module with different leadframe thickness

4.2 Thermal measurement

The verification of the simulation results was done by measuring the thermal impedance of the power modules on a test bench whose structure is depicted in Fig. 4.13. The semiconductor junction temperature is measured indirectly via the forward voltage V_{CE} at a small measurement current I_{meas} (here: 100 mA), whereupon, the dependency of the voltage from the temperature has to be calibrated in a temperature chamber in advance. The measurements starts with loading the semiconductor with a high dc current I_{load} to heat it up while the power module is actively cooled. After reaching thermal equilibrium the load current is switched off within max. 100 μs and only the measurement current is flowing through the semiconductor. This allows the recording of the semiconductor temperature while cooling down. As the cool down process is symmetric to the heat up it can be used to determine the thermal step response of the module which is identical to the thermal impedance.

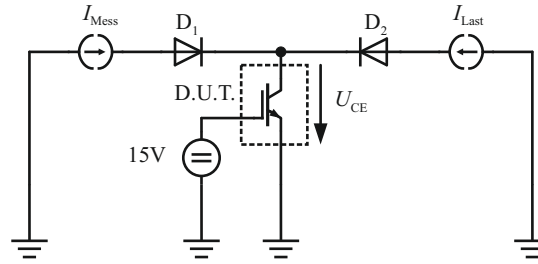


Figure 4.13: Test bench for thermal impedance measurements

The thermal impedances of three power modules were measured: The DCB based module (Type 1), the PCB based module with single sided cooling and electrical insulation (Type 2) and the press-pack module (Type 5). Type 1 and 2 can be used to verify the simulation results. The Type 5 prototype deviates significantly from the simulated construction. Hence, it could only be used to parameterize the simulation model. The results are shown in Fig. 4.14 and 4.15. Due to the fact that the simulation was done with only one IGBT or diode, respectively, the measurement results are multiplied with three to be comparable to the simulation.

For $t < 10^{-2}$ s the simulation results meet the measurements very accurately. For larger times, the simulation overestimates the thermal impedance significantly for both module types. The measured thermal resistance ($t \rightarrow \infty$) is 20 – 50 % below the prediction from simulation. Possible reasons for this deviation are

- inaccuracies of the physical properties of the used materials
- inaccuracies of the thermal impedance measurements
- non-ideal material joints
- additional heat spreading capability of the real module

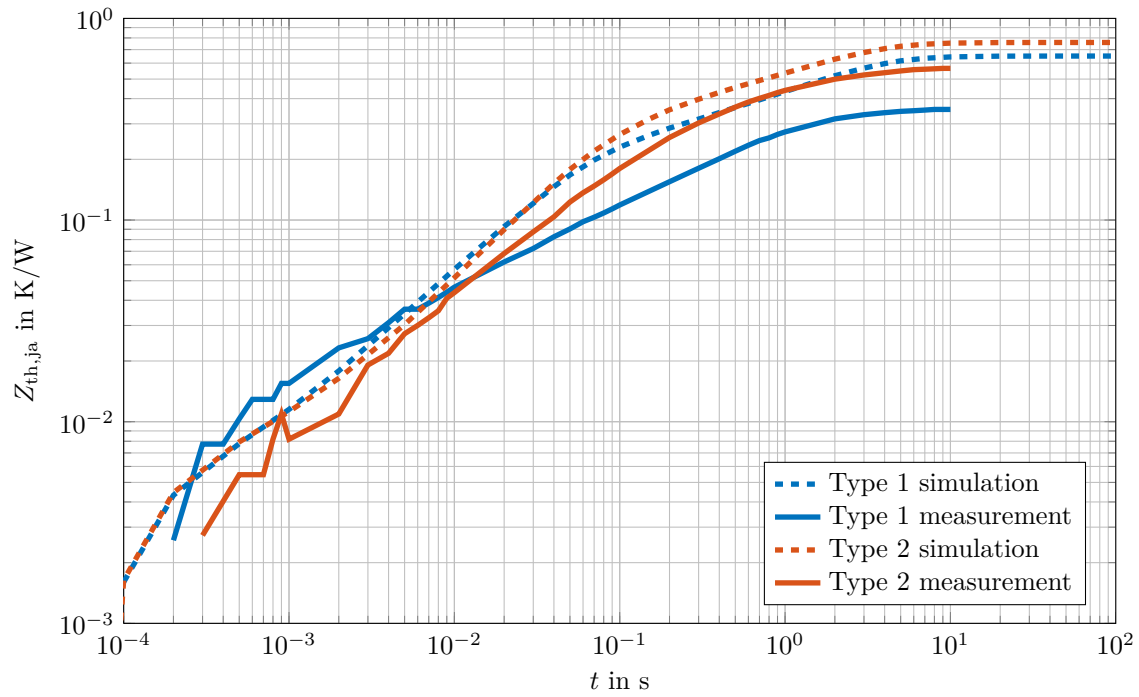


Figure 4.14: IGBT thermal impedance measurement results

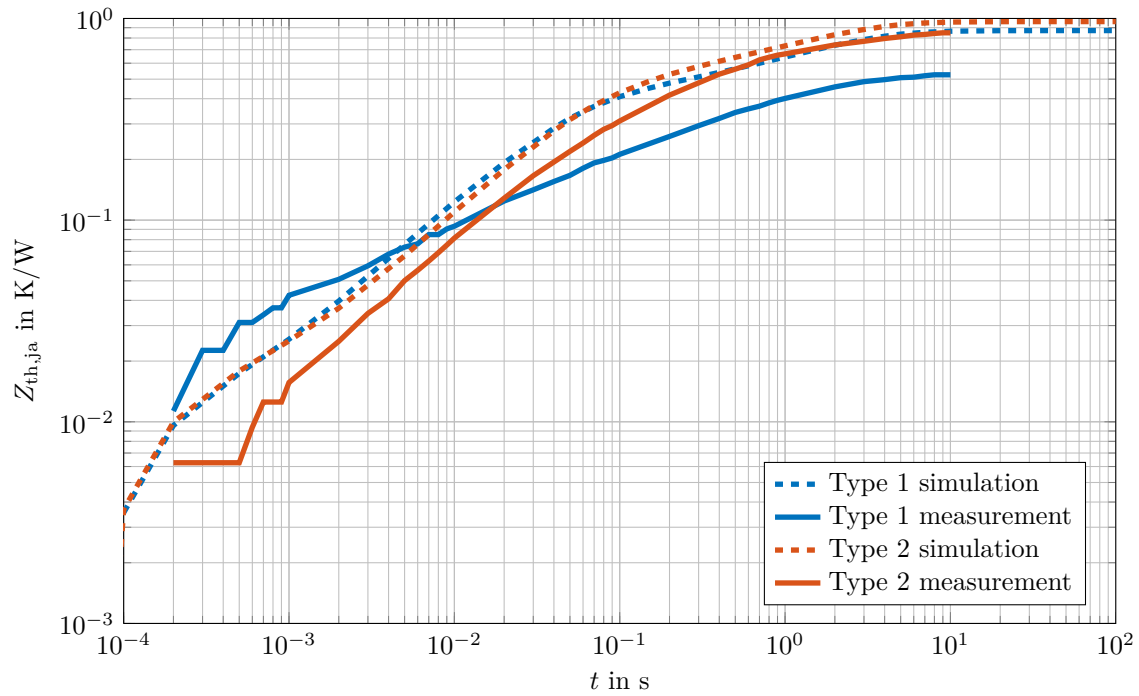


Figure 4.15: Diode thermal impedance measurement results

4.3 Electrical simulation

The design of power modules with chip embedding offers the potential of building switching cells with very low inductances. The switching cell inductance causes overvoltages during power semiconductor turn-off and is also referred to as dc-link inductance. The dc-link inductance of the prototype for the HI-LEVEL project is designed by means of FASTHENRY, a 3D PEEC (partial element equivalent circuit) calculation tool. The PEEC method has been introduced by Ruehli in 1974 [88].

Basically, a small dc-link inductance of power modules can be realized by following the busbar principle. In Figure 2.6 a typical busbar geometry is shown, with an approximation of the structures inductance in Eq. 2.13. According to this, the interconnections between dc-link capacitor and semiconductor have to be built as short ($l \searrow$), as wide ($w \nearrow$) and as close ($d \searrow$) as possible. However, the internal interconnection structure of the most power modules is not built using the busbar principle. Thereby, usually only the inductance of the interconnection between dc-link capacitor and module can be reduced by the inverter design engineer. The inductance of the module stays in the range of 10 – 20 nH and limits the minimum dc-link inductance. Some modules even feature an internal busbar design but still the packaging structure of DCB and bond wires prevents a strict busbar design. This obstacle can be overcome by the chip embedding packaging concept. This concept allows for planar interconnections all over the module, even on top of the chips. Additionally, the dc-link capacitor can be placed on the top layer of the PCB and is thereby very close to the switching cell. The cross section of a possible configuration is shown in Figure 4.16.

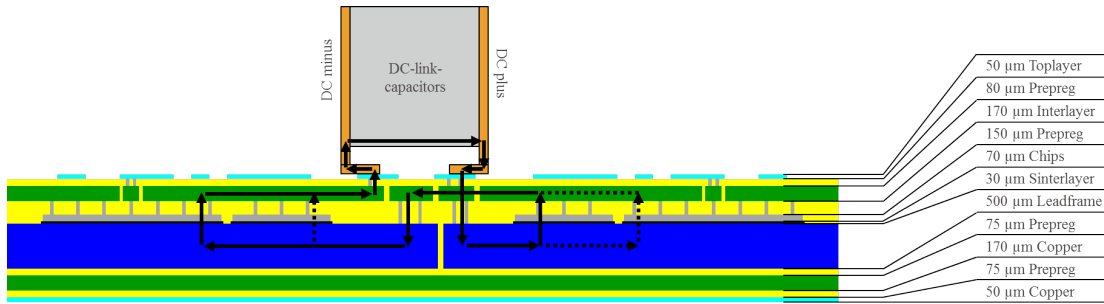


Figure 4.16: Crosssection of the switching cell

The inductance of this structure was simulated while varying different parameters to show how much the inductance can be reduced and which parameters are most sensitive. Fig. 4.17 shows the simulated FASTHENRY geometry.

The simulation start with a reasonable set of parameters ($b_k = 40$ mm, $l_k = 18$ mm, $h_k = 2$ mm, compare Fig. 4.17). The influence of their variation on the dc-link inductance is investigated in the following.

The width of the commutation cell does not affect the area that is spanned by the commutation current. However, it influences the dc-link inductance anti-proportionally. The width of the cooled area in the module is 138 mm while the

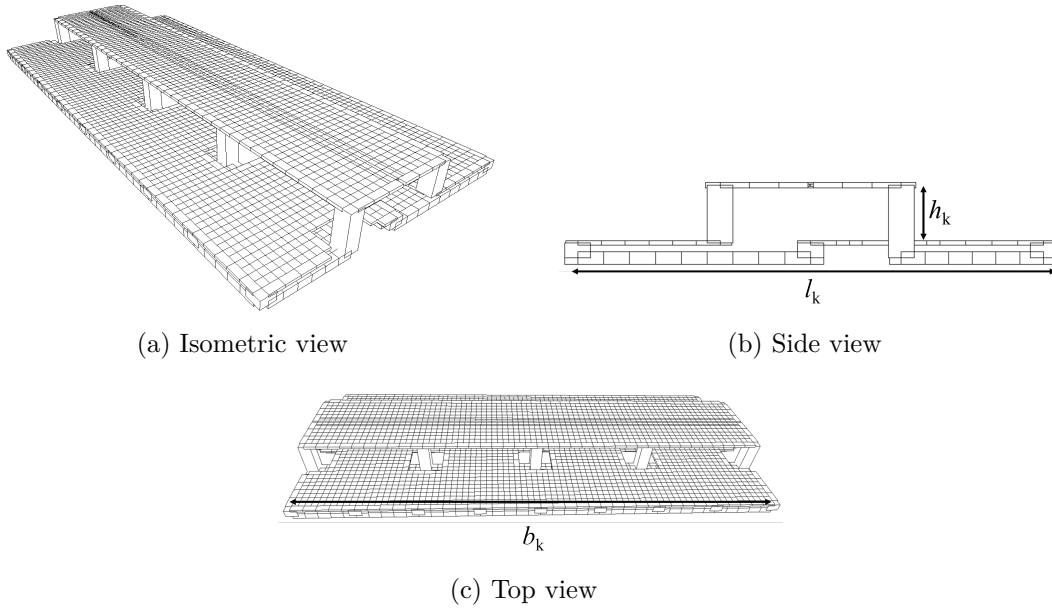


Figure 4.17: Geometry of the commutation cell in PEEC-simulation

module overall width is 174 mm. Subtracting the area needed for the driver contacts, each halfbridge has a maximum width of 40 mm. Fig. 4.18 shows that this width should be fully utilized, whereas a larger commutation cell does not make sense because above 40 mm the dc-link inductance only decreases slightly with increasing width.

Placing all chips as closely together as possible, the length of the commutation cell is only 10 mm. In this case the dc-link inductance reduces to 1 nH (Fig. 4.19). However, a compromise has to be found between a small inductance (close chip placement) and a good cooling performance (wide chip placement to utilize heat spreading). Extending the chips in longitudinal direction leads to a linear increase of the dc-link inductance according to Eq. 2.13.

The area spanned by the capacitors above the PCB contributes significantly to the dc-link inductance according to Fig. 4.20. At the starting value of 2 mm, which corresponds to the real capacitors, the dc-link inductance is 1 nH. By an optimization of the capacitor packaging, a value of 0.5 nH could theoretically be reached. However, this is not possible due to the fixed capacitor design.

Simulation shows that $b_k = 40$ mm, $l_k = 18$ mm are suitable design parameters for the switching cell construction that are used for the HI-LEVEL prototype. The expected dc-link inductance is 1 – 1.5 nH, depending on the dominating frequency.

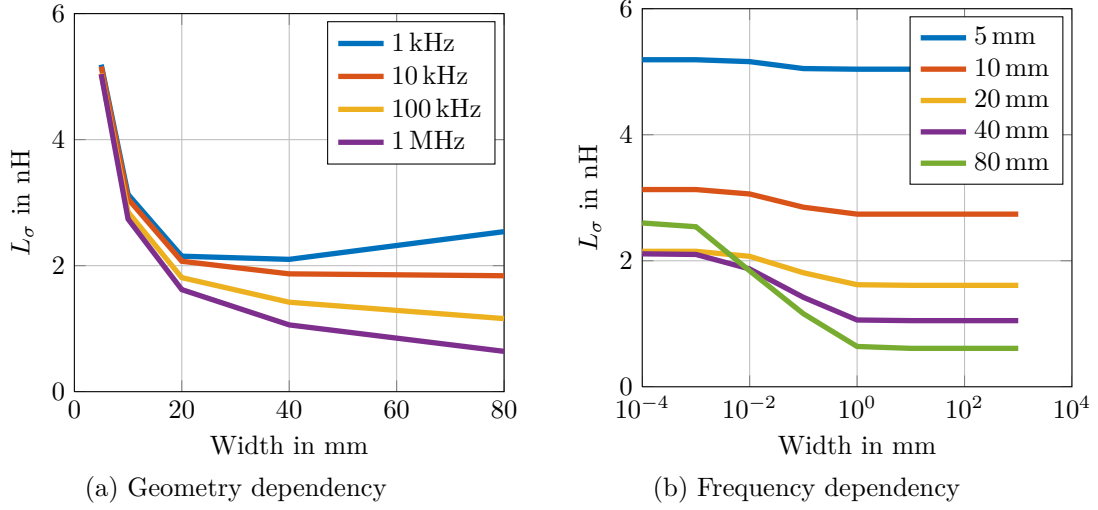


Figure 4.18: Dc-link inductance in dependency of the commutation cell width

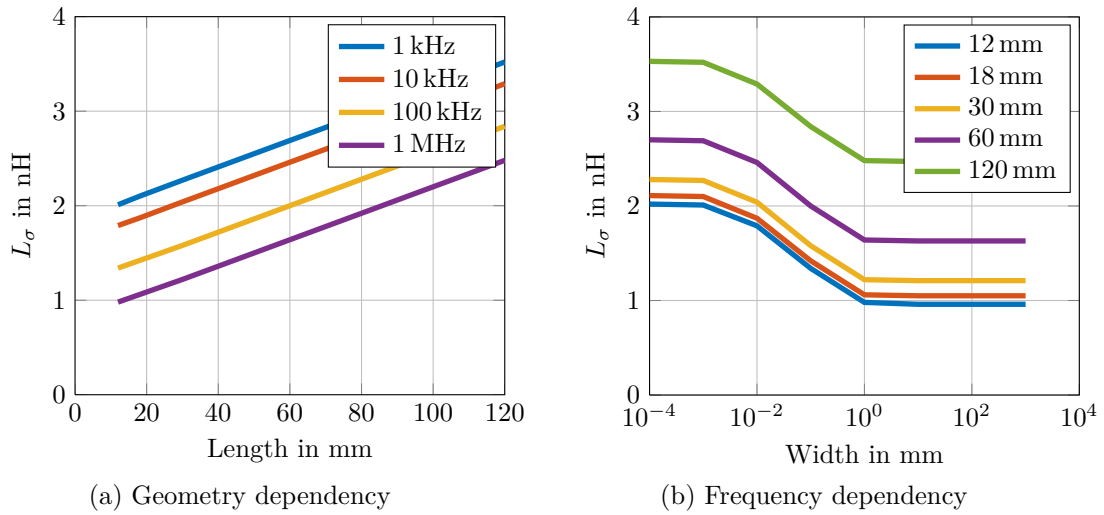


Figure 4.19: Dc-link inductance in dependency of the commutation cell length

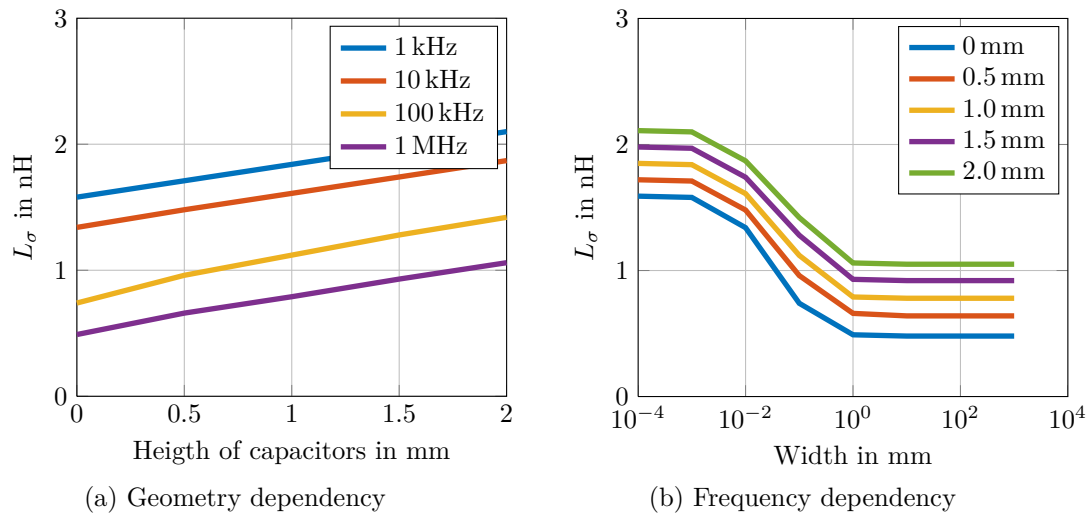


Figure 4.20: Dc-link inductance in dependency of the capacitor height

4.4 Electrical measurement

The CONTINENTAL EPF2-3 (Type 1 module) and the HI-LEVEL demonstrator (Type 2) are electrically investigated. The static and dynamic behavior of both modules, namely output characteristic and switching losses, are extensively tested. The switching characteristics are used to determine the dc-link inductance which is used to verify the switching cell design procedure (section 4.3). Finally, the EMC performance is measured.

4.4.1 Output characteristic

In turn-on state, the IGBT conducts the current I_C from collector to emitter, leading to a forward voltage drop V_{CE} . The relation between V_{CE} and I_C is called output characteristic and describes the conduction behavior of the IGBT. The product of V_{CE} and I_C results into the conduction losses. The same is true for the diode, whose forward voltage and current are called V_F and I_F , respectively.

The measurement of the output characteristics is done on a test bench that was constructed during the HI-LEVEL project [83]. Its structure is depicted in Fig. 4.21. This test bench allows to establish and afterwards decrease the semiconductor forward current within a sufficiently short time, i.e. without significant self-heating of the device under test. A prior setup of the test temperature is done with a heating plate (for temperatures $> 25^\circ\text{C}$) and in a temperature chamber (for temperatures $< 25^\circ\text{C}$), respectively. During the current reduction phase, the device current and voltage are measured simultaneously yielding the output characteristic of the device under test. The current ramp-up phase is not suitable for the measurement because of a voltage oscillation at the beginning of the current buildup.

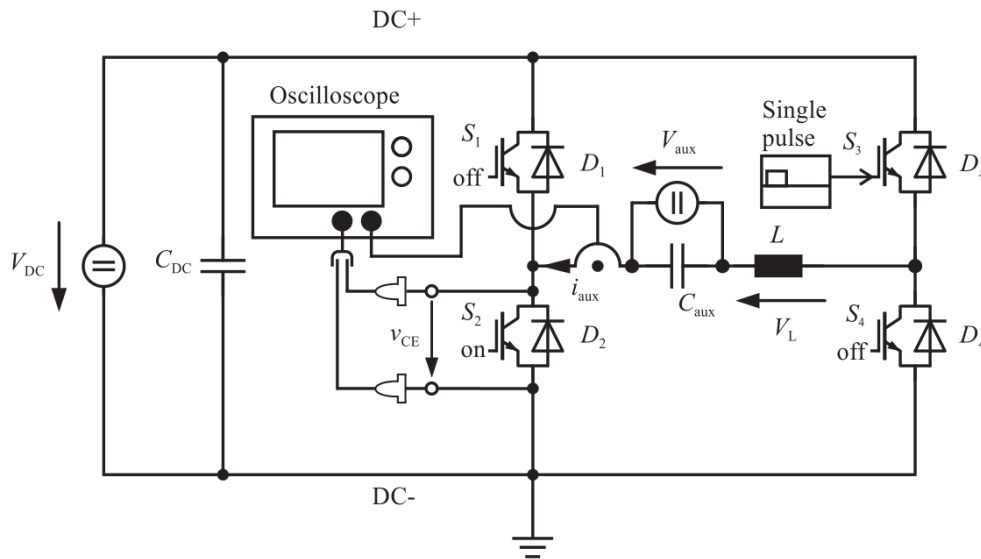


Figure 4.21: Schematic of the test bench for measuring the output characteristic of IGBT and diode, from [89]

Fig. 4.22 shows the measured output characteristics of IGBT and diode in the Type 1 module. Both semiconductors feature a threshold voltage up to which no current flow is detected. Above this voltage the current rises nearly linearly with increasing forward voltage.

The diode forward voltage has a negative temperature coefficient in the complete measured current range. At low currents this is caused by the rising intrinsic charge carrier density that reduces the voltage at the pn-junction at higher temperatures [42]. At high currents the temperature dependency of the voltage across the drift region V_{drift} (Eq. 4.5 with the thickness w_B of the drift region) is dominating with two opposing effects. Firstly, the charge carrier mobilities μ_n and μ_p decrease with rising temperature ($\rightarrow$ increase of V_{drift}). Secondly, the charge carrier lifetime τ_{eff} rises with increasing temperature ($\rightarrow$ decrease of V_{drift}).

$$V_{\text{drift}} = \frac{w_B^2}{(\mu_n + \mu_p) \cdot \tau_{\text{eff}}} \quad (4.5)$$

The resulting temperature coefficient, therefore, depends on the diode technology. The measured characteristic indicates the use of radiation-induced recombination centers because the forward characteristic intersects approximately at nominal current (600 A). Moreover, the temperature coefficient is relatively low ($\approx -2 \text{ mV/K}$). Diodes without recombination centers have an intersection point at much higher current densities. Diodes diffused with platinum do not intersect at all and have a temperature coefficient that is usually significantly higher than -2 mV/K .

The temperature dependency of the IGBT output characteristic is based on the same effect as for the diode. At low current the voltage at the pn-junction dominates and, therefore, the temperature coefficient is negative. At high currents it has to be distinguished between PT-IGBTs (punch-through IGBT) and NPT-IGBTs (non-punch-through IGBT). The influence of the charge carrier lifetime dominates in PT-IGBTs, leading to a negative temperature coefficient. In a NPT-IGBT the voltage across the drift region is dominated by the mobilities which cause a positive temperature coefficient at higher currents. Hence, the evaluated IGBT can be classified as NPT-IGBT. The intersection point of the output characteristic at different temperatures is located at 200 A.

The Type 2 module uses the same semiconductor chips. Consequently, the output characteristic (Fig. 4.23) generally equals Type 1. Above the threshold voltage the forward voltage rises less with increasing current compared to Type 1.

In a direct comparison (Fig. 4.24) this difference becomes more obvious. The deviation of forward voltage increases linearly with rising current. This indicates a smaller ohmic portion in the Type 2 module which is caused by the absence of bond wires. From the bond wire geometry (compare Fig. 4.3) and the electrical conductivity of Aluminum σ_{Al}

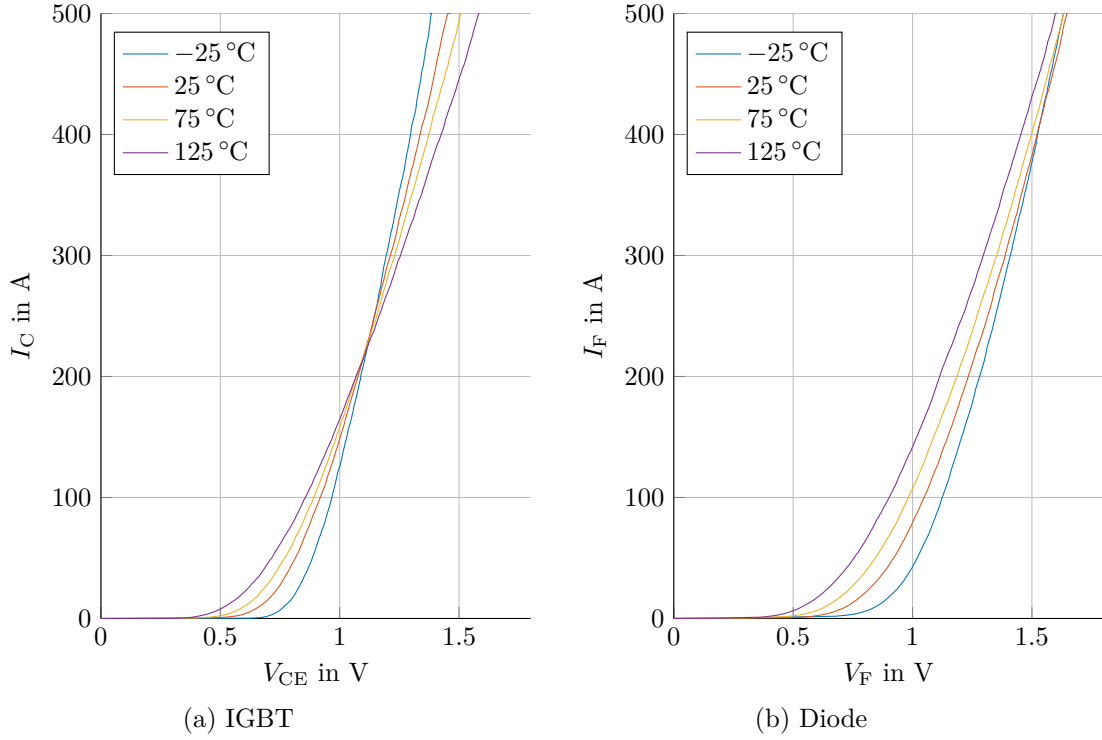


Figure 4.22: Measured output characteristic (Type 1)

$$l = 15 \text{ mm} \quad \text{bond wire length} \quad (4.6)$$

$$d = 400 \text{ } \mu\text{m} \quad \text{bond wire thickness} \quad (4.7)$$

$$N = 24 \quad \text{bond wires in parallel} \quad (4.8)$$

$$\sigma_{\text{Al}} = 37 \cdot 10^6 \frac{\text{S}}{\text{m}} \quad (4.9)$$

the expected bond wire resistance is

$$R_{\text{bondwire}} = \frac{1}{N} \cdot \frac{1}{\sigma_{\text{Al}}} \cdot \frac{l}{\pi \frac{d^2}{4}} \approx 0.5 \text{ m}\Omega \quad (4.10)$$

Using the measurement curves the difference in resistance between the modules can be estimated to $0.4 \text{ m}\Omega$ for both, IGBT and diode. This suits very well to the expected value (Eq. 4.10). Carrying an effective current of 200 A , exemplary, the losses in the bond wires will be 16 W for one IGBT leading to reduced (by roughly 7.5%) conduction losses of the Type 2 module.

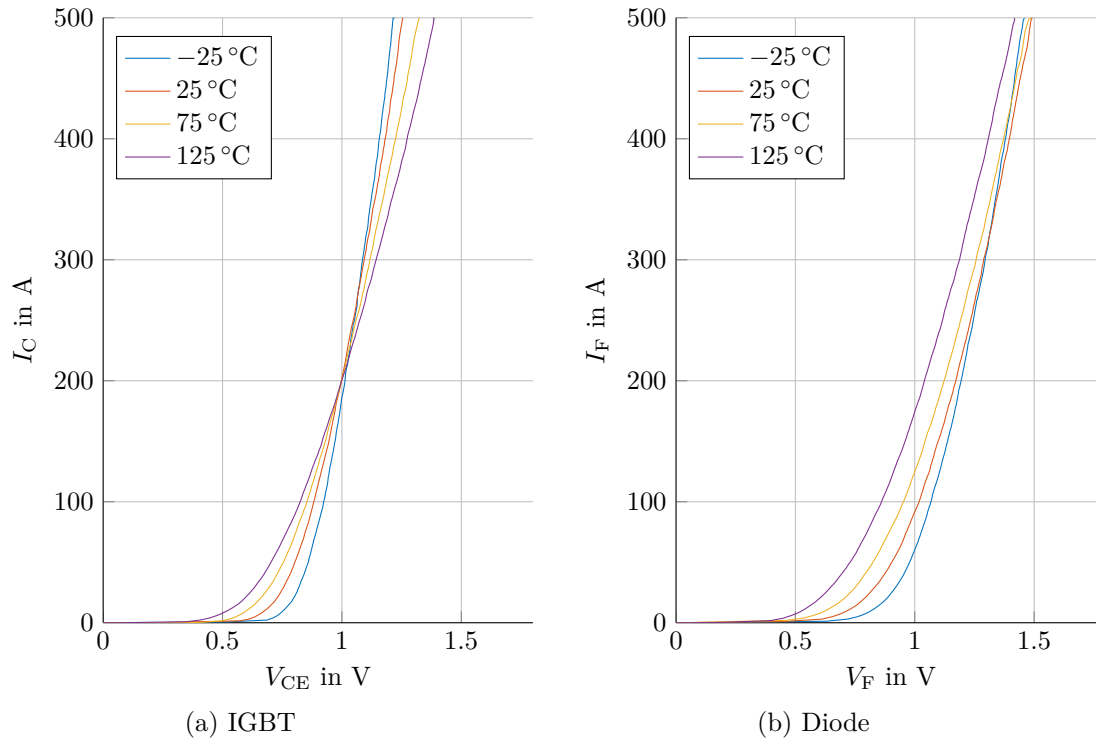


Figure 4.23: Measured output characteristic (Type 2)

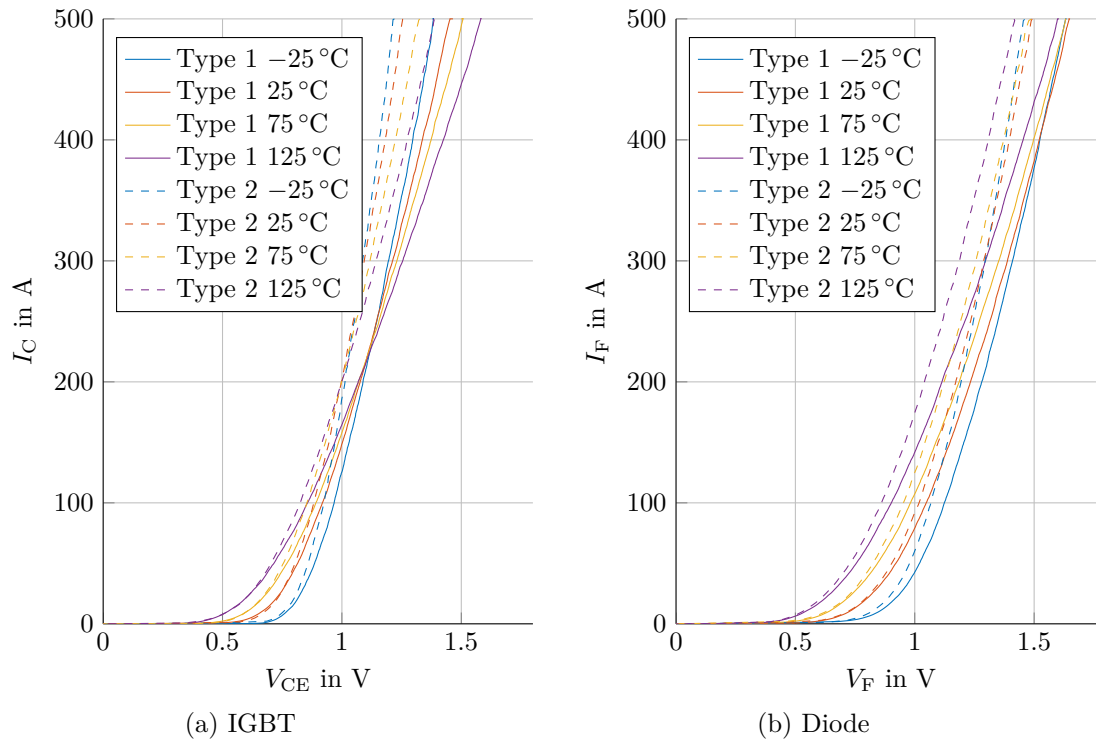


Figure 4.24: Measured output characteristic (Comparison of Type 1 and 2)

4.4.2 Switching characteristic

The double-pulse test stand depicted in Fig. 4.25 was used to record the switching behavior of the examined modules

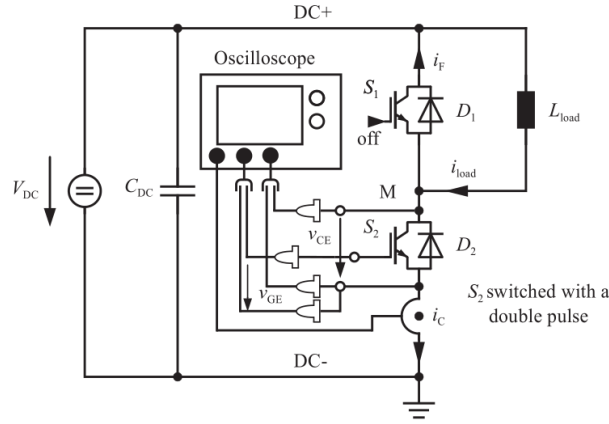


Figure 4.25: Double-pulse test bench for switching loss measurements [89]

4.4.2.1 Turn-off

During the hard turn-off of the IGBT an overvoltage occurs between collector and emitter caused by the stray inductance of the commutation cell (dc-link inductance) that has to be (de-)magnetized when turning current on or off.

In Fig. 4.26 the turn-off characteristic of the Type 1 module is shown. Focus is on the comparison of different turn-off currents. The turn-off overvoltage rises with increasing current due to a higher steepness of the current. Below 150 A the $\frac{dv}{dt}$ of the collector-emitter voltage is reduced. This behavior is caused by the stored charge effect of modern Trench-Field-Stop IGBTs which is described in [90].

The temperature dependency of the turn-off characteristic is shown in Fig. 4.27. It can be seen that the rise time of the voltage is smaller at low temperatures causing less switching losses. In contrast the current slope and, consequently, also the overvoltage is independent of temperature.

The low dc-link inductance of the Type 2 module leads to an extensive reduction of the turn-off overvoltage. However, the dependency of the turn-off current is still visible (Fig. 4.28).

The temperature dependency of the Type 2 turn-off process is also characterized by a steeper voltage slope (at low temperatures) and a temperature independent turn-off overvoltage (Fig. 4.29).

The direct comparison of both evaluated modules (300 V in Fig. 4.30 and 400 V in Fig. C.4) additionally shows the momentary power loss as product of voltage and current. Here it becomes visible that the rise time of the collector-emitter voltage is slightly shorter for the Type 2 module. Consequently, the maximum of the power losses is reached earlier. The following steeper current decrease leads to a significantly reduced turn-off losses of Type 2.

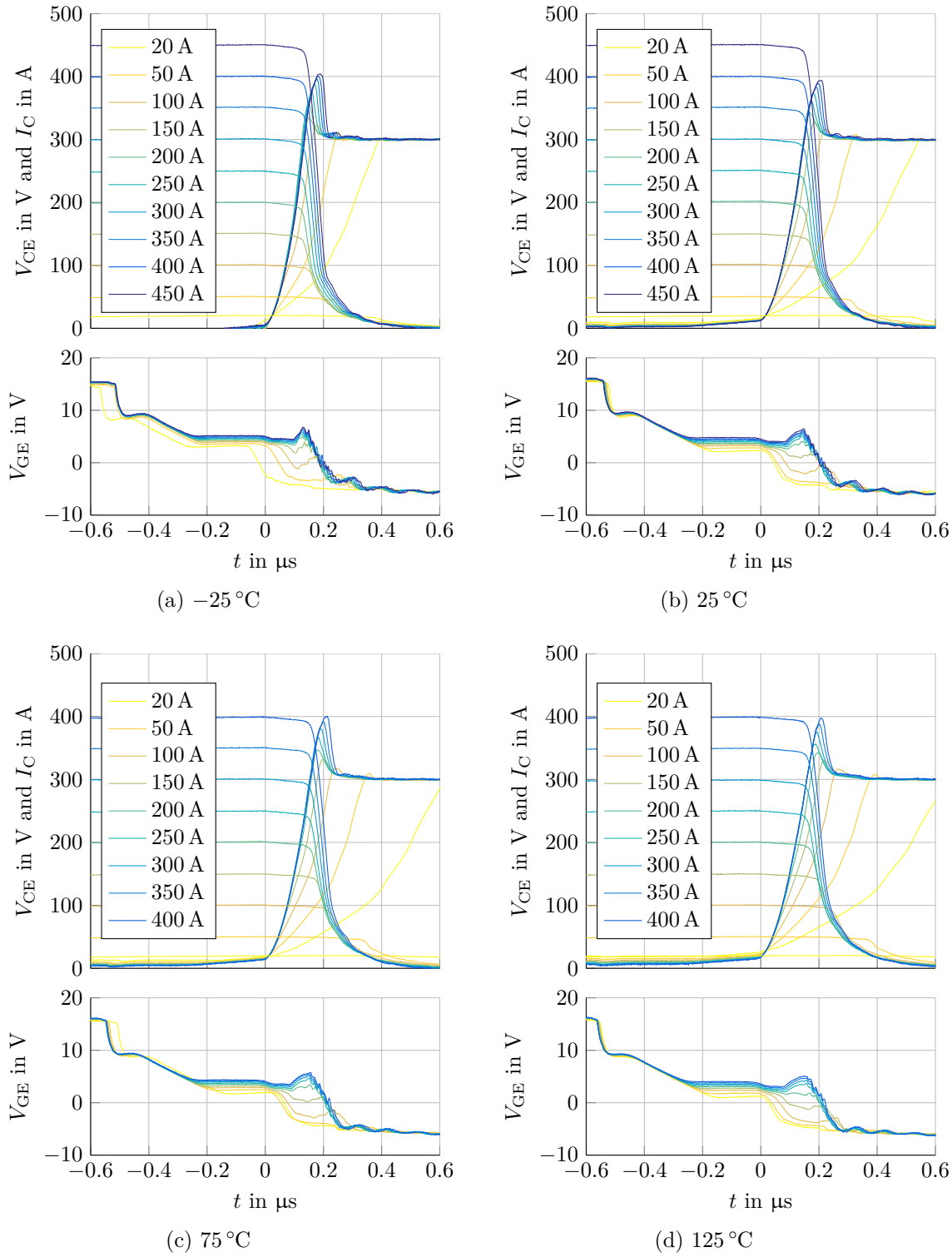


Figure 4.26: Turn-off Type 1 at 300 V

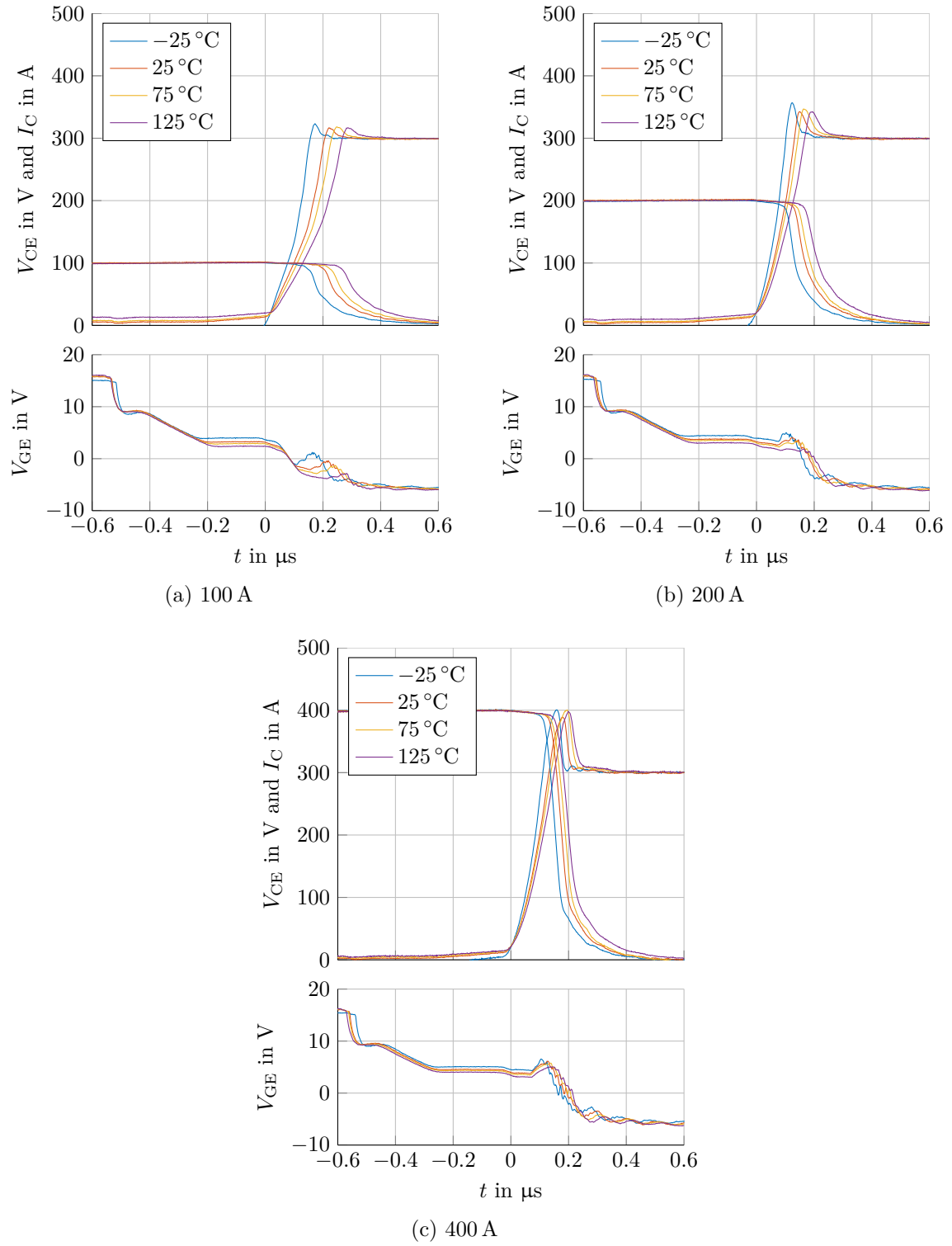


Figure 4.27: Turn-off Type 1 at 300 V

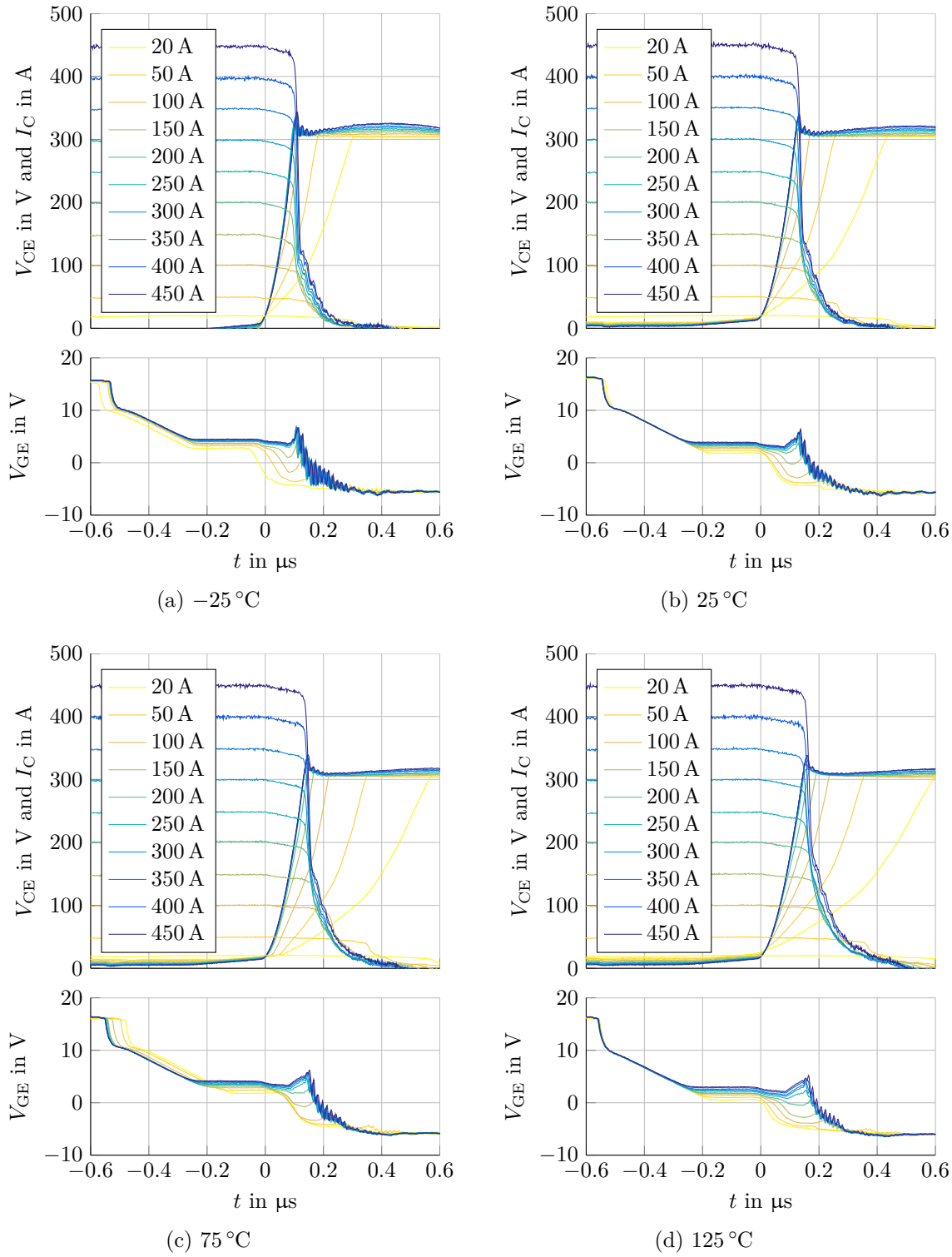


Figure 4.28: Turn-off Type 2 at 300 V

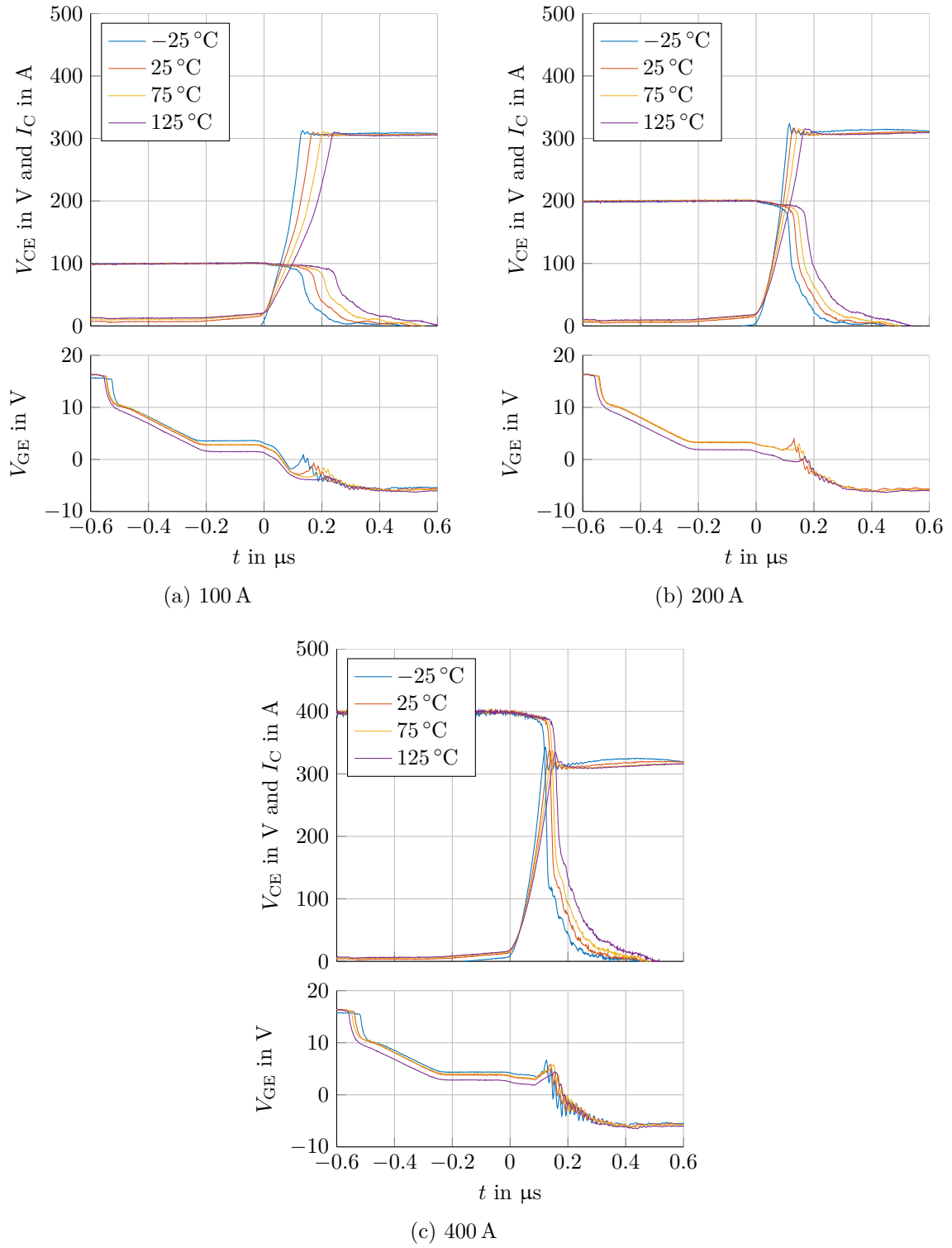


Figure 4.29: Turn-off Type 2 at 300 V

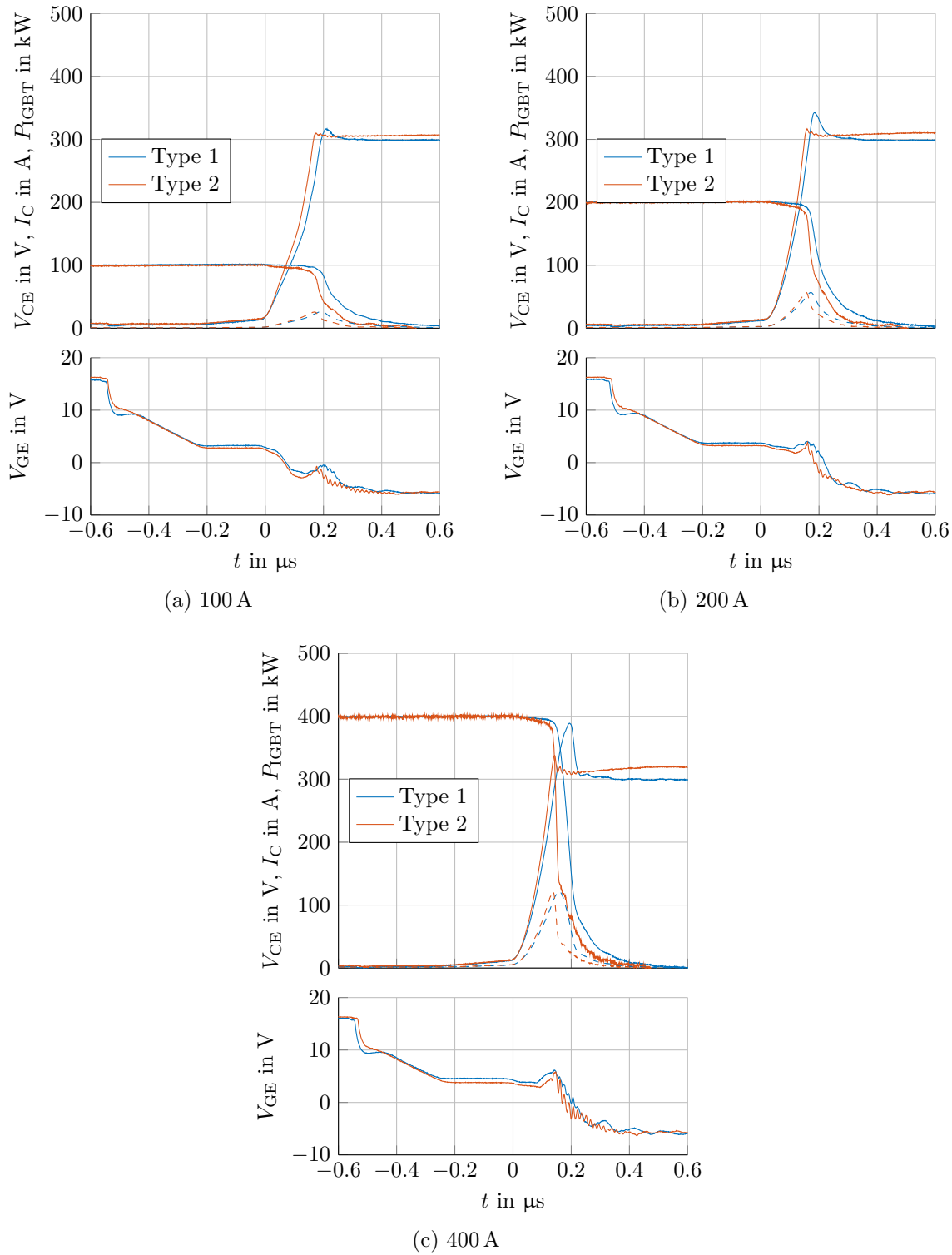


Figure 4.30: Comparison of the turn-off at 300 V and 25 °C

4.4.2.2 Turn-on

The hard turn-on process of the IGBT is characterized by the fact that the device current rises before the collector-emitter voltage starts to fall. The reason for this behavior is the respective free-wheeling diode (FWD) that conducts the full load current before the IGBT is turned on. The FWD cannot block a voltage before its pn-junction is free from charge carriers. This state appears between zero-crossing of the diode current and the reverse-recovery peak.

In Fig.4.31 the turn-on characteristic of the Type 1 module is shown with focus on the current dependency. Initially, the current rises with a certain steepness which is independent of the switched current. The reverse-recovery effect of the FWD causes a current overshoot. This effect appears because the diode stores charge carriers in the space-charge region. These charge carriers are removed by recombination when the diodes current decreases. However, there are still charge carriers left when the diode current reaches zero. Thus, a current flow in reverse direction is enabled for a short time which appears as an overcurrent in the IGBT.

The collector-emitter voltage reduction by

$$\Delta V_{CE} = L_{\sigma} \cdot \frac{dI_C}{dt} \quad (4.11)$$

appears during the current rise period due to the dc-link inductance L_{σ} .

The temperature dependency of the turn-on process is depicted in Fig. 4.32. The reverse recovery effect is strongly temperature dependent leading to increased switching losses at high temperatures. In contrast, the voltage characteristic is almost independent of temperature.

The low dc-link inductance of the Type 2 module causes a faster current rise and less reduction of the collector-emitter voltage (Eq. 4.11). The reverse recovery peak has a more sharp shape compared to Type 1 (Fig. 4.33).

The temperature dependency of the turn-on process is also characterized by a stronger reverse recovery effect at high temperatures and a temperature independent voltage shape (Fig. 4.34).

The direct comparison of both evaluated modules (300 V in Fig. 4.35 and 400 V in Fig. C.5) additionally shows the momentary power loss as product of voltage and current. It can be seen that the Type 2 module has a much faster current rise time. Hence, the maximum of the power losses is reached earlier, the voltage can start to decrease earlier and, finally, the overall duration of the switching process is significantly reduced. However, the Type 2 module has higher peak losses due to a higher reverse-recovery peak and a smaller reduction of the collector-emitter voltage.

A clear and descriptive comparison of the switching behavior is generated by plotting I_C over V_{CE} during switching as done in Fig. 4.36 for an exemplary operating point.

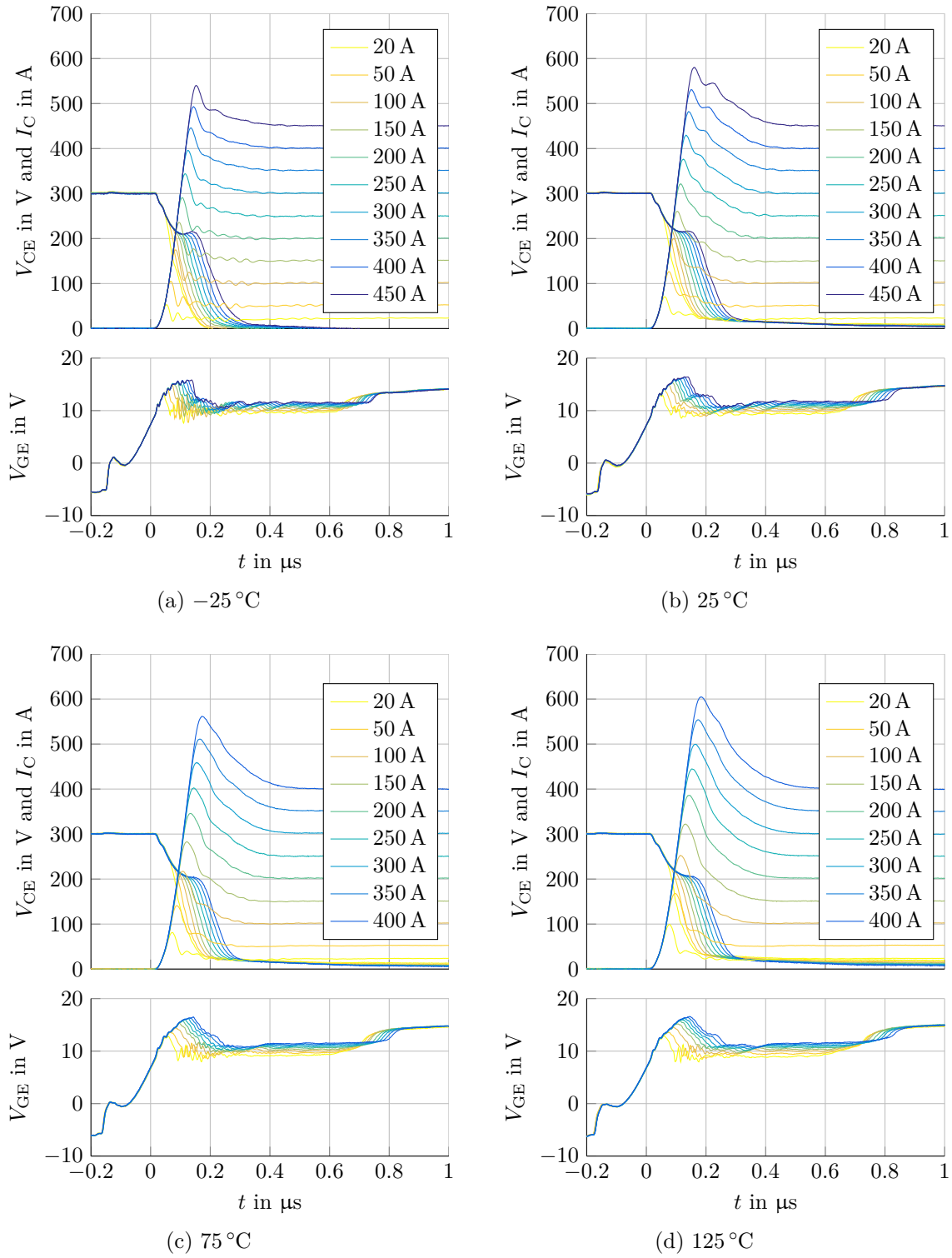


Figure 4.31: Turn-on Type 1 at 300 V

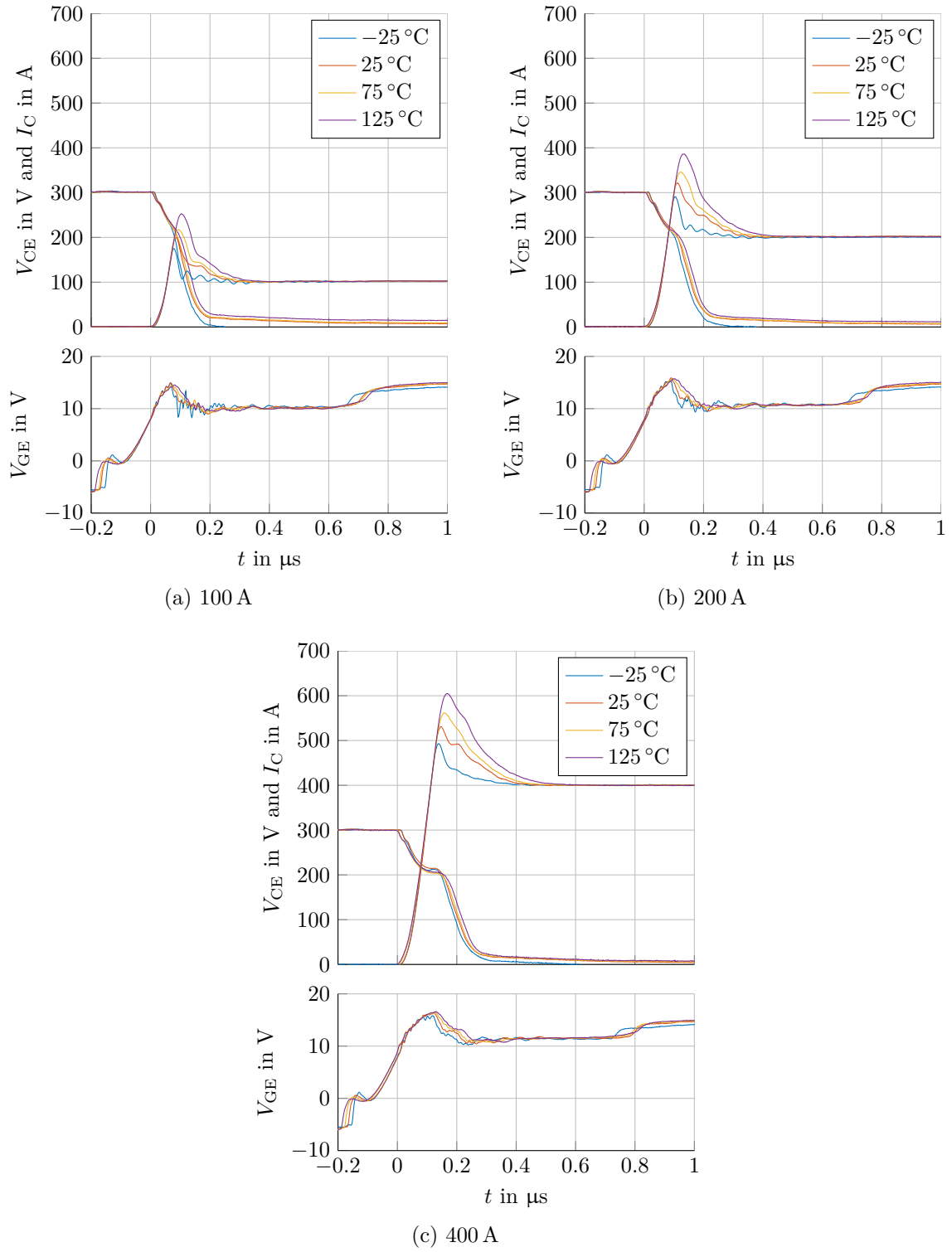


Figure 4.32: Turn-on Type 1 at 300 V

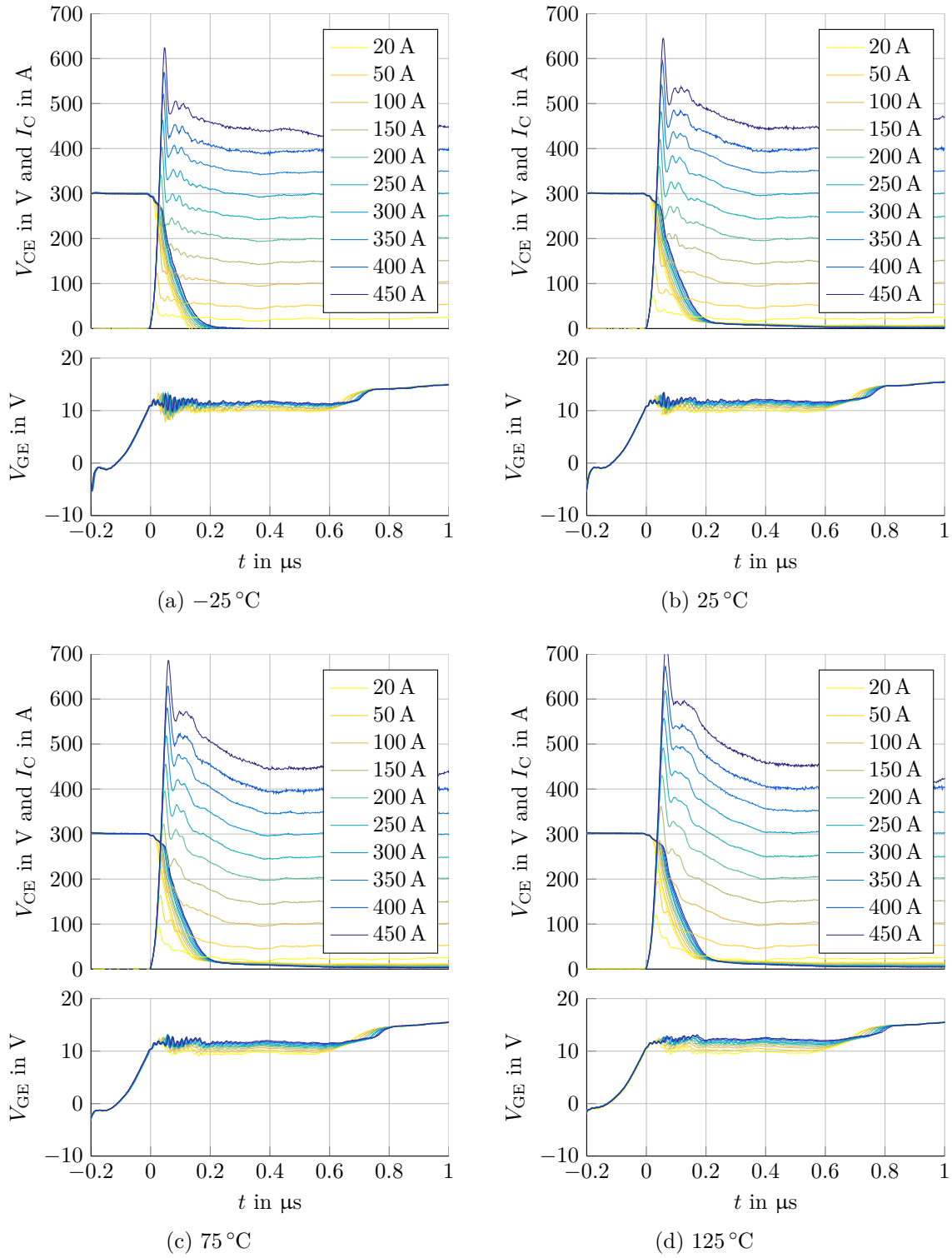


Figure 4.33: Turn-on Type 2 at 300 V

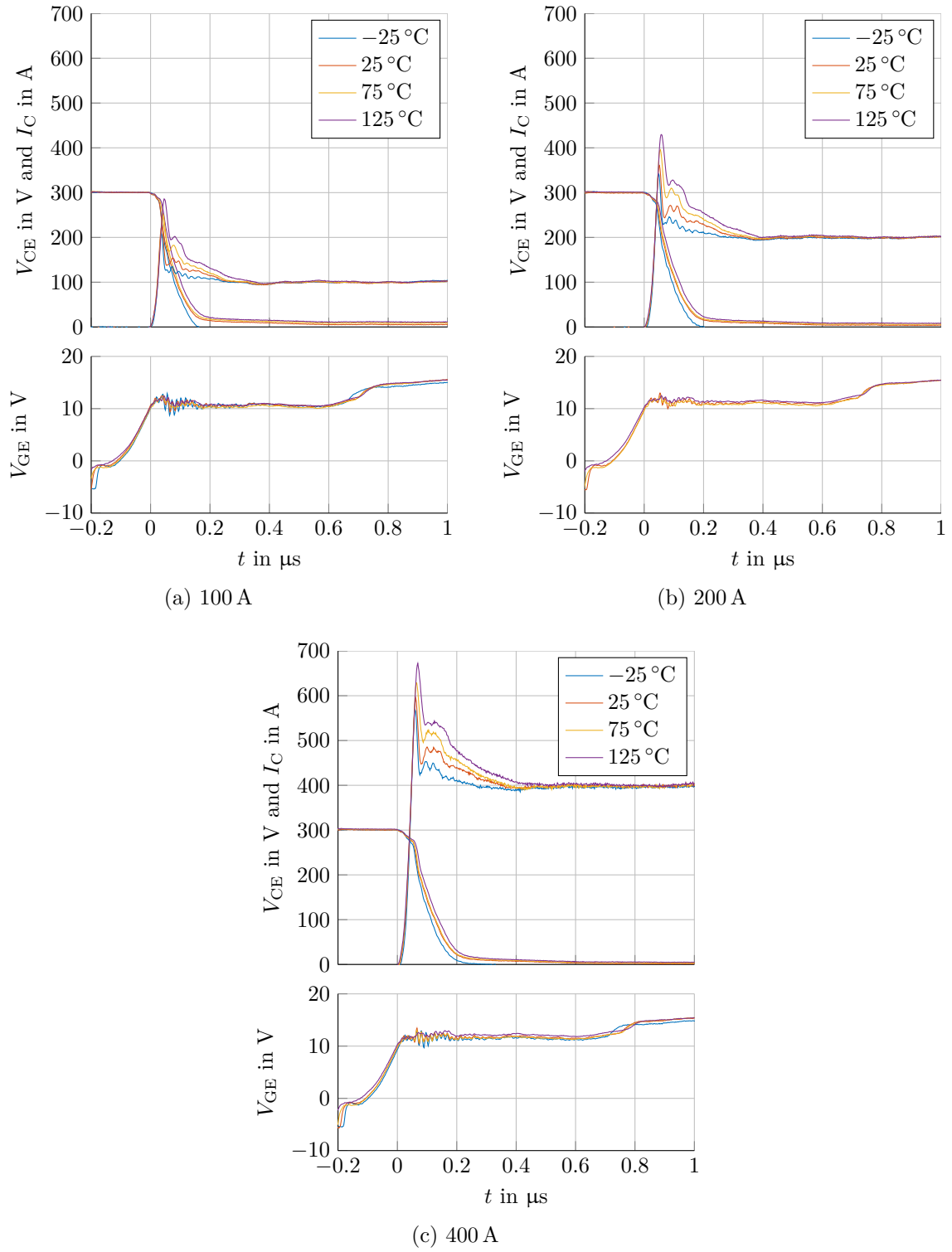


Figure 4.34: Turn-on Type 2 at 300 V

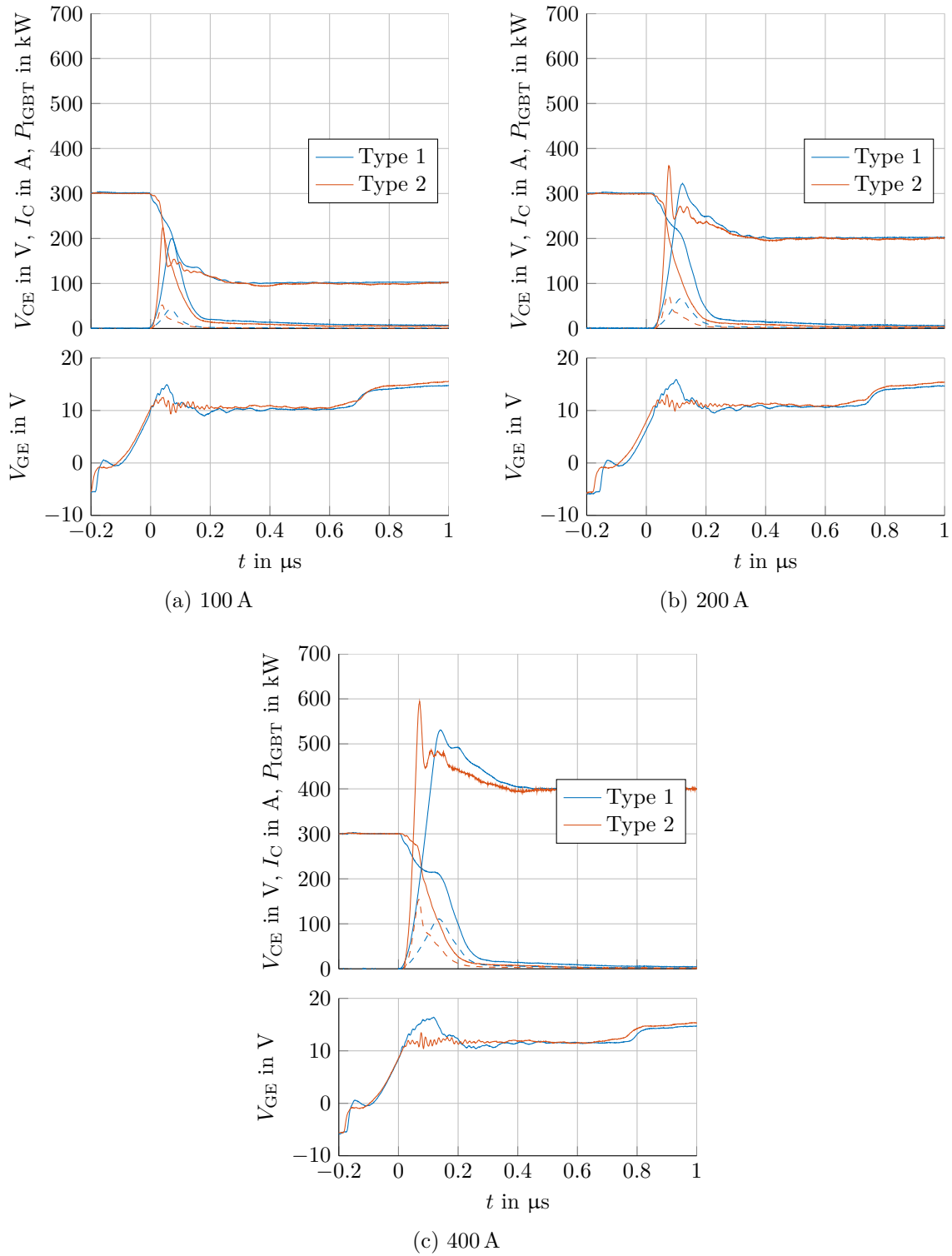


Figure 4.35: Comparison of the turn-on characteristic at 300 V and 25 °C

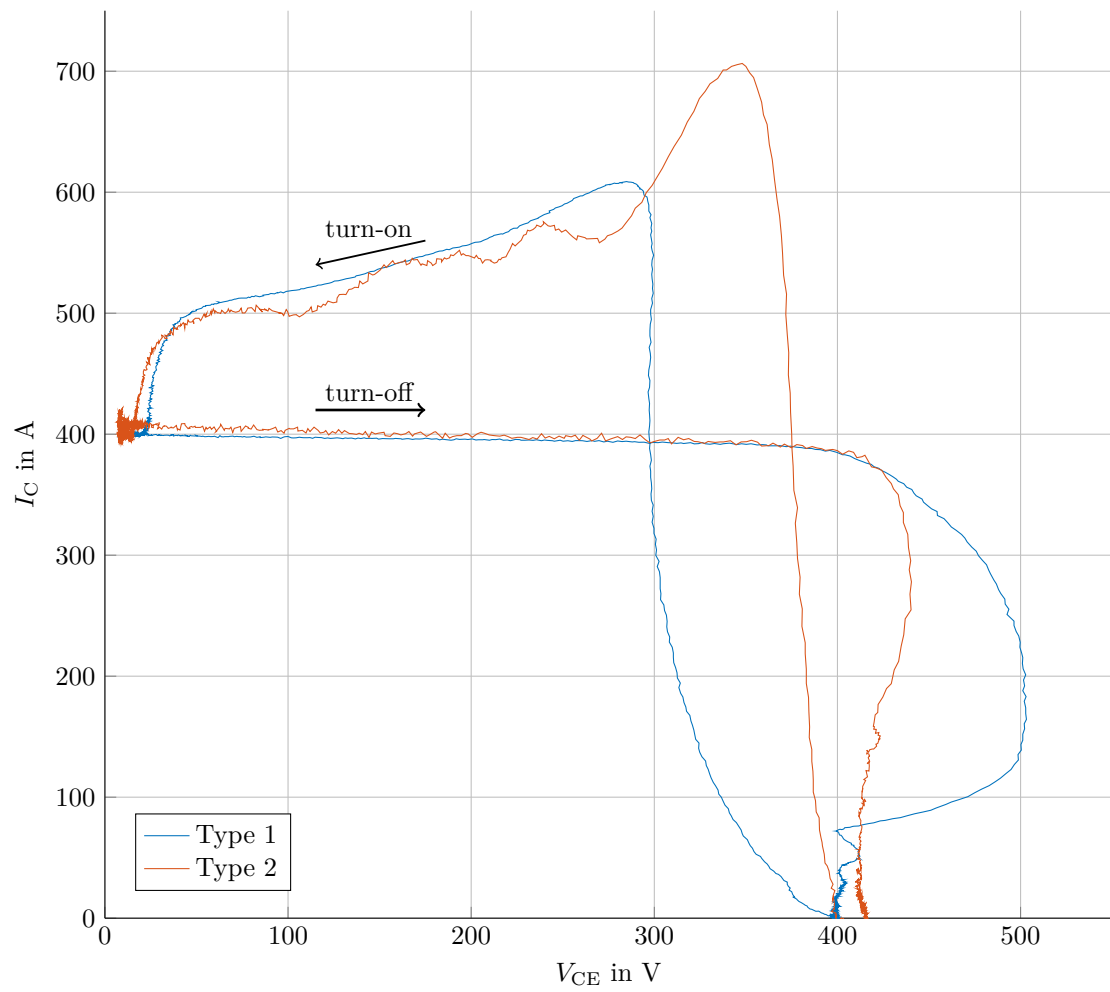


Figure 4.36: IGBT switching trajectory

4.4.2.3 Switching losses

Switching losses are given by loss energy per switching event. For the evaluated modules they are in the range of some mJ. Their calculation is done by integration of the power losses. The integration limits are set at 10 % of the rising and falling value, respectively. For example, the power loss integration of the turn-on process starts when the current reaches 10 % of its final value. It is terminated when the voltage undergoes 10 % of its starting value.

The switching loss energies of the Type 1 module are shown in Fig. 4.37 (300 V) and Fig. C.1 (400 V). Turn-on and turn-off losses of the IGBT, $E_{\text{on,IGBT}}$ and $E_{\text{off,IGBT}}$, are almost equal and rise linearly with increasing collector current. The diode losses $E_{\text{off,diode}}$, caused by the reverse-recovery effect, are comparatively low and the dependency of the collector current is less strong than for the IGBT losses.

In sections 4.4.2.1 and 4.4.2.2 the temperature dependency of the switching processes is investigated. In Table 4.2 and 4.3 the relative variation of the losses with temperature is given for two exemplary current values. IGBT losses show a stronger dependency at lower currents. Against this, the diode losses which are generally more temperature dependent show a higher dependency at high currents.

Table 4.2: Relative variation of switching losses at 300 V,
relating to 25 °C (Type 1)

	$E_{\text{off,IGBT}}$	$E_{\text{on,IGBT}}$	$E_{\text{off,diode}}$
100 A	0.30 %/K	0.42 %/K	0.43 %/K
400 A	0.17 %/K	0.25 %/K	0.89 %/K

Table 4.3: Relative variation of switching losses at 400 V,
relating to 25 °C (Type 1)

	$E_{\text{off,IGBT}}$	$E_{\text{on,IGBT}}$	$E_{\text{off,diode}}$
100 A	0.30 %/K	0.43 %/K	0.4 %/K
400 A	0.12 %/K	0.20 %/K	0.95 %/K

The switching loss energies of the Type 2 module are given in Fig. 4.38 (300 V) and Fig. C.2 (400 V). Turn-on and turn-off losses of the IGBT are also almost equal here. The dependency of the IGBT and diode losses from the collector current is close to that of Type 1.

The increase of switching losses with temperature is similar to the Type 1 module (Table 4.4 and 4.5). However, a stronger dependency at high current is found here. The direct comparison of both modules (Fig. 4.39 and C.3) shows that the novel packaging technology of the Type 2 module with extensively reduced dc-link inductance leads to a reduction of both turn-on and turn-off losses by up to 40 %, whereby, the reduction of turn-off losses is more significant. Against this, the diode losses of the Type 2 module are slightly higher compared to Type 1. The advantage

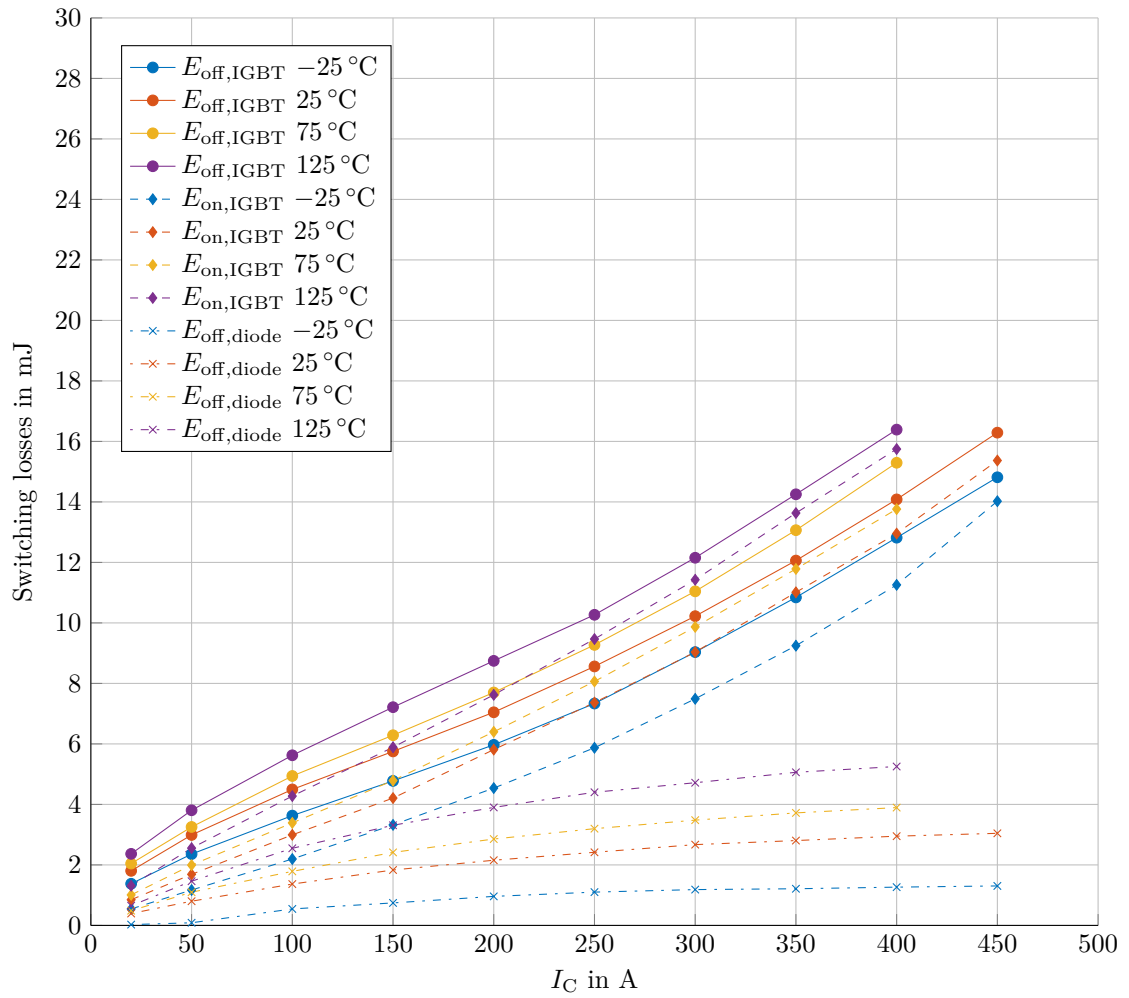


Figure 4.37: Switching losses Type 1 at 300 V

of Type 2 regarding switching losses is stronger the lower the temperature and the higher the dc-link voltage.

Table 4.4: Relative variation of switching losses at 300 V,
relating to 25 °C (Type 2)

	$E_{\text{off,IGBT}}$	$E_{\text{on,IGBT}}$	$E_{\text{off,diode}}$
100 A	0.44 %/K	0.49 %/K	0.43 %/K
400 A	0.32 %/K	0.33 %/K	not measured

Table 4.5: Relative variation of switching losses at 400 V,
relating to 25 °C (Type 2)

	$E_{\text{off,IGBT}}$	$E_{\text{on,IGBT}}$	$E_{\text{off,diode}}$
100 A	0.39 %/K	0.37 %/K	0.40 %/K
400 A	0.28 %/K	0.34 %/K	not measured

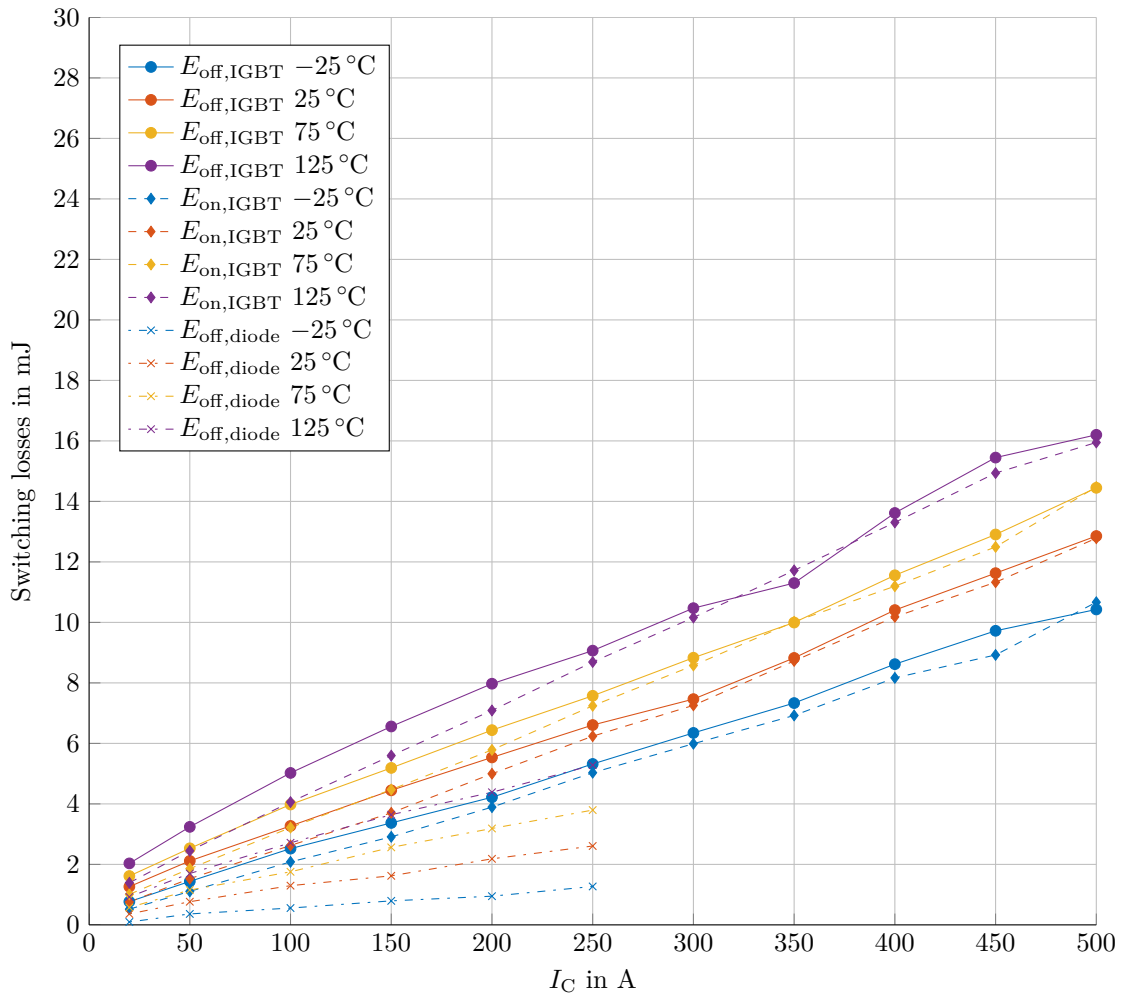


Figure 4.38: Switching losses Type 2 at 300 V

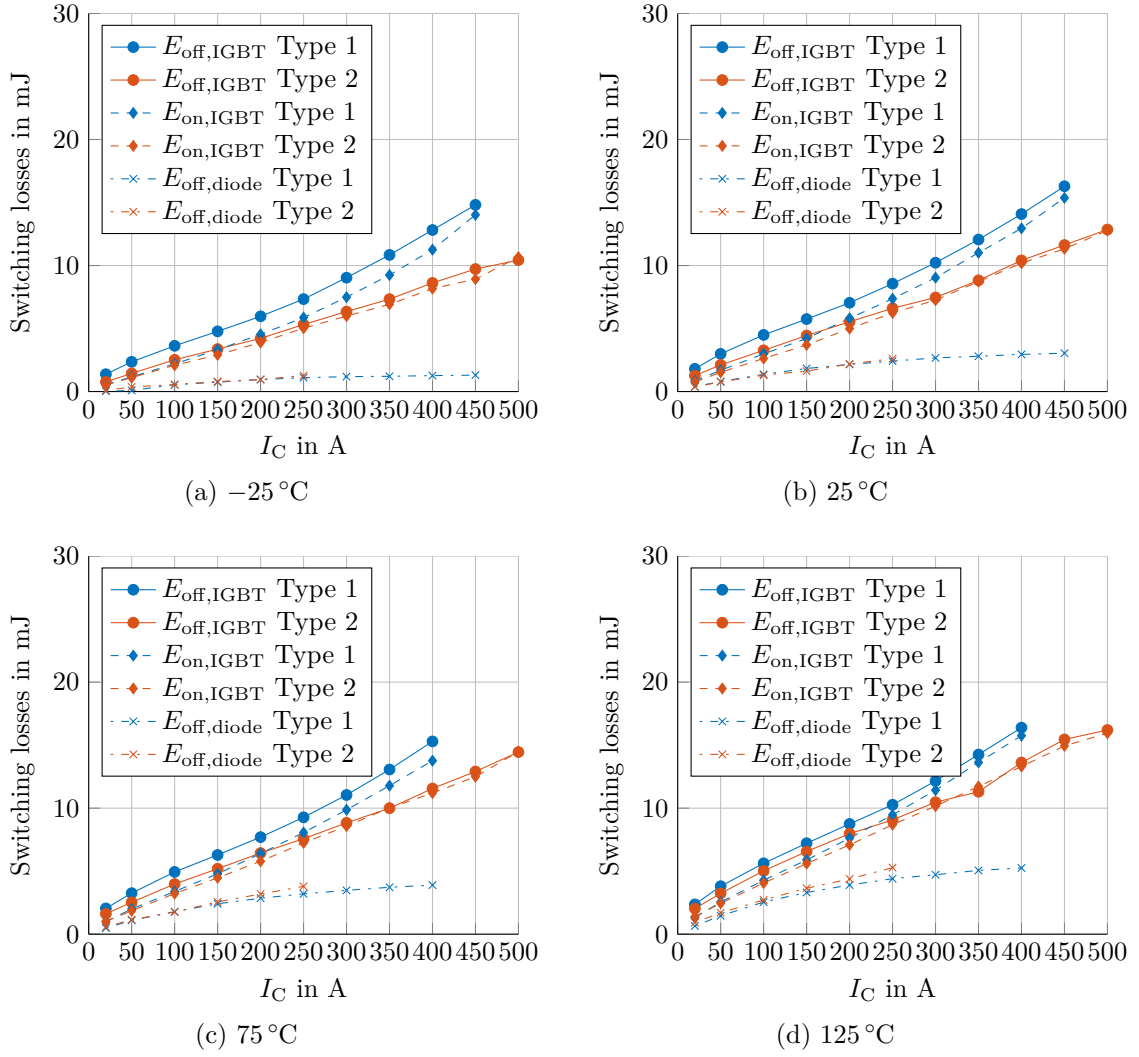


Figure 4.39: Comparison of the switching losses at 300 V

4.4.3 Dc-link inductance

The dc-link inductance L_σ can be determined by measuring the switching characteristic of the IGBT which was done in double pulse tests in Section 4.4.2.3. Since the turn-off overvoltage of the IGBT is a well known phenomenon caused by the dc-link inductance, it is often used to measure the dc-link inductance. However, the turn-off overvoltage is not only caused by the dc-link inductance but also by the forward-recovery effect of the free-wheeling diode. Hence, the diode voltage has also to be measured and subtracted from the IGBTs overvoltage. A more exact measurement is possible during the IGBT turn-on process. Here, the rising IGBT collector current leads to a decrease of the collector-emitter voltage due to the voltage drop across the dc-link inductance. During the rise time of the current, the free-wheeling diode is still conducting a current and, thereby, its forward voltage is usually neglectable compared to the inductive voltage drop. With the basic device equation of an inductance, L_σ can be calculated during the turn-on process as follows:

$$L_\sigma = \frac{V_{DC} - V_{CE}}{\frac{dI_C}{dt}} \quad (4.12)$$

This measurement is done for both modules in a double pulse test at 400 V, 400 A and 25 °C. The respective waveforms can be found in Fig. 4.40. It comes out that the dc-link inductance of the Type 1 module is approx. 15 nH whereas the Type 2 module only has 1.5 nH. The latter value is in good accordance to the simulation results of chapter 4.3 (1 – 1.5 nH).

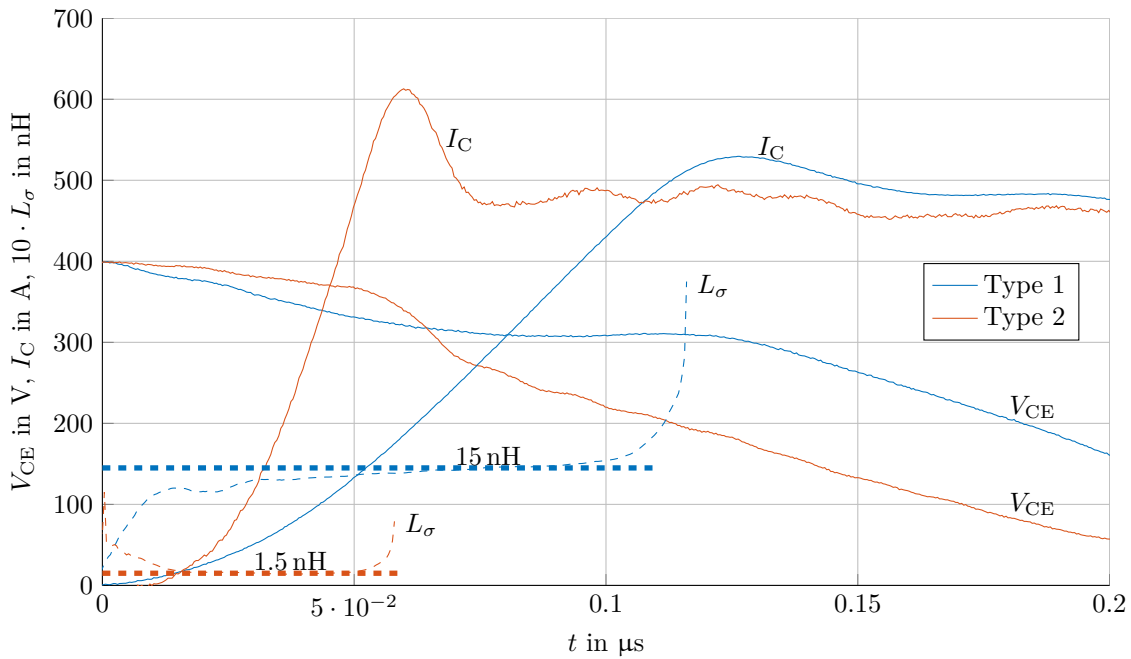


Figure 4.40: Extraction of stray inductance during IGBT turn-on

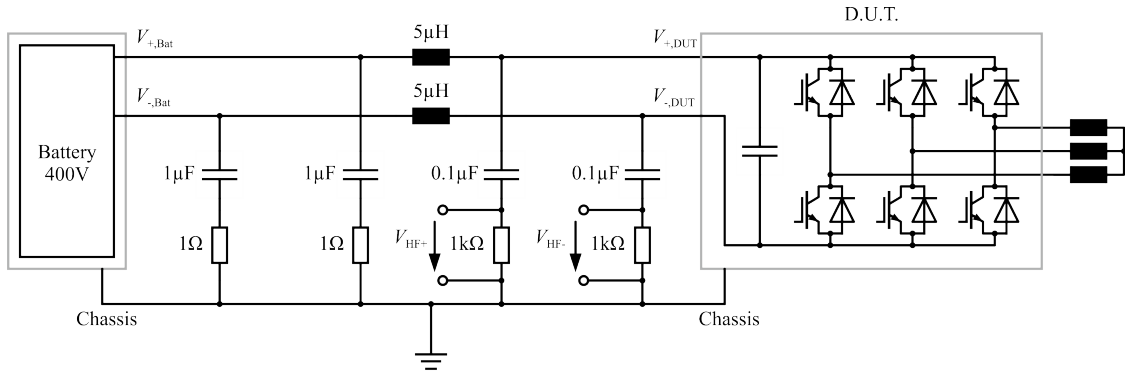


Figure 4.41: EMC measurement with LISN according to CISPR 25 [92]

4.4.4 EMC behavior

The measurement of the EMC behavior is done with a high-voltage line impedance stabilization network (LISN) (Fig. 4.41). The disturbances V_{HF+} and V_{HF-} are measured across the 1-k Ω -resistors. The common mode and differential mode disturbances V_{cm} and V_{dm} are calculated using Eq. 4.13 and 4.14 [91].

$$V_{dm} = V_{HF+} + V_{HF-} \quad (4.13)$$

$$V_{cm} = \frac{V_{HF+} - V_{HF-}}{2} \quad (4.14)$$

Initially, the basic disturbance level of the assembly is measured with running auxiliary units (high voltage power supply, power supply drivers). The measurements are done with driving an apparent power of 60 kVA to the (mainly) inductive load. Fig. 4.42 and 4.43 show the measured disturbance level from 9 kHz – 30 MHz. At low frequencies (< 150 kHz) peak levels at multiples of the switching frequency (10 kHz) are visible. Above 150 kHz the measurement uses a larger bandwidth. Consequently, no discrete peaks are visible in this frequency range.

Common mode disturbances of the modules do not deviate significantly from each other. At least, in the range of 20 – 30 MHz the level of the Type 2 module is a bit lower. The main difference between both modules can be observed in the differential mode disturbances. Above a narrow bandwidth section with raised spectrum at 300 kHz (+10 dB μ V) the disturbance level of the Type 2 module strongly decreases. In the range from 1 – 10 MHz it is more than 20 dB μ V below the spectrum of Type 1. This reduction is caused by the different packaging technologies. The smaller dc-link inductance leads to less voltages across the dc-link inductance during switching events. These voltages are mainly responsible for the differential mode disturbances at high frequencies (above 1 MHz).

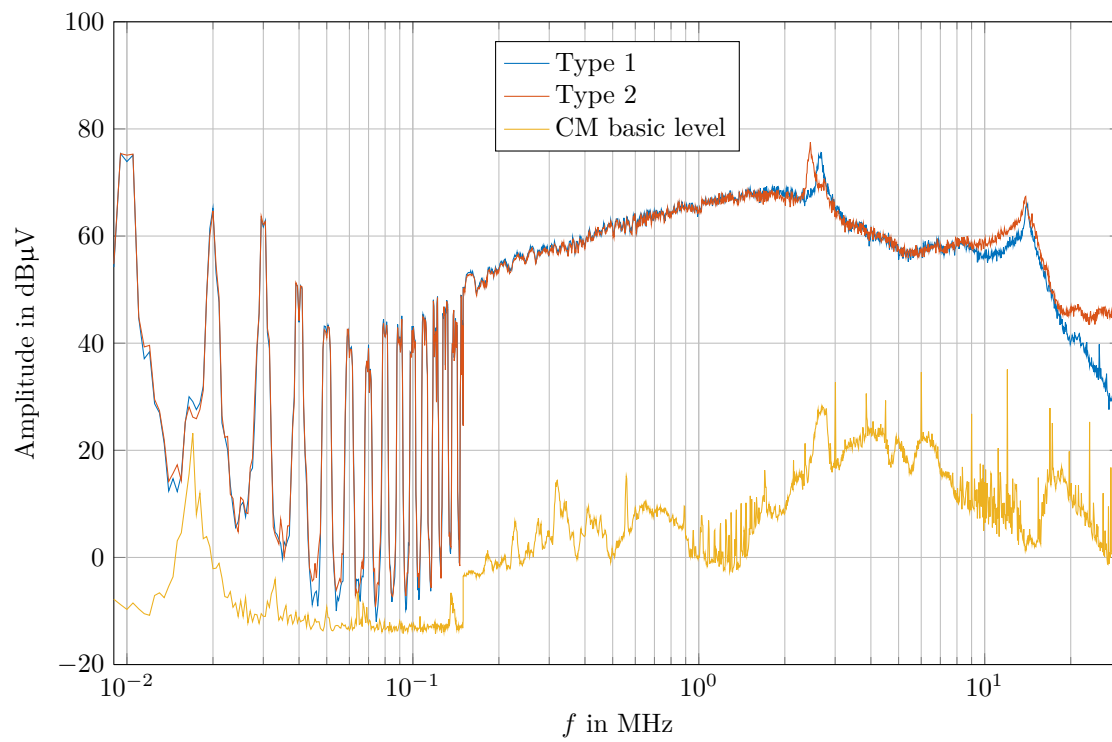


Figure 4.42: Common mode spectrum

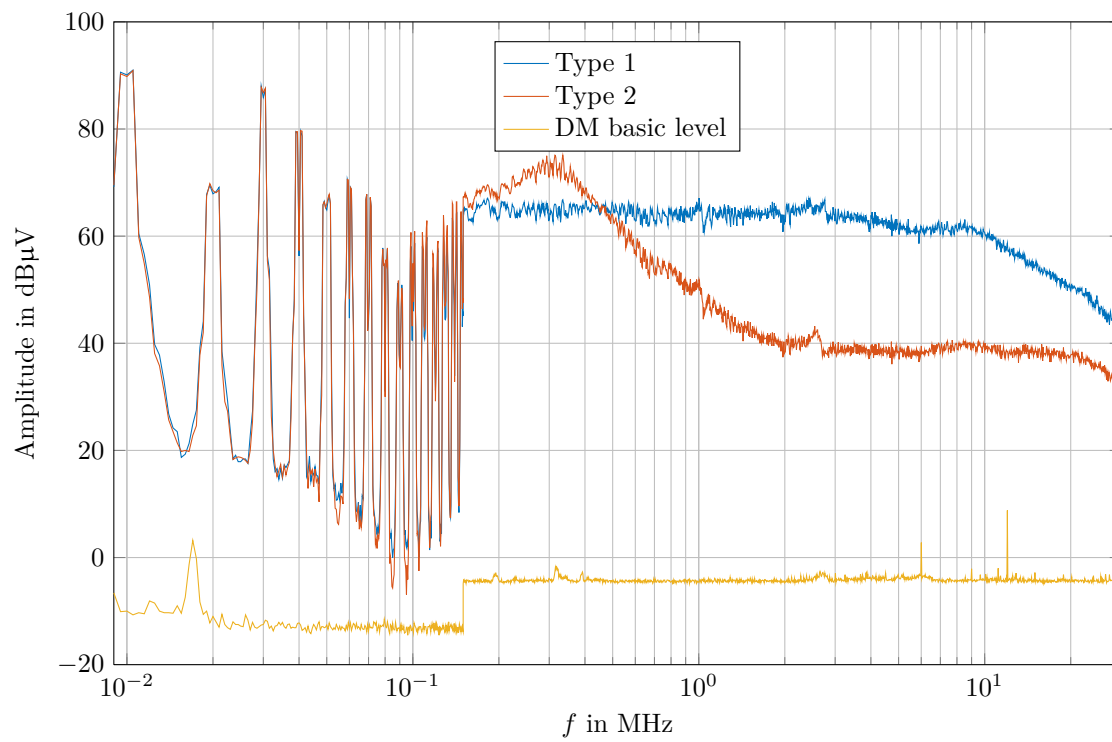


Figure 4.43: Differential mode spectrum

5 System Level Implications

In chapter 4 some advantages of PCB-based power modules on components level are described in detail. Namely, reduction of switching losses, turn-off overvoltages and EMC disturbance level. The impact of these and other advantages on system level are investigated in this chapter. Therefore, the use of different power modules in inverter drives and a dc-dc converter is analyzed by means of circuit simulation. A conventional chip configuration with single chips for IGBT and diode is investigated as well as the reverse conducting IGBT (RC-IGBT) that integrates IGBT and diode on one chip.

5.1 Advantages of PCB based power modules

5.1.1 Integration of driver electronics

In a PCB-based power module the top side interconnection of the power semiconductor is done with micro vias enabling to build thinner modules compared to a bond wire solution. The driver electronics, that are conventionally located on a separate PCB close to the module, can also be integrated to the top side of the PCB based power module. This offers the potential to further increase power density at system level and to put the module in a very narrow installation space. Additionally, a short connection between driver stage and power semiconductor is crucial for clean and high-speed switching, bringing losses down and improving EMI compatibility. Future development could also embed all driver electronics into the PCB to make the power module even thinner. Till now, it appears that the achieved space reduction does not compensate for the higher costs that arise from the additional embedding of a high number of components such as ASICs, small passives, etc.

5.1.2 Integration of current sensors

PCB integration of power electronics comprises the embedding of power semiconductor as well as the integration of power stage and driver electronics into a single PCB. Furthermore, integration of sensor elements becomes feasible. One promising approach is the PCB embedding of a Rogowski coil current sensor. A Rogowski coil works without an iron core. Thereby, only copper windings have to be integrated into the PCB. The development, assembly and testing of such current sensor is done in [93].

The measurement principle of the Rogowski coil is based on an idea from A. P. Chattock in 1887 [94]. Since the publication of W. Rogowski and W. Steinhaus in 1912

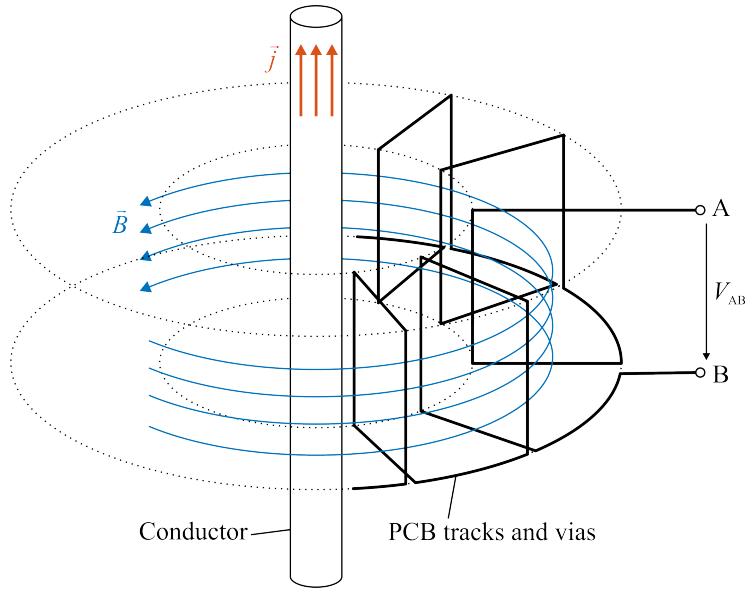


Figure 5.1: Sketch of PCB embedded Rogowski coil, according to [93]

[95] it is called Rogowski coil or Rogowski current transducer. Measuring the magnetic field strength along a closed contour provides the enclosed current according to Maxwell-Ampere equation [96].

$$\oint_C \vec{H} \cdot d\vec{s} = I_{\text{enclosed}} \quad (5.1)$$

Building a coil around a conductor with the current density j , as outlined in Fig. 5.1, the surrounding magnetic field can be measured using the Maxwell-Faraday equation [96].

$$\oint_C \vec{E} \cdot d\vec{s} = -\frac{d}{dt} \iint_A \vec{B} \cdot d\vec{A} = -\frac{d\phi}{dt} \quad (5.2)$$

The measured voltage V_{AB} at the coil terminals A and B is integrated to obtain a signal that is proportional to the current in the enclosed conductor. Due to this relation between current and measurement signal the Rogowski coil can only be used to detect AC signals. At first glance, this is a criterion for exclusion from using it for closed-loop current control for example in a dc-dc converter, because the Rogowski coil would only measure the AC part (Fig. 5.2b) of the output current (Fig. 5.2a). However, a PCB embedded Rogowski coil can be built such that only the current of the high- or low-side semiconductors (Fig. 5.2c) are detected. Still, the output signal from the Rogowski coil has no dc-component (Fig. 5.2d) but due to the fact that the amplitude of the current is always zero during the turn-off interval, the electronics resets the measurement signal while the current is known to be zero. Thereby, the actual current waveforms can be reconstructed (Fig. 5.2e).

A prototype of a PCB embedded Rogowski coil built within the scope of the HI-

LEVEL project [83]. It comprises a MOSFET half-bridge built on a 4-layer PCB. The coil is wound on the inner layers using buried vias. After some iteration steps regarding the integrator electronics, measurements of little noise, good dynamic quality and high immunity to voltage gradients were realized [93].

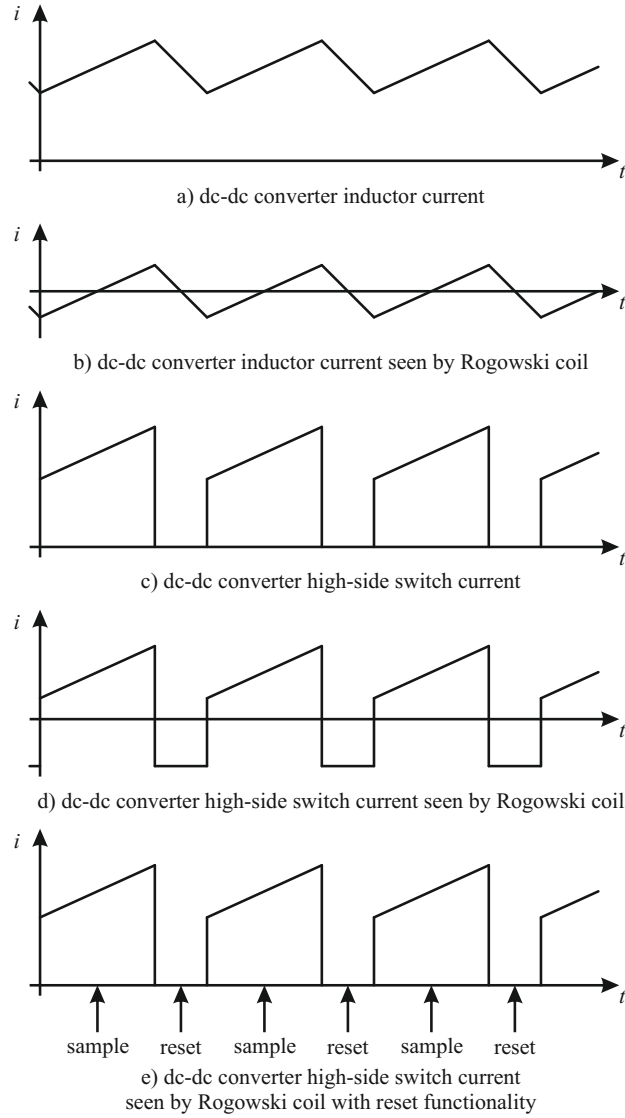


Figure 5.2: PCB embedded Rogowski coil feasible for dc-dc converter current control

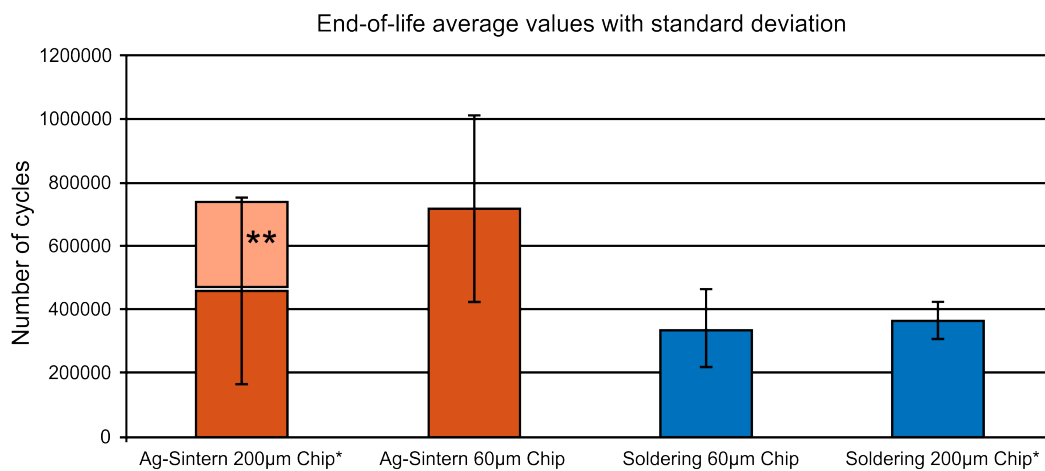
5.1.3 Thermal resistance

The thermal resistance of today's PCB-based power module prototypes is already on the same level as comparable DCB-based modules. Future research on thermally high conductive prepreg materials will bring a clear reduction of thermal resistance, e.g., Panasonic CV2079D with 5 W/mK. Together with large thermal capacities close to the power semiconductors by using thick leadframes materials, modules with superior thermal impedance can be generated. Moreover, double sided cooling further enhances the thermal performance leading to an increased power density.

5.1.4 Thermo-mechanical stress

The advantageous thermal impedance not only leads to lower absolute chip temperatures (if output power is kept constant) but also decreases the amplitude of chip temperature swings caused by the sinusoidal shape of the output current and by changing load conditions. The better CTE match of materials in a PCB based power module causes less critical material joints except for the die attach which is stressed more because the high CTE of the thick copper leadframe is not attenuated as it is the case on a DCB. However, this issue can be overcome by using smaller chips sizes. All this leads to a higher reliability of the PCB based power module.

Power cycling tests of PCB based power modules (p² Pack) show that $5 \cdot 10^5 \dots 1 \cdot 10^6$ cycle with temperature swings of 120 K are possible if an Ag-sintering process is used for the die attach (Fig. 5.3).



* Cycling started with amplitude 80K, later increased to 120K. Adaption from 80K to 120K with Coffin-Manson coefficient = 3

** 4/5 of sintered 200µm chip samples did not reach EOL before test was terminated. Shaded area symbolizes higher lifetime potential.

Chip: MOSFET, 60V

Pcb-material: Panasonic R14-T

Test condition: 120K temperature amplitude, 2s/2s pulse length

EOL criteria: electrical fail, increase in temperature > 30K, $R_{\theta ja}$ +20%

Figure 5.3: Power cycling capability of embedded power semiconductors, according to [97]

5.1.5 Cost

PCB based power modules promise numerous cost advantages:

- Isolations layer: Prepreg instead of ceramics → Save material costs
- Integration of logic and power board → Save connectors
- Enhanced thermal performance → Save cooling
- Higher switching frequencies → Save passives
- EMC measures inside pcb → Save filter components
- Space reduction → Crucial in hybrid cars

Comprehensive studies that consider all manufacturing and overall system costs have not been conducted so far.

5.1.6 Electric performance

In addition to the efficiency gain by reduced conduction and switching losses, there are several advantages that arise from the smaller dc-link inductance.

- The power semiconductors are less stressed by overvoltage peaks.
- The driver circuit of power semiconductors often contains some circuitry (e.g., active clamping) that suppresses high overvoltages that could destroy the power semiconductor. This is especially necessary to safely turn off the device under short-circuit condition. A very small dc-link inductance might allow to omit the additional circuitry.
- If the reduction of the turn-off overvoltage is not the primary goal, the power semiconductors can be switched faster (i. e., higher $\frac{dv}{dt}$ and $\frac{di}{dt}$) to further reduce the switching losses.
- A lower dc-link inductance reduces the characteristic impedance $Z_0 = \sqrt{\frac{L}{C}}$ of the system which leads to a lower tendency of oscillations between dc-link inductance and capacities of chips, busbars and capacitors.
- A higher dc-link voltage is possible due to reduced overvoltages. For some converter types this can be used to increase the output power.
- The enhanced EMC performance makes it possible to use less filter components.

5.2 System simulation

After describing different power modules thermally and electrically in chapter 4 and outlining the general benefits of PCB based power modules, a case study is done to assess quantitatively the advantages by means of exemplary applications. The work flow of the case study is outlined in Fig. 5.7. The semiconductor models for the PLECS converter model are fed by the beforehand acquired data, i.e. thermal equivalent circuit and temperature dependent conduction and switching losses. As the thermal equivalent circuit is obtained by simulation of only one IGBT and diode chip, it is scaled with a factor of three to accord with the real modules, where three chips in parallel are used. Each topology is simulated with Type 1, Type 2 and Type 5 module. Due to the fact, that Type 5 module is not measured electrically, the loss model of Type 1 is implemented. Each module is simulated with two chip variants: Firstly, the conventional chip configuration with single chips for IGBT and diode. Secondly, RC-IGBTs are used. The simulation outputs the characteristic of the junction temperature and the maximum output power for a limited junction temperature depending on the packaging and the chip technology.

5.2.1 Topologies

The two evaluated converter topologies are

1. a B6 drives inverter
2. a three-phase dc-dc converter

Both converters are built with B6 power modules. The respective equivalent circuits are shown in Fig. 5.4 and 5.6.

5.2.2 Operating points

Typical operating points are chosen to simulate the performance of the different module technologies in the specific application.

5.2.2.1 Drives inverter

The drives inverter shall be rated to control a permanent magnet synchronous machine (PMSM) with

- maximum output power $P_{\max} = 50 \text{ kW}$
- rated speed $n_{\text{nom}} = 6,000 \text{ rpm}$
- maximum speed $n_{\max} = 10,000 \text{ rpm}$
- number of pole pairs $N_{\text{pole}} = 5$

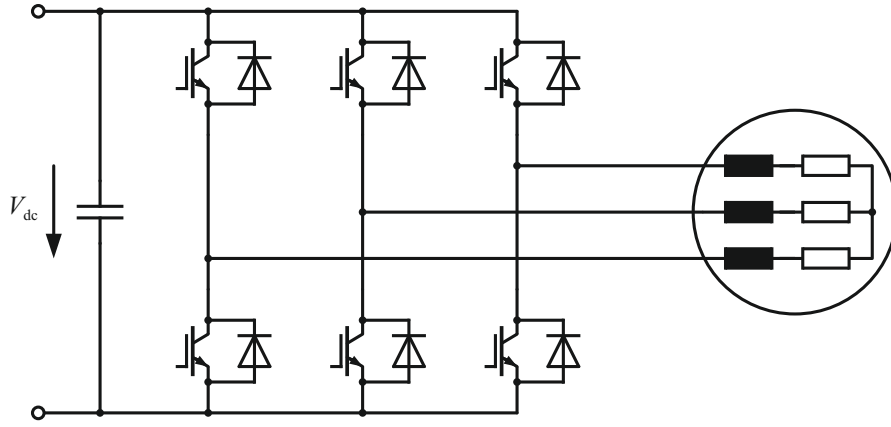


Figure 5.4: Simulated topology: B6 drives inverter

The drives inverter is rated to provide full power $P_{\max}$ to the machine within the dc-link voltage range from 250 to 450 V. The phase voltage is directly proportional to the machine speed n up to nominal speed n_{nom} where the field weakening area is entered. In this area ($n \geq n_{\text{nom}}$) the maximum phase voltage $V_{\text{ph,max}}$ is supplied by the inverter. Depending on the modulation strategy (space vector modulation (SVM) or sine-triangle pulse width modulation (PWM)), the inverter is able to generate $V_{\text{ph,max}}$ according to:

$$V_{\text{ph,max}} = \begin{cases} \frac{d_{\max} \cdot V_{\text{dc,min}}}{\sqrt{6}} = \frac{0.95 \cdot 250 \text{ V}}{\sqrt{6}} = 97.0 \text{ V} & \text{valid for SVM} \\ \frac{d_{\max} \cdot V_{\text{dc,min}}}{2 \cdot \sqrt{2}} = \frac{0.95 \cdot 250 \text{ V}}{2 \cdot \sqrt{2}} = 84.0 \text{ V} & \text{valid for PWM} \end{cases} \quad (5.3)$$

$$\text{with } d_{\max} = \text{maximum duty cycle} \quad (5.4)$$

In the following, it is assumed that the inverter is controlled with space vector modulation (SVM), because a higher utilization of the dc-link voltage can be realized.

The maximum phase current at $P_{\max}$ is

$$V_{\text{ph,max}} = \frac{1}{3} \cdot \frac{1}{\cos \varphi} \cdot \frac{P_{\text{out}}}{V_{\text{ph,max}}} = \frac{1}{3} \cdot \frac{1}{0.85} \cdot \frac{50 \text{ kW}}{97 \text{ V}} = 202.2 \text{ A} \quad (5.5)$$

The thermo-electrical simulation of the drives inverter is done at three different speeds, exemplary. At low speed (1,000 rpm) the diodes carry more current compared to high speed operation. Also, large temperature swings are expected at low speed operation. Contrary to this at rated speed (6,000 rpm) and at high speed (10,000 rpm), when the machine is operated in the field weakening area, the transistors carry more current, but temperature swings tend to be less.

Table 5.1: Simulated operating points of drives inverter

Operation point	Phase current in A	Phase voltage in V	Speed in rpm	Inverter output power in kW	$\cos \varphi$
1	202	16.2	1,000	8.3	0.85
2	202	97.0	6,000	50	0.85
3	202	97.0	10,000	50	0.85

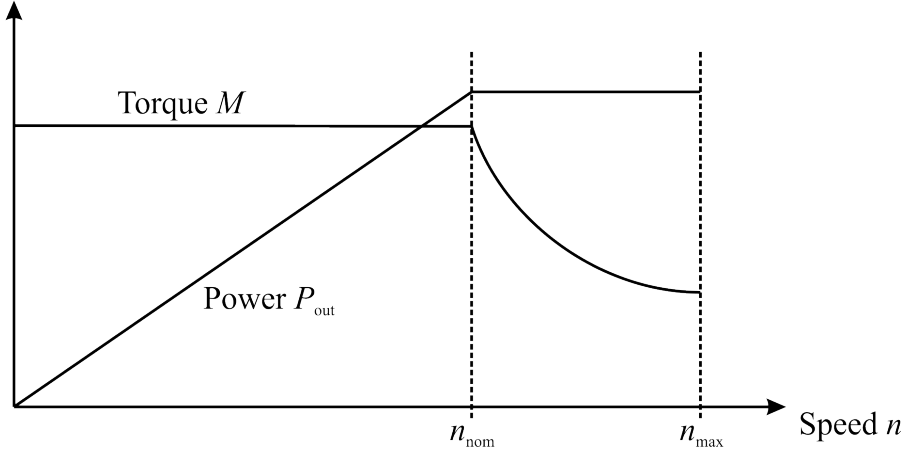


Figure 5.5: Power and torque over speed for PMSM

5.2.2.2 Dc-dc converter

A dc-dc converter (illustrated in Fig. 5.6) for an automotive traction drive is used to link the high-voltage battery and the drives inverter. It adjusts the dc-link voltage to the most advantageous value to make the traction most efficient. To realize recuperation from the electrical machine to the battery, the dc-dc converter has to be able to operate bi-directionally. Usually, the battery voltage is lower than the desired dc-link voltage. Hence, the dc-dc converter operates in boost mode for normal drives operation and as a buck converter during recuperation.

In a propulsion drive inverter all semiconductor chips of a B6-bridge are used due to the sinusoidal output current characteristic. This is not the case for a dc-dc converter. In buck mode, i.e. when the load current I_{load} is positive, only the high-side IGBTs and low-side diodes are conducting and switching current. Vice versa, the low-side IGBTs and high-side diodes are conducting when the dc-dc converter is in recuperating energy, i.e. boost mode (negative load current according to Fig. 5.6). Therefore, using the same power module for a drive inverter and a dc-dc converter leads to diverging output power capabilities.

The performance of different module technologies in a dc-dc converter was compared in a simulation with the following boundary conditions:

- Battery voltage $V_{in} = 225 \text{ V}$
- Inverter dc-link voltage $V_{out} = 450 \text{ V}$

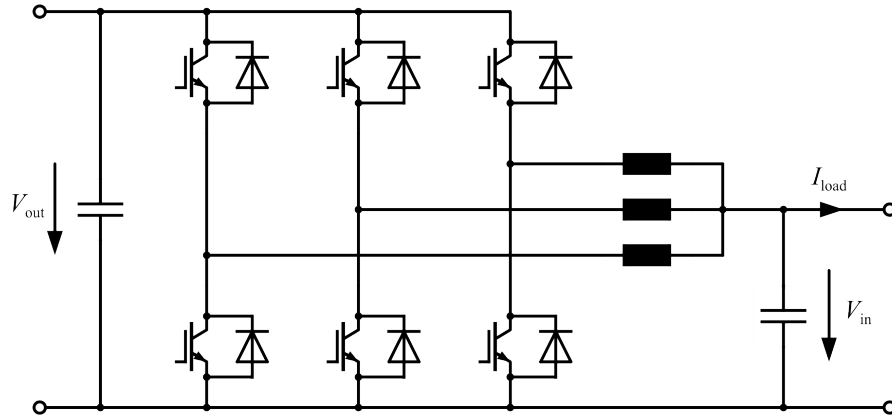


Figure 5.6: Simulated topology: Dc-dc converter

- Switching frequency $f_{\text{sw}} = 10 \text{ kHz}$
- Coolant temperature $T_a = 85^\circ\text{C}$
- Maximum junction temperature $T_j = 125^\circ\text{C}$
- Operation in continuous conduction mode (CCM)

Only boost mode of the dc-dc converter is considered in the following, because of its symmetry compared to the buck mode. Regarding thermal evaluations, the only difference is that losses are shifted from high- to low-side and vice versa. The transferred power is chosen such that the maximum junction temperature is reached ($\pm 0.5 \text{ K}$).

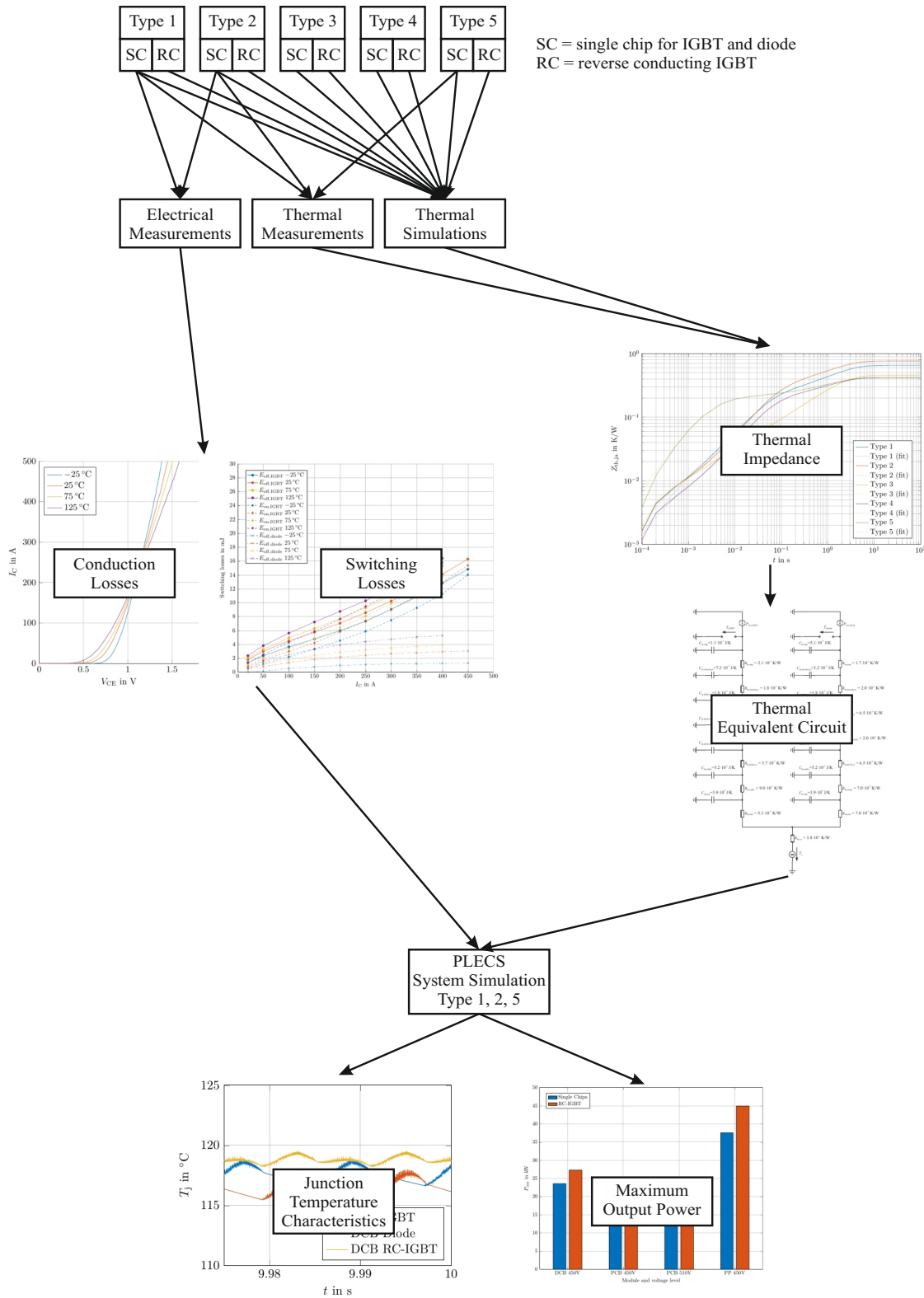


Figure 5.7: Tool chain: From module design to system performance

5.3 Results

5.3.1 Losses

As shown in section 4.4, the semiconductor losses of a Type 2 module are lower compared to a conventional Type 1 module. The resulting losses in an application are analyzed on the basis of a three-phase propulsion drive inverter. The simulated operating points are outlined in Section 5.2.2.1. At the lowest level of the dc-link voltage range (Fig. 5.8(a)) roughly 60 W per chip pair (IGBT with FWD) are dissipated. The losses of the Type 2 module are about 5 % lower compared to the Type 1 module. At rated speed the portion of diode conduction losses is much lower compared to low speed condition. This is due to the higher modulation index used at rated speed. At the upper end of the dc-link voltage range (Fig. 5.8(b)) the same effects can be observed as at 250 V. Torque, and hence also current, remain the same. Therefore, the conduction losses are almost equal for 250 and 450 V. However, the larger dc-link voltage leads to analogously increased switching losses. This is why the overall losses per chip pair are approximately 85 W.

Finally, the advantage of the PCB based power module regarding turn-off overvoltage is incorporated to the loss comparison. The reduction of overvoltage by 60 V (see 4.4.3) is included in the simulation by shifting the dc-link voltage range of the Type 2 module by the same amount of voltage. Consequently, higher phase voltage can be applied to the machine. Keeping the output power constant, lower motor currents are necessary, leading to lower (semiconductor) conduction losses. Simulation shows, that all loss components are decreased at higher dc-link voltage. In this configuration, the advantage of the Type 2 module regarding losses is 14 %.

5.3.2 Characteristic of the junction temperature

The loss simulation applies the thermal equivalent circuits from Section 4.1.3.1 to determine the junction temperatures as well as the temperature of the different packaging layers. Three chips in parallel are used for both topologies. As the dc-dc converter is operated with a stable duty cycle, the junction temperature does not fluctuate significantly. Against this, in a drives inverter the semiconductor chips are conducting depending on the orientation of current flow in the respective motor phase. Consequently, the load on a certain semiconductor is pulsating not only with switching frequency but also with the fundamental electric frequency of the motor. The temperature swings caused by the switching frequency are very small as described above for the dc-dc converter. Against this, at low fundamental frequencies large temperature swings might be induced by the fluctuating current load.

The temperature swings at 1,000 rpm are shown in Fig. 5.9 at 250 and 450 V, respectively, for Type 1 (a)-(b), Type 2 (c)-(d) and Type 5 (e)-(f). Type 1 and 2 reveal very similar swinging characteristics due to their similar thermal impedance curves in the range up to 0.1 s. The swinging amplitude is about 3 K (peak-to-

peak) for the IGBTs as well as for the diodes. For larger time values the thermal impedance of the Type 2 module is higher which causes an increased mean junction temperature even though its losses are lower.

The temperature swings of the Type 5 module are much higher (10 – 13 K), but at a significantly lower mean value. The large temperature swings are caused by the relatively high thermal impedance at small time values (< 0.1 s). The low mean value comes from the small static thermal resistance (Fig. 4.6).

At higher speed the temperature swings become smaller (Fig. D.1) and smaller (Fig. D.2). At 10,000 rpm even the temperature swing of the IGBT in the Type 5 module at 450 V is only 2 K.

Regarding temperature swings the RC-IGBT provides a great advantage: In a module with single chips for IGBT and diode the current changes over to the nearby semiconductor when it switches its orientation in the motor phase. The formerly conducting chip enters a cool down phase until current changes back. This is not the case when using RC-IGBTs because IGBT and diode are combined in one chip. This leads to more stable power dissipation and, consequently, to a smoother junction temperature characteristic. The amplitude of the temperature swing can be reduced by a factor of more than two (compare Fig. 5.9-D.2).

In Fig. 5.10 the temperature characteristic in the different layers of each module is depicted. In the Type 1 and 2 module the layers adjacent to the chip follow the temperature swing, whereas, in the Type 5 module only the temperature of the chip swings and the leadframe temperature remains almost constant.

5.3.3 Power density

The simulation of the dc-dc converter focuses on the maximum output power under the condition of a maximum junction temperature of 125 °C. According to Fig. 5.11, the possible output power is within a range from 21 kW (Type 2) to 37 kW (Type 5) for the single chip configuration. This relates to the thermal equivalent circuits on which the simulation is based on. Changing from single chips to RC-IGBTs an output power increase of 15 – 20 % is obtained because of a better cooling performance. Usually, in a dc-dc converter with single chips the non-active chips are not used at all. They are only necessary when power flow is inverted or zero-crossing of the current occurs. Against this, in a RC-IGBT the chip area of the non-active elements is used as additional cooling path to reduce the thermal impedance (Fig. 2.5).

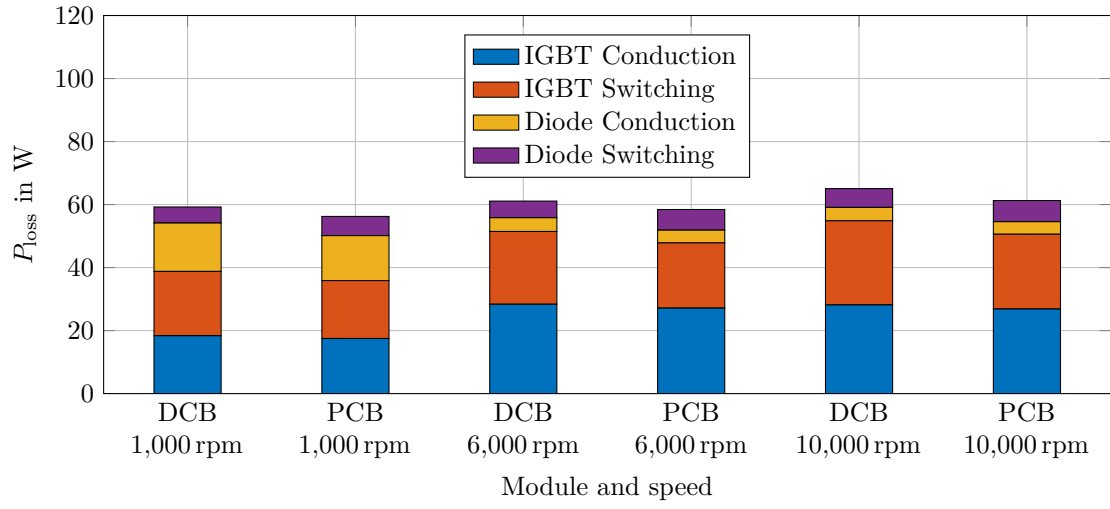
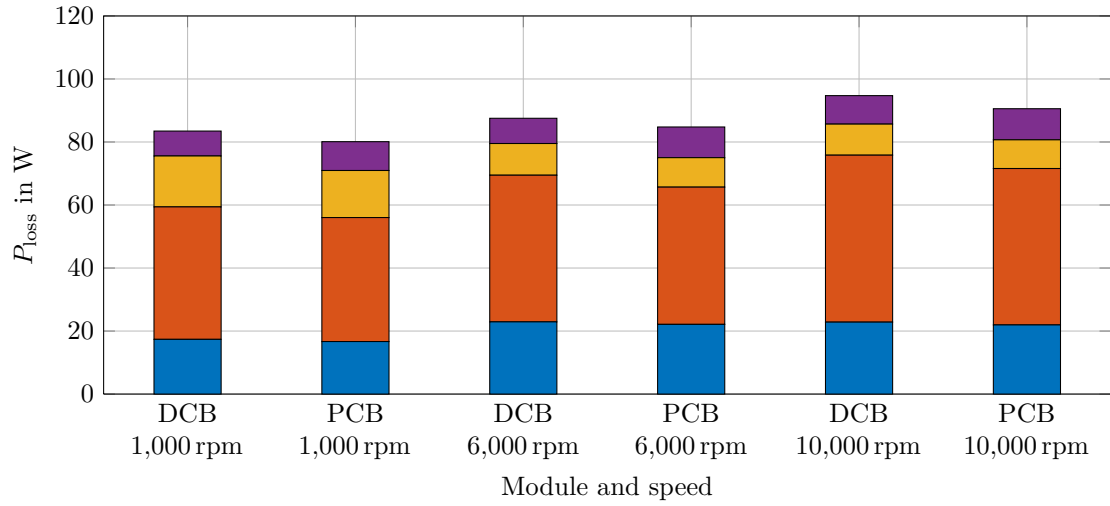
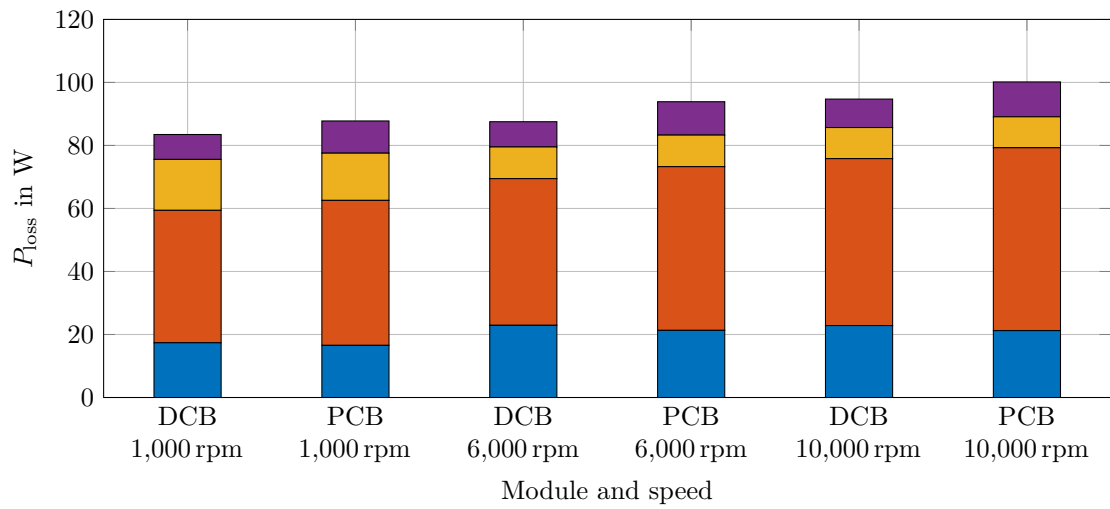
(a) $V_{DC} = 250$ V(b) $V_{DC} = 450$ V(c) $V_{DC} = 450$ V for DCB and $V_{DC} = 510$ V for PCB

Figure 5.8: Semiconductor losses per chip in B6 bridge

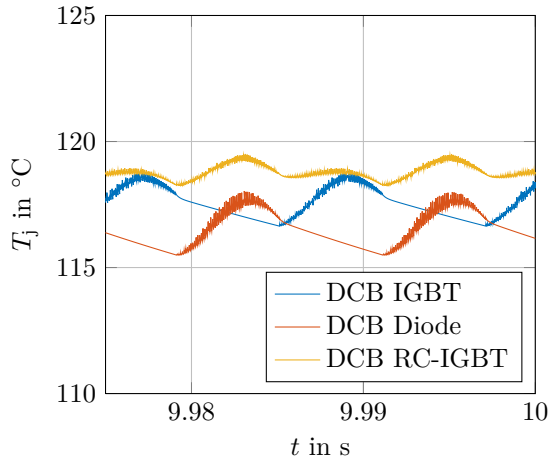
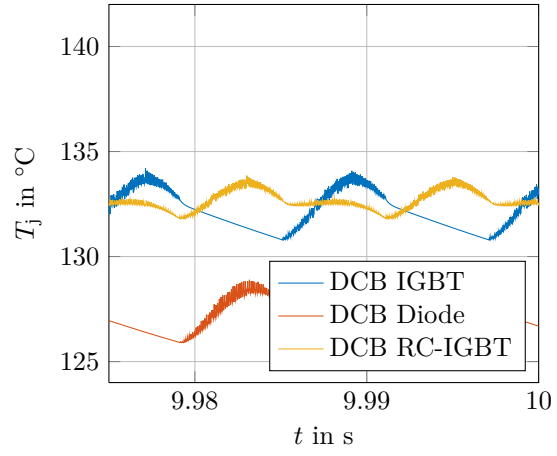
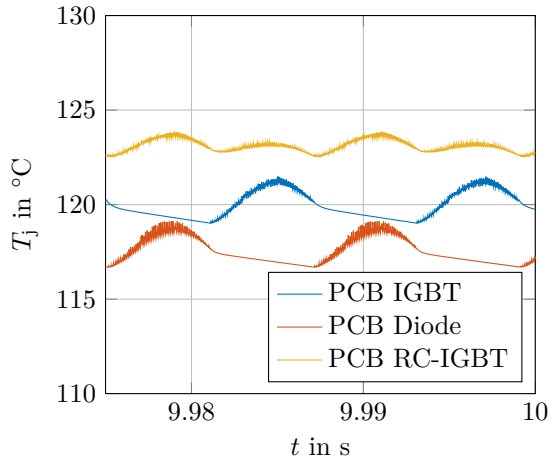
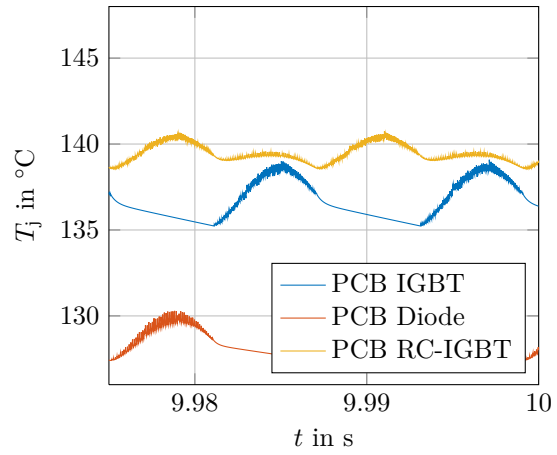
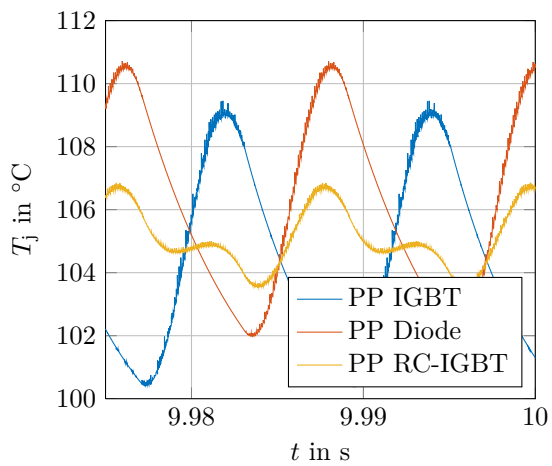
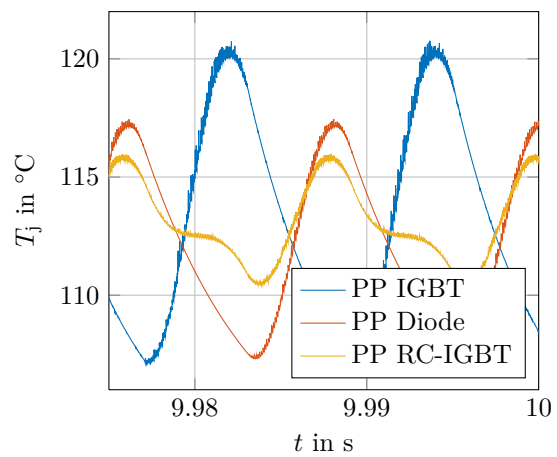
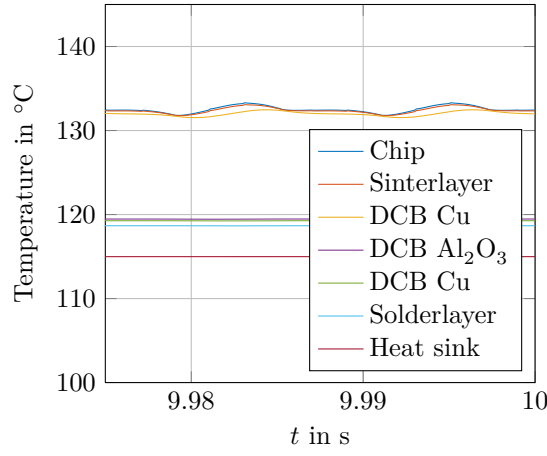
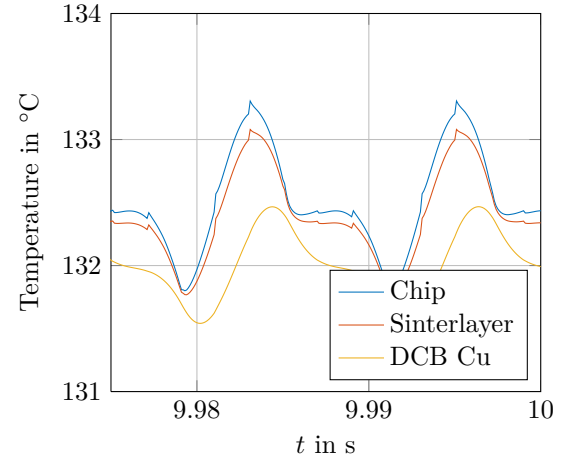
(a) Type 1, $V_{DC} = 250$ V(b) Type 1, $V_{DC} = 450$ V(c) Type 2, $V_{DC} = 250$ V(d) Type 2, $V_{DC} = 450$ V(e) Type 5, $V_{DC} = 250$ V(f) Type 5, $V_{DC} = 450$ V

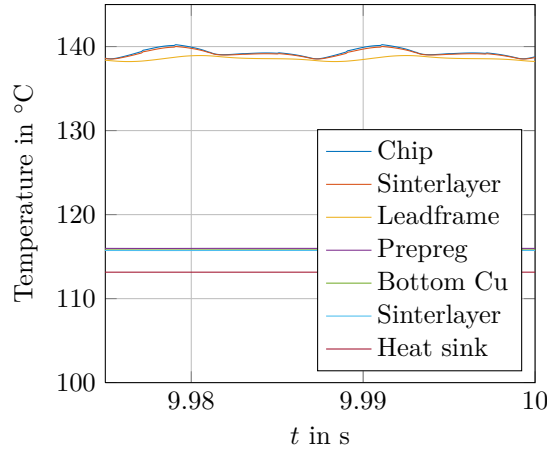
Figure 5.9: Junction temperature characteristic at 1,000 rpm



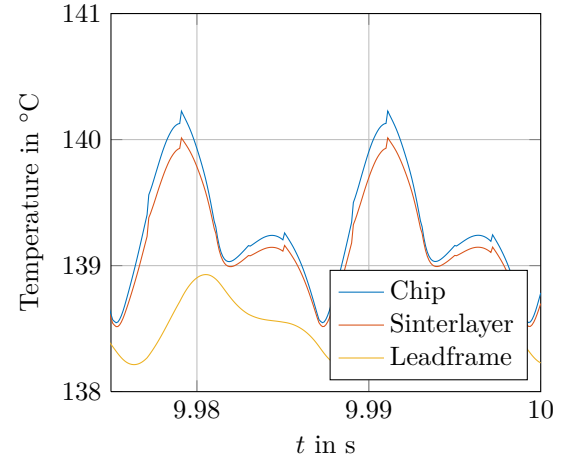
(a) Type 1



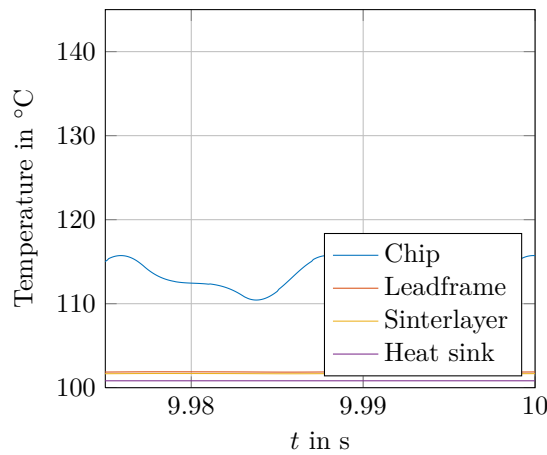
(b) Type 1



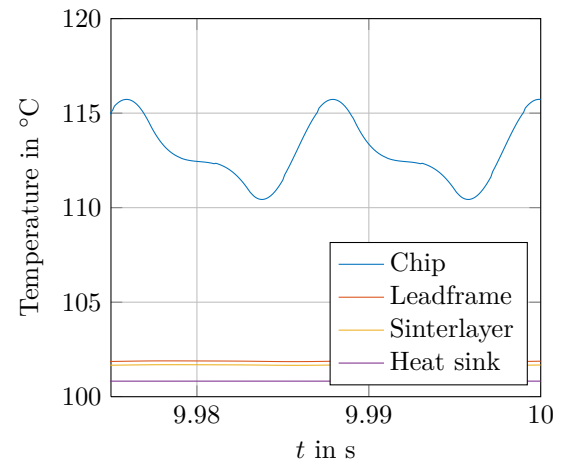
(c) Type 2



(d) Type 2



(e) Type 5



(f) Type 5

Figure 5.10: Temperature characteristic of each layer at 1,000 rpm and $V_{DC} = 450$ V

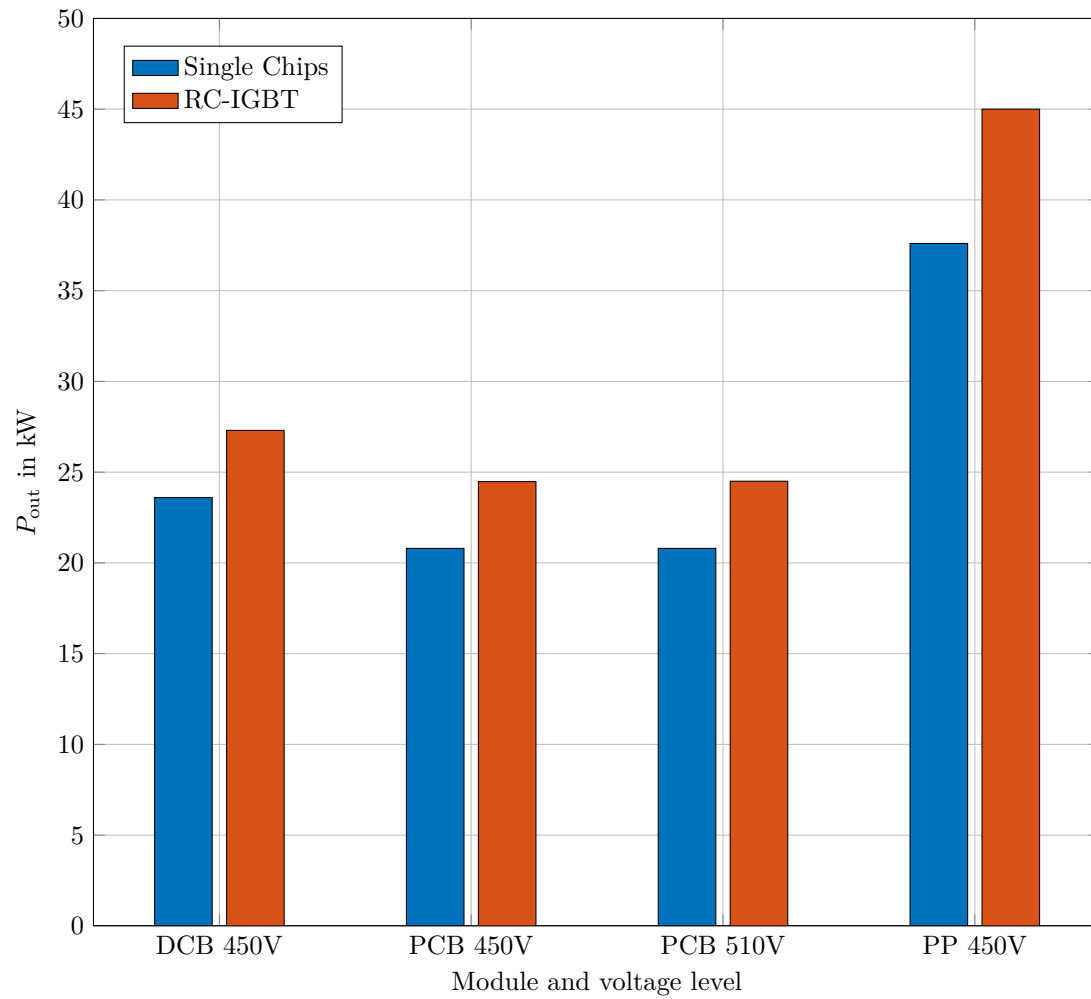


Figure 5.11: Maximum output power of dc-dc converter built with different module technologies

6 Conclusion

6.1 Summary

The objective of this work is to investigate several packaging technologies regarding their suitability for application within an automotive drive train. The simulation of a B6 drives inverter and a dc-dc converter that feeds the drives inverter with energy from the high-voltage battery is used to investigate the achievable power density of each packaging technology and the transient junction temperature characteristics. After discussing the evolution of power module technologies from the first industrial power module (in the year of 1975) to the state-of-the-art, chip embedding is introduced as an alternative packaging technology. It is shown how a 50-kW power module can be built that uses a high-current PCB as an integration platform for embedded power semiconductor chips. The prototype of this module, as well as a state-of-the-art DCB based module and a press-pack IGBT module are characterized by means of thermal and electrical measurements to build the database for the aforementioned simulations on converter level. Besides the measurements, thermal simulations of additional module concepts are done to study variants of PCB based power modules.

The thermal simulations of five different types of modules are done for transient operation modes. Losses are considered homogeneously inside the volume of the IGBT, the free-wheeling diode FWD and RC-IGBT chip, respectively. By suddenly rising the losses from zero to a certain constant positive value the thermal step response, i.e. the transient thermal impedance, of the modules is calculated. The double-sided cooling version of the PCB based power module reduces the stationary thermal resistance by more than 40 % compared to the single-sided cooling version. The press-pack module achieves one of the lowest steady-state thermal resistance. However, the transient thermal impedance at small times ($< 10^{-1}$ s) is high due to the pressure contact. This larger transient resistance causes larger temperature amplitudes during fast thermal cycles. The stationary thermal resistance of the PCB based power module is 17 % higher compared to the DCB based module. The PCB based module without electrical insulation shows an outstanding heat spreading capability which means that an increase of the cooling area highly decrease the thermal resistance. The heat spreading performance of the PCB based module with insulation does not differ from the DCB based module even though its leadframe is significantly thicker than the upper copper layer of the DCB. However, it is possible to highly improve the heat spreading by increasing the leadframe thickness from 0.55 mm to 2...3 mm which is theoretically possible in a PCB production process.

Thermal impedance measurements do not perfectly match the simulation results. Besides possible inaccuracies in the modeling and measurement, the main contributor

to the deviation is the difference between real module geometry and the simplified geometry used for the simulation. This is reasonable because larger deviations mainly occur at high time constants. For use of the thermal impedances in the converter simulations, they are fitted with a Foster network approach. Four RC-elements are found to be sufficient to achieve good accuracy. Additionally, a physically correct thermal Cauer network is generated to enable the simulation of temperatures of all the layers inside the power modules.

Besides the thermal description of the power modules, their electrical parameters are required as input data for the converter simulations. This comprises the conduction as well as the switching losses and, moreover, the occurring overvoltages during IGBT turn-off. The DCB based power module and the PCB based module are extensively tested to get a comprehensive overview of their aforementioned electrical characteristics. It turns out that the lower dc-link stray inductance of the PCB based module causes significantly reduced switching losses (up to 40 %, depending on the operation point). Moreover, the absence of bond wires clearly improves the conduction behavior by reducing the forward voltage drop. The turn-off overvoltages of the modules are mainly determined by their dc-link stray inductance (assuming the same gate control circuit is used). During the design phase of the PCB based module this was accounted for by simulating and optimizing this parasitic inductance with the help of a PEEC tool. Dc-link stray inductance measurements validate the simulation results. With 1.5 nH the inductance is ten times lower compared to the state-of-the-art power module. Finally, the measurement of the EMC performance shows almost identical common mode interference. However, above 1 MHz the differential mode interferences are much lower for the low-inductive PCB based module.

The advantage of PCB based power modules on system level are discussed in chapter 5. Amongst other aspects, a concept for a PCB integrated Rogowski coil is studied that even allows the measurement of dc output currents. The converter simulations are used to deduce the advantage of the PCB based module regarding losses in a real application. In the drives inverter the overall losses are reduced by 5 %. Taking into account the lower overvoltage that allows to increase the dc-link voltage a loss reduction of 14 % is possible. A dc-dc converter in steady state operates at almost constant temperature. Hence, the transient junction temperature characteristics are investigated using the example of the drives inverter that produces more or less sinusoidal output currents. Due to their comparable thermal impedances in the range of up to 0.1 s the DCB and PCB based power modules show similar junction temperature swinging characteristics. Contrary to this, the temperature swing of the press-pack module is much larger due to the high transient thermal impedance at low time constants. The RC-IGBT is able to reduce the temperature swings by a factor of more than two because both losses of IGBT and FWD are generated inside the same chip. The simulation of the dc-dc converter focuses on the maximum output power that can be achieved while keeping the junction temperature below 125 °C. Even though the losses of the PCB based module are lower compared to the DCB based module, its higher steady-state thermal resistance leads to a lower

maximum output power. The press-pack module allows approximately 60 % more output power due to its superior stationary thermal resistance. The RC-IGBT allows to increase the output power by 15 – 20 % because a larger chip area is used for cooling compared to the standard chip configuration.

6.2 Future Work

The tool chain presented in this work reaches from the thermal and electrical design of IGBT power modules via their characterization measurements to system simulations. The simulation output data comprises maximum output power and temperature characteristics of all layers within the module. Together with a detailed mission profile, the junction temperature characteristic can be used as an input to a lifetime model in order to predict the lifetime of the power module, possibly limiting the maximum output power to a lower value than calculated before. The advantage regarding lifetime of the RC-IGBT by reducing temperature swings could be quantified with this and reveal its potential for the respective module concept. The lifetime model has to be obtained from power cycling test. The detailed thermal simulation of the different layers can be used to find the most critical material joints. For this, detailed lifetime models of these material joints are required.

The cost structure of different module concepts is only roughly sketched in chapter 5. A more detailed investigation requires the collection of data regarding material and production process costs as well as an analysis of the expenditures regarding cooling, passive components, EMC filter and installation space.

The thermal impedances of the power modules used for system simulation were taken from thermal simulations. This ensured good comparability between all module concepts. However, the thermal impedance measurements with the available prototypes showed distinct deviations from the simulation results. The main reason for this has not been clearly identified so far. To solve this issue the same geometry has to be used for simulation and measurement which means that either the simulation model has to represent the complete module or measurement samples have to be built that reproduce the simplified geometry that was used in the simulation.

The thermal coupling between IGBT and FWD is taken into account by connecting them to the same heatsink in the thermal Cauer network. This produces fairly accurate results. A more sophisticated approach is to measure the thermal transfer functions between all chips which leads to a multi-terminal thermal network. However, with this method it will be very complicated to generate a Cauer network that represents the real physical module geometry.

Apparently, the amplitude of the junction temperature swings are quite moderate in the examined application due to the high fundamental frequency of the output currents even at low speed of the electric motor. In other applications, such as DFIG systems (doubly-fed induction generator) for wind turbines, much lower frequencies occur. This might utilize the temperature swing reducing properties of the RC-IGBT

even more than in automotive applications and is worth an investigation if the aforementioned lifetime model is made available.

A Material Parameters

Table A.1: Thermal properties of packaging materials

	Thermal conductivity in W/(m · K)	Thermal capacity in J/(g · K)	Thermal capacity in J/(cm ³ · K)
Si	130	0.70	1.63
Cu	400	0.39	3.35
Al ₂ O ₃	24	0.73	2.90
Prepreg	2.5	1.37	2.60
Solder (Sn)	63	0.23	1.65
Ag sinter layer	250	0.24	1.43
Laservias (30 %)	122	1.07	2.83
Laservias (5 %)	22	1.32	2.64

Table A.2: Mechanical properties of packaging materials

	CTE in 10 ⁻⁶ /K	Density in g/cm ³	Young's modulus in GPa
Si	2.6	2.33	170
Cu	17.0	8.70	110
Al ₂ O ₃	6.5	3.97	400
Prepreg	18.0	1.90	22
Ag sinter layer	18.9	6.10	83
Solder (Sn)	23	7.3	50
Laservias (30 % density)	17.7	3.94	48
Laservias (5 % density)	18.0	2.24	26

B Thermal Simulation Results

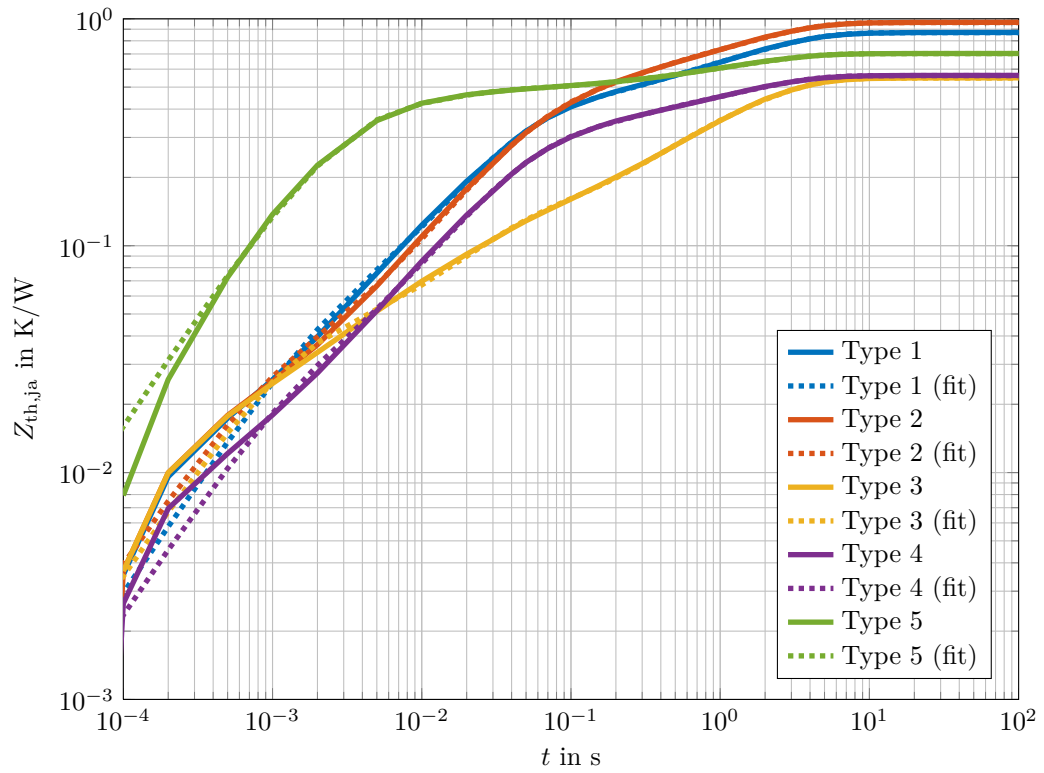


Figure B.1: Diode thermal impedance simulation results (Foster fitting)

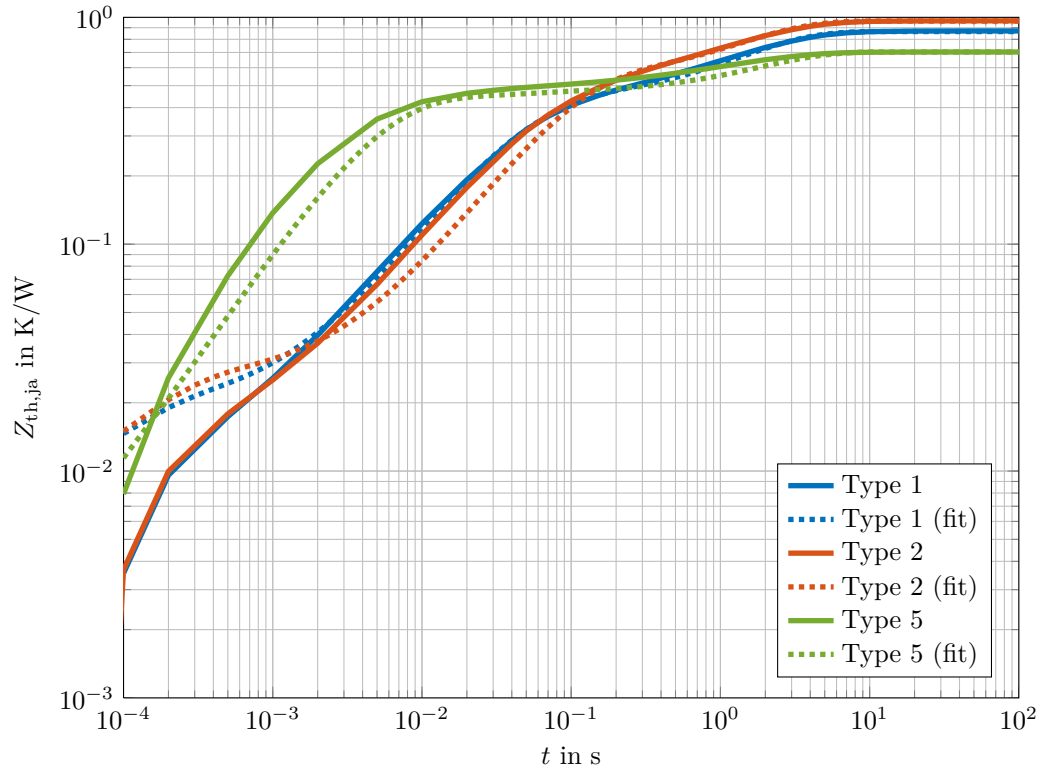


Figure B.2: Diode thermal impedance simulation results (Cauer fitting)

Table B.1: Fitting parameter of diode thermal impedance curves (Foster model)

	i	1	2	3	4
Type 1	R_i in Ω	$3.52 \cdot 10^{-1}$	$1.34 \cdot 10^{-1}$	$3.31 \cdot 10^{-2}$	$3.50 \cdot 10^{-1}$
	τ_i in s	$3.74 \cdot 10^{-2}$	$3.33 \cdot 10^{-1}$	$1.65 \cdot 10^{-3}$	$2.10 \cdot 10^0$
Type 2	R_i in Ω	$3.47 \cdot 10^{-1}$	$3.82 \cdot 10^{-1}$	$2.12 \cdot 10^{-1}$	$2.26 \cdot 10^{-2}$
	τ_i in s	$4.18 \cdot 10^{-2}$	$1.94 \cdot 10^0$	$2.45 \cdot 10^{-1}$	$7.01 \cdot 10^{-4}$
Type 3	R_i in Ω	$3.09 \cdot 10^{-1}$	$1.18 \cdot 10^{-1}$	$8.50 \cdot 10^{-2}$	$3.62 \cdot 10^{-2}$
	τ_i in s	$1.88 \cdot 10^0$	$3.99 \cdot 10^{-1}$	$2.69 \cdot 10^{-2}$	$1.11 \cdot 10^{-3}$
Type 4	R_i in Ω	$2.56 \cdot 10^{-1}$	$1.01 \cdot 10^{-1}$	$1.79 \cdot 10^{-2}$	$1.88 \cdot 10^{-1}$
	τ_i in s	$3.73 \cdot 10^{-2}$	$2.20 \cdot 10^{-1}$	$1.06 \cdot 10^{-3}$	$1.78 \cdot 10^0$
Type 5	R_i in Ω	$1.15 \cdot 10^{-1}$	$3.66 \cdot 10^{-1}$	$1.66 \cdot 10^{-1}$	$5.49 \cdot 10^{-2}$
	τ_i in s	$1.36 \cdot 10^{-2}$	$2.38 \cdot 10^{-3}$	$1.78 \cdot 10^0$	$2.83 \cdot 10^{-1}$

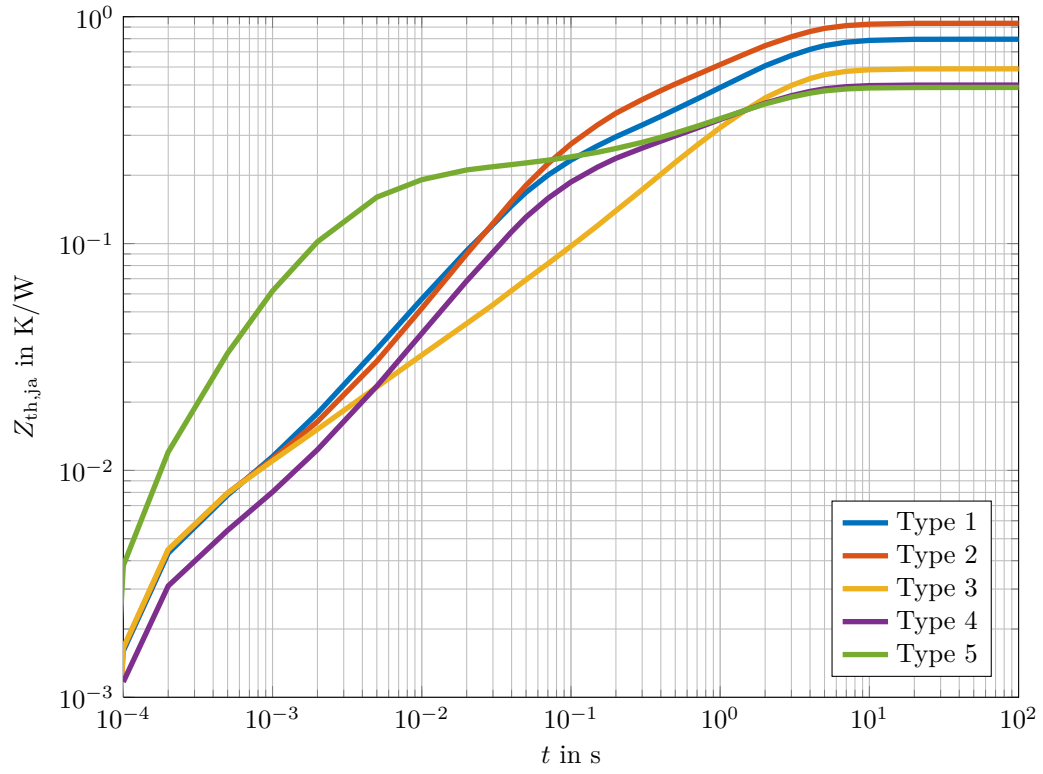


Figure B.3: IGBT thermal impedance simulation results (Diode heated simultaneously)

Table B.2: Fitting parameter of RC-IGBT thermal impedance curves (Foster model)

	i	1	2	3	4
Type 1	R_i in Ω	$9.92 \cdot 10^{-2}$	$1.40 \cdot 10^{-1}$	$8.83 \cdot 10^{-3}$	$3.21 \cdot 10^{-1}$
	τ_i in s	$3.65 \cdot 10^{-1}$	$4.93 \cdot 10^{-2}$	$1.34 \cdot 10^{-3}$	$2.21 \cdot 10^0$
Type 2	R_i in Ω	$5.13 \cdot 10^{-3}$	$1.23 \cdot 10^{-1}$	$3.40 \cdot 10^{-1}$	$2.10 \cdot 10^{-1}$
	τ_i in s	$3.72 \cdot 10^{-4}$	$3.59 \cdot 10^{-1}$	$2.10 \cdot 10^0$	$7.72 \cdot 10^{-2}$
Type 3	R_i in Ω	$1.24 \cdot 10^{-2}$	$2.93 \cdot 10^{-2}$	$8.68 \cdot 10^{-2}$	$2.90 \cdot 10^{-1}$
	τ_i in s	$1.35 \cdot 10^{-3}$	$4.58 \cdot 10^{-2}$	$4.01 \cdot 10^{-1}$	$1.94 \cdot 10^{-0}$
Type 4	R_i in Ω	$6.05 \cdot 10^{-2}$	$1.64 \cdot 10^{-1}$	$1.33 \cdot 10^{-1}$	$3.84 \cdot 10^{-3}$
	τ_i in s	$3.22 \cdot 10^{-1}$	$1.94 \cdot 10^0$	$5.86 \cdot 10^{-2}$	$5.03 \cdot 10^{-4}$
Type 5	R_i in Ω	$3.92 \cdot 10^{-2}$	$1.08 \cdot 10^{-1}$	$1.53 \cdot 10^{-1}$	$4.52 \cdot 10^{-2}$
	τ_i in s	$1.14 \cdot 10^{-2}$	$2.29 \cdot 10^{-3}$	$1.86 \cdot 10^0$	$2.78 \cdot 10^{-1}$

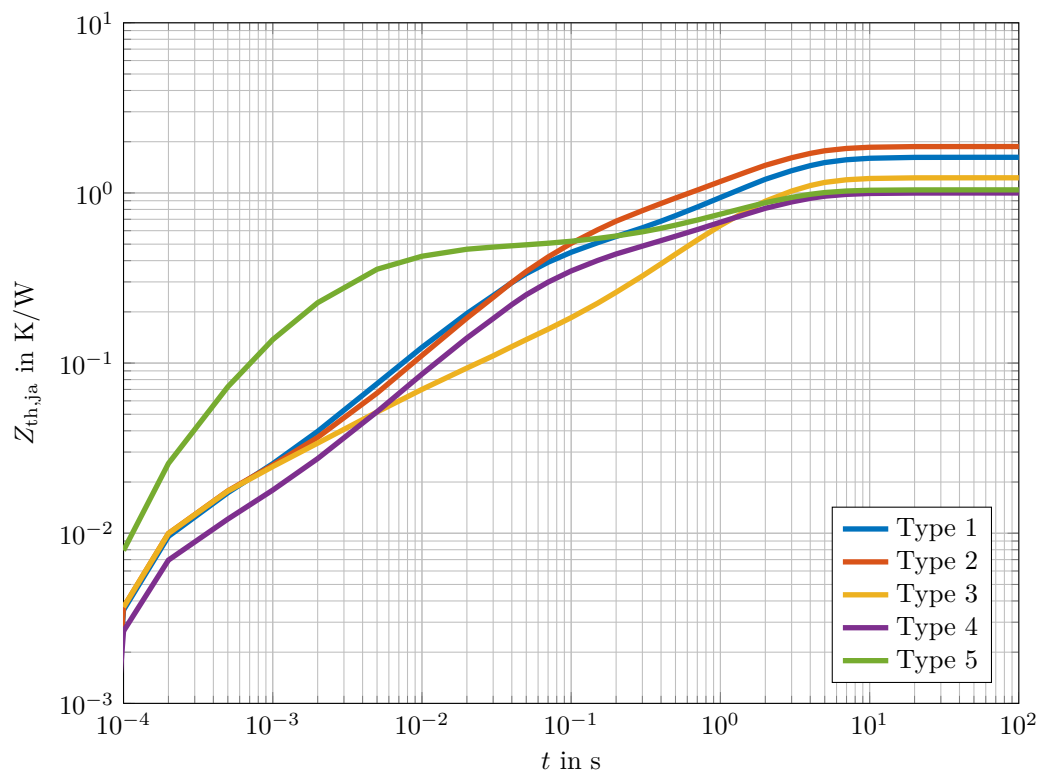


Figure B.4: Diode thermal impedance simulation results (IGBT heated simultaneously)

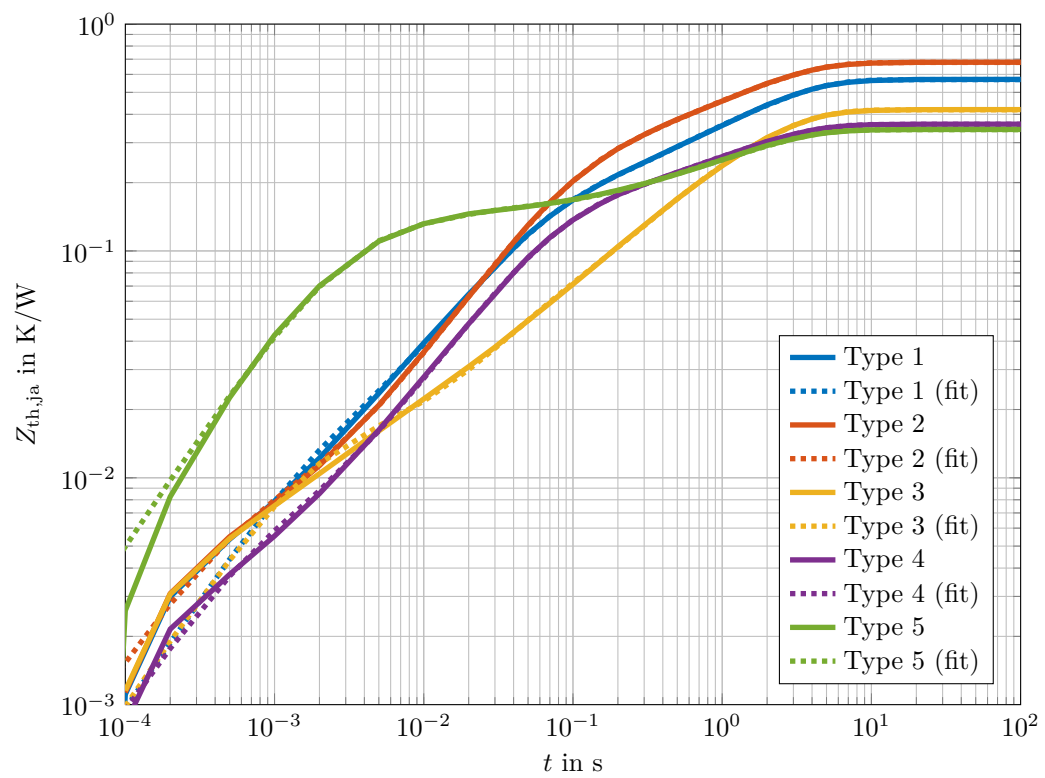


Figure B.5: RC-IGBT thermal impedance simulation results (Foster fitting)

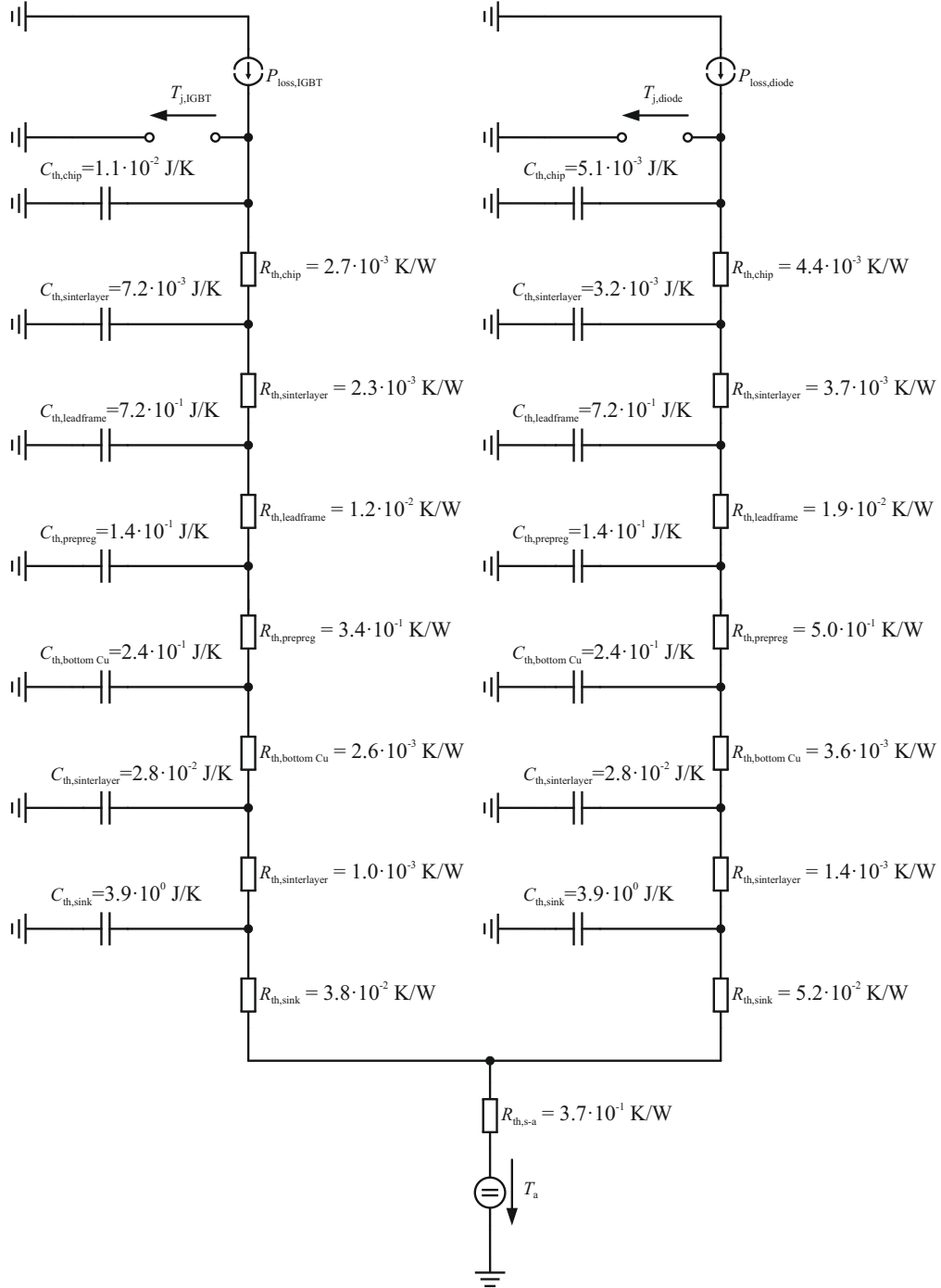


Figure B.6: Cauer thermal equivalent circuit Type 2 module

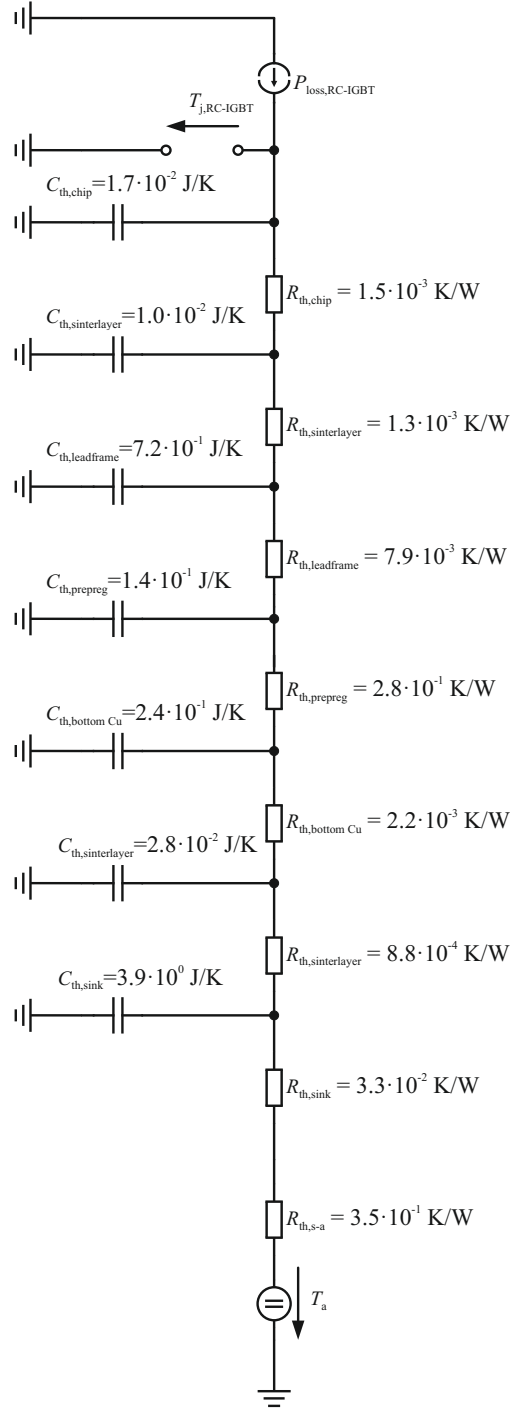


Figure B.7: Cauer thermal equivalent circuit Type 2 module with RC-IGBT

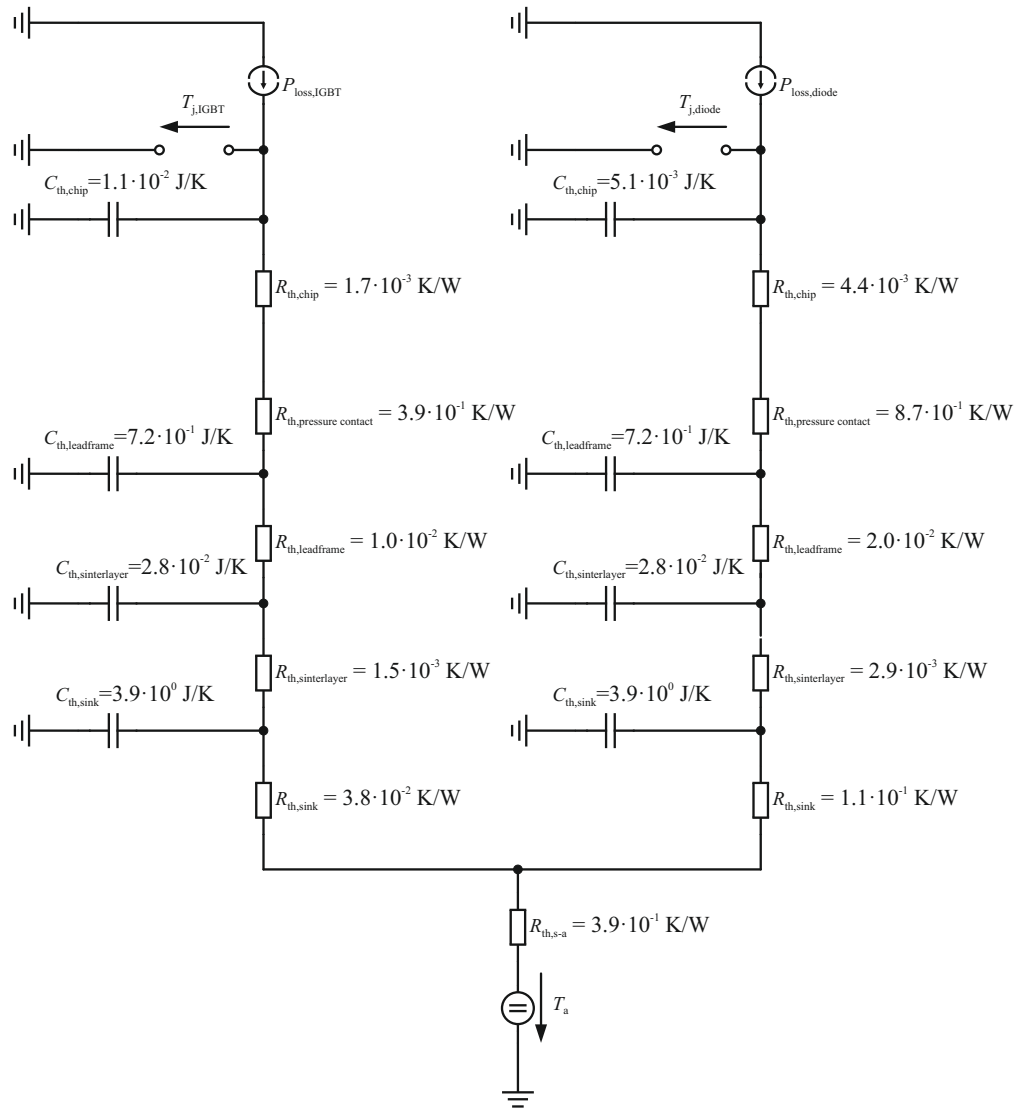


Figure B.8: Cauer thermal equivalent circuit Type 5 module

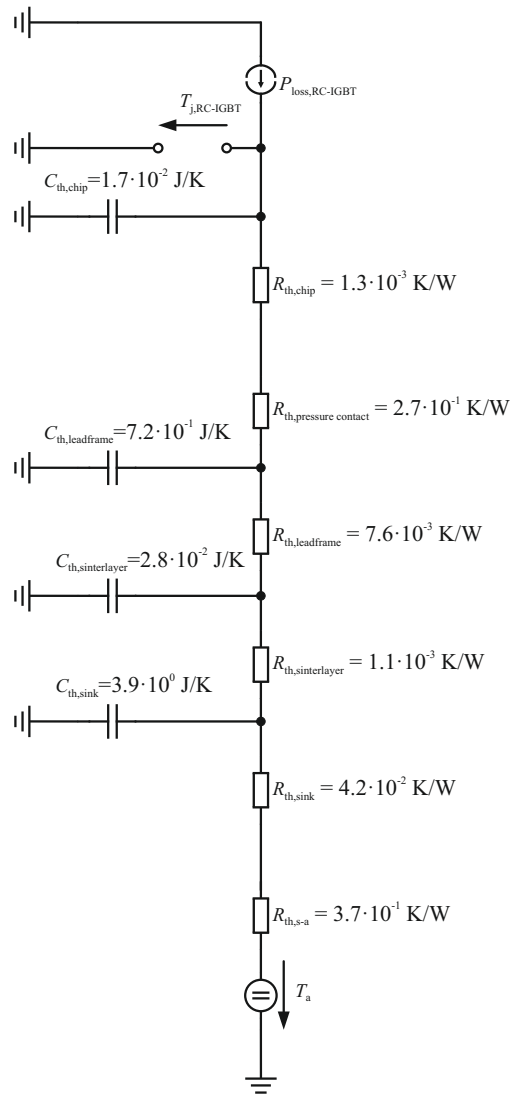


Figure B.9: Cauer thermal equivalent circuit Type 5 module with RC-IGBT

C Electrical Measurements Results

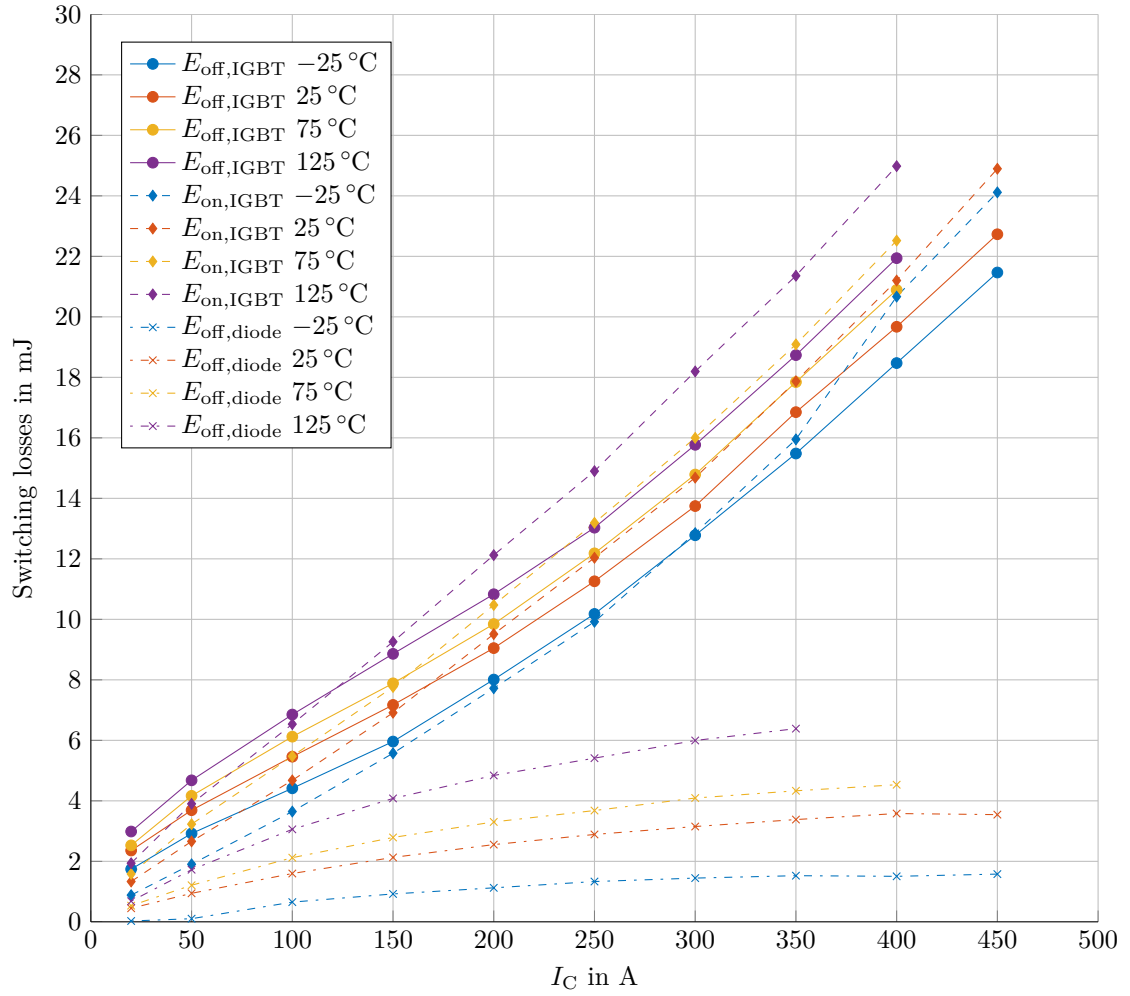


Figure C.1: Switching losses Type 1 at 400 V

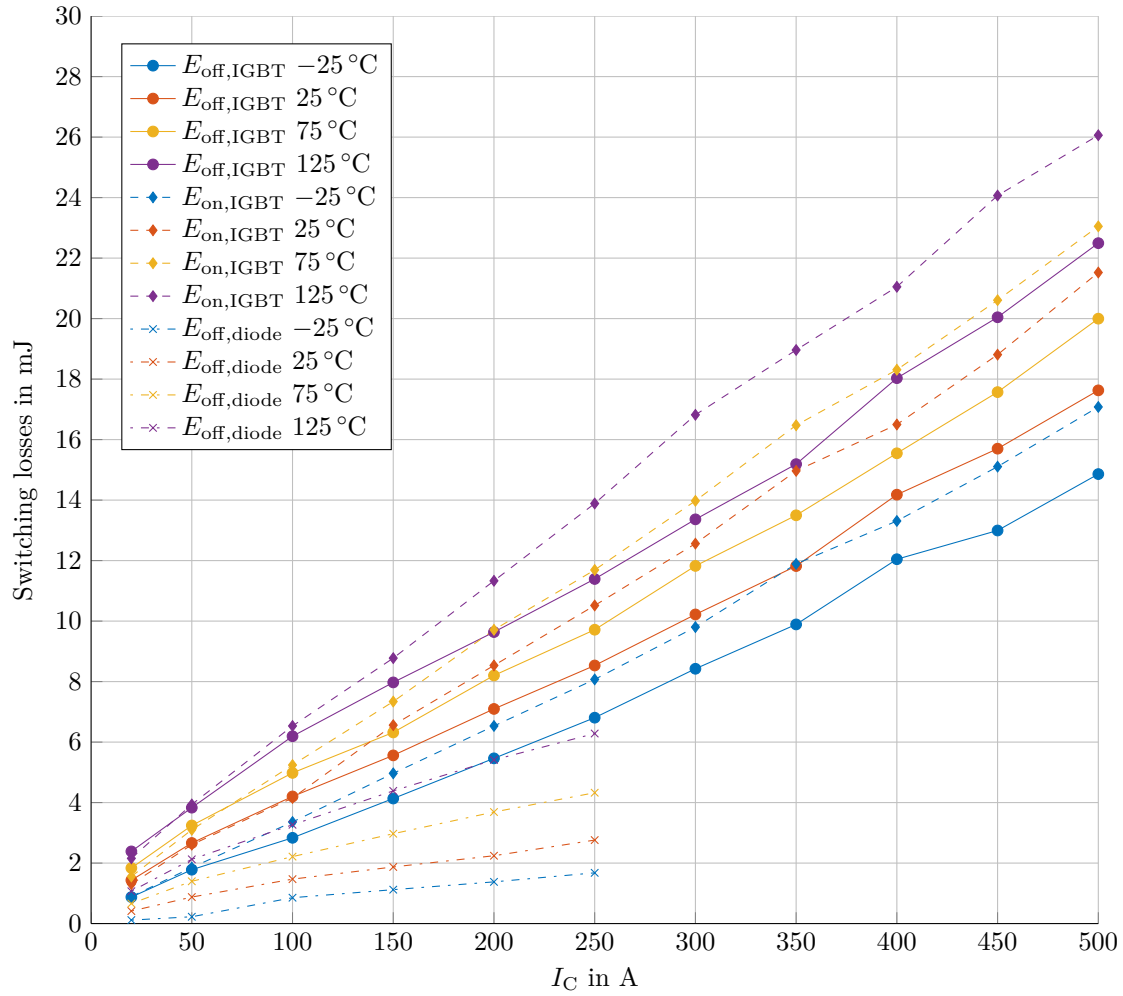


Figure C.2: Switching losses Type 2 at 400 V

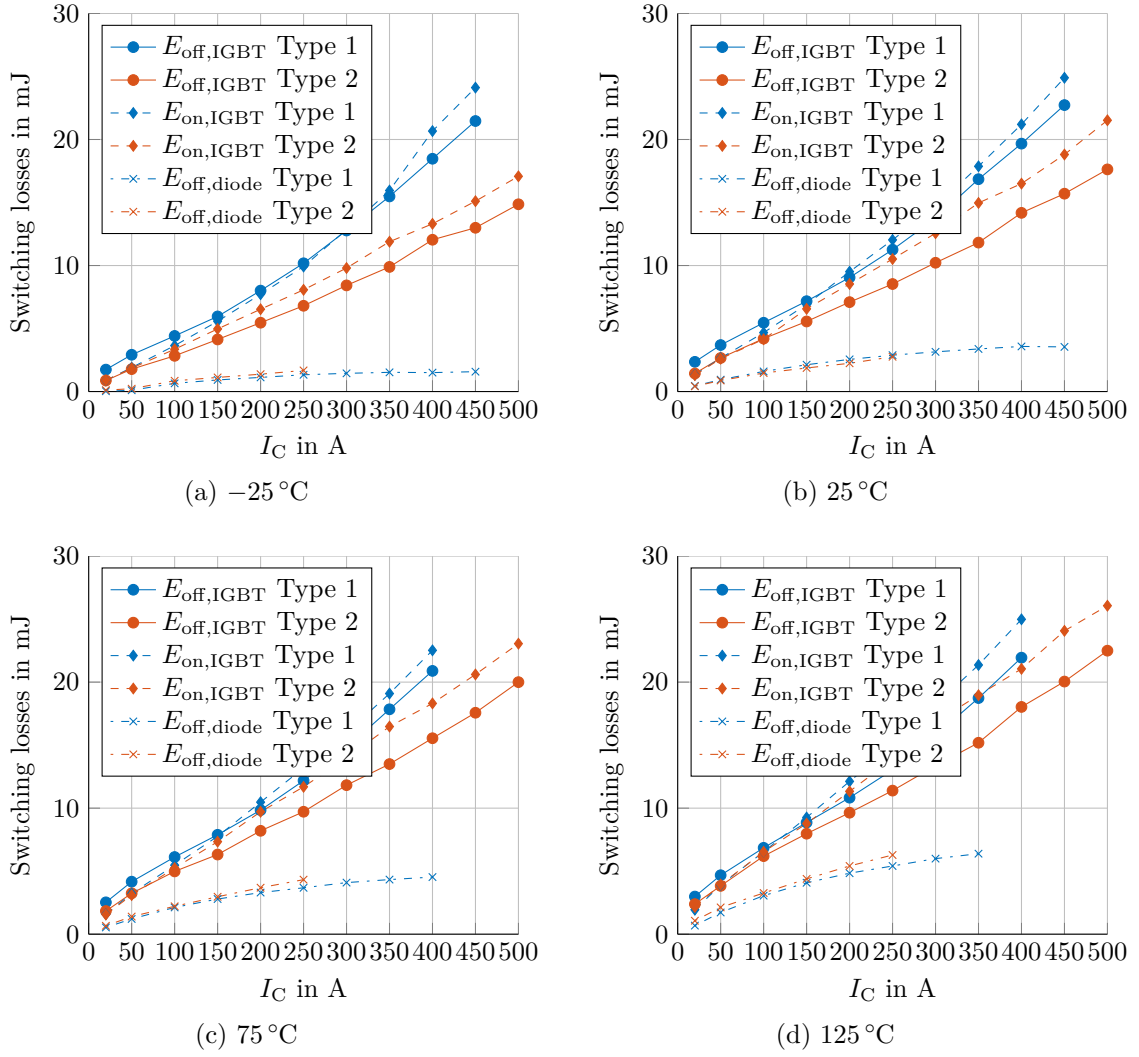


Figure C.3: Comparison of the switching losses at 400 V

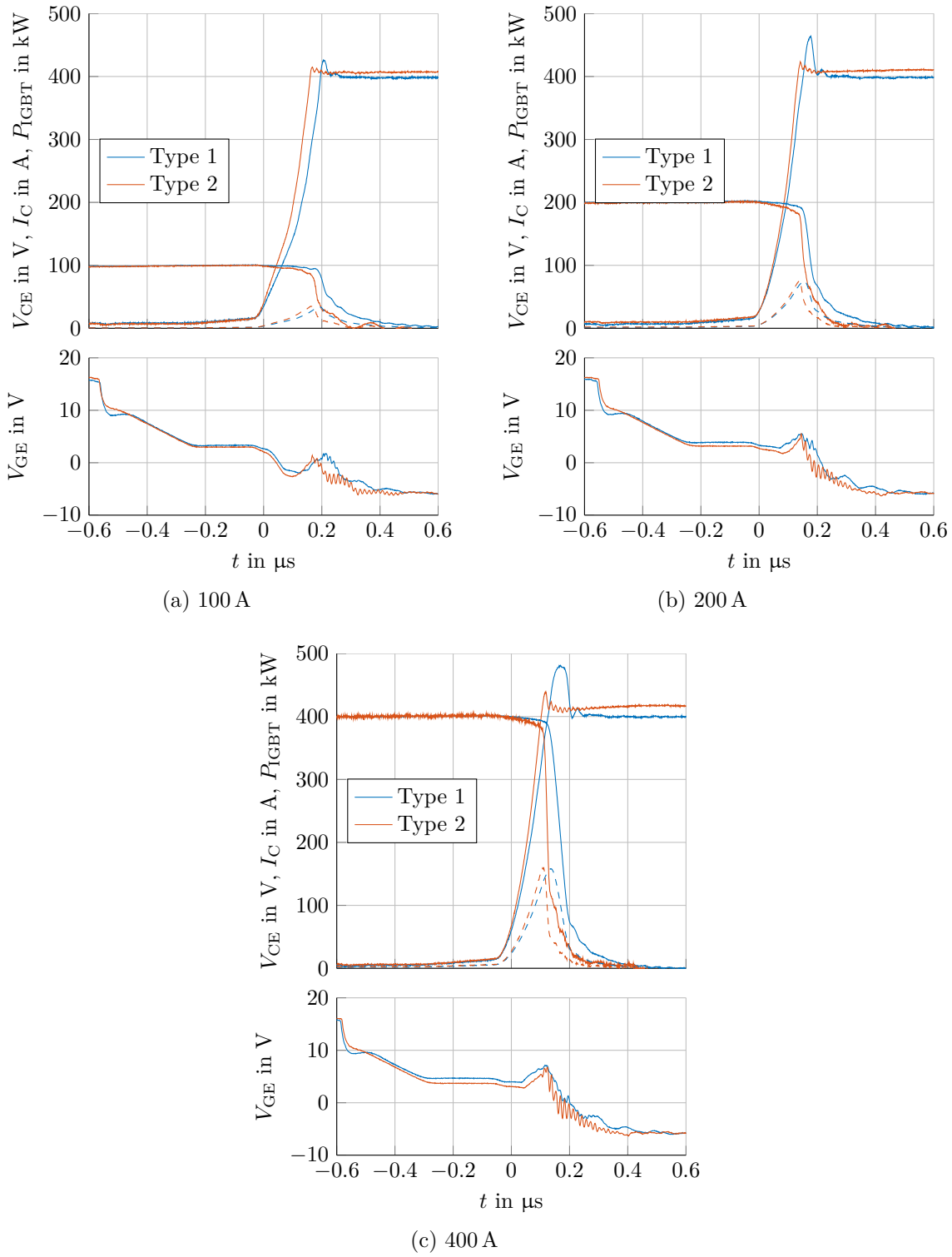


Figure C.4: Comparison of the turn-off at 400 V and 25 °C

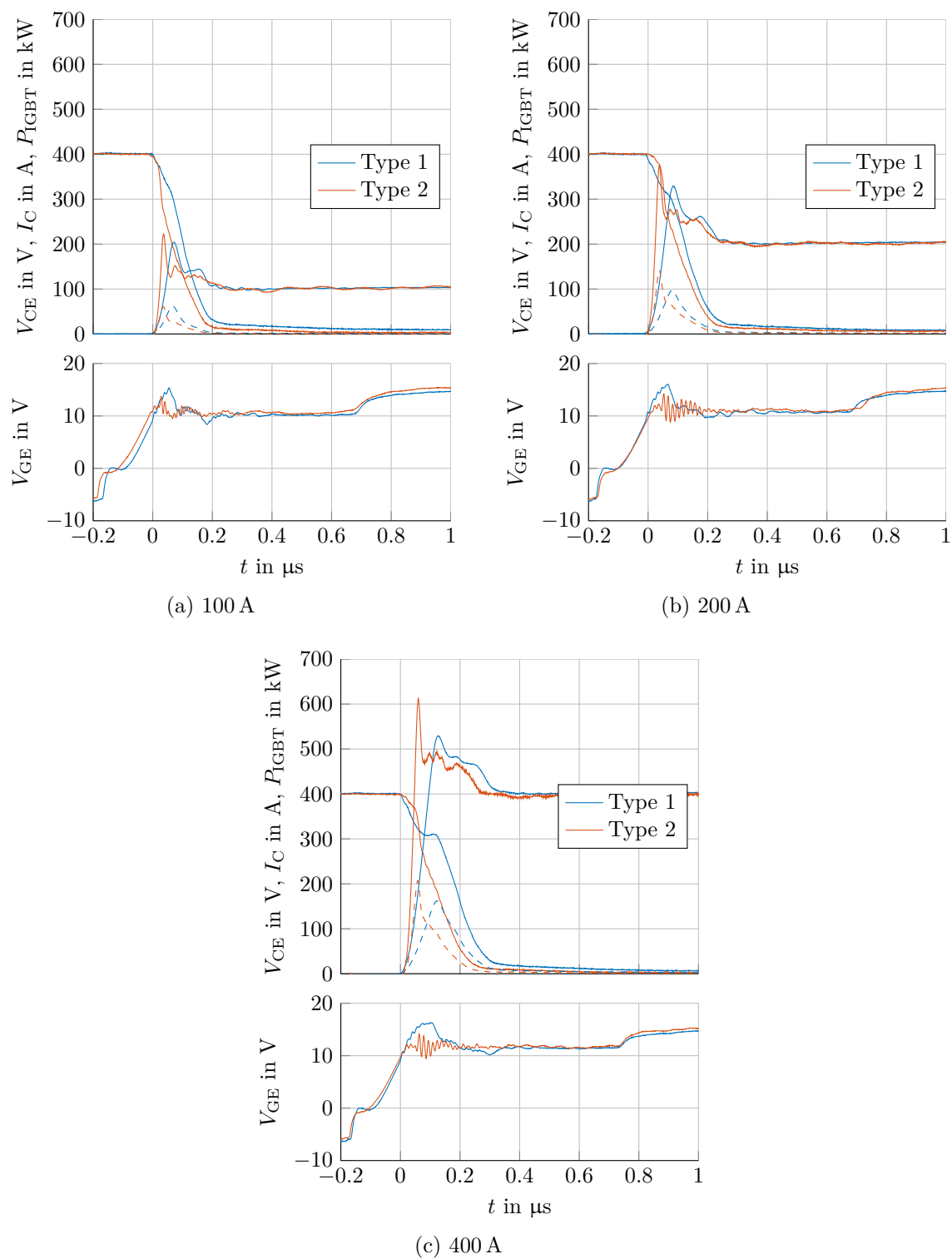
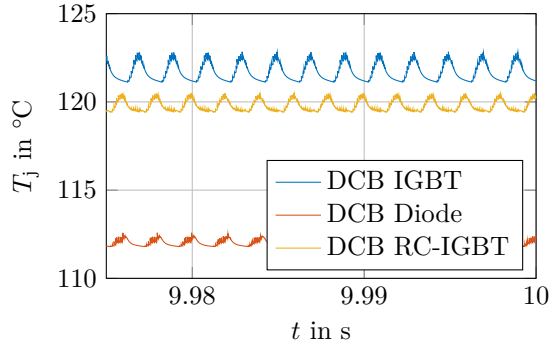
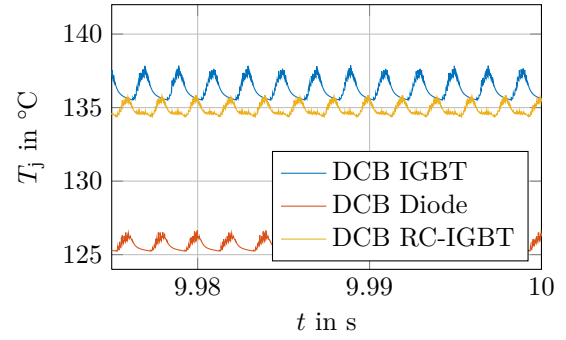


Figure C.5: Comparison of the turn-on characteristic at 400 V and 25 °C

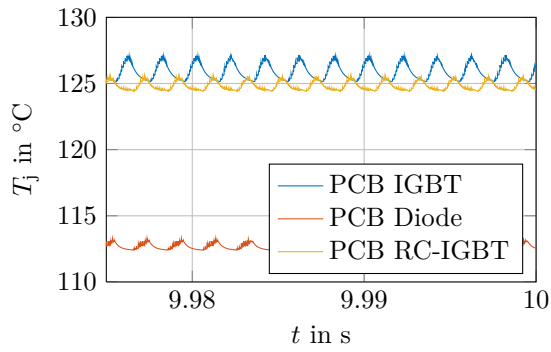
D System Simulation Results



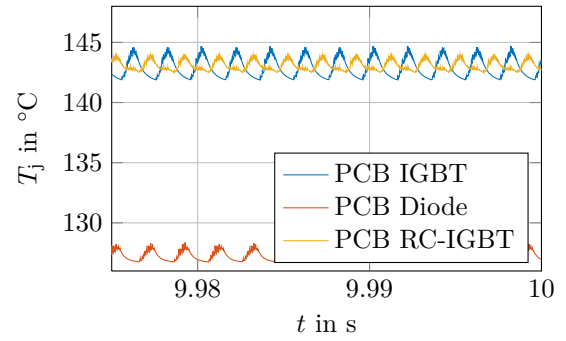
(a) Type 1, $V_{DC} = 250$ V



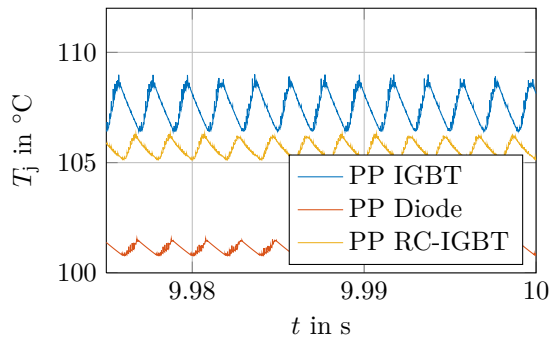
(b) Type 1, $V_{DC} = 450$ V



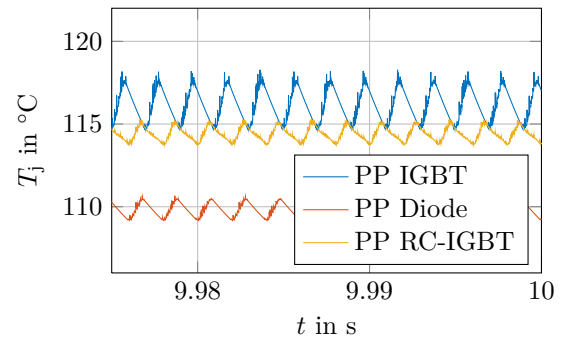
(c) Type 2, $V_{DC} = 250$ V



(d) Type 2, $V_{DC} = 450$ V



(e) Type 5, $V_{DC} = 250$ V



(f) Type 5, $V_{DC} = 450$ V

Figure D.1: Junction temperature characteristic at 6,000 rpm

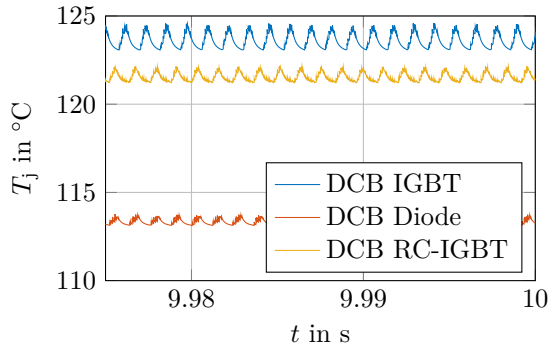
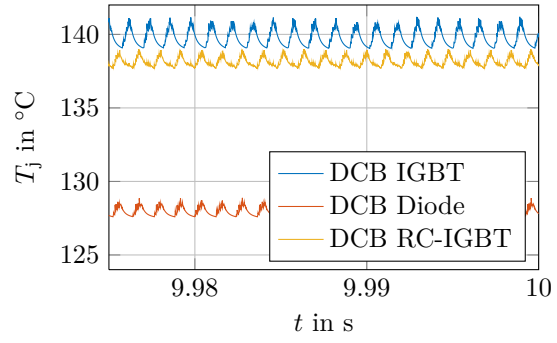
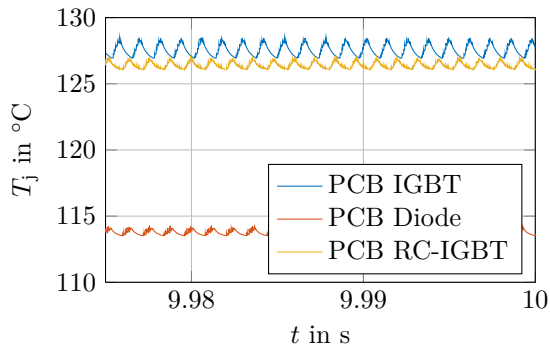
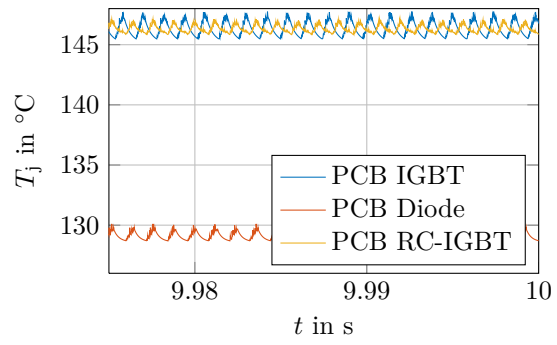
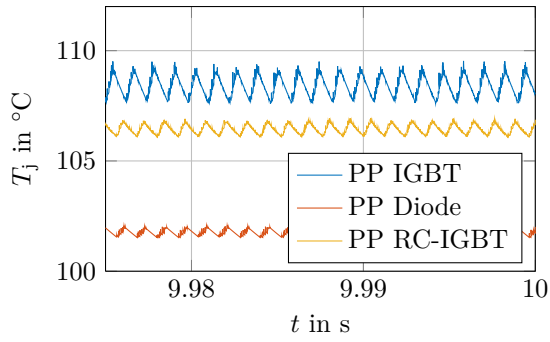
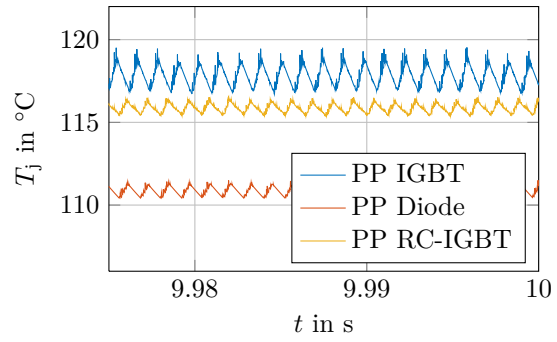
(a) Type 1, $V_{DC} = 250$ V(b) Type 1, $V_{DC} = 450$ V(c) Type 2, $V_{DC} = 250$ V(d) Type 2, $V_{DC} = 450$ V(e) Type 5, $V_{DC} = 250$ V(f) Type 5, $V_{DC} = 450$ V

Figure D.2: Junction temperature characteristic at 10,000 rpm

List of Abbreviations

AC	Alternating current
ASIC	Application-specific integrated circuit
BIGT	Bi-mode insulated gate transistor
CCM	Continuous conduction mode
CTE	Coefficient of thermal expansion
DC	Direct current
DCB	Direct copper bonded
DFIG	Doubly-fed induction generator
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EU	European union
EV	Electric vehicle
FEM	Finite element method
FWD	Free-wheeling diode
HDI	High density interconnect
HEV	Hybrid electric vehicle
HSI	Heat spreading index
HVDC	High-voltage, direct current
IGBT	Insulated gate bipolar transistor
IMS	Insulated metal substrate
LISN	Line impedance stabilization network
MOSFET	Metal-oxide-semiconductor field-effect transistor
MTBF	Mean-time between failures
NPT-IGBT	Non-punch-through IGBT
PCB	Printed circuit board
PEEC	Partial element equivalent circuit
PHEV	Plug-in hybrid electric vehicle

PMSM	Permanent magnet synchronous machine
PT-IGBT	Punch-through IGBT
PWM	Pulse width modulation
PZEV	Partial zero emission vehicle
RC-IGBT	Reverse conducting insulated gate bipolar transistor
SVM	Space vector modulation
VSI	Voltage source inverter
ZEV	Zero emission vehicle

List of Symbols

α	Heat transfer coefficient
ϵ	Emissivity
$\Delta\epsilon_p$	Plastic strain
λ	Thermal conductivity
μ_n	Electrons mobility
μ_p	Holes mobility
μ_0	Permeability of vacuum (magnetic constant)
σ	Stefan-Boltzmann constant
σ_{el}	Electrical conductivity
τ_{eff}	Charge carrier lifetime
A	Surface area
A_{CM}	Acceleration factor for number of cycles
A_T	Thermal acceleration factor
C_{el}	Electrical capacitance
C_{th}	Thermal capacitance
DC-	Lower potential of the dc-link in a converter
DC+	Higher potential of the dc-link in a converter
E_A	Activation energy
$E_{off,diode}$	Diode turn-off losses (Reverse-recovery losses)
$E_{off,IGBT}$	IGBT turn-off losses
$E_{on,IGBT}$	IGBT turn-on losses
H	Magnetic field strength
I_C	Collector current of an IGBT
I	Electrical current
I_F	Forward current of a diode
I_{load}	Heating current for thermal impedance measurements
I_{meas}	Measurement current to detect temperature during thermal impedance measurements
L_σ	Stray inductance
L_{TA}	Lifetime at elevated test temperature
L_{Tu}	Lifetime under normal operation temperature
N_f	Number of cycles to failure
N_{fA}	Number of cycles to failure at increased thermal cycling magnitude
N_{fu}	Number of cycles to failure under normal operation temperature

N_{passive}	Number of passive temperature cycles
N_{pole}	Number of pole pairs
P_{diode}	Losses in a diode chip
P_{IGBT}	Losses in an IGBT chip
P_{loss}	Power losses
P_{max}	Maximum power
Q	Thermal energy
$\dot{Q}$	Heat flow
$\dot{Q}_{\text{cond}}$	Heat flow by conduction
$\dot{Q}_{\text{conv}}$	Heat flow by convection
$\dot{Q}_{\text{rad}}$	Heat flow by radiation
R	Universal gas constant
R_{el}	Electrical resistance
R_{th}	Thermal resistance
$R_{\text{th,ja},0}$	Thermal resistance from junction to ambient without heat spreading
$R_{\text{th,ja,min}}$	Thermal resistance from junction to ambient with maximum heat spreading
T	Temperature
∇T	Temperature gradient
T_{A}	Elevated temperature during accelerated lifetime test
T_{a}	Ambient temperature
ΔT_{A}	Magnitude of thermal cycles during test
T_{high}	Higher temperature limit of standard automotive passive temperature cycle
T_{j}	Junction temperature
T_{low}	Lower temperature limit of standard automotive passive temperature cycle
T_{m}	Medium junction temperature during power cycling
T_{s}	Heat sink temperature
T_{u}	Temperature at normal operation
ΔT_{u}	Magnitude of thermal cycles during normal operation
V	Electrical voltage
V_{CE}	Collector-emitter voltage of an IGBT
V_{cm}	Common mode disturbance in EMC measurement
V_{dm}	Differential mode disturbance in EMC measurement
V_{drift}	Voltage across the drift region
V_{F}	Forward voltage of a diode
$V_{\text{HF-}}$	Disturbance voltage of negative supply terminal in EMC measurement

$V_{\text{HF}+}$	Disturbance voltage of positive supply terminal in EMC measurement
V_{in}	Input voltage
V_{out}	Output voltage
$V_{\text{ph,max}}$	Maximum phase voltage
Z_0	Characteristic impedance
Z_{th}	Thermal impedance
$Z_{\text{th,ja}}$	Thermal impedance from junction to ambient
d	Geometric distance
f_{sw}	Switching frequency
$\frac{di}{dt}$	Slope of changing current
j	Density of the electrical current
k	Boltzmann's constant
l	Geometric length
n	Speed of an electric machine
n^+	Electrons charge carrier concentration in a highly doped region
n_{max}	Maximum speed of an electric machine
n_{nom}	Nominal speed of an electric machine
p	Holes charge carrier concentration
p^+	Holes charge carrier concentration in a highly doped region
t	Time
$\frac{dv}{dt}$	Slope of changing voltage
w	Geometric width
w_{B}	Thickness of the drift region

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