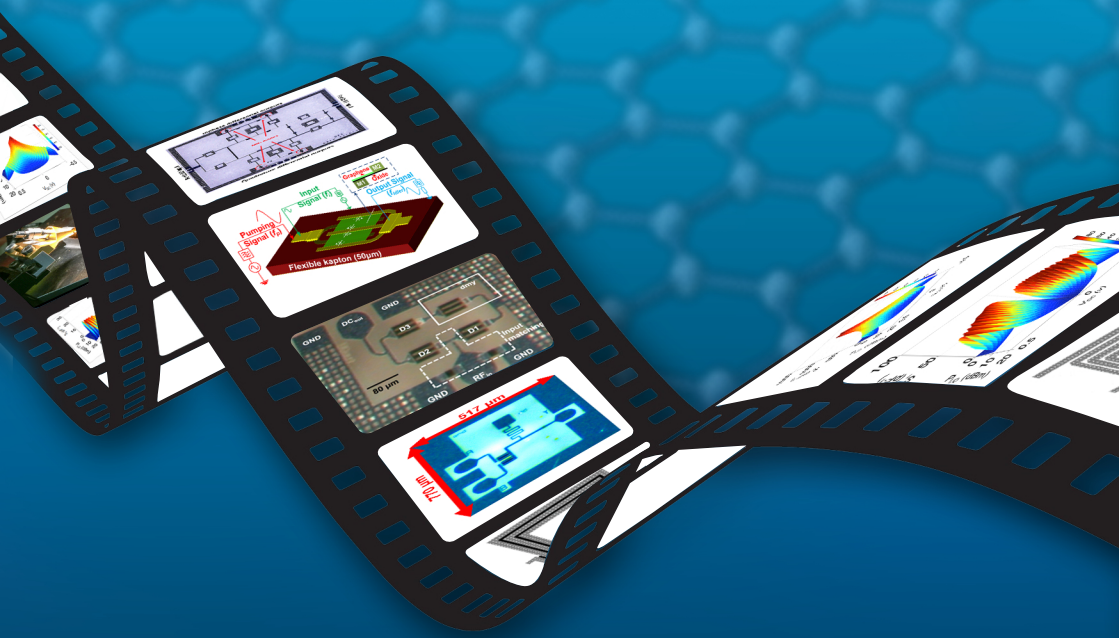
Mohamed Saeed Elsayed

Thin-film Technology for Graphene-based Electronic Devices and Circuits



Thin-film Technology for Graphene-based Electronic Devices and Circuits

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Thin-film Technology for Graphene-based Electronic Devices and Circuits

PhD Thesis

Mohamed Saeed Elsayed

Praise be to Allah, Lord of the Worlds ...

To the memory of my father and to my beloved mother ...

Acknowledgment

This dissertation is the outcome of five years of research. I want to thank all the companions I met in this journey for their support, guidance and fortitude. Definitely, I would like to express my sincere gratitude and gratefulness to Professor *Renato Negra* for allowing me to be a part of his team. Beside his support, motivation, guidance, and stimulation on both technical and personal levels. I want to thank my dear friend, classmate, and roommate *Ahmed Hamed* for his help and support. Without the excellent cooperation with you, this work would have not been possible. I want to thank *Dr. Daniel Neumaier*, *Dr. Zhenxing Wang*, and *Dr. Mehrdad Shaygan* from AMO GmbH for their help and support. Special thanks to my dear friend *Dr. Francisco Pasadas* for his support. Hearty thanks to all my colleagues in the chair of High Frequency Electronics. Special thanks go to *Erkan Bayram*, *Oner Hanay*, *Eduard Heidbricht*, *Saad Qayuum*, *Dr. Muh-Dey Dwei*, *Achim Noculak*, *Torsten Platzbecker*, *Diana Wallusch*, and *Filiz Yurdusever* for their support, and stimulation. Special thanks for *Erkan Bayram*, *Dr. Francisco*

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Preface

This dissertation summarizes my research in graphene-based technology, devices and circuits within the Graphene Flagship project funded by the European Commission.

The kick-off of the project was in October 2013 after only nine years from the rise of graphene in 2004 as a promising 2D material. In 2013, the status of graphene-based devices was beyond the expectations from the electrical features of graphene. The zero-bandgap nature of the intrinsic graphene leads to challenges in fabricating graphene field-effect transistors (GFET)s which can be employed in conventional circuits like other semiconductor devices. One of these challenges is the poor maximum frequency of oscillations (fmax) which is poor compared to the expected from the charge carrier mobilities. In addition, the poor on-off currents ratio imposes challenges to employ GFETs in Boolean logic gates and thus in digital circuits.

This work addresses these challenges by expressing the roadmap of the evolution of GFETs and the employment of these transistors in circuits and systems. Thenceforth, a novel graphene-based device which is the chemical vapor deposition (CVD) metal-insulator-graphene (MIG) diode is presented. The MIG diode is the core contribution of this work by leveraging an interesting feature of graphene which is the graphene quantum capacitance (GCQ). The novel device which uses a similar structure of the thin-film metal-insulator-metal (MIM) diodes but with a distinct charge transfer mechanism allows the implementation of thin-film technology that is employed in high frequency circuit applications. Physical operation of the diode is studied and compared to state-of-the-art MIM diodes showing superior performance in-terms of asymmetry and nonlinearity. Large- and small-signal models are extracted from the characterisation of the fabricated diodes to enable the use of these diodes in circuit applications. In addition, physical design considerations are carried out to ensure high frequency operation of these diodes. An in-house, thin-film monolithic microwave integrated circuit (MMIC) technology integrating MIG diodes together with high quality passives is presented and tested. Different integrated circuits employing the MIG diodes such as power detectors and mixers are implemented at micro- and millimetre-wave frequencies. In addition, thin-film Boolean logic gates are presented thanks to the excellent switching properties of MIG diodes. Another attainment of this work is leveraging MIG diodes in six-port topologies which offer a solution to build receivers at different frequen-cy bands of operation. In that regard, a lumped-element six-port junction is implemented on a glass substrate. Owing to the stable MMIC process together with the repeatability of the CVD MIG diodes successful receiver operation is demonstrated. Last but not least, the employment of the unique properties of the GCQ in parametric amplifier (PAMP) topology to realise canonical transmitter and receiver frontends with positive conversion gain is explored and discussed for the first time.

Aachen, January 14^{th}, 2019

Contents

Chapter 1

Introduction

The burgeoning development in the recent communications standards associated with the evolutionary research in new materials result in the arise of new applications. Particularly, two-dimensional (2D) materials have attracted great attention due to their flexibility, ability of integration alongside with different substrates which is convenient for applications such as Radio Frequency Identification (RFID), Near Field Communications (NFC), Internet of Things (IoT) that could be utilized in flexible electronics, and smart wearables for biomedical purposes and wireless communications.

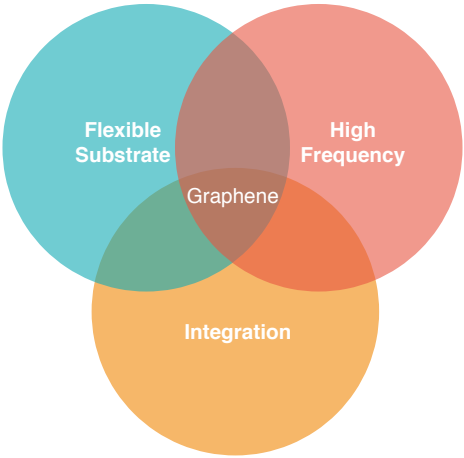


Figure 1.1: Graphene properties for applications in electronic circuits.

1.1 Motivation

Graphene is one promising candidate among the family of 2D materials due to its outstanding electrical and mechanical properties. The reported carrier electron mobility and saturation velocity [1], together with the ability for large-scale integration on different substrates make graphene a perfect candidate for Radio Frequency (RF), millimetre-wave, and submillimetre-wave circuit applications. Fig. 1.1 summarizes the advantages of graphene as an emerging technology that fulfill the requirements for high frequency applications, together with the mechanical flexibility due to its 2D nature. Last but not least, graphene is integrated apace with different substrates without changing the device operation characteristics.

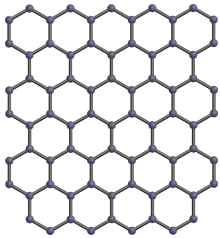


Figure 1.2: Hexagonal lattice structure of graphene [2].

1.2 Thesis contribution

This dissertation presents the novel CVD-based graphene-diode with its outstanding features. To exploit the properties of this diode a thin-film monolithic microwave integrated circuit (MMIC) is realised to integrate the diode alongside with high quality passives to implement high-frequency circuits and systems. The presented technology and circuits outperform state-of-the-art reported other graphene circuits based on graphene transistors and diodes.

1.3 Thesis structure

The structure of this dissertation is divided into seven chapters that are organized as follows:

The first part represents the motivation of this research on graphene and gives an overview on the evolution of graphene transistors and graphene transistors-based circuits, and systems. The structure of this part is represented in *chapter 1* and *chapter 2*. *Chapter 1* highlights the main advantages of graphene as a 2D material, compares the electrical properties of graphene with the existing competitive semiconductors. Then the main methods of preparing graphene are presented and compared. *Chapter 2* represents a literature survey on the basic development of graphene-based transistors and the circuits employing graphene transistors in literature. This part shows the

promising features of graphene as well as the challenges of graphene-based transistors to achieve the expected performance from the superior electrical properties.

Thenceforth, the core contribution of this work: the electronic device which forms the basis of this thesis, the CVD Metal Insulator Graphene, MIG, diode with its features that are employed to realise the presented circuits and systems is illustrated. *Chapter 3* depicts the evolution of the MIG diode starting with a literature survey on the graphene-based diodes. Thereafter, the MIG diode charge transfer mechanism, operation, and physical implementation considerations are discussed. At the end of this chapter, the small-signal model of the developed MIG diode is presented. In *chapter 4*, the in-house developed thin-film Monolithic Microwave Integrated Circuit (MMIC) technology is illustrated. Then, the employment of MIG diodes in different circuit applications are presented and explained. Moving forward to the realised applications of the MIG diodes in high frequency circuits, leveraging graphene properties to demonstrate high frequency circuits together with boolean logic gates is presented. Then, the employment of the MIG diodes in a six-port receiver topology is discussed. The six-port approach has been introduced as a scalable topology which is not limited by the GFET challenges as will be discussed later. In *chapter 6* the Parametric Amplifier (PAMP) concept is discussed for the first time exploiting the promising characteristics of the Quantum capacitance (C_Q) of graphene to the best knowledge of the author. Exploiting the properties of C_Q in parametric downconversion scheme result in a distinct topology which allows the realisation of canonical receiver front ends with positive conversion gain and optimised noise performance.

The last part of this dissertation where a cumulative summary followed by succinct conclusion are presented in *chapter 7*. Thenceforth, the possible future research that could be pursued based on this work is presented.

1.4 Graphene properties

The graphene lattice consists of regular hexagons with a carbon atom at each corner with a bond length of 1.42 Å. A closer look at graphene's crystal lattice is provided in Fig. 1.2.

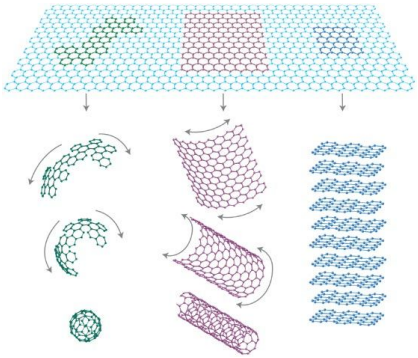


Figure 1.3: Schematic of the graphene's lattice structure illustrating that it is the 2D building material for carbon materials of all other dimensionalities. It can be wrapped up into 0D buckyballs, rolled into 1D nanotubes or stacked into 3D graphite [5].

Each carbon atom has a total of 6 electrons; two in the inner shell and four in the outer shell (valence electrons). Three of the four valence electrons participate in the bonds to their next neighbors on the two dimensional plane making what is called sigma-bond (σ-bond) and leaving one electron freely available in the third dimension for electronic bonding. The fourth π-electron orbital is perpendicularly-oriented upwards and downwards from the sheet layer and delocalized. The π-orbitals overlap and help to enhance the carbon-to-carbon bonds in graphene. The bonding and antibonding of these π-orbitals affect the electronic properties of graphene [3, 4].

Graphene is considered the basic building block for graphitic materials of all dimensions. In other words, graphene layers stack on top of one another form three-dimensional, 3D, graphite. It can be wrapped up into zero-dimensional, 0D, buckyballs, or even rolled into one-dimension, 1D, Carbon Nanotubes (CNT) as shown in Fig. 1.3.

Graphene is a gapless material. Unlike semiconductors, whose band structure has a parabolic shape with an Energy gap (E_G). For example, the energy gap (E_G) for Silicon (Si) is 1.12 eV, and for Germanium (Ge) is 0.67 eV. The band structure of graphene is cone-shaped with the valence and conduction

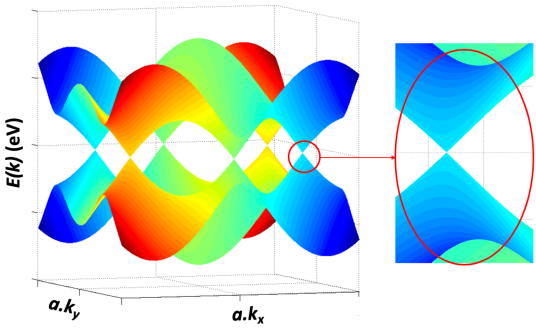


Figure 1.4: Band structure of graphene illustrating the Fermi surface and the zero-gap nature of graphene.

bands touching each other at the K point of the Brillouin zone resulting in a semimetal with no band gap, $E_G = 0\,\text{eV}$.

The band structure of graphene exhibits a linear dispersion relation for charge carriers that can be expressed by (1.1) [6]:

$$E(k) = \pm\gamma\sqrt{1 + 4\cos(\frac{\sqrt{3}a}{2}k_x)\cos(\frac{a}{2}k_y) + 4\cos^2(\frac{a}{2}k_y)}, \tag{1.1}$$

where $\gamma = 2.8\,\text{eV}$ is the nearest neighbor overlap energy, and the constant $a = 2.46\,\text{Å}$. The band structure of graphene is shown in Fig. 1.4, which has been computed using (1.1). The Fermi surface for a lattice material is the energy border between the valence and conduction bands in the momentum space. For this border to be defined, the Fermi energy must fall inside an energy band and not in a band gap, otherwise the valence and conduction bands do not touch at all. Thus, Fermi surfaces only exist for conductors. The Fermi surface of graphene consists of six double-cones with the Fermi energy at the intersection of those.

Table 1.1 shows a comparison of the electrical properties between intrinsic graphene [7], Si, Gallium Nitride (GaN), and Gallium Arsenide (GaAs)

Table 1.1: Comparison between intrinsic graphene and other semiconductors in terms of m^*/m_0, μ_e, μ_h, v_{peak}, and E_G.

	Si	GaN	GaAs	Graphene [7]
m^*/m_0	0.98	0.19	0.063	~ 0
μ_e ($\mathrm{cm}^2/(\mathrm{V\,s})$)	1400	1600	8000	200000
μ_h ($\mathrm{cm}^2/(\mathrm{V\,s})$)	500	200	400	200000
v_{peak} (x10^7cm/s)	1	2.4	1.8	10
E_G (eV)	1.12	3.4	1.43	0

at room temperature. In terms of effective mass (m^*/m_0), electron and hole mobilities, *i.e.* μ_e and μ_h, respectively, peak velocity (v_{peak}), and E_G. The comparison shows clearly, the promising electrical features of graphene compared to other competitive semiconductor materials that are used widely to realise high frequency transistors.

1.5 Graphene preparation methods

There are many methods for preparing graphene as shown in Fig. 1.5. The commonly used methods in graphene-based devices are mechanical exfoliation, thermal decomposition (on SiC substrate), CVD, ...etc.

In this dissertation, only three methods are discussed since most of the published graphene-based electronic devices are based on these three schemes.

1.5.1 Mechanical exfoliation

In mechanical exfoliation, graphene is detached from an already existing graphite crystal. This method is also known as scotch-tape method. Since an adhesive tape has to be used in order to peel single layer graphene (SLG) off the graphite crystal. Repeated peeling has to take place in order to thin down the obtained graphene layers into flakes of few-layer graphene and from there eventually into SLG. Afterwards the tape is attached to the substrate and

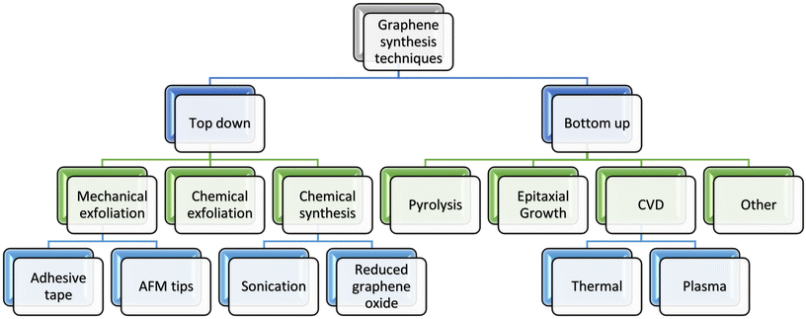


Figure 1.5: A process flow chart of graphene synthesis [8].

then, in order to detach the tape, acetone is used to solve the glue. Finally, one last peeling with an unused tape is performed [1].
It is important to mention that there are other methods to obtain graphene by mechanical exfoliation different from the scotch tape method [9].

1.5.2 Growth on surface

1.5.2.1 Epitaxial growth on SiC

One approach to prepare graphene is thermal decomposition of SiC. Bulk SiC is heated to around 1500 °C in the presence of Argon (Ar) in atmosphere, then, some of the silicon sublimates, leaving a layer of carbon on the surface that rebonds to form a layer of graphene adhered to the surface of SiC.

The exposed SiC face affects both the growth rate the resulting graphene. Growth is much faster on the C face, typically leading to multilayer graphene [9].

Table 1.2: Comparison between graphene preparation methods [9].

	Mechanical exfoliation	Thermal growth on SiC	CVD
Graphene quality	high	moderate	moderate-high[1]
Size of flakes	limited	unlimited	unlimited
Complexity	low	high	high
Repeatability	low	high	high
Cost	low	high	relatively low

[1] Highly dependent on the maturity of the technology.

1.5.2.2 CVD

In CVD, single crystalline transition metals are used as a substrate for growing graphene layers, given the condition of low pressure and high temperature (around 1000 °C). Transition metals should have limited solubility of Carbon such as Copper (Cu), Nickel (Ni), Platinum (Pt). The most widely used metals for such process are Cu and Ni. The metal substrate is exposed to furnace annealing in order to increase its domain size. Then a precursor, *i.e.* a mixture of Methane (CH_4) and Hydrogen (H_2) gases, are flowed through the furnace resulting in carbon atoms from the methane to adhere onto the surface of the metal through chemical adsorption. Thereafter, upon cooling carbon atoms crystallize and solidify into graphene layer on the surface of the metal [10–12].

The summary of the methods discussed in this section is shown in Table 1.2. The exfoliation method produces the highest quality graphene, however, it lacks the repeatability which is crucial for device modeling. In addition, this method is not suitable for mass production and large-scale integration. On the other hand, in the Epitaxial growth on SiC, the quality is moderate and the process is well controlled. The main deficit of this method is the cost of the expensive SiC substrate and the high temperature required. Last but not least, the CVD method could be used to produce repeatable graphene flakes with high quality and lower cost than the Epitaxial growth on SiC [9, 12–14].

Chapter 2

Graphene Field-Effect-Transistors: Device development and circuit applications

In this chapter an insight from an engineering point of view on the major development milestones and published research on graphene-based transistors is given. Later, an overview on the reported circuits and systems based on these graphene devices is presented. Graphene-based transistors are classified according to the used graphene preparation method described in *section 1.5*.

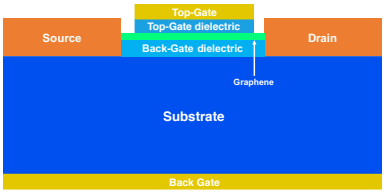


Figure 2.1: Generic GFET structure with top and back gate.

2.1 Graphene field-effect-transistor development

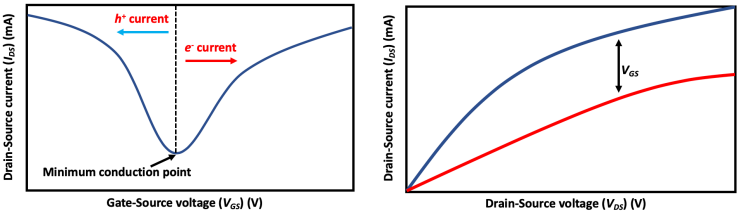
The basic structure of the graphene field effect transistor (GFET) is shown in Fig. 2.1 illustrating the top gate (TG) and back gate (BG) schemes.

Due to the gapless band structure of graphene, the generic direct current (DC) transfer characteristics represented by the drain-source current (I_{DS}) versus the gate-source voltage (V_{GS}) of the GFET is presented in Fig. 2.2a and the generic DC output characteristics represented by the I_{DS} versus the Drain-Source Voltage (V_{DS}) of the GFET is presented in Fig. 2.2b. Two important properties of GFET's are:

- No current saturation: which results in poor DC voltage gain (A_V). In addition, the poor current saturation leads to large drain-source conductance (g_{DS}). Therefore, it is expected that the maximum frequency of oscillation (f_{max}) is rather low.

- No off-state: I_{DS} shows an ambipolarity behaviour with gate-source voltage (V_{GS}), resulting in a poor on-off current ratio of GFETs. Therefore, the usage of GFET to implement switching circuits including boolean logic gates is challenging.

According to *section 1.5* graphene is prepared either by mechanical exfoliation, or expitaxial growth on SiC substrate, or CVD methods. A comparison between the alternate current (AC) behaviour presented by the cutoff frequency (f_T) versus the gate length of GFET's and other semiconductors is presented in Fig. 2.3a [15]. As expected from Table 1.2, the reported f_T of the exfoliated graphene is higher than the epitaxial growth on SiC. For

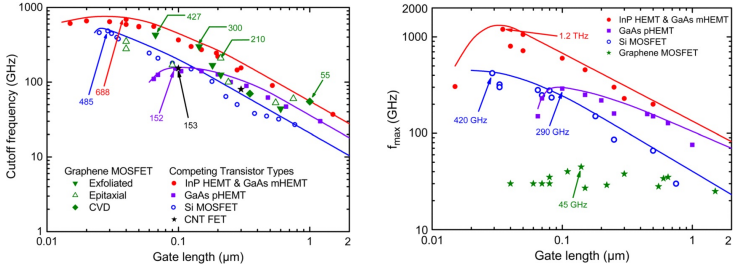


(a) GFET DC transfer characteristics. (b) GFET DC output characteristics.

Figure 2.2: Generic GFET DC characteristics.

the CVD-based devices, the quality of graphene is highly dependent on the maturity of the technology used [12].

The same comparison analogy is conducted for f_{max} in Fig. 2.3b. Except that, in contrast to the competitive f_T performance, GFETs behave poorly in terms of f_{max}.
The reason for this poor f_{max} performance is, as mentioned before, the large g_{DS} caused by the weak saturation of I_{DS} in the output characteristics of GFETs.



(a) f_T of GFETs compared to other semiconductors versus gate length.

(b) f_{max} of GFETs compared to other semiconductors versus gate length.

Figure 2.3: GFET frequency behaviour with scaling [15, 16].

2.1.1 Mechanically exfoliated graphene-based GFETs

The first TG monolayer GFET was demonstrated in 2007 [17]. Where exfoliated graphene is deposited onto SiO_2 on High Resistivity Silicon (HRS) with SiO_2 as TG dielectric and 150 nm gate length. A scanning electron microscope (SEM) image of the GFET is shown in Fig. 2.4.

The effect of the TG on the device's carrier transport was monitored at an effective electric field (E_{eff}) of 0.4 mV/cm. A reduction in the carrier mobility compared to the expected was observed. The hole mobility (μ_h) is reduced from 4790 $cm^2/(V\,s)$ in case of uncovered graphene to 710 $cm^2/(V\,s)$ in case of a TG graphene. As for the electron mobility (μ_e), it dropped from 4780 $cm^2/(V\,s)$ to 530 $cm^2/(V\,s)$. However, these values prove to be promising in comparison with the universal mobilities of Silicon at the same field strength.

GFETs showing f_T in the gigahertz range have been realised. A record f_T of 14.7 GHz for a 500 nm gate length device was demonstrated in [18], where mechanically exfoliated graphene on HRS with 300 nm SiO_2 thermally-grown layer as substrate and atomically deposited HFO_2 as gate dielectric have been used.
Later in [19], which was the first TG GFET to report an f_T of 26 GHz. However, after the deposition of TG dielectrics by atomic layer deposition (ALD), there was significant reduction in both the device conductance and mobility.

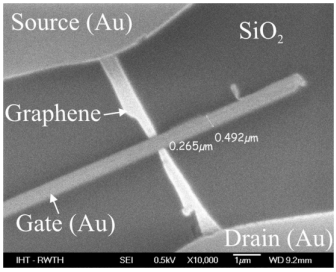
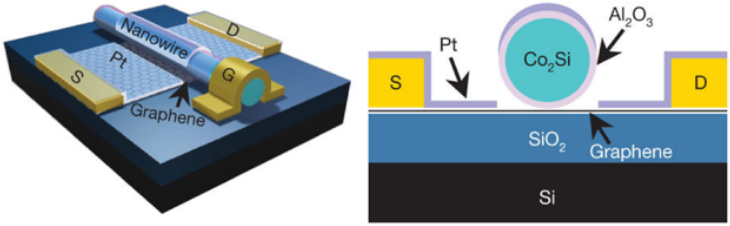


Figure 2.4: SEM of the first TG GFET [17].



(a) 3D plot of NW GFET. (b) Cross-section of the NW GFET.

Figure 2.5: Schematic of the 300 GHz GFET with a Co_2Si/Al_2O_3 core/shell NW as the self-aligned TG [22].

In order to overcome the mobility degradation, it was suggested a year later in 2009 [20] to use polymer buffer between the graphene and the conventional dielectric (high-k HFO_2) in a device with a gate length of 1.1 µm. Despite the fact that the mobility degradation was eliminated, the reported f_T was only 9 GHz.

A dual-gate GFET with an f_T of 50 GHz for a gate length of 350 nm was reported in [21]. This improved performance was achieved due to the dual gate structure that resulted in reducing the access resistance using electrostatic doping through the BG.

In 2010, an intrinsic record high f_T of 300 GHz was reported at 140 nm gate length using nanowire (NW) gate for self-alignment [22]. This reported f_T outperforms the best silicon Metal-Oxide-Semiconductor FET (MOSFET) of comparable sizes, in addition of being comparable to those of the best Indium Phosphate (InP) High Electron Mobility Transistor (HEMT) and GaAs HEMT with similar channel lengths. However, the high f_T recorded is intrinsic; meaning that the contact pad parasitics have been de-embedded.

A significant difference was observed between the intrinsic and extrinsic values of f_T, this is due to the large ratio between the parasitic pad gate capacitances. The measured extrinsic f_T was 2.4 GHz.

In this approach a Co_2Si/Al_2O_3 core/shell NW has been utilized as the self-aligned top-gate onto HRS substrate with 300 nm thermally-grown SiO_2 as illustrated in Fig. 2.5. ALD of Al_2O_3 shell on the Co_2Si NWs with controlled thickness have been used such that the Al_2O_3 shell functions as dielectric whereas the metallic core represents the metal gate. This study introduced a unique approach for self-alignment along with allowing integration of the TG electrodes without introducing damage into the pristine graphene lattices. To prove that this results were owing to the self-alignment technique, Fig. 2.6 shows that the Mutual Transconductance (g_m) was 0.02 mS/µm before and then jumped to 1.27 mS/µm for a V_{DS} of -1 V after depositing the source/drain aligned electrodes.

Despite the high performance exhibited in [22], the scalability of physical assembling NW gates is complicated since unconventional NW-assembly processes are required. Instead of struggling with the challenges of NW assembly, a more scalable approach was suggested in [23] in 2012 based on transferring lithographically patterned gate stacks (Al_2O_3/Ti/Au) onto graphene as the self-aligned top gate. The highest f_T of 427 GHz for a 67 nm gate length on HRS/SiO_2 substrate has been demonstrated.

Fig. 2.7 gives a useful insight into this approach and the fabrication of self-aligned GFETs with transferred gate stacks.

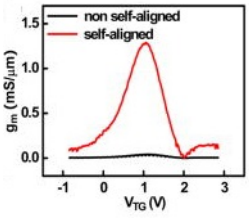


Figure 2.6: Transconductance versus V_{GS} of a TG GFET highlighting the effect of self-alignment [22].

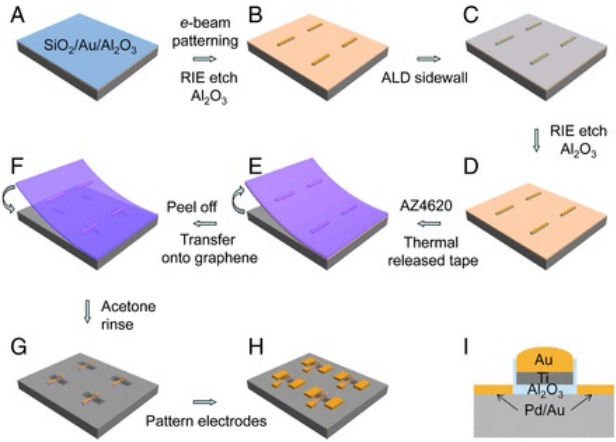


Figure 2.7: Fabrication steps of self−aligned graphene transistors with transferred gate stacks [23].

2.1.2 Epitaxial growth on SiC graphene-based GFETs

The first ever recorded f_T in the gigahertz regime for epitaxial growth on SiC was in 2009. An extrinsic f_T of 4.4 GHz was reported with a corresponding f_{max} of 11.5 GHz using Al_2O_3 as gate dielectric deposited via ALD [24].

According to [25], the highest attained f_T for thermally decomposition on SiC GFETs was 100 GHz for a gate length of 240 nm outperforming that of state-of-the-art Si MOSFETs of the same gate length. A 10 nm thick HFO_2 is deposited by ALD on top of a epitaxial growth on SiC graphene on the Si face of SiC substrate. The reported f_{max} was 14 GHz and 10 GHz for gate lengths of 550 nm and 240 nm, respectively.

In [26], the maximum and most promising intrinsic f_{max} of 70 GHz has been reported for a GFET based on graphene thermally decomposition grown on the C-face. This GFET was built using T-gates to ensure self-aligned contacts. The gate length was 100 nm and the gate dielectric was Al_2O_3. An intrinsic f_T of 110 GHz was reported for these devices. Owing to the T-gate

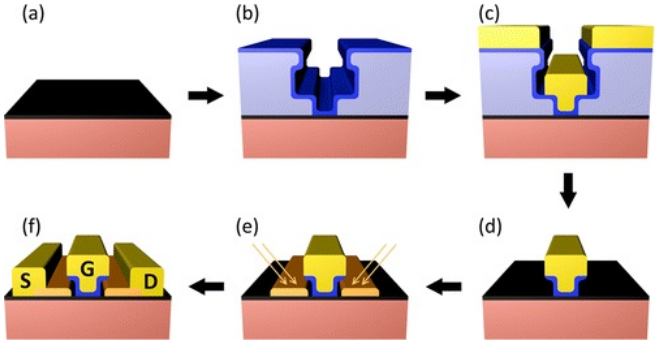


Figure 2.8: Process flow for self-aligned T-gate GFET fabrication (a) Monolayer graphene on C-face of SiC. (b) T-gate patterning, followed by ALD of Al_2O_3. (c) Ti/Au is deposited on top as the gate metal. (d) Lift-off. (e) Angle deposition of Pd/Au to form self-aligned contacts. (f) Ti/Au source and drain contacts are deposited [26].

geometry, the gate resistance is reduced by an order of magnitude compared to a device without it, and over two orders of magnitude compared to using highly doped NW gates. The small Contact Resistance (R_C) of the Pd/Au layers, and the C-face epitaxial growth on SiC graphene was the reason behind this record high f_{max}. The extrinsic f_T and f_{max} were 41 GHz and 38 GHz, respectively. This extrinsic f_T was considered to outperform all other reported GFETs of the same gate length at that time. A schematic illustration for the T-gate fabrication is shown in Fig. 2.8. The same measurements and characterisation were carried out for 240 nm gate length and the reported extrinsic and intrinsic f_T was 33 GHz and 60 GHz, respectively.

2.1.3 CVD grown graphene-based GFETs

In 2011 [27], an intrinsic f_T of 155 GHz was reported for a TG CVD-GFET with a gate length down to 40 nm which was the shortest gate length ever demonstrated on GFET at that time. The CVD graphene was grown on copper film and transferred to a wafer of Diamond-Like Carbon (DLC). A 15 nm Al_2O_3 dielectric is deposited by ALD. Lack of clear saturation is

observed in the DC characteristics as expected. However, a high f_{max} of 20 GHz for a gate length of 550 nm and 13 GHz for 140 nm.
Despite the overall high performance attained, g_m suffers from the short-channel effect at these gate dimensions. Nevertheless, this study confirms the high prospects for graphene transistors to be scaled even further to much smaller device sizes.

Only one year later, *i.e.* in 2012, [28] significant improvement for both values of f_T and f_{max} were achieved in [27].An f_T of 300 GHz for a 40 nm long device instead of 155 GHz in [27]. Equally, an f_{max} of 44 GHz for 140 nm which is twice the 20 GHz previously achieved. The improvement of bringing f_T up to 300 GHz for the same 40 nm long device as well as increasing f_{max} from 20 GHz to 44 GHz was mainly due to higher graphene material quality. Especially, controlling the doping of the gate dielectric is a major factor for boosting the performance of the device.

According to [23] an f_T of 212 GHz for a 46 nm channel length, using a transferred gate stacks approach on a quartz (glass) substrate. This outperforms previously reported CVD GFET performance of comparable channel length, as example the 155 GHz for a 40 nm on a DLC mentioned earlier. As for f_{max}, 29 GHz was obtained with a 220 nm channel length while a device scaled down to 46 nm provided a value of 8 GHz. f_{max} does not scale with the channel length since it also depends on the g_{DS} and the gate resistance.

It is important to mention here that the dramatic difference between intrinsic and extrinsic extraction is due the large ratio between the parasitic pad and gate capacitances as mention before. This ratio is reduced upon the use of an insulating glass substrate.

A study conducted in 2016 [29] proposed the deposition of an Au layer on graphene before device fabrication to ensure protection against unwanted contamination and defect formation in graphene during fabrication. The reported good performance in terms of intrinsic carrier mobility of $8900\,\mathrm{cm}^2/(\mathrm{V\,s})$ associated with a low series resistance of $1520\,\Omega/\mu\mathrm{m}$ were the key to obtain this performance. Furthermore, the gold layer implied a self-aligned process, in which the gate was automatically defined using the same resist pattern as that used for defining the S/D electrodes. Thus, they tackled two of the challenging issues in GFETs by reducing the access length along with lower contamination and fewer defect graphene. The fabricated device used

CVD-grown graphene on SiO_2/Si substrate with AlO_2 as gate dielectric.

In 2016 [30], an f_{max} of 200 GHz and 106 GHz extrinsic and intrinsic, respectively, for a GFET with 60 nm gate length were achieved associated with an f_T of 255 GHz and 70 GHz extrinsic and intrinsic, respectively. The most commonly used transfer method for graphene is Poly Methyl Methacrylate (PMMA) where polymers are used as sacrificial supporting substrate. In this study, an Au film is used instead of polymers to prevent graphene from organic contamination during the fabrication process. At the same time, the Au film is used to form the ohmic contact with the graphene transistors. The T-gate structure is used both for self-alignment and to reduce the gate resistance. Moreover, the insulating layer of Al_2O_3 dielectric layer was deposited by ALD.

In the study reported in [32], the usage of thin AlO_x gate-oxide in TG configuration enabled achieving a voltage gain, A_V, of more than 30 dB while the trade-off between A_V and frequency characteristics of the GFET has been shown.

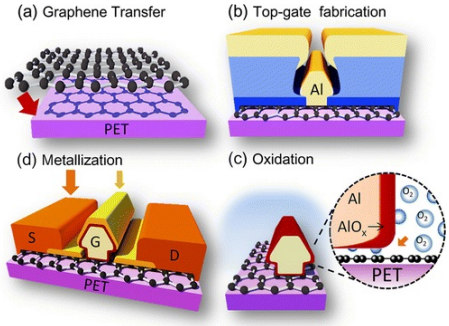


Figure 2.9: Schematic illustration of RF GFET fabrication processes on flexible substrate: (a) transfer of CVD graphene, (b) lithographic definition of aluminum T-gate (c) formation of natural aluminum oxide layer, (d) metalization of self-aligned source/drain contacts [31].

2.1.4 GFETs on Flexible Substrates

The flexibility and robustness of graphene introduces high prospects in using it along side with flexible substrates for flexible electronics and smart wearables applications.

In that regard, a 220 nm gate length with an AlO_x T-gate structure on flexible Polyethylene terephthalate (PET) was demonstrated in [31]. These process steps resulted in a remarkable extrinsic f_T of 32 GHz and f_{max} of 20 GHz. Even when subjected to a strain of 2.5% ,f_T and f_{max} showed 22 GHz and 13 GHz, respectively.

In 2016 [33], a record f_T for GFETs was reported on flexible substrate, where a robust GFET on Kapton substrate exhibited an extrinsic f_T of up to 39 GHz and an f_{max} of 13.5 GHz for 100 nm gate length. The devices showed stable performance and mechanical robustness upon bending, applying fatigue stress, and upon heating. The structure of the device is double bottom-gate and naturally grown Al_2O_3 and is illustrated in Fig. 2.9.

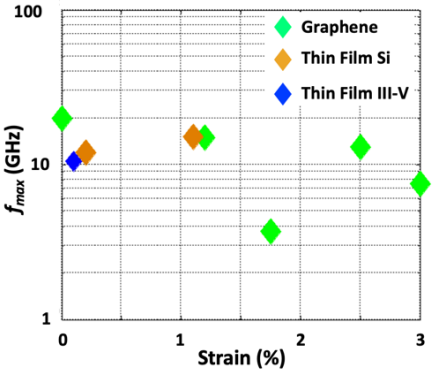


Figure 2.10: Comparison of f_{max} between published GFETs and other thin-film semiconductor transistors as function of the applied strain [31].

Fig. 2.10 [31] shows the potential of graphene [31, 34] for flexible electronics compared to other reported thin-film based transistors on both Si [35, 36] and Indium Arsenide (InAs) as a representative of III-V semiconductors [37].

Table 2.1 shows the comparison between the presented GFETs in this section.

It can be deduced that the development of GFETs based on the graphene preparation methods stated in *section 1.5* on both rigid and flexible substrates could be concluded as follow:

- DC characteristics of GFETs has a poor I_{DS} current saturation, which translates to large g_{DS} and therefore, low A_V and f_{max}. In addition, the inability to turn off the transistor completely represents a challenge in using GFETs specially in boolean logic gates.

- Techniques as self-alignment, T-gate, and the use of Au contacts improved the frequency characteristics of GFETs considerably.

- Using glass and maybe also other high-resistivity substrates reduces the discrepancy between extrinsic and intrinsic extraction of f_T and f_{max}.

- Scaling down the gate length improves f_T. On the other hand, due to short-channel effects, g_{DS} becomes larger and, therefore, f_{max} is reduced.

- Using Au deposition on graphene protects it against contaminations and defects that affect performance and reliability.

- Due to the 2D nature of graphene, it has been shown that GFETs could achieve f_T and f_{max} in the gigahertz range even under strain conditions.

- Further improvements in the gate resistance together with improving current saturation will lead to GFETs with outstanding frequency characteristics expected from the electrical properties of graphene mentioned in *section 1.4*.

Table 2.1: Summary of development of GFETs.

Ref.	Year	Gate length (nm)	Preparation method	f_T (GHz)	f_{max} (GHz)	Intrinsic/Extrinsic	Substrate	Gate Dielectric
[18]	2008	500	Exfoliation	14.7	–	Intrinsic	Si/SiO_2	HFO_2
[19]	2008	150	Exfoliation	26	–	Intrinsic	Si/SiO_2	HFO_2
[20]	2009	1100	Exfoliation	9	–	Intrinsic	Si/SiO_2	HFO_2
[21]	2009	350	Exfoliation	50	–	Intrinsic	Si/SiO_2	Al_2O_3
[24]	2009	2000	epitaxial growth on SiC	4.4	–	Intrinsic	SiC	Al_2O_3
[25]	2010	240	epitaxial growth on SiC	100	–	Intrinsic	SiC	HFO_2
[22]	2010	140	Exfoliation	300	–	Intrinsic	Si/SiO_2	Al_2O_3
[22]	2010	140	Exfoliation	2.4	–	Extrinsic	Si/SiO_2	Al_2O_3
[38]	2011	60	CVD	50	–	Extrinsic	Quartz	Al_2O_3
[27]	2011	40	CVD	155	–	Intrinsic	DLC	Al_2O_3
[28]	2012	40	CVD	300	–	Intrinsic	Si/SiO_2	Al_2O_3
[28]	2012	140	CVD	–	44	Intrinsic	Si/SiO_2	Al_2O_3
[23]	2012	46	CVD	212	8	Intrinsic	Quartz	Al_2O_3
[23]	2012	67	Exfoliation	427	–	Intrinsic	Si/SiO_2	Al_2O_3
[26]	2013	100	epitaxial growth on SiC	110	70	Intrinsic	SiC	Al_2O_3
[26]	2013	100	epitaxial growth on SiC	41	38	Extrinsic	SiC	Al_2O_3
[30]	2016	60	CVD	255	200	Intrinsic	Si/SiO_2	Al_2O_3
[30]	2016	60	CVD	70	106	Extrinsic	Si/SiO_2	Al_2O_3
[31]	2014	200	CVD	32	20	Extrinsic	PET (Flexible)	HFO_2
[33]	2016	100	CVD	39	13.5	Extrinsic	Kapton(Flexible)	Al_2O_3

2.2 GFET-based circuits and systems

Many graphene circuits have been reported covering the frequency range from DC to 200 GHz and employing GFETs. This includes frequency mixers, frequency multipliers, power detectors, amplifiers, and oscillators. On the other hand, due to the poor gain provided by GFETs, only few receiver and transmitter systems have been reported. The limited f_T and f_{max} of GFETs limit the frequency of operation in GFET-based amplifiers. While in the reported frequency conversion circuits the nonlinearities of GFETs have been utilized beyond their f_T and f_{max}. Another issue which affects the employment of GFETs in complex circuits and systems is the low reproducibility of matched devices specially for GFETs with mechanically exfoliated graphene. Accordingly, the presented circuits and systems employ only few number of active devices.

2.2.1 GFET-based Amplifiers

As discussed in *section 2.1*, the performance of GFETs in terms of A_V and f_{max} is limited due to the gapless band structure of graphene. However, graphene-based amplifiers were reported based on Common Source (CS) configurations of GFETs [39–44]. A distributed amplifier scheme has been reported in [45] with four stages of GFETs, each of them in a CS configuration. The circuit has been implemented on a Printed Circuit Board (PCB) by wirebonding the GFETs.

Fig. 2.11 shows the distributed scheme in [45], where four GFETs, each with 400 nm in buried-gate structure were fabricated. Simulations with measured GFETs S-parameters showed promising performance in terms of gain and bandwidth. However, the prototype PCB measurement results did not matched the expectations from the simulations because of the large mismatches between the fabricated GFETs, the limitations on the availability of the required values of the lumped discrete components, and the tolerances in the values of these discrete lumped components. These reasons suggest that an integrated prototype of the distributed amplifier would give better results.

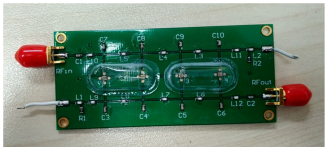
Table 2.2: Performance comparison of GFET-based amplifiers.

Ref.	Technology	Configuration	Gain (dB)	P_{out} (dBm)	Freq. (GHz)
[40]	CVD/Si	CS/Single GFET	5	−12	6
[41]	Exfoliated/Si	CS/Single GFET	10	–	1
[42]	Exfoliated/SiO_2	CS/Single GFET	1.3	–	0.38
[45][1]	CVD/Si	Dist. CS GFETs	5	–	1.5
[45][2]	CVD/Si	Dist. CS GFETs	−20	–	1.5
[43]	Epitaxial/SiC	CS/Single GFET	3.4	–	14.3
[44]	Epitaxial/SiC	CS/Single GFET	8.9	5.1	2.5

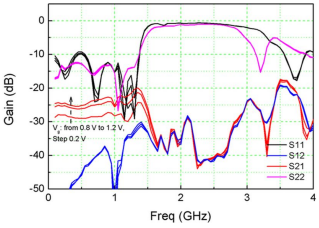
[1] Simulation results.
[2] Measurement results.

Table 2.2 compares the performance of the reported graphene-based amplifiers in terms of gain, Output Power (P_{out}), and frequency.

It could be concluded that due to the low intrinsic A_V and f_{max}, the reported GFET-based amplifiers are not able to deliver high gain and high frequency operation. In addition, the immaturity of the device fabrication limits the use of multiple devices to provide higher gain.



(a) Photograph of the PCB implementation.



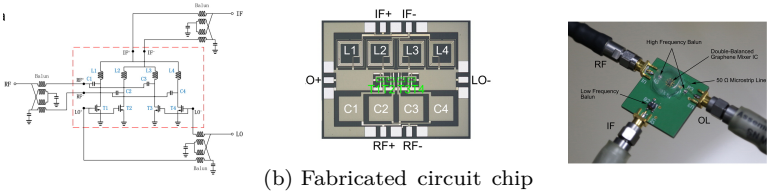
(b) Measured S-parameters for the fabricated amplifier.

Figure 2.11: Four-stages distributed GFET amplifier [45].

2.2.2 GFET-based Mixers

The currently reported GFET mixers are realised as FET-resistive mixers which exploited the GFET nonlinear resistance rather than its transconductance. Additionally, the lack of current saturation in GFETs result in a high linearity of GFET-based resistive mixers. This enables the demonstration of mixers operating at frequencies above f_T and f_{max} of the used GFETs. However, the reported Conversion Loss (CL) of the GFET-based mixers is relatively high compared to other technologies. This is caused by the dependence of the conversion efficiency of the FET-resistive mixers on the Drain-Source resistance (R_{DS}) which ideally changes from zero in the on-state to infinite in the off-state. In case of the GFET and because of its ambipolar behaviour as mentioned in *section 2.1*, the on-off resistance-ratio is always low with high on-resistance and low off-resistance. As a consequence, the reported CL values vary from 45 dB [46] to 18 dB [47] for a local oscillator power Local Oscillator (LO) Power (P_{LO}) of 8 dBm which is the minimum reported CL so far for integrated GFET-based mixers. GFET-resistive mixers are implemented as either fundamental or subharmonic mixers employing mostly, a single-transistor due to yield and repeatability issues. This GFET is either connected to high quality external passive components [46, 48–51] or integrated with passive lumped components or microwave filters [47, 52–54].

In [55] four GFETs have been employed in a double-balanced mixer topology as shown in Fig. 2.12, in addition to a single GFET-mixer to compare the performance improvement by using the double balanced scheme.



(a) Mixer schematic.

(b) Fabricated circuit chip micrograph.

(c) Fabricated PCB.

Figure 2.12: GFET-based double-balanced mixer [55].

Table 2.3: Performance comparison of GFET-based mixers.

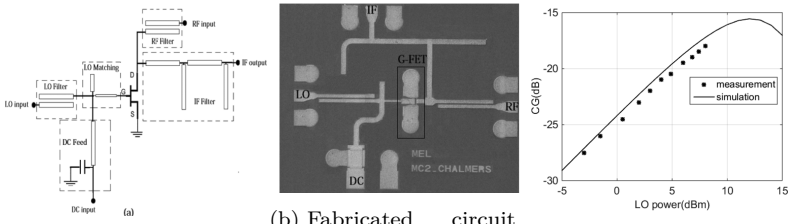
Ref.	Substrate	RF Frequency (f_{RF}) (GHz)	CL (dB)	P_{LO} (dBm)
[48]	Si/SiO_2	0.01	35	0
[52]	SiC	4	27	20
[49]	Si/SiO_2	2-5	20-22	0
[50]	Si/SiO_2	2	24	15
[53]	Si	24-31	19	10
[51]	SiC	$4-20$	14-21	6
[55]	Si	3-5	33-37	8.9
[54]	Si	185-215	28-31	11.5-12.5
[46]	Si	4	45	15
[47]	SiC	88-100	18	8

Table 2.3 compares the key performance parameters of the reported GFET-based mixers sorted according to the publication date. The reported mixer in [47] has been employed as an upconverter modulator for an 8 Gbit/s Orthogonal Frequency Division Multiplexing (OFDM) signal. This shows a promising potential of graphene mixers for high data-rate communications. Fig. 2.13 shows the schematic, the chip micrograph, and compares the simulated and measured CL.

As a conclusion, the GFETs have been employed as resistive mixers exploiting their R_{DS} even at frequencies beyond their f_T and f_{max} providing high conversion loss instead of employing them in active mixer topologies to provide positive conversion gain due to the device limitations.

2.2.3 GFET-based Oscillators

The reported oscillators using graphene devices are so far mainly ring oscillators and they employ GFET complementary inverters. A ring oscillator is constructed by exploiting the delay of an odd number of matched cascaded inverter stages arranged in a loop. However, the maximum reported oscillation frequency so far is 1.28 GHz despite the fact that the maximum



(a) Mixer schematic.

(b) Fabricated circuit chip micrograph.

(c) Fabricated PCB.

Figure 2.13: GFET-based W-band upconversion mixer [47].

Table 2.4: Performance comparison of GFET-based ring oscillators.

Ref.	Substrate	f_0 (GHz) (dB)	P_{LO} (dBm)
[56]	Si/SiO_2	0.035	-20
[57]	Si/SiO_2	1.28	-10
[58]	Si/SiO_2	4.3	-65

reported intrinsic f_T and f_{max} of the stand-alone GFET are above 100 GHz. This limitation is mainly due to the high on-resistance of the GFET which results in a slow charging and discharging of the gate capacitance of one inverter stage by the GFET of the previous stage for relatively low microwave frequencies. Accordingly, the resulting large delay of the individual inverter stages limits the oscillation frequency of such ring oscillators.

For the realisation of higher frequency oscillators significant scaling of the GFET gate-length as well as further reduction of its on-resistance are essential requirements. Moreover, GFETs have the problem of not being able to toggle between rail-to-rail. Therefore, it is difficult to match the input voltage of the next stage by design.

Table 2.4 summaries the performance of the GFET ring oscillators reported so far.

2.2.4 GFET-based Power Detectors

Power detectors are one of the direct applications for exploring the high carrier mobility in graphene. Power detectors are crucial elements in wireless communication systems. Many applications such as: radio-frequency identification (RFID), automatic gain control (AGC), and energy harvesting, require sensitive, low-voltage drop, and low capacitance power detectors.

Employing GFETs in common-source (CS) configuration as linear power detector devices has been reported in [59–61]. The demonstrated GFET power detectors are leveraging the nonlinear channel resistance property above the GFET extrinsic f_T and f_{max} limitations.

The principle challenges of employing GFETs in power detectors are:

- The 3-dB detection bandwidth of GFET detectors is given by $1/(2\pi C_t R_t)$ where C_t is the total gate capacitance which consists of the gate-to-source capacitance, C_{gs}, and gate-to-drain capacitance, C_{gd}. While R_t is the total resistance and is formed by the gate resistance, R_g, in series with the source resistance, R_s. Using GFETs as power detectors has two main limitations. The main limitation comes from the excess capacitance, C_{gs}, which limits the 3-dB detection bandwidth of the power detector.

- Poor tangential signal sensitivity (TSS) and responsivity for frequencies where the transistor acts as a passive element with low current reponsivity.

Table 2.5 shows a performance comparison between different reported GFET-based power detectors.

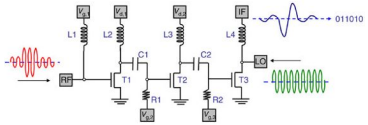
2.2.5 GFET-based Receivers

Based on the discussion in *section 2.1*, the reported graphene receivers based on the use of GFETs are suffering from limited operating frequency and low gain. In addition, the yield for exfoliated graphene is low and the

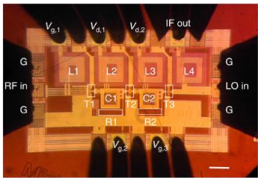
Table 2.5: Performance comparison of GFET-based power detectors.

Ref.	Substrate	Dynamic Range (dB)	Frequency (GHz)
[59]	SiC	45	8.5
[60]	Glass	40	3
[61]	SiC	NA	96

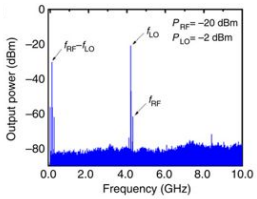
reproducibility is difficult for multiple active devices. Fig. 2.14 shows an integrated three-stages RF receiver in [62] based on GFETs to receiver an RF signal at 4.3 GHz with 10 dB of total system conversion loss. In [63], a single GFET is used as an envelop detector to demodulate amplitude modulation (AM) signal at 2.4 GHz with 34 dB of conversion loss. Additionally, there are very simple receiver frontends with the purpose to demonstrate the ability to demodulate low data-rate, low-power AM, and amplitude shift keying (ASK) signals [62, 64].



(a) Circuit schematic of three-stage graphene receiver IC comprising 11 active and passive components.



(b) Optical micrograph of an IC under testing. The circuit has the dimension of 1020 µm × 600 µm. Scale bar, 100 µm.



(c) Output spectrum of the IC with an input power of −20 dBm at 4.8 GHz f_{RF}.

Figure 2.14: The first three-stages MMIC GFET-based receiver frontend [62].

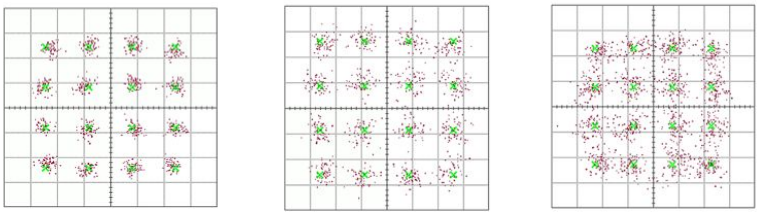
Table 2.6: Performance comparison of GFET-based receivers.

Ref.	Technology	Scheme	f_{RF} (GHz)	P_{LO} (dBm)	DC Power (mW)	CL (dB)
[63]	CVD/kapton	1-GFET	2.45	NA	NA	34
[62]	CVD/Si	3-GFETs	4.3	−2	20	10

Table 2.6 summaries the performance of the reported graphene-based receivers.

2.2.6 GFET-based Transmitters

Due to the limitations of GFETs mentioned in *section 2.1* and the reported limited output power and frequency of operation of the GFET-based amplifiers in *section 2.2.1*, there is no reported full transmitter based on graphene devices till writing this dissertation to the best knowledge of the author. However, the reported W-band digital modulator in [65] shows promising results. Fig. 2.15 shows the constellation diagrams of the 16-Quadrature Amplitude Modulation (QAM) with 4 Gbit/s Fig. 2.15a, 8 Gbit/s Fig. 2.15b, and 16 Gbit/s Fig. 2.15c. On the other hand, the implementation of a power amplifier (PA) to realise the transmitter frontend using GFETs in the W-band is challenging.



(a) 4 Gbit/s, 16-QAM. (b) 8 Gbit/s, 16-QAM. (c) 16 Gbit/s, 16-QAM.

Figure 2.15: Measured constellation diagram of a 16-QAM modulated signals with different data-rates [65].

Therefore, the main limitation to realise high frequency transmitters based on graphene active devices is the performance of reported state-of-the-art GFETs.

2.3 Summary and conclusion

In this chapter GFET device development, challenges, and different technologies are explained. The promising features of graphene are not yet fully employed in the existing GFET technologies and schemes. However, the realised GFETs on flexible substrates outperform transistors fabricated based on other competitive, well established semiconductors technologies.

Thenceforth, the reported research on employing the GFETs in high frequency circuits and systems shows clearly the challenges based on the device physics mentioned in *section 2.1*.

As a conclusion, the demand to explore the features of graphene in another device became more crucial. In *chapter 3* the MIG diode is discussed comprehensively exploring its features and opportunities. Later in *chapter 4*, the demonstration of exploiting the features of the MIG diode in circuits and how it outperforms GFETs in many applications is shown. In addition, the performance of the MIG diode-based circuits is compared with other technologies.

Chapter 3

Metal-Insulator-Graphene diode

3.1 Graphene diodes in literature

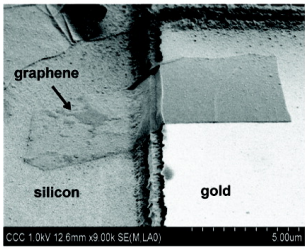
The promising features of graphene are not yet fully utilised by the reported state-of-the-art GFET as shown in *chapter 2*. On the other hand, researches have reported the implementation of graphene diodes to exploit the high electron mobility of graphene. In this section the previous researches carried out to realise high frequency diodes with low series resistance for high frequency applications is summarised briefly. This research took two paths to realise diodes based on the metal-semiconductor Schottky interface; the first is

the established Schottky contact between graphene (as a semimetal) and other semiconductor materials, the second is using graphene/metal contacts. In *section 3.2*, the main contribution of this dissertation which is the CVD-based thin-film metal-insulator-graphene diode with its outstanding low- and high-frequency features is presented. This diode employed the same structure of the metal-insulator-metal diode instead of the metal-semiconductor Schottky contact as will be shown in *section 3.2*.

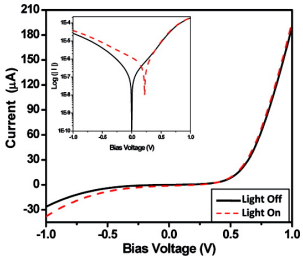
3.1.1 Graphene-semiconductor Schottky contact

Replacing the metal contact with graphene contact to a semiconductor material in a metal-semiconductor Schottky diode has been reported in many researches [66–70]. The contact between graphene and semiconductor creates a Schottky barrier hight (SBH) with a value depending on the used semiconductor and the graphene material. In [67], the contact between graphene and 4H-SiC created a SBH of 0.36 eV. However, the reported current density level was in the range of picoampere.

In [68] the Schottky contact between mechanically exfoliated graphene and Si has been studied. Fig. 3.1 shows the SEM micrograph of the proposed



(a) SEM micrograph of graphene on *n*-Si.



(b) Current–voltage characteristics of the device with and without illumination. The inset figure shows current on a log scale.

Figure 3.1: Graphene/Si Schottky diode [68].

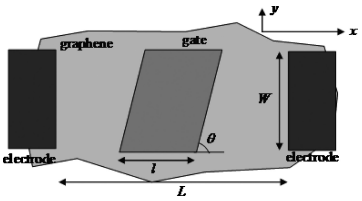


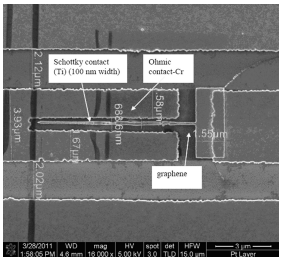
Figure 3.2: Ballistic graphene diode schematic [71].

diode in addition to the measured DC characteristics of the diode. The light sensitivity of the introduced junction has been demonstrated in the I-V showing promising behaviour for light sensing applications [66]. In [69] the reported on-off ratio has been improved by extending the interface with SiO_2 and using doped Si. The use of graphene-semiconductor interface Schottky barrier in solar cells has been discussed in [70].

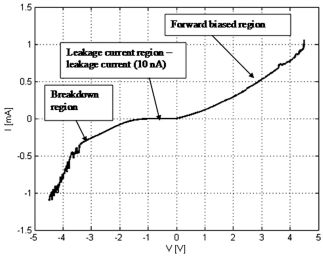
3.1.2 Graphene-metal Schottky contact

Graphene-metal interface has been reported in [71], which led to the development of a graphene-based ballistic diode. Fig. 3.2 represents the schematic of the proposed three terminal nonlinear device where the distance, L, between the metal electrodes is less than the mean-free-path in graphene at room temperature. Another terminal is needed to modulate the transmission coefficient in graphene by an induced electrostatic potential. This terminal is represented by the gate electrode with width, l, and oblique inclination angle, θ, in Fig. 3.2. The predicted Cutoff Frequency (f_c) for this diode was 4 THz.

In [72] a two-terminal device is introduced based on asymmetric metal contacts to improve the nonlinearity and asymmetry of the device. The used metals were Ti with a work function 4.33 eV for the Schottky contact and Cr with a work function of 4.5 eV for the ohmic contact. The fabricated device SEM micrograph is shown in Fig. 3.3. The demonstrated DC characteristics of the fabricated diode showed excellent current density compared to the graphene-semiconductor Schottky diodes. However, the reported asymmetry is low due to the concept of operation which relies on the work function



(a) SEM micrograph of the fabricated diode.



(b) I-V characteristics of the diode.

Figure 3.3: Grapene diode with asymmetric metal contacts [72].

differences of the used metal electrodes. Additionally, in forward bias the device works as a resistor with low rectification properties.

3.2 Metal-Insulator Graphene diode

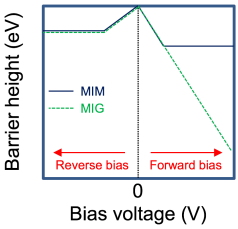
An alternative structure other than the metal-semiconductor structure is the Metal Insulator Metal (MIM) diode structure which have attracted attention due to the two main advantages over semiconductor based *pn*-diodes and Schottky-diodes [73–75].

- First, the low diode series resistance which leads to improved performance in higher frequency applications.

- In addition, these diodes can be fabricated in a thin-film process which makes them attractive for nonsemiconductor based systems like glass and alumina or flexible substrates.

However, the performance of MIM diodes in terms of asymmetry and nonlinearity are inferior compared to other semiconductor based diodes [76]. The main reason is the trade-off between the current density and the diode asymmetry compromised by the thickness of the insulator oxide layer.

(a) MIM [75] and MIG diodes structures.



(b) Barrier height versus applied bias voltage for both MIM and MIG diodes.

Figure 3.4: MIG and MIM diodes structures and barrier hight for forward and reverse biasing conditions [79].

Graphene diodes utilising the MIM diodes structure have been introduced independently in [77, 78] by replacing one metal electrode with graphene. The resulting of this structure is called Graphene-Oxide-Metal (GOM) in [77] based on exfoliated graphene, and MIG in [78] based on CVD graphene.

Fig. 3.4a compares the principal structures of the MIM and the proposed MIG diodes. The MIG diode operation is described by the thermal emission theory. As shown in Fig. 3.4b, in the reverse bias the barrier height for electrons to transfer from M1 to M2 in the MIM and from M to G in the MIG decreases with increasing reverse voltage until it reaches the potential difference between the work function (ϕ_M) of M1 and the conduction band edge of the insulator for MIM. In the case of the MIG diode, the barrier decreases until it reaches the potential difference between the work function of M and the conduction band edge of the insulator. In forward bias, the barrier height for electrons to transfer from M2 to M1 in MIM is reduced until it reaches the potential difference between the work function of M2 and the conduction band edge of the insulator. This creates the necessary asymmetry between forward and reverse operation. In the case of the MIG diode, the barrier height for electrons to transfer from graphene, G, to metal, M, decreases with the increasing forward bias, *i.e.* a bias induced barrier lowering, which explains the high on-current, higher asymmetry for the MIG diode compared to the MIM diode. The reason for that is the different charge transfer concept with the bias induced barrier lowering in the MIG

diode which solves the required trade-off between current density and the asymmetry in the MIM diode.

The main advantage in the proposed diode compared to the diode reported in [77], is processing the MIG device with CVD-grown graphene [78] providing the scalability and repeatability which are necessary for device modeling and their application in complex circuits.

3.3 Physical implementation considerations

The cross section of the MIG diode is shown in Fig. 3.5, comprising an embedded metal electrode, a TiO_2 barrier layer and graphene contacted by a metal electrode on top. The choice of such a geometry has been motivated by the fact that a high quality TiO_2 barrier layer can be grown directly on the metal using plasma assisted ALD, while avoiding the challenging and less reproducible deposition of thin dielectric layers on top of graphene. The MIG diodes fabrication process was implemented on two different substrates to ensure the substrate independence of the device. The used substrates were 500 µm thick HRS with a 1 µm thermal SiO_2 layer and a 500 µm thick glass substrate, in order to minimize the parasitic capacitance through the substrate.

The entire fabrication process is performed using optical contact lithography. Fig. 3.6 illustrates the main fabrication steps. As a first step 200 nm deep trenches are etched into substrate by Reactive Ionic Etching (RIE) for the deposition of the embedded metal electrodes. With the same resist mask, the

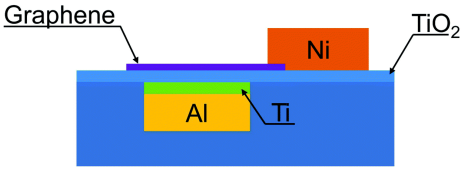


Figure 3.5: MIG cross section schematic.

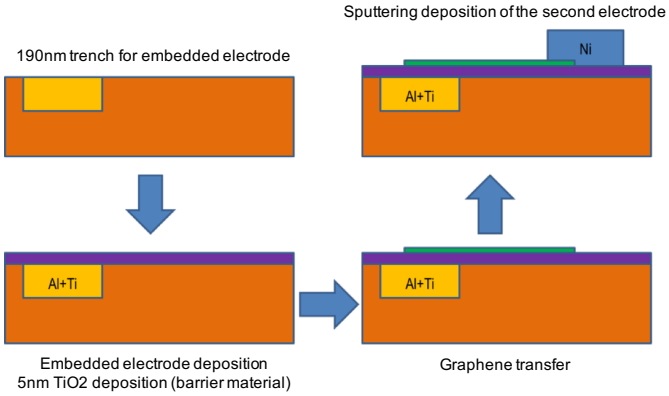
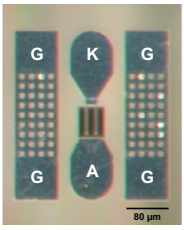
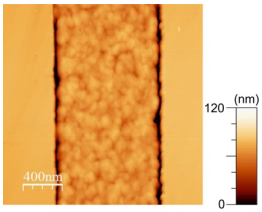


Figure 3.6: MIG diode fabrication process.

trenches are then filled with a stack of 180 nm Al and 20 nm Ti using electron beam evaporation, followed by lift-off. The metal electrode in the trench is properly aligned with the surface of the substrate with a height difference below 10 nm, which is confirmed by a surface profiler. A layer of 6 nm TiO_2 is subsequently deposited by ALD at 300 °C using an oxygen plasma process with titanium tetrachloride ($TiCl_4$) as a precursor. Vias through the TiO_2



(a) Chip micrograph of the fabricated MIG.



(b) Atomic Force Microscope (AFM) image of the embedded electrode before TiO_2 deposition.

Figure 3.7: Fabricated MIG diode on glass substrate with 2 fingers each of 2 µmx40 µm active area.

layer are opened by sputtering with Ar plasma and subsequently sealed with 20 nm Ni without breaking the vacuum. Commercially available graphene grown by CVD on copper foil is transferred onto the sample using PMMA as a supporting layer [80]. After patterning the graphene by means of oxygen plasma, metal contacts to the graphene are fabricated by sputter deposition and lift-off, with a 20 nm Ni and 100 nm Al metal stack. The contact to graphene using sputtered Ni was proved to be ohmic in [56, 81, 82].

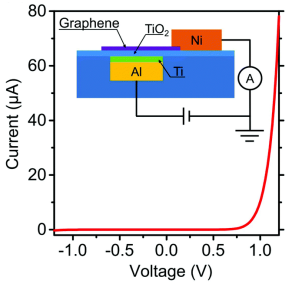
The chip micrograph of the fabricated MIG diode on glass substrate is shown in Fig. 3.7a occupying an overall active area of 160 µm^2 with two fingers. The AFM image of the embedded electrode before TiO_2 deposition is shown in Fig. 3.7b. The Root Mean Square (RMS) roughness of the electrode surface is 6 µm, based on the height distribution from the middle part of the shown AFM image. Due to the excellent surface coverage of the ALD technology, the TiO_2 barrier layer can be formed properly onto the embedded electrode, which is crucial to reduce the fringing capacitance between the two electrodes which improves the performance of the diode as shown in the small-signal model explained in *section 3.5*.

3.4 Diode characterisation

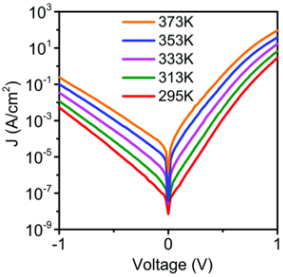
On wafer DC characterisation of the fabricated devices is shown in Fig. 3.8a demonstrating a high current density (J) of 176 A/cm^2 compared to state-of-the-art MIM diodes. The ideality factor, η, of the DC diode is 1.7, extracted according to the following relationship [83]:

$$\ln\left(I_D\right) \propto \frac{e}{\eta k_B T} V_D, \tag{3.1}$$

where, I_D is the diode current, V_D is the voltage across the diode, e is the elementary charge, k_B is the Boltzmann constant, and T is the absolute temperature. The dependency of J on temperature is plotted in Fig. 3.8b for temperatures of 295 K, 313 K, 353 K, and 373 K. While the overall characteristic of the diode in terms of asymmetry and nonlinearity is not significantly affected by the temperature, the absolute current density shows



(a) Measured I-V characteristics.



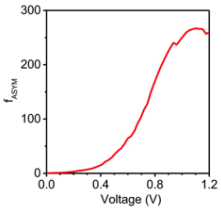
(b) Measured J temprature dependency.

Figure 3.8: Measured DC characteristics of the fabricated MIG diode.

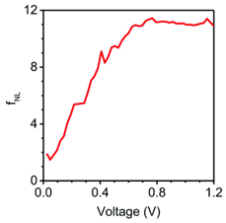
a strong temperature dependency, *i.e.* a clear signature of thermally activated transport across the barrier, as expected for thermionic emission.

The diode rectification Figure-of-merits (FOMs) are used to evaluate the rectifying capabilities of a diode from its DC characteristics [84]. From the measured I-V characteristics the FOMs are calculated according to:

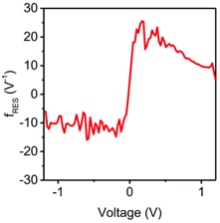
$$f_{Asym} = \left| \frac{J_F}{J_R} \right|, \tag{3.2}$$



(a) Extracted f_{Asym}



(b) Extracted f_{NL}



(c) Extracted f_{RES}

Figure 3.9: Extracted Figure-of-merit (FOM)s of the fabricated MIG diode.

$$f_{NL} = \frac{dJ}{dV} \Big/ \frac{J}{V}, \tag{3.3}$$

and

$$f_{RES} = \frac{d^2J}{dV^2} \Big/ \frac{dJ}{dV}. \tag{3.4}$$

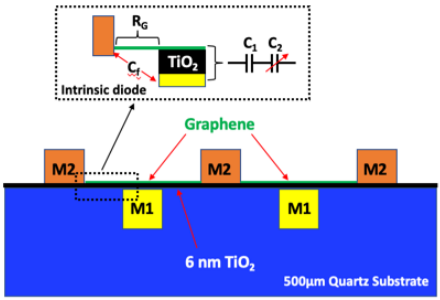
where, J_F is the forward current density, J_R denotes the reverse current density, f_{Asym} represents the diode current asymmetry between the ON and OFF states, f_{NL} measures the deviation from a linear resistor which is calculated as the ratio between the differential conductance and the conductance, and f_{RES} represents the short circuit current responsivity.

Calculating the FOMs of the MIG diodes confirms a high asymmetry up to 525, with a strong maximum nonlinearity of up to 10, and responsivity of up to 27 A/W. The extracted FOMs are plotted in Fig. 3.9. These features, especially in terms of the responsivity, outperform state-of-the-art MIM and Schottky diodes [76, 78]. The calculated f_{RES} of the MIG diode represents a substantial achievement for the graphene technology compared to other diode technologies including Schottky diodes, MIG diodes, tunnel diodes, and spin diodes [85].

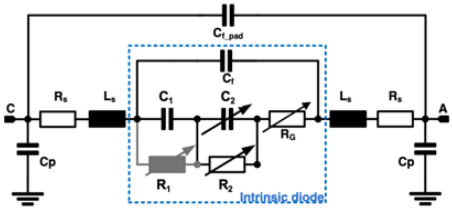
3.5 MIG diode small-signal-model

The chip micrograph of the fabricated MIG diode on glass substrate is shown in Fig. 3.7a. The cross-section of the intrinsic diode is shown in Fig. 3.10a. The diode is composed of the parallel plate capacitor between the metal layer $M1$ and the graphene sheet. Due to the low density of states in graphene, the diode is modeled with two capacitances in series [86].

Accordingly, the diode could be modeled as a series combination of a linear capacitance, C_1, and a bias-dependent, nonlinear capacitance, C_2. Consequently, the DC bias-dependent nonlinear junction resistance is composed of the series combination of the leakage resistances of the two capacitors, R_1 and R_2, and the graphene sheet resistance, R_G. This series combination of C_1, C_2, and R_G is in parallel with the fringing capacitance, C_f, between the two metal electrodes. Fig. 3.10b shows the complete small-signal model



(a) Functional cross-section diagram (not to scale) showing the physical representation of the small signal-model parameters of the intrinsic diode



(b) The complete small-signal model of the MIGdiode

Figure 3.10: MIG diode small-signal model [87].

including the probing pads parasitics. Physical design considerations are applied to reduce the parallel fringing capacitance, C_f, by embedding the first electrode ($M1$) into the substrate. In addition, the physical implementation ensures that the linear series capacitance, C_1, is larger than the nonlinear capacitance, C_2. Consequently, C_2 dominates the equivalent capacitance.

On-wafer S-parameter measurements are carried out from 10 MHz-70 GHz for the fabricated diodes with different bias voltages from -2 V to 2 V. The obtained results are used to calculate the values of the lumped elements representing the small-signal model in Fig. 3.10b.

Values of the bias-independent lumped components are listed in Table 3.1

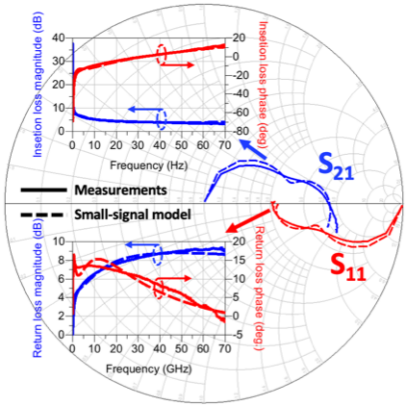


Figure 3.11: S-parameter simulation of the extracted small-signal model in comparison with the measurement results of the MIG diode; insets show the comparison between simulation of the small-signal model and measurements for the magnitude and phase of insertion and return loss [87].

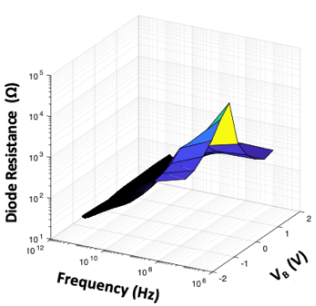
and the bias-dependent elements values at zero-bias presented in Table 3.2 validate the physical design considerations. The extracted value of the linear capacitance, C_1, is about ten-times larger than C_2. Similarly, the value of C_f is twenty-seven times less than C_2. At frequencies higher than 100 MHz, R_1 is practically shorted by the impedance of C_1 providing lower loss at higher frequencies. Accordingly, the MIG diode-based circuits provide substantial improvement at higher frequencies compared to GFET-based circuits as will be shown later in *chapter 4*.

Table 3.1: Extracted bias-independent lumped element components value of MIG small-signal model shown in Fig. 3.10b [87]

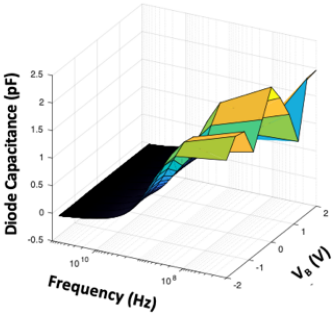
Component	C_p	R_s	L_s	$C_{f_{pad}}$	C_f	C_1
Values	5.4 pF	5.1 Ω	19 pH	1.1 fF	7.8 fF	2 pF

Table 3.2: Extracted bias-dependent lumped element components values at zero-bias of MIG small-signal model shown Fig. 3.10b [87]

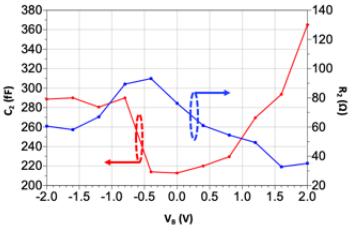
Component	R_G	R_1	C_2	R_2
Values	40 Ω	17 kΩ	212 fF	76 Ω



(a) Measured two-terminal diode resistance versus bias and frequency



(b) Measured two-terminal diode capacitance versus bias and frequency



(c) Extracted bias dependency of C_2 and R_2

Figure 3.12: Fabricated MIG diode AC characterisation.

Also shown in Fig. 3.11 is the comparison between the extracted model and the measurement results over the whole 10 MHz-70 GHz band with less than 1 dB magnitude mismatch and better than 2° phase mismatch for the return and insertion loss shown in the insets.

Fig. 3.12a & 3.12b show the extracted overall resistance and capacitance of the diode across frequency for different bias voltages. Fig. 3.12c demonstrates the bias dependency of C_2 and R_2. The extracted nonlinear capacitance demonstrates the quantum capacitance behaviour, while the extracted resistance proves the bias induced barrier lowering in the junction as presented in *section 3.2*.

The shown model and the characterised diode operation up to at least 70 GHz prove the potential of employing MIG diodes in circuits for higher frequencies with promising performance.

3.6 Summary and conclusion

In this chapter the attempts in research to realise graphene-based diodes showing the different approaches used in this regard is demonstrated. Thenceforth, the CVD-based MIG diode has been indicated showing the device charge transfer physics, physical implementation, and DC and AC characterisations. Last but not least, the small-signal model parameters of the diode have been identified, extracted, and compared with measurements for the frequency band 10 MHz-70 GHz. Later in *chapter 4, 5, and 6* the employment of MIG diodes in circuits and systems is presented and compared with GFETs implementation whenever exist.

Based on the above and as a conclusion, the proposed diode with its outstanding features which not only outperform previous graphene-based diodes, but also can be fabricated in a thin-film process, which enables the realisation of flexible high frequency diodes. The CVD-graphene process provides the aimed repeatability and reproducibility need to realise complex circuits at high frequencies, which is the topic of the remaining chapters of this work.

Chapter 4

MIG diode-based circuits

In this chapter, the employment of the MIG diode presented in *chapter 3* is discussed. The developed thin-film MMIC technology is presented in details. Thenceforth, the implemented circuits which utilize the features of the MIG diode are shown in details.

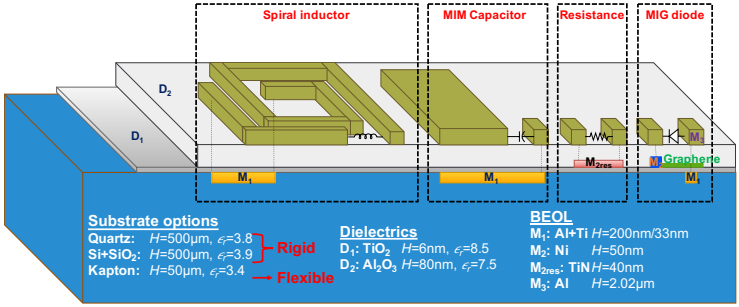


Figure 4.1: Graphene-based MMIC technology.

4.1 Developed Thin-film technology

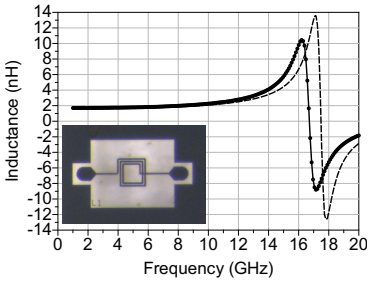
For the first time, the graphene-based MIG diodes presented in *chapter 3* are implemented in MMIC processes on HRS, quartz, and flexible kapton foil substrates. The first version of the MMIC has been reported in [88] which was optimised for GFET devices. Later, the MMIC has been modified to include the MIG device with some optimisation modifications to integrate high quality passives along side with the MIG [89]. The top-view and side-view of the resulted active and passive components are shown in Fig. 4.1. In total, there are six patterning steps for the process, which are all accomplished by photolithography. The functions of all the layers are summarized in Table 4.1. First, the embedded electrode (M_1 layer) is patterned and followed by the RIE of SiO_2. The resulted depth of the trench is 200 nm. By keeping the same resist mask after etching, the metal stack of 180 nm Al and 20 nm Ti is evaporated and followed by lift-off process. Afterwards 6 nm TiO_2 (D_1 layer) is deposited by plasma enhanced ALD at 300 °C using $TiCl_4$ as precursor. Graphene is transferred onto the substrate with PMMA as a supporting layer [80], and then patterned by oxygen plasma etching (graphene layer). The 50 nm sputtered Ni (M_2 layer) forms the contact to graphene-based on a lift-off process. Oxygen plasma is used prior to the metalization to realise a simple edge contact for lower contact resistance [90]. The previous part is the same as the fabrication steps for the MIG presented in *section 3.3*. The following steps are the remaining steps of the MMIC. The thin film resistor (M_{2res} layer) is fabricated also with a lift-off process after sputtering

Table 4.1: Developed MMIC technology layers and their definitions

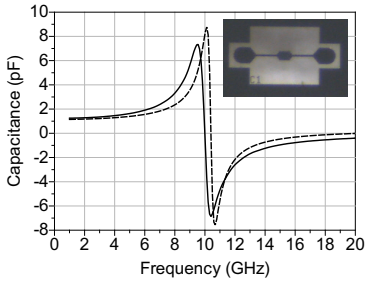
Layer	Functions
M_1	The first electrodes for diodes, the first plate electrode for capacitors, bottom connection for inductors.
D_1	Barrier layer for MIG diodes.
Graphene	Graphene patterning.
M_2	Contact metal for graphene, *i.e.* the second electrode for MIG diodes.
M_{2res}	Thin film resistors.
D_2	Encapsulation for MIG diodes, dielectric for capacitors, separator for inductors.
V	Via through the oxides.
M_3	The second plate electrodes for capacitor, the spiral structures for inductors, interconnection, measurement pads.

deposition of 110 nm TiN, which delivers a sheet resistance of about 50 Ω/□. Subsequently, 80 nm Al_2O_3 (D_2 layer) is grown by ALD at 150 °C using trimethylaluminum (TMA) as precursor and water as oxygen source. The via through the Al_2O_3 as well as TiO_2 (V layer) is etched with diluted HF oxide etchant after patterning. As the last step, 20 nm Ti and 2 µm Al (M_3 layer) is evaporated on the substrate and followed by a lift-off process. The function of the thin Ti before the thick Al is to increase the adhesion of the top metal to the substrate to add the wire-bonding option to the technology.

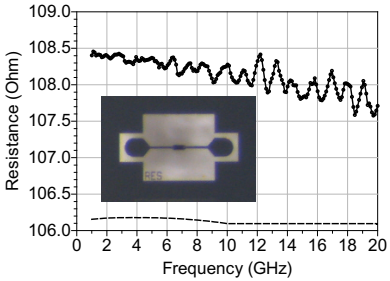
Integrated passives have been fabricated and measured to compare the measurements with the Electromagnetic (EM) simulations using Keysight® Advanced Design System (ADS) Momentum EM tool to prove the proper substrate modeling. Fig. 4.2 shows the comparison between the measurements and EM simulations of inductors (Fig. 4.2a), capacitors (Fig. 4.2b), and resistors (Fig. 4.2c) fabricated on quartz substrate. The agreement between measurements and EM simulations demonstrate a repeatable fabrication process and accurate substrate modeling.



(a) Measured (Solid) and EM simulated (Dotted) inductor



(b) Measured (Solid) and EM simulated (Dotted) capacitor

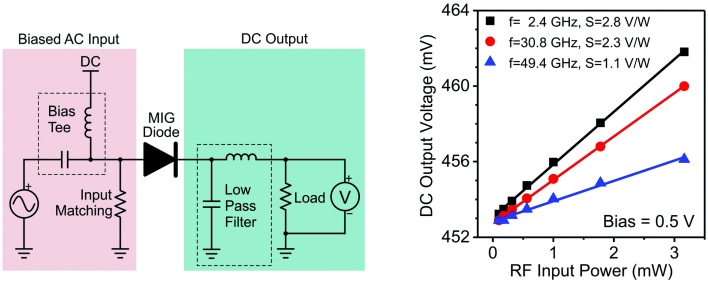


(c) Measured (Solid) and EM simulated (Dotted) resistor

Figure 4.2: Measurements of fabricated passives and EM simulations comparison with chip micrographs insets.

4.2 Power detectors

Power detectors are one of the direct applications for exploring the high carrier mobility in graphene. Power detectors are crucial elements in wireless communication systems. Many applications such as RFID, AGC, and energy harvesting require sensitive, low-voltage drop, and low-capacitance power detectors.



(a) The setup for power detection measurement.

(b) The DC output voltage versus RF input power at different frequencies.

Figure 4.3: Measurement results of the MIG diode configured as high frequency power detector [78].

4.2.1 Single diode rectifier

The rectification of a single MIG diode is demonstrated at RF frequencies. The used setup is illustrated in Fig. 4.3a. A *Rohde&Schwarz® ZVA-50* Vector Network Analyzer (VNA) is used as a calibrated power source with known incident power for the frequency range 2 GHz-50 GHz. The incident power is coupled with a DC bias to the diode using the internal VNA bias-tee. Impedance matching is used to match the input of the diode to the incident RF signal. In order to measure the rectified DC signal. The implemented impedance matching is resistive. Although the resistive matching should be broadband, due to the external connectors it doesn't show the expected broadband matching. S-parameter measurement is carried out for the diode and attaching the impedance matching at the input to select the frequencies such that the corresponding S_{11} is better than -15 dB. A lowpass filter is used at the output of the diode utilizing an external bias-tee. The RF power source and the DC meter as well as the data acquisition are communicated via General Purpose Interface Bus (GPIB) to the Personal Computer (PC).

Power detection characterisation is done at room temperature in ambient environment. The measurements show that essentially no difference was in the DC characteristics of the diode in ambient environment, compared to the

characterised under nitrogen. For the diode biased at 0.5 V, the measured DC output signal versus input RF power for different signal frequencies are plotted in Fig. 4.3b. The RF responsivity of the detector can be calculated based on the slope of the plot. For 2.4 GHz input frequency, the responsivity reaches 2.8 V/W. For higher frequencies, the responsivity drops to 2.2 V/W at 30.8 GHz and 1.1 V/W at 49.4 GHz input frequency. Improvements are expected if the input matching together with the resistive load are integrated on chip. The responsivity of the single-diode rectifier is low compared to other technologies. The reason for that is the low junction resistance of the diode as demonstrated in *section 3.5*. However, the MIG diode rectifier has wide Dynamic Range (DR). Where, DR is the input power range such that the rectifier detects the input signal in its square-law region. The lower limit of the DR is limited by the diode noise, while the upper limit is usually set by the responsivity as will be discussed in the following section.

4.2.2 Linear-in-dB, V-band power detector

The linear-in-dB detector is one type of power detector that is used mostly to measure accurately the power of high peak-to-average ratio RF signals [91]. This technique is used in transmitters to control the output power levels of the PA and in receivers to indicate the RF signal strength in order to adjust the gain of the receiver to ensure a constant signal strength at the input of the Analogue-to-Digital Converter (ADC). This circuit has been reported in [79].

4.2.2.1 Circuit design

The proposed schematic including the MIG diodes is shown in Fig. 4.4. The power detector core consists of the three MIG diodes D_1, D_2, and D_3. D_2 is the main Half-Wave Rectifier (HWR) diode, and together with the clamp diode, D_1, forms a one-stage Cockcroft-Walton voltage doubler circuit [92] to improve the sensitivity of the power detector.

The extended dynamic range is achieved by combining the square-law detector operation with high sensitivity, together with the logarithmic detector

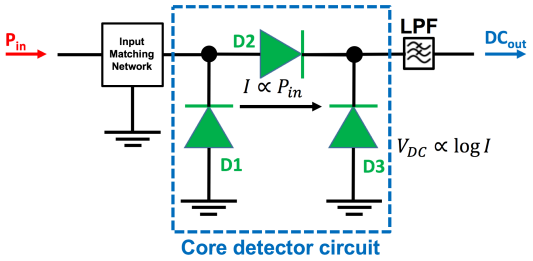


Figure 4.4: Graphene power detector schematic based on MIG diode [79].

operation which has excellent dynamic range. At low input power levels, P_{in}, the clamp diode, D_1, acts as a capacitor, while the HWR operation is done by D_2. Therefore, D_2 operates in the square-law region, producing a current proportional to P_{in}. According to the Taylor expansion of the diode I-V characteristics and assuming a sinusoidal input signal the diode current, i_{D_2}, can be written as:

$$i_{D_2} \approx k v_p^2, k = \frac{I_o}{4\eta V_T}, \tag{4.1}$$

where v_p is the peak voltage of the input signal, I_o is the saturation current, η is the diode ideality factor, and V_T is the thermal voltage.

On the other hand, the input RF power, P_{in}, is related to the input peak voltage, v_p, according to the relation:

$$P_{in} = \frac{v_p^2}{2R_{in}}, \tag{4.2}$$

which leads to the proportionality of i_{D_2} to P_{in}.

At high input powers, the nonlinearity of the shunt diode D_1 is added to the nonlinearity of D_2 resulting in higher compression and extended square-law region for the rectifier circuit. The extracted first-order model of the MIG diode from the DC characteristics of the diode is used to simulate a

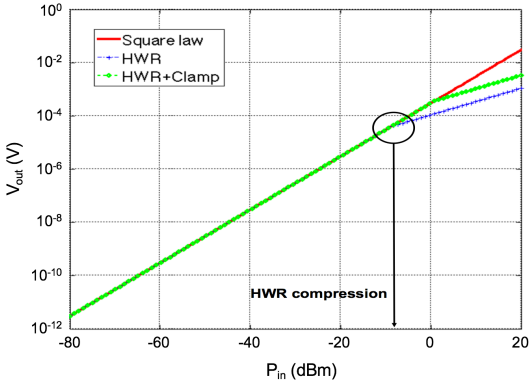


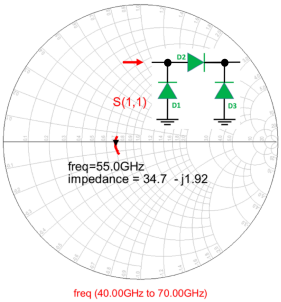
Figure 4.5: Simulated responsivity of the HWR diode and the proposed scheme compared to the square-law detection [79].

HWR circuit formed by the diode D_2 with a resistive load, and the proposed combination of D_1 and D_2 with a resistive load. Simulation results shown in Fig. 4.5 demonstrate the pronounced extension of the square-law region of the proposed detector.

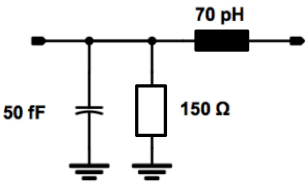
Diode D_3 as a load is responsible to produce an output DC voltage which is proportional to the logarithm of the current. Since the current is proportional to the input RF power, P_{in}, as shown above, the output voltage is proportional to the logarithm of the input power. Since the proposed detector is zero-bias and owing to the properties of the MIG diode, there is no need for an extra DC bias pad. Other advantages of zero-biasing are reduced noise generated by the ON-current of the diodes and low-power operation.

4.2.2.2 Input matching and output lowpass filter

Impedance matching at the input of the power detector is essential to achieve maximum power transfer and to avoid antenna back radiation. Using the measured S-parameters of the MIG diode, the core detector circuit is simulated as shown in Fig. 4.6a, to determine the input impedance at the midband



(a) Simulated core detector circuit input impedance S-parameters.



(b) Input matching circuit schematic.

Figure 4.6: Input impedance design for the linear-in-dB power detector based on the developed MIG diode [79].

frequency of 55 GHz and matching it to 50 Ω.

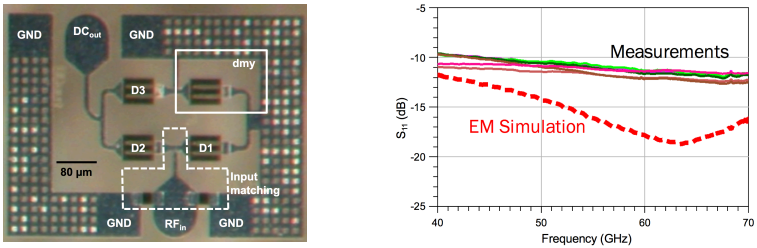
The input matching network, as shown in Fig. 4.6b, is realised by combining resistive and reactive passive components to compromise both low noise and wide bandwidth which is less sensitivity to process tolerances.

The output lowpass filter is implemented by employing an external bias combined with the input impedance of the used DC meter.

4.2.2.3 Measurement Results

The fabricated power detector circuit as shown in Fig. 4.7a occupies a chip area of 0.15 mm^2 including pads. The design is repeated on multiple chips to ensure a statistically stable performance of our Back-End-Of-Line (BEOL) and CVD-graphene process.

To characterise the fabricated detector a Keysight® PNA-X network analyzer is used to measure the S-parameters, as well as a calibrated power source to determine the circuit sensitivity and dynamic range. A Keysight® N8488A



(a) Chip micrographs of the fabricated power detector circuit on 500 µm occupying 360 µm x 430 µm of chip area.

(b) Measured and simulated S_{11} at RF power of −20 dBm for different samples in the frequency band 40 GHz-70 GHz.

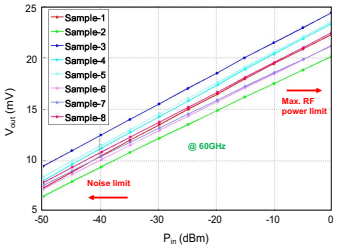
Figure 4.7: Fabricated V-band detector [79].

power sensor and a Keysight® E4418B power meter are employed in the power calibration of the source.

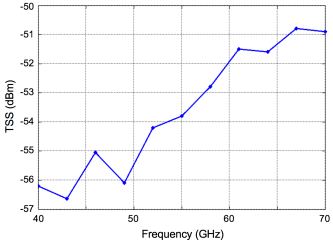
S-parameter measurement results for the fabricated circuits at an RF power of −20 dBm are shown in Fig. 4.7b. The measured input return loss is better than −10 dB for the entire band from 40 GHz-70 GHz for almost all measured samples. Repeatability of the fabricated circuits is also proven by the consistency of the measurement results. Fabrication tolerances lead to a slight shift in the center frequency of the matching network and higher losses compared to the EM simulations.

Detector DR and sensitivity measurements are conducted by sweeping the RF power at certain frequencies in the band and connecting the detector output to a DC meter with 800 kΩ input resistance. Fig. 4.8a shows the measurement results for multiple samples at 60 GHz. The fabricated circuit provides at least 50 dB of DR. Measurements are repeated for different samples and the advantage of CVD graphene process repeatability is demonstrated. Measurements show the increase of the absolute DC voltage with the incident power, the negative sign is only due to the reversed polarity in the DC meter setup.

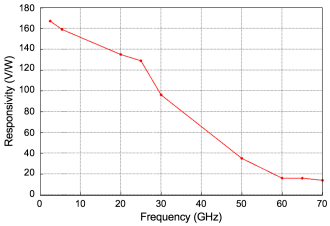
The measured TSS is shown in Fig. 4.8b, demonstrating better than −50 dBm over the entire band.



(a) Detector DR for different fabricated samples.



(b) Measured TSS in the band 40 GHz-70 GHz.



(c) Detector tangential responsivity measurement results up to 70 GHz.

Figure 4.8: Linear-in-dB detector characterisation results [79].

The tangential responsivity in V/W for the fabricated diodes is measured by applying -30 dBm of input power over the frequency range from 2.5 GHz to 70 GHz and measure the output voltage across a 50-Ω load. Since we do not have good input matching for the complete frequency range from 2.5 GHz-70 GHz, the measured S_{11} is used to calculate the incident power on the device which is then used in the graph. Measurement results are shown in Fig. 4.8c. Responsivities as high as 15 V/W at 60 GHz, and 168 V/W at 2.5 GHz depict outstanding responsivity at the 50-Ω load.

Table 4.2 compares the presented power detector with published GFET-based power detectors. All power detectors in this comparison - except for the one presented in this work - are linear detectors based on GFETs. In addition, all GFET-based detectors in the comparison consist of a single

Table 4.2: State-of-the-art comparison with power detectors based on GFETs and other technologies [79]

Ref.	Subs.	Scheme	DR (dB)	Sensitivity (dBm)	Responsivity (V/W)
[59]	SiC	GFET	45	−73	33
[60]	Glass	GFET	40	−60	NA
[61]	SiC	GFET	NA	NA	2
[93]	Al_2O_3	Schottky	25	−55	6000
[94]	PEEK	MIM	20	NA	31
[79]	Quartz	MIG	50	−50	15

device while the presented detector is based on three MIG diodes. It is clearly demonstrated that the measured DR, sensitivity, responsivity, and circuit complexity in the proposed design with repeatable and reproducible results outperform other GFET-based detectors. Compared to other technologies, the large junction resistance of the GaAs Schottky diode-based detector in [93] enables responsivity up to 6000 V/W at the expense of DR and video bandwidth. Compared to the MIM diode-based detector reported in [94], the presented circuit outperforms the MIM diodes-based detector operating at 0.2 V. Performance of MIM diode-based circuits suffers from design challenges especially regarding the oxide thickness [76] which plays a crucial role in increasing the nonlinearity and the charge transfer mechanism.

4.2.3 Distributed power detector

Wideband power detectors have been reported in CMOS either by a 50-Ω brute-force resistive matching as in the subthreshold CS implementation in [95], or by employing a distributed structure as in the Common Gate (CG) detector biased in the resistive regime in [96]. Complementary Metal Oxide Semiconductor (CMOS) detectors suffer from limited DR due to the transistor operation in the limited bias region. The W-band Schottky-diode detector in [93] exploits the high junction resistance, R_j, to achieve high responsivity, sacrificing Video Bandwidth (VBW) and DR.

In this work a distributed power detector using MIG diodes is introduced. A proposed FOM is used to determine the optimum number of stages quantitatively. The distributed detector architecture together with the use of graphene diodes achieve wide RF input matching, outstanding TSS and DR without sacrificing the detector reponsivity. To the best of the author's knowledge, the proposed circuit has the lowest TSS and the widest DR among the reported graphene-based detectors.

4.2.3.1 Circuit Design

The general schematic of the distributed power detector [98] is shown in Fig. 4.9. Referring to the small-signal model presented in *section 3.5*, the inductance, L_{line}, is designed to provide together with the junction capacitance of a single diode, an artificial 50-Ω Transmission Line (TL), achieving wideband input matching. The output load resistance, R_{LPF}, is determined such that its value is greater than the video resistance, R_v, which is the sum of the junction resistance and the diode series resistance. The output capacitor, C_{LPF}, provides an RF ground to eliminate the RF feed-through to the output. VBW is determined by R_v and the parallel combination of the junction capacitances and C_{LPF}.

Accordingly, the extracted small-signal model is used along with EM simula-

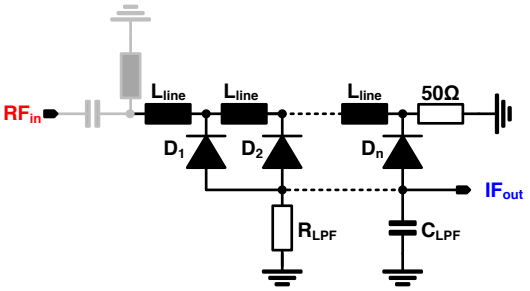
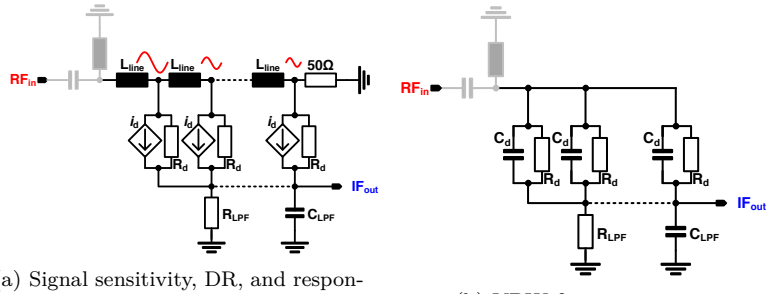


Figure 4.9: Generic n-stage diode-based distributed power detector schematic [97].



(a) Signal sensitivity, DR, and responsivity for n-stages.

(b) VBW for n-stages.

Figure 4.10: Effect of increasing number of stages on the signal sensitivity, DR, responsivity, and VBW.

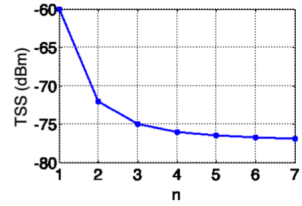
tions to optimise the value of L_{line} in the schematic shown in Fig. 4.9. The TL is implemented using M_3 in the developed MMIC in *section 4.1.*

4.2.3.2 Optimum number of stages

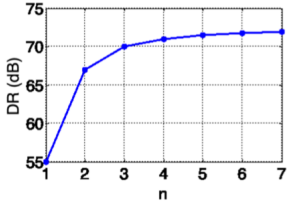
Increasing the number of stages, n, improves the current responsivity (A/W) as shown in Fig. 4.10a, which boosts the Signal-to-Noise Ratio (SNR), resulting in lower TSS. Accordingly, the DR of the detector improves. The improvement in TSS is also affected by the increase in TL loss as the number of stages is increased. This means that the signal strength is reduced as the number of stages increases. To account for the transmission-lines loss, EM simulations are carried out to determine the expected loss.

In the video equivalent circuit shown in Fig. 4.10a, the total R_d is the parallel combination of R_d of the n diodes. Consequently, increasing the number of stages decreases the equivalent R_d. Therefore, the detector voltage reponsivity remains constant as function of number of stages.

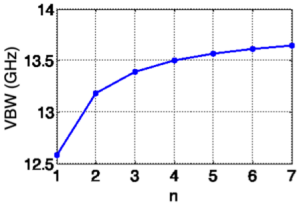
For the VBW as shown in Fig. 4.10b, increasing the number of stages will reduce the equivalent R_v and an increased VBW is noticed for a fixed C_{LPF}. Further increase in the number of stages will make the equivalent C_j comparable to C_{LPF} until a saturation level is reached.



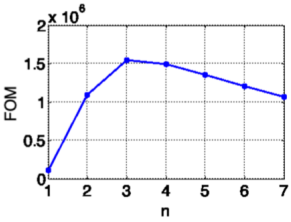
(a) TSS versus n.



(b) DR versus n.



(c) VBW versus n.



(d) The proposed FOM versus n.

Figure 4.11: MATLAB behavioural simulation of and TSS, DR, VBW, and the proposed FOM for the distributed power detector versus number of stages.

To determine the optimum number of stages quantitatively, the figure-of-merit (F_{DPD}) defined as:

$$F_{DPD}(n) = \frac{DR(n)(\text{dB}) \times VBW(n)(\text{GHz})}{TSS(n)(\text{mW}) \times area(n)(\mu\text{m})},$$

is proposed.

A MATLAB behavioural simulation is carried out using a large-signal model of the graphene diode. The loss of the TL is estimated from EM simulations. The pronounced behaviour of the different terms in (4.2.3.2) are shown in Fig. 4.11a for TSS, Fig. 4.11b for DR, and Fig. 4.11c for VBW. All these effects are reflected in the simulation results of the proposed FOM as shown in Fig. 4.11d, demonstrating an optimum number of stages equal to 3 to

maximise the proposed F_{DPD}.

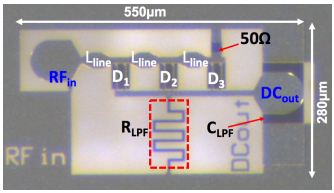
If the area is not present, the optimum number of stage according to the proposed FOM is 8-9 stages such that the VBW is saturating as the equivalent C_j become larger than C_{LPF}.

4.2.3.3 Circuit fabrication and characterisation

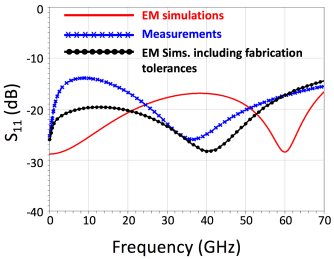
The fabricated prototype of the proposed 3-stage distributed power detector employing MIG diodes is shown in Fig. 4.12a. The total area including pads is 0.15 mm^2. Design values for R_{LPF} and C_{LPF} are 2.5 kΩ and 650 fF respectively. Accordingly, the calculated VBW is around 5 GHz. Measured and simulated S_{11} are shown in Fig. 4.12b. Measurements show better than −13 dB S_{11} up to at least 70 GHz, demonstrating wideband input matching. Fabrication tolerances are noticed in the increased resistance and capacitance, which are responsible for the deviation of S_{11} and the frequency shift compared to the simulation results. The measured S_{11} behaviour is reproducible in EM simulations after adding the characterised fabrication tolerances as also shown in Fig. 4.12b. Additionally, the connections of the diodes to the output lowpass filter shown in Fig. 4.12a are not providing the required RF ground due to their size which also increase the descripency between measurements and EM simulations. Proper star-connection of the diodes outputs to the lowpass filter should also reduce the mismatch between measured and expected S_{11}.

Power detector responsivity, TSS, and DR measurements are carried out using a calibrated RF power source providing the input RF power and a Keysight® B2901A precise nanovoltmeter to record the output voltage. Measurement results for the RF power sweep at different RF input frequencies are shown in Fig. 4.13. A measured DR of 75 dB is achieved at 2.5 GHz and at least 60 dB at 70 GHz due to the limited maximum output power of −7 dBm for the RF power source at 70 GHz. TSS of −75 dBm is measured at 2.5 GHz and better than −65 dBm at 70 GHz is achieved. The measured responsivity is 148 mV/mW at 2.5 GHz and 87 mV/mW at 70 GHz.

Table 4.3 shows the performance comparison between the presented power detector and state-of-the-art power detectors in various technologies. Compared



(a) Chip micrograph of the proposed 3-stage distributed power detector.



(b) Measured S_{11} versus EM simulation results and EM simulations including the measured fabrication tolerances.

Figure 4.12: Fabricated 3-stage distributed power detector [97].

to the GFET implementation in [60], the proposed detector outperforms it in terms of DR, and TSS. Compared to the CMOS implementations in [95] and [96], the limited bias regime for the CMOS transistors leads to low DR. In [93], the high junction resistance results in high responsivity at the expense of limited DR. In the X-band, Common-Emitter (CE) detector in [99], the

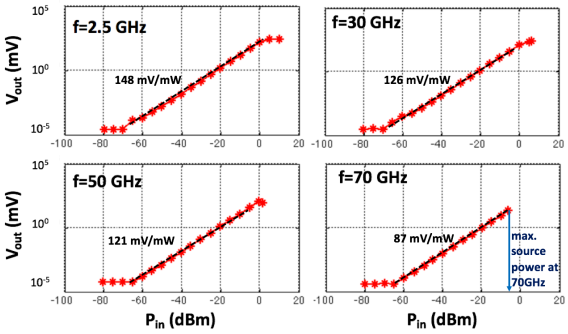


Figure 4.13: Measured output voltage of the distributed graphene power detector versus the incident RF power at different input frequencies [97].

Table 4.3: Comparison with state-of-the-art power detectors

Ref.	Tech.	P_{DC} (mW)	DR (dB)	TSS (dBm)	Freq. (GHz)
[60]	GFET	0	40	-60	3
[95]	65nm-CMOS	0.029	21	-36	0.01-110
[96]	65nm-CMOS	0	20	-40	0.01-110
[93]	GaAs Schottky	0	25	-57	60-110
[99]	0.25μm SiGe	7.2	52	-45	7-20
[97]	MIG	0	> 60	-65	DC-70

obtained responsivity and DR come from the cascode configuration with PMOS diode-connected load with high power consumption. However, the proposed 3-stages detector outperforms the performance in terms of TSS, DR, and power consumption.

4.3 Microwave mixer

In this section, the first reported graphene mixer circuit based on MIG diodes [87] is presented. The lumped elements of the extracted model presented in *section 3.5* shows high potential for the diode to be used in microwave and millimetre-wave circuit applications with better performance than the GFET based mixer circuits. The proposed MIG diode mixer circuit is fabricated on a 500 µm thick glass substrate and is characterised in the frequency band from 1.7 GHz-6 GHz covering many communication standards like Global System for Mobile communications (GSM), Code Division Multiple Access (CDMA), Digital Enhanced Cordless Telecommunications (DECT), ZigBee, Wireless Local Area Network (WLAN), and Bluetooth.

The mixer circuit is shown in Fig. 4.14 with an input RF power combiner. The output of the combiner is fed into an input matching circuit to match the input impedance of the MIG diode to 50-Ω. Then, the zero-bias MIG diode is contacted on-wafer. The diode's output is fed into a resistor to convert it to a voltage signal. The IF voltage signal is buffered using an ultralow distortion

opamp to provide a 50-Ω output impedance with 0 dB overall voltage gain. Fig. 4.15a shows the designed I-to-V 50-Ω IF buffer fabricated on a PCB.

Measured CL for an RF input at 2.4 GHz and an LO input at 2.1 GHz with 5 dBm of LO power is shown in Fig. 4.15b. The circuit demonstrates a CL of 15 dB and an input referred 1 dB compression of 2 dBm. Measured RF and LO return loss and RF-to-LO isolation results are shown in Fig. 4.15c. The mixer circuit provides better than 10 dB input return loss and isolation over the entire band from 1.7 GHz-6 GHz. Fig. 4.15d shows the RF-to-LO isolation measurement performing better than 36 dB in the 2.4 GHz band, with 15 dB coming from the IF buffer.

Table 4.4 summarizes the measured performance of the presented mixer and compares it with state-of-the-art graphene-based mixers. The aim of the comparison with GFET-based circuits is to compare the performance between different devices while the mixing mechanism is based on a single Graphene-based device except for the double balanced scheme in [55] which is based on four GFETs. In terms of CL, the MIG-mixer on a low-cost 500 µm thick glass substrate outperforms other mixer circuits based on exfoliated, CVD, and epitaxial grown GFETs [46–48, 50, 51, 53, 55]. The presented circuit with a single MIG diode achieves the same RF-to-IF isolation as reported in [55] with a double balanced topology. Further improvement of the CL could be achieved by implementing the input power combiner, the

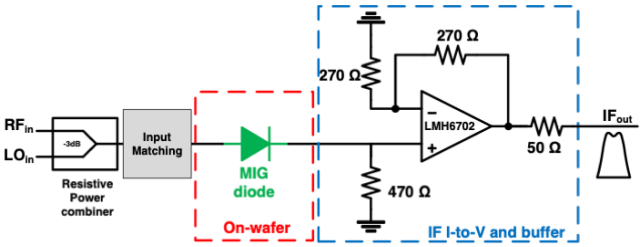
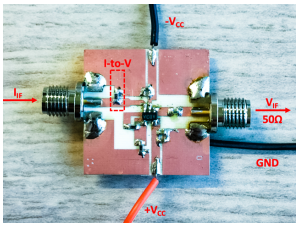


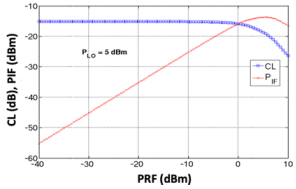
Figure 4.14: Schematic of the proposed down conversion mixer using an on-wafer MIG diode, external hybrid combiner, and an I-to-V 50-Ω Intermediate Frequency (IF) buffer [87].

input matching, and the output IF I-to-V 50-Ω buffer on chip. The expected improvement in CL is at least 3 dB due to the elimination of the loss in the connection cables and external hybrids. Compared to the MIM diode-based mixer presented in [76], the MIG-based mixer outperforms the biased MIM mixer circuit in terms of conversion loss due to stronger nonlinearity of the MIG diode.

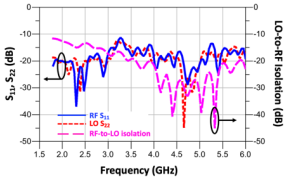
As a proof of concept the proposed circuit has been employed in a life video transmission and reception in the setup shown in Fig. 4.16. The video camera is connected to a standard WLAN transceiver operating in the 2.45 GHz band. The RF input to the mixer consists of a complex OFDM signal with 20 MHz bandwidth *IEEE802.16* standard WLAN signal at 2.442 GHz. The LO is at 2.102 GHz. The output IF signal is at 340 MHz. To demodulate the WLAN signal, a standard WLAN transceiver is used. Using the demodulating receiver at the same frequency of the transmitter does not ensure the elimination of the RF leakage. To solve this problem, the IF signal is upconverted to



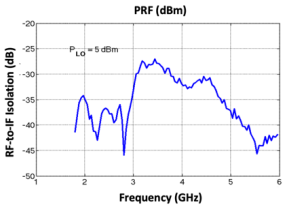
(a) Fabricated I-to-V 50-Ω IF buffer circuit.



(b) Measured output IF power and CL of the mixer circuit versus input RF power.



(c) Measured RF, LO return loss, and LO-RF isolation for the proposed mixer circuit.



(d) Measured RF-to-IF isolation with 300 MHz IF frequency.

Figure 4.15: MIG diode mixer circuit characterisation [87].

Table 4.4: Comparison of the proposed mixer with other mixers

Ref.	Scheme	CL (dB)	f_{RF} (GHz)	LO Frequency (f_{LO}) (GHz)	P_{LO} (dBm)
[48]	CVD	30	0.0105	0.01	0
[50]	Exfoliated	24	1	2.02	15
[53]	Exfoliated	19	24-31	15	10
[51]	Epitaxial	17	10.05	10	−3.5
[55]	CVD	33	3.6	3.5	8.9
[47]	Epitaxial	18	88-100	87-99	8
[46]	CVD	31	4	3.8	15
[76]	Biased-MIM	41	4	3	9.3
[87]	CVD-MIG	15	1.7-6	1.4-5.7	5

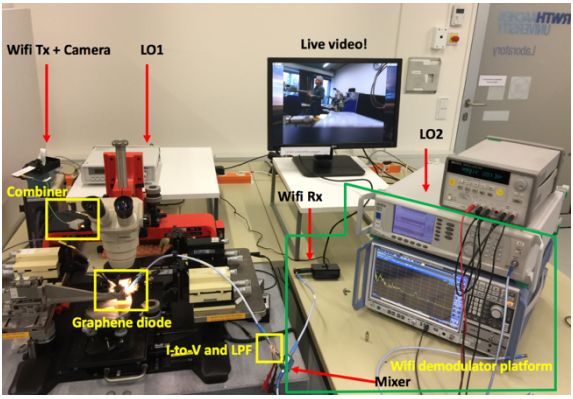
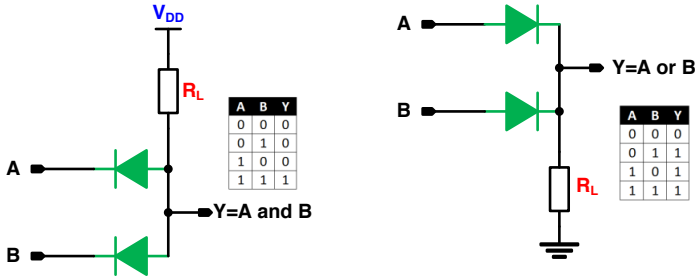


Figure 4.16: Life video transmission and receiption using the proposed mixer circuit.

5.745 GHz using an external LO at 5.405 GHz and a passive mixer. The used setup ensures that the IF downconverted signal using the presented mixer produces the displayed video. The demo was presented in the Mobile World Congress (MWC) in Barcelona. The MIG has been employed in more complex circuits leveraging the features of the MIG diode together with the



(a) DRL AND gate.

(b) DRL OR gate.

Figure 4.17: DRL boolean logic gates.

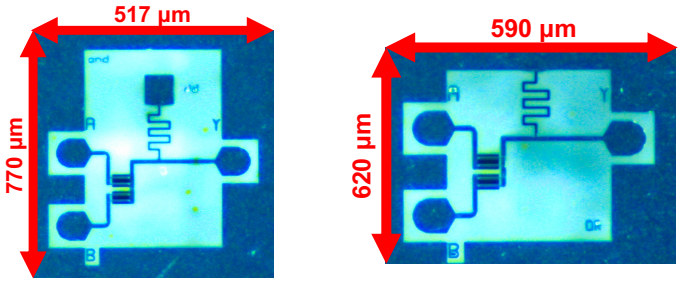
CVD advantage which ensures the reliability in the double balanced topology in [100].

4.4 Thin-film Graphene-enabled memory and logic gates

In the evolution of implementing digital circuits, the employment of diodes in Diode-Resistor Logic (DRL) gates was used to build AND and OR boolean logic gates replacing the bulky and costly active vacuum tubes. The principle limitation of DRL was the driving capability of one gate to drive a following gate, *i.e.* fan-out. A step forward was to add an inverting stage with transistor to add power gain required to enhance the fan-out and to adjust the voltage levels. This later scheme is known as the Diode-Transistor Logic (DTL) scheme. Then, upon the development of integrated circuits and the improvement of transistors. The transistors were employed to perform the logic function along side with amplification to construct the widely used Transistor-Transistor Logic (TTL).

In this section, the employment of MIG diodes to build DRL gates thanks to the excellent diode switching characteristics is demonstrated.

Fig. 4.17 [101] shows the schematics and truth tables of the DRL AND gate Fig. 4.17a and OR gate Fig. 4.17b.



(a) DRL AND gate.

(b) DRL OR gate.

Figure 4.18: Chip micrograph of the fabricated DRL boolean logic gates.

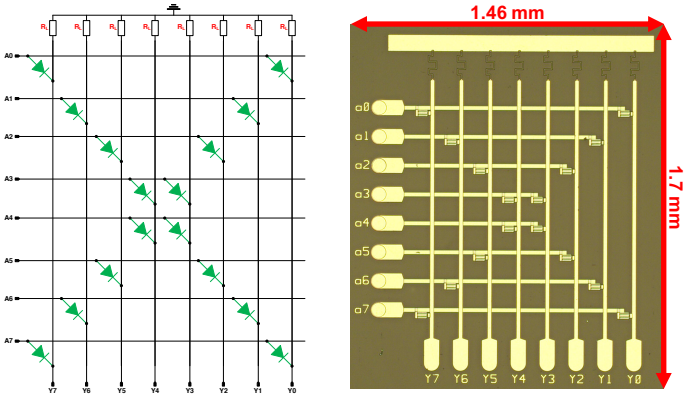
The two DRL gates are fabricated on a quartz substrate with the thin-film MMIC technology as descried in *section 4.1*. The chip micrographs of the fabricated gates are shown in Fig. 4.18.

The AND gate occupies $0.4\,\mathrm{mm}^2$ chip area while the OR gate occupies $0.37\,\mathrm{mm}^2$ chip area as illustrated in Fig. 4.18a and Fig. 4.18b. The fabricated gates were optimised for a demonstration on a PCB after wirebonding the circuit inputs and outputs. Therefore, the circuits were designed with *GSGSG* pads for the inputs as shown in Fig. 4.18a and Fig. 4.18b. Hence, the circuit could only be characterised using DC probes. Consequently, the maximum characterisation frequency is limited by setup.

(a) DRL AND gate.

(b) DRL OR gate.

Figure 4.19: Oscilloscope captured inputs and outputs of the fabricated DRL boolean logic gates.



(a) 8 bit ROM schematic.

(b) 8 bit ROM chip micrograph.

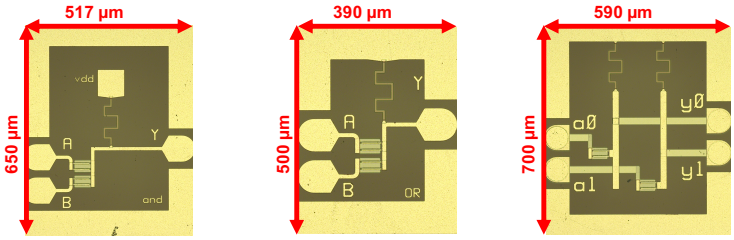
Figure 4.20: MIG diode-based 8 bit ROM.

Fig. 4.19 demonstrates the functionality of the fabricated gates. An oscilloscope is used to monitor the logical inputs and outputs of the DRL gates.

Not only the DRL logic gates were demonstrated in this work. In addition, a 8-bit Read-Only Memory (ROM) is built using MIG diodes as shown in Fig. 4.20a. The ROM is fabricated on the same process for demonstration purpose after wirebonding as discussed before. The chip micrograph of the ROM is shown in Fig. 4.20b occupying a chip area of 2.5 mm^2. The fabricated 8-bit ROM consists of 16 MIG diodes which is considered the largest number of graphene devices in one circuit thanks to the CVD process.

In order to characterise the RF performance of the MIG diode-based DRL boolean logic gates and the ROM, a new design was fabricated in which the *GSGSG* pads were replaced with high frequency *GSSG* probing pads. The chip micrographs of the fabricated circuits are shown in Fig. 4.21. The chip area occupied by the AND gate is 0.34 mm^2, for the OR gate is 0.2 mm^2, and for the 2-bit ROM 0.41 mm^2 as illustrated in Fig. 4.21a, Fig. 4.21b, and Fig. 4.21c, respectively.

Due to fabrication problems, the new fabricated design could not be characterized until the writing of this dissertation.



(a) DRL AND gate. (b) DRL OR gate. (c) 2 bit ROM.

Figure 4.21: Fabricated DRL gates and 2 bit ROM for RF characterisation.

4.5 Summary and conclusion

This chapter demonstrates the exploitation of the unique properties of the MIG diodes in circuits as power detectors, mixers, DRL boolean logic gates, and ROM for the first time. The presented circuits provide operation ranges from DC up to 70 GHz where the upper limitation was determined by the available measurement equipment. Dedicated circuit techniques like Cockcroft-Walton voltage doubler circuit, distributed power detector, and DRL were employed to achieve the demonstrated performance. The CVD process together with the stable and repeatable MMIC technology enable the implementation of complex circuits consists of multiple MIG diodes. The implemented circuits are fully characterised and compared to the performance of state-of-the-art GFET-based circuits. In addition, the comparison with other well established semiconductor technologies like Si and III-V technologies is shown. The realisation of logic gates by GFETs is challenging due to the limitations set by the properties of todays GFETs. The CVD-based MIG diode presented in *chapter 3* promotes the usage of graphene circuits to build systems for applications that require thin-film fabrication for high frequency operation. In the following chapters, more complex systems are discussed in details.

Chapter 5

Six-port receiver

The overview of the published high frequency receiver frontends based on GFETs in *chapter 2* shown that the performance of these receivers rely on the use of GFETs as downconversion mixers with conversion loss. This loss is partially compensated by the use of GFET-based amplifiers at frequencies below the GFETs f_T and f_{max} [62]. These receiver frontends are limited by the ability of the GFETs to provide gain otherwise the loss is high and the sensitivity is poor accordingly. An alternative topology to realise receiver frontends is the six-port scheme which has been reported by the author in [64, 89]. In the six-port topology the MIG diodes are employed as power detectors to utilise their outstanding DR and sensitivity as presented in *chapter 4*.

The evolution of the six-port interferometer was introduced in the 1970's as an accurate method to measure complex ratio of two electromagnetic waves. Since then, it was widely used to build wideband, low-cost, and low-power microwave and millimetre-wave network analyzers [102]. Moreover, the six-port architecture has been reported as a communication receiver, where the frequency conversion is realised by means of additive mixing in the 1990's [103]. Recently, the six-port receiver has drawn a lot of attention for applications that require wideband and low-power operation [104–107].

In this receiver type the complex-modulated and received signal at the frequency, f_{RF}, is linearly added to a reference signal at the LO frequency, f_{LO}. The resulting sum is processed by the nonlinear device, *e.g.* a diode. The output of the nonlinear device includes:

- The rectified wave at DC, *i.e.* a 0 Hz.
- Mixing signals at the sum and difference of the two input frequencies, *i.e.* $f_{RF} \pm f_{LO}$.
- Leakage signals at the fundamental frequencies, at f_{RF} and f_{LO}.
- Higher order harmonics at $nf_{RF} \pm mf_{LO}$, which arise from the nonlinear process in the device.

This output is limited by a Low-Pass Filter (LPF) to the bandwidth of the baseband and only the rectified wave at DC and the signal at $f_{RF} - f_{LO}$ will be observed at the output of the filter. In case of a direct conversion receiver with $f_{RF} = f_{LO}$, the baseband signal is directly observed at the output of the LPF. In six-port receivers, four identical paths of the additive mixer are used with relative phase shifts of 0°, 90°, −90°, and 180° added to the reference signal. This results in the observation of four versions of the baseband signal with the corresponding phases and, hence, the complex I/Q baseband signal can be reconstructed in an analog way. Accordingly, a full-fledged receiver can be obtained by utilizing a linear passive six-port junction and four power detectors.

The proposed six-port receiver configuration is illustrated in Fig. 5.1 and consists of a Wilkinson power splitter, three 90° hybrid couplers, and four

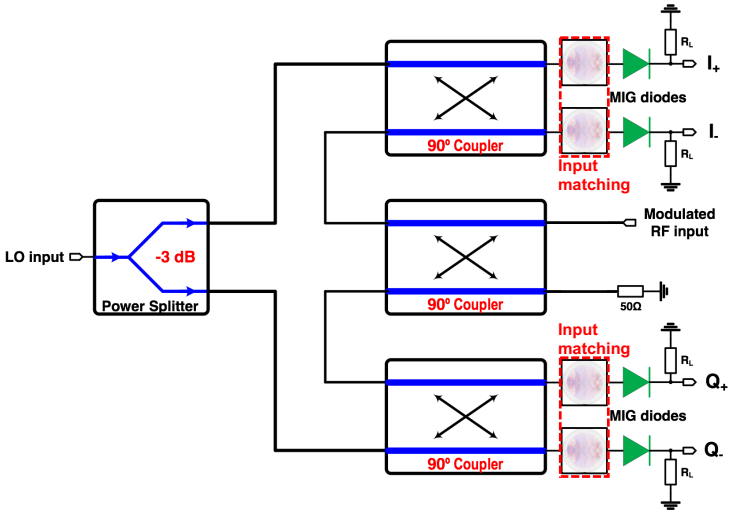


Figure 5.1: Proposed solution: Schematic diagram of the designed six-port receiver frontend showing the 90° quadrature couplers, the power splitter (divider), and the graphene-based power detectors [89].

graphene power detectors. The receiver outputs are fed to a Digital Signal Processing (DSP) unit to calibrate and extract the differential baseband in-phase and quadrature components of the demodulated signal, *i.e.* I^+, I^-, Q^+, and Q^-. Compared to other receiver architectures, the six-port receiver is of relative low complexity and requires only the local oscillator as an active high frequency component besides a Low-Noise Amplifier (LNA) if the required dynamic range of the receiver signal is beyond 40 dB. In addition, due to the fact that the performance of the six-port receiver depends on the linearity of the power detector versus power and frequency of the input signals, it is common to calibrate the six-port receiver to compensate the nonlinearity of the power detectors and the frequency behaviour of the passive junction. The least squares linearization method [108] is used in this work by applying a known data sequence and calculate the coefficients for all outputs. The calculated coefficients are then applied to the received signal.

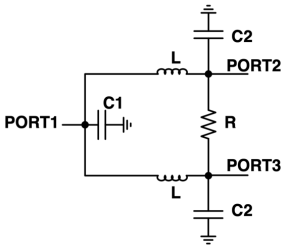
5.1 Six-port junction

Realisation of the passive junction components, which consists of quadrature couplers and power combiner, can be implemented using hybrid $\lambda/4$, long transmission lines providing wideband operation. However, the dependency of the hybrid implementation on the wavelength of the signal makes the size impractical for a compact integration, especially for frequencies lower than 10 GHz. Lumped-element implementation is another option that could be used for lower frequencies.

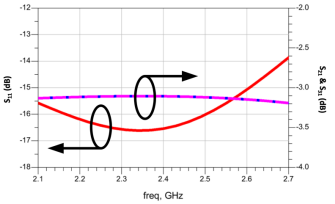
5.1.1 Lumped Wilkinson power splitter

A lumped element implementation of the Wilkinson power splitter for the frequency range 2.1 GHz-2.7 GHz is shown in Fig. 5.2a. The values of the lumped passive components optimised to cover the WiFi-band and adjacent mobile communication frequency bands are shown in Table 5.1.

Fig. 5.2b presents the simulated input return (S_{11}), and insertion (S_{21} and S_{31}) characteristics of the power splitter.



(a) Lumped Wilkinson power splitter schematic.



(b) Lumped Wilkinson power splitter EM simulation results.

Figure 5.2: Lumped Wilkinson power splitter.

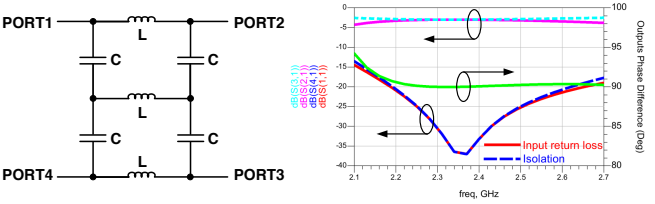
Table 5.1: Values of the lumped Wilkinson power splitter

Component	C_1	C_2	L	R
Value	2.6 pF	1.3 pF	3.3 nH	100 Ω

5.1.2 Lumped quadrature coupler

The chosen architecture of the lumped element coupler for the same frequency range is shown in Fig. 5.3a. The presented architecture has wider bandwidth, better isolation and return characteristics with a lower number of inductors than the conventional implementation [109]. The values of the lumped components are shown in Table 5.2.

As shown in Fig. 5.3(b), the design provides an input return loss, S_{11}, and isolation, S_{41}, below −14.5 dB. The insertion loss, S_{21}, and S_{31}, are symmetric and almost flat with a deviation less than 1 dB over the bandwidth of the receiver. Also the phase difference at the outputs of the coupler is 90° and is almost flat with less than ±5° deviation over the bandwidth from 2.1 GHz-2.7 GHz.



(a) Lumped quadrature coupler schematic.

(b) Lumped quadrature coupler EM simulation results.

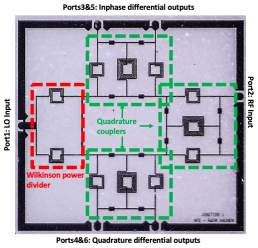
Figure 5.3: Lumped element two-stage quadrature coupler.

Table 5.2: Values of the lumped quadrature coupler components

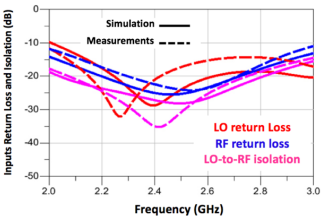
Component	C	L
Value	1.3 pF	3.3 nH

5.1.3 Passive junction characterisation

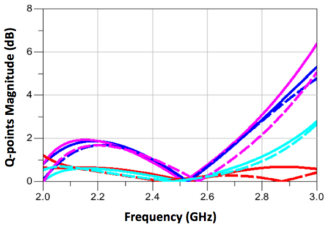
A stand-alone test cell for the passive six-port junction shown in Fig. 5.4a is fabricated to evaluate the RF performance of the junction.



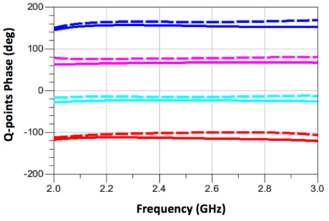
(a) Chip micrograph of the fabricated passive junction test chip occupying 2.3 mm x 1.8 mm chip area.



(b) Measured and simulated return loss and LO-to-RF isolation of the LO and RF inputs.



(c) Measured and simulated magnetiudes of the four output q-points.



(d) Measured and simulated phases of the four output q-points [89].

Figure 5.4: Fabricated six-port junction test cell characterisation [89].

For the passive junction test cell, S-parameter characterisation is performed for the frequency band from 2 GHz-3 GHz using on-wafer GSG probes and the standard calibration substrate. Measurement results indicate good matching between the physical EM simulations and measurements, demonstrating wideband input matching at both RF and LO ports as shown in Fig. 5.4b. Return loss better than -10 dB is measured from 2 GHz-3 GHz and better than 30 dB of LO-to-RF isolation is obtained at 2.45 GHz.

The q-points are the main design measures for the six-port junction, and are expressed as [110]:

$$q_i = -\frac{S_{i1}}{S_{i2}}, i = \{3, 4, 5, 6\}.$$

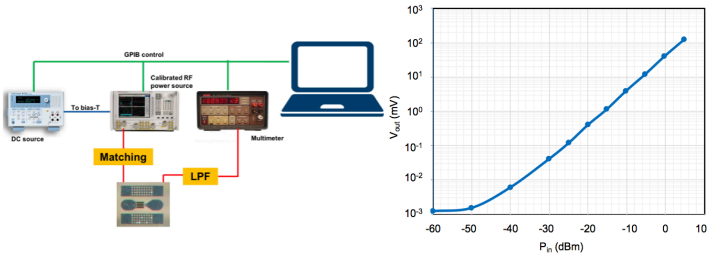
where, S_{ij} are the scattering parameters of the passive six-port junction. Ideally, the q-points magnitudes are unity (0 dB) and the phase differences of successive q-points are 90°.

Fig. 5.4c and 5.4d show the characterisation of magnitudes and phases of the q-points for the designed six-port junction, respectively. Excellent agreement with simulation results is shown. For the bandwidth from 2.1 GHz-2.7 GHz, the magnitudes of the q-points deviate by less than 2 dB, whereas the phase deviations is less than $\pm 5°$ from the design values.

5.2 Six-port receiver realisation

For the prototype receiver, a MIG diode test cell was fabricated on a 500 µm thick glass substrate according to the fabrication steps discussed in *section 4.1*. The diode responsivity was characterised using the setup shown in Fig. 5.5a. Measurements were carried out by sweeping the RF power from a calibrated power source at a single frequency, then the corresponding output DC voltage was recorded. The results indicate, a responsivity of 42 V/W at 2.45 GHz with an RF sensitivity down to at least -50 dBm and a DR of more than 50 dB at zero bias as shown in Fig. 5.5b.

The chip micrograph of the fabricated six-port receiver including the MIG detectors is shown in Fig 5.6a, where four MIG diodes are used with the



(a) Responsivity measurement setup with bias voltage option.

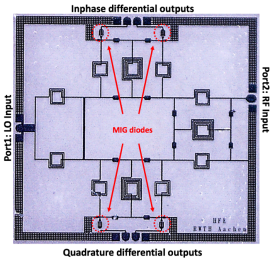
(b) Measured diode responsivity with zero-bias at 2.45 GHz.

Figure 5.5: Measured detector responsivity of the fabricated MIG diode test cell [89].

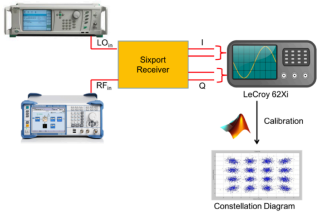
passive six-port junction to realise the receiver circuit. 50-Ω brute-force matching resistors are used at the input terminals of the MIG diodes to guarantee a wideband power matching and lower chip area compared to the reactive matching. However, the resistive matching worsens the noise performance of the receiver compared to a reactive approach. The RF and LO input signals are fed to the circuit through single-ended *GSG* probing pads while a couple of differential *GSSG* probing pads are used to extract the receiver IQ baseband outputs.

The prototype receiver is characterised using the block diagram shown in Fig 5.6b to demodulate a 20 Mbit/s Quadrature Phase Shift Keying (QPSK) signal at 2.45 GHz with −15 dBm modulated RF input power while the LO power was set to 0 dBm. The laboratory setup is shown in Fig 5.6c with measurement devices listed as follow:

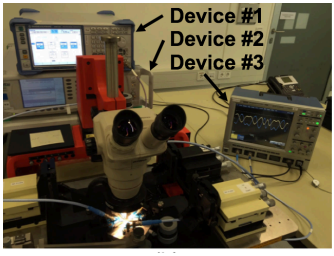
- Device #1: Rohde&Schwarz® vector signal generator used to provide the modulated RF input.
- Device #2: Anritsu® CW generator used to provide the reference LO input.
- Device #3: LeCroy® oscilloscope used to capture the four outputs.



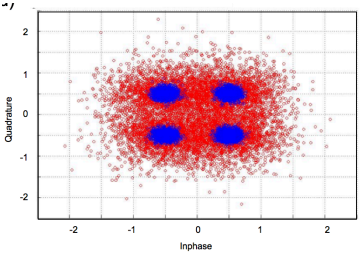
(a) Chip micrograph of the fabricated prototype six-port receiver occupying 2.3 mm x 2.1 mm chip area.



(b) Measurement configuration of the graphene-based receiver frontend including equipments and calibration procedure.



(c) The used laboratory measurement setup showing the measured differential inphase signals waveforms on the oscilloscope screen.



(d) Constellation diagram of a QPSK signal before calibration (red) and after calibration (blue).

Figure 5.6: Characterisation of the fabricated MMIC six-port receiver employing MIG diodes-based power detectors [89].

The recorded I and Q data are fed to a MATLAB algorithm for calibration. For calibration, the least-squares linearization algorithm is applied to the receiver outputs to linearize the MIG diode for different modulations scheme. This calibration model assumes that the diode response is in the linear region which is acceptable for low RF input powers. For higher input powers, more advanced modeling approaches should be used for better constellation and improved error vector magnitude (EVM) [111] which is out of the scope of this work. Fig. 5.6d shows the measured constellation diagram for the captured I and Q data, before (red) and after (blue) calibration. A significant

Table 5.3: Comparison of state-of-the-art graphene-based receivers [89]

Ref.	Active Devices	Modulation	f_{RF} (GHz)	P_{LO} (dBm)	DC Power (mW)	CL (dB)
[63]	1 GFET	AM	2.45	NA	NA	35
[62]	3 GFETs	FM	4.3	−2	20	10
[89]	4 MIGs	QPSK	2.45	0	0	7

improvement of demodulation quality is visible after applying the calibration coefficients. Further improvement could be achieved by adding biasing pads for each MIG diode to enhance the signal sensitivity of the receiver. This helps to align the performance of the four diodes and compensate fabrication process tolerances. In this way, a more distinguishable constellation diagram could be obtained. In addition, reactive matching can be implemented instead of resistive matching which improves the receiver sensitivity as well as the dynamic range.

Table 5.3 shows a comparison with state-of-the-art GFET-based receiver implementations. The presented prototype uses a different implementation method than the conventional architecture used in [62] and [63]. It is clear that the proposed architecture not only outperforms the reported state-of-the-art GFET-based receiver, but it also provides the flexibility of implementing the architecture for different frequency ranges and on different substrates. This in turn enables the use of graphene-based circuits and systems for millimetre-wave, and even submillimetre-wave frequencies on rigid and flexible substrates for various applications.

To sum it up, the represented design approach enables graphene-based receivers overcoming the limitation of f_T and f_{max} of the GFETs as discussed in *chapter 2*. As a proof-of-concept, it has been demonstrated, for the first time, a direct-conversion full-fledged fully-integrated RF receiver frontend fabricated on a thin-film MMIC technology based on MIG devices. This type of receiver is suitable for IoT, RFID systems for medical and communications applications. In addition, the approach is scalable in frequency with either hybrid and lumped-element passive junction implementations. In addition, the power detectors could be implemented using GFETs [64] or MIG diodes [89].

5.3 Summary and conclusion

In this chapter the six-port circuit concept is introduced to build graphene receivers avoiding the constraints implied by GFETs. The main advantage of the six-port topology is that its implementation highly depends on the ability to realisation the high frequency passives and graphene-based power detectors. The shown power detectors based on GFETs in *chapter 2*, and the MIG diodes-based power detectors represented in *section 4.2* could be employed in a six-port receiver topology. The realisation of the passive six-port junction could be achieved either by hybrid or lumped implementations. In addition to the reported six-port receiver in this dissertation, the six-port receiver in [64] has been demonstrated in the W-Band employing GFETs with epitaxially grown graphene on 100 µm SiC substrate. Therefore, the scalability and flexibility of the topology is proven by the two designs with different frequency of operation, implementation, substrate, graphene devices.

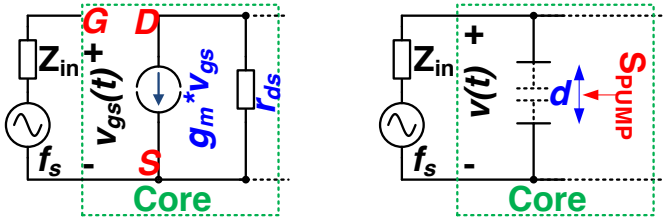
As a conclusion, the six-port topology together with the MIG diodes could be utilized in the implementation of millimetre-wave receivers on flexible substrates based on the proposed thin-film MMIC technology. In addition, the CVD process demonstrates high reproducibility and repeatability proven by the measurement results of the receiver with four matched MIG diodes with no bias whereas the one in [64] needs bias access for each individual diode. Moreover, because it uses GFETs, it has yield issues.

Chapter 6

Parametric Circuits and Graphene Quantum Capacitance

As shown previously in *section 2.1*, GFETs have poor DC current saturation. Accordingly, A_V and f_{max} are limited in state-of-the-art devices. Consequently, realising high-frequency high-gain GFET-based amplifiers is challenging. The shown GFET amplifiers in *section 2.2* rely on g_m and g_{DS} of the transistor to provide signal amplification.

An alternative way to amplify an electric signal is the Parametric Amplifier (PAMP) concept, which relies in varying the reactance value of an inductance



(a) Transconductance amplification. (b) Parametric amplification.

Figure 6.1: Difference between transconductance and parametric amplification concepts.

or capacitance other than varying the transconductance in the traditional transistor implementation. The parametric amplification has been widely used since the 1950's [112–118] before the era of integrated circuits became well established to build transistor-free amplifiers employed for improving the sensitivity of receivers. Consecutive development of metal-oxide-semiconductor (MOS) transistors boosted the use of transconductance based amplification. However, due to the continuous scaling of the transistors, the intrinsic gain is degraded. Accordingly, the PAMP technique started to regain more interest especially in microwave and millimetre-wave domains.

Fig. 6.1 compares the basic schematics of the traditional transconductance and parametric amplifier concepts. Transconductance/transresistance amplification as shown in Fig. 6.1a relies on setting g_m and the Small-signal Drain-Source Resistance (r_{DS}) through the DC operating point of the transistor. The amplification here originates from modulating the injection of energy from the DC source into the load. Contrarily, in the PAMP technique as shown in Fig. 6.1b, the amplification comes from pumping a nonlinear element together with an input signal. Accordingly, the amplification is achieved by delivering energy to the load from an AC power source through the nonlinear element. Consequently, PAMPs have two major advantages:

- The first is the dependency on reactance rather than resistance which means that it is intrinsically noiseless.

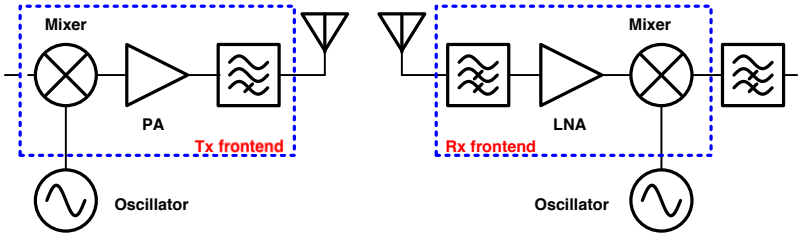


Figure 6.2: Block diagrams of a generic wireless transmitter and receiver frontends.

- The second comes from the simple nature which allows the circuit to adapt well to low power supply voltages required to enable circuits and systems for medical and communications consumer applications.

In addition to the mentioned advantages of the parametric amplifier, it can be also used to perform frequency conversion accompanied with amplification. Accordingly, it is possible to implement the functionality of a canonical receiver frontend consisting of a band selection filter, LNA, and mixer circuits by a transistor-less parametric downconverter amplifier. For transmitters, the frontend represented by the mixer, filter, and PA could be replaced by a parametric up-conversion amplifier as illustrated in Fig. 6.2.

This approach offers a solution to build transistor-less, graphene-based receivers and transmitters with conversion gain.

According to the Manley-Rowe energy model in [113], the small-signal model in [114], and depending on the relation between the three frequencies, *i.e.* Pumping Frequency (f_p), the Input Frequency (f_i), and the PAMP Output Frequency (f_{idler}), the designations of PAMP circuit are:

- **Negative Resistance Amplifier** if $f_{idler}=f_i$.
- **Parametric Downconversion Amplifier** if $f_{idler}<f_i$.
- **Parametric Upconversion Amplifier** if $f_{idler}>f_i$.

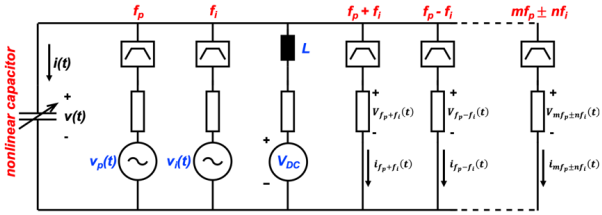


Figure 6.3: Circuit diagram describing the Manley-Rowe [113, 114] equations.

Manley-Rowe relations are deduced by applying the energy conservation principle on the circuit shown in Fig. 6.3:

$$\sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} P_{m,n} = 0, \tag{6.1}$$

where $P_{m,n}$ is the average power at frequency $f_{m,n} = mf_p + nf_i$ For the nonlinear reactance, $P_{m,n}$, its effective real power that can be written according to [113] as:

$$P_{m,n} = V_{m,n} I^*_{m,n} + V^*_{m,n} I_{m,n}, \tag{6.2}$$

where $V_{m,n}$ and $I_{m,n}$ are the coefficients of the double Fourier series of the total voltage and current present at the variable capacitor.

$$v(t) = \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} V_{m,n} e^{j(m\omega_p + n\omega_i)}, \tag{6.3}$$

and

$$i(t) = \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} I_{m,n} e^{j(m\omega_p + n\omega_i)}, \tag{6.4}$$

Using (6.2), (6.3), and (6.4) in (6.1), the Manley-Rowe relations are:

$$\sum_{n=0}^{\infty} \sum_{m=-\infty}^{\infty} \frac{nP_{m,n}}{m\omega_p + n\omega_i} = 0, \tag{6.5}$$

$$\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}\frac{mP_{m,n}}{m\omega_p+n\omega_i}=0. \tag{6.6}$$

Fig. 6.3 illustrates the circuit model describing the Manley-Rowe relations represented by (6.5) and (6.6). These relations assume that the nonlinear element is lossless.

6.1 Parametric Downconversion Amplifier

There are two main classes of the PAMP downconverter amplifier according to the relation between f_{LO} and f_{RF}. Such that f_{LO}=f_p, f_{RF}=f_i, and IF frequency (f_{IF})=f_{idler}. These frequencies correspond for the powers, P_{LO}, RF Power (P_{RF}), and Intermediate Frequency Power (P_{IF}), respectively.

These classes are:

- For f_{LO}<f_{RF} is defined as **Parametric Upper-Sideband (USB) downconversion**: In this case by using (6.5) and (6.6) such that $P_{m,n}$ exists only at the following cases: $P_{1,0}$=P_{LO}, $P_{0,1}$=P_{RF}, $P_{-1,1}$=P_{IF}, it can be shown that:

$$\frac{P_{RF}}{\omega_{RF}}+\frac{P_{IF}}{\omega_{LO}-\omega_{RF}}=0 \tag{6.7}$$

$$\Rightarrow P_{IF}=\frac{f_{IF}}{f_{RF}}P_{RF}. \tag{6.8}$$

  as shown in (6.8), there is no power gain in this topology. However, the low f_{LO} relaxes the design of the LO.

- For f_{LO}>f_{RF} **Parametric Lower-Sideband (LSB)**: in this case f_{IF}=f_{LO}−f_{RF}. In this case, by applying both (6.5) and (6.6) such that $P_{m,n}$ exists only at the following cases: $P_{1,0}$=P_{LO}, $P_{0,1}$=P_{RF}, $P_{-1,1}$=P_{IF}, it can be shown that:

$$\frac{P_{LO}}{\omega_{LO}}+\frac{P_{IF}}{\omega_{LO}-\omega_{RF}}=0, \tag{6.9}$$

$$\Rightarrow P_{IF} = -\frac{f_{IF}}{f_{LO}} P_{LO}. \tag{6.10}$$

A very interesting feature of this operation mode is that there is power gain in this topology. However, it is challenging to design LOs with high output power at high f_{LO}, *i.e.* much higher than the intended RF receiver signal frequency.

6.2 Flexible graphene varactor

The main source of nonlinearity in the graphene-based devices is the quantum capacitance, C_Q [78, 79]. Interestingly, C_Q is a provocative property of graphene that has drawn a lot of attention recently [119]. It originates from the low density of states in Graphene and represents a widely tunable capacitance [120], which can be observed up to very high frequencies. This, in combination with the high carrier mobility in graphene, enables the design of millimetre-wave varactors [121]. The quantum capacitance is expressed as [122]:

$$C_Q(v) = \frac{2e^2 k_B T N L W}{\pi(\hbar\nu_F)^2} \ln\left[2\left[1+\cosh\left(\frac{ev}{k_B T}\right)\right]\right], \tag{6.11}$$

where e is the elementary charge, k_B is the Boltzmann constant, T is the temperature, $\hbar$ is the reduced Planck's constant, ν_F is the Fermi velocity, N is the number of gate fingers, L, and W are the length and width of the junction, respectively. The figures-of-merit of a varactor are defined as:

- Quality factor (Q_F):

$$Q_F = \frac{1}{\omega R_s C_{var}} \tag{6.12}$$

- Capacitance Tunning range (C_r):

$$C_r = \frac{C_{max}}{C_{min}}. \tag{6.13}$$

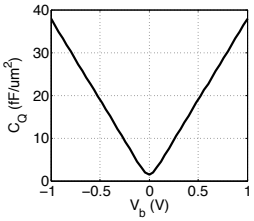


Figure 6.4: Plot of C_Q in fF/µm^2 versus applied voltage.

Fig. 6.4 shows the plot of C_Q in pF/µm^2 versus the applied voltage showing symmetric behaviour around zero-bias. Compared with the three different varactor devices of a MOS-based devices in standard 130 nm CMOS technology illustrated in Fig. 6.5, this shows the unique bias-dependency of the quantum capacitance-based varactors that will be explained later.

The Manley-Rowe relations describe the main behaviour of parametric circuits assuming that the nonlinear device is lossless. In order to account for the parasitic series losses represented by R_s in Fig. 6.6, an elastance model has been introduced in [123], such that:

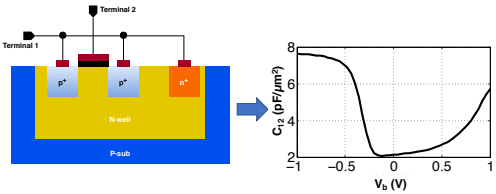
$$v(t) = \int S(t)i(t)dt + R_s i(t), \tag{6.14}$$

where $S(t)$ represents the elastance. The elastance is represented by the following relation:

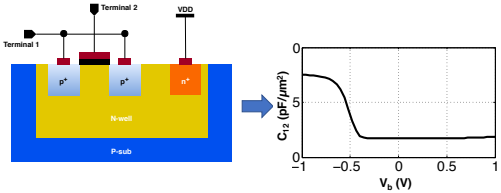
$$S(t) = \frac{1}{C(t)} = \sum_{i=-\infty}^{\infty} S_i e^{ij\omega_{LO}t}, \tag{6.15}$$

$$\Rightarrow S(t) = S_0 + S_1 \mathrm{e}^{j\omega_{LO}t} + S_2 \mathrm{e}^{2j\omega_{LO}t} + S_3 \mathrm{e}^{3j\omega_{LO}t} + ... \tag{6.16}$$

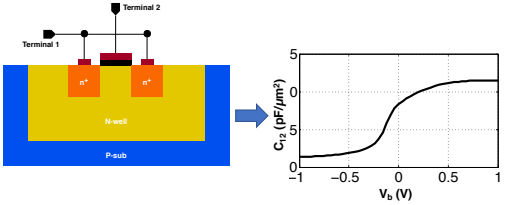
In (6.16), S_i represents the harmonic elastance in the frequency domain whereas the varactor is pumped by the LO signal with frequency f_{LO}. Applying the MOS varactor C-V behaviour shows that S_0 and S_1 are much



(a) MOS capacitor: cross section and simulated C-V characteristics.



(b) Inversion-mode MOS varactor: cross section and simulated C-V characteristics.



(c) Accumulation-mode MOS varactor: cross section and simulated C-V characteristics.

Figure 6.5: Different MOS-based varactors in standard 130 nm CMOS technology.

higher than other higher order S_i terms [124]. Consequently, the phasor representation of the elastance can be expressed as:

$$S(t) \approx S_0 + S_1 e^{j\omega_{LO} t}. \tag{6.17}$$

Fig. 6.7 shows Matlab simulations of $C_Q(t)$ and $S(t)$ for the case of 0 dBm

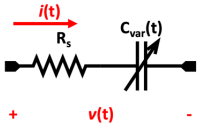
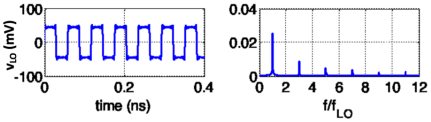


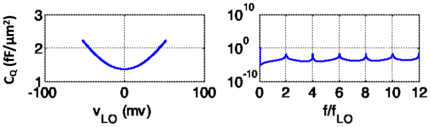
Figure 6.6: Nonideal varactor model.

pumping signal at zero-bias. Unlike the MOS-based varactor case, as C_Q exhibits a symmetric behaviour with the applied voltage, this eliminates the odd harmonics including the fundamental LO frequency, f_{LO}, and generates the even harmonics including S_0 as shown in Fig. 6.7.

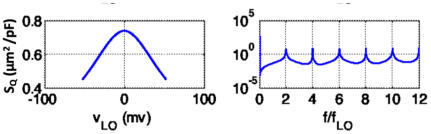
Accordingly, the odd phasor representations of $S(t)$ are neglected in the case of



(a) LO pumping signal with P_{LO} of 0 dBm in the time and in the frequency domain.



(b) Simulated C_Q response versus the applied LO signal in Fig. 6.7a and its frequency domain components.



(c) Simulated $S(t)$ response versus the applied LO signal in Fig. 6.7a and its frequency domain components.

Figure 6.7: Quantum capacitance and elstance behaviour with pumping LO signal.

C_Q at zero-bias condition. At higher bias voltages such that $V_{DC} >> k_B T/e$, (6.11) is reduced to:

$$C_Q(v) \approx \frac{2e^3}{\pi(\hbar\nu_F)^2} v, \tag{6.18}$$

which shows a linear relation of the quantum capacitance value with the applied voltage. Therefore, the odd harmonics are not negligible for nonzero DC bias.

Fig. 6.8 shows the plot of the simulated values of S_0, S_1, and S_2 for different bias points and different LO powers. From Fig. 6.8 some observations are highlighted as follow:

- S_0 exhibits its maximum values at zero-bias. This agrees with the excellent performance of graphene-based power detectors based on both MIG diodes presented in *section 4.2*, and GFETs operated beyond their f_T and f_{max}, as presented in *section 2.2*.

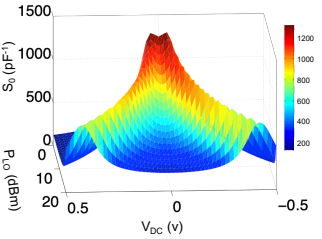
- At zero-bias S_1 is negligible, whereas S_2 is not.

- For bias voltages higher than $k_B T/e$, the quantum capacitance changes linearly with the applied voltage. Therefore, S_2 might be neglected compared to S_1 due to the nature of the applied LO signal as shown in Fig. 6.7a.

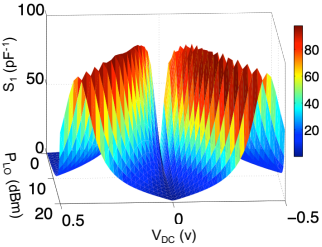
- For low pumping powers, the harmonics of the elastance roll off quickly compared to S_0 and vice versa.

- It has been shown in [120] that Q_F above 100 and C_r above 2 could be achieved for quantum capacitors by reducing the effective oxide thickness (EOT).

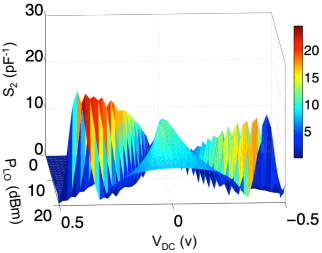
Based on the above conservations, the quantum capacitance unique behaviour with bias together with the achievable high quality-factor and tunning range promote it to be employed in parametric circuits to exploit these features as will be shown in the next section.



(a) Simulated values of S_0 for different bias voltages and LO power levels, P_{LO}.



(b) Simulated values of S_1 for different bias voltages and LO power levels, P_{LO}.



(c) Simulated values of S_2 for different bias voltages and LO power levels, P_{LO}.

Figure 6.8: S_0, S_1, and S_2 for different bias voltages and LO drive levels, P_{LO}.

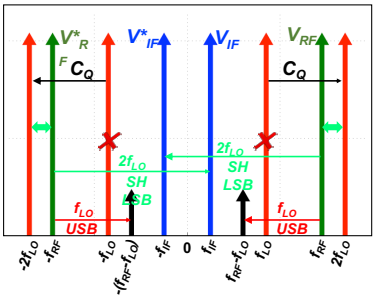


Figure 6.9: Frequency components of the subharmonic lower-sideband PAMP.

6.3 Parametric circuit design and simulations

Many studies have been carried out to find a compromise between a positive CG and relaxing the LO requirements. In [125] the integer-upper-sideband has been proposed by keeping the relations between f_{LO}, f_{RF}, and f_{IF} constant. Other approaches have been reported to enable a flexible choice of the frequencies while modifying the LO signal. Examples are the LO shaping using nonlinear transmission lines (NLTLs) in [126] and the dual-pumping in [127]. These solutions are necessary if CMOS or *pn*-diodes are employed in parametric circuits due to their C-V characteristics. Subharmonic pumping has been proposed in [124] for the cases of AMOS varactors and *pn*-diodes. However, the performance of the subharmonically pumped AMOS was poor compared to the conventional LSB PDC due to the C-V characteristics of the AMOS varactor. For the *pn*-diode, the circuit was not able to provide positive CG with subharmonic pumping. Conversely, for the case of graphene the gain is achievable even at $f_{LO}<f_{RF}$ due to the unique C-V behaviour of C_Q. The properties of the graphene C_Q at zero-bias turn the USB PAMP configuration to a Sub-Harmonic (SH) LSB PAMP under the condition $f_{RF}/2 <f_{LO}<f_{RF}$. This is due to the generation of the second harmonic and suppression of the fundamental LO frequency, f_{LO}, under zero-bias conditions as shown in Fig. 6.9. In addition, there is no need for extra DC input. Fig. 6.10 shows the equivalent circuit of the proposed topology with $f_{IF} = 2f_{LO} - f_{RF}$.

The mathematical explanation of this SH LSB PAMP is presented starting

by the small-signal voltage on the varactor which is represented by:

$$v_{ss}(t) = v_{RF}(t) + v_{IF}(t), \tag{6.19}$$

which is expressed as:

$$v_{ss}(t) = \frac{1}{2}(V_{RF}e^{j\omega_{RF}t} + V_{RF}^{*}e^{-j\omega_{RF}t} + V_{IF}e^{j\omega_{IF}t} + V_{IF}^{*}e^{-j\omega_{IF}t}). \tag{6.20}$$

The same is valid for the small-signal current

$$i_{ss}(t) = i_{RF}(t) + i_{IF}(t), \tag{6.21}$$

which is expressed as:

$$i_{ss}(t) = \frac{1}{2}(I_{RF}e^{j\omega_{RF}t} + I_{RF}^{*}e^{-j\omega_{RF}t} + I_{IF}e^{j\omega_{IF}t} + I_{IF}^{*}e^{-j\omega_{IF}t}). \tag{6.22}$$

Then, for a zero-bias quantum capacitance, with pumping signal at f_{LO}, the elastance is approximately expressed by:

$$S(t) = S_0 + S_2e^{j2\omega_{LO}t} + S_2^{*}e^{-j2\omega_{LO}t}, \tag{6.23}$$

Now, applying (6.20), (6.22), and (6.23) in (6.14) and ignore the resulting components at $2\omega_{LO} + \omega_{RF}$ and $2\omega_{LO} + \omega_{IF}$. By additionally considering only one single side-band for simplicity, as shown in Fig. 6.9, it is possible to express the voltages at RF and IF as follows:

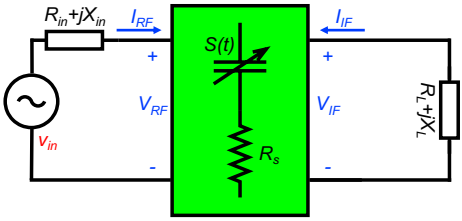


Figure 6.10: SH LSB PAMP equivalent circuit.

$$V_{RF} = I_{RF}\left(R_s + \frac{S_0}{j\omega_{RF}}\right) + I_{IF}^{*}\frac{S_2}{j\omega_{RF}} \tag{6.24}$$

$$V_{IF}^{*} = I_{RF}\frac{-S_2}{j\omega_{IF}} + I_{IF}^{*}\left(R_s - \frac{S_0}{j\omega_{IF}}\right). \tag{6.25}$$

Therefore, the conversion matrix is:

$$\begin{bmatrix} V_{RF} \\ V_{IF}^{*} \end{bmatrix} = \begin{bmatrix} R_s + \dfrac{S_0}{j\omega_{RF}} & \dfrac{S_2}{j\omega_{RF}} \\ \dfrac{-S_2}{j\omega_{IF}} & R_s - \dfrac{S_0}{j\omega_{IF}} \end{bmatrix} \begin{bmatrix} I_{RF} \\ I_{IF}^{*} \end{bmatrix}. \tag{6.26}$$

Applying the loop expressions for the RF and IF sides in Fig. 6.10 the resulting equations are:

$$V_{RF} = v_{in} - Z_{in} I_{RF} \tag{6.27}$$

$$V_{IF}^{*} = -Z_L^{*} I_{IF}^{*}. \tag{6.28}$$

Assuming that the output matching network is tunned to f_{IF}, the power of the downconverted signal, P_{IF}, is given by:

$$P_{IF} = \frac{1}{2}\left|I_{IF}\right|^2 R_L, \tag{6.29}$$

while, the input RF power, P_{RF}, is

$$P_{RF} = \frac{v_{in}^2}{8R_{in}}. \tag{6.30}$$

Using (6.26) to (6.30), the gain at the IF terminal is given by:

$$G_{IF} = \frac{4R_L R_{in}\left|S_2\right|^2}{\left[\omega_{RF}(R_L + R_s)(R_{in} + Rs) - \dfrac{\left|S_2\right|^2}{\omega_{IF}}\right]^2}. \tag{6.31}$$

For noise calculations, the varactor loss, R_s, contributes with the thermal noise e^2_{n,R_s} such that

$$e^2_{n,R_s} = 4kTR_s\Delta f. \tag{6.32}$$

Similarly, the source resistance, R_{in}, contributes with $e^2_{n,R_{in}}$ such that

$$e^2_{n,R_{in}} = 4kTR_{in}\Delta f. \tag{6.33}$$

Therefore, the overall noise factor of the PAMP in Fig. 6.10 is expressed as:

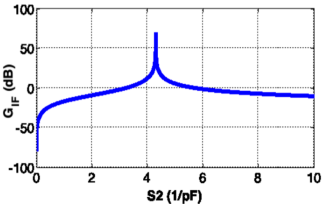
$$F_{IF} = 1 + \frac{e^2_{n,R_s}}{e^2_{n,R_{in}}} + \frac{e^2_{n,R_s}}{e^2_{n,R_{in}} \cdot \left[\dfrac{\left|S_2\right|}{\omega_{RF}(R_{in}+Rs)}\right]^2}. \tag{6.34}$$

It is clear that the gain (6.31) and the noise factor (6.34) are the same as in the standard LSB PAMP replacing S_1 by S_2 in this case. However, the used pumping LO signal frequency, f_{LO} is doubled thanks to the quantum capacitance of graphene. Consequently, the use of graphene quantum capacitance in LSB PAMP configuration achieves the same gain and noise performance of the USB PAMP with half of the f_{LO}.

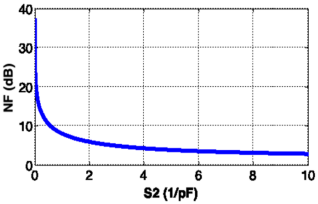
To understand the design challenges and design optimisation based on (6.31) and (6.34), Matlab simulations are carried out. Fig. 6.11 illustrates G_{IF} and Noise Figure (NF) versus S_2. The simulations shown in Fig. 6.11 demonstrate maximum G_{IF} of 70.2 dB at S_2 of 4.3 pF^{-1} with an associated NF of 4 dB when setting the RF frequency to 29 GHz, IF frequency to 5 GHz, LO frequency to 17 GHz, $R_{in} = 50\,\Omega$, $R_L = 50\,\Omega$, and $R_s = 10\,\Omega$.

Interestingly, it is shown in Fig. 6.11 that there are two values of S_2 to achieve the same G_{IF}. The higher value of S_2 corresponds to a lower NF and, thus, better noise performance at the cost of higher pumping power.

To reduce the NF further, another Matlab simulation is carried out at the



(a) Matlab simulations of G_{IF}.

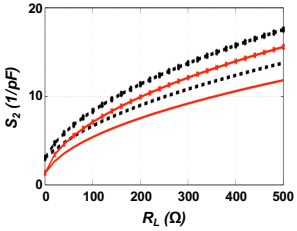


(b) Matlab simulations of NF.

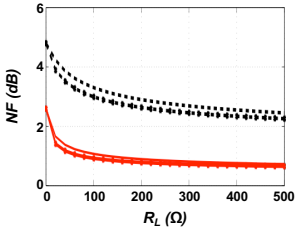
Figure 6.11: G_{IF} and NF versus S_2.

same frequencies to understand the significance of R_L and the varactor losses represented by R_s. Fig 6.12a shows the required S_2 to maintain G_{IF} of 10 dB for an R_{in} of 50 Ω. Fig 6.12a shows again that the gain could be satisfied by two values of S_2, whereas the higher value corresponds to a lower NF as shown in Fig 6.12b. The simulations are done for two values of R_s, where the dotted plots represent results with $R_s = 30\,\Omega$, the solid plots show the results if R_s is reduced to 5 Ω. It is obvious that R_s sets the minimum achievable NF. In addition, the required S_2 to sustain G_{IF} is higher for the larger R_s which again implies a higher pumping power.

To realise the SH LSB PAMP downconverter, a behavioural model of C_Q of graphene is shown in Fig. 6.13. The model coefficients are obtained by the means of least-squares curve fitting method according to the measured C-V



(a) Matlab simulations of S_2.



(b) Matlab simulations of NF.

Figure 6.12: S_2 and NF versus R_L for two values of R_s.

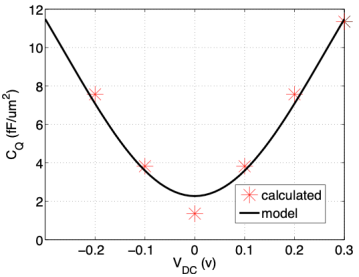


Figure 6.13: C_Q behaviour model compared to the calculated values from measurements.

dependency of the MIG diode in Fig. 3.12 in *chapter 3* considering the diode area and the series resistance.

The model is utilized in the design shown in Fig. 6.14. The common-mode feed of the pumping signal LO reduced significantly the LO feedthrough to the IF output and the LO leakage at the RF input as shown in Fig. 6.14. L_{DC} together with the centre-tapped IF transformer ensure zero DC bias of the diode. C_{RF} and the RF transformer are tuned at f_{RF}, while C_{IF} and the IF transformer are tuned at f_{IF}. The capacitance, C_{block}, AC couples the common-mode LO and the differential RF signals without disturbing the DC operation point of the varactor.

Harmonic Balance (HB) simulations are carried out using ADS from Keysight®.

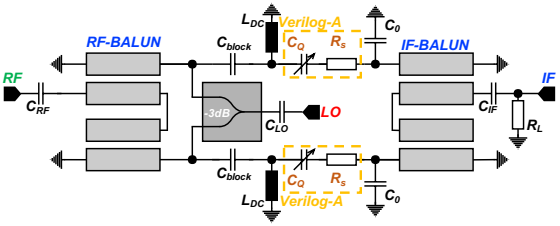
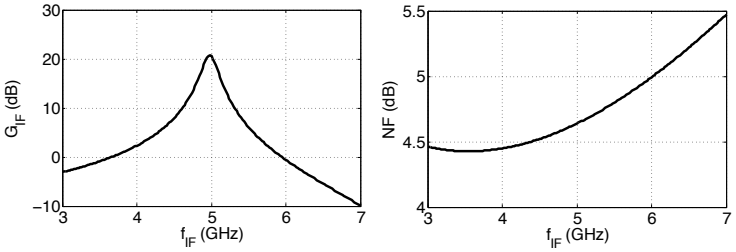


Figure 6.14: Schematic of the proposed SH LSB PAMP downconverter.

Table 6.1: Values of the lumped components of the proposed SH LSB PAMP

Component	C_{RF}	C_{block}	C_0	C_{LO}	C_{IF}	L_{DC}
Value	0.7 pF	1.3 pF	0.9 pF	1.2 pF	2.9 pF	1.8 nH



(a) Conversion Gain. (b) Noise Figure.

Figure 6.15: HB simulation results.

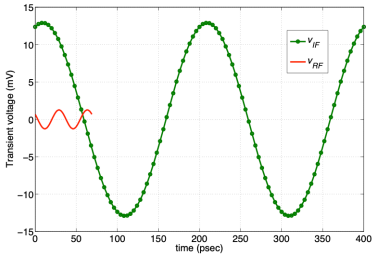


Figure 6.16: ADS transient IF and RF voltage signals.

Values of the lumped passive components optimised for the operating frequencies are listed in Table. 6.1. Simulations are carried out for an RF frequency of 29 GHz, an IF of 5 GHz, with the LO frequency of 17 GHz. The optimum calculated value of S_2 is 6.7 pF^{-1}. The value of S_2 is obtained using a P_{LO} of 3.5 dBm for a diode area of 280 μm^2. The estimated value for R_s is 20 Ω, and the optimum R_L is 90 Ω. The calculated G_{IF} is 23 dB with a NF of 3.8 dB.

The resulting G_{IF} and NF are shown in Fig. 6.15. Compared to the analysis in (6.31) and (6.34), the simulated and calculated values show good agreement for the G_{IF}. For the NF, simulation results demonstrate a 1-dB discrepancy originating from the imperfect tunning of the passive filters in addition to ignoring the noise generated by the load resistance, R_L, in (6.34). Transient voltages of the IF and RF voltage signals show the pronounced gain as shown in Fig 6.16.

6.4 Summary and conclusion

In this chapter, the parametric circuit exploiting the unique properties of the quantum capacitance of graphene has been introduced for the first time. The unique characteristics of C_Q are used to build a distinct RF-powered, subharmonic lower-sideband parametric amplifier without the need for bias voltages. The C_Q enables a distinct LSB PAMP which achieve the same gain and noise behaviour of the upper-sideband parametric amplifier with relaxed LO requirements.

C_Q and its equivalent elastance have been analyzed in both the time and the frequency domains. The analysis shows the potential for the graphene C_Q to be employed in parametric circuits due to its high operating frequency, wide tunning range and excellent quality factor. These properties promote the use of graphene C_Q to build millimetre-wave circuits with positive conversion gain and optimised noise performance.

The presented circuit technique exploiting the C_Q of graphene could employ GFETs or MIG diodes. However, the diode has higher potential due to its physical structure.

The PAMP scheme provides a solution to build receivers and transmitters based on graphene devices avoiding the limitations of the GFETs while providing adequate gain required for employing the circuit in commercial and biomedical applications.

Chapter 7

Summary, Conclusions, and Outlook

7.1 Thesis summary

This dissertation outlines the research started in 2013 after nine years of discovering the field effect in graphene [1]. The main target of this research was to investigate the possibilities to implement high frequency circuits using graphene-based active devices by exploiting the outstanding electrical and mechanical properties of graphene.

In 2013 the status of graphene-based devices was the demonstration of GFETs

with poor frequency properties which were far from the expected performance. The research started by building a thin-film technology with a recipe that could be implemented on different substrates. This technology is integrated along side with the available GFET based on CVD-graphene to ensure the repeatability and controllability crucial for device modeling [88]. Due to the immaturity of available devices and processes, it was decided to pursue two paths: the first was on circuit techniques, *i.e.* by investigating different approaches to build circuits and systems that exploit the properties of the existing GFETs. The second concentrated on the active device itself. This work started by studying the ways on implementing graphene-based diodes. By 2015, the thin-film MMIC technology was established, and the main achievement of this work represented by the CVD MIG diode is realised. The MIG diode exploits the electrical properties of graphene. In addition, the physical design of the MIG diode considers the frequency characteristics of the device. Thenceforth, the MMIC technology was modified to include the MIG diode into the process. The developed MIG diode is considered a big step in the evolution of graphene technology for high frequency applications. Later in 2016 and 2017, the exceptional properties of the MIG were employed in microwave, and millimetre-wave circuits by exploring the MIG diode in circuit topologies as the six-port receivers, the parametric amplifier circuits, and DRL gates.

To understand the progress of the development achieved in the graphene technology, the evolution of semiconductor materials time is listed in Table. 7.1. In 1914 the solid-state materials were classified according to their conductivity into three classes: metals, insulator, and *variable conductors*. It took decades to realise reliable devices with poor frequency properties compared to the existing, well established semiconductor technologies like Si and III-V materials.

This dissertation started in *chapter 1* by showing the motivation on doing research about employing graphene-based devices to build high frequency circuits and systems on different substrates. Accordingly, the outstanding properties are listed and compared to other existing semiconductor technologies. Then the methods used to prepare graphene have been shown focusing on the methods that are mostly used to produce devices. Then a comparison between these approaches is shown from the perspective of a high frequency circuit designer.

Table 7.1: Evolution of Semiconductors

1782	First time to use the term "*Semiconductor*" by Alessandro Volta
1833	Semiconductor effect observation by Michael Faraday
1851	Metal/Semiconductor electrical conductivity temperature dependency
1878	Hall effect
1899	Positive and negative charge carriers proposal
1904	Patent for PbS point-contact rectifiers
1914	Solid-state new classification: variable conductors
1928	Bloch developed the theory of electrons in lattices
1929	W. Schottky confirmed the barrier in a metal-semiconductor junction
1930	Patents for device resembling today's metal–semiconductor field-effect transistor (MESFET)
1931	Concept of hole developed by Heisenberg
1933	Patents for device resembling today's MOSFET
1934	Capacitive control in field-effect transistors
1938	W. Schottky developed potential barrier model in metal-semiconductor junction
1942	Hans Bethe developed the theory of thermionic emission
1948	Bipolar Junction Transistor (BJT)
1952	The first grown junction transistors
1954	BJT with f_T of 500 MHz
1955	First Si transistor
1958	First Integrated Circuit (IC) by Kilby
1963	The first CMOS circuit was proposed by Frank Wanlass

Thenceforth, in *chapter 2*, the main achieved milestones in the fabrication of high performance GFETs are discussed showing the development for the devices fabricated with graphene prepared according to the previously discussed preparation schemes.

The employment of GFETs in different circuit applications is expressed and compared highlighting the advantages and challenges of using GFETs.

Based on the status of GFETs and the circuits that could be implemented by employing GFETs, a conclusion is reached such that a new device is required to solve the issues that the existing GFETs could not achieve.

The attempts to realise a graphene-based diode device are shown in *chapter 3*, till the MIG diode is developed. This diode is the main contribution of this work. Theory of operation, fabrication, physical implementation consideration, DC and AC characterisations are shown comprehensively. A small-signal model has been extracted and compared to the measurement results.

The following step was to prove the capabilities of the invented diode by employing it in circuits that uses the MIG diode properties which substantially advance the performance achieved by relevant circuits relying on the state-of-the-art GFETs. Moreover, MIG diode circuits also outperform the performance achieved by circuits implemented using other competitive semiconductor technologies.

To be able to implement such circuits using MIG diodes, a thin-film MMIC technology was established to integrate the MIG diodes alongside with the process steps and share the mask set with passives as shown in *section 4.1*. The rest of *chapter 4* expressed the designed, fabricated, and measured circuits as mixers, power detects, DRL gates.

In *chapter 5*, the six-port receiver concept has been introduced to build graphene-based receivers without the adherence to A_V, f_T, and f_{max} limitations in GFETs receiver implementations in literature.

In *chapter 6*, For the first time, to the best of the author's knowledge, the PAMP concept is introduced to employ the quantum capacitance of graphene to realise RF-powered receiver and transmitter frontends with conversion gain

and adequate noise behaviour in graphene-based technology. The elastance concept is applied to the C_Q, analyzed and employed in a proposed parametric downconversion circuit with simulated 10 dB gain and 5.5 dB noise figure.

7.2 Conclusions

The presented MIG with its outstanding and distinct properties enables the implementation of microwave and millimetre-wave circuits on different substrates including mechanically flexible ones. The usage of CVD graphene in the presented technology ensures the repeatability and reproducibility of the fabricated active devices. Accordingly, large-signal and small-signal models are extracted from measurements and are employed in the circuit design. The presented thin-film technology including few mask sets empowered the implementation of complex circuits and systems at low production cost. The concept of the six-port together with MIG diodes as power detectors provide a flexible solution to build receiver frontends alongside with different substrates and for different frequency ranges. The MIG diode can be used in parametric circuits to build the canonical function of receiver and transmitter frontends providing positive conversion gain and optimised noise performance. Exploiting the graphene quantum capacitance in parametric downconversion circuits result in distinct topology which was not achievable with other semiconductor technologies. The flexibility and robustness of the presented technology integrating MIG diodes alongside with high quality passives promote the use of graphene in smart wearables and flexible electronics for biomedical and communications applications which is the main motivation to do research on graphene.

7.3 Outlook

The research in graphene is still in the early phases and there are many aspects to be explored in the future.

The MIG diode full-fledged model including large-signal, small-signal, and noise behaviour is to be implemented and verified by more characterisation

including noise measurements. In addition, the physical design might be investigated more to improve the capacitance tuning range and quality factor. Interestingly, these improvements would allow the design of high performance PAMPs featuring upconversion, downconversion, and amplification. Other circuit applications would also make use of the MIG diode as RFID, NFC, and IoT for biomedical and communications usages.

The development in GFET devices should also be continued. In this dissertation the difference of each achieved milestone has been shown in the evolution of graphene technology. In addition, novel circuit techniques should be investigated to make use of the GFET keeping in mind their unique properties other than using them in circuit schemes that were invented for the use of CMOS for example.

Another promising device is the graphene-based heterostructures [128–132]. The major improvement is regarding the transistor switching off in addition to the expected substantial improved frequency characteristics [133] compared to the GFET device concept. The research in these heterostructures might lead to the implementation of graphene-based HEMTs. Circuits employing these graphene-based, heterostructures tunneling transistors have to be implemented.

The concept of PAMP is to be examined extensively in other configurations to proof the concept of employing the value and uniqueness of the quantum capacitance of graphene in this topology.

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List of Abbreviations and Symbols

A_V . . . . . .voltage gain

C_Q . . . . . .Quantum capacitance

C_r . . . . . .Capacitance Tunning range

E_G . . . . . .Energy gap

E_{eff} . . . . . .effective electric field

I_{DS} . . . . . .drain-source current

J . . . . . .current density

P_{IF} . . . . . .Intermediate Frequency Power

P_{LO} . . . . . .LO Power

P_{RF} . . . . . .RF Power

P_{out} . . . . . .Output Power

Q_F . . . . . .Quality factor

R_C . . . . . .Contact Resistance

R_{DS} . . . . . .Drain-Source resistance

V_{DS} . . . . . .Drain-Source Voltage

V_{GS} . . . . . .gate-source voltage

f_{IF} . . . . . .IF frequency

f_{LO} . . . . . .LO Frequency

f_{RF} . . . . . .RF Frequency

f_T . . . . . .cutoff frequency

f_c . . . . . .Cutoff Frequency

f_{idler} . . . . . .PAMP Output Frequency

f_i . . . . . .Input Frequency

f_{max} . . . . . .maximum frequency of oscillation

f_p . . . . . .Pumping Frequency

g_{DS} . . . . . .drain-source conductance

g_m . . . . . .Mutual Transconductance

m^*/m_0 . . . . . .effective mass

r_{DS} . . . . . .Small-signal Drain-Source Resistance

v_{peak} . . . . . .peak velocity

AC . . . . . .alternate current

ADC . . . . . .Analogue-to-Digital Converter

ADS . . . . . .Advanced Design System

AFM . . . . . .Atomic Force Microscope

AGC . . . . . .automatic gain control

ALD . . . . . .atomic layer deposition

AM . . . . . .amplitude modulation

Ar . . . . . .Argon

ASK . . . . . .amplitude shift keying

BEOL . . . . . .Back-End-Of-Line

BG . . . . . .back gate

BJT . . . . . .Bipolar Junction Transistor

CDMA . . . . . .Code Division Multiple Access

CE . . . . . .Common-Emitter

CG . . . . . .Common Gate

CH_4 . . . . . .Methane

CL . . . . . .Conversion Loss

CMOS . . . . . .Complementary Metal Oxide Semiconductor

CNT . . . . . .Carbon Nanotubes

CS . . . . . .Common Source

Cu . . . . . .Copper

CVD . . . . . .Chemical Vapor Deposition

DC . . . . . .direct current

DECT . . . . . .Digital Enhanced Cordless Telecommunications

DLC . . . . . .Diamond-Like Carbon

DR . . . . . .Dynamic Range

DRL . . . . . .Diode-Resistor Logic

DSP . . . . . .Digital Signal Processing

DTL . . . . . .Diode-Transistor Logic

EM . . . . . .Electromagnetic

EOT . . . . . .effective oxide thickness

EVM . . . . . .error vector magnitude

FOM . . . . . .Figure-of-merit

FOMs . . . . . .Figure-of-merits

GaAs . . . . . .Gallium Arsenide

GaN . . . . . .Gallium Nitride

Ge . . . . . .Germanium

GFET . . . . . .graphene field effect transistor

GOM . . . . . .Graphene-Oxide-Metal

GPIB . . . . . .General Purpose Interface Bus

GSM . . . . . .Global System for Mobile communications

H_2 . . . . . .Hydrogen

HB . . . . . .Harmonic Balance

HEMT . . . . . .High Electron Mobility Transistor

HRS . . . . . .High Resistivity Silicon

HWR . . . . . .Half-Wave Rectifier

IC . . . . . .Integrated Circuit

IF . . . . . .Intermediate Frequency

InAs . . . . . .Indium Arsenide

InP . . . . . .Indium Phosphate

IoT . . . . . .Internet of Things

LNA . . . . . .Low-Noise Amplifier

LO . . . . . .Local Oscillator

LPF . . . . . .Low-Pass Filter

LSB . . . . . .Lower-Sideband

MESFET . . . . . .metal–semiconductor field-effect transistor

MIG . . . . . .Metal Insulator Graphene

MIM . . . . . .Metal Insulator Metal

MMIC . . . . . .Monolithic Microwave Integrated Circuit

MOS . . . . . .metal-oxide-semiconductor

MOSFET . . . . . .Metal-Oxide-Semiconductor FET

MWC . . . . . .Mobile World Congress

NF . . . . . .Noise Figure

NFC . . . . . .Near Field Communications

Ni . . . . . .Nickel

NLTLs . . . . . .nonlinear transmission lines

NW . . . . . .nanowire

OFDM . . . . . .Orthogonal Frequency Division Multiplexing

PA . . . . . .power amplifier

PAMP . . . . . .Parametric Amplifier

PC . . . . . .Personal Computer

PCB . . . . . .Printed Circuit Board

PET . . . . . .Polyethylene terephthalate

PMMA . . . . . .Poly Methyl Methacrylate

Pt . . . . . .Platinum

QAM . . . . . .Quadrature Amplitude Modulation

QPSK . . . . . .Quadrature Phase Shift Keying

RF . . . . . .Radio Frequency

RFID . . . . . .Radio Frequency Identification

RIE . . . . . .Reactive Ionic Etching

RMS . . . . . .Root Mean Square

ROM . . . . . .Read-Only Memory

SBH . . . . . .Schottky barrier hight

SEM . . . . . .scanning electron microscope

SH . . . . . .Sub-Harmonic

Si . . . . . .Silicon

SiC . . . . . .Silicon Carbide

SLG . . . . . .single layer graphene

SNR . . . . . .Signal-to-Noise Ratio

TG . . . . . .top gate

TL . . . . . .Transmission Line

TSS . . . . . .tangential signal sensitivity

TTL . . . . . .Transistor-Transistor Logic

USB . . . . . .Upper-Sideband

VBW . . . . . .Video Bandwidth

VNA . . . . . .Vector Network Analyzer

WLAN . . . . . .Wireless Local Area Network

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10/2017	Best young research paper finalist IEEE European Microwave Conference
06/2019	Best student paper finalist IEEE International Microwave Symposium

List of Publications

Peer Reviewed Journal Articles

[J1] E. Bayram, A. F. Aref, M. Saeed, and R. Negra. „1.5-3.3 GHz, 0.0077 mm^2, 7 mW All-Digital Delay-Locked Loop With Dead-Zone Free Phase Detector in 0.13μm CMOS“. in: *IEEE Transactions on Circuits and Systems I: Regular Papers* 65.1 (Jan. 2018), pp. 39–50. ISSN: 1549-8328. DOI: 10.1109/TCSI.2017.2715899.

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The burgeoning development in the recent communications standards associated with the evolutionary research in new materials result in the arise of new applications. Particularly, two-dimensional (2D) materials have attracted great attention due to their flexibility, ability of integration alongside with different substrates which is convenient for applications such as Radio Frequency Identification (RFID),Near Field Communications (NFC), Internet of Things (IoT) that could be utilised in flexible electronics, and smart wearables for biomedical purposes and wireless communications. Graphene is one promising candidate among the family of 2D materials due to its outstanding electrical and mechanical properties, together with the ability for large scale integration on different substrates make graphene a perfect candidate for Radio Frequency (RF), millimetre-wave , and submillimetrewave circuit applications.The goal of this work is to realise a graphene-based device that directly exploits the properties of graphene and enables the realisation of different circuit applications. In this regard, I present a Back End Of Line (BEOL) MMIC, thin-film technology integrating graphene diode alongside with high quality passives.The capabilities of the presented technology together with the graphene diode are demonstrated by designing different circuits.