Two Dimensional Materials-Based Vertical Heterojunction Devices for Electronics, Optoelectronics and Neuromorphic Applications

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Abstract

Advancement of digital microelectronics relied for decades on the classical scaling philosophy guided by the famous evolutionary trend known as “Moore’s law”. However, a slowdown of this relentless device scaling is becoming inevitable due to fundamental physical limits. This led to the rise of a new strategy called “more than Moore (MtM)” that targets on integrated circuit functionality diversification by promoting novel non-digital (analog) applications such as radio-frequency (RF) electronics, power management systems, optoelectronics, sensors, micro/nano electromechanical systems, next generation computing systems, etc. This strategy requires new device concepts and novel materials outperforming conventional ones. Novel two-dimensional (2D) materials such as graphene and molybdenum disulfide (MoS_2) are suitable for MtM applications due to their unique structural, electrical and optical properties. In line with the MtM goals, this thesis investigates vertical hybrid devices based on graphene, MoS_2 and their heterostructures integrated into conventional 3D silicon (Si) for applications toward RF electronics, optoelectronics and neuromorphic computing. The fabrication schemes used here are scalable and semiconductor process technology compatible.

The primary milestone in this thesis has been the investigation of the potential of MoS_2 as the emitter diode of graphene-base hot electron transistors (GBTs). GBTs are promising devices for high-speed analog electronics and they have a vertical architecture comprising a Si-emitter, a graphene-base and a metal-collector, each isolated by a thin barrier. Maximizing the performance of GBTs requires efficient hot-electron injection across the emitter-base-barrier. Theory suggests that this can be realized by using semiconducting barrier materials that form low energy barriers to promote thermionic emission. MoS_2 is a good candidate in this regard owing to its semiconducting behavior with a bandgap and electron affinity values enabling band alignments providing a small barrier with respect to the Si-emitter. Hence, “Si/MoS_2/Metal” vertical heterojunction devices were investigated us-

ing capacitance-voltage (C-V) and conductance-voltage (G-V) techniques. The static dielectric constant of MoS_2 is obtained from the measured C-V data. Measurements under electric-field stress, verified by analytical simulations, have indicated the presence of interface states and mobile negative ions in MoS_2. This observation was further supported by time-of-flight secondary ion mass spectroscopy analysis that showed hydroxyl ions (OH^-) possibly originating from catalytic water splitting by MoS_2. Furthermore, transmission electron microscopy studies reveal the structural properties of the film including its polycystallinity with vertically aligned layers. Next, charge carrier transport properties were investigated across "n^+-Si/MoS_2/Graphene" vertical heterojunction diodes analogous to the emitter diodes of GBTs. Analyses of the measured temperature dependent I-V data in corroboration with analytical models confirmed that the electron transport across the n^+-Si/MoS_2 heterojunction barrier is dominated by thermionic emission. This fulfils the prerequisites for using MoS_2 as the emission barrier of GBTs.

The thesis also includes experiments on the "Si/MoS_2/Metal" vertical heterojunctions for memristive switching. Static (DC) current-voltage (I-V) and resistive switching (RS) characterizations including endurance and state-retention tests demonstrate the memristive functionality of the devices. The switching tests exhibit a bipolar and non-volatile RS behavior with encouraging endurance and state retention for at least 140 DC switching cycles and 2500 seconds, respectively. Controlled C-V, G-V and switching measurements in ambient and vacuum conditions, elucidated by analytical simulations, suggest that the observed RS behavior is due to electric field-driven movements of the mobile OH^- ions along the vertical MoS_2 layers and their influence on the potential barrier at the Si/MoS_2 interface.

In addition, electro-optical characterizations, in particular I-V measurements with and without white light illumination and spectral responsivity (SR) measurements, were carried out on vertical "n^+-Si/MoS_2/Graphene" heterojunction diodes, which exhibit broadband optical sensitivity. The SR data feature multiple peaks in the ultraviolet and visible regions indicating that the measured photocurrent is mainly due to excitations in the MoS_2. In addition, an infrared response is observed for energies below the Si and MoS_2 bandgaps. This may be attributed to absorption in the graphene and/or inter-layer transitions in a staggered band alignment or absorptions via midgap states in the MoS_2

bandgap. In conclusion, the work and findings in this thesis can serve as a guideline for integrating 2D materials and their heterostructures into the existing Si platform to create hybrid heterojunction devices for potential electronic, optoelectronic and neuromorphic applications.

Zusammenfassung

Der Fortschritt in der digitalen Mikroelektronik beruhte jahrzehntelang auf der klassischen Skalierungsphilosophie nach dem "Moore'schen Gesetz". Eine Verlangsamung dieser unerbittlichen Skalierung der Bauteile ist aufgrund grundlegender physikalischer Grenzen jedoch unvermeidlich geworden. Dies führte zur Entwicklung einer neuen Strategie mit der Bezeichnung "More than Moore (MtM)", die auf die Diversifizierung der Funktionalität integrierter Schaltkreise abzielt, indem neuartige nicht-digitale (analoge) Anwendungen gefördert werden, wie z. B. Hochfrequenzelektronik (HF), Leistungsmanagementsysteme, Optoelektronik, Sensoren, mikro-/nano elektromechanische Systeme, Computersysteme der nächsten Generation usw. Diese Strategie erfordert neue Bauelementekonzepte und neuartige Materialien, die den herkömmlichen überlegen sind. Neuartige zweidimensionale (2D) Materialien wie Graphen und Molybdändisulfid (MoS_2) sind aufgrund ihrer einzigartigen strukturellen, elektrischen und optischen Eigenschaften für MtM-Anwendungen geeignet. Im Einklang mit den MtM-Zielen werden in dieser Arbeit vertikale hybride Bauelemente auf der Basis von Graphen, MoS_2 und deren Heterostrukturen untersucht, die auf konventionellem 3D-Silizium (Si) integriert werden, um Anwendungen in der HF-Elektronik, Optoelektronik und im neuromorphen Computing zu ermöglichen. Die hier verwendeten Herstellungsverfahren sind skalierbar und mit der Halbleiterprozesstechnologie kompatibel.

Der wichtigste Meilenstein in dieser Arbeit war die Untersuchung des Potenzials von MoS_2 als Emitterdiode von Heißen-Ladungsträger-Transistoren (GBTs) auf Graphenbasis. GBTs sind vielversprechende Bauelemente für analoge Hochgeschwindigkeitselektronik und haben eine vertikale Architektur, die einen Si-Emitter, eine Graphen-Basis und einen Metall-Kollektor umfasst, die jeweils durch eine dünne Barriere isoliert sind. Die Maximierung der Leistungsfähigkeit von GBTs erfordert eine effiziente Injektion heißer Elektronen über die Emitter-Basis-Grenze. Die Theorie legt nahe, dass dies durch die Verwendung

von halbleitenden Barrierematerialien erreicht werden kann, die niedrige Energiebarrieren bilden, um die thermionische Emission zu fördern. MoS_2 ist in dieser Hinsicht ein guter Kandidat, da es ein halbleitendes Verhalten mit einer Bandlücke und Elektronenaffinitätswerten aufweist, die zu kleinen Barrieren zum Si-Emitter führen. Daher wurden vertikale Si/MoS_2/Metall-Heteroübergangs-Bauelemente mit Hilfe von Kapazitäts-Spannungs- (C-V) und Leitwert-Spannungs-Techniken (G-V) untersucht. Die statische Dielektrizitätskonstante von MoS_2 wurde aus den gemessenen C-V-Daten ermittelt. Messungen unter elektrischer Feldbelastung, verifiziert durch analytische Simulationen, haben Grenzflächenzustände und mobile negative Ionen in MoS_2 nachgewiesen. Diese Beobachtung wurde außerdem durch eine Flugzeit-Sekundärionen-Massenspektroskopie-Analyse unterstützt, die Hydroxyl-Ionen (OH^-) zeigte, die möglicherweise aus der katalytischen Wasserspaltung durch MoS_2 stammen. Darüber hinaus zeigen Untersuchungen mittels Transmissionselektronenmikroskopie die strukturellen Eigenschaften des Films, einschließlich seiner Polykristallinität mit vertikal ausgerichteten Schichten. Anschließend wurden die Eigenschaften des Ladungsträgertransports in vertikalen "n^+-Si/ MoS_2/ Graphen" Heteroübergangsdioden analog zu den Emitterdioden von GBTs untersucht. Analysen der gemessenen temperaturabhängigen I-U-Daten bestätigten in Verbindung mit analytischen Modellen, dass der Elektronentransport über die n^+-Si/MoS_2-Heteroübergangsbarriere durch thermionische Emission dominiert wird. Damit sind die Voraussetzungen für die Verwendung von MoS_2 als Emissionsbarriere von GBTs erfüllt.

Die Arbeit umfasst auch Experimente zu den vertikalen "Si/MoS_2/Metall" Heteroübergängen für das memristive Schalten. Die Charakterisierung der statischen (DC) Strom-Spannungs-Kennlinien (I-V) und des Schaltverhaltens des Widerstands (RS), einschließlich Ausdauer- und Zustandsbeibehaltungstests, weist die memristive Funktionalität der Bauelemente nach. Die Schalttests zeigen ein bipolares und nichtflüchtiges RS-Verhalten mit vielversprechender Haltbarkeit und Zustandserhaltung für mindestens 140 DC-Schaltzyklen bzw. 2500 Sekunden. Kontrollierte C-V-, G-V- und Messungen des Schaltverhaltens unter Umgebungs- und Vakuumbedingungen, die durch analytische Simulationen unterstützt wurden, legen nahe, dass das beobachtete RS-Verhalten auf durch elektrische Felder angetriebene Bewegungen der mobilen OH^--Ionen entlang der vertikalen MoS_2-Schichten und deren Einfluss auf die Potenzialbarriere an der Si/MoS_2-Grenzfläche zurückzuführen ist.

Elektro-optische Charakterisierungen, wie beispielsweise I-V-Messungen mit und ohne Weißlichtbeleuchtung und Messungen der spektralen Empfindlichkeit (SR), weisen eine breitbandige optische Empfindlichkeit von vertikalen "n^+-Si/MoS_2/Graphen" Heteroübergangsdioden nach. Die SR-Daten weisen mehrere Peaks im ultravioletten und sichtbaren Bereich auf, was darauf hindeutet, dass der gemessene Photostrom hauptsächlich auf Anregungen im MoS_2 zurückzuführen ist. Darüber hinaus wird bei Energien unterhalb der Si- und MoS_2-Bandlücken eine Reaktion im Infrarotbereich beobachtet. Dies kann auf Absorption im Graphen und/oder Zwischenschichtübergänge in einer gestaffelten Bandanordnung oder auf Absorption über Zustände in der MoS_2-Bandlücke zurückgeführt werden. Zusammenfassend lässt sich sagen, dass die Arbeiten und Ergebnisse dieser Dissertation als Leitfaden für die Integration von 2D-Materialien und deren Heterostrukturen in die bestehende Si-Plattform dienen können, um hybride Heteroübergangs-Bauelemente für potenzielle elektronische, optoelektronische und neuromorphe Anwendungen zu schaffen.

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List of Acronyms & Abbreviations

IC	integrated circuit
Si	silicon
M/NEMS	micro/nano electro mechanical systems
2D	two-dimensional
3D	three-dimensional
h-BN	hexagonal boron nitride
Bi_2Te_3	bismuth telluride
MoS_2	molybdenum disulfide
$MoSe_2$	molybdenum diselenide
WS_2	tungsten disulfide
WSe_2	tungsten diselenide
BP	black phosphorus
TiS_2	titanium disulfide
$NbSe_2$	niobium diselenide
UV	ultraviolet
IR	infrared
THz	terahertz
TCE	transparent conductive electrode
LED	light emitting diode
CVD	chemical vapor deposition
SiC	silicon carbide
Pt	platinum
Ru	rubidium
Co	cobalt
Cu	copper
Ni	nickel

DRT	dry transfer
WT	wet transfer
ECD	electro-chemical delamination
WCE	wet-chemical etching
PMMA	polymethyl methacrylate
NaOH	sodium hydroxide
KOH	potassium hydroxide
H_2	hydrogen
HCL	hydrochloric acid
DI-water	de-ionized water
O_2	oxygen
$FeCl_3$	iron (III) chloride
IPA	isopropyl alcohol
TMDC	transition metal dichalcogenides
Mo	molybdenum
S	sulfur
VdW	van der Waals
PDMS	polydimethylsiloxane
PI	polyimide
PECVD	plasma-enhanced CVD
ALD	atomic layer deposition
MOCVD	metal-organic chemical vapor deposition
HDPCVD	high density plasma CVD
Ar	argon
VPS	vapor-phase sulfurization
TAC	thermal annealing conversion
MoO_3	molybdenum tri oxide
ME	mechanical exfoliation
PWCR	polymer-assisted wet chemical release
MIS	metal insulator semiconductor
MOS	metal oxide semiconductor
MIM	metal-insulator-metal
MOSFET	metal oxide semiconductor field effect transistor

C-V	capacitance-voltage
G-V	conductance-voltage
I-V	current-voltage
J-V	current density-voltage
AC	alternating current
DC	direct current
HF C-V	high-frequency C-V
DT	direct tunneling
FNT	Fowler-Nordheim tunneling
TAT	trap-assisted tunneling
RT	resonant tunneling
BTBT	band-to-band tunneling
TE	thermionic emission
SE	Schottky emission
FPE	Frenkel-Poole emission
TFETs	tunneling FETs
GBT	graphene-base hot electron transistor
GBHT	graphene-base heterojunction transistor
SLG	single layer graphene
EBI	emitter-base insulator
BCI	base-collector-insulator
HETs	hot electron transistors
CB	conduction band
VB	valence band
CBO	conduction band offset
QE	Quantum efficiency
IoT	internet of things
Memristors	memory resistors
RS	resistive switching
HRS	high resistance state
LRS	low resistance state
TMOs	transition metal oxides
CF	conductive filament
HF	hydrofluoric acid

Cr	chromium
Au	gold
RIE	reactive ion etching
STI	shallow trench isolation
CMP	chemical mechanical polishing
BOE	buffered oxide etchant
OM	optical microscopy (OM)
SEM	scanning electron microscopy
TEM	transmission electron microscopy
FIB	focused ion beam
AFM	atomic force microscopy
RAMAN	Raman Spectroscopy
ToF-SIMS	time-of-flight secondary ion mass spectroscopy
$\mathbf{Bi^+}$	bismuth ions
$\mathbf{OH^-}$	hydroxyl ions
Li^+	lithium ions
BS	bias-stress
+BS	positive bias-stress
-BS	negative bias-stress
SR	spectral responsivity
InGaAs	Indium-Gallium Arsenide
RT	room temperature
FOM	figure of merit
IL	interfacial layer
Gr	graphene
IFL	image force lowering
NVM	nonvolatile memory
V_{FB}	flat band voltage
V_{SET}	SET voltage
V_{RESET}	RESET voltage
$\mathbf{V}_{RVS}$	reverse-biased voltage
$\mathbf{I}_{LRS}$	LRS current
$\mathbf{I}_{HRS}$	HRS current
PVS	pulsed voltage source

List of Symbols & Notations

$\mathbf{V}_G$	gate voltage
V_{th}	threshold voltage
V_{FB}	flat band voltage
$\mathbf{Q}_{ox}$	oxide charges
$\mathbf{Q}_{it}$	interface trap charges
t_i	insulator thickness
t_{ox}	oxide thickness
χ_s	electron affinity of a semiconductor
χ_i	electron affinity of an insulator
$\mathbf{q}$	the elementary charge
E_g	bandgap
Ψ_{Bn}	Fermi potential with respect to the semiconductor mid-gap
Φ_n	Fermi potential with respect to the semiconductor band-edges
C_{ox}	oxide capacitance
C_s	semiconductor capacitance
C_{it}	interface state capacitance
G_{it}	interface state conductance
Φ_m	workfunction of a metal
E_F	Fermi-level
E_V	Energy level of the valence band edge
E_C	Energy level of the conduction band edge
Ψ_s	surface potential of a semiconductor
V_{ox}	potential across an oxide
F_{ox}	electric field across the oxide

Q_s	space charge density
ϵ_0	permittivity of free space
ϵ_{ox}	dielectric constant of the insulator
ϵ_s	dielectric constant of the semiconductor
W_D	depletion layer width
$\mathbf{D}_{it}$	inteface state density
Φ_B	Schottky barrier height
m^*	electron effective mass
h	Planck's constant
$\hbar$	the reduced Planck's constant
J_{DT}	direct tunneling current density
J_{FNT}	Fowlder-Nordheim current density
J_{TAT}	trap-assited tunneling current density
J_{TE}	thermionic emission current density
J_{FPE}	Frenkel-Poole emission current density
A^{**}	the effective Richardson constant
k_B	the Boltzmann constant
Φ_T	energy level of a trap (trap-depth)
$\mathbf{e}^-$-$\mathbf{h}^+$	electron-hole pairs
α	absorption coefficient
J_{ph}	photocurrent density
Θ	photon-flux
P_{opt}	optical power density
ν	frequency of light
λ	wavelength of light
ω	angular frequency
ζ_{it}	capacitance density
e_n	trap emission rate
f(E)	the Fermi-function
g(E)	the density of states
E_a	activation energy

0

Introduction

Advancement of the digital Microelectronics technology relied on the classical scaling philosophy for several decades to maximize device integration density while minimizing performance-to-cost ratio [1], guided by the famous evolutionary trend known as "Moore's law" [2]. However, the trend faced difficulty about 16 years ago due to approaching fundamental physical limits in the integrated circuit (IC) components [3]. This challenge was circumvented by introducing alternative performance boosters such as high-k gate dielectrics with metal gates, high mobility channel materials like strained silicon (Si) and FinFETS for enhanced electrostatic control that limits leakage current. Hence, this era is known as the "more Moore" era as it sustained Moore's law. Nevertheless, the end for the notion of enhancing IC performance through relentless device scaling seems inevitable. As a result, the microelectronics community started engaging in a new strategy called "more than Moore (MtM)". Unlike its predecessors (i.e. "Moore" and "more Moore"), the MtM strategy targets on diversifying the functionality of the IC to promote novel and non-digital (analog) applications such as radio-frequency (RF) electronics, power management systems, opto-electronics, sensors, micro/nano electro mechanical systems (M/NEMS), next generation computing systems, etc [4–7]. This strategy requires new device concepts and novel materials outperforming conventional ones.

Two-dimensional (2D) materials are promising contenders for MtM applications due to their extraordinary properties. They have thickness-dependent band structures and their ultra-thin body provides them with extremely large surface area-to-volume ratio compared to their three-dimensional (3D) counterparts. These make them highly sensitive to external interactions and perturbations [8]. Device researchers are fascinated by this feature as it offers the opportunity to tune and control their electrical properties by external means such as electric field [9–11]. The experimental demonstration of the first 2D material-graphene [9] has paved the way for the rise of other related 2D materials, setting a new trajectory to device research. Numerous research reports since then have contributed to a deeper understanding of the materials and also inspired new applications in various fields [12–14]. As illustrated in Fig.1, 2D materials offer a broad choice in terms of electrical properties. This includes insulators (e.g. hexagonal boron nitride (h-BN) [10]), topological insulators (e.g. bismuth telluride (Bi_2Te_3) [15–18]), semiconductors (e.g. molybdenum disulfide (MoS_2), molybdenum diselenide ($MoSe_2$), tungsten disulfide (WS_2), tungsten diselenide (WSe_2), black phosphorus (BP), etc.) [8, 10, 19, 20], semimetals (e.g. graphene) [8, 9, 21], metals (e.g. titanium disulfide (TiS_2) [8]) and superconductors (e.g. niobium diselenide ($NbSe_2$) [22, 23]). This thesis

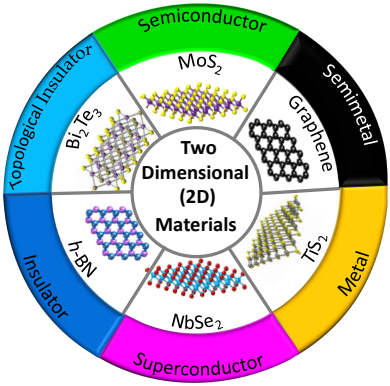

Figure 0.1: Illustration of the 2D materials classification based on their electrical properties offering a wide choice ranging from insulators to superconductors.

focuses on the investigation of vertical heterojunction devices based

on novel 2D materials, in particular graphene and MoS_2 integrated with the conventional 3D Si towards analog transistor [24], photodetector [25] and memristor [26–28] applications. I have also investigated fundamental aspects of the devices such as the dielectric properties of MoS_2 and charge carrier transport across heterojunction barriers. The devices presented in this dissertation are all produced using scalable and semiconductor technology compatible fabrication processes. The overall structure of the thesis will be described at the end of the present chapter.

0.1. Scope and Outline of the Thesis

This dissertation compiles the work I have accomplished my overall PhD research on the investigation of vertical heterojunction hybrid devices based on 2D materials, particularly graphene, MoS_2 and their heterostructure and the demonstration of potential applications towards high speed analog electronics, optoelectronics and neuromorphic computing. The main goal and focus of the study has been integrating the novel 2D materials with conventional Si to understand the fundamental physics giving rise to the observed device characteristics and also to demonstrate prospect applications. Under this guidance, the work was tailored to encompass from the basic understanding of the electronic and dielectric properties of MoS_2 up to the successful demonstration the device applications. Results from the research carried out have been presented in highly renowned international conferences and published in high impact peer-reviewed journals [24–28]. To effectively cover all the important aspects of the work and discuss associated results while ensuring a good story flow, the thesis is structured in totally nine chapters that are outlined as follows:

CHAPTER 1 highlights the important properties, potential applications as well as available production and transfer techniques for the novel 2D materials graphene and MoS_2.

CHAPTER 2 covers the fundamental concepts that are prerequisites for understanding the main contents dealt in the upcoming chapters. It provides brief introductions on metal insulator semiconductor (MIS) structures and current conduction mechanisms that limit the charge carrier transport across them. Following the detailed introduction on the two highly popular 2D materials (graphene and MoS_2) in chapter 1, this chapter also introduces graphene- and MoS_2-based vertical heterojunction devices including capacitors, diodes, photodetectors and

memristors along with their fundamental working principles.
CHAPTER 3 presents the overall methodology used to undertake the research work in the thesis. This includes device design, 2D material synthesis and transfer processes, device fabrication and characterizations as well as film characterizations. The chapter also covers data analysis and simulation that helped to understand and interpret the measured device characteristics.
CHAPTER 4 focuses on the experimental investigations carried out on Si/ MoS_2/chromium vertical structures for a basic understanding of the electronic and dielectric properties of MoS_2 and evaluate the potential of the structures for applications in nanoelectronics. The chapter presents bias-stress capacitance-voltage (C-V) and conductance-voltage (G-V) measurement results and discusses their implications toward the charge dynamics in the material and at the interface.
CHAPTER 5 reports on investigation results with regard to the vertical electron transport across vertical Si/MoS_2/graphene heterostructure devices and demonstrates the viability of the devices for potential applications as emitter diodes for graphene base hot electron transistors.
CHAPTER 6 demonstrates mobile hydroxyl ions-driven nonvolatile resistive switching phenomenon in nanocrystalline MoS_2 with edge terminated vertical layers sandwiched between silicon and chromium electrodes. The study was conducted by using current-voltage (I-V) hysteresis measurements and switching measurements such as endurance and retention tests. The origin of the resistive switching phenomenon is also determined via systematic measurements conducted in subsequent ambient and vacuum measurements.
CHAPTER 7 demonstrates the broad-band photodetection capability of Si/MoS_2/graphene photodetectors whose charge carrier transport has been already investigated in the previous chapter. The experimental investigation was carried out through electro-optical and spectral response measurements that were carried out on the devices. And, finally,
CHAPTER 8 summarizes the achievements of the thesis work and provides outlook on the prospect of further improving the performances of the MoS_2- and graphene-based heterojunction devices for electronic, optoelectronic and neuromorphic computing applications.

1

Fundamentals

This chapter introduces the two most explored two-dimensional (2D) materials, graphene and MoS_2 which the devices investigated in this thesis are based on. The chapter also highlights the relevant fundamental properties, potential applications as well as available production and transfer techniques for these 2D materials.

1.1. Graphene

Graphene is the first single atomic and crystalline 2D material experimentally demonstrated by A. Geim and K. Novoselov in 2004 [9], 57 years after its first theoretical conceptualization by P. R. Wallace [29]. It is composed of carbon atoms covalently bonded in a hexagonal crystal structure where two carbon atoms are arranged per unit cell to form a honey comb lattice [30] with a lattice constant of a = 2.46 Å (Fig.1.1a). Each carbon atom in the hexagonal lattice contributes sp^2 hybrids to form a σ-bond between two carbon atoms 1.42 Å apart. This gives rise to a trigonal planar arrangement (Fig.1.1b) which is the foundation for graphene's structural robustness [31, 32]. The electronic dispersion relation depicted in Fig.1.1c shows the band structure of graphene containing the π (brown)- and π^*(blue)-bands. As illustrated in Fig.1.1d, those bands touch each other at the singularity points known as Dirac points (i.e. at the K and K' points) in the first Brillouin zone [31], making

graphene a semi-metal with no bandgap. The term "Dirac point" is after the British physicist Paul Dirac who derived a relativistic wave equation that describes the band structure of graphene. Figs.1.1c and 1.1d are adopted from Ref. [33].

1.1.1. Properties of Graphene

Graphene possesses several remarkable material properties that may make it a superior material for many applications. Those properties that have relevance to the work in this thesis will be presented in this section.

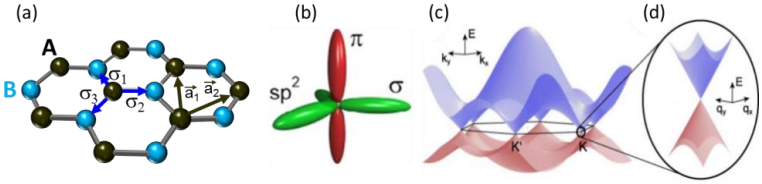

Figure 1.1: Band structure and crystal lattice of graphene: (a) The honeycomb lattice of graphene with carbon atoms covalently bonded in a hexagonal crystal structure that comprises two equivalent triangular sub lattices (red and blue) with unit vectors a1 and a2. The honeycomb lattice cartoon is taken from the internet. (b) Schematics of the σ- and π- orbitals of a single carbon atom in the graphene lattice adopted from Ref. [32]. (c) Electronic dispersion of graphene showing its band structure with the π(brown)- and π^*(blue)-bands touching at the K and K' singularity points called Dirac points [33]. (d) A magnified view showing the canonical form of the dispersion at a Dirac point (reused with permission from Ref. [33], ©2012 IOP).

Structural Properties of Graphene:

Graphene is a cabalistic material with extraordinary and contradictory but reconciled mechanical properties. To mention examples, it is only one atom thick on one hand making it highly flexible with a Young's modulus reaching 1Tpa [34], lightweight (~ 0.77 mg per square meter) and the thinnest material in existence [35]. On the other hand, the σ-bands obtained from the sp^2 hybridization give it a robust crystal structure with record high stiffness and mechanical stability making it the "strongest" material, more stiff than diamond and 300 times stronger than steel [31, 35]. It is brittle on one hand and ductile on the other with the capability to stretch [35, 36]. It is also reported that a single layer graphene has a very high thermal conductivity (up to 5300 W/mK)

[35,37] and that its structural robustness makes it impermeable to gases [35].

Electrical Properties of Graphene:

Graphene has a band structure with no energy gap and with a linear energy dispersion near the Dirac point. This makes it the thinnest conductive material. It can also withstand much larger current density than copper [35]. Its charge carriers have nearly zero effective mass and move with a constant Fermi velocity, hence the name massless Dirac fermions [38]. As a result, graphene achieves ultrahigh intrinsic charge carrier mobility [9, 39] and also exhibits a high saturation velocity [40]. Graphene's structural properties contribute to its unique electrical properties. For instance, the strong σ bonding prevents foreign atoms from infiltrating into its lattice to replace the carbon atoms. This contributes to a micrometer-range electron mean free path and a ballistic transport which may lead to high speed electronic devices [31, 35, 41].

Optical Properties of Graphene:

Graphene's unique optical properties expand the range of potential applications. Due to its ultra-thinness, graphene has about 97% transparency in the visible spectrum [42]. At the same time, its gapless nature and the linear dispersion relation in its band structure for the energy range from -1 to +1 eV lead to a nearly constant optical absorption that spans from the ultraviolet (UV) to the terahertz (THz) regime, providing a broad band light detection capability [42, 43]. In addition, the high charge carrier mobility in the material enables fast photodetection [44, 45].

1.1.2. Potential Applications of Graphene

Owing to its interesting properties listed in section 1.1.2, graphene has become a material of choice for applications in areas including but not limited to electronics, optoelectronics and sensors. Examples of electronic applications include analog RF transistors [32, 46, 47], amplifiers and RF-mixers [48, 49] as well as back-end of the line (BEOL) interconnects [46]. The applications in photonics and optoelectronics include fast and broadband photodetectors, transparent conductive electrodes (TCEs) and touch panels, light emitting diodes (LEDs), lasers and solar cells [44, 45, 50–52]. In the field of sensors and actuators,

graphene's mechanical and electrical properties can be used for strain-, chemical- and biological-sensors [53–55] as well as electromechanical resonators and NEMS transducers [56, 57].

1.1.3. Techniques of Graphene Production

Graphene quality has a tremendous impact on device performance and it is determined, among other technological factors, by the production technique used. Despite the astonishing progress made on synthesis over time, achieving pristine quality graphene remains a major technological challenge that inhibits industrial uptake. Hence, material scientists are still exploring new ways of producing graphene beside the effort put to improve existing ones in terms of both quality and lateral dimension. The production techniques in use today fall in to two general categories: top-down (eg. mechanical and chemical exfoliation) or bottom-up techniques (eg. chemical vapor deposition (CVD) and epitaxial growth).

Mechanical and Chemical Exfoliations:

Mechanical exfoliation provides the best graphene quality through a process of cleaving 2D flakes from a 3D graphite crystal [9, 58]. Despite its simplicity, it poses limitations in terms of scalability and controllability on size, shape and layer number (thickness) of the films produced. These limitations prevent using this technique for moving graphene from fundamental research labs to large-scale industries. In the case of chemical exfoliation, the graphene flakes are exfoliated by either using chemicals that break the vdW bonding between individual layers or by reducing graphene oxide in a suspension [59, 60]. This technique is scalable, but typically results in low quality films with defects introduced during the process. This limits its applicability in high performance electronic and optoelectronic devices.

Epitaxial Growth:

Epitaxial growth process involves thermal decomposition of the surface of a monocrystalline silicon carbide (SiC) in ultrahigh vacuum using high temperatures up to 1300 °C. The carbon in the SiC crystalizes into graphene while the Si sublimes [61, 62]. Growth of Wafer-scale graphene with encouraging quality suitable for device applications has been realized with this method [63]. The main drawbacks of the technique come from the high temperature that introduces strain in

the graphene film and also increases the production's thermal budget. While the earlier hinders device performance, the later incurs a high production cost. Another factor that incurs high production cost is the limited size of SiC wafers and their high cost. In addition, it is very challenging to transfer the graphene from SiC onto target substrates [64].

Chemical Vapor Deposition (CVD):

CVD is the most widely used technique on which the device research community relies to grow the graphene used for experiments on electronic and optoelectronic devices [47, 65, 66], flat panels and TCEs [67]. The process involves melting of carbon atoms from a hydrocarbon gas precursor such as methane (CH_4) in the presence of hydrogen (H_2) and letting them precipitate onto the surface of a metal foil made of transition metals such as platinum (Pt), rubidium (Ru), cobalt (Co), copper (Cu), nickel (Ni) etc. The mostly reported large area, uniform and high quality CVD graphene is commonly grown on either Ni or Cu [68, 69]. The later favors a self-limited growth of monolayer graphene. Although transferring CVD graphene is much easier than the epitaxial one, the process induces mechanical defects (cracks, holes and wrinkles) that can degrade device performance.

1.1.4. Techniques of Graphene Transfer

High quality graphene growth alone cannot ensure high device performance without a quality graphene transfer. The available transfer techniques can be classified as dry transfer (DRT) [9, 70, 71] and wet transfer (WT) methods. While DRT is used for both exfoliated and CVD-graphene to explore suspended devices [71], WT is mostly used to transfer CVD-graphene onto many other desired substrates. Both transfer methods require a prior coating of the graphene-on-Cu samples with a polymethyl methacrylate (PMMA) or any other suitable polymer as a support layer. The method used in this thesis work was the WT. Depending on the procedure followed to separate the graphene layer from the Cu foil, the method can be divided in to two as electrochemical delamination (ECD), also known as bubble transfer, [72, 73] and wet-chemical etching (WCE) [74].

Electro-Chemical Delamination (ECD) Method:

In the ECD method, the edge of the Cu/graphene/PMMA stack is carefully inserted into an electrolyte solution (e.g. 0.25 molar sodium hy-

droxide (NaOH) as used in this thesis) while applying a bias (e.g. ~ 2.8 V as used in this thesis) between the Cu cathode and a graphite anode as illustrated in Fig.1.2. Generation of hydrogen (H_2) bubbles at the Cu/graphene interface delaminates the graphene/PMMA stack from the Cu foil by breaking the van der Waals bonds [72, 73]. Then,

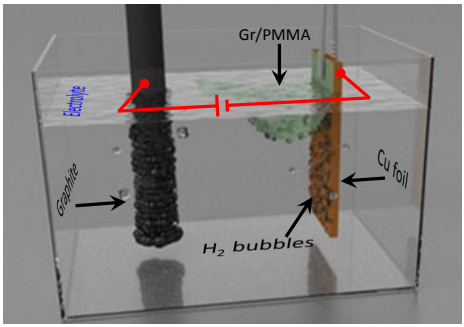

Figure 1.2: Illustration of electro-chemical delamination (ECD) graphene grown on Cu. Schematic (without labeling) courtesy of Dr. Stefan Wagner.

before transferring the stack onto the target substrate, NaOH and metal residues are cleaned from the stack through subsequent hydrochloric acid (HCL) and de-ionized water (DI-water) bathing. This step is meant to minimize the metal contamination level which has remained an issue all wet-chemical etching methods share [75]. Finally, the supporting PMMA layer is removed in hot acetone following a baking step. The main advantages of the ECD transfer are that it is fast and cost effective due to its minimal chemical usage and the prospect of reusing the Cu foil for several growths [72]. On the other hand, a possible disadvantage can be that the delamination speed depends on both the electrolyte concentration and the voltage applied. An aggressive bubble generation may cause holes and cracks in the graphene film.

Wet-Chemical Etching (WCE) Method:

WCE is perhaps the most widely used method for transferring CVD graphene onto arbitrary substrates [74]. The process starts by coating the CVD graphene/Cu sample with a supportive PMMA or similar polymer layer. Then, carbon residues deposited on the back side of the Cu substrate during the growth process are etched using oxygen

(O_2) plasma so that the Cu foil is completely exposed. Unlike the ECD method, the WCE method isolates the graphene layer from the Cu substrate by etching away the Cu using iron (III) chloride ($FeCl_3$) or other Cu etchants as demonstrated in Fig.1.3. Once the Cu is completely etched and the $FeCl_3$ residue is rinsed in DI-water, a further cleaning step in 5% HCL solution is done for ~ 30 minutes followed by another

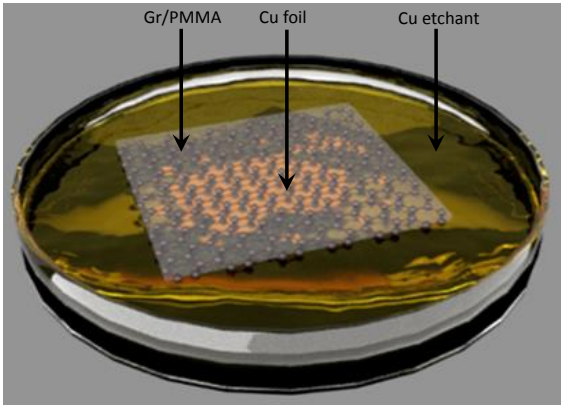

Figure 1.3: Illustration of the wet-chemical etching (WCE) of Cu foil under graphene. Image (without labeling) courtesy of Dr. Stefan Wagner.

30 – 60 minutes of DI-water rinsing to efficiently remove etchant and metal residues [74]. Afterwards, the graphene layer with the supporting polymer is fished out of the DI-water with the target substrate while making sure that the film is lying properly on the desired location of the substrate. The sample is then allowed to dry for over 12 hours in ambient environment inside a wet bench with a laminar flow. Then, to relax wrinkles in the graphene and also to increase its adhesion with the substrate, the sample is baked at 130 °C on a contact hotplate for ~ 5 minutes. Finally, removal of the PMMA layer is done in hot acetone (@85 °C) for about 45 minutes, followed by isopropyl alcohol (IPA) rinse and drying.

1.2. Molybdenum Disulfide (MoS_2)

The discovery of graphene and the immense research activities that followed have inspired the experimental realization of related 2D layered

materials enriching the horizon of materials science. Among the added 2D materials, transition metal dichalcogenides (TMDCs) have drawn the device researchers' attention due to their appealing properties that are suitable for several applications [76–80]. TMDCs are generically represented by the stoichiometric formula MX_2, with "M" standing for the transition metals such as titanium (Ti), niobium (Nb), molybdenum (Mo), tungsten (W), platinum (Pt), etc. and "X" representing the chalcogen elements tellurium (Te), sulfur (S) and selenium (Se) [76,80]. TMDCs have very diverse properties extending from insulating (e.g. HfS_2), semiconducting (e.g. MoS_2, WS_2 and others), semi-metallic (e.g. TiS_2 and WTe_2) and metallic (e.g. NbS_2 and VSe_2) to superconducting (e.g. TaS_2 and $NbSe_2$) [8, 19, 23, 80]. MoS_2 is probably the most versatile and highly explored material in this generic family. Its structural, electrical and optical properties has made it one of the most viable materials for several prospect applications. A single MoS_2 layer is composed of Mo and S atoms configured in such a way that a plane of Mo atoms are sandwiched between two hexagonal planes of S atoms in an octahedral or a trigonal prismatic coordination [76]. Multilayer MoS_2 is formed when such individual 2D layers are stacked vertically at an interlayer distance of ~ 6.5 Å, held together by weak van der Waals (vdW) attraction forces [72, 81]. However, the atoms are bonded with a strong covalent bonding within the plane. A 3D schematic representation of the MoS_2 structure is presented in Fig. 1.4. In multilayer MoS_2, each 2D layer may take the octahedral or trigonal prismatic coordinations and

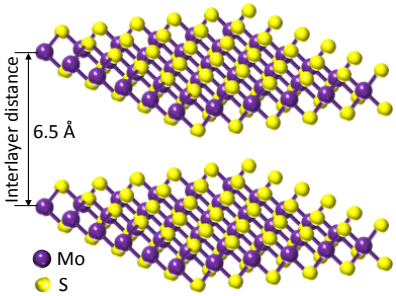

Figure 1.4: 3D schematic representation of MoS_2 layers each containing a plane of Mo atoms with a trigonal prismatic coordination sandwiched between two hexagonal planes of S atoms and separated by an interlayer spacing of ~ 6.5 Å

this gives rise to a large variety of polymorphic structures depending on the crystallographic unit cells' stacking order and the Mo atom coordinations. Among the resulting polymorphs, the most common ones are the 2H (Fig.1.5a), 3R (Fig.1.5b) and 1T (Fig.1.5c) phases. The digits in these names represent the number of layers the crystallographic unit cell contains, while the alphabets indicate the type of symmetry they achieve (i.e. H = hexagonal, R = rhombohedral and T = tetragonal) [76, 82]. The 1T phase exhibits a metallic behavior while the 2H and 3R phases are known for their semiconducting behavior. The MoS_2 films investigated for device applications in this thesis have the 2H-phase. This section will put emphasis on this TMDC material and cover its important aspects including its properties, production techniques, transfer methods and potential applications.

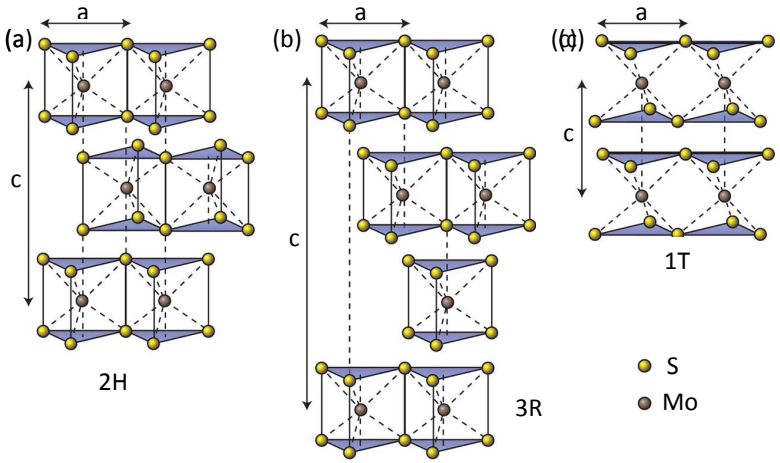

Figure 1.5: Schematics of the polymorphic structures of MoS_2 on the basis of the structural unit cells stacking order and the Mo metal coordination: (a) the 2H phase containing two layers per unit cell and exhibiting hexagonal symmetry and trigonal prismatic coordination, (b) the 3R phase containing three layers per unit cell and exhibiting a rhombohedral symmetry and trigonal prismatic coordination and (c) the 1T phase with one layer in the unit cell, exhibits a tetragonal symmetry and an octahedral coordination. The figure is adopted from ref. [76], ©2012 NPG, and the lattice parameters for MoS_2 "a" and "c" represent the lattice constant and stacking index, respectively. a = 3.15 and c = 12.3 Å [83, 84]

1

1.2.1. Properties of MoS_2

Structural Properties of MoS_2:

Like graphene, MoS_2 has sturdy mechanical stability which is attributed to the strong interatomic covalent bonding. This results in a high in-plane stiffness comparable to that of steel despite its ultra-thinness [85, 86]. It also has a much larger breaking strength than the commonly used flexible substrates such as polydimethylsiloxane (PDMS) or polyimide (PI) which suffers from mechanical failure at a strain of about 7% [87]. Like most of its other properties, MoS_2's mechanical properties also exhibit anisotropic behavior due to the week interlayer vdW binding. MoS_2 is also known for its light-weight and high flexibility [85] originating from its sub-nanometer thickness.

Electrical Properties of MoS_2:

2D MoS_2 is a semiconductor with bandgap ranging from 1.3 eV indirect (in bulk) up to 1.8 eV direct (in monolayer) [88]. According to first principles calculations, the band structure of bulk MoS_2 exhibits the indirect bandgap transition at the Γ-point and with decreasing number of layers, that gradually shifts to a direct transition at the K-point for monolayer (Fig. 1.6) [76, 89, 90]. The presence of this bandgap led to MoS_2 channel transistors with high ON/OFF ratios [76]. Despite being extremely thin, it also offers a theoretical charge carrier mobility of up to ~410 $cm^2 V^{-1} s^{-1}$ [76, 81, 91] which is comparable to that of bulk Si (~450 $cm^2 V^{-1} s^{-1}$) [81, 92]. Also, its ultra-thinness enables excellent electrostatic control of its electrical properties in short channel FETs [10, 93].

Optical Properties of MoS_2:

The electronic band structure of MoS_2 has a direct influence on its optical properties [76]. For instance, the sizeable bandgap enables optical sensitivity in a broad wavelength range. Interestingly, despite its atomic-scale thinness, it also has a higher absorption coefficient compared to its 3D counterparts such as Si [94, 95]. Furthermore, monolayer MoS_2 exhibits a strong photoluminescence and its direct excitonic transition energy at the K-point remains unaffected by the number of layers while its indirect transition energy near the Γ-point shifts considerably [96].

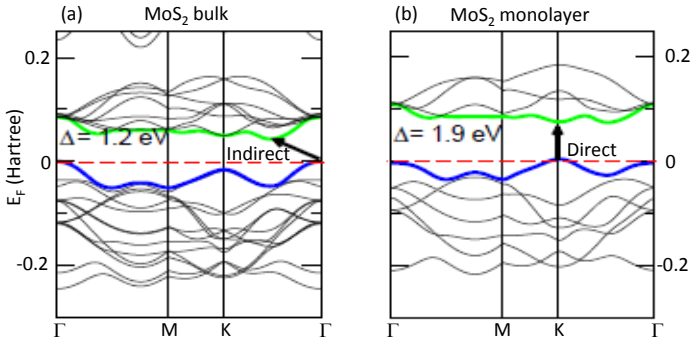

Figure 1.6: Band structures of: (a) bulk and (b) monolayer MoS_2 as obtained from first principles density functional theory (DFT) calculations. The figure is reproduced by permission from ref. [89], ©2011APS. In the figures, the horizontal red dashed lines, the green solid curves, the blue solid curves and the black arrows indicate the Fermi level position, the bottom of the conduction band, the top of the valence band and the fundamental bandgap transitions, respectively, of bulk and monolayer MoS_2.

Chemical Properties of MoS_2:

Like most 2D TMDC materials, MoS_2 exhibits a versatile chemistry [80]. Its reactivity is often associated with structural defects such as sulfur vacancies and metallic edge-states that play a crucial role in catalysis [80,97]. The presence of such active sites gives rise to the material's catalytic property required for applications such as catalytic hydrodesulphurization for extracting sulfur contaminants from fuel [97], lithium intercalation for batteries [98] and catalytic water splitting for hydrogen evolution reactions [8,99–103]. Experimental demonstrations also showed that active sites created by sulfide terminated Mo-edges are the dominant edge structures in 2H-MoS_2 and are responsible for its catalytic property to water [102]. This property has been exploited in this thesis project to realize memristor devices using edge-terminated 2H-MoS_2 with predominantly vertical layers as the active switching medium [26–28].

1.2.2. Potential Applications of MoS_2

The appealing properties described in 1.2.2 have made MoS_2 a potential candidate for several applications. Its tendency to readily disperse in various solutions makes it applicable in composites as a strength-

ening element [85]. Also, its reactivity enables energy-harvesting [99–103] and energy-storage [86] applications. Owing to its reactive nature, ultra-thinness and high surface-to-volume ratio, MoS_2 can be used for humidity-, gas-, chemical- and bio-sensors [104–107]. In addition, its interesting structural and electrical properties such as flexibility, ultra-thinness for a high degree electrostatic control and its semiconducting behavior with a large bandgap makes it a viable candidate for flexible nano-/micro-electronics. These include flexible transistors, MoS_2 channel metal oxide semiconductor field effect transistors (MOSFETs) with high on/off ratios, ICs capable of CMOS logic operations such as logical NOT-AND (NAND) gate, logical inverter, static random access memory and ring oscillators [76, 81, 81, 108, 109]. Optoelectronics is another application area for MoS_2 thanks to its atomic-scale thickness, high flexibility, high transparency, high optical absorption coefficient and its semiconducting nature with a thickness-dependent bandgap. These applications include solar cells [110, 111], LEDs [112], diode lasers [113], flexible phototransistors [114], ultra-broadband and ultrafast photodetectors [115,116], transparent displays [117] and wearable electronics [76, 118]. Furthermore, MoS_2 is recently gaining attention for applications in memristors [111, 119–124] which are building blocks for neuromorphic computing.

1.2.3. Techniques of MoS_2 Production

The capacity of producing atomically thin TMDC materials with precise control on their quality, uniformity, lateral dimensions and thickness is a prerequisite for industry-level applications in electronic and optoelectronic devices. Nevertheless, early research on TMDCs depended on exfoliation techniques, thus fulfilling the above requirements had been a huge challenge for a long time. Later on, continuing research on TMDCs along with the experience achieved from graphene has led to successful CVD growth with promising quality, control and scalability [125, 126]. This section will cover the most frequently used MoS_2 production techniques that fall into two general classifications as top-down (i.e. exfoliation) and bottom-up (i.e. CVD) techniques.

Exfoliation:

Adopted from the early days of the graphene research, micromechanical exfoliation has been widely used by researchers to demonstrate MoS_2. It is a top-down strategy carried out by peeling 2D flakes from

a natural bulk crystal using a sticky tape [127, 128]. Another top-down approach for MoS_2 production is liquid-phase exfoliation where individual layers are separated either by mechanical means (eg. sonication) in water [129] or by ionic intercalations using electrochemistry or solution chemistry [130]. In the latter case, lithium intercalation is commonly used to break the vdWs binding between the layers and facilitate their sonication-assisted isolation [130]. To inhibit agglomerations of the exfoliated flakes, surfactants such as chitosan are added to the solution [131]. Exfoliation techniques have advantages of being cheap and quick, but they also have disadvantages on the lack for systematic control over the shape, size, orientation and thickness of the exfoliated flakes and this limits their applicability to fundamental studies in research labs [126,127]. The main difference between the two techniques is that, while mechanical exfoliation produces small-size pristine quality MoS_2 flakes, chemical exfoliation process is scalable with a relatively lower film quality though. Hence, the later can be suitable for applications such as large-scale printable electronics.

Chemical Vapor Deposition (CVD):

CVD growth of MoS_2 involves thermal decomposition/ sublimation of the Mo and S precursors, followed by their subsequent vapor-phase chemical reactions forming gaseous MoS_2. This precipitates on the growth substrate to form solid-phase MoS_2 nuclei, which then merge and form continuous 2D MoS_2 atomic layers [132]. CVD is a scalable and semiconductor technology compatible production technique [127]. Its potential for producing large-area, uniform and high quality MoS_2 films makes it promising for wafer-scale fabrication of devices and circuitry. CVD has several variants and uses typical growth temperatures in the range of 700 -1000 °C and utilize solid-state precursors for molybdenum (e.g. $MoCl_5$, MoO_3, or Mo) [90, 133, 134] and gas precursors for sulfur (e.g. H_2S or vaporized S) [127, 135]. However, each specific CVD process may slightly differ from the other as the synthesis of the 2D film can be influenced by the surface property of growth substrates, atomic gas flux of precursors and growth temperature [78, 136]. Hence, on the basis of such process variations, the conventional CVD process has evolved over time into several CVD subclasses. These include plasma-enhanced CVD (PECVD) [137], atomic layer deposition (ALD) [127,138], metal-organic CVD (MOCVD) [127, 139, 140] and vapor-phase sulfurization (VPS). PECVD gives the advantage of low temperature synthesis

(150 – 300 °C) enabling MoS_2 growth even on plastic substrates [137], while ALD offers a high thickness-precision thanks to its layer-by-layer growth scheme [127, 138]. The latter is due to a self-limiting reaction of molecules with the substrate's surface following sequential pulses of the gas precursors (typically $MoCl_5$ and H_2S) with purges in between [127, 138]. Being the widely used CVD subclasses, the MOCVD and VPS techniques deserve a more detailed look and, therefore, will be discussed below.

Metal Organic Chemical Vapor Deposition (MOCVD):

MOCVD is a special type of CVD which is widely used by the semiconductor industry for epitaxial growth of monocrystalline films from organometallic precursors. It is also a promising technique to grow wafer-scale MoS_2 films with high-quality [139, 140]. It uses typical gas precursors such as molybdenum hexacarbonyl ($Mo(CO)_6$) for Mo and ethylene disulfide ($(C_2H_5)_2S$) or di-tert-butyl sulfide (DTBS) for S to grow MoS_2 films on SiO_2, fused silica or sapphire (0001) substrates [139, 140]. In the process, the ultrapure precursors are allowed to flow over a heated substrate in a reactor where they thermally decompose and form MoS_2 thin films atom by atom. Surface reactions taking place in the process are precursor molecule adsorption onto the substrate's surface, surface diffusion (surface kinetics), nucleation and film growth followed by desorption of volatile byproducts [78, 127]. Apart from argon (Ar) carrier gas, the process also uses H_2 to facilitate the decomposition of $(C_2H_5)_2S$ to enhance hydrogenolysis which promotes nucleation and finally to remove carbonaceous species generated by the process. MOCVD has advantages such as large-scale MoS_2 growth with high crystallinity and homogeneity, precise regulation of the precursors and control over the morphology and composition of the films.

Vapor-Phase Sulfurization (VPS):

VPS is a simple, cheap and fast technique which is capable of producing scalable and reasonable quality MoS_2 films. It is a CVD subclass that is alternatively referred to as thermally assisted conversion (TAC) and it is widely used to grow MoS_2 films by direct sulfurization of pre-deposited Mo films in a sulfur-rich atmosphere inside a CVD furnace [78, 127, 134, 141–143]. During the process, sulfur powder is evaporated (at about 150 - 250 °C) at an upstream location of the furnace to produce S-vapor that is transported by an inert carrier-gas (typically Ar) to the Mo-coated substrate which is being heated at typical temperatures of 400 – 800 °C

[127,134,141–143]. The sulfur atoms are then chemisorbed onto the Mo crystal face to form ordered phases, creating MoS_2 nuclei which then lead to a complete film formation by sulfur diffusion which is regulated by the growth temperature and pressure [80, 144, 145]. The technique can also be adapted by replacing the pre-deposited Mo film with a thin molybdenum tri oxide (MoO_3) film that requires a two-step process [146]. The first step reduces MoO_3 into MoO_2 through H_2/Ar annealing at about 500 °C, while the second step converts the reduced MoO_2 to MoS_2 via annealing at 1000 °C in a sulfur environment [146]. The advantages of the VPS/TAC technique include, easy and quick access to thin TMD films, scalable growth, growth on arbitrary substrates and better thickness control compared to vapor-phase reaction processes utilizing evaporated Mo and S sources [125]. The size and thickness of the final MoS_2 film is determined by the size and thickness of the initial pre-deposited Mo/MoO_3 films [147]. VPS is also capable of producing MoS_2 layers with vertical orientations apart from the standard horizontal ones by appropriately selecting the initial film thickness and the sulfurization conditions [134, 141–143]. It is suggested that the kinetics in a high temperature rapid sulfurization process produces the vertically aligned MoS_2 layers due to the following reason. Mo converts to sulfide faster than the diffusion rate of sulfur in a high temperature process, thus the natural orientation of the MoS_2 layers becomes vertical as the anisotropic structure of TMD layers facilitates the sulfur diffusion along the vdW gaps rather than across layers [125, 141]. Another hypothesis argues that at high temperature, sulfur diffusion is normally higher at grain boundaries of the polycrystalline Mo film and that leads to the formation of vertical MoS_2 layers for thicker initial Mo films. The MoS_2 films used in all the devices realized in this thesis were VPS-grown films.

1.2.4. Techniques of MoS_2 Transfer

When the target substrate on which devices are to be fabricated is different from the growth substrate, the as-grown MoS_2 films need to be transferred onto the target substrate. To maintain the intrinsic properties of MoS_2, just like any other atomic-scale 2D film, the transfer process is as equally important as the syntheses process because a high quality 2D film can be degraded to a great deal by the transfer process. The extreme mechanical delicacy due to its atomically thin structure makes MoS_2 transfer a very challenging task. The mostly used MoS_2 transfer techniques are briefly summarized below.

Mechanical Exfoliation (ME) Method:

ME is a dry transfer process where micromechanically cleaved MoS_2 flakes on a tape are subsequently pressed against a target substrate until a desired film thickness is achieved. Although not as intensely as in the early days, this transfer techniques is still being used in research labs for fundamental studies as it results in the best crystalline quality for high performance one-off devices. However, the method is not applicable for large-scale device production due the limitations described in 1.2.3. This method is frequently adopted for a residue- and wrinkle-free transfer [132] and nanotransfer printing [148] of CVD-grown MoS_2 flakes.

Polymer-Assisted Wet Chemical Release (PWCR) Method:

PWCR is a widely used method for transferring large-area CVD-MoS_2 films from the growth substrates (typically SiO_2 or sapphire (Al_2O_3)) onto desired substrates. The primary step in the process is to coat the as-grown MoS_2 films with PMMA or any other polymer like in graphene. After baking the samples at about 120 - 150 °C for 3 - 4 minutes, the film is delaminated from the growth substrate using NaOH, KOH or similar solutions [125, 146, 149, 150]. Bubbles generated at the MoS_2/substrate interface while the solution etches the surface of the substrate. The PMMA-supported MoS_2 film will float on the solution when it is completely released from the growth substrate. The MoS_2/PMMA stack is cleaned in DI-water to ensure that the etchant residue is cleaned well. Then it is transferred onto the target substrate and let dry. Finally, the transferred sample is baked again at 120 - 150 °C for 3 - 4 minutes and the PMMA is removed in hot acetone. Once the PMMA is completely removed, the sample is rinsed in IPA and dried with nitrogen gas [125, 132, 146, 149, 150].

2

Fundamental Device Concepts

Basic concepts that are considered necessary to smoothly follow though the overall contents discussed in the upcoming chapters will be covered in this chapter to help readers get a comprehensive understanding of the dissertation.

2.1. Metal Insulator Semiconductor (MIS) Structures

Metal-insulator-semiconductor (MIS) structures are vital elements that are used in many semiconductor devices such as capacitors, diodes and MOSFETs. The stability and reliability of all semiconductor devices rely on the semiconductor's surface conditions, the physics of which can be studied using the MIS system [151, 152]. Therefore, understanding this system is a primary step towards understanding the operation of other semiconductor devices. Fig. 2.1 shows a schematic showing isometric view of a simple MIS structure with a wiring setup in which a gate voltage (V_G) is applied on the metal gate while the semiconductor is grounded.

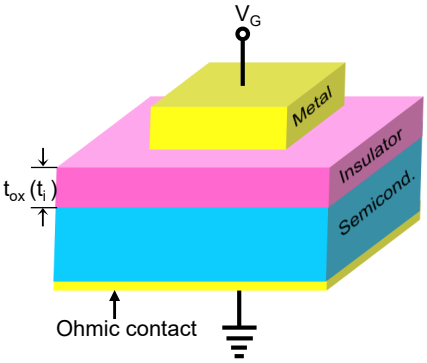

Figure 2.1: Schematic diagram showing the structure of an MIS capacitor with t_i representing the thickness of the insulator layer.

2.1.1. The Ideal MIS System

The most practical MIS device that has been extensively studied since the 1950s is the metal-oxide-silicon (MOS) system to which most Si-based devices and ICs are directly associated [151,153–155]. The present knowledge on the practical MOS system is based on the ideal MIS theory that relies on three basic assumptions [151, 152] that:

1. neither oxide charges (Q_{ox}) nor interface trap charges (Q_{it}) exist in the structure at any biasing conditions (i.e. $Q_{ox} = Q_{it} = 0$),

2. the insulator's resistivity is sufficiently high to prevent carrier transport through it under DC bias, leaving the semiconductor's Fermi-level flat (i.e. $dE_F/dx = 0$), and

3. the work function of the metal (Φ_m) is equal to that of the semiconductor (Φ_s), making the metal-semiconductor work function difference zero (i.e. $\Phi_{ms} = 0$).

Assumption 3 leads to a flat-band condition of the structure at $V_G = 0V$ in which the bands are flat as illustrated in Fig. 2.2a. Hence, the expression

$$\Phi_{ms} \equiv \Phi_m - \left(\chi_s + \frac{E_g}{2q} - \Psi_{Bn}\right) = \Phi_m - (\chi_s + \Phi_n) = 0, \qquad (2.1)$$

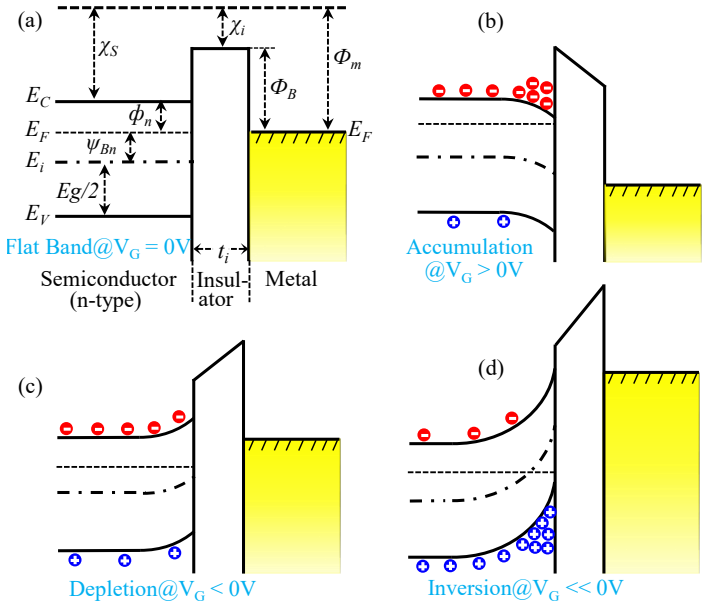

Figure 2.2: Energy band diagrams of an ideal MIS structure with an n-type semiconductor illustrating: (a) flat band ($V_G = 0$), (b) accumulation ($V_G > 0$), (c) depletion ($V_G < 0$) and (d) inversion ($V_G \ll 0$) conditions.

where, χ_s and χ_i are the semiconductor and insulator electron affinities, respectively, E_g is the semiconductor bandgap, q is the elementary charge and Ψ_{Bn} and Φ_n are the Fermi potentials with respect to the mid-gap and band-edges respectively [151]. The voltage at which the MIS system reaches a flat-band condition is called flat-band voltage (V_{FB}) which is determined by using

$$V_{FB} = \Phi_{ms} - \left(\frac{Q_{it} + \frac{x_m}{t_{ox}} Q_{ox}}{C_{ox}} \right), \tag{2.2}$$

where x_m is the center of gravity for the distribution of the total charge in the system, $t_{ox}(t_i)$ is the oxide/insulator thickness and C_{ox} is the oxide/insulator capacitance [151]. $Q_{ox} = Q_{it} = \Phi_{ms} = 0$ for an ideal MIS capacitor and thus Eq.(2.2) gives $V_{FB} = 0$. Upon bias, the MOS system experiences subsequent accumulation, depletion and inversion

of charge carriers on the semiconductor's surface [151, 152]. For an MOS structure with an n-type semiconductor, the energy bands of the semiconductor bend downwards for $V_G > 0$ and approach the Fermi-level (E_F), leading to accumulation of electrons at the semiconductor-insulator interface (Fig.2.2b). However, at a small negative voltage (i.e. $V_G < 0$), the bands bend upwards depleting electrons from the semiconductor surface and forming a depletion region (Fig. 2.2c). When the applied voltage increases further (i.e. $V_G \ll 0$), the bands bend further up and the semiconductor reaches a state of inversion where holes (minority carriers) are populated at the valence band (E_V) edge close to the n-type semiconductor-insulator interface (Fig. 2.2d). The critical voltage below which the MIS system enters inversion is called threshold voltage (V_{th}). The bending of the semiconductor bands in the MIS system is dictated by the potential at the surface of the semiconductor known as the surface potential, Ψ_s, which in turn is influenced by the applied bias. In an ideal MIS structure where $\Phi_{ms} = 0$, V_G is partitioned between the insulator and the semiconductor according to Eq. (2.3)

$$V_G = V_{ox} + \Psi_s, \tag{2.3}$$

where V_{ox} is the potential across the insulator. A positive (negative) V_G applied on the MIS structure with n-type semiconductor results in a positive (negative) Ψ_s as shown in Fig. 2.3a, causing a downward (upward) bending of the semiconductor band edges as illustrated In Figs. 2.3b and 2.3c, respectively. Variations in Ψ_s also lead to variations in the space-charge density (Q_s) as demonstrated by the simulation result depicted in 2.3d where sections of Ψ_s corresponding to the accumulation, depletion and inversion states of the semiconductor are delineated. It is worth to mention that the accumulation, depletion and inversion phenomena in MIS structures with a p-type semiconductor occur in exactly similar manners as in the case with an n-type semiconductor, albeit with a reversed polarity.

2.1.2. Characterization of the MIS System

The MIS system comprises a capacitive device whose electrical properties are usually characterized by measuring and analyzing its capacitance and conductance as a function of bias and frequency [152, 156]. The capacitance contains two parts, namely, the semiconductor and oxide capacitances that are connected in series. Therefore, the total

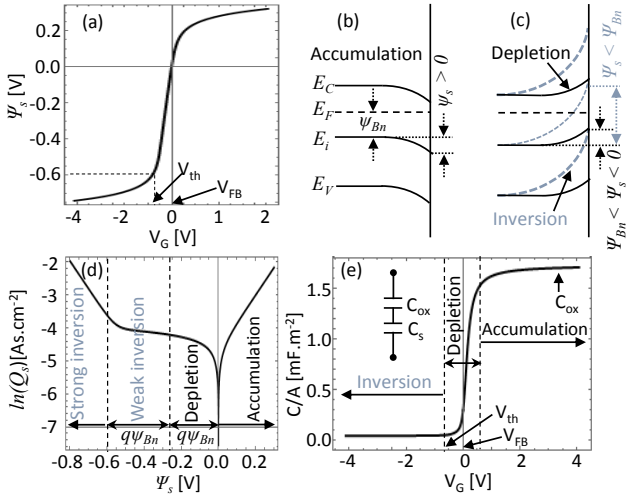

Figure 2.3: Properties of an ideal MIS capacitor with n-type semiconductor: (a) Surface potential, Ψ_s, (b) energy-band diagram at the n-type semiconductor surface at accumulation for $\Psi_s > 0$, (c) at depletion for $\Psi_{Bn} < \Psi_s < 0$ (black) and at inversion for $\Psi_s < 2\Psi_{Bn}$ (gray). The calculation that led to the result in this graph is done by Prof. Olof Engström. (d) Space-charge density as a function of the surface potential and (e) capacitance as a function the applied gate bias, V_G. The inset shows the equivalent circuit model of the MIS system containing the insulator and semiconductor capacitors connected in series.

capacitance of the system is given by

$$C_{tot} = \frac{C_{ox}C_s}{C_{ox} + C_s}, \tag{2.4}$$

where C_{tot} is the total capacitance of the MIS system, C_{ox} is the oxide/insulator capacitance and C_s is the semiconductor capacitance. The oxide capacitance is independent of the applied voltage and can be determined using the expression

$$C_{ox} = \frac{\epsilon_0 \epsilon_{ox} A}{t_{ox}}, \tag{2.5}$$

where ϵ_0 is permittivity of free space, ϵ_{ox} is the dielectric constant of the insulator and A is area of the capacitor [151, 152, 156]. However, the semiconductor capacitance exhibits a voltage-dependent behavior and

it is given by the derivative of the space-charge density with respect to the surface potential as [151, 152, 156]

$$C_s = \frac{dQ_s}{d\Psi_s} \tag{2.6}$$

During depletion, i.e. for $\Psi_{Bn} < \Psi_s < 0$, Eq. (2.6) can be approximated to

$$C_s = \frac{\epsilon_s}{W_D}, \tag{2.7}$$

where ϵ_s is the dielectric constant of the semiconductor and W_D is the depletion layer width. C-V characterization is typically carried out by superimposing an alternating current (AC) probe signal of very small amplitude (i.e. in the range of mV) onto a DC voltage to create a small change in Ψ_s for a particular V_G [152, 156]. Mostly, a high frequency is used for the AC signal so that the slow process of minority carrier generation at the semiconductor-insulator interface cannot keep up with the signal. Hence, the minority carriers do not contribute to the capacitance measured this way and, as a result, the high-frequency capacitance (HF C-V) reaches its minimum in the inversion regime (i.e. $V_G < V_{th}$) where W_D approaches its maximum. On the other hand, the capacitance attains its maximum in the accumulation regime (i.e. $V_G > V_{FB}$) where the total capacitance becomes equal to C_{ox}. In the depletion regime (i.e. where $V_{th} < V_G < V_{FB}$), the capacitance shows a steep increase with bias due to C_s which in turn relies on the bias-dependence of W_D. Fig. 2.3e depicts such a HF C-V characteristics for an ideal MIS capacitor with n-type Si and the inset shows the equivalent circuit model considered. As expected based on Eq. (2.6), the C-V characteristics reveals the distinct operation regimes outlined in Fig. 2.3d.

2.1.3. The None-Ideal MIS System

As discussed in 2.1.1, Q_{ox}, Q_{it} and Φ_{ms} are all assumed to be zero for the ideal MIS system. However, these quantities can have non-zero values for practical MIS devices due to imperfections in the insulator and at the interfaces, causing deviations of the measured C-V characteristics from the ideal. For example, a non-zero Q_{ox} would shift the V_{FB} of the C-V curve from zero (i.e. to the right for a negative Q_{ox} and to the left for a positive Q_{ox}). The amount of the shift, $\Delta\ V_{FB}$, can be used to estimate the concentration of Q_{ox} by using the relation Q_{ox}

= -$\Delta V_{FB} C_{ox}$. Similarly, a non-zero Φ_{ms} results in a V_{FB} shift by the same amount. Also, as experimentally demonstrated by W. Shockley and G. L. Pearson, interface traps, also called interface states, can be present in practical MIS structures [157]. A typical effect of interface traps is stretching out of the C-V curves along the voltage axis as it takes more applied voltage or charge to induce the same amount of surface potential or band bending that is achieved in their absence. This is because filling the interface states requires additional charge [151]. In addition to C_{ox}, Φ_{ms} and D_{it}, C-V measurements can be useful to determine quantities such as insulator thickness, dielectric constant, doping concentration, etc.

2.2. Charge-Carrier Transport across MIS Structures

Unlike the ideal MIS capacitor, practical devices experience charge-carrier conduction across the insulator at sufficiently high electric-fields and temperatures although the conduction mechanism may vary depending on the type, thickness and quality of the insulator and its interfaces. The transport mechanisms can be classified into two general categories either as electrode-/interface-limited and bulk-limited, or as thermal-assisted and thermal-insensitive, or tunneling-based and emission-based, etc. Electrode-/ interface-limited transports mainly depend on the properties of interfaces and the electrode work-function difference and they give rise to asymmetric current conductions at opposite bias polarities, which is not the case for bulk-limited ones. Thermally-assisted transport leads to a temperature-dependent current and corresponding linear activation plots which is not observed for thermal-insensitive ones. Tunneling-based conductions involve quantum mechanical tunneling of carriers through a barrier, whereas emission-based transport relies on the emission of thermally-activated carriers over a barrier. Transport mechanisms covered in this thesis will be categorized with the third classification option.

2.2.1. Tunneling-Based Transports

Tunneling is a transport mechanism based on the quantum mechanical phenomenon in which the wave-function of an electron penetrates through a potential barrier [151]. It occurs for electron energies smaller than the height of the barrier. It depends strongly on the electric-field,

but not on temperature. The probability of an electron to tunnel through a potential barrier is estimated by an important parameter called the quantum mechanical transmission coefficient, T [158], which is given by

$$T = \left(1 + \frac{1}{4}\left(\frac{\Phi_B^2 sinh^2 \gamma w}{E(\Phi_B - E)}\right)\right)^{-1}, \tag{2.8}$$

where $\gamma = 2m^* \sqrt{\Phi_B - E}$, Φ_B is the height of the potential barrier, w is the width of the barrier, E is energy of the incident electron, m^* is the electron effective mass in the insulator, and $\hbar$ is the reduced Planck's constant. Along with other factors, the shape of the potential barrier determines the specific form T would take, thus determining the type of tunneling. Examples of tunneling-based transport mechanisms include direct tunneling (DT) [159–161], Fowler-Nordheim tunneling (FNT) [151, 160, 162, 163], trap-assisted tunneling (TAT) [164, 165], resonant tunneling (RT) [151, 166] and band-to-band tunneling (BTBT) [151, 160, 167]. Brief descriptions of the ones relevant to the study in this thesis are discussed below.

Direct Tunneling (DT):

As described by Eq. (2.3), in subsection 2.2, part of the applied voltage in an MIS structure is taken up by the insulator in the form of V_{ox}. For $V_{ox} < \Phi_B$ at low fields, electrons see a trapezoidal potential barrier. When the insulator is thin enough (usually below 5 nm), they directly tunnel through the complete width of the barrier as illustrated in Fig. 2.4a. Hence, the mechanism is referred to as DT and the resulting current density, J_{DT} is given by [159–161]

$$J_{DT} = BF_{ox}^2 exp\left(-\frac{C\Phi_B^{3/2}\left(1 - \left(\frac{\Phi_B - t_{ox}F_{ox}}{\Phi_B}\right)^{3/2}\right)}{F_{ox}}\right), \tag{2.9}$$

where $B = \frac{q^3}{16\pi^2\hbar\Phi_B}$, $C = \frac{4\sqrt{2m^*}}{3\hbar q}$ and F_{ox} is the electric-field across the oxide/insulator layer.

Fowler-Nordheim Tunneling (FNT):

FNT is a highly field-dependent transport mechanism that dominates the current conduction across MIS structures containing thicker insulators and it occurs at a higher electric-field compared to DT. When

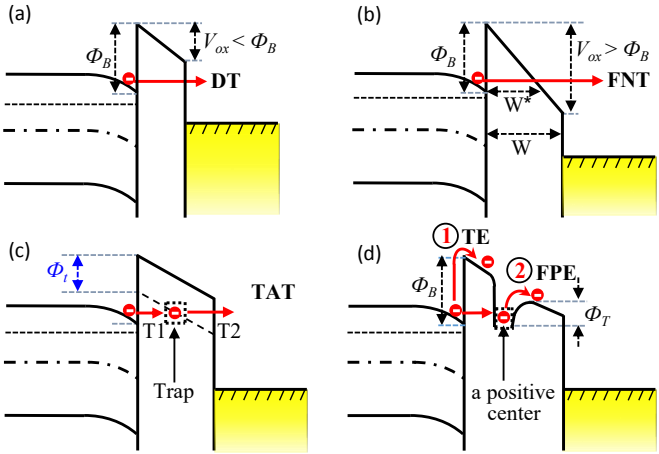

Figure 2.4: Schematic diagrams with illustration of charge-carrier transport across MIS structures by: (a) direct tunneling (Dt), (b) Fouler-Nordheim tunneling (FNT), (c) trap-assisted tunneling (TAT) and (d) Thermion emission (TE) as indicated by arrow 1 and Frenkel-Poole emission (FPE) as indicated by arrow 2.

the applied voltage is high enough such that $V_{ox} > \Phi_B$ as shown in Fig. 2.4b, the electrons now see a triangular potential barrier with an effective barrier-width narrower than the original insulator thickness. The electrons tunnel through the triangular barrier and provide a Fowler-Nordheim current density, J_{FNT}, which is modeled as [151, 160, 162, 163].

$$J_{FNT} = \frac{q^3}{16\pi^2\hbar\Phi_B} F_{ox}^2 exp\left(-\frac{4\sqrt{2m^*}\Phi_B^{3/2}}{3\hbar q F_{ox}}\right), \tag{2.10}$$

Trap-Assisted Tunneling (TAT):

Traps inside the bulk of a defective oxide can create a conduction path for electrons across the barrier by partitioning it into smaller widths. The electrons undergo subsequent tunneling through the partitions and cross the complete barrier. This type of conduction is known as TAT [164, 165]. In a simplified model, TAT can be considered as a two-step tunneling process mediated by a single trap as illustrated in Fig. 2.4c. The TAT current density, J_{TAT} is proportional to the oxide electric-

field, E_{ox} and the trap energy level, Φ_t as given by Eq.(2.11).

$$J_{TAT} \propto exp\left(-\frac{4\sqrt{2qm^*}}{3\hbar F_{ox}}\Phi_t^{3/2}\right), \tag{2.11}$$

where textitΦ_t is the trap depth measured from the conduction band minimum of the insulator [164–166]. TAT can have several variations such as single- and multi-trap TAT, shallow- or deep-trap TAT and elastic- or inelastic-TAT depending on the density of the traps, the energy level of the traps and whether or not energy is conserved, respectively [166].

2.2.2. Emission-Based Transports

Unlike tunneling, in which charge-carriers are transported through a potential barrier, emission requires the carriers to be thermally excited to gain high enough energy and jump over the barrier. The carrier supply for emission could be either the semiconductor or metal surfaces as in the case of thermionic emission (TE), also known as Schottky emission (SE) [151, 168, 169], or a localized trap in the bulk of the insulator as in the case of Frenkel-Poole emission (FPE) [151, 170, 171].

Thermionic Emission (TE):

When a conductive solid-state body is heated to a high enough temperature, charged particles known as "thermions" are emitted from the surface and the process is known as thermionic emission (TE) [151, 168]. In semiconductor devices, the thermions are thermally excited electrons with energies above the top of a potential barrier from where they can be readily swept away by an electric-field and provide an electric current (Fig. 2.4d). The standard TE model showing the relation TE current density, J_{TE} has with electric-field and its strong dependence on temperature can be written as

$$J_{TE} = A^{**}T^2 exp\left(-\frac{q\left(\Phi_B - \sqrt{qF_{ox}/4\pi\epsilon_0\epsilon_{ox}}\right)}{k_B T}\right), \tag{2.12}$$

where A^{**} is the effective Richardson constant given by $\frac{qm^*k_B^2}{2\pi^2\hbar^3}$, T is temperature and k_B is the Boltzmann constant [151]. TE is also referred to as Schottky emission (SE) when the thermally activated electrons are emitted over metal-semiconductor Schottky junctions [169].

Frenkel-Poole Emission (FPE):

FPE is a mechanism based on emission of thermally activated electrons from charged traps in the bulk into the CB of the insulator by overcoming the trap energy barrier, Φ_T, as illustrated in Fig. 2.4d. The PFE model considers that these traps are positive impurity centers whose interaction with electrons at the CB establishes a coulomb potential that decreases with increasing electric-field leading to an increasing thermal emission rate of the electrons [151, 170–172]. FPE occurs typically in the low to moderate field range and it relies on both electric-field and temperature like TE, although its dependence is stronger on the earlier in contrast to TE. The FPE current density, J_{FPE} is modeled as

$$J_{FPE} = F_{ox} exp\left(-\frac{q\left(\Phi_T - \sqrt{qF_{ox}/\pi\epsilon_0\epsilon_{ox}}\right)}{k_B T}\right), \tag{2.13}$$

where Φ_T is the energy barrier the trapped electron faces and it is measured from the trap level to the CB minimum of the insulator [151, 170, 171]. TE and FPE show a similarity as can be noticed from the exponential terms in Eqs. (2.12) and (2.13). However, the barrier lowering in FPE is twice as large as that of TE because of the static nature of the positive center [151, 170].

2.3. 2D Materials-Based Vertical Heterojunction Devices

As stated in chapter 1, the main focus of the work leading to this thesis has been the investigation of heterojunction devices obtained by integrating novel 2D materials with conventional 3D Si in a vertical architecture. Examples of such 2D materials-based vertical heterojunction devices include tunnel diodes [151, 173], tunneling FETs (TFETs) [174, 175], graphene barristor [176], graphene-base hot electron transistors (GBTs) [47, 177, 178], graphene-base heterojunction transistors (GBHTs) [179–181], Photodiodes [151, 182, 183] and memristors [184–188]. To help readers conveniently follow the research results covered in the coming chapters, this section provides a brief description on the structure and functionality of those devices covered in the thesis.

2.3.1. Graphene-Base Hot Electron Transistors (GBTs)

GBTs are three-terminal vertical devices containing an emitter, a base and a collector, with each component isolated from the other by a thin

oxide layer [47, 64, 177, 178, 189–192]. While a single layer graphene (SLG) is used as the base, the emitter and collector of a GBT can be made of either a metal or a doped semiconductor. The oxide layer isolating the base from the emitter is called emitter-base insulator (EBI) and the one separating it from the collector is known as base-collector-insulator (BCI) [47, 177]. The EBI serves as the tunneling barrier, while the BCI works as a filtering barrier that allows the passage of only high energy electrons (hot-electrons) [64, 178]. The structure and functionality of the GBT is inspired by hot electron transistors (HETs) which were introduced in the 1960s by C. A. Mead [193] and whose operation is governed by the principle of hot-electron transport [151, 194]. All the three terminals of the first HET were metals and a high-speed operation was anticipated from them considering the high velocity and ballistic transport of hot-electrons along with a short transit time at the base. However, this required a very thin metallic-base to reduce scattering and achieve the shortest possible base transit time. At the time, this strategy encountered two major challenges: (1) deposition of very thin, highly homogeneous and pinhole-free metal layers became a hurdle and (2) the resistance of metallic films increases intensely when their thickness is decreased and this causes an RC delay and a self-bias crowding, thus limiting the device's performance [64]. As a result, SLG

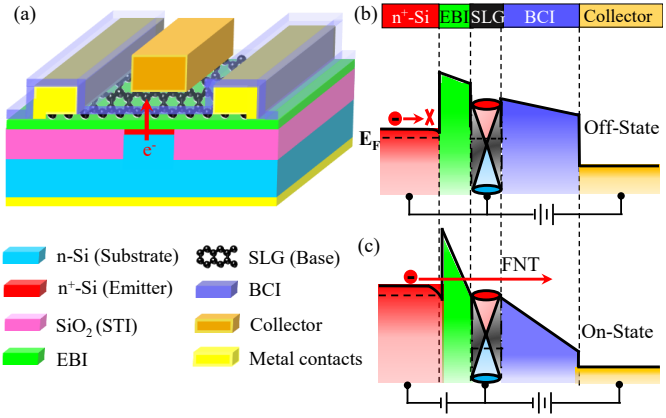

Figure 2.5: : (a) Schematic of isometric and cross-section view of a GBT. Conduction band diagram of a GBT in its active region during the (b) off-state and (c) on-state.

was proposed in place of the metallic-base to mitigate the challenges mentioned above by taking advantage of graphene's one-atom thick body and its ultra-high conductivity [177]. A 3D schematic diagram showing the structure of a GBT is presented in Fig. 2.5a. The GBT operates in the following manner: in the absence of an emitter-base voltage, the device will be in its off-state as the electron injection from the emitter into the base is inhibited by the EBI barrier, which needs to be high and thick enough to suppress TE and DT, respectively as illustrated in the conduction band (CB) diagram in Fig. 2.5b. However, application of an emitter-base voltage that is high enough to change the trapezoidal potential barrier in Fig. 2.5b into a triangular one reduces the effective width of the EBI barrier. This allows hot electrons from the emitter to tunnel through this barrier, move across the graphene layer ballistically and head towards the collector (Fig. 2.5c). Modelling and simulation studies have suggested that GBTs can achieve high on/off ratios, high output resistance (output current saturation) and high cut-off frequency reaching the THz regime, making them promising devices for potential high-speed RF applications [177, 180, 190, 195–198].

2.3.2. Graphene-Base Heterojunction Transistors (GBHTs)

To improve the performance of GBTs and in the meantime to ease the technological challenges in fabricating them, Di Lecce and coauthors proposed a simplified version of the device structure which they named graphene-base heterojunction transistors (GBHTs) [199]. The device concept for GBHTs is adopted from GBTs and their structure comprises a graphene-base sandwiched between two Si layers, i.e. a heavily doped (n^+-Si)-emitter and a lightly doped (n-Si)-collector [181,199] as demonstrated by the 3D schematics in Fig. 2.6a. The contact between the graphene-base and the two Si terminals form a Schottky barrier whose height can be controlled by the base voltage. The performance of GBHTs is based on hot-electron emission across the Schottky barrier and the transport is regulated by TE (Fig. 2.6b) in contrast to GBTs where FNT is the dominating transport mechanism [47]. According to simulation studies, GBHTs are capable of achieving several THZ performances and this makes them potential candidates for applications in high speed electronics [179, 181, 199].

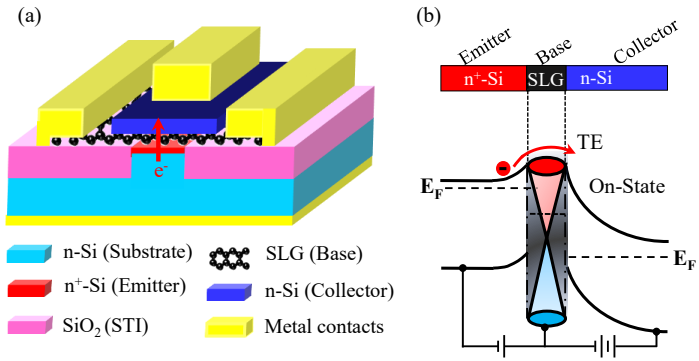

Figure 2.6: : (a) Schematic of 3D isometric and cross-section view of a GBHT and (b) conduction band diagram of a GBHT in its active region during the on-state.

2.3.3. Photodetectors

Photodetectors are semiconductor devices that are capable of detecting optical signals through electronic process of generation, transport and extraction of carriers that provide the output signal in the form of electrical current [151]. Currently available photodetectors can generically be categorized as either thermal detectors or photon detectors. While the earlier operate in the far-infrared wavelength range and are normally used as thermal sensors, the latter detect light through the principle of quantum photoelectric effect by which photons with energy larger than the bandgap (E_g) of a semiconductor are absorbed in it and generate electron-hole (electron-hole) pairs as illustrated in Fig. 2.7a. The photo-generated carriers are then extracted in the form of a photocurrent (Fig. 2.7b) [151]. The absorption of photons in a semiconductor is monitored by an important optical quantity known as the absorption coefficient, α. The photons can be absorbed near the surface of a semiconductor with high α, but penetrate deeper into the one with a small α [151]. Practical applications require photodetectors to achieve high speed and high sensitivity accompanied by low noise. The fundamental metrics that are commonly used to evaluate the optical sensitivity of a photodetector are quantum efficiency and spectral responsivity. Quantum efficiency, *QE*, is defined as the number

of carriers generated per absorbed photon, i.e.

$$QE = \frac{J_{ph}}{q\Theta} = \frac{J_{ph}}{q}\left(\frac{h\nu}{P_{opt}}\right), \tag{2.14}$$

where J_{ph} is the photocurrent density, Θ is the photon flux which is given by $P_{opt}/h\nu$, P_{opt} is the optical power density, $h\nu$ is the incident photon energy with ν and h being the light frequency and the Planck's constant, respectively. The QE is commonly expressed in percentage with the ideal value being 100%. However, in practical cases, it is usually below the ideal value due to current losses caused by incomplete absorption, reflection, carrier recombination etc. The spectral responsivity, *SR*, evaluates the detector's output signal with respect to its input and can be formulated as Eq. 2.15

$$SR(A/W) = \frac{I_{ph}}{P_{opt}} = \frac{qQE}{h\nu} = \frac{QE\lambda\,(nm)}{1240}, \tag{2.15}$$

where λ is the incident photon wavelength and A/W is the unit of SR which means Ampere per Watt. Devices that can be used as photode-

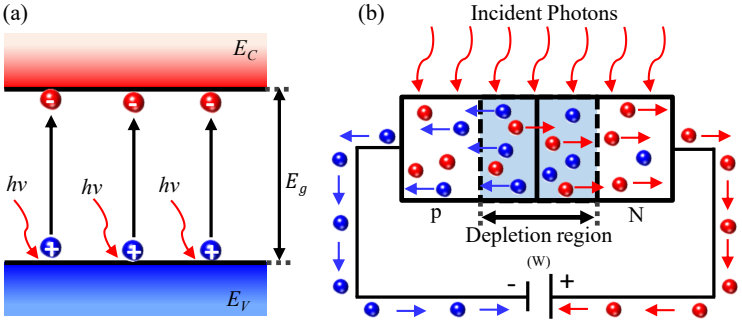

Figure 2.7: : Schematic diagrams demonstrating: (a) the photon-assisted carrier excitations in a semiconductor and (b) generation and extraction of carrier in a semiconductor p-n junction photodiode.

tectors include photoconductors [200], phototransistors [201] and photodiodes [151]. Due to the scope of the thesis, only photodiodes will be summarized in this section. These are semiconductor devices where the semiconductor part forms a depletion region with a high electric-field enabling separation of the photo-generated electron-hole pairs

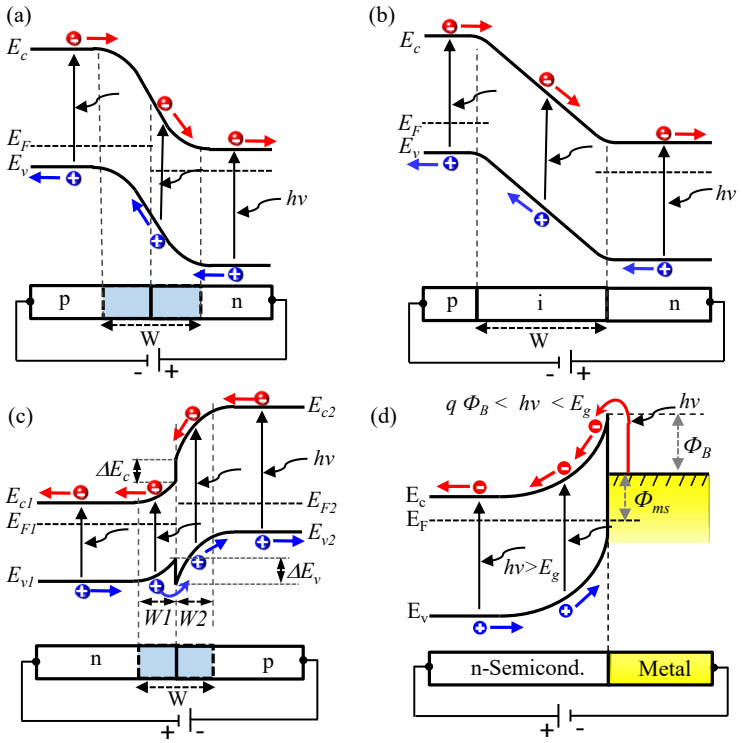

Figure 2.8: : Schematic band-diagrams showing operations of: (a) a p-n junction photodiode, (b) a p-i-n photodiode, (c) a heterojunction photodiode and (d) a Schottky barrier photodiode.

to avoid recombination. While maintaining a thin depletion region reduces carrier transit time and thus increases operation speed, it reduces the *QE* setting a trade-off between the sensitivity and speed of the photodiode [151]. To reduce diode capacitance and carrier transit time while ensuring fast operations in the visible and near-infrared (NIR) wavelength ranges, photodiodes need to be reverse-biased at levels below their breakdown voltages [151]. Photodiodes take the largest portion of the photodetector market as they are widely used in many areas including sensing, imaging, patter recognition, telecommunications and security [183]. The most popular photodiodes are the p-

i-n, p-n junction, heterojunction and Schottky barrier photodiodes. The **p-i-n** (Fig. 2.8a) and **p-n junction photodiodes** (Fig. 2.8b) are considered very similar as the intrinsic layer in the p-i-n structure acts similar to the depletion region in the p-n junction photodiodes. During operation, electron-hole pairs generated inside the depletion region of these devices drift under the electric-field and are extracted at the external circuit to provide current. Part of the carriers generated outside the depletion region can diffuse into it provided that they are within the diffusion length, but those generated beyond the diffusion length recombine in the bulk [151]. **Heterojunction photodiodes** are based on a heterojunction formed between two semiconductors having different bandgaps as illustrated in Fig. 2.8c. The operation mechanism of these diodes is similar to that of the p-n and p-i-n diodes except that the photo-generated carriers in this case need to overcome the heterojunction barriers. Advantages of these devices over the others include good performance at long wavelengths, low dark current for materials with no lattice mismatch, and provide a *QE* that is not influenced by how far the junction is from the surfaces [151]. **Schottky barrier photodiodes** are based on Schottky junctions formed at metal-semiconductor interfaces and they are regarded as highly efficient and fast photodetectors due to their conductive metal layer that allows efficient carrier-collection [151, 182]. In these devices, carriers are generated via either band-to-band excitation or internal photoemission [151, 169]. Like in the other photodiodes, the first mechanism involves excitation of electrons from the valence to the conduction band of the semiconductor for $h\nu$ larger than the semiconductor's band-gap. The second mechanism, which is often used for extracting Schottky barrier height and studying hot electron transport in metals, involves emission of electrons generated in the metal over the Schottky barrier when $h\nu$ is smaller than the semiconductor's bandgap but still larger than the Schottky barrier height (Fig. 2.8d). For enhanced efficiency, the metal layer needs to be semi-transparent and also have a minimal surface reflection so that it does not block the light reaching the semiconductor. Although antireflection coatings on a semi-transparent metal surface minimizes reflection, they are wavelength specific and thus are not suitable for broadband operations. More recently, graphene is considered to alleviate these problems thanks to its single-atomic thickness, very high transparency for all light wavelengths and high conductivity [183].

2.3.4. Memristors

Computers have had a profound impact on mankind from every walk of life and have revolutionized the way we live and do things in this modern age. They have helped to facilitate the advancement of technologies we require in our day-to-day activities. Although the performance and sophistication of computers have grown exponentially over the years, their basic operation scheme is still based on the classical computational concept conceived by Alan Turing and implemented by John von Neumann more than half a century ago. This conventional computing architecture is known as the "von Neumann architecture" [202] in which the computing and memory blocks are physically separated from each other as illustrated in Fig. 2.9. The main drawback

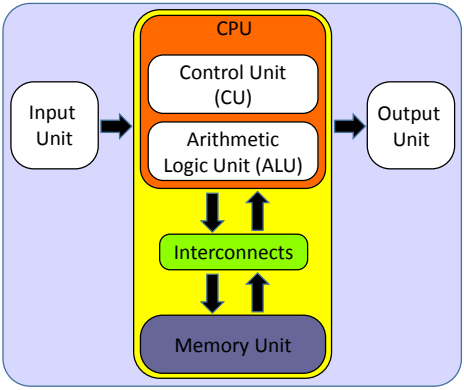

Figure 2.9: : Schematic diagram for the von Neumann architecture demonstrating the conventional computing scheme by computers where the arrows indicate the direction of data transfer between separate blocks, i.e. the central processing unit (CPU) and the memory unit.

of this architecture is the need for data shuttling between the two units which consumes the largest proportions of the total energy and time needed by a computer to perform a single computation. Nowadays, the fastly growing internet for things (IoT) leads to alarmingly increasing demand for computation, storage and communication/transfer of big data which in turn requires high energy use. However, the classical Si-based computing, which relies on the conventional von Neumann architecture, cannot keep up with this ever increasing demand due to

fundamental physical limits and the associated economical (i.e. high energy consumption and long computing time) and reliability issues. Hence, the limitations of the conventional computing paradigm are creating a bottle neck for advancements in application areas such as autonomous systems, bioinformatics, weather forecasting and robotics which all hugely rely on receiving, storing, processing and transferring massive data [203, 204]. This enormous demand has stirred the research and industrial communities' interest for radical thinking and triggered the quest for innovative post-von Neumann computing paradigms that can potentially redefine the principle of computing [203–205]. These highly aspired computing paradigms include nano-computing, molecular computing, optical computing, quantum computing and neuromorphic computing and they are collectively known as next generation computing [203]. Neuromorphic computing is inspired by the extremely efficient computing scheme of the human brain that performs parallel and real-time computations at a very small energy consumption (~20 Watt) [206]. Hence, it envisages replicating these functionalities through artificial neural systems built from electronic components [207]. The human brain is composed of about 86 billion neurons with about 100 trillion connections known as synapses [208]. The astonishing computing skills of the brain rely on the synaptic **plasticity** of these neurons, a feature enabling it to learn, adapt and process new information [209, 210]. Electronic elements with a potential to serve in a neuromorphic computer need to emulate this indispensable feature as a vital component for hardware-based neuromorphic computing systems. The primary examples for plasticity in electronic devices are memristors (memory resistors) which are two-terminal passive circuit elements that exhibit a reversible resistive switching (RS) behavior [184, 185]. They serve as electronic synapses in artificial neural networks made of electronic circuits to emulate the human brain's computing scheme. The RS behavior of memristors is characterized by two resistance state transitions, i.e. the high resistance state (HRS) to low resistance state (LRS) transition called SET and the LRS to HRS transition known as RESET. The bias-stress needed to trigger the SET transition is called the SET programming voltage (V_{SET}) and that required to initiate the RESET transition is similarly called V_{RESET}. Standard memristors have a vertical metal-insulator-metal (MIM) architecture with the insulator serving as the active switching medium and it is commonly made of redox-active materials such as transition metal oxides (TMOs)

or phase change materials (PCMs) [186, 187, 211–214]. The mecha-

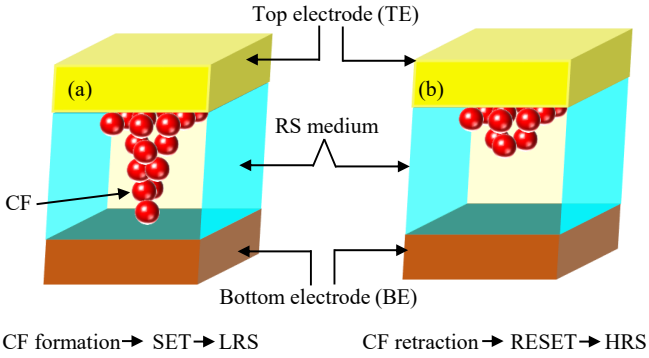

Figure 2.10: : Schematic illustration of a filamentary RS phenomenon in MIM memristors showing (a) conductive filament (CF) formation triggering the set process and leading to LRS and (b) CF retraction causing a reset process that leads to HRS.

nism for the RS in MIM cells is either filamentary or distributed (area-dependent) depending on the amount of space the atomic rearrangements responsible for the state change take during the electro-forming process [184, 213]. TMO-based memristors mostly exhibit filamentary RS where a thin conductive filament (CF) is formed and retracted in the body of the TMO to trigger the SET and RESET transitions, respectively. Although this type of switching can provide a high switching speed along with high LRS/HRS current ratio and excellent integration capability, it suffers from variability and high power consumption due to the CF formation. Distributed RS, on the other hand, does not offer as high a switching speed, but it features low power consumption and takes place in the RS medium homogeneously. The effect is mostly attributed to diffusion and interface phenomena [184, 212, 213]. Also, different types of electrical stresses are needed to induce the SET and RESET transitions in MIM cells of different switching medium. Therefore, depending on the type of electrical stress required, the RS phenomenon can be categorized as unipolar (V_{SET} and V_{RESET} have similar polarity) [213], bipolar (V_{SET} and V_{RESET} have opposite polarity) [213], nonpolar (V_{SET} and V_{RESET} can have any polarity) [215] and threshold switching (LRS is volatile and thus an automatic reset occurs when the bias stress is turned off) [184].

3

Experimental

The work in this thesis involved design and fabrication of devices, characterization of devices, analytical characterization of 2D material films and data analyses followed by interpretation of results. Except the last point, the rest are covered in this chapter.

3.1. Process Technology

This section describes the major semiconductor processes used during the fabrication of the devices investigated in this thesis. These include photolithography, physical vapor depositions such as evaporation and sputtering, reactive ion etching (RIE) as well as synthesis and transfer of 2D material films.

3.1.1. Photolithography

Photolithography (PL) is a fundamental microfabrication process through which geometric shapes on a mask are transferred to the surface of a target substrate. The general principle of a PL process starts with spin-coating of a light-sensitive polymer known as photoresist (PR) on a target substrate which then undergoes baking on hot plate followed by a selective photo irradiation through a pattern mask. This induces a modification in the molecular structure of the exposed part of the PR leading to a change in its solubility. As a result, the exposed PR in case

of a positive tone and the unexposed PR in case of a negative tone resist dissolves away inside a developer solution that is typically aqueous by nature [216]. The intended pattern is formed on the substrate by either deposition of a material or etching of the substrate on areas not covered by the PR. When a PL process is intended for contact pad formation for devices, a lift-off procedure needs to be carried out after the development step. This procedure involves deposition a metal on the developed sample followed by removal of the excess metal siting on places of the sample where the PR is still present. This is done by dissolving the PR inside a moderately heated acetone or other appropriate solvents so that the PR-supported metal is lifted-off and rinsed in subsequent isopropanol and DI-water baths. It is worth noting that results of a PL process are determined by interrelated parameters such as pre- and post-exposure baking (temperature and time) of the PR, light exposure dose (optical power and time) and development time.

3.1.2. Evaporation

Evaporation is a physical vapor deposition (PVD) technique that involves evaporation of a source material placed on a resistive heating filament or boat which is commonly made of refractory metals such as tungsten (W), molybdenum (Mo) or tantalum (Ta). The vapor particles condense on a cold substrate inside a high vacuum chamber ($<10^{-2}$ Pa) in order to avoid oxidation of the source [217]. Such a thermal evaporation process is mostly used for deposition of low melting point materials, while high melting point materials that are also highly sensitive are evaporated by an electron-beam (e-beam) heating in ultrahigh vacuum ($<10^{-6}$ Pa) utilizing crucibles made of quartz, graphite, alumina, zirconia etc. The e-beam can be generated either by thermionic emission or by field-effect cathodes. E-beam evaporation enables reaching high evaporation temperature and avoiding contamination by crucibles [217].

3.1.3. Sputtering

Like evaporation, sputtering is a PVD technique that is mostly used for deposition of metal and oxide films. It is a plasma-based process that takes place inside a confined high vacuum chamber where a target material is attached to a cathode electrode while a substrate holder located right below the target serves as the anode. Application of a high enough static (DC), alternating current (AC) or radio frequency

(RF) bias between the two electrodes ignites a plasma in the presence of a sputter gas, commonly argon (Ar) which becomes partially ionized. The energetic ions are accelerated towards the target and bombard it, ejecting atoms that gradually sediment on the substrate and eventually form a continuous thin film [218]. The deposition rate of this technique is controlled by the generator power and the flow rate of the sputter gas. The rear-side metallization of the devices demonstrated in this thesis were done by using a DC-sputtering process with an Ar sputter gas.

3.1.4. Reactive Ion Etching (RIE)

Reactive ion etching (RIE) is a dry etching technique widely used in micro/nanofabrication technology for patterning materials using chemically reactive plasma. A typical RIE system comprises a parallel plate inside a vacuum chamber, in the bottom portion of which lies a wafer platter that is isolated from the rest of the chamber electrically. Process gases enter the chamber through small inlets at the top and leave through an outlet at the bottom that leads toward the vacuum pump. An electromagnetic field is used to generate the plasma composed of energetic ions that attack a sample surface, react with it and also sputter components away [219]. Other types of RIE systems include inductively coupled plasma (ICP) RIE system in which a remotely coupled plasma is generated using an RF-powered magnetic field that provides high plasma densities albeit with a more isotropic etching profile. Hence, a combination of the parallel plate and ICP RIE appears more efficient as the high density plasma from the ICP enables increased etch rate while the separate RF bias applied to the substrate provides a more anisotropic behavior of the etch profile by creating directional electric fields near the substrate. In contrast to wet chemical etching processes, RIE provides anisotropic etching profiles owing to the mostly vertical delivery of the reactive ions [219]. The outcome of a RIE process is controlled by process parameters such as RF/ICP power, gas flow rate, chamber pressure and etching time.

3.1.5. Synthesis and Transfer of 2D Material Films

The performance and reliability of 2D materials-based devices hugely rely on the quality of the 2D films and the strategy followed to integrate them. Successful integration of the 2D films requires quality synthesis and transfer techniques. The 2D materials used in this thesis are MoS_2 and monolayer graphene. The MoS_2 films were synthesized

using the VPS/TAC technique, the general procedure of which is described in section 1.2.3. The sulfurization process was done for 30 minutes while heating the S-powder and the Mo-films at temperatures of ~150^{o}C and 800^{o}C, respectively. Ar carrier gas was flowing at 20 sccm in the direction from the S-source to the Mo samples while a growth pressure of ~2x10^{-3} mbar was maintained during the process. A schematic diagram illustrating this particular sulfurization process is given in Fig. 3.1. MoS_2 transfer was not required as the films were grown directly on the target substrates which gives a huge advantage by avoiding transfer induced defects and polymer contamination. The

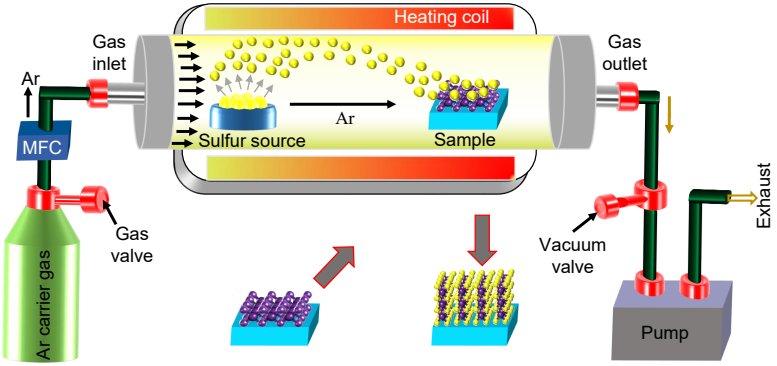

Figure 3.1: :Illustration of the sulfurization process accomplished to convert Mo into MoS_2 films.

monolayer graphene was synthesized on a Cu foil using a "Moorfield nanoCVD" tool that utilizes the principle of CVD which is described in section 1.1.3. The growth parameters used were: H_2/CH_4/Ar flow ratio = 80/5/15%, growth temperature = 950^{o}C, chamber pressure = 10^3 mTorr and growth time = 30 minutes. The graphene films were transferred onto the target substrates by using the wet chemical etching and electro-chemical delamination techniques described in section 1.1.4. After drying the samples overnight, they were baked at 180 ^{o}C for 30 minutes inside an oven. This baking step enhances the adhesion of graphene to the substrate and also expands the PMMA film in the meantime to ensure efficient removal in hot acetone (@75 ^{o}C) in about 45 min followed by additional 15 min cleaning in a fresh acetone, 10 min rinse in IPA, 5 min rinse in DI-water and finally drying using nitro-

gen gas.

3.2. Metrology

3.2.1. *Optical Microscopy (OM):*

Optical microscopy (OM) is widely used for quick examination of sample surfaces in a magnified view [220]. An integrated camera captures images from the OM and generates digital micrographs that provide useful information about the sample's surface [220]. The technique is also often used to inspect device fabrication processes in semiconductor labs. Furthermore, it can be used to examine the degree of uniformity/coverage, grain boundaries and presence of polymer residues and mechanically induced defects such as wrinkles, cracks, holes etc. in 2D material films, provided that these are transferred onto appropriate substrates and that appropriate light filters are used to provide sufficient contrast. Some examples of OM inspections performed in this thesis on MoS_2 and graphene samples are presented in Fig. 3.2.

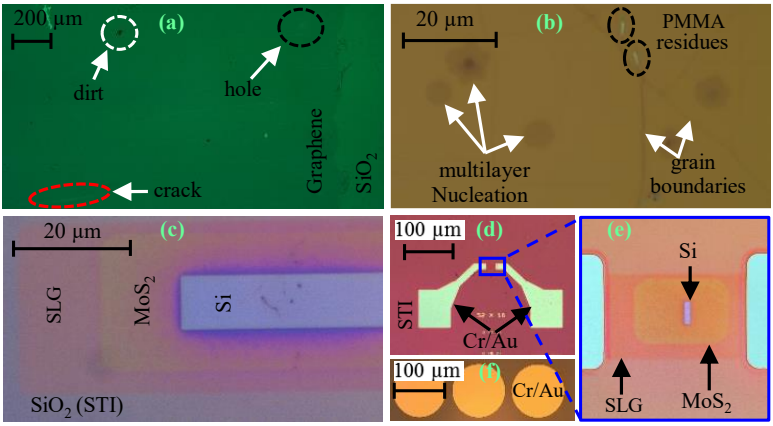

Figure 3.2: : Optical microscopy inspections: (a), (b) show optical micrographs of single layer graphene (SLG) on SiO_2 revealing grain boundaries and multilayer nucleation centers from the Cu growth substrate and the synthesis process. The images also revealed polymer residues, cracks and holes induced by the transfer process. (c) Show an optical micrograph of a MoS_2/SLG heterostructure on a Si active area which is surrounded by SiO_2. (d) and (e) contain micrographs of a fully fabricated Si/MoS_2/graphene heterojunction diode in which both 2D films are distinctly identifiable. (f) Shows an optical micrograph of a Si/MoS_2Cr capacitor.

3.2.2. *Scanning Electron Microscopy (SEM):*

Although OM provides a detailed view of samples which is not achievable by the human naked eyes, the level of magnification and resolution it offers are still not sufficient for inspecting sub-nanometer features. Scanning electron microscopy (SEM) is a convenient technique to bridge this gap. It generates images of a sample by scanning its surface with a focused beam of high-energy electrons that interact with atoms at the surface and produce signals comprising backscattered electrons, secondary electrons, diffracted backscattered electrons, X-rays etc. These signals provide information about the morphology, crystalline structure, orientation and chemical composition of the surface [220]. SEM morphology/topography images are created by map-

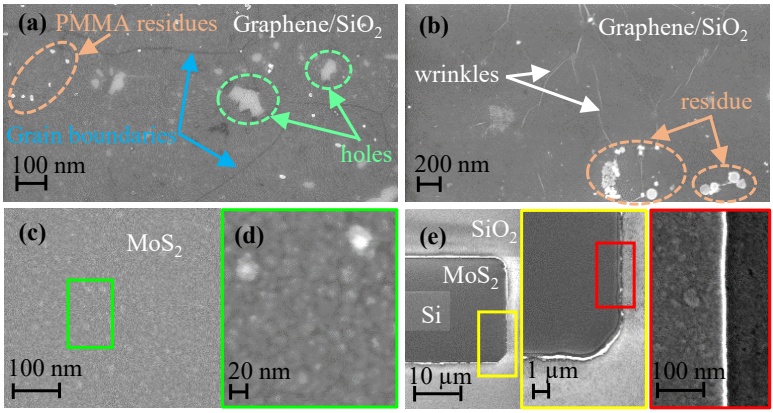

Figure 3.3: : Scanning electron microscopy (SEM) investigations on: (a), (b) graphene on SiO_2 showing grain-boundaries, cracks, wrinkles and PMMA residues. (c) SEM image of as-grown MoS_2 film confirming the homogeneity of the film as can be seen better in (d) and (e) shows SEM images of the MoS_2 film with subsequent magnifications on selected parts.

ping the detected secondary and backscattered electron signals with respect to the beam's position during the scan. The significant advantage of SEM over OM comes from its much higher depth of focus and resolving power owing to the much higher energies (i.e. much shorter wavelengths) of the electron beam used compared to that of the visible light in OM. As a result, SEM provides a magnification and resolution of up to $150x10^3$X and < 8 nm, respectively, while OM gives only $1.5x10^3$X

and only >200 nm. In this thesis work, SEM investigations were carried out to examine surface morphologies of the as grown MoS_2 and transferred graphene films (Figs. 3.3a-e). The images in these figures outline the level of homogeneity and coverage of the MoS_2 films and transfer-induced mechanical defects in graphene.

3.2.3. *Transmission Electron Microscopy (TEM):*

Transmission electron microscopy (TEM) is an important technique that provides atomic resolution of materials. Similar to SEM, TEM employs a focused beam of electrons that irradiates a sample and interacts with its atoms to generate a signal which is used to construct an image that is magnified and focused onto an imaging device such as a CCD camera [220]. However, in contrast to SEM, the electrons are transmitted through the body of the sample in TEM, making it a favorable technique for structural analysis of sample cross-sections. The contrast in TEM images is a result of electron absorptions in the sample based on its composition and thickness, but it is influenced by complex wave interactions at higher magnifications [220]. TEM can be used to determine crystal orientations and sample-induced electron phase shifts as well as chemical compositions and electronic structures of materials. Unlike the techniques described above, TEM requires a sample prepa-

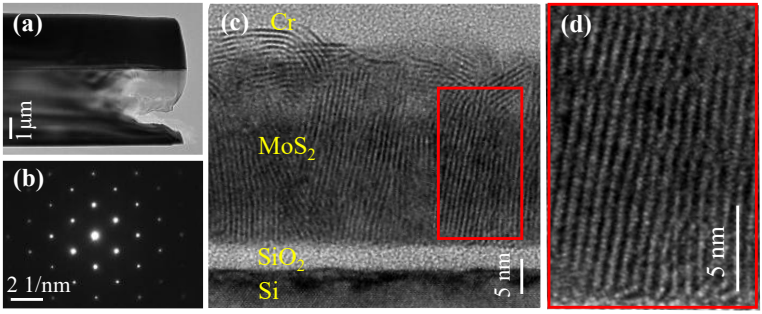

Figure 3.4: Transmission electron microscopy (TEM) investigations on the as-grown MoS_2 film embedded between Si and Cr: (a) shows the lamella carved out of the sample with a FIB technique, (b) an electron diffraction pattern indicating the crystalline nature of the layers in the sample, (c) a TEM cross-section image in which the samples structural composition is clearly delineated. The image also shows that the MoS_2 is polycrystalline and that the layers have a predominant vertical orientation. (d) Shows a magnified view of the MoS_2 part marked by the red box.

ration process which involves carving out of very thin lamellae from the sample using the focused ion beam (FIB) technique. TEM investigations were conducted in this thesis work on Si/MoS_2/Cr samples using a FEI Tecnai G2 F20 TEM system at an acceleration voltage of 200 kV. The required TEM lamellas were prepared in an FEI Helios NanoLab 400S FIB-SEM system and then cleaned with Ar ions at 500 eV in a process called NanoMill to remove amorphous layers formed due to the FIB irradiation. One of the lamellas prepared is shown in Fig. 3.4a. The electron beam irradiated perpendicular to the lamella surface gives the diffraction patter shown in Fig. 3.4b indicating the crystallinity of the materials in the Si/MoS_2/Cr structure. The TEM cross-section image acquired from the investigation and a magnified view of the MoS_2 part are given in Figs. 3.4c and d, respectively. The TEM investigations were done in collaboration with Maximilian Kruth in Prof. Joachim Mayer's group at Jülich Research Center, Ernst Ruska-Centre for Microscopy and Spectroscopy with Electrons (ER-C).

3.2.4. *Atomic Force Microscopy (AFM):*

Another very powerful technique which is used for investigating surface morphologies and nanoscale structures is atomic force microscopy (AFM). An AFM device comprises a laser source, a very sharp and delicate tip attached to an elastic cantilever which is turn connected to a piezoelectric arm, an electronic feedback circuit and a position sensitive photodiode (PSPD) that detects a laser beam reflected from the cantilever. During sample inspection, the tip scans over the sample's surface when appropriate voltages are applied to the piezoelectric to drive the cantilever in x, y and z directions. When the tip touches the surface, it experiences a Van der Waals force whose magnitude is proportional to the tip-to-sample distance. The electronic feedback circuit maintains the tip-to-sample distance during the scan and the upward and downward bending of the cantilever lead to a displacement of the reflected laser beam which translates into the spatial position of the tip with respect to the sample surface. Unlike many other surface monitoring techniques, AFM is limited neither by the type of material surface to be investigated nor by the type of environment in which the measurement is to be carried out [221]. This versatile behavior allows researchers to analyze any material surface in either air, vacuum or even liquid environments. In semiconductor technology, AFM is utilized to obtain information about surface properties of a sam-

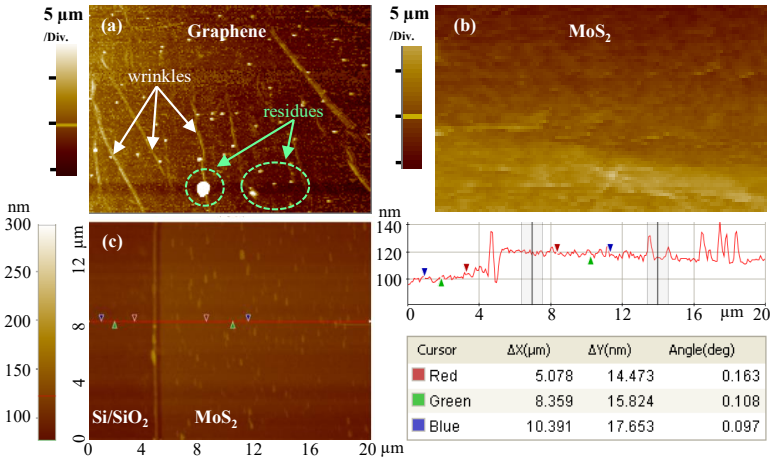

Figure 3.5: : (a) Atomic force microscopy (AFM) topography images on single layer graphene showing the surface morphology with clear signs of wrinkles and polymer residues, (b) a similar measurement on a sample with layered MoS_2 indicating a very homogeneous/continuous film and (c) a topography scan on the MoS_2 film with respect to the underlying SiO_2 substrate with a line profile confirming the MoS_2 film thickness of ~15 nm.

ple such as texture/morphology, topography, roughness, impurities, friction, surface potential distribution etc [221]. It is also an efficient technique to acquire high-resolution nanoscale images and to determine thicknesses of ultrathin films with high precision. In this thesis, graphene and MoS_2 films were analyzed using AFM (Fig. 3.5). The 23 µm x 23 µm topography scan on the as-transferred graphene film (Fig. 3.5a) has clearly outlined features such as wrinkles and residues and the scan on the as-grown MoS_2 film show a homogeneous film with full coverage (Fig. 3.5b). Furthermore, a topography scan was performed across the edge of the MoS_2 film on a 20 µm x 20 µm area as depicted in Fig. 3.5c and a line profile from this data confirmed that the thickness of the film is about 15 nm.

3.2.5. *Raman Spectroscopy (RAMAN):*

Raman spectroscopy is a non-invasive characterization technique in which an incident laser light interacts with molecules of a sample whose

vibrations cause the small portion of the incident light to scatter at a different wavelength [222]. The resulting wavelength shift is strongly

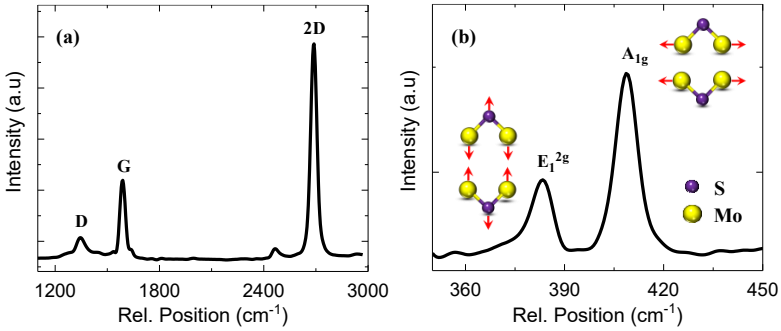

Figure 3.6: : Raman spectroscopy measurements on (a) graphene and (b) MoS_2 samples confirming a good quality monolayer graphene and a 2H-MoS_2 phase formation, respectively.

influenced by the vibrational energies of the molecules, making it the material's unique signature [222]. A Raman data is generally presented as the scattered light intensity as a function of wavenumber, which is an inverse of wavelength, where the peaks in the spectrum correspond to the allowed vibrational modes of the molecules of the material under study. Presence and quality of the 2D material films used in this thesis (i.e. graphene and MoS_2) were inspected by a WITec alpha 300R Raman system that uses a 532 nm wavelength laser at a power of 1 mW. The acquired Raman spectra are given in Fig. 3.6. The first spectrum (Fig. 3.6a) confirmed the presence of graphene through the characteristic "D", "G" and "2D" excitation modes that occur at around 1350 cm^{-1}, 1590 cm^{-1} and 2685 cm^{-1}, respectively. The exhibited very small D-to-G intensity ratio indicates a good quality graphene while the sharp and intense 2D peak with a 2D-to-G intensity ratio larger than 1 indicates its monolayer nature [223,224]. The second Raman spectrum shown in Fig. 3.6b exhibits two prominent peaks at about 384 cm-1 and 409 cm-1, respectively. These peaks correspond to the $E^1{}_{2g}$ and $A^1{}_g$ excitation modes, respectively, confirming a 2H MoS_2 phase formation [132,225]. While the $E^1{}_{2g}$ band results from the in-plane vibration of Mo and S atoms, the $A^1{}_g$ band is due to the out-of-plane vibration of S atoms with respect to the Mo atoms [224,225]. Furthermore, the large $A^1{}_g$-to- $E^1{}_{2g}$

intensity ratio shows a preferred out-of-plane vibration indicating the formation of edge-terminated MoS_2 layers with a vertical orientation [27, 141], consistent with the TEM result in Fig. 3.4c and d.

3.2.6. *Time-oF-Flight Secondary Ion Mass Spectroscopy (ToF-SIMS):*

ToF-SIMS is a surface microanalysis technique which is highly sensitive to nearly all elements and is also applicable to any type of vacuum-compatible material [220]. ToF-SIMS is a destructive technique as it

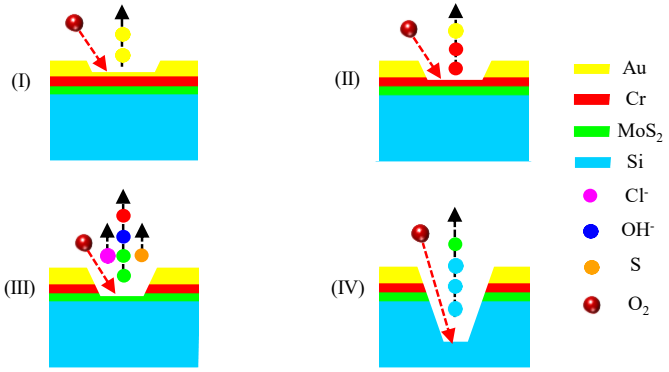

Figure 3.7: Illustration of the process of time-of-flight secondary ion mass spectroscopy (Tof-SIMS) analysis on Si/MoS_2/Cr/Au structures where the Roman numerals I-IV represent the different depth profile sampling stages.

involves bombardment of the sample by primary ions that are accelerated at energies of a few keV to knock out secondary particles [220]. A fraction of the knocked out particles are ionized to become secondary ions and fly into a detector. These are analyzed by a mass spectrometer that accounts for their masses and the amount of time it took them to reach the detector (i.e. time-of-flight), hence the name ToF-SIMS. Being a surface technique, ToF-SIMS provides information only from the uppermost atomic layers of the sample. Nevertheless, it is an efficient and a reliable technique to determine the elemental, isotopic and molecular composition of materials. The elemental/molecular compositions of the "Si/MoS_2/Cr/Au" structures of this thesis were investigated through ToF-SIMS depth profile measurements in the negative ion mode [27]. The measurement procedure started by sputtering a 500

μm x 500 μm spot on the samples by using O_2 ions accelerated at 5 keV to form a clean and contamination-free crater and ensure error-free measurements. Then, following a pre-sputtering step to clean surfaces, subsequent depth profile measurements were done on a 200 μm x 200 μm area in the center of the larger crater using bismuth ions (Bi^+) at 25 keV as illustrated in Fig. 3.7.

3.3. Device Design

The layout design software "KLayout" was used to design the devices that were investigated in this thesis. Figs. 3.8(a) and 3.8(b) show the designed layouts with all the layers overlaid on top of each other to give a full representation of the device structures. The layouts are then arranged such that they all lie within the region of the physical mask that is easily accessible during the photolithography process, i.e. considering factors such as the opening of the mask holder and the XY displacement ranges of both the sample stage and the microscope of the mask aligner where the mask will be fitted during use. Finally, a mask production company fabricates the mask based on the compiled layout file by defining the designed structures using a light-reflective chromium layer on a transparent quartz glass. A photograph of an example mask is shown in Figs. 3.8(c) and (d) to provide a visual impression.

3.4. Device Fabrication

The devices presented in this thesis include capacitors, memristors, heterojunction diodes and photodetectors based on graphene and MoS_2. The fabrication processes for these devices are described below.

3.4.1. *Fabrication of MoS_2-Based Capacitors and Memristors:*

The fabrication process for these devices began with a standard cleaning procedure that was employed on n- and p-type Si (100) substrates. After this step, a hydrofluoric acid (HF) treatment was done to remove the native oxide on the surfaces, followed by deposition of a homogeneous layer of ~5 nm Mo thin films using e-beam evaporation. The Mo films were then transformed into ~15 nm MoS_2 by using the VPS/TAC technique (see section 1.2.3). Then, windows of various shapes (square and circular) and dimensions (100 – 400 μm in diameter) were defined

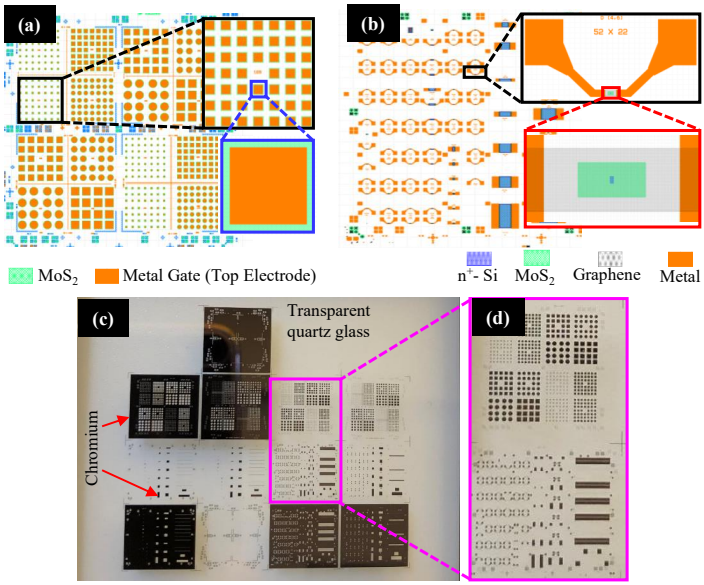

Figure 3.8: : Layout designs showing top-views of: (a) Si/MoS_2/Metal structures and (b) n^+-Si/MoS_2/graphene structures that are analogous to the emitter diode of GBTs comprising n^+-Si emitter, MoS_2 EBI (emission barrier) and graphene base. (c) Photograph of the physical mask on which the layouts for all layers of the complete devices indicated in (a) and (b) are printed on a transparent quartz glass using a chromium light-reflective layer. The magnified section displayed in (d) corresponds to the top-most layers of the designs in (a) and (b).

on top of MoS_2 through a photolithography process. Next, a stack of 20 nm chromium (Cr) and 120 nm gold (Au) metal gates were formed on the defined windows through subsequent processes of thermal evaporation and lift-off. Finally, after a native oxide removal in a diluted HF solution, Cr/Au back contact was deposited on the rear side of the Si substrates by using a magnetron sputtering tool.

3.4.2. *Fabrication of MoS_2 - and Graphene-Based Diodes and Photodetectors:*

The fabrication process for these devices had two phases: (1) the wafer-scale substrate preparation [226] which was done by IHP GmbH in a pilot line and (2) the chip-scale device fabrication which was done

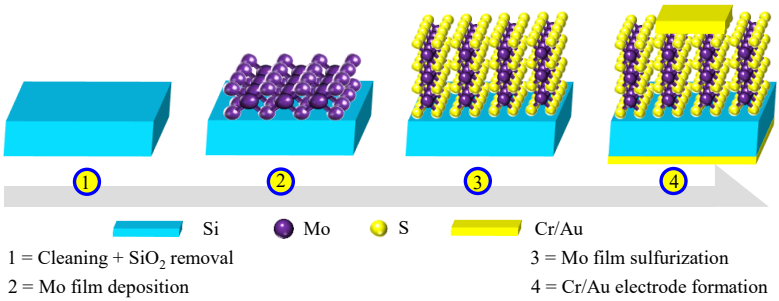

Figure 3.9: : Schematic diagram illustrating the fabrication process flow for MoS_2-based capacitor and memristor devices.

by me as part of this thesis work. In the first phase, 200 mm n-type Si (100) wafers were first patterned through subsequent steps of photolithography and reactive ion etching (RIE) of the Si. Then, the etched trenches were filled by a ~400 nm high density plasma CVD (HDP-CVD)-deposited silicon dioxide (SiO_2) layer to form Si pillars of various dimensions and aspect ratios surrounded by the SiO_2 layer. The SiO_2 serves as a shallow trench isolation (STI) for neighboring devices and it also prevents direct current leakage from the metal contacts into the Si underneath or vice versa. Then, the surfaces of the wafers were planarized using chemical mechanical polishing (CMP) technique to ensure reasonably planar surfaces. Finally, locally doped n^+-Si active regions were created on the Si pillars through phosphorous ion implantation. The second phase started by dicing the wafers into 1.5 cm x 1.5 cm chips. After a standard cleaning procedure, a photolithography step was employed to define windows on top of the n^+-Si active areas for MoS_2 growth. Afterwards, a 7:1 buffered oxide etch (BOE) solution was used for native oxide removal from the n^+-Si surface. Immediately after that, ~ 5 nm Mo films were deposited on the samples via e-beam evaporation and patterned through a lift-off process. Then, the patterned Mo films were sulfurized into ~ 15 nm MoS_2 using the VPS/TAC technique. In the following step, a CVD grown monolayer graphene was transferred on top of the MoS_2 films using the wet chemical etching technique (see chapter 1). After removing the PMMA film, which was used as a supportive layer, the graphene film was patterned through a step of photolithography followed by RIE in oxygen (O_2) plasma. Then,

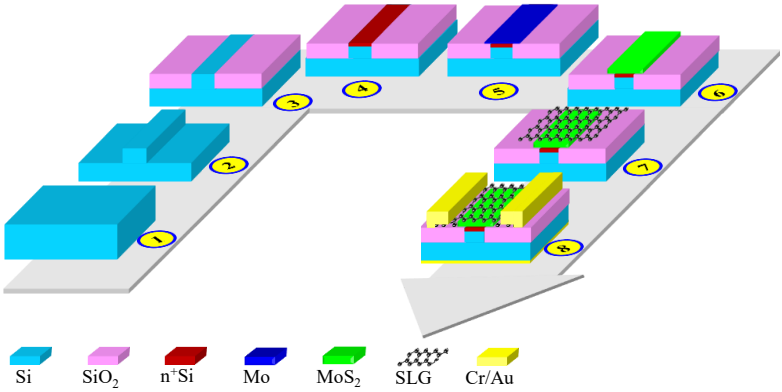

Figure 3.10: : Illustrative schematic diagram showing the fabrication process flow of MoS_2-and single layer graphene (SLG)-based diodes and photodetectors. The numbers represent key process steps involved, i.e. 1= standard cleaning of n-type Si substrates, 2=reactive ion etching of Si to form shallow trenches (~400 nm), 3= HDPCVD of undoped silicon glass (USG) in the trenches followed by a CMP process, 4= phosphorous ion implantation, 5= deposition of ~5 nm Mo film, 6= sulfurization of the Mo film to obtain ~15 nm MoS_2, 7= transferring and patterning the SLG and 8= metallization. The substrate preparation (i.e. process steps 1-4) was done by IHP GmbH, whereas the device fabrication process (i.e. the rest of the process steps indicated in the diagram) were done by me.

following native oxide removal using BOE, metal contacts were formed to the graphene layer by carrying out a photolithography process followed by deposition of 20/120 nm Cr/Au stack by thermal evaporation. After a lift-off process, an additional round of Cr/Au deposition was done on the rear side of the Si substrates to ensure an Ohmic contact to the Si bulk. The overall fabrication process flow is illustrated in Fig. 3.10 using schematic diagrams with isometric-views.

3.5. Device Characterization Methods

After fabrication of the devices, different characterization techniques were employed to examine their electrical, memristive and optical functionalities. This part of the thesis is dedicated to give readers an overview of the variety of device characterizations carried out.

3.5.1. Electrical Characterizations

Capacitance-Voltage (C-V) and Conductance-Voltage (G-V) Characterizations:

C-V and G-V measurements were conducted on Si/MoS_2/Cr capacitors in vacuum (~10^{-4}) at room temperature (RT) by using a Keithley KI-590 admittance analyzer which is connected to a Lakeshore CRX-6.5K cryogenic probestation. The measurements were done by superimposing a 25 mV AC probe signal of 100 kHz frequency to a DC bias that is applied to the metal top gate while the bottom electrode is on ground as shown in Fig. 3.11a. Apart from the standard C-V and G-V measurements, subsequent bias-stress (BS) measurements were also carried out in such a way that a 1min BS with ±4 V is immediately followed by a C-V measurement with the fastest possible scan rate (i.e. 1 ms between data points). This procedure is repeated for several cycles until the C-V/G-V curves do not show any observable shift. This measurements help to understand the charge dynamics inside the dielectric and at the interfaces.

Current-Voltage (I-V) Characterizations:

Room temperature (RT) and temperature-dependent current-voltage (I-V) measurements were done on Si/MoS_2/Cr capacitors and Si/MoS_2/graphene heterojunction diodes, respectively. A Lakeshore CRX-6.5K cryogenic probestation configured with a Keithley 4200 SCS parameter analyzer and a Lakeshore 336 temperature controller was used for the measurements. The sample temperature was varied in the range of 200 K – 300 K with intervals of 20 K during temperature-dependent measurements. All the I-V measurements in this thesis were carried out in a static (DC) mode by using configurations shown in Fig. 3.11a and Fig. 3.11b (without the light source). Also, the measurements were always done by sweeping from zero to positive and from zero to negative to avoid the effect of displacement current at 0 V that often arises when sweeping directly from negative to positive voltage or vice-versa.

3.5.2. Resistive Switching (RS) Characterizations

Studying the MoS_2 memristors and evaluating their performance require electrical measurement schemes that effectively demonstrate their resistive switching (RS) functionality. In this regard, I-V sweeps, endurance tests and state-retention tests were conducted at RT in both ambient and vacuum conditions by using a configuration similar to

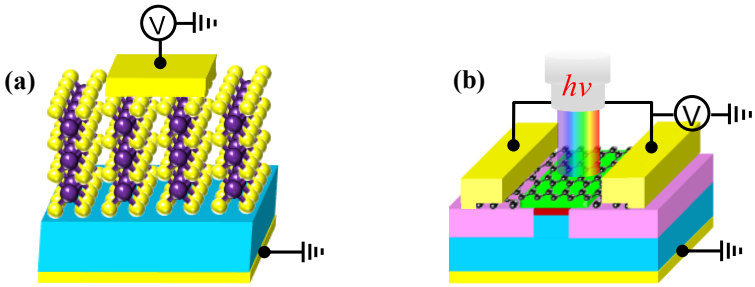

Figure 3.11: : Device schematics with wiring setups used for electrical measurements of the (a) Si/MoS_2/Cr/Au and (b) Si/MoS_2/graphene structures.

what is shown in Fig. 3.11a.

I-V Sweeps:

I-V sweeps were performed to quickly check for hysteretic behavior indicating a potential RS phenomenon. They were carried out in such a way that current was recorded while sweeping the top electrode bias (V_{TE}) in four steps, i.e. step-1 = from zero to -V_{TE}, step-2 = from -V_{TE} back to zero, step-3 = from zero to +V_{TE} and finally step-4 = from +V_{TE} back to zero. The SET and RESET transitions were observed during the steps 1 and 4, respectively. These measurements are also useful to determine the nature of the RS behavior and the corresponding operation window to efficiently design more advanced measurement routines to further investigate the switching behavior.

Endurance Tests:

Once the presence of RS is demonstrating through I-V sweeps, the switching performance is further investigated through endurance tests. Endurance is among the figures of merit (FOM) for RS and it measures how many times a memristor device can be switched back and forth while still maintaining an acceptable switching ratio [184, 227]. The endurance tests were accomplished by subsequent current-time (I-t) measurements in which current levels were read (at a READ voltage of -1.5 V) over time following a SET and RESET programming voltages (-3.5 V and +4 V, respectively) applied on the top electrode for 2 s. These measurements were then repeated for over 100 manual DC switching cycles in a Keithley 4200SCS parameter analyzer. Finally, the resistance

values of each cycle were calculated from the corresponding current values and plotted as a function of switching cycle to provide the endurance graph.

State-Retention Tests :
In addition to endurance, it is also vital to evaluate the non-volatile nature of the RS behavior of memristors if they are to be used for memory applications. The FOM which is commonly used to assess this particular property is state-retention, which is a measure of how stable are the resistance states of a RS device over a period of time [184, 227]. State-retention tests were carried out on the MoS_2 memristors demonstrated in this thesis by using the following procedure. First, a SET programming BS of -4 V is applied on the TE for 2 s followed by repeated readout. Then, a RESET programming BS of +4 V is applied for 2 s followed by another repeated readout. The resistance values obtained from the successive readouts are the plotted as a function time to provide a state-retention graph.

3.5.3. Opto-Electrical Characterizations
To investigate the optical sensitivity of the Si/MoS_2/graphene heterojunction diodes, it was necessary to conduct opto-electrical measurements, i.e. measuring electrical current created by either white- or monochromatic-light irradiated on the samples. The details of these measurements are given in this subsection.

I-V Measurements with and without Light Irradiation :
As a first and quick way of examining the functionality of the heterojunction diodes as a photodiode/photodetector, I-V measurements were done under dark and white light illumination conditions (Fig. 3.11b). The difference between the two measurements provide the photocurrent (I_{ph}) as a function of applied bias. A probestation with a halogen lamp light source and a Keithley 4200SCS parameter analyzer was used to conduct these measurements in ambient conditions.

Spectral Responsivity (SR) Measurements:
A lock-in technique was employed to further investigate the optical responsivity of the devices in a LabVIEW-controlled optical setup using a chopped monochromatic light in contrast to the earlier measurements. The setup encompasses tungsten-halogen and deuterium-arc

lamps to generate light, a monochromator to select a desired wavelength, an optical chopper to modulate the intensity of the light beam, a beam splitter and "FEMTO DLPCA-200" pre-amplifiers along with "Princeton Applied Research Corporation 5210" lock-in amplifiers to measure ultralow current (Fig. 3.12). The lock-in amplifiers operate at

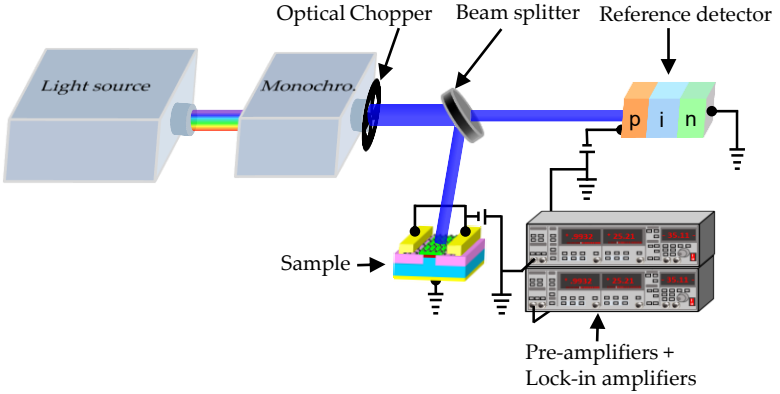

Figure 3.12: : A sematic representation of the optical setup used to measure the spectral responsivity (SR) of the Si/MoS_2/graphene heterojunction photodetectors in this thesis.

a band width and integration time of 0.4 Hz and 300 ms, respectively, and also match the operation frequency of the chopper (i.e. 17 HZ). The wavelength (λ) of the generated light in this setup ranges from 350nm to 2200 nm and the corresponding power density varies between 1 μ $Wcm^{\neg 2}$ and 55 μ $Wcm^{\neg 2}$. To avoid errors, measurements were calibrated by using commercially available reference detectors (Si and Indium-Gallium Arsenide (InGaAs) photodiodes), where the SR is precisely known. The SR of the devices were then calculated from the measured photocurrent data by using the LabVIEW program using Eq. 2.15 (see chapter 1). The program also employs a λ-dependent correction factor that accounts for variations among the preamplifiers, variations in the photo-flux density due to grids and filters in the monochromator and area difference between the measured devices and the reference detectors.

4

Dielectric Properties and Ion Transport in Layered MoS_2

Device applications targeted by this thesis have been the development of emitter diodes for GBTs, photodetectors and memristors based on in-house grown MoS_2 films. The MoS_2 has been used as the emitter-base barrier in the GBT emitter diodes, as the main photoactive layer in the photodetectors and as the active switching medium in the memristors. A primary milestone set to reach this ultimate goal has been the investigation of the material from a dielectrics perspective and understanding its properties. In this regard, investigating the dielectric properties of MoS_2 as a barrier material has been a primary task considering the enormous impact these have on device performance. Si/MoS_2/metal capacitor structures where MoS_2 serves as the insulator (Fig.4.1a) were fabricated for this purpose and admittance spectroscopy studies were conducted to learn about the dielectric properties of the material. The study helped to gain insights into the Si/MoS_2 heterojunction, the corresponding band alignment, the MoS_2 dielectric constant, the interface states at the Si/MoS_2 interface and the presence of mobile ions inside the MoS_2 film. These are addressed in this chap-

ter.

4.1. The Si/MoS_2 Heterojunction

The Si/MoS_2 heterojunction is the essential part of the devices' structure. According to a TEM analysis on Si/MoS_2/Cr/Au structures which is presented in section 3.2.3 and also reproduced here in Fig.4.1b, a very thin (~ 2.5 nm) SiO_x interfacial layer (IL) has formed between Si and MoS_2 during the Mo sulfurization process. Similar observations have been previously reported in relation to MoS_2 growth on Si [142, 228]. One possibility for the IL formation in the present case could be a regrowth of the native oxide during the time interval between the HF treatment and the Mo film deposition steps. Another possibility might be that following the heating of the sample during the Mo sulfurization process (see section 3.1.5), the oxygen escaping from water molecules trapped between Si and Mo oxidizes the Si surface. Also, the two processes may coexist and facilitate the IL formation. The IL is of poor quality potentially due to oxygen vacancies and similar defects favoring current leakage. This is confirmed by the experimental observation that the measured leakage current of the present structures (Fig.4.1c) is almost three orders of magnitude higher than that reported for standard thermally grown SiO_2 with similar thickness and applied DC bias [229]. This suggests that the IL is very permeable to charge carriers under DC bias, making its influence on the charge carrier transport across the Si/MoS_2 junction negligible. Therefore, it is omitted from all band schemes presented in this dissertation.

4.1.1. Band Alignment

The band alignment at the Si/MoS_2 junction and the magnitude of the corresponding energy barrier height can be considered to lie between two extreme scenarios. The first scenario assumes that the affinity rule entirely determines the energy band alignment such that a "Type-I" (straddling) gap forms at the junction and thus the difference between the electron affinities of Si and MoS_2 defines the barrier heights [230]. In the second scenario, the band alignment is assumed to be dictated mainly by "virtual gap states". This would lead to a formation of a "Type-II" (staggered) gap in which the hole-barrier becomes substantially larger than the electron-barrier [230], which is in accordance with the observation of the leakage current in Fig.4.1b. However, in reality, it

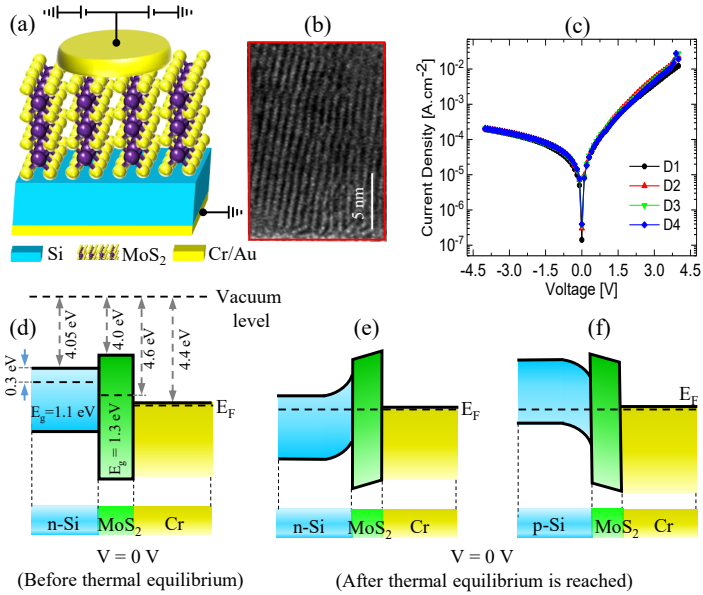

Figure 4.1: (a) Schematic of a Si/MoS_2Cr/Au capacitor with a wiring setup, (b) TEM cross sectional image of a Si/MoS_2/Cr/Au structure showing a predominantly vertical orientation of the 2D MoS_2 layers, (c) I-V characteristics of several devices (D1-D4) showing the level of forward and reverse bias leakage current across the devices. Band schemes illustrating band alignments of the structures (d) before thermal equilibrium is reached and (e), (f) after thermal equilibrium is reached with a focus on n-Si/MoS_2- and p-Si/MoS_2-junctions, respectively.

is more reasonable to expect a combination of the two scenarios [231]. Also, as will be discussed in the next chapter, the presence of negative charges close to the Si/MoS_2 junction may introduce bending in the MoS_2 energy bands and establish an additional barrier for electrons [27]. Based on this reasoning, simplified energy band schemes of the Si/MoS_2/Cr/Au structures are proposed in Figs.4.1d-4.1f.

4.2. Dielectric Properties of the Layered MoS_2

To investigate the dielectric constant and other dielectric properties of MoS_2, "Si/MoS_2/Cr/Au" structures were fabricated on both n- and p-type Si substrates and high frequency (HF) C-V measurements were

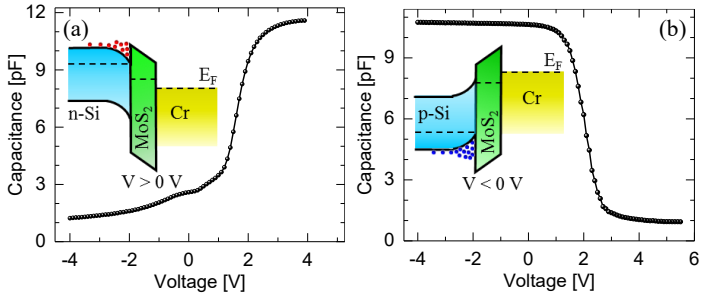

Figure 4.2: C-V characteristics of MoS_2 capacitors on (a) n- and (b) p-type Si substrates at a probe signal frequency of 100 kHz. The insets in both graphs illustrate the band schemes with the devices biased in accumulation. These results suggest a larger hole-barrier than the electron-barrier at the Si/MoS_2 junction.

conducted as described in sections 3.5.1. The HF C-V characterizations were carried out in such a way that the capacitance is measured by an impedance analyzer while superimposing a very small (~25 mV) AC probe signal of 100 kHz frequency to a DC sweep applied on the metal gate.

4.2.1. Dielectric Constant

Figs.4.2a and 4.2b display that the shapes of the C-V characteristics obtained from the present devices bear a resemblance to that of the classic MOS capacitors [151, 152, 156]. The capacitance saturations exhibited by the C-V characteristics confirm the presence of electron- and hole-barriers that are large enough to accumulate electrons and holes, respectively, at the Si/MoS_2 junction. The characteristics from the p-type samples exhibit a capacitance saturation spanning over a large voltage range while the saturation in the n-type samples exhibits a shorter voltage span due to a dominating leakage current arising for biases above 4 V. This suggests that the hole barrier in the structures is reasonably larger than the corresponding electron barrier and the overall observation support the proposed band diagrams in Figs.4.1a and 4.1b. Following the commonly used classical approach [152], the saturated part of the C-V characteristics is used to extract one of the most important dielectric properties of materials, the dielectric constant for the VPS/TAC-grown layered MoS_2. This was accomplished by

using

$$C_{ins} = \frac{C_{SiO_x} C_{MOS_2}}{C_{SiO_x} + C_{MOS_2}}, \tag{4.1}$$

where C_{ins} denotes the insulator capacitance analogous to the oxide capacitance in conventional MOS capacitors, C_{SiO_x} is the IL capacitance and C_{MoS_2} is the MoS_2 capacitance. Here, C_{ins} represents the saturated (voltage-independent) part of the measured C-V characteristics and is considered as the equivalent capacitance of the MoS_2 and SiO_x capacitors that are configured in series. Recalling the model for the voltage-independent oxide capacitance given in Eq. 2.5 of chapter 2 and solving Eq. 4.1 for ϵ_{MoS_2}, one obtains the expression

$$\epsilon_{MoS_2} = \frac{C_{ins}\epsilon_{SiO_x} t_{MoS_2}}{\epsilon_0 A \epsilon_{SiO_x} - C_{ins} t_{SiO_x}}, \tag{4.2}$$

where ϵ_{MoS_2} is the dielectric constant of MoS_2, $\epsilon_{SiO_x} = 3.9$ is the dielectric constant of the interfacial silicon oxide layer, $t_{MoS_2} = 15nm$ is the thickness of MoS_2, $t_{SiO_x} = \sim 2.5nm$ is thickness of the interfacial silicon oxide layer, $\epsilon_0 = 8.85x10^{-12} F/m$ is the permittivity of vacuum and A is the capacitor area = 7850 μm^2. Therefore, the dielectric constant values extracted from the measured data using Eq. 4.2 fall in the range of 2.6 – 2.9, which is in reasonable agreement with the dielectric constant value of ~3 predicted by Santos and Kaxiras [232] for an electric-field range similar to the one where the C-V saturations in Fig. 4.2 occur. The authors demonstrated the electric-field and thickness dependence of the MoS_2 dielectric constant. Here, it is worth noting that the theoretical prediction assumes a monocrystalline MoS_2 containing horizontally aligned layers while the experiment in this work is based on nanocrystalline MoS_2 films with vertically aligned layers and, therefore, the small discrepancy between the two may be expected.

4.2.2. Mobile Ions

The C-V characteristics in Fig. 4.2 show that the V_{FB} of both "n-Si/MoS_2/Cr/Au" and "p-Si/MoS_2/Cr/Au" capacitors has shifted to the right by the same amount, indicating a similar concentration of negative charges inside the MoS_2 films of the two samples. The devices were investigated through measurements involving electric-field stress, which will be referred to as bias-stress (BS) measurements hereafter, to further understand whether these charges are fixed or mobile. The general procedure of these measurements can be found in section 3.5.1. BS C-V and G-V measure-

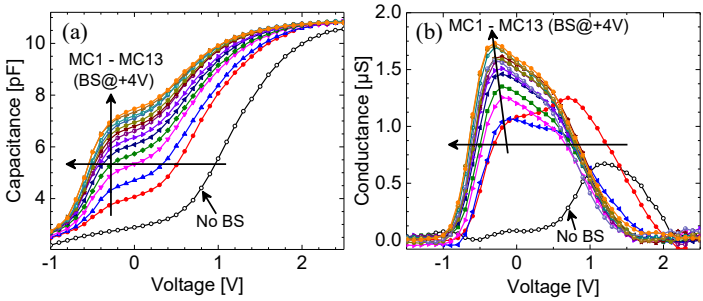

Figure 4.3: C-V and G-V measurements carried out on n-Si/MoS_2/Cr/Au capacitors following subsequent positive bias-stresses (+BS) of +4 V applied for 1 minute: (a) C-V and (b) G-V characteristics exhibiting parallel (left) and vertical (upward) shifts of the curves on the voltage and capacitance/conductance axes in response to the +BS suggesting the presence of negative mobile charges. In addition, the peaks in the conductance curves match in voltage the growing hump in the capacitance curves indicating the role of interface states. The first black curves in these graphs were measured without a BS, while the rest were measured after a 1 minute +BS. The abbreviation "MCx" in the legends means "Measurement Cycle" and the numbers 1, 2, ..., 13 indicate the cycle number.

ments were conducted on the capacitor structures by applying a 1 minute positive BS (+BS) and negative BS (-BS) of +4 V and -4 V, respectively, on the metal gate prior to each measurement cycle. As shown in Figs. 4.3 and 4.4, the results from the devices with n-type Si substrate demonstrate a sequential parallel shift of the measured curves to the left along the voltage scale in response to the +BS (Figs. 4.3a and 4.3b) and to the right in response to the -BS (Figs. 4.4a and 4.4b). This is an indication that the negative charges manifested in Fig. 4.2 are, in fact, mobile charges that move inside the MoS_2 bulk.

Results from BS measurements on p-type samples (Figs. 4.5a, 4.5b, 4.6a and 4.6b) exhibit the same phenomena observed in n-type samples except for an unexpected turn-around effect at the second -BS measurement cycle. As indicated by the yellow arrows in Figs. 4.6a and 4.6b, the turn-around effect occurs in such a way that the C-V and G-V curves show a big shift to the left at the first measurement cycle which indicates a positive charge inside the MoS_2 in contrary to the observations from the n-type samples. This may be caused by a sudden decrease in concentration of the negative charges close to the Si-side. However, the characteristics shift to the right at the second

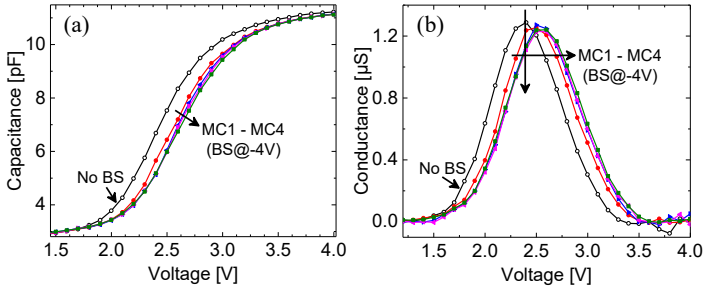

Figure 4.4: C-V and G-V measurements carried out following subsequent negative bias-stresses (-BS) of -4 V applied for 1 minute: (a) C-V and (b) G-V characteristics exhibiting parallel (right) and vertical (downward) shifts of the curves on the voltage and capacitance/conductance axes, respectively, in response to the -BS, as indicated by the black arrows. The decrease in the amplitudes of the conductance curves along with the decrease (absence) of the capacitance humps witnessed in Fig. 4.3a suggest the reduced impact of interface states. Also, the parallel shift confirms the negative mobile charges. These measurements were done on the very same devices and by using a similar procedure as that used to achieve the data in Fig. 4.3.

cycle and continue shifting in this direction for the remaining cycles. This suggests the presence of negative charges which is consistent with the observations from the n-type samples. A legitimate question here can be about the cause of the sudden decrease in the negative charge concentration of these samples at the first cycle. A possible explanation may be that holes accumulated in the p-Si under negative bias interact with the mobile negative charges that are being pushed against the Si-interface by the -BS as illustrated by the schematic diagram in Fig. 4.6c. Another possibility could be that interface states positioned in the upper half of the Si band gap capture electrons from the ions. This would leave the interface with a less negative charge and also modifies the charges distribution such that a similar interaction does not happen for the remaining cycles.

A ToF-SIMS chemical analysis was employed on the samples by following a standard experimental procedure described in section 3.2.6 to identify the origin of the mobile charges. The ToF-SIMS depth profile data revealed presence of negative ions Cl^- and OH^- apart from the expected chemical composition of the device structure (Fig. 4.6d). The Cl^- signal is observed to reach an almost zero count on the sputter

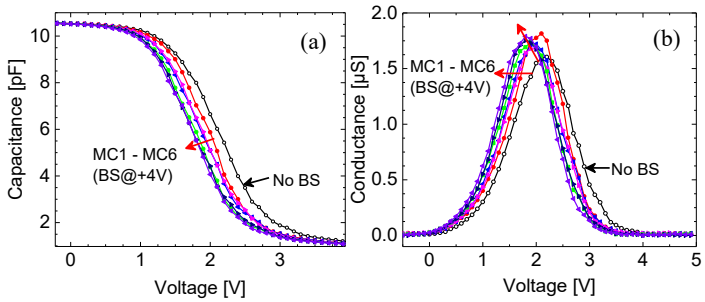

Figure 4.5: C-V and G-V measurements on MoS_2 capacitors with a p-type Si substrate following subsequent positive bias-stresses (+BS) of +4 V applied on the gate for 1 minute: (a) C-V characteristics exhibiting parallel (left) shift and (b) G-V characteristics exhibiting both parallel (left) and vertical (upward) shifts along the voltage and capacitance/conductance axes, respectively, in response to the +BS. The decreasing amplitudes of the conductance curves confirms the presence of interface states while the parallel shift supports the previous observation on the presence of mobile negative charges in the system. The measurement procedure is similar to the ones in Figs.4.3 and 4.4.

time axis much earlier than the other depth profile signals and this may indicate that Cl^- ions are due to sodium chloride (NaCl) surface contamination during sample handling. The OH^- on the other hand shows a signal that spans for a comparable time with respect to depth as that of the S and MoS_2 signals. Based on this outcome, the OH^- ions are considered the most probable candidates to act as the negative mobile charges. These ions themselves are likely to originate from catalytic splitting of water molecules that are adsorbed into MoS_2 during and/or after the device fabrication processes. This assumption is based on the well-known strong catalytic properties of Cr and in particular the edge-terminated MoS_2 films [100, 103, 233–235].

4.2.3. Interface States

Bias-stress (BS) measurements can also give insight about interface-states and the impact they have on device characteristics (see also chapter 3). In addition to the parallel shifts discussed in section 4.2.2, the C-V curves in Figs. 4.3 - 4.6 exhibit vertical capacitance shifts (like the C-V "hump" in Fig. 4.3a) and slope variations with respect to the polarity and number of BS cycles. Furthermore, the BS-dependent variations in the sharpness and intensity of the conductance peaks observed

from the G-V characteristics are clear manifestations of interface-states [236, 237]. What is more striking is that the voltage point at which the growing C-V "hump" occurs perfectly matches with that of the corresponding G-V peaks. Moreover, the decrease in slope of the C-V curves (i.e. the stretching effect along the voltage axis) is consistent with the increase in amplitude of the corresponding G-V peaks. This is a typical sign for the presence of interface-states. Owing to the formation of the SiO_x interfacial layer on the Si, the interface-states under discussion are considered to resemble P_b centers, which commonly occur at Si/SiO_x interfaces [230, 231]. These are well studied during the era of integration of high-k oxides in Si MOSFETs [236, 237]. In summary, based on the experimental observations discussed so far a +BS applied on the devices' metal gate boosts the influence of interface-states (intensifying C-V "humps") while a negative BS diminishes it (absence of the C-V "humps"). The implication of this observation will be discussed in the upcoming section.

4.3. Mobile Ion-Interface State Interaction Dynamics

The interaction between the BS-driven mobile ions inside MoS_2 and the electron states at the Si/MoS_2 interface is evident from the measured data shown in Figs. 4.3 - 4.6. The consistent message conveyed by those figures and the discussion in sections 4.2.2 and 4.2.3 is that the polarity of the applied BS influences the properties of the interface-states (i.e. they are enhanced by +BS and suppressed by –BS). The interaction dynamics and its role in device operation can be explained as the following. To start with, the default/ equilibrium position of the ions is considered closer to the Si-side than to the metal side of the MoS_2. This statement is based on the observations that (1) the influence of interface-states is suppressed (no C-V hump) at no BS and (2) that the parallel shift in the C-V characteristics for -BS (Figs. 4.4) is much smaller and saturates much quicker than that for +BS (Figs. 4.3). The structure of the MoS_2 film comprises 2D layers of predominantly vertical orientation. This is likely to facilitate the movement of the OH^- ions along the van der Waals gaps that are aligned with the direction of the applied electric-field. According to electrostatics, a –BS applied on the metal gate would push the ions further to the Si-interface where they will be in the proximity of the interface-states.

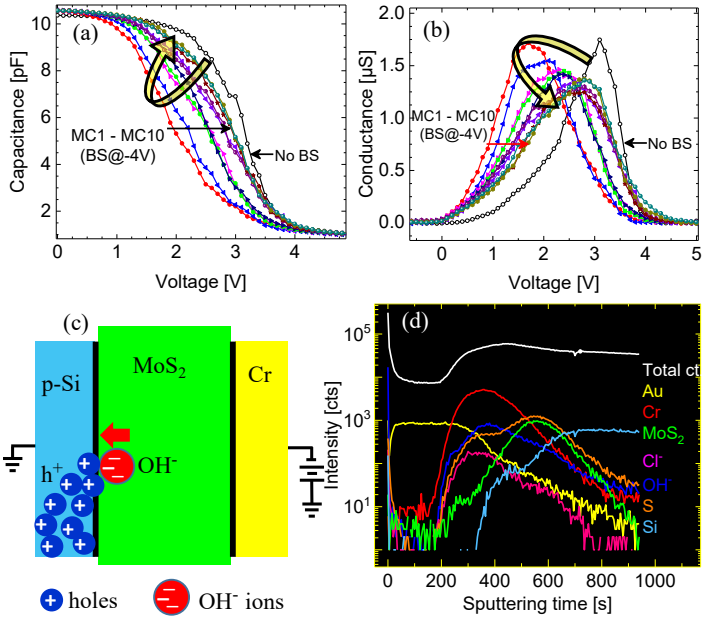

Figure 4.6: C-V and G-V measurements on the devices in Fig.4.5 following subsequent negative bias-stresses (-BS) of -4 V applied on the gate for 1 minute: (a) C-V and (b) G-V characteristics exhibiting both parallel (right) and vertical (downward) shifts along the voltage and capacitance/conductance axes, respectively, in response to the -BS. The decreasing amplitude in the conductance curves further confirms the impact of interface states while the parallel shift further attests presence of the mobile negative charges. The measurement procedure is similar to all the BS measurements in the above figures. The new phenomenon observed in the present graphs is the turn-around effect that occurs at the first BS cycle, which is explained in the main text. (c) Schematic diagram illustrating a possible interaction between the mobile OH^- ions and holes accumulated at the valence band edge near the Si/MoS_2 interface. (d) ToF-SIMS depth profile data revealing presence of OH^- and Cl^- ions in addition to the structural composition of the device structure.

As a consequence, the electron potential of the states experiences a Coulomb force arising from the ions nearby. This influences the energy positions of the states and leads to an electrostatic passivation effect that suppresses their ability to capture and emit electrons, analogous to interface state passivation by atomic hydrogen in SiO_2 [238]. As a result, the activity of the interface-states decreases with increasing –BS cycles as witnessed by the observed gradual increase in slope of the C-V curves, the negligible interface-state capacitance contribution (absence of the C-V hump) and the subsequent decrease in amplitude of the G-V curves. On the other hand, application of a +BS on the gate drags the ions away from the Si interface, freeing the interface-states from the electrostatic passivation effect they were under. As a result, the interface-state capacitance contribution increases in subsequent +BS cycles as indicated by the gradual decrease in slope of the C-V curves, the increase in amplitudes of the C-V hump and the corresponding conductance peaks (Fig. 4.3). The OH^- ion transport described here is similar to the electric-field induced movement of sodium ions (Na^+) in SiO_2 which was discovered during the early development of the MOS system [239].

4.4. Simulation

Analytical simulations were performed to further analyze the experimental data and to verify the interaction dynamics between the field-driven mobile ions and the interface-states described in section 4.3. The simulation involves calculation of theoretical C-V curves and comparing them with experimental data obtained at different +BS cycles while using an interface trap density (D_{it}) distribution resembling that of P_b centers as the fitting parameter. The D_{it} distributions shown in Fig. 4.7a were tuned such that the calculated C-V characteristics (solid curves) fit well with the experimental data (symbols). The result presented in Fig. 4.7b confirms that the observed C-V "humps" most likely originate from the D_{it} peaks and that the concentration and energy maximum of the active interface-states change as a function of BS. The simulation was based on the equivalent circuit model shown in Fig. 4.7c which is similar to the one used in [237]. This model considers all circuit elements involved in the physical “Si/MoS_2/metal” system such as the Si depletion layer capacitance, C_s, the SiO_x IL capacitance, C_{SiO_x}, the MoS_2 capacitance, C_{MoS_2}, the interface-state capacitance, C_{it} and the interface-state conductance, G_{it}. On the other hand, the

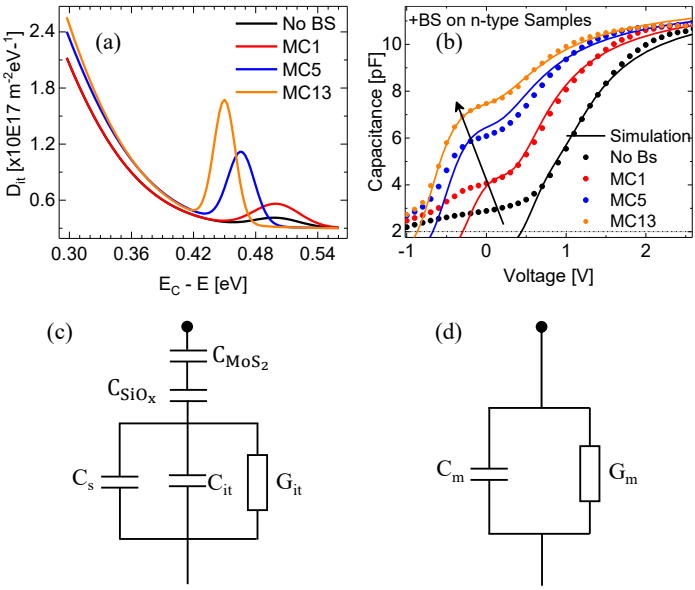

Figure 4.7: (a) Comparison of simulation (solid curves) and experiment data (dots) confirming the impact of the interface state-mobile ion dynamics. The experimental data are taken from the no BS and the 1st, 5th and 13th +BS cycles of the measurements in Fig.4.3. (b) Interface state distribution curves that were used as fitting parameters to fit the simulated C-V curves to the corresponding measured ones. (c) shows the equivalent circuit model the impedance analyzer assumes in measuring the experimental data and (d) shows the equivalent circuit model designed to include all the important elements to better model the actual devices. The grahs in (a) and (b) are adopted from ref. [27], ©2018ACS

impedance analyzer assumes a very simplified circuit model comprising only of a capacitor and a conductor connected in parallel as in Fig. 4.7d.

4.4.1. Background of the Simulation

The measured quantities C_m and G_m obtained from the impedance analyzer are practically influenced by the interface-state capacitance and conductance, C_{it} and G_{it}, respectively. These are produced when interface states capture and emit charge carriers when the applied AC probe signal oscillates the position of the Si Fermi-level ($\Delta\mu$) up and

down with respect to the energy position (ΔE) of the interface-states with energy distribution $D_{it}(\Delta E)$. The capture and emission rates may keep up with the pace of the angular frequency, ω, of the AC signal depending on the energy position of the states with respect to the Fermi-level. Here, it is important to note that the Fermi-function is not a precise step function at finite temperatures and thus the capacitance meter is not able to distinguish between C_{it} due to traps with energy lying at the exact position of the Fermi-level and that at the tails of the Fermi-function. This can be addressed by introducing a quantity known as capacitance density (ζ_{it}) presenting the capacitance per unit area and unit energy [152, 237] as

$$\zeta_{it} = f\left(1-f\right)\frac{q^2 D_{it}^2 e_n^2}{2k_B T\left(4e_n^2+\omega^2\right)}, \tag{4.3}$$

where, q is the electron charge, D_{it} is the energy distribution of interface-states, e_n is the emission rate of the trap, f is the Fermi-function, k_B is the Boltzmann constant, T is the absolute temperature and ω is the angular frequency of the probe AC signal. For a given Fermi-level position $\Delta\mu$, the C_{it} can be obtained by integrating ζ_{it} in Eq. 4.3 with respect to ΔE as in Eq. 4.4 [152, 237].

$$C_{it} = \int_0^{E_g} \zeta_{it}\, d\left(\Delta E\right), \tag{4.4}$$

where, E_g is the band gap of Si. By assuming that the interface states capture and emit electrons much faster than the AC probe signal frequency so that they are completely filled and emptied within a period time of the AC signal, the measured differential capacitance, C_m, can be calculated by using

$$C_m = \frac{C_{MoS_2} C_{SiO_x}\left(C_s + C_{it}\right)}{C_{MoS_2} C_{SiO_x} + \left(C_s + C_{it}\right)\left(C_{MoS_2} + C_{SiO_x}\right)}, \tag{4.5}$$

where, C_s is the Si depletion capacitance and C_{it} is the interface state capacitance as calculated from Eq. 4.4 [152, 237]. The simulated curves in Fig. 4.7 were calculated using Eq.4.5. A Mathematica script originally written by Prof. Olof Engström was adopted for these simulations by tuning parameters to achieve results that agree well with experiments.

4.5. Summary

MoS_2 is investigated as a barrier material to understand its dielectric properties and the accompanying interfaces. The study was conducted by fabricating capacitors based on MoS_2 with vertical layers grown by vapor phase sulfurization and characterizing them using admittance spectroscopy technique. The vertical orientation of the MoS_2 layers is confirmed by cross-sectional TEM investigations. The extracted static dielectric constant of MoS_2 is found in range of 2.6 - 2.9. Capacitance- and conductance-voltage measurements under electric field stress in combination with ToF-SIMS depth profile analysis indicate presence of mobile OH^- ions inside MoS_2 that possibly originating from catalytic splitting of water molecules by the edge-terminated MoS_2 layers. The vertical orientation of the layers facilitates the movement of the ions, presumably, along the van der Waals gaps. Experiments, supported by analytical simulations, show presence of interface states and their interaction dynamics with the mobile ions.

5

MoS_2 Emitter Diodes for Graphene Base Hot Electron Transistors

Efficient emitter diodes are required to realize high performance graphene base hot electron transistors (GBTs) as described in chapter 2. GBTs rely on the vertical transport of high energy electrons (hot electrons) across the injection barrier isolating the emitter from the base (EBI). Therefore, their performance is greatly influenced by the properties of this barrier. As a matter of fact, picking injection barrier materials that form small conduction band offsets (CBOs) with respect to the emitter will provide high level collector currents in the on-state (I_{ON}) [180, 196, 199, 240]. Hence, vertical heterostructures comprising low CBOs similar to the compound semiconductor structures studied by Heiblum and coauthors [241, 242] are predicted to offer high frequency performance up to the THz domain [180, 196, 199]. On the basis of its semiconducting behavior with a band-gap (1.3 eV [88]) and electron affinity (4 eV [243, 244]) values close to that of Si (1.1 eV and 4.05 eV, respectively), MoS_2 became a promising candidate to make an efficient injection barrier for GBTs with an anticipated small CBO with respect to the Si-emitter. This anticipation was confirmed by experimental

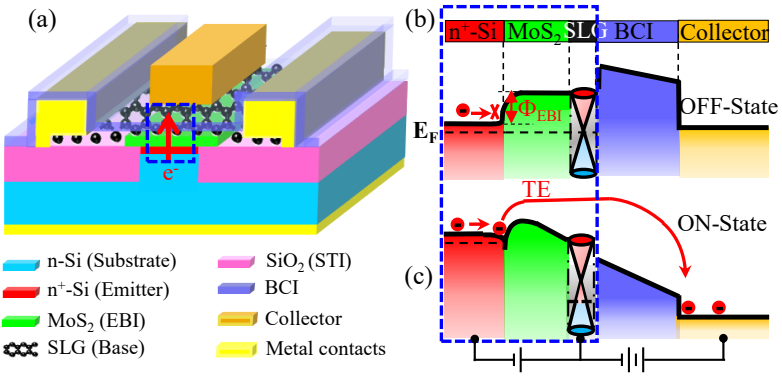

Figure 5.1: : (a) A schematic diagram showing the structure of a GBT in which MoS_2 is used as an emission barrier with the red vertical arrow showing the electron transport direction. Conduction band diagram of the GBT in its active region during (b) OFF-state at a finite collector voltage and (c) ON-state where a higher positive base voltage lowers both the EBI and BCI barriers to allow a thermionic emission of hot electrons from the emitter into the collector as illustrated by the red arrow.

investigations [26, 27] carried out in this thesis as discussed in chapter 4. This small barrier is expected to promote thermionic emission of hot electrons from the emitter into the base. Schematics of the structure and operation principle of a GBT with an envisaged MoS_2 emission barrier is given in Fig.5.1. The prospect of MoS_2 as an efficient emission barrier in GBTs has been explained through experimental investigation of the electron transport across the n^+-Si/MoS_2 heterojunction in n^+-Si/MoS_2/graphene diodes. The findings of the study have been published [24] and are also presented in this chapter.

5.1. The n^+-Si/MoS_2 Energy Barrier for Electrons

The height of the n^+-Si/MoS_2 heterojunction barrier regulates the injection of electrons from the n^+-Si emitter into the graphene base and determines the output current at the collector. The charge state of the MoS_2 film influences the height of the barrier [24] as demonstrated in Fig.5.2. When it is neutral, the electron barrier at the interface, Φ_{B1}, is expected to be very small, less than 100 meV at thermal equilibrium

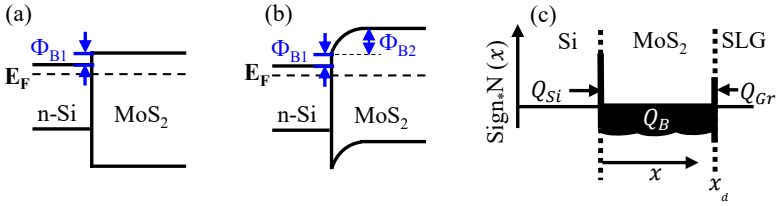

Figure 5.2: Schematic band diagram illustrating the energy barrier that electrons face at the n^+-Si/MoS_2 heterojunction in the case of (a) neutral MoS_2 and (b) MoS_2 containing negative charges in its bulk. (c) Schematic diagram showing partitioning of charges in the "n^+-Si/MoS_2/graphene" system.

(Fig.5.2). The VPS-grown MoS_2 film in the present case, however, has been verified to contain negative bulk charges [26, 27] and the charge alters the shape of the MoS_2 CB such that the barrier maximum moves from the interface to a point on the CB edge (Fig.5.2b). As a consequence, electrons at the Si CB edge would see an extra energy barrier, Φ_{B2}, in addition to Φ_{B1} (Fig.5.2b). The partitioning of the charge among the three components of the Si/MoS_2/graphene (Gr) system can be understood as depicted in Fig.5.2c. The net charge in the system needs to be zero according to the rule of charge conservation. For this to be achieved, the charges at the Si/MoS_2 and MoS_2/Gr interfaces, i.e. Q_{Si} and Q_{Gr}, respectively, should compensate the bulk charge inside MoS_2, Q_B. Therefore, assuming Q_{Si} as a fraction a of Q_B such that $Q_{Si} = aQ_B(x)$, the charge at the graphene interface becomes $Q_{Gr} = (1-a)Q_B(x)$, where x is the distance from the Si/MoS_2 interface into the MoS_2 bulk.

5.2. The Impact of Bulk Charge on the MoS_2 Bands

The negative bulk charge in MoS_2 has a significant impact on the shape of its bands by modifying the electric-field in the structure. This, in turn, influences the electron barrier height at n^+-Si/MoS_2 heterojunction regulating the electron injection. This effect can be modeled by using the Poisson equation such that the total bulk charge, $Q_B(x)$, of an arbitrary depth distribution, $N(x)$, is determined by

$$Q_B(x) = -q\int_0^{x_d} N(x)dx, \tag{5.1}$$

where the minus sign denotes negative charge and x_d is the distance between the Si/MoS_2 and the MoS_2/Gr interfaces as indicated in Fig.5.2c. The electric-field, $F(x)$, at the Si/MoS_2 interface is then calculated by considering a Gaussian depth distribution of the negative bulk charge as shown in Fig.5.3a by using

$$F(x) = \frac{1}{\epsilon\epsilon_0}(Q_B(x) + Q_{Si}) + \frac{(\Phi_{Gr} - \Phi_{Si})}{x_d}, \tag{5.2}$$

where ϵ is the electronic dielectric constant of MoS_2, ϵ_0 is the permittivity of vacuum, Φ_{Gr} is the work function of graphene and Φ_{Si} is the work function of Si. The relation between the electric-field and the applied bias, V, in this system containing a non-homogeneous distribution of charge within the dielectric is more complex than the simple relation $F(x) = \frac{V}{d}$. Fig.5.3b shows the non-homogeneous electric-field in the present system calculated by using Eq. 5.2. The shape of the MoS_2 CB, $E_C(x)$ [eV] is then calculated by integrating the resulting electric-field, $F(x)$, along the MoS_2 thickness as

$$E_C(x) = \int_0^{x_d} F(x)dx. \tag{5.3}$$

The CB curves calculated at different voltages by using Eq. 5.3 are presented as black curves in Fig.5.3c and the magnified versions are presented in Fig.5.3d for clarity. The figures illustrate that the bending of the bands increases with increasing bias while the barrier maximum shifts gradually toward the Si/MoS_2 interface. This leads to a lowering of the charge-induced barrier, Φ_{B2}. As shown in Fig.5.4a, the energy values extracted from the maximum points of the black CB curves in Fig.5.3d match very well with a barrier function used to calculate the I-V characteristics fitted to the measured room temperature I-V. This will be discussed later in this chapter in more detail. This agreement leads to the consideration that the charge-induced barrier, Φ_{B2}, dominates the interface barrier, Φ_{B1} and is responsible for regulating the current conduction across the structure. The model is then used to approximate the concentration of the negative charge by the area under the Gaussian curve in Fig.5.3a, which gives a value of ~2.8x10^{16} m^{-2}. It is worth noting that electrons may experience an attraction force from image charges building up behind them in the Si as they approach the Si/MoS_2 interface. Hence, the image force may give rise to a lowering effect on the heterojunction barrier that intensifies with increasing

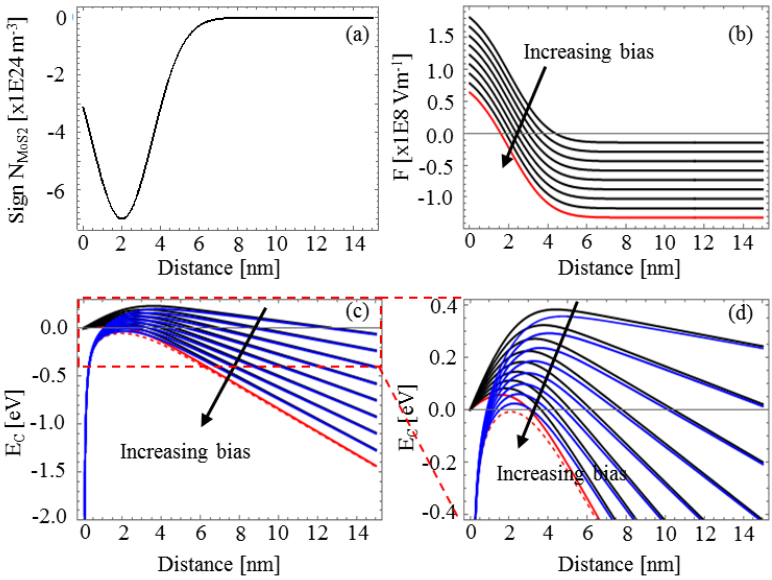

Figure 5.3: (a) a Gaussian distribution assumed for the negative bulk charge inside MoS_2 with the y-axis indicating the charge concentration while the x-axis indicates the distance between the Si/MoS_2 and MoS_2/Gr interfaces. (b) The electric-field calculated for various voltages indicating a relation deviating from $\frac{V}{t_{ox}}$, where t_{ox} represents the oxide thickness, in this case MoS_2. (c) The calculated MoS_2 conduction band, $E_C(x)$ as a function distance from the Si/MoS_2 interface with (blue) and without (black) taking into account the effect of image force lowering (IFL) and (d) the magnified version of the graph for the sake of a better visibility. The red curves in the figures indicate calculations at the highest voltage

bias. To account for this effect, a Schottky lowering factor is introduced such that Eq. 5.3 changes to

$$E_C(x) = \left[\int_0^{x_d} F(x)dx\right] - \frac{q}{16\pi\epsilon\epsilon_0 x}. \tag{5.4}$$

The CB curves calculated using Eq. 5.4 taking the effect of image force lowering (IFL) into account are presented as blue curves in Figs. 5.3c and 5.3d. The term IFL refers to a barrier lowering effect similar to Schottky lowering. In the present case, an electron approaching the n^+-Si/MoS_2 interface encounters an attraction force (image force) due to image charges building up in the n^+-Si. The barrier lowering this image

force causes is called IFL. The CB curves calculated by taking IFL into account provide lower barrier heights compared to those calculated without considering IFL. The energy values at the maximum points of the CB curves calculated with and without IFL were extracted and plotted in Fig.5.4a along with the barrier function obtained by fitting the measured I-V. Fig.5.4a) shows that, unlike the data obtained without considering IFL (black symbols), those obtained by considering IFL (blue symbols) did not show agreement with the barrier function obtained from the I-V fitting. This suggests that IFL is not applicable to the present case, possibly because the IFL effect is more severe at the Schottky junction whereas the dominating barrier in the present case (i.e. Φ_{B2}) is away from it and thus not affected by it. The $E_C(x)$ calculations were carried out by using an electronic dielectric constant value of $\epsilon_i = 3$. This is considering the fact that the interface barrier in the present structure is small and that it allows injection of high concentration of low energy electrons into the CB edge of MoS_2 at higher voltages. In effect, the electrons would attain lower velocity in the MoS_2 crystal and this potentially leads to an electronic dielectric constant approaching the static value achieved from the experiments described in chapter 4.

5.3. Electron Transport across the n^+-Si/MoS_2 Heterojunction

Despite the fact that MoS_2 is one of the highly explored 2D TMDC materials, detailed experimental investigations on the out-of-plane charge carrier transport is not widely available as research focuses rather on the in-plane transport. Zhu and coauthors have investigated out-of-plane carrier transport across exfoliated-MoS_2 sandwiched between two metal electrodes and claimed dominating Fowler-Nordheim and thermal-assisted transports at high and low electric-fields, respectively [245]. However, technological relevance of exfoliated materials is very limited due to lack of scalability. This motivates the present study of vertical electron transport across the n^+-Si/MoS_2 junction. As part of the systematic charge-carrier transport investigation, J-V characteristics were acquired from n^+-Si/MoS_2/Gr diodes at various temperatures ranging from 200 K to 300 K at an interval of 20 K. As shown in Fig.5.4b, the measured results exhibit significant temperature dependence for both bias polarities. This suggests thermally-stimulated charge carrier

transport across the structure. The data also exhibit a diode behavior with asymmetric current originating from the asymmetric electron barriers present at the Si/MoS_2 and MoS_2/Gr junctions in forward- and reverse-biased conditions, respectively. Since GBTs operate only in the

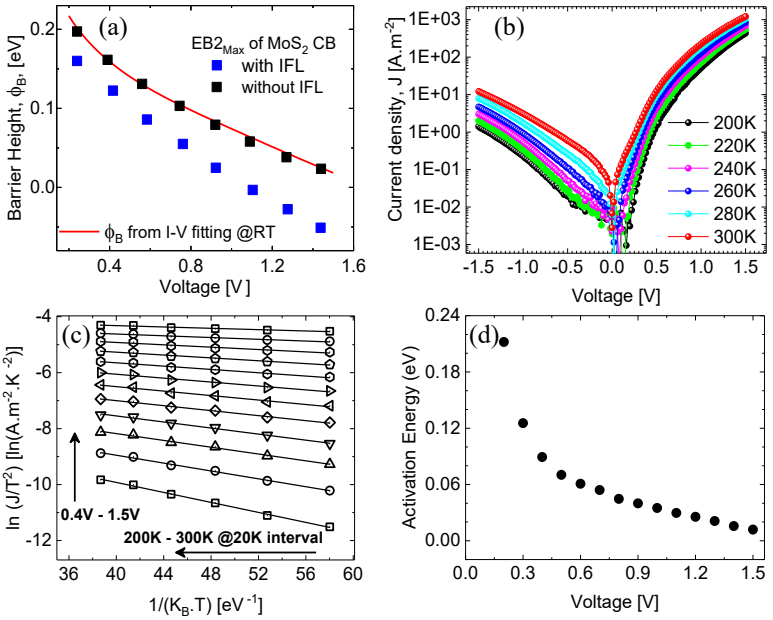

Figure 5.4: (a) Comparison of barrier data obtained from $E_C(x)$ calculations with and without consideration of the effect of image force lowering (IFL) with that obtained from I-V fitting. (b) Temperature-dependent I-V characteristics measured by varying the sample temperature from 200 K to 300 K at an interval of 20 K. The data shows a clear modulation of current with temperature, suggesting a temperature-dependent charge-carrier transport. (c) Richardson plots created by replotting the measured I-V characteristics in (a) in the form of $ln\left(\frac{J}{T^2}\right)$ as a function of $\frac{1}{k_B T}$ and the perfect linearities of the activation plots further suggests a dominating thermionic emission (TE) transport. (d) a barrier height data obtained by plotting the activation energy, E_a, extracted from the slopes of the Richardson plots versus the applied voltage.

forward-biased regime such that hot electrons are injected from the n^+-Si emitter into the graphene base [47], the electron transport investigation here focuses only on this regime. Possibility of the MoS_2/Gr junction to influence the electron transport in the forward-biased con-

dition is assessed through analytical simulations (Fig.8.1) and the outcome confirmed that indeed no electron barrier exists at that junction in this biasing condition. This leaves the electron barrier at the n^+-Si/MoS_2 junction exclusively responsible for the forward current transport [24]. To identify the dominating current transport mechanism, the measured forward biased current was analyzed using the classic transport models that govern semiconductor physics. These models were generally discussed in chapter 2 in section 2.2. The experimental data was examined for correlations with the models for DT, FNT, TAT, FPE and TE. Also, the strong temperature dependence observed in the measured data rules out the possibility of dominating DT or FNT. A second argument for ruling out DT is that the ~15 nm MoS_2 layer in the present devices is too thick to allow DT of charge carriers [160]. Nevertheless, these arguments were verified through analysis of the experimental data by using the SCL, DT and FNT models and no significant correlations were found as expected. A similar procedure employed for TAT and FPE models also ended up with results that showed no dominating TAT or FPE signatures. This leaves TE as the most probable mechanism to dominate the current conduction across the present devices. A strong indication for a possible TE current conduction are plots of $ln\left(\frac{J}{T^2}\right)$ versus $\frac{1}{k_B T}$ which provide linear Richardson plots with negative slopes that match well the TE model given in Eq. 2.12 (Fig.5.4c). Activation energies extracted from the slopes of the Richardson plots (in Fig.5.4c) were plotted as a function the applied bias. The result shows a decreasing barrier height with increasing bias (Fig.5.4d) clearly indicating a bias-dependent barrier lowering effect which is expected for TE. The barrier height before lowering is extracted from Fig.5.4d by extrapolating the linear part of the curve onto the y-axis is ~0.09 eV, which is a reasonable value for the present structure given the expected small CBO between MoS_2 and Si. An illustration of TE-dominated transport of electrons across the forward-biased "n^+-Si/MoS_2/Gr" structures, which are analogous to the emitter diode of a GBTs, is shown the red arrow and the marking with blue dashed box in Fig.5.1c.

5.4. Modelling TE Current across the n$^+$-Si/MoS$_2$ Barrier

TE in metal/Si Schottky structures is modeled by assuming isotropic electronic properties and parabolic energy bands for the metal and ellipsoidal constant energy surfaces for the Si [151, 168, 169, 246]. This is required to maintain a Maxwellian velocity distribution of charge carriers on either sides of the Schottky barrier. In the present device structure, thermally excited electrons from the heavily doped Si overcome the heterojunction barrier, Φ_B, to enter the layered polycrystalline MoS_2 which is a ~15 nm indirect gap semiconductor with more than one possible CB minimum. It is assumed that a Maxwellian distribution of electrons is present in the Si and that only those with a velocity component in the x-direction (i.e. perpendicular to the barrier plane) and an energy larger than Φ_B can enter the MoS_2 CB. The conventional TE model is based on the Boltzmann statistics which is not valid for $\Phi_B <$ ~3kT as is the case for the present structures at high biases. For this reason, the Fermi statistics is used in the present case to ensure a more reliable calculation of current across small energy barriers. Accordingly, the TE current density, J_{TE} is modeled by assuming the relation

$$J_{TE} \propto \int_{\Phi_B}^{\infty} f(E)g(E)dE, \tag{5.5}$$

where $f(E)$ is the Fermi-function, $g(E)$ is the density of states and E is energy of the Si CB. The product $f(E)g(E)$ gives the energy distribution of the electrons moving toward the barrier and it is proportional to $(E-E_F)^{\frac{1}{2}}$ for a Maxwellian electron gas. This leads to the expression

$$J_{TE} = BT\int_{\Phi_B}^{\infty}\left[\frac{E^{\frac{1}{2}}}{1+exp\left(\frac{E-E_F}{kT}\right)}\right]dE, \tag{5.6}$$

where B is a constant, T is temperature, E_F is the Fermi-level in Si and k is the Boltzmann constant. The solution of the integral in Eq. 5.6 will provide an additional pre-factor, T, and this makes the relation between J_{TE} and T quadratic (i.e. $J_{TE} \propto T^2$). Eq. 5.6 is based on the assumption that both the Si and MoS_2 parts have similar density of states as a function of energy so that the electron transmission probability becomes independent of electron energy. This means that a thermally excited electron in the Si will be transferred into MoS_2 and occupy a

state of the same energy as that in the Si. Also, the probability for transfer is assumed independent of energy. Fig.5.5a demonstrates the energy distribution of the electrons in the Si based on the Boltzmann- and Fermi-Dirac statistics. The corresponding distribution in the MoS_2

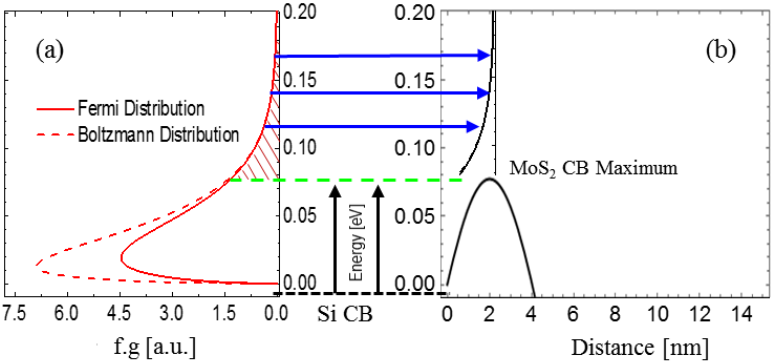

Figure 5.5: (a) $f.g$ vs E curves illustrating the distribution of electrons at the Si CB edge based on the Boltzmann and Fermi-Dirac statistics (dashed and solid curves, respectively). The hatched region indicates the concentration of electrons that can be injected into MoS_2. (b) Illustration of the MoS_2 CB bending with the schematic on the barrier maximum showing the Fermi-tail of the distribution of electron states in MoS_2 which is similar to that of Si for similar energy values. The blue arrows extending from "a" to "b" indicate the electron transport direction and the horizontal green dashed line shows energy of the barrier maximum indicating that electrons injected into the MoS_2 CB are only those having energies above this value. The grahs are reproduced from ref. [24], ©2020ACS.

together with a schematic of the MoS_2 CB is shown in Fig.5.5b. The hatched area under the distribution curves in Fig.5.5a, whose lower boundary is determined by the energy of the MoS_2 CB maximum, indicates the concentration of thermally-excited electrons that can be injected into MoS_2. Furthermore, the arrows in the figure illustrate the direction of electron exchange between states of the two materials having the same energy.

The thermionic current was calculated for three different temperatures (i.e. 200 K, 260 K and 300 K) using Eq. 5.6 which is based on a reasoning similar to the one used Kim et al. [247]. The calculations were based on the consideration that the electron transport from Si to the maximum point of the MoS_2 CB, which is assumed ballistic, is propor-

tional to the concentration of electrons possessing energies above the barrier maximum (hatched region in Fig.5.5a). Then, bias-dependent

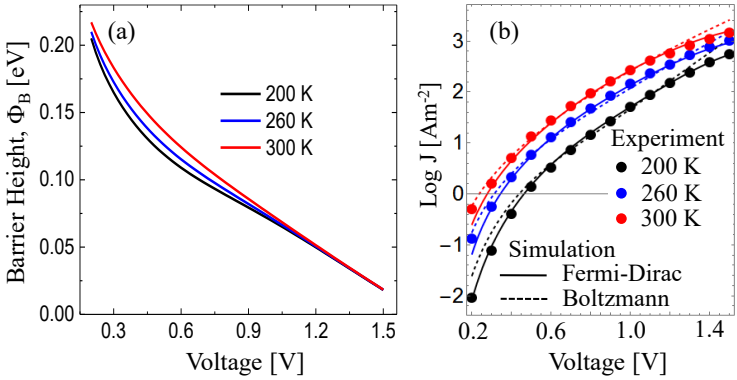

Figure 5.6: (a) Bias-dependent barrier functions used to calculate I-V characteristics that were fitted to the experimental data measured at three temperatures, i.e. 200 K (black), 260 K (blue) and 300 K (red). (b) Fitting of simulated I-V (dashed and solid lines) to the experimental ones (symbols) measured at temperatures of 200 K, 260 K and 300 K. The solid curves show current calculated using the Fermi-distribution while the dashed curves show that calculated using the Boltzmann distribution. The grahs are adopted from ref. [24], ©2020ACS

barrier functions given in Fig.5.6a were used as fitting parameters that were tuned until the calculated I-V characteristics (dashed and solid curves) fitted with the corresponding measured data (symbols) as shown in Fig.5.6b. It is evident from this figure that the calculated current based on the Fermi-distribution (solid curves) agreed with the experimental data better than the ones based on the Boltzmann distribution (dashed curves). The calculated data based on Boltzmann statistics show a clear divergence from the experiment in the higher bias range, which can be explained as follows. The Fermi-distribution in Eq. 5.6 can be approximated by the Boltzmann-distribution for barrier heights larger than ~3kT to achieve the standard Richardson's expression [169, 248]

$$J_{TE} = A^* T^2 exp\left(\frac{-\Phi_B}{kT}\right), \tag{5.7}$$

where the pre-exponential coefficient, A^*, is the effective Richardson constant. However, at higher voltages where the barrier heights fall

below the 3kT limit, the Boltzmann approximation lacks precision as it assumes a larger electron concentration than is practically available (Figs. 5.5a) and thus overestimates the current. Another observation evident from Fig.5.5 is that fitting of the calculated I-V characteristics to that of the measured data at three different temperatures required three distinct barrier functions (Fig.5.5). The implication of this observation will be discussed in the next section.

5.5. Effect of Temperature on the Heterojunction Barrier

The heterojunction barrier height values extracted from activation energies through the Richardson analysis (Fig.5.4d) are compared with the barrier functions obtained from the I-V fitting done in section 5.4 (Fig.5.6). As shown in Fig.5.7, the former are significantly smaller than the latter (Fig.5.6a). The results from Fig.5.6a also suggest that the heterojunction barrier height, Φ_B, changes with both bias and temperature. For convenience, comparison of the barrier data obtained from the two approaches is shown in Fig.5.7a. In an attempt to understand the relationship between the barrier height and sample temperature, T, Φ_B versus T plots are presented in Fig.5.7b for different voltage values. It turns out that Φ_B has a nearly linear relation with temperature such that the barrier height values obtained from activation energies correspond to Φ_B values at $T = 0K$. The bias and temperature dependence of Φ_B is modeled using a first order approximation as

$$\Phi_B(V,T) = \Phi_{B0}(V) + \beta(V,T)\,T, \tag{5.8}$$

where $\beta(V,T)$ is a proportionality factor and $\Phi_{B0}(V)$ is the barrier height at $T = 0K$ for a temperature-independent β. Hence, a graph of $\Phi_B(V,T)$ vs T will provides linear plots with the slope given by $\beta(V)$ and y-intercept given by $\Phi_{B0}(V)$ like in Fig.5.7b. In a thermodynamical context, the proportionality factor, β, is related to a negative entropy change occurring when the electron ensemble coming from the Si enters MoS_2. The observed temperature dependence of Φ_B could also be due to strain at the interface [249] and different temperature dependences of the bandgaps of the two materials. Strain has impact on the band structure in MoS_2 [249], making temperature dependence a possibility. Incorporation of Eq. 5.8 into Eq. 5.7 leads to a modified Richardson's expression given by

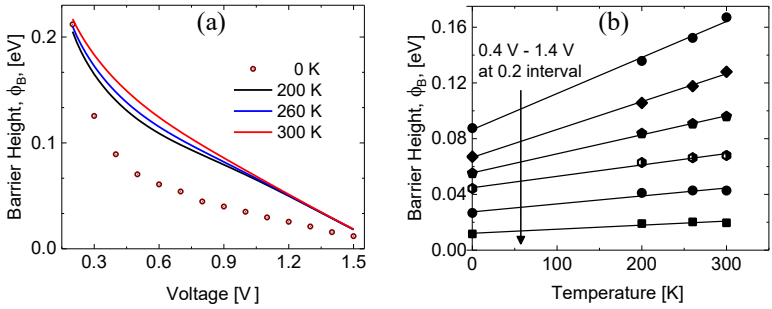

Figure 5.7: (a) Comparison of barrier height data obtained from Richardson's analysis and that obtained by fitting simulated I-V to the measured ones at three temperatures (i.e. 200 K, 260 K and 300 K). (b) a graph showing nearly linear Φ_B vs T plots with slopes and intercepts determined by $\beta(V)$ and Φ_{B0}, respectively. The plots in Fig.5.7a are adopted from ref. [24], ©2020ACS.

$$J_{TE} = A^* T^2 exp\left[-\left(\frac{\beta(V)}{k} + \Phi_{B0}(V)\frac{1}{kT}\right)\right], \tag{5.9}$$

such that Richardson's plots of $ln(\frac{J_{TE}}{T^2})$ vs $\frac{1}{kT}$ provide slopes determined by $\Phi_{B0}(V)$, which corresponds to the barrier height at $T = 0K$.

5.6. Summary

This chapter assessed the investigation of cross-plane charge carrier transport across n^+-Si/MoS_2/Graphene vertical heterostructures for potential application as emitter diodes for graphene base hot electron transistors (GBTs). Electrical characterizations show that the vertical current modulates with temperature. Richardson analysis on the data along with analytical simulations suggest that the current conduction is dominated by thermionic emission, a preferred conduction mechanism for enabling high GBT performance. Analytical simulation results have also demonstrated that the presence of negative charges discovered in chapter 4 induces an energy barrier at the MoS_2 conduction band and that it dominates the interface barrier and thus limits the overall current conduction across the structures. It was also found that the barrier height has a linear dependence on temperature.

6

MoS_2-Based Hybrid Memrsistors

Fast and energy-efficient computing is what the future demands to accommodate the exponential information growth that is imposing a tremendous challenge to the traditional computers we are using today [250]. Neuromorphic computing systems made of brain-inspired artificial neural networks (ANNs) with memristor synapses offer a potential solution to overcome these challenges [250–252]. A wide variety of memristors exist today and some examples from a classification based on the underlying memristive mechanism include electrochemical metallization memory (ECM), valence change memory (VCM), phase change memory (PCM), thermochemical memory (TCM), etc. [250,251]. The most commonly used memristors are often based on transition metal oxides (TMOs). The mechanism driving the resistive switching (RS) behavior of most TMO-based memristors is filamentary (see section 2.3.4) [211, 251]. The high current requirement for the filament formation-retraction process currently limits the use of these devices for mass storage in nonvolatile memories (NVM) and for neuromorphic systems where millions and billions of them need to be integrated. As a potential alternative, the research community is recently showing interest in memristors based on layered 2D materials [120–124,188,227, 253–258], hexagonal boron nitride (h-BN) and others. Their atomic-

scale thickness may enable switching at low external electric-field and the possibility for bio-realistic electronic-ionic interactions may further allow realizing energy-efficient ANNs [256]. MoS_2 is the most explored TMDC material in this regard, but most of the devices reported so far are based on: (1) lateral device configuration and (2) small flakes of mechanically exfoliated or CVD-grown MoS_2. While the former does not give a small foot-print required to achieve high device integration density in practical applications [253], the latter limits scalability which is vital for mass production. Furthermore, there is no clear and universal understanding on the mechanism and origin of the phenomena governing RS in MoS_2. Some of the proposed RS mechanisms for single- and multi-layer MoS_2 include electric-field induced movement of grain boundaries and sulfur vacancies, migration of oxygen ions, lattice distortion, reversible phase modulation and diffusion of metal-ions into the material [120–124, 257]. In this dissertation, systematic experimental investigations supported by analytical simulations were employed to demonstrate the presence and origin of a RS effect in large-area VPS/TAC-grown layered MoS_2 with vertically aligned 2D layers that was used as the active RS medium in vertical "Si/MoS_2/Metal" hybrid memristors [28]. The MoS_2 layer in these devices is grown directly on the Si crystal, which provides transfer-induced polymer residue-free and chemical contamination-free interfaces. Moreover, it sets a route towards integration of novel 2D materials-based memristors into the existing Si technology to enable functionality diversification of ICs.

6.1. Demonstration of Resistive Switching Behavior in Layered MoS_2

6.1.1. DC I-V Sweep Measurements

I-V sweeps exhibiting a hysteretic behavior are commonly used as a quick means of checking a RS phenomenon in memristors. They also serve to determine important parameters such as set and reset voltages that can then be used in more advanced switching tests. Such measurements were carried out on the devices described in the previous section in ambient conditions at room temperature. The tests were conducted in four subsequent sweeping steps using a configuration as schematically shown in Fig. 6.1a. The first step (sweep1) was performed by sweeping the voltage at the top electrode (V_{TE}) from 0 V to -5 V, is followed by a second sweep (sweep2) that spanned from -5 V to 0 V.

Then a third and fourth sequences were done by subsequently sweep-

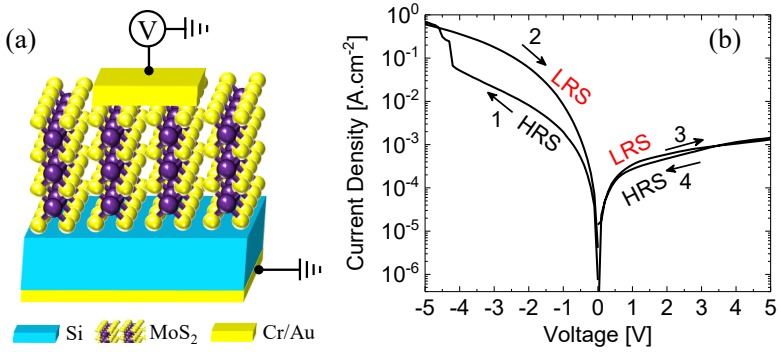

Figure 6.1: Experimental demonstration of a RS behavior in the Si/MoS_2/Metal memristors: (a) schematic of the devices including the wiring setup used during the measurement. (b) a representative DC I-V sweep exhibiting a bipolar RS behavior in the present device structure.

ing V_{TE} from 0 V to +5 V and from +5 V back to 0 V, respectively. The data obtained from these measurements is shown in Fig. 6.1b where bipolar RS behavior is observed with the resistance state alternating between a high resistance state (HRS) and a low resistance state (LRS). The HRS-to-LRS transition, which is commonly referred to as the SET process, occurred during sweep1 at around $V_{TE} = -4V$. The LRS is maintained during sweep2 and sweep3. The LRS-to-HRS transition, which is typically known as the RESET process, took place in sweep4 although the transition is not as sharp as the SET and the switching ratio is also much smaller. A similar asymmetric switching behavior with a larger switching ratio in the SET than the RESET regime has also been reported by Zhu and coauthors for Au/Li_xMoS_2/Au lateral memristors [123]. The effect was attributed to field-driven migration of lithium ions (Li^+) [123]. Apart from the hysteretic behavior, Fig. 6.1b also exhibits asymmetric I-V characteristics indicating that the charge carrier transport is interface dominated, i.e. the asymmetric current originates from the asymmetric hole energy barriers at the Cr/MoS_2 and Si/MoS_2 interfaces under forward- and reverse-biased conditions, respectively. From this, it can be inferred that the observed current conduction in the present devices maybe dominated by conduction of holes across the hole barrier at the Si/MoS_2 interface. This was verified

through a detailed investigation on the charge-carrier transport across the Si/MoS_2 heterojunction as discussed in chapter 5.

6.1.2. Effect of Bias and Sweep-Rate on the RS Behavior

DC I-V measurements were carried out in ambient condition by varying the bias range to assess how the overall switching behavior progresses with applied bias. This helps to identify the appropriate window of operation for the devices. As shown in Fig. 6.2a, a noticeable switching effect occurs only for $V_{TE} \geq \pm 4V$ and that the switching ratio shows a general increasing trend with increasing bias range. Based on these results, further measurements were limited to a voltage range of $\leq 5V$ to avert a potential damage to the devices during subsequent electric-stress. The influence of sweep rate on the RS behavior was tested. The result (Fig. 6.2b.) shows that a slower sweep rate leads to an increasing switching ratio and a decreasing SET voltage (V_{SET}). This was attributed to enhanced ionic diffusions as the slower sweep rate gives more time for ions to diffuse better [253].

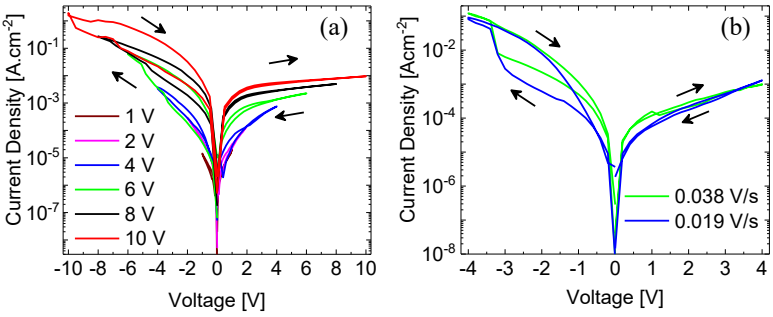

Figure 6.2: (a) I-V sweep measurements performed on the present devices in ambient conditions while varying the sweep range. The result exhibits observable switching for the bias range $V_{TE} \geq \pm 4V$ and scales with the bias range. (b) Ambient condition I-V characteristics of the devices showing that a slower sweep rate leads to an increasing switching ratio and a decreasing V_{SET}, which can be an indication for a possible involvement of ionic movements in the switching process.

6.2. Evaluation of the Switching Performance

The switching was further assessed for durability and non-volatility through endurance and state-retention measurements. The details of these tests will be covered in the following subsections.

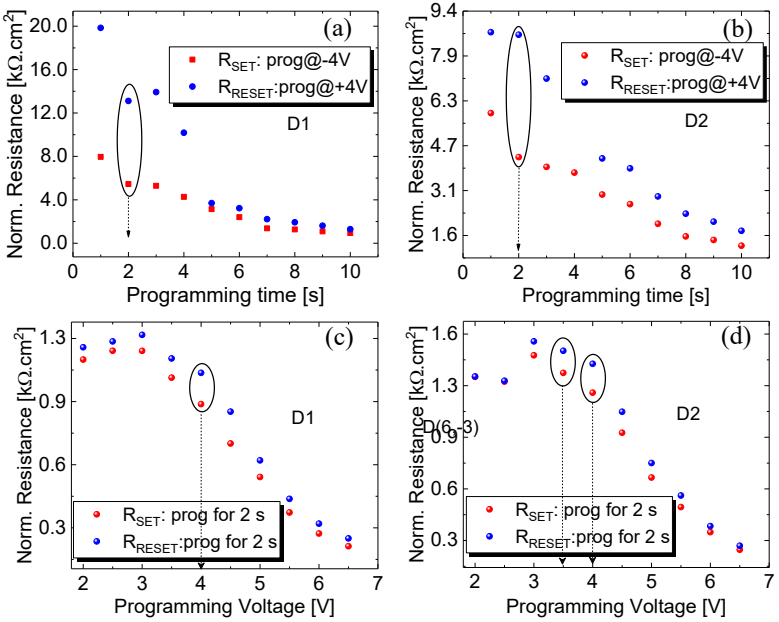

Figure 6.3: (a), (b) Measurements performed to determine the optimal value of the programming time for two devices, D1 and D2. (c), (d) Measurements performed to determine the optimal values of the programming voltages for two devices, D1 and D2.

6.2.1. Determining the Optimal Measurement Window

First, an optimal measurement window is needed to be established prior to conducting endurance and state-retention measurements. This includes determining the optimal values for the reading voltage, the programming voltages and the corresponding programming times for the SET and RESET processes. This is a crucial step that needs to be done empirically. The optimal measurement window of the present devices was identified using the following procedure. First, the starting

values for the SET and RESET voltages were taken from the initial I-V sweep measurements to measure the resistance values at LRS and HRS while varying the programming time, i.e. the length of time the programming bias is kept on. Such measurements were done on few devices and, in the end, the minimum programming time that still leads to a reasonably large switching ratio was selected as the optimal value. Representative results from two devices named D1 and D2 are given in Figs. 6.3a and 6.3b where 2 s was found as the optimum value. This was then used to measure the resistance values at LRS and HRS while varying the programming voltages (Figs. 6.3c and 6.3d). Finally, the optimum programming voltages of -3.5 V and +4 V were achieved for the SET and RESET processes, respectively.

6.2.2. Endurance Tests

Endurance is one of two important figure of merits (FOM) that are widely used to evaluate the switching performance and application readiness of memristors. It serves as a means of evaluating how many cycles a memristor device is capable to switch between LRS and HRS without losing its switching window [184, 227]. Using the optimal programming voltage and time values determined in section 6.2.1, the endurance of the present devices was tested in ambient conditions. This was carried out by following the measurement procedure described in subsection 3.5.2. The endurance data were acquired from several devices on the same chip and a representative example is shown in Fig. 6.4a. A clear RS behavior for at least 140 manual DC switching cycles is demonstrated albeit with a resistance shift for the first few cycles, which may be due to ionic diffusion phenomena. Although the endurance data obtained from all the measured devices share a general similarity, the absolute resistance values show slight differences. Such spatial (cell-to-cell) variability is currently a general issue for memristors and challenges their applicability in computing and memory devices [184]. Cell-to-cell variability of RS in 2D TMDC materials can be partly attributed to spatial inhomogeneity across the TMDC films [121]. At present, this is a general problem but is expected to be alleviated as the synthesis technology matures further.

6.2.3. State-Retention Tests

State-retention is another crucial FOM which is a measure for the stability of the resistance states over time after they are triggered by the

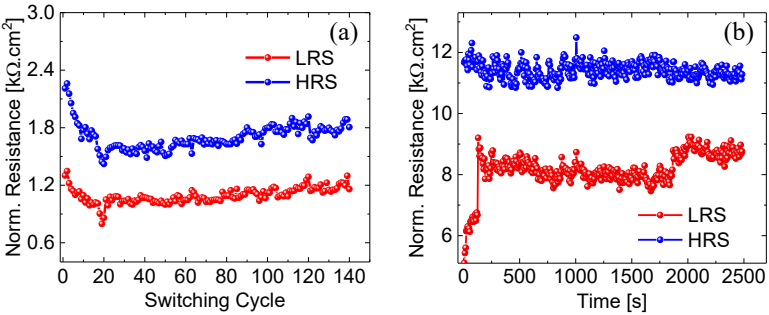

Figure 6.4: (a) Endurance data obtained from the "Si/MoS_2/Metal" hybrid Memristors showing the devices' endurance for at least 140 manual DC switching cycles in ambient conditions. The resistance values in each cycle were obtained from current levels at a READ voltage of -1.5 V following a SET (-3.5 V) and RESET (+4 V) voltages applied for 2 s. (b) State-retention data obtained from the devices demonstrating a non-volatile switching behavior with stable resistance states for at least 2500 s in ambient conditions. The resistance values were obtained from current levels read at a READ voltage of -1.5 V following a SET (-4 V) and RESET (+4 V) voltages applied only at the first cycle for 2 s.

application of the SET and RESET programming voltages [184, 227]. Thus it can be used to identify whether or not a given switching behavior is non-volatile. The retention data of the present devices is achieved by using the measurement procedure described in subsection 3.5.2 in ambient atmosphere. The result is presented in Fig. 6.4b where both the LRS and HRS levels were retained for at least 2500 s. Here, in contrast to the endurance test procedure, the SET voltage was applied only at the very first run to trigger the LRS. The LRS then retained its state until the RESET voltage was applied after 2500th second to switch it to the HRS, which also retained its state for another 2500 s like for the LRS. This asserts the non-volatile nature of the RS phenomena in these devices. Apart from the general positive message it carries, the data in Fig. 6.4b also exhibits a gradual shift of the LRS after 1900 s, which corresponds to the 300th reading cycle. This resistance shift may be due to a random parasitic effect of ionic diffusion during the READ phase. Nevertheless, these are early and first results of RS in vertical TMDCs and effects need further investigation to be fully understood.

6.3. Investigation of Origin of the RS Behavior

Electric-field driven movement of mobile OH^- ions, presumably along the van der Waals gaps of the layered MoS_2 structure, is proposed as the responsible mechanism for the observed RS behavior. The experimental evidence on the presence of the OH^- ions in the device structure and their potential origin are reported in chapter 4 and in previous works carried out during this thesis [26, 27]. There, it was experimentally demonstrated that these ions are mobile and they move towards the Si/MoS_2 interface in response to a negative bias-stress applied on the TE and move away from the interface in response to a positive bias-stress. This observation is in agreement with previous reports suggesting the MoS_2's layered crystal structure along with its anisotropic electronic properties facilitates ionic transports along the van der Waals gaps [98, 123, 259]. Also, analytical simulations described in section 6.3.2 suggest that the position of the OH^- ions with respect to the Si/MoS_2 interface influences the energy barrier height at the junction [24, 28]. Hence, the modulation of the energy barrier heights at the Si/MoS_2 junction gives rise to different resistance states, and thus the RS. As will be discussed in the subsections below, this argument was verified through switching tests accomplished in controlled ambient and vacuum conditions by assessing the influence of water adsorbates in the ambient air on the RS behavior.

6.3.1. Ambient vs Vacuum Switching Performance

The devices were further characterized in vacuum (~7x10^{-3} mbarr). The sample was kept inside a cryogenic probestation with an active pumping for over 60 hours to ensure that water adsorbates are removed from the sample. The resulting I-V sweep (Fig.6.5a) and endurance data (Fig. 6.5a) exhibit much smaller switching ratios compared to their ambient counterparts from the same devices. Similar trends were observed from vacuum measurements on other devices as well. The result is in line with the assertion made at the beginning of the section regarding water adsorbates and their catalytic splitting as the possible origin for the observed RS behavior. For further verification, subsequent ambient-vacuum-ambient switching tests were conducted on a single device which is different from the one in Fig. 6.5. The endurance test conducted initially in the ambient condition exhibited a clear RS behavior (Fig.6.6a) which is almost completely lost in the endurance test performed in vacuum (Fig. 6.6b), consistent with the

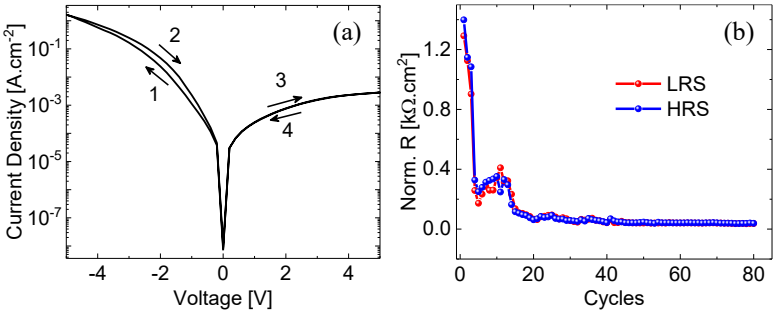

Figure 6.5: (a) DC I-V sweeps carried out on the present devices in vacuum by using the same measurement procedure as that in ambient. The result exhibits that the absence of adsorbates in the vacuum condition resulted in a dramatically reduced RS window compared to the case in ambient condition (see Fig. 6.1b). (b) Endurance test on the same device measured in ambient condition (see Fig. 6.4a). The graph shows that the endurance has degraded considerably in vacuum compared to that in ambient and shows almost no switching behavior, consistent with the result obtained from the I-V sweep in "a".

observation in Fig.6.5. Then, the sample was immediately exposed back to the ambient atmosphere and, the RS behavior was observed again. This experimental observation leads to the conclusion that water molecules in ambient air get adsorbed into the sample and the catalytic splitting of these by MoS_2 [27] (see subsection 1.2.1) gives rise to OH^- ions that drive the RS behavior as explained at the entrance of the present section. Only few experimental reports are available on the vacuum RS functionality of MoS_2-based two-terminal memristors with a vertical architecture. Gate-tunable RS of three-terminal lateral memristors with single layer polycrystalline MoS_2 has been demonstrated in vacuum by Sangwan and coauthors [120, 121]. However, unlike the present case, the vacuum condition did not appear to impact the RS in their case and, as a result, they attributed the RS behavior to migration of grain boundaries and sulfur vacancies. The quenching of the RS in the present devices in vacuum, in contrary to the above reports, indicates that grain boundaries and sulfur vacancies should not have a dominating role in the RS. Another work by Kalita and coauthors reported volatile threshold switching of their "graphene/vertical-MoS_2/Ni" memristors that decreased in vacuum and they attributed the effect to oxygen [124], though without providing experimental evi-

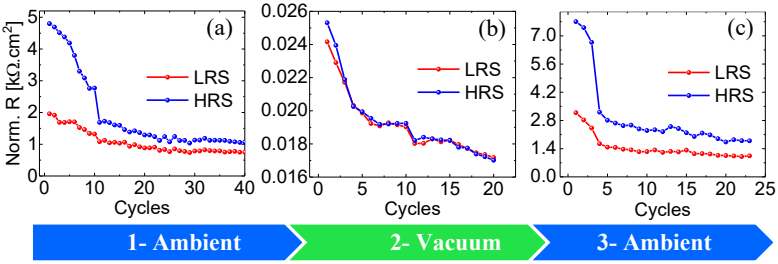

Figure 6.6: Systematic investigation of the effect of adsorbates in the ambient air on the RS behavior: (a) endurance tests in ambient condition showing a clear RS behavior, (b) endurance tests on the same device in a vacuum condition showing no RS behavior in the absence of adsorbates and (c) endurance tests on the same device after it is exposed back to air. The presence of the RS effect in both ambient conditions before and after the measurement in vacuum makes it clear that the effect is caused by water adsorbates in the air.

dences supporting the claim.

6.3.2. The Switching Mechanism

Based on the discussion so far, the mechanism for the RS operation in the current case can be explained as the following. Application of a negative V_{TE} pushes the OH^- ions toward the p-Si/MoS_2 interface and this results in a lower energy barrier height at that interface (i.e. SET). A positive V_{TE} moves the OH^- ions farther away from the interface and gives rise to a relatively higher barrier height (i.e. RESET). Hence, the resistance state of the devices is switched from HRS to LRS by the -V_{TE} and from LRS to HRS by the +V_{TE}. To help better visualize the switching dynamics proposed here, band schemes of the device structure illustrating the SET, READ and RESET conditions are given in Figs. 6.7a - 6.7d. At the READ condition (i.e. $V_{TE} = -1.5V$), the energy bands align such that holes from the Si overcome the energy barrier at the Si/MoS_2 interface and be injected into MoS_2, whereas electrons moving in the opposite direction encounter a much higher barrier at the Cr/MoS_2 interface. This makes the hole injection the dominating transport and thus modulation of the hole barrier height leads to resistance modulation between LRS and HRS. To verify this consideration, analytical simulations were performed by taking into account the position of the OH^- ion distribution which was noticed

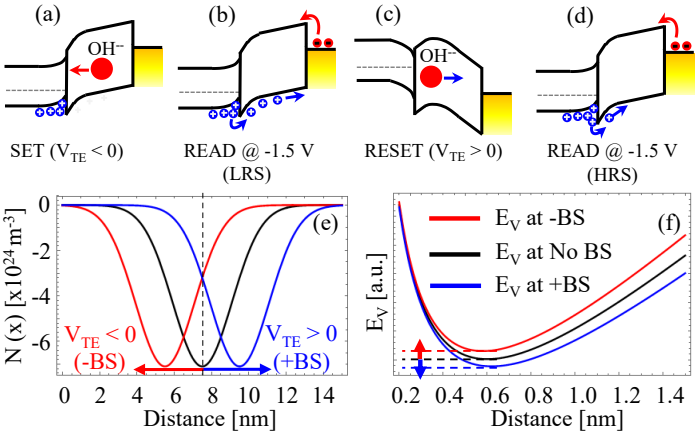

Figure 6.7: Illustrative band schemes of the "p-Si/MoS_2/Metal" memristors showing the alignment of bands during the: (a) SET condition where a –BS pushes the OH^- ions towards the Si/MoS_2 interface and give rise to a decreased energy barrier height, (b) the READ phase in which the current level in the LRS is read at -1.5 V, with the hole barrier height becoming lower in this case. (c) RESET condition where a +BS pulls the OH^- ions away from the Si/MoS_2 interface and give rise to an increment of the energy barrier height, and (d) the READ phase where the current level in the HRS is read at -1.5 V, with the hole barrier height becoming higher this time. (e) Gaussian distribution of the OH^- ions assumed at different positions. (f) Calculated valence band for different charge positions. The contents in this figure are reproduced from ref. [28], ©2020 John Wiley & Sons, Inc.

to influence the electric field distribution across the structure. This, in turn, determines the alignment of the Si and MoS_2 bands and, in consequence, modulates the energy barrier height at the Si/MoS_2 interface. A Gaussian distribution is assumed for the OH^- ions at a random position representing the equilibrium position at no bias-stress (BS) (i.e. the black Gaussian distribution in Fig. 6.7e). Another two similar Gaussians distributions were assumed at positions (1) shifted towards the Si/MoS_2 interface representing a condition with –BS (red Gaussian distribution) and (2) shifted towards the Cr/MoS_2 interface representing a condition with a +BS (blue Gaussian distribution). The valence band (E_V) of MoS_2 is then calculated using the corresponding three Gaussian distributions given in Fig. 6.7e. As shown in Fig. 6.7f, the results demonstrate that the position of the OH^- ion distribution indeed modulates the energy barrier at the Si/MoS_2 interface. This

in turn regulates the charge carrier transfer from Si to MoS_2 and thus modulates the resistance states between LRS and HRS.

6.4. Summary

Si/MoS_2/Cr vertical memristive devices with vertically aligned MoS_2 layers serving as the switching medium were fabricated and characterized. Electrical characterizations on these devices have demonstrated a forming-free bipolar resistive switching behavior. Endurance tests have exhibited stable switching behavior over several cycles. Furthermore, state-retention data have shown that the resistance states can be maintained over a period of time, indicating that the switching behavior is non-volatile. Measurements in subsequent ambient and vacuum conditions in combination with analytical simulations and findings from chapter 4 have confirmed that the observed switching behavior is due to bias-induced movement of OH^- ions presumably along the van der Waals gaps of the MoS_2 active medium. The movement of the ions towards or away from the Si/MoS_2 interface tunes the energy barrier height at the interface, leading to modulating resistance states.

7

MoS_2/Graphene Photodetectors on Silicon

Photodetectors are optoelectronic Semiconductor devices that are used in applications such as sensing, imaging, pattern recognition, telecommunication and security. Advancement in these applications requires photodetectors with broadband sensitivity and high speed optical detection capabilities. 2D materials such as graphene and MoS_2 are being actively explored in this regard owing to their appealing electrical and optical properties summarized in sections 1.1.1 and 1.2.1. Graphene's ultra-thinness, high absorption coefficient for a single atom thickness [42], extremely high charge carrier mobility and a broadband optical absorption have inspired several optoelectronic applications. Some examples are broadband photodetectors, ultrafast photodetectors and transparent conductive electrodes (TCEs) for LEDs, solar cells and touch panels [45,260,261]. Similarly, TMDC materials, in particular MoS_2 is receiving increasing attention from the optoelectronics community due to its properties such as ultra-thinness, high absorption coefficient, tunable optical band-gap [88] etc. which are required for enhanced photodetection performance. Its high detectivity per layer has already led to the realization of phototransistors and photodetectors [115,262,263]. However, most of the reported devices are based on either exfoliated or as-grown MoS_2 films transferred onto technologi-

cally relevant substrates. While devices from exfoliated films lack scalability and reproducibility, those based on transferred films are prone to performance inhibiting polymer residues at interfaces [88, 126, 264]. In this thesis, scalable VPS/TAC- and CVD-grown large-area MoS_2 and graphene films were utilized to fabricate "Si/MoS_2/Graphene" hybrid heterojunction photodetectors with polymer-free interfaces by using scalable and semiconductor technology compatible processes. The layered MoS_2 films were grown directly on the Si enabling easy device integration. The broadband spectral responsivity achieved from these devices are presented in this chapter.

7.1. The Device Structure in Reverse-Bias

The detailed fabrication scheme for the photodetectors supported by illustrative diagrams is given in section 3.4.2. The device structure comprises a vertical stack of n-type Si bulk, ~1 μm highly doped Si (n^+-Si), ~15 nm MoS_2 and a single layer graphene (SLG) as shown in Fig. 7.1a. While the SLG serves both as a transparent conductive electrode and a broadband photo-responsive layer, the MoS_2 and Si layers serve as the main photo generation sites. The n^+-Si segment, which is formed through ion implantation, plays significant roles in the device's operation. Is doping concentration decreases as one goes from the surface to its depth [265]. This leads to a reduction of approximately ~ 0.1 – 0.15 eV of its bandgap at a maximum dopant concentration of ~ 10^{20} cm^{-3} at the Si/MoS_2 interface [266, 267]. A schematic representation of the device and its band diagram at reverse bias are shown in Figs. 7.1a and 7.1b, respectively. In addition, the photo-generation and transfer process of electron-hole pairs are indicated by solid spheres (red for electrons and blue for holes) and arrows, respectively. Due to the high doping concentration, the n^+-Si screens the bulk Si underneath and this makes the full applied voltage appear mainly across the MoS_2 part. This is because the n^+-Si segment has an extremely large capacitance compared to that of MoS_2 and thus, given the inverse relation between capacitance and voltage, there will be a negligible voltage drop across the n^+-Si and the n-Si bulk. As indicated in Fig. 7.1b, the photo-generated electrons in the MoS_2 and n^+-Si segments need to overcome the electron-barrier at the n^+/n-Si junction, Φ_e, to contribute to the measured photocurrent.

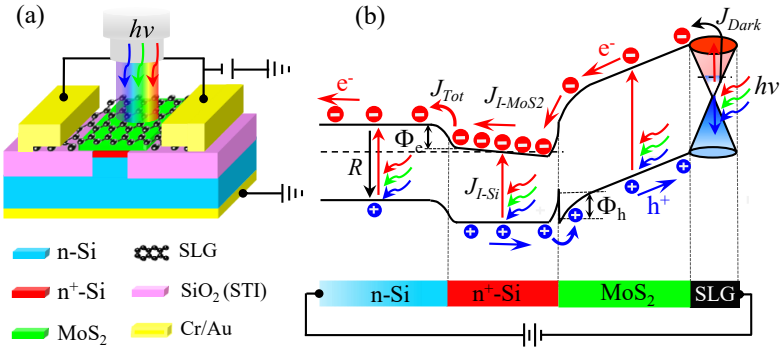

Figure 7.1: Schematics of the "n^+-Si/MoS_2/SLG" hybrid heterojunction photodetectors in a reverse-biased configuration showing (a) an isometric view of the devices and (b) an energy band diagram illustrating the device structure and the corresponding band alignments. This schematic also illustrates the process of photoexcitation, transport of the photo excited carriers and the associated current contributions for the measured photocurrent.

7.2. Photocurrent Generation in the Devices

Opto-electrical characterizations, i.e. I-V measurements with white light illumination and spectral responsivity (SR) measurements with monochromatic light illumination were done on the present devices. Description of the measurement procedures can be found in section 3.5.3. The measured data in Figs.7.2 and 7.3 show that white or monochromatic light irradiation on the device structure generates a bias- and wavelength-dependent photocurrent. The irradiated photons excite electrons possibly from both the valence band and gap-states to the corresponding conduction band of the photo-active materials in the structure, creating electron-hole pairs as illustrated in Fig. 7.1b. During a reverse-biased condition, the photo-generated electrons move towards Si while the corresponding holes move towards the SLG terminal (Fig. 7.1b) to be extracted by the external circuit and provide photocurrent. As stated in chapter 2, only carriers that are generated either in the region of the structure where electric-field is present or in regions lying within the diffusion length of the carriers contribute to the measured photocurrent. Carriers outside of these regions recombine before they are extracted. Considering this and the electrostatic screening effect of the n^+-Si emphasized in section 7.2, only electron-hole

pairs generated within the 15 nm MoS_2 and the 1 μm n^+-Si segments contribute to the measured photocurrent. Those generated in the n-Si bulk undergo recombination as the diffusion length of the carriers is about 1 μm which is only in the range of the thickness of the n^+ segment.As illustrated in Fig. 7.1b, the n^+ region forms a potential well sandwiched between the MoS_2 and the n-Si segments and it serves as a reservoir for electrons that are generated there, those coming from the MoS_2 segment and those due to the thermal current injected from the graphene side. Accumulation of the electrons in the well builds a negative charge that lowers the electron potential difference between the n- and n^+-Si. As a result, the energy barrier at the n^+-/n-Si junction, Φ_e, undergoes lowering until the well reaches a steady-state condition whereby the total electron current entering the well becomes equal to that leaving. The thermal current (dark current) influences all the J-V measurements by impacting the lowering effect on the n^+/n potential step. By presuming the measured photocurrent density, J_{Ph}, to be mainly due to the electrons injected across Φ_e, it can be expressed as

$$J_{Ph} = Aexp\left[\frac{\Phi_{e0} - E_{DI}(V,\Theta)}{kT}\right], \tag{7.1}$$

where A is a constant, Φ_{e0} is Φ_e before lowering, V is applied bias, Θ is photon intensity. $E_{DI}(V,\Theta)$ is a lowering energy quantity originating from the negative charge of excess electrons accumulated in the n^+-well that are coming from the dark-current and the photo-excitations, hence the letters D and I in the subscript. The dark current is dependent only on bias, V, and the photo-excitation depends only on the photon intensity, Θ. As illustrated in Fig.7.1b, the measured photocurrent is equivalent to the total current, i.e. $J_{Ph} \equiv J_{Tot} = J_{I-Si} + J_{I-MoS2} + J_{Dark}$, where J_{I-Si} is current due to illumination of the n^+-Si segment, J_{MoS2} is current due to excitations in the MoS_2 segment and J_{Dark} is the thermal current from the graphene side.

7.3. Photocurrent Due to White Light Excitations

J-V characteristics of the devices with and without white light irradiation are shown in Figs. 7.2a and 7.2b in linear and semi-logarithmic plots, respectively. The inset of Fig. 7.2a shows a magnified linear portion of the reverse current for clarity. The observed asymmetry of the dark current (black curves in Fig. 7.2) indicate a rectifying behavior confirming the diode nature of the structure, albeit with a visibly

high reverse leakage compared to standard photodiodes that result in a nearly constant reverse current [65, 268, 269]. This can be attributed

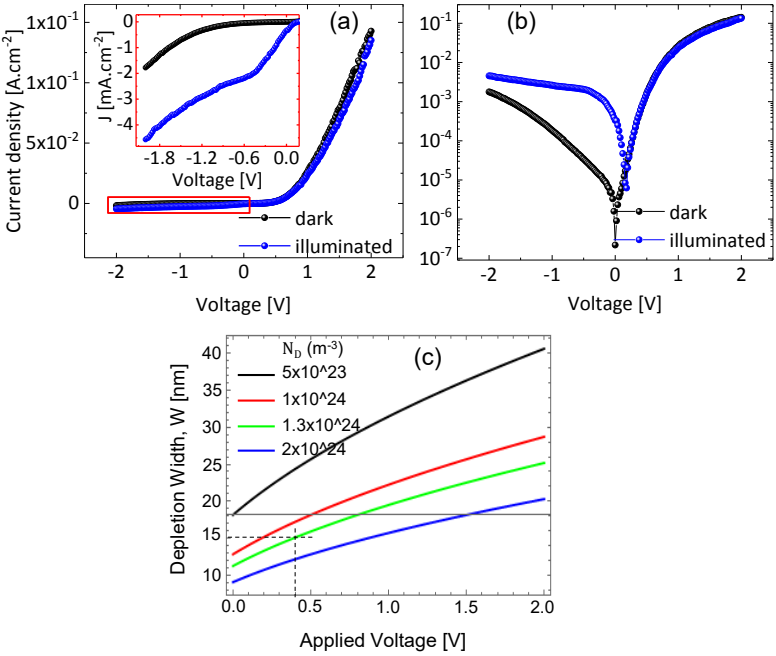

Figure 7.2: I-V measurements on the "n-Si/MoS_2/SLG" photodiodes, under dark and white light-illumination conditions presented as (a) linear and (b) semi-logarithmic plots exhibiting a considerable photocurrent reaching two orders of magnitude. The inset graph in "a" shows a magnified version of the main graph in the reverse-biased regime. (c) Analytical simulations demonstrating the relation between the MoS_2 depletion width, W, and the applied bias for various doping concentrations of the MoS_2 film showing that the 15 nm MoS_2 film is completely depleted already at V ≥ 0.4 V.

to a bias-regulated lowering of the electron-barrier at the SLG/ MoS_2 junction due to a Schottky effect and/or due to a tuning of the graphene Fermi-level. The figure also shows that irradiation of the device with white light gives rise to a significant increase of the reverse current due to excess photo-generated carriers (see the red curves in the figure). Another observation from the J-V data is the kink/shoulder on the red curve at around -0.5 V. This can be explained by the MoS_2 part becoming fully depleted at about that voltage value. Analytical simulations of

the depletion width of MoS_2 at a reasonable electron doping similar to reported values adapted to the present thickness [270, 271] suggest that the MoS_2 film becomes completely depleted already for $V \geq 0.5$ V (Fig. 7.2c). Hence, a voltage increase above that level would not have effect on the depletion width as it has already reached its maximum. It is also noticed that the J-V characteristics has a lower slope after the kink point compared to the slope before. This may be due to an enhanced optical influence that is dominating the dark current for voltages above the kink point because the width of the depletion region in MoS_2 reaches its maximum there. This argument is consistent with what Eq. 7.1 would give for a dominating optical part.

7.4. Photocurrent Due to Monochromatic Light Excitations

The photosensitivity of the present devices was further studied through spectral responsivity (SR) measurements that enable investigation of the influence of incident light wavelength on the photocurrent. The SR measurements were carried out by using a lock-in technique where the measured data are calibrated using commercial Si and AlGaAs reference photodetectors of known responsivity. The detailed procedure employed in conducting the SR measurements can be found in section 3.5.3. The measured SR data indicating photodetection capability in a broad spectral range, i.e. from ultraviolet (UV) to near infrared (NIR) will be discussed below. The calibrated SR measurements here are limited to the wavelength range of 350 – 2000 nm due to the material specific spectral bandwidths of the Si and InGaAs reference photodiodes.

7.4.1. Photodetection in the UV and VIS Regions

The measured SR data covering the spectral range of 360 nm - 1200 nm is depicted in Fig. 7.3a. In contrast to the Si reference photodetector (the black dashed curve in Fig. 7.3a), the present devices exhibit more than one SR peak within the Si operational band and this is consistent with what Yim and coauthors observed for "p-Si/MoS_2" photodiodes [272]. Therefore, combining this observation with the fact that photo excitations inside the Si bulk do not contribute to the measured photocurrent due to the screening effect of the n^+ part (see section7.1), the present SR data can be considered to originate from a dominating

MoS_2 contribution. Thus, they are a finger print of the MoS_2 band structure. The broad SR peak (the first from the right) at ~840 nm (1.48 eV) is associated with the indirect band transition of MoS_2. In Yim et. al's report, a SR peak observed at a similar wavelength position is interpreted similarly [272]. This peak shows a maximum responsivity of ~120 mAW^{-1} at -2 V and this is about 13 times higher than that reported for the "p-Si/MoS_2" heterojunction photodiodes [272]. However, it is also important to note that this SR value is only one-fourth of the responsivity obtained from the standard Si reference diode, further supporting the argument that the measured responsivity comes mainly from MoS_2 despite the largest proportion of the incident light reaches the Si bulk where the photo-generated carriers recombine. A second SR peak is exhibited at a wavelength of ~500 nm (2.48 eV) with its starting point at ~615 nm (~2 eV) suggesting that it is related to the direct band transition of MoS_2 which, according to theory, lies in the range of 1.8 eV - 1.95 eV [88, 273]. Yim et. al, who have used a VPS-/TAC-grown MoS_2 like in this work, have observed a SR peak at a similar wavelength (i.e. 500 nm) and attributed it to the heavy-hole degenerate band of the MoS_2 direct transition [272]. In addition to the two SR peaks discussed, the rising edge of a third SR peak is apparent in the UV portion of the spectrum at around 430 nm (2.88 eV). The exact origin of this peak is not fully understood and needs further investigation. One possible explanation can be that short wavelength photons in UV light are normally absorbed near the surface of the device (to a very shallow depth). Hence, a good interface with minimal recombination would be required between the generation region and the collector electrode to enable effective extraction of the carriers. Since the 2D/2D interface between MoS_2 and the SLG collector in the present devices is expected to be sharp, smooth, polymer-free and also in principle dangling bond-free, one may presume an efficient carrier extraction leading to the observed response. Tao and coauthors have demonstrated an MoS_2/graphene 2D/2D interface with suppressed carrier recombination that enabled fast photodetection with high responsivity [260]. Another interesting observation from Fig. 7.3a is the bias-dependent behavior of the measured SR data. With a careful evaluation, it is noticed that the peak-to-dip ratio of the SR curves remain almost unchanged for the various biases applied. This indicates that the observed bias-dependence is indeed an inherent property of the device and not a parasitic effect incurred by the measurement setup. This enables

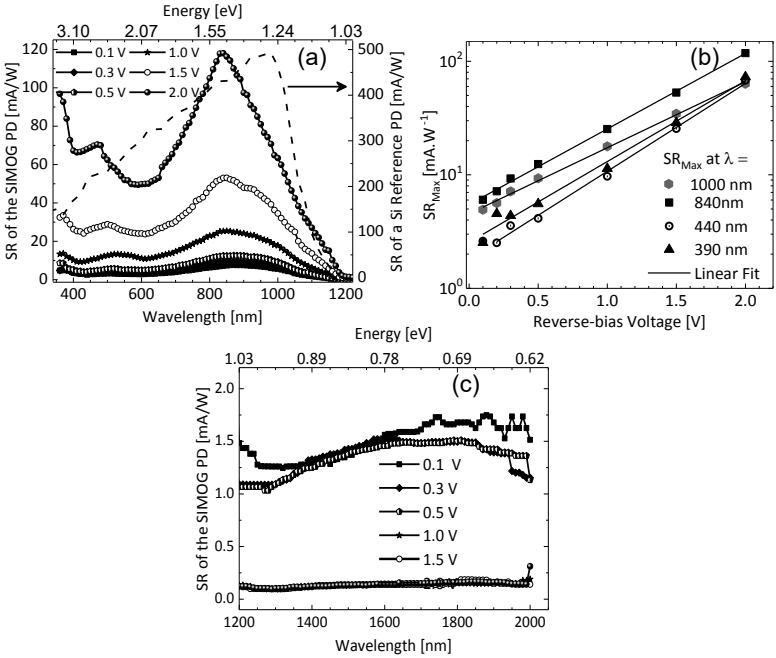

Figure 7.3: (a) The measured SR of the present devices exhibiting a distinct structure in the UV and VIS range that is dictated by the band structure of MoS_2. The black dashed curve is the responsivity obtained from a commercial Si reference photodiode that was used to calibrate the measurements. The data also exhibits an exponential bias-dependent behavior possibly due to a bias-induced modulation the electron barrier at the n^+-/n-Si junction. (b) Semi-logarithmic plots of "SR Vs reverse-biased voltage" data extracted from "a" for different light wavelengths confirming the exponential bias dependence of the SR data. (c) a nearly bias- and wavelength-independent SR of the devices in the NIR region that can be attributed to excitations in the graphene layer as well as absorptions through inter-layer transitions and mid-gap states in the MoS_2 bandgap.

scaling up of the sensitivity of the photodetectors by external bias. To further identify the exact relationship between the SR and V_{RVS}, the maximum responsivity (SR_{MAX}) at 390 nm, 440 nm, 840 nm and 1000 nm wavelength values were extracted from Fig. 7.3a and plotted as a function of V_{RVS} as shown in Fig. 7.3b. The resulting data shows a clear exponential trend between the two quantities. This suggests that the bias-dependence of the SR is possibly due to a bias-regulated lowering effect on the electron barrier at the n^+/n-Si junction (Φ_e), modulating the photocurrent due to electrons transported from the n^+-well. The slope variation observed in the plots at different wavelengths can be because of varying photon intensity with respect to wavelength.

7.4.2. Photodetection in the NIR Region

Further SR measurements conducted in the wavelength range 1200 – 2000 nm (0.62 - 1.03 eV) reveal the potential of the present devices as IR detectors (Fig. 7.3c) in addition to the UV and visible light detection capability discussed above.

This is an unexpected observation given that neither the Si nor the MoS_2 parts should be able to absorb photons of energies way below their optical band gaps, i.e. 1.1 eV and 1.3 eV, respectively. Hence, this part of the responsivity can originate from excitations in the graphene layer which is known for its nearly constant and broadband absorption owing to its gapless nature and linear energy dispersion in its band structure [42, 43, 274]. It should be mentioned that the responsivity value here (1.75 mAW^{-1}) is much smaller than that achieved in the UV and visible regions. Nevertheless, the value is still encouraging given the ultra-thinness of graphene compared to conventional 3D materials such as Si. This observation is consistent with similar responses reported for single layer graphene-based photodetectors [268,275]. Other possible mechanisms that could contribute to the NIR response may include interlayer transitions and absorptions through mid-gap states such as sulfur vacancies in the MoS_2 band gap [115, 276, 277].

7.5. Summary

Photodetectors based on graphene/MoS_2 vertical 2D-heterostructures were fabricated on Si, with a very thin heavily doped (n^+−Si) layer separating the bulk Si from the 2D-heterostructure diode. Optoelectrical characterizations under white light illumination show significant

photoconductivity. Spectral responsivity (SR) measurements carried out by using monochromated light irradiation and a lock-in technique exhibit a broadband response that covers from UV to IR part of the electromagnetic spectrum. In contrast to standard Si photodetectors, the present devices exhibit more than one SR peak in the wavelength range corresponding to the Si operational band. This is due to the n^+-Si layer in the structure giving rise to a screening effect that leads to absence of electric-field in the bulk region. This in turn causes photo-generated carriers in the region to recombine before yielding photocurrent, thus suppressing silicon's contribution so that the measured responsivity is mainly dominated by the graphene/MoS_2 heterostructure diode. The responsivity in the UV and visible regions maybe due the direct and indirect transition bands of the layered MoS_2. The observed IR response with a small magnitude in the energy range well below the band gaps of Si and MoS_2 can be attributed to absorptions in graphene and/or absorptions through defect states within the MoS_2 band gap. Additional observations worth mentioning are the blue-shift and the exponential increase of the SR with increasing bias, which both require further investigations. Overall, this work demonstrates integration of novel 2D-materials with existing semiconductor process technology to realize hybrid devices with a promising potential for next generation optoelectronic applications.

8

Summary and Outlook

8.1. Summary

In this thesis, the two most explored novel 2D materials, MoS_2 and graphene as well as their heterostructure were integrated with conventional 3D silicon to form vertical heterojunction devices that were investigated for electronic, optoelectronic and neuromorphic applications. The fabrication process used is generally scalable and semiconductor technology compatible although certain challenges remain to be alleviated. This paves the way for integration of related 2D materials with the Si platform, fulfilling the essential requirement for "more than Moore" applications. In this regard, for all devices demonstrated in this thesis, MoS_2 films were grown directly on the silicon crystal by using the vapor phase sulfurization technique. This ensured achieving polymer-free interfaces while maintaining large scale production. Transmission electron microscopy studies on the MoS_2 reveal that the film is nanocrystalline and that it contains 2D layers that have a predominantly vertical orientation. Admittance spectroscopy conducted on $Si/MoS_2/Cr$ capacitors establish the dielectric constant of MoS_2 in the range of 2.6 - 2.9. Also, bias-stress capacitance-voltage and conductance-voltage measurements suggest the presence of mobile negative charges inside the film. Time-of-flight secondary ion mass spectroscopy analysis confirm that these are OH^- ions with estimated concentration of

$\sim 2.8 \times 10^{20}$ cm^{-2}. Further characterizations in combination with analytical simulations confirm that interface states with a concentration of $D_{it} = 1.5 \times 10^{13}$ $cm^{-2}eV^{-1}$ exist and that they interact with the electric-field driven mobile OH^- ions. MoS_2 was further investigated for a potential use in graphene base hot electron transistors (GBTs). A crucial step towards realizing high performance GBTs is to enhance the hot-electron injection from the emitter into the base, which in turn requires an efficient emitter-base-barrier that promotes electron transport by thermionic emission. Theory suggests that this can be realized by using low energy barrier materials with respect to the emitter, i.e. by using semiconducting barrier layers [199]. Hence, MoS_2 was chosen for its semiconducting nature with bandgap and electron affinity values enabling band alignments that provide a small conduction band offset with respect to the Si emitter. Therefore, Si/MoS_2/graphene vertical heterojunction devices that are equivalent to the emitter diode of GBTs were fabricated and the charge carrier transport across the n^+-Si/MoS_2 junction was investigated. In this end, temperature-dependent current-voltage characteristics were measured and analyzed. In corroboration with analytical simulations, the experimental data confirmed that the electron transport across the heterojunction is dominated by thermionic emission. This fulfils the prerequisite for using these structures as efficient emitter diodes in GBTs which are promising devices for high speed electronics.

Furthermore, vertical Si/MoS_2/Cr devices were investigated for potential neuromorphic applications. These devices were characterized through I-V sweeps and resistive switching measurements including endurance and state-retention tests. The results generally exhibited a memristive performance with a formation-free, bipolar and non-volatile resistive switching behavior. Endurance and state retention for at least 140 DC switching cycles and for 2500 seconds, respectively, were also demonstrated. Furthermore, results from systematic switching tests carried out in subsequent ambient and vacuum conditions verified that the observed switching phenomenon can be generally ascribed to electric field-driven mobile OH^- ions that are moving along the van der Waals gaps of the layered MoS_2. The general anisotropic property of MoS_2 along with the vertical orientation of its layers and van der Waals gaps aligned parallel to the applied electric field have likely facilitated the movement of the OH^- ions in response to the programming biases applied on the top electrode. Analytical simulations

confirmed that the movement towards and away from the Si/MoS_2 interface modulates a potential barrier at the interface. This regulates the charge carrier transfer across the barrier and thus gives rise to modulation of resistance states of the devices.

Finally, the potential of the Si/MoS_2/graphene heterojunction diodes to operate as photodetectors was demonstrated experimentally. Opto-electrical characterizations (i.e. I-V measurements with light irradiation) of the diodes exhibit broadband spectral sensitivity that covers from the ultraviolet up to the near infrared range of the electromagnetic spectrum. The spectral response data contains multiple peaks in the visible and ultraviolet regions. The response in these spectral regions is dominated by the contribution from the MoS_2 segment which has a thickness of 15 nm. The data also exhibited infrared response in the energy range below the Si and MoS_2 bandgaps and this is attributed to absorptions in the graphene layer, interlayer transitions at the junction as well as absorptions through defect states in the MoS_2 bandgap, most likely originating from sulfur vacancies. In general, the overall investigations and findings of this thesis make substantial contributions for advancement of device research. This also sets a trend for integration of novel 2D materials and their heterostructures with existing Si technology to produce hybrid heterojunction devices for more than Moore applications.

8.2. Outlook

Despite the extensive work accomplished in this PhD thesis, there is room for further improvements in relation to device design, material selection, processes optimization and device characterization. Furthermore, there are experimental observations that require further investigations. This section highlights research activities proposed as potential future work. The ultimate goal for designing and demonstrating the MoS_2-based vertical heterojunction devices that were discussed in chapter 5 was to provide efficient MoS_2 emitter diodes for high performance graphene base hot electron transistors (GBTs). Therefore, utilization of the successfully demonstrated MoS_2 emitter diodes to realize high performance GBTs would be a natural recommendation as future research.

The present memristor structures were good enough to demonstrate the general promise of MoS_2 for neuromorphic computing applications. Further performance enhancement can be achieved by im-

proving the device design, the quality and thickness of the MoS_2 active layer, the type of electrodes and the electrical characterization routines used. In connection with design, implementing cross-bar arrays with suitable cell size would be beneficial as it is the most preferred configuration in real RS products. This design also offers small active cell size which may lead to a higher resistance in the HRS and thus give rise to a larger switching ratio (i.e. larger I_{LRS}/I_{HRS}). Also, it is essential to assess the switching behavior in MoS_2 films synthesized by other techniques such as MOCVD, as the film quality and layer orientation can be different from the films used in this thesis possibly leading to a different switching mechanism as well. Besides, due to its layered nature, MoS_2 provides a switching behavior that modulates with number of layers. Therefore, investigation needs to be done to determine the optimal number of layers that provides the desired switching performance. Extending this application to other TMDC materials should be part of a future activity. Furthermore, the choice of electrode material can influence the switching performance and the use of asymmetric and redox-active electrodes is generally recommended to achieve a bipolar RS behavior. Hence, it would be a good strategy to assess if and how the switching behavior correlates with the metal type so that the most suitable electrodes are found for the MoS_2 memristors. Finally, the switching tests on the present devices were based on manual DC switching measurements as a pulsed voltage source was not available at the time. Hence, future research need to use a more advanced characterization routines in a more optimized setup equipped with a PVS and automated measurement routines.

The broadband spectral responsivity (SR) of the graphene/MoS_2 photodiodes that were built on silicon (Si) is a useful feature for many applications. However, some of the observations from these devices require further investigation that need to be carried out in the future. These include the exponential bias dependence of the spectral responsivity and the observed blue shift of the SR peaks as the reverse bias increases. The device structure, as it is now, allows suppressing the SR of the bulk Si to be able to investigate the performance of the graphene/MoS_2 2D heterostructure photodiodes. The Si in the present design has a technological relevance as it helps achieve the know-how of integrating such devices with the existing Si-based integrated circuit technology. Therefore, the design can be slightly improved by excluding the heavily doped segment such that the SR contribution of the Si part is enhanced.

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Appendices

A- Band Alignment of the Forward-Biased MoS_2/Graphene Junction

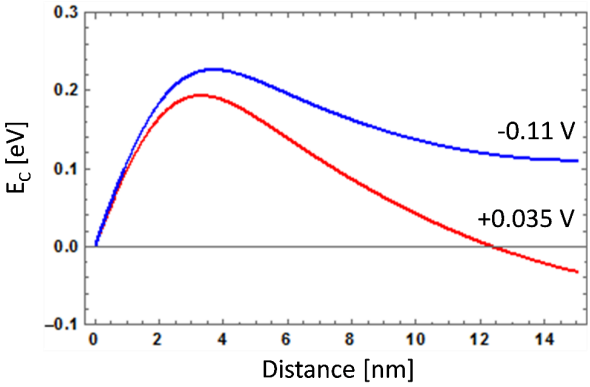

Figure 8.1: Analytical simulation demonstrating variation of the MoS_2 conduction band energy, EC, as a function of distance from the Si/MoS_2 interface. The graph shows two different values of applied voltage, i.e. +0.035 V (red) and – 0.11 V (blue) indicating that the graphene/MoS_2 interface never constitutes an energy barrier in a forward biased junction. The blue curve shows that no considerable barrier is established even for negative biases up to -0.11 V. This verifies that the determining barrier for the forward-biased transport in the n^+-Si/MoS_2/graphene diodes is only the n^+-Si/MoS_2 heterojunction barrier.

B- 2D Material Synthesis Processes

B.1- Graphene Synthesis by Chemical Vapor Deposition

Table 8.1: Chemical Vapor Deposition (CVD) Growth of graphene on copper (Cu) foil.

Step	Process Description	Duration
1	Etching the surface of a Cu foil using 50 g/l (0.2M) $Na_2S_2O_8$ solution	5 min
2	Rinsing of the Cu foil in DI-water followed by drying it with N_2 gas	5 min
3	cleaning the foil in an ultrasonic bath with acetone	10 min
4	Rinsing it with isopropanol alcohol (IPA) and drying it with N_2 gas	5 min
5	Annealing the Cu foil inside a CVD furnace at 900°C and 190 sccm Ar	30 min
6	Annealing the Cu foil (950°C, Ar/H_2 (80%/20%), 10 Torr) for oxide removal	10 min
7	Graphene growth (950°C, $H_2/Ar/CH_4$ (80%/15%/5%), 10 Torr)	30 min
8	Cooling down the furnace	30 min

B.2- MoS_2 Synthesis by Vapor Phase Sulfurization

Table 8.2: MoS_2 synthesis using the vapor phase sulfurization process.

Step	Process Description	Duration
1	A lithography step to define windows for Mo deposition	-
2	Deposition of 5 nm Mo film by e-beam evaporation on Si	-
3	A lift-off process to remove excessive Mo in unwanted areas	-
4	Vaporizing sulfur powder at 150 °C in a quartz tube furnace	-
5	Sulfurization of Mo (800 °C, 20 sccm Ar, P=2x10^{-3} mbar)	30 min
6	Unforced cooling of the furnace to room temperature	few hours

C- Graphene Transfer Processes

C.1- Graphene Transfer by Wet Chemical Etching Technique

Table 8.3: Graphene transfer by wet chemical etching method.

Step	Process Description	Duration
1	Spin-coating Cu/graphene samples with PMMA (2000 rpm, 500 rpm/min)	45 s
2	Baking the Cu/graphene/PMMA samples at 150 °C on a contact hotplate	4 min
3	RIE of the rear side of the Cu foil by O_2 plasma RIE (70 W, 70 sccm O_2, 50 mTorr)	40 s
4	Cutting desired pieces and etching Cu in 0.2 M $Na_2S_2O_8$	60-90 min
5	Rinsing the graphene/PMMA stack inside DI water	30 min
6	Cleaning the graphene/PMMA stack in 1% HCL solution	30 min
7	Rinsing the graphene/PMMA stack in DI water	30 min
8	transferring the graphene/PMMA stack onto the target substrate by scooping it	0.5 - 3 min
9	Drying the transferred graphene/PMMA stack in ambient condition	~4 hours
10	Baking the sample at 180 °C inside an oven	30 min
11	Remove PMMA in hot acetone (70 °C) followed	30 min
12	Rinse the sample in IPA	5 min
13	Transfer to a second acetone bath	20 min
14	Rinse the sample in IPA followed by drying with N_2 gas	0.5 min

C.2- Graphene Transfer by Electrochemical Delamination Technique

Table 8.4: Graphene transfer by electrochemical delamination process.

Step	Process Description	Duration
1	Spin-coating Cu/graphene samples with PMMA (2000 rpm, 500 rpm/min)	45 s
2	Baking the Cu/graphene/PMMA samples at 150 °C on a contact hotplate	4 min
3	RIE of the rear side of the Cu foil by O_2 plasma RIE (70 W, 70 sccm O_2, 50 mtorr)	40 s
4	Cutting the Cu/graphene/PMMA samples into desired pieces	1-2 min
5	Delaminating the graphene/PMMA stack from Cu (0.25 M KOH electrolyte, 2.3 V)	0.5-3 min
6	Rinsing the graphene/PMMA stack inside DI water	30 min
7	Cleaning the graphene/PMMA stack in 1% HCL solution	30 min
8	Rinsing the graphene/PMMA stack in DI water	30 min
9	transferring the graphene/PMMA stack onto the target substrate by scooping it	0.5 - 3 min
10	Drying the transferred graphene/PMMA stack in ambient condition	~4 hours
11	Baking the sample at 180 °C inside an oven	30 min
12	Remove PMMA in hot acetone (70 °C) followed	30 min
13	Rinse the sample in IPA	5 min
14	Transfer to a second acetone bath	20 min
15	Rinse the sample in IPA followed by drying with N_2 gas	0.5 min

D- Device Fabrication Processes

D.1- Fabrication of Si/MoS_2/Metal Structures

Table 8.5: MoS_2 Fabrication process for Si/MoS_2/Metal Structures.

Step	Process Description
1	Cleaning Si substrates in ultrasonic bath using acetone
2	Rinsing the samples in IPA
3	Rinsing the samples in DI water followed by N_2 blow dry
4	Photolithography process to define windows for Mo deposition
5	Removing the native oxide from the Si active areas using a 1:7 BOE solution
6	Deposition of 5 nm Mo film by e-beam evaporation on the Si substrates
7	Lift-off process to remove excessive Mo outside of the active regions
8	Vapor-phase sulfurization of Mo to obtain ~15 nm MoS_2
9	Photolithography step to define windows for gate metal formation
10	Deposition of Cr/Au metal stack by e-beam evaporation followed by lift-off

D.2- Fabrication of Si/MoS_2/Graphene Structures

Table 8.6: MoS_2 Fabrication process for Si/MoS_2/Graphene Structures.

Step	Process Description
1	RCA cleaning of 300 mm Si(100) wafers
2	Creating trenches in the Si through a photolithography process followed by RIE of Si
3	Filling the trenches by SiO_2 deposited by HDPCVD to form shallow trench isolation layers
4	Planarization of the wafer surface by a chemical mechanical polishing (CMP) process
5	Creating n^+-Si active regions through photolithography followed by P ion implantation
6	Dicing the wafers into 1.5 cm x 1.5 cm chips
7	Subsequent cleaning of the chips in acetone, IPA and DI-water
8	Photolithography process to define windows for Mo deposition
9	Removing the native oxide from the Si active areas by using a 1:7 BOE solution
10	Deposition of 5 nm Mo film by e-beam evaporation on the Si substrates
11	Lift-off process to remove excessive Mo outside of the active regions
12	Vapor-phase sulfurization of Mo to obtain ~15 nm MoS_2
13	Transferring single layer graphene on the samples
14	Patterning graphene through photolithography followed by RIE in O_2 plasma
15	Photolithography process to define windows for formation of metal contacts to graphene
16	Deposition of Cr/Au metal stack by e-beam evaporation followed by lift-off

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List of Publications

Publications

Journal publications within the scope of this thesis

5. **M. Belete**, S. Riazimehr, S. Kataria, G. Lippert, M. Lukosius, D. Schneider, A. Bablich, P. H. Bolívar, O. Engström, and M. C. Lemme, "Broadband Spectral Sensitivity in Si/MoS2/Graphene Hybrid Heterojunction Photodetectors", *to be submitted*, 2021.

4. **M. Belete**, S. Kataria, A. Turfanda, S. Vaziri, T. Wahlbrink, O. Engström, and M. C. Lemme, "Nonvolatile Resistive Switching in Nanocrystalline Molybdenum Disulfide with Ion-Based Plasticity", *Adv. Electron. Mater.*, 6(3), Jan. 2020.

3. **M. Belete**, O. Engström, S. Vaziri, G. Lippert, M. Lukosius, S. Kataria, and M. C. Lemme, "Electron Transport across Vertical Silicon/MoS2/Graphene Heterostructures: Towards Efficient Emitter Diodes for Graphene Base Hot Electron Transistors", *ACS Appl. Mater. Interfaces*, 12(8), Jan. 2020.

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