Growth and characterization of InAs nanowire-based Josephson junctions

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vorgelegt von

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Contents

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I do solemnely swear that:

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- **Pujitha Perla**, H. Aruni Fonseka, Patrick Zellekens, Russell Deacon, Yisong Han, Jonas Kölzer, Timm Mörstedt, Benjamin Bennemann, Abbas Espiari, Koji Ishibashi, Detlev Grützmacher, Ana M. Sanchez, Mihail Ion Lepsa, and Thomas Schäpers. *Fully in situ Nb/InAs-nanowire josephson junctions by selective-area growth and shadow evaporation*. Nanoscale Adv., 3:1413–1421, 2021.

- Patrick Zellekens, Russell Deacon, **Pujitha Perla**, H. Aruni Fonseka, Timm Mörstedt, Steven A. Hindmarsh, Benjamin Bennemann, Florian Lentz, Mihail I. Lepsa, Ana M. Sanchez, Detlev Grützmacher, Koji Ishibashi, and Thomas Schäpers. *Hard-Gap Spectroscopy in a Self-Defined Mesoscopic InAs/Al Nanowire Josephson Junction*. Phys. Rev. Applied 14, 054019, 2020.

- **Perla, Pujitha** and Faustmann, Anton and Koelling, Sebastian and Zellekens, Patrick and Deacon, Russell and Fonseka, H. Aruni and Kölzer, Jonas and Sato, Yuki and Sanchez, Ana M. and Moutanabbir, Oussama and Ishibashi, Koji and Grützmacher, Detlev and Lepsa, Mihail Ion and Schäpers, Thomas *Te-doped selective-area grown InAs nanowires for superconducting hybrid devices*. PhysRevMaterials., 6.024602, 2022.

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Abstract

This work delves into the growth mechanism as well as structural and electrical characterization of InAs nanowires (NWs) for Josephson junctions. The superconductors used in this case are aluminum and niobium. Josephson junctions are an essential component of a superconducting qubit. This work describes the evolution of the Josephson junctions within the state-of-the-art and achieving higher transparency of the semiconductor/superconductor interfaces. The first part of the work deals with the optimization of the selective area growth. This method offers greater control of the growth of nanowires and provides higher uniformity. Parameters such as temperature, indium growth rate, and arsenic beam equivalent pressure (BEP) have been optimized to achieve a growth yield of 95%, using a 20 nm thick silicon dioxide mask on a Si(111) substrate. Eventually, the InAs nanowires are grown and optimized for diameters of 70-80 nm and lengths of 4-5 μm. Additional experiments have been performed to dope the InAs nanowires with tellurium. In the case of Josephson junctions, they offer a huge asset, with a doping range of $1\times\ 10^{18}\,\mathrm{cm}^{-3}$ to $1\times\ 10^{19}\,\mathrm{cm}^{-3}$. An increase in the conductance of these nanowires is observed with increased doping and thereby an enhanced critical current of the Josephson junctions. Moreover, Te doping has shown an impact on the diameter and the length of the nanowires, since it is a surfactant. Atom probe tomography investigations performed on these nanowires show additional (211) lateral facets, that shift the hexagonal structure of the InAs nanowire to a partly dodecagon structure at Te doping concentrations greater than $1\times10^{19}\,\mathrm{cm}^{-3}$. Furthermore, the transparency of the InAs/superconductor interface has been tuned. A defect-free interface and a smooth film of a superconductor is a pre-requisite for a high-quality Josephson junction, since this ensures a good coupling between the materials. A complete in-situ method has been adopted, to grow Al and Nb, onto the nanowires, thereby eliminating, any possible exposure of the semiconductor surface to the ambient. To achieve defect-free semiconductor/superconductor interfaces, a brief degassing step is introduced to the nanowires before the growth of the superconducting metals such as aluminum or niobium. This process, ensured enhanced transparency between the materials, thereby strengthening the coupling, by that improving the proximity effect. To be brief, the proximity effect induces Cooper pairs into the semiconductor, i.e. it turns the NW partly into a superconductor. Furthermore, the growth parameters of the metals evaporated are optimized to produce a smooth and defect-free interface and are investigated systematically. Lastly, the in-situ approach is expanded to encompass the fabrication of Josephson junctions at ultra-high vacuum conditions and to include other superconducting and capping materials in the process. The substrates made for this purpose have been prepared in such a way that two nanowires grow in a square trench at 90° to the planes of the trench. The growth windows for the NW growth are meticulously and selectively placed in such a way that one NW shadows the other during the metal evaporation, thus, causing a junction on the latter wire. The superconductors used in this process are optimized to create smooth and defect-free layers. In the case of aluminum, the growth of the metals is found to depend more on the temperature than on the angle of deposition. In contrast, for Nb, the angle of evaporation has a huge effect on the smoothness of the film. The investigations presented in these sections include transmission electron microscopy and corresponding low-temperature electrical measurements. This shadow approach, increased the metal evaporation angles onto the nanowires, from 30° to 87°, thus causing smooth and defect-free layers. This has also been shown to increase the interface transparency, between the NW and the superconductors. Lastly, this platform has also been used to demonstrate the growth of complex NW networks and multiple Josephson junctions.

Zusammenfassung

Josephson-Übergänge sind ein wesentlicher Bestandteil von supraleitenden Qubits. Diese Arbeit beschreibt deren Weiterentwicklung auf Basis von selektivem Wachstum von Halbleiternanodrähten und in-situ Prozessierung. Die hierfür hergestellten InAs-Nanodrähte wurden zunächst strukturell und elektrisch charakterisiert. In den entsprechenden Josephson-Übergängen mit Aluminium und Niob Elektroden konnte nachfolgend eine höhere Transparenz der Halbleiter-Supraleiter-Grenzfläche festgestellt werden. Im ersten Teil beschäftigt sich diese Arbeit mit der Optimierung des selektiven Wachstums. Diese Methode bietet eine größere Kontrolle und ermöglicht somit eine höhere Gleichmäßigkeit des Wachstums der Nanodrähte. Parameter wie Temperatur, Indium-Depositionsrate und Arsendruck wurden optimiert, so dass am Ende eine Ausbeute von 95% erreicht wurde, wobei eine 20 nm dicke Siliziumdioxidmaske auf einem Si(111)-Substrat verwendet wurde. Das optimale Ergebnis wird bei InAs-Nanodrähte mit Durchmesser von 70-80 nm und Längen von 4-5 μm erreicht. Zusätzlich wurden die InAs-Nanodrähte mit Tellur dotiert. Im Falle von Josephson-Übergängen bietet eine Dotierung im Bereich von $1 \times 10^{18}\,\mathrm{cm}^{-3}$ bis $1 \times 10^{19}\,\mathrm{cm}^{-3}$ den großen Vorteil, dass eine Erhöhung der Leitfähigkeit der Nanodrähte und damit des kritischen Stroms der Josephson-Übergänge beobachtet wird. Gleichzeitig hat die Te-Dotierung einen Einfluss auf den Durchmesser und die Länge der Nanodrähte handelt, da es sich um einen oberflächenaktiven Stoff. Atomsondentomographieuntersuchungen zeigen zusätzliche laterale Facetten (211), welche die hexagonale Struktur des InAs-Nanodrahtes bei Dotierungskonzentrationen größer als $1 \times 10^{19}\,\mathrm{cm}^{-3}$ zu einer teilweise dodekagonalen Struktur verändern. Weiterhin konnte die Transparenz der InAs/Supraleiter-Grenzfläche erhöht werden. Eine defektfreie Grenzfläche und eine glatte Schicht des Supraleiters ist eine Voraussetzung für einen hochwertigen Josephson-Übergang, da dies eine gute Kopplung zwischen den Materialien gewährleistet. Hierzu wurde eine vollständige in-situ-Methode angewandt, um Al und Nb auf die Nanodrähte zu deponieren, wodurch eine Kontamination der Halbleiteroberfläche durch Luft vermieden wird. Die gezüchteten Nanodrähte werden hierzu vor der Deposition der supraleitenden Metalle Aluminium oder Niob kurz entgast. Eine Optimierung durch systematische Untersuchungen der Depositionsparameter für die Metalle führt zu einer glatten und defektfreien InAs/Supraleiter-Grenzfläche mit erhöhter Transparenz. Dies ermöglicht die Beobachtung des Proximity-Effekts, bei dem Cooper-Paare in den Halbleiter induziert werden, d.h. der Nanodraht wird teilweise zu einem Supraleiter. Final wird der in-situ-Ansatz für die Herstellung von Josephson-Übergängen bei Ultrahochvakuum-Bedingungen durch die Deposition einer Schutzschicht gegen Oxidation ergänzt. Die zu diesem Zweck hergestellten Substrate werden so präpariert, dass zwei Nanodrähte in einem quadratischen Graben im Winkel von 90° zur Oberfläche des Grabens orientiert sind. Die Nanodrähte werden selektiv so platziert, dass ein Nanodraht den anderen während der Metallverdampfung beschattet und so ein Josephson-Übergang auf dem letzteren Draht entsteht. Im Falle von Aluminium wird festgestellt, dass das Wachstum der Metalle mehr von der Temperatur als vom Abscheidungswinkel abhängt. Im Gegensatz dazu hat bei Nb der Verdampfungswinkel einen großen Einfluss auf die Glattheit der Schicht. Die an diesen Übergängen durchgeführten Untersuchungen umfassen Transmissionselektronenmikroskopie- und entsprechende Quantentransportmessungen. Eine Erhöhung des Depositionswinkels des Metalls auf die Nanodrähte von 30° auf 87°, resultiert in einer glatten und defektfreien Schicht, deren Transparenz zwischen dem Nanodraht und den, Supraleiter erhöht ist. Am Ende wurde diese Technologie verwendet, um das Wachstum von komplexen Nanodraht-Netzwerken und mehrfachen Josephson-Kontakten zu demonstrieren.

1 Introduction

If there´s anything radical that could revolutionize the world, that nonetheless is a quantum computer. It could transform various fields, the quantum impact possibilities are limitless [1].Quantum computation is one of the trending topics in the research community and many top companies [2–5]. These companies are using semiconductors, superconducting qubits, etc to make qubits. Quantum computers, use quantum physics to interpret and compute. They can exceedingly outperform supercomputers at certain tasks [6]. Widely known classical computers encode information in the form of 'bits' that are 0s or 1s. Whereas, a quantum computer uses qubits also known as quantum bits. A quantum computer uses two states likewise its classical counterpart. These two states are rather called as energy states and not as in a ´on´ and ´off´ configuration. In contrast to classical computers, additionally a quantum computer can also be in the superposition of states i.e. energy levels.
The current major drawbacks of a quantum computer are noise and decoherence [7], also scalability w.r.t to qubits. Decoherence can be caused by light, vibrations, or by the inevitable act of measuring a qubit. Decoherence causes the instability in a qubit´s position, thus disturbing a qubit´s state of superposition or entanglement. There is a high need for a robust system. An example of such a robust qubit is a superconducting qubit , which is a collective excitation in a superconducting circuit. These superconducting qubits are popular approaches for large-scale quantum computation, since they are highly controllable and sensitive to charge noises [8]. One such qubit is a transmon qubit i.e. superconducting charge qubit, which is specifically designed to have a reduced sensitivity to charge noise [9–11]. A transmon qubit, that can be controlled by a gate is called a gatemon, where in the Josephson junction is controlled by a gate, as seen in Fig. 1. III-V semiconductor nanowires (NW) combined with superconducting

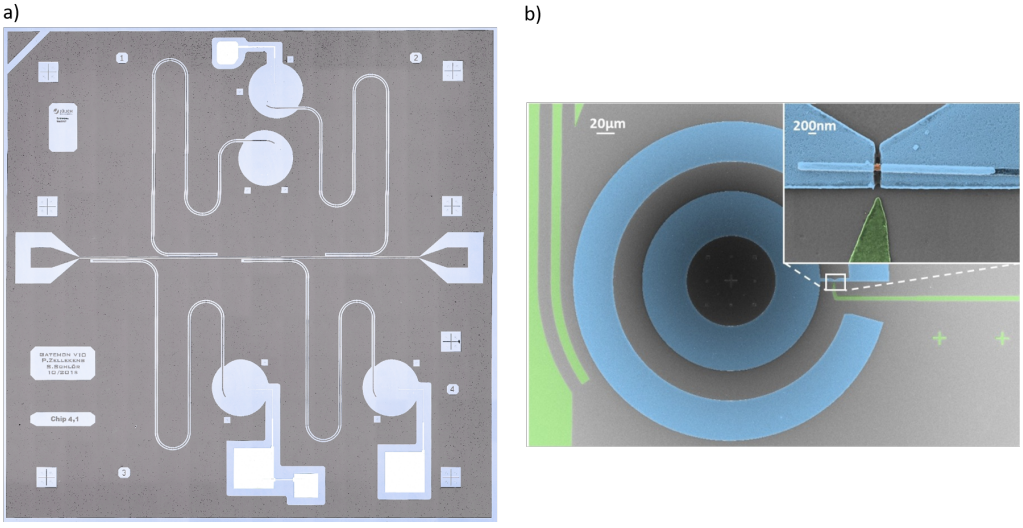

Figure 1: a) A transmon qubit circuit with resonators, gates and feed lines. b) closeup of the resonator (from the transmon qubit circuit) with a Josephson junction on semiconductor nanowire in the inset (designed at RIKEN).

electrodes have proven to serve as versatile building blocks of Josephson junctions [12]. These Josephson junctions are formed by two separated superconducting electrodes that are connected by a NW segment. This NW segment, is the semiconductor part that can be tuned via

a gate electrode to control the critical current of the junction. Furthermore, due to the large Fermi wavelength of the electrons (that are present in the semiconductor part), and limited diameter of the NW, a finite number of discreet Andreev bound states are formed in this Josephson junction. The Josephson current is mainly carried by these bound states. There are coherent transitions present in these states that can be used for qubit operations [13–15]. These SNS (superconductor-semiconductor-superconductor) junctions have also found their place in the topological qubit regime that are based on Majorana fermions [16–20].
InAs and InSb nanowires are well suited candidates to form a Josephson junctions, because of their high transparency towards the deposited superconducting electrodes, which is one of the prerequisites to obtain a sufficiently large supercurrent [21, 22]. A commonly used material is aluminium, since it possesses a small superconductive gap and critical magnetic field, but has a large superconducting coherence length [18, 22, 23]. In particular, when a larger operation temperature is required or the junctions have to be operated at a higher magnetic field, other superconductors such as Nb and its alloys [24–26], Pb [27, 28], or V [29, 30], are the materials of choice. It was already established that a semiconductor NW can be covered in-situ by a superconducting layer [26, 30–32]. SC/SM (superconductor/semiconductor) hybrids in this regard, have always been fascinating and the research has greatly paced to realize these Josephson junctions in-situ at ultra-high vacuum (UHV), without any exposure to chemicals or ambient surroundings. Normally to form a Josephson junction with a small gap between the in-situ deposited superconducting electrodes, wet-chemical etching is employed. However, there have been several reports to achieve short Josephson junctions, by adopting different shadow evaporation techniques, i.e. either by using a NW to cross another as shadow masks [33, 34] or by using a patterned, suspended SiO_2 layer as a stencil mask [26, 30]. In this thesis, different approaches to realize a Josephson junctions using molecular beam epitaxy (MBE) technique are presented, which have proven to be highly promising elements for superconducting qubits.

1.1 Scope Of This Work

This thesis involves in optimization of bottom-up growth of NWs using an MBE technique, and implementation of the MBE technique to produce highly transparent superconducting contacts onto semiconductors. The entire work benefited from the state-of-the-art Nanocluster at Helmholtz Nano Facility (HNF), combining several deposition chambers maintained at UHV conditions. The outline of this thesis is as follows:

- **Chapter 1** This chapter gives brief insights into the essential theory of growth, metal shell growth and physics behind fusing a semiconductor and a superconductor.
- **Chapter 2** This chapter explains about the characterization tools that have been used throughout the thesis.
- **Chapter 3** This chapter describes the different fabrication steps of the samples, that have been used in this thesis.
- **Chapter 4** The optimized results of the substrate fabrication methods are presented in this chapter.
- **Chapter 5** This chapter illustrates the results of the growth and characterization of undoped InAs and Te doped InAs nanowires.

- **Chapter 6** The results of the growth and characterization of InAs/Al half-shell nanowires with ex-situ etched junction is presented in this chapter.
- **Chapter 7** This chapter presents the most novel approach to achieve a Josephson junction device in-situ, with the supporting transmission electron microscopy and low temperature electrical measurements.
- **Chapter 8** The summary and the outlook has been presented in this section.

2 Theory

In this chapter, general theory related to the growth of layers is explained in the thin films section. Gathering the basic understanding from this, the nanowire growth is explained. Furthermore, the growth of superconducting metal shells on the nanowires using MBE at UHV conditions is discussed. Finally, to understand the importance of the semiconductor/superconductor interfaces, the basic transport mechanisms are presented via superconductivity, Josephson effect, and superconductor-normal conductor-superconductor (SNS) junctions.

2.1 Growth Of Thin Films

Josephson junctions with the semiconductor nanowires form a crucial part of a superconducting qubit circuit. These nanowires have to be crystalline. This increases the transparency of the semiconductors and the superconductors, by allowing sufficient current through the semiconductor. Although the growth of nanowires is different than a layer growth, the experimental realization of the different growth modes, helps one understand the mechanism of layer growth which is quite comparable to that of the metal growth of superconductors. The growth of crystalline materials involves a variety of parameters, such as substrate temperature, fluxes of the materials, III-V ratio, etc., that need to be optimized. Some of them include growth direction, composition, disorders, etc. To obtain a high crystalline quality of the materials, MBE growth technique is adopted. Furthermore, to understand the basic mechanism of crystalline growth, a basic understanding of the growth modes is necessary. When a layer is grown onto a desired substrate, it can adopt three different growth modes i.e. Frank-van der Merwe (FM), Volmer-Weber (VW), and Stranski-Krastanov (SK) modes. These modes are schematically shown in Fig. 2. The distinguishing factor amidst the modes, depends on parameters namely, lattice mismatch between the materials, the adatom diffusion length, the adhesion energy, the flux J and the substrate temperature. In Volmer–Weber (VW) growth, the adatom-adatom interaction dominates, this leads to the formation of the islands. As more adatoms reach the substrate, they coagulate on the previous islands and coarsen. This causes rough multi-layers on the substrate. This usually occurs when the lattice mismatch is moderate, and the critical thickness, h_c, value is lower than a monolayer, thus favours island growth. In the Frank–van der Merwe (FM) growth regime, the interaction between the adatoms and the surface dominates, thus leads to a layer-by-layer growth [35]. The film formed here is smooth and complete. This indicates that a new layer forms after a complete layer is formed below it. Hence, occurs when the lattice mismatch between the grown layer and the substrate is small. Here, the layer thickness is below h_c, thus the strain could be relaxed elastically [36]. Stranski–Krastanov growth regime is an intermediate process that consists of both islands and layers. This occurs in the case of highly mismatched systems. The transition of the layer growth to the island growth depends on the key parameter called critical layer thickness h_c. This is the thickness of a wetting layer, where it starts to form an island. This critical thickness parameter depends on the surface energies and the lattice misfit parameters of the substrate and the film. Additionally, strain energy increases as the wetting layer thickens, and this could lead to misfit dislocations [37]. The misfit between the layers, can be expressed in terms of the lattice constant of the substrate a_s and the lattice constant of the desired material to be

grown a_f, as shown in the equation below:

$$\frac{\delta a}{a} = \frac{a_f - a_s}{a_s}. \tag{2.1}$$

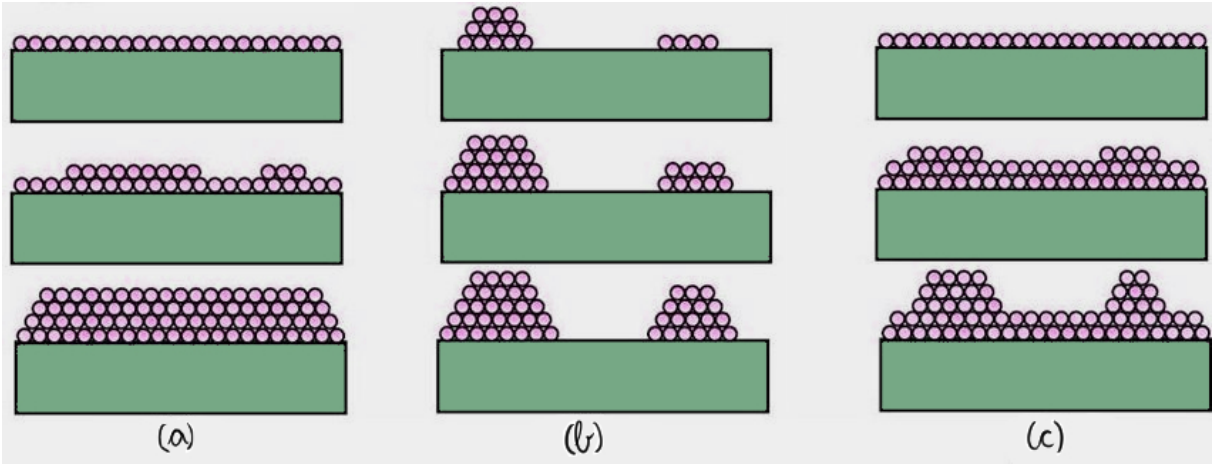

Figure 2: Growth modes of thin films (a) Frank-van der Merwe (b) Volmer-Weber, and (c) Stranski-Krastanov. Image adapted from [38].

This gives a good understanding of different growth regimes and the mechanism behind layer growth. It is also comparable to metal film growth which will be further discussed in the superconductors section. Besides this, nanowire growth is quite different to layer growth, since nanowires have a large surface to diameter ratio.

2.1.1 Nanowires

Nanowires in general have a very high aspect ratio. When they are manipulated via field effect from a gate electrode, the conduction channels can be controlled. This is a desirable quality for fast switching applications. Nanowires are considered to host one-dimensional states due to quantum confinement, which reflects in the efficient charge transport and interesting quantum effects. They can be grown via top-down or bottom-up methods. The first growth of 1D structures by self-assembly in 1964 has been reported by Wagner and Ellis [39], where they used liquid gold droplets on Si substrate to grow Si nanowires. Here, the gold droplets are employed as a catalyst, and the nanowires eventually grew when the droplets are supersaturated and supplied with gaseous Si. Thus, the supersaturation led to the growth of the nanowires between the substrate and the gold droplet. This process was known as vapor-liquid-solid (VLS) growth mechanism. This process has been expanded and restored in early 90´s by Hiruma *et al.* [40, 41] for the growth of III-V nanowires such as GaAs and InAs. These works highlighted the metalorganic vapor phase epitaxy (MOVPE) methods of growth. Henceforth, several other growth methods have come into light, namely, chemical beam epitaxy (CBE), and MBE. Different materials from the groups (IV, III-V, II-VI) have been adopted to grow nanowires using these growth techniques. Apart from gold, also Ag [42], Cu [43], Mo/Au [44] have been utilized as catalysts to grow nanowires.
A typical VLS growth process is schematically illustrated in Fig. 3. Metal nanoparticles are used as a catalyst to grow nanowires. During the growth process, the catalyst is heated above

its eutectic temperature. This creates a liquid metal–semiconductor alloy [45]. When a desired vapour source (NW material) is provided, the eutectic alloy continues to incorporate the semiconductor material via supersaturation, through the vapor/liquid interface. This causes nucleation as more and more of the vapour arrives. Thus, the semiconductor material precipitates and creates a solid/liquid interface (growth interface). Eventually, nanowire growth is achieved. This is followed by solid addition (formation of NW) at the growth interface, thus VLS mechanism. In this process, the metal catalyst, precipitates and a nanowire, thus is formed between the droplet and the substrate. Hence, the metal droplet stays on the tip of the nanowire as the nanowire elongates [45].

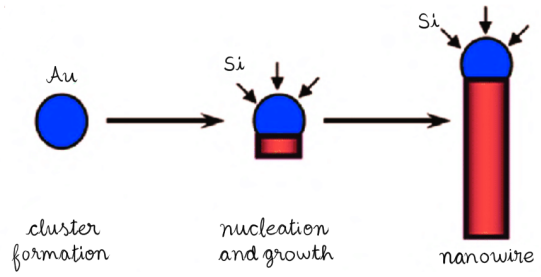

Figure 3: Schematic of VLS growth of silicon nanowires. Gold is used as a metal catalyst, a liquid alloy droplet of AuSi (orange) is initially formed when heated above 363°C. Continuous supply of vapour materials results in nucleation. Thus, the nanowire (green) grows uniaxially. Image adapted from [45].

Contradictingly, using an external catalyst such as gold, often influences the opto-electronic properties of the nanowires. Gold is widely known to diffuse into materials and can be quite detrimental for CMOS fabrication platforms. It causes deep level traps and causes diffusion, and in turn degrades and effects the efficiency of the electronic devices [46, 47]. Hence, alternative methods have been investigated. One such method is a self-catalyst method to grow III-V nanowires using group III element as a catalyst. Here, the axial growth of the nanowire proceeds with saturation of the droplet of group III element with group V. This method is popularly used to grow GaAs nanowires [48]. Here, the nanowires are grown selectively, and the group III droplets are made to form on the holes patterned on Si substrates covered with SiO_2, as a mask. The nanowires grown on these substrates are distributed uniformly on the substrate. The nanowires tend to have different growth rates for the top and the side facets in this case. For the investigations performed in this thesis we have grown InAs nanowires using vapour solid (VS) growth mode. InAs is chosen since it is a widely known, III-V semiconductor and has a very high electron mobility $\approx 3.4\times10^4$ $cm^2V^{-1}s^{-1}$ at room temperature [49]. A VS growth mechanism is adopted since, in contrast to the VLS mechanism, a droplet is not involved during the nanowire growth. This makes it easy to incorporate dopants and growth of ternary structures. There have been only few reports that have demonstrated VS grown methods [50, 51]. Solid conclusions regarding the exact VS growth mechanism have not been made. Hence it is not clearly known if the initial phase of VS growth mode, is dominated by VLS mechanism and further by VS mechanism or by simultaneously saturation of both elements. In-situ growth studies of VS growth mechanism would shed light on this topic, which is lacking currently. Independent of different growth methods, a high occurrence

of stacking faults in these nanowires is observed that degrades the electronic transport and optical efficiency [52, 53].

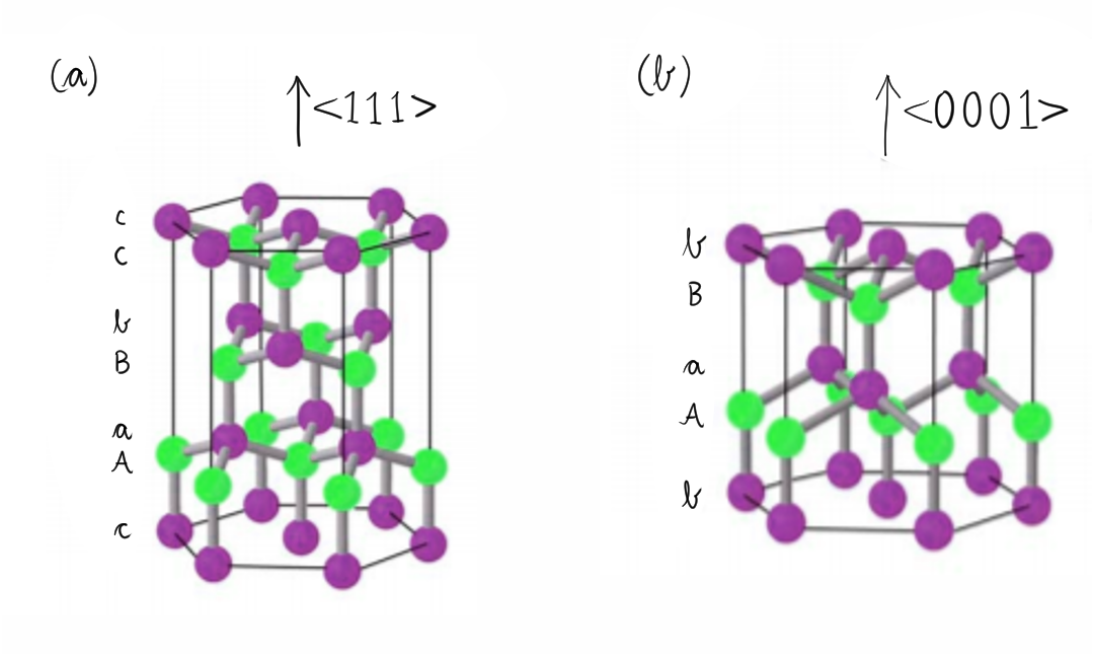

Figure 4: Atomic arrangement of Zinc Blende (ZB) (a) and Wurtzite (WZ) (b) structures along the [111] and [0001] nanowire growth directions. Image adapted from [54].

III-V nanowires crystallize in zinc blende (ZB) structure, and less commonly in the wurtzite (WZ) structures. The most regular structure of zinc blende is analogous to the crystal structure of diamond. It has two face centered cubic (FCC) sublattices that are translated by $[\frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}]\ a$, along the body diagonal. Each sublattice is occupied by one of the two, III-V elements. The position of [000] is occupied by group III atoms, where as group V atoms are seated at $[\frac{1}{4}\ \frac{1}{4}\ \frac{1}{4}]$. The characteristic stacking sequence is represented as a blue and yellow stick figures is seen in Fig. 4. Zinc blende structure forms a stacking of monoatomic layers in the sequence of cAaBbCcA, where as wurtzite shows a stacking of bAaBbA. These two structures are closely related to each other, thus polytypism occurs in III-V nanowires where in small segments of zincblende appears in wurtzite structure. Here Aa plane is replaced with Cc plane or vice versa [54]. It still remains a challenge to control the crystal phase of InAs nanowires in both cases. From the Ph.D studies of T. Rieger [55] and Dimakis *et al.* [50], it was reported that, initially an In droplet forms leading to a VLS growth, which is later consumed, during the growth and the nanowires progresses with VS growth [56].

2.2 Growth Of Superconductive Thin Films

The Josephson junctions prepared for this thesis are based on InAs nanowires/superconductor. The nanowires for this purpose, are initially degassed and a thin superconducting metal shell is evaporated onto these preferably at UHV conditions. In the previous section, the nanowire growth mechanism is already elucidated. This section entirely is based on the growth kinetics of the superconductor metal shell. The superconductor metal film should cover the nanowire conformally. Keeping this concept in mind, evaporation of Al and Nb metals have been performed onto the InAs nanowires that are grown on Si (111) substrates, at UHV conditions. The Al and the Nb shells evaporated here, are half shells that are formed, when the substrate is not rotated during the process. In 2015 a growth model was developed by Peter Krogstrup, that explains the kinetics and the growth of the thin Al films, Suppl. [31]. One of the essential components of a superconducting metal shell is the adatom diffusion length λ_a. This is the mean distance of the adatom, when it lands on the surface and moves along and gets incorporated into the growth of the film. When this movement is assumed as a random walk and the adatom incorporation barrier is considered neglected, from Krogstrup *et al.* [31] the average diffusion length can be defined as:

$$\lambda_a(\rho_a, T_s) \propto \frac{1}{\sqrt{\rho_a}}.\exp - \left(\frac{\delta h_{aa} - \delta\mu_M}{2k_B T_s}\right), \tag{2.2}$$

where, ρ_a is the adatom concentration, $\delta\mu_M$ is the chemical potential of the incorporation site, δh_{aa} is the transition state enthalphy barrier between two nearest adatom sites, k_B is the Boltzmann constant and finally the substrate temperature is T_s. It is also know that, when the flux J increases, the adatom concentration ρ_a on the substrate also increases, that gives rise to

$$J \propto \rho_a. \tag{2.3}$$

Considering Eq.(2.2) and Eq.(2.3), it can be deduced that the adatom length decreases, as the flux J increases and the substrate temperature T_s decreases. When the diffusion length λ_a is small, it results in a small and grainy metal films. Since Al has a FCC i.e. face-centered cubic structure, the adatoms merge into grains and crystallize in [111] crystal direction, which is out-of-plane [57]. The [111] crystal direction, is a quite preferential orientation for grains with lowest surface energy, since it reduces the total energy. This growth regime, where the total surface energy is minimized is called surface driven growth. Considering an in-plane orientation, this occurs to minimize the interface energy as seen, in Fig. 5 (a). This appears until a certain critical thickness and can also vary with different metals.
When the substrate temperature T_S increases the diffusion length of the adatom increases, the grains become spacey and clump together to form bigger clusters, as seen in Fig. 5 (b). When the critical thickness of the grains increase, the growth is dominated by by strain fields and grain boundaries, rather than surface energy minimization, as shown in Figs. 5 (c) and (d). This causes grains with different crystal orientations and the metal film formed here is grainy rather than smooth. It is a prerequisite, to consider the lattice mismatch for the metal that are to be evaporated, so as to reduce the disorders at the interface. In case of a large mismatch of the semiconductor and the superconductor metal, interfacial domains form to decrease the stress caused due to lattice mismatch [58]. For thinner layers, it is known that,

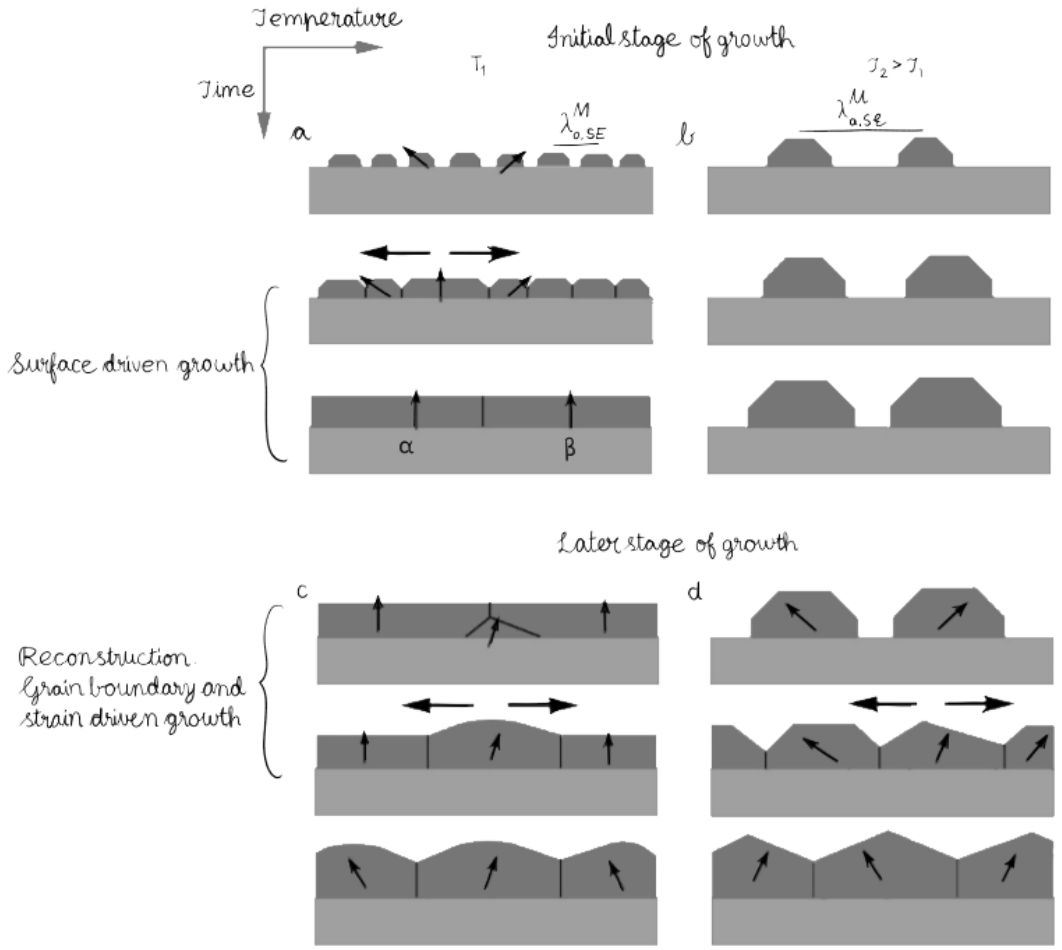

Figure 5: Initial stages of metal shell (blue) growth on InAs surface at high (T_2) and low temperature (T_1) is illustrated. (a) Shows a case of T_1, where small grains form due to low adatom diffusion, then they later merge into a thin film. If the thin film is below a critical thickness, the grains with the lowest surface energy dominate (arrows). (b) Shows a scenario of higher temperature where in the adatom diffusion is higher, that results in larger grains, that are spaced further apart than in scenario (a) (c) and, (d) Represent the cases in which the critical thickness is exceeded. In both temperature regimes, they result in new crystal orientations, w.r.t to the grain boundaries and strain disorder, since these contribute more, when the layers are sufficiently thick, image adapted from (Suppl. [31]).

surface energy minimization dominates. Since the surface-to-volume ratio for thinner layers is high. Aluminium forms a complete and conformal layer and the grains are oriented out-of-plane along the [111] direction as depicted in Fig. 5 (a). For thicker layers, $[11\bar{2}]$ is the preferred orientation, since it is driven by strain reduction [31]. This is attained by reconstruction or relaxation into less mismatched grains, i.e. from [111] to $[11\bar{2}]$, as illustrated in Figs. 5 (c) - (d).

2.3 Superconductivity

This section deals with the evaporated metals such as Al/Nb and their behaviour at ultra low temperatures, where they exhibit superconductivity. Furthermore, this concept is extended to understand Josephson junctions that are designed using semiconductors (InAs nanowires) and superconductors (Al/Nb). In such Josephson junctions, the semiconductor induce superconductivity from the metals at low temperatures. To explain this whole phenomenon of Josephson junctions, it is essential to initially understand, the basics of superconductivity.
Superconductivity was first discovered by Kammerlingh Onnes [59] in 1908 in Leiden, when they dipped Mercury into liquefied helium at 4.2 K. The electrical resistance of mercury drastically dropped and vanished at this temperature, the corresponding phenomenon was named superconductivity. This has gathered a huge attraction and since then various fields in physics and technology have been revolutionized. This further has lead to discovery of many superconducting materials [60]. Another crucial effect that also has been observed in conjunction to the electrical resistance drop in a superconductor is that, when a magnetic field is passed through this superconductor at lower temperatures, it generates its own screening field, that expels the magnetic field, this was coined as diamagnetism. Superconductors are perfect diamagnets at lower temperatures. Although the experiments have been laid down, the theory behind the superconductivity has been formulated much later than the discovery of the superconductivity itself. It has fascinated a pool of scientists and it took several years until BCS theory explained it using many-body physics. It was John Bardeen, Leon Cooper, and John Robert Schrieffer, who modelled it, hence the name [61]. The theory demonstrates that superconductivity is a quantum mechanical state of matter that exhibits zero resistance and perfect diamagnetism. This state is caused due to the electron-electron attraction at very low temperatures. This attraction is mediated via a phonon exchange, thus causing electron-phonon interaction. Hence, Cooper pairs propagate through the material, causing no dissipation, thus electrical resistance drops towards zero. A Cooper pair is a state of two electrons that are weakly bound and can be defined using a wave function. These bound states occupy the same energy state and condensate to form a Bose-Einstein condensate. The two electrons in such a condensate have opposite momenta and form a spin singlet, hence their centre of mass is stable. This superconducting state can be disturbed via several thermodynamic parameters, such as temperature, field, and current. These thermodynamic properties can influence the macroscopic behaviour of the superconductor. Thus, the superconducting state is vanished when there is an increase in temperature, magnetic field, or current [62–64] above a critical value. As mentioned above, since the electrons form a condensate, this many-body interaction can be defined by a macroscopic phase coherent state, that is stated in the equation below:

$$\Psi = \sqrt{n_s} e^{i\phi}. \tag{2.4}$$

Since all Cooper pairs are in the same quantum mechanical state, this equation describes the state of an entire macroscopic superconductor. Here, ϕ is a single phase and $\sqrt{n_s}$ is the single amplitude. Considering the BCS theory, it explains that an electron moving through the crystal lattice, in a state k_1 interacts with the other lattice ions in its proximity through Coulomb interaction and acquires a new energy state, lower than its previous state i.e. k_1 - δk, releasing a phonon. The Cooper pair has the momentum $\hbar k$. Consequently, the released phonon is potentially absorbed by a different electron in the lattice, that is at state k_2, which excites its energy state to $k_2 + \delta k$. While lapped region of the two Fermi spheres, can be seen in Fig. 6, it results in a formation of a Cooper pair. The first electron in the state k_1, attract the near by lattice ions, causes a positive fluctuation in the charge density causing it to

attract the second electron. This interaction via the phonon is the implied electron-electron interaction, which is also depicted in the above Fig. 6. Electrons could pair up using the phonon interaction over larger distances to form Cooper pairs. They do not necessarily, pair up with a nearby electron. Rather, the electron-electron interaction could extend over almost several hundred nanometers, in the range of the coherence lengths [61, 65–67].

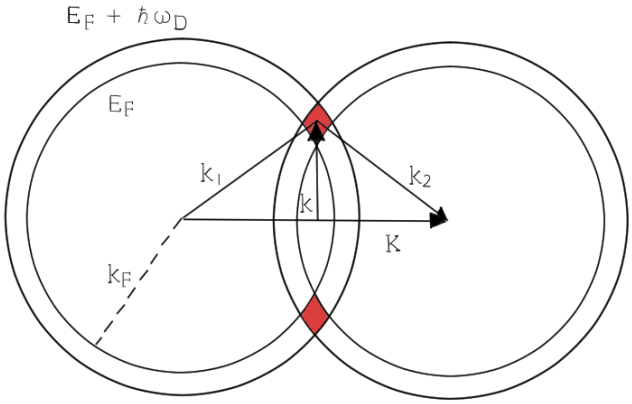

Figure 6: Overlapping Fermi spheres for two interacting electrons in the formation of a Cooper pair. $\vec{k}$ points in the overlapped (shaded area). Image adapted from [68].

The superconductor consists of a BCS ground state where Cooper pairs are occupied, and below this is the Bogoliubov quasi-particle state. This gap Δ_0 is created to protect the BCS ground state. Even though the electron electron interaction is considered to be weak, the energy needed to break up a Cooper pair is twice the energy difference between quasi-particle state energy E and BCS ground state Δ_0. This excited state is known as Bogoliubov quasi-particle state, that is a result of an elementary excitation above a superconducting state, and can be seen in Fig. 7. The Bogoliubov quasi particle is a superposition of an electron and a hole, with opposite spin and momenta.

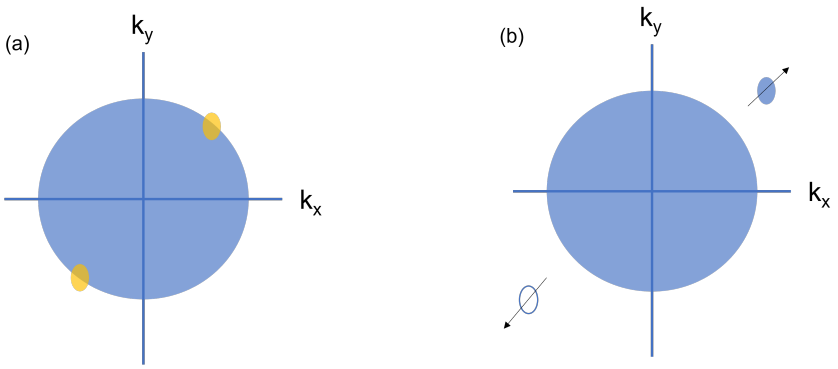

Figure 7: (a) Electrons (yellow) in a Fermi sphere, have opposite momenta and spin describe a Cooper pair in a superconducting state. (b) An elementary excitation above the Fermi sphere, results in quasi-particle that is a superposition of a hole and an electron. They have opposite spin and momenta and are called Bogoliubov quasi-particles (blue and white).

The quasiparticle energy E is determined using the Bogoliubov-de Gennes eigenvalue equation:

$$\begin{bmatrix} H(r) & \Delta_r \\ \Delta^*(r) & -H(r) \end{bmatrix} \begin{bmatrix} u_k(r) \\ v_k(r) \end{bmatrix} = E \begin{bmatrix} u_k(r) \\ v_k(r) \end{bmatrix}. \tag{2.5}$$

Here, $\Delta(r)$ is the coupling energy, while u_k and v_k are electron- or hole-like quasiparticles, $H(r)$ is the Hamilton operator for a single particle. This can also be expressed as

$$H(r) = \frac{-\hbar^2}{2}\frac{1}{m^*} \bigtriangledown^2 + V(r) - \mu, \tag{2.6}$$

where μ is the chemical potential and $V(r)$ is a scalar potential [69]. In case of metals, m^* can be equated to m_e. Thus the eigenvalue E of the Bogoliubov-de Gennes equation is

$$E = \pm\sqrt{\left(\frac{\hbar^2 k^2}{2m_e} - \mu\right)^2 + \triangle_0^* \triangle_0}. \tag{2.7}$$

This equation represents that there exists a gap between excited state and the ground state and this gap of a superconductor does not host any single-particles. As for the energy required to break the Cooper pair, once has to surpass the superconducting gap.

2.4 Josephson Effect

The devices fabricated for this thesis are made of of Al/Nb superconductors separated by few tens of nm of InAs nanowire. This constitutes a Josephson junction, i.e. superconductor-normal conductor-superconductor (SNS) junction. To understand the Josephson effect the concepts are briefly summarized below.
The phenomenon of flow of Josephson current between two distinct and disconnected pieces of superconductors is called the Josephson effect, was discovered by Brian D. Josephson in 1962 [70]. This is a phase-coherent process, that has been formulated for the SIS (superconductor-insulator-superconductor) junction, wherein the weak-link is a thin insulating barrier. The Cooper pairs tunnel through the barrier from one superconducting segment to the other. However, the weak-link chosen in our case is the semiconductor nanowire and thus the Josephson junction in our case, could be approximated to a superconductor-normal conductor-superconductor device, also known as the SNS Josephson junction device.
When a DC current is applied to this SNS device, Cooper pairs travel through the weak-link from one side to another through proximity effect. The superconductor wave function, on either sides decays into the weak-link.
Considering the Cooper pair wave functions

$$\Psi_1 = \sqrt{\rho_1}e^{i\phi_1} \text{ and } \Psi_2 = \sqrt{\rho_2}e^{i\phi_2}, \tag{2.8}$$

where, ρ_1 and ρ_2 are the Cooper pair densities on either side of the junction and the ϕ_1 and ϕ_2 are the corresponding phases. The electrons in a Cooper pair have to have the similar center of mass. This can be satisfied by making the Cooper pairs phase-coherent all along the superconductor. Hence, ϕ_1 and ϕ_2 represent the Cooper pairs in the superconductor section and simultaneously Ψ_1 and Ψ_2 can be substituted in the Schrödinger equation, that results in two Josephson equations. The Josephson current is related to the difference in the phase between the left and the right parts of the weak-link

$$\phi = \phi_1 - \phi_2, \tag{2.9}$$

and the first Josephson equation for the current is

$$I(\phi) = I_c \sin(\phi), \tag{2.10}$$

$I(\phi)$ maxes out at critical current I_c, and additionally the phase difference ϕ can be varied according to the current I flowing through the junction. This means that an increase in I results in the increase of the phase ϕ and a corresponding decrease of the coupling energy E_c

$$E_c(\phi) = -\frac{\hbar}{2e} I_c \cos(\phi). \tag{2.11}$$

The systems behaves as a single superconductor in the presence of an infinitely thin barrier, which phases out ϕ_1 and ϕ_1 [67]. The coupled Schrödinger equations with ansatz from 2.8, gives

$$V(t) = \frac{\hbar}{2e} \frac{\partial \phi}{\partial t}. \tag{2.12}$$

It is deduced that the Josephson voltage depends on the time-derivative of the phase difference (ϕ). These equations (2.10) and (2.12), characterize the Josephson effect.

2.4.1 Proximity Effect And Andreev Reflections

This section deals with the physics of fusing a superconductor to a normal conductor, that is a basis of an SNS Josephson junction. When a non-superconductor is bought in close proximity within a superconductor, Cooper pairs travel from the superconductor (S) into the normal conductor (N) known as proximity effect. The semiconductor then partly turns into a superconductor, this is known as induced superconductivity. This means that the wave function of a superconductor decays through the non-superconductor, and this decay depends on the coherence length of the non-superconductor. This proximity effect would be ideal if the interface between S and N has a high transparency. Thus, the interface between the InAs nanowire and superconductors (Al/Nb) has to be clean for the effective proximitization of the NS. Any impurity at the interface, decreases the coherence lengths and thus diminishes the effect. InAs nanowires in general are known readily be proximitized if there exists a transparent interface between S and N [22]. Thus there have been several attempts to improve the interface between the InAs nanowire and the superconductors (Al/Nb) in this thesis. As for the SNS Josephson junctions, the Josephson current is known to flow through the superconducting segments without any dissipation [62, 63, 69] at zero bias. It is assumed that the superconductor and the normal conductor have the same Fermi-energy and electron densities. Here, interaction between the bound Cooper pairs in the superconductors and free electrons in the normal conductors are explained. This is known as a reflection process at the boundaries of the materials (S and N) and was introduced by Alexander F. Andreev in 1962 [71]. The process was named after him and called the Andreev reflection. To make the process simpler, it is assumed that the electron gas in the normal conductor grazes with the superconductor without any additional barriers that could cause normal reflections at the interface at zero bias. The Andreev reflection process is depicted in Fig. 8.
When a conducting electron with energy $E_F < E_e < \triangle_0$, travels from a normal metal into a superconductor, as see in Fig. 8 (a), there happens to be no corresponding energy state within $\triangle_0$. Hence it needs to pair up to travel through the superconducting regime. Thus, it pairs with another electron from the Fermi sea of the normal conductor [69]. This results in a hole in the Fermi sea, that the paired-up electron created. Accordingly, to conserve the momentum this hole with the charge $+e$ is retro-reflected, as seen in Fig. 8(b), and travels back in the opposite direction of the incident electron, and into the normal conductor. This

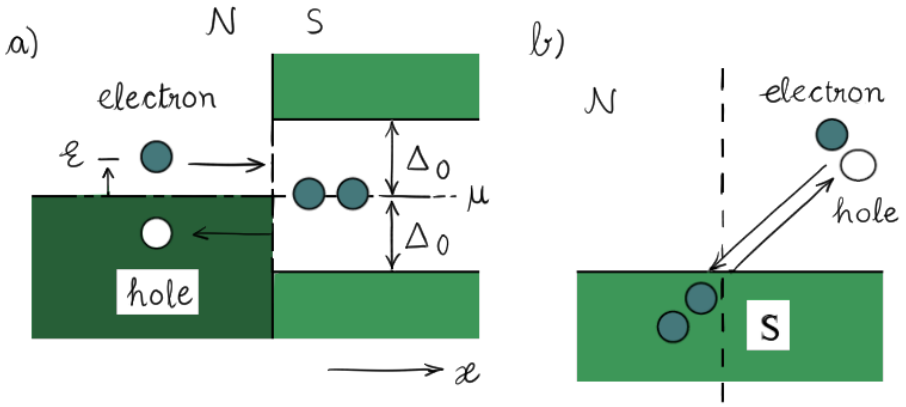

Figure 8: a) Energy diagram of the Andreev reflection process b) Scattering process in the real space. Image taken adapted from [69].

process could also occur in the reverse way, when the Cooper pair in the superconductor, drives through the normal conductor. The paired-up electrons redeem themselves in the channel of the normal conductor. One of the electron goes into the normal conductor channel and the other combines with a hole of the Fermi sea of the normal conductor.

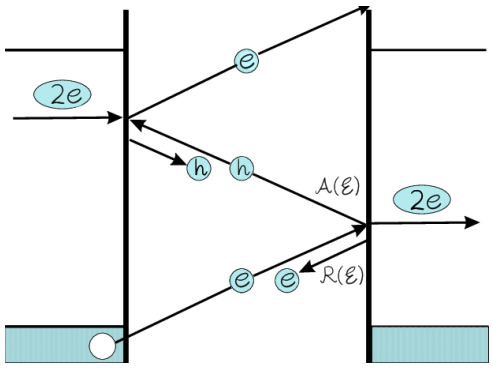

Figure 9: Multiple Andreev reflections, that are caused between two superconductors in a close proximity of a non-superconductor. A charge transfer of $-2e$ per cycle, can be observed. Image adapted from [72].

In case of a superconductor-normal conductor-superconductor (SNS) junction, Andreev reflections take place at both S/N interfaces. An incident Cooper pair from the superconducting region reaches the interface to a normal conductor and dismantles itself into two electrons, wherein one of the electron is absorbed by a hole. The other electron travels through the normal conductor and sees the second interface. Here it needs to pair up again to enter the superconducting region thus, it pairs up with an another electron and retro-reflects a hole. This hole is reflected back through the normal conductor and engages in the same process near the first interface. This process is known as multiple Andreev reflections and occurs with a bias. This causes a simultaneous electron and hole transfer through the normal conductor Fermi sea, can be seen in Fig. 9. Thus creates a charge of $-2e$ per cycle [69]. Each Andreev reflection process is a phase coherent process. Additionally, energy and momentum are also conserved in this process [69]. Hence, when an interface between S/N is quite transparent, multiple Andreev reflections are observed in the junction area and can be seen as subharmonic

peaks in a differential resistance graph, deduced from the low temperature electrical measurements. Hence, there were several approaches undertaken in this thesis to increase transparency between the InAs nanowires and Al/Nb superconductors, to observe these quantum effects.
'

3 Experimental And Characterization Techniques

In this chapter, the experimental tools for the nanowire (NW) crystal growth and the other characterization techniques are illustrated.

3.1 Growth Techniques

The sample growth by MBE, during the course of this thesis was performed at the Nanocluster at Helmholtz Nano Facility (HNF). This is one of the world-class, state-of-the-art clusters built by Scienta Omicron GmbH. It is a UHV tool combining 10 deposition chambers that are group III-As MBE, group III-As/Sb MBE, ALD, metal MBE, phase-change MBE, an oxide sputter chamber, a metal sputter chamber and a metal oxide MBE. This classic built grants a huge possibility to investigate a lot of material combinations within the UHV conditions. In this thesis, the MBE technique is adopted to grow NWs and then a metal layer, is evaporated by an electron beam (e-beam) maintaining ulta high vacuum (UHV) conditions.

3.1.1 Molecular Beam Epitaxy

Epitaxy is a process of growing crystalline materials on a crystalline substrate. The high purity of the source materials together with the UHV conditions results in a extremely good quality of the grown layers. With this technique, growth of atomic layers is possible at relatively low growth rates i.e. less than 1 μm/hr. This empowers a greater control on the crystal structures. To achieve a high quality of epitaxial layers, it can only be grown at pressures below $\approx 1 \times 10^{-9}$ Torr. To achieve these low pressure, the chamber is pumped using a cryo pump, an ion getter pump and additionally a cryo shield. The cryo shield acts as a pump and also as a thermal isolation between the effusion cells. Two MBE systems have been used, during the course of this thesis. The first one, MBE A, which is equipped with one As and one Sb cracker and additionally Ga, In and Al effusion cells. Furthermore, Si, C, and GaTe are the dopant cells. MBE A is used to grow InAs nanowires, where the planar growth rates are optimized on GaAs(100) substrates. MBE B is a metal MBE where the materials Al, Nb, Pt, Ti, and AlO_x are used for deposition. Both MBE A and MBE B are connected to each other via a large UHV transfer line. MBE A was used for the growth of the InAs NWs, where in the planar growth rates are tested on GaAs (100) substrates. This is then optimized to the nanowire growth rates. As and Sb fluxes are measured in beam equivalent pressures (BEP). Figure 10 shows an overview of a part of the Nanocluster. MBE Chamber (A), used for NW growth is coloured green. The round transfer chamber marked silver (D), contains a robotic arm, which distributes the samples to the different chambers. The actual transfer is depicted in blue (c). Here, a small train is used to transport the substrates to any desired chamber. Chamber MBE B (B) is coloured yellow, here the metal deposition takes place. The preparation chamber is used for degasing the samples is coloured in purple. The samples are transferred to the load-lock, and is coloured in red.
In chamber A MBE (schematic can be seen in Fig. 11), the effusion cells have a crucible containing the deposition material and is heated up via a filament until a desired pressure is reached. These crucibles contain group III elements and dopants. There are shutters, placed in front of these cells to open and close them. Cell temperature defines the amount of materials that comes onto the sample. Arsenic is supplied via a valved cracker source and the amount of

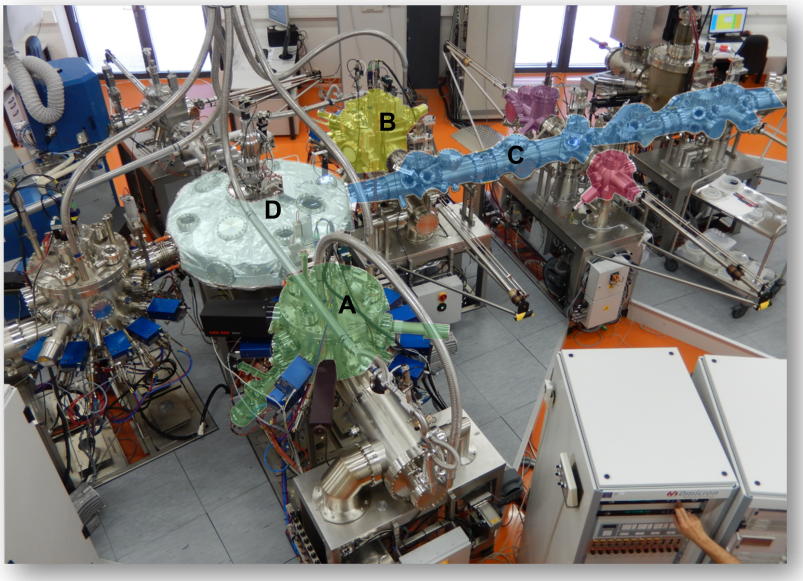

Figure 10: An overview of a part of the Nanocluster. Chamber MBE (A) in green, Chamber MBE B (B) in yellow, transfer line (C) in blue, round transfer chamber (D) in silver.

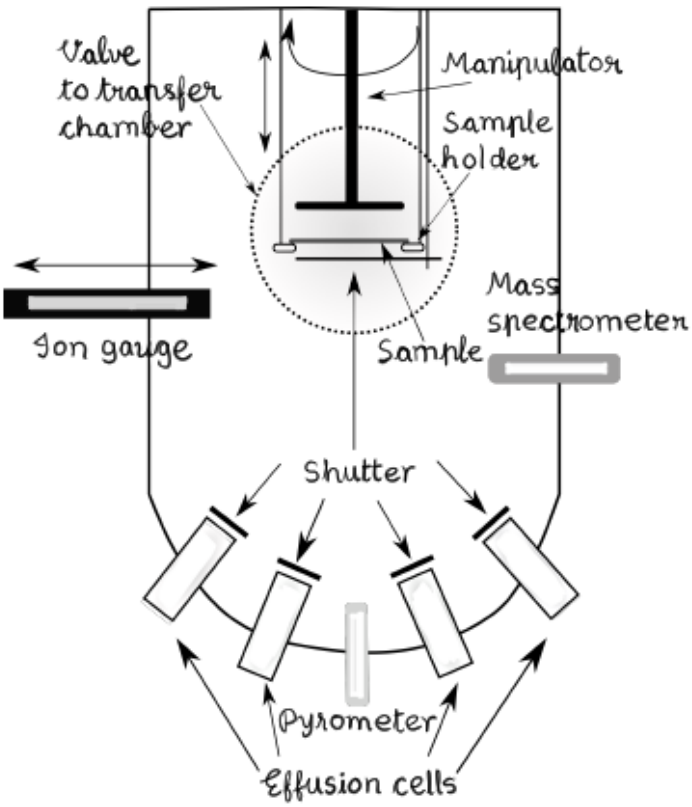

Figure 11: Schematic illustration of MBE chamber A. Image adapted from [73].

arsenic is controlled by the valve position and the reservoir temperature of the As cracker cell. The BEP (beam equivalent pressure) of As flux, is determined by the ion gauge. This whole

system is maintained at UHV (ultra high vacuum) conditions to obtain large mean free path of atoms. UHV is achieved by using a combination of cryo, ion getter pump and a cryopanel. The cryopanel condenses the residual gases, thus acts like a pump. For a III-V system growth, group III flux determines the growth rate, where as group V is just supplied in excess. The growth rate is further measured using RHEED (reflection high energy electron diffraction). In the MBE growth the interface abruptness is on an atomic level and the dopant inclusions can be controlled precisely, thus giving rise to high quality layers.
All metal depositions took place at chamber B, which is a metal MBE, as seen in Fig. 12. In the metal MBE chamber B, electron beam evaporators were used for deposition. Here, an electron beam hits a firm ingot of the evaporation substance which is placed in a crucible. This melts the ingot and leads to an evaporation of the material, can be seen in the schematic of Fig. 12. Thus, the flux J is controlled by the electron beam current and not by the temperature of the filament. The flux of the electron beam evaporators can be controlled via a residual gas analyzer feedback loop (RGA-loop). Here, a mass spectrometer detects the amount of evaporated material and uses this information to adjust the electron beam current to stabilize the targeted flux. The substrate is fastened by the substrate holder which also serves to heat and rotate the sample during growth. The desired materials are filled into the pockets and these are shifted to the gold position (see schematic Fig. 12) , so the angle of deposition w.r.t substrate normal, α i.e. 32.3 $^\circ$ always remains constant. Only one material at once can be evaporated, hence the desired material has to be shifted to the position of the gold pocket.

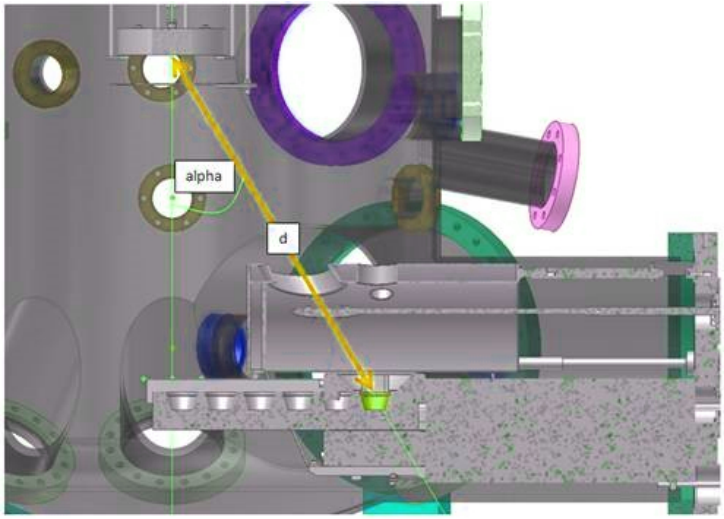

Figure 12: Schematic illustration of the metal MBE deposition system with pockets, gold pocket for the desired metal usage. Image provided Benjamin Bennemann.

3.2 Analysis Techniques

3.2.1 Scanning Electron Microscopy

In the field of NW research, the first and the foremost feedback technique used is the scanning electron microscopy (SEM). This is used to determine the yield, the aspect ratio and the surface morphology of the NWs. This work began with the optimization of substrate preparation for selective area epitaxy (SAE) of InAs NW arrays. A detailed study with the help scanning electron microscopy (SEM) was carried out to make this process reproducible. For this purpose a Zeiss 1550 VP Scanning Electron Microscope was used as an non-invasive analysis of the grown NWs and other structures. The SEM uses a focused beam of electrons to produce a high resolution image of the sample, allowing resolutions as small as 0.8 nm. The NW growth samples were imaged at a working distances less than 2 mm when viewing from the top, and when rotated at 30° with respect to the electron beam gun the working distances was always kept less than 6 mm. The samples for viewing the NWs are imaged with the accelerating voltages of 15-20 keV. Additionally, when the nanostructures have to be imaged with PMMA resist on them, the samples are sputtered with few nm of Iridium to prevent the resist burning due to the electron bombardment.

3.2.2 Micromanipulator

The in-situ Josephson junction samples were all transferred using a micromanipulator which is equipped in ZEISS Sigma 300 SEM. The Zeiss SEM is armed with a Kleindiek micromanipulator with 100 nm needles used for manipulation. This manipulator is a piezoelectric system that allows for XYZ motion for picking up nanowires and exactly placing them on gates etc. The manipulator tip is grounded to reduce the electrostatic effects which are caused by the charging effects of the SEM electron beam. The whole equipment is an exclusive tool which operates with a great precision and allows for the transfer of the desired NW on to any target substrate.

3.2.3 Transmission Electron Microscopy

Transmission electron microscopy (TEM) analysis helps to determine the crystalline quality, presence of defects, and composition of the material system. The scanning transmission electron microscope images were collected using a Jeol ARM 200F operating at 200 kV for high resolution images and a Jeol 2100 was operated at 200 kV to obtain low resolution images in TEM mode. The samples were prepared by gently sweeping the carbon net-mesh grids across the surface of the as grown samples. The cross-sections were prepared by sputtering the samples with Pt and by milling trenches through the sample, as seen in Fig. 13.

3.2.4 Atom Force Microscopy

Atom force microscopy (AFM) is used for measuring the etched depth and profile of holes with varying width and pitch for nanowire growth. The surface information is collected and stored by scanning on the surface with a mechanical needle like probe. Piezoelectric elements help in having tiny but accurate movements, which helps in precise scanning. A Park AFM (NX20) was used in the non-contact mode with the cantilevers for coarse scanning, PPP NCHR (k = 42 N/m; f = 310 kHz) and for high resolution, C14/Cr Au (k = 5 N/m; f = 130 kHz). AFM analysis done on Si(111) with etched holes, can be seen in Fig. 14. Additional data from AFM analysis is presented in the appendix 9.1.

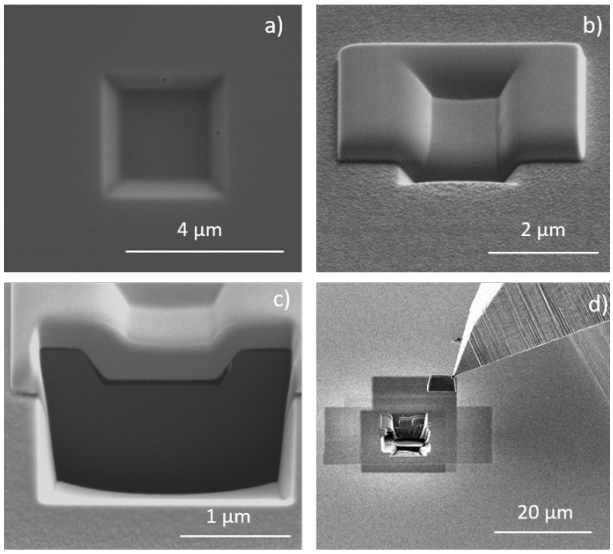

Figure 13: FIB (focused ion beam) based lamellae preparation. (a) Sample with square trenches. (b) A thick platinum layer is deposited on the desired area. (c) Ga ions used by the FIB to make a cross-section through the etched square. d) A thin cross-section (lamella) is cut and taken out on a grid for TEM analysis.

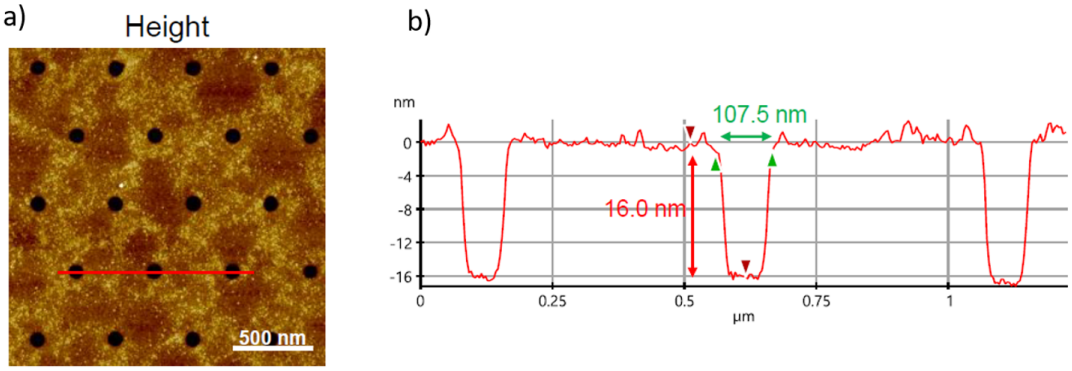

Figure 14: AFM. (a) AFM micrograph of the surface of the substrate with arrays of 80 nm holes. (b) The depth profile and the roughness of the given substrate.

3.2.5 Ellipsometer

Ellipsometry is based on polarization of light, used to characterize ultra thin films in the range of few nm. Ellipsometery uses a model based system to estimate the layer thickness. The layer thicknesses of the analyzed samples can be much smaller than the wavelength of the light. Hence, it is effectively used to record thickness measurements of thin films. An Accurion nanofilm RSE, fast spectroscopic ellipsometer is used measure the thickness of the resists and the oxides deposited during the course of this work.

3.2.6 Dry Etching

Dry etching is performed using reactive-ion etching (RIE) processes. It is an effective tool in micro-fabrication technology. It utilizes the chemically reactive plasma to remove the material

from the substrate. Electromagnetic field is used to produce the plasma under low pressure (vacuum). Thus, the high-energy ions formed due to the plasma, react with the substrate. All the RIE processes used in this thesis are performed by an Oxford PL 100/ICP RIE system with the cryo processing equipment [74].

4 Sample Fabrication

Through the course of this PhD project, all the sample fabrication and the process optimization was performed at the Helmholtz Nano Facility (HNF), a state-of-the-art cleanroom facility. The cleanroom has an area of 1100 m^2 and belongs to class 1 [75]. HNF operates equivalent to Semiconductor Industry Association (SIA) standards [19]. The following sections of this chapter summarizes all steps of the fabrication processes used in this thesis.

4.1 Silicon (111) Substrate Preparation

All the substrates for NW growth are based on Si wafers and are fabricated in a CMOS-compatible cleanroom to avoid cross-contamination.The substrate preparation for NW growth is an important step in selective area epitaxy (SAE) to have a good control over the vertical yield of the NWs. This process is optimized to have a moderately high yield of vertical NWs, crystallite free growth which is desired for greater homogeneity of the NWs. Figure 15 shows a schematic for the substrate preparation for SAE of the NWs. The growth substrates are n-doped As, Si(111), which are patterned with different hole diameters.

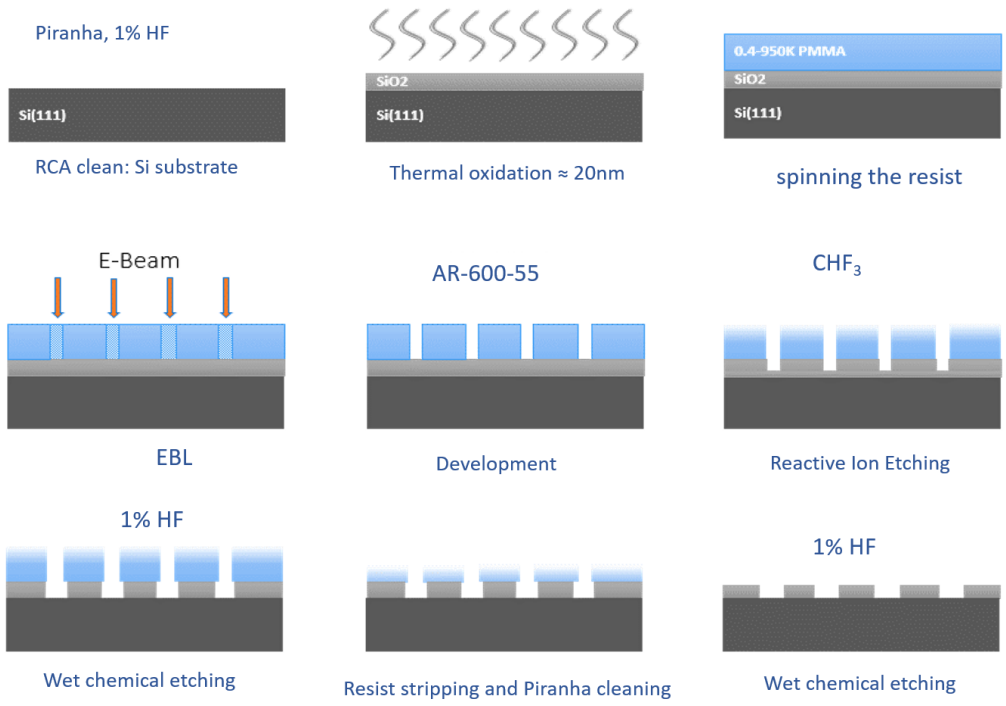

Figure 15: Schematic of the process steps: Fabrication of Si (111) substrates for NW growth

The process steps of the preparation of the pre-patterned substrates are as follows:

- A 100 mm n-doped Si(111) wafer is cleaned with strong piranha solution (H_2SO_4 and H_2O_2) to remove organic contaminants and native oxide from the substrate surface for 10 min. A 5 min HF dip is performed to passivate the Si surface, until it gets to the oxidation chamber.

- Within the next 15 minutes after cleaning, the wafer is thermally oxidised using the Massoud model [76] 990 °C for 33 min. These parameters are established for a SiO_2 thickness of 20 nm, with a precision of $\pm$ 2 nm through out the entire wafer, which is confirmed by the ellipsometry. The thermal oxide is proven to be a good mask, for growth selectivity.

- After oxidation, the wafer is then coated with AZ5214E resist at 4000 rpm for 60 s using the spin coater. Later it is soft baked for 5 min at 90°C. This is done to protect the surface of the wafer from any contamination that from the next step of wafer dicing process. It is then diced into 2.5 $\times$ 2.5 cm^2 sized square samples.

- The protective AZ5214E resist is then removed in an ultrasonic bath at high power with acetone and isopropyl alcohol (IPA) for 15 and 5 min, respectively.

- A 2 minute O_2 plasma bombardment, with 300 W and 200 sccm of O_2 flow is performed on these samples prior to the PMMA coating to increase the hydrophillicity of SiO_2 and which improves PMMA adhesion to the SiO_2.

- To further improve the resist adhesion, the samples then are treated with HMDS at 120°C and then spin-coated with PMMA AR-P 679.04 950K resist at 6000 rpm for 30 s and soft baked at 180°C for 10 min. A 200 nm-thick-resist is obtained, which is confirmed with ellipsometry.

- Then EBL writing is performed to define the mask on the PMMA resist for SAE. For development of this positive resist, the samples are dipped in AR-600 55 developer solution for 70 s with continuous stirring movements and thereafter a slower development is performed for better contrast of the 20-80 nm structures, by a 3 min dip in an IPA (isopropyl alcohol) solution.

- After the development, a quick O_2 plasma cleaning for 15 s with 300 W and 200 sccm of O_2 is conducted to remove residual resist in the holes.

- So the hole array pattern can now be transferred onto SiO_2 by a combination of dry and wet chemical etching. Dry etching the hole completely, can cause a harmful damage to the silicon surface underneath [77], which affects the vertical yield of the nanowires and potentially could also result in a parasitic growth. Thus, roughly 16 nm of the SiO_2 is removed with RIE and the remaining 4 nm by dipping the sample in 1% HF for 60 s, which is considered to be a smoother etch.

- After the pattern is etched into the SiO_2 layer, PMMA resist is removed using acetone and IPA in ultrasonic bath for 15 and 5 min, respectively. This is followed by a 10 min O_2 plasma cleaning with a power of 300 W and 200 sccm gas flow.

- Eventually cleaned in a strong piranha solution (H_2SO_4:H_2O_2 = 3:1; 96% H_2SO_4 and 37% H_2O_2) for 10 min, and is finally rinsed in de-ionized (DI) water for 10 min.

- Prior to loading the sample into MBE load-lock, it is dipped in 1% HF for 60 s, to remove any native oxide on the growth substrate. The contrast between the hard mask SiO_2 and the Si(111) is clearly seen. The finished substrate, before and after the growth of the nanowires with 500 nm pitch on Si(111) substrate is shown in Figs. 16 (a) and (b), respectively.

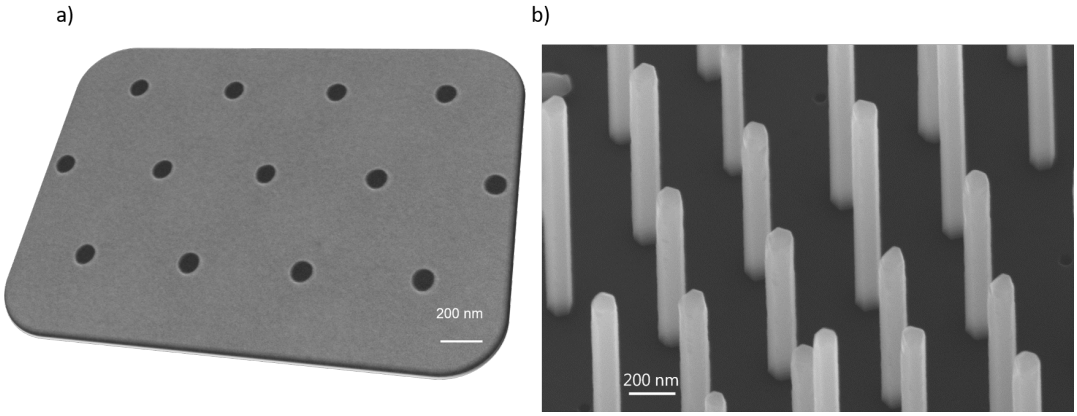

Figure 16: a) SEM micrograph of processed holes with 500 nm pitched array, clear contrast seen between the etched holes and the SiO_2 mask. b) SEM micrograph of InAs nanowires grown on this substrate.

4.2 Silicon (100) Substrate Preparation

This sections demonstrates the fabrication process for combination of the in-situ evaporation of superconductor half-shells and realizing weak-links, in-situ on an InAs NWs. The InAs NWs are grown in way that a NW grown on a tilted Si(111) facet shadows another NW grown from an adjacent Si(111) facet during a metal deposition. The junction width is determined by the diameter of the NW. Two different methods are employed for the NW growth on the Si(111) facets. Firstly, a random growth procedure is performed for a study and as a quick & dirty method and secondly, as a betterment, a SAE technique using a pre-pattered SiO_2 growth mask is performed. This can be achieved as follows, given the geometry of the metal MBE chamber and the orientation of the metal crucible, the substrate is engineered in a way that two NWs are grown from elevated adjacent surfaces, grow out and meet each other by closing passing each other. Then, while still under UHV, the superconducting shell is deposited via e-beam evaporation with the direction of deposition is perpendicular to both nanowires, which causes smooth and crystalline metal shells on the semiconductor without any interfacial distress. The process here are optimized together with Timm Mörstedt and Abbas Espiari, master students at PGI-9.
When the substrate is not rotated during metal evaporation, it creates a half-shell on both the NWs, a shadow is cast on the lower wire by the upper wire leaving a weak link within the Josephson junction on the NWs. The idea of an engineered substrate for this arrangement is seen in Fig. 17. To obtain this kind of a substrate, two processes i.e. random growth process and SAE process have been developed.

4.2.1 Substrates For Random Growth

This process steps to achieve these substrates are explained below.

- Initially a n-type Si(100) wafer is cleaned using a strong Piranha and 1% HF to remove organic matter or native oxide. The piranha solution consists of three parts sulfuric acid (H_2SO_4) to one part hydrogen peroxide (H_2O_2). Later a 10 minute Hf dip is performed to passivate the Si surface, until it gets to the oxidation chamber.

- The substrates are thermally oxidized withing 15 min under a high temperature of 990°

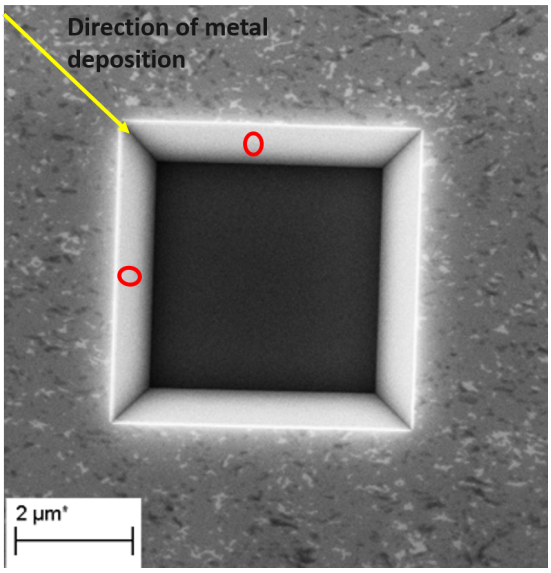

Figure 17: SEM micrograph of a substrate for template assisted growth :Si(100) substrates with exposed Si(111) facets at an elevated angle and the potential position of the nanowires depicted in the red, with 45° deposition of the metal.

in an oxidation furnace. The wafer is then thermally oxidized and the oxide thickness can be calculated using the Deal-Grove model:

$$t = \frac{d^2}{B} + \frac{dA}{B}, \tag{4.1}$$

with the growth time *t*, thickness *d* and reaction-dependent parameters A and B [78].

- After oxidation, the wafers are coated with AZ resist at 4000 rpm for 60 s, soft baked for 5 min at 90 °C. This acts as a protective resistive for dicing. Then the sample is diced into 2.5 cm by 2.5 cm squares for further processing. Then the resist is removed by acetone for 15 min and IPA for 5 min in at high power in an ultrasonic bath.

- The samples are then prepared for random growth process, can be see in Fig. 18. The samples are coated with PMMA 950k in a spin coater. The sample is spun at 2000 rpm with 500 rpm/s pre-acceleration for 30 s with a closed lid. This results in a resist thicnkess of 220-240 nm.

- The process of realizing these arrays of squares is presented in the schematic in Fig. 18. An array of squares with a size of 2, 3, 4, 5 μm with a pitch (distance between squares) of 10 μm is written into the resist using electron beam lithography (EBL). Later, the sample is developed using an AR 600-55 developer for 70 s and into IPA for 3 min for better contrast. After that, the residual resist in the structures is removed by oxygen bombardment for 15 s at 300 W and 200 sccm.

- To etch the pattern into the resist an anisotropic dry etching process with RIE using CHF_3 and O_2 gases is used to etch silicon dioxide. The sample is etched at very low temperature of 5 °C for 4 min at 50 sccm/2 sccm. The remaining few nanometers of

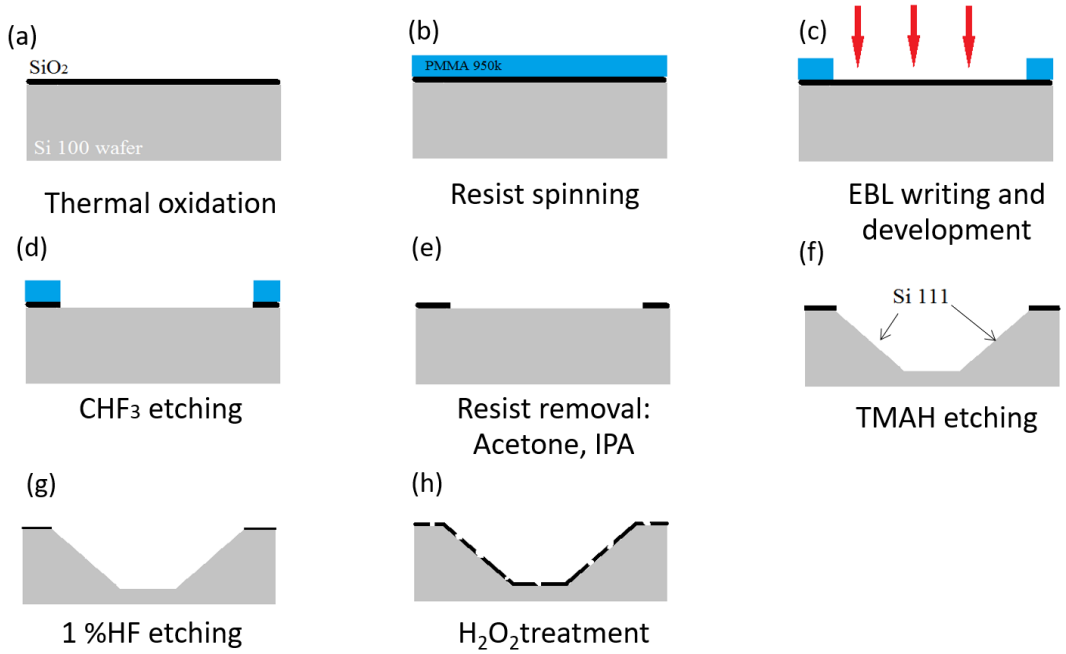

Figure 18: Schematic of the Si (100) substrate fabrication processes.

oxide is smoothly etched by 1% HF for 60 s. Then the resist is removed completely by acetone for 15 min and IPA for 5 min using a high powered ultrasonic bath.

- The squares are now processed without any oxide in them. Then these squares are etched into the Si(100) underneath to expose (111) facets, thus forming square trenches. Before etching the samples with tetramethylammonium hydroxide (TMAH), a 20 s quick Hf dip is performed so that the Si(100) surface is native oxide free and TMAH is penetrable. TMAH is chosen here since, it is a selective etchant and etches Si(100) fast, but Si(111) is etched relatively slow. Additionally, TMAH also etches the SiO_2 mask, but rather slowly at a rate of 0.2 nm/min [79, 80]. Hence, SiO_2 thickness should be taken into account. The samples are etched in TMAH for 90 s that resulted in square trenches exposing Si(111) facets with depths of 300-350 nm.

- The substrate is dipped into Hf for a quick rinse to remove native oxide. Later dipped into H_2O_2 for 45 s to create a oxide of 2 nm. The oxide layer formed here is porous and when heated causes pinholes. These pinholes in the oxide layer can act as nucleation sites to grow InAs nanowires [81]. The finished product can be seen in Fig. 19 where the randomly grown NWs, most likely shadow each other from the adjacent Si(111) facets and form a fully in-situ Josephson junction.

4.2.2 Selective Area Epitaxy Substrates

For many reasons, the selective area epitaxy (SAE) process of fabricating the samples is a betterment of the procedure mentioned above for random growth process. The idea behind the process can be seen in the schematic presented in Fig. 20. To obtain substrates suitable for SAE, two additional processes of EBL are necessary which includes EBL markers to align

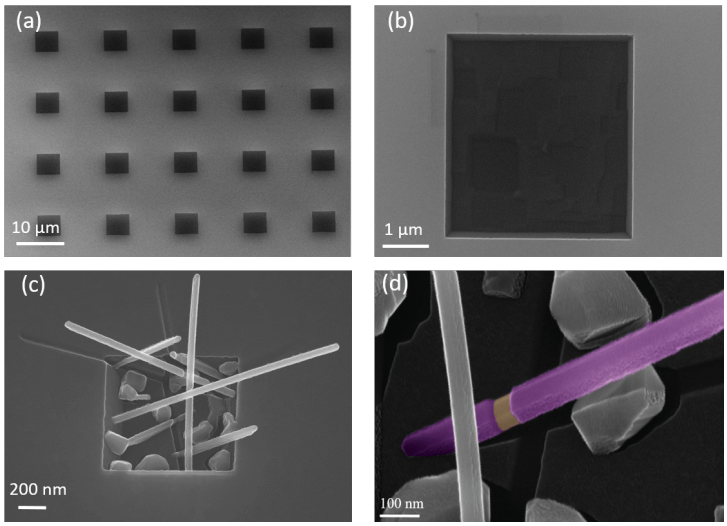

Figure 19: Substrate processing steps for achieving a Josephson junction with a weak-link formed in-situ by shadowing.

the 80 nm holes on the adjacent Si(111) facets, as a first step, and to write 80 nm holes on these substrates, as the last step. The process steps are as follows:

- The first EBL step is to implant the 20 μm $\times$20 μm squared EBL markers onto the sample surrounding a group of 90$\times$ 90 square arrays. These markers ensure that amongst this set of 90 $\times$ 90 squares, all the growth holes are aligned to each other. So it begins with a diced Si(100) wafer with a 20 nm of thermal oxide layer. The sample is spin-coated with UV6 resist at 4000 rpm. This results in a resist thickness of approximately 600 nm. Furthermore, the resist is soft baked at 130 °C for 1 min. After the EBL writing process, the sample is developed using MF CD-26 solution for 90 s. Further on, the markers are etched into SiO_2 and Si by dry etching anisotropic RIE process. First, a RIE with CHF_3 and O_2 is used to etch the 20 nm oxide layer for 3 min and then 2 min of SF_6 etching is used to etch deep into Si at 20 °C. This etches 1μm deep EBL markers into the substrate. Later the remaining UV6 is removed with 10 min using acetone and 5 min using IPA in a high powered ultrasonic bath. This process constitutes the first EBL step.

- The second EBL step with PMMA, constitutes of the square writing, and hole placement on the Si(111) facets. Once after the squares are etched with TMAH, the oxide mask is entirely removed by a 5 min dip in HF. Now that the samples have etched markers in them, and the squares are etched into them without any hard-mask. Subsequently, a thermal oxidation step is repeated to create the oxide mask for the entire wafer again which now covers even the TMAH etched squares. However, in this case the oxide thickness on (100) and (111) surfaces is not identical, mainly because the growth rate at a certain temperature is different on different facets of Si and also because the ratio A/B as mentioned in Eq. (4.1) is vastly different for (100) and (111) surfaces at the same temperature [78]. This results in a 25 nm thick oxide layer on (111) surfaces compromising the layer on (100) surfaces down to 18 nm, which is still sufficient considering the silicon oxide loss due to HF etching in the following steps.

- The last and the third EBL step comprises of defining growth holes for SAE. The hexagonal holes are written as 80 nm hexagons in the PMMA resist. Except for missing the

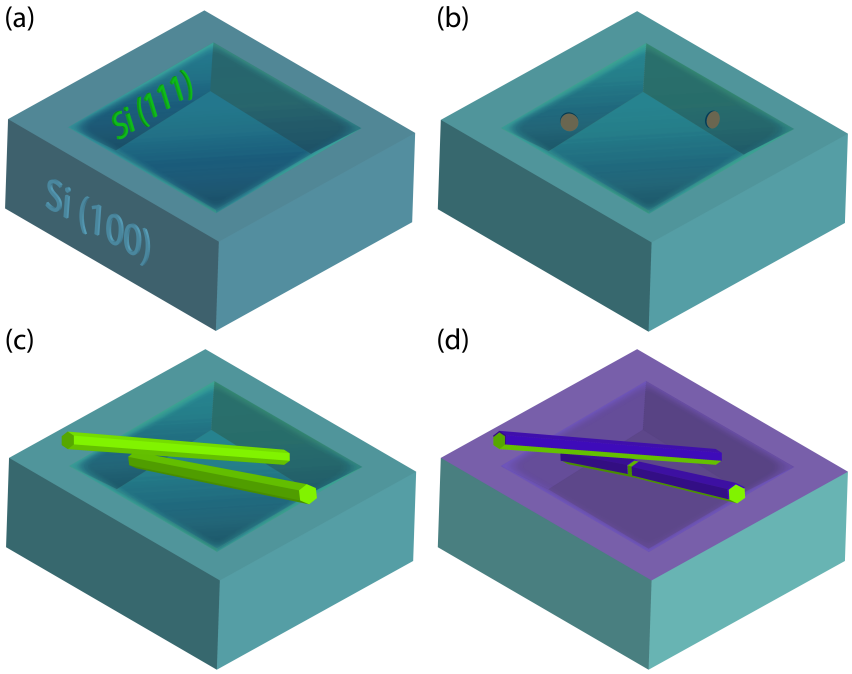

Figure 20: Schematic of substrate processing steps for achieving a Josephson junction with a weak-link formed in-situ by shadowing.

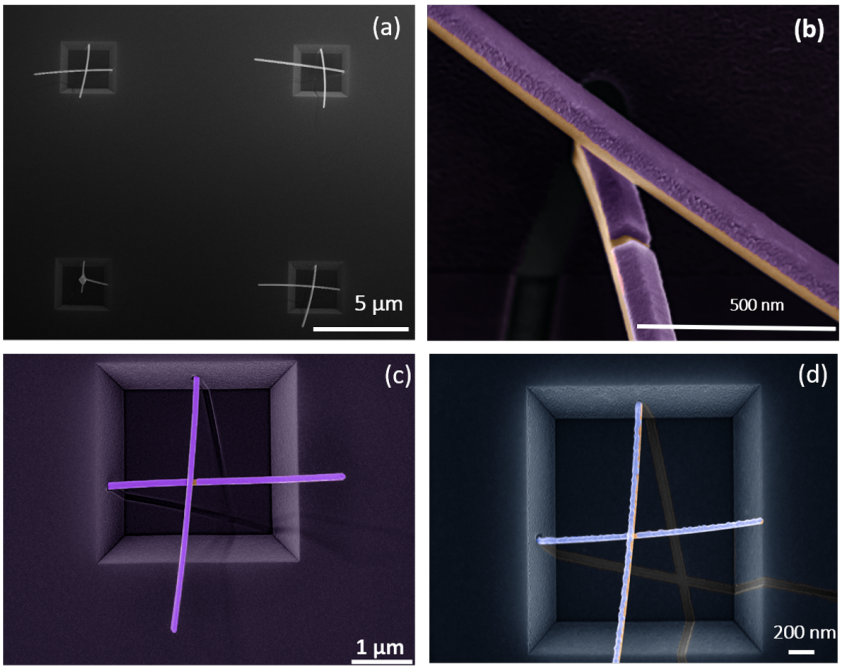

Figure 21: SEM micrographs of the processed substrate. (a) Yield of this process was about 80%. (b) close-up of the weak linked Josephson junction, with Nb as a superconductor. (c) One of the etched squares with nanowires crossing each other forming a weak link during Nb deposition. (d) The same situation, but with Al as a superconductor.

TMAH etching step the third EBL process is similar to the one in Fig. 15. The holes then are etched with a combination of RIE dry etching and HF wet etching as mentioned in Si(111) processing. First, the silicon dioxide layer is etched with CHF_3 of 2 min and

50 s at 20 °C at 50 sccm. Eventually, the rest of the 4-5 nm of SiO_2 is etched with 1% HF for 60 s. The samples are then loaded into the MBE load-lock for further growth process and metal deposition steps. The finished sample in Fig. 21 gives a brief outlook. Other possible structures that could be grown using this platform are mentioned in the appendix 9.3.

4.3 InAs Nanowire Growth

Firstly, for the optimization of the parameters for the substrates for SAE, the samples were used for testing the growth of InAs NWs. After verifying the effectiveness and reproducibility of the growth process with respect to yield, morphology, substrate preparation, substrate temperature, growth time, etc, [55, 77, 82], then several sets of wires like InAs NWs, InAs-Te doped NWs, InAs/Al half-shell and full-shell NWs, InAs/Nb half-shell NWs were grown. The SAE substrates processed during the course of this thesis, was optimized for 100 kV acceleration voltage for EBL writing with altered substrate preparation and growth parameters.

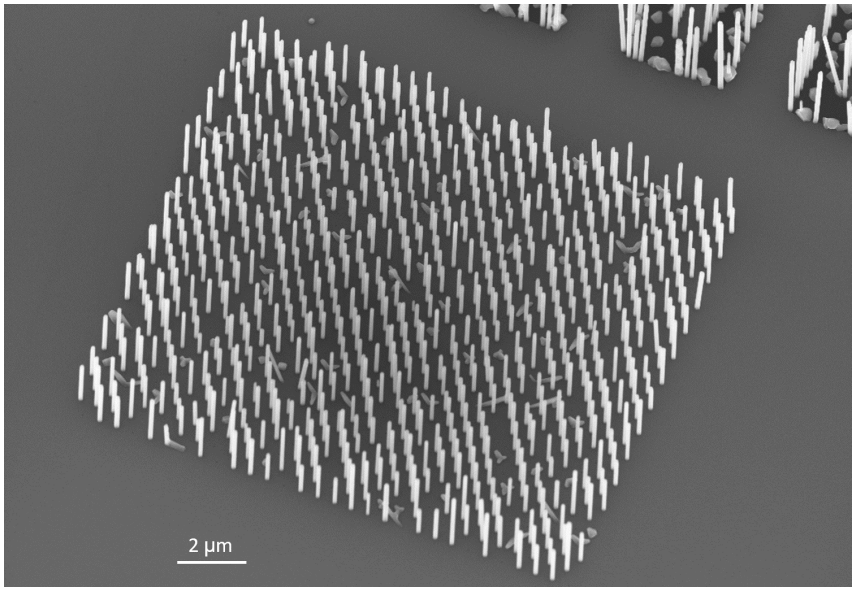

Figure 22: InAs NW array grown on Si(111) substrate

The InAs nanowires are grown by MBE (vapor-solid growth) with an In growth rate of 0.08 μm/h and an As BEP of 4×10^{-5} torr. The substrate temperature for the growth of InAs NWs was 480 °C. These values were optimized [77] with respect to high NW yield, low crystallite density and to obtain an average NW diameter of 150 nm. Figure 22 shows the sample with NWs that were grown with these conditions for a standard growth time of 2 h 30 min. For probing quantum mechanical effects and reduce the channels of conduction as well, a reduced diameter would facilitate lowering of classical contributions to the transport.
Thus, in order to obtain thinner nanowires, a technique comprising of growing the NWs for 10 min in a optimized window and later grown for 2 h 30 min with reduced In growth rate of 0.03 μm/h and an As BEP of 3×10^{-5} mbar [55, 83].
Figure 23 shows the NWs grown on similar samples, providing comparison between higher and lower fluxes of In and As. The inset positively resulted in a high NW yield and a low crystallite density as well. The NWs were found to be, on average, of a homogeneous length and diameter too. The average length obtained for a growth time of 2 h 30 min was found

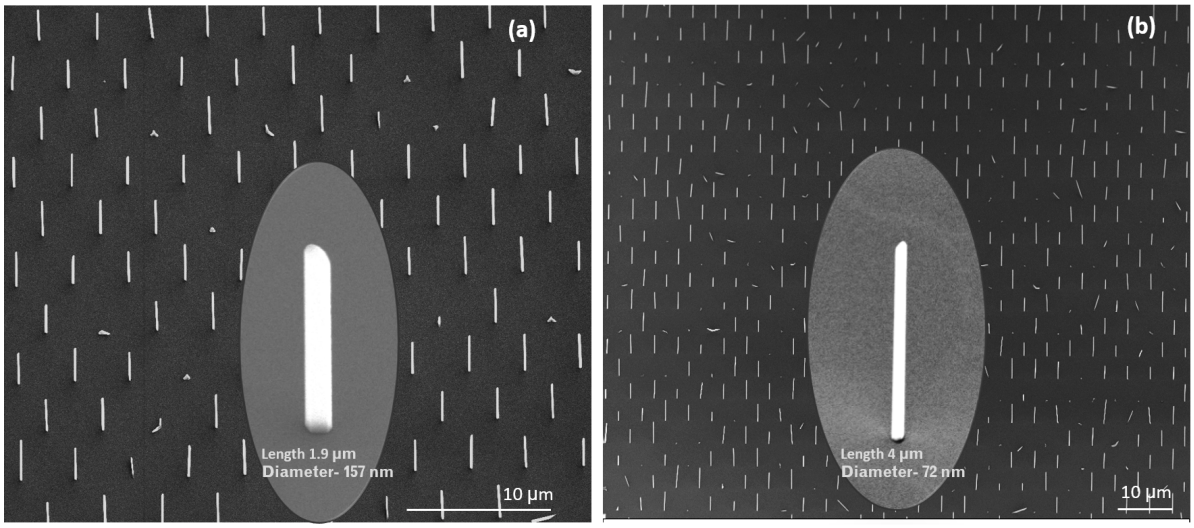

Figure 23: InAs NW array grown on Si(111) substrate. (a) With higher fluxes. (b)With higher fluxes and then reduced to lower fluxes.

to be around 3-3.5 μm. Henceforth, this technique was implemented for growth of InAs NWs to have a diameter smaller than 100 nm. This process resulted in the reproducibility of NWs with diameter of 70-80 nm with a high yield.

4.4 Te Doping

A n-type doping is performed on the InAs NWs by incorporating Te-atoms via a GaTe effusion cell during the NW growth in MBE A. Here, a GaTe-cell instead of an elemental tellurium source was used due to the high vapor pressure of Te. The calibration of GaTe cell is done using Hall measurements, which were conducted on GaAs layers grown on semi-insulating GaAs (001)-substrates. Based on this calibration, for the InAs NW doping, the GaTe-cell was set to the corresponding temperatures of doping concentrations observed enabling the incorporation of Te atoms. At higher concentration of Te, it causes InAs nanowire faceting, i.e. changes in morphology is observed [84, 85].

4.5 Metal Shell Deposition

The deposition of the superconductors aluminum, niobium, palladium, titanium and aluminium oxide took place in a metal MBE, using an electron beam evaporator. Initially the metal is deposited on a planar Si substrate to estimate the growth rate by XRR, done with help of Dr. Gregor Mussler.

4.5.1 Aluminium Deposition

After the NW growth, the sample is transferred into the preparation chamber under UHV. It is baked again in the preparation chamber at 400°C for 20 minutes and 450 °C for 5 minutes.

This is necessary in order to prevent from potential AlAs interlayers, which might form during the metal deposition due to an As film at present after NW growth. The desorption procedure removes the arsenic overgrowth on InAs NWs [31]. For the Al growth the sample is cooled overnight to achieve a temperature of -6 °C, because Al is less likely to form droplets at lower temperatures [31]. To attain such low temperatures, the water cooling has to be disconnected and every heat source within the MBE chamber, i.e. all other cells have to be turned off. After turning off other sources, the temperature drops due to the cryogenic shield, starting from ambient temperature down to -6° C in about 15 hours. The sample is left over night and the deposition is done the next day, without a substrate rotation, which causes directional deposition in order to obtain an Al half-shell and on rotation to obtain full aluminum shells. A 25 nm aluminium half shell is deposited at a pressure of 3.3×10^{-9} bar for 40 s. The morphology and the crystallinity of the Al films depends on the substrate temperature.

4.5.2 Niobium Deposition

To obtain a smoother and a crystalline film of niobium, the temperature is much high when compared to Al [86, 87]. Also the deposition angle between the Nb metal crucible and the substrate is kept almost at 90°, this changes the morphology and the growth mode of Nb [84]. The Nb deposition process is very similar to aluminium, but the substrate temperature is higher i.e. 50 °C and the Nb pressure is 2.6×10^{-9} bar for 180 s.

4.5.3 Aluminium Oxide Deposition

An in-situ deposition of AlO_x is used to cap superconductor metal surfaces. Al when deposited has a post-growth diffusion, which takes place when the sample is taken out from -6° C to room temperature, this changes the whole morphology of Al. The post-growth diffusion has some detrimental effects such as formation of non uniform Al layer and diffusion into the weak-link area. This scenario of post-diffusion can be avoided by depositing AlO_x at low temperatures in-situ [31][88]. The AlO_x is deposited in-situ onto the superconductor metal, in the same metal MBE chamber and at the substrate temperature which is maintained for the superconductor.

4.6 SEM With A Micromanipulator

SEM is a visual and vital tool used to examine nanostructures and in this case for nanowire yield, surface morphology and aspect ratios of the structures. It uses a focused beam of electrons to produce high-resolution images. A *Kleindiek* micromanipulator is installed in the SEM that helps in precise manipulation of nanostructures using nano-needles [89]. With this set up a physical manipulation is allowed with a nanometer precision and using a 100 nm tip and a good resolution of the SEM. One can pick up the envisioned nanostructure and accurately place it on a target substrate.

5 Substrate Analysis

In this chapter, substrates prepared for different processes are analysed and the corresponding results are presented.

5.1 Si (111) Substrate Preparation

The substrate preparation is a crucial step in SAE, to have a good control over the vertical growth of the NWs. A high yield of vertical NWs, crystallite-free growth as well as growth selectivity is desired for homogeneity. All the sample processing steps started with a brief wafer cleaning process which is a standard RCA cleaning. This process step is known to improve the surface quality by getting rid of the organic contaminants and native oxide, further improves the atomic roughness on the wafer. In order to obtain position controlled nanowires, a 20 nm thick dielectric layer of SiO_2 is thermally grown on the Si wafer after the cleaning procedure. The thickness of the SiO_2 is confirmed with ellipsometry, using the model with Si and SiO_2. The thickness is varied throughout the wafer within a range of 20 ± 1 nm. A 220 nm PMMA resist is used as a mask for EBL to write few tens of nanometer structures, the PMMA resist layer thickness is also confirmed using ellipsometer, but the model is calculated with the thickness of SiO_2 taken into account.

5.1.1 Effect of Electron Beam Lithography

The hole structures written by EBL, have been varied to see the influence of the growth, depending on the pitch and the diameter of the holes. For this purpose, attaining the right combination of EBL dose and the development time is a must.

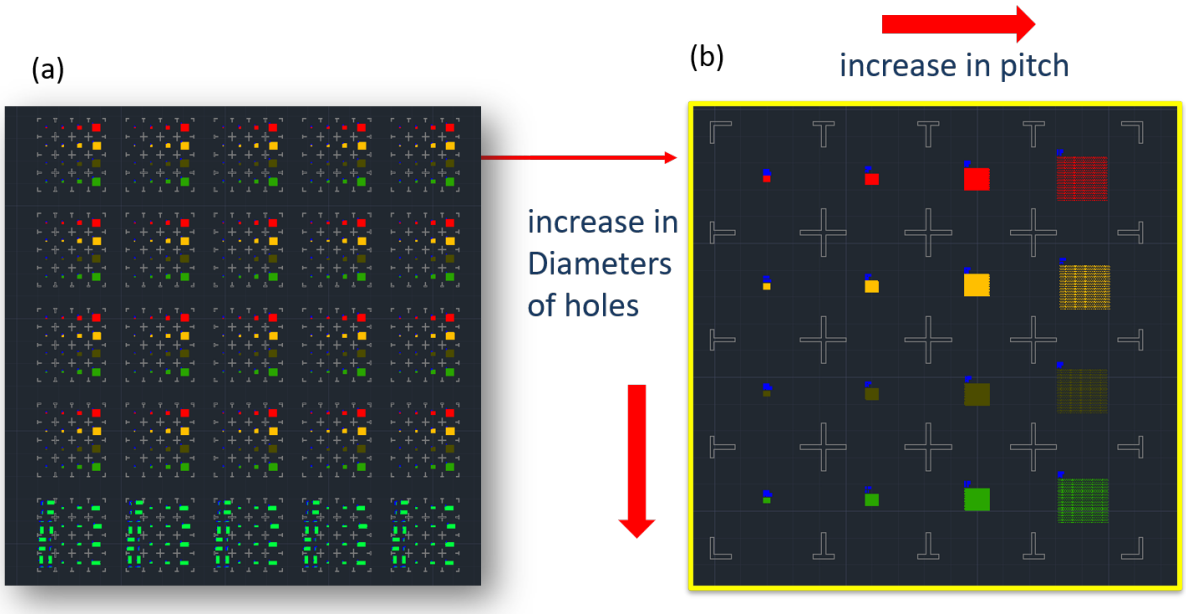

Figure 24: EBL mask (a) The overview of the mask, (b) The arrays of holes with varrying pitch of 500 nm, 1 μm, 2 μm, 4 μm and a varying hole diameter of 20 nm, 40 nm, 60 nm, and 80 nm. The bottom on (a) shows striped structures written to obtain the rough etch rates with a DEKTAK.

The arrays of holes written with EBL are varied along the column. The electron beam lithography (EBL) mask designed can be seen in Fig. 24. The EBL doses were varied from 900 μ C/cm^2 to 960 μ C/cm^2 at 100 kV with 200 pA beam current. The right dose was found at 920 μ C/cm^2, which is a combination of optimized development time and RIE parameters, which is evidently shown in the next section. The sample with PMMA resist written over by EBL, is further developed by AR-600 55 solution. To ensure a right development, the sample is developed for a specific time and then the depth profile is measured using AFM. Using this estimation, it is found that 70 s is the optimum development time with an additional 3 minute dip in isopropyl alcohol (IPA) solution to give contrast to the nanostructures. The crucial step here is to obtain resist-free developed structures, thus a short oxygen plasma treatment for 15 seconds with 300 W, 200 sccm oxygen right after the development is performed. The SEM micrograph in Fig. 25 shows the effect of the EBL doses. Figure 25 (a) shows the arrays written with a lower dose. It shows a lot of crystallites and tilted nanowires, which could be due to premature development of the nanostructures. In contrast, Fig. 25 (b), shows an optimized dose where are the nanostructures written in an array have been uniformly developed. With a yield of 95% of InAs nanowires. As seen before in Fig. 24, the nanowire mask for SAE is designed to test

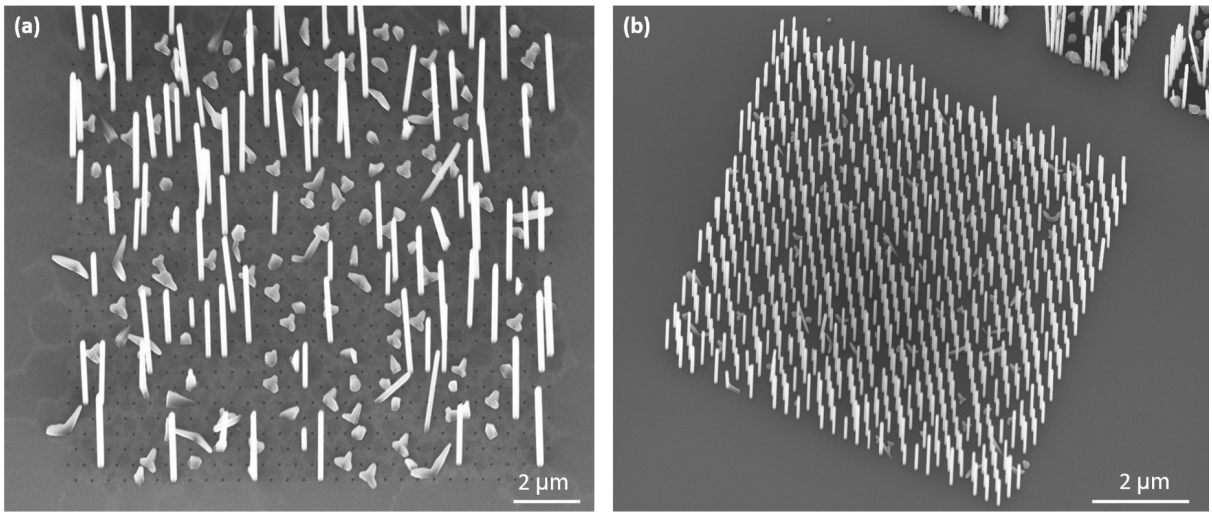

Figure 25: Effect of EBL. (a) The NW arrays written with lower dose 900 μ C/cm^2. (b) NW array with the right dose 920 μ C/cm^2 at 100 kV.

various hole diameters and pitches. In order to observe the nanowire growth behaviour and the yield. Further on, the samples have been optimized for a higher nanowire (NW) yield, as well as for homogeneity in diameters and lengths [82]. Atomic force microscopy (AFM) was conducted on these samples to check the depth profile of the holes, which is illustrated in the next section. These results also proved that the depth profile of the holes is more homogeneous for a diameter of 60 nm and 80 nm. Hence, the observations and results deduced from this paved a way to optimization and reproducibility. A new mask, as seen in Fig. 26, was used for the growth during this work which was written on the samples with optimized EBL parameters, and only consisting of 80 nm holes with a 4 μm pitch. It was observed that the highest yield was obtained for a hole diameter greater than 40 nm and a pitch greater than 2 μm. The reason for this is attributed to growth regime dominated by diffusion limited rather than material competitive growth. Therefore, considering these results, the new mask has been written, as shown in Fig. 26, with four quadrants filled with holes of 80 nm in diameter and the pitch being the distance between any two holes is 4 μm.

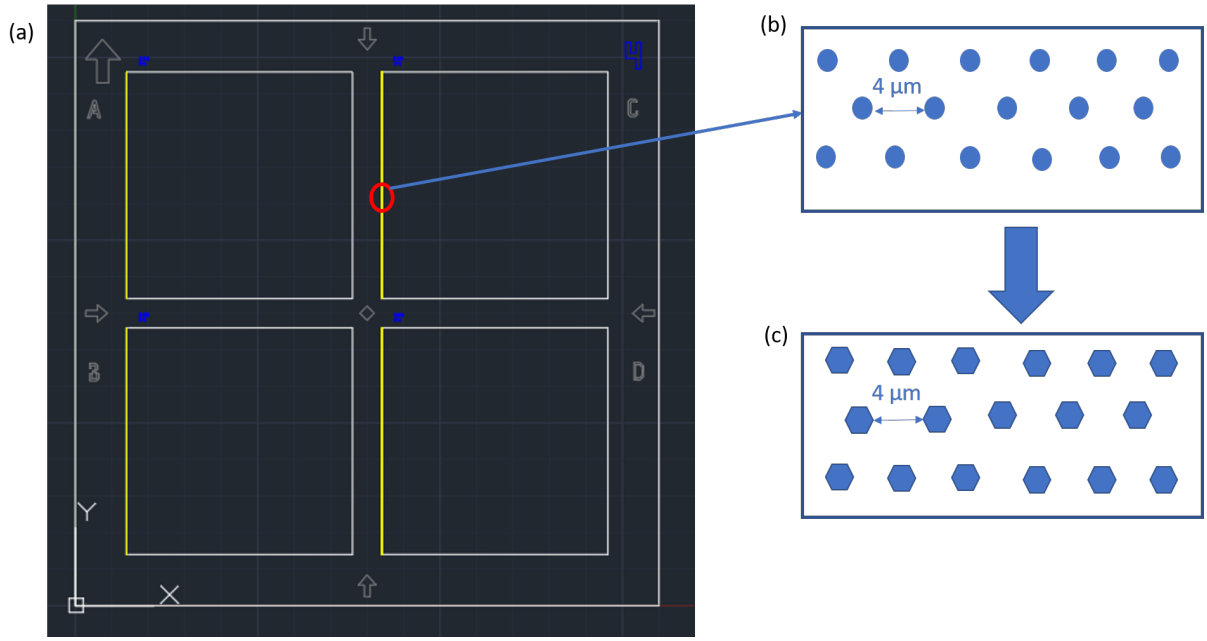

Figure 26: EBL mask with growth windows (a) EBL mask overview: Yellow stripes representing the hole array for position controlled nanowire growth which will be repeated through the quadrant during EBL writing, (b) circular nanowire growth holes written, (c) hexagonal nanowire growth holes written.

The next important optimization step done during the course of this thesis is to study the shape of the holes written and its effect on the growth of the nanowire. This study not only proved that the shape of the hole does not matter but also reduced the EBL writing time of these holes by 86%. The EBL writing for these circular arrays is a 14 h long process, and the simple change of the hole shape reduced the EBL writing time to 1 h 45 min process. This is because a circular hole when written by the EBL is first defined using a helix, so the electron beam is directed along this path, from the outward of the circle to the inward center of the circular hole. This translates every beam point to a set of coordinates, which is a very long process. in contrast, the hexagonal hole the shape is defined by the electron beam in rows of points just along the hexagon which results in fewer coordinates to read, thus shorter time. As can be seen in Fig. 27, no change is observed in the NW morphology indicating that the hexagonal hole provides the same environment for facilitating the growth of the NWs as the perfectly circular one.
This has also been confirmed on the samples etched with TMAH, where the holes are written on the Si (111) facets of a Si(100) sample, where in the holes written on these facets are at 54.7 ° to Si(100) plane, as seen in Fig. 28. As a result, projects the hexagonal holes written on these tilted facets have a slight oval shape. This illustrates the fact that the nanowire morphology remains same regardless of the growth hole. In summary one finds that, a window opening to the Si surface is a mere necessity. Eventually, the droplets nucleate near the edge of the hole (of any shape or size), where the energy is minimum [82, 90]. The important point being that the ratio of NW/hole diameter is 1, which was optimized in our process to be a hole diameter of 80 nm. To learn more about the geometry or the structure of the hole, a focused ion beam (FIB) cut is performed on these samples, and are covered by platinum for protection. A cross-sectional cut with Ga-ions (FIB) is further performed and the imaging is done with a high magnification SEM. The samples prepared for these tests are first written

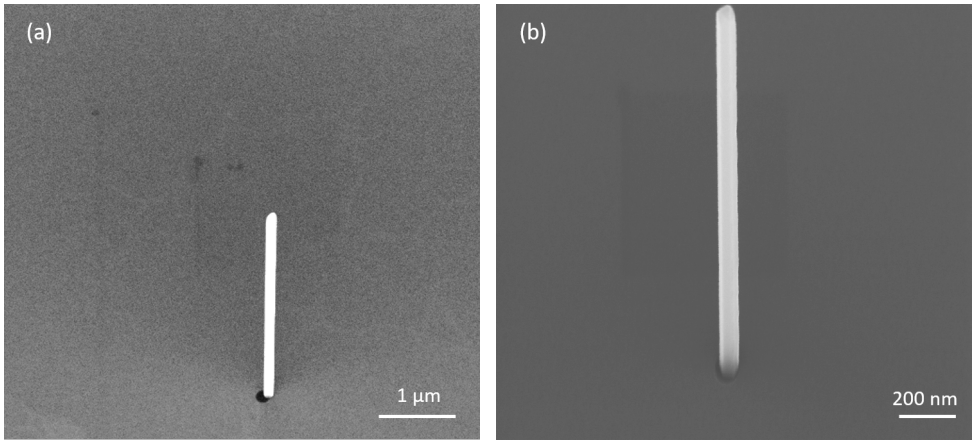

Figure 27: SEM-growth window shape written by EBL. (a) Circular hole shape, (b) Hexagonal hole shape.

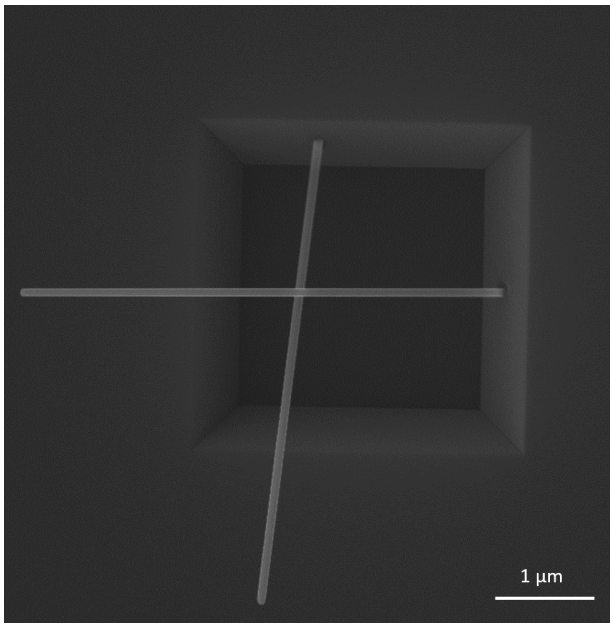

Figure 28: SEM micrograph of the nanowire grown out of the elongated hexagon holes written on tilted Si(111) facets, showing NW growth is still similar to the other counterpart environments

by EBL, developed, and then finally etched with RIE. Figure 29 shows the cross-sectional FIB cut of both the holes. Figure 29 (b) depicts the hexagonal hole etched, that has a pronounced trench shape than the circular one in Fig. 29 (a).
These SEM micrographs, as seen in Fig. 29, show the FIB cross-sections of the holes with different shapes etched by RIE. It can be seen that the hole is not etched entirely. This remaining oxide (5-6 nm) would be etched by HF later. HF etching is an isotropic process known to smoothen the edges of the holes.

5.2 Effect Of Reactive Ion Etching

Reactive ion etching (RIE) is the most efficient combination of ion bombardment and chemical etching. This process is the key to obtain straight NWs and a high NW yield. It consists of CHF_3 gas etchant which is a anisotropic etchant, which affects the geometry of the hole.

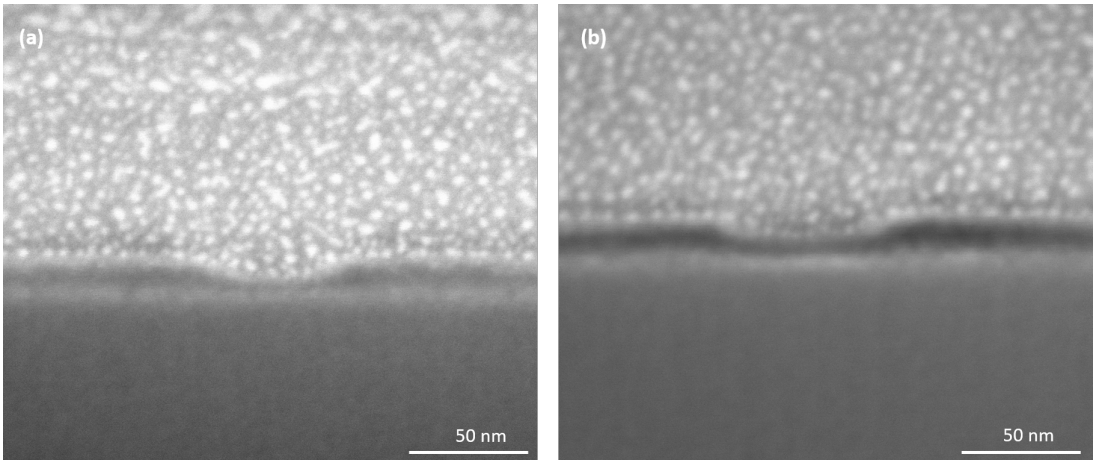

Figure 29: FIB cross-sections, RIE etched and the samples covered with Pt (dotted metal deposited in the SEM micrograph) for protection, the gray layer below is the Si (111) the darker layer is the SiO_2 layer which is etched by RIE (a) circular hole, (b) hexagonal hole

The parameters used are gas (CHF_3) flow 50 sccm, with an RF power of 101 W and a DC bias of 340 V. Optimizing the RIE parameters is a continuous process, since the etch rates could be changed with maintenance of the RIE system. Various AFM tests were conducted on these substrates to check the accuracy and reproducibility of the process parameters. The SiO_2 thickness was 20 nm which was maintained through the entire course of the PhD project, which has proven to be an effective mask for the SAE process. The etch rates from RIE were determined using plain test samples covered with SiO_2. Ellipsometry measurements were conducted on such samples before and after RIE to determine the oxide thickness and thus to obtain an average etch rate. The etch rate was taken using both the RIE-4 and RIE-5 tools, the difference between the tools is the geometry of the etching chamber. The RIE-4 chamber is equipped with nitrogen cooling which allows for a low temperature etching. The temperature used for RIE 4 etching process is 5°C, the low temperature etching ensures a controlled uniform etching. The etch rates have been calculated, the important finding here, is that the etch rates on the plain samples i.e. without any constrictions as in the nanostructures (written by EBL) is higher than the samples with geometric constrictions i.e. nanostructures written by EBL. This can be attributed to the fact that the gas etchants have to penetrate through these nanostructures, to etch them whereas on the plain samples, it is easy to etch away several layers at much shorter time. The etch rates are $\approx$ 10 $\%$ higher on the plain samples than the nanostructured samples. The etch rates for both RIE set-ups have been estimated, even though the etch rates in both machines seem almost similar. The fact that this is evaluated to a nanometer scale changes everything. Figure 30 shows the etch rates estimated by both tools but at different temperatures.
The etch rate for RIE-5 is higher being 0.4 nm/sec, which requires 40 seconds to etch 16 nm of SiO_2 on the plain samples and an estimated 30 seconds for etching on the nanostructures. In contrast, the etch rate at RIE-4 is much lower being 0.095 nm/sec, which takes 169 seconds to etch 16 nm of SiO_2 on a plain sample and an estimated 180 seconds to etch on the nanostructures. Figure 31 shows the unchanged yield and morphology of the nanowires processed by using both tools.
The next tested optimization process was the addition of O_2 to the CHF_3 gas, the process parameters such as RF power and DC bias are kept similar as the process described above,

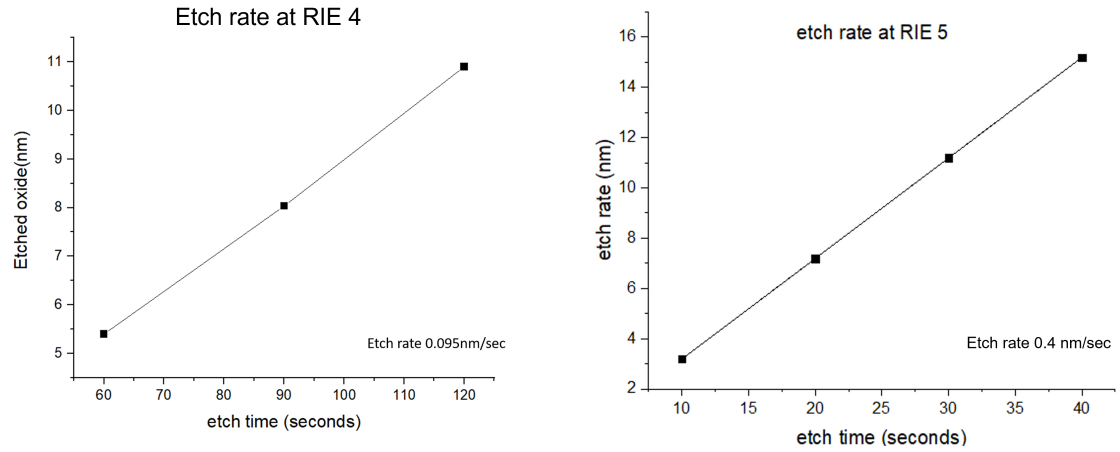

Figure 30: RIE etch rates on plain samples with Si (111) and a 20 nm ,thermal oxide of SiO_2, (a) RIE-4 etch rate at 5° C, (b) RIE -5 etch rate at 20 ° C.

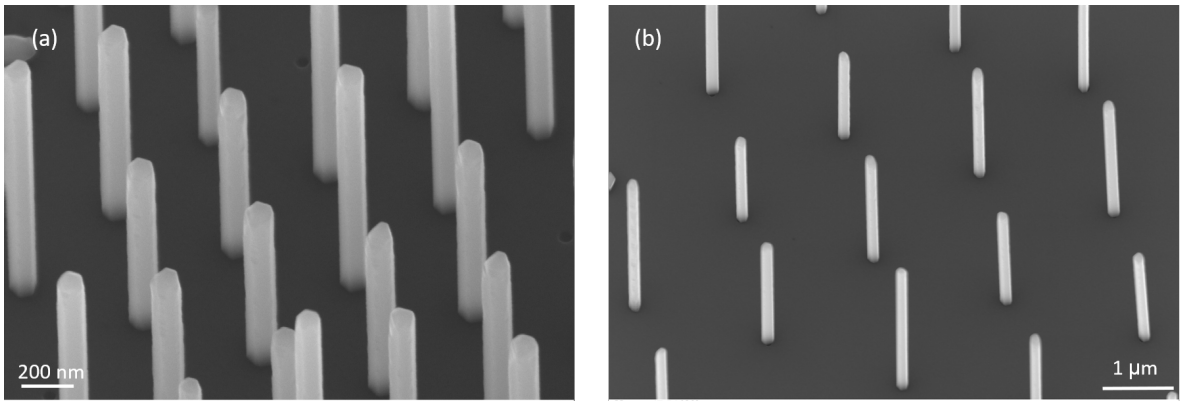

Figure 31: Nanowire arrays with 95% yield, (a) RIE-5 processed nanowire arrays with 500 nm pitch, (b) RIE-4 processed nanowire arrays with 2 μm pitch

but the gas flow is changed to CHF_3/O_2 i.e. 50 sccm/8 sccm. Flat and vertical sidewalls were achieved with the etch rate of 0.175 nm/sec. The etch rate has increased by 13% on an addition of 8 sccm of O_2. However, the profile quality is very sensitive to the addition of O_2. Significant side walls have been observed with a slight addition 8 sccm O_2 addition to the CHF_3 plasma. It is also observed that the micro–trenching increases significantly with the addition of O_2 gas. This is due to the fact that oxygen ions physically bombard the dielectric film, which in turn gives a deep and flat trench-like profile, whereas CHF_3 chemically etches, giving rise to a bow shaped trench. The FIB cross-section of the profiles of the etched holes have been compared and shown in Fig. 32. The samples provided for FIB have been coated with PMMA and then written by EBL for 80 nm holes. Subsequently, they are etched by RIE for 98 seconds and 87 seconds, respectively.
The NW growth yield can be seen in Fig. 33. The NW nucleation does not seem to alter significantly for different trench profiles, the nucleation still seems to happen at the edge of the trench. In Fig. 33 the NW have different lengths and diameters. This is due to changed growth parameters. Regardless of the trench profile, the NW yield or the way they nucleate has been a constant process.

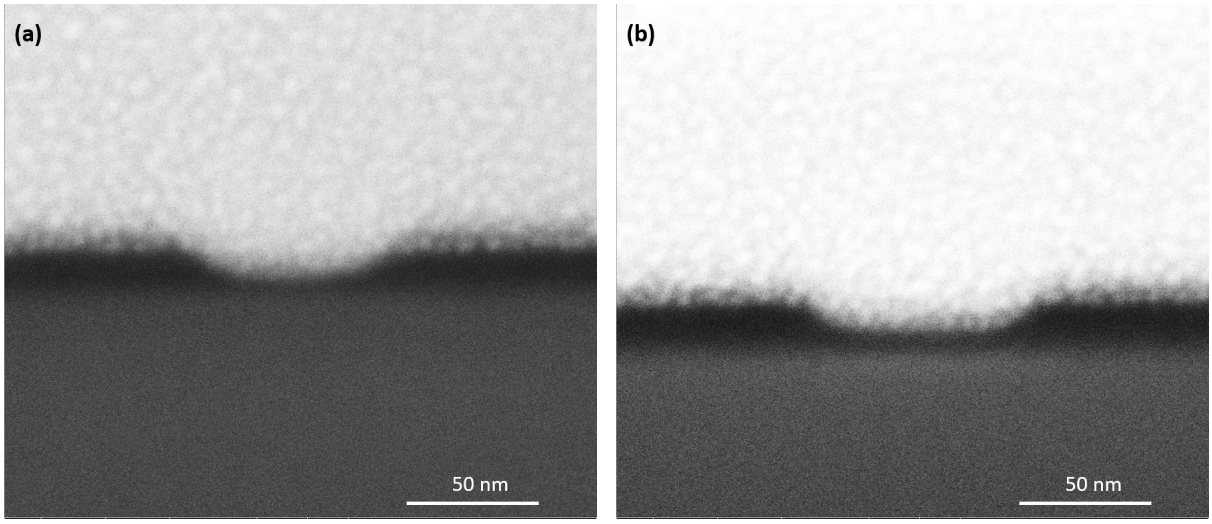

Figure 32: SEM micrographs of the FIB cross-sections of the RIE etched hole profile. (a) etched with CHF_3 for 98 s, (b) Etched with CHF_3 and O_2 for 87 s.

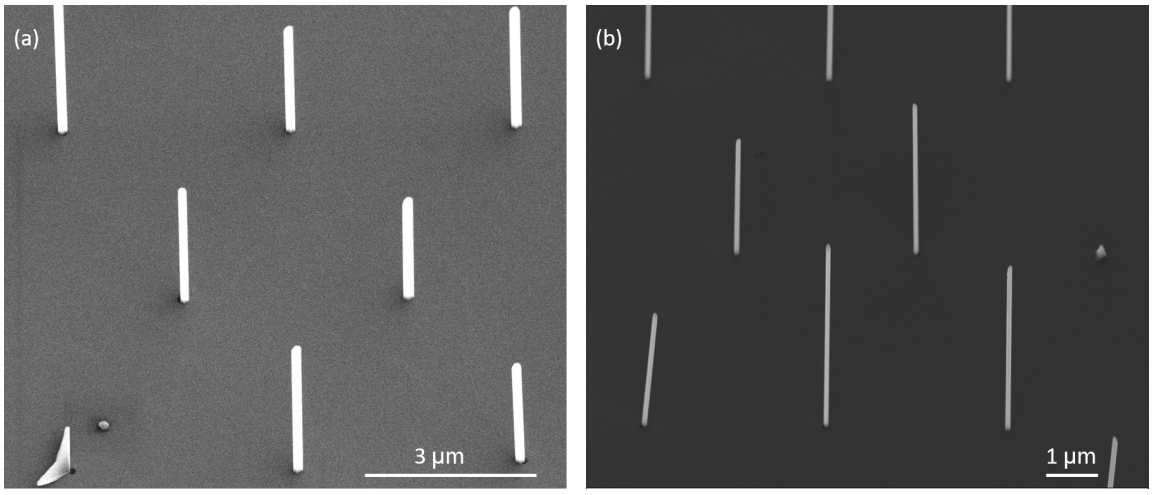

Figure 33: Growth and yield of NWs, (a) NW growth on RIE etched nanowire arrays with CHF_3, (b) NW growth on RIE-etched nanowire arrays with CHF_3 and O_2.

5.3 AFM Analysis

The EBL mask used to define the arrays for SAE has multiple fields i.e. range of varying hole diameter, pitches, as seen in Fig. 34. Furthermore, to study the affect of RIE on the different diameters of nano-holes, atomic force microscopy (AFM) analysis was conducted on the samples to check the depth profile of the holes. The samples prepared for this study are Si samples covered with SiO_2. All the samples have been RIE etched with CHF_3 for 98 seconds, with the goal to remove 16 nm of SiO_2.

The analysis of the different diameters can be found in Table 1, which gives the diameter of the etched hole and the depth. The depth ($\approx$ 16 nm) is very homogeneous for the nominal diameter of 80 nm. The 80 nm is chosen as an optimal diameter and the corresponding NW yield on 80 nm hole arrays can been seen in comparison with other diameters in Fig. 35. The parasitic growth is less with a vertical yield of 95%.

There are several factors which could hinder the yield and the morphology of the NWs, these

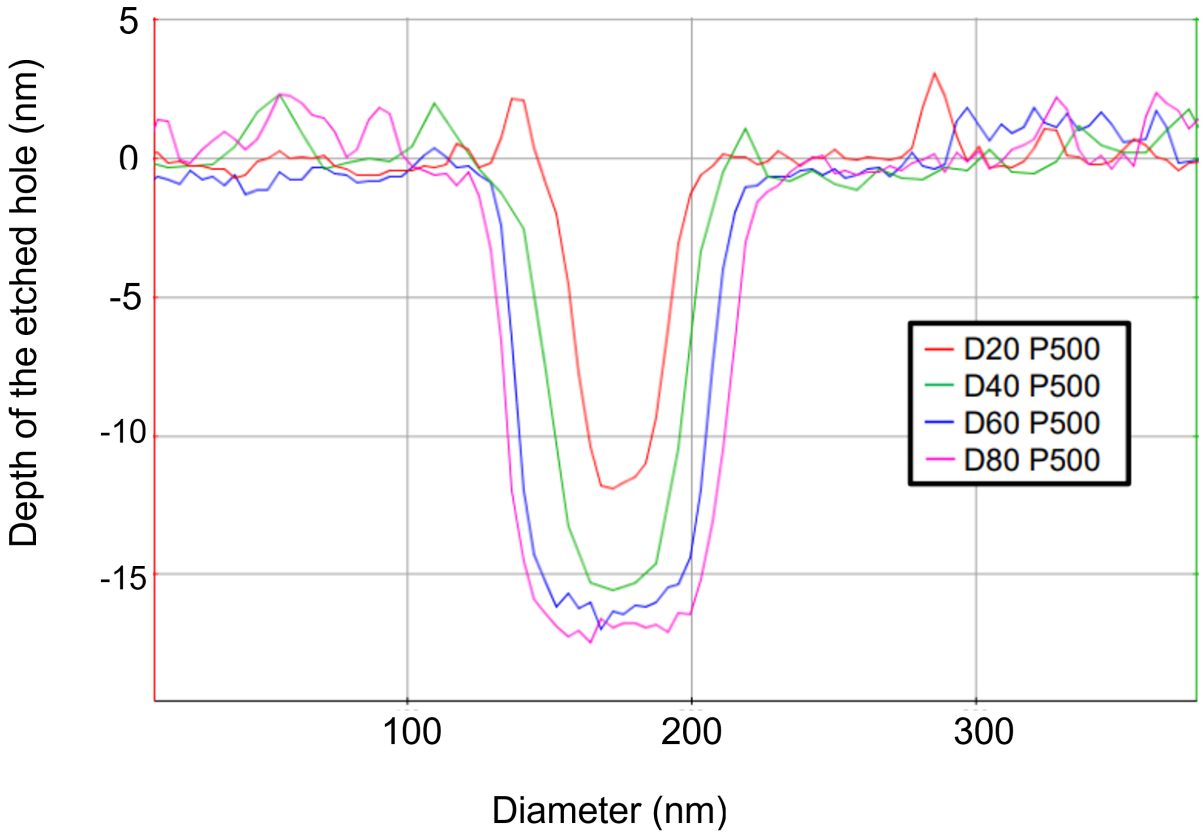

Figure 34: Depth profiles of all the diameters probed. D: hole diameter in nm, P: pitch in nm

Parameters	D20	D40	D60	D80
Width (nm)	55.10 ± 1.91	68.20 ± 3.30	81.08 ± 3.77	102.2 ± 3.14
Depth (nm)	12.70 ± 0.71	14.57 ± 0.71	15.50 ± 1.02	16.10 ± 0.12

Table 1: Summarized width and pitch values from AFM analysis measurements shown above with D as diameter and P as pitch in nm.

are known as parasitic deformities. Figure 36 shows one of such flawed sample. The defects have been marked which are the potential causes against a good NW yield. The ones marked in yellow are NWs growing in one of the three (111) directions and are angled at 70.4° to the substrate. The ones circled in green are also some of the nanowires which start to grow in two (111) directions and result in small V-shaped structures, this can be attributed to over etching with RIE and into the Si surface and further by altering the Si crystal underneath which has also been observed by Tomioka *et al.* [91]. The ones marked in red are the holes which have not been developed well because of the low doses. This could cause a irregular hole openings which do not create an environment for NW nucleation.
In summary, the optimized parameters for a nanowire array with good yield comprises of RIE etching of 16 nm of SiO_2 and leaving 4 nm which is further etched by HF. This two-step etching technique combines the anisotropic etching of RIE which resulted in cylindrical holes. And with smooth etching with HF, resulted in unwanted etching of Si substrate. Performing this step increased the yield by 30 %.

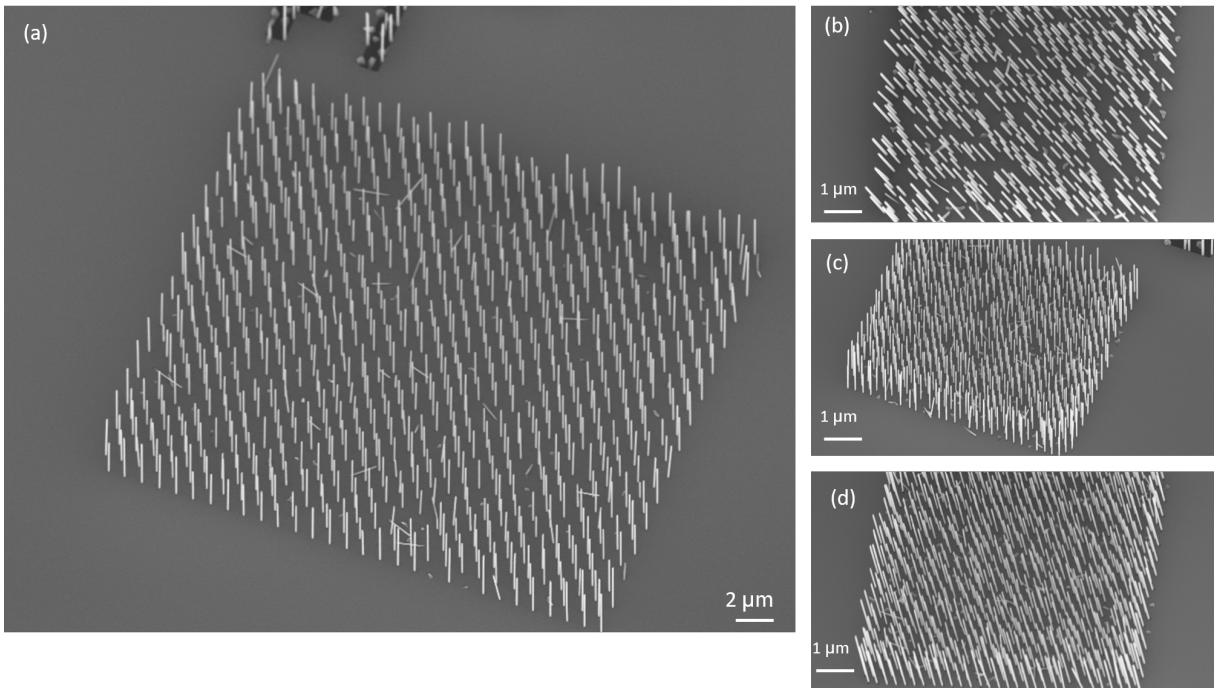

Figure 35: NW array of different hole diameters, (a) 80 nm diameter/pitch 500 nm, (b) 20 nm diameter/pitch 500 nm, (c) 40 nm diameter/pitch 500 nm, (d) 60 nm diameter/pitch 500 nm

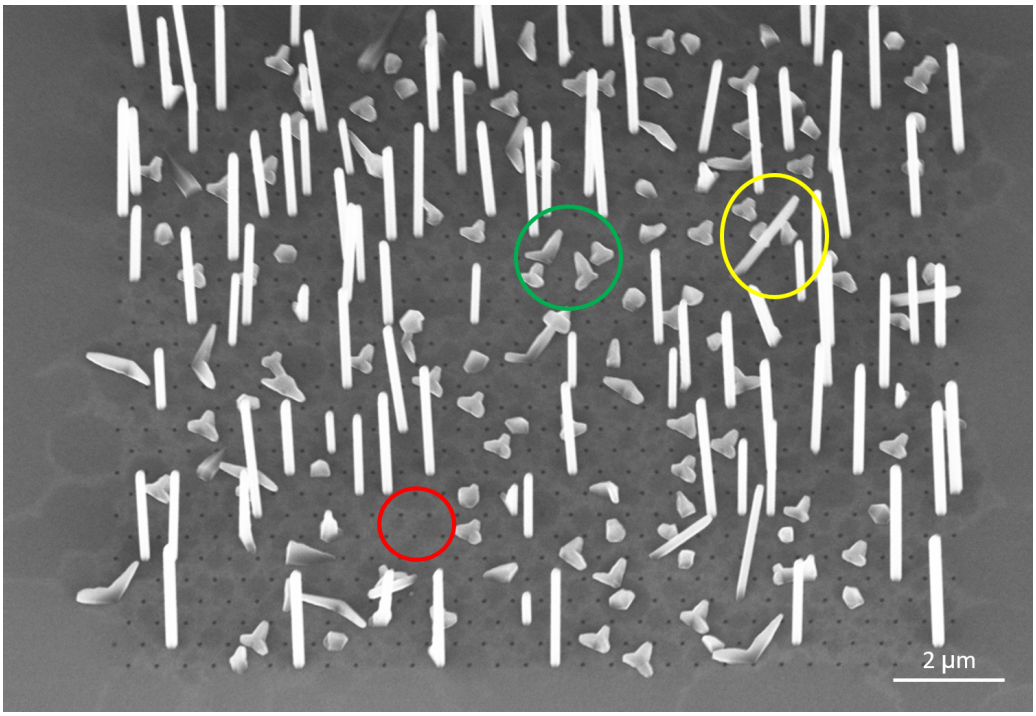

Figure 36: Sample with low NW yield. Marked in yellow are the NWs which are titled, in green are the V- shaped structures and in red are the empty growth holes.

Finally, after incorporating all the factors which are discussed above, the NW yield has increased to 90 % with homogeneous NW morphology, in length and diameter, as seen in Fig. 37.

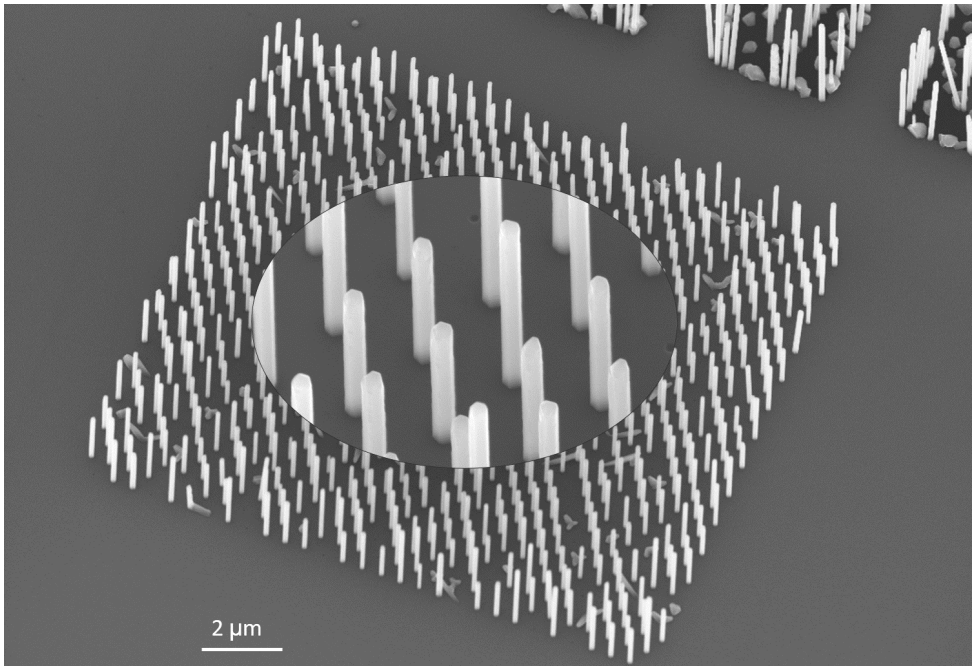

Figure 37: Nanowire array with a yield of 95% grown by using the optimized parameters.

5.4 Si(100) Substrate Preparation

In this section, the different steps of Si (100) substrate fabrication results are analyzed. These substrates have been fabricated to produce InAs NWs on tilted side facets with different superconducting shells, with an in-situ weak-link.

5.4.1 Random Growth

The first method used to check as a proof concept was the random growth, where the the wires are grown in such way that they could possibly cross each other closely and in turn shadow one other during the metal shell deposition. For this reason, a certain geometry is required, where the NWs grow on different Si(111) facets, inclined at an angle. The chosen substrates are Si(100) wafers, when etched with TMAH, Si(111) facets are revealed at angled at 54.7° with respect to the substrate normal. These facets are later used to grow nanowires. Initially the samples are cleaned and covered with 20 nm thermal SiO_2. Then the squares to be etched are written by EBL on the PMMA covered substrate. The EBL design can be seen in Fig. 38. It has four quadrants with different sizes of squares i.e. 2 μm, 3 μm, 4 μm, and 5 μm. These different square sizes are designed to find the optimal square which fits to the nanowire lengths. The squares are then developed and etched by RIE to remove SiO_2 locally. The patterned SiO_2 layer is employed as a dielectric hard mask used for subsequent selective-.area growth.
The Si (100) surface is exposed in the square troughs, as see in Fig. 38(c). However, the large contrast between the squares trough and the surroundings, already depict that, most of the SiO_2 has been etched away. A HF dip around 20-30 s has to be performed before TMAH etching to remove the native oxide. If a HF dip is omitted, the remaining oxide can act as a barrier. This causes non-uniform etching which can be seen in Fig. 39. In contrast to this, the samples etched without any barrier can be seen in Fig. 40. The etched squares are bigger than what is written by EBL which has also been observed in case of growth holes in the

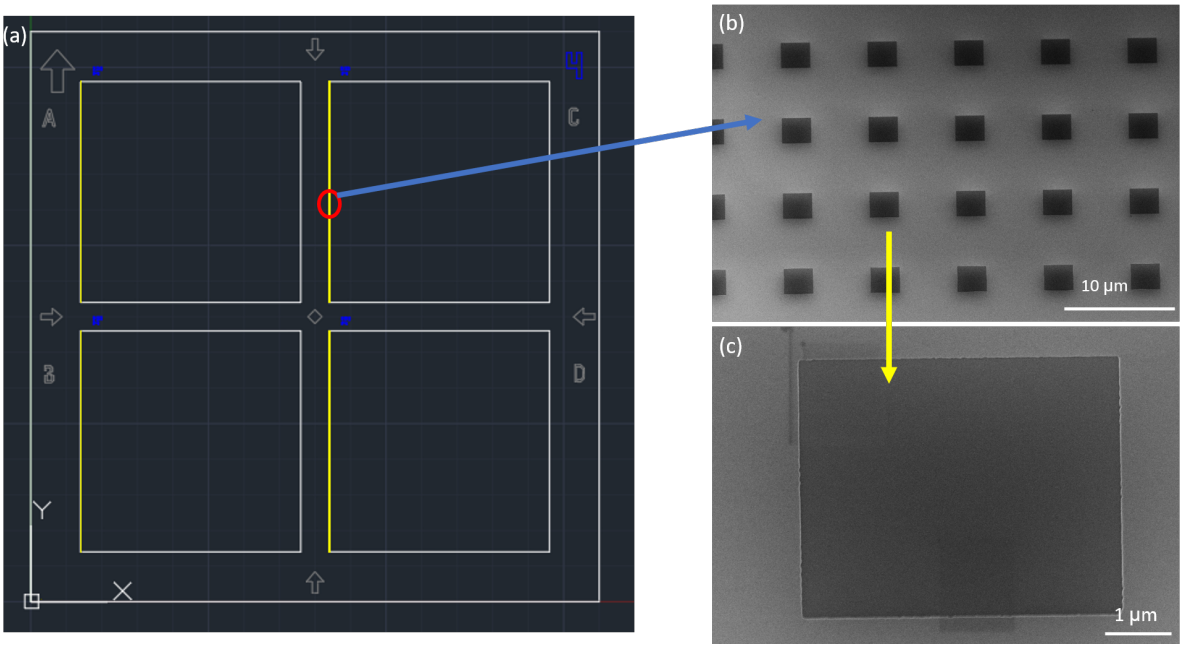

Figure 38: EBL mask with different square sized windows, (a) EBL mask designed for a 2.5 cm mask, four quadrants each with 1 cm x 1 cm dimensions (b) written squares, (c) one of the square etched with RIE. Resist removed, shows a contrast of the SiO_2 removal.

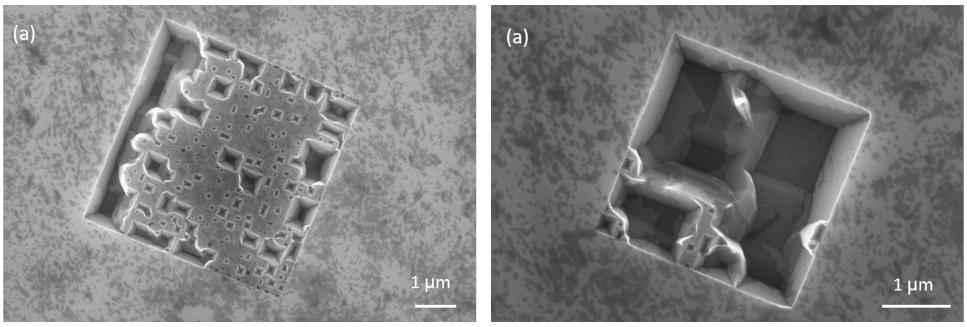

Figure 39: Remaining SiO_2 on the surface acts as a barrier and prevents the TMAH etchant to penetrate through, after 1 min.

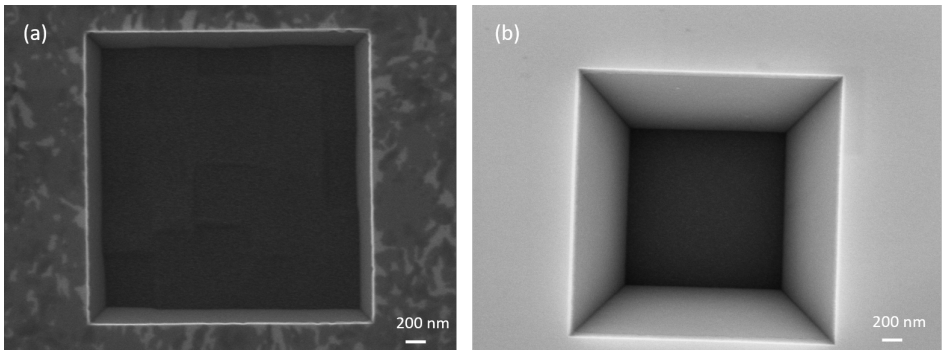

Figure 40: TMAH etching of Si(100) substrate: (a) for 1 min, (b) for 3 min.

previous section. The square with an etch time of 90 s and a corresponding trench depth of 200 nm have been used for this thesis.
A similar technique was used by Gazibegovic *et al.* [33] on InP (100) substrate to create (111)

facets, which are later used to grow nanowires. Khan *et al.* [34] used a similar structuring process on InAs (100) substrates, while Ting-Yuan *et al.* [92] used a similar technique on Si (100) substrates to grow nanowires for silicon photonics. After the trenches with a desired depth are formed, the samples have been treated with H_2O_2 for pin hole creation. The pin holes formed on the Si (111) facets are of irregular sizes and shapes which can cause a variety of structures to grow like nanowires, crystals, titled nanowires, and others. An overview of the random growth of NW on square-patterned structures can be seen in Figs. 41 (a)-(d). These images give an impression on the yield of the shadowed nanowires to obtain weak-linked NW hybrids, in different sized square patterns.

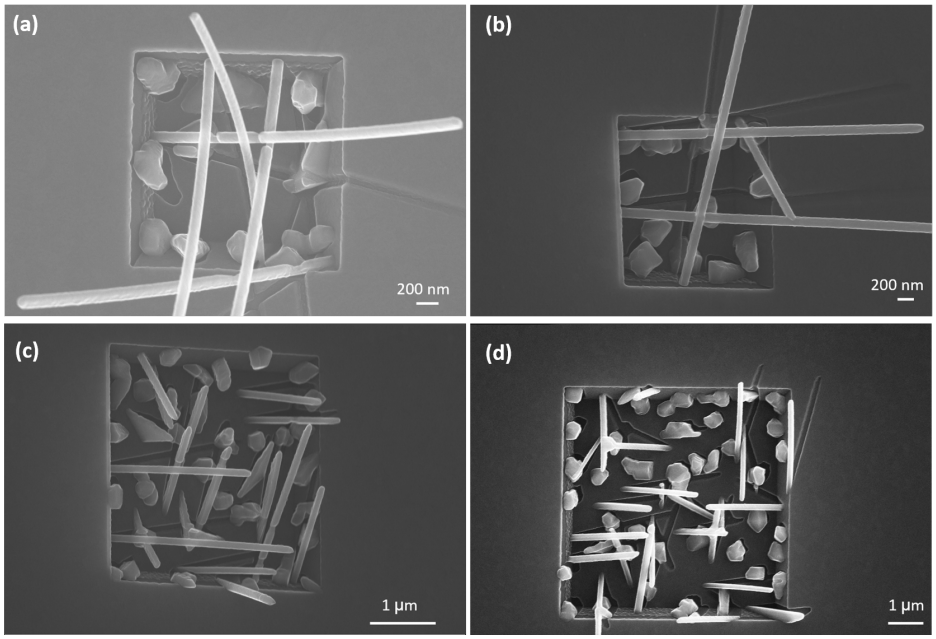

Figure 41: Overview of random growth process on square patterned substrates with different square sizes written by EBL. InAs nanowires, with Nb metal are the depicted nanowires. (a) 2 μm, (b) 3 μm, (c) 4 μm, and (d) 5 μm.

According to the optimized growth parameters, the NW can reach up to 3-4 μm in length. The optimal square size of the trench was found to be 3 μm where the trench contains the largest number of shadowed wires, as shown in Fig. 42. It can be seen here, that the nanowire grow outwards without a directional preference, from all four facets of the square trench and even from below the square, there is no control in such a process. The nanowires grown here have an average length of about 3.5 μm which is larger than the side of the 3 μm squared trench, so the probability of forming the junction is high and the squares yield on an average of 7 junctions out of 5 NWs. This observation was made after surveying several 3 μm squared trenches. There are different possibilities of merging nanowires and several interesting structures can be seen in this process, which can be used as NW networks to observe further interesting quantum effects [93, 94].

5.4.2 Selective Area Epitaxy

The selective area epitaxy method, in fact is an advancement compared to the random growth, since it allows a full control of the in-situ weak-link fabrication. The SAE method is a much more flexible method which eliminates the parasitic growth and increases the probability by

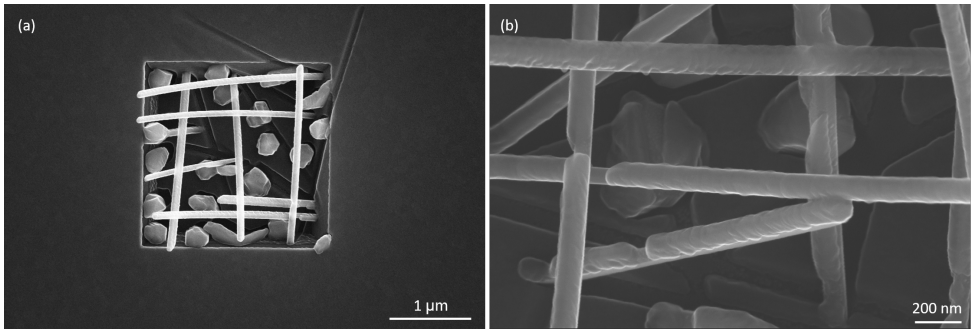

Figure 42: (a) Optimized 3 μm sized square shows, a higher probability of shadowed NWs to obtain Josephson junctions. (b) InAs/Nb Josephson junctions, with an in-situ formed weak-link.

90 % to achieve a uniform and well-positioned, weak-linked InAs NW hybrids. In order to achieve a position controlled growth, the holes are written by EBL, i.e. hexagonal holes which have been discussed in the previous section of Si (111) substrate preparation. The hexagonal holes when written on the angled Si (111) facets result in a slight distortion as an elongated hexagon. These hexagonal holes designed using AUTOCAD can be seen in Fig. 43. The hole on one facet was fixed in the middle whereas the holes on the other facets have been varied with a distance of 100 nm. This is performed to find out which alignment fits, given that the NWs grow at an angle and shouldn't merge with each other but rather cross each other closely. These holes are written on the Si (111) facets, which were etched by TMAH, and then have been been thoroughly oxidized.

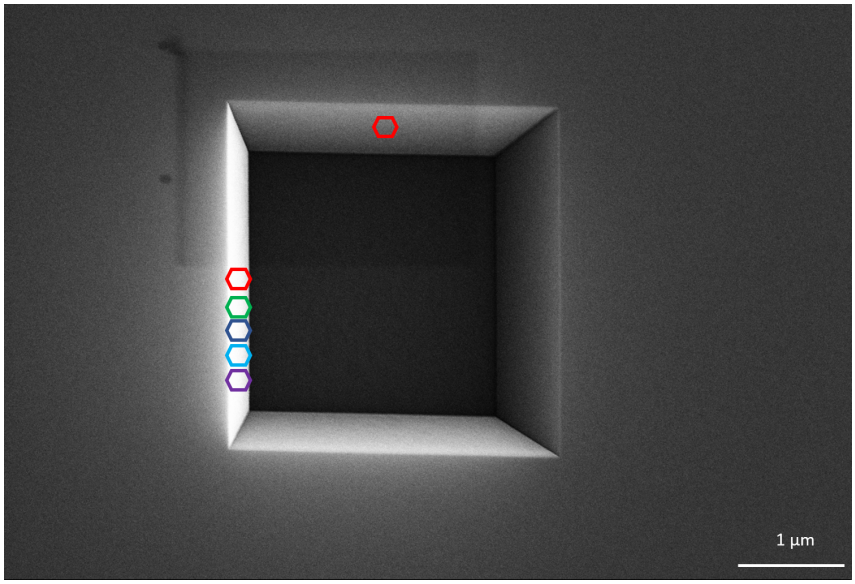

Figure 43: AUTOCAD design of hexagonal holes, with varied distances.

The holes are exposed with several doses ranging from (900-1200) μC/cm^2 along the columns and the NW hole position is varied along the rows. These holes on the Si (111) are aligned with the help of specially designed EBL makers, which can be seen in Fig. 44. Each set of squares are surrounded by three EBL markers, there are several fields repeated on the entire area of the sample.
The holes written on the Si (111) facets are hexagons, and a dose test was performed to determine ideal process parameters, as seen in Fig. 45. The smaller doses expose an uneven

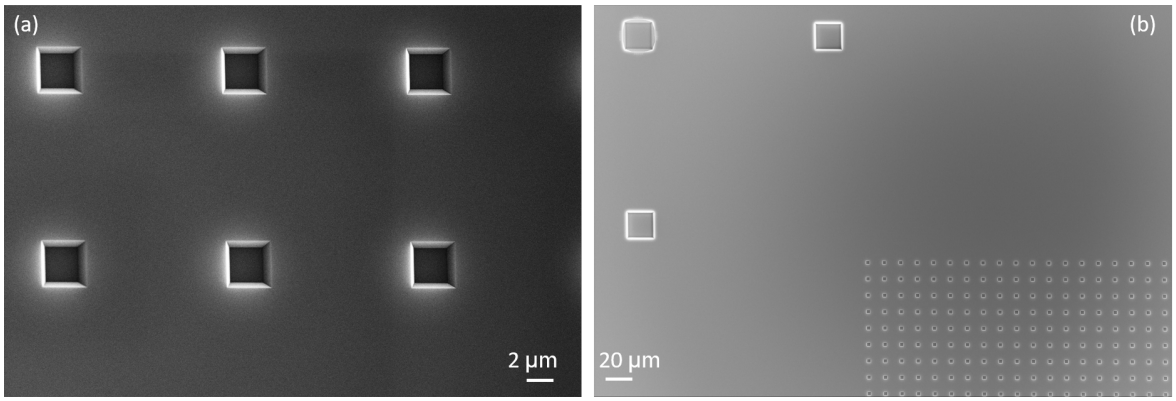

Figure 44: Holes on Si (111) facets, (a) oxidized 3 μm sized squares, (b) EBL markers etched into Si to align the holes.

area of SiO_2 for RIE etching which leads to no nanowire in this hole. Larger holes expose more area for growth, increasing the diameters to 150 nm which could cause two NWs per hole to nucleate. The optimum dose was found to be 950 μC/cm^2 at 100 kV EBL writing.

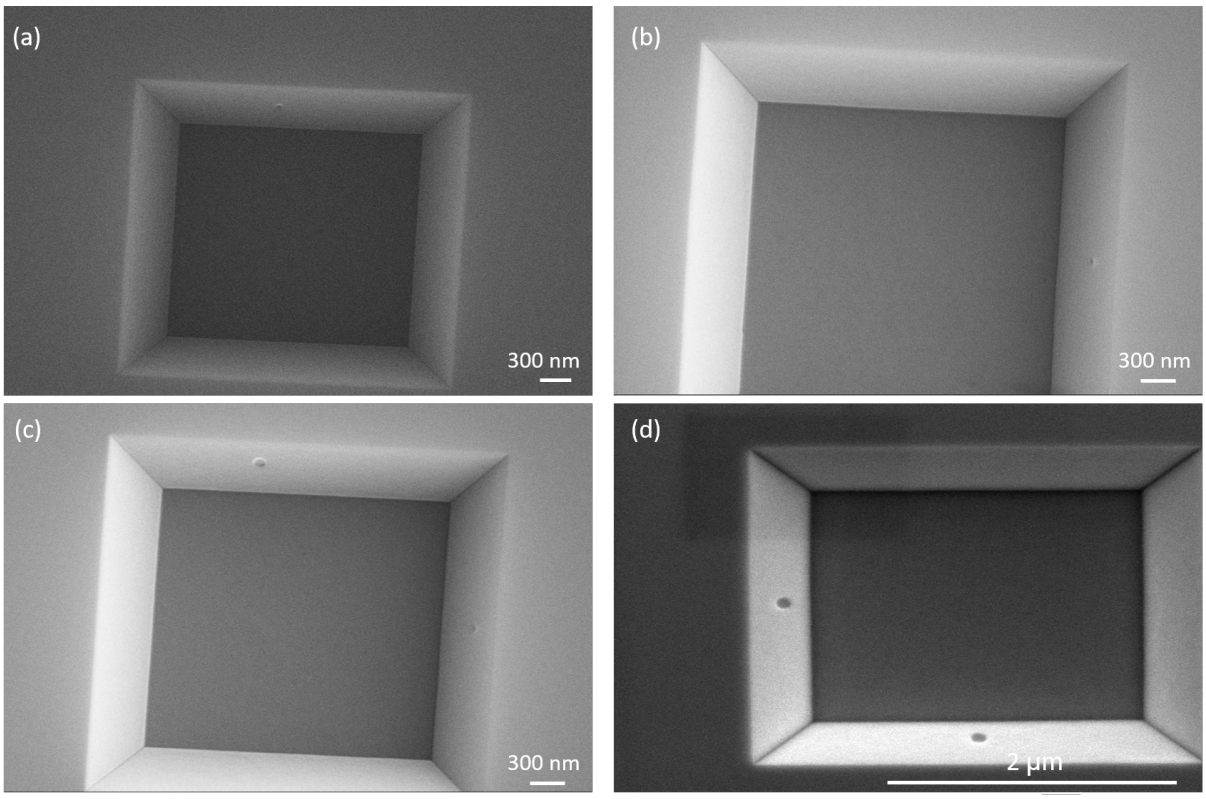

Figure 45: Hexagonal holes written with different EBL doses. (a) 900 $\frac{\mu C}{cm^2}$, (b) 920 $\frac{\mu C}{cm^2}$, (c) 940 $\frac{\mu C}{cm^2}$, (d) 50 $\frac{\mu C}{cm^2}$.

The process of RIE etching is crucial. To asses this effect on the holes written on the tilted Si (111) facets, a FIB cut of the cross-section of these holes is performed, as seen in Fig. 46. The profile of the trench can also be seen. It is visible that the resist layer in black is not conformal on the Si trench, it is thicker at the bottom than at the edges at the top, which is due to the spinning of the resist. The resist thickness for the spin parameters was calculated to be 240 nm

but instead a 120 nm thick layer is found at the bottom of the trench and around 35 nm at the edges. This could cause a potential problem while etching later with HF, because HF tends to lift up PMMA resist during etching. The hole etched through PMMA resist is slanted and etched through well without reaching the Si. This is intentionally designed to leave few nm of SiO_2 for a smooth HF etching later on. The hole etched here has the right diameter and has been developed well and can be clearly seen in the right side image of Fig. 46.

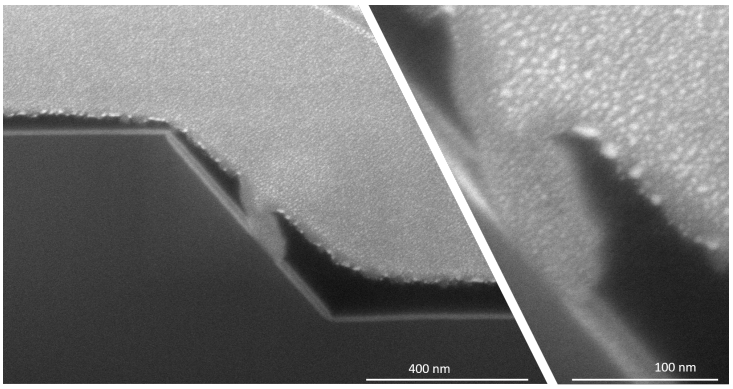

Figure 46: Hole on the Si(111) facet, etched by RIE through the PMMA resist. The thin gray area between the (black) resist and the Si surface is the SiO_2. The image on the right is the zoom-in of the etched hole. Cross-sections prepared by FIB.

The profile of the further etched hole can be seen in Fig. 47, the oxide layer can be identified as the gray coloured film running along the side edge and the metal in the background is Pt used to protect the surfaces while ion milling. An isotropical, HF etching is performed once the resist is removed which can give slight rounded edges to the growth hole. Also a thin film of native oxide can be seen in the right side image of Fig. 47.

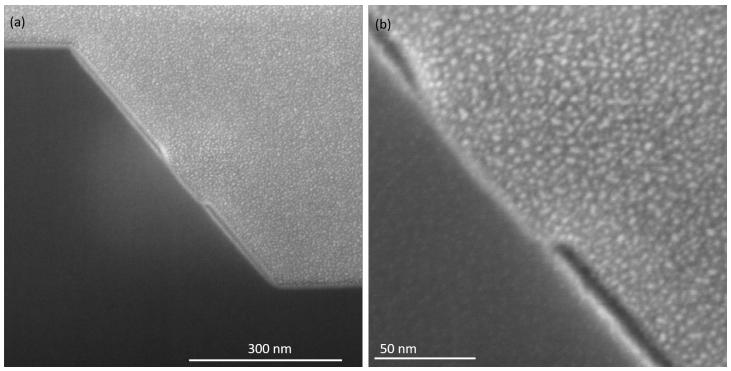

Figure 47: (a) Etched hole after the RIE and HF steps, PMMA is removed. (b) Zoom-in of the hole etched, SiO_2 in black. Cross-sections prepared by FIB.

The first results of the growth can be seen in Fig. 48. The selectivity of the hard mask worsened. It has become porous and a parasitic growth can be seen along the bottom edges of the trench. The parasitic growth seen here can hinder the formation of a perfect NW hybrid with weak-link and is highly undesirable, this caused because the oxide layer is too thin at the bottom edge of the trench, which could have acted as a layer for pinhole formation and further crystal or nanowire growth. Figure 49 shows the corresponding profile of the SiO_2 layer along the square trench. Different thicknesses is expected due to the thermal growth processing parameters where the growth of oxide is different on different crystal orientations

of Si thus forming 23 nm on the Si (111) edges and 16 nm on the top and on the bottom of the Si (100)square. This thickness is observed after RIE etching of the holes and the sample undergoes a further HF dip, which could cause a considerable loss of the oxide, making it thin enough for the NW nucleation during growth.

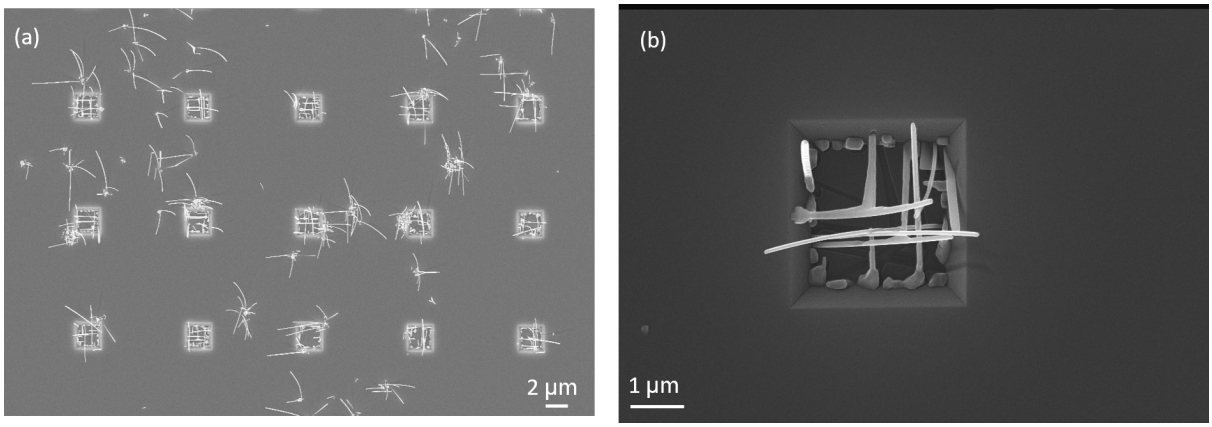

Figure 48: (a) Overview of the SiO_2 mask around the square trenches, NWs nucleate due to thinning of the SiO_2 mask. (b) Overview of the square trenches, where NWs/crystals grow from the bottom edges, due to a thinner oxide.

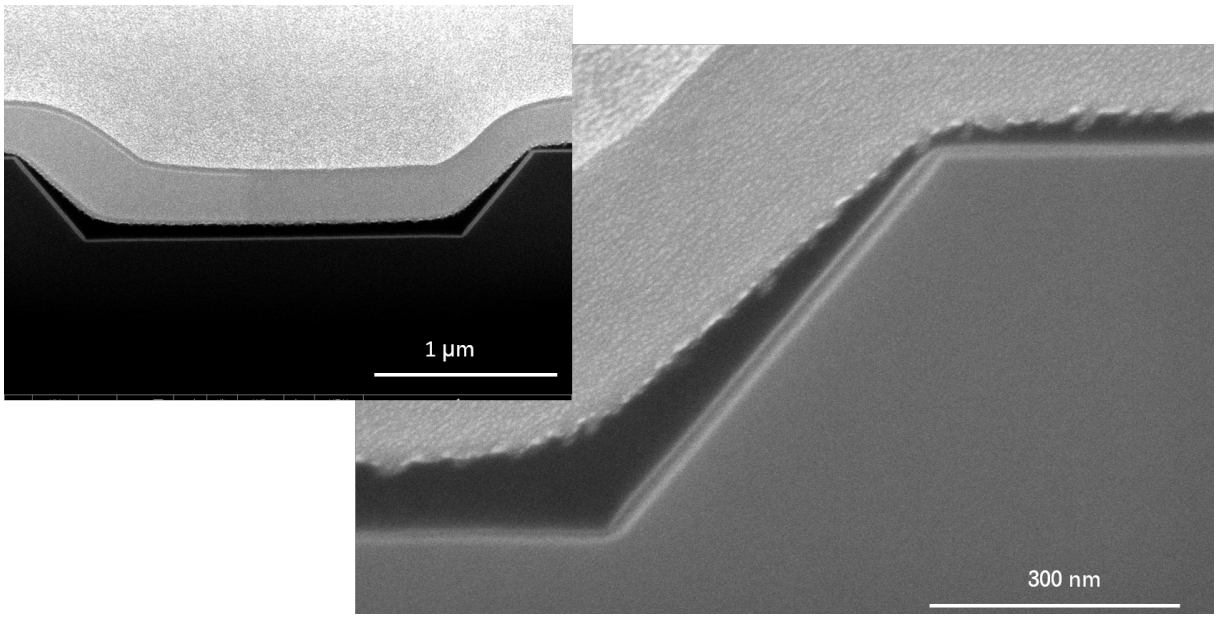

Figure 49: Overview of the profile of the square trench seen in the top left image. The gray overall covering is the Pt (used for protection), PMMA resist in black. On the right, is the zoom-in of the resist coverage along the sides of the square trench. It shows uneven coverage. Resist thinning can be seen, along the top part of the trench. Underneath the resist is the SiO_2 layer that is much thinner on the bottom part of the trench and thicker on the tilted facet of the trench. Thinning on these oxide layers can be seen in the corners. Cross-sections prepared by FIB.

The growth selectivity problem is due to instability of the PMMA resist during HF etching process, it lifts up the resist and causes further unwanted etching of the oxide. This opens up growth windows on the mask, hence the parasitic nanowire growth. This can be tackled by

treating the sample with O_2 before coating the sample with resist to increase the SiO_2 surface polarity and affinity towards PMMA. Further by using a photoresist with an adhesion promoter i.e. hexamethyldisilizane (HMDS) at 130°C. The second problem of the uneven oxide thickness can be tackled by increasing the growth time of the thermal process, which results in 18 nm on the Si(100) surface and 25 nm on the Si(111) surface, this has proven to be beneficial. The corresponding results can be seen in Fig. 50. There is a considerable reduction in the parasitic growth.

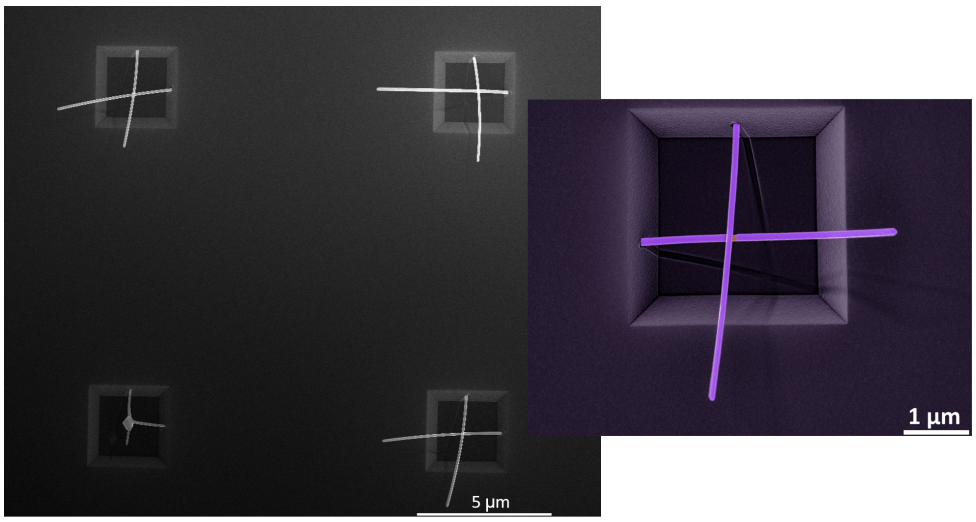

Figure 50: Optimized Si (100) substrates for InAs NW hybrid growth with in-situ weak-link. The yield of these samples is 75 %. The false coloured image on the right, shows a junction.

6 InAs And InAs-Te Doped Nanowires

6.1 InAs Nanowires

In this section, the selective area growth (SAE) of InAs nanowires i.e. on the lithographically patterned Si (111) substrates, using MBE growth technique is presented. Furthermore, the influence of MBE parameters like In growth rate and As flux, growth temperature, growth time, and crystal structure are elucidated here.

6.1.1 Growth Kinetics

Since 1964, there have been an enormous number of experiments of growing nanowires with a gold catalyst [39]. Nevertheless Au has been proven to be incompatible on CMOS platforms, and is also known to cause degradation of the nanowire itself over a period of time. Therefore, we have adopted self-catalyst methods at PGI-9 to grow nanowires. In general, there are two methods to grow III-V nanowires i.e. with and without the use of foreign catalyst. The first one being a self-catalyst method using vapour-liquid-solid (VLS) growth mode [95] where a group III material is intentionally deposited prior to the growth. The second method consists of a VS growth mode, where both III-V materials are constantly supplied, which leads to a crystal growth [50]. In this thesis we have embraced the VS growth mode to grow nanowires under As-rich conditions. Although, it is slightly uncertain to determine how the initial VS growth of InAs nanowires takes place. The studies are not clear, whether the InAs NWs form from an droplet-mediated VLS [96] or a vapor-solid (VS) growth mode [50, 97, 98]. The possible reason could be that even if the In droplets exist during the nucleation, they could have been desorbed or consumed by excess As during the growth. Biermanns *et al.* [99] have also explored the structural composition of the InAs nanowires using in-situ time-resolved X-ray scattering and diffraction measurements during the MBE growth. They have reported presence of liquid indium during the nucleation. It was present for a short time interval during the nucleation phase and was later consumed by the high As conditions. As far as we are concerned, we have also not observed In droplets after the growth, which might have formed during the nucleation phase and have been consumed during the further growth process under As-rich conditions.

6.1.2 Growth selectivity And Vertical Yield

SAE is a position-controlled growth method to grow the InAs nanowires. This method is known to increase homogeneity of the nanowire growth and gives a better morphological control of the grown structures. An important parameter for SAE is the growth selectivity, which critically depends on growth temperature. Growth selectivity is defined as the growth that happens at the predefined patterns and not on the hard mask SiO_2 [83]. The growth performed at a temperature of 480 °C resulted in nanowire formation in the predefined holes. Since, at a substrate temperature of 480 °C, Indium has a high surface diffusion on SiO_2, this resulted in a much lower adatom sticking coefficient of In on SiO_2. Thus, it sticks on Si(111) surface, and the InAs nanowires only nucleated at the etched holes. For our In and As flux parameters, growth temperatures above 500 °C resulted in mere In droplets. The growth temperature of 480 °C, provided an excellent selectivity and a high growth yield. The first optimized

parameters for the InAs nanowires with an In growth rate of of 0.08 μ/h and an As flux of 4$\times$ 10^{-5} torr at 480 °C for a growth time of 2 h resulted in InAs nanowires with average lengths of 1.5 μm and 120 nm in diameter. Most of the nanowires grown using these parameters exhibited a hexagonal-shaped cross-section with (110) facets, similar to those nanowires grown by non-selective method [55]. Apart from these parameters, the yield i.e. the nanowire/hole ratio has to be high for a process to be a fruitful one. Crystallites are one of the major parasitic influences which affect the yield of a nanowire array. One of the causes of the formation of crystallites could be an unevenly etched hole or over-etched hole [96]. A consistent approach of processing the patterns, which includes controlled development times after EBL and a frequent calculation of etch rates of silicon dioxide with RIE and HF is undertaken to take care of the hole diameter consistency. To achieve a high yield of vertical nanowires, a thermal annealing

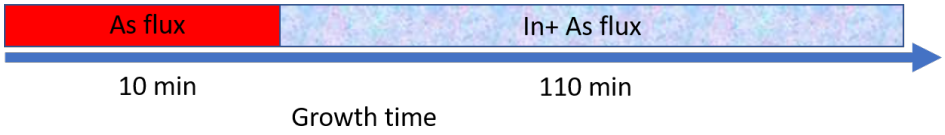

Figure 51: Growth time of InAs nanowires.

of Si substrate is done at 700 °C to obtain a 7×7 reconstruction on Si surface and then prior to the InAs growth, a brief supply of As on Si substrate is performed for 10 min and then the In shutter is opened as well for the growth process illustrated in Fig. 51. The substrate is exposed initially for 10 min to As flux also known as As pre-annealing. Then the group III flux (In) shutter is opened, along with the As shutter for the rest of the growth process for the remaining 110 minutes. The As_4 pre-annealing was initially presented by Tomioka *et al.* to improve the vertical nanowire growth rate [91] by using MOVPE methods. They have reported that an As_4 pre-wetting has a huge effect on the polar/nonpolar nature of the InAs/Si(111), which in turn effects the nucleation of the nanowire, hence its vertical directionality [83]. But given that the As_4 molecule readily desorbs at 250°C, hence As_4 supply at 480°C prior to the In flux supply should not have any influence on the surface kinetics.
Regardless, we have observed the vertical nanowire yield of all performed growth runs to be more than 95%. We have observed that tilted wires and other crystallites are caused by damages in Si (111) substrate. The step which has been crucial is that of RIE etching of the holes, where in CHF_3 gas can etch the Si surface within few seconds. This has been tackled by making sure that the etch time is calculated precisely using AFM measurements and the etching is stopped, leaving 5-6 nm of SiO_2, which is later smoothly etched by a HF. This step tremendously reduced the parasitic growth. An important conclusion here is that a high vertical growth yield depends largely on the crucial parameters like an accurate and reproducible pattern processing, precise etching of holes and less on nucleation conditions. On an other note the selective area epitaxy method has also been used to grow GaAs, that resulted in 40% yield, as can be seen in appendix 9.2.

6.1.3 Influence Of Pitch

In the following section, the morphologies of InAs nanowires grown are investigated. The InAs nanowire configuration, based on the given set of growth parameters substantially depended on the pitch i.e. the distance between any two holes.
In Fig. 52 SEM micrographs of InAs nanowires are shown for different pitches but with a constant etched hole diameter of 80 nm. Here, the lengths of the nanowires have been observed to evolve with the pitch. The nanowire diameters for pitches 500 nm and 1 μm have been varying with a range of $\pm$40 nm. Whereas, for a pitch of 2 μm, there has been only a slight variation in diameter from 125 nm to 132 nm, i.e around 7 nm. In contrast to this, for 4 μm pitches and higher, the nanowire diameters have been constant, at 80 nm etched hole sizes. This can be seen in Fig. 52, where the etched hole diameters have been 80 nm. Hence, the nanowire diameter and the lengths for pitches above 4 μm, have been found to be independent of the pitch [77, 82, 100].

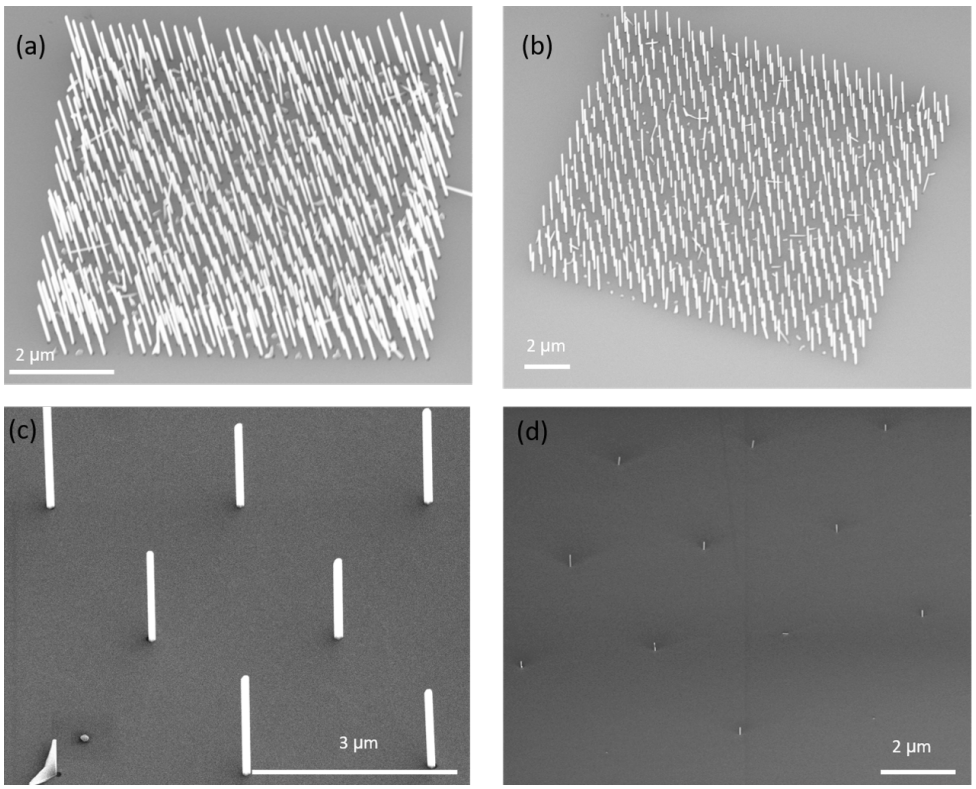

Figure 52: Nanowires grown on different pitches: SEM micrographs of 30° tilted substrate with nanowires (a) 500 nm pitch (b) 1 μm pitch (c) 4 μm pitch (d) 30 μm pitch. The diameters and the lengths of the nanowire become more uniform with the increase in pitch.

Figure 52 (a) and (b) shows the nanowires with 500 nm and 1μm pitch. Nanowires in these pitches are known to be in the competitive regime. Figure 52 (c) and (d) the nanowires here seem quite uniform for larger pitches, depicts a diffusion limited regime. In the competitive regime, nanowires have a pitch that is less than or in the order of 2$\times$ diffusion length of In adatoms [77, 83]. Thus, the nanowires during the growth compete with the neighbouring atoms, which reflects on the nanowire growth rate along the axial and radial directions [101]. Whereas, in the diffusion limited regime the pitch is two times greater than the diffusion length of In adatoms, and the nanowire growth is independent on the neighbouring growth.

This causes a uniform growth among all the nanowires [82]. Bearing all this in mind, the further fabrication of the samples have been optimized to 4 μm pitch size and 80 nm hole diameter, to achieve greater uniformity.

6.1.4 Effect Of In And As Fluxes

The growth of InAs nanowires is performed via VS growth mode. The growth is limited by In atoms and very low indium fluxes affect the nanowire diameter and higher fluxes of indium favour crystallites rather than nanowires [55]. The In growth rate was varied between 0.06-0.08μm/h. It has been found that growth rate of 0.08μm/h is optimum w.r.t to the diffusion lengths in this growth. The As BEP was kept constant at 4×10^{-5} torr and the growth time for 2 h. The SEM micrographs in Fig. 53 shows the impact of In flux on the nanowire growth.

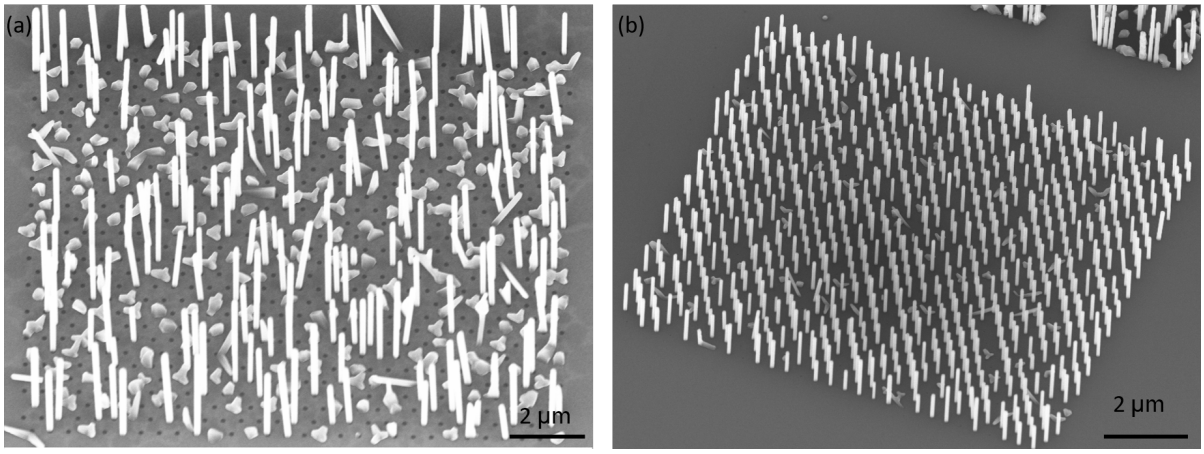

Figure 53: SEM (30° tilted substrate) micrographs: growth of InAs nanowire growth (a) 0.06 μm/h of In rate (b) 0.08 μm/h of In growth rate.

Figure 53 clearly shows the impact of the In flux. With a 0.06 μm/h In rate, there are crystallites and the nucleation of In in the holes is very much limited and the resulting yield is around 25%, which is inadequate. The group III element in the nanowire growth is a sticking element in comparison to the As. Thus, with reduced In growth rate the nanowire density, length, and the diameter decrease linearly. A consistency in the length and diameter of the InAs nanowire have been observed below 0.1 μm/h of In rate at the given substrate temperature and As flux. It has been observed that at 0.08 μm/h of In flux, the yield of nanowires increased to 95% (see Fig. 5.40 (b)). This is the result of the right combination of the substrate temperature, As flux and 1 μm diffusion lengths of the In atoms which cause nucleation in every hole. The right III-V ratio causes an axial growth of the nanowires. At higher In fluxes of 0.1 μm/h, the growth of crystallites have increased and the nanowires became thicker due to more material availability at the adatom capture area.
The As flux is responsible for the axial growth of a nanowire. A low As supply means an In rich environment, which favours the growth of crystallites rather than nanowires. Figure 54 shows the effect of the change in As BEP on the nanowire growth at a fixed growth temperature of 480°C, and an In rate of 0.08 μm/h. Figure 54 shows the effect of As BEP on the nanowires (a) initial In growth rate of 0.08 μm/h for 10 min and later changed to a lower rate of 0.03 μm/h for 110 min with an As beam equivalent pressure (BEP) of 2.5 $\times10^{-5}$ torr. In contrast, Fig. 54 (b) depicts a clear and distinct axial growth with a higher As BEP of 2.5 $\times10^{-5}$ torr. The

nanowires in the latter case, have resulted in longer nanowires, this is due to higher diffusion of As atoms along the wire length, supporting the axial length [83].

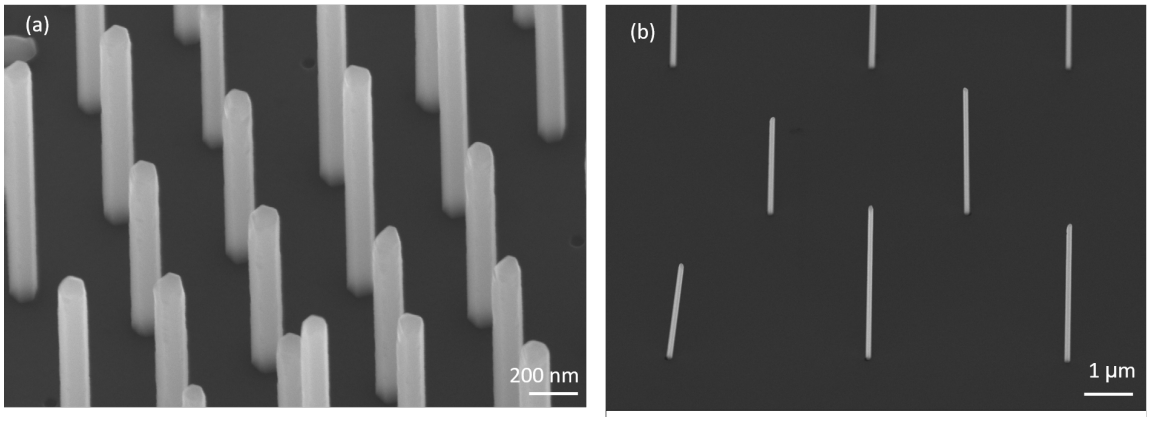

Figure 54: SEM micrographs: nanowire grown with different As_4 fluxes. (a) As flux of 2.5 $\times 10^{-5}$ torr (b) As flux of 3.5 $\times 10^{-5}$ torr.

For higher As BEP $> 2.5 \times 10^{-5}$ torr, the nanowires grown on the larger pitches of 2μm and 4μm exhibit slightly higher growth rates when compared to the 500 nm pitched ones. A decreased diameter for higher As fluxes has also been observed. This can be attributed to an enhanced sidewall diffusion of In adatoms under high III/V ratios [83]. For high As fluxes, a low nanowire diameters of 65-70 nm was noticed. It also has to be noted that at a certain As flux the growth kinetics limit the nanowire diameter. The change in fluxes during the growth, could essentially cause tapering in the nanowires but this has been suppressed due less In adatom incorporation at the bottom facets (110) of the nanowire.

6.1.5 Morphology and Crystal Structure

The InAs nanowires growth by self-seeded VS growth method have a hexagonal morphology, with facets belonging to (110) family. Figure 55 shows the top view of the InAs nanowires, where in tilted nanowires, mostly hexagon nanowires and very few irregular hexagons is depicted. In the inset an irregular hexagon can be seen clearly, with concentric rings on top. This is the top of the wire with a rounded rough shape, caused due to abruptness of the stoppage of the growth process [102]. These wires are grown initially with In rate of 0.08 μm/hr and with an As BEP of 4 $\times 10^{-5}$ torr for about 10 min and later switched to lower fluxes i.e. In rate of 0.03 μm/hr and an As BEP of 3 $\times 10^{-5}$ torr to achieve 70-80 nm nm thin nanowires. It has to be noted that there has been changes in the fluxes which could cause a slight tapering at the bottom end of the nanowire. One possible explanation to the irregular hexagon shapes is that they are mostly likely caused when one (110) facet grows faster than other the other, in high III/V ratio environments. Uneven accumulation of group III and group V atoms could be a major source for irregularities in the facet formation which in turn causes variations of surface diffusion of the atoms [83, 103].
Bulk InAs has zincblende (ZB) structure, which is cubic structure with a layer stacking sequence of ABCABC [104]. For the InAs nanostructures, grown on Si (111), it crystalizes in wurtzite (WZ) structure. Wurtzite has has a hexagonal close packed (hcp) structure with ABAB layer stacking [83]. This can be seen in the TEM images in Fig. 56 of InAs nanowires.
To analyse the crystal structure the InAs nanowires, they are smeared off a Cu grids for TEM analysis. The TEM micrographs depict a heavily disordered InAs nanowire crystal with

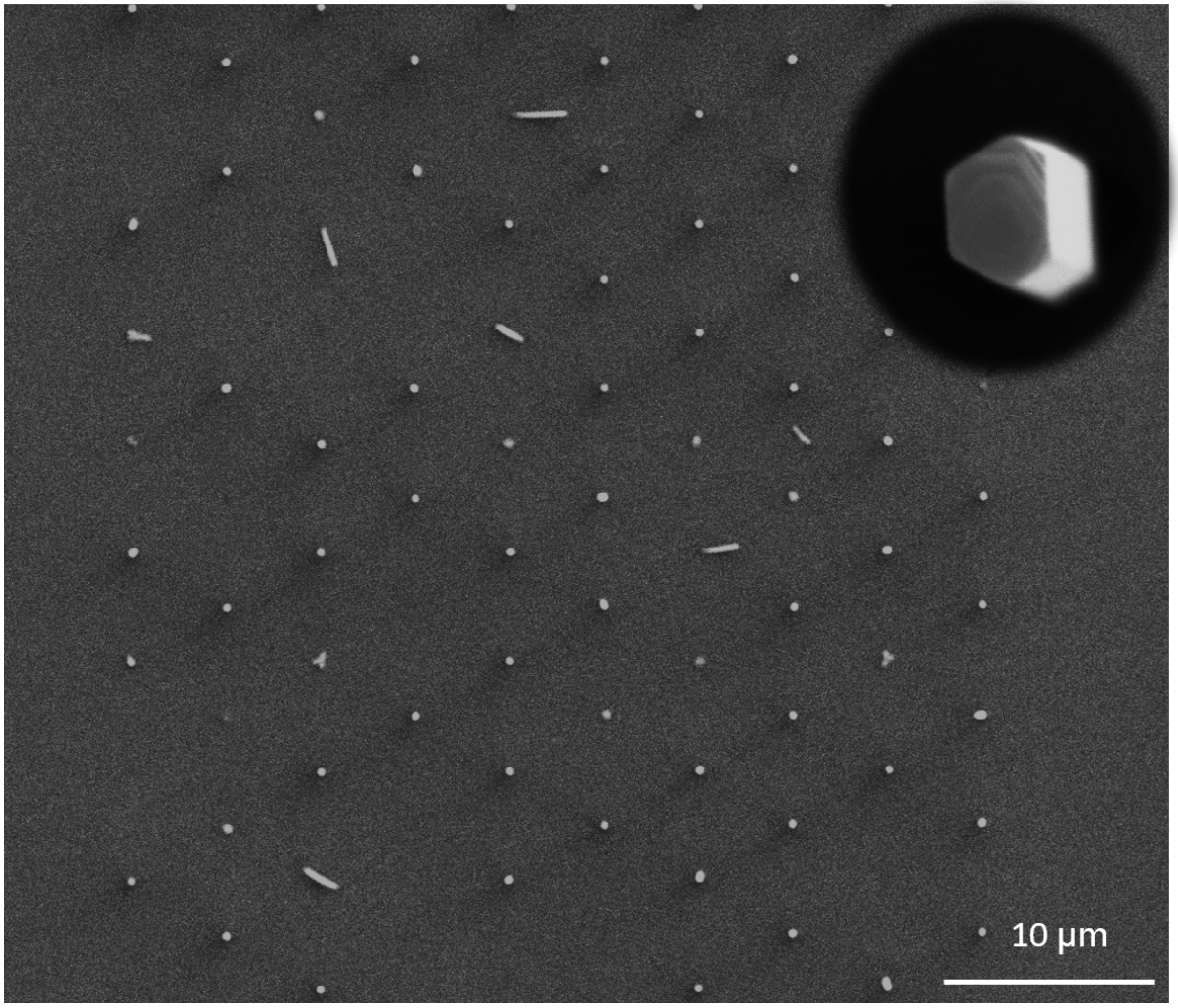

Figure 55: SEM micrographs of top view of InAs nanowire in an array, tilted nanowires can be seen, top-facets are hexagons, irregular hexagons can be seen in the inset.

repeated stacking faults. In the TEM micrographs on the left of Fig. 56, the stacking faults and the other defects occur in different contrast (stripes). The crystal structure of InAs can be seen on the right of Fig. 56 where the wurtzite and ZB stackings are marked. There two ZB types can be seen which are relatively rotated also known as rotational twins. Improvements to the InAs nanowire growth are possible. Biermanns *et al.* [99] have reported that, after the nucleation process, the nanowires grow without liquid indium, hence it starts out as a VLS growth and turns to VS growth later. This results in nanowires with a defective wurtzite crystal structure with densely spaced stacking faults. Hence to improve the crystal structure, InAs nanowires are shown to grow with In droplet Rieger *et al.* [105] have demonstrated that the crystal structure includes larger wurtzite inclusions, and demonstrated a superlattice growth of InAs. Grap *et al.* [106] have reported similar results. This in fact proves that the highly disordered crystal structure could be improved by a controlled inclusion of In droplet in the VLS growth mode.

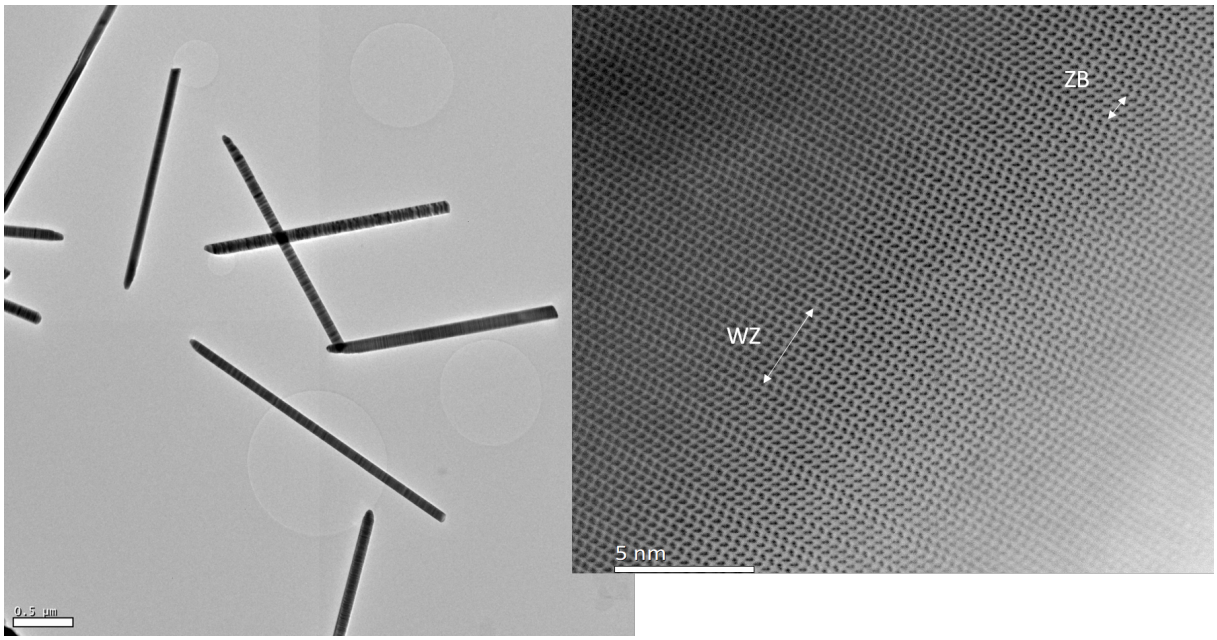

Figure 56: TEM micrographs of InAs nanowires, the whole wires can be seen with different contrast and the rings are stacking faults and the right image is the STEM micrograph of the center of the nanowire showing the crystal structure.

6.2 Tellurium Doping

In this section, results of in-situ Tellurium (Te) doping of VS grown InAs nanowires by MBE is presented. Tellurium dopants are incorporated via evaporating the gallium telluride (GaTe) cell. Indium, arsenic, tellurium shutters are opened simultaneously for 3.5 h to grow InAs-Te nanowires. The effect of doping on the morphology of the nanowires is discussed with the help of scanning electron microscopy (SEM) and atom probe tomography (APT). The increase in conductivity of the nanowires is presented by means of low temperature electrical measurements. The results presented this section have been published in [107].
Tellurium belongs to group VI, indium belongs to group III, whereas arsenic belongs to group V. Hence tellurium is an n-type doping. Correspondingly, the chemical properties of Te are closely related to As than In, thus it is known to occupy As sites in the zinc blende lattice [108]. Tellurium atoms add free electrons to the nanowire, thus pushing the Fermi level towards the conduction band. This increases the number of charge carriers in the channel, there by increasing the conductivity. The nanowires were grown with different doping concentrations. The concentration has been varied by means of the GaTe cell temperature. The substrate temperature is 480°C, In growth rate is 0.08 μm/h and an As, beam equivalent pressure (BEP) of 4×10^{-5} torr for for the first 10 minutes. Later on the GaTe cell shutter is also opened. The nanowire growth is then proceeded with In growth rate of 0.03 μm/h, with a varied As BEP is between 3-3.5 $\times10^{-5}$ torr for 3.5 h to grow the nanowires, with the optimized parameters from the previous section. Arsenic BEP is varied depending on the doping concentration to negate the surfactant effects of the Te incorporation [109]. The first results of these wires with a Te-dopant concentration of 1×10^{-18}cm^{-3}, can be seen in Fig. 57. The Te dopant concentration is varied each time, so is the As flux. Tellurium incorporation is known to increase the diameter and decrease the axial length of the nanowire. This trend was also reported previously for Te doped GaAs nanowire as well as Si doped InAs nanowires [55, 110, 111]. To counteract this effect, As flux was tuned in accordance to the dopant concentration to obtain the nanowire with desired dimensions. An increase in arsenic flux is known to diffuse the In atoms along the axis of the wire.

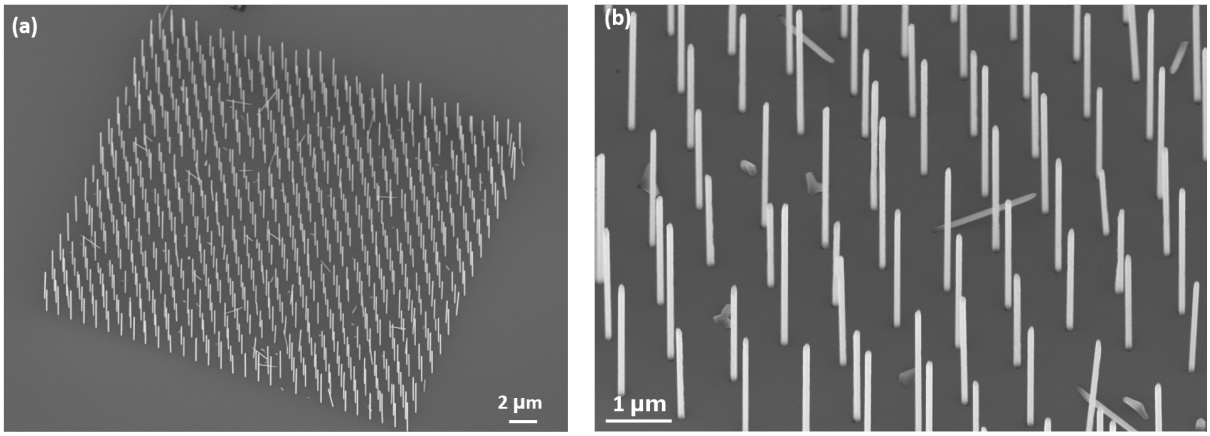

Figure 57: SEM micrographs of InAs- Te doped nanowires growth selectively with a Te concentration of 1×10^{-18}cm^{-3}. (a) The nanowires grown in 80 nm wide holes and 1μm pitch, shows uniformity in length and diameters. (b) Closeup of the nanowires shown in (a).

The parameters of the in-situ doped samples with tellurium are summarized in table below 2. The concentration of the dopants are varied and correspondingly the As flux has been

increased and the nanowires are grown for 3.5 h. Figure 58, shows the resultant nanowires from different growth runs. Sample 6 resulted in an average increase in diameter of about 51% when compared to sample 1 and about 40% decrease in length. In Fig. 58 (d), it can be clearly seen that at a doping range of 2.5 $\times$ 10^{-19}cm^{-3}, i.e. sample 6 has developed additional [211] facets (seen as streaks along the wire). These additional facets are caused due to tellurium incorporation into the nanowire. One possible explanation is that Te atoms increase the lattice parameter of the crystal structure. In conclusion, increasing the doping concentration result in an increase of the diameter and a decrease in the axial lengths of the nanowires [112–115]. This important observation, has also been supported by atom probe tomography analysis in the next section. Formation of additional facets, causes the nanowire to switch from a hexagonal to dodecagonal structure. In Fig. 58 (c), sample 5 has unstable facets.

Sample no.	Te doping conc. (cm^{-3})	GaTe cell temperature (°C)	As flux (torr)
A	undoped	-	2.5×10^{-5}
1	5×10^{17}	420	3×10^{-5}
2	1×10^{18}	437	3×10^{-5}
3	5×10^{18}	478	3.5×10^{-5}
4	7.5×10^{18} (GaSb shell)	489	3.5×10^{-5}
5	1×10^{19} (GaSb shell)	497	3.5×10^{-5}
6	2.5×10^{19} (GaSb shell)	520	4×10^{-5}

Table 2: Overview of the InAs nanowires with different concentrations of Te dopants.

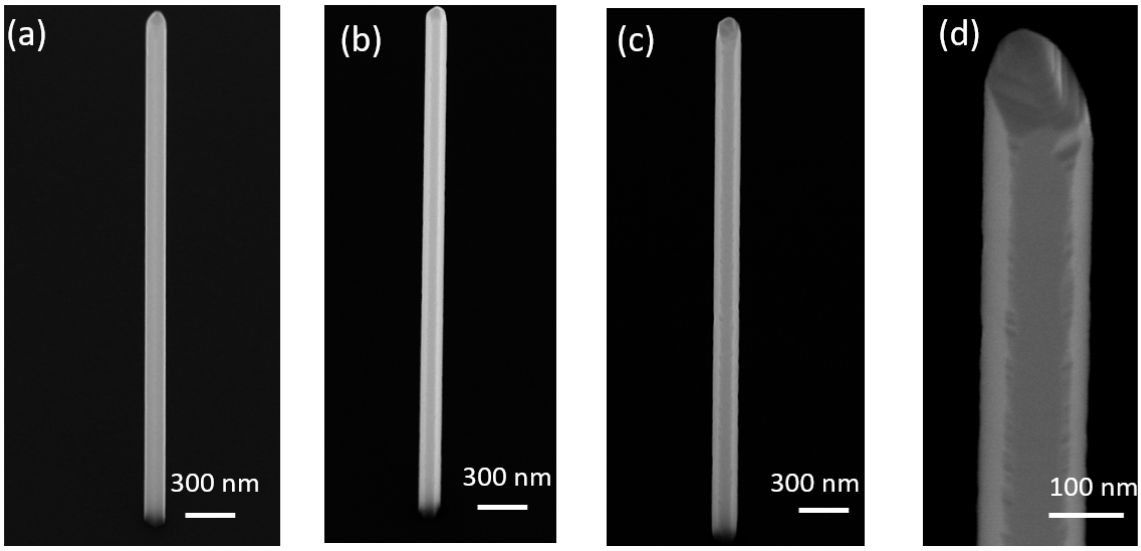

Figure 58: SEM micrographs of InAs nanowires grown with various Te concentrations. (a) Sample 2, with Te conc. of 1 $\times$ 10^{18} cm^{-3}. (b) Sample 3 with Te conc. of 5 $\times$ 10^{18} cm^{-3}. (c) Sample 5 with Te conc. of 1 $\times$ 10^{19} cm^{-3}. (d) Sample 6 with Te conc. of 2.5 $\times$ 10^{19} cm^{-3}, [211] facets can be seen clearly.

Tellurium atoms have a large covalent radii and tend to diffuse slowly and further suppressing the diffusion of the host indium atoms. This behaviour is identical to that of antimony. InAs(Sb) nanowires showed similar behaviour, besides Sb effect was much less pronounced than Te itself [116–118]. This is caused due to the surfactant effect of Te atoms. Furthermore, an increase in arsenic flux, did not influence the Te dopant effect, beyond a Te concentration of $1 \times 10^{19}\,\mathrm{cm}^{-3}$.

6.2.1 Atom Probe Tomography Analysis

Atom probe tomography (APT) analysis has been performed on these samples. Only samples with Te concentration greater than $5 \times 10^{18}\,\mathrm{cm}^{-3}$, could be used since the setup limits the detection concentration. Samples 4, 5 and 6 from table. 2 have been used for the analysis. Here, the atoms are evaporated into ions by using an electric field. Impurities at ppm level could be detected and mapped. APT is a well-established method, used for semiconductor nanowires, to observe the doping concentrations. The first procedure involves isolating the nanowire and making a target. First a dummy wire is picked by a manipulator in an SEM, which is then used to pick up the target wire. Later, both wires are transferred to a Si post. Eventually the dummy wire is broken off. Hence, the target wire remains attached to the Si post. Ultimately, the target wire is evaporated using an electric field and tomographed, as seen in Fig. 59.

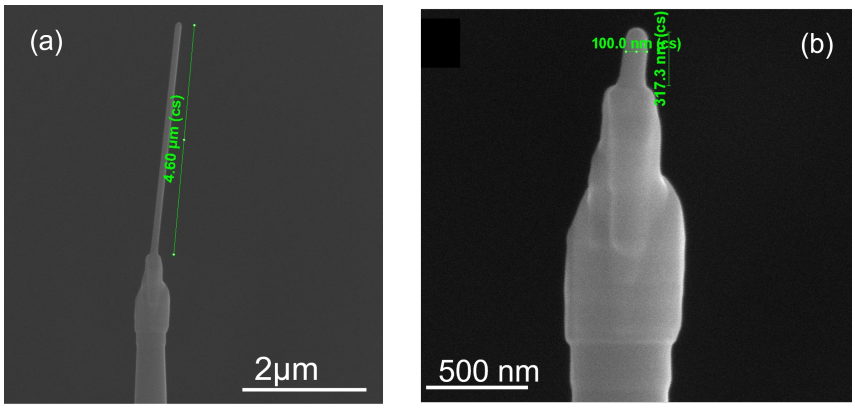

Figure 59: (a)Target wire together with the dummy are transferred to a Si post and the dummy is broken off, leaving the target wire attached to the Si post. (b) The evaporation of the nanowire performed, from the top of the nanowire and tomographed [119].

After the nanowire sample is attached to the Si post, a voltage is applied between a tip-shaped sample and an electrode creating an electric field of 10 V/nm on the tip surface. Subsequently, a laser pulse temporarily heats the apex of the sample allowing for the removal of ions from the surface by the electric field. Thereon, the ions are accelerated and projected from the tip-surface onto a position sensitive single ion detector using an electric field. Thus, the time-of-flight and the impact position of the ion on the detector are recorded. This data allows to reconstruct a 3D atomic model of the sample [119]. A schematic illustration of the setup is depicted in Fig. 60.
The atom probe tomography set-up was able to detect, doping concentrations that are higher than $5\times\ 10^{18}\,\mathrm{cm}^{-3}$. Hence, the samples prepared for the analysis used in this chapter are, $7.5 \times\ 10^{18}\,\mathrm{cm}^{-3}$, $1\times\ 10^{19}\,\mathrm{cm}^{-3}$ and, $2.5\times\ 10^{19}\,\mathrm{cm}^{-3}$. The first results of the APT analysis, can be seen in Fig. 61 (a). Figure 61 (a) is a 2D map of the nanowire radial surface, of InAs

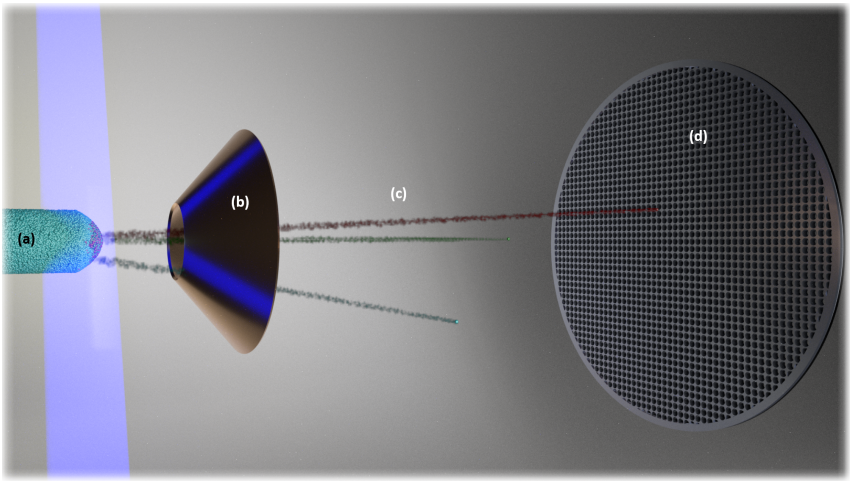

Figure 60: (a) Nanowire sample, attached to the Si post, ions being projected on to the electrode. (b)Electrode, gathering the ions by means of the electric field applied. (c) Ions are accelerated towards the position sensitive single ion detector. (d) Detector that gathers the information about the the time-of-flight and the impact position of the ion.

nanowire with a doping concentration of $1\times\ 10^{19}\,\mathrm{cm}^{-3}$. The reconstructed data, does not include the entire wire, rather a middle region. The size of the detected region is fixed (solid angle) and hence a certain percentage of the diameter of the tip (≈50-60%) was only detected and reconstructed. This problem could be fixed by taking an InAs nanowire with a 50 nm thick GaSb shell. Figure 61 (b) shows the corresponding APT image. It provides a complete picture of the dopant profile. The red marked hexagon in Fig.61 (b) is the InAs nanowire core and the circular dashed lines (marked) is the expected field of view of the nanowire without shell. In Fig. 62, it is quite evident that the evaporated atoms that are projected onto the detector are limited. This is due to the shadow of the electrode. This causes the ions at the edge to fly past the detector. Hence they are not detected. Thus, the reconstructed data comes only from the middle region of the sample. To overcome the detection problem, all the samples are grown with GaSb shell of 50 nm for the APT analysis.
Sample A, 4, 5, and 6 nanowires with GaSb shell have been used for the APT analysis and the corresponding 2D radial maps of the core and the shell have been tomographed. The nanowire for this analysis has been analyzed, radially, throughout the entire wire and thus the Te atoms evaporated are detected and re-constructed. The samples have been presented with comparison to an undoped core-shell nanowire, as seen in Fig. 63 (a). It can clearly be seen in Fig. 63, (b), (c) and (d), that the Te doping concentration increases with increase in the GaTe cell temperature i.e. w.r.t to the nominal doping. The Te dopant concentration is mapped along the radius of the nanowire, here the pixel sensitivity is plotted, and is converted to the Te conc.% ($1\ \times\ 10^{-4}$= 0.01 %). It can be observed that the, Te atoms tend to accumulate at the inner corners of the hexagonal (111) facets, thus developing lateral (112) facets. One possible explanation of this accumulation at the inner corners is attributed low energy, further in-situ growth studies with TEM is necessary to shed light on the Te dopant profiles. Further on, the majority of Te atoms are concentrated in the middle of the nanowire. This clearly shows that the dopant incorporation is inhomgeneous. The entire nanowire, with the shell has been analyzed. The atoms are evaporated beginning with the top and proceeding to the bottom of the nanowire. Te concentration levels for samples 4, 5, and 6 are presented in Fig. 64. The core-shell nanowire on top of the figure is re-constructed by APT analysis. The

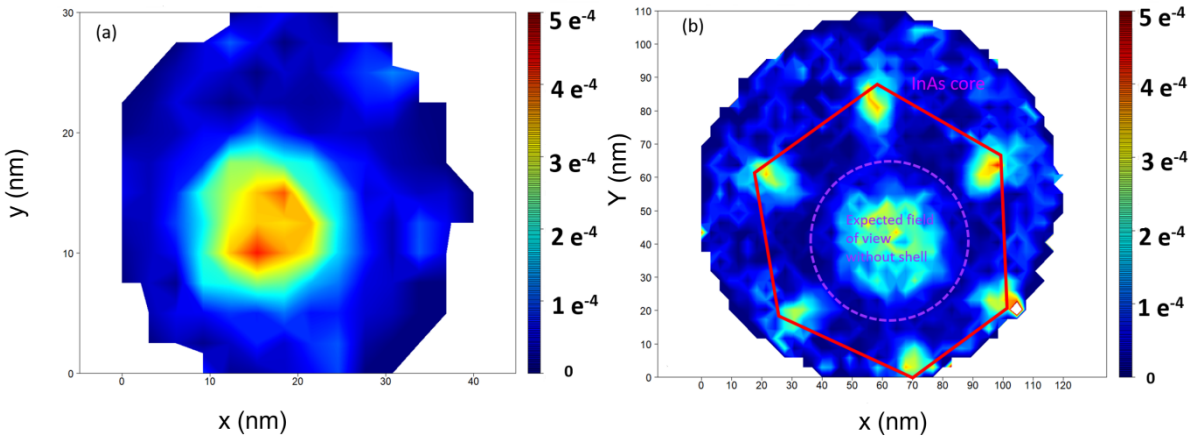

Figure 61: Two-dimensional radial maps of InAs-Te doped nanowire with te concentration of $1\times 10^{19}\,\mathrm{cm}^{-3}$. (a) Without GaSb shell, the Te conc. is only detected in the middle of the nanowire. (b) With GaSb shell, shows the complete Te doping profile. The red marked hexagon is the InAs nanowire core and the circular dashed lines (marked) is the expected field of view of the nanowire without shell.

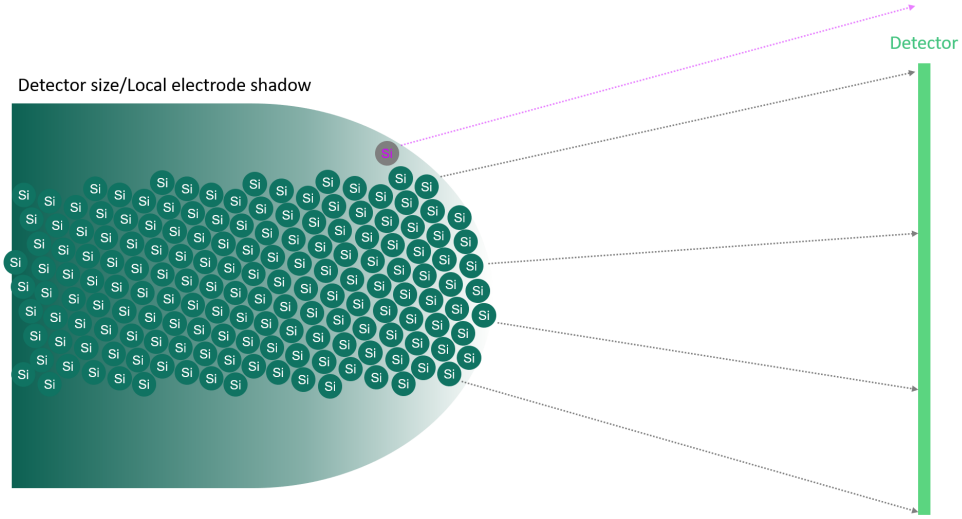

Figure 62: Schematic of the APT setup shows the shadowing of the electrode, on the nanowire that is being evaporated, shows the inner atoms being projected onto a detector, and the outer atoms flying away.

arrows shows the direction of the evaporation of the nanowire. It can be seen distinctly that the Te concentration increases with the corresponding nominal doping. Sample 4 and 5 have a Te concentration, that is almost similar. The Te atom concentration varies by a factor of 2 to 3 along the length of the nanowire. Tellurium atom concentration is higher at the bottom of the nanowire, which is due to the surfactant property of Te adatoms. The corresponding Te concentration values have been deduced from the Fig. 64. The unit cell structure of the InAs nanowire, has been approximated as wurtzite, with a-lattice parameter as 4.2742 Å and c-lattice parameter as 7.0250 Å with 5 atoms in the unit cell [120]. Furthermore, it has been calculated, that InAs has 3.89×10^{22} atoms/cm^3. This has been further multiplied by

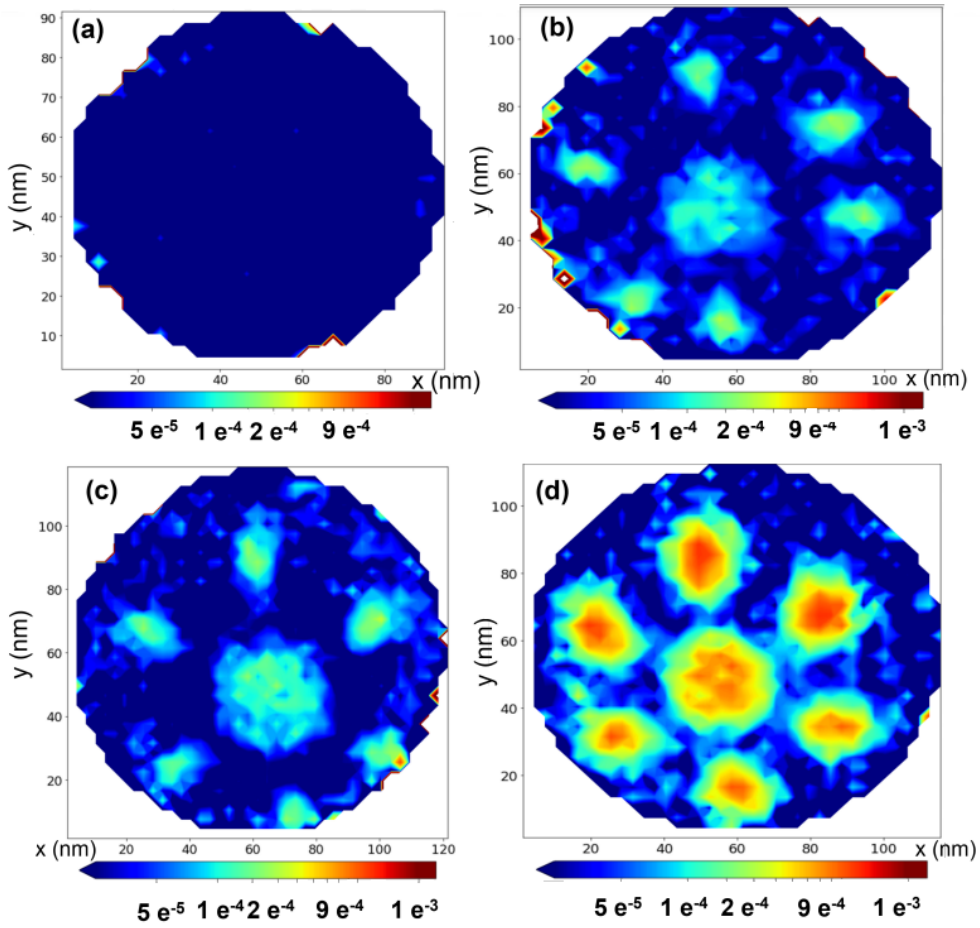

Figure 63: 2D radial maps of the InAs nanowires (a) InAs nanowire with GaSb shell, with no Te doping. (b) InAs nanowire with GaSb shell, with Te conc. of $7.5\times\ 10^{18}\,\mathrm{cm}^{-3}$. (c) InAs nanowire with GaSb shell, with Te conc. of $1\times\ 10^{19}\,\mathrm{cm}^{-3}$. (d) InAs nanowire with GaSb shell, with Te conc. of $2.5\times\ 10^{19}\,\mathrm{cm}^{-3}$.

the Te conc. %, to acquire the Te doping values from the APT analysis, as can be found in table. 3. These are approximated values, since the whole wire is considered as wurtzite. To obtain closer/real values of Te doping concentration in the wires, once can estimate the percentage of zinc blende inclusions in the wurtzite structure, from the diffraction patterns of the nanowires (TEM analysis) and calculate it.

Sample no.	Nominal Te conc. (cm^{-3})	Te (%)	Cal. Te conc. (cm^{-3})
4	7.5×10^{18}	0.004-0.008	1.55×10^{18} - 3.12×10^{18}
5	1×10^{19}	0.004-0.011	1.55×10^{18} - 4.27×10^{18}
6	2.5×10^{19}	0.01-0.04	3.89×10^{18} - 1.55×10^{19}

Table 3: Nominal and calculated values of Te conc. in the InAs nanowires.

An increase in Te dopant concentration led to an increase in the unstable facets of the nanowires. Figure 65 are the InAs cores that are reconstructed using APT analysis. The cores are mapped with facet changes. At higher Te concentration, the nanowires develop a steady facets and form dodecagonal structures, as seen in Fig. 65 (c). The reconstructed 3D

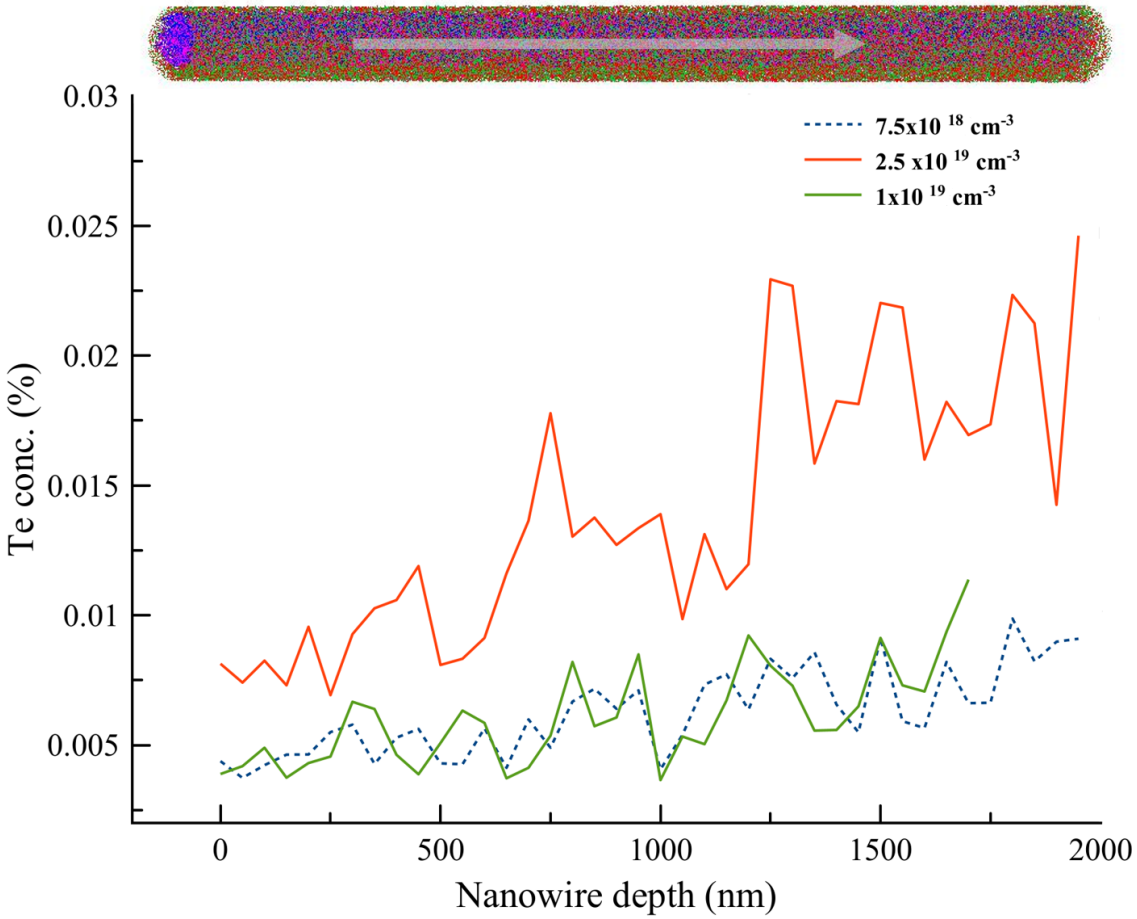

Figure 64: Te concentration of different nanowires w.r.t nanowire depth. The direction of evaporation of the analyzed nanowire is shown on the top.

data of the nanowires can be further analysed to know their structure. This analysis is done by inspecting each 1 nm segment of the nanowire from the re-constructed, rotating it and looking at the structure. These results are presented in Fig. 66, (a) is the hexagonal structure of the InAs core, whereas (b) is the transition into a dodecagon, where the facets are rounded (red arrow), i.e. (112) facets are starting to occur, (c) the InAs core has completely transitioned into a dodecagonal structure, hence the additional (112) facets.
A similar observation has been done by Rieger et al. [121] on InAs nanowire with a shell of GaSb. GaSb shell was observed to have, dodecagonal shape with (110) and (211) facets. This is due to the surfactant behaviour of Sb like Te, that tends to form lateral facets by increasing the adatom sticking coefficient [122].
An analogous observation has been confirmed by TEM analysis and can be seen in Fig. 67. The InAs core cross-section has been analyzed under the microscope. The Te concentration in this wire is $2.5\times\ 10^{19}\,\mathrm{cm}^3$. An ADF image, of the core is seen, the facets are marked and shows a dodecagonal structure. The GaSb shell has been dissolved during the preparation of the cross-section for the analysis.

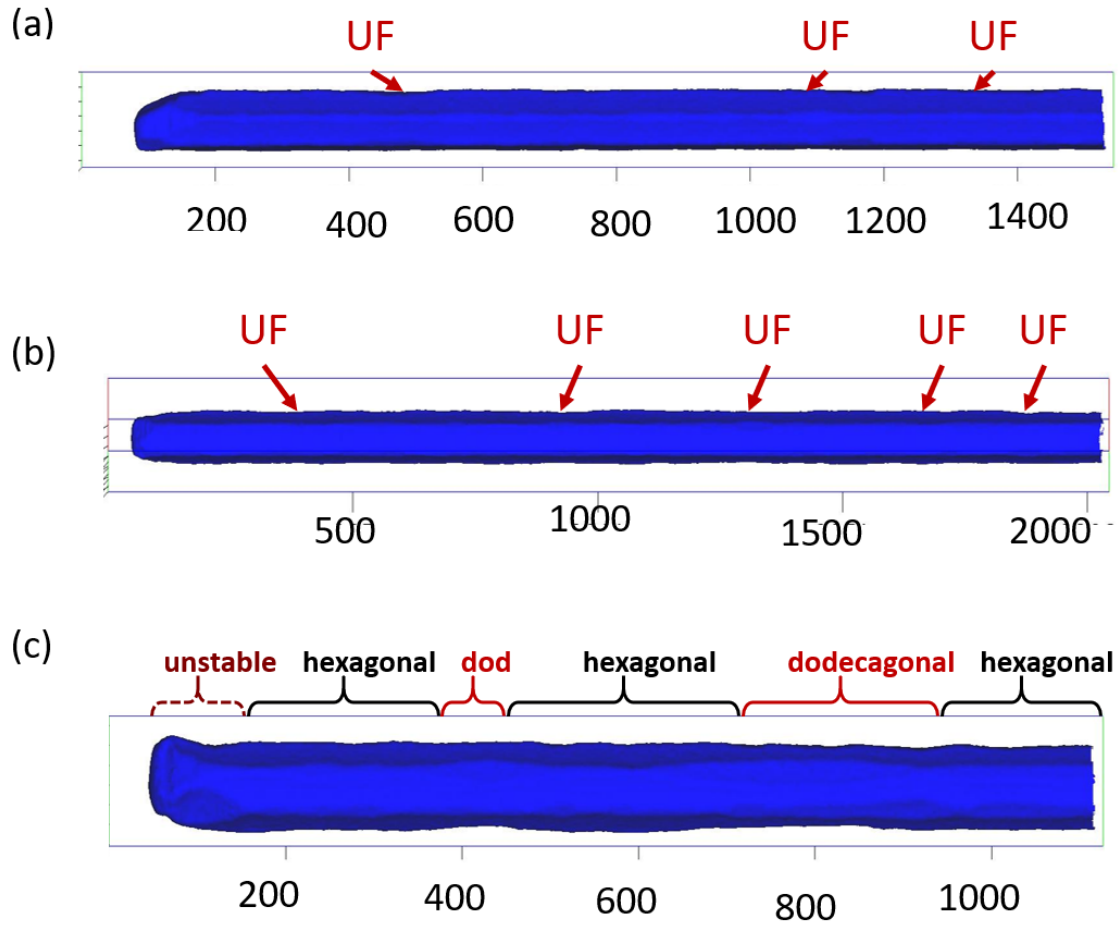

Figure 65: APT reconstructed depth profiles of the InAs core with Te doping of different concentrations (from top to bottom of the wire). (a) InAs nanowire core with Te conc. of 7.5$\times$ 10^{18} cm^{-3}, few unstable facets are seen along the line. (b) InAs core with Te conc. of $1\times$ 10^{19} cm^{-3}, the number of unstable facets increase with increase in the dopant concentration. (c) InAs core with Te conc. of 2.5$\times$ 10^{19} cm^{-3}, there can be seen few unstable facets and some of them have evolved into dodecagonal facets throughout the wire.

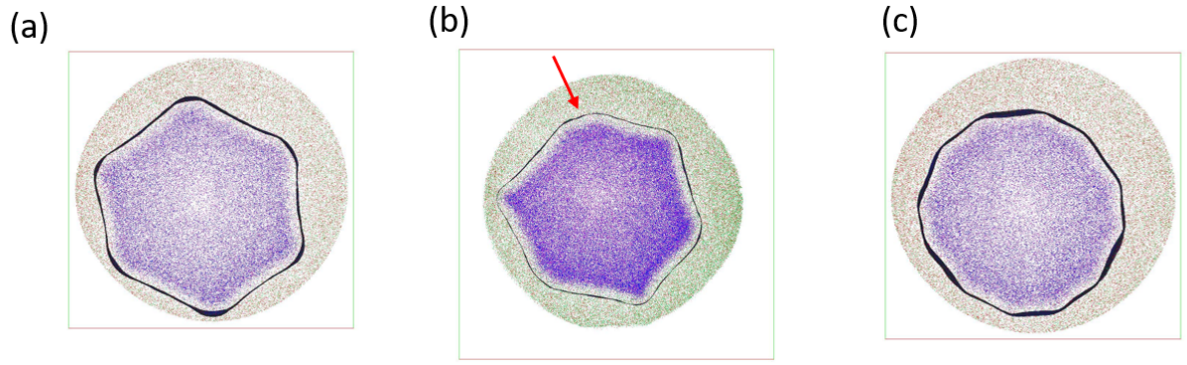

Figure 66: APT reconstructed radial profiles of InAs-Te doped nanowires, with facets. (a) A stable hexagon with 6 facets. (b) Hexagon with unstable facets, that are lateral (marked in red are unstable facets). (c) A stable dodecagon with 12 facets.

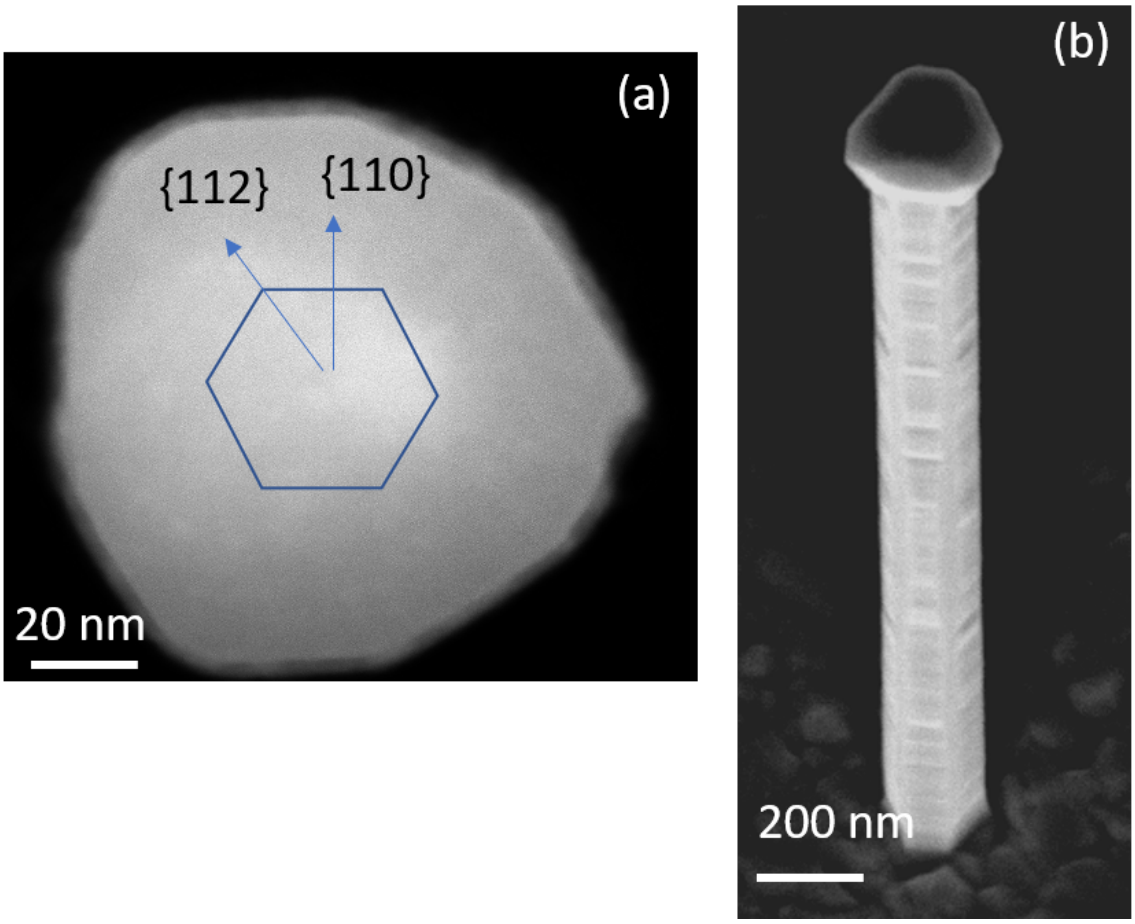

Figure 67: A high maginified SEM micrograph of the InAs-Te doped (with 2.5$\times$ 10^{19}cm^{-3}) and GaSb shell. (a) A cross-section made by FIB, radial profile of the nanowire, the lateral facets (211) can be clearly seen, and the structure is a stable dodecagon. (b) Corresponding, whole of InAs-Te doped nanowire with GaSb shell, with 12 facets and a GaSb cap on top of the wire.

6.2.2 Electrical Measurements

The electrical measurements on the different Te doped nanowires without GaSb shell was done by Anton Faustmann, at PGI-9, Forschungszentrum Jülich. The InAs nanowires doped with different Te concentrations are measured at room temperatures w.r.t to the ratio of nominal distance between the contacts and the cross sectional area, d_{nom}/A. A is determined by average diameters of the nanowires. The gold contacts on the nanowires are layed-out in a four terminal scheme to eliminate the contact resistances. Sample 1, 2, 3, and 5 are measured, and the corresponding results, can be seen in Fig. 68. A linear increase w.r.t the contact separation length, for each set of doped wires is observed. This evidently confirms the ohmic behaviour of electrical transport in the nanowires. Increase in conductivity can be seen with increase in the Te doping concentration. The spread of the resistance data is due to the different diameters of the nanowires. Averaging the data, it can be concluded that the general conductivity is increased for high doped nanowires.
The nanowires for the four-point measurements are fabricated using sample 3 with in-situ Al shell. These are measured in a AuGe shunt resistor scheme, the shunt resistor is fabricated by EBL and by further metal deposition. These nanowires are placed on a 5 nm/10 nm thick Ti/Pt gate pad covered with a 3 nm/12 nm Al_2O_3/HfO_2 stack (used as dielectric), with the help of

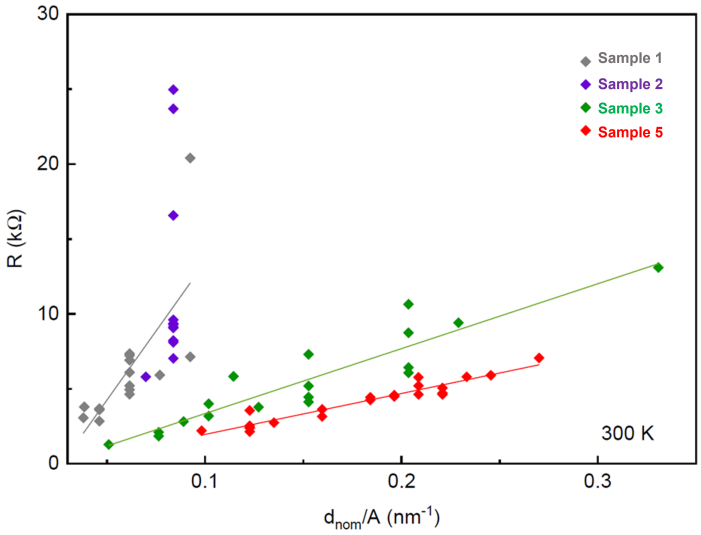

Figure 68: Electrical measurements: Four-terminal resistance R of different Te doped InAs nanowires at room temperature plotted against the quotient of nominal contact distance d_{nom} and mean nanowire cross section area A. The data is fitted using linear fit, thus determines the resistance.

an optical microscope and a micromanipulator. The NbTi shells are evaporated ex-situ onto these wires. The low temperature electrical measurements are performed in a ^{3}He/^{4}He dilution refrigerator with a base temperature of 15 mK. Figure 69 shows a comparison of undoped and doped wires with Al shell made into Josephson junctions.

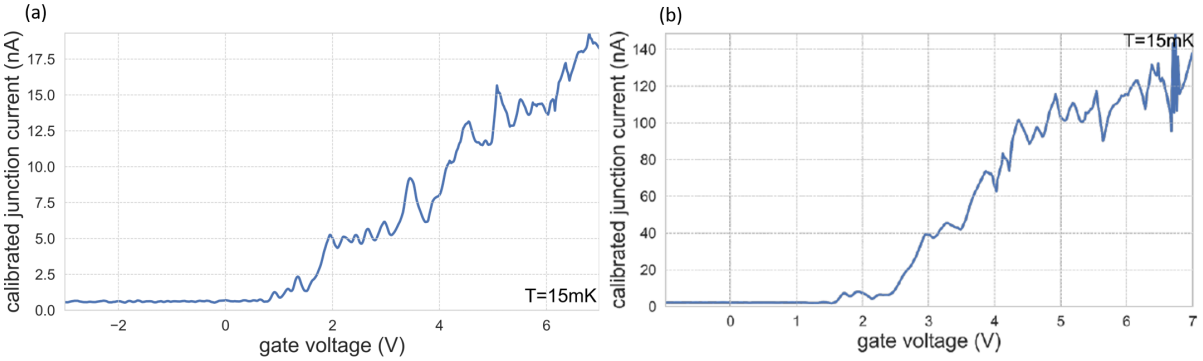

Figure 69: Low temperature electrical measurements at 15 mK. (a) Critical current for the undoped nanowires, after subtracting the shunt contribution is around 18 nA at a gate voltage of 7 V. (b) Whereas for medium doped wires, there is a current of 150 nA, observed this is due to the increase of the charge carries due to Te doping.

The corresponding critical current of the junction w.r.t gate voltages (tuned by a bottom gate) of the Josephson Junction can also be seen in Fig. 69. The Josephson junctions are highly tunable with a gate. Figure 69, shows the evolution of nanowire within a gate voltage range of -2 V to 7 V. The junction current is subtracted from the shunt resistor contribution, hence called calibrated junction current. A critical current of 150 nA is observed, whereas for undoped wires a mere 17.5 nA of critical current is seen in the junction. This clearly indicates that the dopants caused additional electrical charge carriers in the conduction band. Thus the doping results in an increase of the critical current of the Josephson junctions.

7 InAs/Al Nanowires

This chapter elucidates on the InAs/Al half-shell nanowires that are fabricated in-situ. The nanowires are grown by selective-area epitaxy method. Eventually a superconducting Al half shell is evaporated. This is done by an in-situ method in contrast to the traditional method of ex-situ evaporation of superconducting contacts. The interface between the semiconductor and the superconductor has been observed to be very sharp in the in-situ process. The quality of the Josephson junctions is demonstrated by SEM and TEM analysis and corresponding low temperature transport measurements. In the previous chapters, the nanowires have been grown and the superconducting contacts have been later evaporated onto the nanowires. This process is known as ex-situ, i.e. the nanowire is normally wet-chemically etched or sputtered by Ar^+ to remove the native oxide of the nanowire. Eventually, the superconducting contacts are evaporated onto the nanowire. This process is done by standard EBL processes. The whole process of depositing superconductors onto the nanowires via an ex-situ approach exposes the nanowire to different polymers, chemicals, etc. This can be quite detrimental for the interface between the nanowire and the superconductor, i.e. the above mentioned processes could leave residues and thus cause subgap states within the semiconductor. It is of a paramount importance to tailor the interface between the nanowire and the superconductor deposited onto it. Controlling the properties of semiconductor/superconductor interfaces via an in-situ method is a most sought after method for improving the efficiency of the electrical devices. Interfaces with atom-scale uniformity is a necessity to achieve a good induced gap. An in-situ approach of epitaxial aluminum, as a superconductor onto a single crystal InAs nanowire, has been first performed by Krogstrup *et al.* [123]. This process yields a higher transparency between the interfaces, which tackled the soft-gap problem in the induced superconducting gap in InAs/Al structures. This versatile technique has been assimilated in this work to create a method of in-situ deposition of superconductors on nanowires.

7.1 Aluminium Half-shell Growth

To observe a hard gap and bound states (Andreev reflections) between the superconductor and a semiconductor, the contact between the two have to be intimate. The major pre-requisites of achieving such hybrids is firstly that the interface between the semiconductor and the superconductor has to be of high quality. Secondly, the shell has to be crystalline and smooth along the length of the nanowire. The smoothness of the shell further enhances the contact properties w.r.t external sputtered metal contacts. The sputtering is an uniform process all over the wire although any defects at the interface can lead to a non-transparent contact. The superconductor shell can be deposited in two ways, i.e. by rotation, we can obtain a full-shell whereas without rotation, a half-shell is obtained. Although, a symmetric potential is obtained with full-shell structures, we are interested in the SC half-shell structures on the nanowires. These enable greater benefit as, three facets of the nanowire are exposed. This means that half of the nanowire is covered with a SC shell. This partial coverage, allows the tuning of the Fermi level in the nanowire via a gate, thus resulting in change of the carrier concentration. Whereas for a full-shell shields the wire electrostatically, and tuning the Fermi level is a laborious work.
The InAs nanowires are grown on the Si(111) substrates via VS growth mode by. As mentioned

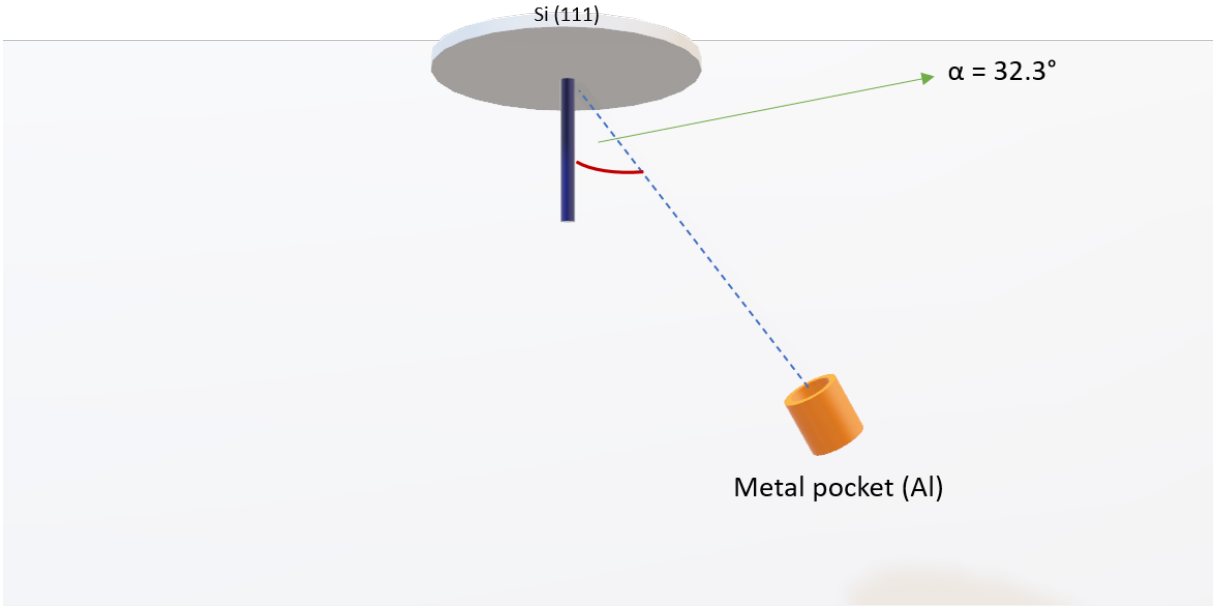

Figure 70: Schematic of the geometrical relations in the metal MBE.

in the InAs nanowire chapter to obtain thinner nanowires, the growth proceeded in two steps. First step consisted of the nanowires are grown at a higher substrate temperature of 480 °C with an In growth rate of 0.08 μm/h and an As (BEP) of $\approx 4 \times 10^{-5}$ torr for 10 min. And in the second step, to decrease the width of the nanowires, the substrate temperature is decreased to 460 °C simultaneously with a reduced In growth rate of 0.03 μm/h and an As_4 BEP of $\approx 3 \times 10^{-5}$ torr for 2.5 h resulting in $4 - 5\,\mu$m long and $70 - 80$ nm wide nanowires with six (110) facets. Eventually, the nanowires undergo an arsenic desorption process, thus they have area heated at a substrate temperature of 400 °C for 20 min and at 450 °C for 5 min, this removes the additional arsenic around the nanowire. Thus, this process helps in reduction of arsenic condensation on the nanowire, hence preventing the formation of AlAs layer at the interface upon Al metal deposition. Afterwards, the sample with nanowires is mounted onto the metal MBE chamber. The whole setup is contained in ultra high vacuum (UHV) environment. In Fig. 70 the geometry of the setup is illustrated. The metal MBE has a metal pocket, set up by default at 32.3° to the substrate thus to the nanowires. This is a small impinging angle of metal deposition. The details of the setup has already been dealt with in the experimental methods chapter. It has been already reported that the substrate temperature for Al metal deposition is of a huge importance rather than the impinging angle [33, 73, 123]. This was taken as an initial parameter to vary in the following experiments for Al deposition.

It has to be noted that in Fig. 71, the samples for 50° C and 2° C, has been done on Si (111) substrates that are not pre-patterned. This was performed to study the effect of the impinging angle of Al flux, on the nanowires that grow at different directions. The nanowires on these substrates primarily grown towards the (111) direction, but there are also nanowires that grew astray. The major concern is to maintain uniformity amongst the grown nanowires in terms of lengths and diameters. Hence for this purpose selective area growth on pre-patterned substrates is used once the parameters have been optimized. For all experiments, an Al pressure of 2.5 $\times 10^{-5}$ mbar for 20 seconds has been taken. This parameter is higher than in the experiments performed by Güsken *et al.* [73], the higher pressure leads to a faster

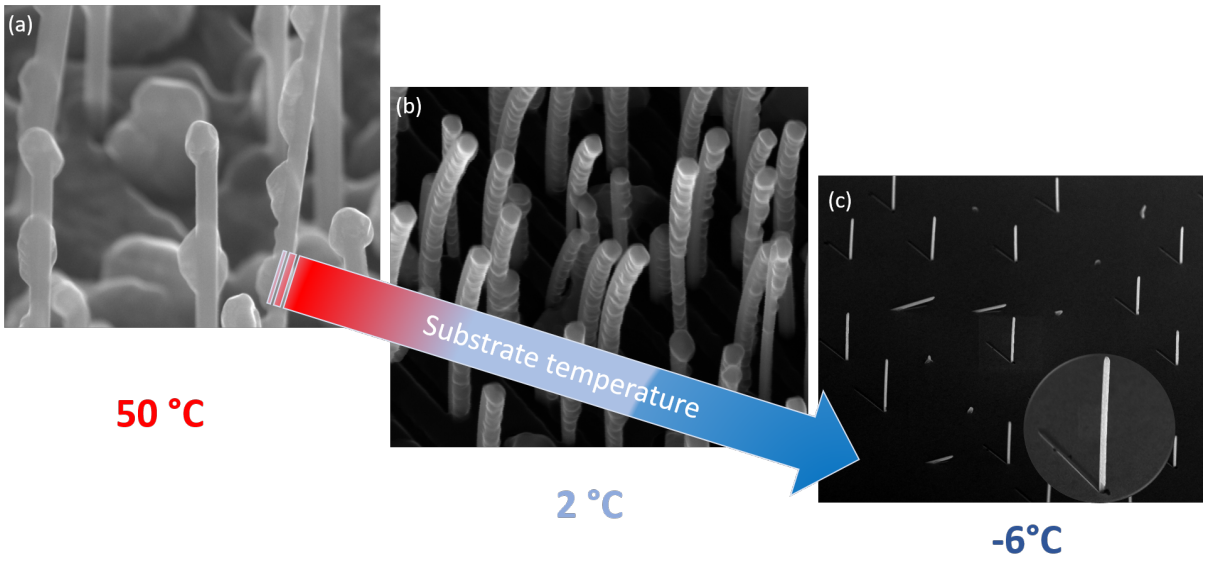

Figure 71: Al metal evaporation on InAs nanowires: (a) Al metal islands at 50 °C. (b) Al metal islands forming a complete layer at 2 °C. (c) A complete smooth and compact Al half shell at -6 °C.

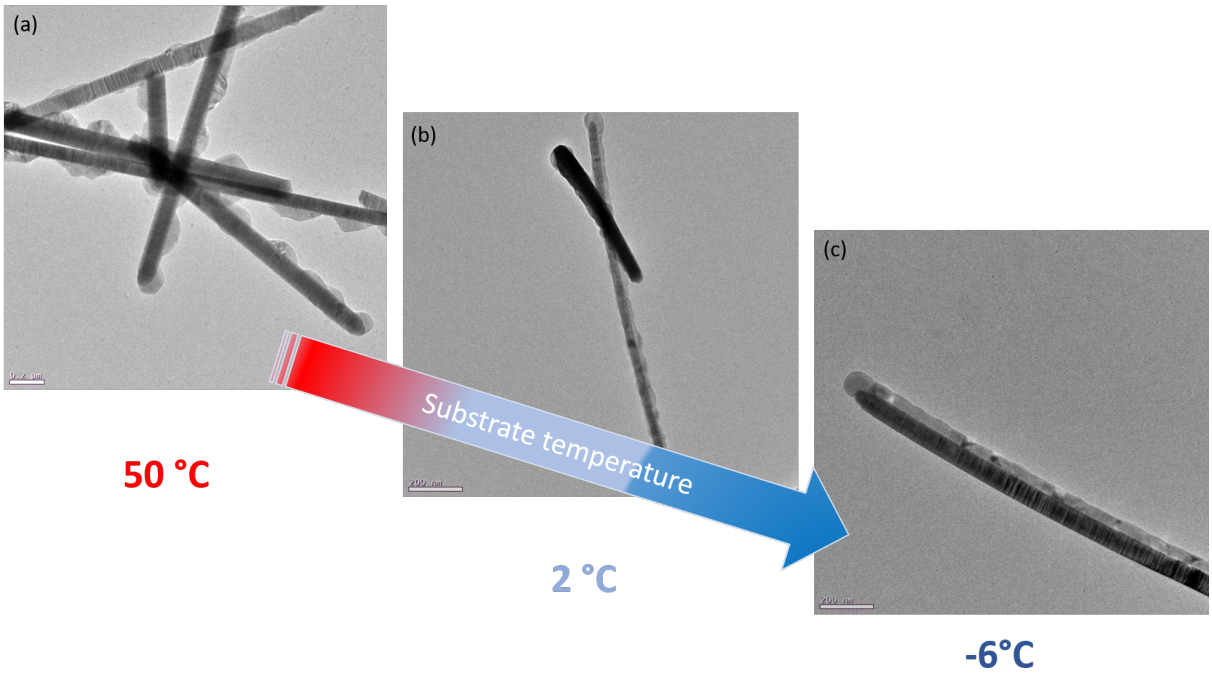

Figure 72: TEM micrographs of InAs/Al half-shell nanowires corresponding to Al deposition at different temperatures.

growth i.e. reduces the exposure of the wire to heating from the deposition. A shell thickness of 25 nm has been kept constant, as it has been observed that the layers of 25 nm and above have been demonstrated to have a compact and smooth film on a plain Si substrate. Figure 71 shows the experimental outcome, performed by varying the substrate temperatures. The temperatures have been varied i.e. 50° C, 2° C, -6° C. A temperature of 50° C has been obtained by subsequent heating of the substrate. The 2° C has been gained by switching off,

the heat inducing sources and waiting for the temperature to stabilize. The -6° C temperature has been achieved overnight by turning off all the heat inducing sources and with a cryogenic shielding which takes about 15 hours for the temperature to stabilize. A 25 nm thick Al layer has been evaporated on the nanowires. The shell coverage can be seen in Figs. 71 (a), (b), and (c) for different temperatures. The corresponding TEM overviews can be seen in Figs. 72 (a), (b) and (c). There one can observe an improvement of Al shell coverage from both, the SEM and TEM micrographs. This evolution of Al adatom migration w.r.t the substrate temperature is indispensable. The diffusion lengths of impinging Al adatoms on the InAs facet decreases with the substrate temperature. As the substrate temperature is lowered the diffusion lengths of the adatoms can be seen suppressed, there by forming clusters of Al and eventually form layers. At -6° C, the adatom diffusion is significantly reduced, there by forming a compact and smooth Al layer along the nanowire. Figure 73 shows a SEM micrograph of the corresponding nanowire, where the Al shell, has covered three complete facets of the nanowire in Fig. 73 (b) towards the left part of the wire is the overbearing Al layer. The shell thickness on the side facets of the nanowire is 30% thinner than the facet that is directly facing the metal flux. The thickness of the middle facet is 25 ± 3nm and the thickness on the side facets is around $17 \pm$ 2 nm. Figure 73 (a) shows the nanowire with Al half shell, that is compact and smooth. The shadow can be seen on the mask, this depicts the direction of the metal deposition.

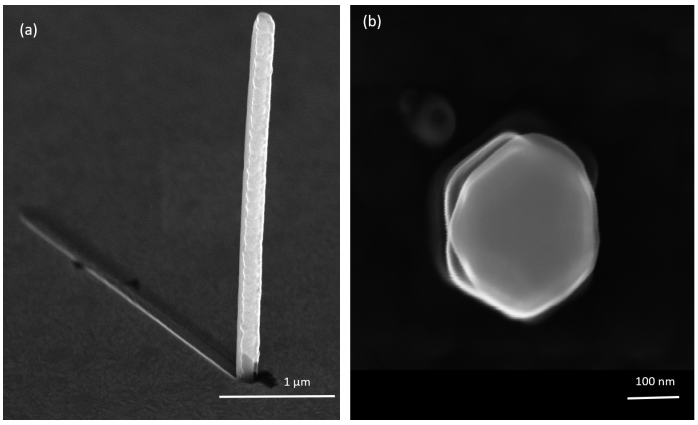

Figure 73: Optimized Al half shell growth at $-6\,^{\circ}$C. (a) InAs nanowire grown selectively with Al half shell, shadow depicts the direction of the Al flux. (b) View from the top of InAs nanowire shows a hexagonal structure, where in three left facets are covered with Al.

7.2 Towards In-situ Josephson Junctions

An essential observation from the samples grown at 1° C can be seen in Fig. 74. These are the nanowires grown randomly on Si (111) substrate, and the substrates are titled by 30° for imaging. The pinholes formed on this substrate are due to the H_2O_2 treatment. These pinholes are formed at random places on the substrate and with different dimensions. It is an uncontrolled process. Hence the nanowires that grow in these pinholes, are directed mostly in (111) direction with some tilt and some of them even towards the (100) direction, as seen in Fig. 74 (a). This SEM micrograph shows in nutshell, the nanowires grown at different angles. While, most of the studies with Al layer deposition onto nanowires assert that the substrate temperature is an important factor to achieve smooth Al shells, the study from Kang *et al.*, [124], have shown the effect of the impinging Al flux onto the nanowires. They have

demonstrated that at 0° C a smooth Al layer i.e. crystalline was achieved, just because of growing the nanowires at an angle. This angle increases the impinging Al deposition angle. Thereby causing the Al adatom incorporation on the nanowire surface to be smooth with small diffusion lengths, without the need of further cooling it down.

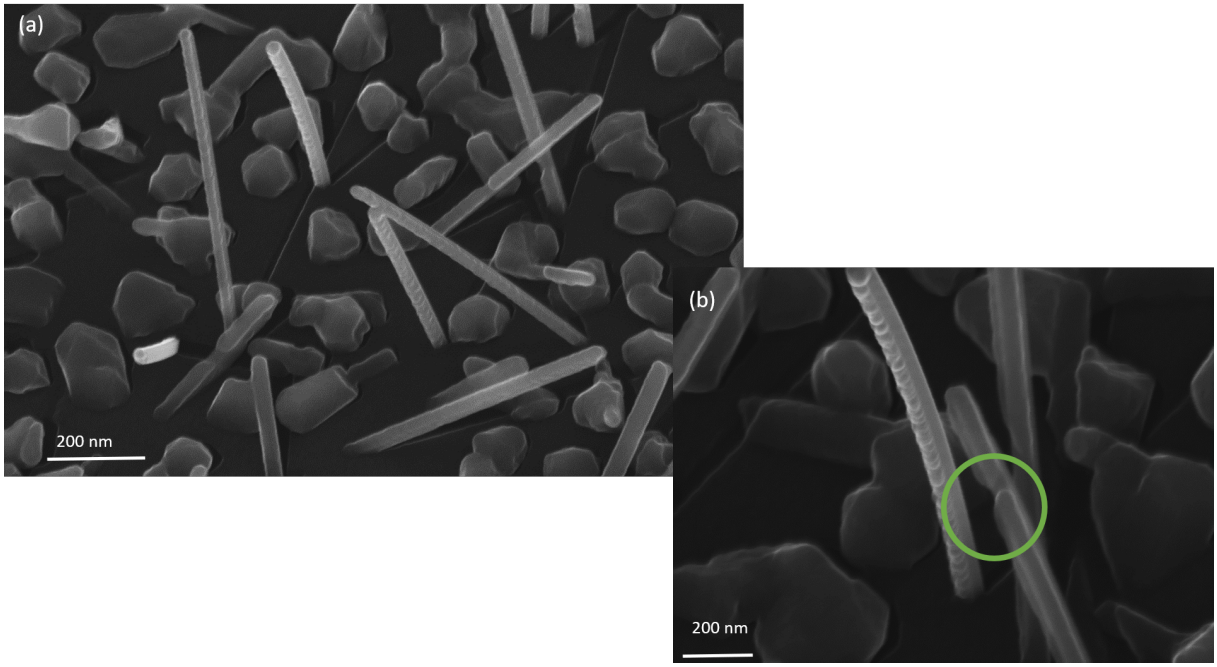

Figure 74: SEM micrographs of InAs nanowires at 30 ° tilt. (a) InAs nanowires with Al half shells deposited at 1 °C, depicts the smoothness change with the orientation of the nanowire. (b) In-situ Josephson junction (green) formed due to shadowing from aother wire across it.

This is what has also been observed with our samples, with the Al deposition at 1° C. The nanowires grown in different orientations can be seen Fig. 74(a). It can be seen that the Al shell deposited is different for every other orientation of the nanowire. This is related to the diffusion lengths of the Al adatoms. It can be concluded that, for nanowires that are more titled and are against the metal flux, have an metal flux impinging angle of 87 °. Hence causes smoother shells. Smaller impinging angles results in Al shells with many islands, i.e. rougher shell corresponds to Al clusters, which could be crystalline still at this temperature. It can observed that the nanowires which are reclined, have much smoother Al layers compared to the perpendicularly grown ones. It has to be noted that both of these nanowires have hexagonal structures with atomic flat facets. The reclining nanowires have an impinging angle greater than 80°. Figure 74(b) clearly shows a difference in the Al smoothness between the nanowires grown at different orientation. Figure 74(b), shows a weak-link, that is caused due to the shadowing of another wire. This idea (green highlighted) is a seed for the next chapter, which creates in-situ Josephson junctions. The SEM micrograph depicts a SNS Josephson junction that is caused by shadowing by another wire across it during the metal deposition.

7.3 Transmission Electron Microscopy (TEM) And Electrical measurements

The samples that are grown at $-6°$ C are further inspected to asses the quality of the Al half shell and the interface between the superconductor and the semiconductor. In order to

analyze the structural properties of the InAs-Al core-half-shell nanowires with 25 nm shells, scanning transmission electron microscopy (STEM) was used. The nanowires were transferred to carbon Cu grids by smearing it on the growth substrate. In Fig. 75 the nanowires on these holey copper grids are depicted. Figure 75 (a) shows the complete wire that is inspected for further analysis. The red marked square is a detailed segment of the InAs/Al interface and the green square shows the InAs wire itself. Figure 75 (b) shows InAs nanowires grown by the catalyst-free method with a polytypic crystal structure with stacking defects. Figure 75 (c) shows the 25 nm Al half shell, with different Al grains along the nanowire.

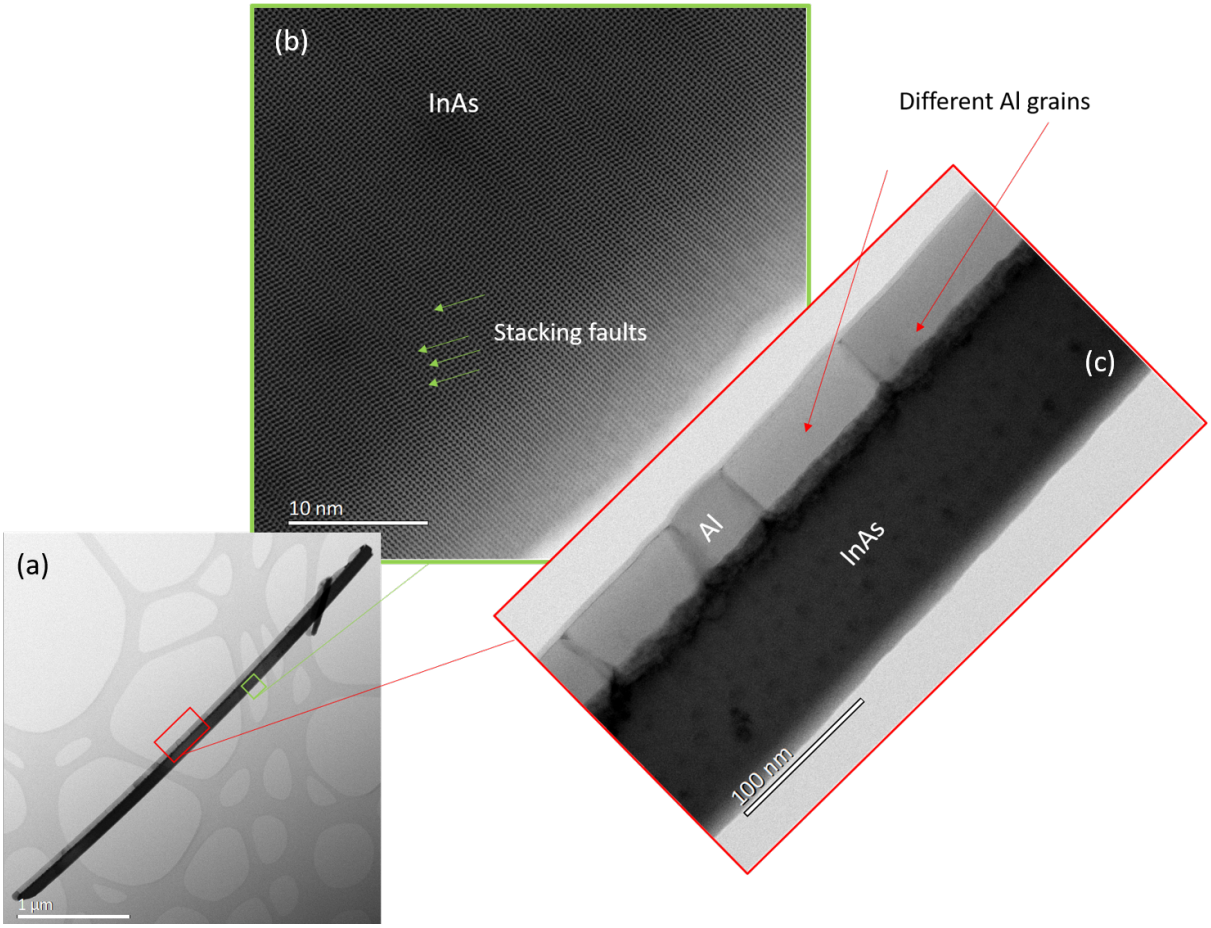

Figure 75: bright field- STEM micrographs of InAs nanowires with Al half shells. (a) Complete nanowire with Al half-shells. Marked in red is the InAs/Al interface area, green is a part of InAs nanowire. (b) probed area (green) from (a) depicting the stacking faults within the InAs nanowire. (c) Red probed area with InAs and Al. Different grains of Al can be seen (change in contrast means differently oriented Al grains).

These Al grains are oriented in different directions, one towards the viewing direction which is lighter in colour, while the other grains are oriented away from the viewing direction is darker in colour. There have been two dominant aluminum grains, observed, as marked in Fig. 75 (c), with a clear grain boundary. This finding is similar to that of Krogstrup *et al.* [31]. The Al grain orientation formation is irrespective to the stacking defects present in the nanowire, hence it is not epitaxial. The evaporated Al layer evaporated is uniform along the length of the nanowires and smooth. It has been observed that the thickness varied along the wire as 23 ± 2 nm. The differently oriented grains, also with different contrast, can be seen with two

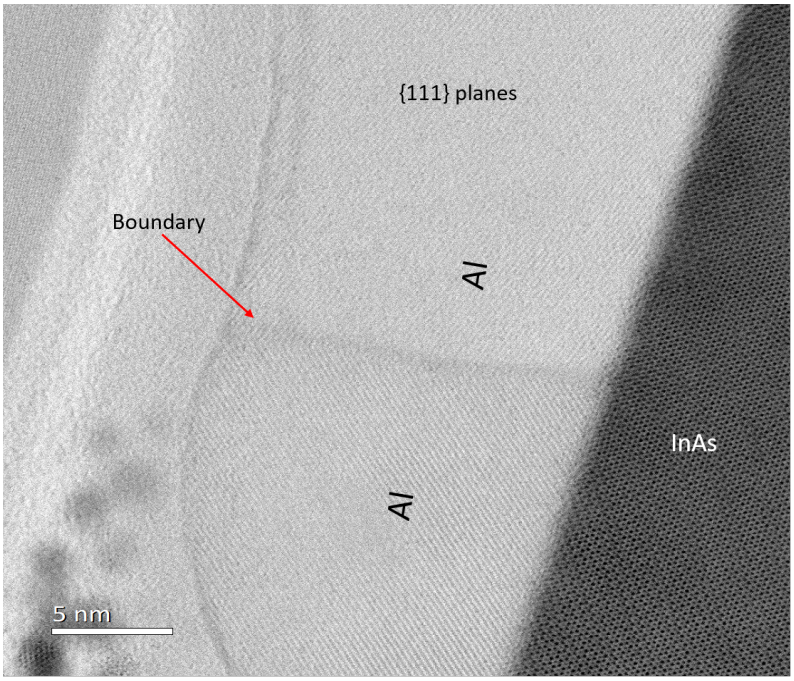

Figure 76: Scanning TEM micrograph of the interface between InAs and Al, the grain boundary is marked. No visible deterioration of the interface is found.

viewing directions with grain boundaries marked by a red arrow in Fig. 76. The predominant grain orientations include $(\bar{1}\bar{1}\bar{2})$, (110) and (111). These orientations are different from the previous works of Krogstrup *et al.* [31], Kang *et al.* [124], and Carrad *et al.* [26], but consistent with the work of Güsken *et al.* [73]. These authors have evaporated aluminum at much lower temperatures, using nitrogen cooling at 77 K thus causing the grains to be larger with lesser inconsistencies in the orientations. We have observed more than two orientations of Al grains. This is attributed to the Al diffusion at higher temperatures i.e. at -6° C. These are formed due to a low surface energy at this particular temperature to minimize the strain [31]. As discussed before by Fig. 76, different Al grain orientations have been observed. Importantly, the change in phase of the nanowire does not affect the change in the Al grain orientation. In other word, the stacking faults within the InAs nanowire do not disturb the crystal structure of the Al. Thus making Al non-epitaxial. The high magnification image of the interface between the Al and InAs, as seen in Fig. 76, has been observed to be sharp and smooth, with no defects or other dislocations found in between crystalline InAs and Al without the AlAs layer in between.

7.4 Electrical Measurements At Low Temperature

The low temperature electrical measurements on the InAs/Al nanowires have been performed in a ^{3}He/^{4}He dilution refrigerator at 15 mK at RIKEN. To obtain a weak link on the Josephson junction device, it was etched with transene-D. Later on superconducting contacts with NbTi are sputtered. The nanowire is also accompanied by a AuGe shunt resistor, which prevents hysteresis. The shunt resistor consists of of a 10 nm thick, 1 μm wide, and 7 μm long AuGe stripe with a known resistance of $R_{\text{shunt}} = 80 - 140\,\Omega$. The nanowires are placed on Ti/Au gate pad, that is covered by a 3 nm/12 nm stack of Al_2O_3/HfO_2. The nanowires are placed by means of a manipulator with an indium wire as a tip under an optical microscope. A

subsequent deposition of 90 nm NbTi is performed.

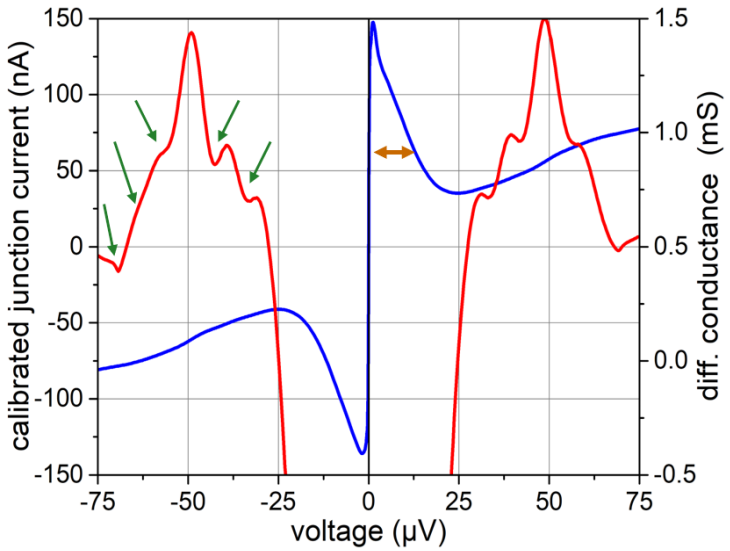

Figure 77: Differential conductance (red) with respect to the voltage swept from -75μV to 75 μV. The peaks (green arrows) on the graph are attributed to multiple Andreev reflection features. The junction current (blue) is also plotted against voltage. The yellow arrow shows a deviation from the regular IV curves. No hysteresis is observed.

Figure 77 shows a calibrated junction current in blue and differential conductance in red w.r.t bias voltage. The IV curve is different than the one without a shunt resistor where an abrupt switch to a superconducting branch is usually observed. Even though this is a calibrated graph, i.e. the shunt resistor contribution has been carefully removed from the data, its signatures can be seen. These signatures are evident in the smooth switching to the superconducting branch (yellow arrow). The additional peaks also known as subharmonic gap structures (green arrows) are a signature of multiple Andreev reflections (MAR) [125]. The appearance of these peaks and the consequent increase of the conductance in the junction area, is a clear indication of high transparency. These measurements thereby prove that the junction transparency is indeed high, which translates into a a non-defective interface between the semiconductor and the superconductor. The in-situ Al deposition technique and the arsenic desorption procedure have thus worked efficiently.

8 In-situ Josephson junctions via shadow evaporation

8.1 Introduction

In this chapter, fabrication and processing of fully in-situ Josephson junctions is presented. This novel method is based on the evaporation of a superconductor on InAs nanowires to achieve in-situ Josephson junctions by an elegant shadow mask technique. This results in a Josephson junction with two superconductor leads and a semiconductor weak link in between. The aforementioned method is irrespective to the superconducting materials used and the corresponding substrate preparation has been already discussed in the previous chapters 9 and 10. This is used as a foundation for the shadow mask technique and for the deposition of superconducting materials such as Al and Nb [126, 127].
Generally, aluminium is the foremost choice for a superconductor due to its large coherence length [128, 129]. Aluminium is also known to be easily compatible with the standard fabrication techniques. Besides this, its low critical magnetic field is a drawback, and calls for robust material systems, such as Nb and its alloys [24–26], Pb [27], V [29, 30], and Sn [34]. As discussed in chapter with InAs/Al Josephson junctions with ex-situ etched weak links, a method to deposit metal on a semiconductors [123] has been already established. Furthermore, to make a Josephson junction device, the traditional method to achieve a weak link is by wet chemical etching. However, recently there has been progress in achieving a pristine weak link without exposing the Josephson junction to chemicals, which is via a shadow evaporation technique, i.e. using one nanowire to shadow another nanowire [33, 34] or by with the help of a suspended SiO_2 layer as a template used for shadowing the other wire [130].
In order to obtain a Josephson junction, we circumvented the traditional methods and utilized the in-situ techniques. This chapter describes a method to realize a Josephson junction in an MBE system without breaking the vacuum. The complete process is realized in two steps. The first process is the tactical placement and growth of nanowires on tilted Si (111) surfaces to cast shadows on one another. The latter involves, in-situ evaporation method of superconductor half-shells on an InAs semiconductor nanowire. The refinement of the process is discussed here in [32]. The technique involves deposition at higher angles, that bypasses the problem with smaller deposition angles of 32.3° discussed in the previous section, additionally making it easy for incorporation of several other materials.

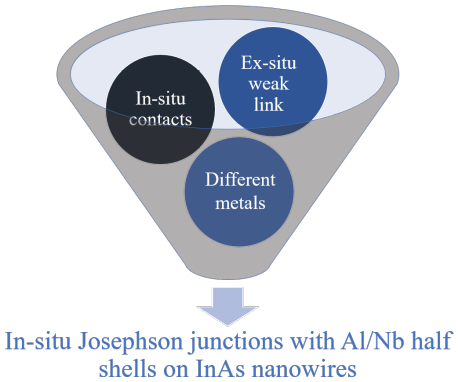

Figure 78: Overview of the fully in-stu prepared Josephson junctions.

This novel method interpreted in Fig. 78 involves growing nanowires on tilted Si (111) planes which in turn elevates the metal deposition angle to 87°, which leads to smoother shells and there by upon shadowing causes the formation of weak links [127]. The importance of higher deposition angles has already been reported by Güsken *et al.* [32]. Here, it was reported that the Nb metal deposition is smoother at 87° rather at 25°. This forms a basis for the improvised method, presented in this chapter. The quality of the deposited superconductors is confirmed by the SEM and TEM analysis, while the transparency of the semiconductor/superconductor interface is ascertained by the low temperature transport measurements. The results presented in this chapter are published in Ref. [126, 127].

8.2 Nanowire Growth On Tilted Si (111) Surfaces

For the desired Josephson junction, the semiconductor segment has to be suspended with two closely separated superconducting electrodes, which forms a superconductor-semiconductor-superconductor Josephson junction. This can be achieved with nanowires growing on adjacent Si(111) facets, in fact, closely passing each other without merging. One nanowire grows higher than the other and during the metal deposition, the higher wire casts a shadow on the lower one. Two procedures have been adopted. The first method is a random growth method, i.e. a proof of concept to demonstrate the feasibility of the junction formation, whereas the second is a sophisticated method, which involves a selective area growth. The nanowire growth procedure for both methods was same as mentioned in the selective area growth chapters 6, 7, 8. For the nanowires grown on the Si (111) facets, in the random growth method, the control of the growth of nanowires depends on the pinholes formed due to the H_2O_2 treatment.
The InAs nanowires are grown via VLS method on the Si (111) facets which are angled at 54.7° w.r.t the Si (100) substrate plane by molecular beam epitaxy (MBE) and are self-catalysed. The whole process involves two steps. In the first step the substrate is heated to 480° C and the InAs nanowires are grown with a higher In growth rate of 0.08 μm/h and an As flux As_4 (BEP) of $\approx 4 \times 10^{-5}$ mbar for 10 min, as discussed in the previous chapters. Then the parameters are lowered to In growth rate of 0.03 μm/h and with an As BEP of 3 $\times 10^{-5}$ mbar for 2.5 h at 460 ° C. This resulted in $4 - 5\,\mu$m long and $75 - 80$ nm wide nanowires. The nanowires grown in the high arsenic containing environments, thus are subjected to undergo an arsenic desorption procedure. For this purpose, the substrate is transferred to a heating chamber, wherein the substrate with the nanowires is heated initially for 20 min at 400 ° C and later on at 450 ° C for another 5 minutes. This process eliminates all the As coating on the nanowire. The next step involves the metal deposition. For this, the substrate is transferred into a metal MBE. The heating chamber and the metal MBE (Al, Nb metals) and the MBE (InAs nanowire growth) are all connected in the nanocluster, so the complete process is in-situ. UHV is maintained through the entire process. The metal deposition parameters and details will be elaborated in the individual sections for Al and Nb separately.

8.3 InAs/Al Nanowires

8.3.1 Random Growth

To further assess the superconducting materials used, the results of the the random growth of InAs/Al nanowire Josephson junctions are presented in Fig. 79. The nanowires are grown initially in an MBE system and then the Al metal deposition is performed 45 ° in place to the substrate. The substrate is cooled down to -6° C with an Al flux of 2.5 $\times 10^{-5}$ mbar for 40 seconds. As mentioned before, the nanowires grown on the substrates treated with H_2O_2, cannot be controlled, because of the random pinhole formation. Thus the nanowires are grown all through the square troughs i.e on the four side facets and also from the bottom of the trench and do not have any directional preferences. As a result, these samples have a high probability of shadowing and crowding of nanowires. The nanowires are grown with same parameters in 2, 3, 4, and 5 μm squared troughs. The 3 μm square troughs, have nanowires that are grown longer than the one side of the square trough. This means that the nanowires grown in these troughs are longer and they shadow each other, thus greater yield. The nanowires grown in these ones have a length of 4 -5 μm (longer than the square side) so they project outward and pass closely along with the nanowires in the same trough. The number of the shadowed junctions is high in these structures. The overview of all possible outcomes of the random growth can be seen in Fig. 79. Also seen is the high parasitic growth in these prepared substrates, mainly constituting crystals, broad whiskers growing in the creases, and nanowires growing from the crystals and a lot of misdirected nanowires. The misdirection is due to the Si (100) surface underneath these square troughs. The inevitable parasitic growth is mainly caused due to the porous oxide layer of around 2 nm formed by the H_2O_2 treatment which causes non-uniform pinholes when heated [55]. The growth of crystals, whiskers and other structures growing out can be quite detrimental for nanomanipulation and for forming a weak-link at the middle region of the nanowire. The density of the nanowires and the crystal growth can be monitored by reducing the In and As fluxes but this would reduce the number of shadowing junctions and also decreases the length of the nanowires [32].
The nanowires grown on these substrates have four possible outcomes, as shown in Fig. 79.

- Fig. 79 (a): X-like junction (red) forms when both the nanowires merge towards each other and still keep growing. In this case the nanowires grow at a same rate
- Fig. 79 (b): Nanowires growing out and merge to form L-junction-like (green) structures
- Fig. 79 (c): T-like junctions (yellow) form when one nanowire grows into the other wire and merges, in this case one nanowires grows faster than the other
- Fig. 79 (d): The desired Josephson junction is formed, when two nanowires closely cross each other and the shadow of the top wire is cast on the bottom. The Al half-shell is deposited on the three facets of the nanowire and is smooth.

Even though for this thesis, only the Josephson junctions are of greater importance, nevertheless the X, L, T like junctions have been found to have great applications in terms of nanowire networks. Minghaun et al. [131] have used the L- type junctions as nanowire kinks for InP nanowires and studied the crystal structure of the kinks. On the other hand, Heedt et al. [94] have demonstrated that the nanowires grown on V-shaped grooves (similar to the X-like structures) on a Si (100) substrate, grow perpendicularly on the Si (111) facets, merge and form monocrystalline junctions. These structures have been proven to work far well

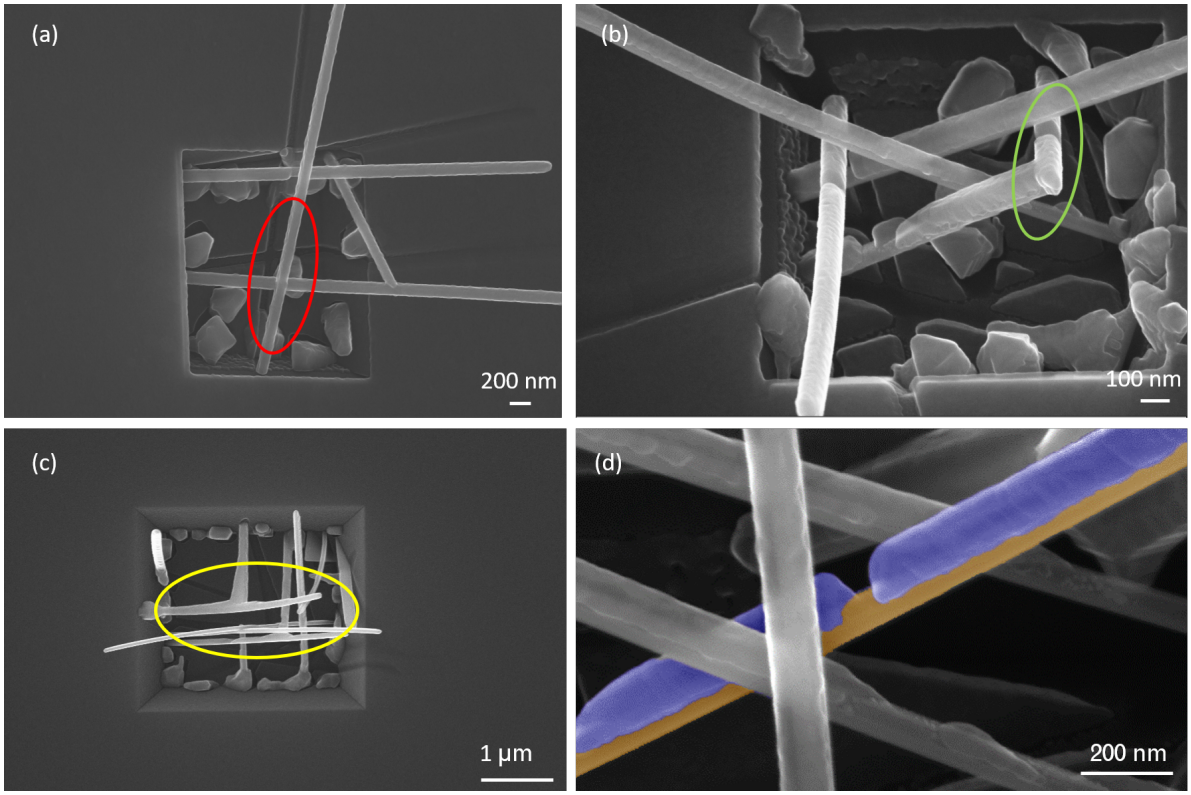

Figure 79: SEM micrographs of random growth of InAs/Al Josephson junctions. (a) X-like junction. (b) L-like junction. (c) T-like junction.(d) Close-up of one of the Josephson junction depicting a smooth Al shell (blue) of around 50 nm with a junction length (yellow) of 45 nm.

for electronic multi-terminal devices. The X-like structures have emerged from the concept of selectively growing nanowires on etched Si (111) facets of a Si (100) substrate has been first demonstrated by Gazibegovic et al. [33] for Majorana device applications. They have shown that, when two nanowires growing outward from the opposite Si (111) facets merge, the angle between is fixed, around 109.4 °. They established this by using InSb nanowires with an Al half-shell via VLS-growth with a gold particle catalyst. This forms an X-like junction, wherein the nanowires keep growing into their intended directions even after merging. This is attributed to the slight misalignment caused due to a small offset. Even if the offset is large enough, the nanowires look as if they are fused together when a shell larger than the offset is deposited on the wires. This can be often seen in nanowires with Al shells rather than Nb due to the enhanced Al diffusion at -6° C.
Figure 80 shows Al half-shells on InAs nanowire, depicts multiple islands due to shadowing of the two or more wires. The shell covers smoothly on three facets of the nanowire. The middle facet directed towards the metal deposition has a thickness of ≈ 50 nm. The Al thickness on the adjacent facets is 30 % smaller than the middle one and is around $32 - 35$ nm. The problem with Al deposition at $-6°$ C is the faster diffusion rate of Al, as seen in Figure 80 (a) and (b). The residual atoms can be seen in the weak-link area, and on the edges of the nanowire, where the film vanishes. The droplets in the junction area is not a continuous film of Al, but grains which have been later oxidized. This diffusion rate can be reduced by depositing Al at a lower temperature, typical temperatures range around -20 °C, or even at liquid nitrogen temperatures. The diffusion of the Al can also be tackled by capping the Al layer in-situ i.e. with aluminum oxides. This dielectric layer on the top forms a compact layer

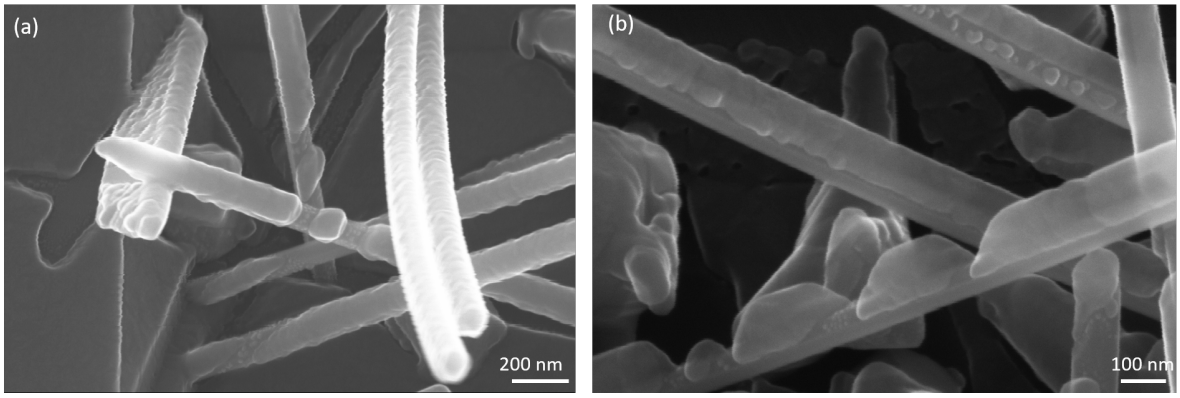

Figure 80: SEM micrographs of the weak-link formed by shadowing in the random growth process. (a) Nanowire with multiple weak-link, and the Al droplets visible in the weak-link areas. (b) Shows Al droplets on nanowire side facets.

around nanowire, thereby stopping the diffusion. The first results of the dielectric capping of the Al and Nb half-shell samples have been presented in the outlook section. The first experiments for the deposition of the Al shell for 40 s have resulted in a thickness of 50 nm, as seen in Fig. 80. The Al layer thus formed is smooth and a closed film. The further attempts have been to reduce the Al thickness to 25 nm. This reduces the time of exposure to the metal deposition to 20 s. The 25 nm layer is just as beneficial as the 50 nm layer for a good functioning of the Josephson junction device. The results of the thinner Al layer i.e. 25 nm can be seen in Fig. 81 (a) and (b). The half-shells covered three facets of the nanowire and the thickness on the middle facet is around 25 nm and the adjacent facets have an Al layer of $\approx 16 - 18$ nm. The metal shell deposition occurred from the left top corner of the trough to the right bottom of the troughs, as seen in Fig. 80. The shadows seen, depict the direction of the metal deposition. It has also been observed that the thicker Al shells i.e. more than 25 nm are generally smoother [32]. The Al half-shells grown using this process show similarities with Al shells on InSb nanowires, grown by Gazibegovic *et al.* [33]. They have reported no traces of residual Al droplets in the weak-link area. This is due to the substrate temperature during the Al deposition which occurred at liquid nitrogen temperatures, thereby reduced the diffusion rates of Al. Furthermore, to analyse the semiconductor and the superconductor interface, STEM-EDX studies are presented in the TEM analysis section 8.3.2.

8.3.2 Selective Area Growth

The key requirements to achieve a proper Josephson junction is that the junction formed by shadowing should be perpendicular to the nanowire, in the middle at best. The junction must also be free of any residual metal droplets. The nanowires potentially have to be grown from the right Si facets i.e. Si (111) so that the wires procures a right direction to cause a shadow on the other wire on the adjacent Si (111) facet. Additionally, samples without parasitic growth also makes it easy for nanomanipulation. Nanomanipulation involves identifying specific nanowires (with junctions) and transferring them onto a different substrate by using micro-sized needles in the SEM. This inspires the selective-area approach, which has already been discussed in the substrate analysis chapter. The holes are etched on the adjacent facets, wherein the placement of one hole is fixed on one facet and the other facet is placed with an offset. SEM micrographs of the results of different placements are presented in the supplementary section,

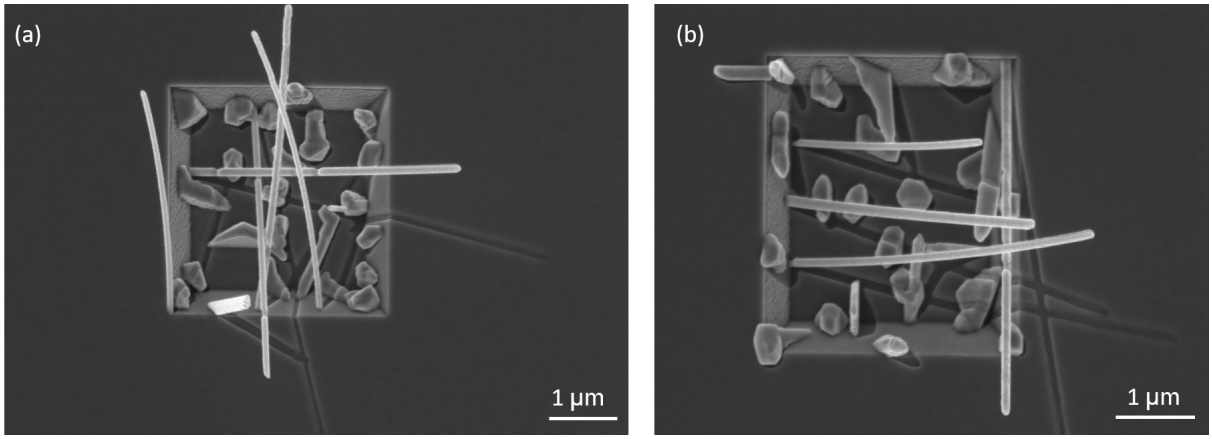

Figure 81: SEM micrographs of the InAs/Al Josephson junctions with 25 nm Al half-shells. (a) and (b) show an overview of the thinner shells and depict the smoothness. The metal deposition occurred from top left corner to the bottom right corner of the 3 μm square trough (shadows traced).

as this could be used as an further extension towards networks but right now the focus is on the wires obtained in Fig. 82. Since we have already established Al half-shells with 25 nm, the next attempt was to have much thinner shells i.e. with 15 nm. It has already been reported by Güsken *et al.* [32] that the aluminium shells with thickness more than 25 nm are generally smooth, besides this we made an attempt for thinner shells. Since the reduced Al thickness i.e. 15 nm, helps in enlarging the critical fields of the Josephson junctions.

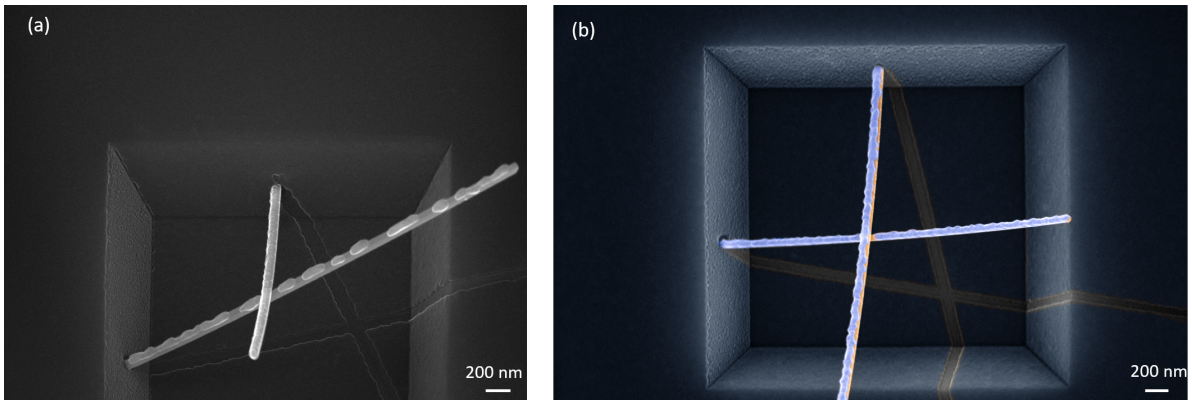

Figure 82: SEM micrographs of the SAE grown InAs/Al Josephson junctions. (a) 30 ° titled micrograph depicting the uneven film formed on the bottom wire, granular structure at 2.5 $\times 10^{-5}$ mbar of Al pressure. (b) SEM micrograph taken from top, shows a complete film of Al half-shell on the sample grown at Al flux of 1.5 $\times 10^{-5}$ mbar.

The first attempt at the selectively-grown Josephson junctions can be seen in Fig. 82 (a). The hole on the left facet is placed 100 nm away from the centre of the facet and the hole on the top facet is placed right in the middle of the facet. The nanowires are grown with the same parameters as mentioned in the random growth section. This resulted in nanowires which are $4 - 5\,\mu$m in length i.e. longer than the side of a 3 μm square trough. The parameters are similar to that of randomly grown nanowires, except that the substrate temperature is reduced to -9 ° C and a shell of 15 nm of aluminium is deposited at 45 ° in plane to the substrate. This is broken down as the angle between the Si (111) facet and the Si (100) plane below is fixed at 54.7 °. Hence, the nanowires grow almost perpendicular to this elevated Si (111) facet. This

makes the axis of the bottom (the one that is shadowed) to be projected at 87 ° to the metal flux direction. The nanowire on the top acts as a shadow casting structure, which later will be removed during the nanomanipulation. It is important to note that both nanowires are inclined toward each other by an angle of 10 ° each. This is the main reason why the junction shifts toward the bottom wire.
The metal deposition depicted in Fig. 82 has taken place from left top corner to the bottom right and the shadows depict the direction of the flux. The higher flux of 2.5 $\times 10^{-5}$ mbar for 20 s resulted in an inhomogeneous layer of Al half-shell on the bottom nanowire, as seen in Fig. 82 (a), which is due to a fast flux rate for a thinner shell of 15 nm. It can be seen that the Al adatoms diffuse along the nanowire, forming big grains and a non-closed film. This is attributed to the incoming Al beam flux i.e. the diffusion length of the adatoms increases with the Al pressure, which was reduced for the later experiments. The increased diffusion length of the adatoms, makes the Al to diffuse along the nanowire forming bigger islands. Generally, shells with a thickness of 25 nm or above have not exhibited the non-uniformity of the film due to the Al adatoms coalescence, thus forming a closed layer. There is a critical thickness parameter for the shell thickness to be uniform and closed. This depends on the diffusion lengths of Al adatoms and their ability to fuse together. Thereby, the partial pressure of the Al cell has been reduced to 1.5 $\times 10^{-5}$ mbar which is 1.6 times lower than the previous parameters above, thus decreasing the diffusion lengths of the Al adatoms. The Al deposition rate on the nanowire is 0.162 nm/sec. The deposition time has been adjusted to 80 s to achieve 15 nm, of Al shell. The result can be seen in Fig. 82 (b). It can be clearly seen how the Al adatoms diffuse along the wire to form a continuous film. One finds distinct lattice orientations of the Al islands, which have just begin to grow bigger and merge. Contrastingly, for thicker Al shells the islands form and merge, and the additional flux of Al, keeps forming a layer on top of the previous layer and covers up the grain orientations. Hence, figure 82 (b), shows the different grain orientations of the Al, presenting the roughness of the 15 nm Al layer. The selective area growth samples have a reproducible yield of 75%. It was quite evident that for shells less than 15 nm, the incoming Al beam flux plays a crucial role and the diffusion lengths of the Al adatoms depends on it. Moreover, the interface between the InAs and Al half-shell has not been compromised. The details of it showing high transparency greater than 80% will follow in TEM and low temperature transport measurement analysis.

8.3.3 Transmission Electron Microscopy Analysis

The key to a good Josephson junction lies in the details i.e. the quality of the interface between the semiconductor and superconductor and also on the roughness of the superconductor material. The interface between the semiconductor and superconductor has to be highly transparent. It is greatly considered to have a smooth superconductor shell. This enhances the contact of external superconducting leads on the half-shell. In order to analyze the InAs-Al core-half-shell nanowires with 25 nm shells, scanning transmission electron microscopy (STEM) was adopted by H Aruni Foneska and Ana Sanchez at University of Warwick, UK. Nanowires on the growth substrate were transferred to holey carbon Cu grids by smearing it off. The InAs nanowires grown by the catalyst-free method have a polytypic crystal structure with several defects. Figure 83 (a) shows an STEM image of a FIB prepared cross-section of nanowire. There are two predominant Al grain orientations present with a clear grain boundary. These findings are similar to that of Krogstrup *et al.* [31]. Figure 83(b) shows a low magnified image of a half-shell nanowire with two predominant Al grains. The Al layer evaporated is uniform

along the length of the nanowires and is continuous [31]. Al thickness from the cross-sections can be observed and it shows that the thickness is varied by 30 ± 2 nm, around the facets, as seen in Fig. 83 (c). The balling up of Al i.e. the granular coarse structure as seen in fig.8.5(b), is related to the relatively high deposition temperature (-6° C). A similar tendency although has been observed at -30° by Krogstrup *et al.* [31] and there by decreasing the temperature further more to -120° C [88], a conformal deposition was obtained. The maximum thickness of the Al layers on these Josephson junctions is around 30 nm. The Al half-shell consists of large grains (> 25 nm) with three different orientations. Two differently oriented Al grains can be observed in Fig. 83 (c) [126]. The predominant grain orientations include $(\bar{1}\bar{1}\bar{2})$, (110) and (111). These orientations are different from the previous works reported in references [26, 31, 124], but consistent with the work of our group [73]. In our case, this is attributed to the Al diffusion at higher temperatures which leads to different grain orientations, which are formed due to a low surface energy at this substrate temperature, and to minimize the strain [31].

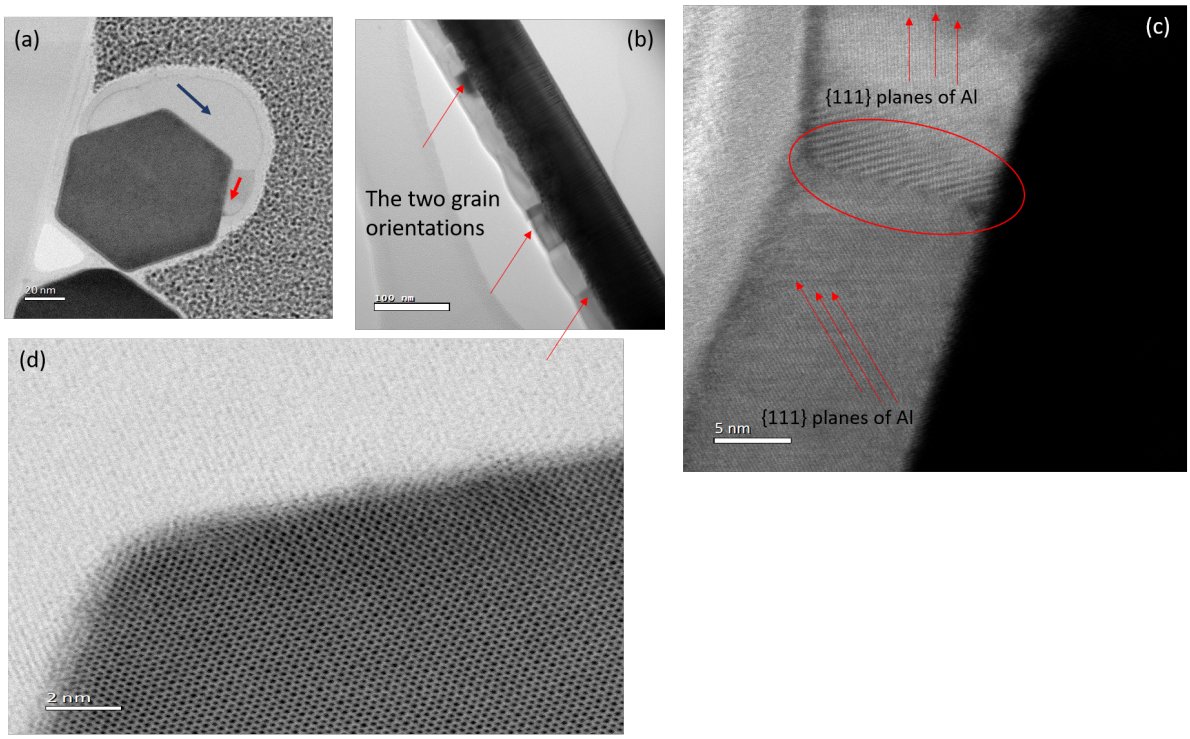

Figure 83: (a) Bright field (BF) STEM image of a nanowire cross-section depicting the Al half-shell. Red and blue arrows depict different grains. (b) BF scanning transmission electron microscope (STEM) image of the nanowire with two predominant aluminium grains marked (contrast of the grains changed due to their orientation). (c) High magnified STEM image of Al grains, grain boundaries can be seen in the red circle marked where the two grains meet and gives out a Moire pattern. (d) High resolution image of the InAs-Al interface [126].

The Al grains seem to be independent to the phase change of the InAs nanowire. That means the stacking faults within the InAs wire do not disturb the crystal structure of the Al. A high magnified TEM image of the interface between the Al and InAs can be seen in Figure 83 (d), the interface is sharp and smooth, with no defects. There has been no evidence of AlAs layer in between. The desorbtion method sucessfully eliminated the AlAs. As for the STEM analysis is concerned there has been no evidence supporting an AlAs layer as thick as 2.5 nm in energy dispersive x-ray (EDX) data.

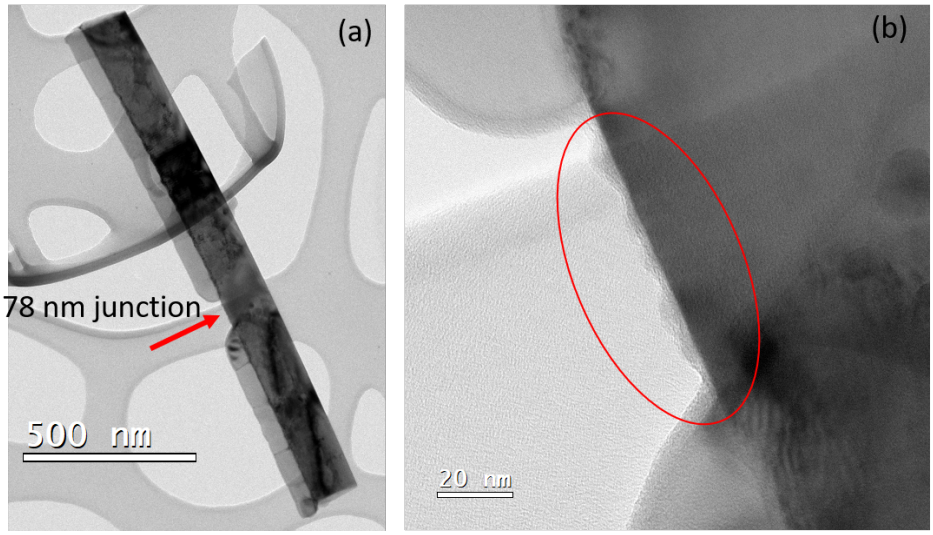

Figure 84: (a) Bright field image of the weak-link on the naowire with Al half-shell showing a 78 nm long weak-link and the smooth film of Al. (b) Magnified bright field image of the weak-link showing the oxidized Al droplets.

Apart from the Al crystal structure, the junction has also been analyzed. Figure 84 (a) shows a bright field STEM nanowire with Al half-shell with a 78 nm long junction. The weak-link was observed to have few small, droplets of Al that are oxidized, which was also observed in the SEM micrographs. These oxidized Al droplets can be seen clearly in Fig. 84 (b) (indicated by red circle in the image) . This is attributed to the high diffusivity of Al grains at -6° C. This problem can be tackled by e.g lowering the substrate temperature or by capping the Al (the results of this will be shown in the outlook chapter). However, a quick rinse in transene D, etches away aluminum oxide and the residual Al in the junction area and there was no evidence of parallel metallic bypass that is observed in the subsequent low temperature transport measurements.

8.3.4 Low Temperature Transport Measurements

Low temperature transport measurements, on the in-situ Josephson junctions are performed at RIKEN, Japan. The advantage of using the fully in-situ prepared Josephson junctions is that the impurity free interface provides a high contact transparency, which is ascertained by the basic junction characteristics i.e. by excess current measurements and the hard-gap spectroscopy. All etching and metal-evaporation steps are performed with the aid of standard e-beam lithography techniques. These substrates are equipped with gate electrodes, made of Ti/Au (5 nm/10 nm). The nanowires is laid on a gate stripe pattern where in the middle gate is electrically connected and the others provide a mere mechanical support for the wire. Subsequently, the whole substrate is covered by a ALD grown dielectric layer, that consists of 3 nm/12 nm of Al_2O_3/HfO_2. A transmission line is used which supports both AC and DC measurements. It is terminated by an on-chip bias tee [126]. These components are prepared using titanium nitride (80 nm, sputtering performed at room temperature). The nanowires were later transferred onto the electrostatic gates by an SEM-based micro-manipulator setup. To achieve an ohmic coupling between the contacts, NbTi, and the Al shell, a combination of a wet-chemical etching and dry etching is used. The contact separation is chosen to be 1.5 μm in order to reduce the effects of the wide contacts made by superconductor NbTi on

the actual weak-link Josephson junction characteristics [126].

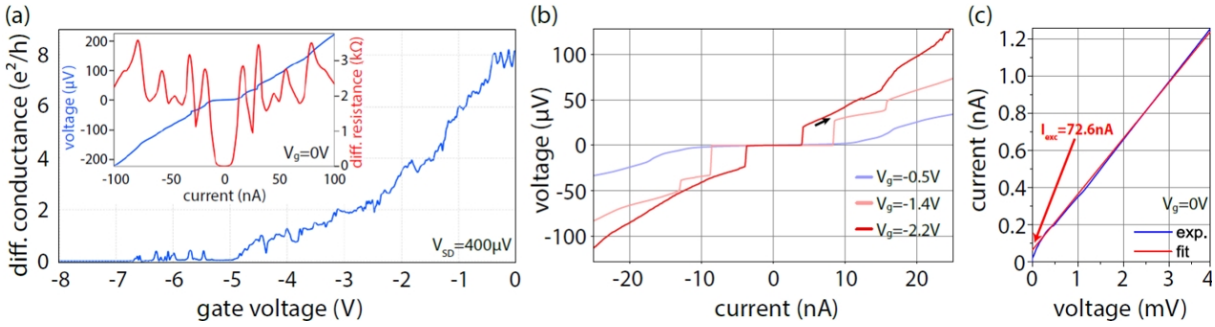

Figure 85: (a) Conductance G vs. gate voltage (voltage-driven setup), shows a consistent voltage drop of 400 μeV. The inset shows the (IV) characteristics at zero gate voltage, a supercurrent of 21 nA can be observed. The differential resistance curve consists of peaks and these are signatures of subharmonic gap structures. (b) IV curves at gate voltages of -0.5, -1.4, and -2.2 V, respectively. (c) (IV) Current-voltage characteristics at $V_g = 0$ V that is extrapolated to large bias voltages [126].

A He3/He4 dilution refrigerator at 15 mK is used for the low temperature electrical measurements. $I - V$ measurements are traced with a current bias supply from a battery-powered current source and the voltage measured with a battery-powered differential voltage amplifier. The gate response, is due to the semiconducting weak-link segment on the nanowire Josephson junction. Figure 85 (a) shows a full gate sweep for one of the Josephson junction i.e. conductance of the junction in a voltage-biased configuration is plotted. A constant voltage drop of 400 μeV is observed across the junction. Nanowire is seen to be completely pinched off for voltages below -6.7 V. The plot in Fig. 85 (a) gives an entire spectrum of the evolution of the nanowire into different regimes. Above these values a single electron transport is observed and is further realized in Fig. 86(a). Above -5 V, gate voltages, the nanowire opens up, wherein its conductance limited by a low-transparency tunnel coupling to the electron reservoirs in the contacts. The conductance has increased by $2e^2/h$ within the range of -5 to -3 V. Finally at gate voltages above -3 V, the (IV) characteristics show a classic Josephson junction behaviour with a supercurrent response, as seen in Fig. 85 (a) inset. The corresponding differential resistance curve shows signatures of the subharmonic gap structures [126, 132, 133]. The IV curves are also plotted with different gate voltages, in the Josephson junction behaviour region of -2.2 to -0.5 V. It is observed, that the switching current of the Josephson junction device can be tuned. The additional constant-voltage-sections arise due to self-induced Shapiro steps (due to the circuit design). At gate voltage of $V_g = -0.5$ V, a critical current of $I_c = 11$ nA and a normal state resistance of $R_N = 6.33\,\mathrm{k\Omega}$ is observed, with I_cR_N product of 70 μV. While, other two IV curves at -1.4 V and -2.2 V resulted in an I_cR_N=72μV and 75μV with $R_N = 8.7\,\mathrm{k\Omega}$ and $11.8\,\mathrm{k\Omega}$, respectively [126].
The observed I_cR_N product varied slightly for the three different gate voltages measured even though the normal state resistances are higher. The excess current in the Josephson junction is attributed to Andreev reflections and is a measure of the interface transparency. Figure 85 (c) shows IV characteristics with larger current biases. By extrapolating the current voltage curve in the range $V > 400\,\mu$V a finite current I_{exc} of 72.6 nA is extracted. From the theory of Octavio–Tinkham–Blonder–Klapwijk [132–134], a ratio of $eI_{\mathrm{exc}}R_N/\Delta = 1.31$ is obtained at zero gate voltage, which results in a barrier strength of $Z = 0.38$ and a corresponding contact transparency $\mathcal{T} = 0.88$ [126].
These values are quite comparable to values that are obtained for hydrogen-cleaned supercon-

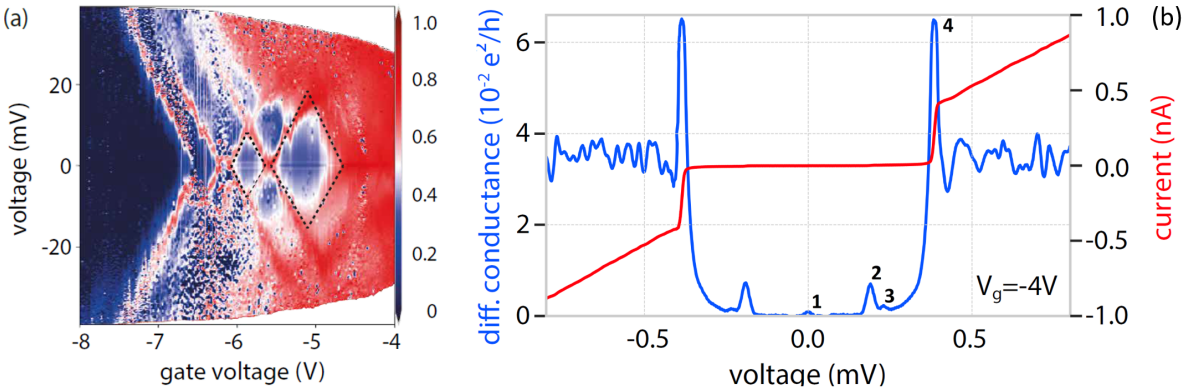

Figure 86: (a) Gate-response of the nanowire for gate voltages between -8 and -4 V, shows a set of Coulomb diamonds (indicated by the black dashed lines). (b) Voltage-driven tunnel spectroscopy measurement of the junction at $V_g = -4$ V [126].

ductor/nanowire junctions, i.e. Al/InSb [33] and NbTiN/InSb [135].

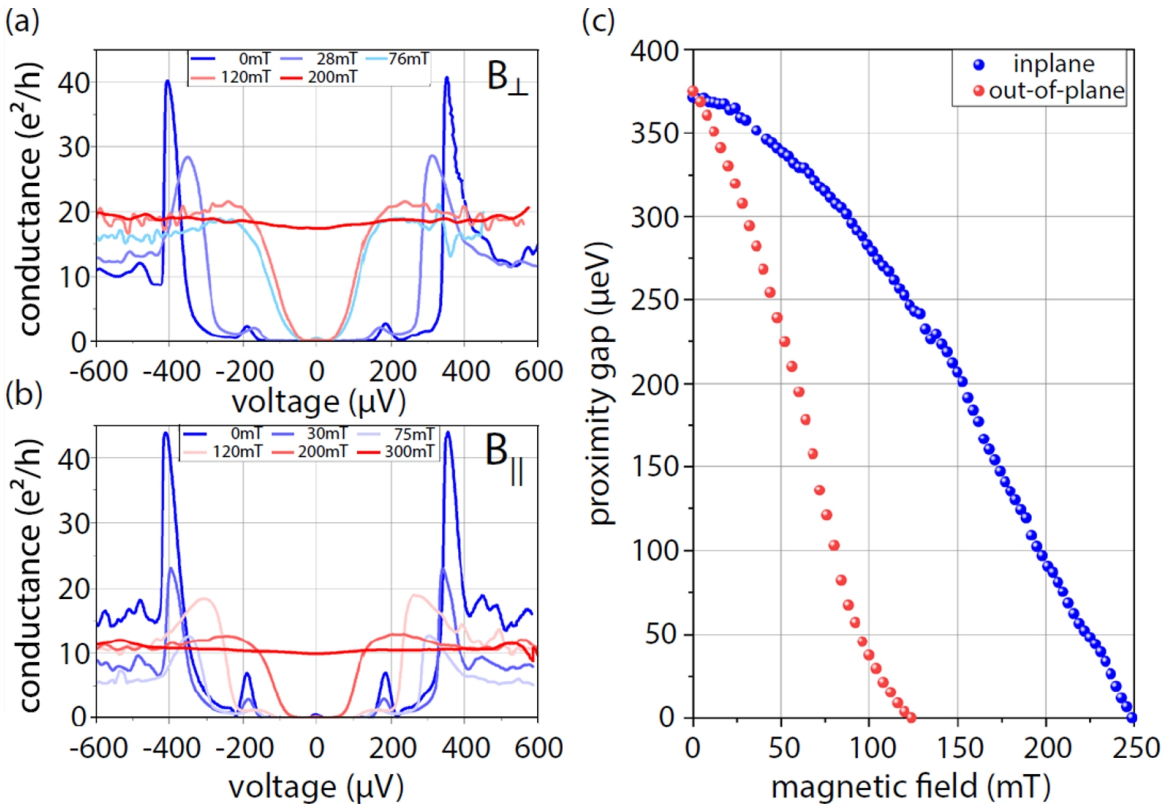

Figure 87: Differential conductance curves as a function of bias voltage for different magnetic fields w.r.t to nanowire axis (a) shows a perpendicular field (b) shows a parallel field. (c) For magnetic fields between 0 and 250 mT, the width of the proximity gap 2Δ is realized [126].

Figure 86 (a) illustrates the above mentioned Coulomb blockade features which is a sign of a single quantum dot in the weak-link region. Figure 86 (b) gives the information of the induced superconducting gap, where the differential conductance plotted against the voltage in the tunnel regime. This is obtained by applying a negative gate voltage to the NW junction which drives the device into the tunnel-limited regime [136]. There are several features seen

in the gap, these are numbered. It can be seen that there are small peaks in between the two dominant peaks (4). These peaks are as follows (1), is the superconducting state, (2) and (3) correspond to sub-gap structures. The proximity gap observed here is $2\Delta = 380\,\mu$eV. This has also been observed by Chang *et al.* [137] in their tunneling experiments. Proximity effect created an induced gap in the InAs nanowire. The Josephson junction is formed by two proximitized nanowire segments, that are separated by tunnel barrier, therefore 2Δ is measured. The Δ value is comparable to the bulk Al gap ($\Delta_{Al} = 200\,\mu\mathrm{eV}$) [138] is a sign of a good coupling between Al and InAs. A strong decrease of conductance between peaks (4) and (2) by $G/G_N \approx 0.02$ has been observed. It further dropped to $G/G_N < 0.001$ between peaks (2) and (1) [126]. This behaviour is a clear indication of a hard gap [136, 137, 139]. Another benchmark to assess the quality of a Josephson junction is verifying the robustness of the device towards a magnetic field. Figures. 87 (a) and (b) depicts the conductance vs. bias voltage for an out-of-plane field orientation and for a parallel field orientation. Figure 87(c) shows a plot of magnetic field against the width of the proximity gap 2Δ between 0 and 250 mT. The energy gaps were calculated using the first derivative of the differential conductance. A critical field of B_c=130 mT is calculated for an out-of-plane orientation, contrastingly for the in-plane field orientation a B_c=250 mT is observed. It is quite evident that both the in-plane and out of-plane measurements show a typical damping and smearing out effect of the gap edge peaks. In conclusion, the Al/in-situ Josephson junctions proves to be promising in terms of gap-hardness, gate tunability of the junction, interface transparency, and magnetic field resilience [126].

8.4 InAs/Nb Nanowires

8.4.1 Random Growth

Niobium is an intriguing superconductor, since it can withstand magnetic fields greater than 1.5 T and higher temperatures. Thus this resilience, piqued interested in the Josephson community to have Nb as a superconductor, complementary to Al. Nb is not easily compatible with wet chemical etching agents to create junctions. Hence, the shadow evaporation method of creating a in-situ junctions offers much more control over Nb. Junctions smaller than 45 nm with Nb have been achieved through this method. Firstly, for the proof of concept, the random growth was performed. The InAs nanowires are grown in a similar way as mentioned in the InAs nanowire chapter. The Nb flux parameters have been optimized to 2×10^{-9} mbar for 180 seconds to achieve a 25 nm half-shell at a substrate temperature at 50 °C [32]. The corresponding results of the random growth can be seen in Fig. 88 where the Nb is transparent on the InAs and reveals the hexagonal structure of the InAs nanowire facets. Figure 88 (b) shows Nb half-shell free of Nb droplets and the edges of the shell are much sharper than Al. Niobium adatoms have a slower diffusion rate compared to Al at 50 °C. This makes the Nb adatoms to form large fragments. Also, slow diffusion rates helps Nb to form a homogeneous and a continuous films. It has been already established that for Nb, the direction of deposition plays a major role in the smoothness of the film rather than the substrate temperature [73, 140]. Bending of the nanowires has also been observed due to the lattice mismatch of InAs and Nb. This phenomenon is found to be more pronounced in Nb structures than in Al ones. InAs has a lattice parameter of 6.05 Å, while it is 4.05 Å for Al and 3.04 for Nb it compounds to Nb having a larger mismatch when compared to Al, resulting in a stronger bending. Nevertheless, a slight bending of the nanowires during Al deposition has also been observed [31, 84].

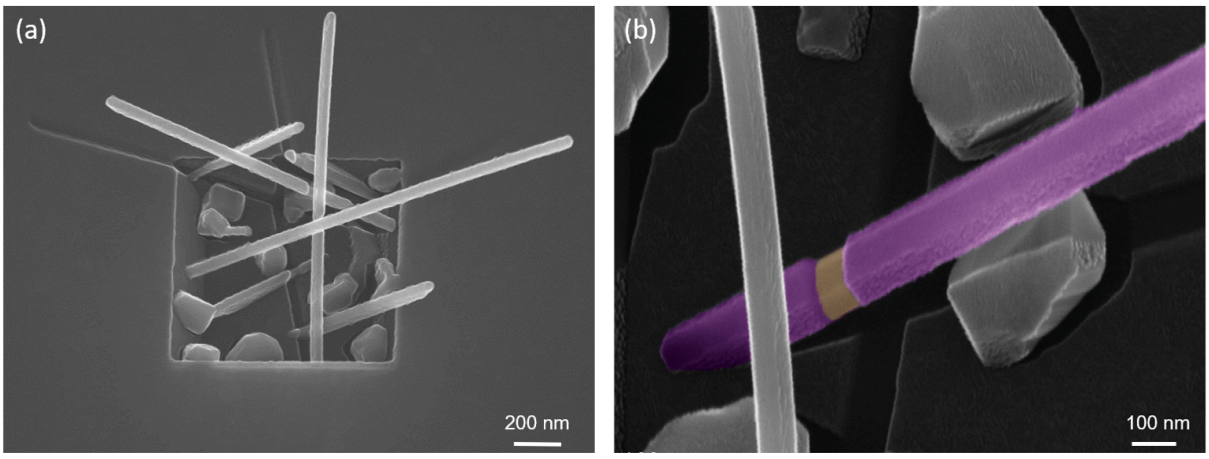

Figure 88: (a) Randomly grown InAs/Nb nanowire Josephson junctions in a 3 μm square troughs the Nb metal deposition occurred from down right corner to the top left corner of the trough (shadows traced). (b) Close-up of the weak-link formed on the InAs/Nb Josephson junction, the 25 nm thick Nb, is transparent on the InAs core reveals the hexagonal (110) facets.

8.4.2 Selective Area Growth

The samples with the selective area growth give the nanowires a greater edge, with Nb deposition in terms of positioning the junction on the nanowire and eliminating parasitic growth. The tilted facets of the troughs, in turn increases the deposition angle to the nanowire. The calculated angle is around 87° with respect to the nanowire axis. This is an additional benefit, which makes the Nb adatoms on the nanowire to diffuse slower and form smooth and large fragments, before they merge to form a closed and compact film. The samples with selective area growth with Nb shell deposition can be seen in Fig. 89. The nanowires are slightly bent inwards due to the lattice mismatch of Nb with InAs. In Fig. 89 (c) it can be seen that the Nb half-shell covers three facets of the nanowire. This SEM mcirograph is a 30 ° titled image which clearly shows the junction formed with two Nb metal segments on the InAs nanowires. A 45 nm wide junction has been formed which is not possible via chemical etching, which makes this method quite attractive and promising. The intended thickness of Nb was 25 nm and this turned out to be $\approx$ 22 nm thick on the middle facet (the facet directed toward the metal flux). This constitutes relatively bigger grains of sizes ranging from 15-30 nm making the film homogeneous and a complete.
The two adjacent facets of the top wire are much more grainy when compared to the wire with the junction below. This is due to the higher deposition angle on the lower wire when compared to the top wire. This is clearly visible in Fig. 90, the SEM micrographs are 30 ° tilted, and show a large contrast in the grain sizes on the side facets of the top and bottom nanowires. This is attributed to the steep angles of deposition on the side facets of the nanowire, resulting in column-like growth.

8.4.3 Transmission Electron Microscopy Analysis

The TEM analysis for these samples has been done at University of Warwick. For the side view analysis, the holey carbon grids are rubbed against the nanowire array substrates. The cross sections were prepared using FIB. The EDX measurements were performed using an Oxford Instruments detector and a Jeol ARM 200F (also used for microscopy). Figure 91 shows the

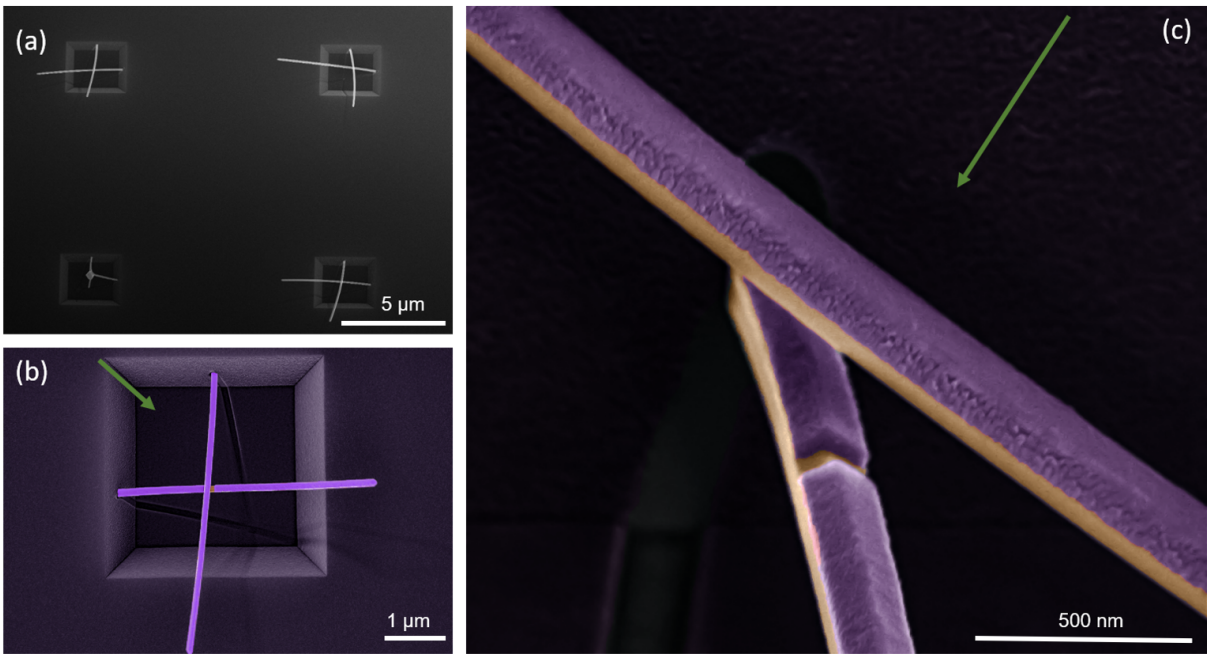

Figure 89: (a) Four troughs with selectively grown Nb covered InAs nanowires. The yield is about 75%. (b) The Nb meal deposition in the 3 μm square troughs. The green arrow showing the direction of the Nb metal flux, the left and the bottom Si (111) facets are smoother and the top and the right Si (111) facets are rougher, due to the directional Nb metal evaporation (pink). (c) 30 ° tiled SEM micrograph, showing the close-up of the weak-link formed on the Josephson Junction, this also depicts the 87 ° between the nanowire axis and the direction of the Nb metal flux on the middle facet [127].

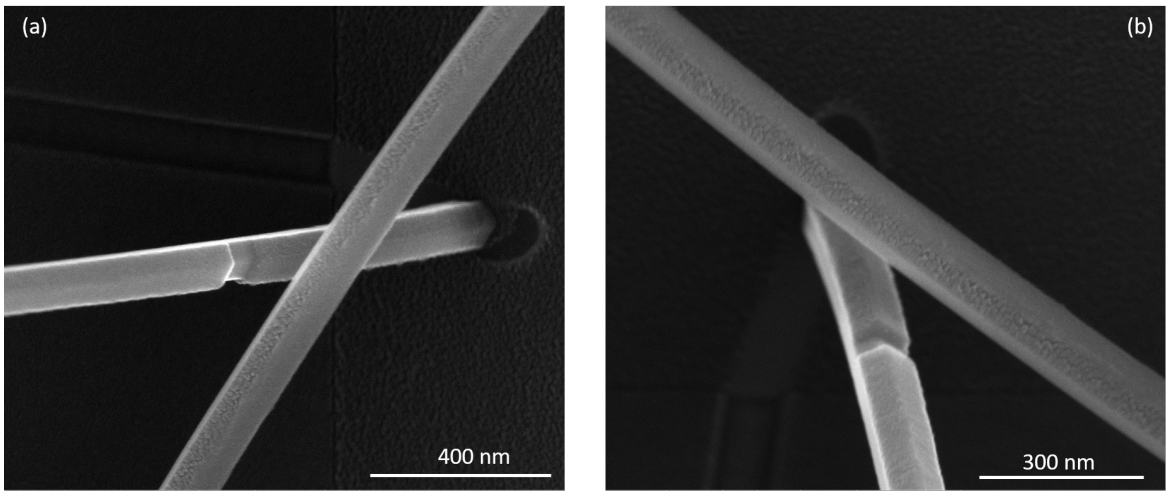

Figure 90: (a) SEM micrograph (30° tilted) of the two nanowires placed to form a junction. Top wire has grainy facets. (b) Contrast seen in the grains of adjacent facets of the top and the bottom wires. The bottom wire with the junction has smoother adjacent facets.

first side view results of the Nb shell on InAs nanowire, (a) shows the whole nanowire with Nb as a shell, the red box indicates the inspected area shown in (b). Figure 91 (b) shows the magnified Nb shell part, depicting different grains along the length of the shell and the grain boundaries depicted in broken lines. Figure 91 (c) shows the dark field images of the different Nb grains, the one on the zone axis is coloured dark and the other out of the zone axis is the bright coloured one. Figure 91 (d) depicts several columns like grains oriented in

different directions and there are more than two, unlike Al, furthermore (e) shows a bright field scanning transmission electron microscope (STEM) image of a Nb-InAs junction. In Fig. 91 (f) energy dispersive x-ray (EDX) can be seen, it is superimposed on the annular dark field (ADF) image. The junction width measured is about 55 nm and the area is clean and free of any residual metal atoms. The nanowire has been uniformly covered with a thickness of 22 nm with a ± 2 nm variation along the nanowire.
The side-view analysis of the nanowire also shows a polytypic crystal structure of InAs nanowire with wurtzite (WZ) and zincblende (ZB) segments, with high density of stacking faults, can be seen in Fig. 91 (a). The polytypic structure of the nanowire has no influence on the metal grains orientation.

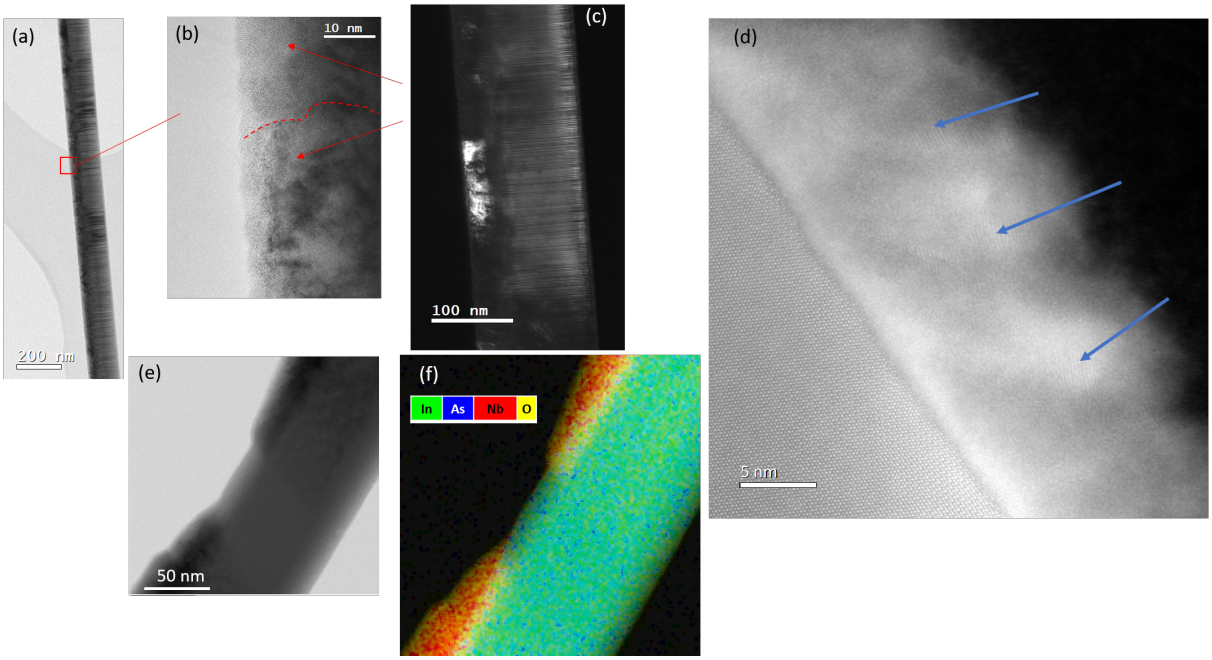

Figure 91: (a) TEM image of the InAs-Nb nanowire side view, marked in red is the probed area in (b). (b) High magnified bright field TEM image of the nanowire revealing the different grains and the grain boundary depicted in the dotted red line. (c) Dark field image of (b) depicting the Nb grains, that are smaller than 12 nm. (d) High magnified bright field image of the InAs core and the Nb half-shell, blue arrows depicting the different Nb grains. (e) Bright field STEM images of the junction with two separated Nb electrodes. (f) shows the corresponding ADF superimposed with EDX elemental map of (e). Both images show the clean junction without any impurities [127].

The niobium metal evaporated is polycrystalline all along the nanowire with small column-like grains oriented in more than two directions. An amorphous layer is seen in the Fig. 92 (a). It shows a higher magnification of of the InAs-Nb interface revealing a $\sim$1 nm thin and uniform amorphous layer along the wire. Figure 92 (b) shows the InAs-Nb interface scanned by EDX. The line scan of the amorphous region, that is present at the interface, contains a high percentage of As and shows a decreasing behaviour in the curve. The In curve behaviour is slightly different than As, as it initially behaves like As, but there appears a sudden increase that is little beyond the interface (red arrow depicts the hump) before it drops down. The increase in the In can be accounted to the stable formation of Nb and As. This stable compound has a tendency to push In away, towards the interface. This could be a possible reason for the In hump in the curve. The amorphous layer is comprised of As: 25-40%, In: 5-20% and,

Nb: 45-60% (considering only Nb, As and In). But it clearly is not a artefact, rather a diffusion in this region and it contains a higher percentage of As and Nb. It can be deduced from the ternary phase diagram of In-As and Nb at room temperature, from [141], and observed that there exists, no tie-line between InAs and Nb. This means that InAs and Nb form stable compounds, even at room temperature [141] due to the reactivity. Thus, the layer formed is amorphous due to diffusion. This has been observed in many other semiconductor-metal interfaces, that also have caused amorphisation [135, 142, 143]. The amorphous layer seems like a diffusion of Nb into InAs forming a Nb-In-As compound that is ascertained by the EDX line scan across the interface [127].

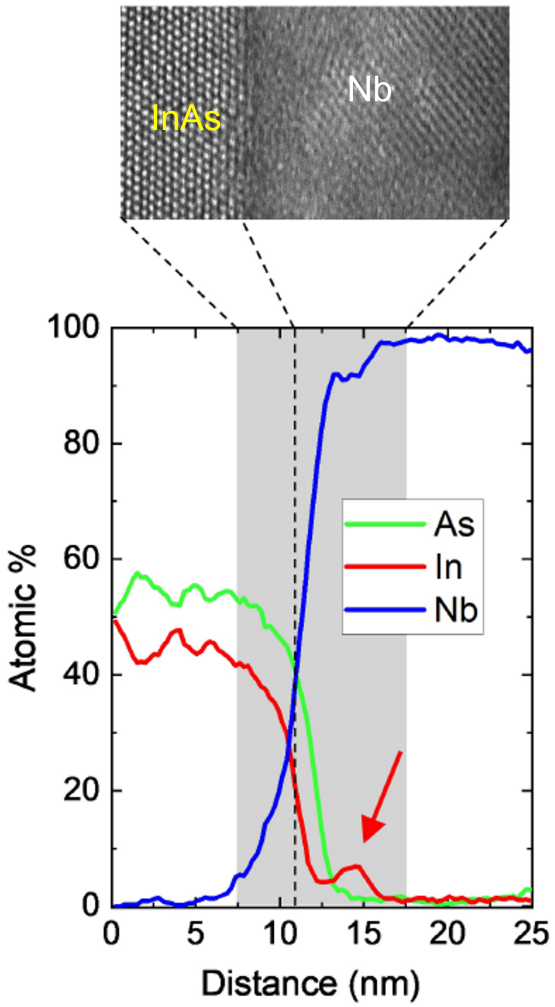

Figure 92: (a) Interface region of InAs and Nb in a high magnification ADF image. (b) EDX line scan profile along the yellow arrow in (a) shows the InAs probed in green is the interface and orange is the Nb. Also seen is the hump pointed (red arrow) indicating the presence of In in this interface [127].

Figure 92 (a) shows an ADF image of the cross-section, and a corresponding elemental map in (b). The nanowire cross section has Nb deposited on three of the six ($\{11\bar{2}0\}$ type) side facets. It is quite evident that the middle facet (red arrow) has a thick metal layer ($\sim$22 nm), and is smooth and consists of large grains of sizes $\sim 15 - 30$ nm. Contrastingly, the adjacent facets (marked in blue), show column-like growth with grains really less than 15 nm,

thus seen as grainy. This is due to a steeper deposition angle on these facets. This makes it looks a bit rough and grainy, and has a thickness of 16 nm. Nb metal on all the three facets of the hexagonal wire is polycrystalline in structure. The variation of the smoothness of the Nb film is due to the difference between the deposition angles on the hexagonal nanowire facets [144]. This results in a growth rate of 0.112 nm/sec on the middle facet where most of the flux is directed and on the adjacent sides the flux is reduced to 0.08 nm/sec. Due to the 120° orientation of the adjacent facets, makes the angle between the incoming metal flux and the nanowire facet smaller. This clearly explains that, the Nb growth rate on the adjacent facets is 28.6% less than that of the middle facet.
A further EDX scan is performed on the nanowire cross-section to make sure that the amorphisation is native to the nanowire sample, as seen in Fig 92 (c),(d), and (e). The bright field image of Fig. 93(a) shows a lighter ring around the nanowire, which is amorphous. Figure 93 (c) shows Nb in green covering the outer part i.e. the shell and creeping in towards the ring (amorphous layer). Figure 93 (d) shows In in yellow extending beyond the outer dark line. Finally Fig. 93 (e) shows the map of As distribution enveloping the nanowire and the ring completely. This proves that the diffusion has formed an amorphous layer constituting a stable In-As-Nb compound. One of the reasons for the In hump is that, the excess In from InAs has been expelled and segregated beyond the junction, thus forming an In rich band (hump in Fig. 91 (b)). The occurrence of many tie-lines between Nb_xAs_y and In/Nb_3In in the In-As-Nb phase-diagram [141], suggests that these compounds can also form at room temperatures. Several other reports have been mentioned similar effects, such as Pt-GaAs, where gallide formation occurred at metal interface [143]. Regardless, subsequent low temperature transport measurements do not show any significant effect from this amorphous layer, except that the transparency is lower when compared to Al.

8.4.4 Low Temperature Transport Measurements

To assess the quality of the in-situ Josephson junctions, low temperature measurements were performed in a similar way to that of Al half-shells. These measurements are performed at RIKEN, Japan. The Nb half-shells were contacted by NbTi while the junction, i.e. InAs part, is controlled by the bottom gate, that is used to manipulate the charge concentration. Figure 94 (a) depicts current-voltage (IV) curves at different gate voltages at 15 mK. A huge switching current of $I_\mathrm{c} = 75$ nA and a re-trapping current of $I_\mathrm{r} = 60$ nA, have been detected at zero gate voltage. These measurements are similar to those observed by Günel *et al.* [24]. Shapiro induced steps can be seen, at the left lower end of the graphs. This is due to the special architecture of the circuit geometry. For gate voltage of $V_\mathrm{g} = 7$ V, an increase in critical current of $I_\mathrm{c} = 133$ nA and a retrapping current of $I_\mathrm{r} = 67$ nA has been observed. At $V_\mathrm{g} = -7$ V gate voltages, the switching and retrapping currents are lowered to 40 nA and 25 nA, respectively. The values of the switching current of the largest voltage tripled in comparison to the smallest gate voltage applied. Figure 94 (b) shows the IV characteristics of the same junction for large bias currents. At a gate voltage of V_g=7 V an excess current of $I_\mathrm{exc} = 327.8$ nA and a normal state resistance of $R_\mathrm{N} = 2850\,\Omega$ have been deduced.
Unlike InAs-Al Josephson junctions, no complete suppression of I_c could be achieved for extended negative voltages in the case of Nb ones, i.e. no complete pinch-off of the nanowire segment. One of the reasons is that due to a changed Fermi level pinning at the interface, which could have caused an enhanced carrier accumulation. Additionally, the amorphous layer at the interface, i.e. the diffusion also would have aided to this process (also seen in the TEM

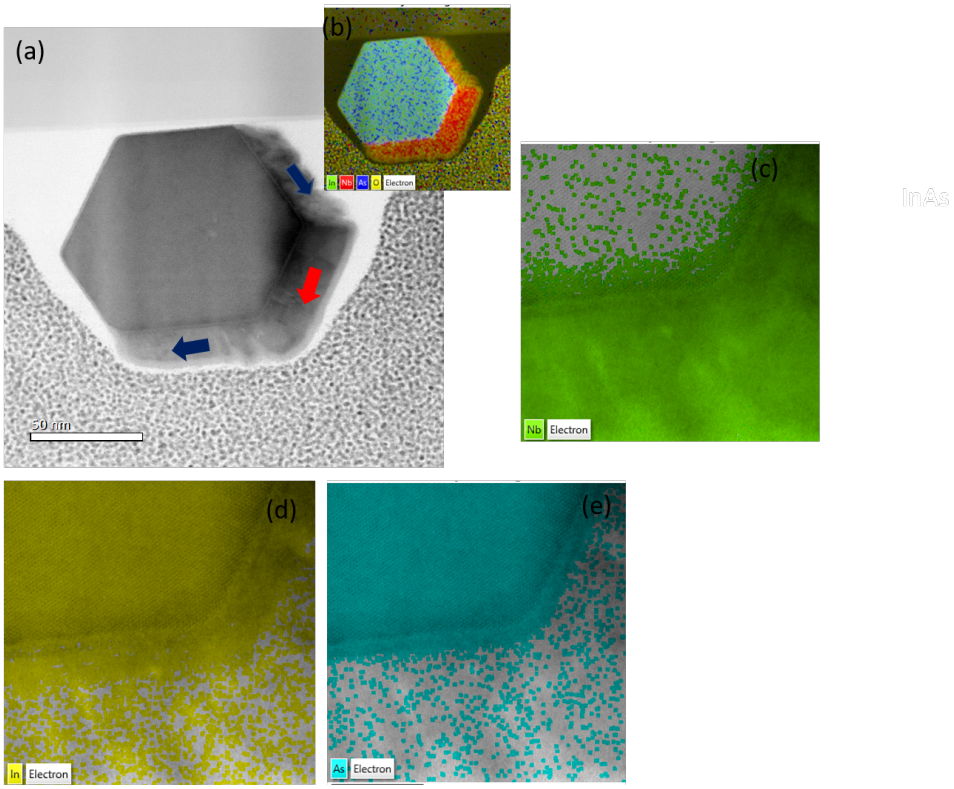

Figure 93: (a) Bright field image of a nanowire cross-section, with a corresponding elemental map in (b), depicts the nanowire cross section and Nb is deposited on three side facets (arrows). (c) Mapping of Nb in green and (d) In in yellow and (e) As in blue, all the three elements seen in the amorphous area.

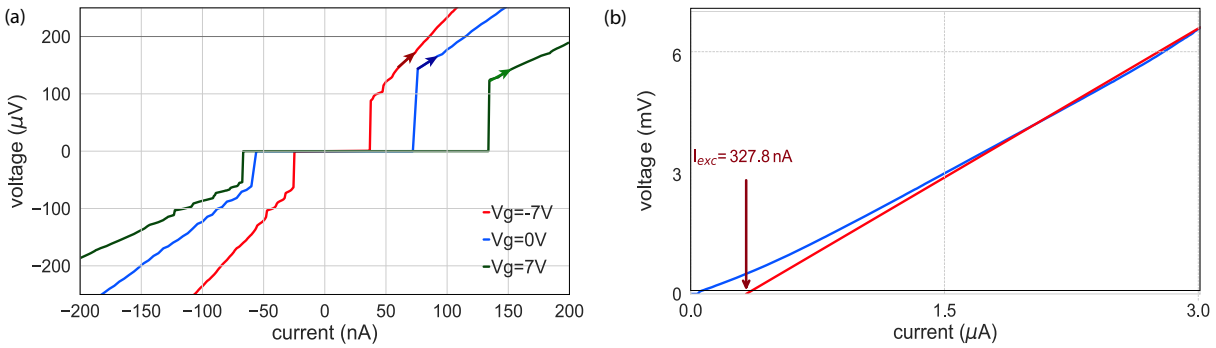

Figure 94: Current-voltage characteristics of an InAs/Nb junction measured at $V_{\mathrm{g}} = 0\,\mathrm{V}$, $-7\,\mathrm{V}$, and $7\,\mathrm{V}$. (b) IV curve of the junction at large bias currents at a gate voltage, V_{g}=7 V [127].

analysis). Because of the incomplete pinch-off, no tunnel spectroscopy could be performed to find out the hardness of the induced superconducting gap. Nonetheless, a robust supercurrent is observed across the junction due to the large superconducting gap of Nb.
The key factor here is the junction transparency, for this IV characteristics up to large bias voltages at $V_{\mathrm{g}} = 0\,\mathrm{V}$ are performed. This is done similarly to the InAs-Al Josephson junctions, where in the excess current is deduced from the linear extrapolation of the bias voltage range above the superconducting gap, $2\Delta/e$. From the excess current measurement, I_{exc} =327.8 nA and a normal state resistance of $R_{\mathrm{N}} = 2850\,\Omega$ is deduced and is fitted to the corrected Octavio–Tinkham–Blonder–Klapwijk theory [132, 133]. A ratio of $eI_{\mathrm{exc}}R_{\mathrm{N}}/\Delta$ =0.623 with a barrier

strength of $Z = 0.69$ is derived with an interface transparency factor of $\mathcal{T} = 0.68$. This has also been observed by Günel *et al.* [24] for nanowire Josephson junctions with Nb. The junction transparency is still considered to be large. It showed no detrimental effect at the interface related to the amorphous layer observation in the TEM analysis.

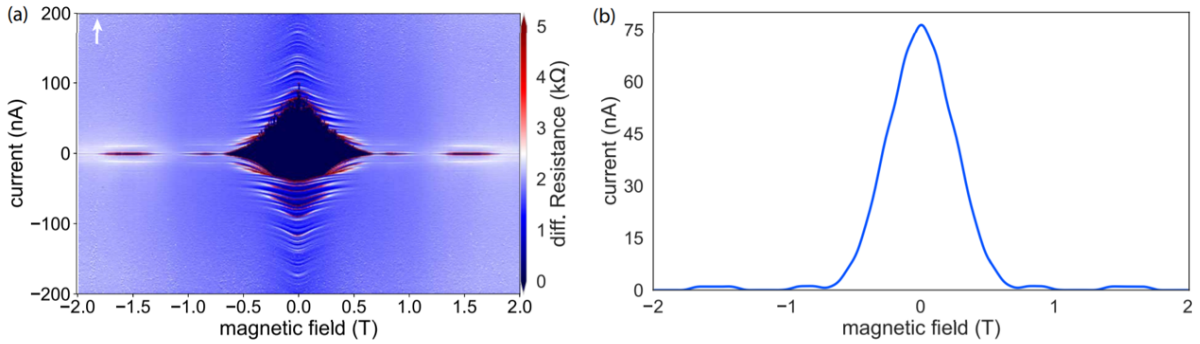

Figure 95: (a) Magnetic field dependent differential resistance for $V_g = 0$ V. The magnetic field is oriented in-plane along the nanowire axis. (b) Field-dependent magnitude of the switching current, evidently shows that the supercurrent re-appears for fields up to 2 T [127].

The in-situ Josephson junctions have to be tested against the magnetic fields. Since these are prepared by employing Nb, and Nb is known to have a higher resistance w.r.t a magnetic field compared to Al, i.e. the induced proximity gap can withstand fields greater than 1 T. The magnetic field measurements shown in Fig. 95 are the benchmark measurements to show robustness of the junction´s induced superconductivity against the magnetic fields. Figure 95 (a) shows the weak-link Josephson junction device response w.r.t to the change in differential resistance, when the applied magnetic field is parallel to the nanowire axis. A lobe-like pattern is found at zero magnetic field. It can be seen that at large magnetic field magnitudes i.e. ± 0.7 T, the supercurrent seems to be suppressed.
The strong asymmetry of the lobe-like pattern along the current axis at zero magnetic field is due to the difference in switching and retrapping currents. The stripes along the current axis at the zero magnetic fields are the self-induced Shapiro steps which have been arising also in Fig. 94 (a) at the retrapping branches. In-plane magnetic field measurements show that there is no clear decrease in the superconducting gap energy w.r.t the field, rather the device exhibits alternating sections with and without a super-current. As can be seen in Fig. 95 (b) that the device can also hosts Josephson super-current i.e. the lobe structure re-appears for a brief range of the magnetic field i.e >1 T and upto 2 T.
In summary, our results show that the junctions are highly transparent. There has been no residues of metal atoms, evident in the transmission electron microscopy. Besides the amorphous layer of In-As-Nb at the interface could have been the reason that the nanowire could not be pinched off at the negative voltages. The interface transparency of 0.68, is still large enough to show signatures of a Josephson supercurrent, this has also been quite comparable to Kaveh et al. [145] with a contact transparency of 0.7 and also has been realized by Günel et al. [24]. There has been no visible signs of the amorphous layer presence in the low temperature transport. Thus, above fabricated Josephson junctions seem to be promising for future quantum device applications.
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9 Summary And Outlook

Superconductor/semiconductor Josephson junction devices form an essential component for many of the electronic devices for quantum information [146–149]. These junctions can be used in topological qubits, gatable transmon devices, and Andreev qubits [15, 150–155]. The aim of this thesis was to realize highly transparent semiconductor/superconductor structures for Josephson junctions. This has been achieved in several steps, as summarized below:

- Self-catalysed InAs nanowire growth via vapour-solid mode has been optimized on the selective area substrates, i.e. Si(111). A growth yield of 95% has been achieved. Uniform diameters of 75 $\pm$5 nm has been achieved with lengths around 4-5 μm.

- Eventually a successful n-doping to the InAs nanowires with tellurium has been performed. A change in the morphology of InAs nanowires has been observed. This is due to the surfactant behaviour of tellurium, which decelerates axial diffusion of indium. With the increase in tellurium doping concentration, an increase in the diameter of the nanowire and a corresponding decrease in the axial length of the InAs nanowires has been observed. We have also observed that an increase in As pressure counteracts the tellurium surfactant behaviour and thereby helps indium atoms to diffuse along the wire. A doping range from 1×10^{18}cm^{-3} to 1×10^{19}cm^{-3} has been reported to increase the conductance of the InAs nanowire significantly. Tellurium doping that is greater than 1×10^{19}cm^{-3} leads to a significant increase in the diameter and a decrease of the lengths of the nanowires. At higher Te concentrations, atom probe tomography and TEM studies on these nanowires, reported that the nanowires lose their hexagonal cross-section and procure additional lateral facets that are (211) facets. These effects cannot be compensated with an increase in arsenic pressure. The reason between the switch is still unknown and could be due to the non-uniform Te incorporation.

- Furthermore, we fabricated self-catalyzed InAs/Al Josephson junctions on Si(111) substrate. This means that the weak-link has to be etched ex-situ, although the superconducting contacts are in-situ. Although it is has been quite established that the InAs nanowires grown on silicon (111) have stacking defects, the aluminium evaporated on those substrates at 30° have been reportedly smooth and crystalline and don not depend on the phase variation of the nanowire itself. Thus the interface between the semiconductor and the superconductor is defect free. This has been aided by the degassing step that is introduced after the growth of InAs nanowires. No diffusion has been observed. InAs nanowires posses a smooth and closed Al film with this process. The stacking faults observed in the nanowire have not been transferred to the Al shell and the orientations of the Al grains are irrespective to the crystal structure of the nanowire. The Al grains have predominantly two or more orientations. These orientations are associated to surface energy minimization. The substrate temperature had a major effect on the diffusion of Al atoms and at lower temperatures, it aided a smooth and crystalline metal layer.

- To include more materials and achieve a weak-link in-situ, a shadow mask evaporation scheme is presented in this thesis. The Josephson junctions formed in this process, circumvent the most detrimental fabrication steps, such as ex-situ etching methods, thus providing an enhanced device quality. This evaporation scheme, furthermore allows for

an encapsulation of the Josephson junction devices with dielectrics. This encapsulation protects the delicate surface states that are crucial for electrical measurements. The presented work here, enables future approaches in the realm of hybrid device architectures, new nanomaterial hybrids to increase T_c and in-situ encapsulation of surfaces. This method also allows to achieve smaller junction widths, w.r.t the diameter of the nanowire. In addition, the process has proven itself to be reproducible, and to further increase the device quality. The main transformation of the shadow evaporation scheme is that the evaporation angles are elevated to 87°. This platform helps to extend it to several materials, such as Nb where in the smoothness of the Nb film depends on the deposition angles [32]. The higher elevated angle of deposition, increases the Nb growth rate, i.e. the diffusion length of the Nb adatoms increase, in contrast to Al. The Niobium shells formed here are smooth, coherent, and crystalline. Thus, the Josephson junctions with Nb, formed using this platform have been reported to be highly transparent. The transmission electron microscopy studies proved that there is no deformities at the interface. Although a 2 nm thin amorphous layer is observed at the interface. This could be possibly due to diffusion. Nevertheless, due to the large interface transparency of 0.68, the junctions showed evident signatures of large Josephson supercurrent in the low temperature transport measurements [127]. The amorphous layer could be potentially recrystallized using post-growth annealing techniques. This issue could be additionally tackled by using a barrier e.g. titanium (also known to improve electrical contacts) between the superconductor and the semiconductor that is transparent and suppresses the diffusion of As into Nb [156].

- InAs/Al Josephson junctions produced using this shadow evaporation method show excellent properties w.r.t gap-hardness, interface transparency, and magnetic field resilience. The aluminum shell deposited is smooth and crystalline. Nonetheless, at a substrate temperature of -6°C, Al adatom diffusion rate is still higher, which causes the Al grains to form islands. These islands have been seen around the edges, where the Al films fades, also in the weak-link area thus forming a metallic bridge. This metallic bridge could cause a potential short-circuit. Although the sizes of these islands are of few nanometers, and eventually could oxidize, a junction free of any residue is greatly desired. This could be tackled by encapsulation of the Al layer or by evaporating the Al layer at much lower temperatures.

A promising extension of this thesis, would be to extend the shadow evaporation platform to incorporate different superconductors. Developing such new material combinations helps to access exotic regimes at large magnetic fields. These materials could also increase the critical temperature T_c, examples of such materials are lead and NbTiN, etc. Lead is also known to be epitaxially matched to InAs [28], so is vanadium [30].
Apart from this, the shadow platform can also be used for encapsulation of the hybrid nanowires with dielectrics. The deposition of dielectrics is important for materials like Al. From Fig. 80 and Fig. 84, there have been visible droplets of Al in the weak-link area. One big concern was that these islands/droplets, could bridge the two separate Al electrodes. This is not desirable as it could cause a potential short circuit. The presence of these droplets is mainly caused due to the post-growth diffusion of Al. That is, when the nanowire hybrid samples are transferred from colder to warmer temperatures [88]. This can be suppressed using a in-situ dielectric deposition of AlO_x on Al. This self-terminating AlO_x, freezes in the Al layer onto the nanowire facets, suppressing its further diffusion along the wire. This has to be done in-situ, right after

the Al deposition, at sufficiently low temperatures.
Likewise, niobium hybrids could also be encapsulated. Niobium is known to oxidize faster, which qualitatively causes new surface effects. The compound Nb_2O_5 forms as micro-crystals [157]. This could degrade the device performance. As for the initial attempts, we used the metal MBE to coat the samples with AlO_x of 3 nm, whilst the substrates are rotated. Nevertheless, an isotropic deposition of AlO_x, would ensure that the samples are completely encapsulated, for this purpose atomic layer deposition at UHV is highly recommended [158]. Fig. 96 (a), shows a BF and ADF STEM images of the junction of a InAs/Al/AlO_x. The suppression of the Al adatom diffusion can be observed. The junction area is free from any Al atoms. The AlO_x layer is grainy, due to the evaporation method used.

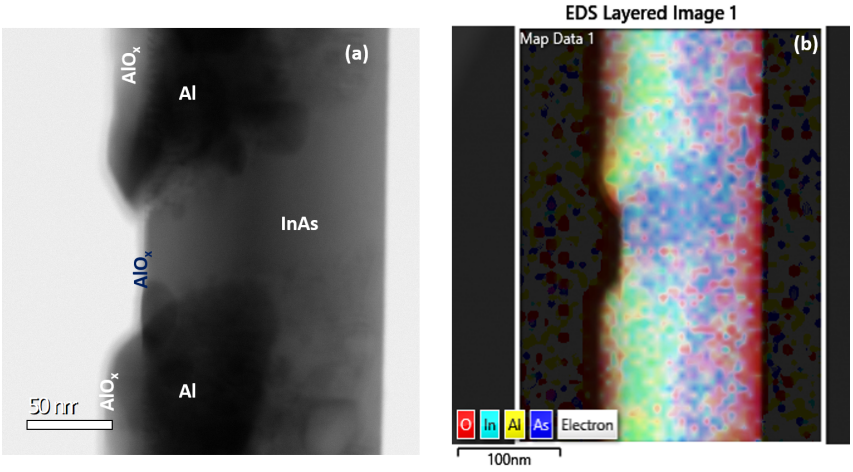

Figure 96: a) ADF STEM micrograph of InAs/Al/AlO_x nanowire hybrid, with the junction. b) Corresponding, EDX elemental map.

The corresponding EDX elemental map of the ADF image, can be seen in Fig. 96 (b). It shows that the AlO_x layer covers all the Al layers and the junction area, i.e. the six facets of the nanowire are covered by AlO_x. Similarly, in Fig. 97 (a) an ADF image of an InAs/Nb/AlO_x nanowire can be seen, while (b) shows an elemental EDX map of the corresponding nanowire with a encapsulation of the nanowire hybrid with AlO_x. Figure 97 (c) demonstrates a cross-section of the nanowire showing that AlO_x conformally covers the nanowire on all the six facets.
Additional experiments for an interlayer between the nanowire and the superconductor have been performed. Figure 98 shows an elemental EDX map, superimposed on an ADF image of InAs/Ti/Al/AlO_x. A 3 nm titanium inter-layer is deposited in-situ, without rotating the substrate. This ideally, improves the metallic contact of Al to the InAs nanowire and should combat any diffusion of Al into InAs. This concept could also be extended to InAs/Nb nanowire hybrids, and should potentially help to cope with the inter-diffusion. The titanium layer is coloured red and the Al layer is in yellow colour, as seen in Fig. 98, these layers are embedded on top of each other, and shows up in orange colour.
Another promising extension towards this thesis would be an approach towards lateral growth of nanowires onto a substrate. This could lead to a greater path towards scalability. Qubits comprising of nanowires have also been able to show promising steps towards scalability like their counterparts i.e. 2-D layer systems. This lies in the approaches of nanowire networks, wherein complicated nanowire networks are grown laterally onto a substrate, and additionally selective deposition of superconductors/metals is performed [159, 160].

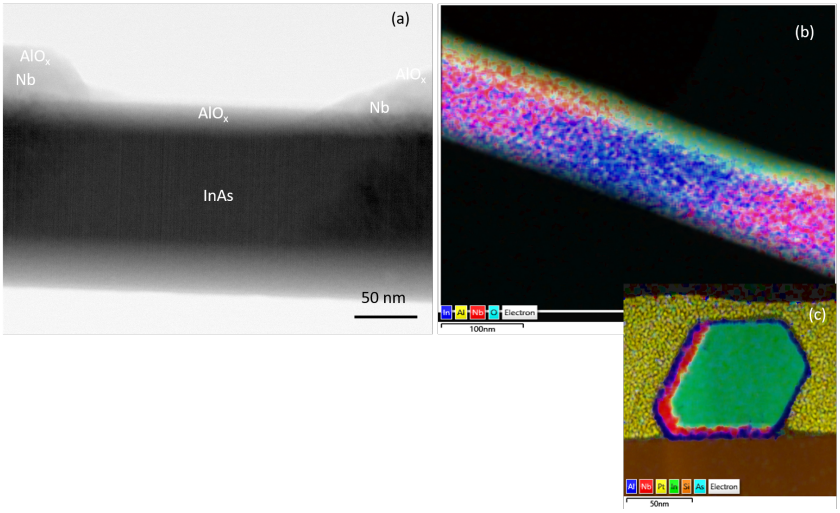

Figure 97: a) ADF STEM micrograph of an InAs/Nb nanowire covered with AlO_x. b) Corresponding EDX elemental map superimposed on a). c) STEM micrograph of cross-section of InAs/Nb/AlO_x nanowire hybrid, showing AlO_x covering all the six facets of the nanowire.

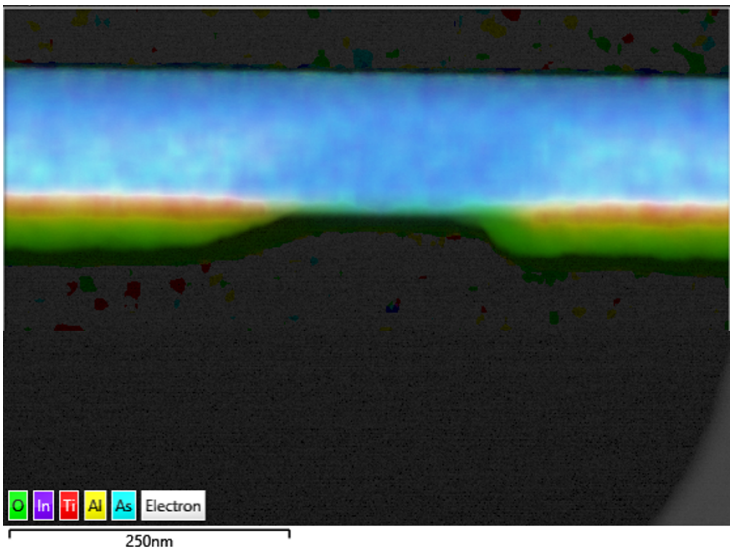

Figure 98: EDX elemental map of STEM micrograph of InAs/Ti/Al/AlO_x nanowire, showing Ti buried under Al, in a uniform layer and AlO_x encapsulating the whole nanowire.

Appendix

9.1 Substrate Preparation

Atomic force microscopy (AFM) on Si(111) substrates with 20 nm SiO_2. The holes on these substrates are etched using reactive ion etching (RIE) using ChF_3 gas to achieve a depth of 16 nm.
Figure 99, shows a hole with a 55.7 nm diameter, that is etched to a depth of 12.2 nm. The hole diameter is intended to be 20 nm.

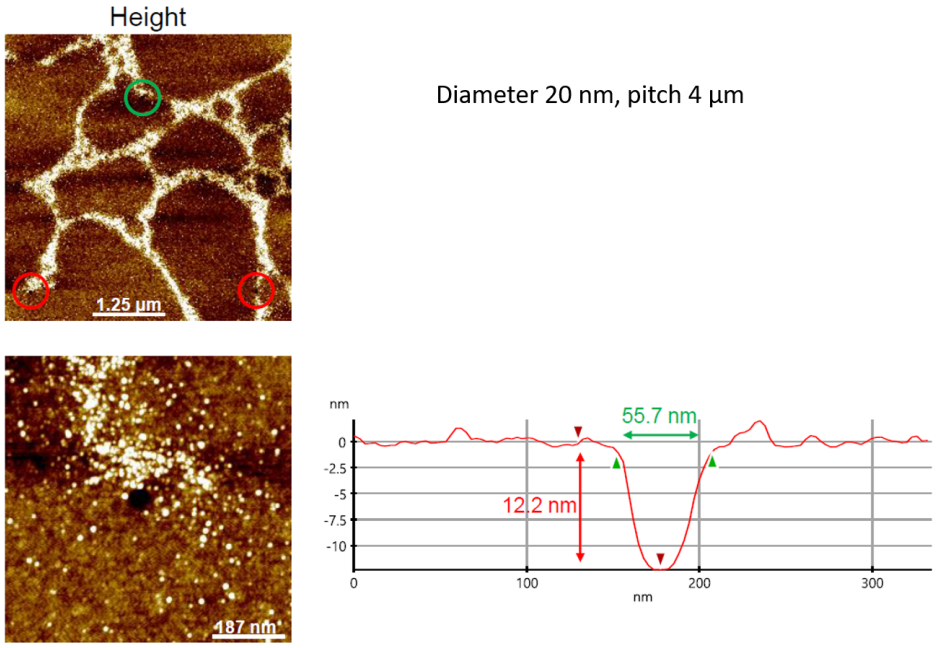

Figure 99: AFM micrograph of Si(111) substrates, top image shows the green marked hole that is probed, bottom image shows a zoom in of the hole. Holes with diameter 20 nm and 4 μm pitch probed.

Figure 100, shows a 63.4 nm hole diameter, that is etched to a depth of 13.1 nm. The hole diameter was intended to be 20 nm.

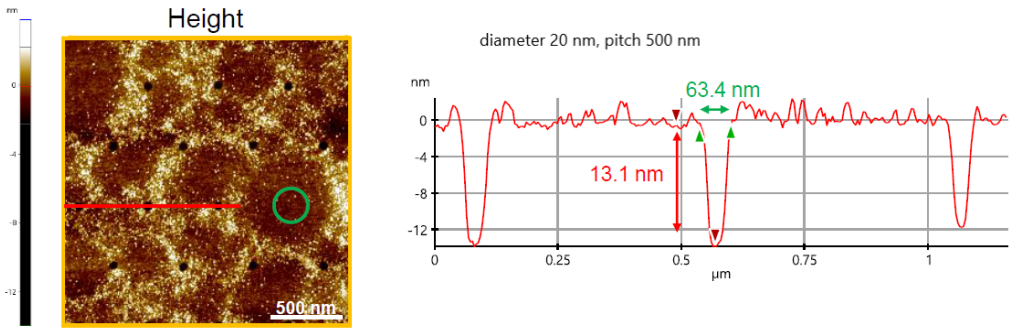

Figure 100: AFM micrograph of Si(111) substrates, holes with diameter 20 nm and 500 nm pitch probed.

Figure 101, shows a 71.8 nm hole diameter, that is etched to a depth of 15.5 nm. The hole diameter was intended to be 40 nm.

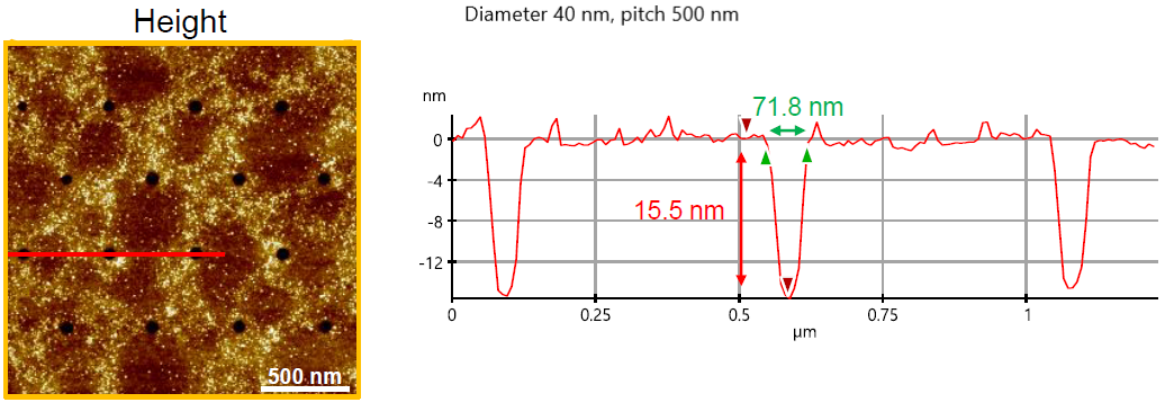

Figure 101: AFM micrograph of Si(111) substrates, holes with diameter 40 nm and 500 nm pitch probed. The holes marked in red are the ones that are measured.

Figure 102, shows a 79.3 nm hole diameter, that is etched to a depth of 13.5 nm. The hole diameter was intended to be 60 nm.

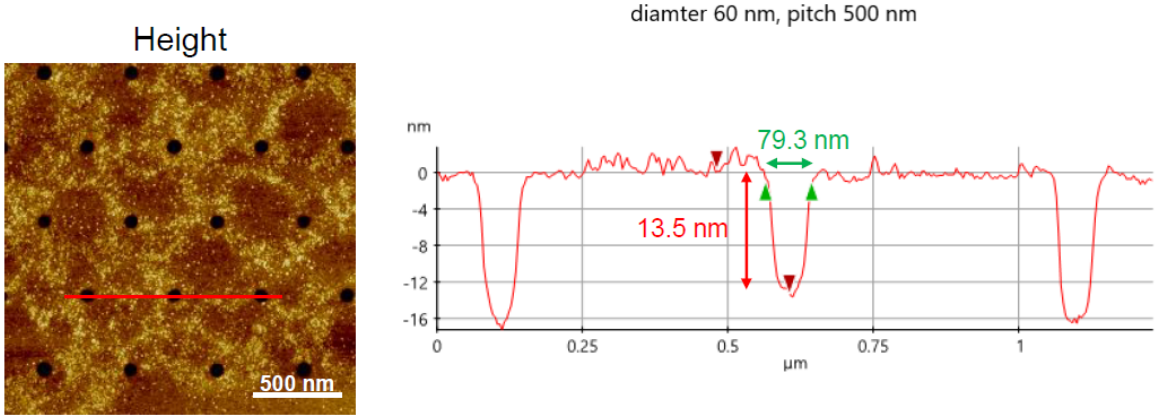

Figure 102: AFM micrograph of Si(111) substrates, holes with diameter 60 nm and 500 nm pitch probed. The holes marked in red are the ones that are measured.

Figure 103, shows a 103.8 nm hole diameter, that is etched to a depth of 16 nm. The hole diameter was intended to be 80 nm.
Figure 104, shows a 107.5 nm hole diameter, that is etched to a depth of 16 nm. The hole diameter was intended to be 80 nm.

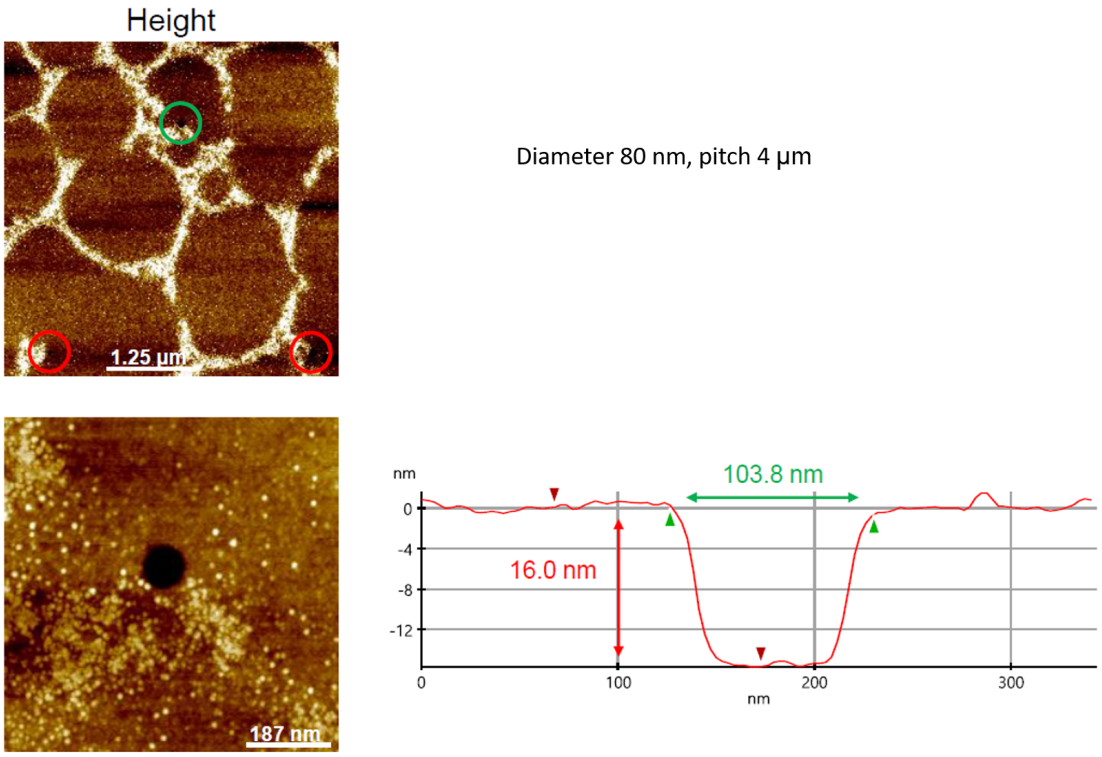

Figure 103: AFM micrograph of Si(111) substrates, holes with diameter 80 nm and $4\mu m$ pitch probed.

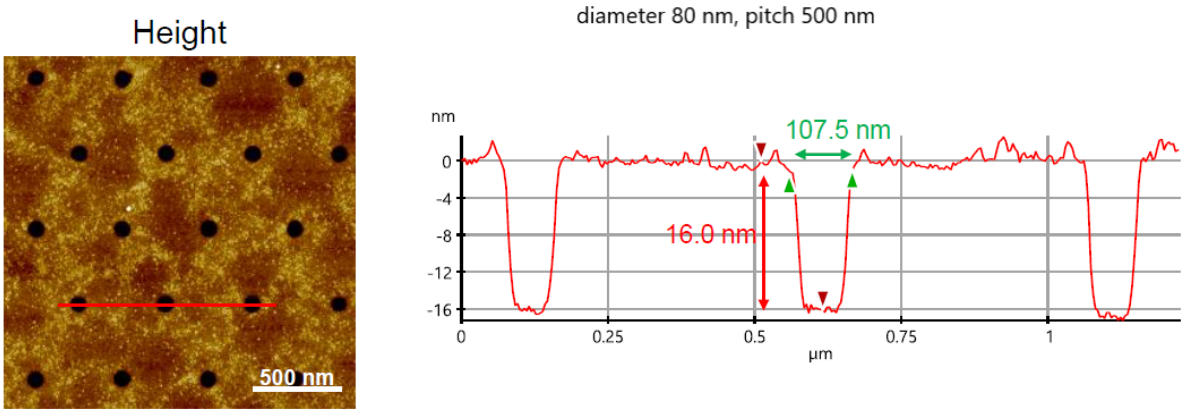

Figure 104: AFM micrograph of Si(111) substrates, holes with diameter 80 nm and 500 nm pitch probed. The holes marked in red are the ones that are measured.

9.2 GaAs Nanowire Selective Area Epitaxy

GaAs nanowires are grown selectively on a Si(111) substrate, covered with 20 nm of SiO_2. The holes are etched with a combination of RIE using CHF_3 gas and HF for 40 s. This should leave 2-3 nm of SiO_2 in the holes. The growth parameters used are, substrate temperature of 620°C, a Ga flux of 0.1 μm/hr and an As_4 flux of 5×10^{-6} torr, with a Ga-droplet pre-deposition time for 45 s. The 2-3 nm of SiO_2 in the holes, prevents the gallium droplet etching the Si surface, this causes alteration of the Si surface. Since the solubility of Si in liquid Ga is significantly higher [102]. Figure 105, shows the Ga dopelts in the holes and the nanowires grown with the above mentioned parameters.

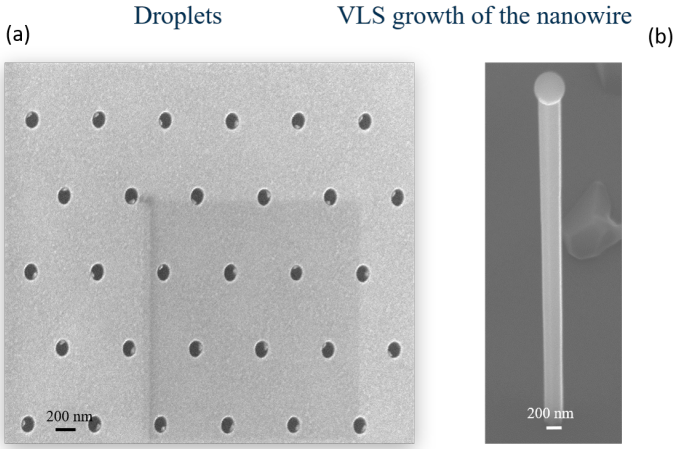

Figure 105: a) SEM micrograph of Ga droplets after 45 s pre-deposition time. The dropelts, tend to stick to the edge of the etched hole, closer to SiO_2. b) The resultant nanowire after 1.5 h growth time, shows a Ga droplet at the axis. The dimensions of the wire are 80 nm in diameter and 2μm in length.

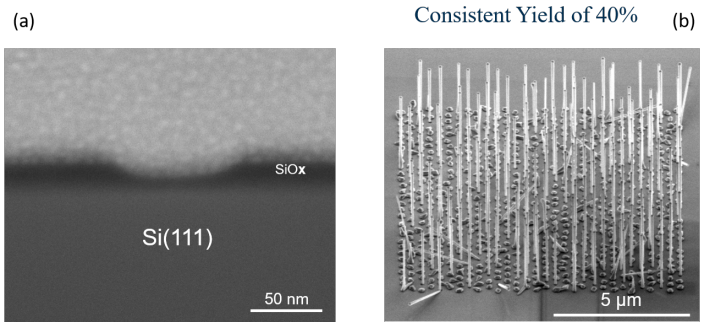

Figure 106: a) SEM micrograph of the etched with 1-2 nm of SiO_2 left in it. b) SEM micrograph of the GaAs nanowires grown selectively with a yield of 40%, populated densely with crystallites.

Crystallites constitute the major parasitic growth, as seen in Fig. 106 (b). Crystals form on unevenly etched holes, as seen in Fig. 107 (a). Empty holes with a crystal formation on top. In Fig. 107 (b) and (c) show the gallium diffusion into Si, this is one of the reasons it results in GaAs crystals. Ga droplet is known to etch silicon [102].
To prevent the Ga droplet from etching Si, instead of 2-3 nm, a 6 nm thick SiO_2 is left in the holes as seen in Fig. 109 (a). Then the process is performed as follows, firstly the substrate

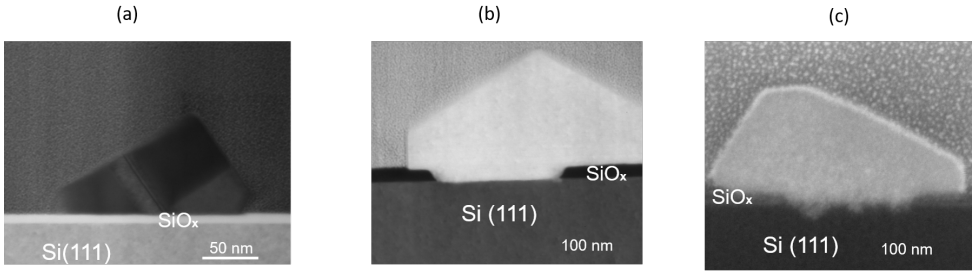

Figure 107: Crystal formation. a) On a unetched hole or a dent. b) and c) Si dissolved into GaAs, since Ga droplet is known to etch Si away..

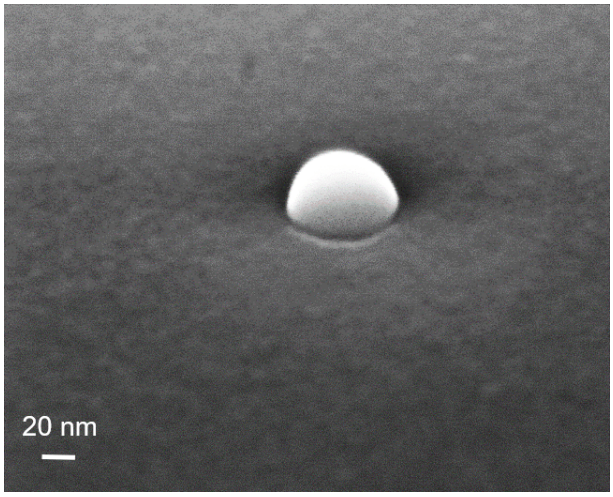

Figure 108: Gallium droplet formed after induced etching and left to nucleate on the holes.

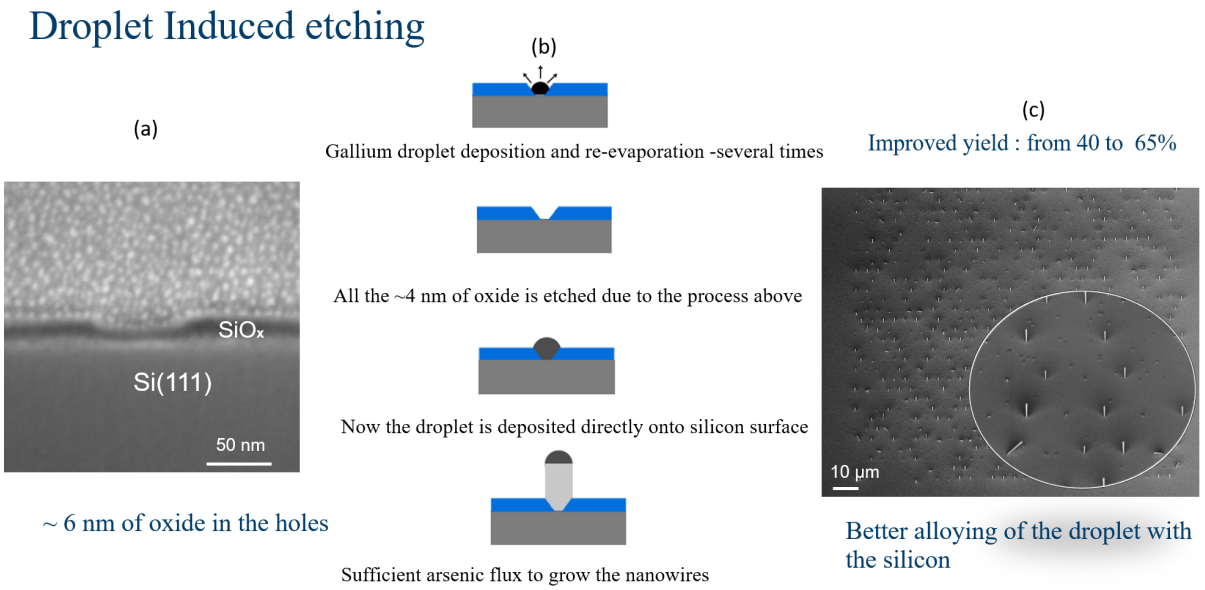

Figure 109: a) SEM micrograph of the etched hole with 6 nm of SiO_2. b) Process of Ga droplet induced etching. c) SEM micrograph of the improved yield of 65%.

is heated to 600°C and Ga droplet is made to form at a Ga rate of 0.08 m/h for 90 s. The substrate is kept for 5 min after the droplet deposition, this helps to etch the SiO_2. Then, the

Ga droplet is then, desorbed at this temperature, when it is left another 15 min. This process is repeated for 5 times. At the final step, Ga droplet is left to nucleate, as be seen in fig. 108. This droplet is also known to cover the entire hole, thus increases has an increased surface area and the its angle to the substrate is also known to increase. Then subsequently the nanowires are grown. The growth parameters used are substrate temperature of 620°C, Ga flux of 0.1 μm/hr and As_4 flux of 5×10^{-6} torr for 1.5 h. This improved the nanowire yield from 40 to 65%, as seen in Fig. 109 (c). Federico Matteini *et. al* have also shown that Ga droplets with contact angles around 90° to the substrate, result in nanowires that grow perpendicular to the substrate [161].

9.3 In-situ Josephson Junctions

The fabrication platform of producing Josephson junctions as explained in chapter in-situ Josephson junctions, could potentially be extended to produce complex structures. By shadowing more than one wire, multiple junctions on one wire can be produced, as seen in Fig. 110, in the case of random growth. This approach in principle could be translated to selective area growth as well.

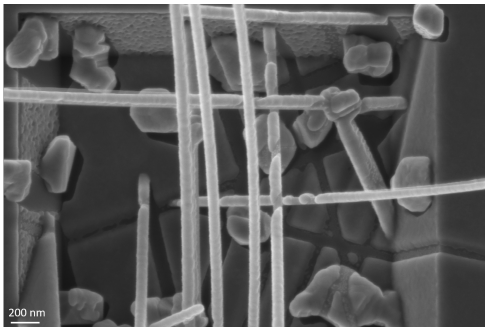

Figure 110: Nanowires with Al shell, multi-junction nanowire on the bottom.

Another application of this platform, could be used for fabrication of nanowire networks. Nanowire networks have proven to improve quantum transport properties like strong spin-orbit coupling and phase coherence [94]. Thus makes it interesting for topological quantum computation based applications [162]. These nanowire networks are demonstrated in Fig. 111, that two nanowires grown from the holes, that are exactly placed in the middle of the Si(111) facet, grow out and merge into the each other. There is no change in the diameter after the over-growth of these nanowires and additionally they do not ball-up together. The nanowires still retain their crystal structures.

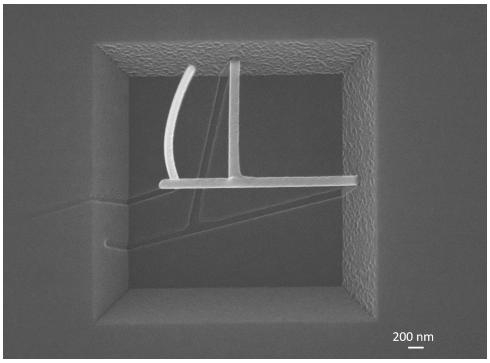

Figure 111: Nanowires merged together to form a T-shaped structure.

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List of Publications

The results presented in this thesis have been published in the scientific journals below.

- **Pujitha Perla**, H. Aruni Fonseka, Patrick Zellekens, Russell Deacon, Yisong Han, Jonas Kölzer, Timm Mörstedt, Benjamin Bennemann, Abbas Espiari, Koji Ishibashi, Detlev Grützmacher, Ana M. Sanchez, Mihail Ion Lepsa, and Thomas Schäpers. *Fully in situ Nb/InAs-nanowire josephson junctions by selective-area growth and shadow evaporation*. Nanoscale Adv., 3:1413–1421, 2021.

- Patrick Zellekens, Russell Deacon, **Pujitha Perla**, H. Aruni Fonseka, Timm Mörstedt, Steven A. Hindmarsh, Benjamin Bennemann, Florian Lentz, Mihail I. Lepsa, Ana M. Sanchez, Detlev Grützmacher, Koji Ishibashi, and Thomas Schäpers. *Hard-Gap Spectroscopy in a Self-Defined Mesoscopic InAs/Al Nanowire Josephson Junction*. Phys. Rev. Applied 14, 054019, 2020.

- **Perla, Pujitha** and Faustmann, Anton and Koelling, Sebastian and Zellekens, Patrick and Deacon, Russell and Fonseka, H. Aruni and Kölzer, Jonas and Sato, Yuki and Sanchez, Ana M. and Moutanabbir, Oussama and Ishibashi, Koji and Grützmacher, Detlev and Lepsa, Mihail Ion and Schäpers, Thomas *Te-doped selective-area grown InAs nanowires for superconducting hybrid devices*. PhysRevMaterials., 6.024602, 2022.

Other publications

- Marvin M. Jansen, **Pujitha Perla**, Mane Kaladzhian, Nils von den Driesch, Johanna Janßen, Martina Luysberg, Mihail I. Lepsa, Detlev Grützmacher, and Alexander Pawlis. *Phase-Pure Wurtzite GaAs Nanowires Grown by Self-Catalyzed Selective Area Molecular Beam Epitaxy for Advanced Laser Devices and Quantum Disks*. ACS Applied Nano Materials 2020 3 (11), 11037-11047

- Patrick Zellekens, Natalia Demarina, Johanna Janßen, Torsten Rieger, Mihail Ion Lepsa, **Pujitha Perla**, Gregory Panaitov, Hans Lüth, Detlev Grützmacher, and Thomas Schäpers. *Phase coherent transport and spin-orbit interaction in GaAs/InSb core/shell nanowires*. Semiconductor Science and Technology, 35(8):085003, Jun 2020.

- Peter Schüffelgen, Tobias Schmitt, Michael Schleenvoigt, Daniel Rosenbach, **Pujitha Perla**, Abdur R. Jalil, Gregor Mussler, Mihail Lepsa, Thomas Schäpers, and Detlev Grützmacher. *Exploiting topological matter for majorana physics and devices*. Solid-State Electronics, 155:99–104, 2019.

List of Presentations

Conference contributions

- Workshop on Thermo-Electric Transport in Nanowires, Eindhoven, The Netherlands, December, 2017: poster presentation- *Self-catalysed MBE-grown III-V nanowire arrays*
- DPG (Deutsche Physikalische Gesellschaft) conference, Berlin, March, 2018: oral presentation- *Self-catalysed MBE-grown III-V nanowire arrays on Si(111) substrates*
- 700-Heraeus-Seminar, Bad Honnef, April, 2019: poster presentation- *In-Situ grown superconducting contacts on InAs nanowires*
- Nanowire week, Pisa, Italy, September, 2019: poster presentation-*In-situ prepared superconducting Al and Nb contacts on InAs nanowires*
- Deutscher MBE Workshop, Würzburg, October, 2019: oral presentation-*Fabrication of in-situ Josephson contacts on InAs nanowires*

Curriculum Vitae

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05.2007 – 05.2010: Bachelor of Science in Physics, Sri Satya Sai University, Anantapur, B.Sc. Thesis: Characteristics and applications of solar cells.

07.2011 – 05.2013: Master of Science in Physics, National institute of Technology, Tiruchirappalli, Master thesis: Fabrication of multiwalled carbon nanotube incorporated polymer free-standing films.

Since 08.2016: PH.D. in Physics, Forschungszentrum Jülich (PGI-9), RWTH Aachen, Ph.D. dissertation: Growth and characterization of InAs nanowire-based Josephson junctions.

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