Development and production of an intelligent PMT readout system for OSIRIS

Von der Fakultät für Mathematik, Informatik und Naturwissenschaften der RWTH Aachen University zur Erlangung des akademischen Grades eines Doktors der Naturwissenschaften genehmigte Dissertation

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Abstract

The Jiangmen Underground Neutrino Observatory (JUNO) is a neutrino detector currently under construction in South China. The experiment is built to contribute substantially to central unsolved neutrino physics questions. Examples are the determination of the neutrino mass ordering and precision measurements of neutrino mixing angles.

An inalienable prerequisite for precise measurements is a high radiopurity of the detector, especially of the liquid scintillator. In order to investigate the radioactivity of the liquid scintillator, the dedicated Online Scintillator Internal Radioactivity Investigation System (OSIRIS) is built. It uses photomultiplier tubes (PMTs) for the detection of light caused by radioactive decays. A new system is developed for OSIRIS which attaches the PMT readout electronics directly at its back. This system directly processes the digitized PMT signals and is therefore denoted as intelligent PMT (iPMT).

The design of the iPMT system with a focus on the electronics is described in detail. As part of this thesis, an FPGA design for the PMT readout and the control of the iPMT is implemented and tested. Furthermore, an FPGA design for the synchronization of the iPMTs with each other and with calibration systems in OSIRIS is developed.

Characterizing measurements with a focus on central capabilities of the system are presented. This includes properties of the readout chain and an evaluation of the timing and synchronization system. An exemplary evaluation of the performance with a PMT is presented.

Concluding, the electronics assembly of the iPMTs for OSIRIS is described. Prior shipment to China, the iPMTs undergo functional verification tests, and the corresponding results are presented. In total, 75 iPMTs are successfully tested for the use in OSIRIS.

Zusammenfassung

Das Jiangmen Underground Neutrino Observatory (JUNO) ist ein Neutrinodetektor, der sich in aktuell in Südchina im Aufbau befindet. Das Experiment ist darauf ausgelegt substantielle Beiträge zu zentralen ungelösten Fragen der Neutrinophysik zu leisten. Dazu gehören beispielsweise die Bestimmung der Neutrino Massenordnung und Präzisionsmessungen von Neutrino Mischungswinkeln.

Um genaue Messungen zu gewährleisten sind sehr geringe radioaktive Verunreinigungen des Detektors, inbesondere des Flüssigszintillators, nötig. Um die Radioaktivität des Flüssigsszintillators zu überprüfen, wird das dedizierte Online Scintillator Internal Radioactivity Investigation System (OSIRIS) gebaut. Es nutzt Photomultiplier Tubes (PMTs) zur Detektion von Licht welches durch radioaktive Zerfälle hervorgerufen wird. Ein neues System, bei der die PMT Ausleseelektronik direkt am PMT befestigt wird, wurde für OSIRIS entwickelt. Dieses System verarbeitet die digitalisierten PMT Signale direkt und wird daher als intelligenter PMT (iPMT) bezeichnet.

Der Aufbau des iPMT Systems wird im Detail beschrieben, wobei der Fokus auf der Elektronik liegt. Als Teil dieser Arbeit wurde ein FPGA Design für die Auslese der PMTs und Kontrolle der iPMTs entworfen, implementiert und getestet. Desweiteren wurde ein FPGA Design für die Synchronisierung der iPMTs untereinander und mit Kalibrationssystemen in OSIRIS entwickelt.

Charakterisierende Messungen mit dem Fokues auf zentralen Fähigkeiten des Systems werden vorgestellt. Dies beinhaltet die Evaluation der Synchronisierung, sowie Eigenschaften der Datenauslese. Beispielhaft wird die Performance an einem PMT präsentiert.

Abschließend wird der Zusammenbau der Elektronik der iPMTs für OSIRIS beschrieben. Vor dem Export nach China wurde die Funktionalität der iPMTs getestet und die entsprechende Ergebnisse werden präsentiert. Für den Einbau in OSIRIS wurden insgesamt 75 iPMTs erfolgreich getestet.

Contents

Acronyms

AC **A**lternating **C**urrent.

ADC **A**nalog-to-**D**igital **C**onverter.

ASIC **A**pplication-**S**pecific **I**ntegrated **C**ircuit.

AV **A**crylic **V**essel.

BER **B**it **E**rror **R**ate.

CD **C**entral **D**etector.

CDR **C**lock and **D**ata **R**ecovery.

DAC **D**igital-to-**A**nalog **C**onverter.

DAQ **D**ata **Acq**uisition.

DC **D**irect **C**urrent.

DCR **D**ark **C**ount **R**ate.

DMA **D**irect **M**emory **A**ccess.

EB **E**vent **B**uilder.

EEPROM **E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory.

FPGA **F**ield **P**rogrammable **G**ate **A**rray.

FSM **F**inite-**S**tate **M**achine.

FWHM **F**ull **W**idth **H**alf **M**aximum.

HG **H**igh **G**ain.

HV **H**igh **V**oltage.

IBD **I**nverse **B**eta **D**ecay.

IC **I**ntegrated **C**ircuit.

IO **I**nverted **O**rdering.

IP-Core **I**ntellectual **P**roperty Core.

iPMT **i**ntelligent **P**hoto**M**ultiplier **T**ube.

I²C **I**nter-**I**ntegrated **C**ircuit.

JTAG **J**oint **T**est **A**ction **G**roup.

JUNO **J**iangmen **U**nderground **N**eutrino **O**bservatory.

LFSR **L**inear-**f**eedback **S**hift **R**egister.

LG **L**ow **G**ain.

LS **L**iquid **S**cintillator.

LSB **L**east **S**ignificant **B**it.

LVDS **L**ow **V**oltage **D**ifferential **S**ignaling.

MG **M**id **G**ain.

NO **N**ormal **O**rdering.

OS **O**perating **S**ystem.

OSIRIS **O**nline **S**cintillator **I**nternal **R**adioactivity **I**nvestigation **S**ystem.

p.e. PMT output signal equivalent to one **p**hoto **e**lectron.

PCB **P**rinted **C**ircuit **B**oard.

PGA **P**rogrammable **G**ain **A**mplifier.

PL **P**rogrammable **L**ogic.

PMNS **P**ontecorvo-**M**aki-**N**akagawa-**S**akata.

PMT **P**hoto**M**ultiplier **T**ube.

PoE **P**ower **o**ver **E**thernet.

PPS **P**ulse **P**er **S**econd.

PRBS **P**seudo **R**andom **B**inary **S**equence.

PS **P**rocessing **S**ystem.

RAM **R**andom **A**ccess **M**emory.

RoB **R**ead**o**ut **B**oard.

SB **S**urface **B**oard.

SCB **S**urface **C**onnector **B**oard.

SCCU **S**low **C**ontrol and **C**onfiguration **U**nit.

SNR **S**ignal-to-**N**oise-**R**atio.

SoC **S**ystem-**o**n-a-**C**hip.

TB **T**rigger **B**oard.

TCP **T**ransmission **C**ontrol **P**rotocol.

TIA **T**rans**i**mpedance **A**mplifier.

TTS **T**ransit **T**ime **S**pread.

UART **U**niversal **A**synchronous **R**eceiver **T**ransmitter.

UDP **U**ser **D**atagram **P**rotocol.

VHDL **V**ery High Speed Integrated Circuit **H**ardware **D**escription **L**anguage.

VULCAN Integrated circuit dedicated for PMT readout designed by ZEA-2, Jülich.

Chapter 1

Introduction

In 1930, Pauli postulated the existence of a very light particle, the neutrino, to explain the continuous energy spectrum of the β decay. The existence of this particle could be confirmed almost three decades later, in 1956, by the Cowan-Reines neutrino experiment at the Savannah River Plant with a nuclear reactor as neutrino source [1]. Since then, many experiments have been conducted to unriddle the properties of neutrinos.

In 1968 the Homestake experiment measured neutrinos from the sun and found hints for a discrepancy between the standard solar model and the experiment [2]. The detection rate of solar neutrinos was significantly lower than predicted by the standard solar model, which was then called the *solar neutrino problem* [3].

A possible explanation had already been proposed several years earlier by Pontecorvo in 1957 [4]. He suggested neutrino oscillations as quantum mechanical phenomenon, in which the oscillations are due to the interference of different massive neutrinos [3, p. 245].

The existence of neutrino oscillation has been proven first by the experiments Super-Kamiokande in 1998 [5] and SNO in 2001 [6], which was recognized by awarding the 2015 Nobel prize to the leaders of the two experiments.

Following measurements of the neutrino mixing angle θ_{13} by DayaBay [7], Double-Chooz [8] and RENO [9] allowed the meaningful planning of further experiments [10].

One of those experiments is the **J**iangmen **U**nderground **N**eutrino **O**bservatory (JUNO), which is currently under construction in South China. It aims to provide precise measurements of neutrinos from various sources. Large effort is put into the control and monitoring of the radiopurity of the detector materials to reduce the backgrounds for the experiment. Of foremost importance is the radiopurity of the **L**iquid **S**cintillator (LS). A dedicated detector – the **O**nline **S**cintillator **I**nternal **R**adioactivity **I**nvestigation **S**ystem (OSIRIS) – is built to monitor the radiopurity of the LS. Chapter 3 gives an overview over the neutrino experiment JUNO and its sub-detector OSIRIS.

OSIRIS' measurement of the radioactivity is based on the detection of light induced by the decay of radioactive isotopes. In order to detect these faint light signals, large area **P**hoto**M**ultiplier **T**ubes (PMTs) are used.

A novel system of the readout of PMTs is implemented for OSIRIS. It features a dedicated set of electronics attached at the back of each PMT and is called **i**ntelligent **P**hoto**M**ultiplier **T**ube (iPMT). A detailed description of this system is given in Chapter 4.

As part of the electronics, **F**ield **P**rogrammable **G**ate **A**rrays (FPGAs) are used for the PMT readout and data processing. The development of the FPGA designs is part of this thesis and presented in Chapter 5. A characterization of the system, including

the evaluation of the readout performance and the synchronization, is presented in Chapter 6.

As final section, parts of the production of the iPMTs are described in Chapter 7. This includes the assembly of the electronics and functional verification tests of complete iPMTs.

A summary of the results and an outlook on future developments are given in Chapter 8.

Chapter 2

Neutrino oscillation

The current best model describing elementary particles and their strong, electromagnetic and weak interactions as a quantum field theory is the standard model. Nonetheless, the experimental evidence exists, that the model is incomplete in several aspects, one of them regards the field of neutrinos.

(Anti-)Neutrinos are massless fermions in the standard model [11, p. 285] and exist in three flavors (particles: ν_e, ν_μ, ν_τ antiparticles: $\overline{\nu}_e, \overline{\nu}_\mu, \overline{\nu}_\tau$). They interact only weakly via charged current interaction ($W^\pm$) or neutral current interaction (Z^0) with other standard model particles. It has been observed that neutrinos periodically change their flavor depending on their energy and traveled distance. This phenomenon is called neutrino oscillation.

In contradiction to the standard model, neutrino oscillation requires non-vanishing neutrino masses. A flavor eigenstate of a neutrino, as it is produced from the interaction with a charged lepton can be written as linear combination of mass eigenstates

$$|\nu_\alpha\rangle = \sum_{\kappa=1}^{n} U^*_{\alpha\kappa} |\nu_\kappa\rangle \tag{2.1}$$

with the flavor eigenstates ν_α ($\alpha = e, \mu, \tau$), the number of light neutrino $n = 3$[1], the complex conjugate of the elements of the mixing matrix $U_{\alpha\kappa}$ and the mass eigenstates ν_κ ($\kappa = 1, 2, 3$) [11]. U is a 3 x 3 unitary matrix describing the flavor eigenstates as linear combinations of mass eigenstates

$$\begin{pmatrix} \nu_e \\ \nu_\mu \\ \nu_\tau \end{pmatrix} = \begin{pmatrix} U_{e1} & U_{e2} & U_{e3} \\ U_{\mu 1} & U_{\mu 2} & U_{\mu 3} \\ U_{\tau 1} & U_{\tau 2} & U_{\tau 3} \end{pmatrix} \begin{pmatrix} \nu_1 \\ \nu_2 \\ \nu_3 \end{pmatrix}. \tag{2.2}$$

[1] Ignoring the possibility of additional sterile neutrinos, which do not undergo weak interactions [3, p. 247].

This matrix can also be written in the form of three rotations (with the second rotation depending on the phase δ_{CP}) and a phase matrix [11, p. 288, 12]

$$\begin{aligned} U &= \begin{pmatrix} 1 & 0 & 0 \\ 0 & c_{23} & s_{23} \\ 0 & -s_{23} & c_{23} \end{pmatrix} \begin{pmatrix} c_{13} & 0 & s_{13}e^{-i\delta_{\mathrm{CP}}} \\ 0 & 1 & 0 \\ -s_{13}e^{i\delta_{\mathrm{CP}}} & 0 & c_{13} \end{pmatrix} \begin{pmatrix} c_{21} & s_{12} & 0 \\ -s_{12} & c_{12} & 0 \\ 0 & 0 & 1 \end{pmatrix} P_\eta \\ &= \begin{pmatrix} c_{12}c_{13} & s_{12}c_{13} & s_{13}e^{-i\delta_{\mathrm{CP}}} \\ -s_{12}c_{23} - c_{12}s_{13}s_{23}e^{i\delta_{\mathrm{CP}}} & c_{12}c_{23} - s_{12}s_{13}s_{23}e^{i\delta_{\mathrm{CP}}} & c_{13}s_{23} \\ s_{12}s_{23} - c_{12}s_{13}c_{23}e^{i\delta_{\mathrm{CP}}} & -c_{12}s_{23} - s_{12}s_{13}c_{23}e^{i\delta_{\mathrm{CP}}} & c_{13}c_{23} \end{pmatrix} P_\eta \end{aligned} \tag{2.3}$$

with $c_{ij} \equiv \cos\theta_{ij}$, $s_{ij} \equiv \sin\theta_{ij}$ and the matrix P_η describing the Majorana phases which can be neglected for neutrino oscillation [13] (in case of Dirac particles P_η becomes the identity matrix). U is known as the **P**ontecorvo-**M**aki-**N**akagawa-**S**akata (PMNS) mixing matrix giving credit to those persons which formulated the mixing of different neutrino families [11].

The four free parameters in the matrix are denoted as the mixing angles $\theta_{12}, \theta_{13}, \theta_{23}$ and the CP-violating phase δ_{CP} [14].

In order to observe the neutrino oscillation, the time evolution of the flavor state has to be considered, since the neutrino is created as a pure flavor state in a weak interaction. The time evolution of a massive neutrino is given as superposition of planar waves

$$|\nu_\alpha(t)\rangle = \sum_{\kappa=1}^{n} U^*_{\alpha\kappa} e^{-iE_\kappa t} |\nu_\kappa\rangle \tag{2.4}$$

with $E_\kappa = \sqrt{\mathbf{p}_\kappa^2 + m_\kappa^2}$ and m_κ ($\mathbf{p}_\kappa$) the mass (momentum) of the neutrino mass eigenstate ν_κ (quantities are expressed in natural units ($c = \hbar = 1$)) [3, p. 248].

The mass eigenstate can be expressed in terms of flavor eigenstates as following [3, p. 248]:

$$|\nu_\kappa\rangle = \sum_\alpha U_{\alpha\kappa} |\nu_\alpha\rangle . \tag{2.5}$$

Substituting the mass eigenstate in Eq. (2.4) results in

$$|\nu_\alpha(t)\rangle = \sum_\beta \left(\sum_{\kappa=1}^{n} U^*_{\alpha\kappa} e^{-iE_\kappa t} U_{\beta\kappa} \right) |\nu_\alpha\rangle \tag{2.6}$$

with $\beta = e, \mu, \tau$ [3]. By this, the time evolved flavor state is expressed in terms of different flavor states. Since the mixing matrix U is not diagonal, a pure flavor eigenstate at $t = 0$ becomes a superposition of different flavor states for $t > 0$. The composition of the mass eigenstates is visualized in Fig. 2.1.

The probability for the transition from a flavor state α to a flavor state β when the neutrino interacts and produces a charged lepton is given as [3, p. 249, 11, p. 288]:

$$P_{\nu_\alpha \to \nu_\beta}(t) = \sum_{\kappa=1,j=1}^{n} U^*_{\alpha\kappa} U_{\beta\kappa} U_{\alpha j} U^*_{\beta j} e^{-i(E_\kappa - E_j)t}. \tag{2.7}$$

In the ultra-relativistic limit $t \simeq cL$, the dependency of $P_{\nu_\alpha \to \nu_\beta}(t)$ on t is expressed as dependency on the distance L (baseline) [3].

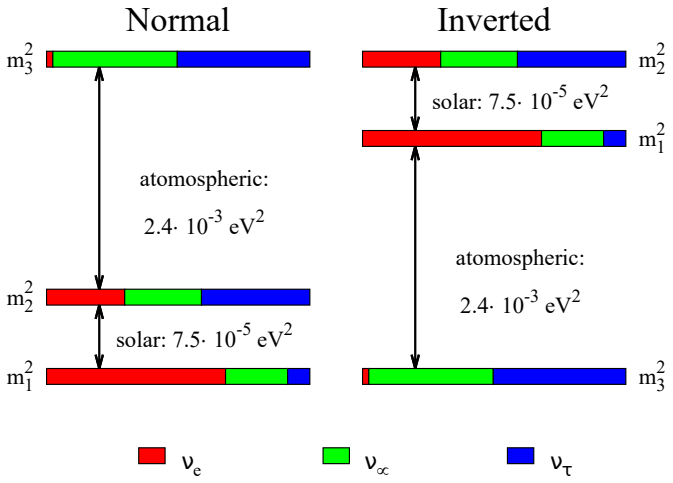


FIGURE 2.1: Illustration of the flavor composition of the three mass eigenstates m_1, m_2 and m_3 [15]. The colors indicate the flavor composition of the mass eigenstates. Additionally the two mass ordering options (normal / inverted) are depicted. The relative ordering $m_2 > m_1$ is known from solar neutrino measurements [16], but whether $m_1 < m_2 < m_3$ or $m_3 < m_1 < m_2$ is true, is unknown.

The transition probability in Eq. (2.7) is derived for neutrinos. For the case of anti-neutrinos, the corresponding coefficients can be calculated by the complex conjugate of the elements of U [3, p. 255]. As example, the electron anti-neutrino survival probability in vacuum is given

$$P_{\overline{\nu}_e \to \overline{\nu}_e} = 1 - \sin^2 2\theta_{13}(c_{12}^2 \sin^2 \Delta_{31} + s_{12}^2 \sin^2 \Delta_{32}) - c_{13}^4 \sin^2 2\theta_{12} \sin^2 \Delta_{21} \tag{2.8}$$

$$\begin{aligned} &= 1 - \sin^2 2\theta_{13} \left[c_{12}^2 \sin^2 \frac{\Delta m_{31}^2 L}{4E} + s_{12}^2 \sin^2 \frac{\Delta m_{32}^2 L}{4E} \right] \\ &\quad - c_{13}^4 \sin^2 2\theta_{12} \sin^2 \frac{\Delta m_{21}^2 L}{4E} \end{aligned} \tag{2.9}$$

with $\Delta_{ij} = \Delta m_{ij}^2 L/4E$ and $\Delta m_{ij}^2 \equiv m_i^2 - m_j^2$, with the baseline L and the electron anti-neutrino energy E [17, 18, p. 2].

The vacuum solution can be used for reactor neutrino experiments on earth, since the terrestrial matter effects on $P_{\overline{\nu}_e \to \overline{\nu}_e}$ are mostly negligible small, due to low neutrino energies and baselines $L < 100\,\text{km}$ [18, p. 21].

The mass squared difference Δm_{21}^2 is also denoted as "solar" mass splitting, due to its dominance for solar ν_e oscillations. The "atmospheric" mass splitting Δm_{31}^2 is dominant for atmospheric ν_μ and $\overline{\nu}_\mu$ oscillations.

More comprehensive overviews of neutrino oscillation are given in [14], [11, p. 285 ff.] and [3].

2.1 Neutrino sources

Neutrinos are generated by weak interactions either in man-made or natural sources. Due to their very low cross-section, a high flux in combination with large detectors is typically required for their measurement.

The sun produces a high flux of neutrinos via several processes, predominantly via the fusion of protons to helium [19]. The Homestake experiment, which has given first hints towards the neutrino oscillation, detected neutrinos from the sun.

Other naturally occurring neutrinos are generated from cosmic rays in Earth's atmosphere and therefore known as atmospheric neutrinos. Also supernovae are interesting sources, either in the form of a burst of neutrinos which are emitted during an explosion or in form of the flux of all past explosions, the Diffuse Supernova Neutrino Background (DSNB) [19].

In order to investigate neutrinos, dedicated accelerator-based neutrino sources have been designed. An example is the T2K experiment, where a 30 GeV proton bream is used to generated neutrinos which are measured in the far-detector Super-Kamiokande at a distance of 295 km [20].

Another important man-made neutrino source with a very high flux, which are not specifically designed as neutrino sources, are nuclear reactors. During the fission of low-enriched ^{235}U, the isotopes from ^{235}U, ^{239}Pu, ^{238}U, and ^{241}Pu and their decay chain products undergo decays and generate $\overline{\nu}_e$ [19, p. 14]. The existence of neutrinos was actually proven by measurements with a nuclear reactor at the Savannah River Plant in 1956 [1]. Since then, several experiments like DoubleChooz, DayaBay or RENO have used reactors to investigate neutrinos and also upcoming experiments as JUNO use them as neutrino source.

2.2 Open neutrino physics questions

There are several open question related to the field of neutrino oscillations. One major question is the ordering of the neutrino masses. The **N**ormal **O**rdering (NO) refers to the order $m_1 < m_2 < m_3$, whereas the **I**nverted **O**rdering (IO) refers to $m_3 < m_1 < m_2$. From atmospheric and solar neutrino measurements it is known that $\Delta m^2_{21} \ll |\Delta m^2_{31}| \simeq |\Delta m^2_{32}|$ [11, p. 301]. Unknown is, whether $m_3 > m_1$ (NO) or $m_3 < m_1$ (IO) is realized in nature. A visualization of the two mass orderings is given in Fig. 2.1.

Determining the neutrino mass ordering would unriddle one of the major open neutrino physics questions, and is thus, one of the main focus of the neutrino experiments currently under construction [16, 21]. Knowing the mass ordering helps to define parameters for future experiments like neutrinoless double decay searches. Furthermore, it is a key parameter of the neutrino astronomy and neutrino cosmology [15].
Further open questions are [19]:

- The absolute mass scale of neutrinos
- Exact measurement of the neutrino properties
- CP violation
- Whether neutrinos are Majorana or Dirac fermions

- The number of neutrino generations. From the measurement of the total Z^0 decay width, it is known that there are three light[2] weakly interacting neutrino generations [11, p. 285], but it would be possible that so-called sterile neutrino exist

More comprehensive overviews of open questions are given in [19, 22]. To answer open neutrino physics questions, several new experiments are under construction. The reactor anti-neutrino detector JUNO is one of them, with a focus on the neutrino mass ordering and the precision measurement of neutrino mixing parameters.

[2] light refers here to a neutrino mass $m_\nu \leq m_{Z^0}/2$ [11, p. 285].

Chapter 3

The Jiangmen Underground Neutrino Observatory

The **J**iangmen **U**nderground **N**eutrino **O**bservatory (JUNO) is a future neutrino detector aiming to solve fundamental open questions in the regime of neutrino physics. The detector is currently under construction in South East China at about 40 km distance to Kaiping city, Jiangmen city, Guangdong province [15, p. 29]. The location is chosen to have an equal distance (baseline) of 52.5 km to the cores of each of two nuclear power plants in Yanjiang and Taishan (cf. Fig. 3.1).

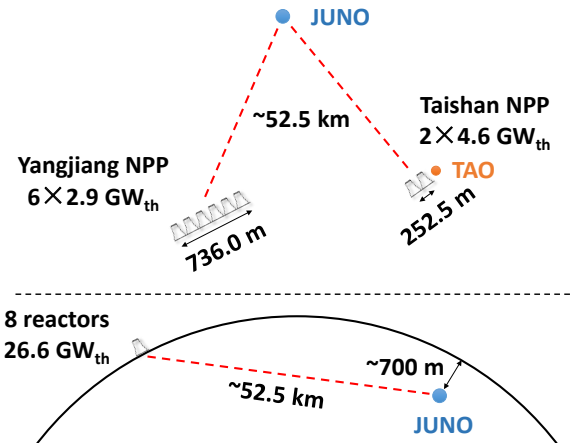


FIGURE 3.1: Relation of JUNO to the nuclear power plants in Yangjiang and Taishan [23]. The Taishan Antineutrino Observatory (TAO) is a detector for measuring a reference anti-neutrino spectrum in a distance of about 30 m from one reactor core [24].

3.1 JUNO overview

An overview picture of the experimental site of JUNO and its campus is given in Fig. 3.2. JUNO itself is located underground with an overburden of more than 700 m of rock to shield the detector from cosmogenic background [15, p. 30].

A drawing of the central detector hall of JUNO is shown in Fig. 3.3. The central part of the detector is a spherical **A**crylic **V**essel (AV) with a diameter of 35.4 m holding 20 kt of LS. The AV is instrumented with 17 612 20″ PMTs and 25 600 3″ PMTs which are also denoted as **C**entral **D**etector (CD) [25]. The expected photo-coverage is more than 75 % and it is aimed for an energy resolution of $< 3\,\%/\sqrt{E[\mathrm{MeV}]}$ at

FIGURE 3.2: Image of the JUNO site under construction [23]. The underground facilities can be accessed via the slope tunnel or the vertical shaft.

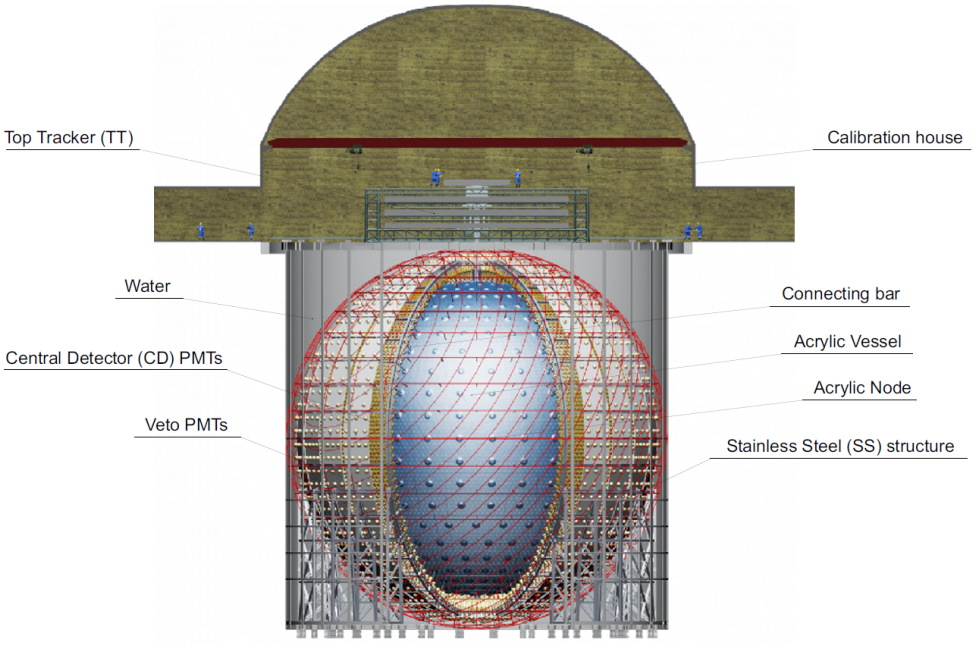


FIGURE 3.3: Overview of the underground experimental hall [25].

1 MeV [25]. The AV and the PMTs are mounted on a stainless steel support structure which is placed in a cylindrical water pool to shield the detector from radioactivity of the surrounding rock. The water pool is also instrumented with PMTs (Veto PMTs) to detect cosmic ray muons via Cherenkov radiation [18, p. 110]. Additionally, the so-called top tracker is placed on top of the water pool to help with tagging and track reconstruction of cosmic muons.

Further facilities underground are rooms for the electronics, power and the LS purification (LS hall).

3.2 JUNO physics program

JUNO detects the electron anti-neutrinos from the nuclear reactors via the **I**nverse **B**eta **D**ecay (IBD) reaction [15]

$$\overline{\nu}_e + p \rightarrow e^+ + n.$$

A positron e^+ and a neutron n are created from the reaction between the electron anti-neutrino $\overline{\nu}_e$ and a free proton p. The positron subsequently annihilates with an electron into two 511 keV photons. The neutron loses its energy via scattering and thermalizes. It is captured by a free proton about 200 µs later and yields a 2.2 MeV γ-ray [15]. This characteristic coincidence of a prompt (annihilation) and a delayed signal (capture) is used for the event selection. With a total combined thermal power of 26.6 GW from the nuclear reactors, about 60 IBD counts per day are expected [25].

Fig. 3.4 shows a sketch of the IBD energy spectrum. This is a plot of the surviving electron anti-neutrinos as function of their energy (cf. Eq. (2.8)). The mass ordering is visible in the fine structure oscillation. A high energy resolution is required to distinguish the two orderings.

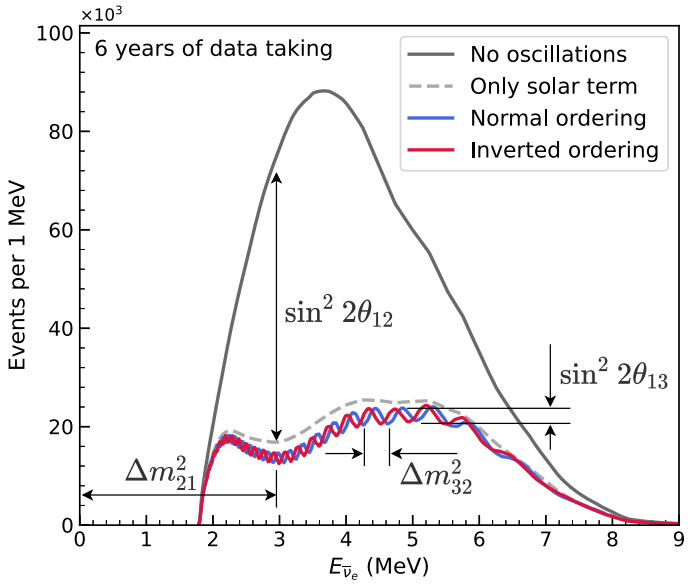


FIGURE 3.4: Visualization of the JUNO IBD energy spectrum after six years of data taking [23]. The dip around 3 MeV corresponds to the solar oscillation term, whereas the fast oscillation corresponds to the atmospheric term.

The IBD measurements can not only be used to determine the neutrino mass ordering, but also for the precise determination of other neutrino mixing parameters. JUNO aims to achieve a precision in the order of 0.5 % to 0.7 % for the parameters $\sin^2\theta_{12}$, Δm^2_{21} and $\left|\Delta m^2_{ee}\right|$ [15, p. 55]. A comparison of those three parameters with the current best fit values from the combination of experimental data is given in Table 3.1.

TABLE 3.1: Comparison of those oscillation parameters for which JUNO's precision is higher than the combined fit of current measurements. These global fit values are taken from [26]. Data for JUNO are taken from [15, p. 63] and include estimations for systematic uncertainties.

	Δm^2_{21}	$\lvert\Delta m^2_{31}\rvert$ resp. $\lvert\Delta m^2_{ee}\rvert$	$\sin^2\theta_{12}$
Global 1σ	2.8 %	1.3 %	4.0 %
JUNO expected 1σ	0.59 %	0.44 %	0.67 %

Apart from the determination of the neutrino mass ordering and neutrino precision measurements, JUNO has a rich non-oscillation neutrino physics program. Those neutrinos do not stem from the nuclear reactors, but from other sources. Examples are the measurement of low energetic atmospheric neutrinos [27], diffuse supernova neutrino background [28], supernova burst neutrinos [29], geo-neutrinos [30] and searches for dark matter [31]. A comprehensive overview over the physics program is given in [15].

One part of the physics program is the measurement of solar neutrinos. In contrast to IBD events, these do not feature a coincidence signal but correspond to single events [32]. Thus, even lower backgrounds are required compared to IBD measurements.

3.2.1 JUNO Backgrounds

Accidental backgrounds mimic the prompt and delayed events and need to be reduced. The radioactivity from the LS itself is denoted as *internal background*. In contrast, backgrounds from other detector components, the rock, the air, etc. are called *external background*. Several sources of natural radioactive backgrounds like ^{238}U, ^{232}Th, ^{40}K, ^{226}Ra or ^{222}Rn can be present in the materials used for the detector [25].

Rigorous effort has been put into the control of radioactivity in JUNO (described in more detail in [25]). It is a key factor to reduce the internal and external backgrounds to reach the required detector performance.

Apart from the careful selection of detector materials, the impact of the external background can be reduced by implementing an (energy dependent) fiducial volume cut. By this, events at the outer shell close to the border of the AV are excluded from the analysis. A fiducial volume cut is not useful for the internal background originating from the LS itself since the signals are distributed uniformly in the sensitive volume [32]. Therefore, the contamination of the LS with radioactive elements has to be minimized to reach the target detector performance.

A multi-step purification plant is installed to remove radioactive contaminants from the scintillator. This includes Al_2O_3 filtration columns (for improving optical properties), distillation (to remove heavy metals and improve the transparency), water extraction (to remove radioisotopes from U/Th chains and ^{40}K), and steam stripping

(to remove gaseous impurities, such as Kr and Rn) [32, p. 19]. Tests with prototype plants have shown that the target contamination limit of $1 \times 10^{-15}\,\mathrm{g\,g^{-1}}$ for U/Th is within reach [32, p. 19].

In order to verify the efficiency of the purification plant and for monitoring the LS during filling, the dedicated detector OSIRIS is built as last part of JUNO's purification chain [33].

3.3 OSIRIS

The **O**nline **S**cintillator **I**nternal **R**adioactivity **I**nvestigation **S**ystem (OSIRIS) is part of JUNO's liquid scintillator filling chain and located underground in the LS hall. As one of the last elements before the inlet to the CD AV it is designed to verify the radiopurity of the LS. Depending on the requirements from different analysis programs, two different limits for the concentration of isotopes of the U/Th decay chain are identified. A limit for the U/Th concentration for IBD-based analyses is set to $1 \times 10^{-15}\,\mathrm{g\,g^{-1}}$, and a limit for solar neutrino based analyses is set to $1 \times 10^{-16}\,\mathrm{g\,g^{-1}}$ – $1 \times 10^{-17}\,\mathrm{g\,g^{-1}}$ [33]. OSIRIS is designed to asses the $1 \times 10^{-15}\,\mathrm{g\,g^{-1}}$ limit in real-time before filling the detector [25].

3.3.1 Detector design

A drawing of the detector is shown in Fig. 3.5. A cylindrical steel tank with a height of 9 m and a diameter of 9 m houses most of the detector elements and the AV which is filled with 21 m^3 LS [33]. This vessel is surrounded by an ultra-pure water buffer for shielding against external radiation. 75 PMTs are placed within the buffer. 64 of them are facing towards the AV and are optically separated from the remaining PMTs. Latter build the muon veto and measure events by detecting Cherenkov radiation in the water buffer. Further parts of the detector like electronics racks are placed on the top of the steel tank.

Liquid temperatures OSIRIS is located ∼700 m underground where the rock has a temperature of ∼31 °C [18, p. 281]. The temperature of the ultra-pure water tank will be cooled to 21 °C which is the target temperature for the LS for the CD. The LS for OSIRIS is preheated to provide layers of LS within the AV due to the temperature induced densities differences. This filling strategy should prevent larger mixing between LS already residing in the AV and new LS.

3.3.2 iPMT system

The light detection system for OSIRIS is a new development called intelligent Photomultiplier Tube (iPMT). These are PMTs with electronics directly attached to their back. For the synchronization of multiple iPMTs, additional electronics is required in form of so-called **S**urface **B**oards (SBs) which are located on top of the steel tank. The SBs provide also trigger signals for the calibration systems. The iPMT system is described in greater detail in Chapter 4.

The PMTs cover ∼9 % of the full solid angle and provide a light yield of about $280\,\mathrm{p.e.\,MeV^{-1}}$ [33, p. 3]. The corresponding energy resolution is assumed as $\sigma_E \approx 6\%\sqrt{E[\mathrm{MeV}]}$, whereas the resolution of the three-dimensional vertex reconstruction is expected to be in the order of 24 cm [33, p. 19].

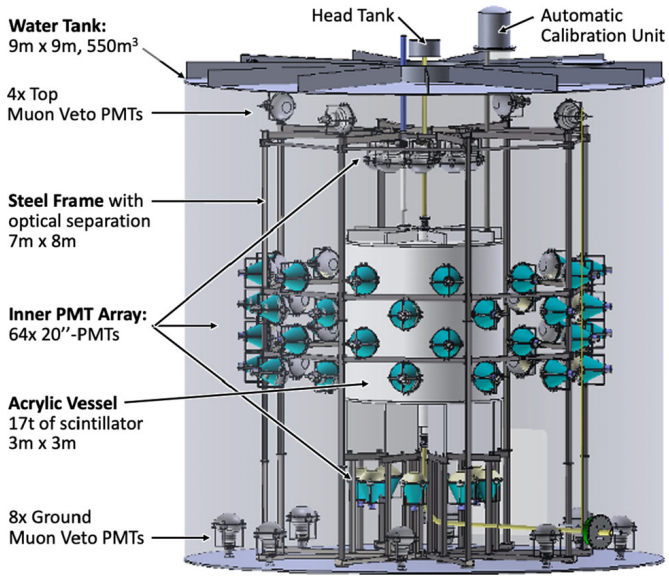


FIGURE 3.5: Overview of the OSIRIS detector [33]. Not all infrastructure on top of the water tank is shown.

3.3.3 Event Builder

As part of the iPMT concept, the event trigger is implemented purely software based. All iPMTs send their self-triggered hits[1] to a central instance, which is called **E**vent **B**uilder (EB). This software decides which data should be kept for later analysis and which data are discarded. The default trigger mode for the operation of OSIRIS is a coincidence of five PMT hits within a window of 70 ns [33, p. 16].

3.3.4 Calibration systems

OSIRIS features two calibration systems, a *fiber system* and a *source insertion system*. The tasks of the fiber system are the precise calibration of the relative timing and charge of the iPMTs. Therefore, light can be injected from 24 different diffusors into the detector. A laser with a pulselength of 80 ps and a wavelength of 420 nm is used to illuminate the PMTs with very low light intensities [33, p. 12].

The source insertion system is based on the so-called automatic calibration unit (ACU) from the Daya Bay collaboration. It supports up to three sources which can be lowered individually into the detector via a cable. For OSIRIS, a blue LED, a multi-gamma source and a low-activity potassium source are foreseen. The LED can be used for cross-checking the fiber system and for higher light intensities. The multi-gamma source is primarily foreseen for the energy and position reconstruction. The low-activity potassium source will be used to monitor the LS light yield via the decay of ^{40}K [33, p. 14f.].
Both system are described in more detail in [33, p. 12 ff.].

[1] Hits are signals which fulfill selection criteria, like crossing a certain threshold. These signals may be induced by random noise or by impinging light.

3.3.5 OSIRIS detection mechanisms and sensitivity

OSIRIS measures the concentrations of uranium and thorium by detecting a coincident decay of isotopes of the respective decay chain. Part of the decay chain of ^{238}U is the isotope ^{214}Bi which decays via β^- radiation into ^{214}Po with a branching ratio of $> 99\,\%$[2]. It features a broad energy spectrum with an end point energy of about 3.2 MeV. ^{214}Po decays with a half life of $T_{1/2} = (163.46 \pm 0.04)\,\mu s$ via α emission into ^{210}Pb. The emitted α particle has an energy of about 7.8 MeV, but the visible energy is reduced to 0.5 MeV to 1 MeV due to quenching[3] [33, p. 22]. The fast coincidence is denoted as Bi–Po event. A simulation of the ^{214}Bi – Po energy spectrum including energy cut windows, which are used for the event selection, is shown in Fig. 3.6.

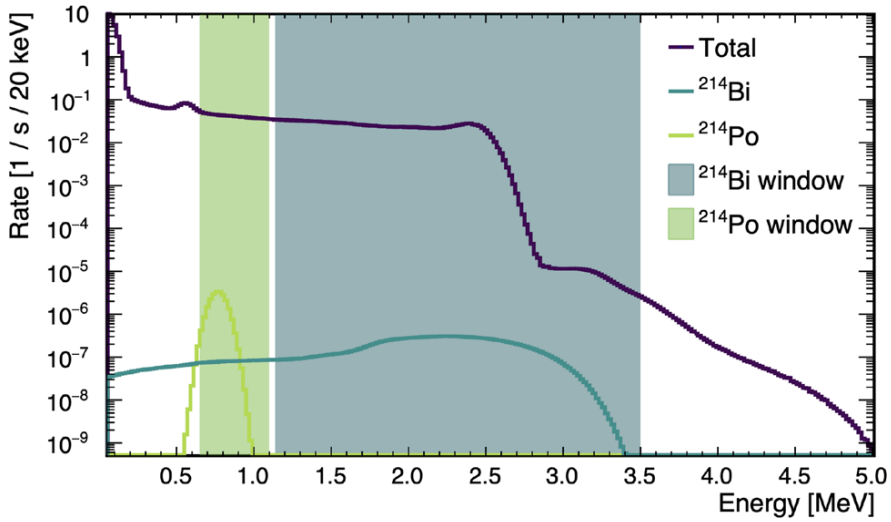


FIGURE 3.6: OSIRIS Bi–Po energy spectrum with energy cut windows for ^{214}Bi – Po [33].

A similar coincident signal is present in the decay chain of ^{232}Th with the β^- decay of ^{212}Bi into ^{212}Po with a branching ratio of $\sim$64 %. ^{212}Po subsequently decays into to ^{208}Pb via α emission with a half life of $T_{1/2}(^{212}\text{Po}) = (294.3 \pm 0.8)$ ns.

Backgrounds Backgrounds for OSIRIS stem from natural and cosmogenic radioactivity. Most radioactive decays produce single events and do not feature a coincident decay as in case of the Bi–Po. Nonetheless, accidental coincidences from single-events have to be considered [33]. Main contributors to OSIRIS backgrounds are ^{40}K and the isotopes from the ^{238}U and ^{232}Th decay chains (especially radon) from the outer detector material and the surrounding rock. A simulation of the total background is given in Fig. 3.7.

Determination of U/Th abundance With the assumption of a secular equilibrium, the limit on the mass abundance of ^{238}U/^{232}Th can be directly calculated from the measured Bi–Po rates [33]. With the presence of radon emanated in the JUNO LS system the assumption of secular equilibrium does not longer hold. ^{222}Rn (^{220}Rn)

[2] These and following nuclear data in this section are taken from [34].

[3] Quenching is part of the non-linear response of the scintillator to the ionization density [11, p. 554].

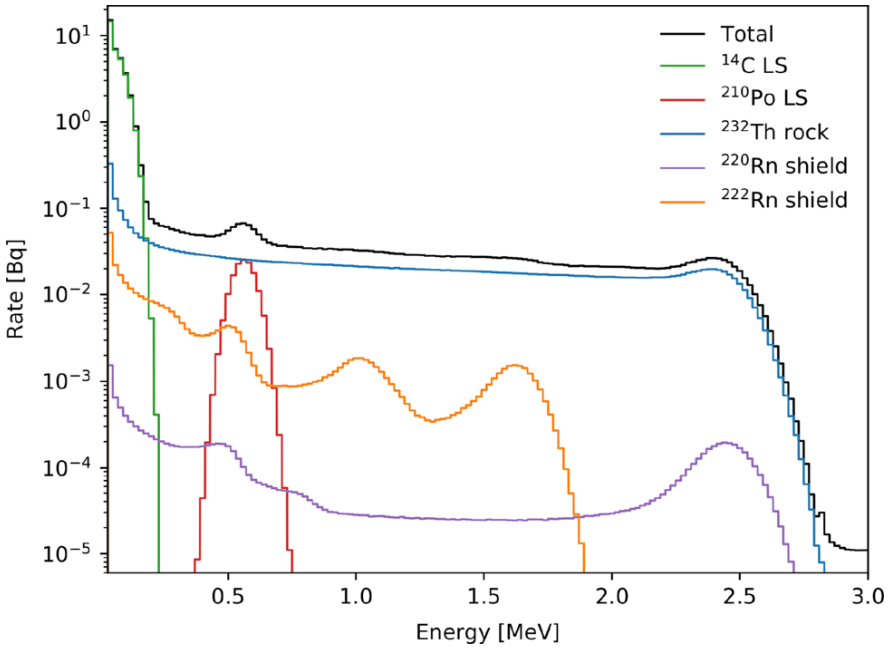


FIGURE 3.7: Energy spectrum of the total background rate [33].

are precursor isotopes of ^{214}Bi (^{212}Bi) within the respective decay chain, introducing an additional Bi–Po rate superimposed on the Bi–Po events originating from U/Th decays. With relevant half lifes in the order of hours to few days, the isotopes are relatively short lived.

The radon contamination leads to different effective measurement times to reach the required limits depending on the operation mode.
OSIRIS will be used in two operation modes. In the so-called batch mode, OSIRIS is filled with a LS sample and observes this for a time in the order of weeks. With the known decay profile of the radon isotopes, a time dependent fit can be performed. Fig. 3.8 displays the corresponding sensitivity for two scenarios of radon contamination. It takes 7 (2.5) days to reach the $1 \times 10^{-15}\,\mathrm{g\,g^{-1}}$ limit for U (Th) [33].

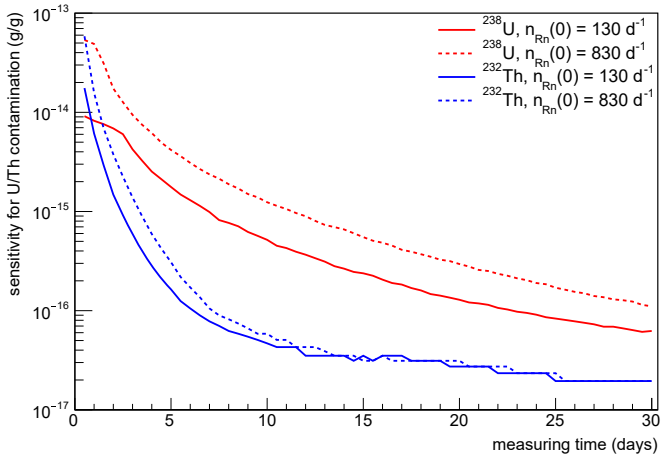


FIGURE 3.8: Sensitivity of OSIRIS to ^{238}U/^{232}Th for two different scenarios of an initial radon contamination of 130 and 830 counts per day [33].

In the continuous operation mode, the LS is constantly replaced with fresh scintillator by feeding it at the top of the AV at an expected rate of about $1\,\mathrm{m}^3\,\mathrm{h}^{-1}$. Thus, the passage of the scintillator through OSIRIS takes almost one day [33]. In this case, the determination of the U/Th contamination requires a more elaborated analysis taking into account the reduction in the decay rates when the LS slowly sinks within the AV. The sensitivity in this mode depends highly on the knowledge of the off-equilibrium radon rate. The expected upper limits are in the range from $1.4 \times 10^{-14}\,\mathrm{g\,g}^{-1}$ to $\sim 1 \times 10^{-15}\,\mathrm{g\,g}^{-1}$ and thus close to the IBD limit. A more detailed description of the analysis is given in [33].

Chapter 4

Intelligent Photomultiplier Tube System

This chapter gives a detailed description of the iPMT system. The first section motivates the architecture and describes the design goals. The second part introduces shortly the basic principles of PMTs. The remainder of the chapter gives a detailed description of the system with a focus on the electronics design.

4.1 Motivation and Concept

Neutrino detectors instrument typically large volumes, due to the very low cross-section of neutrino interactions with matter. Examples for such detectors are Double-Chooz with a target volume of 2 times 8 t [35], DayaBay with a target volume of 8 times 20 t [36], SuperK with a volume of 50 kt [37] or JUNO with its target volume of 20 kt [15]. Cost efficient devices to cover the large detector surfaces are PMTs. Typically, they have a diameter in the range from 8" (DayaBay [38, p. 17]) up to 20" (SuperK [37, p. 8], JUNO [18, p. 137]).

Due to the dimensions of the detectors, long coaxial cables are typically used to transmit the analog signals from the PMTs to the signal processing electronics. DoubleChooz, for example, used cables with a length of 20 m [35], DayaBay used cables with a length of up to 52 m [38].

The use of long coaxial cable has significant effects on the signal due to attenuation. Table 4.1 gives an overview over typical frequency dependent attenuation values for coaxial cables. The bandwidth required for PMT pulses is typically in the range up to ∼400 MHz [39]. These effects becomes more severe with larger detectors. For the so-called external readout scheme for JUNO, coaxial cable length in the range of 80 m to 100 m were assumed [18, p. 223], which would result in an attenuation as given in Table 4.1. The frequency dependent attenuation leads also to a dispersion resulting in a pulse distortion and reduction in amplitude [40]. This effect can become especially important at low signal levels close to the noise floor.

In order to mitigate problems with long analog cables, a concept with digitizing and processing electronics directly attached to the PMT has been developed. They are named **i**ntelligent **P**hoto**M**ultiplier **T**ube (iPMT), expressing the goal to design a system around a conventional PMT with a higher degree of integration and advanced functionality. The expression "intelligent PMT" has originally be coined for this concept for the JUNO central detector [18, p. 210ff.]. It has been developed as one of the possible readout schemes for JUNO, but has not been chosen as final scheme [39].

TABLE 4.1: Cable attenuation for different coaxial cables for a length of 100 m. RG303 has been used in DoubleChooz [35]. 609C5019A is a cable which has been evaluated for an external readout scheme for JUNO [18, p. 223]. Aircell 7 is a dedicated low-loss cable, but not suited for PMT's operating high voltage. An attenuation of 3 dB (10 dB) corresponds to an attenuation of the amplitude from 100 % to ∼71 % (∼32 %) (using: attenuation [dB]$= 20 \cdot \log_{10}(V_{\mathrm{rx}}/V_{\mathrm{tx}})$ with the initial amplitude V_{tx} and the recorded amplitude V_{rx}).

frequency [MHz]	RG303 [71] [dB]	609C5019A [18, p. 223] [dB]	Aircell 7 [72] [dB]
50	9	-	4.29
100	13	12.3	5.97
200	19	17.7	8.59
300	24	-	10.64
400	28	-	-

A solution with short cables (about 1 m) to a dedicated box for digitization and processing for three PMTs is used for JUNO instead [25].

The idea of the intelligent PMTs is implemented in OSIRIS as described in Section 3.3 but with a complete redesign of the electronics. The concept aims for

- high **S**ignal-to-**N**oise-**R**atio (SNR) by mounting the electronics directly on the PMT pins
- use of the dedicated PMT readout **A**pplication-**S**pecific **I**ntegrated **C**ircuit (ASIC) VULCAN with advanced functionality
- implementation of performance improving algorithms at device level
- easily deployable system with standalone detector units
- use of commercial electronics for power distribution and system level trigger to profit from cost reduction in highly competitive markets

Further design goals of the iPMT are based on the requirements for OSIRIS. This has the consequence of partially relaxed requirements compared to JUNO, especially regarding reliability due to the shorter expected run-time of OSIRIS. Several aspects are taken into account for the design of the iPMTs, covering requirements from physics, system integration and mechanics.

Physics requirements The SNR should be on a level that the signals on single p.e. level (cf. Section 4.2) are clearly resolved and that the trigger threshold can be chosen such that those events are recorded. Large signals should be measurement with a lower resolution for signals up to several hundred p.e. The time resolution should be such that the PMT **T**ransit **T**ime **S**pread (TTS) σ_{TTS} (which is in the order of 1 ns to 1.5 ns, cf. Fig. A.1b) is the dominant contributor.

System requirements The data transmission capability of the system should be sufficient to transmit waveforms with a rate of the **D**ark **C**ount **R**ate (DCR) (cf. Section 4.2.1) of the PMTs plus a reasonable margin to the EB of OSIRIS (cf. Section 3.3.3).

Since the water buffer of OSIRIS is kept at a temperature of 21 °C [33], heat which is produced by the iPMTs in the water buffer has to be removed. Thus, the power per channel should be on a reasonable level, which is for JUNO considered to be in the order ≈10 W [39, p. 2].

Mechanical requirements Since the iPMT electronics is mounted at the back of a PMT (cf. Fig. 4.2) the design aims for a diameter in the order of the PMT neck diameter. With a glass diameter size of about 7.5 cm close to the signal pins, the **P**rinted **C**ircuit **B**oard (PCB) diameter was chosen to 10 cm.

4.2 Photomultiplier tubes

Since the iPMT is built around a PMT, a brief overview of relevant general PMT properties is given in this section.

Working principle PMTs are very sensitive light detectors which are able to resolve signals ranging from single photons up to few thousand photons. A sketch of the working principle is given in Fig. 4.1a. An impinging photon is converted via the photoeffect in the photocathode into an electron. The electron is accelerated and focused towards the first dynode. Through secondary emission of electrons by the dynodes, further electrons are generated and an electron avalanche builds up [41]. The output signal of the PMT is the electron avalanche at the anode which can be measured as a current. The charge which corresponds to the signal of a single photon is denoted as single photon electron equivalent, short 1 p.e. (or single p.e.).

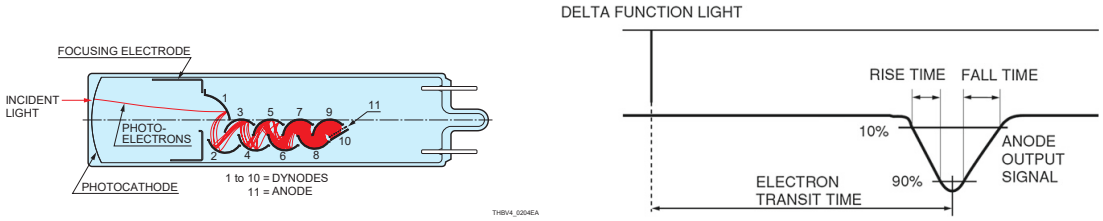
4.2.1 PMT properties

The PMT properties which are of most relevance for this thesis are given in the following, more detailed information can be retrieved in [41].

Dark count rate Signals on single p.e. level are generated in a PMT even without illumination. This effect is called dark current, respectively dark count. It occurs mainly due to thermal emission of electrons from the photocathode or dynodes, which are subsequently amplified like electrons generated by impinging photons. The term **D**ark **C**ount **R**ate (DCR) refers to the signal rate for a certain threshold, often chosen to 50 % of the mean single p.e. amplitude.

Transit Time Spread The transit time denotes the time between the generation of a photo electron at the cathode and the signal output at the anode. More relevant for the detector is the variation in the transit time, which is denoted as **T**ransit **T**ime **S**pread (TTS). For the PMT type used for OSIRIS, the TTS is in the range of 1 ns to 1.5 ns (cf. distribution in Fig. A.1b[1]).

[1] Fig. A.1b states the TTS in terms of the **F**ull **W**idth **H**alf **M**aximum (FWHM). This can be converted into a standard deviation under the assumption of a gaussian TTS with $\sigma_{\mathrm{TTS}} = \mathrm{FWHM}_{\mathrm{TTS}}/(2\sqrt{2\ln 2})$.



(a) (b)

FIGURE 4.1: (a) Sketch of a PMT cross section [41]. (b) Definition of transit time, rise time and fall time [42].

Gain The gain is defined as the current at the anode over the photoelectron current from the photocathode [41, p. 48 f.]. An alternative name for gain is therefore "current amplification". The gain g of a PMT is highly dependent on the applied high voltage and can be approximated by

$$g = A \cdot V^{kn} \tag{4.1}$$

with the applied high voltage V, with the constants A, k being determined by the structure and material of the PMT and n, the number of dynodes [41, p. 48f.]. In Fig. A.2a the gain vs. voltage curve is shown, a gain of $1 \times 10^7\, e\, e^{-1}$ is the nominal gain for the PMT type used in OSIRIS.

Rise and fall time The rise time of a PMT signal is defined as the time difference between reaching 10 % and 90 % of the amplitude as depicted in Fig. 4.1b. Accordingly, the fall time is defined as time from 90 % to 10 % of the peak pulse height. The rate of change of the signal puts certain requirements on the readout electronics in term of the bandwidth. Most relevant parts of the signal are expected in a frequency range up to $f = 1/T_{rise}$ with the signal rise time T_{rise} [40]. The typical rise time for *Hamamatsu* 20″ PMTs is 6 ns [73], corresponding to $f \approx 170$ MHz.

Hamamatsu PMT R15343 OSIRIS uses high-quantum efficiency PMTs of the type *Hamamatsu* R15343 which are identical to the type R12860 [43, 33, p. 93]. The PMTs have ten dynodes, which are arranged in a box and line structure [73]. Table 4.2 lists the properties of the type R12860.

4.3 iPMT mechanics overview

Fig. 4.2 shows a drawing of the main elements of an iPMT. The PMT is surrounded by an electromagnetic shielding consisting of alumina foils and amorphous metal. A PMMA (Polymethylmethacrylat) ring is glued to the PMT and the ring is screwed to a stainless-steel holder. On the backside of the PMT, a stack of electronic PCBs is soldered on the pins (electric connectors) of the PMT. This stack is described in detail in Section 4.4. It is encapsulated in a stainless steel shell, which is glued to the PMMA ring. The procedure of gluing all components onto the PMT is referred to as *potting*. For a better heat transfer, the shell is filled with mineral oil. A detailed description of the potting procedure is given in [44].

TABLE 4.2: Properties of the PMT type R12860. For the OSIRIS PMTs, the distribution of the nominal voltages is given in Fig. A.1c and a distribution of the TTS in Fig. A.1b.

property	value
diameter	508 mm
weight	approx. 8 kg
typical quantum efficiency at 390 nm	30 %
typical gain	1×10^7 e/e
voltage for typical gain	2000 V
typical rise time	6.0 ns
typical TTS (FWHM)	2.4 ns

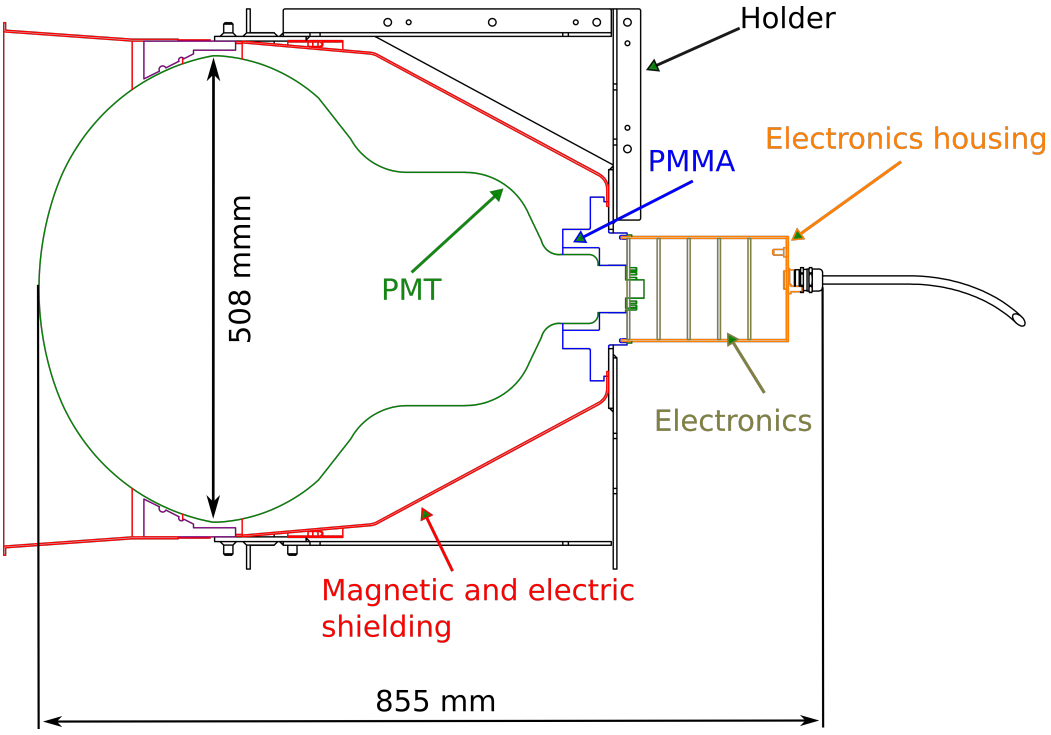


FIGURE 4.2: Sketch of an iPMT including the holder for mounting in OSIRIS. Drawing provided by Cornelius Vollbrecht.

4.4 iPMT electronics stack

This section explains the electronics parts of an iPMT. Fig. 4.3 gives an overview of an assembled electronics stack. It consists of five boards with a diameter of 10 cm each. The development of the electronics was done by the working group under the leadership of Jochen Steinmann. Drawing the schematics and the PCB layouts have been done by Jochen Steinmann, whereas the work of this thesis concentrated on the debugging, testing and validation of the designs. The iPMT electronics stack consists of the following boards, which are abbreviated based on their functionality as following:

PoE-Board The abbreviation PoE stands for **P**ower **o**ver **E**thernet, a standard for transmitting power via twisted-pair cables. Since this technique is used on the board, it is referred to as **P**ower **o**ver **E**thernet (PoE)-Board.

SCCU-Board The **S**low **C**ontrol and **C**onfiguration **U**nit provides interfaces to other components and manages readout and control of sensors (also known as "Slow Control").

Readout-Board Main tasks of the **R**ead**o**ut **B**oard (RoB) are the PMT signal digitization (readout) and processing.

HV-Board The HV-Board provides **H**igh **V**oltage (HV) for the PMT. The typical PMT supply voltage for the used type is in the order of 2000 V.

Base-Board The PMT requires certain voltages being applied to the pins which are connected to the different dynodes. The supply voltage from the HV-Board is divided into the required voltages on this board.

4.4.1 Connectivity

The iPMT features a single CAT5e cable as power and data connection. The cable contains 4 twisted-wire pairs with an alumina foil based shielding for each pair. A braided shield encloses all wires. As measure against the propagation of water along the cable in case of a cable damage, a water-blocking powder is included. The outer jacket consists of high-density polyethylene (HDPE), which is used for its compatibility with ultra-pure water. The assignment of the wire pairs is shown in Table 4.3. Pairs 1 & 2 implement standard 100 Mbit Ethernet combined with PoE. Pairs 3 & 4 are used for synchronous transmission between the SB and the iPMT. The SYNC RX connection provides a dedicated data stream with an embedded 125 MHz clock signal for the synchronization of the iPMT (sync data stream).

The length of the cable varies depending on the mounting position within OSIRIS. For iPMTs mounted at the top of the detector the cable length is 17 m, for those at the center ring 22 m and iPMTs at the bottom have 25 m long cables [33, p. 12].

4.4.2 PoE Board

This board implements handling of the PoE protocol and subsequent conversion of the voltage from the PoE level to 24 V and 5 V. A picture of the board is shown in Fig. 4.4a with a highlighting of different functional blocks. PoE is a standard which defines the power delivery of twisted-wire pairs used in Ethernet communication. This board

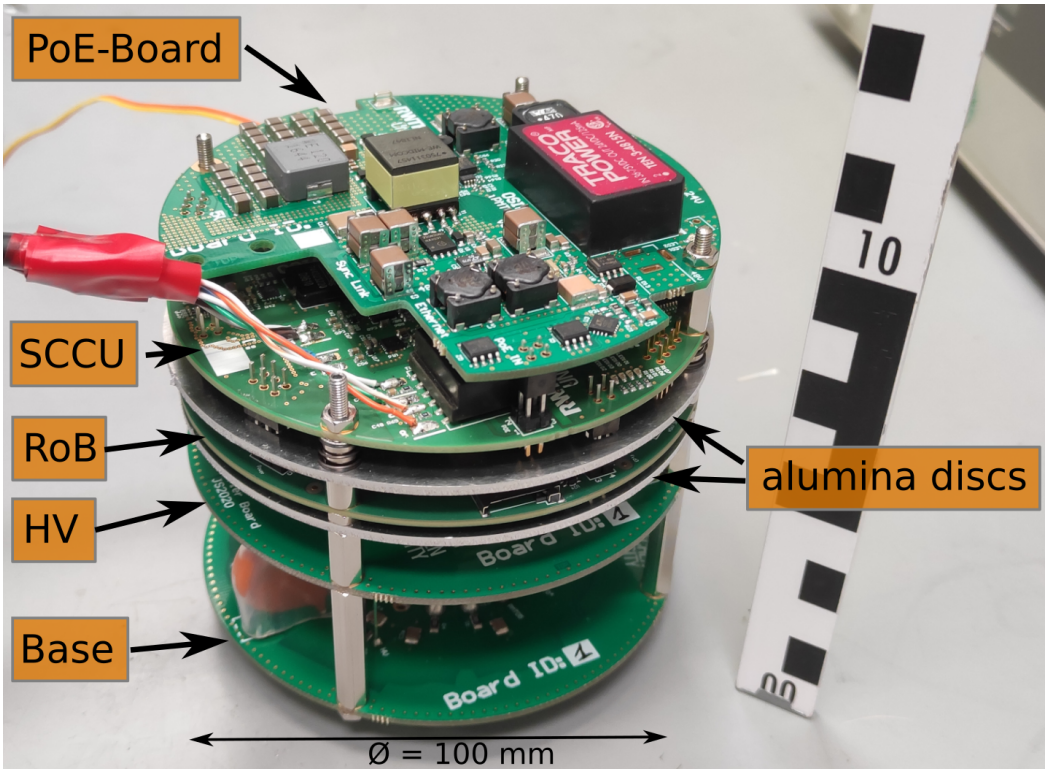


FIGURE 4.3: Assembled electronics stack. Alumina discs are placed above and below the RoB for better heat transfer. The black/white divisions on the folding rule have a width of 1 cm.

TABLE 4.3: Wire pair assignment of the iPMT CAT5e cable.

pair	name	function
1	ETH RX	asynchronous receive and power over ethernet
2	ETH TX	asynchronous transmit and power over ethernet
3	SYNC TX	synchronous transmission to SB
4	SYNC RX	synchronous receive from SB

implements the standard 802.3at-2009 PoE, also known under the name PoE+ by using commercially available **I**ntegrated **C**ircuits (ICs). Two twisted-pairs are required for the power delivery. The voltage is in the range from 42.5 V to 57 V. The standard defines different classes of devices with varying delivered power. The iPMT is defined as a so-called Class 4 device, which would allow a maximum delivered power of 25 W. The next lower Class 3 allows for a maximum power of 12.95 W which has been considered as too limited. However, the power required by an iPMT is with about 10 W much lower and furthermore limited by the maximum power of the internal converters[2]

The PoE voltage has to be converted according to the requirements of the different components on the different boards. In a first step this is done by using an isolated DC/DC converter which converts the PoE input voltage to 5 V (denoted as 5 V DC/DC in the following). Other boards implement further conversion steps to e.g., 3.3 V, 2.5 V or 1 V as required on each board. A structural overview is given in Fig. 4.4b.

4.4.3 SCCU - Slow control and configuration unit

The **S**low **C**ontrol and **C**onfiguration **U**nit (SCCU) is the central communication interface of the iPMT. This board hosts a 4-port Ethernet switch (3 ports are used) to connect the Ethernet uplink with the RoB and with a microprocessor on the SCCU. This microprocessor is a STM32 IC which is based on an ARM Cortex CPU (cf. Fig. 4.5a).

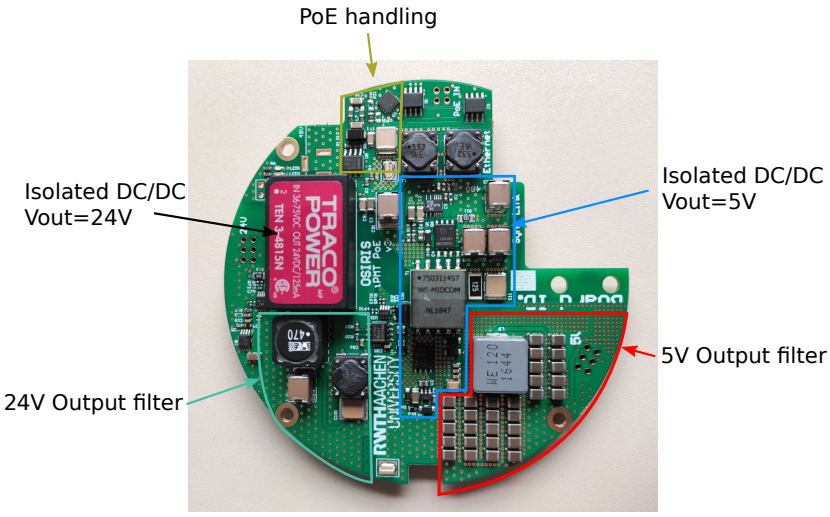
The firmware for this chip has been written by Tim Kuhlbusch. It is stored on an internal 512 KiB flash memory. Changing the firmware of the STM32 after potting of the iPMT is not possible. Therefore, the firmware has been improved and verified over more than two years to ensure a correct operation.

The SCCU is used to interface to other system components (also on other PCBs) and provide access to these components via Ethernet (visualized in Fig. 4.5b). Thus, the SCCU acts as protocol translator between different (hardware) protocols and Ethernet. This includes the following protocols:

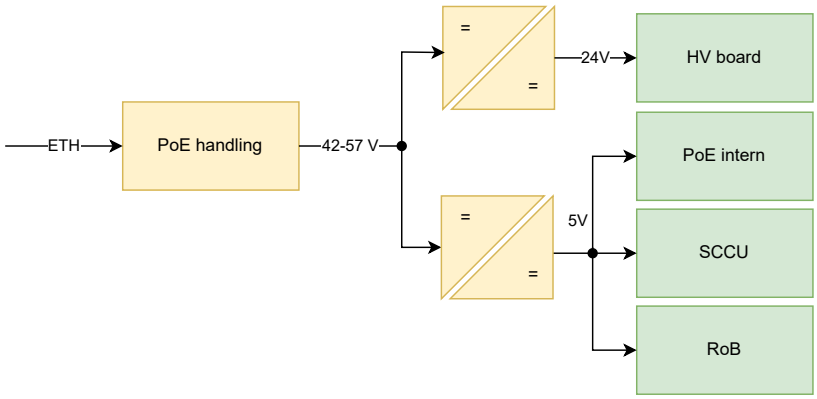
- **I**nter-**I**ntegrated **C**ircuit (I²C) to PoE, SCCU, RoB (via a custom **U**ser **D**atagram **P**rotocol (UDP)[3] based protocol)
- **J**oint **T**est **A**ction **G**roup (JTAG) connection to VULCAN and ZYNQ (via Xilinx Virtual Cable protocol [74])
- **U**niversal **A**synchronous **R**eceiver **T**ransmitter (UART) to the ZYNQ (via a telnet like protocol)
- EIA-485 to the HV module (same protocol as UART)

[2]The maximum input power of the 5 V converter is up to ∼16 W. Additionally, the 24 V converter would be able to deliver up to 3 W. However, since this converter only supplies the HV module for the PMT, the load is rather stable and limited by the maximum PMT HV setpoint. A typical input power of the 24 V converter is 0.8 W (cf. Table 6.1).

[3]a simple connectionless communication protocol without error checking and corrections.

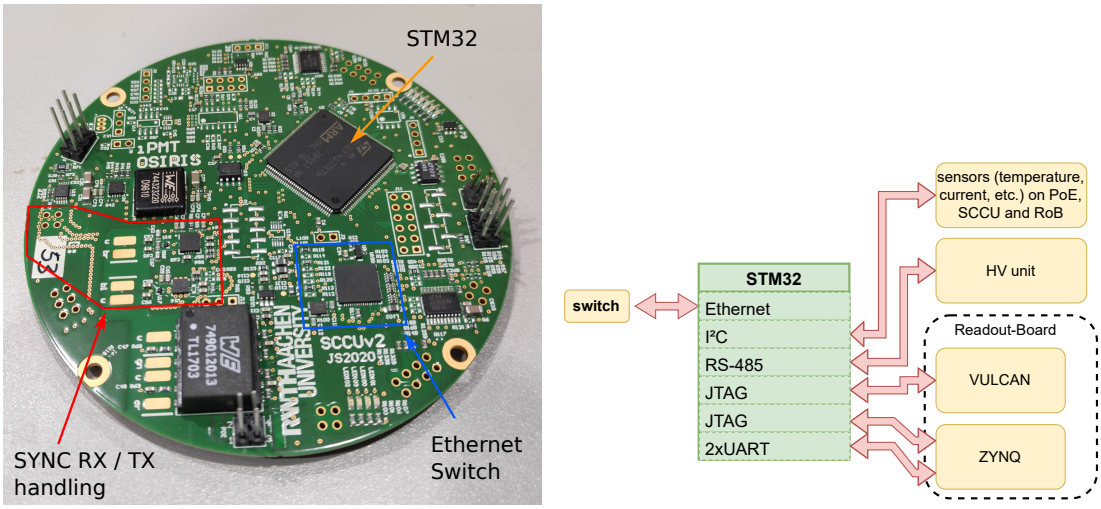


(a)



(b)

FIGURE 4.4: (a) PoE-Board with functional blocks labeled. (b) Overview of the power distribution.



(a) (b)

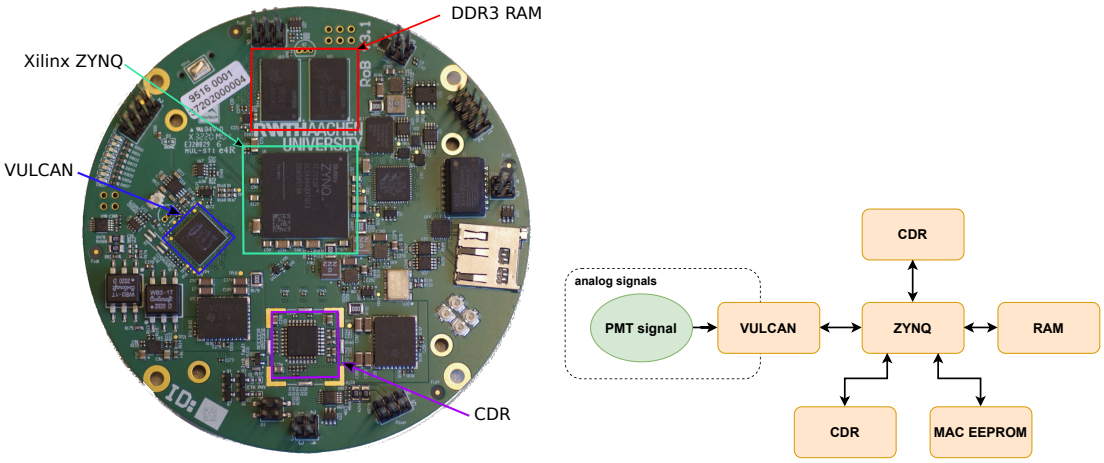
FIGURE 4.5: (a) SCCU PCB design with important components highlighted. (b) The STM32 IC on the SCCU provides access to different components via Ethernet by interfacing their respective protocol. VULCAN and the ZYNQ are described in Section 4.4.4.

4.4.4 Readout Board (RoB)

The central components for the digitization and processing of the PMT data are placed on the RoB. Since this boards contains components which are crucial for the understanding of the system, they are described in detail in the following sections.

ZYNQ The central component of the RoB is a Xilinx XC7Z020. This device is a so-called **S**ystem-**o**n-a-**C**hip (SoC). An SoC integrates a number of functional blocks on one chip. For the XC7Z020 a dual-core ARM A9 Cortex processor is combined with an FPGA from the Artix-7 family of Xilinx. This allows to implement functionality as "hardware" in the FPGA part of the SoC, as well as in software, which is executed by the dual-core processor. In the following, the term **P**rogrammable **L**ogic (PL) is used as name for the FPGA part of the ZYNQ (cf. Fig. 4.7) and **P**rocessing **S**ystem (PS) denotes the dual-core processors. An overview of further functional blocks which are available in the SoC is given in Fig. 4.7. Only a selected functionality is used by the iPMTs. This includes:

- I²C
- UARTs
- SD card (for debugging purposes only)
- 100 Mbit Ethernet
- DDR3 RAM
- XADC for monitoring of the supply voltages and temperature



(a) (b)

FIGURE 4.6: (a) RoB with different highlighted components. An explanation of the components is given in Section 4.4.4. Design partially supported by ZEA-2. (b) Overview of building blocks of the RoB.

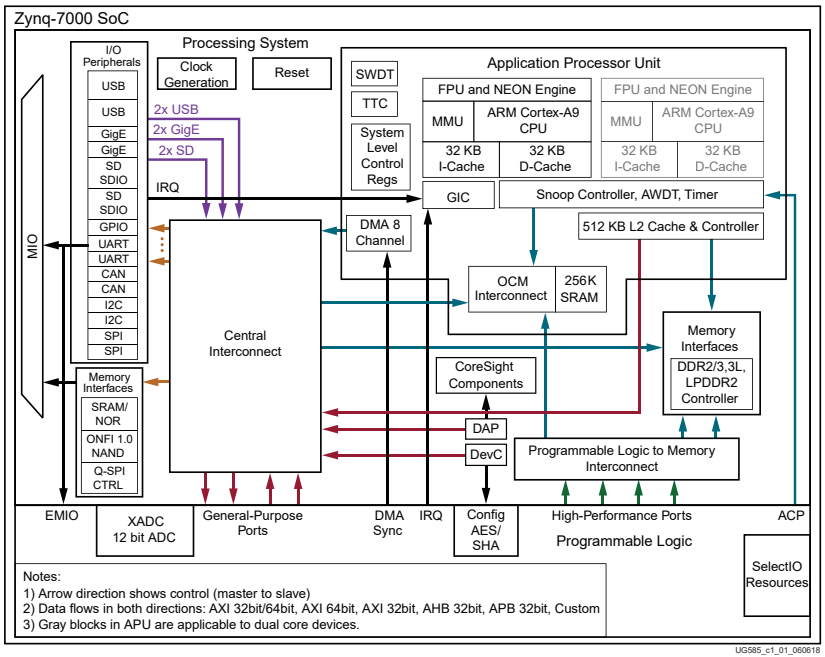


FIGURE 4.7: Overview of the Zynq-7000 functional blocks [75, p. 27].

DDR3 RAM In total 8 Gbit of DDR3 memory (2 ICs with each 4 Gbit) are used in the design. RAM is required by the **O**perating **S**ystem (OS) which is executed on the PS as well as for short term memory for the storage of PMT data.

MAC EEPROM The design hosts a memory (**E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory (EEPROM)) with a pre-configured EUI-48 node address (also known as MAC address) in a non-writable section. These kind of addresses are used to identify devices in networks. For the iPMT, the address is used to uniquely identify the RoB (the SCCU hosts a dedicated EEPROM for their identification). The address is read during the boot stage (cf. Section 5.6) and subsequently used for network communication.

CDR An important IC is the **C**lock and **D**ata **R**ecovery (CDR) chip. The used device is a *Micrel SY87700AL*. From an input data stream it generates a clock ("recovered" clock) with the same frequency as the bit rate of the data stream. A copy of the input data stream and the "recovered" clock, which is properly aligned with the data stream, are sent out. This allows for the transmission of a clock signal and a data signal over one transmission line. For the iPMTs, this enables an efficient use of the four wire-pairs (cf. Table 4.3). It allows for having a synchronous uplink connection (from the iPMT to the SB) instead of having two downlinks, which would be otherwise required for clock and data transmission. A more detailed explanation of the data stream is given in Section 5.4.2, whereas details of the CDR functionality are given in Appendix C.

Reference clock (REFCLOCK) A crystal oscillator *Silicon Labs Si530* is part of the design to serve as low-jitter clock, especially as reference for the CDR. It has a fixed frequency of 125 MHz.

VULCAN

The readout board features a highly integrated receiver chip for PMTs with the name VULCAN. It has been developed by the central institute of engineering, electronics and analytics (ZEA-2) of the Forschungszentrum Jülich. Foreseen to be used as part of the readout electronics of the JUNO detector, it is designed to fulfill the requirements given in the JUNO conceptual design report [18, p. 193 ff.]. The objective of this receiver chip is the digitization and processing of the PMT signal.

A challenge for the digitization is the wide dynamic range range from sub single p.e. to few thousand p.e. with the required time resolution using only one **A**nalog-to-**D**igital **C**onverter (ADC). In order to overcome this problem, some experiments have used parallel digitization of the output signal with two different gains [45, 46]. Also the JUNO central detector electronics scheme is designed with two gains [47]. The concept of using two simultaneous sampling tracks is extended by VULCAN to three tracks (Fig. 4.8a), which are denoted as RX (receiver).

The chip is highly configurable, featuring in total 329 register. 80 of them are so-called status register, which are connected to status information of sub-modules and read-only. 249 registers are used for configuration of the different modules in the design.

Interfaces VULCAN provides a JTAG interface for the access to the aforementioned registers, it is connected to one JTAG port on the SCCU. For the data transmission, VULCAN implements in total 20 **L**ow **V**oltage **D**ifferential **S**ignaling (LVDS) lines, which are divided into 16 ADC sample lines, three trigger lines and one clock signal. They are used to interface with the FPGA (cf. Section 5.2.4).

Input section Each RX features a transimpedance amplifier, a subsequent amplifier stage and an 8 bit ADC (Fig. 4.8b). The configuration of each RX is independent from the other RX. Thus, different amplifications for the individual RX can be configured to achieve the desired dynamic range. The RX are named by the configured amplification: The receiver with the highest amplification is denoted as **H**igh **G**ain (HG), the next lower amplification as **M**id **G**ain (MG) and the lowest one as **L**ow **G**ain (LG). Design values for the covered ranges and the corresponding precisions are given in Table 4.4. The connection of VULCAN to the PMT and the VULCAN configuration are described in Section 6.3.1.

TABLE 4.4: Design values for the range and precision of the three VULCAN receiver tracks [48, p. 14].

receiver name	range	precision
HG	0 p.e. to 10 p.e.	0.1 p.e.
MG	0 p.e. to 100 p.e.	1 p.e.
LG	0 p.e. to 1000 p.e.	10 p.e.

Signal processing VULCAN is a highly integrated receiver chip which also implements data processing and is not a pure ADC. Therefore, the data from the three ADCs are internally transferred to a dedicated data processor. Transmitting the data from the three ADCs to an other chip like the FPGA would require a very high-throughput connection with a high number of parallel data-lines and/or with very high speeds. Since the simultaneous transmission of data from all three ADCs is not required, it has been decided to implement only the transmission of one ADC output at the same time [48, p. 46]. This is denoted as *data selection*.

Data selection The data selection algorithm is implemented in the data processor of VULCAN. It is designed to select and transmit data from the RX which provides the highest resolution. An exemplary visualization of the data selection process is given in Fig. 4.9.

The selection process works roughly in the following manner: Data are selected from the HG RX as long as they are below or equal to a configurable upward switching threshold. If the ADC data cross the threshold, data are selected from the MG RX. The same logic applies for the transition from the MG to LG RX, but with a dedicated threshold. In order to prevent fast switching between the different RX if the data are close to the switching threshold, a hysteresis is implemented. When data are readout from the MG (LG), data in the HG (MG) have to fall below another configurable downward switching threshold to be selected. A detailed explanation of the algorithm is given in [48, p. 48ff.].

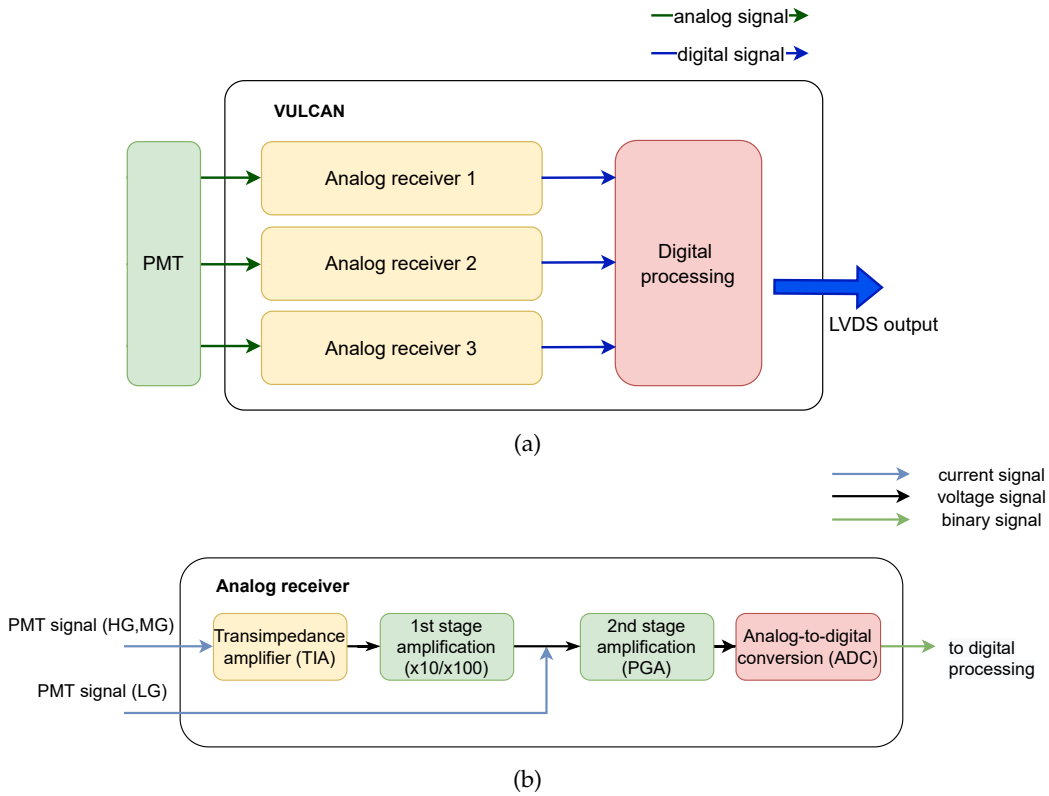


FIGURE 4.8: (a) Overview of VULCAN building blocks. (b) Scheme of one VULCAN receiver block.

The assignment of the physical receiver chain to its function as HG, MG or LG can be configured. Furthermore, it is possible to prevent switching to other receiver chains by setting a switching threshold of 255. The combination of those configuration options allows also the readout of a single RX, which is especially helpful for debugging purposes and for understanding the system response.

VULCAN can be configured to use the three trigger lines for decoding the source RX from which data were selected in terms of HG, MG and LG (i.e. not the RX number is decoded but the gain). The 16 data lines transmit two 8 bit samples from the same ADC. Thus, the data selection selects the ADC as source which provides the highest resolution for both samples. If a switching between ADCs would fall in between those samples, data would be selected from the ADC with the lower resolution.

Further data reduction mechanism are implemented in VULCAN, including the intermediate storage of data within a circular buffer and the suppression of noise ([49], [48, Chapter 5]). These modes are not used in this thesis. Selected data are transmitted via LVDS lines to the FPGA without further processing.

Time resolution The IC is originally designed for sampling rates up to $1\,\mathrm{GS\,s^{-1}}$ [50], which is based on the JUNO design requirements [18, p. 197ff.]. For the iPMTs, VULCAN is configured with a sampling rate of 500 Msps, since the chip is not validated for the full sampling rate.

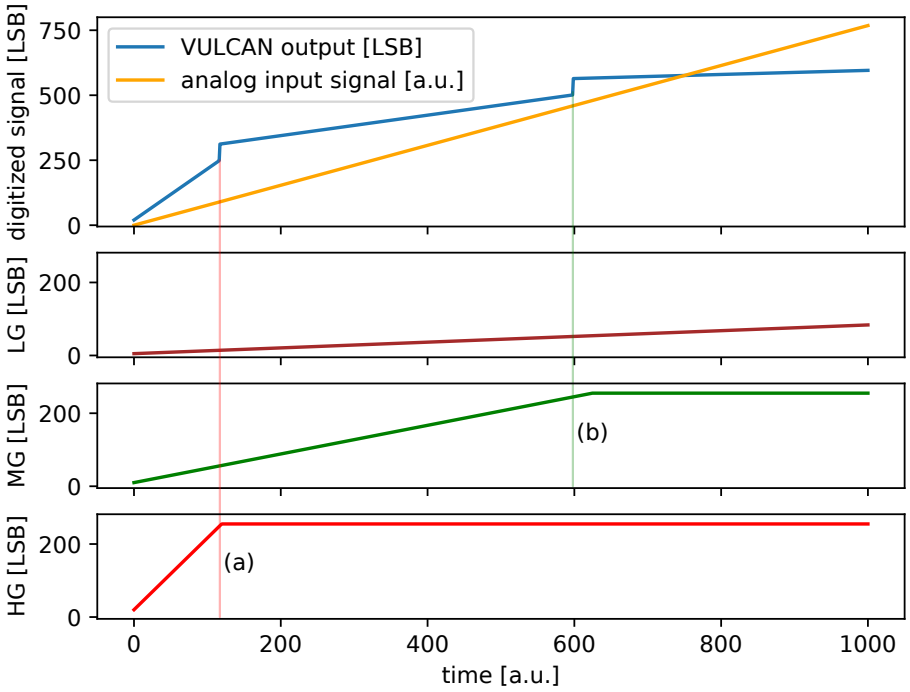


FIGURE 4.9: Visualization of the data selection within VULCAN for a HG to MG gain ratio of 5 and a MG to LG gain ratio of 5. Each receiver has an individual baseline level which are set here to 20 for the HG, to 10 for the MG and to 5 for the LG. The upper plot depicts the output of the data selector with the most significant bits decoding the source receiver (0 LSB to 255 LSB: HG, 256 LSB to 511 LSB: MG, 512 LSB to 767 LSB: LG). Data are selected from the HG receiver as long as the HG upward switching threshold (250 LSB) is not crossed. Switching to the MG receiver is done at *(a)*. Subsequently data are selected from the MG RX until the MG upward switching threshold of 245 LSB is crossed at *(b)*.

Bandwidth The input bandwidth for VULCAN is determined by the requirements from PMT signals. VULCAN is designed for a bandwidth up to 500 MHz, to provide a fast rise time of pulses and accurate pulse shaping [51, p. 10f.].

Input impedance The transimpedance amplifier determines VULCAN's input impedance. It has a design value for the combined input impedance of about $10\,\Omega \parallel 10\,\Omega = 5\,\Omega$ (cf. Section 6.3.1).

Phase-locked loop (PLL) An analog phase-locked loop frequency synthesizer has been designed for VULCAN with a focus on low noise, low jitter and high reliability [51, 52, 53, 54]. It provides the internal clocks for the ADC and the digital part of VULCAN as well as the LVDS output clock. The control voltage of the PLL is connected to an XADC input of the ZYNQ. This is useful for debugging purposes and checking the configuration of the PLL. The control voltage output is disabled per default to avoid effects on the PLL and has to be enabled via the configuration.

4.4.5 HV and Base

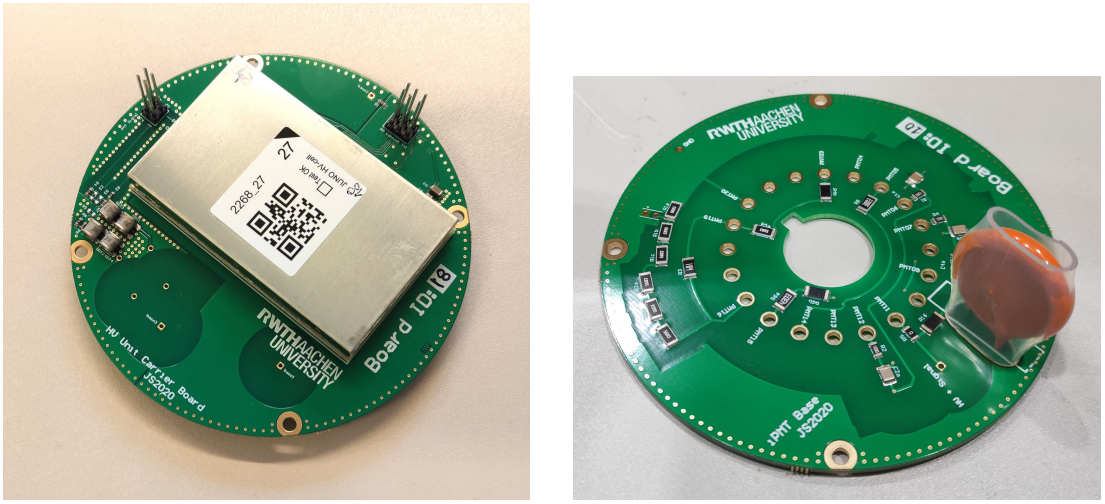
Electronics for providing the correct voltages for the PMT operation are spread over the HV Board and the Base. The HV Board hosts the HV module (cf. Fig. 4.10a) and passes thePMT signal through to the RoB.

HV module The HV module is a dedicated module for generating an output voltage up to 3000 V from an input voltage of 24 V. A microcontroller is integrated into the module for monitoring and control of the high voltage. Communication to the HV module is done via a EIA-485 interface connected to the SCCU. Key parameters of the module are given in Table 4.5. The module has been developed by members of the JUNO collaboration under the leadership of JINR Dubna, Russia.

TABLE 4.5: Parameters of the HV module [39].

parameter	value
input voltage	24 V
output voltage range	800 V to 3000 V
maximum output current	300 µA
output ripple	∼10 mV

Furthermore, a high voltage capacitor with a capacitance of 10 nF is used to eliminate the high voltage **D**irect **C**urrent (DC) component for subsequent circuits (this capacitor is called *coupling capacitor* in the following). It is required since the photo cathode is on ground potential, which results in a positive high voltage for the anode. This scheme is typically used to have a single cable for the high voltage and PMT signal transmission [38, p. 18], [18, p. 59]. An alternative scheme would be the use of negative high voltage for the cathode (also called anode grounding scheme). This would have the disadvantage, that when grounded material like magnetic shieldings are in close contact to the photo cathode, electrons would be attracted to this ground potential, leading to an increase in noise [41, p. 87].



(a) (b)

FIGURE 4.10: (a) High voltage carrier board. The HV module is covered with an alumina casing. (b) Voltage divider circuit for the PMT.

Base The Base Board is supplied with the positive high voltage from the HV module on the HV board. A voltage divider-circuit is implemented, based on the recommendation from *Hamamatsu*. Fig. 4.10b depicts the final version of the base.

4.5 Surface Board electronics

As described in Section 4.6 the **S**urface **B**oard (SB) is required within OSIRIS for timing and synchronization purposes. The name derives from the fact that they are located on top of the OSIRIS steel tank, opposed to the iPMTs located inside the tank.

The SB acts as a backplane for up to nine modules. One module slot is dedicated for the so-called **T**rigger **B**oard (TB). The other eight slots can be filled with **S**urface **C**onnector **B**oard (SCB). Fig. 4.11 depicts a SB with a plugged **T**rigger **B**oard (TB) and a SCB.

Surface Board Backplane The central element of the SB is a SoC module from *Trenz Electronic* (type TE0720-03-1CF). It features a Xilinx XC7Z020 SoC as it is used for the RoB (cf. Section 4.4.4), 1 GB DDR3-**R**andom **A**ccess **M**emory (RAM), a 1 Gbit Ethernet connection and a 32 MB flash memory. The FPGA of the SoC connects to the slots for the Trigger Board and SCBs. A 125 MHz crystal oscillator (*Silicon Labs Si530*) is available as reference clock source (same type as on the RoB).

Trigger Board The Trigger Board is used as interface to the calibration systems and for the clock and sync data stream distribution between SBs. It provides the following connections:

- 1 x High-speed differential clock input
- 4 x High-speed differential clock output
- 1 x High-speed differential data input (for sync data stream)

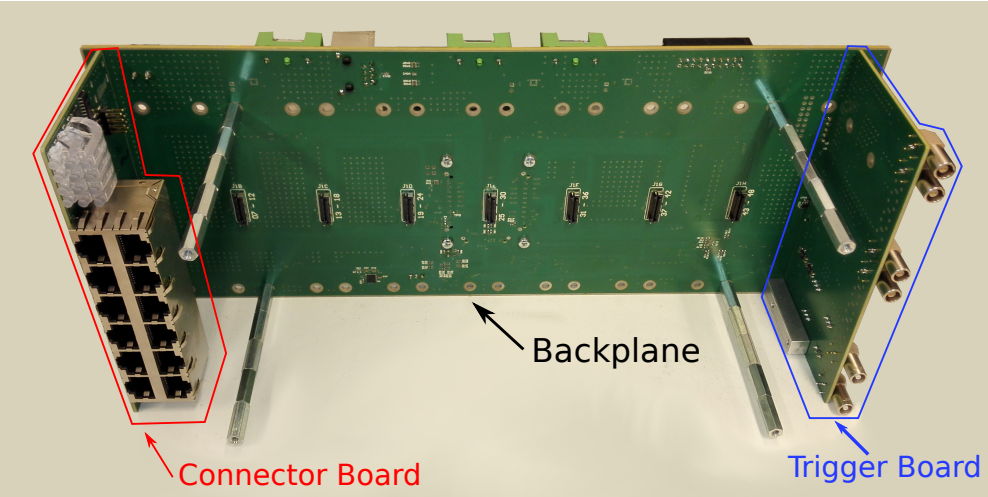


FIGURE 4.11: Image of a Surface Board backplane with a single SCB and a TB. The TB has not all connectors placed which are required for final operation (only one clock output and one data output are populated).

- 4 x High-speed differential data output (for sync data stream)
- 2 x 2 single ended trigger outputs

The clock outputs are used to distribute a clock signal from one SB to other SBs. The outputs provide all the same signal by utilizing a dedicated clock buffer, which creates copies of the clock signal with a well controlled jitter. The same applies for the differential data outputs for the sync data stream.

The trigger outputs are arranged in two pairs. Each pair receives a dedicated signal from the FPGA and a dedicated buffer is used to create copies of the signal for the two outputs of this pair. It is possible to configure each output either with 3.3 V or 5 V level.

Surface Connector Board Each SCB provides connections for up to six iPMTs. Two RJ45 connectors per iPMT are used. One socket directly connects to the iPMT. It provides the synchronous connections via the SCB (SYNC RX and SYNC TX, cf. Table 4.3) and the asynchronous connection which is passed through from the second RJ45 connector (ETH RX and ETH TX). This second socket is connected with a PoE switch to provide power and a network connection to the iPMT.

4.6 Timing system within OSIRIS

This section describes several aspects of the iPMT concept which are relevant for its use within OSIRIS as detector system. A description of the requirements is followed by an explanation how it is implemented.

Timing system In order to synchronize the data from the iPMTs and the calibration systems within OSIRIS, a timing system is required. This system is based on timestamps which are used to tag the information from the iPMTs and the calibration systems. A timestamp is a 64 bit integer number providing nanosecond resolution.

The upper 32 bit are used to store a UNIX-timestamp. The lower 32 bit state the nanoseconds within the second.

The information which need to be tagged with a timestamp are:

1. the trigger for the LED and Laser calibration system.
2. waveform data from the iPMTs

A major part of the timing system is implemented in the SB. Fig. 4.12 shows an overview of the system with the SBs as central component. The SB implements a master clock, which is based on a 125 MHz oscillator. The trigger signals for the calibration system are generated within the SB and directly tagged with a timestamp. This information is sent to the EB for further processing (event building).

For the iPMTs, a copy of the master clock is sent to each iPMT. This procedure ensures, that all iPMTs run on the same frequency as the master clock. This clock signal is embedded in a data stream which implements a specific protocol (sync data stream, cf. Section 5.4.2). Part of this protocol is also the transmission of a timestamp once per second (therefore called **P**ulse **P**er **S**econd (PPS)) which is used as synchronization signal. Due to differences in the cable length and signal routing, the synchronization signal may arrive at different times at the iPMTs. These differences have to be calibrated for a precise timing. Applying the calibration values for the iPMTs is implemented in the EB.

The implementation of the system requires that the signal travel times to the respective system are constant and that random fluctuation (jitter) are controlled. For the LED and Laser calibration system this is not covered in this thesis. An evaluation of the timing and synchronization of the iPMTs is given in Section 6.7.1.

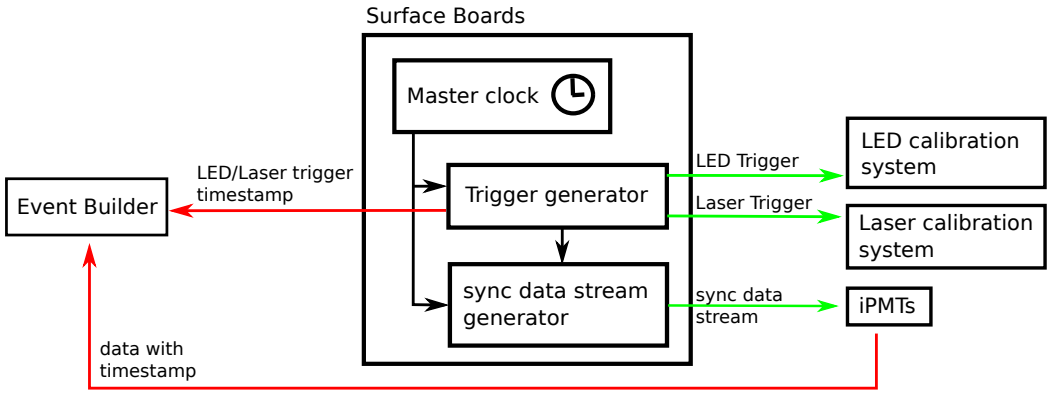


FIGURE 4.12: Overview of the timing scheme within OSIRIS. A master clock is generated on one Surface Board. Trigger information for the LED and Laser calibration system (cf. Section 3.3.4) are generated and sent to the EB (cf. Section 3.3.3). A copy of the clock signal is embedded in the sync data stream and sent to the iPMTs together with a PPS signal.

Opposed to other experiments like JUNO, the timing system for OSIRIS does not provide a sub-nanosecond accuracy. For example, in JUNO the accurate timing is required for the event correlation between the central detector and veto detectors and for the comparison with other experiments [18, p. 204]. These requirements do not apply to OSIRIS, therefore the timing system is not optimized for a high accuracy.

4.6.1 Connecting multiple Surface Boards for OSIRIS

With each SB hosting up to eight SCBs, it is possible to connect up to 48 iPMTs per SB. Thus, at least two SBs are required for the 75 iPMTs in OSIRIS. The boards are equally populated, but one of them is required to work as master clock source as it is needed by the timing system. This is achieved by connecting the boards as depicted in Fig. 4.13. It allows to have the boards equally equipped and running with the same FPGA configuration and software. Only the cable connections determine which of them acts as master clock source.

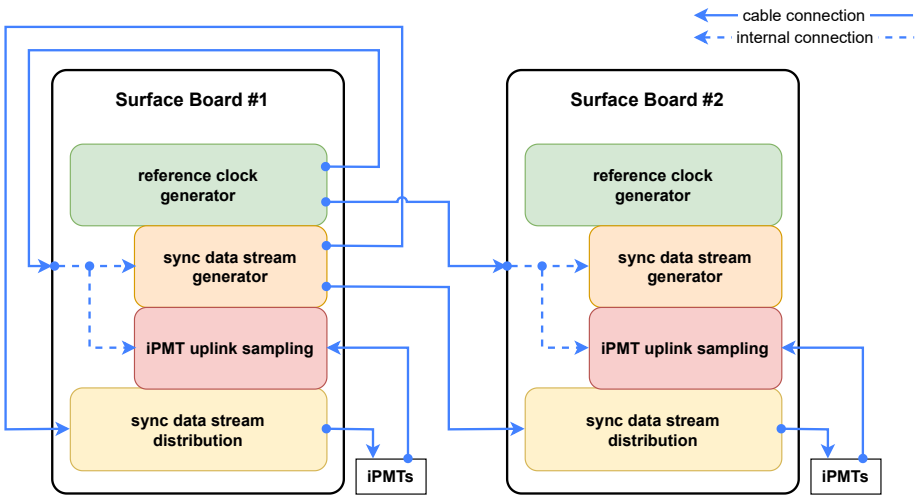


FIGURE 4.13: Scheme of connecting two SBs for the use within OSIRIS with Surface Board #1 as master clock source. The reference clock from Surface Board #1 is required on the Surface Board #2 to sample the data which are sent from the iPMTs to the SB (cf. Section 5.4.2).

Chapter 5

FPGA and software design

This chapter covers the implementation of FPGA designs for the iPMT system and closely related software. A short general introduction into FPGA designs is given in Section 5.1, followed by the details of the designs for the iPMTs in Section 5.2 and for the SBs in Section 5.4. A short explanation of the trigger system in OSIRIS and its integration with the iPMTs is given in Section 5.3. Sections 5.5 and 5.6 cover the software infrastructure of the iPMT system.

5.1 General design considerations

This section describes general properties and procedures for the FPGA designs. It applies to both, the iPMT and SB FPGA design.

The creation of an FPGA design is a multi-step procedure which relies heavily on the toolchain given by the FPGA vendor. Since the iPMT system is based on FPGAs from Xilinx, the used toolchain is the *Xilinx Vivado Design Suite* in version 2018.3. Appendix D.1 gives a more detailed overview over the design flow.

FPGA elements An FPGA is an IC with a set of building blocks whose connections can be configured. Basic elements are e.g., logic function blocks and storage elements like flip-flops. Certain elements may be specific to certain families of FPGAs or vendors. Some element names are given explicitly in the following text, details and further references for them are given in Appendix D.2.

Debugging Xilinx provides **I**ntellectual **P**roperty Cores (IP-Cores) which are designed for testing and debugging purposes. Namely these are the System integrated logic analyzer (System ILA, [76]) and virtual input/output (VIO, [77]). The System ILA core can be used to monitor the internal signals and interfaces. The signals are recorded as waveforms within the FPGA and can be readout via the JTAG interface.

The VIO core is used to read and drive signals within the FPGA. These are typically slowly changing, low-bandwidth signals which would be implemented in hardware as LED (for outputs) or as switches (for inputs) [77].

5.1.1 Clock domains

FPGAs use clock signals to synchronize signal transfer between FPGA elements. Elements are part of a clock domain if they are driven by the same clock signal. It can become necessary to have multiple clock domains due to design decisions and other constraints.

Clock domain crossing When data need to be passed between clock domains, this is know an *clock domain crossing*. Special techniques have to be used to ensure the correct data transfer. A suitable technique depends among other on the frequency relation between the clocks, the number of bits and the interpretation of the data [55]. The FPGA designs presented in this thesis use so-called *Xilinx Parameterized Macros* [78] which implement synchronization circuits for clock domain crossing.

5.2 iPMT FPGA design

The design is targeted for a Xilinx XC7Z020 SoC, which is described as part of the RoB in Section 4.4.4.

5.2.1 Structural overview

The functionality of the iPMTs which requires precise timing, for example, the synchronization, is implemented in the PL part of the SoC. Other design aspects as handling configuration parameters and the transfer of recorded waveform data to the EB which do not require a real-time handling are implemented in the PS. Fig. 5.1 visualizes the different components of the iPMT which are connected to the SoC.

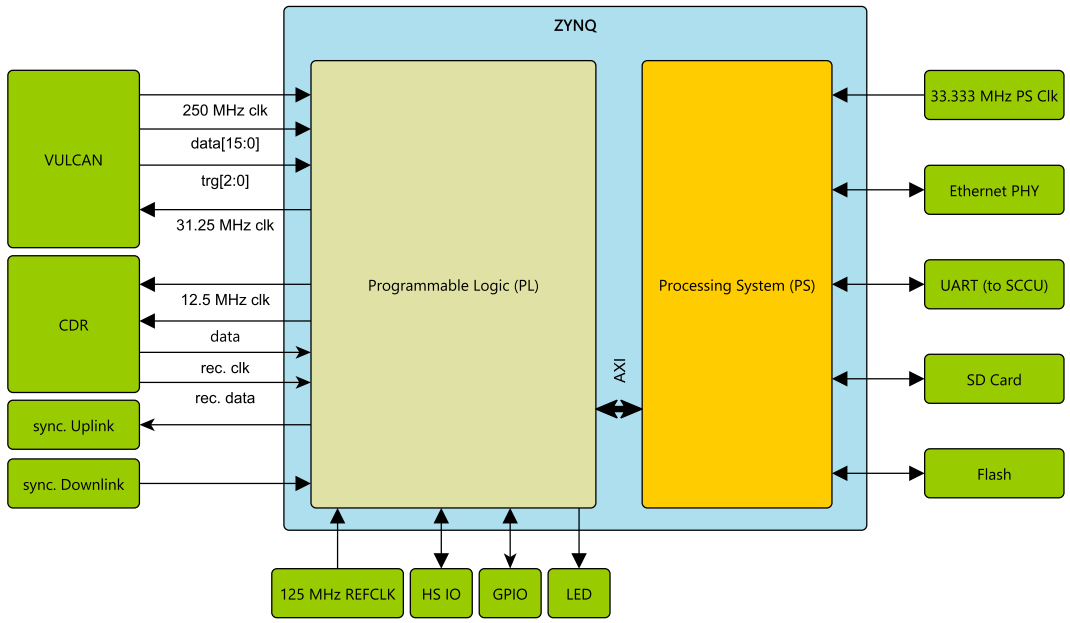


FIGURE 5.1: Block diagram of the ZYNQ on the RoB and connected ICs. HS IO denotes **h**igh **s**peed **i**nput/**o**utputs, which can be used for debugging purposes. GPIO are **g**eneral **p**urpose input/outputs also available for debugging and testing. LEDs are onboard light emitting diodes which can optionally be connected as status indicator.

The communication between the PL and the PS is mostly based on the AMBA Advanced extensible interface (AXI). AXI is a family of communication buses by ARM which has been extended by Xilinx for the use within their devices [79].

5.2.2 Clocking structure

The distribution of clock signals is a central design task. A scheme of the most important clocking parts is displayed in Fig. 5.2. The clocking scheme of the iPMT has to cope with two basic situations which affect the clocking scheme:

1. with a valid recovered clock
2. without a valid recovered clock

The setup with a valid recovered clock is the expected normal operation within OSIRIS. In that case, the sync data stream is transmitted to the CDR for recovering the clock and data stream. The recovered clock signal has a frequency of 125 MHz. Subsequently it is passed via several clocking elements and divided by four, resulting in the target reference clock for VULCAN of 31.25 MHz.

For the case that the CDR is not able to recover a clock signal, the reference clock for VULCAN is derived from the onboard 125 MHz crystal oscillator. This situation can occur when the iPMT is used for testing without being connected to a SB.

The processing of the data which are digitized by VULCAN is always clocked by the clock provided by VULCAN itself. Clock division from 250 MHz to 125 MHz is done by a clock synthesizer primitive (MMCM, cf. Appendix D.2).

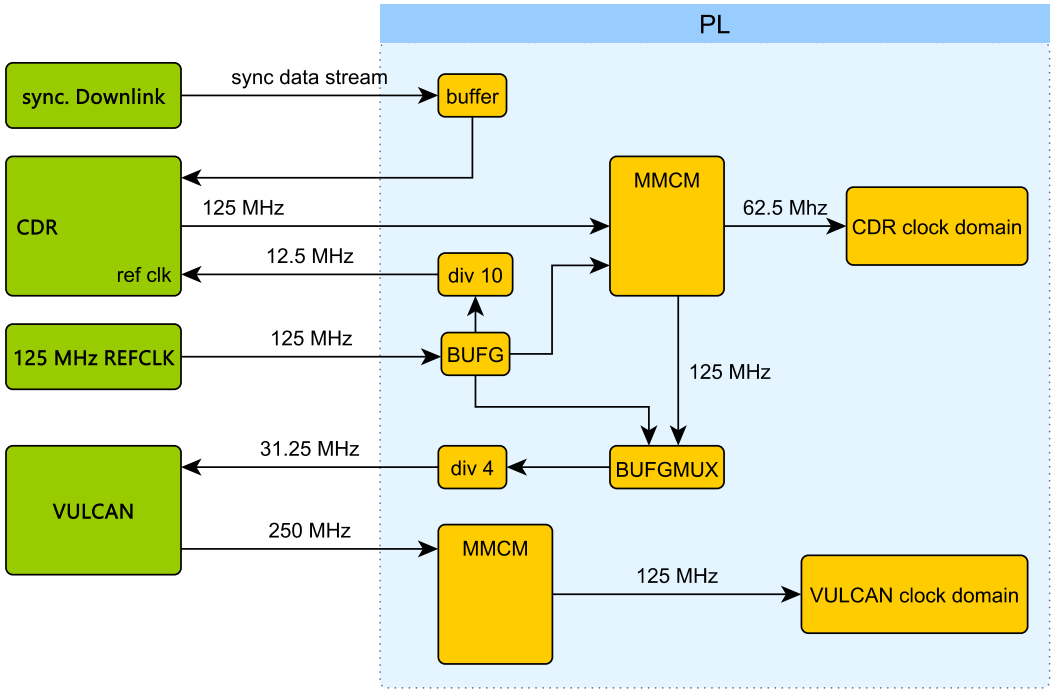


FIGURE 5.2: Overview of the clock distribution. Explanations for FPGA elements are given in Appendix D.2.

5.2.3 Blockdesign

Fig. 5.3 shows a schematic overview of the design with functional blocks, described in following paragraphs. The overall structure of the description is based on the structure

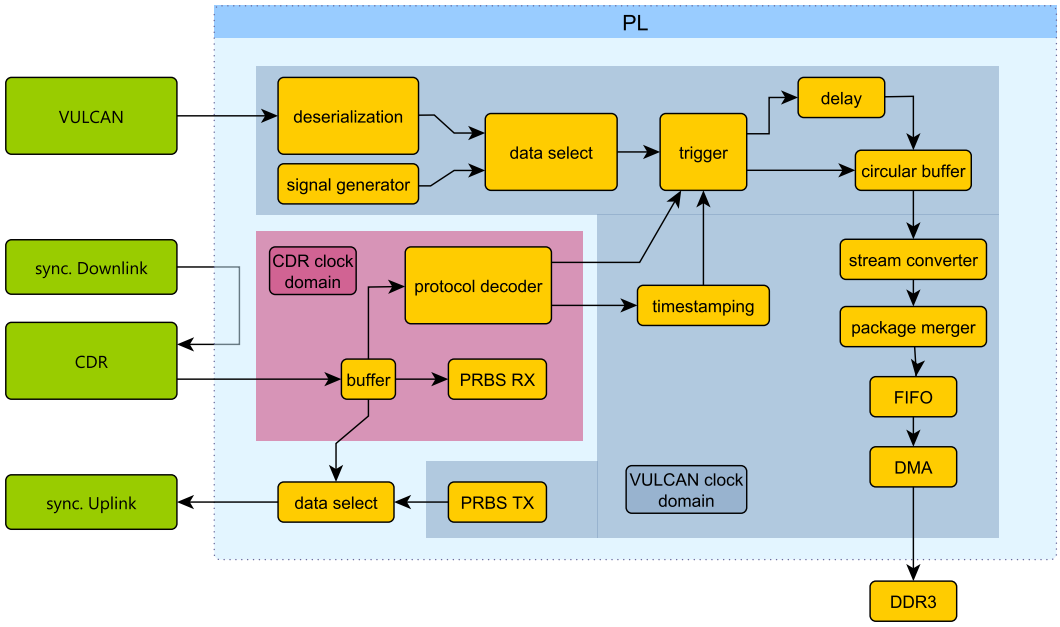


FIGURE 5.3: Schematic overview of design modules. For sake of clarity not all connections are drawn. The "PRBS TX" module uses a 62.5 MHz clock which is derived from the VULCAN clock. The "data select" block uses data from different clock domains and is therefore not assigned to one clock domain.

of the data readout (i.e. following the arrows starting at VULCAN in Fig. 5.3). Thus, the description starts with the data reception in Section 5.2.4, followed by a description of the trigger in Section 5.2.6 and details of the data processing in Section 5.2.7.

Sections 5.2.8 and 5.2.9 describes the modules which are part of the CDR clock domain.

5.2.4 VULCAN data interface

VULCAN has in total 20 LVDS outputs which are connected to the FPGA. One of those lines is the clock signal, 16 lines are data lines and the remaining three lines are denoted as trigger lines. Providing a clock along with the data is a design approach which is called *source-synchronous*. It simplifies the timing parameter for the design [56].

Deserialization The VULCAN data stream is clocked with a frequency of 250 MHz. This frequency is relatively high and data processing at this frequency would make the timing more complicated than at lower clock frequencies. Therefore, the data and clock frequency are lowered to 125 MHz. Dedicated elements in the input section of the FPGA (ISERDESE2, cf. Appendix D.2) are used to deserialize the data stream by two. Thus, the following data processing chain is designed for the processing of four 10 bit samples (8 bit ADC data and 2 bit for decoding the source RX, i.e. HG, MG or LG) in parallel.

Signal generator For testing purposes a digital signal generator is implemented, providing a configurable triangular shaped signal.

5.2.5 Readout window

A readout window is a contiguous block of 10 bit samples recorded from VULCAN. The maximum size of one readout window is fixed in the design to 120 samples, corresponding to 240 ns. A trigger signal is implemented to issue the storage of a single readout window. In order to achieve effective longer readout windows, it is possible concatenate multiple shorter readout windows by issuing additional triggers with a time difference $\Delta T \leq 240\,\text{ns}$. If the trigger signals have a $\Delta T < 240\,\text{ns}$, all readout windows except for the first one, have a size of ΔT.

5.2.6 Trigger

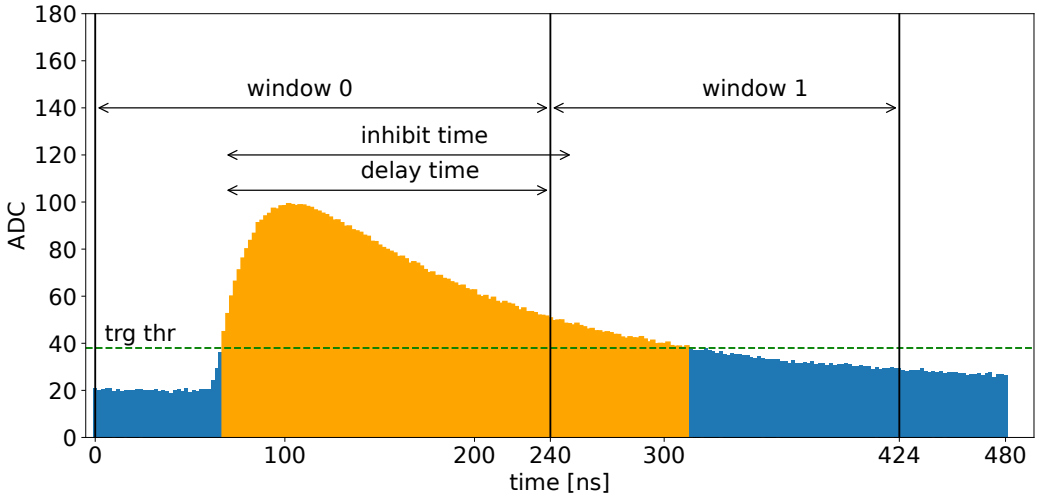


FIGURE 5.4: Visualization of the trigger procedure with an active threshold trigger and a follow-up trigger. The first window is triggered due to the samples over the threshold. The position of the window relative to the trigger can be adjusted with the delay. The second window is triggered as follow-up because the trigger condition was fulfilled contiguously. The second window has the length of the inhibit time (184 ns).

The trigger module generates trigger signals for subsequent modules in the design. Based on several trigger sources, the internal state and the configuration, the trigger decision is implemented. The following trigger sources are available:

Threshold trigger The ADC data stream is compared with a configurable threshold. The trigger condition is met if a sample is equal or greater to the configured threshold value. Additionally, it can be required that up to four consecutive samples are above the threshold value.

Follow-up trigger A follow-up trigger is issued when the trigger condition has been fulfilled contiguously until the trigger inhibit time is reached (see below for a description of the trigger inhibit). Thus, this trigger increases the effective readout window length and is intended to record longer pulses, e.g., originating from a muon. A visualization of a recorded waveform with a follow-up trigger is given in Fig. 5.4.

Software trigger Via the PL-PS interface a signal can be sent from the PS to the trigger module to issue a single trigger. This is useful for recording random readout windows, e.g., for determining the baseline.

External trigger The external trigger is connected to a high-speed input pin on the RoB (HS IO). Thus, it is only usable during development when the external pins are still accessible.

New-timestamp trigger A timestamp is sent on regular basis from the Surface Board to the iPMT (normal interval: 1 s, cf. Section 5.2.8). This trigger is issued on every reception of a timestamp.

Synchronous link trigger As described in Section 5.4.2, the synchronous link protocol supports sending up to four different trigger signals which can be enabled individually as trigger source. Two of them directly correspond to the LED/Laser trigger signals.

Automatic follow-up In order to generate multiple consecutive readout windows initiated by an other trigger source (threshold, external, new-timestamp or synchronous link trigger), the automatic follow-up trigger can be used. A configurable number of triggers with intervals of 240 ns are issued when the condition of the initiating trigger source is fulfilled. During an active automatic follow-up trigger (i.e. until the configured number of trigger has been issued) other trigger sources are ignored. This trigger mode is especially useful for debugging and testing purposes when an effective longer readout window is required.

Trigger mode in OSIRIS

The default trigger mode for OSIRIS is the threshold trigger in combination with a follow-up trigger. The delay and inhibit times have to be adjusted according to the requirements of the waveform reconstruction. During commissioning of OSIRIS and for debugging purposes, other trigger modes might be helpful as well.

Trigger inhibit

In order to prevent too short readout windows, it is possible to inhibit the generation of new triggers for a configurable number of clock cycles after a previous trigger. The trigger inhibit is overridden by the automatic follow-up trigger.

Timestamp and trigger bit assignment

A timestamp is saved when a trigger signal is issued. This timestamp has a resolution of 2 ns if the threshold trigger is used (corresponding to the VULCAN sampling speed), for other trigger sources it has a resolution of 8 ns. Additionally, for all trigger sources, except for the automatic follow-up, a trigger bit is saved along with each individual ADC sample to indicate when the trigger condition was met. For the threshold trigger the trigger bits are assigned for each sample individually, for other trigger sources, the four samples which are processed in parallel are assigned with the same trigger bit value.

5.2.7 Data processing

Delay The trigger signal and corresponding information as the trigger source and timestamp can be delayed to shift the readout window. The delay is configurable in a range from 0 to 127 clock cycles, corresponding to 0 ns to 1016 ns. As the trigger signal corresponds to a stop signal for the following readout structures, a delay setting of 0 ns corresponds to a readout window containing only data before the trigger.

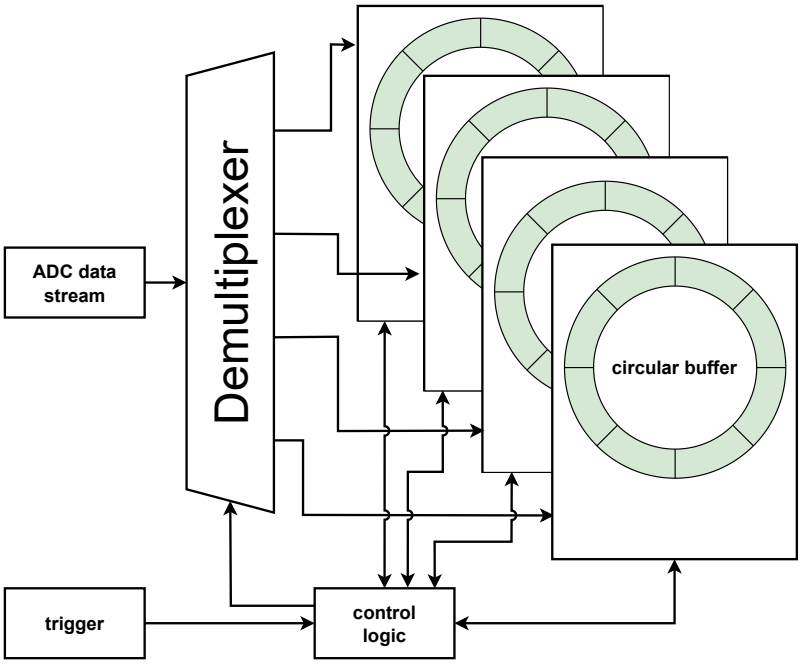


FIGURE 5.5: Schematic overview of the circular buffer module. Only 4 of 8 circular buffers are drawn for the sake of clarity.

Circular buffer The ADC readout is based on the concept of circular buffers (also known as ring buffers). The data stream from the ADC is written continuously to a set of storage elements in such a way, that writing is continued at the beginning if the end has been reached (wrap-around). If the writing to one buffer is stopped by a trigger signal, the next buffer is selected for writing. A schematic overview is shown in Fig. 5.5. Within the design, 8 circular buffers with a size of 120 samples each are instantiated. The size of the individual buffer determines the aforementioned maximum readout window length of 240 ns.

Stream converter Stopped circular buffers are converted into a data stream in the *AMBA* AXI4-Stream Protocol [80]. Subsequently, Xilinx IP-Cores with a AXI4-Stream interface can be used in later stages. The data from one circular buffer and the corresponding meta-information (such as the timestamp and the trigger source) are called *package*. The format of the package corresponds to the format which is used for the transmission to the EB and is described in Appendix B as "Waveform subevent". Each package has the size of 192 Bytes.

Package merger Multiple packages are concatenated in order to reduce the transfer overhead from PL to PS. The number of merged packages is configurable during run-time.

FIFO For package buffering and mitigation of transfer delays, a Xilinx AXI4-Stream Data FIFO is used. FIFO is the abbreviation for **F**irst **i**n **F**irst **o**ut, describing the working principle, that elements which are stored first, are also released first (like in a normal waiting queue). With a size of about 1 Mbit it can store approximately 680 packages.

Data transfer to PL (DMA) Data residing in the aforementioned FIFO are transferred via **D**irect **M**emory **A**ccess (DMA) to the RAM. The transfers are initiated by the software running in the PS (iPMTClient, cf. Section 5.5.2).

5.2.8 Clock and data recovery integration

As described in Section 4.4.4 a dedicated clock and data recovery IC is placed on the RoB. The recovery data rate is fixed to a range of 94 Mbit s^{-1} to 156 Mbit s^{-1}, which matches best to the used 125 Mbit s^{-1} (possible ranges are defined in [81]).

The CDR requires a very low jitter for the reference clock for reliable operation [81]. It has been found during the development, that clocks synthesized by an MMCM in the PL are not sufficient to guarantee a stable operation. This is one reason for having a dedicated crystal oscillator on each RoB (cf. Section 4.4.4) with a frequency of 125 MHz. To generate the required reference clock of 12.5 MHz for the CDR, the clock division is done by a simple clock divider instead of using an MMCM (part of the clock distribution scheme in Fig. 5.2).

CDR clock handling

The synchronous downlink signal (SYNC RX) is not directly connected with the CDR, but with the FPGA. From the FPGA the SYNC RX signal is then passed through to the CDR (cf. Fig. 5.2). A drawback of this solution is possible noise pickup from the FPGA, but it has the advantage of higher flexibility and allows for other algorithm handling the sync data stream in the future. One example implementation is the pure digital clock and data recovery approach presented in [57]. It is based on a numerically controlled oscillator and a digital phase detection, exploiting among others advanced phase shifting features of Xilinx' MMCM. In order to be able to implement the described technique as a backup or alternative for the CDR, a loop-back has been added to the design, as it is mentioned as precondition in [57, p. 1955].

5.2.9 Protocol decoder and timestamping

Protocol decoder The design contains a decoder for the sync data stream protocol[1] to decode the reception of triggers and the synchronization timestamp.

[1] cf. Section 4.6 for an overview of the timing system and Section 5.4.2 for the description of the protocol.

Timestamp generator

The generation of the timestamp is based on two counters. One counter counts with the frequency of the internal clock (125 MHz) to provide a nanosecond timestamp with a resolution of 8 ns. This counter is reset when the nominal number of 125×10^6 clock cycles is reached. The counter for seconds increments on every reset of the nanosecond counter.

The timestamping circuit provides two modes of operation, a *local* and a *remote* mode. For the *local* mode, the start timestamp of the seconds counter can be set via the PS system as a UNIX-timestamp (counting the seconds since January 1st 1970, 00:00 UTC). This procedure allows for setting the timestamp with an accuracy in the order of 1 s. If the *remote* mode is chosen, the next correctly transmitted timestamp from the protocol decoder is used as start timestamp and as start signal. Any following transmitted timestamp does not influence the timestamping.

5.2.10 Pseudo random bit sequence generator

In order to qualify digital transmissions, the measurement of the number of bit errors is an important quality criterion. For measuring this quantity, a known sequence of bits is transferred via a transmission line and evaluated at the receiving end. The measured number of bit errors is is divided by the total number of transmitted bits to calculate the **B**it **E**rror **R**ate (BER).

A standardized way of generating the random bit sequences is the use of a **P**seudo **R**andom **B**inary **S**equence (PRBS) generator [82]. Such a generator can be implemented by using shift registers with a fixed length with feedbacks (**L**inear-**f**eedback **S**hift **R**egister (LFSR)). This is easy and cheap to implement within an FPGA and therefore commonly used. For testing, PRBS7 is used, in which "7" refers to the maximum length of a unique bit sequence.

The sending part uses a LFSR to produce the bit sequence to be sent via the transmission line. The receiving part has to synchronize first by filling its LFSR. After successful synchronization, the measurement of the bit errors is possible by comparing the received bits to the output of the LFSR.
A description how PRBS streams are used for the verification of the synchronous connection of the iPMTs is given in Section 6.7.

5.2.11 Outlook

Possible extensions and improvements of the design depend on the available resources. The resource usage for the current design is listed in Table 5.1. It has to be considered that in real applications not all resources can be used. Achieving a valid design which respects all requirements, especially regarding the timing of signals (timing closure) is becoming more difficult or even impossible with too high resource utilization. The maximum usable resources depend on the use case, the FPGA family and other factors.

Table 5.1 reveals a high portion of resources blocked for debugging purpose. The debugging circuits are deliberately not removed from the design to allow debugging during the commissioning phase of OSIRIS and for upcoming developments.

Improvements of the design could include the implementation of more advanced signal processing. An example algorithm is a matched filter. Such a filter can be used to detect a signal within a noisy waveform, in case of white gaussian noise it is the

TABLE 5.1: Resource utilization of the iPMT FPGA design. Detailed explanation of the design elements are described in [78, p. 256ff.]. All design elements which are part of a System ILA (explained in Section 5.1) are classified as "used for debug".

Name	Available	Used	Used for debug	w/o debug	Used %	used % w/o debug
Slice LUTs	53200	27580	15033	12547	52%	24%
Slice Registers	106400	51479	27753	23726	48%	22%
F7 Muxes	26600	1991	526	1465	7%	6%
F8 Muxes	13300	658	50	608	5%	5%
Block RAM Tile	140	96	30	66	69%	47%
DSPs	220	0	0	0	0%	0%
MMCME2_ADV	4	2	0	2	50%	50%
BUFGCTRL	32	12	0	12	38%	38%

optimum filter [58]. Dedicated digital-signal-processing (DSP) blocks are especially useful for the implementation of such a filter in an FPGA.

Another method which may be implemented on the FPGA using DSPs are artificial neural networks. Relevant tasks could be the triggering or the extraction of features from triggered waveforms.

All 220 DSP blocks are available in the current design for such future developments.

5.3 Triggering with the Event Builder

As described in Section 5.2.6, each iPMT runs a trigger on its VULCAN data stream. From an OSIRIS point of view this is a "local" trigger, since it only takes into account a single PMT. Since the light signal from an event is spread over multiple PMTs, the information from all iPMTs needs to be taken into account for the event detection.

In case of an event, the amount of light which is seen by an individual PMT can be very low, i.e. on single photon level. Also dark counts of the PMTs are mostly on single p.e. level and the signal does not contain any information whether it is a signal induced by an impinging photon or noise (dark count). Since the actual event rate in OSIRIS is in the order of few Hz, the vast majority of waveforms which are triggered "locally" by an iPMT are dark counts.

All waveforms of all iPMTs are sent to a central unit, called EB. The structure of the EB and its connection to the iPMT system is shown in Fig. 5.6. The task of the EB is to decide which waveforms have to be stored for the later physics analysis. This process is also called trigger. Several trigger modes can be implemented in this purely software based system, including special triggers for calibration, debugging and performance measurements. The normal trigger mode for the detection of events in OSIRIS is the time correlation of events.

The EB software is developed and maintained by the OSIRIS group of the JUNO collaboration.

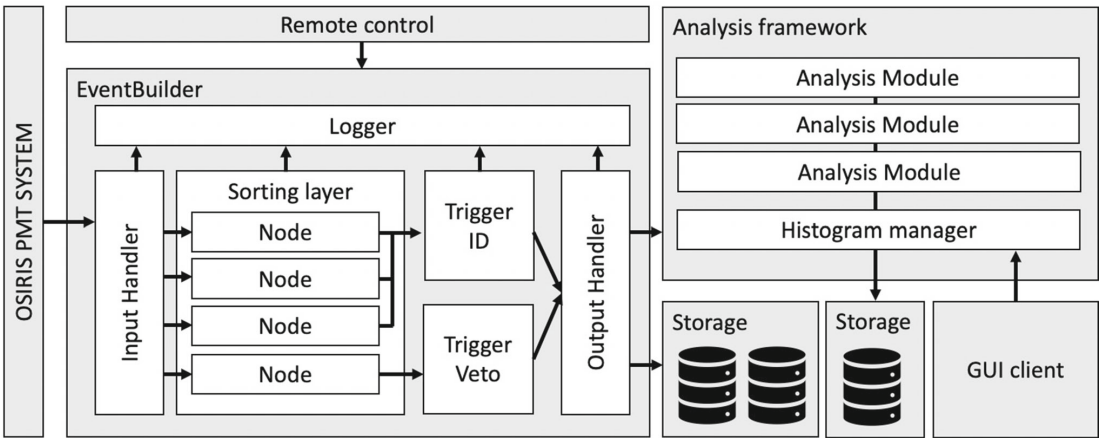


FIGURE 5.6: Scheme of the OSIRIS **D**ata **Acq**uisition (DAQ) software. The datastreams from the iPMTs and SB are denoted in this graphic as "OSIRIS PMT System" [33].

5.4 Surface Board FPGA design

The **S**urface **B**oard (SB) is the central unit for the synchronization of the iPMT system and the integration with the OSIRIS calibration systems as described in Section 4.5 and Section 4.6. Following tasks are implemented by the SBs:

- Providing a clock signal for all iPMTs
- Providing a synchronization method
- Providing trigger signals for the calibration systems

5.4.1 Clocking structure

Fig. 5.7 depicts an overview of the clocking structure and of the distribution of the sync data stream.

The FPGA uses one clock synthesizer (MMCM, cf. Appendix D.2) to provide different clock frequencies for the design. The default input clock for the MMCM is provided via the "Clk input" on the TB. This input is connected to the "Clk fanout" from the master SB. The master SB provides the master clock, i.e. the 125 MHz reference clock. For the master SB, a cable connects the "Clk fanout" with the "Clk input" port on the same TB, denoted therefore as "loop cable".

The sync data stream is generated on both SBs, but only one of the streams is distributed via the sync data stream fanout on the TB to both SBs. The sync data stream is then passed through the FPGA and distributed to the SCBs which send the stream to the iPMTs. Thus, the cable connection determines which SB acts as source for the sync data stream, similar as it is done for the clock signal.

The motivation for this distribution structure is that both SBs can use the same firmware with the same configuration.

5.4.2 Blockdesign

Fig. 5.8 shows a structural overview of the design. The individual modules are described in the following sections.

Timestamping

The SB reuses the timestamping module of the iPMT which is described in Section 5.2.9. It provides only the option to set the start timestamp via the PS, the "remote" mode is not available.

Laser/LED trigger generator

The SB provides trigger signals for the LED and Laser calibration system in OSIRIS (cf. Section 4.6). The generation of the trigger signals is based on individual counters for each of the systems. When reaching its maximum count value, the counter is reset and a trigger signal is issued. The maximum count value is individually configurable for the LED and Laser system in a range which corresponds to trigger rates between < 1 Hz up to several 100 kHz. Expected trigger rates for the calibration systems in the order of few kHz are thereby covered. An internal inhibit signal prevents the

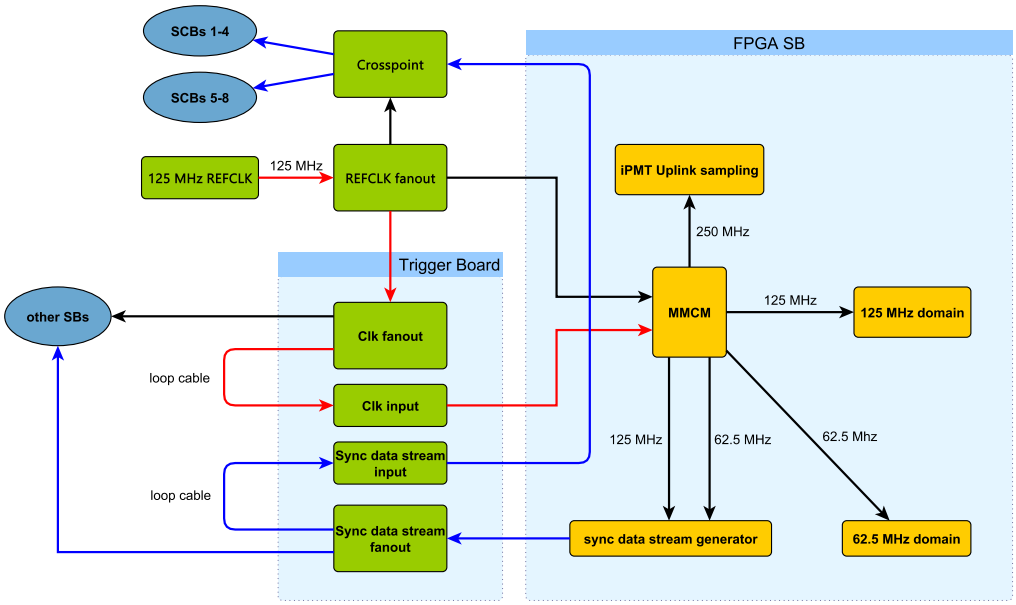


FIGURE 5.7: Structure of clock and sync data stream distribution on the SB. Black and red lines are clock signals. The red lines indicate the default clocking scheme for the master SB. Slave SBs would receive the clk signal and the sync data stream not via a loop cable but from the master SB. Blue lines are sync data stream signals. Fanouts are used for creating copies of signals. A crosspoint is used to assign outputs to an individually selected input.

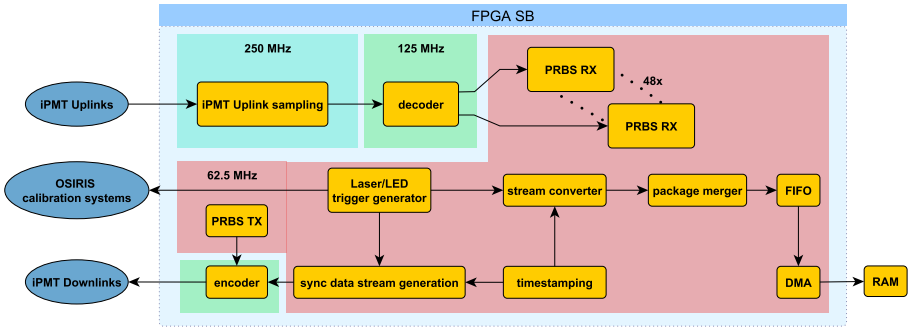


FIGURE 5.8: Blockdiagram of the SB FPGA design. The 62.5 MHz, 125 MHz and 250 MHz clock domains are highlighted in different colors. Those clocks are generated phase aligned from one central clock synthesizer (cf. Fig. 5.7).

generation of a trigger during an active transmission of the sync data stream (see Section 5.4.2) in order to avoid collisions.

The timestamps of the trigger signals are transferred to the PL in the same structure as it is done for the waveform packages in the iPMT FPGA design. A dedicated stream converter for the Laser/LED trigger timestamps has been implemented to create "LED/Laser trigger subevents" in the format as described in Appendix B. The description of the transfer structure is given in Section 5.2.7, starting with the paragraph package merger. For the SB design, the FIFO has a size of 66 kbit, which is significantly lower than in the iPMT design due to the reduced package size and lower expected package rates. With a package size of 256 bit, up to 264 packages can be stored in this FIFO.

Sync data stream generator

As explained in Section 4.6, the sync data stream is sent to the iPMTs primarily to provide a clock and transmit a UNIX-timestamp. For debugging and testing purposes also the transmission of trigger signals is implemented.

The hardware used at the receiving end (i.e. on the iPMT) puts restrictions on the transmitted signal. The iPMT uses the *Texas Instruments DS15EA101*, which is an adaptive cable equalizer [83]. This chip is used to counteract frequency-dependent cable losses of the signal during transmission. Due to the adaptiveness of the cable equalizer it might pickup noise if signals are sent only with large time intervals, thus leading to wrong signals.

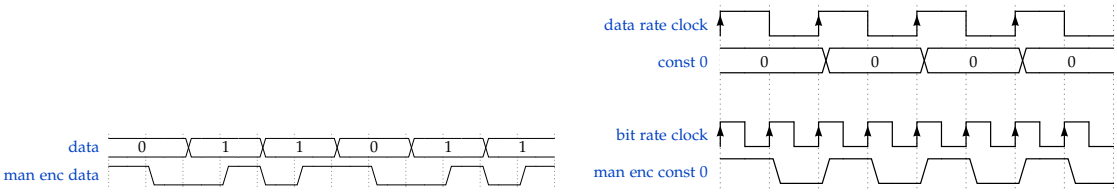
A similar restriction is raised by the CDR IC. It requires a minimum amount of transitions, as it loses its ability to recover a stable clock otherwise (more detailed description in Appendix C).

A code which provides a high number of transitions, also if constant data are sent, is the manchester code.

Manchester code The manchester code uses two bits to encode one bit (abbreviated as 1b2b). This has the effect of a rather low efficiency of 50 %, respectively an overhead of 100 %. Since the actual amount of data which needs to be transmitted is rather low, this is not a relevant drawback. The advantage of the manchester code is that it is easy to implement and use. Furthermore, the transmitted signal is free of a direct-current component, which allows AC coupling [59, p. 143]. For this purpose, coupling capacitors are used for the synchronous connections between the SB and the iPMTs. If the requirements for this link should change in future developments, the en-/decoding can be easily adapted in the firmwares.

The bit rate, here the number of transmitted 1s and 0s, of the link is 125 Mbit. The symbol rate, i.e. the rate with which the information are transmitted, is due to the manchester encoding, 50 % of the bit rate, thus 62.5 Mbit. A visualization of the code is given in Fig. 5.9.

Trigger transmission The trigger signals which are issued for the LED/Laser system (cf. Section 5.4.2) are also transferred to the iPMTs. In total, four different trigger sources can be implemented to be transmitted. In the current status are these the two different trigger for the LED/Laser and a delayed version of them.



(a) Manchester encoding of a data stream.

(b) Constant input data (here a constant zero) create a clock like signal with a frequency of the data rate. The actual bit rate clock has twice the frequency.

FIGURE 5.9: Examples for manchester encoding with a code definition as used for Ethernet [84]. A zero is expressed as a high signal followed by a low signal. A one is expressed as low signal followed by a high signal.

Timestamp transmission Every time the seconds counter of the timestamp (cf. Section 5.2.9) increments, the updated seconds timestamp is also transmitted to the iPMTs. The transmission of the timestamp has precedence over the transmission over the trigger signals. If both signals are issued at the same clock cycle, the timestamp has the higher priority and is transmitted. An ongoing transmission of a LED/Laser trigger would not be interrupted. For this rather rare case, the timestamp might not be transmitted. Since the timestamp is only required once for setting the start timestamp for the iPMT internal counter, this would only delay this setup of the start timestamp by one second. The second purpose of the timestamp, i.e. to possibly crosscheck the timestamps, is also just mildly affected, since the cross check would also be delayed by one second.

Sync data stream protocol The protocol is implemented by using a **F**inite-**S**tate **M**achine (FSM) for the generation and reception of the data stream (protocol de-/encoder). The protocol consists of a header, a data payload and a trailer. The header for the transmission of a timestamp is b0001[2]. Whereas the header for the transmission of a trigger starts with bXX11, with XX being in the range from b00 to b11, depending on the source of the trigger (e.g., Laser or LED). The data payload is the 32 bit timestamp in case of the timestamp transmission. No payload is defined for the trigger transmission. The trailer of all transmissions is a parity bit. This is used to detect single bit errors in the transmission [60, p. 210f.].

iPMT Uplink sampling

For each iPMT an individual uplink signal (SYNC TX) is connected to the FPGA of the ZYNQ on the SB. This is a difference to the downlink signal (SYNC RX) which is the same signal for all iPMTs.

In order to correctly sample the received bits, a clock signal with the appropriate frequency is required. For the downlink this is solved on the iPMTs by using the dedicated CDR IC. Using the same CDR IC for every channel on the SB is not necessary and would not be feasible for cost reasons and the limited number of FPGA pins. Instead, the uplink data have to be transmitted from the iPMT from the VULCAN clock domain, which is itself based on the recovered downlink clock. This makes it

[2]The preceding "b" means that the following number is written in binary representation with the least significant bit first.

possible to sample the uplink bits on the SB with the master clock, since they have the same frequency and a fixed phase relation.

Each uplink channel has an individual phase shift due to different lengths of the signal transmission lines. The differences occur mostly due to different CAT5 cable lengths of the iPMTs, but also due to different routing lengths on the PCB for the different channels. Thus, each uplink channel has to adjust its sampling point for a reliable transmission. By sampling the incoming data streams more often than normally required – a technique called oversampling – a valid sample point can be chosen. Instead of sampling with a frequency of 125 MHz, as it would be normally required, the data streams are sampled with 500 MHz[3], resulting in 4 x oversampling. The subsequent recovery of the data is partially based on [85]. The output of the sampling module is passed through a manchester decoder, since the uplink uses the manchester code as well. Each uplink data stream is connected to a PRBS receiver IP-Core (cf. Section 5.2.10), to allow for measuring the bit error rate for each channel simultaneously.

5.5 iPMT software infrastructure

The iPMT system requires additional software infrastructure for its operation which is explained in the following sections.

5.5.1 PetaLinux

In order to exploit the capabilities of the SoC on the iPMTs and SBs, a small embedded Linux distribution is used. The free of charge product *PetaLinux* is offered by Xilinx for this purpose [86]. An advantage of implementing functionality in the Linux system is the use of standard programming languages like C++. Typically development time is shorter for such languages and required knowledge is less specific than for the design of FPGAs. Thus, functionality which does not require a precise timing, like the sending of already recorded waveform packages, is implemented within the PS.

5.5.2 Processing System Software

Several tasks have to be implemented in the PS of both ZYNQ systems, on the SB and on the iPMT. Since the tasks are similar, the software is based on a common code base. The software running on the iPMT (SB) ZYNQ is called iPMTClient (SBClient).

Data transfer Both clients manage the data transfer from the PL to the PS. Those transfers are initiated from the client software. Subsequently the data are written from the PL to the RAM for buffering and then sent to the EB.

Control and interfaces Several parameters of the PL and the clients need to be controlled and configured. The clients provide therefore a wide set of human readable commands (e.g., in the form "trg_set_delay 10"). The commands are interpreted by the respective client software. If the command affects the PL, the corresponding data are transferred via the AXI bus system to the FPGA.

[3] Fig. 5.8 locates the sampling block in the 250 MHz clock domain since the input data are sampled on the falling and rising edge of a 250 MHz clock, which results in an effective sampling frequency of 500 MHz.

The clients provide three interfaces for the command access. A command line interface is mostly used during the development and testing phase. A UDP and a **T**ransmission **C**ontrol **P**rotocol (TCP) interface are provided for issuing commands from other software.

5.5.3 Network services

A number of network services is required for the operation of the iPMT system:

DHCP For assigning IP addresses to the individual iPMTs DHCP is used. Each SCCU and each RoB have a unique MAC address by which they are identified. The DCHP configuration is populated based on a database which stores the MAC addresses of the components building an iPMT.

TFTP TFTP is a simple file transfer protocol which is used to deploy the Linux image to the iPMTs.

DNS A DNS system is used to assign a name for each network component of the iPMT. For an iPMT with the number 1, that would be "sccu001" and "rob001". By determining the network name on the linux system the iPMT can identify its own number.

NFS The NFS protocol is used to distribute the required software and scripts to the iPMTs. Since the iPMTs can be identified based on their internal number (see paragraph DNS) this system features a high degree of flexibility which software to run. This can be used to update the running software as well as for development and debugging purposes.

5.6 System startup and configuration

The iPMTs are designed as a flexible system with an easily changeable FPGA design and configuration. Two system parts of the iPMT are configurable, respectively software-based. These are the PL and the PS of the ZYNQ SoC. The firmware which is used on the SCCU can not be changed without direct physical access to the board (cf. Section 4.4.3).

A 32 MB flash memory is available as non-volatile storage for the FPGA bitstream and parts of the PS software. This flash can be written via the JTAG interface from the SCCU to replace the FPGA bitstream which is loaded during the startup. The procedure of the system startup after powering the system is depicted in Fig. 5.10.

First boot stage The First Stage Boot Loader (FSBL) is loaded from the flash. It initializes the FPGA with the bitstream from the flash memory. Additionally it reads the MAC address from the MAC EEPROM (cf. Section 4.4.4) and configures the network interface with this MAC. The FSBL hands over to the Second Stage Boot Loader (SSBL).

Second boot stage U-Boot [87] is used as SSBL. It requests an IP address from the DHCP server. Part of the answer to the request is also the name of a boot image. By configuring the DHCP server accordingly, it is thus possible to provide different images to be loaded by different iPMTs, e.g., for debugging and development purposes.

The boot image file is loaded from the TFTP server and subsequently booted (next stage).

Third boot stage The third boot stage is the booting of the PetaLinux image. This also includes executing scripts which mount a network directory (NFS) for access to further software.

Changing the FPGA bitstream Apart from the aforementioned method to change the FPGA bitstream by writing to the flash and reboot the system, there is a second option. Xilinx provides a method to program the PL from the PS via a so-called "FPGA Manager". Thus, it is possible to change the FPGA design during the run-time. This method does not write to the flash and is therefore only a temporary change, i.e. until the next power cycle.

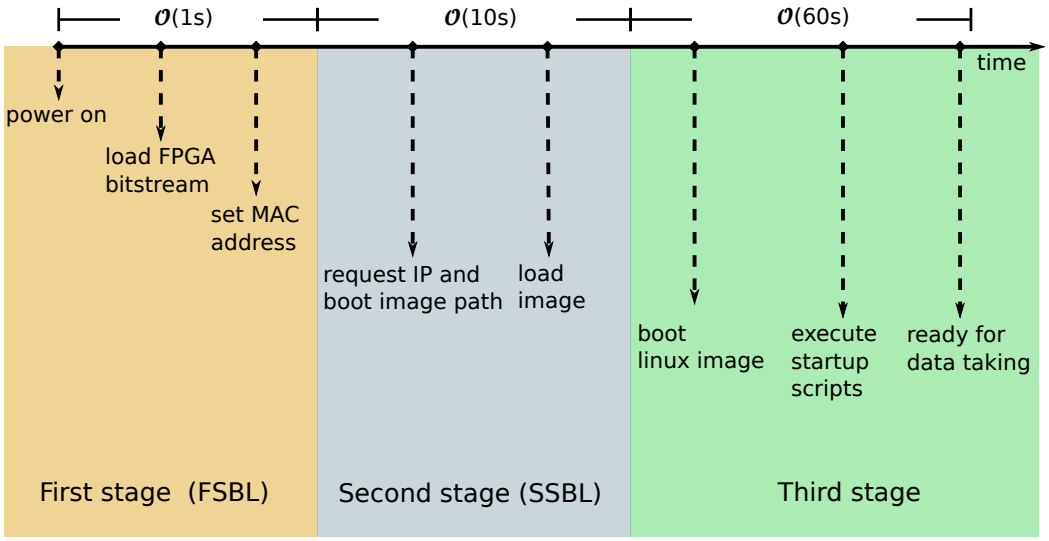


FIGURE 5.10: Startup sequence of an iPMT. Details for the steps are explained in Section 5.6.

5.6.1 VULCAN configuration database

A further part of software infrastructure which is required for the iPMT system is a database for configuration values of VULCAN (cf. Section 4.4.4), which has been designed within the working group. VULCAN is a highly configurable ASIC and some registers require an individual configuration for each chip. Therefore, the database is designed such that most of the parameters are taken from a default configuration. Values deviating from the default ones are stored separately. The configuration of one VULCAN is then built based on the default configuration and the changes which overwrite the default values. Approximately 18 of the ∼250 registers need to be configured for each chip individually.

For bookkeeping purposes, every configuration value is assigned with a timestamp (also the default values, since they can change over time, too). This allows for the reconstruction of a certain configuration for a given time.

5.6.2 Slow control and monitoring

The software framework *Experimental physics and industrial control system* (EPICS) is used as basis for the slow control and monitoring of the OSIRIS detector [33, 61]. Integrating the iPMT system into the EPICS framework requires developing so-called input/output controllers (IOCs). These are software entities which integrate the support for a certain functionality into the framework. This can be, for example, the readout of a temperature sensor or the configuration of a device.

IOCs have been developed within the working group for several components. These cover reading sensor data (like temperature, voltage and current) from the SBs, SCBs and from the PoE, SCCU, RoB and HV module for each iPMT. Furthermore, also control and status commands which are provided by the iPMTClient respectively SBClient are integrated into EPICS via dedicated IOCs.
Approximately 100 variables are provided via the IOCs for monitoring and control for each iPMT [33].

Chapter 6

iPMT system characterization

This chapter summarizes multiple measurements for the characterization of the iPMT system. It is structured such, that single or less complex parts of the system are characterized first and more complex features involving multiple system components are described later.

Sections 6.1 and 6.2 present measurements of the PoE board and the system power requirements. Section 6.3 and Section 6.4 describe the tuning of VULCAN parameters, which is followed by a current calibration of VULCAN in Section 6.5.

Measurements of the data transfer limits (Section 6.6) and an evaluation of the synchronization (Section 6.7) are presented. An evaluation of a fully assembled single iPMT with PMT data is presented in Section 6.8.

6.1 PoE Board

The PoE board hosts the central voltage converters for the iPMTs as described in Section 4.4.2. Characterizing measurements have been performed by using combinations of resistors as load.

Efficiency The efficiency of the 48 V to 5 V DC/DC is measured for output currents in the range from 0.5 A to 2.5 A. For currents of about 1.5 A and above, an efficiency in the order of (83 ± 1) % is measured, as shown in Fig. 6.1. The required current of an iPMT is in the order of 1.5 A (cf. Table 6.1).

The PoE input voltage is also converted to 24 V for the **H**igh **V**oltage (HV) board by the commercially available DC/DC *Traco TEN3-4815N*. It has a typical efficiency of 84 % [88].

Maximum power The maximum output power on the 5 V rail is mainly limited by the transformer. For output currents above ≈2.7 A (13.5 W) the transferred power is at maximum. For higher currents, the output voltage drops significantly and the transferred power declines.

The 24 V rail provides a maximum output current of 125 mA [88], of which about 25 % are actually used (depending on the voltage for the PMT).

6.2 Power consumption

The power consumption of the iPMTs is a relevant property for planning and providing resources for OSIRIS. Since the iPMTs are powered via PoE (cf. Section 4.4.2) special switches with a sufficient power budget are required for the operation. Furthermore,

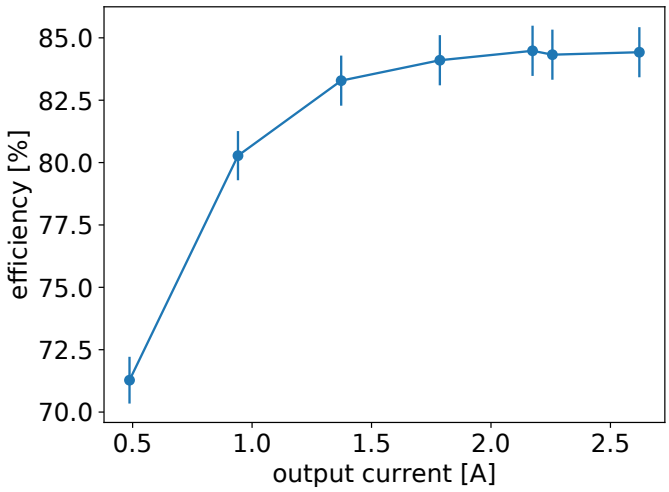


FIGURE 6.1: Efficiency of the 48 V to 5 V DC/DC.

the power is mostly transferred into heat, thus increasing the shell temperature and subsequently transferring the heat into the OSIRIS water buffer. As the water buffer should be kept at a constant temperature, the water has to be cooled. Therefore, a 10 kW heat exchanger is foreseen to counteract the heat transfer from the LS, the iPMTs and other heat sources [33, p. 8].

The power consumption of the iPMTs is highest during data taking when all system components are active. A distribution of the maximum power consumption as measured by the PoE switch is given in Fig. 6.2. These data were taken during evaluation measurements before shipment of the iPMTs, with the iPMTs in an isolated container with a temperature controlled at about 17 °C. An additional airflow over the stainless steel shell was provided for better heat transfer to the environment. The total power for all iPMTs in the OSIRIS water tank of about $75 \cdot 10\,\mathrm{W} = 750\,\mathrm{W}$ is less than 10 % of the total power of the heat exchanger for the water buffer.

To classify this power consumption it can be compared to the target power consumption of the electronics for JUNO. Based on the conceptual design report [18], a power consumption of about 10 W per channel can be deduced [39]. With a mean power consumption of $(9.9 \pm 0.1)\,\mathrm{W}$ this requirement is fulfilled.

Power consumption of the individual boards Via the voltage and current sensors, a more detailed insight into the power consumption of the individual boards can be gained. Table 6.1 shows an exemplary distribution for the different boards during PMT data taking (i.e. during maximum power consumption). The main consumer is the RoB with VULCAN and the ZYNQ. Changes in the software and FPGA design can lead to variations of the power consumption of the RoB part. With a power consumption of about 7.4 W on the 5 V rail, the maximum output power of the 48 V to 5 V DC/DC is utilized to about $7.4\,\mathrm{W}/13.5\,\mathrm{W} = 55\,\%$[1].

[1] 13.5 W is the approximate maximum output power which corresponds to about 16 W input power.

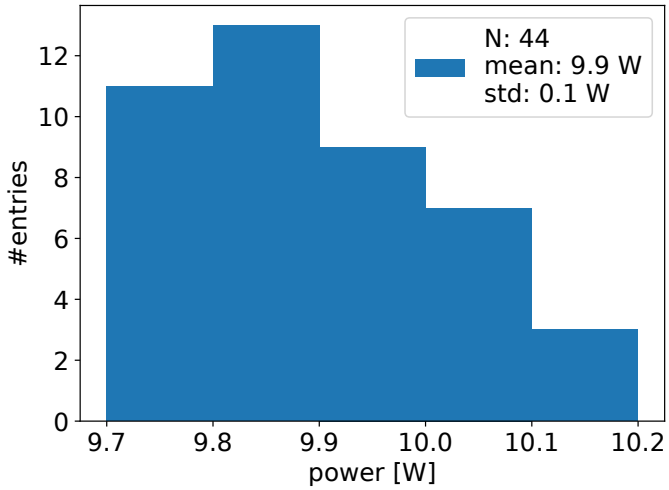


FIGURE 6.2: Maximum power consumption of fully operational iPMTs as reported from the PoE switch (thus including losses due to cables and converters). The resolution of the power measurement of the switch is 100 mW.

TABLE 6.1: Power consumption of an iPMT splitted up for the individual boards. (*) Assuming a 35 m Cat5e cable with a DC resistance of $0.129\,\Omega\,\mathrm{m}^{-1}$ (based on AWG 26/7 wires used for the iPMT cable [89]) and a current of $(1.39\,\mathrm{W} + 7.49\,\mathrm{W} + 0.78\,\mathrm{W})/48\,\mathrm{V} \approx 200\,\mathrm{mA}$.

Board(s)	voltage rail	measured power	converter efficiency	calculated power pre converter @48 V
PoE	5 V	minor contribution (not measured)		
SCCU	5 V	(1.14 ± 0.01) W	(83 ± 1) %	(1.38 ± 0.02) W
RoB	5 V	(6.21 ± 0.06) W	(83 ± 1) %	(7.49 ± 0.12) W
HV+Base	24 V	(0.65 ± 0.01) W	84 %	(0.78 ± 0.01) W
cable loss estimate*				0.18 W
			Sum	(9.84 ± 0.12) W
			PoE switch power	9.8 W

6.3 VULCAN configuration

This section explains the signal chain from the PMT to the three VULCAN RX and the configuration of VULCAN. Tim Kuhlbusch has characterized VULCAN partially in his master thesis [62]. In the following text the implementation for OSIRIS is described.

6.3.1 VULCAN internal signal chain and PMT connection

VULCAN features three identical receiver (RX), containing each one 8 bit ADC, which is build up by four 6 bit ADCs, for the digitization of the PMT signal. Fig. 6.3 displays a scheme of one receiver. It can roughly be divided into three blocks, the

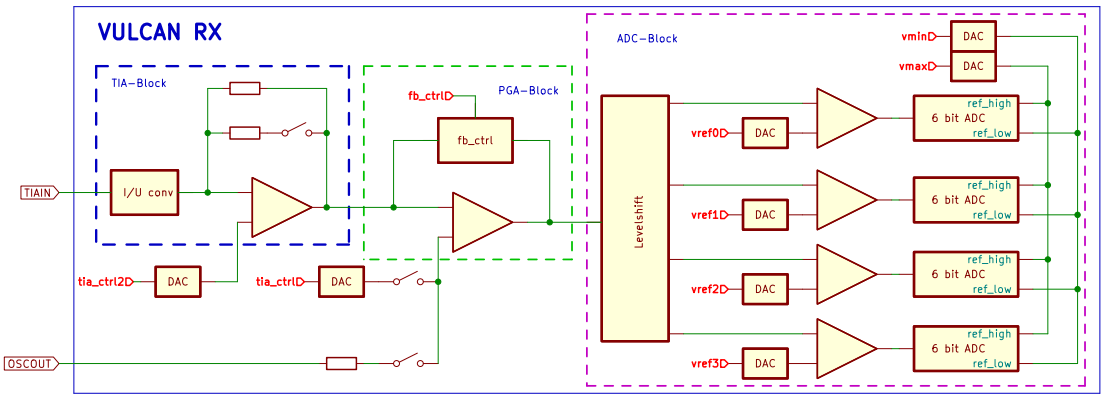


FIGURE 6.3: Simplified scheme of the VULCAN input section of one receiver block. Configurable parameters are highlighted in red (not all configuration options are drawn).

Trans**i**mpedance **A**mplifier (TIA), the **P**rogrammable **G**ain **A**mplifier (PGA) and the ADC. The TIA block contains the current to voltage conversion and provides the first stage amplifier. The amplification of the first stage can be switched between two settings which differ by design by a factor 10.

In a second amplification stage, a **P**rogrammable **G**ain **A**mplifier (PGA) is used. Originally implemented for the amplification of the signal, it can also be used to attenuate the signal, with the drawback of possible unstable settings. It has been found that it allows for gain factors in a range of about 0.22 to 2.2 relative to its nominal gain [62].

The ADC block consists of four 6 bit flash ADCs which combine to one 8 bit flash ADC. All 6 bit ADCs have two common reference voltages (denoted as `vmin` and `vmax`) which allow adjusting the input range. By reducing the voltage difference between `vmin` and `vmax` an additional amplification can be implemented, but has the drawback of increased noise, because the voltage difference for a digitization step becomes smaller.

Two PMT signal paths are used depending on the signal amplitude. For small and medium signals in the range from 0 mA to ≈ -20 mA the input which is denoted as *TIAIN* is used.

For large signals below -20 mA the TIA input saturates and electrostatic discharge diodes (ESD) become conductive (diodes not drawn in Fig. 6.3) [97]. The voltage across the diodes is measured via the pin *OSCOUT*. Internally, the signal bypasses the first amplification stage and the voltage signal is directly fed into the PGA.

For the iPMT, the connection between the PMT and VULCAN is implemented as depicted in Fig. 6.4. The PMT anode is on positive high voltage, thus can not directly be connected to VULCAN. Therefore, a 10 nF high-voltage capacitor is used to decouple the PMT signal. Following, a dedicated circuit is used to match the PMT output impedance of about 150 Ω to 200 Ω to VULCAN's input impedance of about 5 Ω (each *TIAIN* input has an impedance of about $Z_{\text{TIA}} = 10\,\Omega$.). The input impedance of the combined VULCAN input Z_{VULCAN}, i.e. the node after the 10 µF capacitor is calculated to

$$\begin{aligned} Z_{\text{VULCAN}} &= (Z_{\text{TIA}} + 30\,\Omega) \parallel (Z_{\text{TIA}} + 30\,\Omega) \parallel (Z_{\text{OSCOUT}} + 27\,\text{k}\Omega) \\ &\approx (Z_{\text{TIA}} + 30\,\Omega) \parallel (Z_{\text{TIA}} + 30\,\Omega) \\ &= 0.5 \cdot (Z_{\text{TIA}} + 30\,\Omega) \\ &= 20\,\Omega. \end{aligned}$$

The additional impedance of the *OSCOUT2* input path (including the 27 kΩ resistor) can be neglected since it is high-ohmic compared to the *TIA* inputs. The input impedance of the RoB is estimated to

$$Z_{\text{ROB}} = [(Z_{\text{VULCAN}} \cdot G_T) + R_C] \cdot G_T = 195\,\Omega \tag{6.1}$$

with the transformer impedance ratio $G_T = 3$ and the resistor between the transformer $R_C = 5\,\Omega$. The 22 pF capacitors are placed close to the input pins for the stabilization of the TIAs. The contribution of the 10 µF capacitor is neglected here, since its reactance for relevant frequencies above 100 kHz is smaller than $X_C = 1/(2\pi f C) = 0.16\,\Omega$ and thus negligible small. The high ohmic paths over the 22 kΩ resistor which is parallel to Z_{ROB} has a negligible effect as well:

$$Z_{\text{ROB}} \parallel 22\,\text{k}\Omega \approx 193\,\Omega. \tag{6.2}$$

This impedance matching has been found in an iterative approach and provides reasonable results especially with respect to under- or overshoot after pulses, which would hint towards impedance mismatch.

RX1 and RX3 use the *TIAIN* input pin and are configured with a high (RX1) and medium (RX3) gain. It is possible to swap RX1 and RX3 by adapting the configuration. RX2 is used for high signals, requiring a low gain, which is accomplished via the *OSCOUT* pin. Using RX2 as HG or MG would require hardware changes and is thus not possible after the iPMT has been potted.

6.4 VULCAN parameter tuning

VULCAN is a highly configurable ASIC which makes it very flexible, but with the drawback of high complexity regarding the configuration. The vast majority of configuration values is the same for all chips. For certain registers an individual configuration per chip is required, due to variations of the temperature, supply voltages and semiconductor production.

At least six parameters need to be adapted for each of the three receiver blocks. They are denoted as `tia_ctrl`, `tia_ctrl2` and `vref0` to `vref3` in Fig. 6.3. The configuration of `tia_ctrl` and `tia_ctrl2` is described in Section 6.4.1 and used for setting the baseline. Subsequently, the alignment of the individual 6 bit ADCs `vref0` to `vref3`

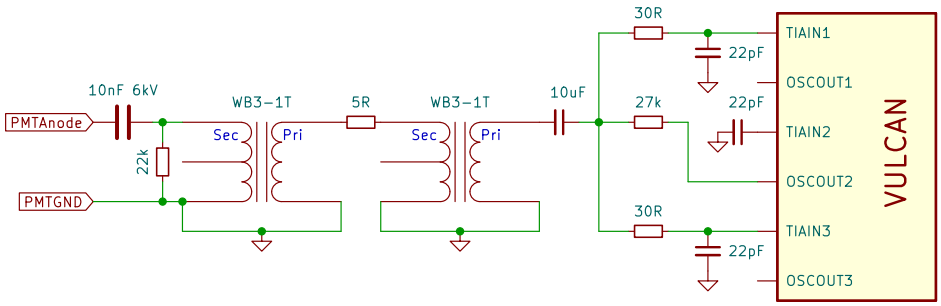


FIGURE 6.4: Schematic of the PMT to VULCAN connection. The number appended to the VULCAN pin names denotes the number of the RX. The transformer WB3-1T has an impedance ratio of 3:1 (sec:pri) [90]. The impedance matching is based on the patent [63].

is described in Section 6.4.3. The determination of the sample order parameter is given in Section 6.4.4.

The measurements in this section are predominantly done with a so-called half-stack. This is a stack consisting of the three boards PoE, SCCU and RoB. Base and HV are missing at this stage due to constraints for the order of assembly steps for the production of the iPMTs.

6.4.1 Baseline alignment

The term *baseline* refers here to the ADC output value without input signal. The target values for the baselines for each RX are given in Table 6.2. Lower baseline values for MG and LG are motivated by lower noise compared to the HG.

TABLE 6.2: Target values for the baseline levels and the thresholds for switching to the next RX.

RX	baseline target [LSB]	upward switching threshold [LSB]
HG	20	250
MG	10	250
LG	5	-

The parameters `tia_ctrl` and `tia_ctrl2` can be used to control the baseline level. How the baseline value changes in dependency of `tia_ctrl` and `tia_ctrl2` depends also on the configuration of the RX. A sweep of `tia_ctrl` and `tia_ctrl2` for each receiver block is shown in the diagonal plots (top left to bottom right) in Fig. 6.5. This kind of scan was developed in the context of [62] and is reproduced due to the changes in the configuration and hardware.

RX1 is configured as HG, using the high amplification setting in the first stage. For low values of `tia_ctrl2` approximately in the range from 0 LSB to 100 LSB and for high values in the range from 225 LSB to 255 LSB, saturation regions of the amplifier are reached. In the central region, both parameter show a strong influence on the baseline of ~ -5 LSB/LSB for `tia_ctrl`, respectively ~ 6 LSB/LSB for `tia_ctrl2`.

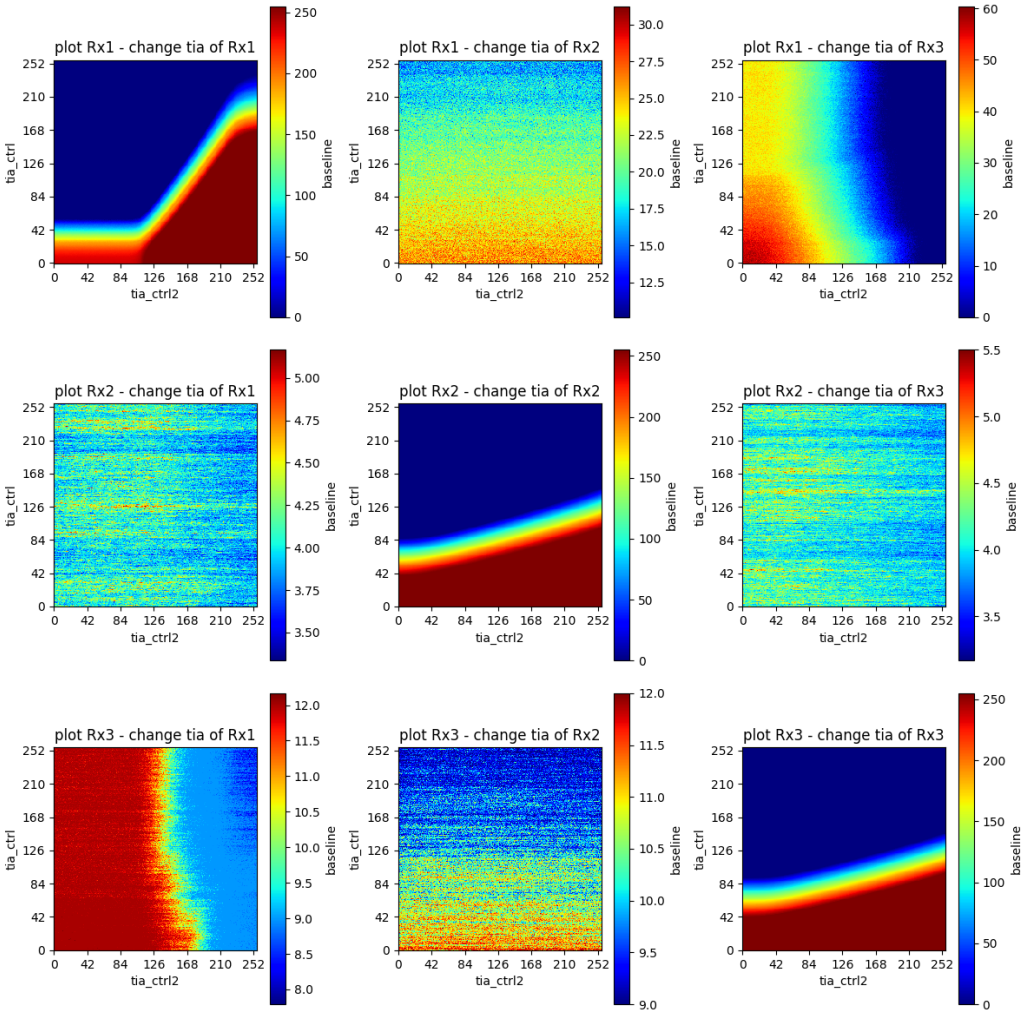


FIGURE 6.5: Sweep of the `tia_ctrl` and `tia_ctrl2` parameters in steps of 1 LSB for the HG (left column, RX1), LG (middle column, RX2) and MG (right column, RX3). The baseline value is the depicted by the color-coded z-axis. Mind the adapting scales for the off-diagonal plots.

For RX2 and RX3 the gradient in the `tia_ctrl2` axis is reduced, since the first stage amplifier is set to its low amplification setting. The gradients are ~ -5.5 LSB/LSB for `tia_ctrl`, respectively ~ 1.5 LSB/LSB for `tia_ctrl2`.

It has been found, that the biasing via `tia_ctrl` and `tia_ctrl2` are mutually affecting the baseline value of the other receivers. This effect is shown in the off-diagonal plots in Fig. 6.5. Especially changing RX3 (MG receiver) can shift the baseline of RX1 (HG receiver) by several tens of LSB.

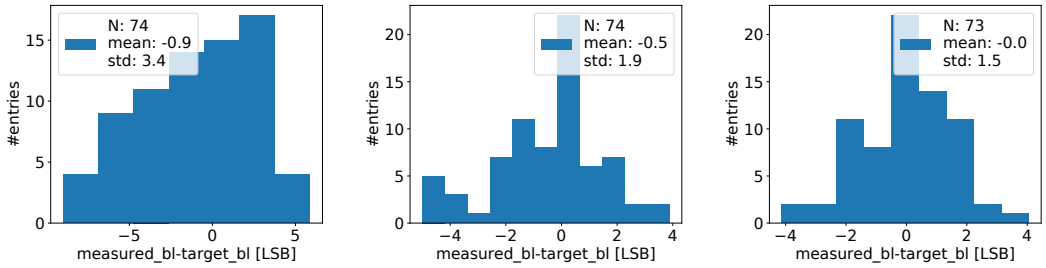
The configuration parameter for the baseline are determined by using a minimizer with the following loss function:

$$L(\mathbf{bl};\mathbf{t}) = \sum_{i=0}^{n}\sum_{j=0}^{m}(t_i - bl_j)^2 + e^{-10\cdot(bl_i-3)} \tag{6.3}$$

With the baseline sample vector **bl** with a length m, with the number of RX taken

into account n (normally $n = 3$) and the baseline target values $\mathbf{t}$. The exponential term is a penalty for values close to zero. The starting parameters are determined with a binary search.

Fig. 6.6 shows the comparison between the target baseline values and the baseline values which were recorded afterwards. The distributions are centered close to zero,



(a) ADC1 – HG (b) ADC2 – LG (c) ADC3 – MG

FIGURE 6.6: Comparison of the target baseline values and the measured baseline values.

showing that the procedure works in general. The large tails especially for the LG receiver can be problematic, since the baseline gets very close to 0 LSB. This tests shows that the procedure might require slight improvements or a slightly (5 LSB) higher target baseline for the LG.

These results depend on environmental factors, foremost the chip temperature. Therefore, it might be necessary to repeat this procedure when external factors change and the determined values might not be directly usable for OSIRIS, due to other equilibrium temperatures than during the tests.

6.4.2 Temperature effect on the baseline

The VULCAN baseline values have shown a strong temperature dependence in previous measurements [62, p. 47]. This has been reevaluated for the final design and for all three RX exemplarily with one setup.

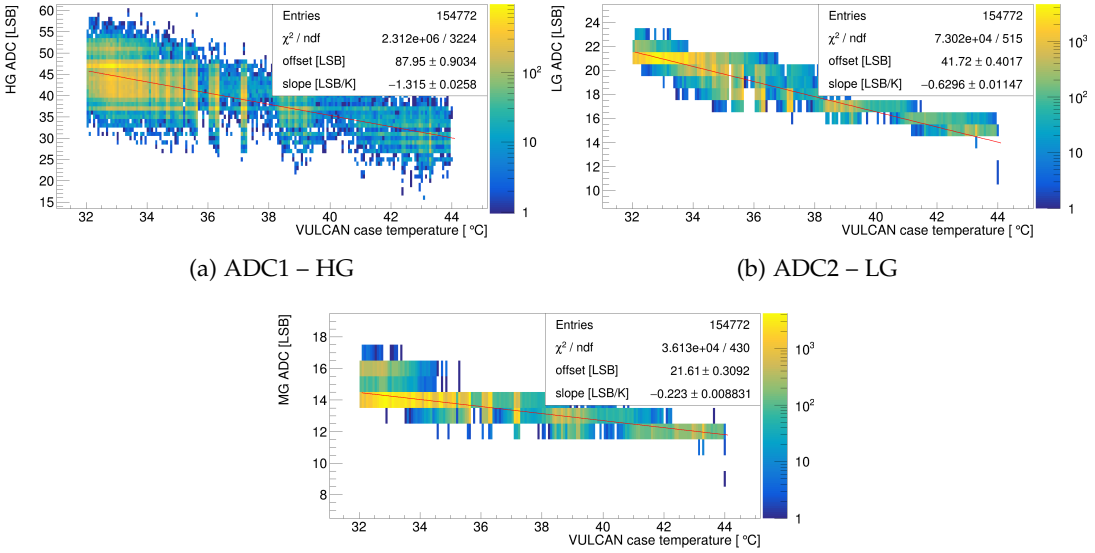
An iPMT halfstack is placed within an isolated shipping container, which is temperature controlled and set to a target temperature of 17 °C. A fan generates an airflow for the setup. This airflow is slowly varied to achieve a temperature change. VULCAN does not provide an internal temperature diode or a comparable sensor. Instead, a transistor is placed in contact to the VULCAN case as proxy.

Data are recorded without an input signal and plotted in dependence of the measured temperature in Fig. 6.7. The correlations between the ADC output and the temperature for the different RX are summarized in Table 6.3.

The largest influence is observed for the HG ADC with about -1.3 LSB/K. For the operation of OSIRIS this has the consequence that alignments of the baseline (described in Section 6.4.1) need to be performed after the setup has warmed up to a stable temperature.

6.4.3 ADC alignment

A further part of VULCAN which requires tuning in the analog domain, is the actual ADC. As depicted in Fig. 6.3 the ADC of each receiver block is composed of four 6 bit



(a) ADC1 – HG

(b) ADC2 – LG

(c) ADC3 – MG

FIGURE 6.7: Correlation of ADCs output and VULCAN case temperature without input signal.

TABLE 6.3: Baseline temperature dependence of VULCAN.

RX	gain config	slope LSB/K
1	HG	-1.32 ± 0.03
2	LG	-0.63 ± 0.01
3	MG	-0.22 ± 0.01

ADCs. The four 6 bit ADCs share the two reference voltages, `vmin` and `vmax`. These range parameters are not used for tuning but rather kept fixed for all three RX. An offset can be configured for each 6 bit ADC individually, these are denoted as `vref0` to `vref3`. These parameters are used to align the 6 bit ADCs such that their input ranges build a contiguous range without overlaps or "holes". If the input ranges of two 6 bit ADCs overlap, the slope of the output signal increase in this overlap region. If a gap is apparent between two 6 bit ADCs, the slope is zero in the gap region.

The appearance of an overlap or a gap depends also on the digital configuration of VULCAN. Two modes, gray-code or count-ones, can be used to convert the output of the individual comparators to a binary output. In the count-ones mode, the sum of all comparator bits is calculated and converted into a binary output. For the gray-code mode, the first transition between ones and zeros is used for the conversion to the binary output. Additionally, a single bubble error correction is implemented in VULCAN which can be enabled separately. It corrects the bits based on the majority of the comparator itself and neighboring comparators [48, p. 96].

A procedure was developed within the working group to align the 6 bit ADCs. In previous measurements ([62, p. 23f]) linear pulse signals from a signal generator were used for the alignment. The aim was to develop a method which is also usable when VULCAN is connected to the PMT and no pulse generator can be connected. This can be achieved by exploiting the internal **D**igital-to-**A**nalog **C**onverters (DACs) which

are controlled by the parameter `tia_ctrl` and `tia_ctrl2`. The basic idea is to use the DACs to provide a static signal for the ADCs by shifting the baseline. It is assumed, that the DACs are sufficiently linear. The ADC output is not evaluated via a readout of the LVDS output, but by reading the internal status registers via the JTAG interface.

Configuration of the RX The effect of changing `tia_ctrl` and `tia_ctrl2` is depicted in Fig. 6.5 for the different receiver configurations. For the alignment procedure, each RX is configured with a high amplification in the first stage (left upper plot of Fig. 6.5). This has the advantage that a comparatively low gradient can be achieved along the `tia_ctrl` direction when using a `tia_ctrl2` value of 255. Thus, the ADC input is changed only via the `tia_ctrl` parameter, which is called "`tia_ctrl` scan" in the following procedure. Furthermore, the digital part of VULCAN is configured to use gray code for an easier transition detection.

Procedure The algorithm requires an "endpoint" target value, this is the lowest `tia_ctrl` value which results in an ADC output of 0 LSB. The target value itself is called anchor. The procedure is described in Algorithm 1. Fig. 6.8 shows an exemplary result of the described procedure. A slight non-linearity especially within the region from 0 LSB to 64 LSB of the ADC can be observed.

Algorithm 1 Procedure for 6 bit ADC alignment.

DETERMINE VREF0
- Set `vref0` to its start value
- Set all other buffers such that they do not contribute (i.e. set `vref1` to `vref3` to 255)
- **for** target number iterations **do**
  - Set new value for `vref0`
  - Scan over `tia_ctrl` in the relevant region
  - Fit a linear model to the recorded points and extrapolate the value for `tia_ctrl` at the endpoint
  - Change `vref0` such, that the endpoint moves closer to the anchor value
  - Store `vref0` and the resulting endpoint
- **end for**
- Set `vref0` to the best matching value, i.e. the value which minimizes the difference between endpoint and anchor
- Shift start value of `vref1` to `vref3` by the difference `vref0` - "best matching value"

DETERMINE VREF1 TO VREF3
- **for** `vrefX` with X in (1,2,3) **do**
  - Set current buffer to start value
  - **for** `vrefX` in range around start value **do**
    - Scan over `tia_ctrl` in relevant region
    - Fit lines to region around ADC border (borders are at 64, 128, 192) for previous ADC and current ADC
    - Calculate and store the difference of the lines at the respective border
  - **end for**
  - Use the value which resulted in the smallest difference
- **end for**

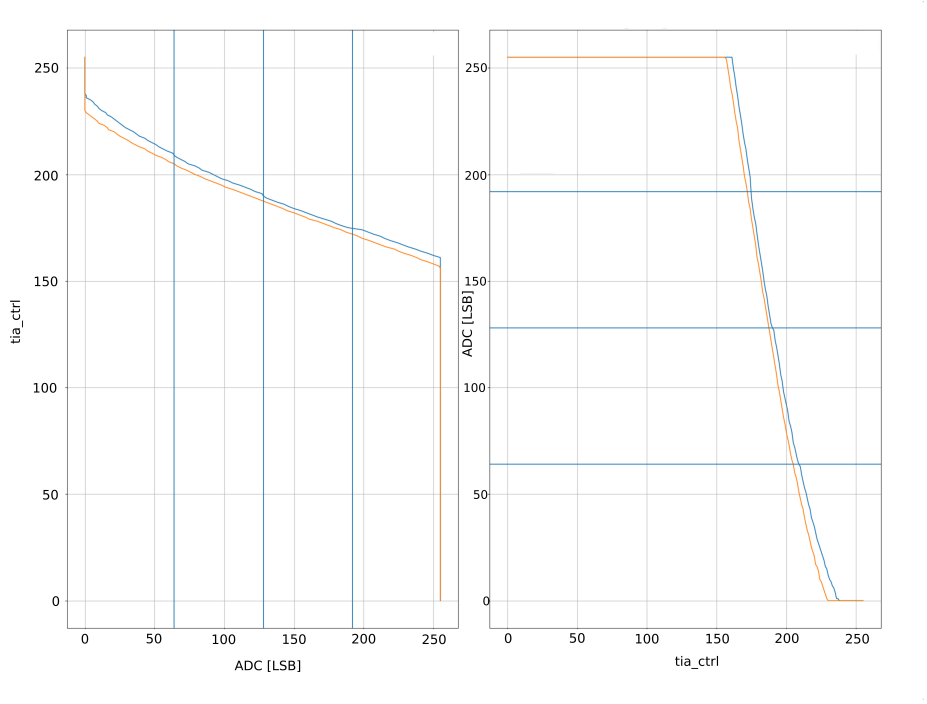


FIGURE 6.8: Comparison of the ADC output for a tia_ ctrl scan over the whole range before and after alignment. The blue line depicts the output for a `tia_ctrl` scan before the alignment, the orange line after the alignment procedure.

This procedure was used for the production for the OSIRIS iPMTs. A visual check was employed to control the results. In few cases this has shown a failure of the procedure, which was then either repeated or a manual adjustment of the vref values was performed.

6.4.4 Sample order detection

VULCAN provides the option to reorder digitized samples within blocks of four samples. Internally, VULCAN uses different clock frequencies for the data processing in the ADC and in the digital part. Four samples from the ADC are processed within one clock cycle of the data processor [48, p. 45]. To process the samples in the correct time order it is required to configure a sample ordering different from the order $[1, 2, 3, 4]$. It has been found that there are two possible ordering schemes, $[3, 4, 2, 1]$ and $[2, 1, 3, 4]$. The second ordering is a by two samples shifted version of the first ordering. A possible explanation for this behavior is a missing synchronization between clocks for the analog part and the digital part of VULCAN. Both clocks are derived from the VULCAN internal PLL and thus have a fixed phase relation. The correct sample order has to be determined at least for every power cycle.

When evaluating a recorded waveform, the start of the four sample block is not determined. This leaves two start options for each ordering scheme, since two samples are transmitted on every clock cylce from VULCAN to the FPGA. Thus, four different schemes have to be evaluated to determine the correct ordering.

Following procedure was developed to determine the sample order automatically:

1. Configure VULCAN with sample order [1,2,3,4].

2. Prepare a self-triggered waveform readout with a trigger threshold set to 50 LSB above the baseline value.

3. Change the `tia_ctrl` configuration by e.g., -20 LSB. This leads to a fast baseline shift as depicted in Fig. 6.9 which is easy to evaluate for a correct sample order by eye.

4. Evaluate $D(\mathbf{r}) = \sum_{i=0}^{N_r-2} |r_{i+1} - r_i|$ for all four ordering schemes. $\mathbf{r}$ denotes the waveform sample vector with a length N_r.

5. Apply the sample ordering which minimizes D.

6. Record a waveform for visual cross check.

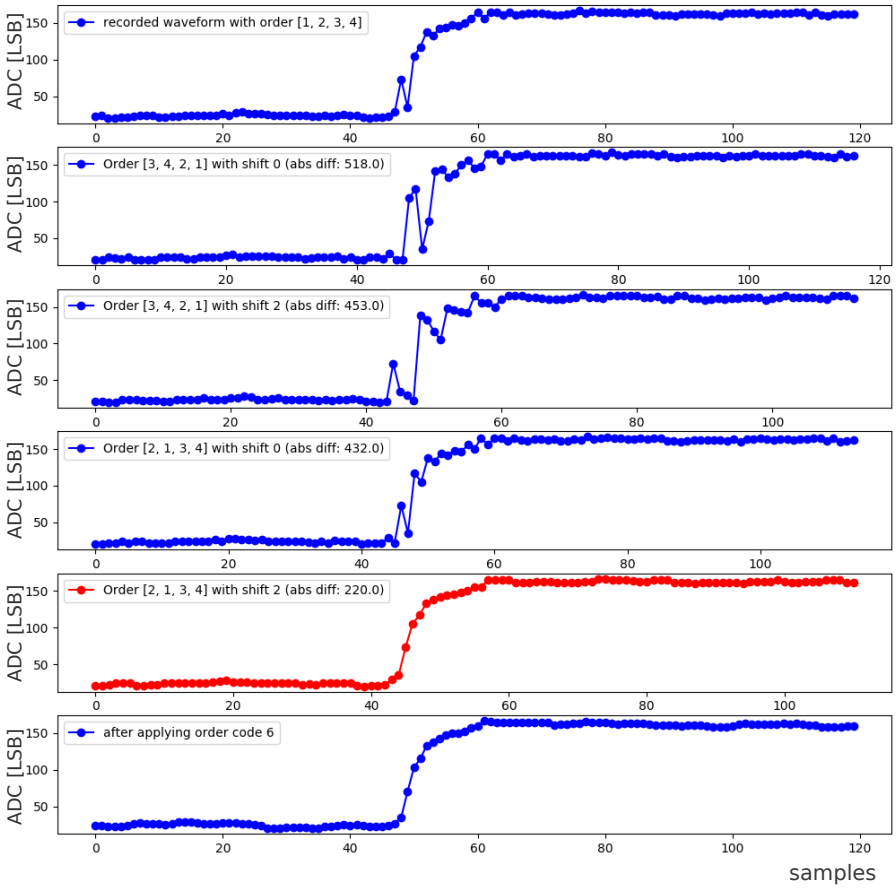


FIGURE 6.9: Visualization of the sample ordering scheme. The upper most plot shows the recorded waveform without any reordering (VULCAN configured order $[1, 2, 3, 4]$). The four subsequent plots depict the evaluation for the four different reordering schemes. Highlighted in red is the reordering scheme which has been found to be correct. The last plot is recorded after applying the correct ordering scheme.

The described procedure has been performed for all produced iPMTs and visually checked for correctness. Eight VULCANs have shown different behaviors with the procedure for when using the HG (RX1) receiver. One example is given in Fig. 6.10. A significantly different slope is apparent, making it more difficult to evaluate the correctness of the sample ordering by eye. For all eight VULCANs a different RX (either MG or LG), which shows a reasonable response to the `tia_ctrl` change, is used.

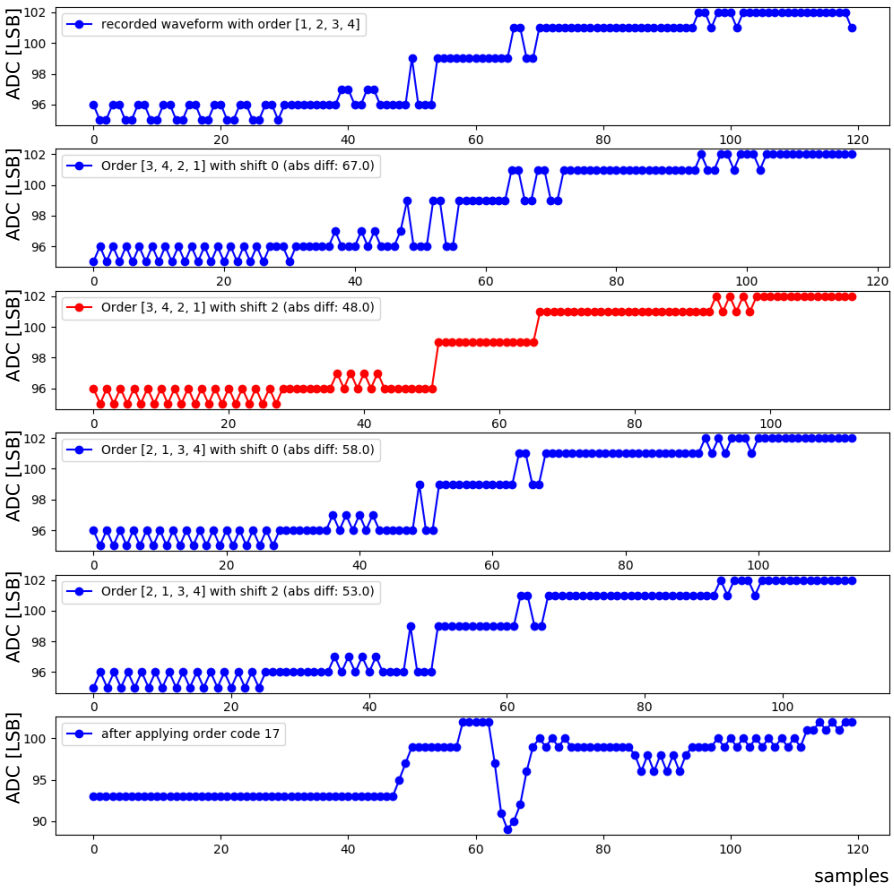


FIGURE 6.10: Example for a sample reorder procedure which shows a slow response to a `tia_ctrl` change.

6.5 VULCAN absolute current calibration

In the context of the characterization of the halfstacks, an absolute current calibration is performed for all VULCANs. This calibration aims to provide a conversion from ADC counts to a current unit.

Following plots contain often more entries than the 75 entries which would be expected based on the number of iPMTs for OSIRIS. In total, 95 final electronics sets

have been produced to have a number of spares in case of defects and for testing and debugging purposes. Thus, following plots include also stacks which will not be part of OSIRIS.

Since the impedance matching (cf. Fig. 6.3) is DC blocking and should be part of the characterization, an **A**lternating **C**urrent (AC) source is required for the calibration signal. As PMTs are (negative) current sources (or current sinks), an AC current source with sufficient bandwidth would be required, which is unfortunately not available. Instead, a normal pulse generator which acts as voltage source is used (*Tektronix AFG31021B*). In order to determine the input current, the voltage drop across a resistor is measured with two oscilloscope channels (*Tektronix DPO2024B*), as depicted in Fig. 6.11.

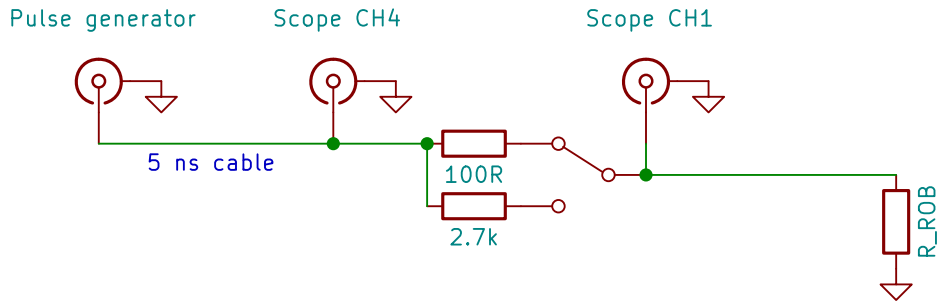


FIGURE 6.11: Connection setup for absolute current calibration. The pulse generator replaces the PMT as signal source. The signal is inserted in front of the impedance matching, but after the 10 nF coupling capacitor (cf. Fig. 6.4) on the RoB. The resistor R_ROB is used here as symbol for the impedance matching and VULCAN.

The input current $i(t)$ is given by

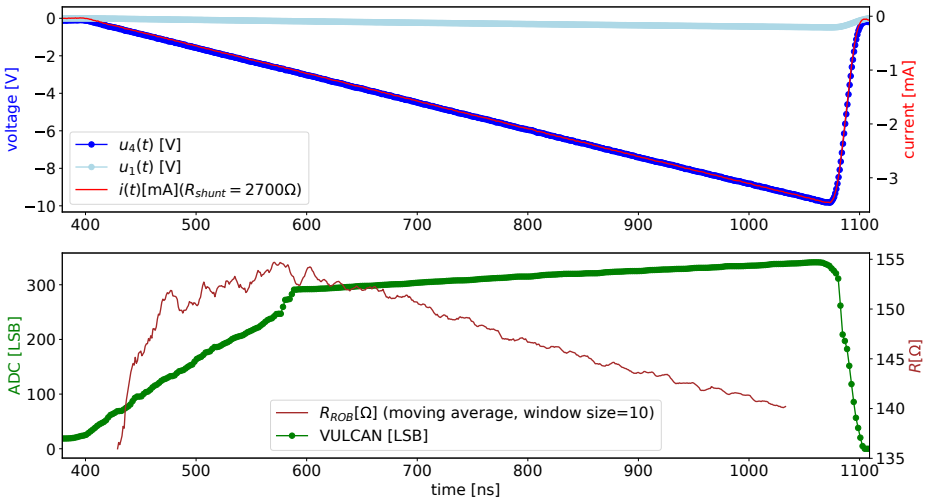
$$i(t) = \frac{u_4(t) - u_1(t)}{R_{\text{shunt}}} \tag{6.4}$$

with $u_4(t)$ the measured voltage of scope channel four, $u_1(t)$ the measured voltage of scope channel one and the resistor between the channels R_{shunt}. With a single R_{shunt} is is not possible to cover all three RX with a reasonable resolution, since the minimum output voltage of the pulse generator is $-10\,\text{V}$. Therefore, it is possible to choose between two resistor values $R_{\text{shunt}} = 100\,\Omega$ and $R_{\text{shunt}} = 2.7\,\text{k}\Omega$ via a relay. The $2.7\,\text{k}\Omega$ resistor covers approximately the range to a current of $-3.5\,\text{mA}$ (cf. Fig. 6.12a) and the $100\,\Omega$ resistor to $-25\,\text{mA}$ (cf. Fig. 6.12b).

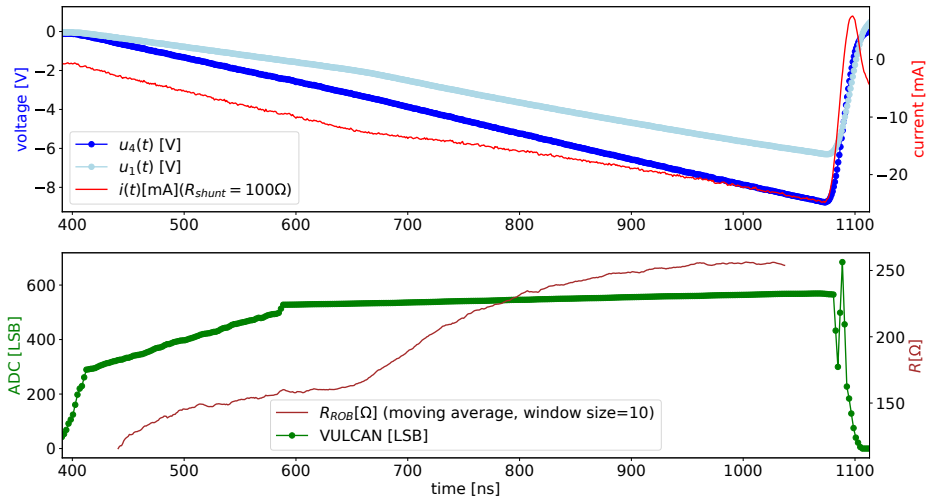
The measured input resistance $R_{\text{ROB}}(t)$ is calculated via

$$R_{\text{ROB}}(t) = \frac{u_4(t)}{i(t)}. \tag{6.5}$$

The tested halfstack is connected to the SB. One trigger output of the SB is used to trigger the pulse generator and the iPMT is configured to use the synchronous link trigger with an automatic follow-up trigger number of 10 (corresponding to a time of 2.64 µs, cf. Section 5.2.6). This ensures the synchronization between the signal generator and the readout from the iPMT. The oscilloscope is not directly synchronized but uses its own threshold trigger on channel four. The recorded voltages are averaged over 10 waveforms. For each setting, 1×10^4 triggers are recorded, which correspond to 900 waveforms with a length of 2.64 µs each.



(a)



(b)

FIGURE 6.12: (a) Example for $R_{\text{shunt}} = 2.7\,\text{k}\Omega$, covering the HG RX and parts of the MG RX. The upper plot depicts the measured voltages and the calculated current. The lower plot shows the averaged recorded waveform and the calculated resistance R_{ROB}. (b) Example for $R_{\text{shunt}} = 100\,\Omega$ which covers HG, MG and LG. The spike on the falling edge is an artifact caused by a swap in the gain assignment bits. For R_{ROB} in (a) and (b) the plotting is restricted to the range corresponding to the 5 % to 95 % range of $u_1(t)$. Uncertainties are not plotted for the sake of clarity.

In a normal configuration, VULCAN transmits data from the RX which are selected by the switching thresholds as it is shown in Fig. 6.12b, where VULCAN switches to receivers with lower gain when the switching threshold is crossed. In order to record data from only one RX, the RX-to-gain assignment is temporarily changed such, that the target RX is declared as HG. In combination with a switching threshold of 255 LSB for the HG to MG switching, only data from the target RX are recorded, even when the maximum count of the ADC of 255 LSB is reached. An example of such a recording is given in Fig. 6.13.

Method

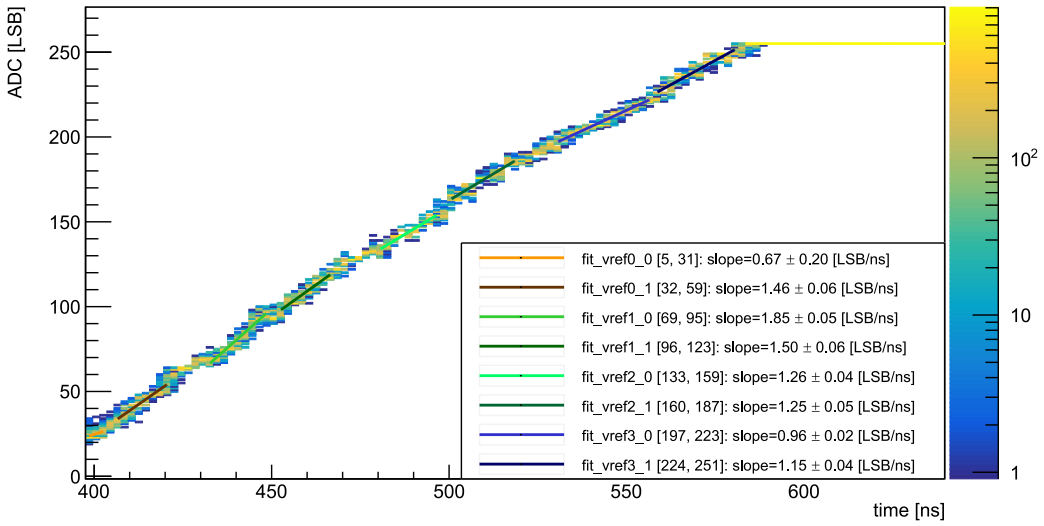


FIGURE 6.13: Histogram of 909 waveforms with fits of linear functions. For the sake of clarity only the subrange fits are shown. The saturation of the ADC is reached approximately at 580 ns.

Linear functions are fitted individually to the recorded VULCAN data and to the scope data. The resulting current slopes are divided to receive a LSB to current conversion factor. The fit to the VULCAN data is splitted into several linear sections. Fits are performed for each 64 LSB vref region individually (0 LSB to 63 LSB, 64 LSB to 127 LSB, 128 LSB to 191 LSB and 192 LSB to 255 LSB). Data around 6 bit ADC borders (at 64 LSB, 128 LSB and 192 LSB) are excluded from the fit with a margin of 5 LSB in both directions. Additionally, fits are performed for two subranges of each 32 LSB for each vref region. This is done, since every 6 bit ADC is split into two 32 bit regions based on different transistor types. An example for a fit of the subranges is shown in Fig. 6.13.

Results

Figs. 6.14 to 6.16 show the results of the current calibration for the three RX. The plot range for all subplots in the figures is restricted to not include outliers. An outlier is

here defined as those data points which are below R_l or above R_u. Those are defined as:

$$\mathrm{IQR} = Q_3 - Q_1 \tag{6.6}$$
$$R_l = Q_1 - 1.5 \cdot \mathrm{IQR} \tag{6.7}$$
$$R_u = Q_3 + 1.5 \cdot \mathrm{IQR} \tag{6.8}$$

where IQR (inter quartile range) is given by the difference between the median of the upper data half Q_3 and the median of the lower data half Q_1. The statistics given in Figs. 6.14 to 6.16 (N, mean, std and median) do not include the outliers.

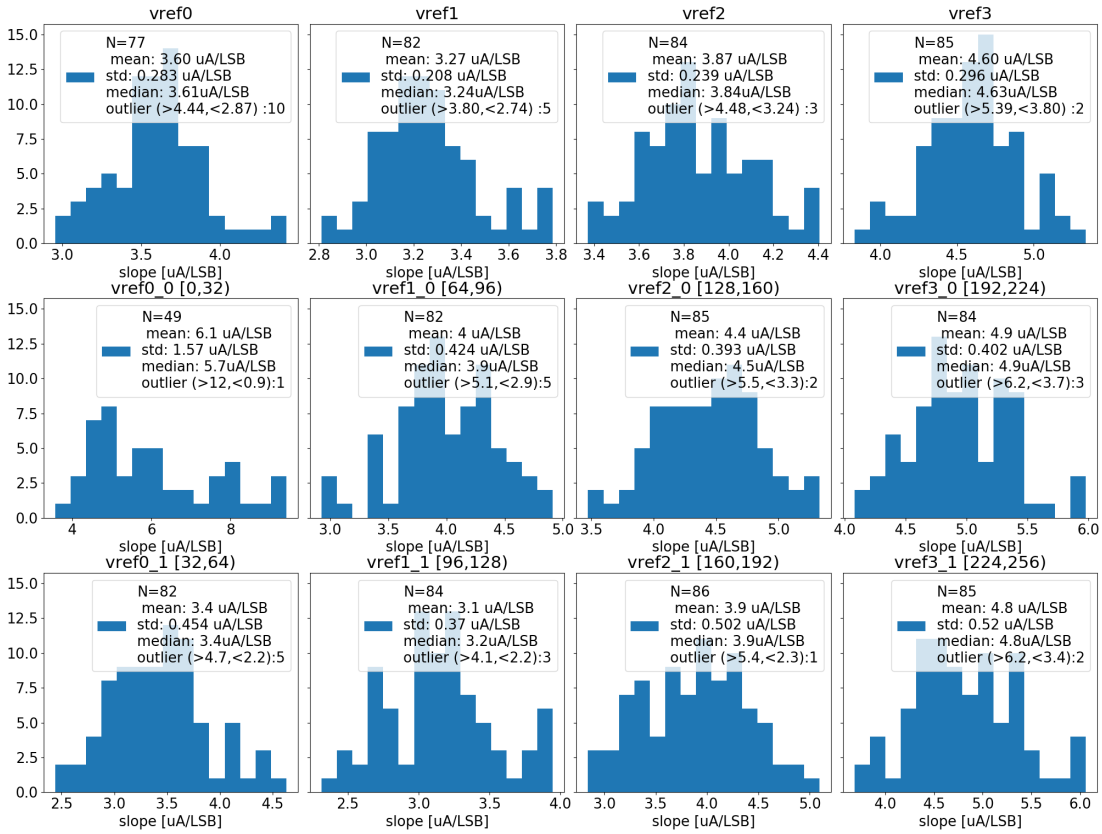


FIGURE 6.14: Current calibration results for HG RX with $R_{\mathrm{shunt}} = 2.7\,\mathrm{k}\Omega$. vref{1,2,3,4} denote fits to the whole vref range, whereas the suffix "_0" ("_1") marks the fit to the lower (upper) 32 bit in the vref region.

The results for the HG RX are shown in Fig. 6.14. Less entries are plotted for the lowest vref region (i.e. vref0_0), since the number of points is often not sufficient for a fit due to a high baseline. A tendency to higher gains for higher signal ranges can be observed. Median values of the distribution are in the range from 3.5 µA/LSB to 5 µA/LSB.

MG distributions are shown in Fig. 6.15. Their median gain is in the range of about 35 µA/LSB to 50 µA/LSB.

Fig. 6.16 depicts the distribution for the LG. This RX shows by design two characteristic slopes (cf. upper plot in Fig. 6.18). The first part for a current in the range from 0 mA to −12 mA is the region where the voltage drop is measured when the ESD diodes are not conducting. For a higher absolute current, the ESD diodes start

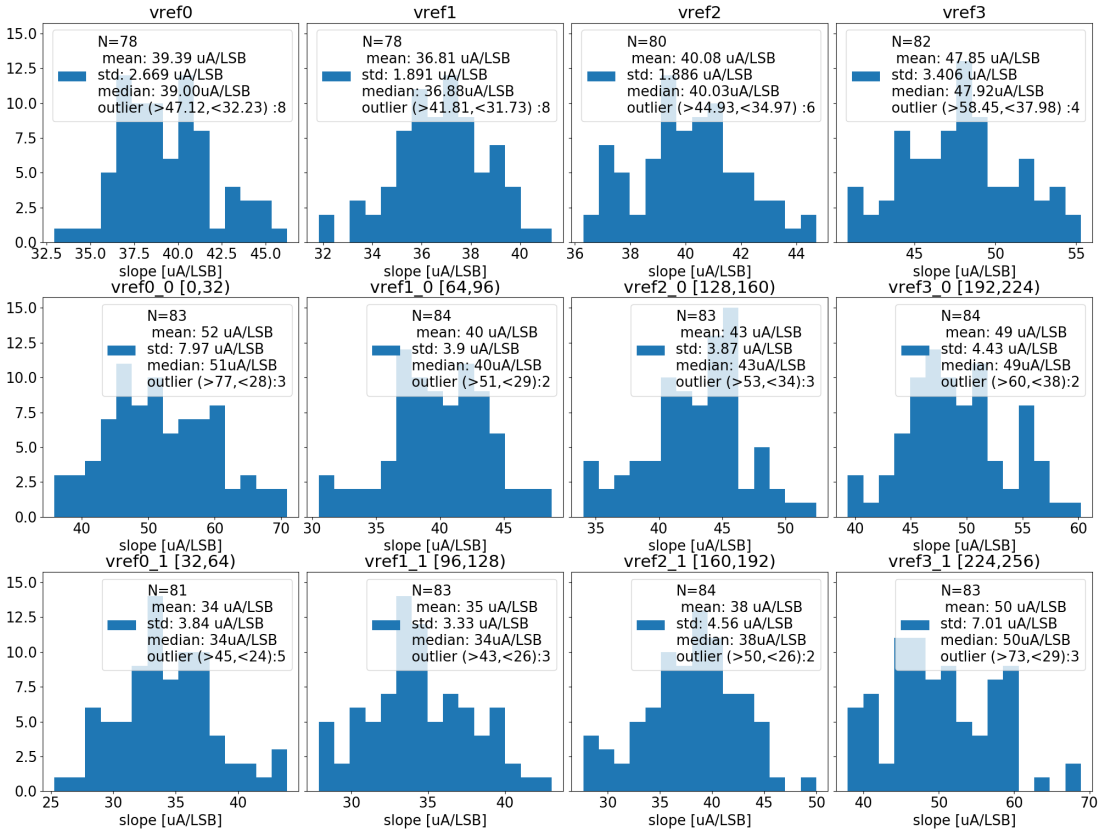


FIGURE 6.15: Current calibration results for MG RX with $R_{\text{shunt}} = 100\,\Omega$. vref{1,2,3,4} denote fits to the whole vref range, whereas the suffix "_0" ("_1") marks the fit to the lower (upper) 32 bit in the vref region.

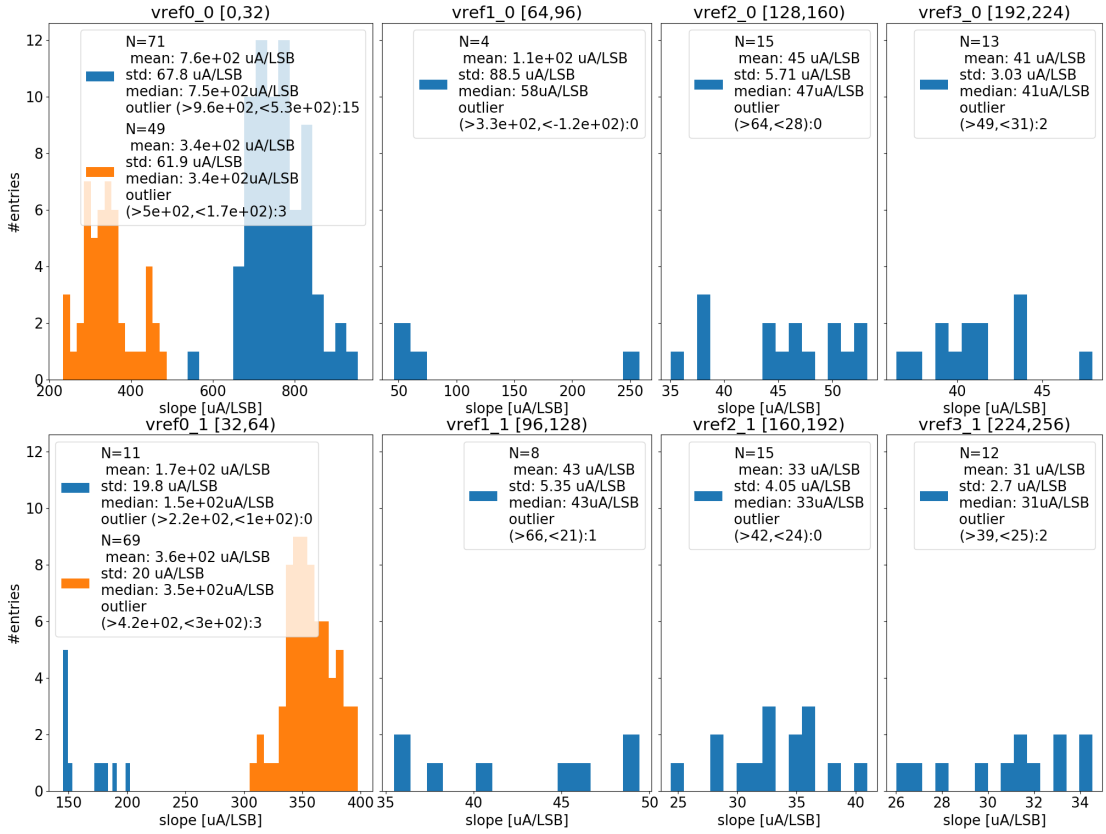


FIGURE 6.16: Current calibration results for LG RX with $R_{\text{shunt}} = 100\,\Omega$. Only sub vref range fits done, whereas the suffix "_0" ("_1") marks the fit to the lower (upper) 32 bit in the vref region. Those vref regions above 64 are from LG with "high gain LG". The orange histogram content displays results for currents below $\approx -12\,\text{mA}$.

conducting and the gain changes. The MG range has been by configured to use the PGA in a damping setting in order to increase the current which is covered by the MG to avoid the first region of the LG. The distribution of the LG results is given in Fig. 6.16. The number of fits in the regions vref1_0 and vref1_1 is so low, because data around the region where the ESD diodes start conducting are excluded due to the non-linearity.

Limitations of the method

Comparing measurements with the two R_{shunt} values have shown that a systematic shift to lower gains is observed with $R_{\text{shunt}} = 100\,\Omega$ for the MG. This manifests in the lower MG region where data from measurements with $R_{\text{shunt}} = 2.7\,\text{k}\Omega$ are approximately 20 % higher than those with $R_{\text{shunt}} = 100\,\Omega$.

This behavior has been investigated further by using R_{shunt} values in the range from 0.1 kΩ to 5.6 kΩ for one board. Fig. 6.17a depicts the corresponding plot for the HG. The plotted values are restricted to $R_{\text{shunt}} > 1\,\text{k}\Omega$, because the number of points are not sufficient for the fits for lower values of R_{shunt}.

The corresponding plot for MG is shown in Fig. 6.17b. There are less points for the upper vref, since the absolute current is not high enough for the high resistor values to reach those regions.

Except for `vref0`, both plots show increasing gain values with the increase of the vref number (for a fixed resistor value). The calculation of the gain is based on the current measurement and the measurement from VULCAN. The current measurement does not show a non-linear behavior[2], but the non-linearity clearly is measured within VULCAN. A non-linearity especially in the HG has already been observed in previous measurements (cf. [62]). Still, it is not clear what the actual source of the non-linearity is. But the distribution of the vref values which show a non-linearity in combination with these measurements hint towards VULCAN as one possible source.

Furthermore, Fig. 6.17b and Fig. 6.17a show a clear trend to lower gains for increase in resistance. For `vref0` there is a minimum gain around 1 kΩ. Here the impedance mismatch of the signal generator output to the RoB input impedance might play a larger role.

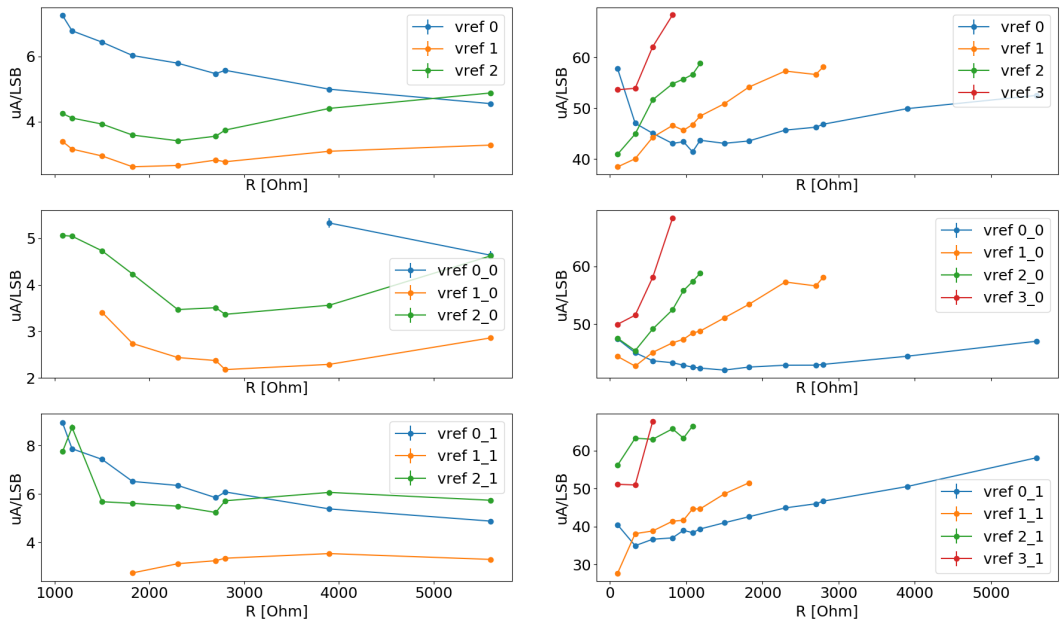
Deviating LG gain

During the current calibration, 15 of 95 VULCANs have shown a significantly higher gain for the LG RX. An example comparison between a "normal" and "high gain" LG is shown in Fig. 6.18.

VULCANs with "high gain" LG show in general a non-linearity and a reduced gain, which is typically in the order of the MG gain (30 µA/LSB to 50 µA/LSB. It was not possible to find an explanation or a workaround for this behavior.

As a consequence, information for very high p.e. number, corresponding to currents of $\sim -20\,\text{mA}$ and lower are missing. The exact waveform shape can not be recorded due to the limited range. Other methods like a time over threshold or fitting with a pulse model may still help to extract relevant information. The plots reveal another aspects of the LG behavior. The baseline level drops to zero after these pulses.

[2] similar to the current in Fig. 6.12b, the slope change occurs for currents outside of the MG range (lower than $\sim -12\,\text{mA}$).



(a) (b)

FIGURE 6.17: Measurements with multiple resistor values for HG (a) and MG (b). Errors bars are drawn, but smaller then the marker size. Fits for `vref0_0` are missing, since there are often not enough points above the baseline. This is less prominent in (b) due to a lower baseline for the MG. `vref3` is not plotted due to an oscillation structure for this specific stack.

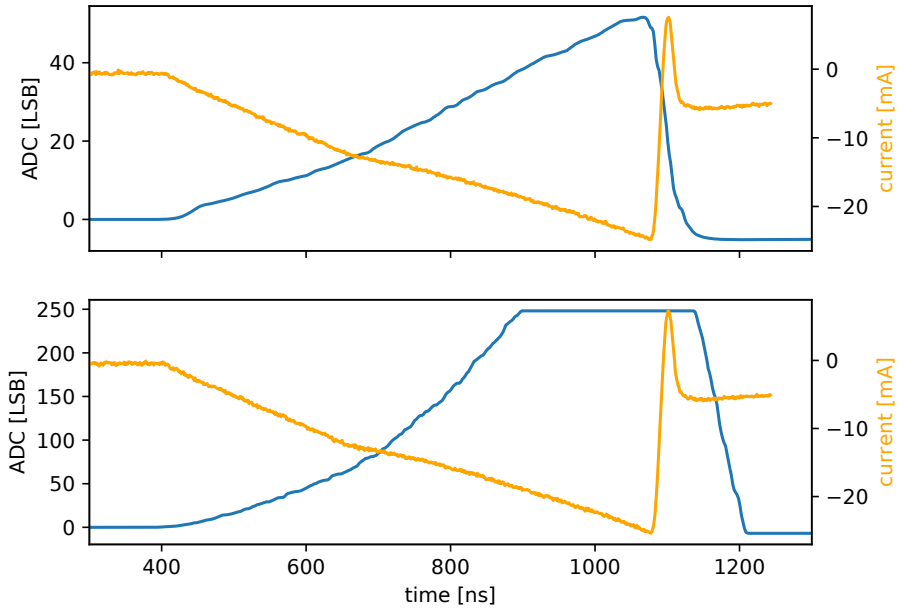


FIGURE 6.18: Comparison of a "normal" (upper plot) and "high gain" (lower plot) LG RX. Drawn in blue is the averaged and baseline corrected waveform from VULCAN. Drawn in orange is the input current, which corresponds to the current shown in Fig. 6.12b.

This undershoot phenomenon is a generally known behavior which relates among other factors to the discharge of the coupling capacitor [64].

6.5.1 Input-referred noise

The measurements which have been recorded in the context of the absolute current calibration are also used to determine the noise levels with DC input signal (also known as input-referred noise). A noise free code resolution (NFCR) similar to the definition in [91] can be calculated with:

$$\mathrm{NFCR} = \log_2 \frac{2^{N_{\mathrm{bits}}}}{\max(N_{\mathrm{p2p}}, 1)} \tag{6.9}$$

$$N_{\mathrm{p2p}} = 6.6\sigma_S \tag{6.10}$$

with the number of bits $N_{\mathrm{bits}} = 8$ and the peak to peak inputs noise (N_{p2p}) based on the standard deviation of the noise sample distribution σ_S. The noise sample distribution is taken from the baseline region in front of the signal generator pulses which were used for the current calibration. The $\max(N_{\mathrm{p2p}}, 1)$ function is used to limit the maximum NFCR to 8 bit. Especially for the LG, the noise level can be low and the resulting N_{p2p} is below 1 LSB.

Fig. 6.19 shows the calculated input referred noise for the three RX. Some measurements are excluded due to too low baseline settings, which is especially prominent for the LG RX due to the low target baseline of 5 LSB. The HG RX shows the lowest average number of noise free bits. MG and LG show average higher number of noise free bits, but also a larger variation.

The NFCR is measured here only for a single baseline settings for each VULCAN. Thus, this measurement can be heavily influenced by the behavior of individual bits, which may be close to their switching threshold and thus switching very often[3]. Furthermore, these measures do not take into account "dynamic" noise e.g., due to clock jitter and other factors and is not to be confused with **E**ffective **N**umber **O**f **B**its (ENOB) [91].

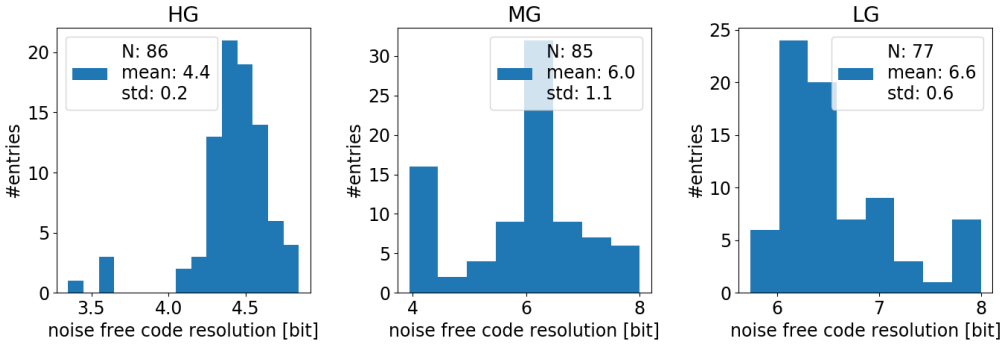


FIGURE 6.19: Noise free code resolution of the three RX.

[3]This behavior may be actually desirable to gain resolution by averaging [91].

6.5.2 Range, gain ratio and precision

Based on the current calibration results, closely related properties are calculated. The plots are restricted to those setups which are later used in an iPMT for OSIRIS. The total range in mA is calculated based on the results for the subrange vref gains. For ranges which do not have a valid fit, the value from the closest available region is taken. This applies especially for the LG, where for most iPMTs no data are available for currents below $\approx -25\,\mathrm{mA}$. Data from the range 32 LSB to 64 LSB are used for the extrapolation in those cases. A possible non-linearity of regions above $\sim$64 LSB are therefore not taken into account in this estimates.

The actual usable range of an RX is reduced by the settings for the baseline and switching threshold. Table 6.2 lists the assumptions which are used here for the calculation.

By dividing the respective reduced ranges, the gain ratios between the RX are calculated and plotted in Fig. 6.20. For the LG/MG ratio, those boards with a "high gain" LG cause the left part of the distribution with a ratio in the range from 2 to 4. The design values of VULCAN are given in Table 4.4 for comparison. For both ratios, the measured values are distributed around the design value ratio of 10, when the "low gain" LG are excluded.

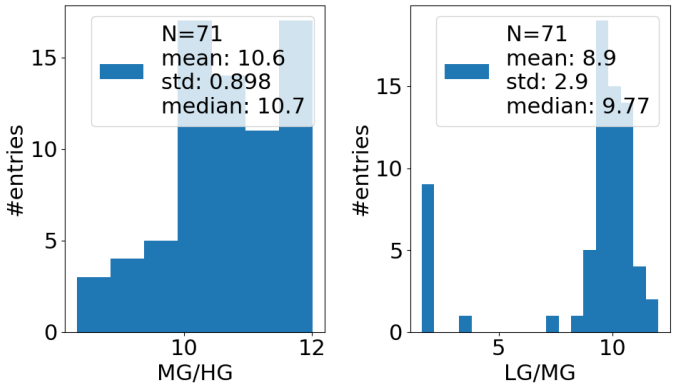


FIGURE 6.20: Gain ratio calculation based on the range of the RX.

Using a fixed conversion factor of $120\,\mu\mathrm{A\,p.e.}^{-1}$, which is based on a single p.e. amplitude of 6 mV over 50 Ω, the range of the RX in p.e. is estimated (a comparison with range estimates based on measured single p.e. amplitudes is given in Fig. 7.8). Fig. 6.21 shows the respective plots. Especially the values for the LG are only an estimate, due to not-determined non-linearities. Those VULCANs with a "high gain" LG have shown a non-linearity, but it is not clear if this effect is also present for the other LG. Furthermore, the PMTs itself are known to deviate from linear behavior for large pulses [41]. Fig. 6.22 shows the calculation of the noise levels expressed in p.e. for each RX.

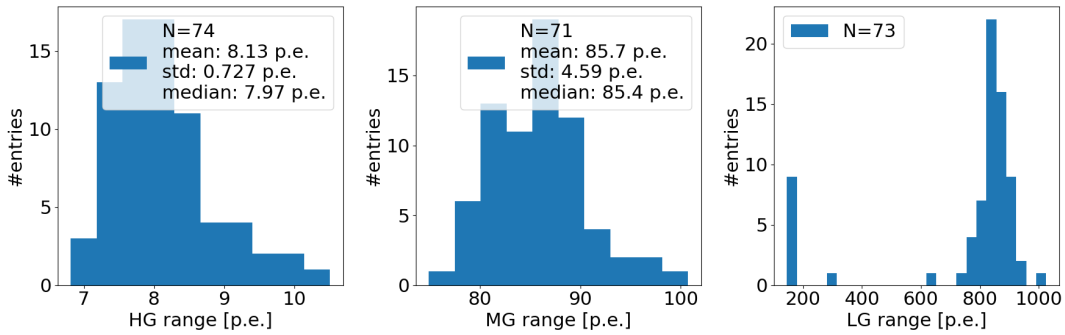


FIGURE 6.21: RX ranges in p.e. Two iPMTs are excluded in the MG due to invalid fits.

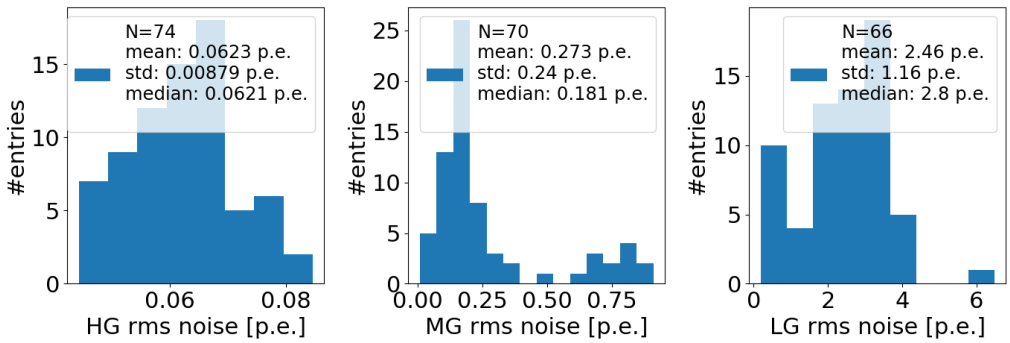


FIGURE 6.22: RMS noise (precision) in p.e. with a single p.e. amplitude of 120 µA and a LSB to current conversion based on the mean gain for the respective RX based on all subregion vref fits (for HG and MG). For LG, the subregion fit results for low absolute currents are used (i.e. when the ESD diodes are not conducting).

6.6 Readout transfer capability

To validate the readout capability of the system, a dedicated measurement is performed.

Setup An electronics halfstack is connected with an approx. 24 m long cable with a SB and further with a 2 m cable to a PoE switch. The cable length setup resembles the situation within OSIRIS for the iPMTs with the longest cables. A signal generator is directly connected to the VULCAN input and configured to provide a short pulse. The period between pulses is adjusted to simulate different event rate situations. The iPMT halfstack operates in the self-triggered mode, resulting in a single recorded packet per signal generator pulse. Each packet corresponds to a time window of 240 ns, which is subsequently sent to a readout instance.

Measurement procedure Pulse generator frequencies in the range from 1 kHz to 71 kHz with a step size of 5 kHz are chosen and data are recorded for each frequency for 60 s.

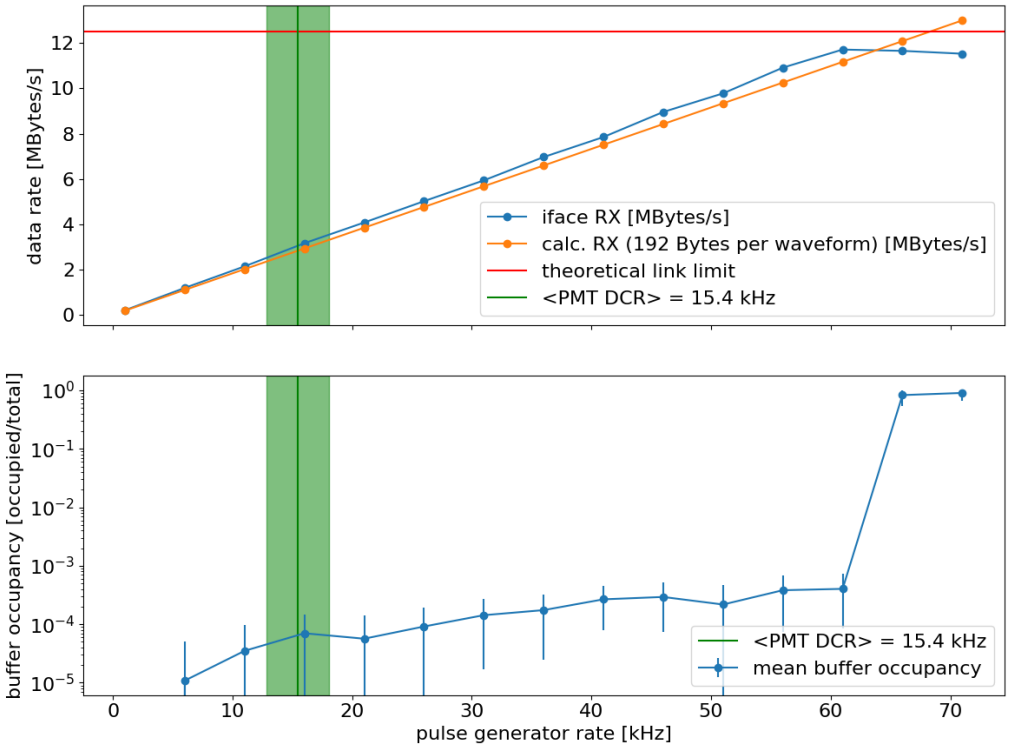


FIGURE 6.23: Upper plot: data rates of the connection to the iPMT. The line "iface RX" depicts the received data rate on the network interface of the readout computer. The theoretical limit is based on the link speed of 100 Mbit s^{-1}, corresponding to 12.5 MBytes/s. Lower plot: occupancy of the waveform buffer on the iPMT. For the signal rate of 1 kHz, the processing of the waveform is sufficiently fast, that the data are directly sent out, which results in a buffer occupancy of 0 (missing data point for 1 kHz). In both parts: plotted with a green solid line is the mean DCR of the PMTs for OSIRIS with the standard deviation drawn as shaded region.

Results Fig. 6.23 depicts the measured transfer rates from the iPMT to the readout computer as well as the buffer status on the iPMT. As soon as the buffer status starts to fill up significantly, event loss is unavoidable sooner or later. Relevant fill up starts in the frequency range between 61 kHz and 65 kHz. The expected data rate is calculated by $r(f_{\text{gen}}) = f_{\text{gen}} \cdot s_{\text{packet}}$ with the frequency of the pulses f_{gen} and the size of a data packet $s_{\text{packet}} = 192\,\text{Byte}$ (the packet protocol is given in Appendix B). One reason for the divergence of the receive rate of the interface and the calculated receive rate is the TCP protocol overhead. A (small) constant offset is additionally introduced by sensor readout on the SCCU (which will also be present in the later experiment).

The readout rate of the iPMTs has to suffice the expected hit rate within OSIRIS. This rate is dominated by the DCR of the PMTs (cf. Fig. A.1a for a distribution of the DCR). Additionally, larger signals, like those originating from muons may require a prolongation of the readout window. With a muon rate of 0.38 Hz for the OSIRIS detector [33, p. 18] the contribution to the trigger rate is on sub-percent level compared to the DCR, even if the readout window is several times longer (which are effectively multiple triggers). With a maximum stable readout rate of ≈60 kHz the iPMT supports continuous rates up to three times the DCR for most PMTs.

Also the receiving end has to cope with the readout rate. Therefore, the OSIRIS event builder has been tested to support data rates more than twice the measured DCR for all PMTs simultaneously [33, p. 16].

6.7 Synchronous link and synchronization verification

This section covers measurements for the timing system and synchronization of the iPMTs (cf. Section 4.6). In order to ensure a stable operation, the reliable transmission of the sync data stream to the iPMTs is of foremost importance. Therefore, **B**it **E**rror **R**ate (BER) measurements are conducted as explained in the following paragraphs.

Bit error rate estimation

The target of the measurement is the verification of the link quality, i.e. the integrity of the transferred data. A measure for the integrity is the so-called **B**it **E**rror **R**ate (BER) (or Ratio) [65]. It can be defined as the number of incorrectly transmitted bits, n_e, over the total number of bits, n:

$$\text{BER} = \frac{n_e}{n}.$$

Incorrectly transmitted bits are those which are sent as zero (one), but falsely recorded as one (zero).

The probability of a number of bit errors (and thus a BER) can be estimated to a certain confidence level by measuring the number of bit errors. This is expressed by

$$\text{CL} = P(P(e) < \alpha | n_e, n) \tag{6.11}$$

with the confidence level CL, the true BER $P(e)$ and a hypothesis for the BER, α. The probability of n_e wrong bits for n transmitted bits can be described with a binomial distribution

$$P(n_e) = \binom{n}{n_e} p^{n_e} (1-p)^{n-n_e} \tag{6.12}$$

with the probability of an error p.

Based on Eq. (6.11) and Eq. (6.12) the following equation can be deduced [65]:

$$n = -\frac{\ln(1-\mathrm{CL})}{p} + \frac{\ln\left(\sum_{k=0}^{n_e} \frac{(np)^k}{k!}\right)}{p}. \tag{6.13}$$

It relates the total number of bits which need to be transferred for a certain number of bit errors for a given confidence level and BER. The hypothesis for the BER is used for p.

Eq. (6.13) can be used to answer the two following questions:

1. How many bits need to be transferred for a given hypothesis of the BER, assuming a low number of number of errors. Answering this question helps in planning the measurements with regard to the required test time.
2. For a given measurement either an estimate of the BER for a target confidence level or an estimate of the confidence level for a target BER can be calculated.

Example In this example it is assumed that a confidence level of CL = 90 % for a BER = $p = 10^{-12}$ should be reached, while no error is detected. Especially latter assumption simplifies Eq. (6.13) significantly. With the given assumptions Eq. (6.13) results in a number of transmitted bits of

$$n = -\frac{\ln(1-\mathrm{CL})}{\mathrm{BER}} \approx 2.30 \cdot 10^{12}.$$

With a bit rate of 125 Mbit s^{-1} this corresponds to a measurement time of ≈5.12 h.

Application for the iPMT uplink The sync data stream from the SB to the iPMTs has a bit rate of 125 Mbit s^{-1}, while the symbol rate is 62.5 Mbit s^{-1} due to the manchester encoding. An occupancy of the link can be calculated as ratio of the symbol rate used by the protocol to the link symbol rate (the description of the protocol is given in Section 5.4.2). 5 bit are required to transmit a LED/Laser trigger and 37 bit are used for the transmission of a timestamp. For a scenario with a trigger rate of 10 kHz for the Laser[4]), this results in 50 037 bit s^{-1}. The corresponding link occupancy is 50 037 bit s^{-1} / 62.5 Mbit s^{-1} $\approx 8.0 \cdot 10^{-4}$. Thus, the probability that single errors coincide with a data transmission is rather low.

Testing procedure

The calculation of the bit error rate as described before requires the knowledge of the transferred stream on the receiver side. Therefore, a **P**seudo **R**andom **B**inary **S**equence (PRBS), generated by an IP-Core within the FPGA is used (cf. Section 5.2.10). Once the receiver side has synchronized to the stream, the following bitstream can be calculated and it is possible to determine wrong bits. The synchronization itself is only reasonably possible when the stream has a low error rate. Fig. 6.24 depicts the general setup for one iPMT connected with a SB (the sending unit is denoted as PRBS TX and the receiving unit as PRBS RX). The iPMT system allows for three different measurement schemes:

[4] A rate of 10 kHz was assumed to estimate the time for a charge calibration run in [33, p. 13].

1. Using the SB as sender and evaluating the received bits directly on the iPMT.
2. Using the iPMT as sender and the SB as receiver. This requires the sync data stream on the iPMT downlink in order to have the iPMT running on the same clock as the SB.
3. Using the SB as sender and as receiver. The iPMT forwards the received data stream directly back.

Results of PRBS tests are reported as part of the production tests in Section 7.3.2.

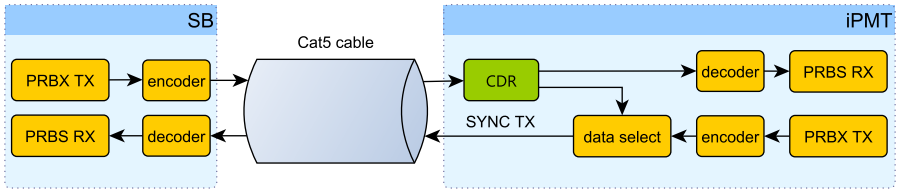


FIGURE 6.24: Simplified diagram of the connection of a single iPMT with a SB for bit error rate measurements with PRBS data streams.

6.7.1 Synchronization test

Based on a stable link, which has proven to show a reliable operation, a verification of the timing system of the iPMT system is performed. The basic idea behind this test is the simulation of events with a single source which is independent from the iPMT system and record the data with two iPMT halfstacks.

Test setup description The setup for this test is depicted in Fig. 6.25. Two iPMT electronics halfstacks are connected to a SB for the reception of the sync data stream and to a switch for the data transmission to the DAQ. Instead of using a PMT as signal source, a pulse generator (*Tektronix AFG3021B*) is connected to the respective VULCAN input on the iPMT stacks. This has the advantage that additional sources of timing uncertainty as the TTS of the PMT or the time stability of a light source do not have to be taken into account.

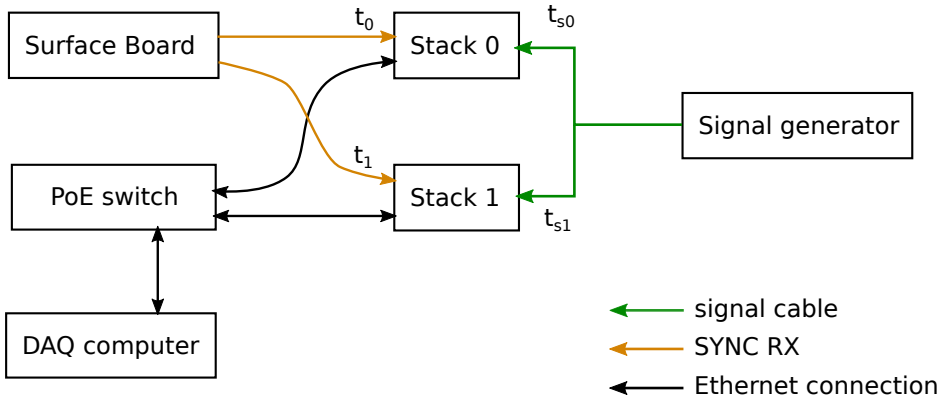


FIGURE 6.25: Setup for synchronization test with two iPMT halfstacks.

Measurement settings The pulse generator is configured to produce pulses with an amplitude roughly saturating the HG range of VULCAN and a frequency of 200 Hz. The measurement time sum ups to 12 h divided into 6 times 2 h.

When starting the measurement, the initial timestamps are transferred to both iPMTs via the synchronous link. Due to differences in the transmission line lengths, dominated by different CAT5 cable lengths, the timestamps are processed at different times. Thus, signals from the pulse generator digitized at the same time, are tagged with different timestamps. This difference is denoted as ΔT_0

$$\Delta T_0 = t_1 - t_0 \tag{6.14}$$

with synchronous signal transmission times for the respective iPMTs, t_0 and t_1.

In this setup also the analog signal connection from the signal generator to the analog input of VULCAN is not matched in length. The respective signal propagation times are denoted here as t_{s0} and t_{s1}. Thus, the measured time difference ΔT can be expressed as

$$\Delta T = \Delta T_0 + t_{s1} - t_{s0}. \tag{6.15}$$

Analysis The iPMTs are configured to trigger at a fixed threshold of 100 LSB. For each pair of triggered waveforms the time difference in nanoseconds is calculated

$$\Delta T = T_{sec,1} \cdot 10^9 + T_{nano,1} - T_{sec,0} \cdot 10^9 + T_{nano,0} \tag{6.16}$$

with the timestamp parts with a resolution of seconds $T_{sec,0}$, $T_{sec,1}$ and the nanosecond timestamp parts $T_{nano,0}$, $T_{nano,1}$ with a resolution of 2 ns. Fig. 6.26 shows these time differences over the measurement time. The projection of this measurement to the y-axis is given in Fig. 6.27.

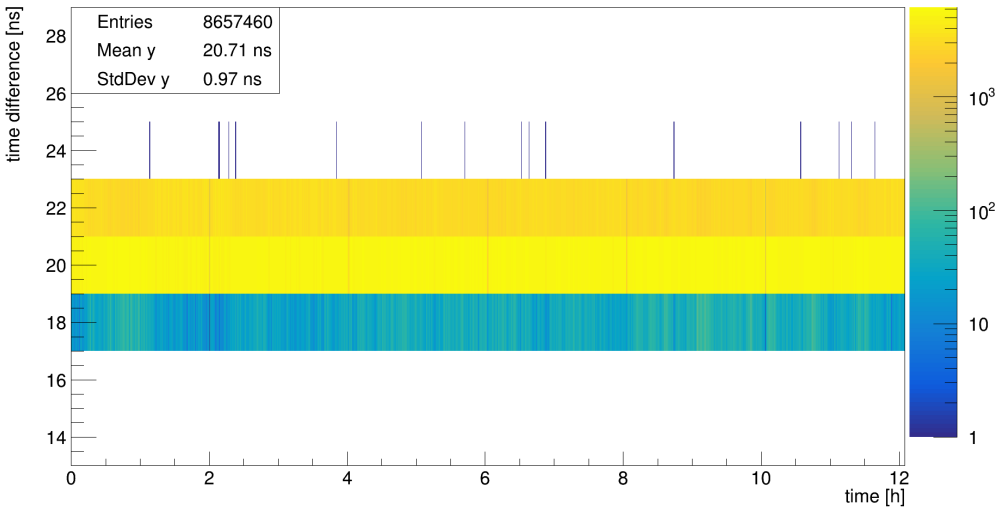


FIGURE 6.26: Distribution of the time differences versus the time. The splitting into 2 h chunks is visible by the lower number of entries especially for the time difference bin for 20 ns.

The trigger time can be determined more precisely when taking the actual waveform data into account. A linear interpolation is performed, taking into account two

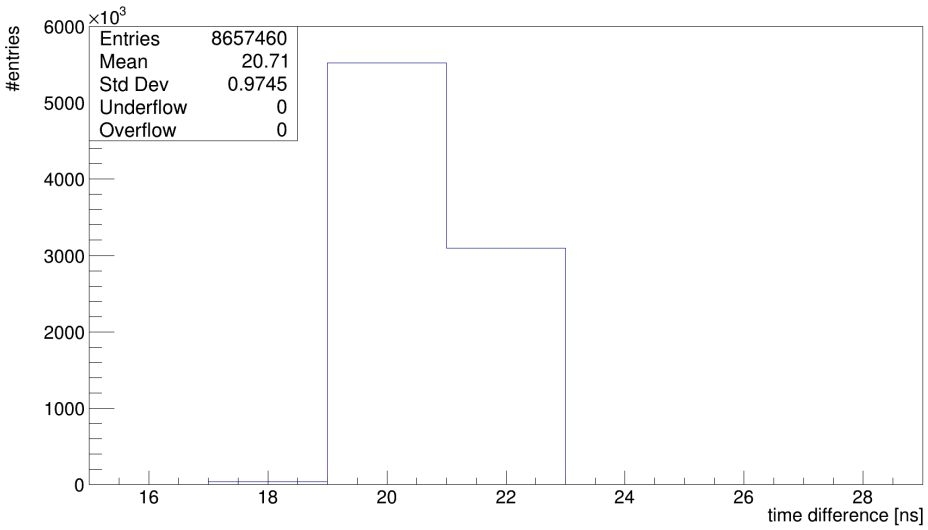


FIGURE 6.27: Distribution of timestamp differences of two iPMT electronics stacks with a timestamp resolution of 2 ns.

data points before and after the first sample equal or greater to the trigger threshold of 100 LSB. An exemplary waveform is shown in Fig. 6.28.

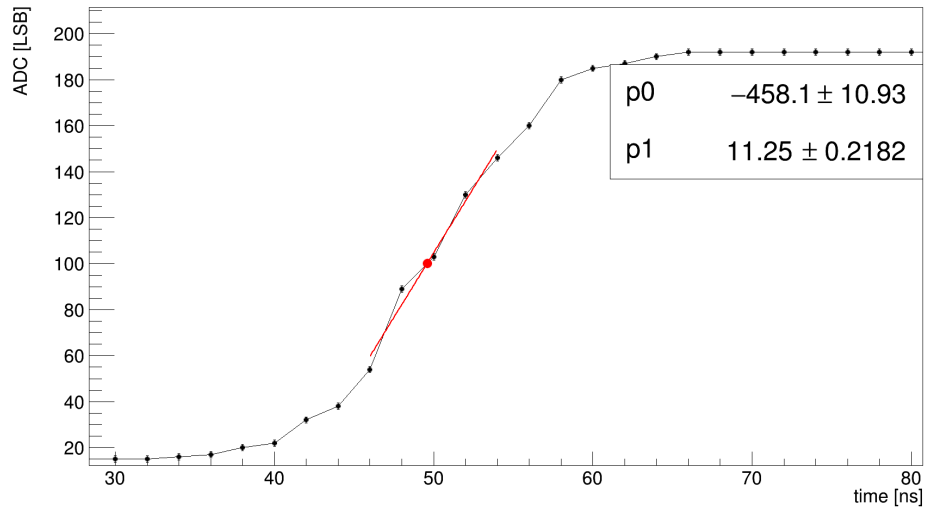


FIGURE 6.28: Exemplary waveform with a linear interpolation.

The same dataset as shown in Fig. 6.27 with applying the linear interpolation is depicted in Fig. 6.29.

Both Figs. 6.27 and 6.29 show that the timestamp difference is stable and limited. The actual value of the absolute time difference is not important and depends on the chosen cable length for the setups. The mean TTS of the PMTs which are used within OSIRIS is 2.6 ns (FWHM, cf. Fig. A.1b). Under the assumption of a gaussian distribution corresponds this to a standard deviation of $\sigma_{\mathrm{TTS}} = 2.6\,\mathrm{ns}/(2\sqrt{2\ln 2}) \approx 1.1\,\mathrm{ns}$. The

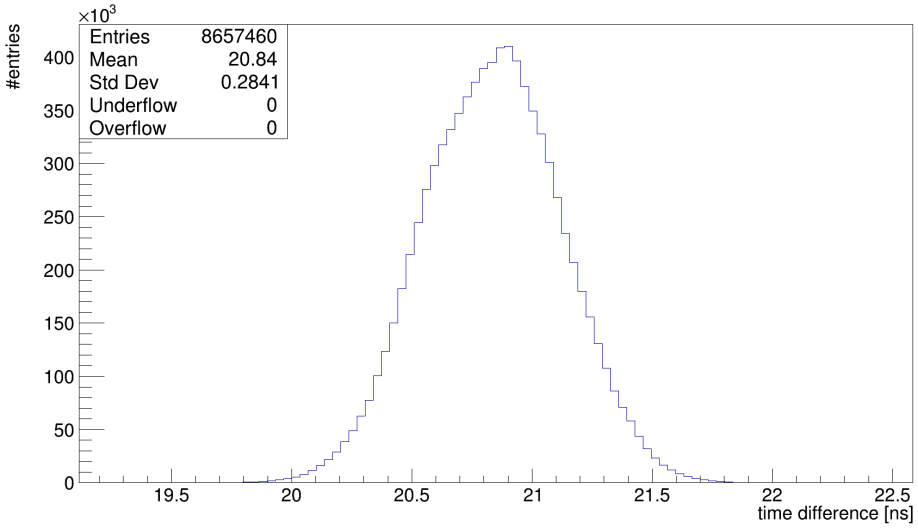


FIGURE 6.29: Distribution of the timestamp difference with interpolation of the trigger time based on the waveforms.

standard deviation of the interpolated timestamp distribution is 0.28 ns $\approx 0.25\sigma_{\text{TTS}}$. Thus, the TTS of the PMT itself is the dominant source of timing uncertainty.

The jitter of the measurement setup itself can be estimated based on the noise level and rising edge slope. It can be calculated with

$$\sigma_{\text{time}} = \frac{\sigma_{\text{noise}}}{\left|\frac{dV}{dt}\right|} \tag{6.17}$$

with the noise and statistical fluctuations σ_{noise} and the signal slope $|\frac{dV}{dt}|$ [40, p. 318]. σ_{noise} is estimated by the standard deviation of the sample distribution of the first ten samples of every waveform for one 2 h dataset for each stack. $\left|\frac{dV}{dt}\right|$ is extracted from the mean value of all linear interpolations of the rising edge.

TABLE 6.4: Timing properties of both stacks. The calc. jitter is computed using the mean signal slope as $\frac{dV}{dt}$ and the σ_{noise} for Eq. (6.17).

	mean signal slope [LSB/ns]	σ_{noise} [LSB]	calc. jitter [ns]
stack 0	10.46 ± 0.84	1.3814 ± 0.0003	0.13 ± 0.01
stack 1	13.24 ± 0.56	1.7508 ± 0.0003	0.14 ± 0.01

Table 6.4 summarizes the timing properties which are extracted from the datasets for both stacks. The combined time jitter is calculated from the quadratic addition of the individual jitter to (0.19 ± 0.01) ns. This shows that the interpolated time difference of 0.28 ns is close to the level of what can be expected from the setup.

In order to improve on the time jitter of the setup, it becomes clear from Eq. (6.17) that there are two options. One possibility is a faster rising edge, but the minimum leading edge time of 18 ns of the signal generator is already used and would thus

require different equipment. The second factor, σ_{noise}, can not be changed but using the MG or LG receiver, which feature an intrinsic lower noise, would be a possibility.

Another effect which typically needs to be considered is the time walk. It is a signal dependent shift of the trigger time caused by variations of the amplitude or the rise time [40, p. 317]. It is not relevant here, since the amplitude and rise time of the pulses generated by the pulse generator are sufficiently stable.

Crosscheck measurements

Two crosscheck measurements have been performed to check the system behavior with different settings. For one crosscheck, an additional CAT5 cable with a length of 20 m was added in the path of stack 1 (increasing t_1). The corresponding distribution of the interpolated timestamps is given in Fig. E.2. With a propagation delay of $\approx 5\,\text{ns}\,\text{m}^{-1}$ for twisted pair cables [66, p. 11], and a length of the added cable of 20 m, the expected shift in the time difference is about 100 ns. Based on the measurements with interpolated trigger times, the measured time difference is $20.84\,\text{ns} - (-74.15\,\text{ns}) = 94.99\,\text{ns}$. The 5 ns difference can be explained by a not exactly measured cable length and a slightly different propagation delay.

For another crosscheck measurement, the respective local reference clock is used for each iPMT. Both oscillators on each stack have the same nominal frequency of 125 MHz, but the actual frequency differs by a few parts per million [92], leading to a relevant time difference within seconds. The measured time drift is depicted in Fig. E.1 where the time difference evolution is plotted against the measurement time. A linear drift is expected and observed.

6.8 iPMT evaluation with a PMT

Previous sections covered characterizing measurements without PMT. This section presents measurements based on a fully assembled iPMT, as it is shown in Fig. 6.30.

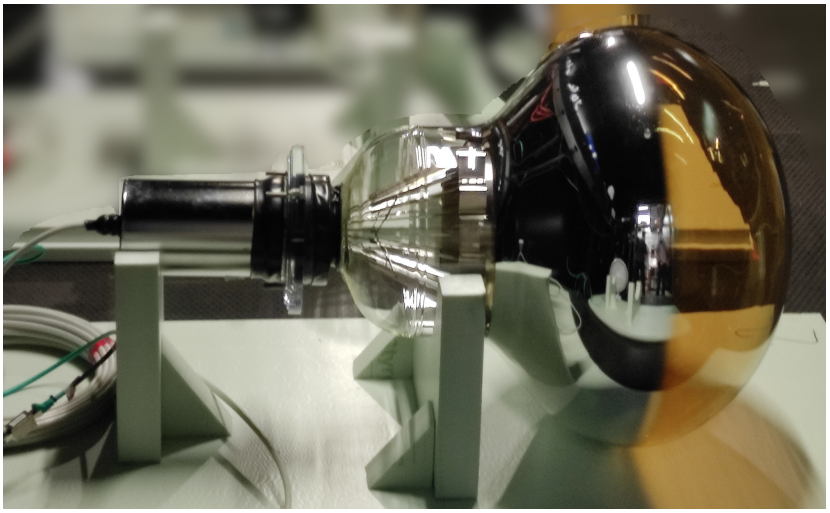


FIGURE 6.30: Assembled iPMT in preparation for testing without magnetic shielding (cf. Fig. 4.2 for a drawing of the iPMT for comparison).

Setup The iPMT is located in a box which is lined with FINEMET[5] sheets for magnetic shielding (not shown in Fig. 6.30). An LED pulser is placed within the box to illuminate the PMT. The trigger input of the pulser is connected to a SB trigger output. This allows to use the synchronous link trigger on the iPMT to synchronize the readout with the LED pulses.

Configuration The high voltage is set to the voltage measured from *Hamamatsu* which corresponds to a gain of 1×10^7. Events are recorded with a low light intensity in order to have only a very low number of more than 1 p.e. Approximately 5 % of the triggered waveforms contain a single p.e.

6.8.1 Charge spectrum

For every recorded waveform its baseline corrected charge is calculated with the baseline b defined as

$$b = \frac{1}{N_{\mathrm{bl}}} \sum_{i=0}^{N_{\mathrm{bl}}-1} s_i. \tag{6.18}$$

The recorded waveform samples are denoted as vector $\mathbf{s}$, and the number of baseline samples $N_{\mathrm{bl}} = 20$. The baseline corrected charge is then calculated via

$$Q_{\mathrm{blc}} = \sum_{i=N_s}^{N_e-1} (s_i - b) \tag{6.19}$$

[5] FINEMET is a soft nanocrystalline magnetic material with a high permeability and a high saturation flux density.

with the start of the integration region N_s and the end of the integration region N_e. A visualization of the baseline and charge region is given in Fig. 6.31. A histogram of the baseline corrected charges (charge spectrum) for 100×10^3 triggered LED pulses is given in Fig. 6.32.

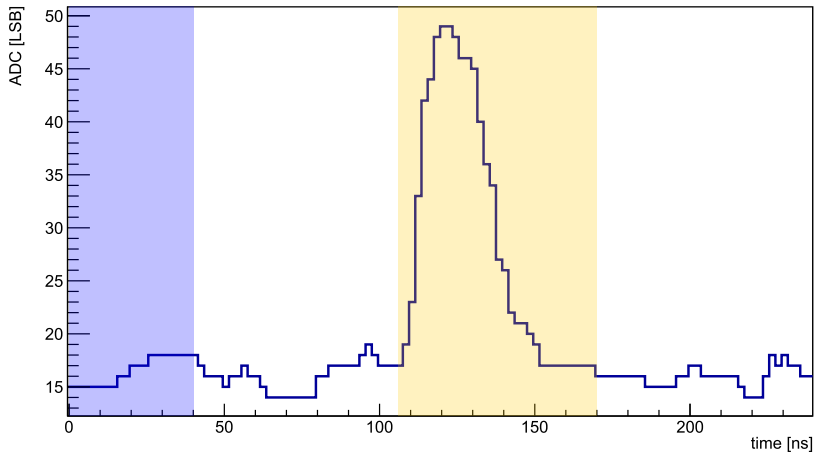


FIGURE 6.31: Exemplary waveform of a single photo electron event. The blue shaded area is the region which is used to determine the baseline value (time range 0 ns to 40 ns). The orange shaded region marks the charge integration region from 106 ns to 170 ns.

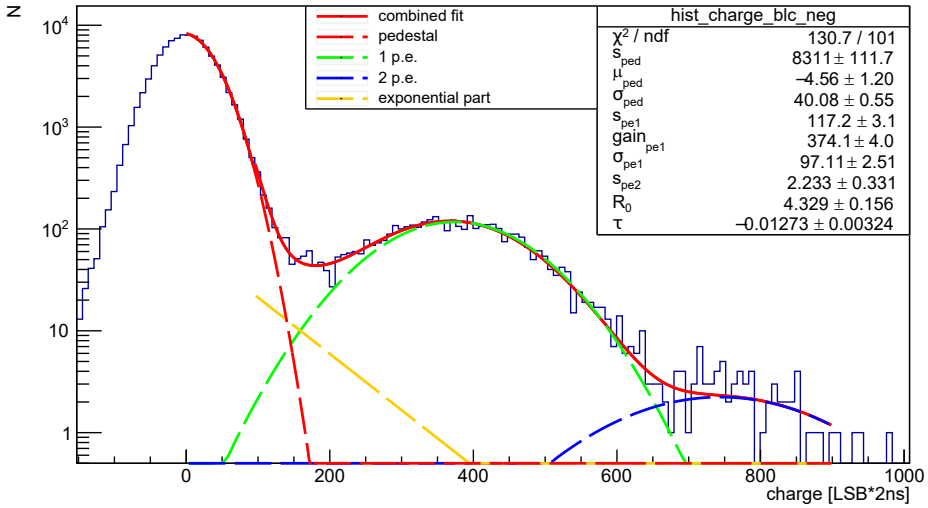


FIGURE 6.32: Exemplary baseline corrected charge spectrum with a low light level illumination. The fitted function is described in Eq. (6.20).

The charge spectrum can be described by a combination of multiple effects which are described in the following fit function f_{fit} (similar to [67]):

$$f_{\text{fit}}(x) = f_{\text{ped}}(x) + f_{\text{pe1}}(x) + f_{\text{pe2}}(x) + f_{\text{exp}}(x) \tag{6.20}$$

$$f_{\text{ped}}(x) = s_{\text{ped}} \cdot e^{-0.5\cdot((x-\mu_{\text{ped}})/\sigma_{\text{ped}})^2} \tag{6.21}$$

$$f_{\text{pe1}}(x) = s_{\text{pe1}} \cdot e^{-0.5\cdot((x-(\mu_{\text{ped}}+\text{gain}_{\text{pe1}}))/\sigma_{\text{pe1}})^2} \tag{6.22}$$

$$f_{\text{pe2}}(x) = s_{\text{pe2}} \cdot e^{-0.5\cdot((x-(\mu_{\text{ped}}+2\cdot\text{gain}_{\text{pe1}}))/(\sqrt{2}\sigma_{\text{pe1}}))^2} \tag{6.23}$$

$$f_{\text{exp}}(x) = \begin{cases} e^{R_0+\tau\cdot(x-x_v)} & \text{if } x > x_v \\ 0 & \text{otherwise} \end{cases}. \tag{6.24}$$

$f_{\text{ped}}(x)$ is a gaussian component to model the noise, also denoted as pedestal or noise peak. $f_{\text{pe1}}(x)$ and $f_{\text{pe2}}(x)$ are gaussian models as well to describe the charge signals corresponding to one, respective two p.e. Since the PMT is a linear amplifier for this low number of p.e., the respective gaussian mean values are correlated via the variables gain_{pe1} and σ_{pe1}.

$f_{\text{exp}}(x)$ is an empirical approach to include other effects into the model to better describe especially the region between pedestal peak and single p.e. peak. The variable x_v is the start point of this fit contribution and starts on the falling edge of the pedestal peak.

A number of characteristic properties can be calculated based on the charge spectrum. One of them is the peak-to-valley ratio (P/V) which describes the relation between the single p.e. peak height to the "valley" between the pedestal peak and the single p.e. peak. As position for the valley, the minimum value of the fitted function between single p.e. peak and pedestal peak is used. For the fit given in Fig. 6.32 the P/V is calculated to

$$\text{P/V} = \frac{119.7 \pm 3.1}{43.6 \pm 4.8} = 2.74 \pm 0.31. \tag{6.25}$$

The P/V which is reported for this PMT from *Hamamatsu* is 3.32 which is slightly better than the presented measurement.

As another characteristic property, the charge signal-to-noise level can be defined based on the charge spectrum as [68]:

$$\text{SNR} = \frac{\text{gain}_{\text{pe1}}}{\sigma_{\text{ped}}} \tag{6.26}$$

$$= \frac{2 \cdot (374.1 \pm 4.0)\,\text{ns LSB}}{2 \cdot (40.08 \pm 0.55)\,\text{ns LSB}} = 9.33 \pm 0.16. \tag{6.27}$$

The signal charge resolution can be calculated with

$$\frac{\sigma_{\text{pe1}}}{\text{gain}_{\text{pe1}}} = \frac{2 \cdot (97.1 \pm 2.5)\,\text{ns LSB}}{2 \cdot (374.1 \pm 4.0)\,\text{ns LSB}} = 0.2596 \pm 0.0072. \tag{6.28}$$

Comparing these measurements with [69, p. 183], where average results for the charge resolution of 0.274 ± 0.017, the P/V of 3.66 ± 0.52 and for the SNR of 13.62 ± 0.58 for the JUNO *Hamamatsu* PMTs are given, shows clearly a lower performance of the here presented measurements. Parts of the deviations may be explained by the relative high noise level in the HG RX (cf. Sections 6.5.1 and 6.5.2), affecting predominantly the SNR and the P/V, whereas the relative deviation in the charge resolution is less prominent.

Average waveform Section 6.8.1 shows an average waveform based on a charge cut of $\pm 1\sigma_{\text{pe1}}$ around the single p.e. charge. A clear sine wave with a frequency of 62.5 MHz is visible within the data before and after the pulse. The specific frequency hints towards the synchronous link as source for this artifact. Since the trigger is issued via this link, the data have a fixed phase relation to this signal and the sine wave signals cancel out only to a limited amount due to jitter of the trigger signal. With a peak-to-peak amplitude of the sine signal with about 0.7 LSB and an average signal amplitude of 28.3 LSB this is an effect in the order of 0.7 LSB/28.3 LSB $\approx$ 2.5 %. The peak-to-peak amplitude is probably underestimated due to the aforementioned trigger jitter, thus the effect might be more severe for single waveforms.

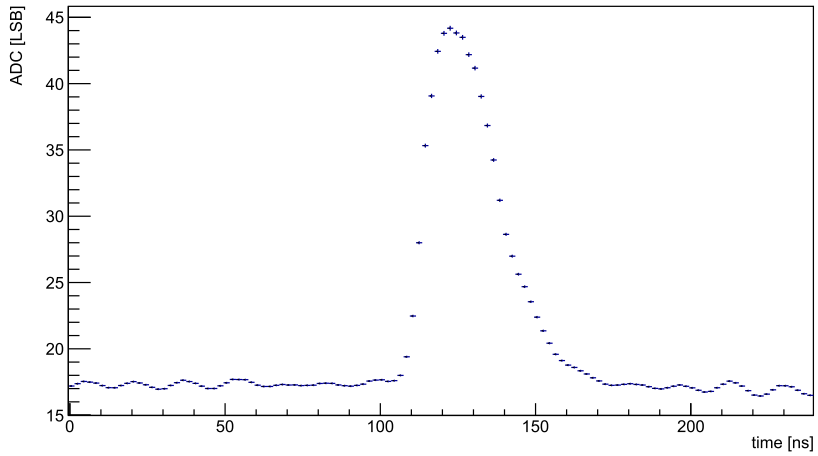


FIGURE 6.33: Averaged single p.e. waveform based on waveforms with a Q_{blc} in $[Q_{\text{pe1}} - \sigma_{\text{pe1}}, Q_{\text{pe1}} + \sigma_{\text{pe1}}]$ with $Q_{\text{pe1}} = \mu_{\text{ped}} + \text{gain}_{\text{pe1}}$.

Gain In order to calculate the gain, it is necessary to use the results from the current calibration. For the iPMT presented in this section, the current calibration result is $c = (3.18 \pm 0.13)\,\mu\text{A/LSB}$ for the lowest 6-bit ADC region (up to 64 LSB). With a fitted gain of $g = 2 \cdot (374.1 \pm 4.0)\,\text{ns LSB}$ this result into a gain G of

$$G = c \cdot g/e = (2.38 \pm 0.10)\,\text{pC}\,e^{-1} = (1.49 \pm 0.06) \times 10^7\,e\,e^{-1}. \tag{6.29}$$

This is 50 % higher than the expected gain of $1 \times 10^7\,e\,e^{-1}$. One possible explanation for the difference is that the current calibration is not an adequate replacement for the PMT.

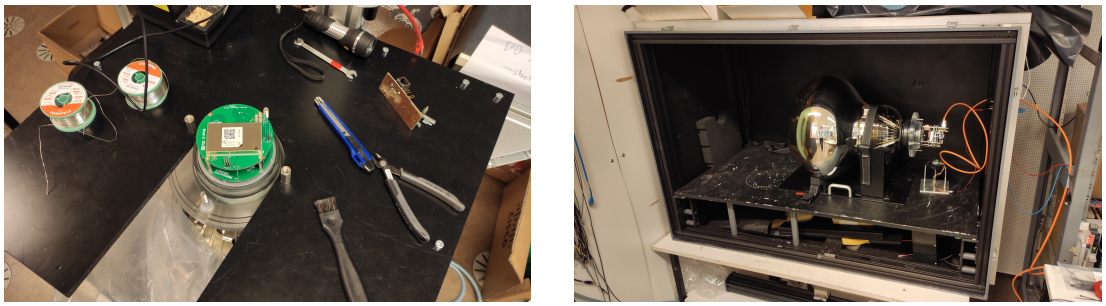
Another possible explanation is that the HV value from the vendor is recorded under different conditions. This can be e.g., a different base configuration. The vendor HV values for the PMTs were not checked for all PMTs.

Chapter 7

iPMT production

The assembly of an iPMT is a complicated process involving several steps to get from the bare PMT to an assembled iPMT. This includes especially several gluing steps, e.g., for attaching the PMMA ring (cf. Fig. 4.2) to the PMT neck. Gluing related assembly steps are described in more detail in [44]. In the following section the assembly of the iPMT electronics is described. Section 7.2 describes the tests which have been performed and Section 7.3 summarizes the test results.

7.1 iPMT electronics assembly



(a) (b)

FIGURE 7.1: (a) Image of an iPMT during the electronics assembly after soldering the Base and the HV module. (b) Partially assembled iPMT placed in a darkbox for a test of the PMT to VULCAN connection.

The assembly of the electronics has been predominantly done by Jochen Steinmann and myself. Following steps have been performed for each iPMT for mounting the electronics on a PMT:

1. Solder a Base on the PMT
2. Solder a HV board on top of the Base
3. Connect a tested and soldered electronics halfstack
4. Run a script to
   (a) assign the iPMT electronics to an PMT in a database
   (b) test the connection to the HV module
5. Solder pins between HV and RoB

6. Test the iPMT in a darkbox to
   (a) verify the functionality of the interfaces between boards
   (b) test the connection between VULCAN and the PMT
7. Solder the CAT5e cable to the SCCU
8. Test the iPMT with cable
   (a) Ethernet test by setting up the connection
   (b) Short PRBS test (10 s) to detect links with high BER or line swaps

After these assembly steps, the shell is glued to the PMT and filled with oil. A deformable bottle is glued into the shell to counteract the pressure increase when the oil expands due to heat induced by the electronics (cf. [44]).

7.2 Verification tests in the cooltainer

All iPMTs are tested before packaging and shipment. For testing several iPMTs in parallel, a large dark room is required. For this purpose, an isolated container with climate control ("cooltainer") is available.

The interior view of the cooltainer is given in Fig. 7.2. During the tests, the target temperature was set to about 17 °C and fans were used to provide an airflow over the shells.

Six temporary testing places are built on the floor of the cooltainer. Due to the connection from inside to outside of the cooltainer, the effective cable length is approx. 10 m longer than later in OSIRIS. Each testing place has an individual LED pulser for the illumination of the PMT.

Magnetic and electric shielding was not available for these tests. It is known that even relatively small magnetic fields as the earth magnetic field have relevant effects on the PMT properties [41, p. 252]. Therefore, these tests do not reflect the real performance of the iPMTs but are rather functional verification tests.

7.2.1 Parallel tests

Following two tests are typically run over night to give the PMTs time to "cooldown", i.e. to reduce the DCR to a normal level [41, p. 70]. These tests run in parallel for all iPMTs in one test batch. When a test was started before the weekend, longer measurement times of more than 2 days could occur over the weekend.

PRBS A PRBS test is performed with the SB as sender and receiver. This verifies both, the SYNC RX and the SYNC TX connection. This setup has been described as the third measurement scheme in Section 6.7.

DCR The development of the DCR is monitored by measuring the trigger counts for trigger levels from 0 LSB to 100 LSB with a switching interval of 2 s. In parallel, data are recorded via the VULCAN status registers. Since these data are randomly chosen, they represent most of the time the baseline value. This reduced readout is preferred over a readout of complete waveforms, since the

FIGURE 7.2: Testing places for the iPMTs in the cooltainer.

information are sufficient to monitor the DCR and the waveform readout of all iPMTs in parallel is not feasible with the available hardware[1].

7.2.2 Serial tests

The following tests are run in serial since most of them require the illumination of the PMT and illuminations for different PMTs should not interfere.

HV sweep Single p.e. spectra as shown in Fig. 6.32 are recorded for seven HV set points. HV values with a ΔV of $[-100, -50, -25, 0, 25, 50, 100]$ relative to the nominal HV setpoint for a gain of $1 \times 10^7\, e\, e^{-1}$ (as determined by *Hamamatsu*) are used. The synchronous link trigger is used to synchronize the readout with the LED trigger.

Self trigger threshold scan Datasets for several trigger thresholds which are in the range of about half the single p.e. amplitude are recorded self-triggered.

Self triggered large pulses A dataset with a trigger of 255 LSB is recorded. This records only data which have at least a part of the signal in the MG.

Large pulses with LED illumination Due to a low rate of very high amplitude signals, very large signals are generated with high LED pulser settings. The synchronous link trigger is used to synchronize the readout with the LED.

7.3 Test results

7.3.1 Electronics temperatures during cooltainer test

As part of the verification, also the operating temperature of the electronics is monitored. In contrast to the later use within OSIRIS when the iPMTs are emerged in water, they are air cooled. Therefore, it is expected that the measured temperatures are in general upper temperature limits, since the heat transfer from the shell is better to water than to air.

During these tests, only the horizontal orientation of the iPMTs is tested (cf. Fig. 7.2). Within OSIRIS up to 28 iPMTs are upward/downward facing, which has an effect on the temperature, due to the convection direction than being perpendicular to the electronic boards orientation.

Three temperature sensors are selected because the corresponding components are major heat sources:

1. The ZYNQ temperature is measured via an internal diode. The absolute maximum junction temperature rating is given as 125 °C and the recommended operating temperature range is −40 °C to 100 °C (industrial temperature range chip) [93].

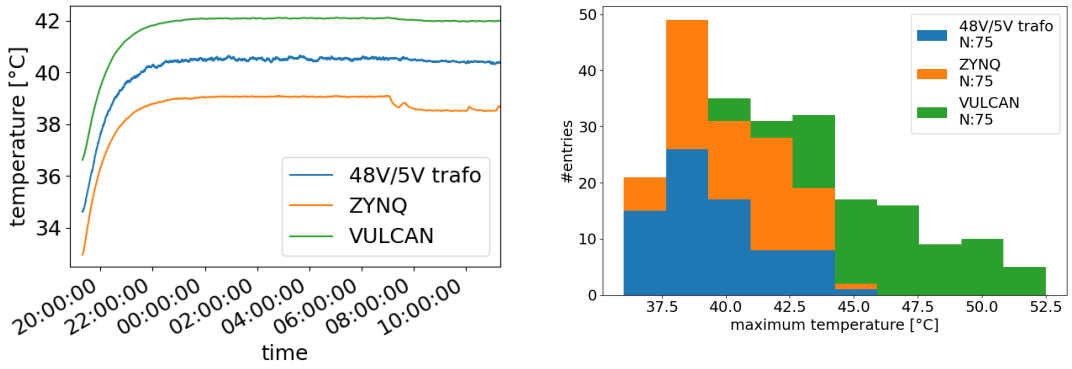
2. The VULCAN case temperature is measured via a temperature sensor in close contact to the case. VULCAN has been partially tested for a temperature of 80 °C [51] (the design target performance and functional temperature range is 0 °C to 85 °C and the functional temperature range −40 °C to 100 °C [98]).

[1] This includes limitations by the link speed which is limited to 60 kHz continuous trigger rate as well as lacking processing power (the EB was not usable for this task at this time).

3. The temperature of the transformer of the 48 V to 5 V DC/DC is measured by a sensor in contact to the transformer. The transformer has an operating temperature range of −40 °C to 125 °C [94].

Fig. 7.3a shows a typical temperature profile of the three selected sensors after starting an iPMT during the cooltainer test. The data storage started some time after power up, explaining the relatively high temperature at the beginning of the plotting. The temperatures change slightly over time (after 7:00 in the exemplary plot) due to different measurement programs.

Fig. 7.3b shows the maximum temperature reading of each of the three sensors for all tested iPMTs. The reported temperatures are all well within the operating temperature ranges reported above. Lower temperatures generally increase the reliability of the electronics and thus increase the lifetime of the system.



(a) Temperatures of central components of one iPMT during the cooltainer test.

(b) Stacked distributions of the maximum temperature for central components during the cooltainer test for all iPMTs.

FIGURE 7.3: Temperature monitoring data from the cooltainer test.

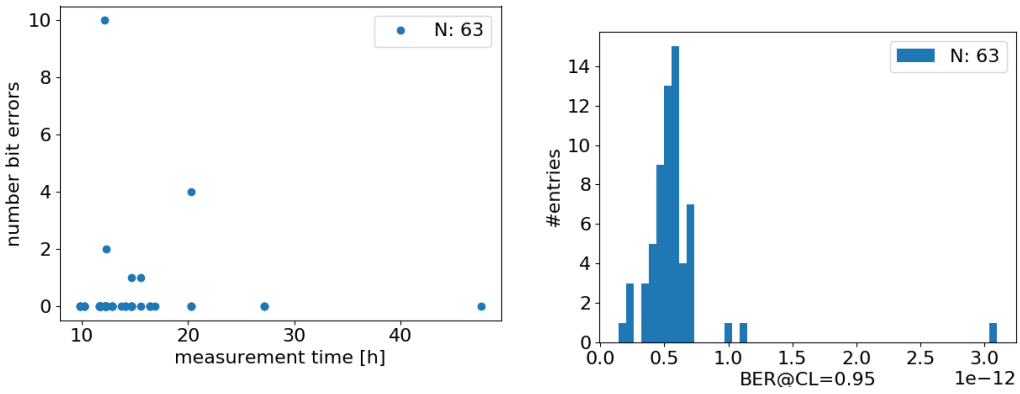
7.3.2 PRBS test

The PRBS test has shown that 63 iPMTs did not have any synchronization loss. A synchronization loss is defined here as more than 20 % bit errors within 127 bit. Fig. 7.4a depicts the number of bit errors for those iPMTs without synchronization loss. Most of them have not a single bit error, resulting in a BER $< 1 \times 10^{-12}$ for a confidence level of 95 % for most stacks (depending on the measurement time). For the 12 iPMTs with synchronization loss, the maximum time without loss ranges between 2.5 h and 45 h. The longer measurement times over the weekend are in general less prone to external noise.

The measurements have shown that the iPMTs are able to stay synchronized over hours to days, but are generally sensitive to external noise. Within OSIRIS the iPMT electronics will be supplied by an AC-DC-AC uninterruptible power supply (UPS) which should help to reduce external noise.

7.3.3 DCR

An exemplary dark current rate scan is shown in Fig. 7.5. With a typical single p.e. amplitude of 22 LSB, the threshold over the baseline of about 11 LSB corresponds to



(a) (b)

FIGURE 7.4: (a) Number of bit errors for those iPMTs without synchronization loss versus the measurement time. (b) Corresponding BER for a fixed confidence level of 95 %. The BER is calculated numerically based on Eq. (6.13).

0.5 p.e. A DCR of 12.8 kHz is reported for this PMT by *Hamamatsu*. The minimum measured DCR of about 15 kHz is slightly above this value, but the difference is within typical variations between recorded trigger rates for adjacent trigger thresholds. An increase in the DCR after 6:00 is visible due to a light leak, probably through the ventilation for the cooling system.

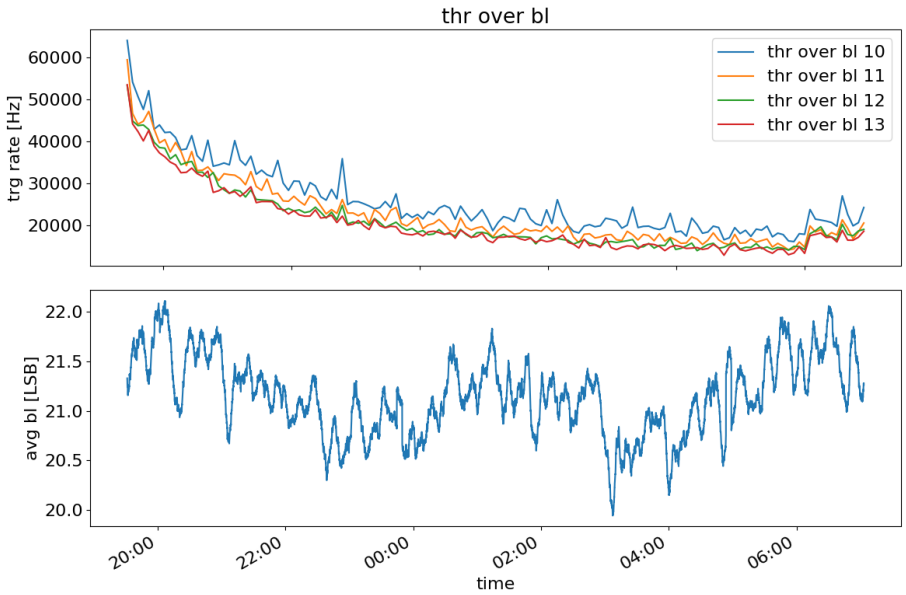


FIGURE 7.5: Trigger rates for different trigger thresholds over the baseline. A threshold of about 11 LSB corresponds to half a single p.e. amplitude for this iPMT. A moving average with 100 samples is applied for plotting the average baseline (lower plot).

7.3.4 HV sweep

The HV sweep is done with a low light level to record charge spectra with mostly single p.e. hits. Fig. 7.6 depicts an example of a high voltage sweep for one iPMT.

The exponential behavior of the amplification is clearly visible as a linear dependency in the logarithmic plot. Nonetheless shows the χ^2/ndf a slight mismatch between model and data, which can also be recognized in the residual graph. Factors leading to this mismatch may be an underestimation of the gain uncertainty and contributions of the second p.e. peak which are not correctly fitted.

A HV sweep measurement has been conducted for each iPMT and checked visually. The automatic fitting procedure failed occasionally for individual charge spectra, especially for low HV setpoints.

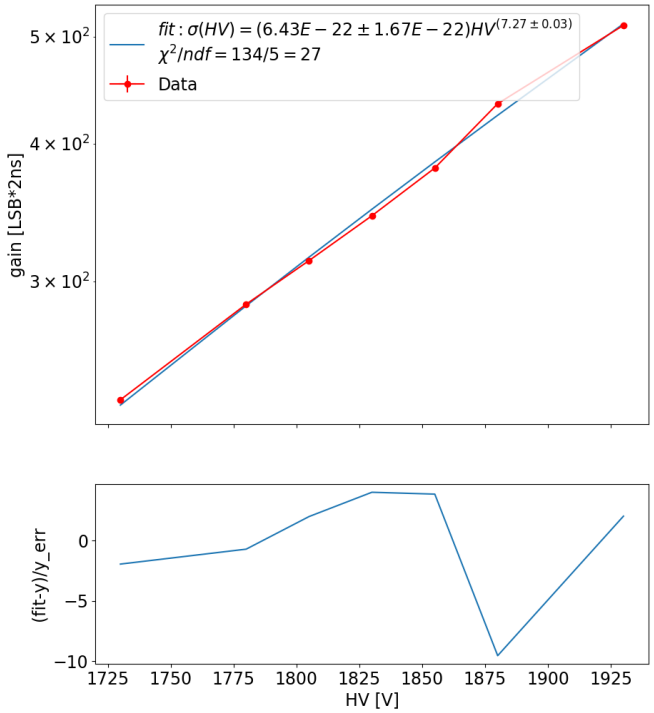


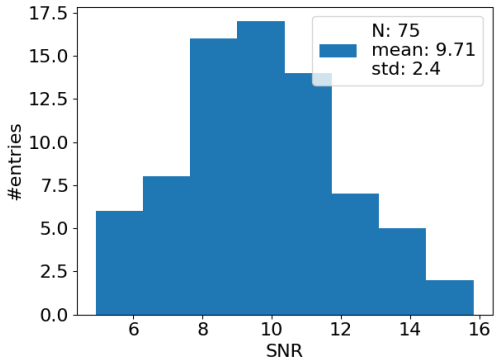
FIGURE 7.6: High voltage sweep for iPMT031. The fitted function is $f(x) = \alpha \cdot x^{\beta}$.

Fits to the respective charge spectra for the nominal HV setting are used to extract some characteristic figures. Distributions of the resulting SNR, charge resolution and P/V are shown in the Figs. 7.7a to 7.7c. Table 7.1 compiles a list of values for the aforementioned characteristic figures as they were recorded in the context of PMT mass testing for JUNO.

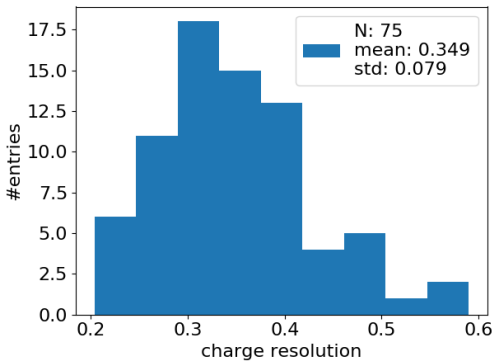
TABLE 7.1: Selection of characteristic properties of JUNO *Hamamatsu* PMTs as measured by [69, p. 183].

property	value
SNR	13.62 ± 0.58
charge resolution	0.274 ± 0.017
P/V	3.66 ± 0.52

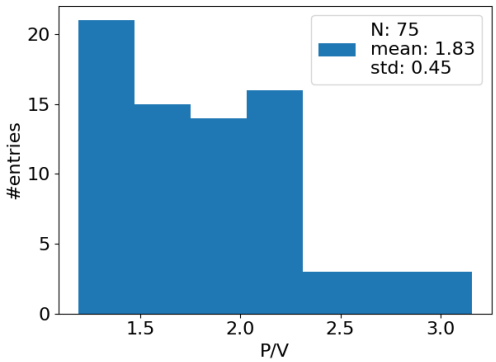
Figs. 7.7a to 7.7c show a large spread in these values, which might be related to varying effects of the earth magnetic field (EMF) depending on the orientation of the PMT (especially the first dynode) with respect to the EMF.



(a) Signal to noise ratio.



(b) Charge resolution.



(c) P/V.

FIGURE 7.7: Distributions from iPMT verification tests without magnetic shielding.

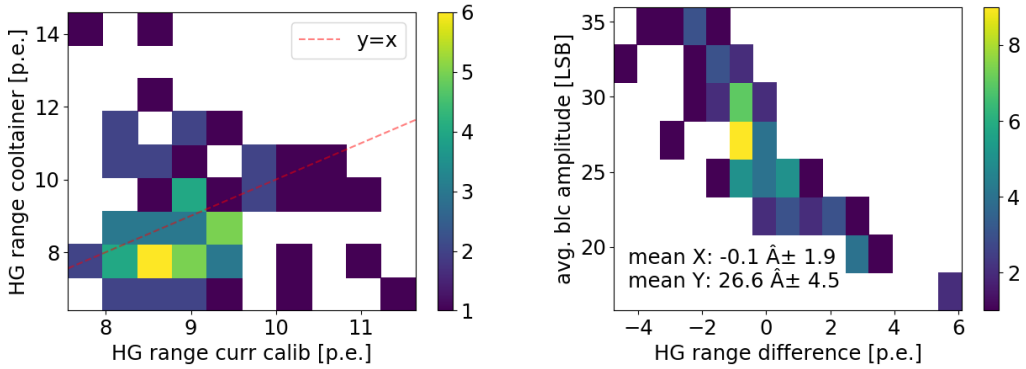
Based on the extracted single p.e. amplitudes in LSB, the HG range in p.e. units can be determined. With the target baseline $bl_t = 20$, the switching threshold $t_{sw} = 250$ (cf. Table 6.2) and the average baseline corrected single p.e. amplitude a the range R is calculated with

$$R = (t_{sw} - bl_t)/a. \tag{7.1}$$

Fig. 7.8a plots the HG range as calculated with Eq. (7.1) (amplitude method) against the HG range as determined by the current calibration (cf. Fig. 6.21). The values are roughly distributed along the line $f(x) = y$, where both method yield the same range. A slight tendency to higher values can be recognized for the current calibration method. In general shows the amplitude method a higher spread with some high values around 14 p.e. to 18 p.e. Fig. 7.8b depicts the difference between the two methods plotted against the average baseline corrected single p.e. amplitude. The distribution is centered around zero, but few iPMTs have either very low (around 12 LSB) or high (around 35 LSB) average amplitudes, which results in large deviation from the current calibration results.

The current calibration has shown non-linearities which are taken into account by using the corresponding gain for each vref subregion. In contrast, the range in p.e.

does not take into account possible non-linearities in upper vref regions above the single p.e. amplitude.

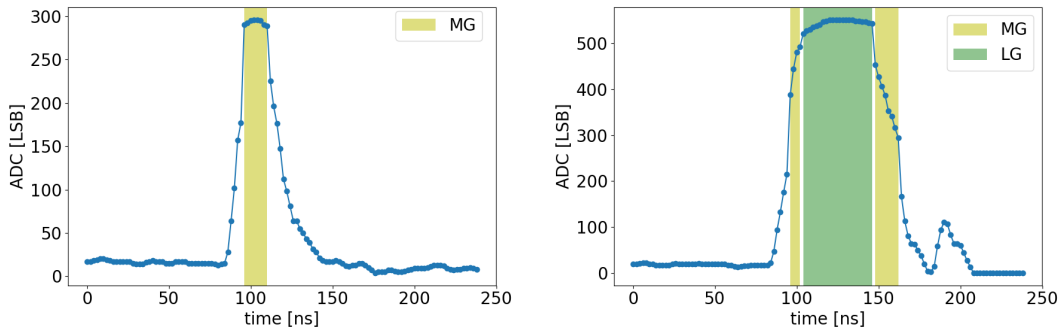


(a) (b)

FIGURE 7.8: (a) Comparison of HG ranges as determined by the current calibration and cooltainer tests.. The x values are given by the HG range resulting as evaluated in the current calibration (cf. Fig. 6.21). The y values are calculated based on the single p.e. amplitude as determined during the HV sweep for the nominal HV setpoint for a gain of 1×10^7. The dashed line is only for optical guidance. (b) The x values are calculated as the difference of the cooltainer HG range minus the current calibration HG range, whereas the y values are given by the respective baseline corrected average single p.e. amplitude.

7.3.5 Large pulses

The large pulse data have been checked visually for major flaws, like missing data in the MG or LG region, but none of them were found. Fig. 7.9a shows an exemplary large pulse which reaches up to the MG and Fig. 7.9b shows an exemplary large PMT pulse reaching up into the LG.



(a) (b)

FIGURE 7.9: Example plots for large pulses with signals up to the MG (a) and up to the LG (b).

7.4 Production summary

The OSIRIS working group at the Physics Institute III B has produced 80 iPMTs for OSIRIS in the year 2021. During the production 5 PMTs have lost their photo cathode due to an air leak. A possible explanation is the different expansion of PMT glass and PMT connector during the application of a shrinking tube as additional protection layer.

Therefore, only 75 PMTs (instead of 76) are available for OSIRIS and tested in the cooltainer. The loss of one iPMT can be tolerated for the muon veto. It has been simulated that the loss of 2 to 3 PMTs in the muon veto has no major influence on the muon veto efficiency [33, p. 12].

Furthermore, three SBs have been produced, tested and verified for the use in OSIRIS. Two of them are required for the operation, one serves as a spare unit.

75 iPMTs have been successfully tested. The tests results show that the iPMTs are functional, but show a rather large variation in the measured properties. A definite evaluation on the performance will be possible based on measurements with the calibration systems in OSIRIS with the proper magnetic shielding and the final grounding scheme, which is expected to have significant influence on the noise level.

7.5 Typical characteristics of an iPMT

Summarizing the measurements presented in this and the previous chapter, Table 7.2 gives an overview of the characteristic properties of an iPMT. Those properties which are based on PMT measurements have a limited informative value due to the missing magnetic shielding. Exemplary measurements with magnetic shielding have shown that characteristics like a P/V can be within 2σ comparing with the manufacturer measurement.

The use of VULCAN has been challenging due to several reasons. The chip has a complex configuration which includes the tuning of the parameter as well as the connection to the PMT with a proper impedance matching. A performance limiting factor of the system is the noise level in the HG RX. Two major noise source are VULCAN itself and the sync data stream signal.

TABLE 7.2: Typical characteristics of an iPMT. When a range is given, this refers to the first and third quartile of the corresponding distribution. The table summarizes results from different measurement setups with different constraints. Thus, the number of iPMT taken into account differs between given values as stated in the corresponding sections. (*) The LG range is linearly extrapolated and "high gain" LG are excluded. (**) Data are recorded without magnetic shielding.

property	value/range
power consumption (including efficiencies and cable loss)	9.8 W to 9.9 W
electronics operating temperature (air cooled)	45 °C
maximum continuous trigger rate (240 ns readout window)	∼60 kHz
HG range end	7.6 p.e. to 8.5 p.e.
HG precision (RMS)	0.057 p.e. to 0.068 p.e.
MG range end	83 p.e. to 88 p.e.
MG precision (RMS)	0.14 p.e. to 0.27 p.e.
LG range end*	8.3×10^2 p.e. to 8.8×10^2 p.e.
LG precision (RMS)	1.7 p.e. to 3.2 p.e.
P/V**	1.4 to 2.1
signal charge resolution**	0.29 to 0.39
charge SNR**	8.0 to 11.3

Chapter 8

Summary and outlook

Summary

In this thesis a short overview over the neutrino detector JUNO and its physics program is presented. This includes an introduction to the radiopurity detector OSIRIS as part of the liquid scintillator filling chain of JUNO. The focus of the following chapters is the detector development for OSIRIS.

The iPMT system for OSIRIS features the concept of integrating processing electronics directly with the PMT. A detailed description of this electronics is given, which has partially been developed as part of this thesis. One focus was the development of FPGA designs for the iPMTs and the SBs, which is summarized in Chapter 5. As part of these designs, especially the data readout and the synchronization are important functions. It has been shown that the readout of the electronics is capable to use the full available link speed and supports continuous readout rates of up to three times the DCR of the PMTs. As part of the characterization, the uncertainty on the synchronization between two iPMTs was evaluated to be less than 0.28 ns.

Part of the design is the highly integrated ASIC VULCAN, which is a newly developed chip dedicated for PMT readout. Parts of the tuning of VULCAN parameters have been presented. An absolute current calibration has been performed to estimate the range and precision of the individual RX. Typical maximum signals covered by the individual RX are about 8 p.e. (HG), 85 p.e. (MG) and 850 p.e. (LG). The corresponding median precisions are 0.06 p.e. (HG), 0.2 p.e. (MG) and 3 p.e. (LG).

The individual steps of the electronics assembly of the iPMTs are presented. Functional verification tests of all 75 fully assembled iPMTs are successfully performed.

Outlook

OSIRIS is a demonstrator for the use of the iPMT system. The iPMT concept could also be valuable for other experiments. A part which is a potential limitation for the scalability of the iPMT system for larger experiments is the software trigger, since it has to temporarily store the data from all PMTs and process them in the trigger logic. In order to reduce the data rate to the software trigger instance, algorithms for the data reduction could be implemented on the iPMT. A large part of the transmitted data is the complete waveform. This could be reduced by implementing the reconstruction of photo electron hits on the iPMT. Thus, only a reduced set of information like the time and charge of a hit would be transmitted.

Further work could also include the implementation of more algorithms to improve the performance of the system and make it more "intelligent". Possible additions

would be the implementation of better trigger methods as an integral trigger or a matched filter.

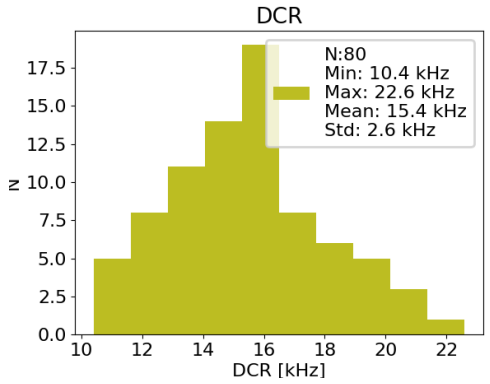
Another interesting option would be the implementation of a neural network either in the FPGA part or the processing system part of the ZYNQ. This could allow for a higher signal to noise ratio of triggered events for sub single p.e. signals. This could also include the optimization of the network parameters individually for each iPMT to account for different noise patterns.

Appendices

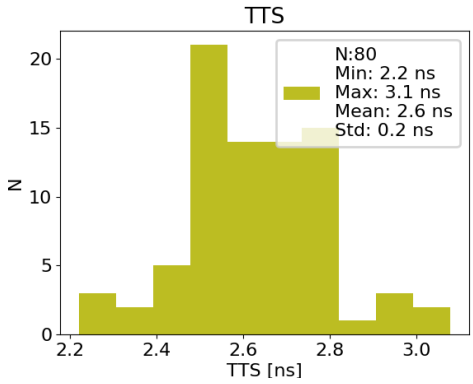
Appendix A

OSIRIS PMT parameters

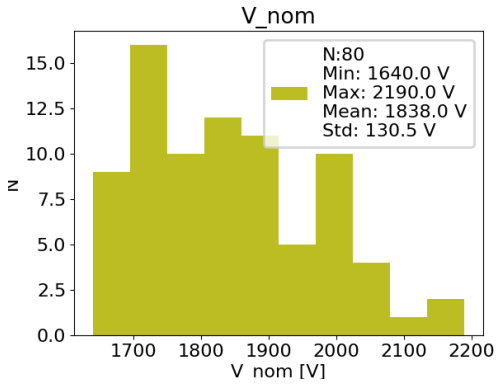
PMTs for OSIRIS have been characterized by *Hamamatsu*. Histograms of the DCR, TTS and nominal voltage are given in Fig. A.1.



(a) Dark count rate distribution.

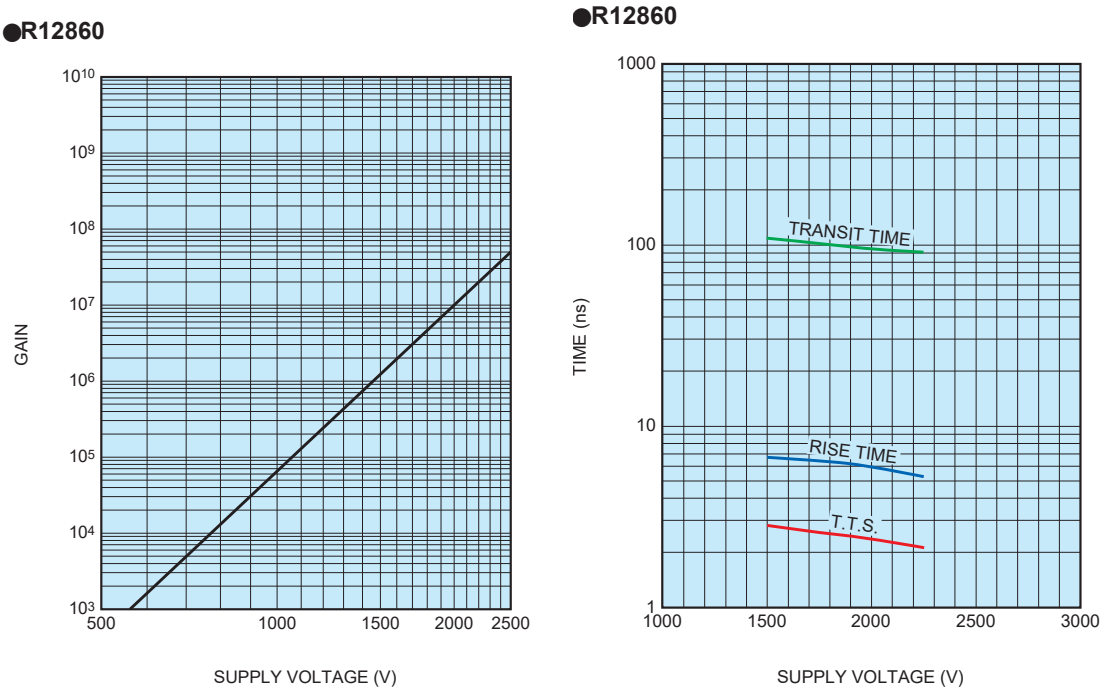


(b) Transit time spread distribution (FWHM).



(c) Nominal voltage distribution for a gain of $1 \times 10^7\, e\, e^{-1}$.

FIGURE A.1: Properties of the PMTs type *Hamamatsu R15343* for OSIRIS.



(a) Gain.

(b) Transit time, **T**ransit **T**ime **S**pread (TTS) (FWHM) and rise time.

FIGURE A.2: Properties of the PMT type *Hamamatsu R12860* as proxy since those data are not available for the type *R15343* [73].

Appendix B

Data transmission protocol

JUNO internal reference: JUNO-doc-6335-v2

Header format

General

The datastreams are expected to be transmitted via the TCP protocol using per default the port 54321 (same port for all type of subevents).

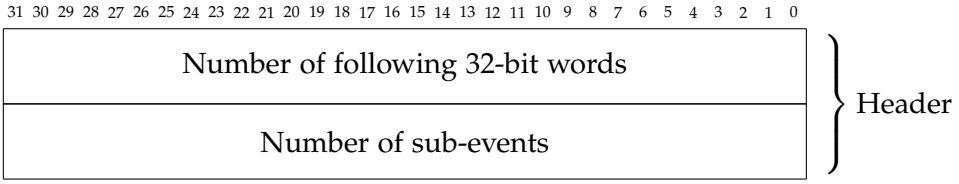


FIGURE B.1: Header format.

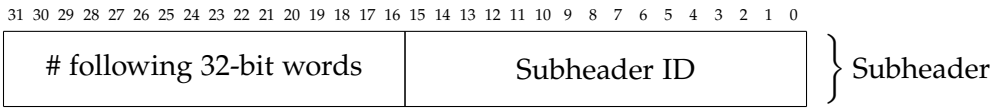


FIGURE B.2: General format of the first word in the subheader.

Each package consists of a header and a number of subevents. Each subevent has an own header with the first word as stated in the Subheader format.

Subevents

Waveform subevent

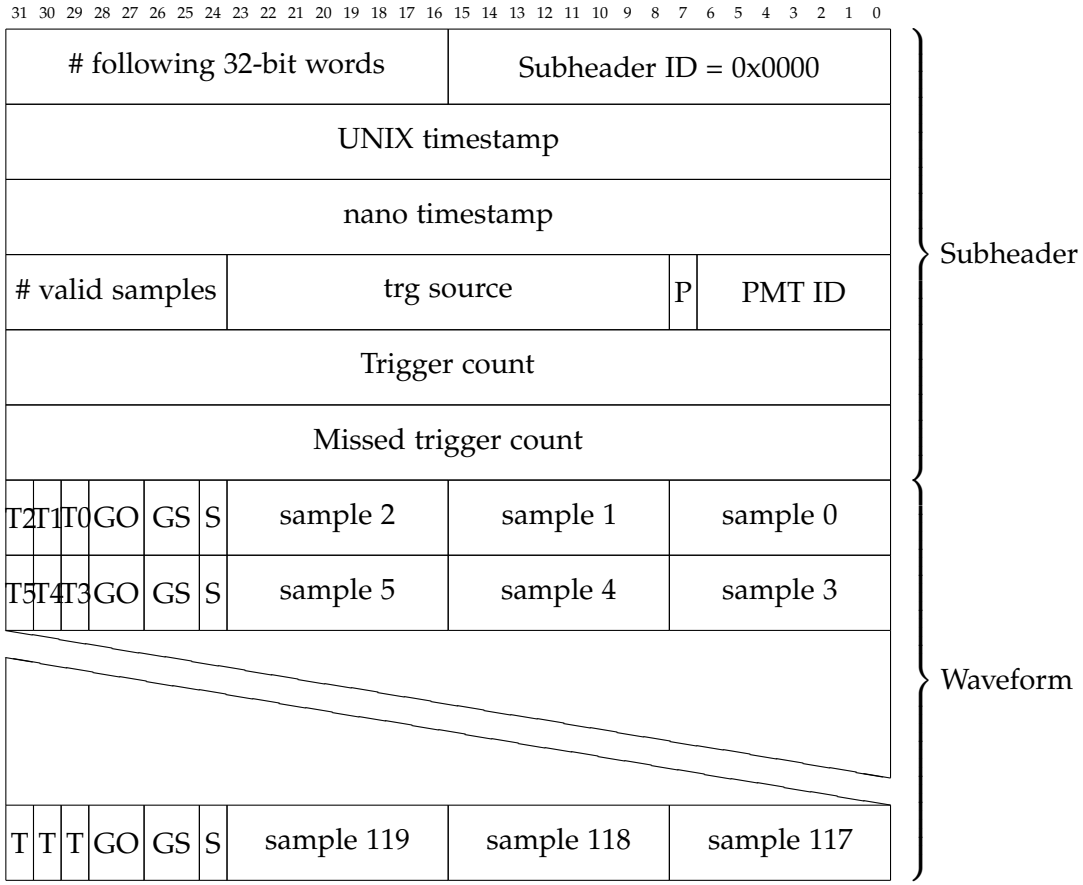


FIGURE B.3: Waveform event format.

Timestamp

The timestamp gives the time of the first trigger in the readout window (the very first sample which has the trigger bit set). For the threshold trigger the timestamp has a precision of 2 ns (VULCAN sampling speed). For the other trigger, the timestamp has the precision of 8 ns (internal clk frequency). The word 'UNIX Timestamp' states the seconds of the timestamp (since 1st january 1970, 00:00 UTC). The 'nano timestamp' states the nanoseconds part.

PMT ID and trigger source

bits (name)	value	description
[6:0] (PMT ID)	0-127	PMT ID
[7] (P)	0	waveform data are packed

[7] (P)	1	waveform data are unpacked
[23:8] (trg source)	-	Trigger source mask (high if the specific trigger condition was fulfilled for this waveform at the trigger time)
[8]	0/1	threshold trigger
[9]	0/1	software trigger
[10]	0/1	external trigger
[11]	0/1	follow up trigger
[12]	0/1	threshold above baseline trigger
[13]	0/1	equality trigger
[14]	0/1	sync trigger (new-timestamp trigger)
[18:15]	0/1	sync link trigger
[23:19] (trg source)	-	t.b.d
[31:24] (valid samples)	-	Number of valid samples divided by 4 in the waveform

The trigger source is given for the first sample with the trigger bit set (the timestamp is also given for this sample).

Threshold trigger

The trigger condition is fulfilled if a sample is greater or equal to the threshold.

Software trigger

Debugging/testing trigger. A trigger request can be set by the control software of the iPMTs. A 0→1 transition issues a new trigger.

External trigger

Debugging/testing trigger. This requires a trigger signal connected to the external trigger input on the Readoutboard. A 0→1 transition issues a new trigger.

Sync trigger (new-timestamp trigger)

The Sync Trigger is issued by the Surface Board. The initial sync trigger is used to set the timestamp and start the timing module.
The sync trigger overwrites the inhibit counting (restarts it) in the current implementation. This is done to guarantee a generation of a waveform tagged with the sync trigger bit for every sync trigger. Otherwise it could interfere with dark count events and might be inhibited (depending on the dark count rate, in the order of a few times per day).

Sync link trigger

The Surface Board provides all iPMTs with the same Clk+Data stream. The datastream features a protocol including the transmission of four different trigger.

Trigger count

32bit counter which increments on every trigger signal. Overflows after $2^{32} - 1$.

Missed trigger count

32bit counter which increments every time when a trigger signal arrives and the internal buffers are full. Overflows after $2^{32} - 1$.

Waveform data

32 bit data contain three 8bit samples from the VULCAN ADCs, the source ADCs (gain) and a trigger bit for each sample. VULCAN transmits two samples on each clock cycle to the FPGA. Those two samples have the same gain (they are taken from the same ADC). The trigger bits are high if a trigger condition was fulfilled. If there are multiple trigger enabled at the same time (e.g treshold trigger and external trigger) the information which of the enabled trigger sources was fulfilled at which time is not saved. Only for the very first active trigger bit in the readout window this information is given in the trigger source mask. The trigger sources have different precisions, thus activating multiple consecutive trigger bits if the condition is fulfilled (see and). E.g. the external trigger is evaluated for blocks of four samples. If the external trigger condition is met, four consecutive samples get their trigger bit set.

bits (name)	value	description
[24] (S)	0	ADC sample 0 and ADC sample 1 have the same gain.
	1	ADC sample 1 and ADC sample 2 have the same gain.
[25:26] (GS)	0 to 2	gain of those samples which have the same gain.
[27:28] (GO)	0 to 2	gain of the sample which can have a gain different from the other two.
[29] (T0)	0 or 1	trigger bit sample 0
[30] (T1)	0 or 1	trigger bit sample 1
[31] (T2)	0 or 1	trigger bit sample 2

LED/Laser trigger subevent

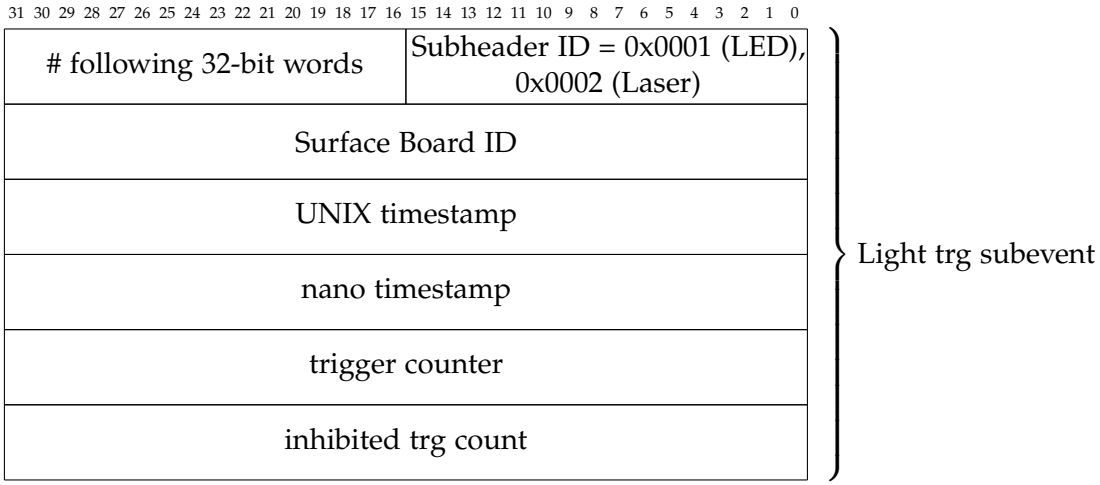


FIGURE B.4: LED/Laser trigger subevent format.

Timestamp

The timestamp format is the same as described in the waveform timestamp.

Trigger count

Counter which increments for each generated trigger (individual counter for LED and Laser). Overflows after $2^{32} - 1$.

Inhibited trg count

Information for debugging/error control. If the generation of triggers collides with an other trigger or a timestamp synchronization, it is inhibited. Each inhibited trigger increments the counter by one. It overflows at $2^{32} - 1$.

Appendix C

Clock and data recovery

The CDR fulfills the central requirement to generate a clock with the frequency of the data bit rate from a data stream. For this purpose, the chip SY87700AL is used for OSIRIS.

Working principle An overview of the functional blocks of the chip is shown in Fig. C.1. The input data stream (RDIN) is passed through a phase detection mechanism to the output pins (RDOUT). The phase detection in combination with a frequency detector is used to align a generated clock with the output data stream. A reference clock with a frequency of 12.5 MHz, corresponding to 1/10 of the data bit rate, is provided to act as "training" frequency [81]. The input and output signals of the chip are exemplarily depicted in Fig. C.2.

In order to successfully detect and maintain the frequency of the data stream, a sufficient number of transitions in the data stream is required. The chip is designed to fulfill the minimum transition density required by a list of transmission standards. For the iPMTs, manchester encoding is used to ensure a sufficient transition density at all times (cf. Section 5.4.2).

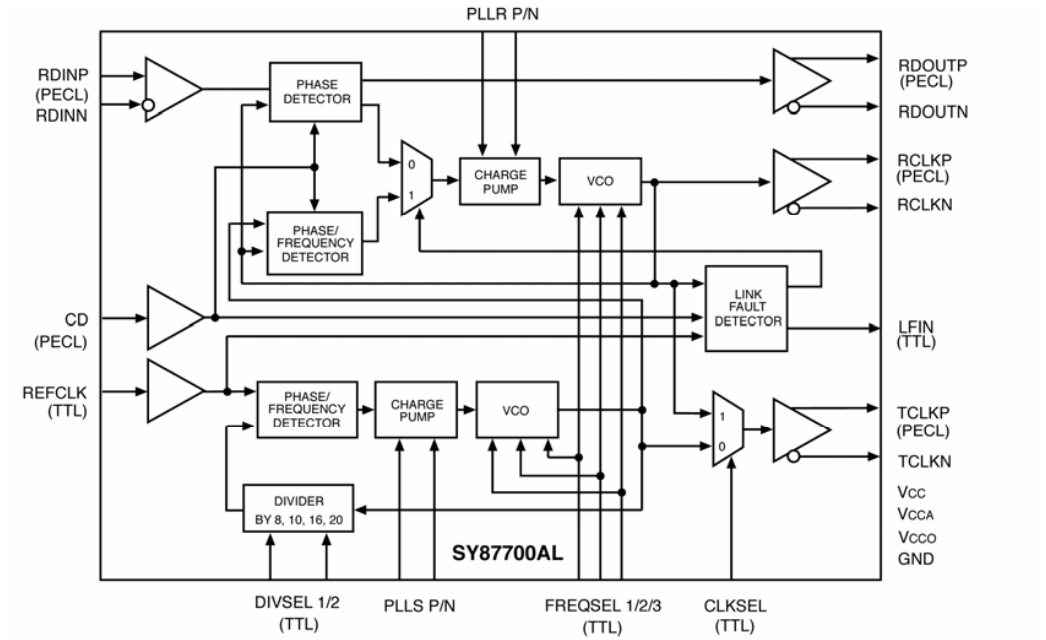


FIGURE C.1: Functional block overview of the CDR chip SY87700AL [81].

Timing relation A key question is if the chip has a constant delay of the input data to the output data. If the chip would shift the data output stream such that the input to output delay is changing over time, a calibration procedure would be required after each relevant change of the delay. There is no problem if each iPMT has a different delay, since this has the same influence as an additional cable delay, which will be calibrated.

The data sheet of the chip explains that the generated clock is aligned to the data, the data are not shifted to match the generated clock. Furthermore, only a phase detection mechanism is drawn in the block diagram of the chip (Fig. C.1), which should not include variable delays.
It has been measured how the input to output relation changes after several power cycles. No relevant change in the timing relation has been observed.

Transmission spectra Fig. C.3 shows a comparison of transmission spectra for typical signals used in the iPMT system.

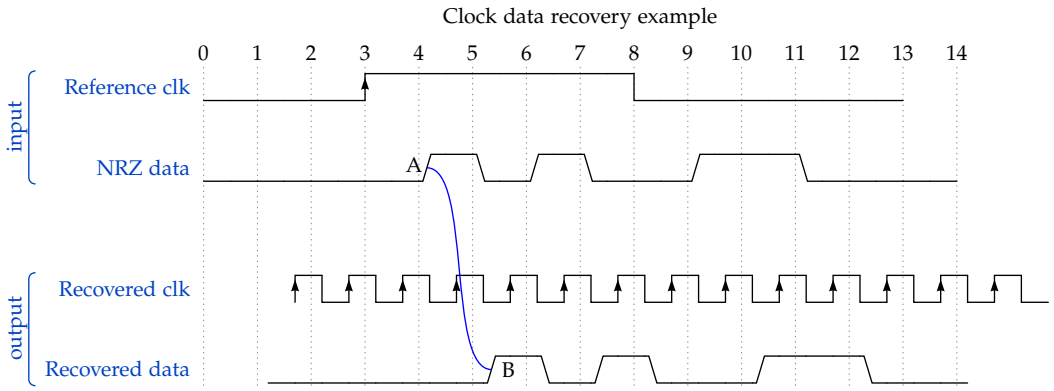


FIGURE C.2: Two inputs are provided for the chip: a reference clock and the input data stream. The chip provides an output data stream which is a delayed copy of the input data stream (blue line from A to B). The recovered clock is aligned with the output data stream such that the rising edge is in the center of the data eye. NRZ stands for non-return-to-zero and describes a line code which assigns each bit value to a line state (typically a binary 1 is signaled by a logic-level high and a binary 0 by a logic-level low).

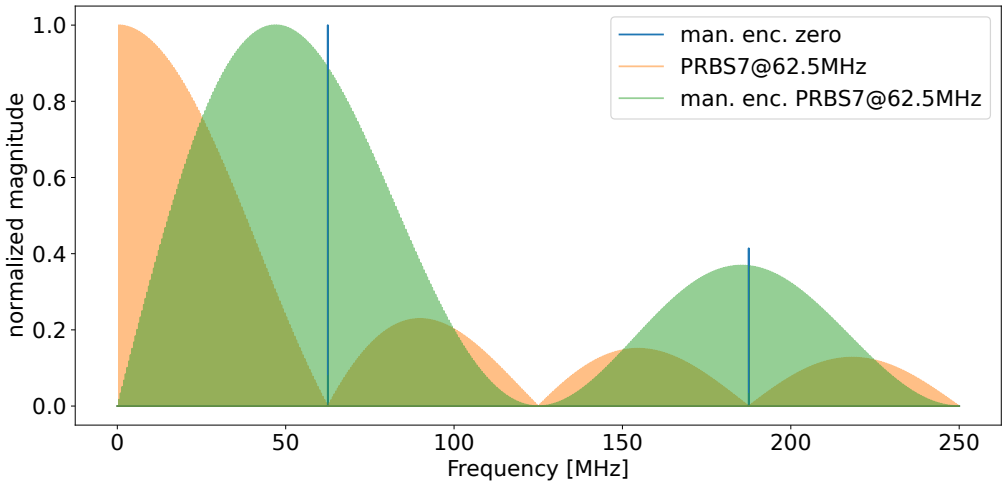


FIGURE C.3: Fast fourier transform of different binary data streams up to a frequency of 250 MHz. Plots are individually normalized to their maximum. "Man. enc. zero" denotes a data stream of constant zero with a data rate of 62.5 Mbit with a manchester encoding applied, resulting in a bit rate of 125 Mbit. This data stream is an approximation of the sync data stream. The orange spectrum depicts a PRBS-7 stream with a bit rate of 62.5 Mbit. The green curve displays the stream with an additional manchester encoding applied.

Appendix D

FPGA design

The following sections give a short overview of the FPGA design flow in Appendix D.1 and some specific FPGA elements in Appendix D.2.

D.1 FPGA design flow

Design coding The first step in the design procedure is the description of functionality in a textual format. The **V**ery High Speed Integrated Circuit **H**ardware **D**escription **L**anguage (VHDL) is used to describe the behavior of the design. This code aims to be as hardware independent as possible. Thus, the use of elements which are specific to the used devices is minimized.

Code may be packed into units, to provide an encapsulated functionality for easy reuse, which are then called IP-Core.

Not all design code has to be coded by hand. *Xilinx* provides a graphical design interface which is partially used to model the functionality in a block design fashion. The graphical representation is automatically converted into code for further design steps.

Simulation An optional next step is the simulation of the described circuits. A behavioral simulation is used to verify that the written code behaves as intended. This type of simulation does not simulate the details of FPGA elements. For example, delays introduced by an element or by connection paths are not simulated. Advantageous of this type of simulation is, that it can be used at an early stage of development and is fast. The open-source simulator ghdl[1] is used as tool for the behavioral simulations. Other types of simulation are post-synthesis functional simulation or post-implementation functional simulation. They use more information about the implementation in the hardware and give in general a more accurate description of the design.

Synthesis The synthesis describes the process of generating a netlist from the code files [70, p. 219]. A netlist is the description of FPGA elements and their connections. Since the availability of the elements depends on the target hardware, this step is vendor and FPGA specific.

Place and route This process creates a mapping of elements in the netlist and physical elements in the FPGA including their connections [70]. The result of this process is the configuration of the FPGA, also denoted as bitstream.

[1] `https://github.com/ghdl/ghdl`

Timing analysis An important step to be done with the placed and routed design is the analysis of the timing. It tests the time behavior of the design against given constraints taking into account the delays of the FPGA elements and their connections. This type of analysis is called static timing analysis, as it does not take into account the exact dynamic behavior of signals [70, p. 221]. The procedure of converging to a timing compliant design is called timing closure.

A static timing analysis is part of the design procedure for both described designs and checked for violations. The designs are free of violations with the implemented set of constraints.

D.2 FPGA elements

This section explains a few elements of the FPGA which are used in the design, but the list is not exhaustive. More information can be found in [78, 95].

BUFG/BUFGCTRL/BUFGMUX A dedicated clock buffer designed to reach to almost every element in the FPGA (global clock buffer). BUFG/BUFGCTRL/BUFGMUX are names for design primitives which actually refer to the same hardware element. BUFGMUX/BUFG are BUFGCTRL elements with reduced functionality.

Block RAM Tile A block of **R**andom **A**ccess **M**emory for storing large amounts of data in the FPGA. The block RAMs of the ZYNQ are each 36 kB large, have two independent access interfaces (dual-port) and support port widths up to 72 bit [95].

DSP Digital signal processing elements for performing multiplication and accumulation.

ISERDESE2 The ISERDESE2 primitive is a dedicated serial-to-parallel converter which is designed for the application in source-synchronous interface designs [96, p. 143]. Every I/O port features the option to use an ISERDESE2 [95].

F7/F8 Muxes Dedicated 2-to-1 look up table multiplexer whose inputs are connected to the output of local look up tables.

MMCME2_ADV The **M**ixed-**m**ode **c**lock **m**anager (MMCM) is a frequency synthesizer which can be used for a wide frequency range from 4.69 MHz to 800 MHz for the used device [93, p. 54]. It provides up to six different output clock frequencies and a lock signal to indicate the phase and frequency alignment status between reference and feedback clock [93, p. 83].

Slice LUT Look up tables with up to six inputs and one output for the implementation of any 6-input logic function [78].

Slice Register Group of flip-flops. Flip flops are single bit clocked storage elements.

Appendix E

Synchronization test

Fig. E.1 depicts the result of a synchronization test measurement with the setup as described in Section 6.7.1. The reference clock for VULCAN is on both stacks the respective onboard clock. The drift between the both clocks is measured to about $-5.95 \times 10^{-7} \frac{\text{ns}}{\text{ns}}$, corresponding to $\approx -0.6\,\text{ppm}$. This is on the level of the typical initial accuracy of $\pm 1.5\,\text{ppm}$ as stated by the vendor [92]. Fig. E.2 depicts the interpolated timestamp difference for the setup with an additional CAT5 cable with a length of 20 m (cf. Section 6.7.1).

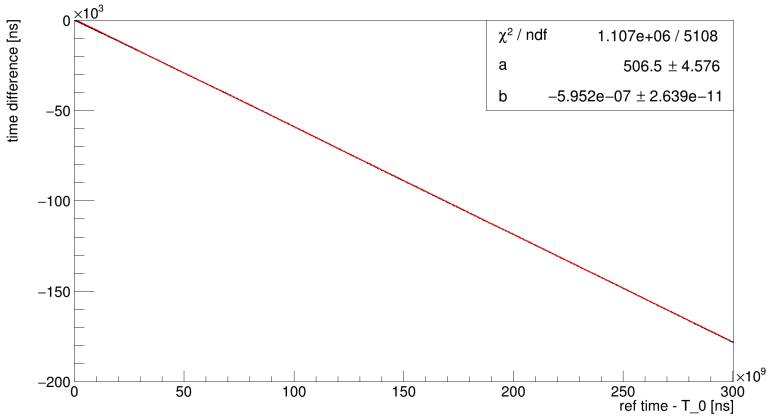


FIGURE E.1: Synchronization test measurement with onboard reference clock. A linear function $f(x) = a + bx$ is fitted to the data.

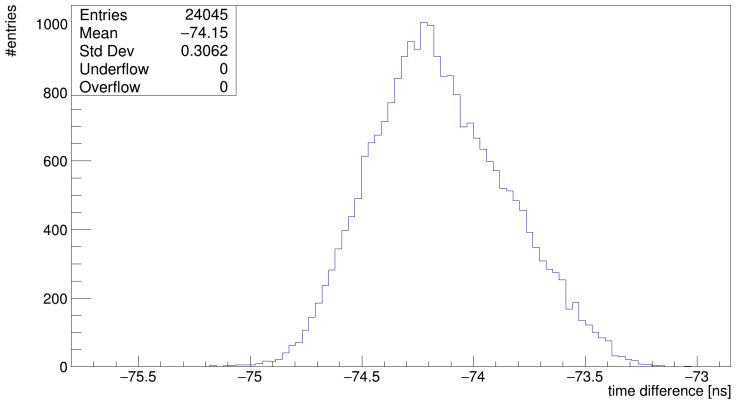


FIGURE E.2: Time difference distribution for synchronization test with an additional 20 m cable for setup one.

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Eidesstattliche Erklärung

Ich, Christian Wysotzki

erkläre hiermit, dass diese Dissertation und die darin dargelegten Inhalte die eigenen sind und selbstständig, als Ergebnis der eigenen originären Forschung, generiert wurden.

Hiermit erkläre ich an Eides statt

1. Diese Arbeit wurde vollständig oder größtenteils in der Phase als Doktorand dieser Fakultät und Universität angefertigt;
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4. Wenn aus anderen eigenen- oder Veröffentlichungen Dritter zitiert wurde, wurde stets die Quelle hierfür angegeben. Diese Dissertation ist vollständig meine eigene Arbeit, mit der Ausnahme solcher Zitate;
5. Alle wesentlichen Quellen von Unterstützung wurden benannt;
6. Wenn immer ein Teil dieser Dissertation auf der Zusammenarbeit mit anderen basiert, wurde von mir klar gekennzeichnet, was von anderen und was von mir selbst erarbeitet wurde;
7. Kein Teil dieser Arbeit wurde vor deren Einreichung veröffentlicht.

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