A Contribution to Integrated Power Electronics for Smart Active Gate Drivers

Von der Fakultät für Elektrotechnik und Informationstechnik
der Rheinisch-Westfälischen Technischen Hochschule Aachen
zur Erlangung des akademischen Grades eines

Doktors der Ingenieurwissenschaften

genehmigte Dissertation vorgelegt von

Léon Weihs, M.Sc

aus

Berlin

Berichter: Univ.- Prof. Dr.-Ing. Stefan Heinen
Univ.- Prof. Dr. techn. Harald Pretl

Tag der mündlichen Prüfung: 06.09.2024

ACKNOWLEDGEMENT

Firstly, I would like to thank the person who pushed through to achieve this milestone in unprecedented times.

I want to thank Univ.-Prof. Dr.-Ing. Stefan Heinen for providing the opportunity to work at his research laboratory as well as for providing the infrastructure and means for multiple successful tape-outs and their subsequent testing. This goes hand-in-hand with Dr.-Ing. R. Wunderlich, constantly going to extra mile to enable, facilitate and enhance the laboratory's ability to do research through meticulous navigation of the academia working maze and of publicly funded projects. In addition, I wish to thank Univ.-Prof. Dr. techn. H. Pretl for his keen interest, thorough review, and helpful suggestions.

I further thank all my colleagues over the years at the Integrated Analog Circuits and RF Systems Laboratory for their invaluable contributions and sharing of knowledge, including T. Herzog, T. Lange, J. Kuhn, J. Zoche, R. Heinen, L. Wang, A. Meyer, J. Bastl, C. Nardi and J. Meier. I would further specifically like to thank L. Rolff for showing me the pragmatism often required in academic environments, M. Hanhart for his invaluable feedback and insights in the most-difficult of times, J. Grobe for his suggestions, assistance and help in absolutely all manners, my office colleague E. Wehr for the daily discussions and crucial tape-out contributions, K. Vohl for his indispensable role in all tape-outs and T. Zekorn for his support and incessant drive. A special thank you also goes to T. Lauber, not only for his technical expertise, but also for his meaningful impact in making the years at IAS fly by.

Furthermore, I want to thank all those who supported me throughout the years, friends and family who provided encouragement and wisdom and for delivering just the right amount of perspective at the right time.

CONTENTS

LIST OF FIGURES

LIST OF ABBREVIATIONS

µC	microcontroller
2-DEG	two dimensional electron gas
ADC	Analog to Digital Converter
AlGaN	Aluminium Gallium Nitride
ASIC	application specific integrated circuit
BV	breakdown voltage
DAC	digital to analog converter
DC	direct current
DMOS	double-diffused MOSFET
EM	electromigration
EME	electro-magnetic emissions
EMI	electro-magnetic interference
EMR	electro-magnetic radiation
ESR	equivalent series resistance
FIFO	first-in first-out register
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
HEMT	high electron mobility transistor
HV	high-voltage
IC	integrated circuit
JFET	junction field effect transistor
LDMOS	lateral double-diffused MOSFET
LDO	low-dropout regulator
LSB	least-significant bit
LUT	look-up-table
MOS	metal oxide semiconductor
MOSFET	metal oxide semiconductor field effect transistor
NMOS	n-channel metal-oxide-semiconductor
opamp	operational amplifier
PCB	printed circuit board
PLL	phase locked loop
PMOS	p-channel metal-oxide-semiconductor
PMU	Power Management Unit

PWM	Pulse Width Modulation
QFN	quad flat no leads
SAR	successive approximation register
SiC	Silicon Carbide
SIMO	single-inductor, multiple-output
SOI	silicon-on-insulator
SPI	serial peripheral interface
UART	Universal Asynchronous Receiver Transmitter
UVLO	under-voltage lockout
VCO	voltage controlled oscillator
VDMOS	vertical diffused MOSFET
ZVS	zero-voltage switching

CHAPTER 1

INTRODUCTION

Power electronics, a branch of electrical engineering that deals with the conversion, control, and regulation of electrical power, has been a key transformative factor in the advancements of modern technology. The field, which emerged in the mid-20th century, has seen remarkable progress, particularly in the development of DC-DC converters. Dating back to the late 1950s, the origins of power electronics lie with the commercial introduction of the transistor, a solid-state, semiconductor-based device that could be used for switching of electricity [9]. This breakthrough paved the way for the development of power electronic circuits capable of controlling and converting electrical power efficiently, enabling and catering to copious diverse applications. Today, power electronics are omnipresent. The use of electronics has invaded almost every aspect of our lives, often times creating strong habituations, making us increasingly reliant on their functionality in order to effectively go about our daily activities.

Monolithic integration of power electronics in the form of integrated circuits (ICs) allowed for the introduction of handheld devices. This sparked the growth of new markets, enabling entirely new applications, and fostering developments into fields previously left to industrial applications that would start reaping the benefits of the economies of scale through massive consumer adoption, pushing down prices and demanding increasing performance. One such sector experiencing substantial growth was and remains the battery industry. Through engineering persistence and market demand providing the funding, battery cell density has seen remarkable increases, with the main objective of increasing mobile and wearable device running time without compromising their utility. This has allowed energy density of mass-produced batteries to roughly quintuple over the past 50 years [85], increasing to around 750 W h/L.

Another enabler and beneficiary of this technological revolution is the semiconductor industry [1]. Deep integration of complex electronics onto

a single piece of silicon has allowed mobile devices to thrive. This success can be attributed to a combination of factors. The exponentially increased device density through technological scaling has allowed designers to include more and more circuitry into an area of silicon, increasing functionality and decreasing area intensive, bulky external components. This can be seen in the miniaturisation of logic circuit boards in consumer applications such as phones and laptops. Simultaneously, technological scaling has led to a reduction in capacitive losses, allowing for increased operation frequencies through the decrease in device size (area) as well as the steady lowering of supply voltages. The benefits of scaling technology node sizes have translated into substantial efficiency improvements, that in turn were channelled into increased performance and longer battery life. While these improvements can be directly attributed to tremendous advancements in semiconductor, specifically silicon semiconductor, fabrication methods, they were enabled by the mass adoption of consumers. The economics of monolithic integration ideally suit this environment, spreading higher initial implementation costs and lower manufacturing and parts costs over the total number of products sold. As each node iteration has seen significant increases in cost per area, the break-even number of required units shipped is continuously pushed higher, as reflected by consumer demand.

With the mass consumer adoption of these devices, it quickly became evident that direct current (DC) would serve as the energy carrier throughout all components, from the power source to the dissipating load. Consequently, the necessity of conversion between multiple DC voltage levels came into focus in order to satisfy the input requirements of the many different loads. Technological scaling has driven the demand for lower output voltages relentlessly, while battery voltages have remained constant, being defined by the chemical potential of their internal composition, with the common lithium-ion cells situated at around 3.7 V. Simultaneously, through increased battery pack density, the market demands for increased power throughputs have pushed voltage levels used for charging of the packs higher in order to reduce resistive power losses as per Ohm's law.

Additionally, surrounding industries have profited and seen similar growth from the increase in consumption of digital services on the consumer side. Sectors such as telecommunications and datacenters have seen exponential increases in power throughputs, driving market demand for DC-based systems that can effectively provide the necessary energy, focussing on both volumetric and electric efficiency. Furthermore, the worldwide surge

in renewable energy sources, specifically home solar installations, has led to a momentous increase in demand for DC-DC converters, due to their inherent DC output. This vast market force has required manufacturers and designers to develop new solutions, adopt new technologies and continuously advance their level of monolithic integration to push the limits of costs while maintaining device longevity, through sheer mass production capabilities.

1.1 High Voltage Converters

Today's demand for higher voltages is unmatched. Most notably, the automotive sector is currently undergoing its largest shift in the past century. The strides seen in the portable devices market is creating new expectations in the automotive market that car manufacturers are expected to meet. However, more importantly, the electrification of the drivetrain is set to contribute significantly to the increase of the automotive electronics market, set to reach over USD 400 bln by 2030 [76], with expectations of around half of vehicular costs to stem from electronics [75, 12]. To meet consumer expectations regarding range and charging time, manufacturers are facing the relentless challenge of increasing their vehicular efficiency. This challenge is being tackled through two primary approaches: minimising weight and enhancing electrical efficiency.

The change to higher voltage rails is beneficial to both. Reduced resistive losses allow for more efficient drivetrains, while also allowing for a reduction in conductor thickness, reducing the weight of the wiring harness, which has become a significant contributor to vehicle weight and costs [86, 92]. Furthermore, higher power throughputs allow for faster charging times, a decisive metric in consumer consideration. It is therefore understandable that all major manufacturers are planning to shift to 800 V high-voltage systems from currently used 300 V to 400 V [92], and are also planning on increasing their internal on-board DC bus from 12 V systems to the higher 48 V standard. Figure 1.1 gives a conceptual overview of the many different voltage rails required within an electric vehicle, illustrating the presence of DC-DC converters throughout. Similarly, the previously mentioned developments in datacenters are seeing matching trends, with modern datacenters planned entirely around high-voltage DC systems. Likewise, the USB standard, found in all modern portable consumer applications, is

increasing power throughputs through the use of higher 48 V busses [91], and personal computer power standards are similarly shifting away from the legacy 3.3 V and 5 V rails to only supporting the higher 12 V rail [6].

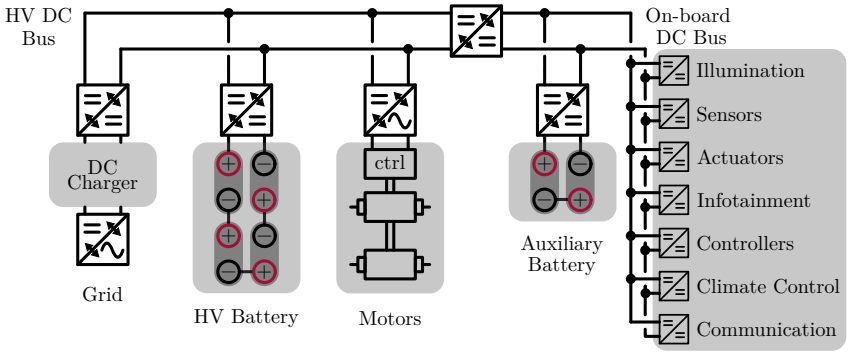

Figure 1.1: Conceptual overview of electric automotive DC Bus system.

Through monolithic integration, bulky discrete components can be omitted, lowering solution footprint and weight. By increasing the operating frequency, the required size of passive components can further be decreased, thereby reducing component weight. However, while the low-voltage sector of DC-DC converters has profited from the innovations and strides in the silicon semiconductor realm, few of the benefits of technological scaling have found their ways into high-voltage applications, hindering further chip-level integration. Physical limitations imposed by material properties such as breakdown field strengths, carrier mobilities and dielectric constants pose barriers to the developments on silicon. The approach has thus changed towards the consideration of novel materials, with two materials currently seeing the strongest adoptions: Gallium Nitride (GaN) and Silicon Carbide (SiC). This shift has opened the door to new possibilities while sidestepping the barriers faced in the developments using silicon technologies. The innovations in the use and manufacturing of wide-bandgap semiconductors have enabled the aforementioned trends by providing high-voltage switches able to cater to high power loads, while facing vastly reduced switching losses. However, the increase in operating frequency also creates new challenges, namely the inherent increase in switching losses faced by other components. This has renewed interest in soft-switching techniques that can be used as a countering mechanism, while also benefiting device lifespan and reducing

electro-magnetic radiation (EMR), two critical factors in modern power electronics design due to the stringent requirements set forth in automotive applications.

1.2 Scope of this Thesis

The thesis aims at the heart of the currently sought objective of the power electronics industry: how modern DC-DC converters can further increase energy density while simultaneously reducing costs. The proposed answer lies in the efficient use of existing components and the incorporation of novel functionalities into indispensable ICs. By finding further use in key components and increasing the utility of existing ICs, additional ones can be omitted, saving area and weight, and reducing assembly, maintenance, and parts costs.

The thesis begins by introducing different modern switches and the theory behind the proposed novel zero-voltage switching (ZVS) detection mechanism. It then goes on to describe the universally deployed buck converter as an application, detailing sources of losses that affect its efficiency and expanding on the dependency on switching frequency and choice of switches.

The work then introduces ZVS and gives an overview of current detection mechanisms, before introducing the novel technique. To understand its use and application area, gate drivers are addressed next, delving into the design and considerations of a current-mirror based output stage.

To demonstrate functionality, the work then presents two discrete implementations of the proposal, acting as motivational steps for a fully integrated solution, which is presented thereafter. The work thereby demonstrates the possibility of a fully integrated, closed-loop, high-voltage capable adaptive dead-time regulation mechanism. Finally, a conclusion and outlook summarise the findings and discuss shortcomings and future possibilities.

CHAPTER 2

BASIC CIRCUITS AND THEORETICAL BACKGROUND

This chapter acts as an introductory chapter, to refresh or introduce the basic concepts that form the backbone of this thesis. It is constructed as to first introduce some of the concepts in transistor topologies and developments, after which it introduces the buck converter that motivates the concept proposed by this work.

2.1 Switches

Switches regulate the flow of electricity. Whether it be in ICs, in discrete form on a printed circuit board (PCB) or housed in an electrical outlet, all switches act to control current, enabling or disabling its flow. Switches come in a variety of sizes and functioning mechanisms, ranging from mechanical, over magnetic to electrostatic, depending on the voltage and current they are required to switch as well as the form factor they may encompass. In integrated circuits, the most common type of switch is the transistor. It too comes in numerous variations, and has seen countless innovations and improvements, the most famous of which is the constantly shrinking device size, as described by Moore's law for the purpose of digital logic. Although not as prominent, the discrete transistor, as used on PCBs, has also benefited from advancements in semiconductor manufacturing capabilities and refinements. Discrete transistors form the backbone of modern electronics, finding their application in almost every modern electronic device. This section aims to introduce the background concept of the transistor before introducing the novelties in power transistors, in order to explain the theoretical background of the implementation of this work.

2.1.1 JFET

The junction field effect transistor (JFET) is a simple semiconductor construct that acts as a field effect transistor [102]. It commonly has three terminals, known as gate, source and drain. It features a simple construct, shown in Figure 2.1, in that the gate terminal contacts an n-type material, and the source and drain terminals contact a p-type material, typically in form of the underlying substrate.

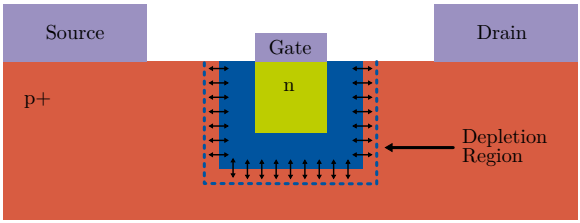

Figure 2.1: Conceptual cross-sectional illustration of a JFET structure.

As the p-type material is conductive on its own, the device is referred to as nominally on, allowing current to flow between drain and source. If a reverse bias is applied to the gate terminal, the naturally occurring, isolating depletion layer can be expanded to cover the entire conduction region, thus pinching off the conductive channel. Similarly, if a forward gate bias is applied, the depletion region can be reduced, reducing the conduction resistance.

2.1.2 MOSFET

The metal oxide semiconductor field effect transistor (MOSFET), shown in Figure 2.2, is a special type of transistor, in that it uses an oxide as isolation between the control terminal (gate) and the conductive channel, creating a capacitively controlled device that requires no continuous input current [59]. By providing a differently doped channel than the source and

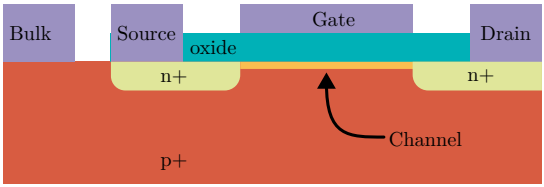

Figure 2.2: Conceptual cross-sectional illustration of a planar MOSFET.

drain regions, the MOSFET is able to be a nominally off device, also known as an enhancement mode device.

Figure 2.3 conceptually illustrates the metal oxide semiconductor (MOS) capacitance formed at the gate terminal, isolated from the surrounding source and drain connections. Due to the fact that the carrier concentration is not constant throughout the material, the total capacitance is represented by the series connection of multiple capacitors and can be described by Equation 2.1, with t_{ox} describing the thickness of the gate oxide, $A = w \cdot l$ referring to the area of the structure, ε_{ox} defining the electric permittivity of the material (oxide) and V_{fb} referring to the flat-band voltage required by the material.

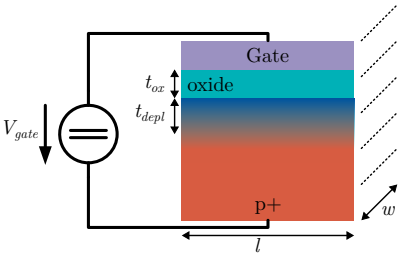

Figure 2.3: Conceptual cross-sectional illustration of a MOS capacitor.

$$C_{mos} = \begin{cases} C_{ox} & \text{for } V_{gate} < V_{fb} \\ \frac{C_{ox} \cdot C_{depl}}{C_{ox} + C_{depl}} & \text{for } V_{gate} \geq V_{fb} \end{cases} \quad \text{with } C_{ox} = \frac{A}{t_{ox}} \cdot \varepsilon_{ox} \tag{2.1}$$

The expansion of the depletion region into the substrate is complex to describe. An abstracted representation of its capacitance is given in Equation 2.2. The depth of the depletion region t_{depl} is highly dependent on the doping profile of the material as well as surrounding structures. However, what can be said is that the region expands with higher voltage. Thus, the overall capacitance decreases with rising voltage due to the expansion of the depletion region further into the substrate [7]. Within a MOS structure, the depletion width reaches a maximum value upon achieving strong inversion of the channel. This creates a lower limit for the capacitance value. Of additional note is that in the context of a MOSFET, at large positive voltage bias, the capacitance asymptotes to the larger, oxide capacitance, as the inversion layer charge is supplied from the source region [7]. However, the gate-drain capacitance must also take into account the effect of the deep depletion region forming in the drift region under the gate oxide due to the respective PN junction sweeping out minority carriers [7].

$$C_{depl} = \frac{A}{t_{depl}} \cdot \epsilon_{Si} \tag{2.2}$$

The capacitors formed within the MOSFET structure are of great significance to designers. They are the main source of switching losses and directly affect the switching characteristic of the switch, defining its dynamic properties and interaction with the remaining circuit components. An overview is given in Figure 2.4. The capacitors originate from the different materials and contact interfaces of the structure. Thus, the geometry and material properties are critical design parameters that can be used to alter the dynamic behaviour of the transistor.

The input capacitance C_{in} is of notable interest to designers as it represents the amount of charge that needs to be brought onto and removed off the gate in order to enable and disable it. It is defined as the sum of the gate-source and gate-drain capacitance, as in Equation 2.3. It is therefore the deciding property when choosing an appropriate gate driver, in order to achieve the targeted switching speeds and transition gradients.

The gate-drain capacitance C_{gd} is the most significant capacitance, as it is situated between the input of the switch, and its output node, forming a feedback path to what is known as the Miller effect [65]. It is therefore

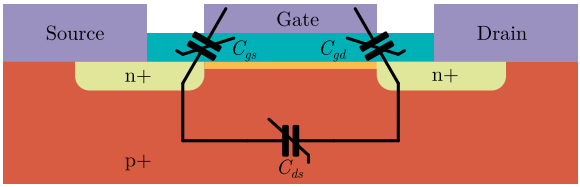

Figure 2.4: Illustration of a planar MOSFET with parasitic capacitors.

also referred to as the reverse-transfer capacitance C_{rss}. The Miller effect is responsible for the occurrence of the Miller plateau, a region in the gate voltage transition where the voltage remains unchanged, even though charge is brought onto/off it. This is due to the simultaneous charge/discharge of the drain-gate capacitance by the drain-current. C_{gd} is often extremely non-linear and undergoes wide voltage swings, causing it to require significant amounts of charge during the switching cycle, which must be taken into account when designing circuits.

$$C_{in} = C_{gs} + C_{gd} \tag{2.3}$$

The output capacitance C_{oss} is defined as the sum of gate-drain and drain-source capacitance as in Equation 2.4. It is of interest to characterise switching losses at the output side of the switch and thereby has a significant role in the circuit's efficiency. It, too, is highly non-linear, in large part due to the gate-drain capacitance.

$$C_{oss} = C_{gd} + C_{ds} \tag{2.4}$$

All three of the main capacitances greatly vary with the operating point of the transistor due to changes in carrier concentrations created by varying depletion zones, channel modulations, doping profiles and field concentrations. For static characterisation, designers therefore often rather rely on the total amount of charge stored on the capacitors to differentiate between

designs and estimate switching losses. Dynamic characterisations rely on accurate modelling of the parasitics and often require actual physical testing to fully verify switching behaviour.

2.1.3 Power MOSFET

The transistor, as presented above, is ideal for use in integrated circuits, as it can be contacted from above. This is typically a requirement for ICs as lithographic processes rely on growing and depositing layers on top of each other from an initial sheet of silicon. Thus, a bottom contact is difficult to achieve, although an industry target that is currently being deployed in the most advanced process nodes [31]. This has the disadvantage of being limited in its ability to withstand high voltages, due to the lack of separation between the terminals. Power MOSFET are designed to have high voltage barriers without breaking down. While many types of power MOSFETs exist, optimised to tackle various challenges, the focus of this work lies on the currently popular and most promising future candidates.

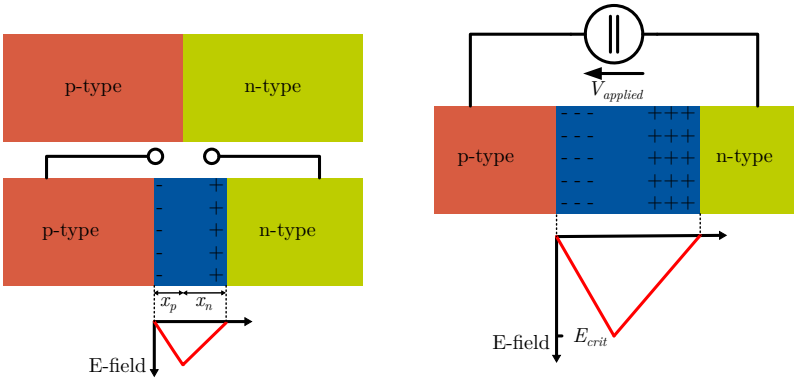

Figure 2.5: PN interface upon interfacing (idealised), at natural equilibrium and at critical reverse bias.

The voltage limit of transistors is set by the onset of an effect referred to as avalanche breakdown [7, 94]. To understand this mechanism, Figure 2.5 presents a simple PN junction. A depletion layer is formed at the interface due to the diffusion of mobile carriers. As the principle of charge equality

must hold, (defined in Equation 2.5, with Donor (n-type) concentration N_D and Acceptor (p-type) concentration N_A), the field builds linearly to a maximum at the interface junction as described by Equation 2.6.

$$N_A \cdot x_p = N_D \cdot x_n \tag{2.5}$$

$$E_{max} = -\frac{q \cdot N_D \cdot x_n}{\epsilon} = -\frac{q \cdot N_A \cdot x_p}{\epsilon} \tag{2.6}$$

Thus, any electrons or holes that diffuse or otherwise reach this region get pushed back out due to the high E-field present within the region. This intrinsic potential, also known as built-in potential, is described by Equation 2.7, where V_T denotes the thermal voltage, and n_i the intrinsic carrier concentration of the material at the given temperature.

$$V_0 = V_T \cdot ln\big(\frac{N_A \cdot N_D}{n_i^2}\big) \tag{2.7}$$

However, as an external voltage gets applied to the junction, further carriers get forced into this region, causing the depletion region to widen, as calculated by transforming Equation 2.6 to Equation 2.8, and the E-field strength to increase. Thus, the acceleration and kinetic energy of the repelled carriers also increases.

$$t_{depl} = x_n + x_p = \sqrt{\frac{2 \cdot \epsilon}{q}\big(\frac{1}{N_D} + \frac{1}{N_A}\big) \cdot (V_0 - V)} \tag{2.8}$$

At what is known as the critical field strength, carriers are accelerated sufficiently to, upon impact with surrounding atoms, excite electrons from the valence to the conduction band. These ionised atoms create highly mobile charge carriers that in turn can generate new mobile carriers, setting off an avalanche effect within the depletion region. This results in a substantial increase in current, known as avalanche breakdown, and thus defines the maximum operating voltage of the device. The exact value of the critical field strength is a function of material doping, bandgap, material type (PT or NPT), geometric dimensions, and permittivity [84] [7].

The power MOSFET category covers a wide range of voltages, depending

on the given process and application, but are typically defined as devices withstanding more than 5 V. However, as the critical field-strength is directly affected by the size of the device, in modern process nodes with extremely small devices, a 5 V transistor may already qualify as a power MOSFET.

2.1.4 LDMOS

The lateral double-diffused MOSFET (LDMOS) was introduced as an improvement on the double-diffused MOSFET (DMOS). A conceptual illustration is shown in Figure 2.6. Their suitability for integration in silicon fabrication processes has allowed them to be, to this day, the backbone of power ICs. In contrast to the typical MOSFET, the LDMOS has an extensive drift region extending to the drain contact, through which carriers must travel. This region acts as an absorbing region for the lateral and vertical fields and, along with the gate oxide strength, determines the breakdown voltage of the device and is thus typically lightly doped so as to achieve a high breakdown voltage (BV).

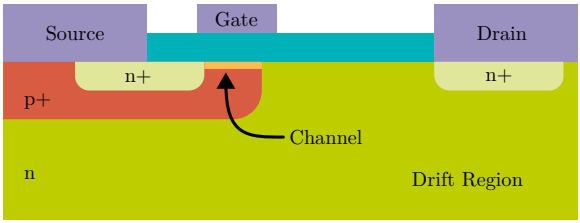

Figure 2.6: Conceptual illustration of an LDMOS buildup.

However, as the current flow is mainly constrained to the surface of the drift-region due to the E-field being strongest there, they have the disadvantage of relatively low current capability due to high on-resistance [79]. Further steps can be taken to increase their performance, such as resurf and modulated doping profiles. These have the objective of distributing the E-field more evenly throughout the drift region, and thus achieving higher current density at the same resistance level. The previously discussed linear E-field limits

the efficiency of the device used in regard to BV, as much of the cross-sectional area of the device is subject to an E-field much lower than the critical field strength. By subjecting more of the region to a higher E-field, the BV of the device is increased.

2.1.5 VDMOS

Vertically diffused MOSFETs (VDMOS) improve on planar LDMOS in that they make use of vertical integration of the MOSFET structure along its 111 crystallographic plane [51]. The drain region can then be contacted from below as illustrated in Figure 2.7. Thus, a much larger region is able to conduct current, while the drift region can be made significantly longer through the thickness of the n-type drift layer. This does not increase wafer area and is thus also cheaper than a corresponding LDMOS design. However, by making use of the third dimension, it becomes difficult to use within ICs and is therefore commonly found in discrete MOSFETs. They feature significantly higher breakdown voltages as well as current capability. Similar performance enhancements can be found in VDMOS, such as modulated doping profiles, to further decrease the on-resistance through a more homogenous E-field distribution.

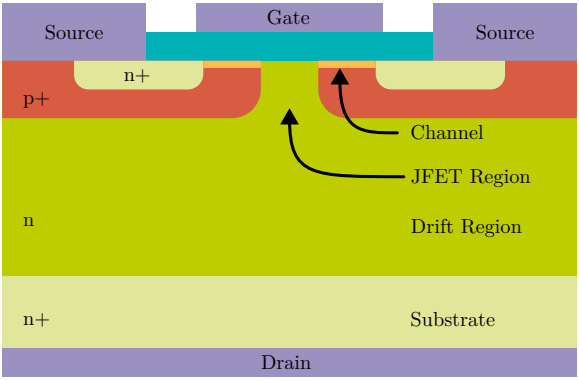

Figure 2.7: Conceptual illustration of a bottom contacted VDMOS buildup.

Of significance in vertical MOSFETs, is the change in dynamic behaviour. The gate-drain capacitance is now formed vertically through the entire stack of the device. This presents further challenges in the design of such transistors to ensure that effects such as the Miller plateau remain manageable for gate drivers, as well as switching losses to remain small enough [80]. As illustrated in Figure 2.8, the input capacitance is made up of a multitude of smaller capacitances. The gate source capacitance is dependent on the gate oxide thickness, as well as the overlap of gate metal and n+ overlap as well as p+ overlap. The more complex reverse transfer capacitance is a function of the depletion width within the JFET region and can be calculated similarly to the MOS capacitance presented in Equation 2.2 [60]. The overall dependency on the drain bias voltage is significant, rising with lowered bias [7].

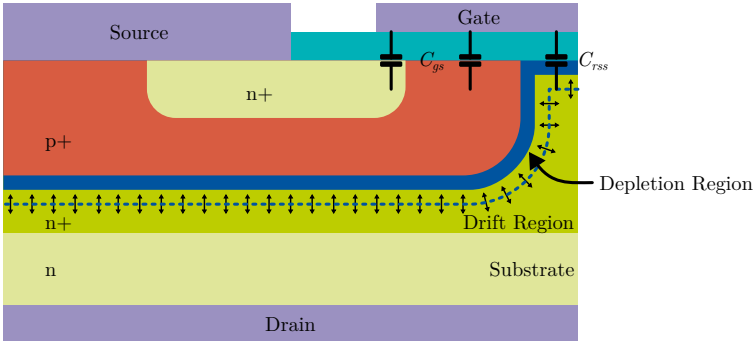

Figure 2.8: Illustration of internal capacitances of VDMOS [7].

Figure 2.9 expands on the detailed internal equivalent circuitry and their voltage dependency when the device is turned off and no conductive channel is present. C_{ov} represents the overlap capacitance between gate and source, which may be significant, notably when the source metal is wrapped around and over the gate. The depletion capacitance C_{depl} mentioned in Section 2.1.2 is replaced by the more general C_{JFET} capacitance to better represent its complex modelling. Advanced designs have multiple doping layers with varying thicknesses and profiles, such as the prominent current spreading layer, to enhance on-resistance and improve the dynamic behaviour of the device. This results in multiple depletion regions being stacked and causing complex interfaces and voltage dependencies. Analo-

gously, physics based approaches have been widely used to model the reverse transfer capacitance, often times using a constant capacitance value anchor and one or more cascaded, variable capacitors to represent the depletion regions within the JFET area. The resulting piecewise models have been further developed to feature continuous functions to counter conversion issues of circuit simulators at the discontinuity [69]. This splitting of behaviour has resulted in high accuracy models [15, 69].

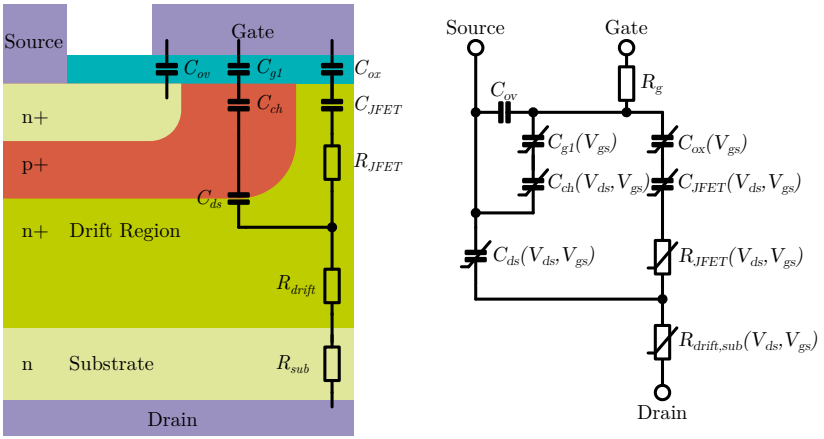

Figure 2.9: Illustration of detailed internal capacitances of VDMOS in non-conductive state [87].

The rate of depletion region expansion can be comprehended through Equation 2.8, illustrating the dependency on doping concentration. As noted by [60], temperature dependency is also present and should be considered. As the JFET region differs significantly from the drift region, as well as other advanced layers not mentioned in this context, so does the rate of expansion throughout these. The capacitive profile thereby becomes highly dynamic, as each expands differently with an applied voltage V_{gd}. Figure 2.10 illustrates the expansion of the depletion region throughout the transistor at different voltages. All in all, this should serve to underline the importance and complexity of the reverse transfer capacitance. For designers, this requires the final verification of proper behaviour to be the real-life evaluation of the device in application.

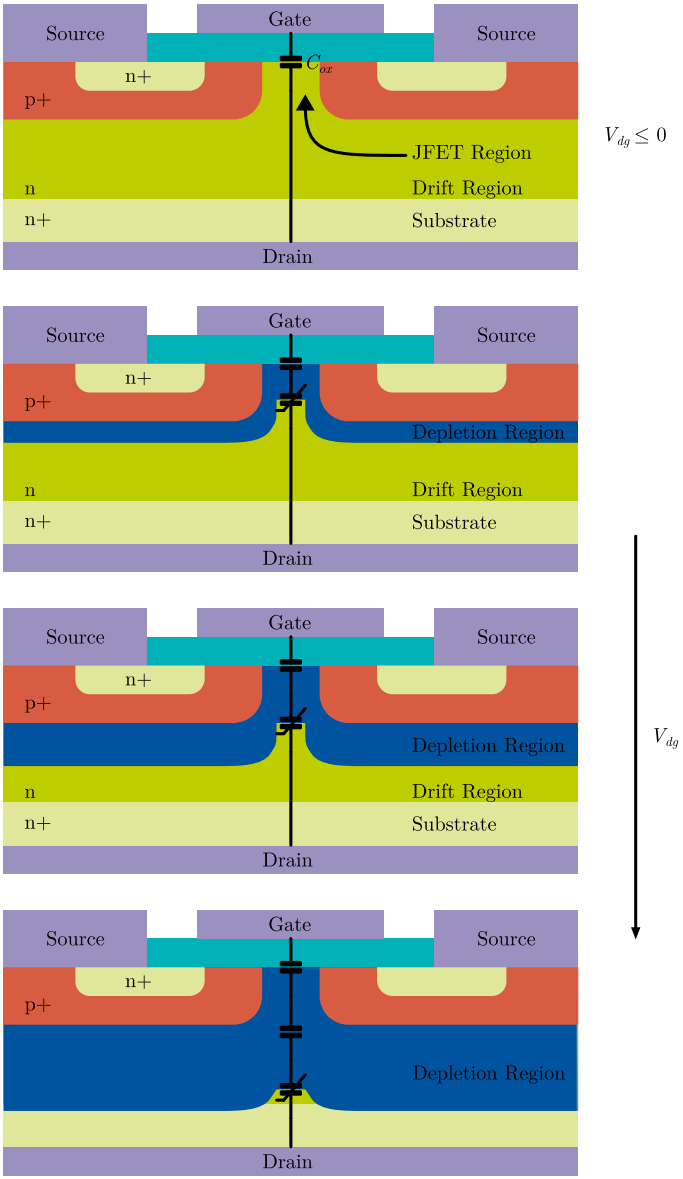

Figure 2.10: Conceptual illustration of the expansion of the depletion region within a non-conducting VDMOS with rising voltage, modelled using cascaded variable capacitors.

2.1.6 GaN HEMT

Gallium Nitride (GaN) is a III/V compound semiconductor that features around three times the bandgap energy of Silicon. This gives it the inherent property of requiring more energy to ionise, and thus can withstand a higher critical E-field strength. In order to create a structure similar to a MOSFET, a voltage controlled conductive channel is necessary. In GaN, this can be done by forming a hetero interface between Aluminium Gallium Nitride (AlGaN) and GaN. Due to the lattice arrangements of the two materials, namely the strain induced by the Al content, a piezo polarisation occurs at the interface, allowing for free carriers to emerge and form what is known as an electron gas. This region is referred to as the two dimensional electron gas (2-DEG) due to its concentration at the interface and thus lack of vertical depth. The carriers experience extremely high mobility in this region, which is why these devices are referred to as high electron mobility transistors (HEMTs). By adding a p-doped GaN layer on top of the AlGaN layer, the 2-DEG can be depleted within the gate region, resulting in a conductive channel controlled by the gate voltage. The device is thus nominally off (enhancement mode) and can be used in power applications. GaN transistors exist for medium power applications, with voltage ratings up to 650 V and peak current ratings up to 150 A [42], currently finding commercial application in phone and laptop charging infrastructure.

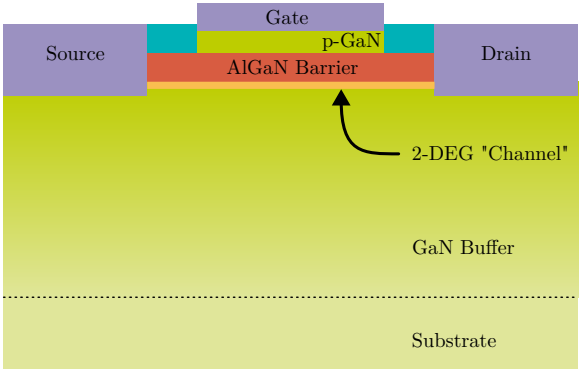

Figure 2.11: Conceptual illustration of a buffered e-mode GaN HEMT.

Their main advantage lies in the minuscule dynamic capacitance and on-resistance. This is in part due to their lateral geometry as well as due to the extremely high conductivity of the 2-DEG. This makes them attractive for high frequency applications, due to the lower dynamic losses experienced, as well as the potential of much reduced resistive losses in high current scenarios. They feature a highly non-linear reverse transfer capacitance. These effects are difficult to model physically, being dependent on the design of the transistor. In GaN HEMTs featuring a field plate, which is commonly used to increase the device's breakdown voltage and reduce on-resistance, the difference in expansion of the lateral and vertical depletion regions within the 2-DEG are attributed as the source of these non-linearities [18], thus splitting the capacitive curve into multiple regions of separate dependency. The lateral arrangement currently limits the current density of the devices, which is an area that is expected to improve with the development of vertical transistors, that should increase their application range to converters in medium high power levels (5 kW to 10 kW) [79, 57]. Another challenge faced by GaN transistors is their inherent lack of a body diode, as there is no PN junction within the device. Instead, the device undergoes reverse conduction when the gate-drain voltage surpasses the threshold voltage, which can in turn be defined by the sum of gate-source and source-drain voltage as in Equation 2.9. This results in increased losses as the voltage drop across the device, defined by the threshold voltage minus the gate-source voltage is higher than that of a typical diode, lying at around 1.7 V [41].

$$V_{gd} = V_{gs} + V_{sd} > V_{th} \tag{2.9}$$

2.1.7 SiC

Silicon Carbide (SiC) MOSFETs differ from typical MOSFETs mainly in the material used. SiC is a compound IV/IV semiconductor that, similarly to GaN, features a much higher bandgap than silicon, leading to a reduction in field-strength within the material. They can thus be made significantly smaller than conventional Si-based MOSFETs and thereby feature a lower on-resistance as well as parasitic capacitances, two aspects that are critical to efficiency. Alternatively, they can withstand higher voltages than Si-based transistors, thus enabling their use in novel applications, such as high frequency, high-voltage DC-DC converters. SiC has proven to be a reliable and feasible alternative to Si, in part also due the high thermal

conductivity of SiC, whose market share is still being held back by production costs, which must be weighed against the efficiency gains obtained. The major advantage of the wide bandgap switches, namely enabling high frequency switching, also has downsides. The faster switching transitions are a major source of electro-magnetic emissions (EME), which can interfere with surrounding electronics. This has also been a source for scepticism in the deployment of SiC, notably in the automotive sector, where electro-magnetic interference (EMI) is a significant concern, and additional shielding measures may outweigh (physically) any benefits obtained from smaller passive components [44]. Another drawback to SiC MOSFETs is their high driving voltage requirement. Often times lying between −5 V to fully disable and 15 V to enable the device, they require specialised gate drivers and cannot be used as an immediate drop-in alternative to Si.

In contrast to GaN, vertical SiC MOSFETs are commercially available in voltage classes up to 1700 V, with peak current ratings of over 500 A [89], and are thus targeting applications in the high power range (10 kW to 1000 kW), ranging from electric automotive to train drive systems, datacenter supplies, HVDC links and conversion systems in renewables such as wind turbines.

Material	Bandgap Energy (eV)	Breakdown Field (MV/cm)	Electron mobility ($cm^2/V\,s$)	Thermal Conductivity (W/cm K)
Silicon (Si)	1.12	0.3	1450	1.5
Gallium Nitride (GaN)	3.39	3.5	1500	1.3
4H-Silicon Carbide (SiC)	3.26	3	900	4.9

Comparison of properties of different semiconductor materials.

2.2 Buck Converter

The buck converter, also known as step-down converter, is a switch-mode DC-DC converter that reduces the DC voltage, making use of an inductor and a capacitor to filter out undesired harmonics of the switching frequency [26]. Being a switch-mode regulator allows it to achieve much higher efficiencies than a linear regulator [77]. It is of extraordinary importance and found in essentially every electronic appliance. Battery powered appliances are bound to have one within their battery charging circuit, between the outlet and the battery. Almost every computer requires them to efficiently provide a stable voltage to the processor, as modern microprocessors run at relatively low voltages, but extremely high currents, thus requiring extremely efficient conversion. As almost every modern application incorporates some sort of microprocessor, the applications for buck converters are essentially endless, from washing machines to drones, audio amplifiers, infotainment systems, solar panel regulators and every portable device in-between. Many of these fields encounter their main challenge in the efficiency of the system, underscoring the relevance of research and development in this regard.

2.2.1 Operating Mechanism

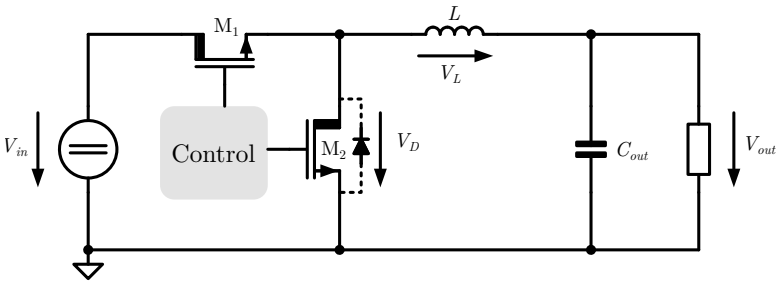

Figure 2.12: Schematic illustration of a synchronous buck converter (non-dashed).

Figure 2.12 shows a schematic implementation of a synchronous buck converter. The buck converter consists of an inductor L, two switches (M_1 and M_2, of which the latter may be swapped out for a diode to obtain a

non-synchronous converter, when efficiency is not as important), and an output capacitor C_{out}. Macroscopically, it operates in two stages, illustrated in Figure 2.13 [90]. In a first, on-phase, the switch M_1 is enabled.

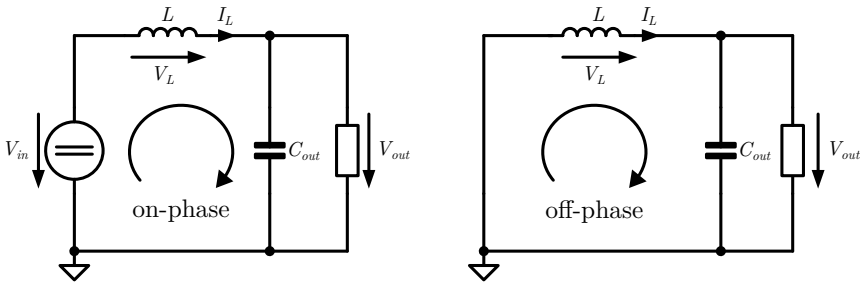

Figure 2.13: Idealised equivalent circuit during on-phase (left) and off-phase (right) of the buck converter.

Thus, current may flow from the input voltage source, through the switch, through the inductor into the load and onto the output capacitor. During the on-phase, the voltage across the inductor can therefore be calculated to Equation 2.10, disregarding a voltage drop across M_1. As the input voltage is higher than the output voltage, the resulting voltage is positive, leading to the current through the inductor I_L increasing linearly.

$$V_L = V_{in} - V_{out} > 0 \tag{2.10}$$

In the second stage, the off-phase, M_1 is disabled, and (in the case of a synchronous converter) M_2 is enabled. As the inductor is now in a magnetised state, the current flow is maintained. Thus, current now flows through M_2, through the inductor to the output. However, the voltage across the inductor is now negative, as described in Equation 2.11, with the voltage across M_2, often being negligibly small.

$$V_L = -V_{out} < 0 \tag{2.11}$$

This leads to a linear decrease in the inductor current, demagnetising the inductor. The inductor current thus follows a triangular ramp pattern in its steady state, determined to Equation 2.12, with the inductor value L

and operating frequency $f_{sw} = 1/(t_{on} + t_{off})$.

$$\Delta I_L = \frac{(V_{in} - V_{out})}{f_{sw} \cdot L} \cdot D \tag{2.12}$$

The ratio of on-phase to off-phase hereby determines the output voltage as described in Equation 2.13, through the value of the duty cycle, D.

$$V_{out} = V_{in} \cdot \frac{t_{on}}{t_{on} + t_{off}} = V_{in} \cdot D \tag{2.13}$$

This basic operation mode is known as continuous operation. Should the inductor current reach zero during the off-phase, it is referred to as non-continuous operation, yielding a more complex output voltage dependency, as given by Equation 2.14, with further dependency on the inductor value, output current I_{out} and operating frequency.

$$V_{out} = V_{in} \cdot \frac{1}{\frac{2 \cdot L \cdot I_{out} \cdot f_{sw}}{D^2 \cdot V_{in}} + 1} \tag{2.14}$$

The control mechanisms of buck converters range widely, including constant on-time regulators, Pulse Width Modulation (PWM) control using voltage or current mode control and model-predictive control to name a few [19, 67, 83, 11, 58, 73, 27]. While being vast and active topics of research, the choice of control is typically dependent on the application requirements including simplicity of implementation, efficiency requirements, dynamic requirements, component availability and cost. Two key aspects of all regulation mechanisms are the achieved values of output voltage ripple and inductor current ripple.

The inductor current ripple, as mentioned in Equation 2.12, is directly related to the switching frequency. Thus, by increasing the switching frequency, a smaller inductor can be used, while maintaining the same current ripple. This is one main motivation behind the trend towards high frequency converters, as inductors pose a significant contribution to the costs to the converter, due to both their weight (through the amount of expensive copper windings and shielding required) and their size occupying costly space both on the PCB and within the enclosure of the converter.

Output voltage ripple refers to the amount of voltage swing the output sees throughout the operation of the converter. During the on-phase, the output

capacitor is charged, increasing the voltage, while during the off-phase, this charge is removed from the capacitor to the output. It is thus directly related to the inductor current ripple and can be defined more accurately by Equation 2.15. This forms the second main motivation behind high frequency converters, as once again, a higher switching frequency can yield a lower output voltage ripple or allow for the use of a smaller output capacitor. As output voltage ripple is a direct nuisance to the converter, which aims to provide a stable output voltage, designers often require large output capacitors to minimise this ripple, due to the sensitivity of following stages, such as microprocessors.

$$\Delta V_{out} = \Delta I_L \cdot \frac{1}{8 \cdot f_{sw} \cdot C_{out}} \tag{2.15}$$

2.2.2 Losses

Switch-mode converters are highly efficient circuits, often reaching efficiencies well above 90 % [82]. Nevertheless, in part due to their employment in portable applications, persistent interest in improved efficiency is fostering sustained research into pushing the boundaries of complexity and implementations further. This section addresses the multiple major sources of losses in buck converters, to motivate the application of this thesis.

Figure 2.14 presents a more detailed buck converter, including parasitic capacitances, and resistances of the major components. While not exhaustive, the added components sufficiently represent the main components [81, 36]. The two transistors have their main three voltage dependent internal capacitors added as well as the internal gate resistor R_{gx}, while the inductor and output capacitor have an additional equivalent series resistance (ESR) R_{ESR} added. Figure 2.15 presents the transient switching waveform of the converter in continuous conduction mode throughout one and a half cycles. The top curve illustrates the triangular inductor current I_L, while the middle curve shows the voltage at the switch node, V_{sw}, at the intersection of the two switches and the inductor. This illustration again sufficiently represents the mentioned signals and voltages but is not to be considered as a realistic representation. Stray parasitics cause significant ringing and non-linearities throughout all transitions that must be considered during implementation, but do not contribute to the underlying principles.

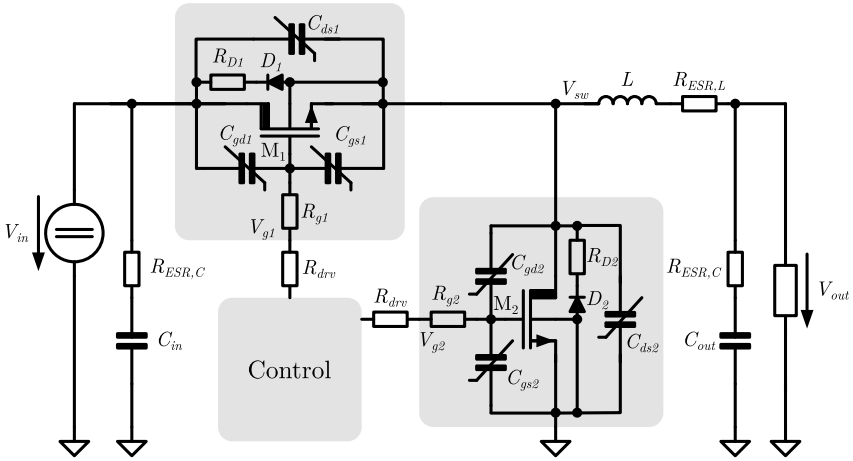

Figure 2.14: Buck converter schematic with added parasitic components of switches, capacitors and output inductor.

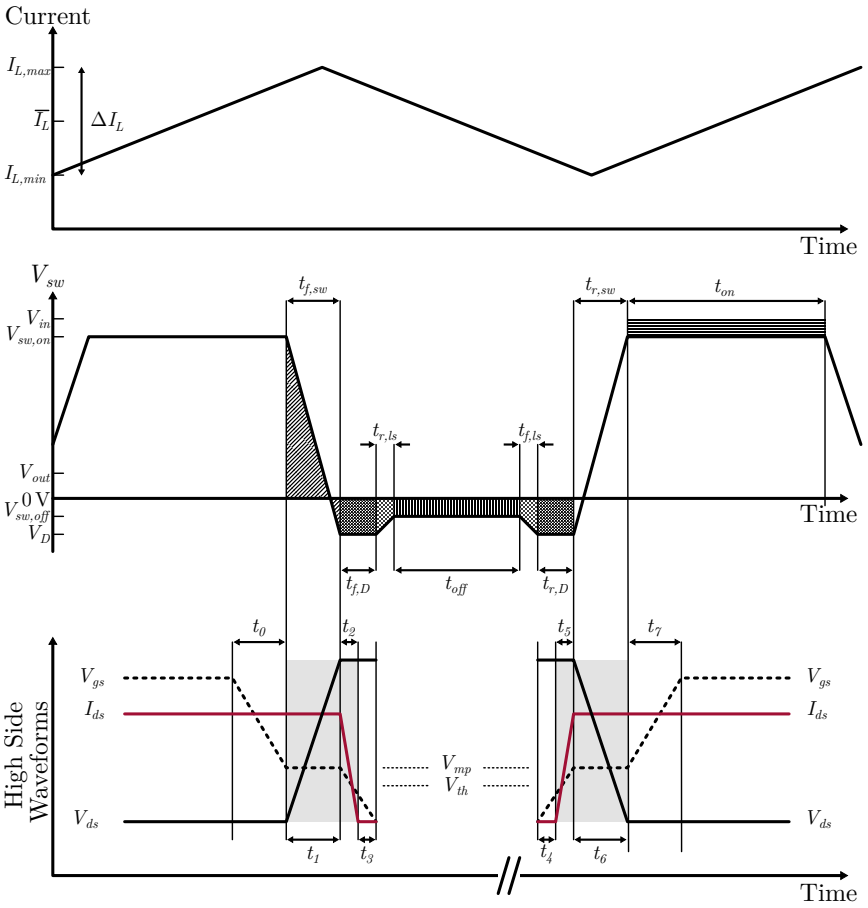

Figure 2.15: Illustrative inductor current (top), switch node voltage (middle) and high-side transistor waveforms (bottom) for a continuous conduction synchronous buck converter.

Conduction Losses

Conduction losses occur in all conducting components of the circuit. These include the inductor (with equivalent series resistance $R_{ESR,L}$), the high-side MOSFET M_1 during the on-phase t_{on} (horizontally shaded area), and the low-side MOSFET M_2 during the off-phase t_{off} (vertically shaded area) in Figure 2.15. As the current is continuously changing throughout these time intervals, in order to compute the power loss accurately, the respective root-mean-square inductor current is considered.

Equations 2.16, 2.17 and 2.18 model the conductive losses of the converter, with the on-resistances $R_{on,\mathrm{M1}}$ and $R_{on,\mathrm{M2}}$ of M_1 and M_2 respectively. Note that they are frequency independent and can thus only be reduced by choosing components with lower resistances.

$$P_{res,L} = R_{ESR,L} \cdot \left[\overline{I_L}^2 + \frac{\Delta I_L^2}{12} \right] \tag{2.16}$$

$$P_{res,hs} = R_{on,\mathrm{M1}} \cdot D \cdot \left[\overline{I_L}^2 + \frac{\Delta I_L^2}{12} \right] \tag{2.17}$$

$$P_{res,ls} = R_{on,\mathrm{M2}} \cdot (1 - D) \cdot \left[\overline{I_L}^2 + \frac{\Delta I_L^2}{12} \right] \tag{2.18}$$

Gate Driving Losses

Gate charge losses occur when driving charge to and from the gate terminals of the switches when enabling and disabling them. These are relevant for the choice of driver circuit in order to ensure satisfying enabling and disabling performance of the devices, such as target transition gradients. By using the gate charge of the devices, provided by the manufacturer, the overall losses are described by Equation 2.19. Naturally they are dependent on the switching frequency, showcasing the motivation behind the use and development of low input capacitance devices.

$$P_G = V_{gs} \cdot f_{sw} \cdot (Q_{gate,hs} + Q_{gate,ls}) \tag{2.19}$$

Transistor Switching Losses

The switching losses of the two transistors occur during transition of the switch node. They occur every time there is an overlap between the voltage across the device and a current flowing through the device. Fundamentally, they can be traced back to the finite time required to turn on the switch. The high-side waveforms are presented at the bottom of Figure 2.15 to show the turn-on and turn-off transition of the high-side switch.

At the start of t_0, the driver circuit begins discharging the gate terminal of the switch. Upon the gate-source voltage reaching the Miller plateau (V_{mp}), the drain-source voltage begins to rise. t_1 ends with the drain-source voltage reaching its maximum and the current beginning to drop. The gate-source voltage then drops further during t_2. Once the threshold voltage of the device is reached (t_3), the device no longer conducts and the entire output current, which at this point is the peak inductor current $I_{L,max}$, has been commutated to the low-side body diode. The switching losses occur during t_1 and t_2, highlighted in grey, as in these time intervals the voltage across the device as well as the current it conducts are non-zero.

Upon re-enablement, the switch initially does not conduct (t_4) until the threshold voltage is reached. The current $I_{L,min}$ then begins to commutate from the body diode to the switch (t_5). Upon reaching the Miller plateau, the switch begins to charge the switch node, reducing V_{ds} (t_6). Once the node is charged, the gate voltage rises to its maximum, further reducing conduction losses (t_7). The time intervals during which switching losses occur (t_5 and t_6) are again highlighted in grey.

$$\begin{aligned} P_{sw,hs} &= \frac{1}{2} \cdot V_{in} \cdot I_{L,max} \cdot f_{sw} \cdot (t_1 + t_2) \\ &\quad + \frac{1}{2} \cdot V_{in} \cdot I_{L,min} \cdot f_{sw} \cdot (t_5 + t_6) \qquad (2.20) \\ &\approx V_{in} \cdot \overline{I_L} \cdot f_{sw} \cdot t_{r,hs} \qquad (2.21) \end{aligned}$$

Equation 2.20 quantifies these two losses, which may be roughly approximated further under the assumption that rise and fall times are similar. Ignoring this assumption, the two time intervals are defined by the rate at which the driver is able to push charge onto and pull charge out of the gate terminal of M_1. The faster the driver is able to turn off the device, the lower the time interval during which these losses can occur.

Equations 2.22 and 2.23 define these time intervals as a function of the respective gate currents, that are defined in Equations 2.24 and 2.25, with the final gate-source voltage $V_{gs,max}$, the internal gate resistance R_{gate} and the external gate resistor used for the turn-on process $R_{drv,on}$. Similarly, the currents during t_5 and t_6 can be defined, with the marking difference of using $R_{drv,off}$, which may be different depending on the design.

$$t_1 + t_2 = \frac{Q_{on}}{I_{g,on}} = C_{in} \cdot \frac{V_{mp} - V_{th}}{I_{g,on|t_1}} + C_{gd} \cdot \frac{V_{in}}{I_{g,on|t_2}} \tag{2.22}$$

$$t_5 + t_6 = \frac{Q_{off}}{I_{g,off}} = C_{gd} \cdot \frac{V_{in}}{I_{g,on|t_5}} + C_{in} \cdot \frac{V_{mp} - V_{th}}{I_{g,on|t_6}} \tag{2.23}$$

$$I_{g,on|t_1} = \frac{V_{gs,max} - 0.5(V_{mp} + V_{th})}{R_{drv,on} + R_{gate}} \tag{2.24}$$

$$I_{g,on|t_2} = \frac{V_{gs,max} - V_{mp}}{R_{drv,on} + R_{gate}} \tag{2.25}$$

Lastly, charge on the output capacitor of M_1 (C_{oss}) gets dissipated during the turn-on event of the switch. These losses are quantified in Equation 2.26, with $C_{oss} = C_{gd} + C_{ds}$ being highly voltage dependent, decreasing asymptotically with increasing voltage. Overall, these losses are increasingly relevant for high-voltage and high frequency converters and display another advantage of using wide-bandgap semiconductors in these applications.

$$P_{Coss,\mathrm{M1}} = V_{in}^2 \cdot f_{sw} \cdot C_{oss,\mathrm{M1}} \tag{2.26}$$

While this only covers the losses encountered in the high-side switch, it is often enough to consider these. This is due to the fact that the low-side switch does not encounter the same voltage/current transitions. When it is enabled, ideally the voltage across it is zero. In the exemplary waveforms presented in Figure 2.15, it is actually slightly negative, as the switch's body diode conducts before the switch is enabled. This delay is called dead-time. During the other transition, when M_2 is disabled, the same is true, as the current immediately commutates to the body diode, resulting

in no considerable voltage across the device ($V_D - V_{sw,off} \approx V_D$). Thus, switching losses of the low-side transistor can be described by Equation 2.27 with the commutation times $t_{r,ls}$ and $t_{f,ls}$.

$$\begin{aligned} P_{sw,ls} &= \frac{1}{2} \cdot V_D \cdot I_{L,max} \cdot f_{sw} \cdot t_{r,ls} \\ &\quad + \frac{1}{2} \cdot V_D \cdot I_{L,min} \cdot f_{sw} \cdot t_{f,ls} \qquad (2.27) \\ &\approx \frac{V_D}{2} \cdot \overline{I_L} \cdot f_{sw} \cdot (t_{r,ls} + t_{f,ls}) \qquad (2.28) \end{aligned}$$

Furthermore, its output capacitor losses are non-existent, as the charge gets pulled out by the inductor. Thus, the energy stored in it is re-used in the output path, contributing to the output power and not losses.

Diode Losses

In consequence, the diode losses during time interval $t_{r,D}$, when the body diode of M_2, D_2, is conducting, must be considered. They cause further frequency dependent conductive losses represented by Equation 2.29. In GaN HEMTs these losses are higher than in Si, due the device undergoing reverse conduction, resulting in a much higher forward voltage. SiC MOSFETs also experience higher losses due to the forward voltage of their body diode being around four times higher than Si [78].

$$\begin{aligned} P_D &= V_D \cdot f_{sw} \cdot I_{L,max} \cdot t_{f,D} + V_D \cdot f_{sw} \cdot I_{L,min} \cdot t_{r,D} \qquad (2.29) \\ &\approx V_D \cdot f_{sw} \cdot \overline{I_L} \cdot (t_{f,D} + t_{r,D}) \qquad (2.30) \end{aligned}$$

Furthermore, when M_1 is enabled, the diode must undergo reverse recovery to transition to the blocking state. This is quantified by the amount of time the diode requires to recover, t_{rr}, as well as the peak reverse-recovery current I_{rr}, or the overall reverse recovery charge Q_{rr} This charge thus contributes to the losses of the converter through Equation 2.31 and requires consideration when choosing the device. GaN HEMTs, lacking a body diode, do not suffer from these losses.

$$P_{rr,D} = \frac{1}{2} \cdot V_{in} \cdot f \cdot I_{rr} \cdot t_{rr} \tag{2.31}$$
$$= V_{in} \cdot f_{sw} \cdot Q_{rr} \tag{2.32}$$

Diode losses can be reduced by making use of a low resistance, Schottky diode in parallel to the body diode. This is often considered a useful approach. However, in high-frequency converters this approach becomes less beneficial. While not drawn in the parasitic consideration in Figure 2.14, a stray inductance is located between the MOSFET channel and the source terminal. This source inductance causes a delay in the commutation of the current between the internal body diode (which is connected in a low-inductance path) and the external Schottky diode (which, depending on the design, also has the additional inductance formed by bond wires, packaging, and PCB traces [4]).

Capacitive Losses

Capacitive losses occur due to the charge and discharge of the input and output capacitor. They consist of leakage, dielectric losses as well as resistive losses, that are bundled as an equivalent series resistor ($R_{ESR,C}$). The output capacitor undergoes losses in each switching phase, amounting to Equation 2.33, while the losses on the input capacitor are given by Equation 2.34.

$$P_{Cout} = \frac{1}{12} \cdot \Delta I_L^2 \cdot R_{ESR,C} \tag{2.33}$$

$$P_{Cin} = D \cdot (1 - D) \cdot \overline{I_L}^2 \cdot R_{ESR,C} \tag{2.34}$$

The output capacitor losses show the link between output voltage ripple and inductor ripple, acting as a trade-off to the benefits of high-frequency converters.

2.3 Zero-Voltage Switching

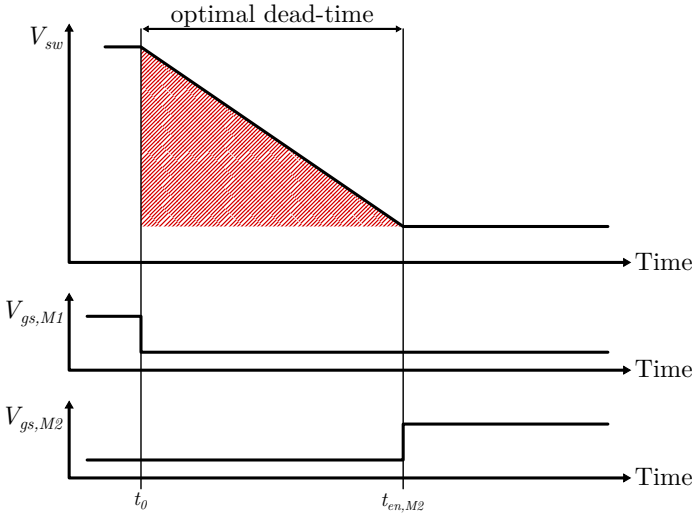

Figure 2.16: Illustrative ideal switch node voltage transition and corresponding transistor gate voltages.

As can be deduced from Section 2.2.2, switching losses are a major hassle in converters. And as was apparent from the consideration of M_2, switching under no voltage has significant benefits. This condition is referred to as zero-voltage switching (ZVS) and has multiple benefits [54].

The biggest benefit is efficiency. The non-existent switching losses allow for higher power throughputs and enable new applications through the use of higher switching frequencies, which in turn has numerous advantages and enables additional use cases including increased converter density, lower cooling requirements and lower component cost.

Secondly, ZVS vastly reduces ringing and can thereby lead to lower electromagnetic emissions. This is of interest in many applications, notably the automotive sector, where significant investments in shielding are required to ensure electro-magnetic norms are maintained for compatibility with sensitive and security relevant sensors and communication busses. These

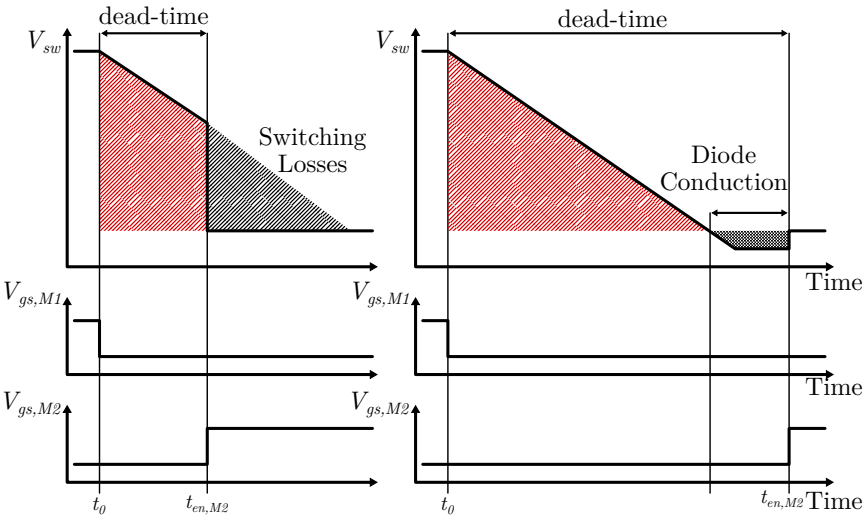

Figure 2.17: Illustrative early and delayed switch node voltage transition and corresponding transistor gate voltages.

cause additional production and development costs, as well as increased product weight, resulting in less range [72, 43, 32].

Lastly, the soft transition reduces internal device stress due to reduced current/voltage spikes. This increases device lifespan [49], which is of great interest, as replacement of these switches is often costly, requiring the replacement of the entire, highly integrated converter module.

To better understand the crossover of M_2, Figure 2.16 presents the mentioned transition for an optimal dead-time. At timepoint t_0, the high-side transistor is disabled. As the continuity of the current through the inductor must be maintained, the voltage of the switch node is forced to decrease. The charge stored on the switch node is thus pushed to the output. If one were to enable the low-side switch now, any charge remaining on the switch node would be sunk to ground and thus wasted. If delayed too long, the switch node voltage drops below zero, and current is provided to the output through the body diode. These two suboptimal dead-times are illustrated in Figure 2.17, with the shaded areas representing the losses incurred.

Zero-voltage switching has the prerequisite of a topology that allows for it to occur. In the example of the buck converter discussed previously, this is the case for M_2. For M_1, however, ZVS is not possible in this configuration. It can, however, be enforced through the use of resonance [54, 66]. By adding a resonant tank in parallel to the switch, an alternating voltage across the device can be brought about. Through proper timing of the driver circuit, M_1 can thus be enabled/disabled under zero-voltage condition.

Alternatively, the output inductor L can be re-used, with an additional switch across it to create the resonant tank with minimal additional components, as illustrated in Figure 2.18. A third phase is enabled by the switch S_1. After disabling M_2, but before enabling M_1, S_1 is closed. This short across the inductor causes the switch node voltage to rise to the output voltage. The subsequent disabling of S_1 causes the voltage at the input to rise due to the resonant tank formed between itself and the output capacitors of M_1 and M_2. This sinusoidal increase in the switch node voltage allows the controller to turn on the high-side transistor at the peak of the resonance, when the switch node voltage almost reaches V_{in}, resulting in ZVS.

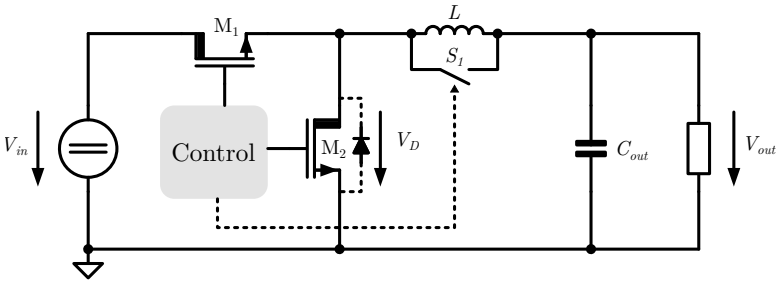

Figure 2.18: Schematic of a buck converter with fully enabled ZVS.

While enforceable, the control mechanism is relatively complex, and not helpful in understanding the underlying transition. This section therefore focusses on the ability of inherent ZVS of M_2, covering the transition in more detail on a circuit level.

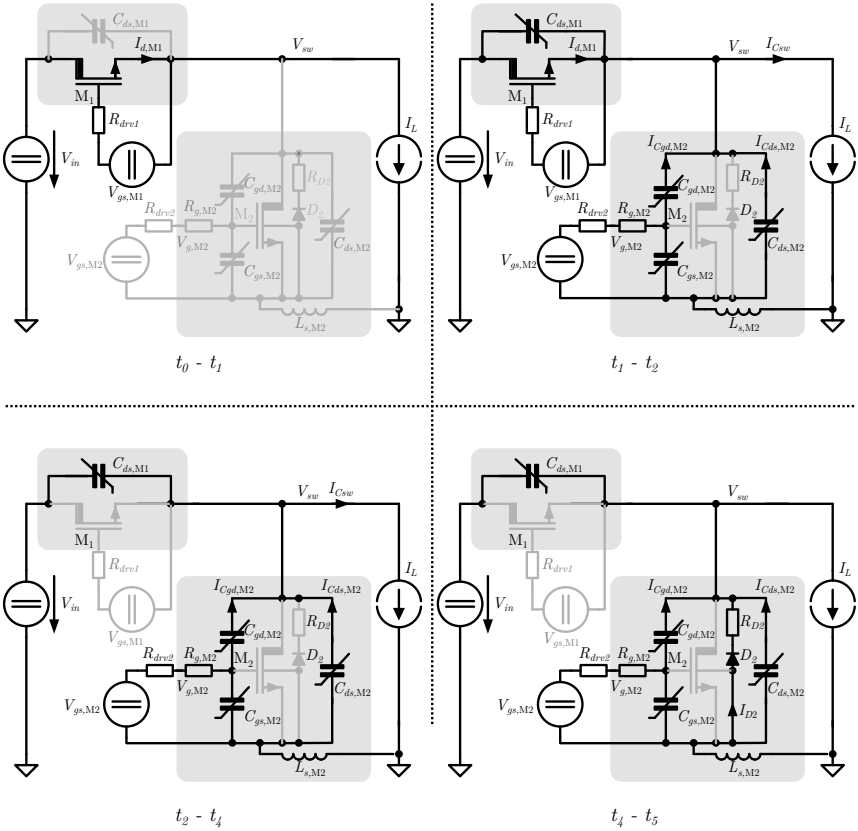

Figure 2.19: Equivalent conducting circuits for the four stages making up the switch node voltage transition.

2.3.1 Operating Principle

Figure 2.19 illustrates the conducting circuits of a conventional buck converter before, during and after the transition, while Figure 2.20 illustrates the accompanying waveforms of interest throughout the transition [48].

At t_0, the high-side transistor is disabled, leading to a drop in $V_{gs,\mathrm{M1}}$ to the Miller plateau value. This voltage is then maintained, as the gate-drain capacitor is charged. The output current during this time interval is still provided by the transistor $\mathrm{M_1}$ as it is still conductive, however with a higher conducting resistance, as detailed in Equation 2.20 and thus contributing to additional losses.

At t_1, the Miller plateau has been surmounted, and the drain current $I_{d,\mathrm{M_1}}$ starts to decrease, until $V_{gs,\mathrm{M1}}$ reaches the threshold voltage of the transistor at t_2. The decrease in current must be compensated for, as the output current must be maintained due to the magnetisation of the output inductor. This difference in current is provided by charging/discharging of the output capacitors of $\mathrm{M_1}$ and $\mathrm{M_2}$, as well as parasitic capacitance of other origin at the switch node and is represented by I_{Csw}. The output capacitor of $\mathrm{M_2}$ consists of $C_{gd,\mathrm{M2}}$ as well as $C_{ds,\mathrm{M2}}$. The current originating from each is proportional to their individual capacitance. At t_2, the entire output current is provided by the switch node capacitance, $\mathrm{M_1}$ is entirely disabled.

At t_4, the switch node voltage drops to zero. Although seemingly little changes, this timepoint is of key importance to the concept presented in this work. Figure 2.21 illustrates the current loop formed by the low-side switch. As during the previous interval, the output capacitor of $\mathrm{M_2}$ partially provides the output current through $I_{Cgd,\mathrm{M2}}$ and $I_{Cds,\mathrm{M2}}$. To better detail the changes in current occurring in this interval, the defining dependencies of current flow into/out of a capacitance must be considered.

For a linear capacitor, the charge stored on the capacitor is defined by the capacitance and the voltage applied:

$$Q = C \cdot V \tag{2.35}$$

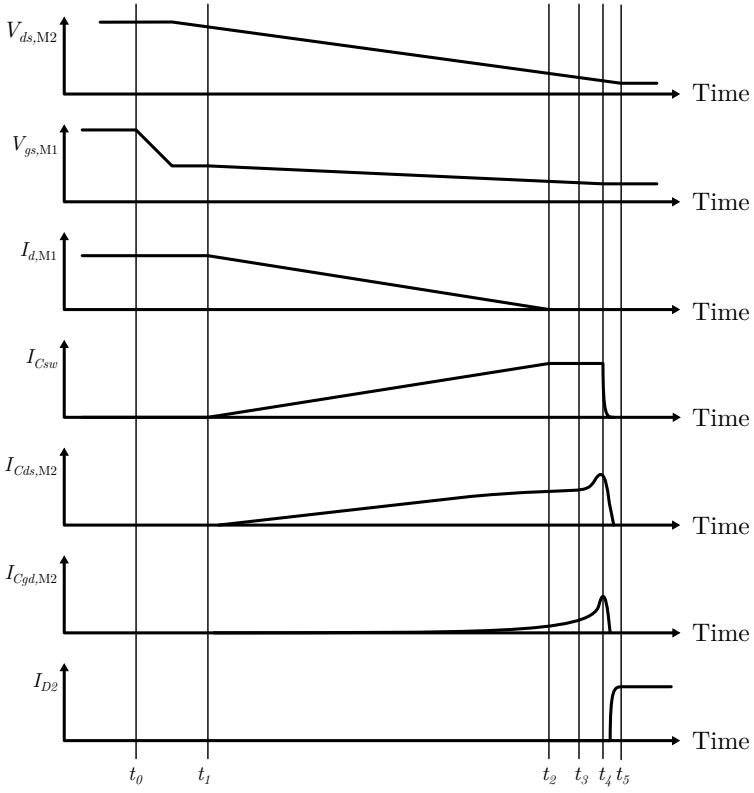

Figure 2.20: Waveforms describing the transition through dead-time.

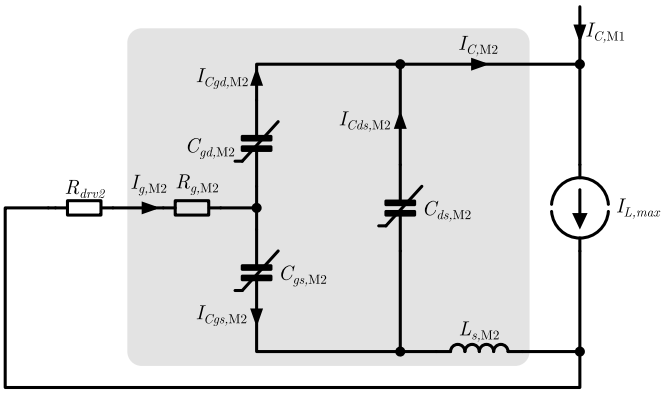

Figure 2.21: Schematic view of current flow throughout M_2's parasitic capacitors at t_4.

As the current is defined as the differential of charge, for a linear capacitor it can be defined by Equation 2.36.

$$\begin{aligned} I &= \frac{\delta Q}{\delta t} \\ &= C \cdot \frac{\delta V}{\delta t} \end{aligned} \tag{2.36}$$

For a non-linear capacitance, the same assumptions cannot be made. Instead, the charge must be defined by its dependency on the voltage at a differential voltage as in Equation 2.37.

$$C(V) = \frac{dQ}{dV} \tag{2.37}$$

The current remains the differential of charge over time, however by incorporating the dependency on voltage, Equation 2.38 is derived.

$$\begin{aligned} I &= \frac{\partial Q}{\partial t} \\ &= C(V) \cdot \frac{\delta V}{\delta t} \end{aligned} \tag{2.38}$$

Under the assumption that the change in voltage over time remains constant, a direct proportional relationship is established between the capacitance value and the current flow into/out of the capacitor.

Due to the relation of Equation 2.39, the two currents $I_{Cgd,\mathrm{M2}}$ and $I_{Cds,\mathrm{M2}}$ are therefore proportional to the respective capacitance value.

$$V_{Cds,\mathrm{M2}} = V_{Cgd,\mathrm{M2}} + V_{Cgs,\mathrm{M2}} \tag{2.39}$$

The current loop that closes the circuit for $I_{Cgd,\mathrm{M2}}$ also flows through the driver stage, labelled $I_{g,\mathrm{M2}}$, as in Equation 2.40.

$$I_{g,\mathrm{M2}} = I_{Cgd,\mathrm{M2}} + I_{Cgs,\mathrm{M2}} \tag{2.40}$$

As discussed in Sections 2.1.2 and 2.1.5, both the gate-drain capacitance and the drain-source capacitances are extremely non-linear. Thus, depending on the device, the capacitance value can increase dramatically at low voltages. This increase in capacitance causes the slopes of $I_{Cgd,\mathrm{M2}}$ and $I_{Cds,\mathrm{M2}}$ to increase proportionally. The rise in $I_{Cgd,\mathrm{M2}}$ thus causes a rise in $I_{g,\mathrm{M2}}$, which can be detected by the gate driver. This phenomenon forms the basis of the novel detection mechanism presented and discussed in this thesis, finding further use in existing capacitors of the high-voltage switch. The fact that this current flows within the gate path gives additional merit to the concept, as an integrated sensing approach within the gate driver further allows for a low complexity and scalable solution.

Finally, at t_5, the voltage of the switch node has reached the (negative) forward voltage of D_2. The switch node capacitance is fully discharged, and the output current is entirely provided by the body diode of the low-side transistor.

2.3.2 Efficiency

The benefits in efficiency come directly from the non-existent switching losses discussed in Section 2.2.2. Early switching results in the loss of charge stored on the MOSFET's output capacitors and other parasitic capacitance on the switch node, as detailed in Equation 2.41. Late switching results in

diode conduction, increasing resistive losses as well as the required reverse recovery losses, and is detailed in Equation 2.42.

$$P_{early} = \underbrace{\frac{1}{2} \cdot C_{sw,eff}(V_{sw}) \cdot V_{sw}^2(t_{dt}) \cdot f_{sw}}_{\text{Non-ZVS Losses}} \tag{2.41}$$

$$P_{late} = \underbrace{Q_{rr} \cdot V_{in} \cdot f_{sw}}_{\text{Reverse-recovery}} + \underbrace{I_{out} \cdot V_F \cdot t_{dt} \cdot f_{sw}}_{\text{Diode-conduction}} \tag{2.42}$$

Of particular interest here is the dependency of the losses on the dead-time t_{dt}. While delayed turn-on results in a linear increase in losses, due mostly to the increased conduction losses of the body diode, early switching has a quadratic dependency on the drain-source voltage (V_{ds}). With a linear decrease in V_{ds} with respect to time, the quadratic dependency is thus also found in the time-domain. Thus, early switching can be much more harmful, and increasingly so with high-voltage (HV) converters, than delayed switching, depending on the output current.

2.3.3 Detection

Dead-time used to prevent current through-shoot can be added as a constant time factor. However, as just discussed, achieving accurate dead-time is key to maximising converter performance. This section discusses multiple possible approaches used to implement zero-voltage switching control.

Direct Sensing

The simplest method is direct sensing of the switch node voltage [3]. A simple comparator suffices to detect the voltage dropping below a threshold $V_{th,zvs}$, such as 0 V, thus signalling to the controller to enable M_2, as illustrated in Figure 2.22. For low voltage applications, where the switch node voltage remains within the voltage realms of the controller, direct sensing of the node can occur. For HV applications, a simple resistive divider consisting of R_1 and R_2 can be used to divide the high voltage

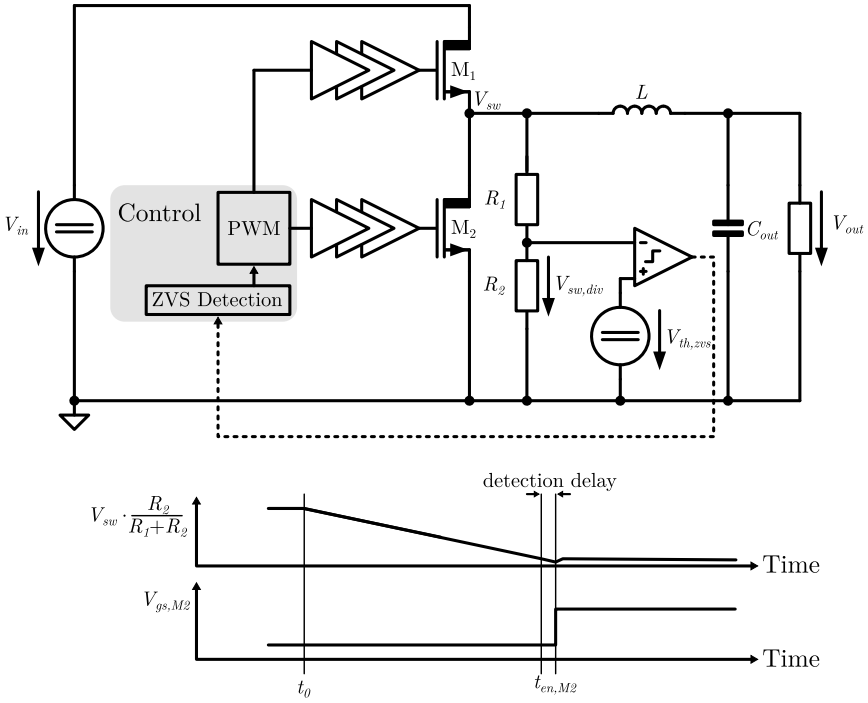

Figure 2.22: ZVS detection mechanism based on a resistive voltage divider and comparator.

into the controller's voltage domain, indicated by $V_{sw,div}$. Alternatively, for fast-changing, high-frequency converters, a capacitive divider can be used additionally or in combination to act as a high-pass.

Auxiliary Windings

Magnetic sensing uses an auxiliary winding L_w on the inductor, as shown in Figure 2.23, which represents a scaled down version of the inductor voltage through the winding ratio of the two coils n, bringing it to a manageable level [14]. Sensing the zero-crossing of the winding can then be used to determine the appropriate dead-time required for ZVS. This can be used for both high-side and low-side ZVS and is feasible in high-frequency high-voltage converters. However, it significantly complicates the magnetic design as well as occupies more space due to the additional inductance and can suffer from significant delay due to the signal processing required [16].

Body Diode Sensing

Another approach to evaluating the required dead-time senses the body diode forward voltage V_{D2}, as illustrated in Figure 2.24. As soon as it drops below a certain value, the low-side switch is enabled. However, once again, the sensing components of the controller and/or comparator must be able to tolerate the high voltages occurring at the switch node. For low voltage approaches, this method is feasible, however for high-voltage approaches integrating the switches on-chip, a high-voltage process is required, which may not be available and suffer from increased costs and limited bandwidth. Apart from the concerns regarding voltage tolerance, another major downside of body diode sensing is the temperature dependency of the forward voltage [93], that should be taken into account. Alternatively, the use of a current-sense FET can inhibit the expensive SiC body diode conduction [71]. Furthermore, in GaN, where the absence of a body diode causes much higher losses, approaches that prevent it entirely are preferred.

An unconventional approach relies on the electroluminescent properties of SiC, whereby photons emitted from the device once the depletion layer of the PN junction is reverse charged, can be detected. This signals that body diode conduction is about to occur and can thus be used as a reliable indicator for ZVS [40], while being significantly more complex in its implementation.

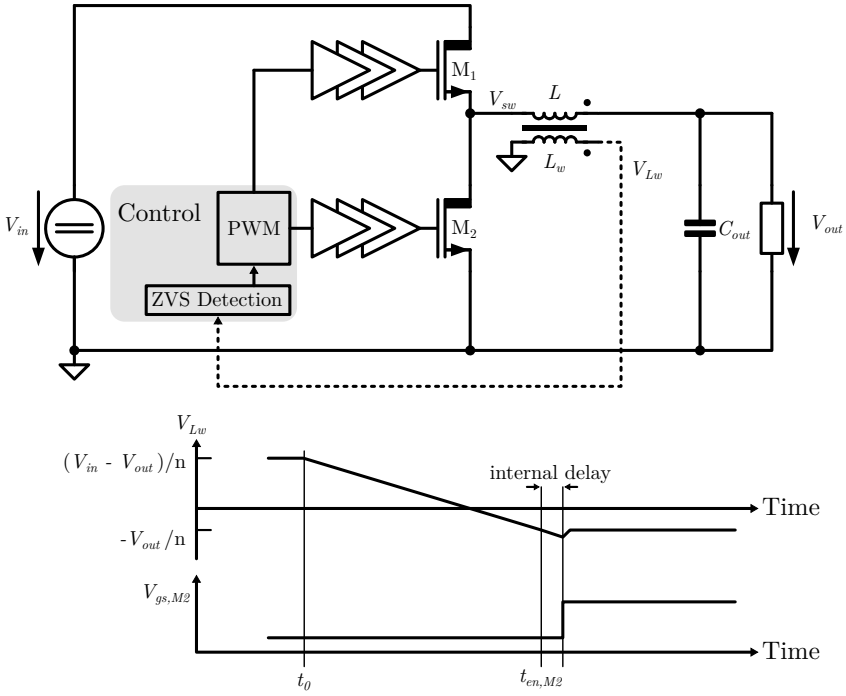

Figure 2.23: ZVS detection mechanism based on auxiliary winding of the inductor.

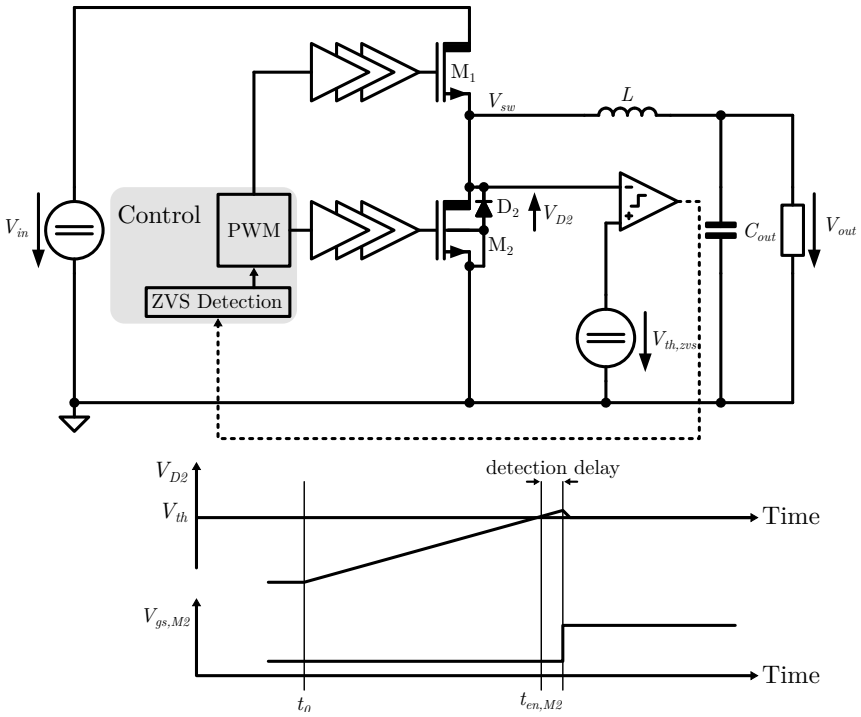

Figure 2.24: Body diode conduction detection mechanism enabling ZVS.

2.3.4 Predictive Slope Sensing

The inherent delay that is present in sensing the voltage, waiting for the comparator to toggle, for the controller to output a trigger signal and then the driver stage to charge the gate-terminal, can result in body diode conduction. Thus, a different approach was developed, using a predictive strategy. Figure 2.25 illustrates such an approach in a simplified manner. As the declining voltage slope of the switch node is mostly linear, the zero-crossing can be predicted by capturing two timepoints, measuring the slope, and interpolating to the crossing.

Internal delays can thus be circumvented. However, the accuracy of the sensed information is a crucial requirement, both in magnitude and in temporal resolution. While purposefully simplified in this example, the accuracy of predictive systems hinges on the previously made assumption of linearity. The prediction accuracy thus heavily relies on accurately modelling non-linearities of the voltage transition, with dependencies on temperature, voltage and load condition creating challenging scenarios for accurate implementations [5].

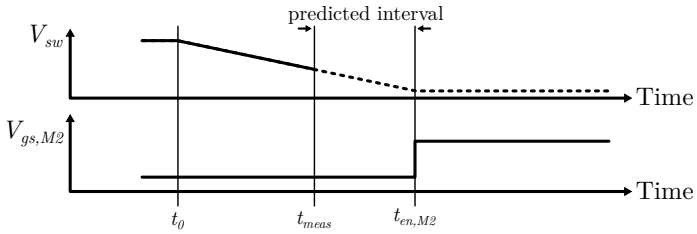

Figure 2.25: Predictive dead-time regulation based on switch node voltage transition.

2.3.5 Adaptive Dead-time

While predictive approaches have seen intensive research, other approaches instead rely on regulation. The simplest approach is to make use of one of the sensing mechanisms and, instead of directly setting the dead-time,

regulating the dead-time to its optimal value over multiple switching cycles. This allows the controller to correct for intrinsic delays, resulting in an adaptive system.

Within adaptive regulators, one differentiates between one-shot adjustments, whereby the dead-time is set in a single step within one switching cycle, and unit-bit adjustments, where the dead-time is adjusted by a fixed amount every switching cycle, resulting in a slower, less dynamic system, as shown in Figure 2.26 [61, 13]. Adaptive dead-time regulation can therefore be seen as an enhancement to the steady-state dead-time mechanisms, extending their use-cases, with the offerings of modern processes enabling temporal resolutions within the hundreds of picoseconds [13, 99].

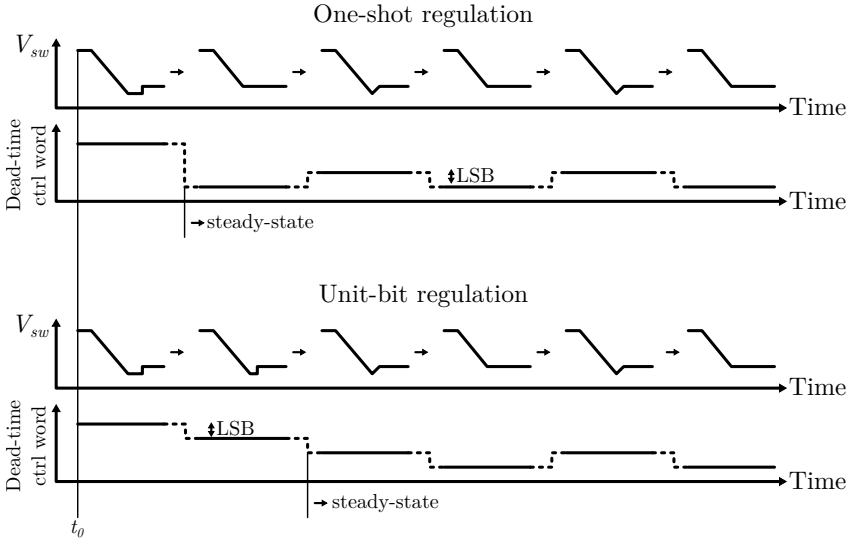

Figure 2.26: Comparison of one-shot and unit-bit regulation in adaptively controlled systems.

2.3.6 Caloric Measurement

An entirely different approach makes use of caloric measurements. By measuring both the input and the output power, the controller can adjust

the dead-time over multiple cycles and target a maximum efficiency. This approach thus guarantees peak efficiency and is also referred to as maximum efficiency point tracking [2].

Tracking for maximum efficiency can be done using numerous methods such as perturb-and-observe or hill climbing, while care needs to be taken to ensure that the global maximum is found. Similarly, maximal efficiency can be targeted through minimising average duty cycle commands, which in turn can be done by optimising the dead-time, ideally in digitally controlled implementations [104].

2.3.7 Gate Current Sensing

All previously mentioned approaches require either high-voltage capability or additional components when used in HV applications. Voltage dividers increase the needed PCB space, component count, implementation time and costs. Furthermore, additional components directly affect reliability, acting as additional potential sources of failure during assembly and operation. In the case of high-voltage converters, these disadvantages further increase, as HV components are more costly, necessitate more PCB area due to isolation requirements, and are more prone to failure.

In the case of integrated converter ICs, the use of additional components can be circumvented by instead relying on HV capable processes and making use of integrated circuits instead. However, these suffer from other, significantly more detrimental disadvantages, such as low bandwidth, high cost, limited device availability and slower (if at all existent) digital performance. Furthermore, as the voltage requirements increase, the approaches become increasingly prone to errors due to ringing and noise affecting the sensing mechanisms. To filter these out, even more external circuitry must be added, further increasing design complexity and cost.

As discussed in Section 2.3.1, a key contribution to the output current during dead-time is attributed to the gate-drain capacitance. As defined by Equation 2.40, this current (I_{Cgd2}) forms part of the gate current (I_{g2}), and can as such be sensed in the gate path. Simple measurement of this current would not immediately imply anything. However, due to the non-linearities in the gate-drain capacitance, which are dependent on the gate-drain voltage as shown in Equation 2.1, information is encoded into

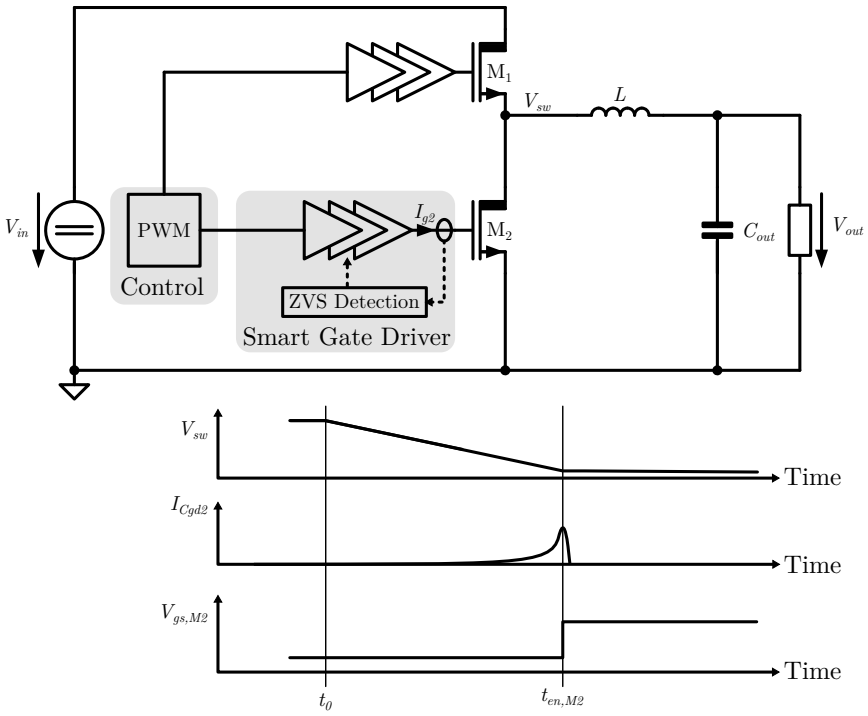

Figure 2.27: ZVS detection mechanism based on gate current sensing.

the current. Specifically, by analysing the gate current, the non-linearities in the capacitance become apparent. By knowing the voltage at which they occur, the voltage across the switch can thus be inferred, which in turn can be used for dead-time regulation. Specifically, the gate-drain capacitance and its change in respect to voltage may peak at 0 V, resulting in the gate current peaking markedly.

This work introduces and discusses this novel approach to ZVS detection that offers numerous benefits compared to established variants. One clear advantage of this innovation is the fact that no supplementary components are required, as the gate-drain capacitance is finding additional use as the sensing component. This also allows for reduced sensing delays, as the measurement, the sensing logic and the corresponding response occur within a single IC. Furthermore, no high-voltage capability is required. In fact, this mechanism has no voltage reliance at all. The non-linearities are there, independent of the applied voltage. The sensitivity to those non-linearities is constant throughout the spectrum, as the sensed quantity is a current.

The voltage at the gate is defined by the gate driver, thus sensing of the current can be incorporated into the driver topology as shown in Figure 2.27, requiring no additional implementation steps for designers, and thereby resulting in a scalable solution. The disadvantage lies in the fact that the non-linearities of this capacitance are defined by the manufacturer of the switch, through the design of the transistor. Thus, not all transistor topologies may be suitable for ZVS sensing in this manner.

CHAPTER 3

GATE DRIVERS

Having introduced both the switches and their applications in DC-DC converters, the main building block bridging the gap between the two is introduced in this section. The gate driver receives the trigger signal from the converter control block and amplifies it to interface with the gate of the power semiconductor. Thus, gate drivers can be commonly found for various applications, specified to the needs of the power semiconductor and the respective use-case, differing in switching speeds, in their ability to drive an entire half-bridge or just a single device, at all relevant voltage levels and with numerous additional safety and reliability features.

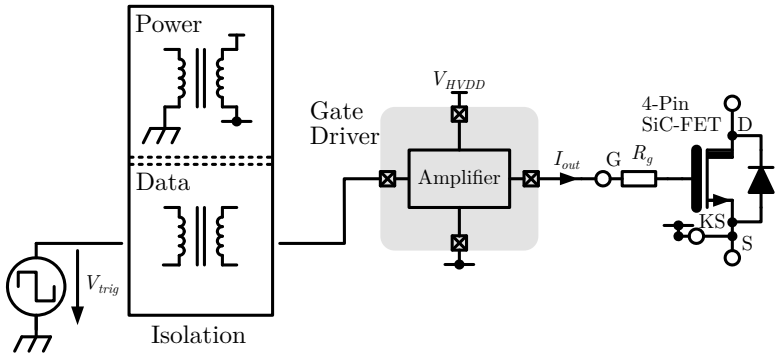

Figure 3.1: Conceptual overview of a SiC Gate Driver.

As the primary role of the gate driver is to apply a voltage between the gate and (kelvin-) source terminal of the power semiconductor, it must also operate in the appropriate voltage domain. This often times means that the ground of the gate driver is (kelvin-) source of the power switch, while a positive supply voltage referenced to this voltage must be available. Gate drivers are therefore galvanically isolated from the rest of the circuit. This isolation and its supply voltage are typically provided by a flyback DC-DC

converter. If the gate driver allows for it, the higher voltage can also be generated by use of a bootstrap diode. Furthermore, the trigger signal must also be transmitted to this voltage domain. Thus, isolation is also required to trigger the driver. Gate drivers can be broadly separated into three categories that are discussed in this chapter.

3.1 Conventional Gate Drivers

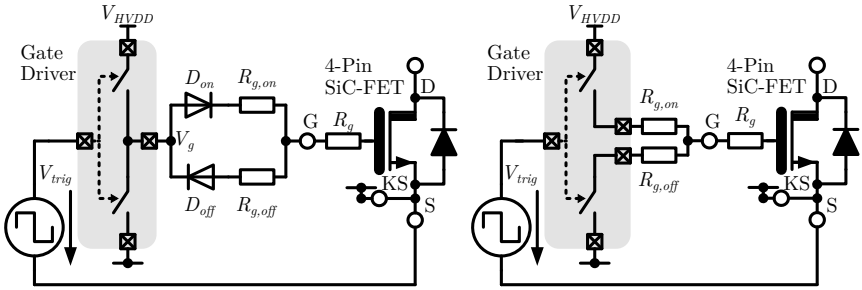

Figure 3.2: Conventional gate drivers using diodes (left) and dual outputs (right) to differentiate turn-on and turn-off dynamics.

Conventional gate drivers provide an output current that is non-controlled. By simply switching the output terminal to its supply or ground, the gate terminal of the device is charged/discharged at the fastest rate possible. The limit in current provided by the driver is typically set by the supply voltage and the internal design of the gate driver, its output resistance, typically originating from the on-resistance of the switch used within the driver. The other limiting factor is the input gate resistance of the switch.

To alter the switching behaviour, in order to e.g. satisfy EMR requirements, an additional resistor can be placed in the gate path, reducing the peak gate current and thus increasing the switching time. This resistor also has use as part of a low pass filter that dampens ringing on the gate voltage induced by the inductance along the gate path. To differentiate the turn-on characteristic of the driver from its turn-off profile, one can make use of diodes to allow the use of two different resistors. Some gate drivers also

provide two outputs, one for turn-on and one for turn-off, thus facilitating the implementation, as illustrated in Figure 3.2.

The simplicity of their implementation leads to very low-cost devices, making them attractive for a lot of simple applications. They are, however, not suited for applications where the EMR reduction obtained by the resistor is no longer sufficient, leads to significant switching losses or to the switching time becoming too long to meet the required performance of the controller.

3.1.1 Inverter-based Gate Drivers

Inverter-based gate drivers make use of cascaded inverters to achieve the wanted output driving strength. Each stage is thereby dimensioned to drive the next stage without acting as a limiting factor in the cascade. This topology is often used on-chip, but rarely for discrete power semiconductors. This is due to the high switching losses associated with each stage, the cumulative propagation delay, and the inflexibility in driving strength.

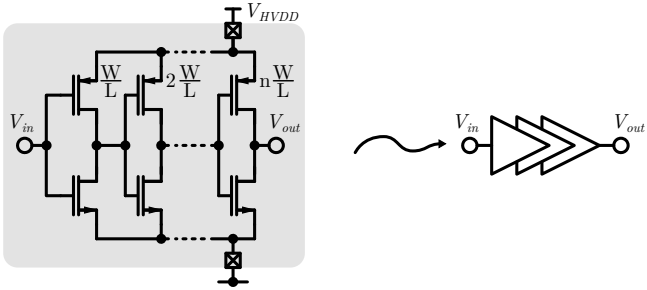

Figure 3.3: Cascaded inverters with a fan-out of two.

3.1.2 Resonant Gate Drivers

By adding an inductor to the gate path, a resonant tank is created. Figure 3.4 illustrates a full-bridge-based resonant gate driver that can be used to recover gate charge by using the inductor L and appropriate driving of the four switches [23]. Resonant gate drivers were introduced to reduce losses associated with the charge and discharge of the gate terminal. The

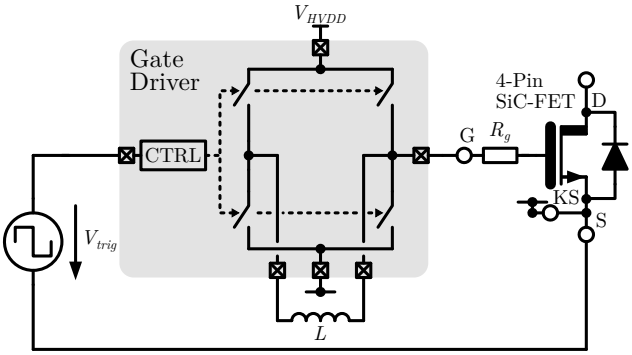

Figure 3.4: Schematic of full-bridge-based resonant gate driver.

inductor acts as an energy storage tank, recuperating the charge brought onto the gate terminal instead of sinking it. They can also be of benefit in high-frequency applications, where large gate currents are needed to achieve appropriate switching times. Furthermore, they may be used to reach gate voltages higher than the supply. This can be used to drive transistors that require higher voltages, such as SiC switches. As inductors are difficult to integrate, this topology adds an extra external component to the gate driver, as well as significant additional complexity through its control mechanism.

3.2 Active Gate Drivers

The second category contains active drivers, acting in a limited closed-loop configuration. These are either voltage, current or resistance based. The three output variants are illustrated in Figure 3.5. The advantage of active topologies lies in their ability to actively control their output throughout the switching transition, depending on the current state of the transition, with a set, pre-defined change in behaviour. An example of this application would be to increase the driver's output strength at the Miller plateau to increase switching speed [68], or to reduce driving strength towards the end of the transition to reduce ringing caused by overshoot due to the gate inductance [74].

For this reaction of the driver to occur, some feedback signal is required.

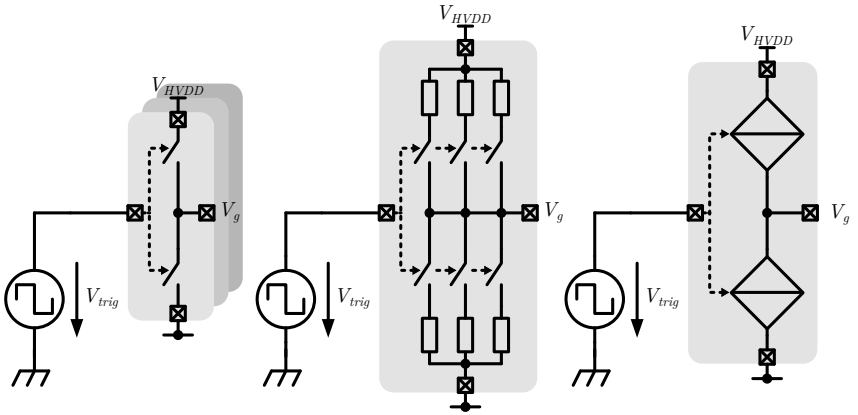

Figure 3.5: Conceptual schematics of three topologies of active gate drivers.

This could be in the form of the gate voltage being sensed, to allow for Miller plateau detection, or the voltage across the kelvin-source inductance as an indicator of switching transition slew rate [56]. Furthermore, protective features such as overvoltage and overcurrent protection can be added to the driver by making use of this feedback.

3.2.1 Voltage Based Drivers

Voltage-based active drivers are similar to the conventional drivers but make use of either multiple output stages that can be activated throughout the transition [70, 45, 22, 52], or use PWM to modulate the output [8]. Alternatively, the output voltage can also be varied throughout the transition through variation of the supply voltage [21].

3.2.2 Resistive Gate Driver

Resistance-based drivers are similar to voltage-based drivers, but instead of layering multiple output stages, the actual resistance in the output path is varied. This can be done by using actual resistors in the output path that are connected/disconnected throughout, or by varying the on-resistance

of the switch through the gate-source voltage applied to obtain a specific resistance [50, 88, 46]. Designers must keep in mind the trade-offs and concessions made in poor matching performance of on-chip resistors and the high thermal dependency of the on-resistance of MOSFETs.

3.2.3 Current-based Drivers

Current-based drivers make use of current sources and sinks to provide a mostly constant output current. Similarly to voltage and resistive drivers, in the active form, the sources can either be varied [68] or multiple constant stages can be combined to vary the total output current. Figure 3.6 illustrates a simple current-based driver. A control block selects which of the current sources are activated, biasing them to provide their respective output current value, summing to the total output current I_{out}.

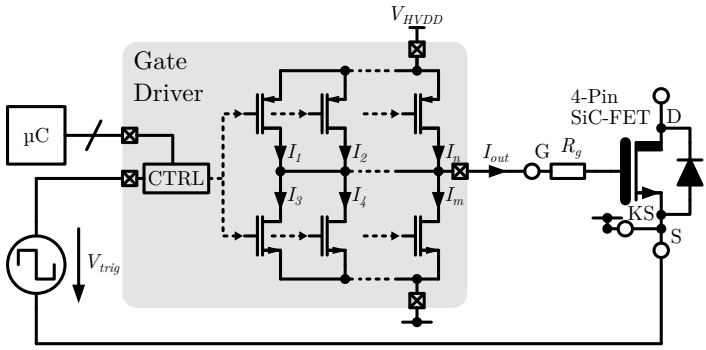

Figure 3.6: Conceptual schematic of current-based gate driver using MOSFET as sources and sinks.

Due to the implementation of current sources in ICs, the term current-based is only valid to a point. The current is typically provided by current mirrors. The output current is thus only voltage independent to a certain degree, limited by the channel modulation factor of the transistor. Furthermore, as the voltage across the switches decreases, the supplying switch leaves its saturation region, and thus the output impedance drops significantly. The

current source driver thereby acts more as a resistive gate driver, blurring the differentiation, and resulting in significant deviation of the output value.

Current-based drivers have significant advantages. In contrast to previous topologies, matching and temperature dependency are not critical contributors to variance in output values. Furthermore, the output can be calibrated easily if desired and the voltage dependency can be, relatively speaking, much lower for a large section of the transition.

Lastly, the valued modularity comes without the burden of significant additional complexity. Through scaling of the transistors, matching stages providing different current levels can easily be created, while simply adding more stages scales the output current linearly. This reduced implementation effort, in combination with all the previously mentioned advantages, make them a popular choice for active gate drivers.

3.3 Programmable Gate Drivers

The third category is referred to as programmable drivers. The driving topologies remain the same ones previously mentioned. The distinction comes from the feature-set. Often times pre-programmed, these can directly incorporate feedback from the current or previous transition and then adapt their driving profile following a specific optimisation. They operate in a closed-loop, targeting a specific objective, such as minimal ringing or to meet a dv/dt target, as illustrated in Figure 3.7. Being programmable, they often interface with an external controller that can be used to set a profile that is executed upon receiving a trigger signal and can be optimised for a specific transistor model [106, 38].

While in research and academic applications the feedback and optimisation may occur using additional sensors and FPGAs/microcontrollers, integrated solutions can incorporate the sensing and optimisation internally. One such approach uses multiple profiles stored internally that can be executed depending on the measured signal [45].

This makes these drivers much more feature complex and thus cumbersome to implement. At the same time, they offer designers the widest range of flexibility when it comes to controlling the gate voltage. Programmable gate drivers are further characterised by their temporal and driving strength

resolution, as well as their voltage rating, to fit the requirements of the targeted semiconductor.

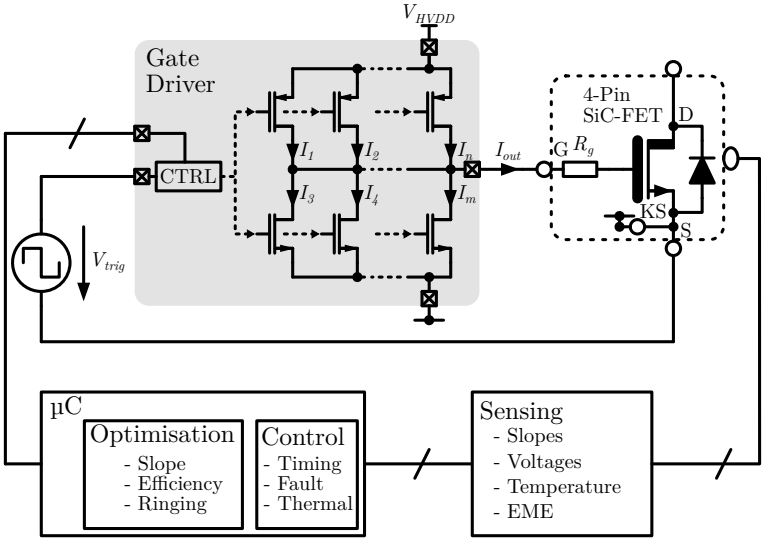

Figure 3.7: Conceptual overview of programmable gate drivers in closed-loop configuration.

3.4 Fully Integrated Gate Driver

The following section presents a fully integrated gate driver application specific integrated circuit (ASIC), developed at IAS. It represents a third generation active gate driver, incorporating the experience and results gained from previous versions into its development. The design goals were multiple: a variable output voltage allows for an appropriate solution for all common power switches. This is enabled by a flyback converter, whose control mechanism is included in the ASIC. The IC must also feature sufficient temporal resolution to drive fast-switching GaN HEMTs. This is enabled by the use of a high-speed clock and control loop. Lastly, the driver output stage is based on the current-mirror topology, enabling programmability and modularity of the output current.

3.4.1 Isolated Supply

A simplified overview of the integration of the flyback control stage is presented in Figure 3.8. The flyback single-inductor, multiple-output (SIMO) features five output voltages: V_{PMU_HVDD} which is variable from 20 V down to 6 V, V_{PMU_AVDD} which is regulated to 5.5 V, V_{PMU_DVDD} which is regulated to 1.8 V, $V_{PMU\_GND\_KS}$ which is the kelvin-source potential of the output switch and V_{PMU_HVSS} which is variable from 0 V to −5 V. To provide the ability of using 5 V transistors in the high voltage domain, a further voltage rail, V_{FVSS}, is generated from the high voltage supply V_{PMU_HVDD}, lying 5 V below it.

The ASIC can thereby supply SiC MOSFETs with driving voltages of 20 V to −5 V, sensitive GaN HEMTs with ranges from 6 V to 0 V as well as everything in-between. This provides applications of the IC ample flexibility to switch all commonly used power transistors, within the broad range of trade-offs in performance or longevity optimised profiles.

V_{PMU_AVDD} is used to supply the internal 5 V rails for analog and digital circuitry, I/O cells as well as the power rail for the current mirrors used in the output stage. The multiple rails are regulated by internal low-dropout regulators (LDOs), providing isolation from each other for noise and ripple suppression. V_{PMU_DVDD} is similarly used for the internal 1.8 V rails for the clock synthesis and the majority of digital logic.

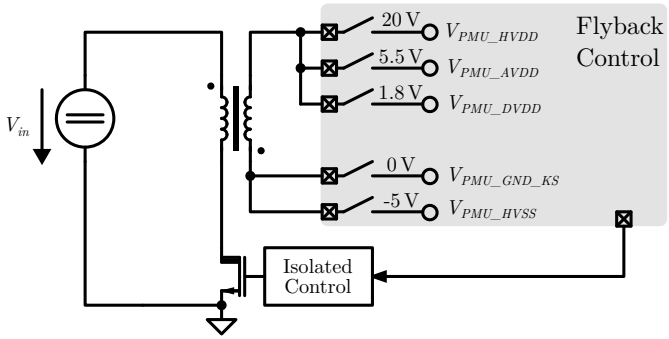

Figure 3.8: System overview of SIMO flyback integration within the gate driver ASIC.

Note that the voltages presented here are effectively referenced to the kelvin-source potential of the switch, for easier understanding. In reality, the voltages are regulated in reference to V_{PMU_HVSS}. Thus, $V_{PMU\_GND\_KS}$, for example, is regulated to 0 V to 5 V above V_{PMU_HVSS}.

Through the deep integration of the converter, the ASIC requires only minimal additional components, consisting of a coupled inductor for the isolation, a primary side switch as well as an isolated driver for the switch. Commercially available solutions also exist containing both in one package, minimising additional component footprints [10]. The IC only requires a single 15 V primary-side supply, labelled V_{in}, enabling a compact solution.

3.4.2 Driver Stage

The driver stage is implemented as a distributed current mirror, as illustrated in Figure 3.9. This topology offers numerous benefits, as discussed in Section 3.2.3. Due to the benefits of the silicon-on-insulator (SOI) technology used for this ASIC, the individual current mirrors can be effectively isolated from each other, without requiring cumbersome isolation/blocking wells used in conventional HV BCD technologies. This allows the driver stage to be implemented through the use of modular blocks, that can be added as

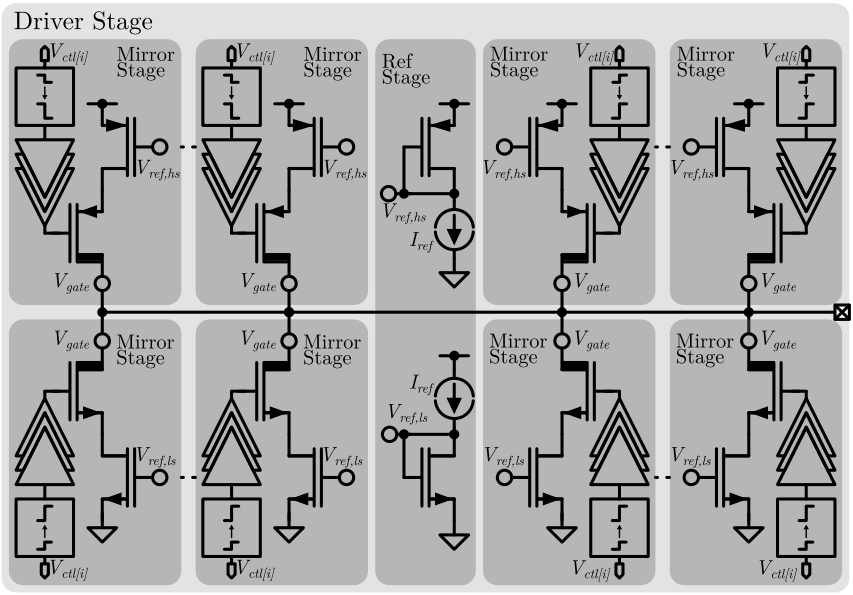

Figure 3.9: Topological overview of the output current mirror-based driver modularity of the implemented gate driver ASIC.

one pleases, to fill up available area or to meet driving strength parameters, in this case resulting in 32 stages in the final design.

Mirror Stages

Each block contains both the low-voltage mirror transistor, acting as the current source/sink, and the high-voltage blocking transistor protecting it from the high/low gate voltage, as well as the drivers and the required level-shifters. To overcome the challenges faced in timing of the switching events of each individual stage, the focus of this implementation lied on reducing the delay of each current mirror to turn on or off.

The main challenge faced in the design of the driver stage is the gate capacitance of the high-voltage blocking transistors. Substantial amounts of charge must be brought to and off of the gate terminals to enable or disable the individual stages. The main goal was therefore to reduce the gate area, while remaining within the technological electromigration (EM) rules of interconnecting metal layers and vias. The low-voltage mirror transistor is thus also minimised in size, to match the current density of the high-voltage transistor. This reduction in gate area, however, requires a higher gate voltage to drive the necessary current. The limitations faced hereby is the current density in the layout stage. This limits the gate voltage, which in turn limits the minimal gate area. Through careful considerations and layout, the enable/disable time was reduced to just 100 ps to meet the target of the gate driver. This in turn also sets the requirements for the level-shifter output stage, driving the high-voltage blocking transistor.

Reference Current Mirror

Acting as a current reference is a simple non-cascode diode-connected MOSFET M1 in Figure 3.10. I_{ref} is provided by the IC's Power Management Unit (PMU). It is used to generate a reference current of around 1 mA within the reference stage, which is then mirrored out to the mirror stages of the driver by M8. The current mirror ratio to the driver stage is chosen as 1:128.

This value is very large for a current mirror, resulting in large deviations in the output current from the theoretical nominal value of 128 mA. However,

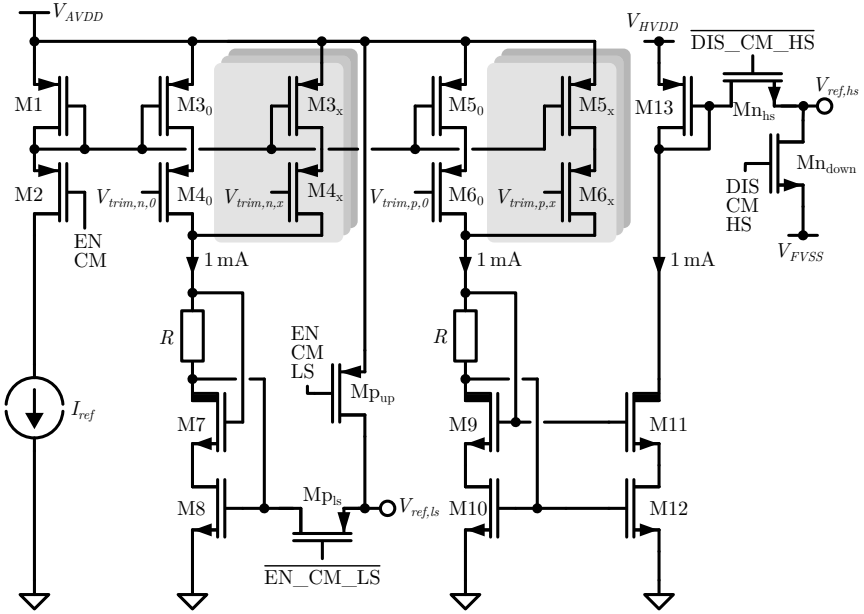

Figure 3.10: Schematic of current mirror reference circuit for high-side and low-side mirror stages.

as the actual nominal value is not of much significance, this error can mostly be ignored. Overall, this ratio is thus beneficial, as it reduces ohmic losses within the driver stage due to the reference current being enabled continuously.

Nevertheless, the reference current stage is implemented using multiple transistors of different widths, connected in parallel, which are labelled M3, and can thus be calibrated should a desired nominal output current per stage be desired. What is however of interest, is the similarity of p-channel metal-oxide-semiconductor (PMOS) and n-channel metal-oxide-semiconductor (NMOS) sources. Thus, care was taken in both the design as

well as the layout of the reference stage to ensure matching of both through the use of large areas, common centroid arrangements and numerous dummy structures. To provide a reference current to the PMOS current sources of the driver stage, the reference current is also copied to M5, using the same topology as previously to ensure matching. The current is then mirrored to the high-side using M10 and M12 as a current mirror, and M11 as a blocking transistor. The actual reference transistor is thus M13, which has the same area scaling to the PMOS driver stages as M8 has to the NMOS stages. Furthermore, the PMOS stage supports similar trimming using M6, and can thus be calibrated.

The reference diode voltages are not immediately connected to the driver stage. To provide the possibility of unregulated source/sink behaviour, thereby acting as a voltage-based driver, the current mirrors can be entirely disconnected using the digital EN_CM_LS and DIS_CM_HS signals at $\mathrm{Mp_{ls}}$ and $\mathrm{Mn_{hs}}$. Simultaneously, $\mathrm{Mp_{up}}$ and $\mathrm{Mn_{down}}$ pull the respective voltage node to V_{AVDD} or V_{FVSS}, thus fully enabling the driver stage mirror transistors. This mode is not intended for continuous use, as EM violations as well as thermal load will cause faster deterioration of the IC.

While the nominal output current value is not of major significance, the linearity of the stages to each other is. Thus, interference of stages with each other should be cared for, as well as matching of the stages ensured. The latter was done by choosing low voltage (5 V) transistors as mirror transistors and not HV ones, which feature much worse matching performance, while the former was enhanced by making use of large RC filters between the individual stages as shown in Figure 3.11.

When a single stage is enabled, a large current inrush through the gate-drain capacitance shifts the gate voltage of the mirror transistor to a different value than the one set by the reference transistor. This causes the settled current to deviate from the one set by the current mirror ratio. To minimise this effect, the gate terminal is supported by adding as much capacitance as possible between it and its source node ($C_{dc,ls/hs}$), while a large resistor is added in between it and the reference transistor voltage ($R_{dc,ls/hs}$) to prevent the change from propagating to other stages.

The resulting RC filter thus limits the effect of a single source mostly to itself, while maintaining linearity of sources to each other. Note that this isolation of sources also results in the reference current mirror not being able to rapidly absorb this inrush of current to return to the nominal diode

voltage. However, in order for it to effectively deal with this inrush, it would have to react within the rise time of the source, i.e. in well less than 100 ps, with a simultaneous inrush on all sources. This would require a reference current orders of magnitude larger than the chosen 1 mA. The higher reference current would result in tremendous static losses, as well as much larger surface area requirements to meet EM rules as well as ensure minimal IR drop, making this approach impractical. However, as all sources are affected equally, the effect essentially causes a shift in the nominal output value, which, as previously discussed, is not of great significance, and can be calibrated for if desired. The only relevant operating point for this increased settling time is during initial startup of the IC, when the reference current mirror has to charge all mirror stages to the nominal diode voltage. During startup, however, other procedures with far greater time constants take place, thus making it a non-issue.

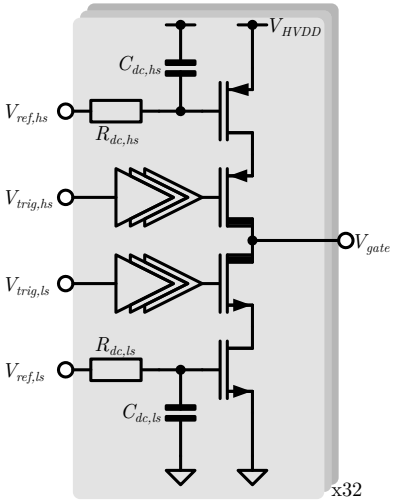

Figure 3.11: Inter-stage filtering of mirror stages within the driver stage.

Level-Shifter

The high-voltage PMOS blocking transistor in the high-side current mirror stages requires a negative gate-source voltage to conduct. It operates in the high-side voltage domain, defined by V_{HVDD} and V_{FVSS}. Thus, to interact with it, signals must be shifted from the V_{AVDD} domain to this higher one. This task is performed by the level-shifters. The design of the level-shifters goes hand-in-hand with that of the current mirror, as the level-shifter output acts as a driver of the HV blocking transistor. Thus, the dimensioning of this output stage directly affects the overall performance of the driver stage. The primary task, however, lies in acting as a voltage shifter, to address the PMOS current mirror in its voltage domain.

As the primary target of this output stage is programmability, the end-user should interact with a reliable and consistent interface. Thus, the performance of the current mirror stages should be independent on it being a PMOS or an NMOS source. Matching of the two was therefore considered a key design goal. In accordance with this, both current mirrors are driven by the same level-shifter, such that signal delay is matched. While the low-side level-shifter shifts from the V_{AVDD} 5 V domain to the same 5 V domain, the high-side version shifts from the 5 V domain to the 20 V one. This generates another design challenge for the level-shifters. They should function reliably for both voltages, and all in-between as V_{HVDD} is designed to be variable down to 6 V.

To ensure reliable operation across voltage ranges, temperature, and process corners, the level-shifter uses HV transistors to clamp the low-voltage 5 V input transistors. The implemented schematic is shown in Figure 3.12. The design is based on the known cross-coupled latch design previously proposed by [53], with adaptations and improvements for this specific application.

On a rising edge on the input signal IN, the pulse generator circuit, featured in the lower part and consisting of inverters and NAND-gates, generates a pulse at the gate of HV transistor M1 through the signal delay introduced by the uneven use of inverters. The pulse length is set to be sufficient to pull down the gate voltage of M3, thus initiating the transition. The pulse length can further be doubled by manually setting DOUBLE high. Although the design was verified in all conditions to function nominally, as this is a critical component of the IC, the precautionary addition of this doubling of pulse length was implemented nonetheless.

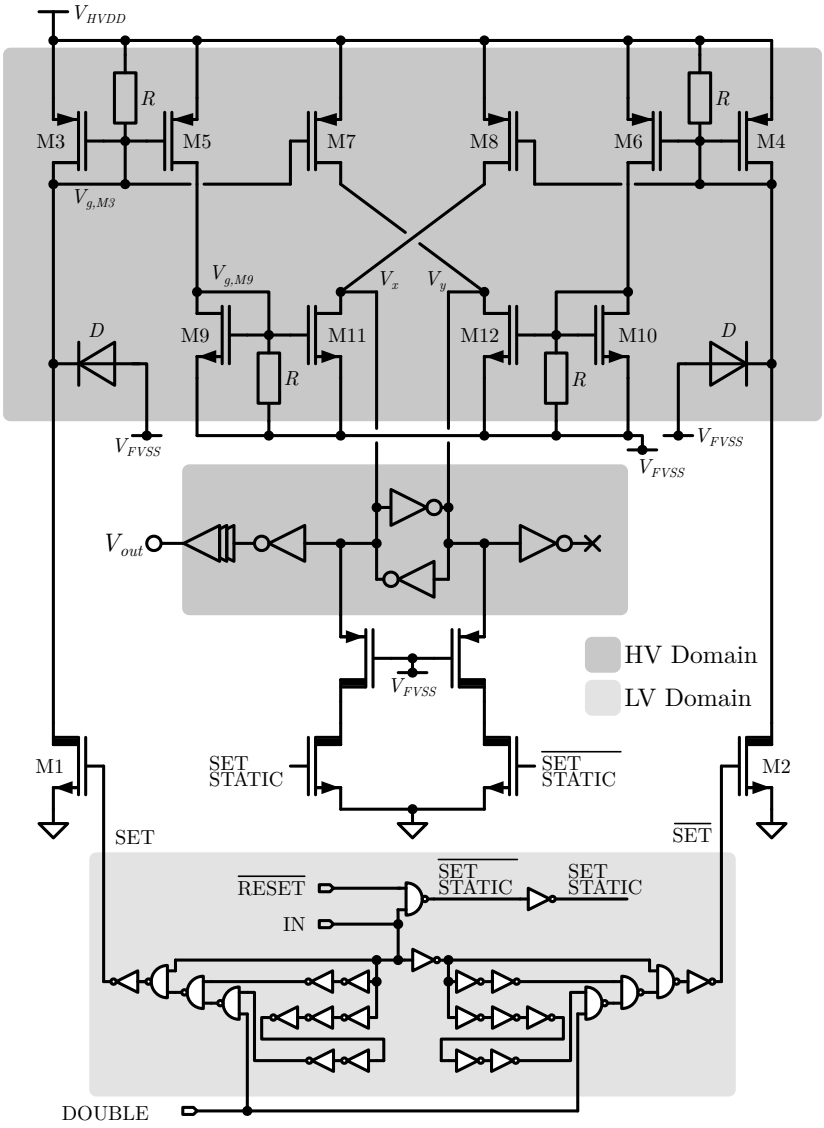

Figure 3.12: Schematic of implemented level-shifter with highlighted voltage domains.

Through enabling of M3, the gate of M5 is pulled low. Once M5 is turned on, this pulls up $V_{g,M9}$ enabling M11, which in turn pulls down V_x. Simultaneously, M7 is enabled and pulls up V_y. The self-enforcing inverters are forced to toggle, driving V_{out} high. Thus, a rising edge of the input enables the output. The inverse transition, on the other side of the circuit occurs for the falling edge of the input, disabling the output.

Large resistors R are added to the gate terminals of M3, M4 and M9, M10 to ensure that the operating condition returns to a defined state after a trigger event. To ensure that $V_{g,M3}$ is not pulled below the minimal V_{FVSS}, thus damaging M3, a diode D with sufficiently small turn-on delay, is connected to $V_{g,M3}$. The same is done for M4.

This level-shifter is transition-triggered, meaning that it faces the same obstacle as capacitively coupled level-shifters, in that the static operating state of the input is not enforced on the output. During startup of the IC, this may be an issue, as the input may be high but, the edge not having been detected, the output remains low. Only on the next rising edge would the level-shifter trigger. To circumvent this, additional HV transistors were added which are driven by the SET_STATIC and its inverse. These ensure that the static condition of the level-shifter is properly defined. Simultaneously, the level-shifter can now be put in a defined RESET state during startup, ensuring that the driver stage is disabled and not causing increased current consumption which may inhibit the startup procedure of the voltage rails. This implementation has the advantage of having no static current consumption, as no path will conduct for longer than is defined by the pulse length set or until the output has toggled. Although static current consumption is not of major concern for gate drivers, a low power solution is always favourable to reduce on-chip temperature and overall system efficiency.

Overall, the level-shifter has a delay of 1.16 ns to 2 ns across required operating voltages, process corners and temperatures from −40 °C to 150 °C, measured from 10% rise of the input signal until 90% of the output change is reached. Nominal delay is not a critical parameter of the driver, as it has to be calibrated for in the external controlling microcontroller in any case, as multiple other sources of delay exist, mainly in the custom digital driver control. However, minimising it is still desirable to enhance usability. The critical parameter of delay mismatch between rise and fall transitions remains below 15 %, ensuring consistent performance.

3.4.3 Floorplan and Performance Analysis

Figure 3.13 presents an optimised floorplan of the entire IC. The PMU contains the control for the flyback converter as well as the LDOs providing the different voltage rails, current reference circuits, the bandgap reference providing the reference voltage for all other regulators [97] and control circuitry for reliable and consistent startup of the IC. The appropriate pins are thus placed along the top left corner of the IC. The used SOI technology allows the use of multiple grounds throughout the ASIC. This enhances performance through isolation, reducing cross-coupling noise. To ensure that the different grounds maintain the same DC voltage, down-bonds connect them to the conductive, exposed pad of the package, acting as the neutral point of the star arrangement.

The digital logic of the IC is placed in the centre. This was chosen strategically to allow interfacing with all other components without having to route signals across the entire IC. External interfacing is provided by just six pins, four for communication through SPI, RESET and TRIGGER, which thus require insubstantial routing effort. The reference clock is generated by a phase locked loop (PLL) placed just beside it, while a custom digital block is seated right next to the output driver stage. This stage acts as the controlling logic of the driver stage, deciding which stages to turn on or off at what timepoint.

An output buffer allows the output of multiple internal signals in combination with an internal multiplexer to be evaluated in testing and debugging. An Analog to Digital Converter (ADC) is placed at the top, allowing the IC to sense various signals of interest. These include various internal voltages to enable internal calibrations as well as the gate, drain, source, and kelvin-source voltages of the driven power MOSFET, allowing the IC to act as a programmable driver in the intended closed-loop feedback system.

By not constraining the driver stage to a corner, but instead placing it along an entire side of the IC, the top metal supply, output, and ground connections are easily placed and routed as rectangles, forming homogeneous structures with uniform current density profiles. This also allows for a low IR drop, as many pads can be placed in parallel throughout the top metal's height, as well as improving EMI due to the well-defined straight-line current flow direction.

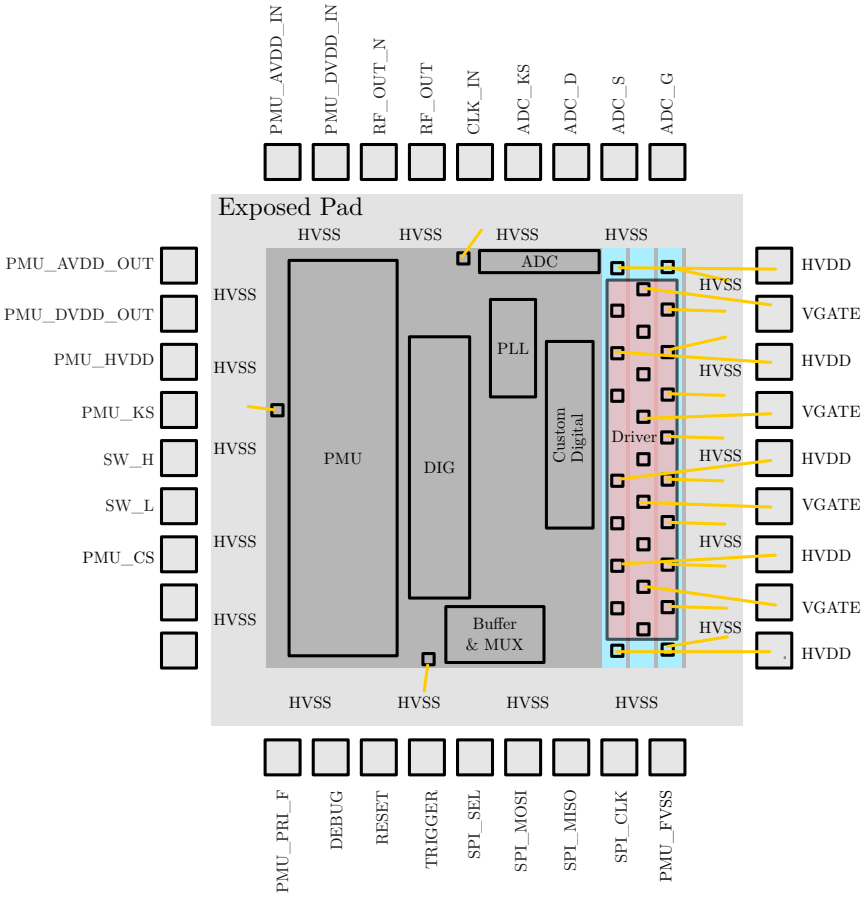

Figure 3.13: Planned floorplan in QFN36 package with conductive exposed pad and bonded driver stage.

Furthermore, the overall inductance of the output stage can be reduced, as the current flow of the HVDD pins and the VGATE pins are in opposite direction. The same applies to HVSS, although the much lower profile down-bonds are expected to have less of an effect. Figure 3.14 illustrates the equivalent schematics, highlighting the current loop formed by the output stage during charging and discharging of the gate.

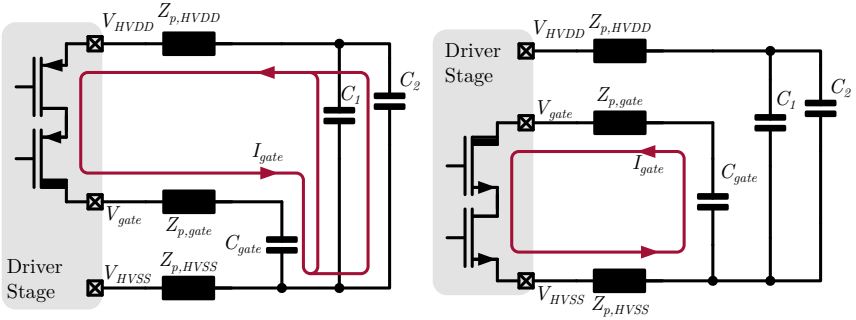

Figure 3.14: Current loops formed by the driver output stage.

The output inductance is the main parasitic parameter limiting gate drivers' dynamic performance. It limits the speed at which the output current can ramp up to the desired value and introduces ringing through parasitic resonant circuits. Stray inductances increase with the area encircled by the current loop. Minimising this area is therefore the main goal to improve the driver's performance. The height of the bond should therefore also be reduced as much as possible. However, this is a parameter of the bonder and often not a variable that can be influenced in academic environments. Thus, an industry standard profile is assumed for the following analyses.

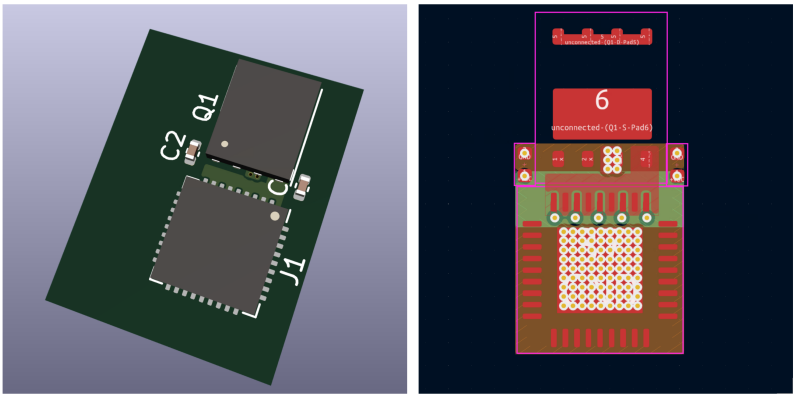

Figure 3.15: Implementation of the ASIC on a PCB using minimal arrangement in 3D (left) and the corresponding layout view (right).

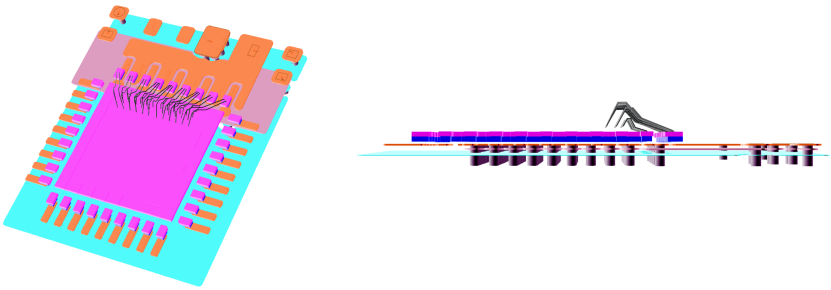

Figure 3.16: Corner view (left) and side angle view (right) of the PCB layout and bond wires used in ADS.

Performance Analysis

Figure 3.15 illustrates the planned configuration of the IC's implementation. The IC (J1) is placed as close as possible to the driven MOSFET (Q1). In order to obtain a proper representation of parasitic influences on the driver stage, alongside the packaged IC, two decoupling capacitors (C1 and C2) are placed on the left and right side. These would ideally consist of ultra-low inductance capacitors, closing the loop between V_{HVSS} and V_{HVDD}. The driven transistor is placed as close as possible to the output stage.

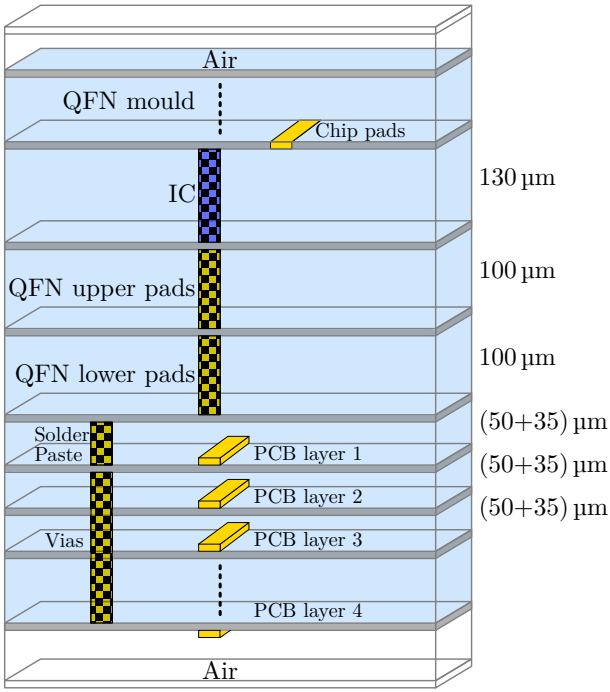

Figure 3.17: Layer stack used for ADS simulation of the ASIC driver stage.

Figure 3.16 presents a three-dimensional view of the implemented driver stage of the IC, with bonds placed as drawn in the floorplan, ensuring that

no shorts are created between overlapping bond wires. The chosen package is a quad flat no leads (QFN) 36 package, with nine pads on each side.

The driver's output gate signal V_{gate} is connected to the top PCB layer and traced directly to the gate contact of the power switch. V_{HVDD} is found on the second layer of the PCB, with the ground layer V_{HVSS} placed on the third. An overview of the used stack is shown in Figure 3.17.

Three layers of PCB metal are used, with an industry standard separating distance of 50 µm and copper conducting traces. Reducing the distance between these layers is key to reducing the overall loop inductance. Thus, a thin four-layer PCB should be used, or a six layer PCB with the three top layers being of close proximity. The solder paste layer contacts the PCB metal to the pads of the QFN package while bond wires then bridge the gap between the IC and the pads within the QFN mould. The down bonds connect to the conductive exposed pad of the package, which is connected to the ground plane through as many vias as can fit within the exposed pad region. V_{HVDD} is connected to the second plane with vias in close proximity to the pins, within the package footprint. Using this layout, ADS was used to generate an S-parameter model that contains the parasitic impedance formed by the current loop. This model can then be placed within the ideal current loop, acting as an in-path impedance similarly to the ones illustrated in Figure 3.14.

Figure 3.18 and Figure 3.20 illustrate simulation results using the mentioned parasitics and an ideal capacitance at the gate node, instead of a SiC or GaN transistor, to act as a just reference. The driver stage is enabled to its maximum (regulated) output current strength for a duration of 50 ns. Figure 3.18 illustrates the charging phase of the gate, i.e. when charge is being added to the gate terminal, causing a rise in voltage. The output current, I_{gate} is therefore positive, charging the gate (capacitor), $V_{gate,pad}$, to around 6 V. What is clearly apparent, is a large current overshoot occurring when the current stage is enabled. The current settles to the target value of around 4 A within 1.3 ns, while having a rise time of around 200 ps.

$V_{bw,gate}$ represents the voltage difference between the pad of the gate terminal and the end of the PCB trace. A voltage drop of 35 mV can thereby be attributed to the bond wires and PCB trace, which results in a resistance of around 9 mΩ. Further optimisation can certainly be done in order to reduce the enclosed loop area further, however, the resulting gate path inductance of only 0.5 nH attests to the quality of this topology. Of interest is also

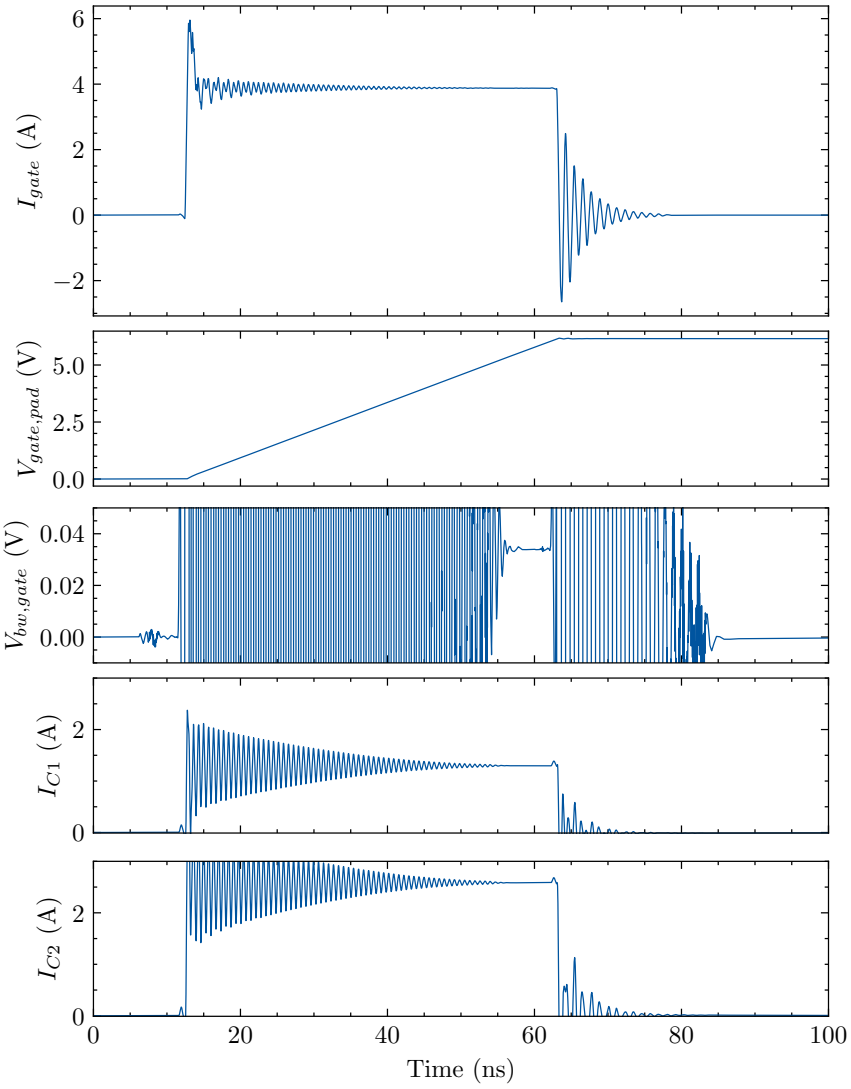

Figure 3.18: Simulation results of enabled NMOS sources with added parasitics in the IC's output current loop.

the origin of the current flowing from V_{HVDD}. Due to the symmetrical layout of the output stage as well as the two decoupling capacitors, one would expect the current to be split almost evenly. The results, however, show that around two thirds of the current flows through the right (viewed from above) loop I_{C2}, and only one third through the left (I_{C1}). This is explained by the fact that the gate contact of the power switch is located on the right side of the PCB, causing the right current loop to have a lower resistance than the left loop.

A comparison to the final implementation using post-layout extracted schematics but no bond or PCB parasitic components is shown in Figure 3.19. While the performance degradation is substantial, it is unavoidable in such a bond wire packaged ASIC due to the inherent inductance of the bonds.

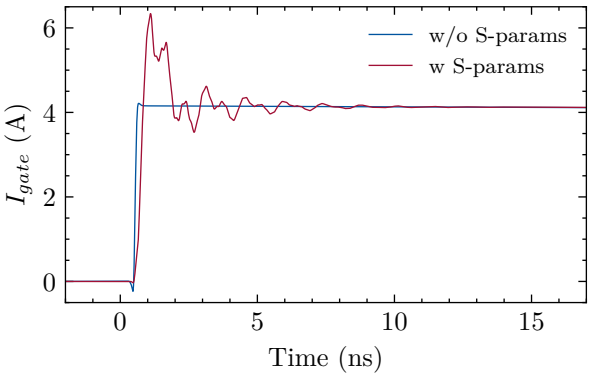

Figure 3.19: Comparison of full output driver stage enablement with and without added parasitics.

Similar performance can be seen on the discharge phase of the output stage, presented in Figure 3.20. Note that the current is now displayed as negative, due to the PMOS stages being enabled. The output voltage is thereby reduced from an initial 15 V to around 9 V, as the driving strength is matched to the charging transition. While the voltage drop on the output bonds is the same, the much lower voltage drop across the down-bonds and the exposed pad ($V_{bw,HVSS}$) is noticeable, and to be expected due to their much shorter length as well as there being more of them.

While the rapid, extreme transition presented show the driver in its most

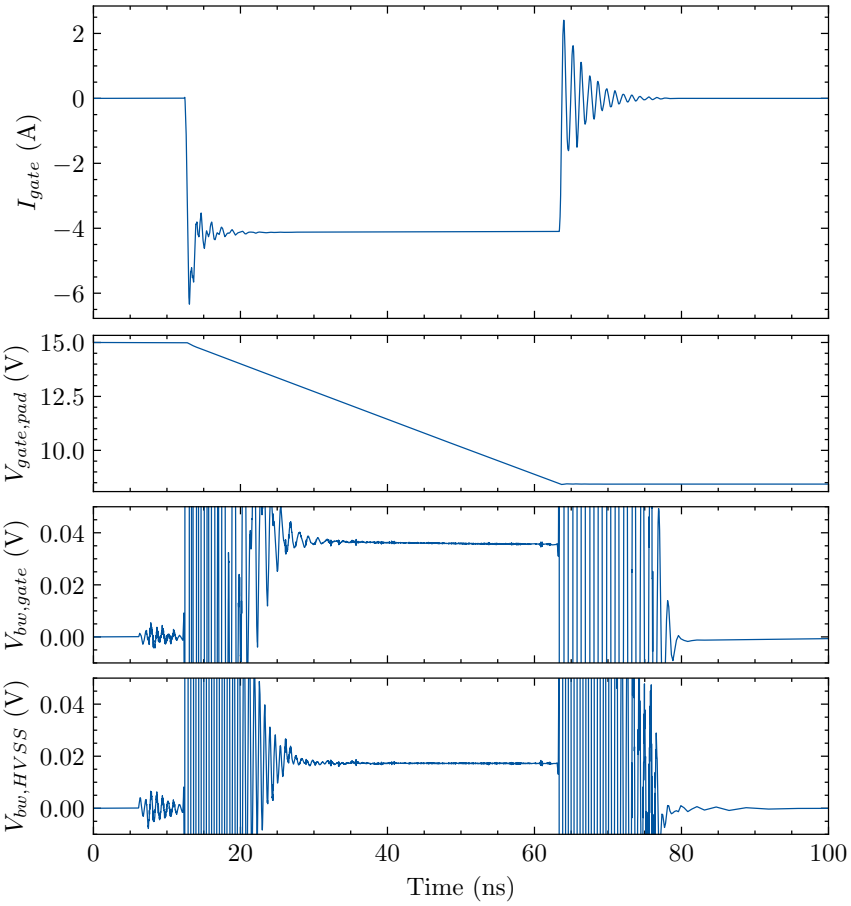

Figure 3.20: Simulation results of enabled PMOS sources with added parasitics in the IC's output current loop.

challenging operating condition, this is not an expected application. To illustrate the linearity offered by the driver, Figure 3.21 shows the driver undergoing a linear increase in output driving strength (PMOS and NMOS), showcasing the expected 100 ps rise time of the internal output current. While the parasitic inductance of the bonds and traces prevent the rapid transitions, the linear increase is present, at the expected rate. Ringing is thus also much reduced.

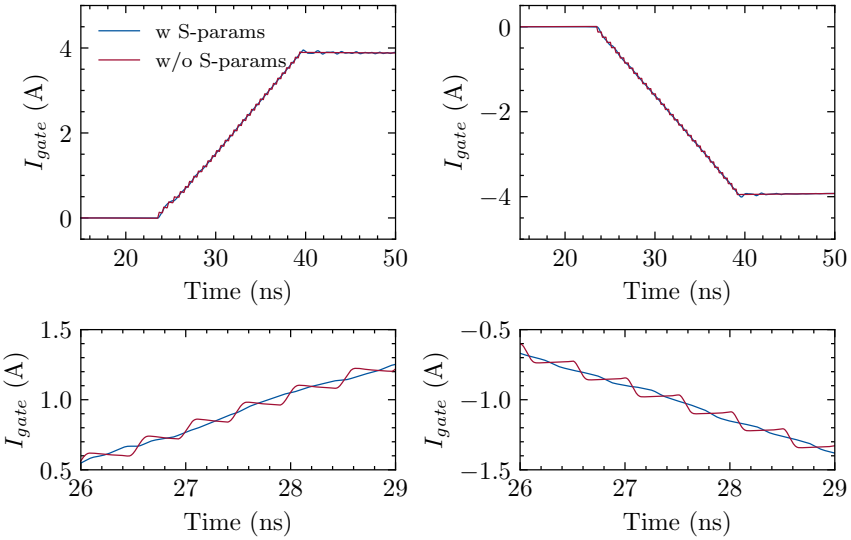

Figure 3.21: Post-layout extracted simulation of linear increase in driving strength, with and without added parasitics, for PMOS (left) and NMOS (right), with zoomed in sections (bottom).

The main motivation behind the ASIC is gate-shaping. Figure 3.22 presents a shaped profile that reduces the driving strength around the (expected) Miller plateau to reduce associated EMI. This is done in multiple steps, so as to achieve a smooth output voltage transition. The bottom plot illustrates the control word, representing the ideal current profile. The top curves illustrate the profile applied to the charging PMOS stages using post-layout extracted models, with and without the added parasitic components, as well as the corresponding NMOS stages. The current sources thereby show good performance, with the PMOS turn-off transitions showing slightly

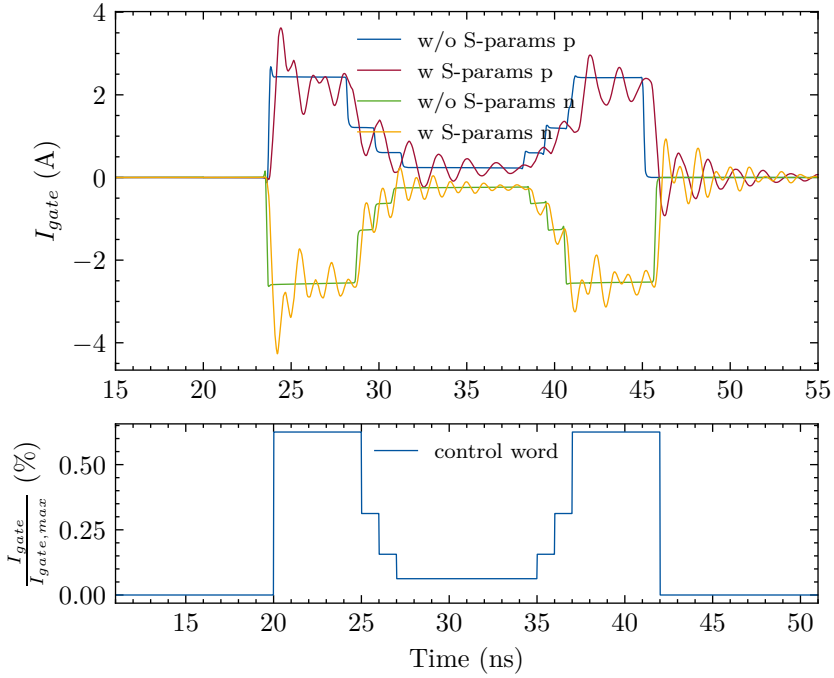

Figure 3.22: Comparison of output driver stage enablement using Miller-reduction profile with and without added parasitics.

slower performance than the NMOS stages. This is attributed with the higher gate-source voltage experienced by the PMOS transistors. While the parasitic ringing is once again substantial, the profile is recognisable.

The simulation results illustrate the necessity of such extractions. Typical values of 2 nH per bond wire cannot be assumed, as the effects of cross coupling of bond wires as well as their parallel reduction cannot be estimated accurately. The driver stage delivers respectable performance for a bond wire packaged IC. Significant further performance deterioration is not expected to originate from the internal layout of the ASIC, but rather from the remaining PCB layout as well as the parasitics found within the package of the driven transistors. To achieve better performance, one would resort to a different packaging method, such as flip-chip. This would eliminate

the bond wires, resulting in much lower output impedance. Commercial applications have offered these solutions, however for academic purposes they remain difficult to obtain.

CHAPTER 4

DISCRETE IMPLEMENTATIONS

In order to validate the theory previously presented, two discrete converters were implemented: one based on SiC MOSFETs and one based on GaN HEMTs. The core concept of all discrete implementations lies on the buck converter topology discussed previously. This therefore necessitates a half-bridge circuit with an inductive load, that acts as a testbench, facilitating a switching environment, where the effects of soft-switching, hard-switching and all intermediate variants can be measured and evaluated. The following sections describe and evaluate both systems. The discrete implementations act as a stepping stone to an integrated implementation, presented later, demonstrating the feasibility of the approach, and were previously published in [99].

4.1 SiC - Based Buck Converter

The first demonstrator is based on a SiC switches. Figure 4.1 shows a block-level overview of the converter and the required surrounding circuitry implemented to validate the proposed mechanism.

4.1.1 Implementation

The design, based around a half-bridge, is made up of two Wolfspeed C3M0045065K switches [17] M_1 and M_2. These power transistors are meant for relative high voltage applications, providing a maximum switching capability of 650 V and 49 A with an on-resistance of 45 mΩ.

Figure 4.2 shows the implemented PCB. The two switches are seen standing upright, with the gate driver to their left. R_2 and R_5 act as gate resistors (equivalent to $R_{g,hs}$ and $R_{g,ls}$ in Figure 4.1), while the low side has a second resistor that is used for the sensing mechanism (R_{sns} in Figure 4.1). The two switches are driven by an EiceDRIVER 2EDF7275K gate driver [24], providing two isolated outputs, $V_{g,hs}$ and $V_{g,ls}$, one for each switch. It

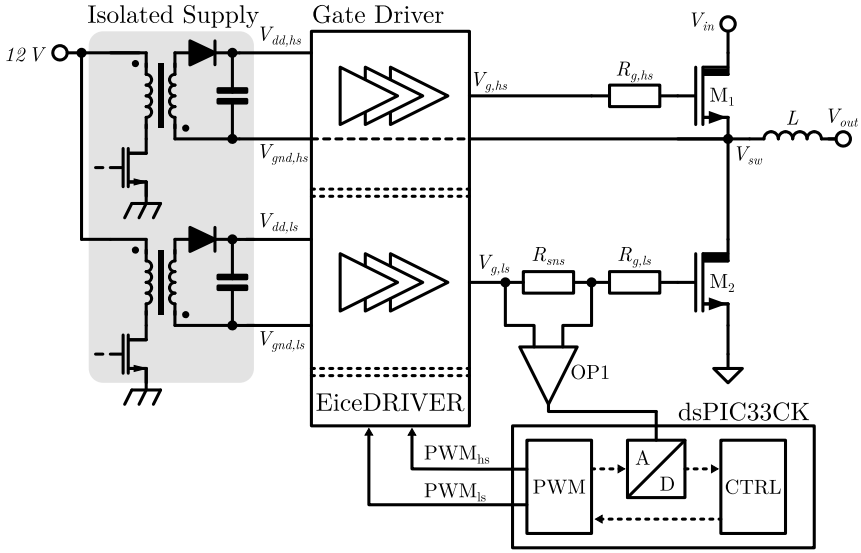

Figure 4.1: Block-level system overview of the SiC-based demonstrator converters.

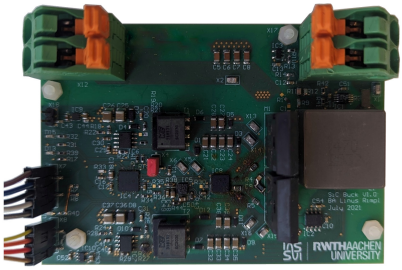

Figure 4.2: PCB implementation of SiC-based demonstrator.

provides an output driving strength of 4 A when acting as a source and up to 8 A acting as a sink. The driver has an internal input-to-output isolation, facilitating communication with the regulating microcontroller's voltage domain. The driver's two output voltages are supplied by two independent flyback converters, which are provided with an external 12 V rail. These are based on the Auxiliary Gate Drive Transformer series by Würth Electronic and the LT8302 Flyback Controller by Analog Devices [25, 20]. They provide an output voltage of 15 V, 0 V and −4 V. The control loop of the buck is implemented on a 16-bit dsPIC33CK with precise, dedicated PWM modules, allowing for resolutions down to 250 ps [64].

The measurement across the added gate resistor R_{sns} is done using an ADA4830 as a differential operational amplifier (opamp) OP1. With a low gain of 0.5 V/V, this opamp was chosen due to it relatively large −3 dB bandwidth of 84 MHz and more notably its large common mode input voltage range of −10 V to 9.5 V. This high voltage range is necessary due to the direct gate connection. The input of the opamp thus sees the high and low voltages of the gate terminal and must be able to withstand them.

The dsPIC33CK features a 12-bit SAR ADC with multiple dedicated cores, one of which is used to sample the measured voltage, and thereby provides enough resolution to capture the gate current accurately. This is done by binding the ADC sampling trigger to the high resolution PWM module. As the PWM module provides extremely high temporal resolution, it can thus shift its trigger delay for the low-side enable signal to occur at peak current, ensuring that ZVS is maintained.

Figure 4.3 details the implemented algorithmic flow that the µC follows in order to set and maintain optimal dead-time. Initially, a long dead-time $\mathrm{dt}_{\max}$ is set and counter i is reset. The chosen value ensures that shoot-through is ruled out under all operating conditions and can be overwritten manually. While this long dead-time is set, the inductor current has sufficient time to discharge the switch node entirely, allowing for body diode conduction to occur. By shifting the trigger delay of the sample time $t_{s[i]}$ 250 ps at a time using the dedicated PWM module, the entire gate-current curve, throughout the dead-time transition, can thus be reconstructed using the discrete measurements, and is successively saved in an array.

The characteristic gate-drain capacitance for this switch was extracted from the manufacturer's model and simulated as shown in Figure 4.4, matching the datasheet results at low voltages, while deviating at higher voltages [17].

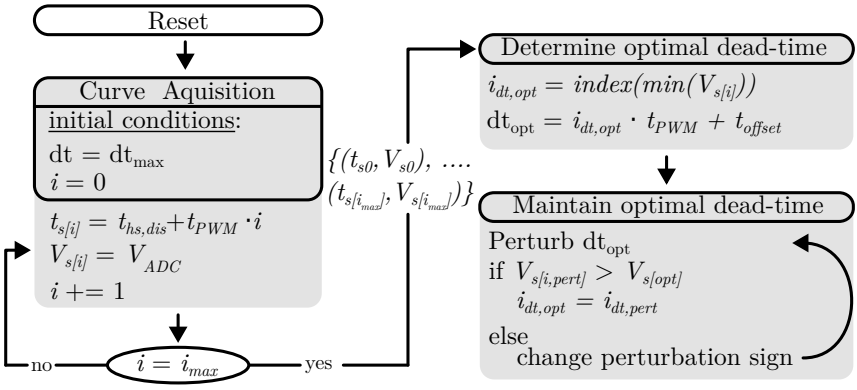

Figure 4.3: Algorithmic flow for gate current acquisition and dead-time regulation of discrete SiC-based demonstrator.

This deviation, however, is not important, as the sensing relies on the non-linearity of the curve, with a defining increase at low voltages. Once acquired, the minimal value of the array, minimal due to an inversion in the sampling process, representing the peak in gate-current, can then be extracted and the optimal dead-time thus inferred as the sampling frequency is known.

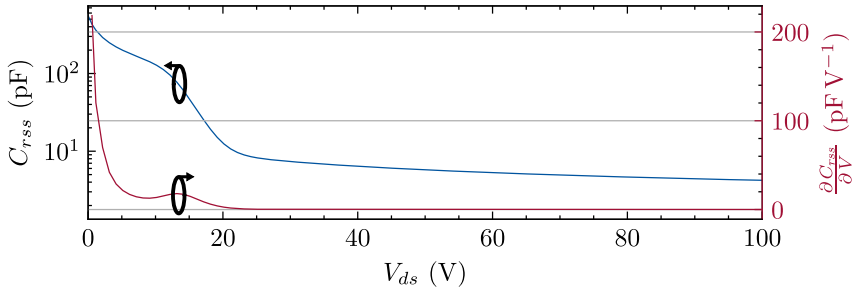

Figure 4.4: Gate-drain capacitance and non-linearity of C3M0045065K.

While this allows the converter to operate in its optimal operating point,

it is limited to the specific operating condition. Changes in load current or input voltage require a different dead-time. The optimal dead-time therefore needs to be tracked continuously. This is done using a perturb-and-observe algorithm. By applying a small perturbation to the dead-time and comparing the sampled value to the previous, determined to be optimal, sample, the controller can verify whether it is still optimally set or whether the dead-time should be increased/decreased further, without resorting to reacquiring the entire curve.

4.1.2 Measurements

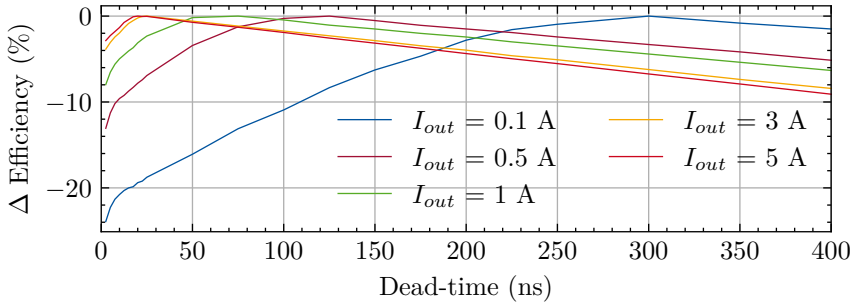

Figure 4.5: Efficiency loss due to misplaced deadtime at $V_{in} = 32\,\mathrm{V}$, $f = 500\,\mathrm{kHz}$ and $D = 0.25$.

To better motivate the need for optimal dead-time switching, Figure 4.5 illustrates the relative losses of mistimed low-side switching. As discussed in Section 2.3.2, an optimal timepoint exists for each operating condition, in this case dependent on the output current. Delayed switching results in a linear decrease in efficiency, as expected, due to the heightened conduction losses associated with body diode conduction that increase linearly with time. Early switching results also show the quadratic increase in losses, which are associated with the wasteful discharge of the switch node. The steep drop-off in efficiency at extremely low dead-times is associated with the appearance of shoot-through. The results thus confirm the theory presented in Section 2.3, while emphasising the desire to prevent early switching. Although measured at an input voltage of only 32 V, the general validity

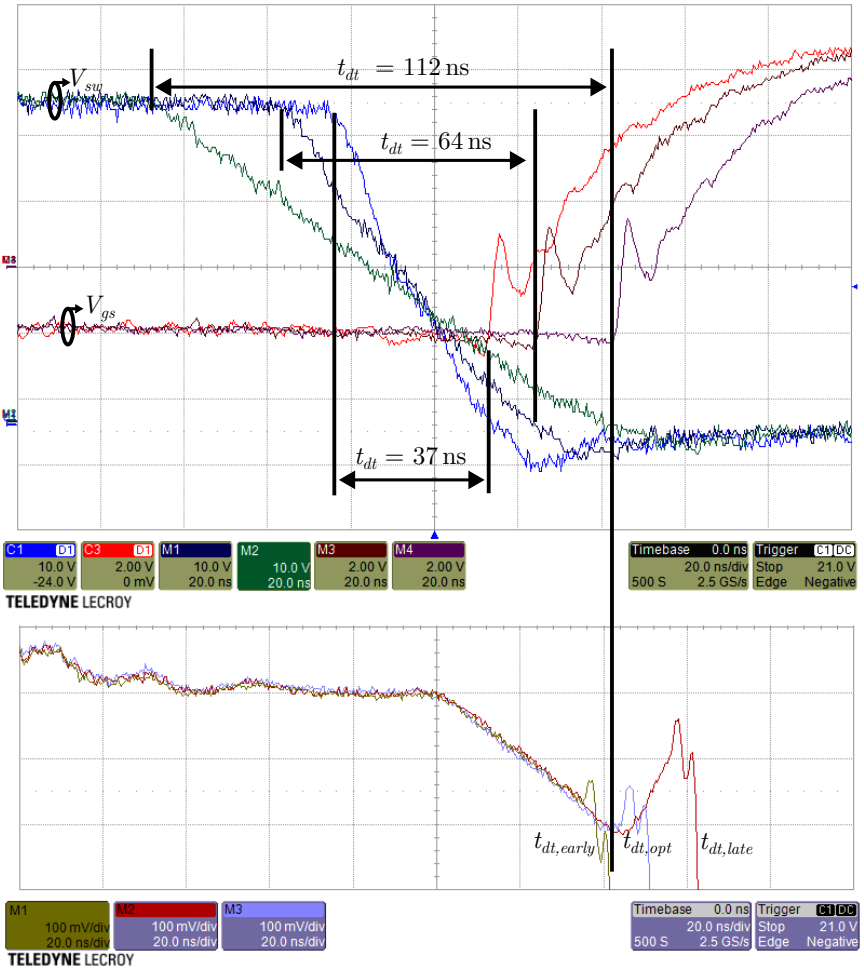

Figure 4.6: Measurement of switch node and gate-source voltages signals at three load conditions (upper), gate current at three dead-times (lower).

of the conclusions are voltage independent, as is the concept presented. A more detailed discussion is presented in Section 4.3.

Figure 4.6 presents measurement results of the SiC-based converter at three different load current values. It shows the switch node voltage, V_{sw}, transition with $I_{L,peak}$ of 0.5 A, 1 A and 1.5 A, thus offering different ideal dead-times due to its varying slopes. This was achieved by attaching an electronic load to the output of the converter, and a DC source at the input, while running a static duty cycle. Simultaneously, the gate-source voltage of the low-side SiC MOSFET, V_{gs}, is recorded to illustrate the enabling switching timepoint for the three conditions. The system is thus able to accurately define the optimal dead-time switching point. Additional inductive behaviour nevertheless causes the switch node to fall slightly below 0 V during the fastest transition. This is in part due to parasitic inductances, but also due to the fact that the gate driver is not turning on the switch rapidly enough, hence why the undershoot worsens with increasing steepness. Though, as previously discussed, the occurrence of undershoot, while ideally unwanted, is not as significant in terms of efficiency.

In the lower graph of Figure 4.6, the output of the opamp is showcased for the slowest of the three transitions, for three different dead-times: an early switching point $t_{dt,early}$, set manually, the system's targeted, optimal, switching time $t_{dt,opt}$, and a delayed dead-time $t_{dt,late}$. This latest is equivalent to the maximum dead-time of the regulation mechanism, $\mathrm{dt}_{\max}$, mentioned previously and shown in Figure 4.3, that is set initially. The curves represent the sensed gate-current, illustrating that a peak (valley) occurs at the optimal timepoint, which is targeted by the regulator mechanism.

The switch's large capacitance of $C_{rss} = 700\,\mathrm{pF}$, allows for a smooth sampling of the gate current, as is apparent when considering the system's internally sampled values, shown in Figure 4.7. It corresponds well to the measured curve from Figure 4.6. The sampled values also show a noticeable peak (valley), which denotes the system's target switching point. The continuous dead-time optimisation can thus run in the background and is constrained only by the sample speed of the µC, running at 100 MHz.

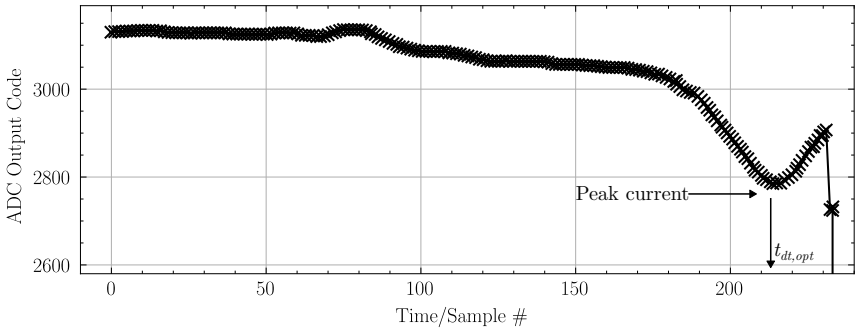

Figure 4.7: Sampled ADC values of gate-current sensing microcontroller.

4.2 GaN - Based Buck Converter

Figure 4.8 gives a system level overview of the GaN-based implementation. The design is again based around a half-bridge, this time made up of two GaN HEMT switches. The GaN HEMT are GS-065-008-1-L [41] and provide a maximum switching capability of 650 V.

4.2.1 Implementation

The gate-drain capacitance of the said HEMTs ranges from 0.3 pF to 13 pF. While being much lower than the SiC equivalent (by around one order of magnitude), the non-linearity towards low voltages is still present, as illustrated in Figure 4.9, and therefore sufficient to be used to detect the zero voltage condition.

The two switches are driven by isolated gate drivers LMG1020 [55]. The system is again controlled by a dsPIC33CK using its dedicated high resolution PWM modules. Due to the high common mode voltage, the differential voltage across the low side resistor is divided down using a resistive divider. The subsequent voltage is then fed to a TI OPA847 [103] set up as a differential amplifier configuration to provide defined gain. The OPA847 has a gain-bandwidth of 3.9 GHz and achieves an output slew rate of up to 950 V/µs. However, the sampling stage of the dedicated ADC core of the subsequently connected microcontroller is not able to handle such rapidly

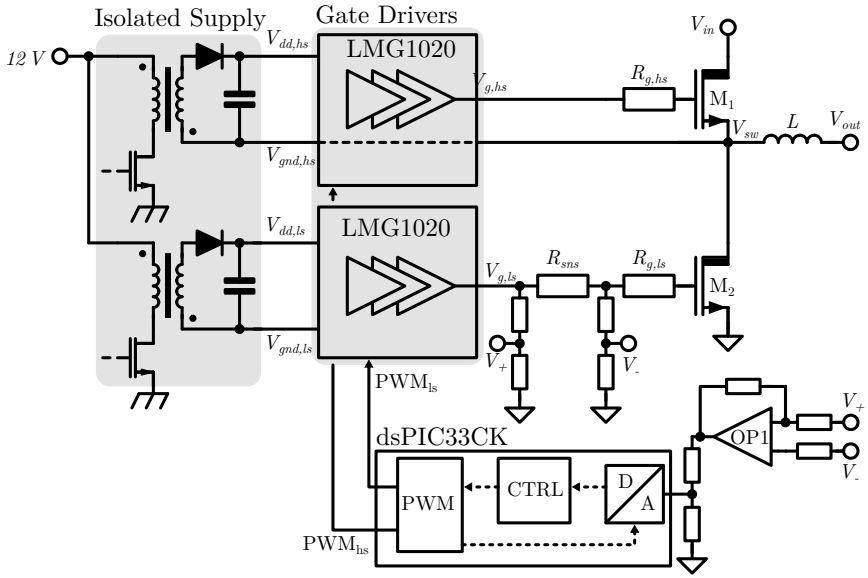

Figure 4.8: Block-level system overview of the GaN-based demonstrator converter.

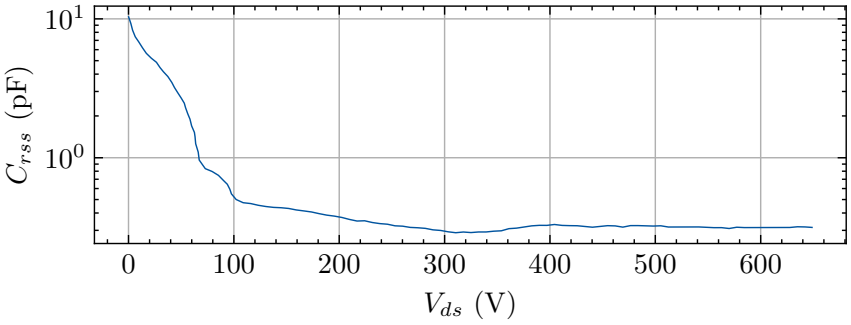

Figure 4.9: Gate-drain capacitance of GS-065-008-1-L.

changing $\delta V/\delta t$, resulting in errors in the measurement. As a slower output would categorically break the concept of the system, the output voltage of the opamp is divided down a second time before going to the ADC input, thus enabling the µC to accurately sample the gate current.

Figure 4.10 shows an image of the implemented system. It consists of three PCBs, working together. The top and largest PCB contains the buck converter and peripheral connections. The GaN HEMTs can be seen in the middle of the PCB. The ball-grid-array packaging is partly to thank for the extremely low capacitances of the switches. The lower PCB contains the controller and interfacing. The third PCB houses the sensing mechanism and opamp. This modular setup allows for rapid iteration and enabled the overcoming of the challenges with both the sensing and the microcontroller ADC limitations encountered during testing.

Figure 4.11 details the implemented ZVS algorithm. It is an adapted form of the one presented in Figure 4.3. Due to the much lower nominal value of the gate-drain capacitance, the gate-current is more susceptible to noise and parasitics. However, more importantly, the transition also occurs more rapidly, meaning that the sample time is a lot shorter. Combined, these effects make the optimal timepoint more difficult to extract. Maintaining the optimal dead-time through perturbation becomes non-viable. Instead, the entire curve acquisition is repeated periodically to ensure that suboptimal switching due to load changes are not maintained for significant time intervals, as well as when the outer control loop signals a change in duty cycle, which is bound to mean a change in dead-time is necessary. While these two additional triggers do not offer the dynamic regulation obtained in the SiC demonstrator, they do allow for transient evaluation and verification of the system's underpinning theory, which is the main goal of the demonstrator.

4.2.2 Measurement

Even though the switch node capacitance is vastly lower for this demonstrator, ZVS is still desirable. Figure 4.12 underscores this, by illustrating efficiency losses over different dead-times. Although much lower, similarly to the SiC implementation, a linear decline becomes apparent for delayed switching, while early switching results in a quadratic loss in efficiency. This, once again, motivates the preference of slightly delayed switching to early switching.

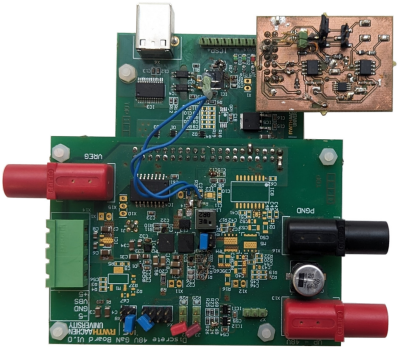

Figure 4.10: PCB implementation of GaN-based demonstrator.

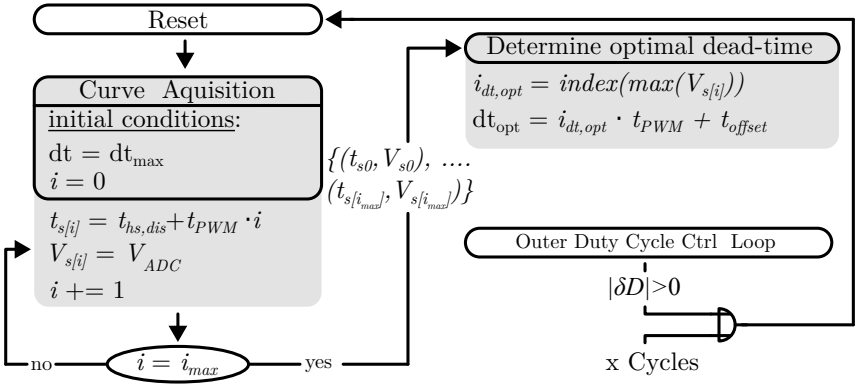

Figure 4.11: Block-level system overview of the demonstrator converters.

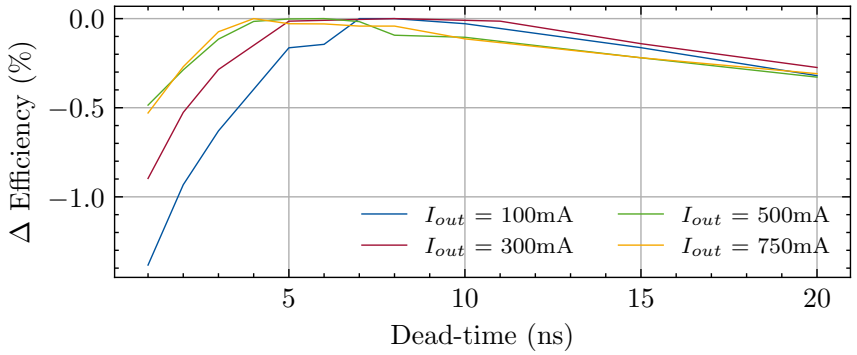

Figure 4.12: Efficiency loss due to misplaced deadtime at $V_{in} = 40\,\mathrm{V}$, $f = 333\,\mathrm{kHz}$ and $D = 0.2$.

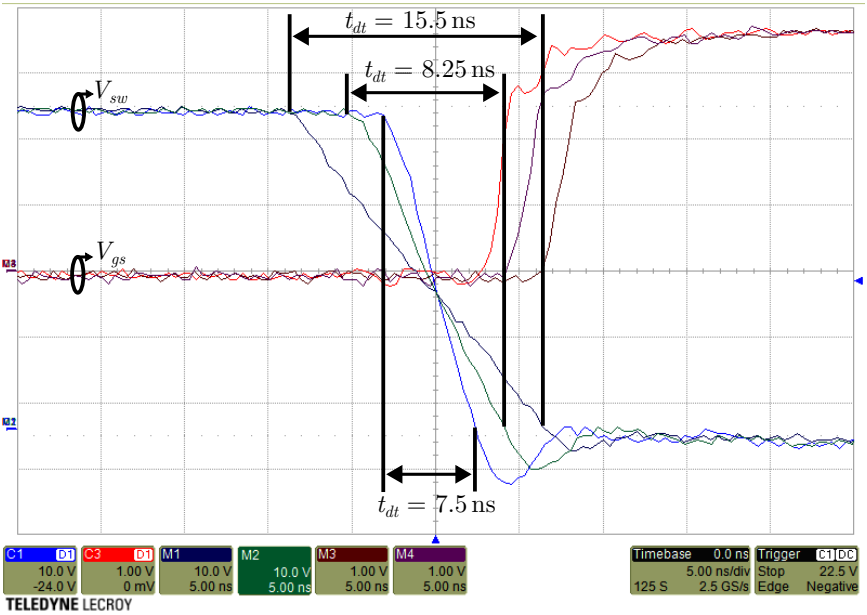

Figure 4.13: Measurement of switch node and gate-source voltages signals at three load conditions.

The system was once again evaluated at multiple load currents through the use of an electronic load and a static input voltage source, presented in Figure 4.13. The multiple load currents again offer varying $\delta V/\delta t$ values of the switch node voltage during the transition, and thus different ideal dead-times of the converter. The system regulated the dead-time to 15.5 ns, 8.25 ns and 7.5 ns respectively. Parasitic inductances in the gate path, as well as measurement inaccuracies lead to ringing on the switch node, increasing with slope steepness. The gate-source voltage is once again presented alongside, indicating the turn-on times of the low-side switch.

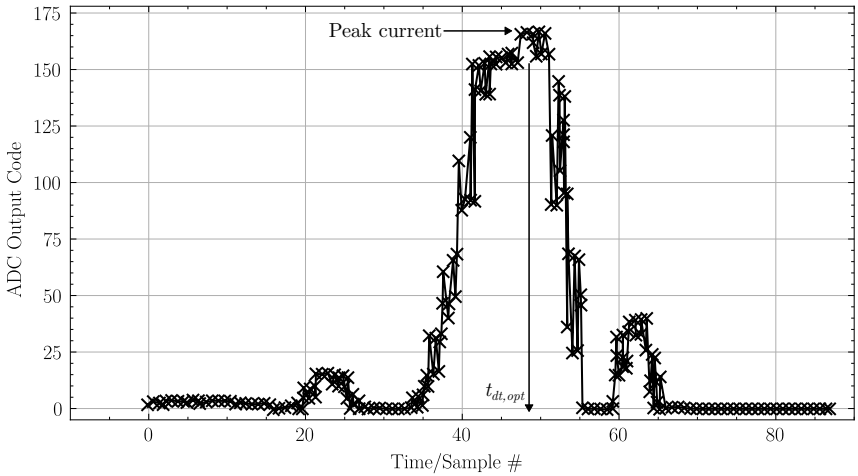

Figure 4.14: Sampled ADC values of gate-current sensing microcontroller.

Figure 4.14 presents the system's internally measured ADC samples. These were not measured separately due to the sensitivity of the measurement. What is immediately apparent is the increased noise compared to the SiC measurement of Figure 4.7. This is attributed to the much lower capacitance of $C_{rss} = 17\,\text{pF}$, leading to parasitic elements having a higher influence on the targeted measurement. The limitations of discrete implementations thereby become apparent, as a fully integrated solution could provide interconnections with much lower impedance.

Nevertheless, the peak current is apparent and detectable by the regulating mechanism, which can thus infer the optimal switching point. The increased

noise, however, prevents the use of a perturb-and-observe approach due to the multiple plateaus and local maxima in the curve. Instead, the system relies on regularly reacquiring the entire curve and finding its maxima.

4.3 Discussion

The results from the discrete implementations of the proposed sensing mechanism showed that the modelled non-linearity of the gate-drain capacitance is indeed present. This corroborates the theory behind the varying expansion of the depletion layer within the vertical SiC MOSFET, depending on the doping profile of the specific area. This admission is in itself sufficient to conclude that the presented concept is a novel approach to ZVS detection that can be used for dead-time regulation.

While the used switches support, and are meant for, high-voltage levels, the proposed demonstrators were tested at relatively low input voltages. The first reason for this is of practical nature. High voltage testing is not an easy feat. Measuring equipment including sources and loads quickly deteriorate in performance as the voltage levels increase, while availability of probing equipment is significantly reduced. Furthermore, safety precautions must be taken, increasing the complexity and hemming the flexibility of the setup significantly. Moreover, high-voltage capability must be guaranteed throughout the design of the converters, through adequate isolation of the components. High voltages at the switch node also increase the difficulty of accurately recording waveforms due to the decreased capture resolution. The second reason is that it is simply not required. The sensing mechanism can handle large voltages inherently. Its sensitivity stems from low voltage scenarios, thus a high voltage implementation is needless.

The presented results showed great promise for the chosen approach. While the implementations differ slightly from each other, they are not to be regarded as industry-ready applications, but rather as proof-of-concept approaches. Thus, dynamic behaviour and performance of the converter itself was not the focus of the implementations, neither were compactness, component count nor costs, which were thus also not discussed further.

The measurement results also show the limitations of such a system. Performance is highly dependent on the parasitic influences within the system

as well as the performance of commercially available components and their sometimes unpredictable interactions. Discrete implementations are thus inherently limited. Nevertheless, the approach was shown to work for both commercially available switches, a typical SiC MOSFET and a GaN HEMT with an extremely small C_{rss}. This motivated the next chapter of the thesis, investigating a fully integrated approach, where internal sensing of the current can be done with all the possibilities analog and mixed-signal circuitry offers, without requiring additional components, sparring the parasitics of traces and packages, and providing the user with a solution that can substitute a conventional implementation.

CHAPTER 5

GATE DRIVER ASIC

Having confirmed the modelled results with discrete implementations of the proposed sensing mechanism, the next step is the integration of the approach within a gate driver. This was done in two versions of the Gate Shaper IC (GSIC) developed at IAS. The following section presents a brief overview of the ASIC, its abilities and purpose, before delving into the details of the two implementations. A broad overview of the IC is illustrated in Figure 5.1, showcasing the IC alongside required external components.

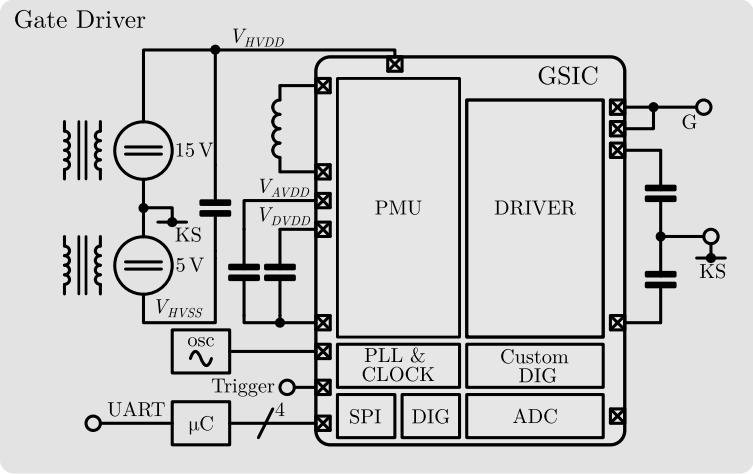

Figure 5.1: Simplified overview of gate driver structure, including ASIC and external components and interfacing.

5.1 ASIC 1

5.1.1 Overview

The IC features an internal Power Management Unit (PMU) based on a single-inductor, multiple-output (SIMO) buck converter topology, an internal phase locked loop (PLL) and clock generator using an external RC oscillator, a burst-mode Analog to Digital Converter (ADC), a digital block for external interfacing using serial peripheral interface (SPI), digital calibration and configuration, and a custom digital logic, referred to as Driver Control, that enables a high-speed output driver circuit. The following section delves into more detail of the implemented building blocks. Figure 5.2 is presented as a more detailed overview, with the different blocks highlighted appropriately.

PMU

The PMU provides outputs for $V_{AVDD} = 5\,\mathrm{V}$ and $V_{DVDD} = 1.8\,\mathrm{V}$ from the input voltage source, $V_{HVDD} - V_{HVSS} = 20\,\mathrm{V}$. The input voltage is provided by a discrete isolated Flyback converter, that also provides a negative voltage rail of $V_{HVSS} = -5\,\mathrm{V}$. This allows the gate driver to apply a negative voltage between the gate and kelvin-source terminals, ensuring the SiC MOSFET is turned off. As the IC is implemented in a triple well BCD process and not in SOI, negative voltages are not manageable on chip, due to diode conductions throughout bulk. Thus, the entire IC is referenced to V_{HVSS}, ensuring only positive voltages are found on-chip.

The SIMO buck converter operates at a fixed frequency of 500 kHz and is designed to supply around 0.4 W of sustained power to the two voltage rails, sufficient for the continuous operation of the gate driver. The power switches are integrated in the driver, with an external inductor L providing the magnetic storage. An external sense resistor R_{sense} is also required for input current sensing.

Apart from the SIMO, the PMU also features an under-voltage lockout (UVLO) circuit that monitors all other generated voltages and manages the startup procedure, a bandgap voltage reference that provides a temperature stable reference voltage, various startup circuits, multiple LDOs generating

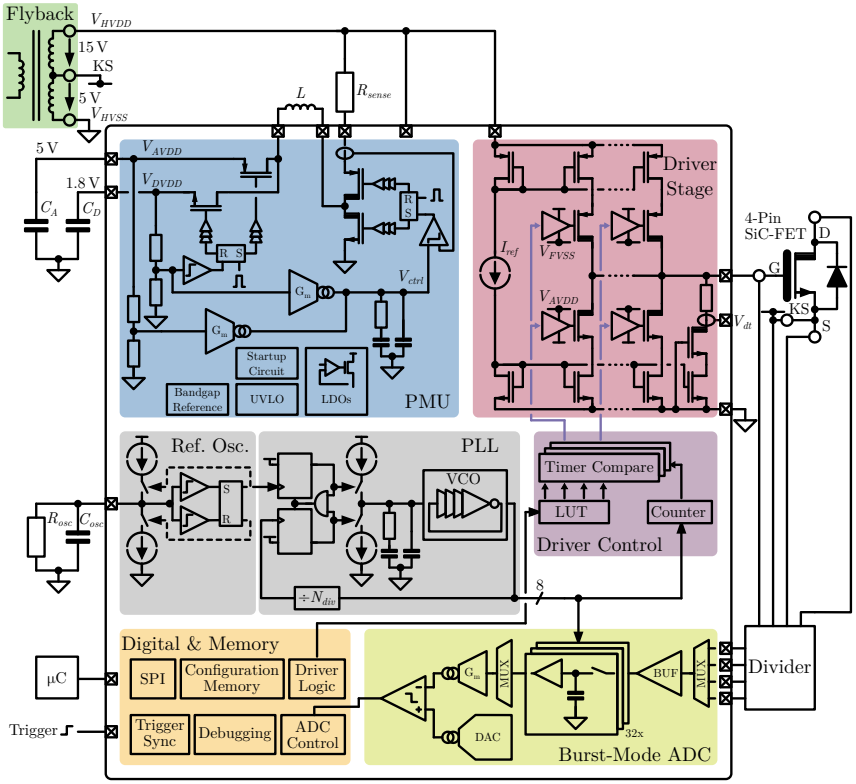

Figure 5.2: Detailed overview of gate driver ASIC with external periphery and driven SiC MOSFET.

locally isolated voltage rails and providing noise reduction for sensitive circuits such as the voltage controlled oscillator (VCO) and a linear regulator providing $V_{FVSS} = V_{HVDD} - 5\,\mathrm{V}$ for the high side voltage domain.

Clock Generation

The on-chip clock generator circuit makes use of an external, parallel RC tank to form a relaxation oscillator. This was implemented to ensure accurate operation, due to the fact that process variations can result in a significant alteration of the RC-constant when using on-chip devices ($\pm$ 30 % are not unusual). In industrial production, this would be accounted for through automated post-fabrication trimming. However, this is not feasible in an academic environment. Digital trimming could be implemented, however it would occupy additional area and add complexity to testing and usage in applications, requiring manual calibration for each IC. Furthermore, due to the lack of persistent memory, the added steps would have to be performed during every reset of the IC. Thus, the choice of using external components was made, as discrete components with extremely tight tolerances ($< 1\%$ variation) are easily obtainable and thereby offer a simple alternative approach. The associated cost however, in increased PCB area, reduction in degree of integration (additional implementation and soldering steps and therefore sources of failures) and most notably a package pin that is bound and cannot be used for a different, more important function, is not negligible.

The generated frequency of 8 MHz acts as the input for the integer-N charge-pump based PLL, which outputs 832 MHz and is tunable in 16 MHz steps through a digitally adjustable divider ratio. The PLL provides eight output phases by tapping both ends of each stage of the voltage controlled oscillator (VCO), thus enabling 150 ps of effective time resolution. The eight phases are provided to the driver control circuit as well as the burst-mode ADC, requiring accurate phase matching during the layout of the IC to ensure minimal phase-spacing misalignment.

Burst-Mode ADC

The burst-mode ADC allows sampling of multiple signals throughout the switching transition. It has four inputs that can be multiplexed to its 32

internal sample-and-hold stages, that offer an input voltage range of 1 V to 4 V. The four inputs are associated with the gate voltage, the drain voltage, the source voltage and kelvin-source, which can be used to establish a complete representation of the turn-on/turn-off transition of the device.

To achieve this extreme timing resolution, the ADC makes use of an interleaved sampling stage, whereby the 32 input sample stages are shifted through at the set sampling frequency. The signals on the sampling stages are then multiplexed and fed to a common SAR ADC for conversion. This process is not time critical, as the conversion only occurs once per switching period of the driver. It consists of a 7-bit current-steering digital to analog converter (DAC) and a 6-bit DAC used for offset calibration.

However, as mentioned previously, one critical operating condition is that these signals must have a relatively low voltage amplitude. Thus, an external divider is required to reduce the actual amplitude to a safe range. This, in turn, is challenging, as dividers are often not linear across the entire frequency range and the signals require measurement accuracy in both their DC value as well as in their rapid transitions. This can be somewhat circumvented by implementing two bandpass filters, one centred around the transition speed and one at low frequencies, to ensure both are properly represented [39].

Driver Stage

The driver stage consists of 34 NMOS and PMOS current sources. These are made of low voltage transistors forming current mirrors from a reference current source and cascaded high-voltage blocking transistors that enable the high output voltage. This topology was chosen due to the much better matching characteristics of low-voltage devices, thus aiming for the linearity and similarity of stages relative to each other. Furthermore, the much-reduced channel-length modulation of the low-voltage transistors enables a wider voltage range with constant output current. Each current source is enabled and disabled by driving the high-voltage blocking cascode transistor. To improve the output stage's accuracy further, the mirror ratio between the reference and the driver stage was kept small. To reduce the losses associated with the high reference current required, it is kept in a disabled state until the trigger signal is detected, at which point it is rapidly enabled.

The current sources are able to provide a theoretical cumulated 5 A of source and sink current from a 20 V supply, with 31 of those nominally providing a coarse resolution of 128 mA and three providing a fine resolution of 32 mA. Through manual setting of the reference source, these values can be increased by 25 %. By making use of the high-speed clock, the driver stage is able to trigger these sources in 150 ps intervals. The driver stage thus offers a programmable interface for the emitted gate current, for both the charging and the discharge phase.

However, due to limitations in the digital implementation, these trigger events cannot be chosen entirely arbitrarily. A single source/sink can only be enabled and disabled once throughout a switching event, and the rise and fall time of each current source is simulated to 2 ns. Thus, while they can be triggered much faster, an external regulator has to take into account these practical limitations when proposing a specific gate shape profile, as what is essentially offered in time resolution concerns the turn-on event of the internal current sources, not their final value. Assuming, however, that these operate uniformly, this differentiation can be disregarded for now.

Driver Control and Digital

An illustrative overview of the control system is presented in Figure 5.3. As the 832 MHz reference clock is too fast for synthesised digital logic in

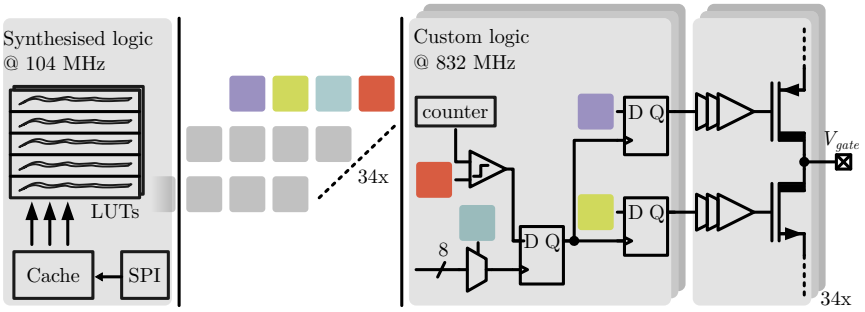

Figure 5.3: Conceptual illustration of the implemented driver control logic across frequency domains.

the technology used for this IC, the clock is divided by eight, resulting in a slower 104 MHz clock. This clock is used for all synthesised logic, including SPI, the cache, and register banks. These include various configurable registers for trimming and adjustment of various blocks (e.g. the reference voltages for LDOs, selection of multiplexer inputs, debugging settings, etc.) as well as status bits of various blocks. All registers are also cached. This is necessary to enable the writing of a look-up-table (LUT) for the driver, while keeping a valid look-up-table saved in the registers for the continuous operation of the gate driver. The IC has two LUTs, one for each transition, in order to provide programmability for both cycles. The LUT contains the shaping data, consisting of a piece-wise constant waveform, indicating the driving strength at the various timepoints. As synthesised logic is not able to run at the mentioned 832 MHz, the high-speed part of the driver control block is implemented and verified manually. The LUT data is translated into individual state and timing definition for each of the current sources and stored in 34 first-in first-out registers (FIFOs), one for each current source pair (NMOSand PMOS). These are then re-sampled in the high frequency clock domain and set flip-flops at the corresponding current sources. Each FIFO contains the state of the appropriate flip-flops, the transition time, and which phase to use. Each flip-flop is then triggered by the appropriate phase of the PLL in combination with two timers, thus achieving the 150 ps timing resolution of the driver stage. The two timers are set through the slower clock domain and thus limit the number of available transitions to two per slow clock cycle. The PWM input at the Trigger pin of the IC is synchronised to the high frequency clock, and thus also to the slower clock. Once tuned, the synchronised trigger then sets off various internal loops, such as enabling the driver's current reference. Various internal delays can be used to postpone the trigger signal from reaching the current sources. One of these is a 6-bit delay, based on the slower clock, allowing for delays in ca. 10 ns steps with a maximum delay of around 615 ns.

5.1.2 Implementation

Figure 5.4 illustrates the implementation of the proposed concept in this IC. The current sources in the driver stage offer an ideal tool to apply the proposed current measurement scheme within the gate output path. This was done by adding a supplementary current mirror stage, labelled M4 and M5. This is trivial to implement, as additional dummy stages are already

present within the driver stage to improve matching of the current source stages.

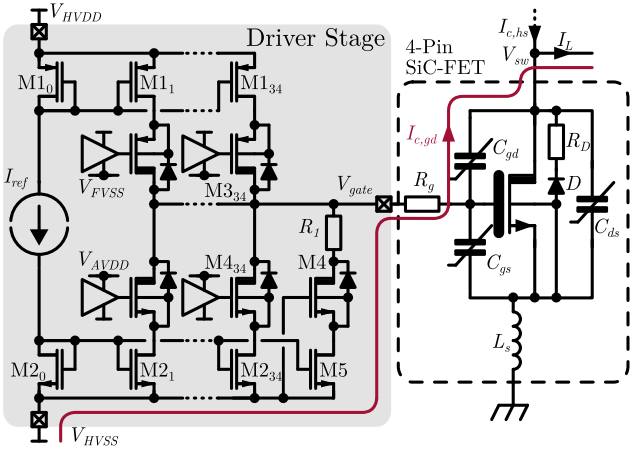

Figure 5.4: Schematic of gate driver output stage with added current sensing implementation and highlighted target current.

Thus, the proposed implementation can make use of already existent silicon, without consuming additional area. This used stage is permanently disabled, and thus has no influence on the operation of the gate driver throughout its standard operation. The current flow through the body-diodes is sensed resistively by tapping the voltages above and below the resistor R_1.

The current is then converted to a voltage through the sensing mechanism illustrated in Figure 5.5. A reference voltage $V_{d,M10}$ biases the gates of $M1_1$ and $M1_2$. The voltage difference generated across R_1 due to the to-be-measured current $I_{c,gd}$ generates a difference in the source voltages of $M1_1$ and $M1_2$, resulting in a mismatch in the injected currents I_1 and I_2. This difference is supplied by $M3_0$, mirrored and amplified by current mirror $M3_1$ and then converted to a voltage across R_2.

Figure 5.6 gives a more detailed implementation overview. This current-based amplifier is favourable due to its high speed and low input offset, as well as tolerance to common-mode voltage swing going below zero during the measurement phase. The layout of this stage requires special attention

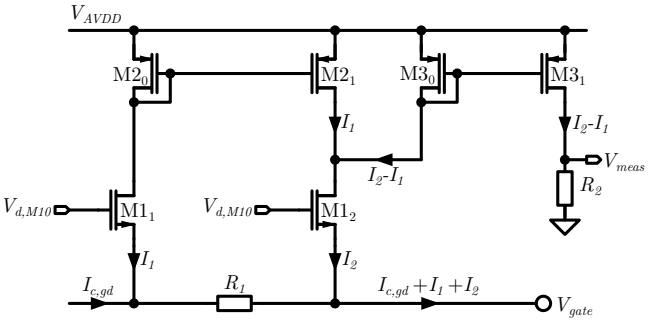

Figure 5.5: Simplified schematic of current-sense mechanism in the driver output path.

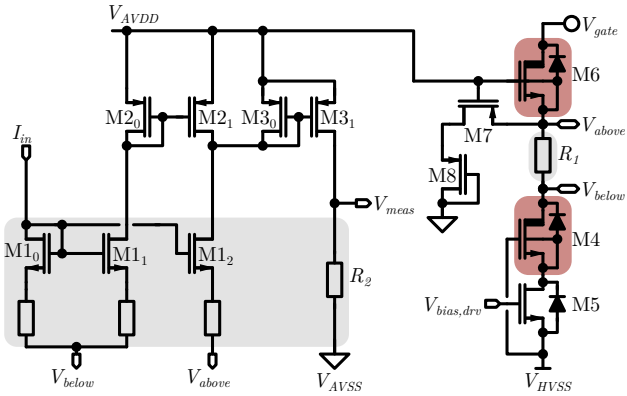

Figure 5.6: Detailed schematic of current-based amplifier for current sensing in driver output path.

to ensure proper isolation due to possible body diodes conducting. M6 is added to ensure that V_{above} cannot rise above $V_{AVDD} = 5\,\mathrm{V}$. To protect the 5 V transistors, M7 and diode-connected M8 act as a clamp, discharging the node when needed. $\mathrm{M1_x}$, R_1 and R_2 are isolated in a p-well contacted to V_{below}, while M4 and M6 are in their own HV well, isolated from substrate. All other components are in their respective customary wells, connected to V_{AVDD} or V_{HVSS}, as highlighted. The different grounds of the IC come together on the exposed pad of the IC's package to ensure DC equalisation. The final output voltage, V_{meas}, is connected to one of the IC's I/O pin to be measured externally.

5.1.3 Test setup

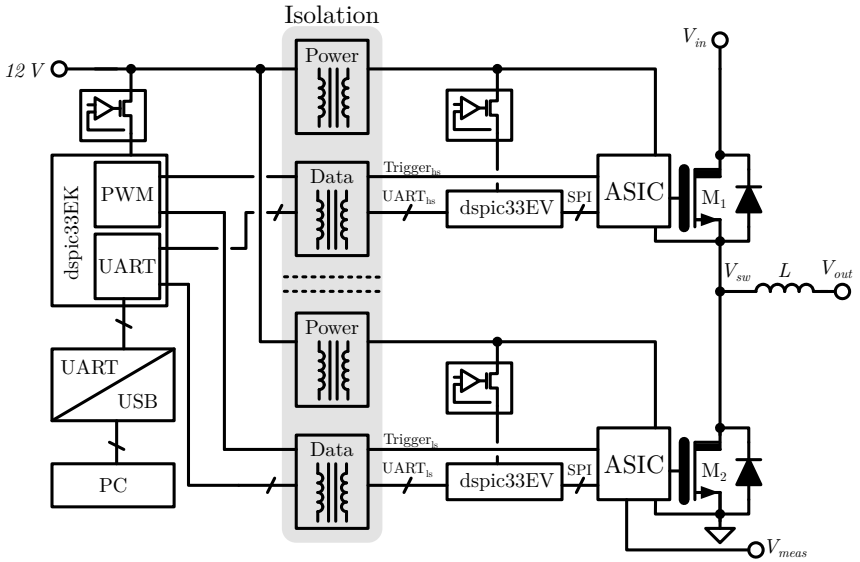

Figure 5.7: Overview of test system for ASIC in half-bridge configuration.

The test setup consists of a buck converter using C3M0045065K SiC MOSFETs as illustrated in Figure 5.7. The switches are each driven by an ASIC, which is supplied by a discrete Flyback MGJ6D241505LMC.

A dspic33EV sits beside each ASIC, supplied by local LDOs from the Flyback's output. The µC is able to drive 5 V outputs, allowing it to act as an interface to the ASIC, handling the conversion between UART and SPI. It is used to set the trigger delay of the ASIC to achieve ZVS.

Controlling the buck converter loop is a dspic33CK. Its PWM module is used to send out two trigger signals that are brought to the respective ASICs through digital isolators as $\text{Trigger}_{\text{hs}}$ and $\text{Trigger}_{\text{ls}}$. It also provides the UART interface to the operator and distributes the transmitted commands out to the respective microcontrollers. An image of the assembled PCB is shown in Figure 5.10.

5.1.4 Measurements

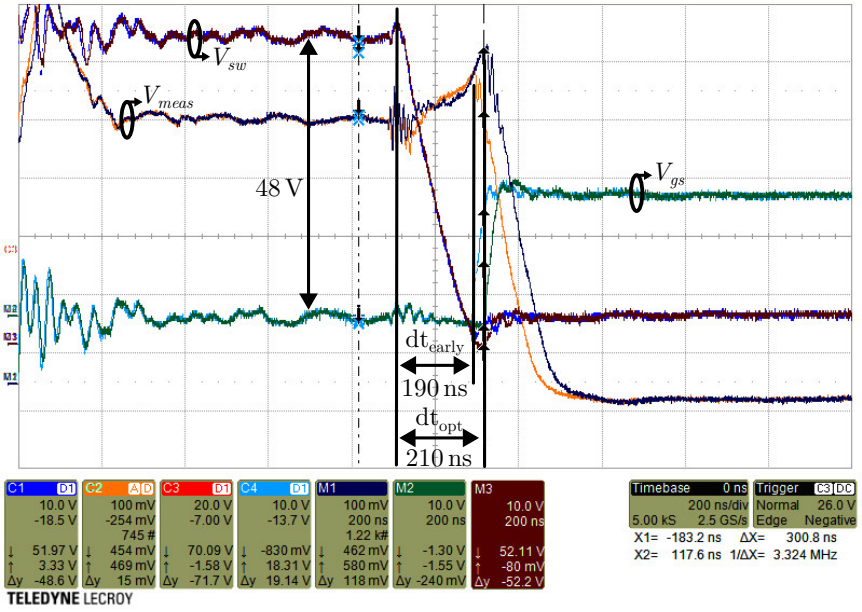

Figure 5.8: Measurement of transition signals at early and optimal switching.

Figures 5.8 and 5.9 present measured results of this initial version of current sensing. The system does not regulate itself to achieve ZVS, but is instead

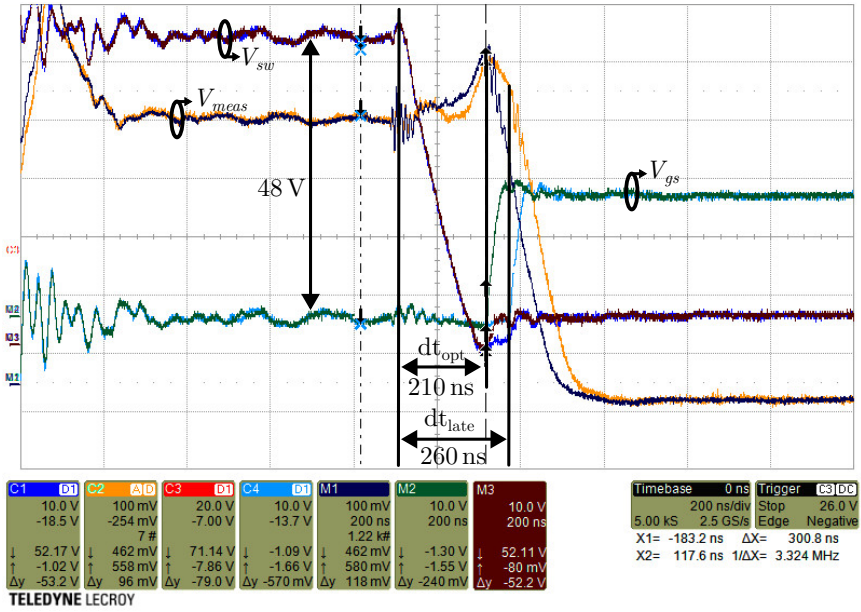

Figure 5.9: Measurement of transition signals at optimal and late switching.

implemented to see if the chosen approach would yield a signal that would confirm the theory and reaffirm the results achieved in Chapter 4. Thus, the target signal is pushed out of the IC and measured with an oscilloscope at different dead-times. These are set manually by varying the internal delay of the trigger signal $\text{Trigger}_{\text{ls}}$ pushed to the gate driver ASIC of the low-side switch M2.

Figure 5.8 shows three measured voltages in two scenarios. The first scenario is one where the dead-time is set to be too short, i.e. low-side switching is done early, with dt_{early} set to 190 ns. The second scenario is with the optimal dead-time set at $\text{dt}_{\text{opt}} = 210\,\text{ns}$. For both scenarios, Figure 5.8 presents the switch node voltage V_{sw} with its expected linear decrease throughout the transition, the output gate-source voltage V_{gs} and the target signal V_{meas}. The gate-source voltage indicates the timepoint when the output gets activated, increasing the output voltage from $-5\,\text{V}$ to $15\,\text{V}$. V_{meas} shows the expected curve, previously seen in similar fashion in Chapter 4, building up to its peak throughout the transition.

To be assured that the curve does indeed reach a peak value, Figure 5.9 presents the same measured signals, this time at the optimal dead-time set for the first scenario, and a delayed dead-time of $\text{dt}_{\text{late}} = 260\,\text{ns}$ forming the second scenario. The target curve is seen indeed peaking at the optimal dead-time, and then decreasing in amplitude, as expected. These results confirm the assumptions previously made, acting as a further stepping stone to a fully integrated, regulated solution, presented next.

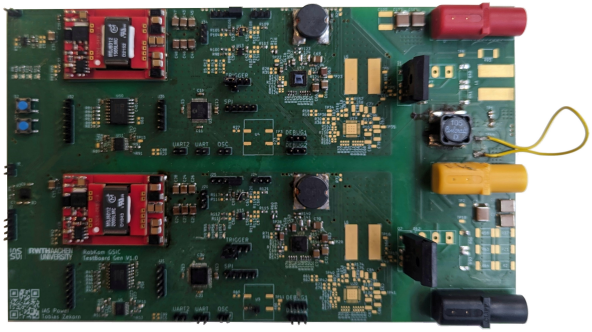

Figure 5.10: Test PCB for gate driver ASIC in a buck configuration.

5.2 ASIC 2

5.2.1 Overview

The second version of the Gate Shaper IC is very similar to the first in its design and implementation and can be seen as an evolutionary revision. Figure 5.11 illustrates the detailed block-wise overview of the IC. While incremental improvements were made to the PMU and the ADC, the substantial differences can be found in two areas: the clock generation circuit and the dead-time control circuitry.

Clock Generation

The clock generator was enhanced by adding a phase error correction block. This process makes use of the already-present ADC to measure adjacent phase differences ϕ_{err}. The accompanying digital implementation then adjusts the phase delay of the two phases exhibiting maximum and minimum phase error by one LSB of the calibrating resolution. The process works iteratively, ensuring that, in due time, the phase-error between the eight phases is continuously minimised, accounting for process variations and layout asymmetries.

Dead-time Regulation

The dead-time regulation mechanism is enabled through on-chip evaluation of the sensed gate current. This allows for a monolithic solution that integrates sensing, evaluation, and actuation within the IC, reducing parasitic influences. The ASIC thus acts as a fully integrated closed-loop gate driver. The addition is implemented as a mixed-signal solution, consisting of a digital control logic block, as well as additional and enhanced analog circuitry to achieve peak current detection. Furthermore, integration with the on-chip ADC was realised by adding an input at the multiplexer for the sensed current signal and implementing corresponding logic for measurement evaluation.

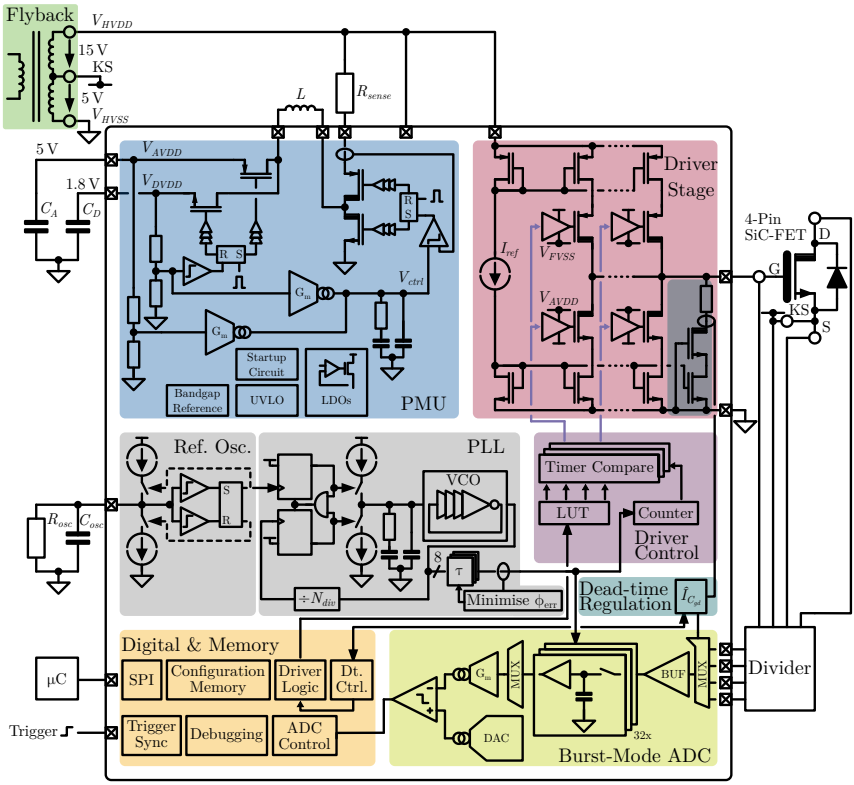

Figure 5.11: System overview of second generation gate driver ASIC with additional dead-time regulation.

5.2.2 Implementation

The implementation of the proposed concept consists of small changes to the sensing mechanism, such as the addition of trimming transistors M3, as shown in Figure 5.12, as well as the deep integration of the control mechanism within the driver logic.

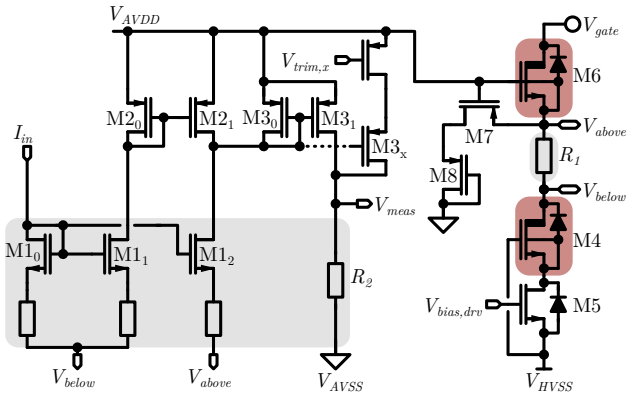

Figure 5.12: Modified gate current sensing circuit implementation.

This integration consists of on-chip evaluation of the sensed voltage. A simple peak detection mechanism that makes use of a diode and a sampling capacitor is not viable for two reasons. Firstly, the high bandwidth required by the system would require a diode capable of conducting fast enough, which was not available in the used technology. Secondly, the precise value of the sensed voltage was not known. While the measurements done so far confirmed the theory, deviations were seen from the nominal values expected. This is attributed to inaccuracies in the manufacturers' models and parasitic impedances both within the chip and from the measuring instruments. Thus, a more robust approach, maximising flexibility of operating conditions, was chosen to ensure that the system could be configured to function. Once tested and evaluated, a simpler, more dynamic, and more targeted implementation could follow. A system overview is given in Figure 5.13. After sensing and amplifying the voltage across R_1, V_{meas} is fed to comparator Q2. Figure 5.14 illustrates the schematic of the comparator.

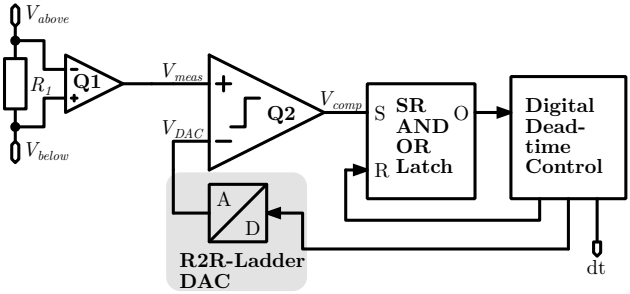

Figure 5.13: System overview of dead-time regulation mechanism.

The requirements for Q2 are confined to its low common-mode voltage capability. Thus, a non-cascoded PMOS input stage (M_1, M_2) is chosen. The second requirement of low propagation delay is addressed through the use of a single, high gain topology, with a large input stage. This is simultaneously beneficial to matching performance, although not a critical metric. As the output of the comparator is interpreted by a logic latch implemented in the 1.8 V domain, the output voltage is shifted appropriately using an inverter highlighted in Figure 5.14.

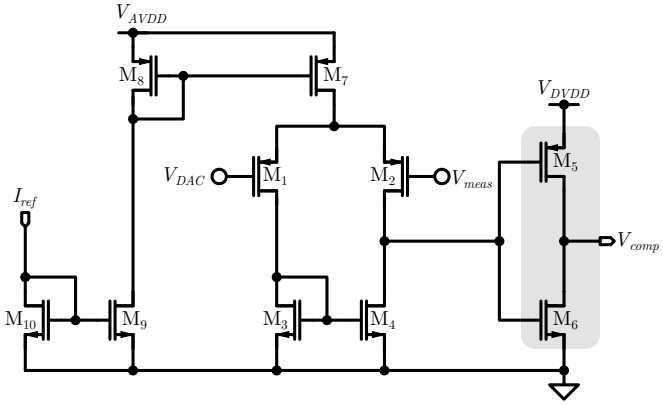

Figure 5.14: Schematic of comparator Q2.

As the goal of the implementation is to target the peak value in the time-domain, a regulation loop is formed to reach the peak value in multiple steps. The comparator compares the sensed voltage to a reference voltage set by an 8-bit resistive DAC. The DAC uses an R2R ladder, shown in Figure 5.15, that makes use of resistive unit elements to build up a binary weighted resistance. Binary weighted designs benefit from simplicity of implementation, good area scaling, and good matching performance due to the use of unit elements that can be arranged using common centroid techniques in the layout stage. The unit elements are connected to either a reference voltage or to GND, creating a resistive divider that is controlled by the digital input word $V_{ctl<7:0>}$.

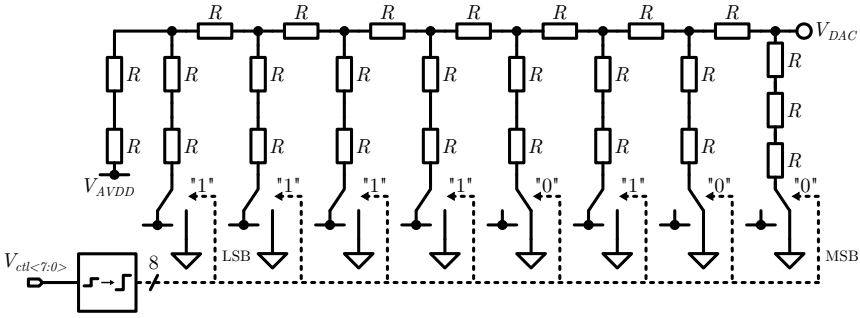

Figure 5.15: R2R-ladder based DAC implementation.

As the output of the ladder is connected exclusively to the input of Q2, and only expected to toggle once per switching cycle, no further buffer structure is needed to increase driving strength. This reduces implementation effort, while also benefiting accuracy as no further source of voltage deviation is introduced. As the DAC is part of the peak sensing mechanism, the most important factor is monotony of the transfer function. Care must be taken to ensure differential non-linearity remains within one LSB. The design thereby benefits from the good matching performance attained through the use of unit elements. To provide maximum flexibility, the DAC is supplied with a wide input range of up to 5 V through V_{AVDD}, thus requiring a level shifter to interpret the digital control word. An internal inversion ensures that an increase in binary control value results in an increase in output voltage. The 8-bit ladder thereby results in an LSB of 20 mV.

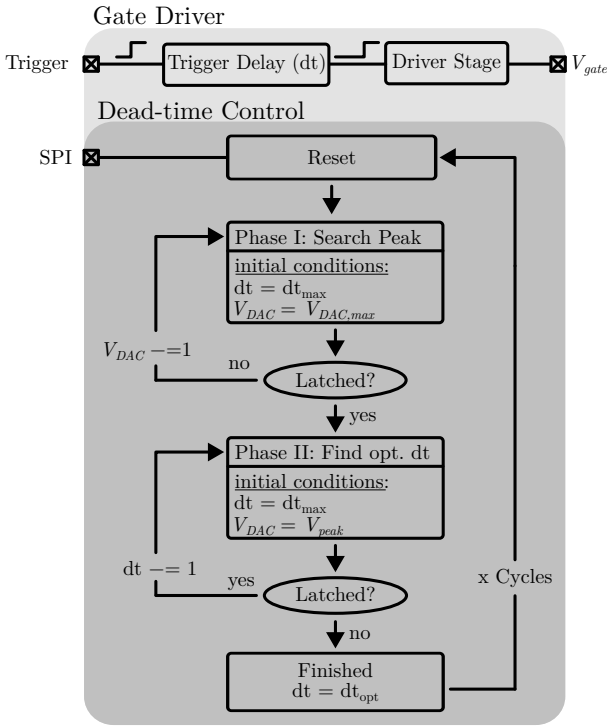

Figure 5.16: State-machine and interaction of digital regulation of dead-time within the gate driver.

The output of the comparator is evaluated by an SR-AND-OR latch, which in turn is evaluated by a custom digital control algorithm that sets the reference value V_{DAC} as well as the dead-time dt. The specific SR latch topology was chosen due to all possible input states resulting in valid and defined output states.

The algorithm followed is illustrated in Figure 5.16, with a timing diagram illustrated in Figure 5.17. Its main objective is to delay the incoming Trigger signal such that the dead-time of the converter is set optimally. The trigger delay is thus indirectly the dead-time and therefore referred to as such, dt. This custom delay of up to 630 ns is applied in steps of 10 ns, before allowing the driver stage to engage. The algorithm deducing how much delay to apply consists of two consecutive loops and is clocked by the input Trigger signal.

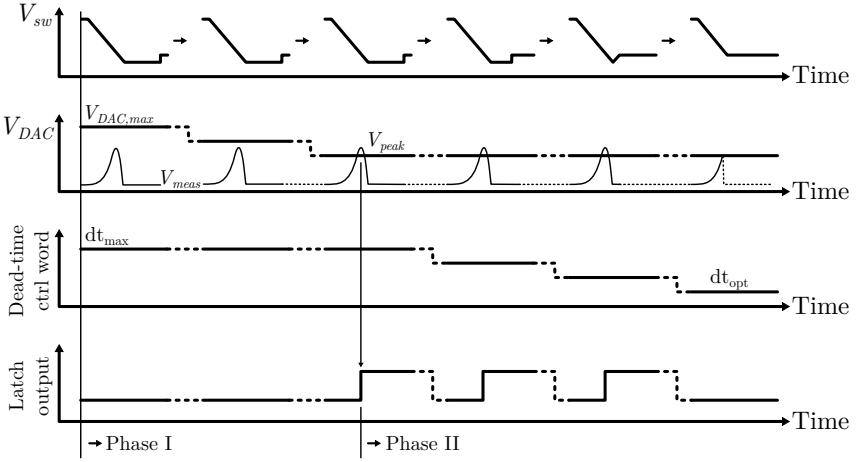

Figure 5.17: Timing diagram of dead-time regulation algorithm.

The first loop, labelled Phase I, searches the nominal peak current value. By applying a long delay, dt_{max}, the switch is bound to undergo reverse conduction, and the gate current is guaranteed to have reached the targeted peak value within the delay period. V_{DAC} is thus initialised to a maximum value and iteratively reduced, cycle-by-cycle, until the SR latch first latches due to the comparator toggling. This indicates the highest value the gate

current reaches and remains set at Q2's input as $V_{DAC} = V_{peak}$. In application the initial set value $V_{DAC,max}$ can be overwritten externally to speed up this process if the signal range is known. Figure 5.18 presents post-layout extracted simulation results of the proposed mechanism using manufacturer provided models of the C3M0045065K SiC MOSFETs, illustrating the targeted peak voltage of V_{meas} and the transition of the switch-node voltage V_{ds} with the long dead-time set.

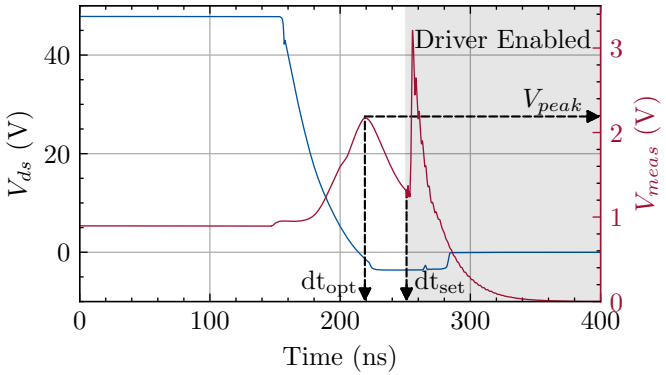

Figure 5.18: Post-layout extracted simulation of switch node and corresponding internally sensed voltage.

Having found V_{peak}, the second loop (Phase II) is initiated, with the goal of finding the timepoint at which the peak current occurs, $\mathrm{dt}_{\mathrm{opt}}$. This iterative process incrementally reduces the set dead-time, until the latch no longer latches, indicating that the gate-current no longer reaches the previously determined peak value. This is illustrated in Figure 5.19 using post-layout simulations for three set dead-times. Late switching would cause the latch to trigger, optimal switching would as well. Early switching would not allow latching to occur as the set comparator voltage is not reached within the transition time. At the switching event, a peak is seen in the measured voltage. This is due to the inrush current caused by the now active driver output stage. It, however, does not affect the latch, and thus the regulating mechanism, as internally the sensing mechanism is disabled as soon as the driver stage is engaged.

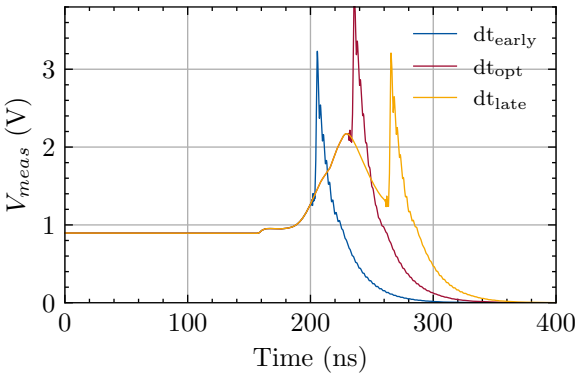

Figure 5.19: Post-layout extracted simulation of internally sensed voltage at multiple set dead-times.

The entire process is repeated after a set number of cycles to ensure optimal dead-time is maintained with changing operating conditions of the converter. The defined internal values of the system as well as the different stages of the presented state machine can be overridden externally through the SPI, ensuring maximum flexibility of this test system.

5.2.3 Test setup

The same test setup as with the previous generation of the gate driver was used. The pin-out remaining unchanged allowed for a swap-in application of this ASIC. Figure 5.20 presents a micrograph of the ASIC.

5.2.4 Measurements

Similar to the previously presented measurements for the first variant of the IC, Figure 5.21 showcases the switch node voltage and corresponding low-side gate-source voltage at three dead-times, with early and late switching being set manually at an input voltage of 100 V, while the regulated dead-time dt_{reg} is set optimally by the implemented loop. These measurements follow the simulation results presented earlier, with early switching resulting in the premature and rapid discharge of the switch node, and late switching

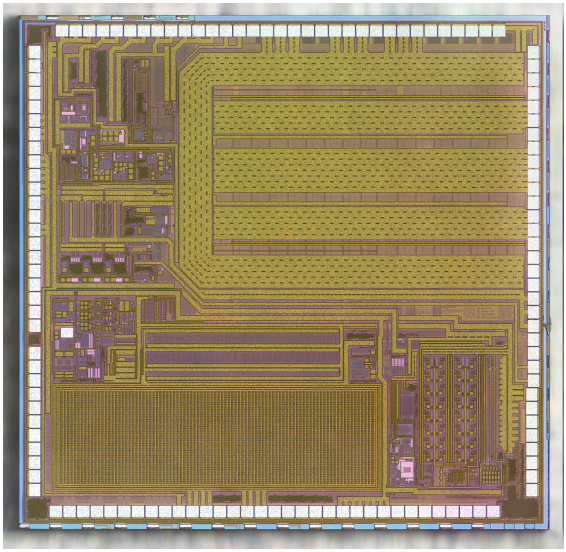

Figure 5.20: Micrograph of ASIC 2.

causing diode-conduction. To ensure rapid enablement of the switch, the driver strength was maximised, resulting in the overshoot seen in V_{gs}.

To further illustrate the regulator's functioning, Figure 5.22 presents three measurements of the switch node voltage and gate source voltage, showcasing the ability of the system to achieve ZVS at multiple load conditions. This time, the input voltage is set to 200 V to demonstrate the high voltage capability of the mechanism. As discussed previously, the high-voltage capability is inherent to the design of the mechanism, limited by the switch's voltage rating.

Figure 5.23 presents a transient capture of the regulating algorithm to illustrate the proper behaviour of the implementation. The top plot illustrates the switch-node voltage V_{sw} toggling from 0 V to 100 V and the gate-source voltage of the low-side transistor V_{gs} varying between −5 V to 13 V, as expected during normal operation of the buck converter. The lower plot shows a representation of the set dead-time using the oscilloscope's internal capture mechanism. The function evaluates the delay between a 5 % drop in the switch node voltage and the rise in gate-source voltage. It is thus not a

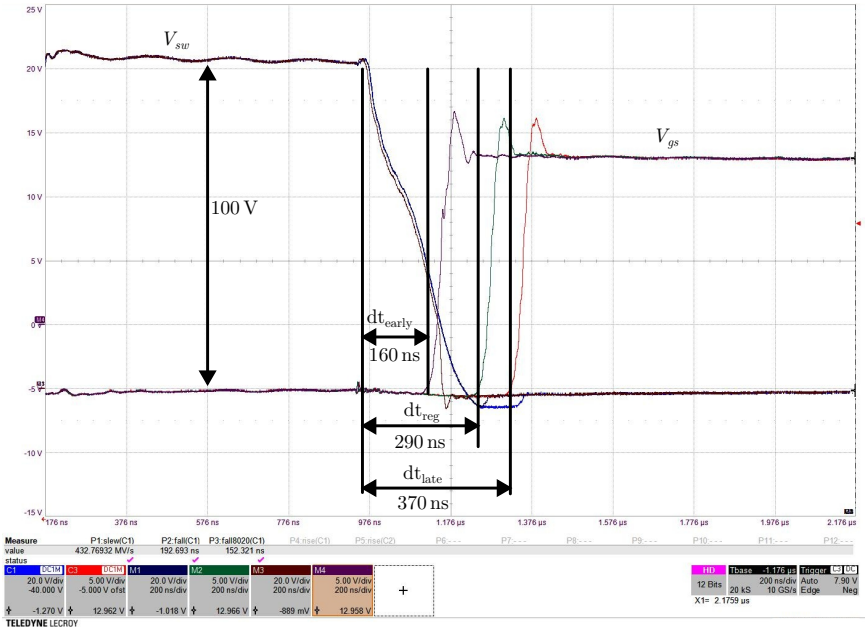

Figure 5.21: Measurement of transition signals at early, late and optimal switching.

nominally accurate measurement of the dead-time, but a relative depiction, sufficient for the explanatory showcase of the mechanism's transient behaviour. The initial phase of the algorithm, during which the peak voltage is searched, results in the expected long dead-time. This is accompanied by body-diode conduction, seen in the top plot, with the switch-node voltage reaching negative values. The second phase of the algorithm reduces the dead-time linearly until the optimal dead-time is found. At this point, body-diode conduction is no longer occurring, resulting in the switch-node voltage remaining non-negative.

To properly assess the functioning of the mechanism at multiple load conditions, Figure 5.24 presents the efficiency losses across dead-times of the test buck converter. This was captured through sequential variation of the dead-time up to the longest value possible, with simultaneous efficiency capture through measurement of the input and output voltage and current

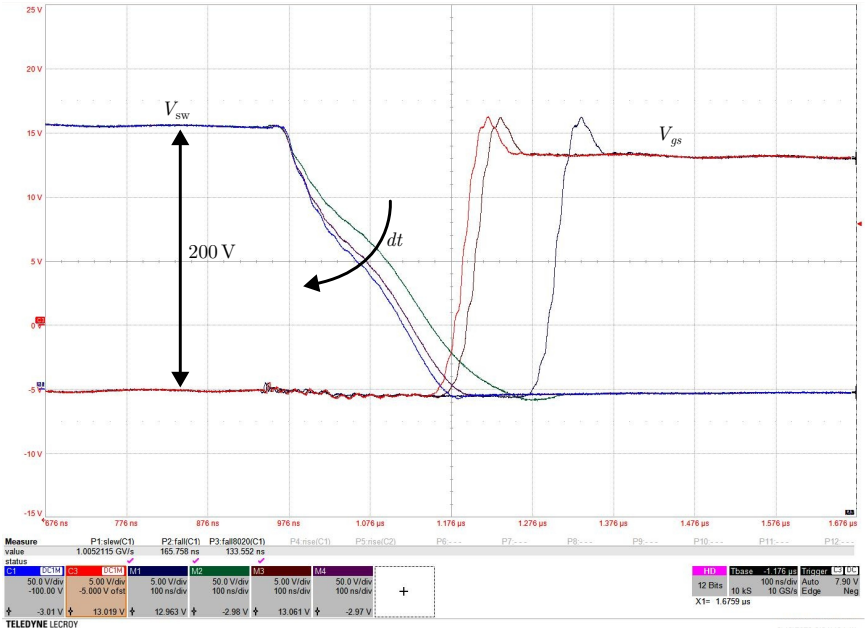

Figure 5.22: Measurement of transition signals at three load conditions.

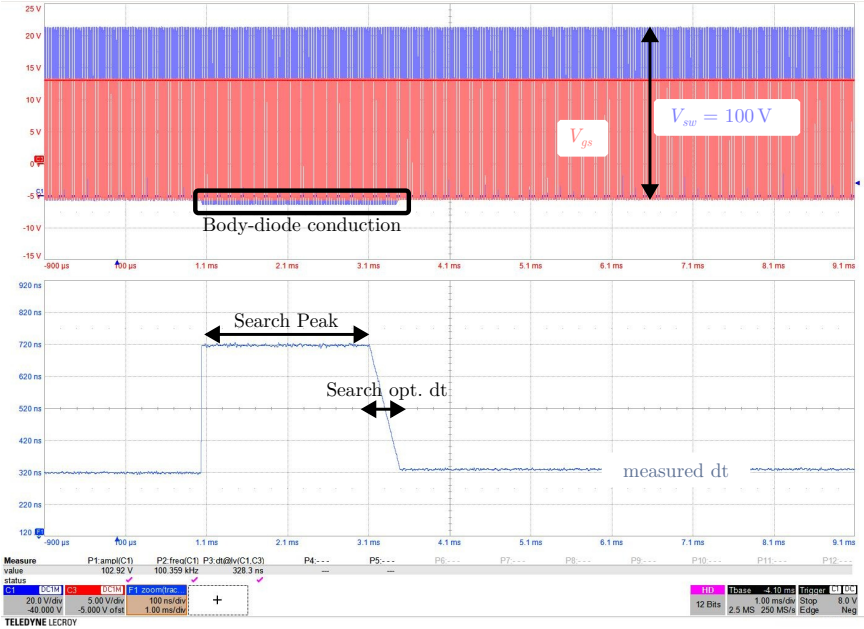

Figure 5.23: Transient capture of dead-time regulating algorithm.

values. As nominal efficiency is not of primary interest, as well as accurate capturing of efficiency not being an easy feat due to inaccuracies in measuring equipment and potential sources of error and arbitrariness from the use of additional helper voltages, the relative efficiency value was chosen as a neutral representation of the effect. The loss in efficiency was thus calculated by referencing each captured value to the maximum value measured. After the sequential capture, the dead-time regulation was enabled, and allowed to complete a few cycles. The set value was then read back over SPI and is highlighted with a circle in Figure 5.24. This process was repeated for four different values of load current to showcase multiple operating points. The results demonstrate the functioning, with deviations between the regulated optimal dead-time and the actual optimal dead-time being within one LSB, representing the quantisation error.

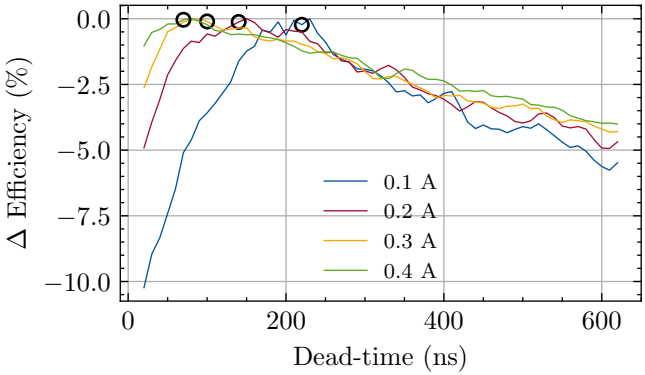

Figure 5.24: Relative efficiency across dead-times and load conditions, with corresponding regulated dead-time highlighted.

CHAPTER 6

CONCLUSION AND OUTLOOK

6.1 Conclusion

Power electronics are foundational to our daily lives. Their relevance is steadily increasing, with energy efficiency and density being key areas where consumers are expecting improvements to further increase usability and reduce inhibitions. The increasing relevance of high-voltage rails in consumer, automotive, datacenter and DC-based energy sectors is creating momentous demand for compact, high-voltage converters that can meet the energy throughput while reducing associated conversion losses. To reduce passive component cost and weight, industry is pushing for increased depth of integration as well as higher switching frequencies. Novel power switches, based on wide-bandgap semiconductors are enabling converters fitting these requirements, while simultaneously creating new challenges in complying with EMI standards, and increasing device longevity that are being confronted by new generations of active gate driver ICs. However, to further reduce the number of components, and increase the energy density of converters, new approaches are required, making more efficient use of components already present in the design.

This thesis presented a novel mechanism to adaptively delay the trigger event of a transistor in order for it to switch under the zero voltage condition. This allows the application to reduce device stress, and node ringing and increase system efficiency. The proposed method works by measuring the gate current and correlating it to the transfer capacitance of the device, thus allowing for the voltage across it to be inferred by detecting marking non-linearities in the transfer function. By integrating the mechanism into the gate driver IC, no additional external components are required. This is a significant advantage in compact converter designs, and specifically so in high-voltage applications due to added component cost and isolation constraints.

The work covered the basic build-up of modern semiconductors, notably modern power MOSFETs used to push boundaries of converter designs through the use of wide-bandgap semiconductors, introducing and explaining the origin of the non-linearity in reverse transfer capacitance that underpins the proposed mechanism. To motivate the importance of ZVS, an appropriate, ubiquitous use-case was introduced, in form of the buck converter. The operating mechanism was explained, and the sources of losses were investigated with a strong focus on the dependency on accurate dead-time setting. Various currently known and used approaches to dead-time regulation were presented and discussed. These include static approaches, as well as modern adaptive and predictive regulation, using a multitude of detection methods, after which the proposed approach was introduced and detailed.

To motivate the integration within the gate driver IC, these were addressed next. Gate driver design and various topologies were discussed, with challenges in the design of output driver stages being investigated further through the proposal and simulation of a programmable, current-based gate driver and its required components: isolated power supply, high-speed level-shifters, current mirror reference and driver stage, in a modern SOI process. The proposal pushes the boundaries of modern active gate drivers, offering technology-limited temporal resolution and programmability as well as an unmatched degree of integration through its variable, application specific supply voltage generation, supporting all modern power transistor requirements. The influence and the associated limitations of parasitic components, including the floorplan layout, bonding and package inductance were discussed, setting the stage for the integration of dead-time regulation as an additional component of closed-loop gate drivers.

The work then presented two discrete implementations of the proposed concept. The first, based on high-voltage vertical SiC MOSFETs, and the second, based on GaN HEMTs, showcased the adaptations needed for the different technologies. These were used to validate the theory previously discussed, both in terms of the efficiency benefits of ZVS, as well as the functional validation of the proposal and its underpinning modelling of the reverse-transfer capacitance. The affirming results of the demonstrators thus act as motivation for a custom, fully integrated solution that would benefit from reduced parasitics and increased flexibility in signal processing, while showcasing the benefits of the topology in not requiring external components.

Finally, the work introduced two gate driver ASICs conceived, developed, implemented and measured at IAS, with the proposed concept built in. Suited for gate-shaping applications, the ASICs make use of a high-speed current-based driver output stage. The individual building blocks of the ICs were discussed before introducing the measurement setup implemented for gate current sensing. Targeting SiC MOSFETs, the ASICs were tested in a buck converter topology driving appropriate switches. The first ASIC implemented just the measurement concept, confirming simulation results and providing an initial testing ground for the ASIC and the design choices made during its development. The affirming results thus justified a fully integrated regulation mechanism. This was presented in form of the second-generation ASIC, where a fully functioning demonstration of a mixed-signal implementation, consisting of a closed-loop regulation adaptively delaying the trigger signal to enforce ZVS, was showcased, with measurements confirming the proposed technique.

Concluding, the findings showed that the proposed approach can be used to achieve ZVS in a buck converter, without having any components connected to the switch node, bar the already-present switching transistors. Achieving both theoretical discovery and experimental validation, using commercially available discrete solutions, and in the integration of a custom designed ASIC, of a novel, and innovative approach, speak to the success of the research and its potential.

6.2 Outlook

The scope of this thesis lies in the introduction of a new concept for voltage sensing across a power transistor. The results show the feasibility of the proposed approach. Nevertheless, ample room remains to further investigate the possibilities of this concept.

Remaining within the bounds of the thesis, two major limitations emerge. The first is the resolution of dead-time variation available to the integrated driver. The major benefits of the ASIC, namely high speed through the 8-phase PLL and custom digital logic as well as low delays through internal connections are thus not fully utilised. A new generation of gate driver ASIC should make use of the full temporal resolution achievable within the

technological and design constraints of the driver stage and its controlling logic in such a way as that the dead-time regulation can make use of it.

The second limitation currently faced is the duration of the regulating mechanism. The algorithm works iteratively, and thus requires multiple switching cycles to determine the optimal dead-time. To improve the dynamic behaviour of the system, a process that captures and processes the transient gate current, determining the optimal delay within one switching cycle of the converter is conceivable. This idea was investigated during the design of the second-generation ASIC. The use of the on-chip burst-mode ADC was planned and implemented, with custom digital logic facilitating the timed acquisition, rapid evaluation of the curve and subsequent setting of the dead-time within 1 µs. However, due to a lack in ADC resolution, the implementation of this approach could not be showcased effectively.

Considering outlooks beyond the scope of the work, the first limitation encountered is the dependency on the peak of the transfer capacitance. To achieve ZVS using the implemented solution, the capacitance is expected to rise significantly and peak at 0 V. While the latter is typical, the rapid rise cannot always be assumed. As discussed in Chapter 2, device manufacturers actively affect the characteristic of this capacitance through the design of the power transistor. Hence, not all transistors exhibit this behaviour. A broader approach could instead entail the combination with other detection mechanisms, such as a predictive approach. To increase device compatibility, other points could instead be detected, and the ideal switching time then predicted using different models describing the voltage slope: a linear one fitting the choice of ZVS transition in the discussed buck converter, or more complex models, such as a sinusoidal one for forced ZVS through resonance. This would thus also broaden the application range. Furthermore, by focussing on multiple detection points, important parameters such as transition $\delta V/\delta t$ could be sensed and fed back to the system regulator, giving more insight into the system's behaviour and thereby acting as a feedback source for gate-shaping applications.

Finally, another outlook lies in the future development of power transistors. Currently, device manufacturers may not knowingly design the capacitance with these possibilities in mind, as it is typically seen more as a nuisance than of active interest. Thus, the main goal of designers lies in minimising it in order to reduce switching losses. However, as shown in this thesis, both goals can be achieved. While small capacitance values will yield lower

currents, a sufficiently sensitive measuring circuitry can be implemented to consistently sense the non-linearity. One major outlook of the approach is thus the active shaping of the capacitance. Through targeted design, manufacturers can assist gate driver designers and provide the necessary non-linearities that gate drivers can in turn make use of. This approach is most probable in manufacturers that provide both switches and drivers, and could thereby provide deeply integrated and coordinated solutions to customers.

BIBLIOGRAPHY

[1] World Semiconductor Trade Statistics (WSTS). *Historical Billings Report*. Tech. rep. Accessed: 2024-01-5. 1987-2024. URL: https://www.wsts.org/67/Historical-Billings-Report.

[2] J.A. Abu-qahouq, H. Mao, H.J. Al-atrash, and I. Batarseh. "Maximum Efficiency Point Tracking (MEPT) Method and Digital Dead Time Control Implementation". In: *IEEE Transactions on Power Electronics* 21.5 (Sept. 2006), pp. 1273–1281. ISSN: 0885-8993. DOI: 10.1109/tpel.2006.880244.

[3] B. Acker, C.R. Sullivan, and S.R. Sanders. "Synchronous rectification with adaptive timing control". In: *Proceedings of PESC '95 - Power Electronics Specialist Conference*. PESC-95. IEEE. DOI: 10.1109/pesc.1995.474797.

[4] Kyota Aikawa, Tomohumi Shiida, Ryunosuke Matsumoto, Kazuhiro Umetani, and Eiji Hiraki. "Measurement of the common source inductance of typical switching device packages". In: *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*. 2017, pp. 1172–1177. DOI: 10.1109/IFEEC.2017.7992207.

[5] Mohsin Asad, Amit Kumar Singha, and Ravada Madhu Sudhan Rao. "Dead Time Optimization in a GaN-Based Buck Converter". In: *IEEE Transactions on Power Electronics* 37.3 (Mar. 2022), pp. 2830–2844. ISSN: 1941-0107. DOI: 10.1109/tpel.2021.3116126.

[6] *ATX12VO (12V Only) Desktop Power Supply*. online. Intel Corporation, 2022. URL: edc.intel.com.

[7] B. Jayant Baliga. *Fundamentals of Power Semiconductor Devices*. Springer International Publishing, 2019. ISBN: 9783319939889. DOI: 10.1007/978-3-319-93988-9.

[8] Steffen Beushausen, Arne Hendrik Wienhausen, and Rik W. de Doncker. “GaN-Based Active Gate-Drive Unit for IGBTs in Medium-Voltage Applications”. In: *2019 21st European Conference on Power Electronics and Applications (EPE ’19 ECCE Europe)*. IEEE, Sept. 2019. DOI: 10.23919/epe.2019.8914945.

[9] W.F. Brinkman, D.E. Haggan, and W.W. Troutman. “A history of the invention of the transistor and where it will lead us”. In: *IEEE Journal of Solid-State Circuits* 32.12 (1997), pp. 1858–1865. DOI: 10.1109/4.643644.

[10] Broadcom. *ACPL-355JC-000E*. Mar. 2023. URL: https://docs.broadcom.com/doc/ACPL-355JC-IGBT-and-SiC-MOSFET-Gate-Drive-Optocoupler-DS.

[11] B. Bryant and M.K. Kazimierczuk. “Modeling the closed-current loop of PWM boost DC-DC converters operating in CCM with peak current-mode control”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 52.11 (2005), pp. 2404–2412. DOI: 10.1109/TCSI.2005.853904.

[12] Annabelle Shu; Peng Chen. “Continental says automotive electronics to take up 45 of vehicle costs in 2035”. In: *DigiTimes Asia* (Sept. 2023). Accessed: 2024-1-5. URL: https://www.digitimes.com/news/a20230906PD202/automotive-ic-continental.html.

[13] Ching-Jan Chen, Ping-Kun Chiu, Yen-Ming Chen, Pin-Ying Wang, and Yu-Cheng Chang. “An Integrated Driver With Adaptive Dead-Time Control for GaN-Based Synchronous Buck Converter”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 69.2 (Feb. 2022), pp. 539–543. ISSN: 1558-3791. DOI: 10.1109/tcsii.2021.3098310.

[14] Fu-Zen Chen and Dragan Maksimović. “Digital Control for Improved Efficiency and Reduced Harmonic Distortion Over Wide Load Range in Boost PFC Rectifiers”. In: *IEEE Transactions on Power Electronics* 25.10 (Oct. 2010), pp. 2683–2692. ISSN: 0885-8993. DOI: 10.1109/tpel.2010.2050702.

[15] Zhipeng Cheng, Han Peng, and Jimin Chen. “More Accurate Miller Capacitor Modeling for SiC Switching Characteristic Prediction in High Frequency Applications”. In: *2019 IEEE 4th International Future Energy Electronics Conference (IFEEC)*. 2019, pp. 1–6. DOI: 10.1109/IFEEC47410.2019.9015024.

[16] Lin Cong and Hoi Lee. "A 150V monolithic synchronous gate driver with built-in ZVS detection for half-bridge converters". In: *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, Mar. 2018. DOI: 10.1109/apec.2018.8341270.

[17] *Cree C3M0045065K Silicon Carbide MOSFET*. C3M0045065K. Rev. 1. Cree, Inc. 2020. URL: https://assets.wolfspeed.com/uploads/2021/05/C3M0045065K.pdf.

[18] Dejana Čučak, Miroslav Vasić, Oscar García, Jesús Angel Oliver, Pedro Alou, José Antonio Cobos, Ashu Wang, Sara Martín-Horcajo, Maria Fatima Romero, and Fernando Calle. "Physics-Based Analytical Model for Input, Output, and Reverse Capacitance of a GaN HEMT With the Field-Plate Structure". In: *IEEE Transactions on Power Electronics* 32.3 (2017), pp. 2189–2202. DOI: 10.1109/TPEL.2016.2569404.

[19] Cecil W. Deisch. "Simple switching control method changes power converter into a current source". In: *1978 IEEE Power Electronics Specialists Conference*. 1978, pp. 300–306. DOI: 10.1109/PESC.1978.7072368.

[20] Analog Devices. *LT8302 Datasheet*. Rev G. URL: https://www.analog.com/media/en/technical-documentation/data-sheets/LT8302-8302-3.pdf.

[21] Xia Du, Yuqi Wei, Andrea Stratta, Liyang Du, Venkata Samhitha Machireddy, and Alan Mantooth. "A Four-level Active Gate Driver with Continuously Adjustable Intermediate Gate Voltages". In: *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2022, pp. 1379–1386. DOI: 10.1109/APEC43599.2022.9773689.

[22] Harry C. P. Dymond, Jianjing Wang, Dawei Liu, Jeremy J. O. Dalton, Neville McNeill, Dinesh Pamunuwa, Simon J. Hollis, and Bernard H. Stark. "A 6.7-GHz Active Gate Driver for GaN FETs to Combat Overshoot, Ringing, and EMI". In: *IEEE Transactions on Power Electronics* 33.1 (2018), pp. 581–594. DOI: 10.1109/TPEL.2017.2669879.

[23] Wilson Eberle, Zhiliang Zhang, Yan-Fei Liu, and Paresh C. Sen. "A Current Source Gate Driver Achieving Switching Loss Savings and Gate Energy Recovery at 1-MHz". In: *IEEE Transactions on Power Electronics* 23.2 (2008), pp. 678–691. DOI: 10.1109/TPEL.2007.915769.

[24] *EiceDRIVER™ 2EDi product family*. 2EDF7275K. Rev. 2.8. Infineon. 2022. URL: https://www.infineon.com/dgdl/Infineon-2EDF7275K-DataSheet-v02_08-EN.pdf?fileId=5546d462636cc8fb0163b0900069305a.

[25] Würth Elektronik. *750318131*. July 2022. URL: https://www.we-online.com/components/products/datasheet/750318131.pdf.

[26] Robert W Erickson and Dragan Maksimovic. *Fundamentals of power electronics*. 2nd ed. Springer Science & Business Media, 2001. ISBN: 978-0-7923- 7270-7. DOI: 10.1007/b100747.

[27] Carlos E Garcia, David M Prett, and Manfred Morari. "Model predictive control: Theory and practice—A survey". In: *Automatica* 25.3 (1989), pp. 335–348.

[28] Jan Grobe, Michael Hanhart, Fabian Maul, Léon Weihs, Leo Rolff, Ralf Wunderlich, and Stefan Heinen. "Design of a Flexible Bandgap Based High Voltage UVLO with Pre-Regulator". In: *2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. 2020, pp. 1–4. DOI: 10.1109/ICECS49266.2020.9294922.

[29] Jan Grobe, Léon Weihs, Michael Hanhart, Ralf Wunderlich, and Stefan Heinen. "Monolithic Integration of a 400 V GaN Half-Bridge Converter With Output Voltage Regulation". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* (2024), pp. 1–1. DOI: 10.1109/TCSII.2024.3398783.

[30] Jan Grobe, Léon Weihs, Jonas Zoche, Ralf Wunderlich, and Stefan Heinen. "A Fast-Response Resonant GaN Converter with Post-Regulation for Distributed DC-Grid Feed-In". In: *2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. 2023, pp. 185–188. DOI: 10.1109/PRIME58259.2023.10161877.

[31] W. Hafez et al. "Intel PowerVia Technology: Backside Power Delivery for High Density and High-Performance Computing". In: *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*. IEEE, June 2023. DOI: 10.23919/vlsitechnologyandcir57934.2023.10185208.

[32] Weijie Han, Qi Cheng, Chen Chen, and Hoi Lee. "Conductive EMI Reduction Techniques for Soft-switched Half-bridge Buck Converters in Automotive Applications". In: *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2022, pp. 646–649. DOI: 10.1109/APEC43599.2022.9773597.

[33] Michael Hanhart, Leo Rolff, Léon Weihs, Jan Grobe, Jonas Zoche, Ralf Wunderlich, and Stefan Heinen. "An integrated Boost Controller with MPPT for Submodule PV Applications". In: *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*. 2021, pp. 231–234. DOI: 10.1109/ESSCIRC53450.2021.9567804.

[34] Michael Hanhart, Léon Weihs, Leo Rolff, Jonas Zoche, Jan Grobe, Ralf Wunderlich, and Stefan Heinen. "An Integrated 50 V Boost Controller With Digitally-Assisted MPPT for Submodule PV Applications". In: *IEEE Open Journal of Power Electronics* 4 (2023), pp. 221–236. DOI: 10.1109/OJPEL.2023.3250762.

[35] Michael Hanhart, Jonas Zoche, Jan Grobe, Léon Weihs, Leo Rolff, Ralf Wunderlich, and Stefan Heinen. "A Half-Bridge Gate-Driver for high-efficient Boost Converter Applications with single-sided ZVS and an adaptive Ringing Suppression Technique". In: *ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC)*. 2022, pp. 289–292. DOI: 10.1109/ESSCIRC55480.2022.9911336.

[36] Xing He, Daniel Li, and Vincent Zhang. "An accurate approach for calculating the efficiency of a synchronous buck converter using the MOSFET plateau voltage". In: *Texas Instruments, Application Note* (2020).

[37] Stefan Heinen, Léon Weihs, Erik Wehr, Tobias Zekorn, Kenny Vohl, Johannes Kuhn, Michael Hanhart, Jan Grobe, and Ralf Wunderlich. *Advances in Analog Circuit Design 2024*. Springer, to be published 2024. Chap. Smart High Voltage Integrated Circuits.

[38] Jochen Henn, Rik W de Doncker, and Stefan Heinen. "Gate driver integrated closed-loop control for electromagnetic emissions and switching losses of wide bandgap power electronic converters". PhD thesis. Institut für Stromrichtertechnik und Elektrische Antriebe, RWTH Aachen University, 2023.

[39] Jochen Henn, Laurids Schmitz, and Rik W. de Doncker. "Dynamic Control of the Switching Behavior of SiC MOSFETs in Converter Operation". In: *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*. 2022, pp. 1–8.

[40] Borong Hu, Yunlei Jiang, Luke Shillaber, Hengyu Wang, Chengmin Li, and Teng Long. "Optically Triggered Self-Adaptive Zero Voltage Switching". In: *IEEE Transactions on Power Electronics* 38.9 (Sept.

2023), pp. 10600–10605. ISSN: 1941-0107. DOI: 10.1109/tpel.2023.3290113.

[41] GaN Systems Inc. *GS-065-008-1-L 650 V E-mode GaN transistor Datasheet*. GS-065-008-1-L. Rev. 220712. 2022. URL: https://gansystems.com/wp-content/uploads/2022/07/GS-065-008-1-L-DS-Rev-220712.pdf.

[42] GaN Systems Inc. *GS-065-150-1-D2*. 2021. URL: https://gansystems.com/gan-transistors/gs-065-150-1-d2/.

[43] Texas Instrument. "An overview of conducted EMI specifications for power supplies". In: *Design note* (2018).

[44] Masakazu Kanechika, Tsutomu Uesugi, and Tetsu Kachi. "Advanced SiC and GaN power electronics for automotive systems". In: *2010 International Electron Devices Meeting*. IEEE, Dec. 2010. DOI: 10.1109/iedm.2010.5703356.

[45] Shusuke Kawai, Takeshi Ueno, Hiroaki Ishihara, Satoshi Takaya, Koutaro Miyazaki, Kohei Onizuka, and Hiroki Ishikuro. "A Load Adaptive Digital Gate Driver IC With Integrated 500 ksps ADC for Drive Pattern Selection and Functional Safety Targeting Dependable SiC Application". In: *IEEE Transactions on Power Electronics* 38.6 (2023), pp. 7079–7091. DOI: 10.1109/TPEL.2023.3244200.

[46] Shusuke Kawai, Takeshi Ueno, Hiroki Ishikuro, and Kohei Onizuka. "An Active Slew Rate Control Gate Driver IC With Robust Discrete-Time Feedback Technique for 600-V Superjunction MOSFETs". In: *IEEE Journal of Solid-State Circuits* 58.2 (2023), pp. 428–438. DOI: 10.1109/JSSC.2022.3201270.

[47] Johannes Kuhn, Tim Lange, and Léon Weihs. "Auslegung eines diskreten Stromquellen-basierten Gate Treibers für SiC MOSFETs". In: *Beiträge zum 18. Dortmunder Autotag*. Technische Universität Dortmund, 2023.

[48] Gi-Young Lee, Chang-Tae Ju, Sung-Soo Min, and Rae-Young Kim. "Gate Driver for Wide-Bandgap Power Semiconductors With Small Negative Spike and Switching Ringing in Zero-Voltage Switching Circuit". In: *IEEE Access* 9 (2021), pp. 145774–145784. ISSN: 2169-3536. DOI: 10.1109/access.2021.3122937.

[49] Binhong Li, Nestor Berbel, Alexandre Boyer, Sonia Bendhia, and Raul Fernandez-Garcia. “Study of the impact of hot carrier injection to immunity of MOSFET to electromagnetic interferences”. In: *Microelectronics reliability* 51.9-11 (2011), pp. 1557–1560.

[50] C. Licitra, S. Musumeci, A. Raciti, A.U. Galluzzo, R. Letor, and M. Melito. “A new driving circuit for IGBT devices”. In: *IEEE Transactions on Power Electronics* 10.3 (1995), pp. 373–378. DOI: 10.1109/63.388004.

[51] K.P. Lisiak and J. Berger. “Optimization of nonplanar power MOS transistors”. In: *IEEE Transactions on Electron Devices* 25.10 (1978), pp. 1229–1234. DOI: 10.1109/T-ED.1978.19257.

[52] Dawei Liu, Harry C. P. Dymond, Simon J. Hollis, Jianjing Wang, Neville McNeill, Dinesh Pamunuwa, and Bernard H. Stark. “Full Custom Design of an Arbitrary Waveform Gate Driver With 10-GHz Waypoint Rates for GaN FETs”. In: *IEEE Transactions on Power Electronics* 36.7 (July 2021), pp. 8267–8279. ISSN: 1941-0107. DOI: 10.1109/tpel.2020.3044874.

[53] Dawei Liu, Simon J. Hollis, Harry C. P. Dymond, Neville McNeill, and Bernard H. Stark. “Design of 370-ps Delay Floating-Voltage Level Shifters With 30-V/ns Power Supply Slew Tolerance”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 63.7 (2016), pp. 688–692. DOI: 10.1109/TCSII.2016.2530902.

[54] K.-H. Liu and F.C.Y. Lee. “Zero-voltage switching technique in DC/DC converters”. In: *IEEE Transactions on Power Electronics* 5.3 (1990), pp. 293–304. DOI: 10.1109/63.56520.

[55] *LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-ns Pulse Width Applications*. Texas Instruments. Oct. 2018. URL: https://www.ti.com/lit/ds/symlink/lmg1020.pdf?ts=1698245649595&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FLMG1020.

[56] Yanick Lobsiger and Johann W. Kolar. “Closed-loop IGBT gate drive featuring highly dynamic di/dt and dv/dt control”. In: *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2012, pp. 4754–4761. DOI: 10.1109/ECCE.2012.6342173.

[57] Josef Lutz, Heinrich Schlangenotto, Uwe Scheuermann, and Rik De Doncker. “Semiconductor power devices”. In: *Physics, characteristics, reliability* 2 (2011).

[58] Robert Mammano. “Switching power supply topology voltage mode vs. current mode”. In: *Elektron Journal-South African Institute of Electrical Engineers* 18.6 (2001), pp. 25–27.

[59] Stefanos N. Manias. “Fully Controlled Semiconductor Devices”. In: *Power Electronics and Motor Drive Systems*. Elsevier, 2017, pp. 695–805. DOI: 10.1016/b978-0-12-811798-9.00010-x.

[60] T. McNutt, A. Hefner, A. Mantooth, D. Berning, and Sei-Hyung Ryu. “Silicon carbide power MOSFET model and parameter extraction sequence”. In: *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC ’03.* Vol. 1. 2003, 217–226 vol.1. DOI: 10.1109/PESC.2003.1218298.

[61] Luyan Mei, David Williams, and Wilson Eberle. “A Synchronous Buck Converter Using a New Predictive Analog Dead-Time Control Circuit to Improve Efficiency”. In: *Canadian Journal of Electrical and Computer Engineering* 36.4 (2013), pp. 181–187. ISSN: 0840-8688. DOI: 10.1109/cjece.2014.2303521.

[62] Alexander Meyer, Leon Weihs, Ralf Wunderlich, and Stefan Heinen. “Adaptive Test Bench Generation, Simulation and Parameter Extraction for AMS Circuitry”. In: *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*. 2021, pp. 1–4.

[63] Alexander Meyer, Léon Weihs, Ralf Wunderlich, and Stefan Heinen. *Semi-Automatic Test Bench Generation and Parameter Extraction Tool using Cadence SKILL*. Presented at Cadence Live Europe. 2022.

[64] Microchip. *dsPIC33CK64MP105 FAMILY*. URL: https://ww1.microchip.com/downloads/aemDocuments/documents/MCU16/ProductDocuments/DataSheets/dsPIC33CK64MP105-Family-Data-Sheet-DS70005363E.pdf.

[65] John M. Miller. “Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit”. In: *Scientific Papers of the Bureau of Standards* 15.351 (1920), pp. 367–385. URL: http://web.mit.edu/klund/www/papers/jmiller.pdf.

[66] T. Mizoguchi, T. Ohgai, and T. Ninomiya. “A family of single-switch ZVS-CV DC-to-DC converters”. In: *Proceedings of 1994 Power Electronics Specialist Conference - PESC’94*. Vol. 2. 1994, 1392–1398 vol.2. DOI: 10.1109/PESC.1994.373866.

[67] Ned Mohan, Tore M Undeland, and William P Robbins. *Power electronics: converters, applications, and design*. John wiley & sons, 2003. ISBN: 978-0-471-22693-2.

[68] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito. "A new adaptive driving technique for high current gate controlled devices". In: *Proceedings of 1994 IEEE Applied Power Electronics Conference and Exposition - ASPEC'94*. 1994, 480–486 vol.1. DOI: 10.1109/APEC.1994.316360.

[69] Blake W. Nelson, Andrew N. Lemmon, Sergio J. Jimenez, H. Alan Mantooth, Brian T. DeBoi, Christopher D. New, and Md Maksudul Hossain. "Computational Efficiency Analysis of SiC MOSFET Models in SPICE: Dynamic Behavior". In: *IEEE Open Journal of Power Electronics* 2 (2021), pp. 106–123. DOI: 10.1109/OJPEL.2021.3056075.

[70] Wai Tung Ng and Andrew Shorten. "Efficiency enhancement and EMI suppression via dynamically adjustable gate driving strength". In: *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*. 2011, pp. 1–4. DOI: 10.1109/MWSCAS.2011.6026365.

[71] Akimasa Niwa, Takanori Imazawa, Ryota Kojima, Masahiro Yamamoto, Takanari Sasaya, Takanori Isobe, and Hiroshi Tadano. "A Dead-Time-Controlled Gate Driver Using Current-Sense FET Integrated in SiC MOSFET". In: *IEEE Transactions on Power Electronics* 33.4 (Apr. 2018), pp. 3258–3267. ISSN: 1941-0107. DOI: 10.1109/tpel.2017.2704620.

[72] John Noto, Gary Fenical, and Colin Tong. "Automotive EMI shielding–controlling automotive electronic emissions and susceptibility with proper EMI suppression methods". In: (2010). URL: https://www.laird.com/sites/default/files/2018-11/Laird-EMI-WP-Automotive-EMI-Shielding-040114.pdf.

[73] A.R. Oliva, S.S. Ang, and G.E. Bortolotto. "Digital control of a voltage-mode synchronous buck converter". In: *IEEE Transactions on Power Electronics* 21.1 (2006), pp. 157–163. DOI: 10.1109/TPEL.2005.861193.

[74] Niall Oswald, Philip Anthony, Neville McNeill, and Bernard H. Stark. "An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations". In: *IEEE Transactions on Power*

Electronics 29.5 (2014), pp. 2393–2407. DOI: 10.1109/TPEL.2013.2278919.

[75] Martin Placek. "Electronics systems have vastly improved vehicle safety over the evolution of the car, such as airbags and anti-lock braking systems." In: *Statista, Deloitte, Semiconductors – the Next Wave* (Jan. 2023). Accessed: 2024-1-5. URL: https://www.statista.com/statistics/277931/automotive-electronics-cost-as-a-share-of-total-car-cost-worldwide/.

[76] Martin Placek. "Projected size of the automotive electronics market worldwide 2021-2027". In: *Automotive Electronics Market: Global Industry Trends, Share, Size, Growth, Opportunity and Forecast 2023-2028* (2023). Accessed: 2024-1-5. URL: https://www.statista.com/statistics/1236129/global-automotive-electronics-market-size/.

[77] Abraham Pressman, Keith Billings, and Taylor Morey. *Switching Power Supply Design*. New York: McGraw-Hill, 2009. ISBN: 978-0071482721.

[78] Infineon Technologies René Mente. "Silizium versus Siliziumkarbid: zwei MOSFETs im Vergleich". In: *Elektronikpraxis* 10 (May 2020), pp. 26–28.

[79] Massimo Rudan, Rossella Brunetti, and Susanna Reggiani. *Springer Handbook of Semiconductor Devices*. Springer International Publishing, 2023. ISBN: 9783030798277. DOI: 10.1007/978-3-030-79827-7.

[80] T. Sakai and N. Murakami. "A new VDMOSFET structure with reduced reverse transfer capacitance". In: *IEEE Transactions on Electron Devices* 36.7 (1989), pp. 1381–1386. DOI: 10.1109/16.30945.

[81] Rohm Semiconductor. *Switching Regulator IC Series: Efficiency of Buck Converter, Application Note*. Application Note. 2022.

[82] Z. Sha, X. Wang, Y. Wang, and H. Ma. *Optimal Design of Switching Power Supply*. Wiley, 2015. ISBN: 9781118790946. URL: https://books.google.vu/books?id=B0b3CQAAQBAJ.

[83] Robert Sheehan and Hilton Anatole. "Understanding and applying current-mode control theory". In: *Power Electronics Technology Exhibition and Conference*. Vol. 10. PES07 Dallas. 2007.

[84] Oleksiy Slobodyan, Jack Flicker, Jeramy Dickerson, Jonah Shoemaker, Andrew Binder, Trevor Smith, Stephen Goodnick, Robert Kaplar, and Mark Hollis. "Analysis of the dependence of critical electric field on semiconductor bandgap". In: *Journal of Materials Research* 37.4 (Feb. 2022), pp. 849–865. ISSN: 2044-5326. DOI: 10.1557/s43578-021-00465-2.

[85] Vaclav Smil. "Waiting for Superbatteries: They still can't match the energy density of liquid fuel". In: *IEEE Spectrum* 59.12 (2022), pp. 21–21.

[86] Siemens Digital Industries Software. *Automotive trends create new challenges for wiring harness development*. Tech. rep. Accessed: 2024-1-5. 2019. URL: https://www.plm.automation.siemens.com/media/global/en/Siemens_SW_Automotive_trends_create_new_challenges_for_wiring_harness_development_WP_tcm27-66866.pdf.

[87] Roger Stark, Alexander Tsibizov, Ivana Kovacevic-Badstuebner, Thomas Ziemann, and Ulrike Grossner. "Gate Capacitance Characterization of Silicon Carbide and Silicon Power mosfets Revisited". In: *IEEE Transactions on Power Electronics* 37.9 (2022), pp. 10572–10584. DOI: 10.1109/TPEL.2022.3164360.

[88] S. Takizawa, S. Igarashi, and K. Kuroki. "A new di/dt control gate drive circuit for IGBTs to reduce EMI noise and switching losses". In: *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196)*. Vol. 2. 1998, 1443–1449 vol.2. DOI: 10.1109/PESC.1998.703241.

[89] Infineon Technologies. *IMZA120R007M1H, CoolSiC™ 1200 V SiC Trench MOSFET*. 2023. URL: https://www.infineon.com/dgdl/Infineon-IMZA120R007M1H-DataSheet-v01_20-EN.pdf.

[90] Ulrich Tietze, Christoph Schenk, and Eberhard Gamm. *Halbleiter-Schaltungstechnik*. 13th ed. Berlin: Springer-Verlag, 2010. 1711 pp. ISBN: 978-3-64-201621-9.

[91] *USB Power Delivery Specification Revision 3.1*. USB Implementers Forum, Inc (USB-IF), Jan. 2023. URL: https://usb.org/document-library/usb-power-delivery.

[92] Dave VanderWerp. "Porsche Taycan's 800-Volt Architecture Enables Slimmer Wiring, Faster Charging, Less Heat". In: *CarAndDriver* (Sept. 2019). Accessed: 2024-1-5. URL: https://www.caranddriver.com/news/a28903284/porsche-taycan-ev-800-volt-charging-performance/.

[93] Zhiqiang Wang, Fei Yang, Steven L. Campbell, and Madhu Chinthavali. "Characterization of SiC Trench MOSFETs in a Low-Inductance Power Module Package". In: *IEEE Transactions on Industry Applications* 55.4 (July 2019), pp. 4157–4166. ISSN: 1939-9367. DOI: 10.1109/tia.2019.2902839.

[94] Prof. Dr.-Ing. R. Waser. *Skript zur Vorlesung Grundlagen elektronischer Materialien und Bauelemente*. 7th ed. Vol. 2. RWTH Aachen University, 2014.

[95] Léon Weihs. "Design and Implementation of an Integrated DC-DC Step-Up Converter for Solar Tiles". BA thesis. Aachen, Germany: Integrated Analog Circuits and RF Systems Laboratory: RWTH Aachen University, Sept. 2017.

[96] Léon Weihs. "Design and Implementation of an Integrated Linear Voltage Regulator". MA thesis. Aachen, Germany: Integrated Analog Circuits and RF Systems Laboratory: RWTH Aachen University, Aug. 2019.

[97] Leon Weihs, Michael Hanhart, Jan Grobe, Jonas Zoche, Ralf Wunderlich, and Stefan Heinen. "A -102 dB PSRR 1.2V Bandgap Voltage Reference for use in a Standalone MPPT Boost Converter for Solar Submodules". In: *2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. IEEE, Oct. 2022. DOI: 10.1109/icecs202256217.2022.9971084.

[98] Leon Weihs, Michael Hanhart, Leo Rolff, Ralf Wunderlich, and Stefan Heinen. "Design of an integrated Maximum Power Point Boost Converter for PV Submodules". In: *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*. 2021, pp. 1–4.

[99] Léon Weihs, Jan Grobe, Linus Rimpl, Tobias Zekorn, Ralf Wunderlich, and Stefan Heinen. "An Adaptive Dead-Time Control Method for Gate Drivers Using Gate Current Measurement Enabling ZVS in High Frequency HV DC-DC Converters". In: *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2023, pp. 1–5. DOI: 10.1109/ISCAS46773.2023.10181638.

[100] Léon Weihs, Erik Wehr, Kenny Vohl, Tobias Zekorn, Ralf Wunderlich, and Stefan Heinen. "A Fully Integrated Adaptive Dead-Time Controlling Gate Driver Enabling ZVS in HV Converters". In: *ESSCIRC*

2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC). 2023, pp. 201–204. DOI: 10.1109/ESSCIRC59616.2023.10268753.

[101] Léon Weihs, Jonas Zoche, Jan Grobe, Ralf Wunderlich, and Stefan Heinen. "Sub-modular MPPT for Decentralised Grid Feed-in Under Fast Changing Irradiation Applications". In: *2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. 2023, pp. 361–364. DOI: 10.1109/PRIME58259.2023.10161806.

[102] Dr Heinrich Welker. "Elektrisches Halbleitergeraet". DE970420C, US2798989A.

[103] *Wideband, Ultra-Low Noise, Voltage-Feedback OPERATIONAL AMPLIFIER with Shutdown*. OPA847. Texas Instruments. Dec. 2008. URL: https://www.ti.com/lit/ds/symlink/opa847.pdf?ts=1698301741579&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FOPA847.

[104] Vahid Yousefzadeh and Dragan Maksimovic. "Sensorless optimization of dead times in dc–dc converters with synchronous rectifiers". In: *IEEE Transactions on Power Electronics* 21.4 (July 2006), pp. 994–1002. ISSN: 1941-0107. DOI: 10.1109/tpel.2006.876850.

[105] Tobias Zekorn, Léon Weihs, Kenny Vohl, Michael Hanhart, Leo Rolff, Ralf Wunderlich, and Stefan Heinen. "Long Term Evaluation of a Pantile-based Maximum Power Point Tracking DC-DC Power Converter for Solar Roof Tiles". In: *2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe)*. 2023, pp. 1–8. DOI: 10.23919/EPE23ECCEEurope58414.2023.10264385.

[106] Shuang Zhao, Audrey Dearien, Yuheng Wu, Chris Farnell, Arman Ur Rashid, Fang Luo, and Homer Alan Mantooth. "Adaptive Multi-Level Active Gate Drivers for SiC Power Devices". In: *IEEE Transactions on Power Electronics* 35.2 (2020), pp. 1882–1898. DOI: 10.1109/TPEL.2019.2922112.

[107] Jonas Zoche, Michael Hanhart, Jan Grobe, Leon Weihs, Leo Rolff, Ralf Wunderlich, and Stefan Heinen. "Design of a High PSRR Multistage LDO with On-Chip Output Capacitor". In: *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*. 2021, pp. 1–4.

CURRICULUM VITAE

Name	Léon Weihs
2019	Master of Science Electrical Engineering, Information Technology and Computer Engineering RWTH Aachen University, Germany
2017	Bachelor of Science Electrical Engineering, Information Technology and Computer Engineering RWTH Aachen University, Germany
2013	University Admission

LIST OF PUBLICATIONS

Peer Reviewed Journals

Jan Grobe, Léon Weihs, Michael Hanhart, Ralf Wunderlich, and Stefan Heinen. "Monolithic Integration of a 400 V GaN Half-Bridge Converter With Output Voltage Regulation". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* (2024), pp. 1–1. DOI: 10.1109/TCSII.2024.3398783

Michael Hanhart, Léon Weihs, Leo Rolff, Jonas Zoche, Jan Grobe, Ralf Wunderlich, and Stefan Heinen. "An Integrated 50 V Boost Controller With Digitally-Assisted MPPT for Submodule PV Applications". In: *IEEE Open Journal of Power Electronics* 4 (2023), pp. 221–236. DOI: 10.1109/OJPEL.2023.3250762

Peer Reviewed Conference Papers

Léon Weihs, Erik Wehr, Kenny Vohl, Tobias Zekorn, Ralf Wunderlich, and Stefan Heinen. "A Fully Integrated Adaptive Dead-Time Controlling Gate Driver Enabling ZVS in HV Converters". In: *ESSCIRC 2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC)*. 2023, pp. 201–204. DOI: 10.1109/ESSCIRC59616.2023.10268753

Léon Weihs, Jan Grobe, Linus Rimpl, Tobias Zekorn, Ralf Wunderlich, and Stefan Heinen. "An Adaptive Dead-Time Control Method for Gate Drivers Using Gate Current Measurement Enabling ZVS in High Frequency HV DC-DC Converters". In: *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2023, pp. 1–5. DOI: 10.1109/ISCAS46773.2023.10181638

Léon Weihs, Jonas Zoche, Jan Grobe, Ralf Wunderlich, and Stefan Heinen. "Sub-modular MPPT for Decentralised Grid Feed-in Under Fast Changing Irradiation Applications". In: *2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. 2023, pp. 361–364. DOI: 10.1109/PRIME58259.2023.10161806

Leon Weihs, Michael Hanhart, Jan Grobe, Jonas Zoche, Ralf Wunderlich, and Stefan Heinen. "A -102 dB PSRR 1.2V Bandgap Voltage Reference for use in a Standalone MPPT Boost Converter for Solar Submodules". In: *2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. IEEE, Oct. 2022. DOI: 10.1109/icecs202256217.2022.9971084

Leon Weihs, Michael Hanhart, Leo Rolff, Ralf Wunderlich, and Stefan Heinen. "Design of an integrated Maximum Power Point Boost Converter for PV Submodules". In: *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*. 2021, pp. 1–4

Tobias Zekorn, Léon Weihs, Kenny Vohl, Michael Hanhart, Leo Rolff, Ralf Wunderlich, and Stefan Heinen. "Long Term Evaluation of a Pantile-based Maximum Power Point Tracking DC-DC Power Converter for Solar Roof Tiles". In: *2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe)*. 2023, pp. 1–8. DOI: 10.23919/EPE23ECCEEurope58414.2023.10264385

Jan Grobe, Léon Weihs, Jonas Zoche, Ralf Wunderlich, and Stefan Heinen. "A Fast-Response Resonant GaN Converter with Post-Regulation for Distributed DC-Grid Feed-In". In: *2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. 2023, pp. 185–188. DOI: 10.1109/PRIME58259.2023.10161877

Michael Hanhart, Jonas Zoche, Jan Grobe, Léon Weihs, Leo Rolff, Ralf Wunderlich, and Stefan Heinen. "A Half-Bridge Gate-Driver for high-efficient Boost Converter Applications with single-sided ZVS and an adaptive Ringing Suppression Technique". In: *ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC)*. 2022, pp. 289–292. DOI: 10.1109/ESSCIRC55480.2022.9911336

Michael Hanhart, Leo Rolff, Léon Weihs, Jan Grobe, Jonas Zoche, Ralf Wunderlich, and Stefan Heinen. "An integrated Boost Controller with MPPT for Submodule PV Applications". In: *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*. 2021, pp. 231–234. DOI: 10.1109/ESSCIRC53450.2021.9567804

Jonas Zoche, Michael Hanhart, Jan Grobe, Leon Weihs, Leo Rolff, Ralf Wunderlich, and Stefan Heinen. "Design of a High PSRR Multistage LDO with On-Chip Output Capacitor". In: *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*. 2021, pp. 1–4

Alexander Meyer, Leon Weihs, Ralf Wunderlich, and Stefan Heinen. “Adaptive Test Bench Generation, Simulation and Parameter Extraction for AMS Circuitry”. In: *SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME*. 2021, pp. 1–4

Jan Grobe, Michael Hanhart, Fabian Maul, Léon Weihs, Leo Rolff, Ralf Wunderlich, and Stefan Heinen. “Design of a Flexible Bandgap Based High Voltage UVLO with Pre-Regulator”. In: *2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. 2020, pp. 1–4. DOI: 10.1109/ICECS49266.2020.9294922

Invited Publications and Presentations

Stefan Heinen, Léon Weihs, Erik Wehr, Tobias Zekorn, Kenny Vohl, Johannes Kuhn, Michael Hanhart, Jan Grobe, and Ralf Wunderlich. *Advances in Analog Circuit Design 2024*. Springer, to be published 2024. Chap. Smart High Voltage Integrated Circuits

Johannes Kuhn, Tim Lange, and Léon Weihs. “Auslegung eines diskreten Stromquellen-basierten Gate Treibers für SiC MOSFETs”. In: *Beiträge zum 18. Dortmunder Autotag*. Technische Universität Dortmund, 2023

Alexander Meyer, Léon Weihs, Ralf Wunderlich, and Stefan Heinen. *Semi-Automatic Test Bench Generation and Parameter Extraction Tool using Cadence SKILL*. Presented at Cadence Live Europe. 2022

Monographs

Léon Weihs. “Design and Implementation of an Integrated Linear Voltage Regulator”. MA thesis. Aachen, Germany: Integrated Analog Circuits and RF Systems Laboratory: RWTH Aachen University, Aug. 2019

Léon Weihs. “Design and Implementation of an Integrated DC-DC Step-Up Converter for Solar Tiles”. BA thesis. Aachen, Germany: Integrated Analog Circuits and RF Systems Laboratory: RWTH Aachen University, Sept. 2017