Development of device design, processing, and instrumentation for scaleable universal quantum computation in silicon germanium heterostructures.

Von der Fakultät für Mathematik, Informatik und Naturwissenschaften der RWTH Aachen University zur Erlangung des akademischen Grades eines Doktors der Naturwissenschaften genehmigte Dissertation

vorgelegt von

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Preface

When worlds collide powerful forces are at play. Misdirected, these tectonics threaten to destruct, but also raise new fields. In high-school I was fascinated of the story of Andrew Wiles and his breakthrough in solving Fermat's last theorem merging algebraic geometry and number theory. In 2007 Guido Burkhard introduced my fellow freshmen and me to the concepts of theoretical physics and teased the idea of quantum computing - a theoretical concept of merging quantum physics and computer science with vast implications for cryptography and intractable problems in computing (Figure 1). This Hilbert-space-race to me appears as one of our generations greatest challenges, that requires to bring together people of many disciplines with mindsets as persevering as creative, and with vast mental capacities. Participating is an experience as inspiring as it is humbling. I am looking forward to serve the area as a translator between the two seemingly disparate worlds of beautiful science and accessible early societal applications.

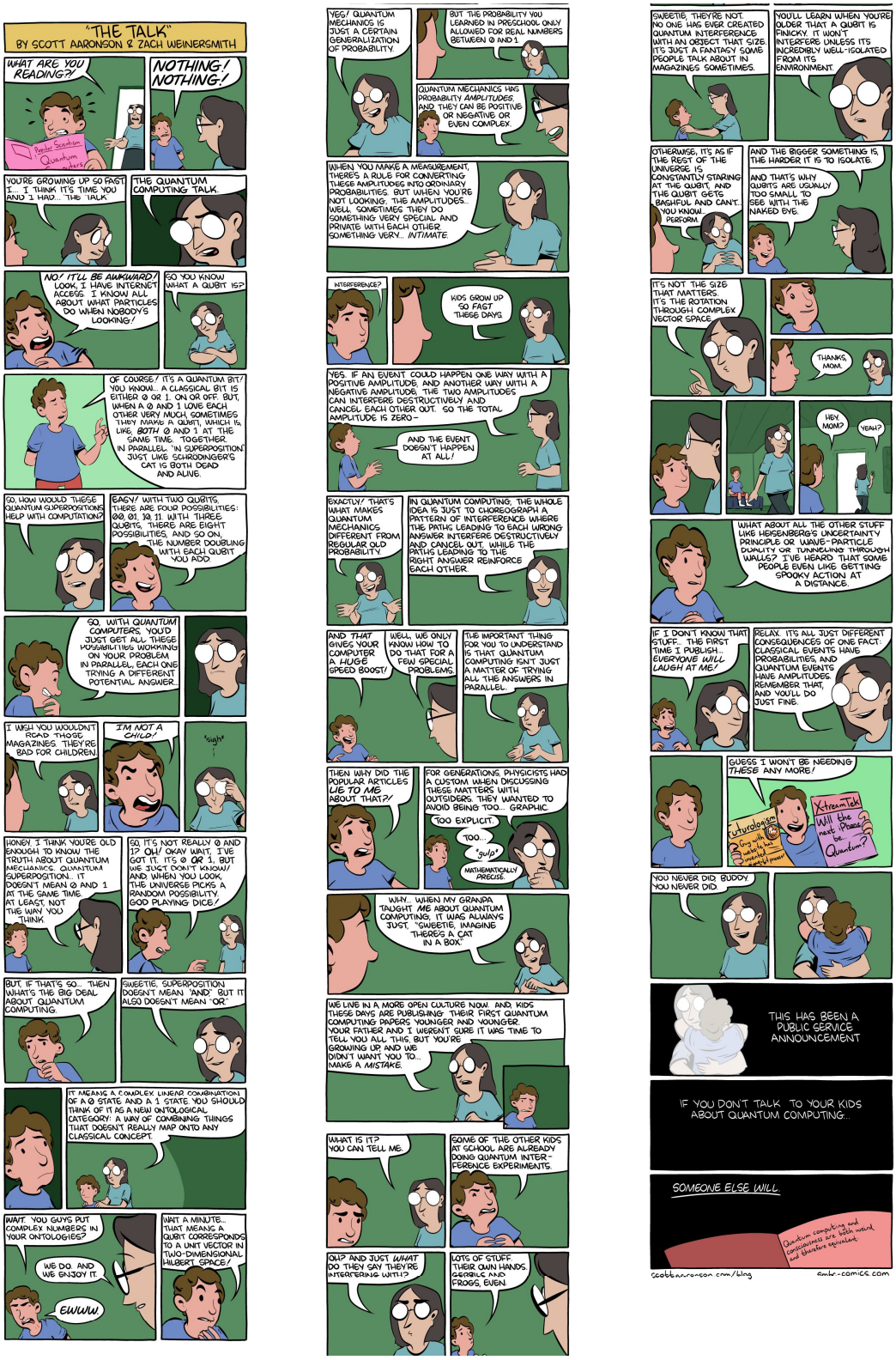

Figure 1.: The Talk - Saturday Morning Breakfast Cereal by courtesy of Zach Weinersmith

Acknowledgements

As a result of a many-year, sometimes meandering journey, this thesis was accompanied and guided at its turns and crossings by generous, warm, and witty guides and fellows, to whom I want to express my greatest appreciation and deepest gratitude. My most profound thanks go to Professor Dr. Hendrik Bluhm for giving me the opportunity to work in his great group, which has an ambitious and curious culture, and for supervising my Ph.D. work. Hendrik with your communication at eye level and joy of scientific discourse, you shaped my understanding of the theory of quantum information science and computing, scientific instrumentation, and pragmatic, intuitive approaches to resolving soft- and hardware issues. I especially value your guidance in scientific communication style during thesis writing. I want to thank Dr. Lars Schreiber for his guidance on the choice of topic, providing the resources to build the scientific setup, as well as the clean room infrastructure facilitation in Aachen. Lars, your work ethic impressed me deeply, and I am thankful for your guidance in the emerging field of silicon quantum computing and detailed feedback on the early drafts of my thesis. Thank you, Professor Dr. Thomas Schäpers, for taking the time and effort as a second reviewer. Thank you, Prof. Dominique Bougeard. Without your and your group's support - especially Christian Neumann and Floyd Schauer - the results of this thesis would not have been possible within a Ph.D. half-life. You provided the quantum dot samples, insightful and regular exchanges on developments of the sample, setup design, and -tuning. Prof. Christoph Stampfer and your team, I want to thank you for the collaboration on the filter box, providing Triton-setups for testing, and driving the efforts with Bachelor students at your institute. I owe special thanks to the group members of the silicon project: Arne Hollmann, your calm and perseverance were critical not only for the hard du-

ties you took over, be it the sample bonding or the ill-configured and stubborn evaporator(s). Without you, we may have lost critical samples or our minds. You were a great office mate, providing an open ear for discussions, new ideas on tuning with your wide Ph.D. network, and the occasional reminder to take science not too seriously. Jan Klos, I am glad and thankful you pursued the open topic of simulating electrostatic and quantum-dynamic properties of the samples, which, with its many discussions and great results, helped to better understand the experimental challenges with our samples. Inga Seidler, your tact and finesse were blissful for the reliability and quality of the fabrication processes and our male-surplus team structure. I want to thank my master's students: Bernhard Klemt you were the first student I supervised and I am glad you bared with me and the institute until the start of your Ph.D., supporting in characterizing the early interposer-prototypes, extending our nanolithography methods to new samples. Felix Borjans, thank you for taking over the experiments we pursued with the first dilution refrigerator setup we built, so I could prepare the second and revised dry-fridge, improving the tunability of our sample and measurement setup, which contributed to the basis of our first publication. Daniel Jirovec, you endured with me the setup and testing of the second dilution refrigerator and I want to thank you for the discussions and contributions to improving the measurement electronics. Tom Struck, you were a great support during the final months of my work at the institute, driving the migration to Python scripted measurement analysis and running immediate analysis. I want to thank my enthusiastic bachelor students - Martin Adams, Lars Feuser, Jacob Foos, Arne Havemann, Philipp Schrinner, and Alexander Shushchyev - for their contributions e.g. to independent validations of sample and setup properties, supporting design decisions, and contributing evidence to prove their functionality. In the silicon team, we built on the great experience from the gallium-arsenide group: Tim Botzem your patience with introducing new group members to the depths of special-measure and quantum dot tuning is invaluable. Thank you for sacrificing time, nerves, and finally hair. Simon Humpohl, your software framework and installation support for the high-frequency equipment measurements and control jump-started the spin-experiment tests in the time-critical final phase of my work. Pascal Cer-

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Contents

Abstract

In this thesis, a measurement and control setup for Elzerman readout and silicon spin qubit experiments, like T1 measurements, is designed and optimized. Developments in amplifier choice and testing, impedance matching, and the design and concept of an interposer-PCB integration platform result in a low-noise, high-bandwidth setup which, after first characterizations, is sufficient for experiments on universal control in silicon quantum dots. Remaining dominant contributions are identified. For critical thermalization with single-spin qubit readout, we have designed and produced multiple cryogenic filters for up to 192 DC lines with transmission characteristics comparable to less scalable PCB solutions. The identified and resolved limitations allow for Elzerman readout at below 1.5 T. Developments in electron beam fabrication enable the smallest gate pitch reported for gate-confined single-layer quantum dots. A setup and tuning protocol is revised to identify dis-functional samples early in the tuning process. The low-frequency noise within the 10-kHz measurement bandwidth for undoped MBE structures is significantly lower in our sample than in previously reported CVD samples. A triangulation method has been developed and improved to quantify the influence of the displacement, the respective electric field strength due to disorder charges and subsequently define limits on defect localization in the sample stack. These are consistent with estimates from other work. These experiments show that the MBE-grown heterostructures, sample fabrication, and measurement setup are suitable for silicon single-spin experiments and provide a direction to further improve reliability, tunability, and fidelity of laterally defined qubits in undoped silicon heterostructures.

In dieser Arbeit wird ein Messaufbau entworfen und optimiert für Elzerman Auslese- und Silizium Spin-Qubit-Experimente. Weiterentwicklungen der vorhandenen Verstärker, Impedanzanpassung sowie das Design und Konzept einer Interposer-PCB-Integrationsplattform ergeben einen rauscharmen Aufbau mit hoher Bandbreite, der nach ersten Charakterisierungen für Experimente zur universellen Steuerung in Silizium-Quantenpunkten genügt. Es werden die verbleibenden dominanten Rauschbeiträge identifiziert. Für die kritische Thermalisierung zur Single Spin-Qubit-Auslese haben wir Tieftemperaturfilter für bis zu 192 DC-Leitungen entwickelt, produziert und Limitierungen aufgewiesen. Diese sind mit weniger skalierbaren PCB-Lösungen vergleichbar und für die Elzerman-Auslese bei unter 1,5 T geeignet. Die Verbesserung der Elektronenstrahllithographiefertigung ermöglichten den kleinste veröffentlichten Gate-Abstand für einlagige Quantenpunkte. Für Funktionstests wurden Setup- und Tuning-Protokolle überarbeitet. Das niederfrequente Rauschen innerhalb der 10 kHz Messbandbreite für undotierte MBE-Strukturen ist in unserer Probe deutlich geringer als in zuvor berichteten CVD-Proben. Um den Einfluss von Unordnung zu quantifizieren, habe ich eine Triangulationsmethode eingeführt und verbessert, um die Quantenpunktverschiebung und die jeweilige elektrische Feldstärke aufgrund von Störladungen zu ermitteln und Abschätzungen zur Stöhrstellenposition zu geben. Diese sind im Einklang mit Schätzungen aus anderen Veröffentlichungen. Diese Experimente zeigen, dass die MBE-gezüchteten Si/SiGe-Undotierten Heterostrukturen, die Probenherstellung und der Messaufbau für Silizium-Einzelspin-Experimente geeignet sind und geben eine Richtung zur weiteren Verbesserung der Zuverlässigkeit, Durchstimmbarkeit und Gatter-Genauigkeit von lateral definierten Qubits in undotierten Silizium-Heterostrukturen.

Chapter 1.

Introduction to Quantum Computing and Thesis Structure

> [...] Trying to find a computer simulation of physics seems to me to be an excellent program to follow out. [...] And I'm not happy with all the analyses that go with just the classical theory, because nature isn't classical, dammit, and if you want to make a simulation of nature, you'd better make it quantum mechanical, and by golly it's a wonderful problem, because it doesn't look so easy.

(R. Feynman 1982 [1])

Richard Feynman's quote inspired many to pursue quantum computing. Little more than a quarter century after his death we can simulate the ground state of the water molecule on these postulated machines Nam et al. [2]. On the way to these results, "ground-breaking experimental methods that enable measuring and manipulation of individual quantum systems" brought Serge Haroche and David J. Wineland the 2012 Nobel prize in physics – the first for the new interdisciplinary field of quantum information followed 10 years later by Alain Aspect, Anton Zeilinger and John F. Clauser for their contributions to understanding quantum entanglement and advancing the field of quantum information. Physicists, engineers, mathematicians, and computer scientists at leading universities and companies worldwide realize the vision of understanding the fragility of quantum mechanical systems

and their coherent control on increasingly integrated quantum computer chips. These systems achieved the thresholds needed for error correction with leading approaches in ion traps [3], superconducting qubits [4] or spin-qubits of various host materials like gallium arsenide [5] or silicon [6]. The latter platform encodes quantum information in the spin degree of freedom of electrons, holes, or nuclei. It builds towards leveraging its great similarity to standard semiconductor technology. This approach may enable scaling to millions of qubits required for algorithms with provable speed-up like Shor's factoring [7], and large-scale error correction [8]. High-quality materials with low defect densities, first achieved in GaAs enabled precise control and complex pulse schemes to prolong the lifetime of the systems by orders of magnitude [9]. Improvements in material quality and the absence of nuclear spins in ^{28}Si supported the rise as a major host material for spin qubits during the last decade and enabled high fidelity gates in silicon [6]. This motivated the pursuit of research paths focusing on multi-qubit coupling via resonators or shuffling systems. Besides challenges in scalable system engineering for 2D lattices of qubits including miniaturized and cryogenic electronics, more basic research is necessary to establish this goal. Spawning multiple almost identical quantum mechanical systems reliably and effortlessly in many devices would free capacities to identify and remedy current limitations. One of these is gate fidelities bounded by noise originating in the host material or cryogenic setups at scale. This thesis establishes the experimental setup for silicon spin quantum computing at our institute. I show that the low defect-density MBE-grown heterostructures [10], sample fabrication, and measurement setups in collaboration with the University of Regensburg are suitable for silicon single-spin experiments. Secondly, based on a variety of samples and high-frequency setup experiments. I provide a direction to improve further the reliability and tuneability of laterally defined electron-spin-qubits in undoped silicon heterostructures. These results are structured as follows:

- **Scientific Context:** This chapter gives an introduction to the theoretical background of quantum mechanics for quantum information science, quantum dots and quantum transport, and state-of-the-art silicon spin-

qubit implementations and experiments.

- **Fabrication:** The sample design regarding heterostructure and gate layout is discussed and improved. The Aachen/Jülich fabrication process is introduced, and an e-beam study is presented, increasing the number of feasible control structures. The gate layout of the silicon quantum dot was improved to ensure a sufficient working range of the charge sensor by switching from a narrow T-shape to a split-gate design. To further reduce the influence of disorder in quantum dot tuning and to improve the charge readout signal new gate designs need to be fabricated. This thesis presents processes introduced at our local facilities in Aachen and Jülich building on a review and improvement of recent methods in the fabrication of Silicon/Silicon Germanium quantum dots.

- **Instrumentation:** Critical choices in materials, filters, and amplifier components are motivated and characterized. For Elzermann-readout critical thermalization, the design, production, and characterization of cryogenic filters are presented. Limitations are identified and solutions are proposed to further improve thermalization. For sample-agnostic and future complex devices, a small- to medium-scale integration platform is introduced. The platform for different electron-spin quantum computing platforms (e.g GaAs and Si), for microwave control and DC or RF readout of S-T0 or single-spin qubits and quantum buses, is characterized and improved.

- **Quantum-dot design and tuning:** A setup and tuning protocol is developed to determine functional samples and support developing and tuning undoped silicon samples toward scalable approaches. Properties relevant to dot tuning and qubit control (hysteresis, low-frequency noise spectra, and electron temperature) are characterized, and a triangulation method for the dot position is introduced, to support tuning and as a probe for the local disorder. Follow-up measurements prove that the heterostructure, sample, and setup enable spin qubit experiments.

Chapter 2.

Fundamentals and Scientific Context

This chapter revises the theoretical background, experimental concepts, and recent results for spin-quantum information processing in Silicon/Silicon-Germanium (Si/SiGe) Quantum dots at a level required for this thesis's experimental design and measurement discussions. It covers the experimental setup, quantum transport, and relaxation time measurements. I assume the reader has a master-level background in experimental solid-state quantum computing. Still, I will also repeat a few more basic concepts in the style of introductory reviews in leading scientific journals.

2.1. Theoretical Background

Quantum Mechanics for Quantum Information Science

The basis of quantum information processing builds upon the simplest non-trivial quantum system – a two-level system or quantum bit with the quantum state $|\Psi\rangle$ and parametrization:

$$|\Psi\rangle = \cos\frac{\theta}{2}|0\rangle + e^{i\phi}\sin\frac{\theta}{2}|1\rangle \tag{2.1}$$

with basis $|0\rangle$, $|1\rangle$, $0 \leq \phi \leq 2\pi$, $0 \leq \theta \leq \pi$ and the normalization condition $\langle\Psi|\Psi\rangle = 1$. The global phase is experimentally inaccessible and, therefore,

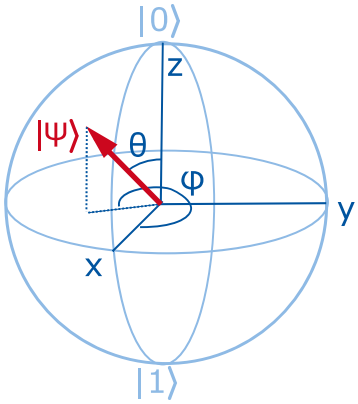

Figure 2.1.: Blochsphere representation: Each spin state is represented by a point on the Bloch sphere $|\Psi\rangle = \cos\frac{\theta}{2}|0\rangle + e^{i\phi}\sin\frac{\theta}{2}|1\rangle$ with the azimuth angle ϕ and the altitude angle θ.

neglected. All these states $|\Psi\rangle$ can be mapped to a unit sphere called a Bloch sphere (see Figure 2.1). In first approximation, the dynamics of this system are assumed to be isolated from any environment and thus described by the time-independent Schroedinger Equation:

$$\hat{H}|\Psi(t)\rangle = i\hbar\frac{\partial|\Psi(t)\rangle}{\partial t} \tag{2.2}$$

$|\Psi(t)\rangle = \hat{U}|\Psi(0)\rangle$ with the time evolution operator $\hat{U} = e^{-i\frac{\hat{H}t}{\hbar}}$ solves the differential equation in this case of a time-independent Hamiltonian. The physical implementation of a qubit we use at our institute is the spin degree of freedom of single electrons. In practice, this spin-1/2-system is not perfectly isolated from its environment. In experimental quantum computation, we have access to several phenomenological parameters describing the effects induced by the environment. Two of them sufficiently describe the qubit dynamics for this thesis and enable a directed exploration of limiting effects and their control: The relaxation time T_1 and the dephasing time T_2. I follow the concise description of Clarke and Wilhelm Clarke and Wilhelm [11]. The relaxation time T_1 characterizes the energy dissipation processes, relaxing the spin from the first excited state to the ground state. The dephasing time T_2 characterizes the time it takes to randomize the phase difference between the two eigenstates.

A more formal way to describe the influence of the environment leading to the relaxation of our spin-1/2 quantum system was covered by my successor in Hollmann et al. [12]: The minimal Hamiltonian describing the system, its environment or bath, and their interaction is:

$$H = H_S + H_B + H_{SB} \tag{2.3}$$

where H_S is the system Hamiltonian of the qubit, H_B is the Hamiltonian of the surrounding bath and H_{SB} describes the system-bath interaction. A theoretical initial state before coupling system and bath can be described as the product state of qubit and bath $|\Psi\rangle = |\Psi_S\rangle \otimes |\Psi_B\rangle$. Describing the environment observed in our solid-state physics experiments as a bath is intentional and relates to its thermodynamic origin of describing a system with many degrees of freedom that are largely unknown and uncontrollable. For the purpose of this thesis relaxation measurments is sufficient to model the environment as classical noise coupling to the system Hamiltonian in practice. In practice, we integrate the noise over the duration of an experiment and several repetitions. This representation can even be extended to guide numerical pulse optimization via the filter function formalism, e.g., in Gallium-Arsenide qubits by Botzem et al. [13]. A convenient and widely applied mathematical approach that can describe this ensemble of quantum states is the density matrix formalism described in Nielsen and Chuang [14]. It describes the ensemble of quantum states by a number of states ψ_i, where i is the index, with the respective probabilities p_i. The density operator or density matrix is then defined by

$$\rho \equiv \sum_i p_i |\Psi_i\rangle\langle\Psi_i| \tag{2.4}$$

and describes an ensemble of pure states. The time evolution of our system is then described by the following phenomenological transformation of the density matrix describing our qubit in interaction with its bath given by Nielsen and Chuang [14]:

$$\begin{bmatrix} a & b \\ b^* & 1-a \end{bmatrix} \rightarrow \begin{bmatrix} (a-a_0)\, e^{-t/T_1} + a_0 & b e^{-t/T_2} \\ b^* e^{-t/T_2} & (a_0-a)\, e^{-t/T_1} + 1 - a_0 \end{bmatrix} \tag{2.5}$$

With a_0 characterizing the thermal equilibrium state, which in our experiments is the spin-1/2 system ground state, thus $a_0 = 0$. The electron-spin relaxation time T_1 in silicon silicon-germanium quantum dots is typically limited by the intrinsic and the artificial spin-orbit coupling; the latter is due to the magnetic field gradient of a micromagnet we use for electrical qubit control and single qubit addressability. Section 2.2 discusses a more profound background on material-specific effects. As a note of caution, I want to add that relaxation times can be reduced by several orders of magnitude via valley-orbit-coupling effects. This is the case if the Zeeman splitting matches the device- and dot-tuning-specific splitting of valley-states: This is the "spin-valley hot-spot" of the external magnetic field, where the short-lived valley-states strongly interact with the typically isolated electron-spin-states as introduced by Huang et al. [15] and Hollmann et al. [12].

Quantum Dots and Quantum Transport

Quantum transport experiments, especially Coulomb blockade measurements, are relevant for the qubit read-out-sensor operation and initial characterization of the quantum dot. The dot will house the electrons used for our qubit experiments, formed from a two-dimensional electron gas in a semiconductor heterostructure. I will briefly introduce the concept of transport through a quantum dot in the constant interaction model in a level of detail sufficient to describe the relevant physics of our characterization experiments. The following model describes our transport measurements of our small capacitance quantum dots, below the order of femtofarad, at low temperatures in the millikelvin-range characterized by $e^2/C \simeq \Delta E \gg k_B T$ with e the electron charge, C the dot capacitance, ΔE the dot energy level separations, k_B the Boltzmann constant and T the temperature. Additionally, the tunnel couplings of the dot to the left (Γ^l) and right (Γ^r) electron reservoirs are small compared to energy splitting and temperature energy scale ($k_b T, \Delta E \gg h\left(\Gamma^l + \Gamma^r\right)$). The reservoirs are experimentally held in thermal equilibrium. The constant interaction model assumes that the interactions of charged particles on and around the dot can be parametrized by a single constant capacitance C_Σ as experimen-

tally observed in a stable setup. Additionally, it is assumed that the single particle eigenenergies are independent of these interactions, thus independent of the number of electrons. In the experiments relevant to this thesis, we measure an electrical current through a quantum dot at liquid helium temperatures, driven by small source-drain-bias voltages $eV_{SD} < e/C$ up to a few millivolts and sweep the dot potential induced by a gate voltage V_G on a capacitively coupled metal gate. These measurements result in windows of blocked current, known as Coulomb blockade, that alternate with peaks in conductivity. This observation can be explained by taking into account the following contributions: Firstly, the energy given by the sum of the single electron eigenenergies or orbital levels ϵ_i, which are quantized due to the hundred-nanometer-scale electrostatic confinement of the quantum dot system. Secondly, the electrostatic energy is given by the Coulomb repulsion between electrons on the quantum dot. Finally, the potential energy from dot electrons with background charges and the potential from the capacitively coupled metal gates as described by [16] or a reduced version of Hanson et al. [17], which excludes negligible capacitive coupling for small source and drain voltages:

$$E(N) = \sum_{i=1}^{N} \epsilon_i + U(N) = \sum_{i=1}^{N} \epsilon_i + \frac{e^2 N^2}{2C_\Sigma} + eN\left(\frac{Q_{bg}}{C_\Sigma} + \sum_{j=1}^{n} \frac{C_j}{C_\Sigma} V_j\right) + const. \quad (2.6)$$

with C_Σ the self-capacitance, N number of electrons on the dot, Q_{bg} background charge (sometimes simplified to donor charge) at zero gate potentials, metal gate potentials (V_j), and capacitances (C_j). The quotient $-\frac{C_j}{C_\Sigma}$ is referred to as lever-arm α. The energy released or absorbed by removing or adding the Nth electron to the island, also known as the electrochemical potential μ_N according to Hanson et al. [17] is:

$$\mu_N = E(N) - E(N-1) = \epsilon_N + \frac{e^2}{C_\Sigma}\left(N - \frac{1}{2}\right) + e\left(\frac{Q_{bg}}{C_\Sigma} + \sum_{j=1}^{n} \frac{C_j}{C_\Sigma} V_k\right) \quad (2.7)$$

With this description, we can reproduce the Coulomb blockade diamonds typically observed in the gate voltage - source-drain voltage plane, where the current is blocked for specific gate voltages because the chemical potential

of the dot is not within the bias window of the source and drain reservoirs. The width of these diamonds is determined by the addition-energy $E_{add}(N) = \mu(N+1) - \mu(N)$. This spacing between consecutive Coulomb resonances can be derived from the previous equation and is given by two contributions of the difference between the single electron eigenenergies $\Delta\epsilon = \epsilon_N - \epsilon_{N-1}$ and the onsite Coulomb repulsion $E_C = \frac{e^2}{C_\Sigma}$.:

$$E_{add}(N) = \mu(N+1) - \mu(N) = \Delta\epsilon + E_C \tag{2.8}$$

At large electron numbers and realistic potentials (anharmonic, finite height), this addition energy is approximately constant due to the reduction of level spacing. Due to spin—or valley degeneracies, electrons can occupy the same orbital with varying spin and valley index, requiring only the coulomb repulsion energy. Transport through the quantum dot sets in if the chemical potential of a quantum dot state is within the bias window ($eV_{SD} = \mu_S - \mu_D$) of the source μ_S and drain μ_D-chemical potentials since electrons can tunnel from occupied states in the source to unoccupied ones in the dot and drain. For simplicity and experimental relevance, I sketch the source and drain occupation as step functions and omit the finite broadening of the Fermi distribution for non-zero temperatures. These transport regions cover the cases (a), (b), and (d) in Figure 2.2. The width of the conducting regions along the V_G axis decreases with reduced source-drain voltage, resulting in sharp resonances at zero bias. The remaining "diamond" shaped regions exhibit zero current due to the Coulomb blockade (case c)). Along the edges of these Coulomb diamonds, the change in potential at the metal gate compensates for the change in bias voltage; thus, the slope yields the lever arm $\alpha = e\Delta V_{SD}/\Delta V_G$, where V_{SD} is the source-drain bias voltage and V_G is the metal gate voltage. Due to our symmetric geometric gate design and voltage operation, we observe symmetric diamonds as sketched in Figure 2.2. Generally, the lever arm can vary for asymmetrical bias voltages and significant differences in capacitive coupling of the reservoirs to the dot, resulting in tilted diamonds.

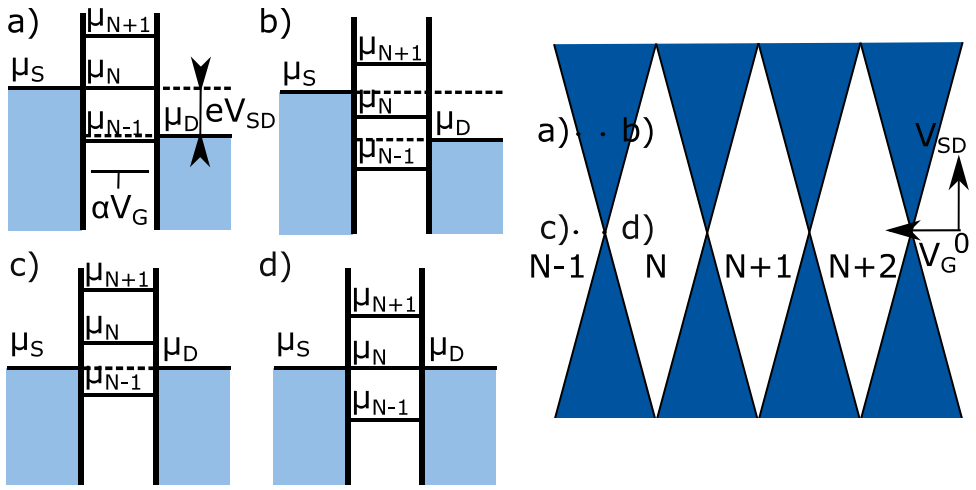

Figure 2.2.: transport in single quantum dots: a) $\mu_N = \mu_S$ dot level resonant with the source chemical potential transport sets in, b) $\mu_D < \mu_N < \mu_S$ dot level is within the bias window, resulting in inelastic transport, c) $\mu_N > \mu_S$ no state available in the quantum dot, resulting in Coulomb blockade, d) $\mu_N = \mu_S = \mu_D$ resonant tunneling at zero bias.

2.2. State-of-the-Art Silicon Spin-Qubit Experiments

Leading implementations that have reached surface code error thresholds in the field of silicon spin quantum computing are metal-oxide-semiconductor (MOS) structures in silicon that induce quantum dots at the interface between silicon and thermally grown silicon oxide with aluminum gates and silicon/silicon-germanium heterostructures where the dots are formed at the band offset at the silicon/silicon-germanium interface of the silicon quantum well. Implanted phosphorus ions in MOS devices are a third platform that achieved error rates within the surface-code error threshold. DiVincenzo [18] presented necessary proof of principle steps for building a scalable implementation. Figure 2.3 shows these milestones in the above systems.

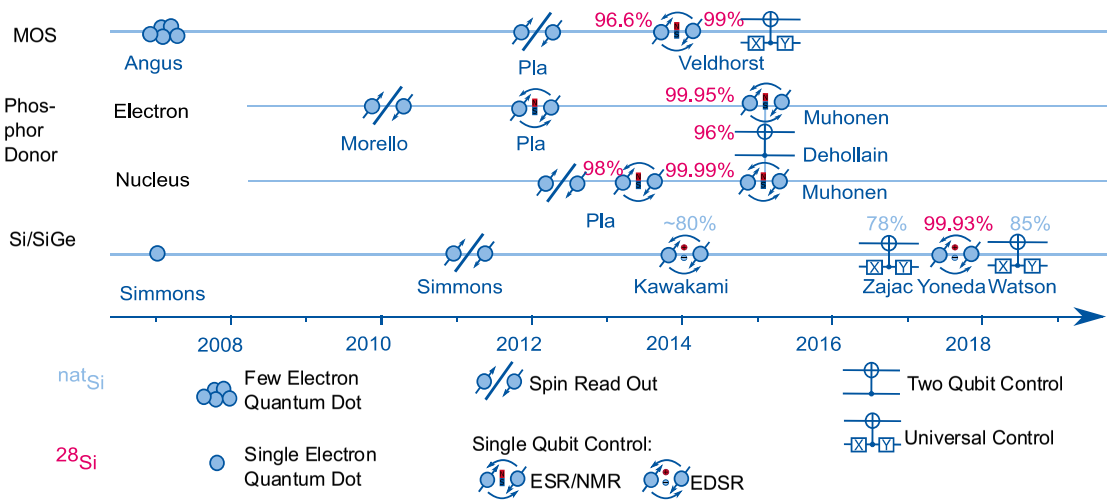

Figure 2.3.: Silicon spin qubits state of the art: Experimental milestones in silicon spin quantum computing: Formation of few and single electron quantum dots, spin readout via spin to charge conversion, single qubit control by electron or nuclear magnetic resonance or electric dipole spin resonance with randomized benchmark single-gate fidelity and two-qubit control using exchange interaction or hyperfine interaction (Bell-state fidelity by tomography).

1. A scalable well-defined 2-level system: The established platforms use electron or nuclear (phosphorus donor) spins as natural two-level systems as proposed by Kane [19] and Loss and DiVincenzo [20].

2. Initialization in a simple state like $|000..\rangle$: The system reaches its well-defined ground state by reloading the electron and waiting for multiples of the relaxation time. Faster relaxation channels due to loading through excited orbital states can reduce this time to 30 ms Simmons et al. [21].

3. Readout of the qubit state: The spin state is usually read out by spin-selective tunneling to the electron reservoirs as first achieved by Elzerman and Hanson [22] and shown in Figure 2.4. The method detects a characteristic rectangular pulse in the sensor current if and only if a spin-up electron has occupied the dot.

4. An universal set of gates (single qubit rotations around two independent axes, two-qubit gate): The electron-spin can be controlled by introducing a second time-dependent magnetic field, which changes the rotation axis of the spin. This effect is called electron-spin resonance (ESR) and is shown in Figure 2.5. For the sake of technical simplicity, the spin is driven by a plane rather than a rotating wave, resulting in additional precession of the spin around the Rabi drive path at the first harmonic of the resonance frequency. This effect averages out since the experiment's resonance frequency is large compared to the Rabi drive frequency. This simplification is called the rotating wave approximation. The ESR is realized by attaching high-frequency current lines to the sample surface. Via the magnetic stray field manipulation, speeds of 150 kHz Veldhorst et al. [23] were achieved. Electric dipole spin resonance (EDSR) is a faster and fully electrical alternative. Electrically induced displacement of the quantum dot induces variations in the magnetic field. As spin-orbit coupling Golovach et al. [24] is small in silicon, a micro magnet induces a $\delta B_z/\delta x$ or $\delta B_z/\delta y$ gradient, transducing an electrically induced shift along the 2DEG plane into B_z variations. First achieved in GaAs, Yoneda et al. [6], Pioro-Ladriere et al. [25] reported 30 MHz operating speeds in

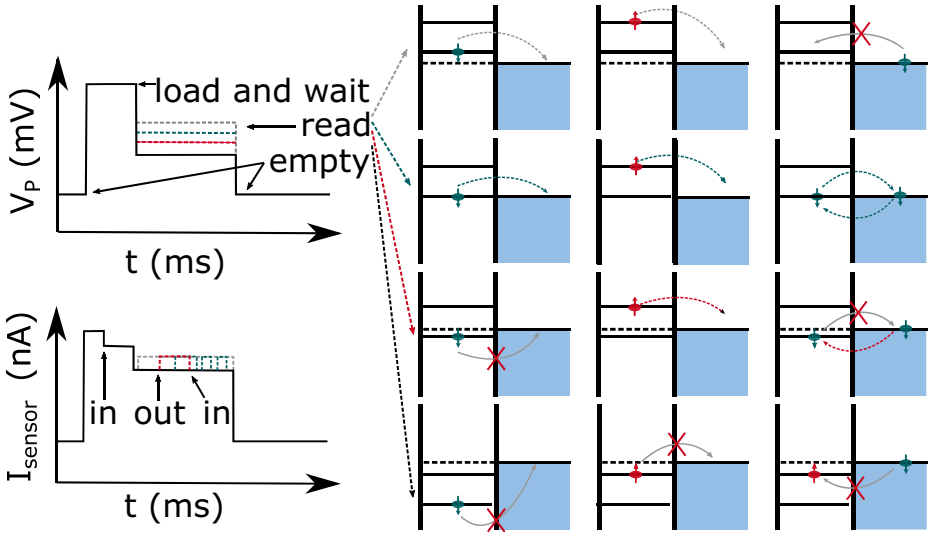

Figure 2.4.: Elzerman spin readout tuning: A voltage pulse, consisting of an "empty", "load and wait", "read", and "empty" level, unloads any electron by shifting the spin-up and down chemical potential above the lead chemical potential, initializes a new electron by shifting both below the lead potential, then waits in the read stage, followed by unloading again. Four regimes of sensor reaction set the variation of the read-level voltage. They all reproduce the voltage pulse shape due to a sensor-gate capacitive coupling with additional discrete jump modulations due to electrons tunnel "in" or "out" events. The left side shows the first tunnel behavior for spin-down (left), spin-up (middle), and further tunnel events (right): grey – spin-independent out event followed by the blockade, petrol - telegraphic spin-independent in-out events, pink – spin-dependent out event followed by a blockade, spin-independent blockade.

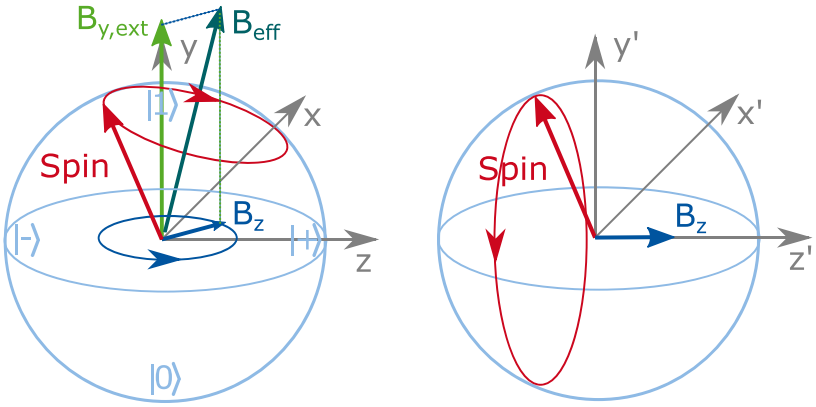

Figure 2.5.: electron-spin resonance: In the laboratory frame (left) the spin precesses around the external field with $f_{res} = g\mu_B B_{y,ext}/h$. A rotating transverse field, e.g.,B_z, shifts the effective rotation axis B_{eff}. Controlled z- or x-rotations ("Rabi drive") are achieved in the rotating frame of the spin (right) when there is a constant $B_{z/x}$, which results in a Rabi drive frequency $f_{Rabi} = g\mu_B B_z/h$. This condition is fulfilled if $f_{res} = f_{B_z}$.

silicon/silicon-germanium devices.

5. Long decoherence times on the operating time scale: A high T_1 is relevant since the relaxation time limits dephasing time. T_{1e} in silicon dots is reported to reach second timescales Yang et al. [26] but can be reduced to milliseconds at magnetic field "valley hot-spots", where short-lived charge-sensitive valley-states are resonant with the Zeeman-split spin-states. A high bandwidth and well-isolated control setup increase the working window outside the hot spot by increasing the upper bound magnetic field for control and decreasing the lower bound magnetic field for readout. T_{2e*} in Silicon is limited by the hyperfine interaction with the ^{29}Si with natural abundance of 5%. Isotope purification improved T_{2e}^* from 55 ns to 270 μs Muhonen et al. [27] in MOS devices. Silicon/silicon-germanium reports state T_{2e}^* 20μs limited by the EDSR spectral width. Nuclear spin lifetimes reach minute timescales Pla et al. [28] and $T_{2n}^* = 300$ ms, up to 30 s for CPMG refocusing pulses Muhonen et al. [27], promising quantum memory applications. The noise's spectral decomposition helps identify and quantify effects, such as characteristic

correlations due to interference or other sources and helps understand the underlying limitations of dephasing times. The correlator of a noisy signal $\beta(t)$ is the expected value of the product of the signal at time t and an incremental Δt later:

$$S_\beta(\Delta t) = \langle \beta(t) \cdot \beta(t + \Delta t) \rangle \tag{2.9}$$

Highly correlated signals (e.g., $\beta(t) = const$) result in a constant correlator, and uncorrelated signals result in rapidly decaying $S_\beta(\Delta t)$. More complex functions with intermediate behavior are less intuitive (e.g., sine waves resulting in cosine behavior). The Fourier transform of the correlator or spectral density is used to identify the characteristic frequencies of the noise:

$$S_\beta(\omega) = \int dt e^{i\omega t} S_\beta(t) \tag{2.10}$$

Correlated sinusoidal signals result in clear peaks, a Gaussian wave package is qualitatively unchanged, and completely uncorrelated signals (white noise) are uniform distributions in frequency space. In between these extremes are signals with slowly decaying correlations, which the slope of their spectrum can characterize as $1/f^\alpha$. This spectrum coincides with spectra from multiple sources of telegraphic noise (e.g., electron traps loading and unloading) with a broad band of characteristic switching times. Yoneda et al. [6] report a $1/f^{1.01}$ spectrum of the qubit frequency from the minute to the microsecond time scale, probably induced by charge noise coupling via a micro magnet-induced longitudinal magnetic field gradient.

The long-term goal of the silicon project in our group is the high-fidelity universal control in MBE-grown, isotopically purified silicon/silicon-germanium heterostructures by EDSR control. Figure 2.6 depicts the sample design concept.

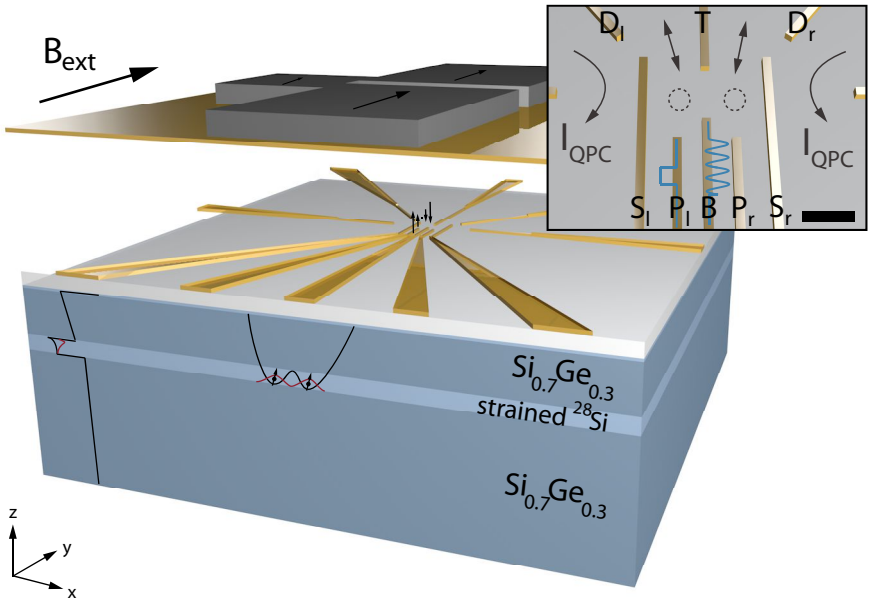

Figure 2.6.: Double quantum-dot micro magnet sample concept: "The Si-SiGe heterostructure including the conduction band structure (black), the 2DEG wave function (red), and the dot potential with the electron wave functions are depicted. The confining gates, the global accumulation gate (gold), and the micro magnet (gray) are separated by aluminum oxide. The magnetic stray field yields a gradient at the dot site required for single qubit manipulation. The inset shows the fine gate layout with a black scale bar of 200 nm length and the dot regions (circles). Side gates (S) set the dot's width, the top gate (T) tunes the interdot barrier, the bottom gate (B) is used for dot displacement, and plunger gates (P) shift the chemical potential of the dots. Two gates on the verge form narrow constrictions (quantum dot contacts/quantum dots). Diagonal gates (D) tune the dot-lead barrier. QPC currents (IQPC) employed for charge sensing and generic gate signals (blue) for pulsing the dot potentials (Pl) and modulating the dot position in EDSR (B) are sketched." Leonhardt [29]

Chapter 3.

Undoped Silicon Double Quantum Dot Design and Fabrication

This chapter introduces the different gate layouts and heterostructures used and developed in this thesis. The design principles are motivated by electrostatic simulations that support the tunability and reliability of quantum dots for scalable silicon computing. In the Helmholtz Nano Facility (HNF) Helmholtz Nano Facility [30], sample processing methods and improvements are presented to fabricate the next generation of sub-100 nm quantum dots in undoped silicon heterostructures grown by the group of Dominique Bougeard.

3.1. Introduction to the Design of the Provided Heterostructures

The 3-layer stack concepts used in this thesis are depicted in Figure 3.1. For initial sample design evaluations, modulation-doped samples were used with a nanomagnet and top gate to control the dopant noise (Borjans [31]). All other devices tested in this thesis are of Stack type 2 with undoped heterostructure. Stack 3 was developed as a basis for future sample designs, fabricated in Aachen, Germany, and using micro magnets as an alternative to the nanomagnet design to compare the suitability for high-fidelity control.

The devices used for milestone experiments in this thesis, produced by Dominique Bougeard's group and the devices developed in our group as ground-

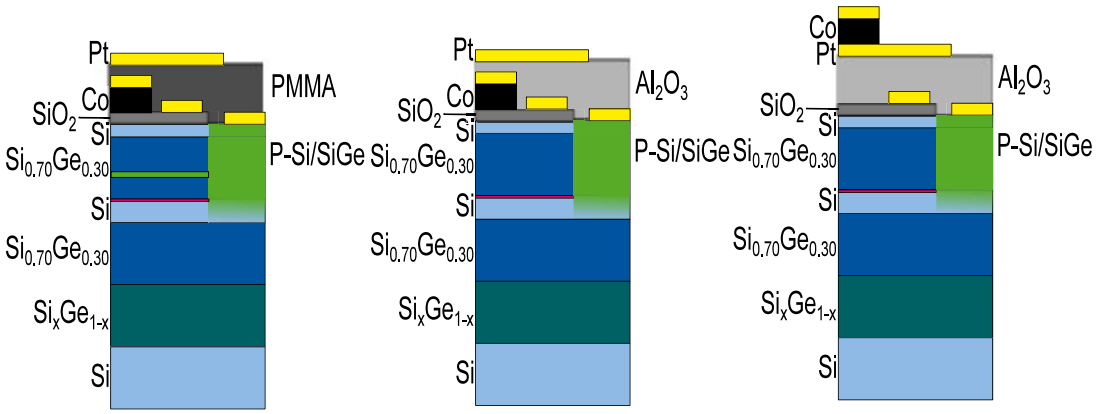

Figure 3.1.: Sample layer stacks used in this thesis: All samples provided use the Regensburg heterostructure: left - Stack type 1 - doped heterostructure with nanomagnet used for the "Hell"-setup characterization, dot tuning, and sample noise evaluation Borjans [31] – fabricated in Regensburg; center - Stack type 2 - undoped heterostructure with nanomagnet used for "SHF"-setup characterization – fabricated in Regensburg, accumulation-induced 2DEG, dot tuning, sample; right - Stack type 3 - undoped heterostructure with micro magnet used for fabrication quality improvements, tested in accumulation experiments - fabricated in Aachen.

work for next-generation samples, are based on the undoped structure of stack types 2 and 3. Dominique Bougeard's group in Regensburg provides the wafers. As reported in Neumann [10], they are grown by molecular beam epitaxy (MBE), where an e-beam evaporator produces a directed beam of atoms that is absorbed and diffused on a heated substrate with atomic layer precision. The MBE is used specifically for silicon and germanium and operates at UHV (ultra-high vacuum) chamber pressures of 10^{-11} mBar and rates of 0.05-1 Å/s. The purified ^{28}Si is grown from a 60-ppm ^{29}Si source one order of magnitude lower than in reported samples [6]. As available methods for substrate production (e.g., Czochralski process) cannot produce binary materials on the periodic table of the element's main group with constant composition, a silicon wafer followed by a graded buffer with varying composition (5%-30%) over 3.75 μm is used. The change in composition induces dislocations due to the different

lattice constants. A constant composition layer of 500 nm ensures the termination of the remaining dislocations Neumann [10]. The 12 nm quantum well is followed by a $Si_{0.7}Ge_{0.3}$ spacer. The thickness of 45 nm is a trade-off between high mobility due to high distance to surface defects, high magnetic gradients, and sharp confinement for a shallow 2DEG. A 1.5 nm silicon cap prevents germanium oxidation and thus damage to the heterostructure. To prevent charge occupation in the cap, its thickness is less than three nm according to simulations in Leonhardt [29] and tests with 7 nm cap samples Neumann [10].

3.2. Review and Improvements on Silicon Quantum Dot Device Design for Efficient Tune-Up

A higher effective mass in silicon compared to gallium arsenide increases the tendency to localize electrons in unintentional dots. The first gate-controlled intentional double quantum dots Maune et al. [32] with S-T0 oscillations were observed in dot systems with approximately 80 nm dot distance. The only system with universal control was provided in a larger design with two unintentional dots in one quantum dot by Watson et al. [33] and a small system by multilayer design by Zajac et al. [34]. This is the first indication of disorder effects on the scale of a few 100 nm and motivates the question of which gate layout is suitable for tunable, robust quantum dot tuning.

Our gate design should provide the following functionality for undoped samples:

1. Lead 2DEG occupation – Creation of a homogeneous 2DEG up to lead tunnel barrier
2. Dot definition – Gates that generate a localized electron system
3. Lead tunnel barrier control – Tunability within the ms-readout time scale
4. Interdot tunnel barrier – Microsecond tunnel rates for fast exchange gates

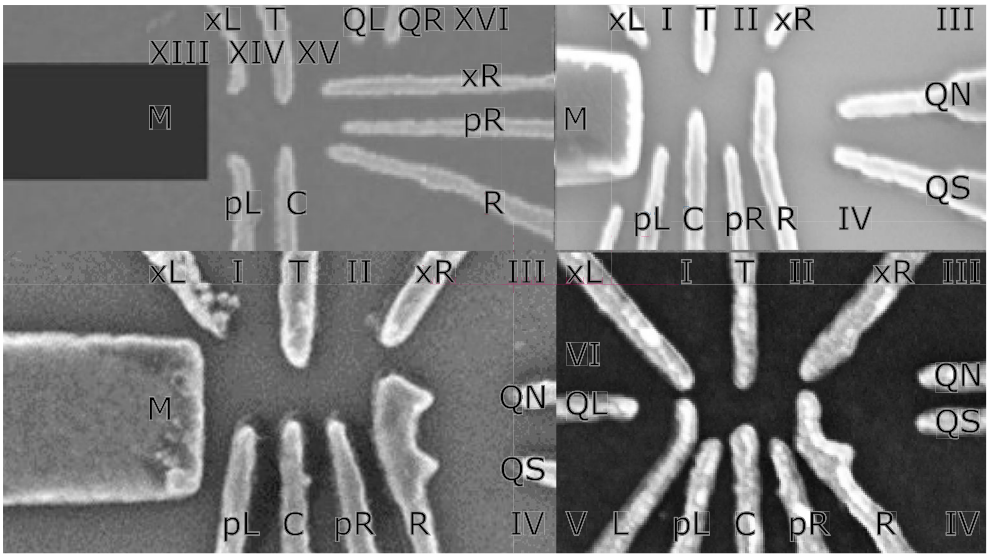

Figure 3.2.: Comparison of the gate layout design type (not to scale, for size reduction, see Figure 3.3): top left - "RBd1" with nanomagnet on the left asymmetric gate layout; top right - "RBud2" with nanomagnet M, increased symmetry, retracted plunger gates, and vertical overlap between R- and T-gates; bottom left - "RBud2" with nanomagnet increased symmetry prolonged plunger gates, shortened R-T overlap; bottom right - "ACud1" symmetrical design with a micro magnet (outside fine gate plane) and additional QPC sensor.

5. Dot potentials – Control of the electron number
6. Dot position – EDSR qubit control by shifting the electron in the magnetic gradient

Doped samples typically required additional gates to deplete the dopant-induced 2DEG connecting the sensor reservoirs to the quantum dot reservoirs. This resulted in lower electron temperatures of the dot reservoirs, facilitating Elzerman readout. In undoped samples, since all fine gates screen the effect of the accumulation gate, this functionality is ensured by feeding one set of gates along the interface of the two reservoirs needing isolation. Ideally, each gate controls one of those parameters to reduce the tuning effort for compensation; this property is called orthogonality.

Figure 3.2 depicts all double-dot designs used in this thesis. The initial design was "RBd1" with a symmetry axis along the double-dot connecting line. "RBud2" is the second Regensburg design symmetric to the T-C axis and is

oriented on the designs from Delft TU Watson et al. [33]. "RBud3" is the third Regensburg design with a shorted side gate "R" and a prolonged diagonal gate "xR/L". The final design written in Aachen is "ACud1" without nanomagnet M and 45° lead openings. The gates' names represent the same functionality in each design: xR/xL - lead barrier tuning; T/C - interdot tunnel-barrier tuning; M/L/R - dot definition; QL/QR/Q/QN/QS - sensor barrier and potential tuning; pL/pR - dot potential tuning and microwave-frequency position shifts. The Roman letters stand for ohmic contacts. The following ideas motivate the main design changes: For reliable tuning, dot-confining electric fields should ideally be more significant or comparable to defect-induced fields, or defects should be scarce on the device scale. Assuming disorder densities in the range of 10^{12}-$10^{14}\,\mathrm{cm}^{-2}$ Bean [35] and 100 nm dot diameters, this corresponds to 100-10000 defects per dot area. The electric field strength (E) of a single charged defect at distance d from the quantum dot is given by (ϵ_0 - vacuum permittivity, $\epsilon_r = 11.7$ - silicon-relative permittivity, e - electron charge):

$$E = \frac{1}{4\pi\epsilon_0\epsilon_r}\frac{e}{d^2} \tag{3.1}$$

A single charged defect at a 1 nm distance creates a 120 mV/nm field, and the corresponding potential has a full-width half maximum (FWHM) of 4 nm. For a defect on the heterostructure surface with a 35 nm distance, this results in an FWHM of 0.1 mV/nm, and 60 nm. Electrostatic simulations for a gate configuration close to experimental values of Sushchyev [36] yield 0.165 mV/nm for "RBud3" and 0.175 mV/nm for "ACud1" in the interdot tunnel barrier region for dot distances of 130 (RB) and 77.5 nm (AC). This scaling factor would reduce the number of defects per qubit by a factor of three. Assuming identical defect distribution over the sample also improves the yield of qubits when focusing on the detrimental tail of the defect distribution in close proximity to the qubit. In conclusion, gate-induced fields and the potential variations are of the same order as the defect-induced ones, with the main contribution assumed to be from interface defects. A smaller dot diameter would be preferable to reduce the number of unintentional dots. These estimates also coincide with the observation of suppressed tunnel coupling and quantum dots in reservoirs

Borjans [31]. Thus, a large opening angle between gates confining the ohmic is preferable. Designs "RBd1" and "RBud2" have gates running in parallel at lead sites: M,xL at XIII, M,pL at XII, T,M,xL at I, QL,T at XV, and T,R,xR at II. These configurations prolong the tunnel barrier region with the risk of unintentional dots. "RBud3" and "ACud1" open directly at the tip of "T" to minimize this channel length. In addition, the prolonged diagonal gates and shortened side gates improve the orthogonality of the design by increasing the lever arm of the diagonal gates, as backed by simulations in Adams [37]. The plunger gates are also prolonged in the two newest designs to improve the lever arm of the high-frequency control.

3.3. Aachen/Jülich Fabrication Processes: 50-nm Pitch e-beam and Optical Lithography, Metallization, Implantation, Dry Etching, and Gate Dielectric Deposition

The final sample fabricated from silicon/silicon-germanium heterostructures is based on implanted ohmics, a multilayer gate metallization, and a micro/nano magnet. In the first step, the wafer is sawn into 3x3 devices of 7x7 mm or, for later versions, 4x4 devices of 10x10 mm. The following paragraphs present the basic concepts of the processes implemented at HNF in the context of this thesis as a foundation for future devices with micro magnets, high-resolution gates, and multilayer processes.

Optical Lithography and Metallization

All micron-resolution structuring processes were performed using the AR4040 Image Reversal Resist. All processes are negative, but increase mask windows for alignment for the Mesa etching. The undercut of the negative processed resists additionally supports lift-off in the metallization process. The 0.7-μm thickness ensures single-micron resolution. All other parameters were cho-

sen at a sweet spot insensitive to experimental conditions (e.g., temperature, humidity). To reduce caking during the implantation, which leads to lift-off residues, a thick resist of 1.4 μm was chosen. Metals were deposited by physical vapor deposition in a PLS570 by applying a 5-nm titanium sticking layer at a rate of 0.1 nm/s and 15-nm platinum at 0.4 nm/s (see recipe Appendix D).

Electron-beam Lithography (EBL) for Scalable Quantum Computing in Si with 50-nm Pitch

A comprehensive study was carried out to determine limiting process parameters and generate lift-off gate patterns for 25 nm gate width and 50 nm pitch devices. Ultrasonic development proved helpful in removing the remaining resist particles that created rough edges and constrictions that resulted in ruptures in the metal gates. Furthermore, cold development has improved the minimal available line width. These experiments were performed with the Raith `e_LiNE` with a maximum acceleration voltage of 30 kV at the highest stable e-beam configuration of 20 kV (Leonhardt [29]). For the investigations in this thesis, the method was introduced at the HNF and optimized for the lidded spinner, which provides strong-edge bead suppression. Best results were obtained for two layers of 50 k (639.04) PMMA and one layer of 950 k (679.02) PMMA, resulting in 100$\pm$20 nm resists with an initial height of the 50-k resist of 80 nm for a sufficient undercut. On the one hand, this layer combination is high enough to ensure a reliable undercut and, thus, lift-off, and on the other hand, it does not limit the resolution due to collapsing trenches with higher resistances. Klemt [38] observed a significant variation in height with samples of different sizes (10x10 mm). To further increase the development contrast, pure IPA was used, as suggested in Busnaina [39]. At Forschungszentrum Jülich, it was possible to use the Vistec EBPG 5000plus in 50 kV and occasionally in 100 kV mode, limited due to 100 kV induced filament shorts. I carried out the initial study, and the best results with the Vistec e-beam writer were reproduced by Bernhard Klemt. Table 3.1 shows the results of the study: While for 20 kV ultra sonic descum processes resulted in 110-nm pitch and 35-nm gate widths, the development at 0°C could slightly improve the gate width

Table 3.1.: line width and pitch for different EBL processes

e-beam technology	Development	Pitch	line width
Raith 20 kV	RT	110 nm	35-40 nm
Raith 20 kV	0°C	110 nm	32-35 nm
Vistec 50 kV	RT	60 nm	30-35 nm
Vistec 50 kV	-5°C	52 nm	30-35 nm
Vistec 100 kV	RT	50 nm	20-25 nm

by 10%. In the Vistec tests, cold development at -5°C slightly decreased by 15% in pitch. In contrast, increasing the acceleration voltage allowed 60-nm pitch at 50 kV and 50 nm at 100 kV. The line width is also reduced to 30 and 20 nm. Alternatively, more complex descum processes using argon sputtering or reactive-ion etching with oxygen reduced the pitch by isotropic etching of the resist or showed no improvement. This shows that, as expected from Shawn Wu et al. [40], the improved beam focus at high acceleration voltage achieves sufficient undercut and resolution to improve the pitch by a factor of 2.2 and the line width by 1.75. In addition, at 100 kV, the process does not require additional cold development (no improvements in pitch or yield have been observed). It yet achieves high stability against dose variations of 20% for the coarse dose and 30% for the fine dose. This reduces the number of dose tests and increases the yield to 80-90% compared to less than 50% with previous processes. The resulting recipe, including optimized software control configuration and comments on the EBL writing, can be found in Appendix D. These contributions enabled a device design in which the dot diameter is at the level of the smallest reported gate-defined quantum dots, while two additional gates are included. Figure 3.3 shows the dot sizes in gallium arsenide, the smallest reported samples in single-layer Si, and devices produced in Regensburg used in this thesis.

Ohmic Contact Implantation

Ohmic contacts are realized by implantation of phosphorus-donor atoms at 20 keV with a dose of $5 \cdot 10^{15}\,\mathrm{cm}^{-2}$, followed by a 5-K/sec ramp to 700°C and

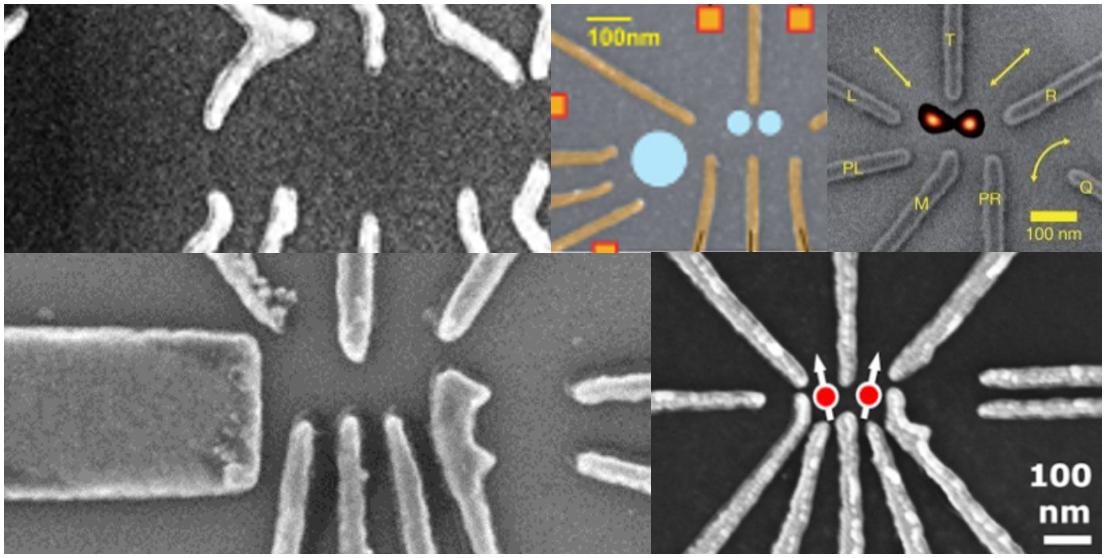

Figure 3.3.: **e-beam pitch development and dot diameter (images drawn to scale):** upper row from left to right - sample generations in gallium arsenide(⌀=0.3 μm), Silicon (Tarucha Group Tokyo ⌀=0.09 μm , HRL ⌀=0.1μm Maune et al. [32]); bottom left - device of the Regensburg cooperation RBud3 Neumann [10] (⌀=0.16μm); bottom right - smallest devices AC design at 100 kV, ultrasonic descum, optimal resist height and combination of PMMA (⌀=0.085μm).

a 15-sec plateau annealing in a rapid thermal annealing step to incorporate the donors at the lattice spots, thereby achieving highly degenerated donor systems near the metal-insulator transition and thus creating a conductive path along growth direction up to the 2DEG in the quantum well Hollmann [41]. To avoid channeling effects along the main crystallographic axes, the ion beam is tilted by 7° against the surface normal. An electrically isolated accumulation gate induces the 2DEG up to the implanted region.

Dry Etching

Etching processes define markers and mesa. Etched markers are sufficient for 20 nm alignment Moers et al. [42] and offer the advantage of metal-free CMOS-compatible fabrication and tool access up to the final steps of gate metallization. Removal of the quantum well under the gate structures outside the quantum-dot region reduces potential leakage currents in case of defects in

the dielectric. It reduces the parasitic accumulation gate capacitance, which is detrimental to RF readout. The reactive ion etching equipment available at HNF enables well-controlled automated dry-etching processes with tetrafluoromethane (CF4) and sulfur hexafluoride (SF6). The first CF4 recipes showed an insufficient selectivity between resist and heterostructure, limiting the etch depth to less than 0.5 μm. Using SF6 as an etchant reduces the physical etch rate and increases the chemical etch rate, resulting in higher selectivity with increased anisotropy. Two processes were implemented by Seidler [43] with different etch rates for the 1-μm marker etching and 100-nm mesa etching by changing the amount of O_2 as a moderator, resulting in etch rates of 1-10 nm/s for Si and 1-50 nm/s for SiGe (see Appendix D).

Gate Dielectric Deposition

For sufficient electrical isolation, atomic layer deposition (ALD) between heterostructure and multiple gate layers offers a method of depositing dielectrics (e.g.,Al_2O_3, HfO_2) with single-atomic layer precision and Angstrom roughness. The precision is achieved by a self-limiting process of alternating saturation of the oxidized sample surface with aluminum atoms from a gas stream of the tetramethylaluminium (TMA) precursor and oxidation by an ozone gas pulse. Before the deposition, the interface is cleaned with acetone and IPA, followed by removing organic material with piranha etch, a mixture of sulfuric acid and hydrogen peroxide. A hydrofluoric acid etch removes the native silicon oxide to create a clean Al2O3-Si interface. The main goal of these steps is to reduce the charge defect density at the interface and dielectric to reduce sample noise and the influence of disturbances in dot tuning. The ongoing research has discussed methods of thermal oxidization and hydrogen saturation by forming gas annealing Spruijtenburg et al. [44] to improve the oxide quality.

Conclusion

In this chapter, design alternatives reduced in size and with additional gate electrodes were presented and motivated to improve the sample tunability for

reduced tunnel barrier opacity and the influence of disorder. New methods for fabricating silicon/silicon-germanium quantum dots were reviewed, and the procedures established at HNF Jülich were reviewed. Increased acceleration voltage and resist stack tuning in electron beam fabrication enabled the smallest gate pitch reported for gate-confined single-layer quantum dots, reducing the number of defects per dot and increasing the number of free control parameters by two additional gates compared to state-of-the-art samples.

Chapter 4.

Instrumentation for Scalable Silicon-Spin Quantum Computing

The research on qubit storage and gate techniques, as well as long-range interconnects for small-scale integrated quantum circuits, places diverse demands on multiple physical and technical properties of the scientific instruments. To meet these requirements, this chapter motivates the design decisions derived from the challenges of the milestone experiments in silicon single-electron-spin quantum computing. Technical possibilities in measurement and control electronics, sample isolation methods, and cryogenic setups are evaluated and experimentally validated. A chip-design-agnostic cryogenic microwave-bandwidth small-scale-integration platform, consisting of a multilayer printed circuit board (PCB) and a novel PCB-to-quantum-chip silicon interposer, is introduced and optimized to reduce super-high-frequency bandwidth (3-30 GHz band, SHF or centimetric waves according to ITU nomenclature [45]) and crosstalk that outperforms conventional quantum-chip design-specific PCB-only solutions in proof-of-concept tests. The presentation of the pre-characterization setup "Bertha", the low-frequency control setup "Hell", and the super-high-frequency control setup "Kurt", which were used for the experiments in this thesis, concludes this chapter on the instrumentation for the precise and fast characterization of early prototypes (e.g., electrical test structures, Hall bars, and quantum dot devices) and final quantum chip samples (e.g., newer two-qubit, future quantum-bus, or small-scale integrated quantum computer devices).

4.1. Experimental Setup Blueprint Derived from Constraints of Silicon electron-spin System Implementation

Heterostructure- and Device Prototype Testing

The optimization of quantum chip design and fabrication processes relies on fast feedback cycles of prototype design, fabrication, and characterization. Early prototypes for testing new materials, fabrication processes, or sample types are evaluated by electrically testing the basic functional parts of the devices. In the case of our silicon quantum-dot devices, these are accumulation gates for the induction of 2DEG, ohmic contacts, or reservoirs to provide electron source and drain, and depletion gates to shape quantum point contacts or quantum dots. Relevant benchmarks are GΩ resistances of each gate to any other electrical contact within their operating intervals (ca. $-2\,\mathrm{V}$ - $4\,\mathrm{V}$) and low kΩ resistances only in the desired current paths of ohmic contacts and 2DEG considerably lower than the conductance quantum ($25.8\,\mathrm{k\Omega}$). The same criteria of electrical isolation between signal lines and low electrical resistance (typically a few Ω) along signal lines also apply to other sample types and the wiring of the setup. This ensures that current flows through the charge sensor of the sample (in the order of $100\,\mathrm{k\Omega}$ but not along other paths (leakage currents). Newer devices achieve these benchmarks even at room temperature by utilizing well-isolating dielectrics. A sufficient number of voltage channels is required to test all electrical contacts and allow for very short test cycles of less than one day for early prototype tested. For the measurement of the kΩ to GΩ resistances, a room temperature test setup with adequate voltage sources and an ampere meter is sufficient.

Quantum Dot Testing

Based on established materials and stable fabrication process, final quantum chip samples, which have passed the quality control of fabrication, pass these electrical tests at room temperature to large extents. Therefore, the tests are

omitted in order to avoid possible damage when rebonding from the chip carrier to the final sample board or chip. The next steps in the progress to quantum bits are the formation of quantum dots and the control of their system parameters: the electron number on the dot, the tunnel rates between lead and dot, dot, and dot (see Chapter 2). The first milestone are the Coulomb blockade measurements. To resolve these features, the charging energy should be significantly higher than any disturbance in the sample or the connected electrical components. The thermal broadening of the electron-Fermi distribution in the reservoirs limits the resonance widths. The thermalization of the electrons to liquid helium temperatures (1-4 K), which is achieved in typical setups, results in a sufficient broadening of 100-400 μeV. Measured resistances are in the range of a conductance quantum 25 kΩ, biases in the range of a few mV resulting in nA currents. These signals are orders of magnitude larger than typical noise levels of control and measurement instruments and other electrical components. Immersing evacuated rods (dipsticks), which hold the sample wiring, filter elements, and the cold finger with the sample holder and sample, in helium dewars, achieves tests of 2DEG accumulation, gate pinch-off, and Coulomb blockade within one to two days. This is the last quick test before experiments on quantum dots in the few-electron regime and finally, qubit-relevant characterizations are executed.

Electron Charge Control - Quantum Dot and Sensor Tuning

A highly sensitive charge sensor is required to reach single-electron quantum-dot occupations and observe single-electron tunneling. We utilize the high transconductance $\frac{dI}{dV}$ of quantized conductivity steps in a quantum point contact or Coulomb resonances in a quantum dot capacitively coupled to the quantum dot under investigation. These signs, ls in the order of a few picoamper, es translate to microvolt variations for typical 10-100 kΩ sensor resistances and set the specifications for amplifiers and voltage sources. To achieve a sufficient signal-to-noise ratio, the measurements are preferably performed at temperatures of <100 mK to maximize the transconductance. The transconductance is limited by the temperature broadening of the lead's Fermi distribution. An-

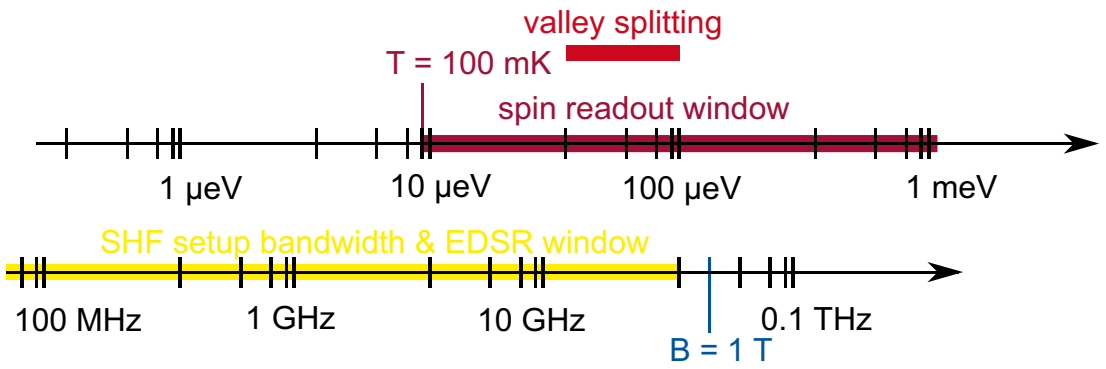

Figure 4.1.: Energy and frequency scales: Zeeman splitting energy scale and corresponding resonance frequencies. Yellow - setup band up to 20 GHz limited by impedance steps at sample-holder connections; Bordeaux - spin readout window limited by lead-electron temperature broadening - 100 mK as a reference; Red - the critical window of the observed valley splittings with fast-relaxation hot spot; Blue - 1 T magnetic field resonance as reference.

other source of electrical noise is thermal fluctuations in resistors or capacitors (Johnson Noise), which are used in low-pass filters to isolate the sample from high-frequency electrical noise on the signal lines extending to room-temperature equipment. Choosing elements with less than 100 kΩ and more than 100 nF at room temperature or cooling the elements to liquid-helium temperatures ensures sufficient noise performance even for 10 kHz bandwidth (BW) lines given by the root-mean-square voltage variations of $v_{rms} = \sqrt{k_B T \cdot R}$ and $v_{rms} = \sqrt{k_B T / C}$, e.g., typical resistors are in the range 100 Ω-10 kΩ, and capacitors in the range 0.1-10 nF (for cut-offs range 1 Hz-100 kHz as used in low-frequency control for transport measurements) and are cooled below 1 K.

electron-spin Measurement and Control

Spin readout in the Elzerman scheme requires a large Zeeman splitting compared to the thermal broadening of the Fermi distribution in the reservoirs.

This guarantees that unoccupied lead states are only available for high-energy up-spin and not for spin-down electrons. Electron temperatures of 100 mK (corresponding to 8.6 µeV or 75 mT) and below provide a low background of false positive (spin-down) counts and additional flexibility in the choice of a magnetic field, e.g., to avoid valley relaxation hot spots with low T_1 and T_2. Spin control via EDSR is limited by the bandwidth of the SHF control lines: Magnetic fields of 1 T ($E_{Zeeman} = 115\,\mu eV$) require 28 GHz signals. The EDSR transition line width is approximately 50 kHz [6], which is is due to the reduced Overhauser field fluctuations of 2μT in isotopically purified Si^{28} compared to natural silicon (1.85 mT) or gallium-arsenide (3.6 mT) [46]. This shallow line width enables high-fidelity gates and many-qubit frequency multiplexing only if transitions are driven precisely at the resonance frequency. A magnetic field supplied by the superconducting magnet without drift aids resonant driving during benchmarking runs of hours to days without recalibration of the drive frequency. Low-noise power at the resonance frequency compared to the mW drive signals minimizes over- or under-rotation.

4.2. Thermal and Electromagnetic Sample Isolation

In order to achieve the specified requirements, the sample must be thermal and electrical isolated to ensure low temperatures of the atomic lattice and attenuation of any unwanted electronic signals from the timescale of the experiments (millisecond spin readout times up to days for relaxation time or gate-benchmarking measurements) on timescales corresponding to thermal (THz) radiation. This section reviews the concepts for designing the isolated setups used in this thesis and supports the process of "noise hunting" by providing an overview of noise sources, physical mechanisms, and characteristic frequencies as well as measures to mitigate noise. The black-body model can be used to quantify the attenuation of any excitation by room temperature, which is necessary to avoid any sample disturbance. Planck's law describes the spectral

distribution of radiation power for a black body at a given temperature.

$$S_{E,T} \propto \frac{1}{\exp \frac{E}{k_b T} - 1} \tag{4.1}$$

The attenuation required to completely thermalize room temperature excitations is given by the quotient of S_E at 30 mK and 300 K.The result is an attenuation of four orders of magnitude at low frequencies and an exponential quantum cut-off range of a few GHz. This sets the threshold for the optimal thermalization and evaluation of the following measures. Thermal insulation is crucial to achieving low sample temperatures as the cooling capacities in modern cryostats are typically less than 1 A radiative transfer is excluded by using polished, highly reflective metallic radiation shields for each temperature stage. The heat conduction between the stages is reduced by generating a sufficient vacuum (1×10^{-4} mbar) and AC coaxial lines, that are superconducting for insulation below 1 K levels. Each isolated stage consists of materials with high thermal conductivity at the respective temperatures. Materials with high electrical conductivity are used, such as oxygen-free high-thermal conductivity (OFHC) copper ensure sufficient thermal conductivity at mK-Temperature to their vanishing thermal conductivity; superconducting materials are to be avoided when thermalizing DC lvity. Alternatively, magnetic fields that break superconductivity (e.g., aluminum bond wires - critical field 10 mT [**?**]). Within the stages, all parts are thermalized (especially parts connected with higher temperature stages, such as wires) by providing plane metal contact surfaces that are connected with sufficient pressure. Wires are clamped or wound around copper rods and fixed with cryo-compatible heat-sink varnish (e.g., GE varnish). The inner conductors of coaxial cables can be thermalized by electrical attenuators which connect the inner conductor to the ground via a resistive voltage divider. The effectiveness of the thermal insulation can be evaluated by temperature measurements at the mixing chamber plate using ruthenium-oxide or SQUID-noise thermometers and later by measurements of the electron temperature by determining the width of the Fermi distribution in the reservoirs. Electrical isolation is of utmost importance to avoid unwanted

excitations in the device under test and to obtain a measurement signal, that is clearly distinguishable from any background signal. As magnet quenches or failure can generate life-threatening voltages, rectifier diodes (e.g., IXYS MDD4412N1BA) are used. Their non-linear I-V curve insulates low-voltage signals from the setup but prevents dangerous high-voltage buildup. Electric interference can be caused by direct electromagnetic (EM) coupling into the signal line or into the shielding ground, which is particularly important for differential measurements (inner and outer conductors). Furthermore, indirect effects such as dissipation, microphonics, or piezoelectrics add further channels for conversion, e.g., mechanical signals to electrical noise. This list presents the most important mechanisms and measures to minimize their impact:

Resistive coupling takes place via of electric interference from control and measurement devices to the signal line. Sources that couple resistively can be control or measurement electronics (amplifiers, voltage sources, arbitrary waveform generators, microwave sources) connected directly to the signal line (in case of wrong specifications or malfunctions) or other devices that share the ground line and are not optimized for low-noise measurements, such as PCs (especially switching power supplies generate kHz-switching signals), data transfer equipment (GPIB, LAN generate signal bursts), or electronic devices in nearby rooms. Building ground tends to carry a variety of signals, especially if several rooms share them and the grounding rod does not have a significantly low resistance towards the soil(several orders of magnitude lower than the resistances in the setup) or is located at a distance of the order of ten meters from noise sources such as buildings. Residual signals can be filtered by lumped element filters like RC- or Pi-filters or by dissipative filters specifically designed for the application such as copper powder epoxy filters. The design of these filter boxes is discussed in detail in the chapter Instrumentation. Common mode interference from switching power supplies can be suppressed by wrapping measurement lines around ferrites (available for the range 100 kHz-100 MHz). For the isolation of high-frequency to microwave electronics such as arbitrary waveform generators or microwave sources, high-performance isolation transformers (e.g., Breimer-Roth BE1600) are used on the power supply side of the equipment. This is due to the absence or high cost of high-bandwidth (low-

distortion) isolation amplifiers.

Inductive coupling of alternating magnetic fields occurs when loops of low-impedance cables are created, typically by connecting equipment ground to the setup ground and closing the loop to the building ground. The induced currents caused by stray fields from transformers, and power lines increase with loop size and are dominated by power-line hum (50 Hz), its higher harmonics, and the kHz noise from switched-mode power supplies. Various contact and wire resistances cause voltage fluctuations at the differential inputs and outputs of the measurement devices, leading to noise on the signal line. The effects can be minimized by the correct choice of measurement equipment and by establishing low-resistance contacts (sub-mΩ range) along a star-like grounding scheme in order to minimize the buildup of voltage differences. Helpful measures are the use of batteries instead of noisy power supplies, galvanic insulation of the setup ground from all other ground, removing unnecessary insulation from LAN/USB-cables, use USB (Delock G62588)/GPIB (TI GPIB 120B) isolators, setting measurement equipment in- and outputs to "floating" (devices should use at least MΩ insulation resistors), gain-one insulation amplifier circuits (INA118, AMP03 with at least MΩ resistances to ground) or optocouplers (photodiode-phototransistor circuits) with kilohertz up to several megahertz bandwidths in low-frequency signal lines. If unavoidable, minimize the loop size by using twisted-pair wires (e.g., woven loom inside the refrigerator) in current-carrying lines connected to ohmics. During the setup process, make sure that new parts (typically: still line, pulse-tube lines, setup racks, supply lines, Fisher connections) are well insulated. This allows the insulation 1-10 MΩ to be achieved without great effort, which has proven to be sufficient for our sample systems. The direct coupling of alternating magnetic fields is less problematic because the Earth's magnetic field or radio signals are weak compared to the applied fields and gradient fields used for EDSR but could be further reduced by μ-metal shields with low permeability.

Capacitive coupling directly couples electric fields into any signal line. It can easily be avoided by using coaxial cables and minimizing the length of cables carrying small signals by positioning amplifiers with sufficient noise performance early in the signal line.

Indirect EM-coupling is caused by dissipative effects in lumped elements (Johnson noise in resistors and capacitors), which are related to current and voltage fluctuations, microphonics either by cables moving in magnetic field gradients and thereby inducing currents, or capacitance changes, e.g., due to variations in the plate distance, piezoelectric effects, typically found in dielectrics (e.g.,All X7R, less pronounced in NP0) of lumped element capacitors. Further mechanisms are thermoelectric effects together with thermal drift, e.g., due to different wiring materials that can generate voltage and current levels harmful to the sample, or triboelectric effects where charges are separated by the movement of a dielectric against the outer conductor [47]. These channels can convert mechanical vibrations of rotary valves (140 Hz for the pulse-tube valves) or from the pulse-tube pressure bursts (periods of seconds, audio frequency range) into electrical noise. These effects can be reduced by using coaxial cables with a conductive dielectric coating (e.g., graphite - Huber& Suhner RG174 for BNC applications), fixing of the wires in magnetic fields (with GE varnish or cryo-compatible adhesive foil such as Kapton), damping of mechanical oscillations by wrapping the compressor lines with acoustic insulation foil (10 mm foam and 1 mm lead), and decoupling of the pulse-tube valves with spring suspensions and bellows from rack and cryostat.

During the stage of setting up the cryostat and before connecting any equipment, the grounding quality is ensured by resistance measurements from the cryostat ground to possible ground connections. The final setup (without sample) or new control and measurement equipment can be tested by using low-noise preamplifiers (e.g., voltage amplifier - SR560, IV-converter BaselSP983 for kΩ sample resistances) connected to a spectrometer (Agilent E4446A) or oscilloscope (Tektronix DPO 7104C) to generate the noise spectrum directly or from time-traces and fast Fourier transform. Note that this equipment may also require grounding insulation (isolation transformers, isolation amplifiers, or battery power supplies). The derived noise spectra display broadband contributions (corresponding to short correlation times – “uncorrelated noise” or “white noise”), sharp peaks (“interferences” from coherent signals from electronic equipment), and intermediate contributions (“colored” or “pink” noise with a millisecond to second correlation times which, for example, originate

from switching processes in semiconductors, temperature drift in amplifiers, or aging in photo elements with $1/f$ behavior). Using low- and high-impedance test resistors (including a sample dummy) makes it possible to distinguish the contributions of voltage noise and current noise in the system and predict the noise level for future sample characterizations. The exemplary shape of the obtained spectra and the respective sources are shown in Figure 4.2. To identify the dominant sources, it may be helpful to plot the running total of the RMS noise ($\sqrt{\Sigma S(f) \cdot \Delta f}$ - with power spectral density $S(f)$ and frequency increment Δf).

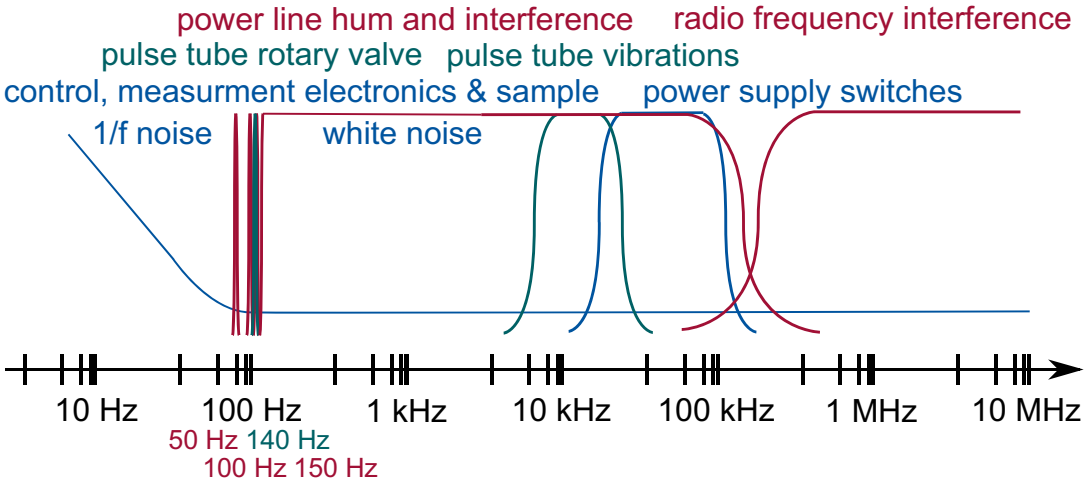

Figure 4.2.: Noise and interference: Spectral distributions of noise sources in quantum transport setups with cryogen-free cryostats. Blue - direct resistive coupling sources; Bordeaux - inductive and capacitive coupling sources; Petrol - indirect coupling of mechanical vibrations.

4.3. A Robust and Compact Cryogenic Lowpass Filter Thermalizer for $\mathcal{O}(100)$ Lines and Identification of Limiting Effects

Quantum transport applications in quantum computing or 2D materials require well-isolated and thermalized systems to measure and utilize sensitive quantum effects. One application is reducing the electron temperature to increase the Elzerman readout fidelity. Sample complexity is increasing, and higher sample throughput is required for studies on reproducibility and hero device discovery. This increases the size and complexity of the setup, and the cryostats in our labs reach the order of 100 DC lines for multi-sample cooling and future multi-qubit or quantum-bus chips.
This section provides an overview of the design principles of a combined compact lumped-element and dissipative filter, evaluates current design limitations in an additional test setup, and presents approaches to resolve these and realize a scalable thermalizer approach using an RC-, copper-powder filter combination to meet the specifications for spin readout and control introduced in Section 4.1.

In the widely used lumped element approaches with RC filters, Pi filters are limited by parasitics that generate resonances in the radio-frequency range relevant to our experiments and do not provide the required exponential cutoff. Evolved solutions use the dissipation of skin-effect eddy currents in metal-powder epoxy filters [48–51], copper tapeworms [9] or thermo-coax [52], and reach $\sim 10\,\mathrm{mK}$ thermalization, but have a large footprint or the tendency to break due to thermal cycling. An overview of the different filters can be found in [53].

We designed and produced reproducible, compact filters with $\mathcal{O}(100)$ lines that are robust against thermal cycling and high voltages as tested in [54] that are based on the PCB copper-powder filter design of [51]. For further details, see Appendix B. To identify the limiting effects generating detrimental resonances in the gigahertz band as observed in other groups [51] and in our filterbox, I developed and characterized a two-port prototype resulting in design

improvement principles for the multi-line box to achieve a >120 dB attenuation up to 50 GHz. These figures are limited by background noise levels in relation to the maximum output amplitude of the measurement setup and measurement time.

Filterbox Blue Print

The ideal attenuation of the room temperature part of the setup characterized by black-body radiation with spectral density $S(\omega, T = 300K) = \hbar\omega / (e^{(\hbar\omega/k_bT)-1}$ at room temperature is achieved when the resulting spectrum at the sample site corresponds to the mixing-chamber temperature of 30 mK ($S_E(300\,\mathrm{K})/S_E(30\,\mathrm{mK})$). The resulting curve with a 45-dB attenuation at low frequencies and an exponential cut-off gigahertz range is depicted in Figure 4.3. The filter should withstand tens of cooling cycles up to the mK working point and maintain its attenuation performance. In addition, the design should be robust enough for transport experiments in graphene. These samples leveraging multi-layer graphene and high electric fields to tune material parameters require back-gate voltages up to 180 V (to create out-of-plane electric field gradients) and 100 mA currents (for disorder reduction by current annealing) as sample requirements of Stampfer AG at the 2nd Institute of Physics. A modular design allows retrofitting for new samples. Weight and form factor should be within the specifications of the cryostat supplier.

As suggested by Bladh [53], RC filters form the first filter stage, followed by a metal-powder filter stage based on the skin effect and dissipation at high frequencies. Simulations of the expected transmission curves of the individual stages, including parasitics (estimates based on geometric dimension), are depicted in Figure 4.3. RC filters with a high kHz-bandwidth are chosen for the ohmic readout lines and low Hz-bandwidth filters for the gates. Both show resonances caused by parasitic LC resonances in the 10-GHz range. Pi filters reduce the effect, but only metal-powder filters can produce the exponential cut-off by the skin effect ($\propto e^{\sqrt{\omega}}$).
The design of the resulting filter box with 48 lines is shown in Figure 4.4. The 48-line design consists of a cooper-powder filter box with robust CINCH con-

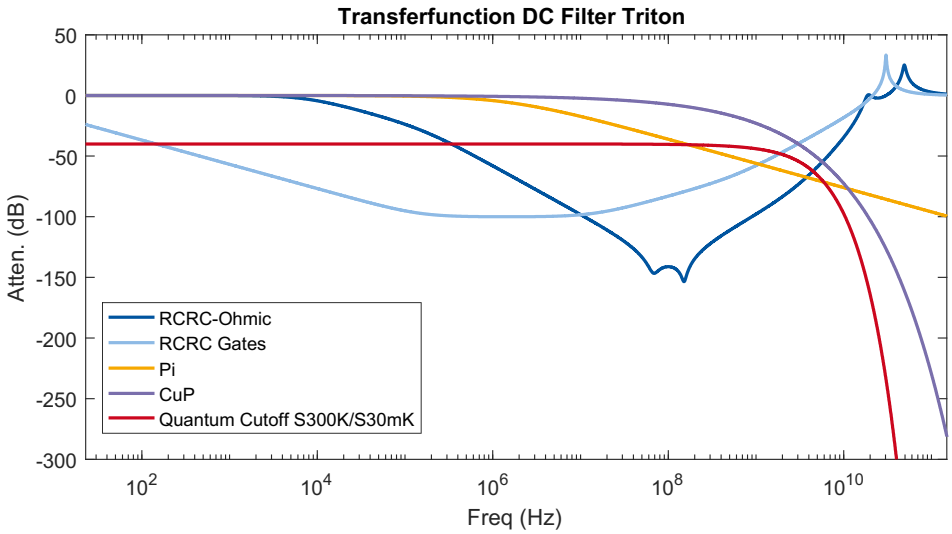

Figure 4.3.: Simulated power-transfer functions for two-stage RC filters (including LC parasitics) with 1 kHz "ohmic" and 1 Hz "gates" cut-off' filters (based on device specifications), "CuP" metal-powder (e.g., Cu) filters with 500 MHz exponential cut-off target for optimal attenuation and combined simulated effect of all filters.

nectors and two 24-line two-stage RC filters with electrically insulated chambers to reduce parasitics and crosstalk from one filter stage to the next. All interfaces have grooves to minimize the penetration of evanescent fields. Details on the chosen materials, circuit elements, PCB design, fabrication, detailed technical specifications for graphene experiments, and tested PCB design options can be found in [54].

Filter Box Evaluation Result

The transmission characteristic of the filter box shown in Figure 4.5 exceeds the required quantum cut-off,MHz. Up to 5 GHz, the characteristic curve is below the required cut-off frequency. The necessary attenuation below 70 MHz is achieved outside the filter box at the breakout box. The gigahertz-range transmission dominated by the dissipative filter requires further evaluation: In the 3-20 GHz interval, it resembles the qualitative behavior of the modules in [51] with resonances up to 50 dB (Figure 4.5), far above the VNA background

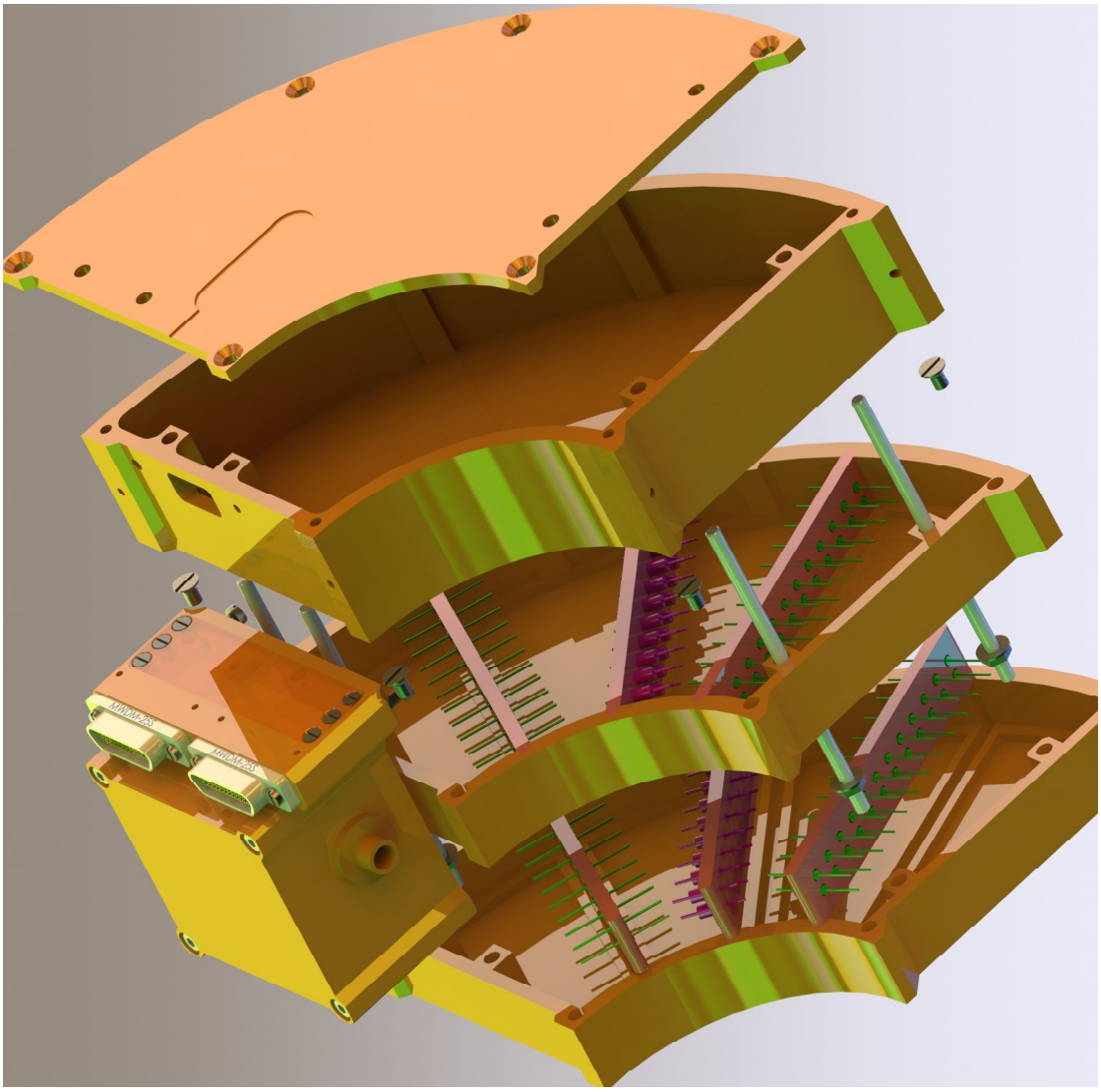

Figure 4.4.: 48-line filter-box Module CAD 3D drawing (without wiring): From top to bottom - copper-powder filter lid, a 48-line box with feedthrough (filter PCBs not shown), 2x 24-line RC-filter boxes with glued-in feedthrough lumped elements; Left - input isolation box with CINCH connectors, output isolation box with copper rod connector.

noise level and the levels required for ideal thermalization. Transmission above 10 GHz is done in the same order as capacitively coupled SMA cables with face-to-face male connectors at a pin spacing of 1 mm. Mueller [51] introduced large quantities of iron-containing Eccosorb to reduce the resonances. This is

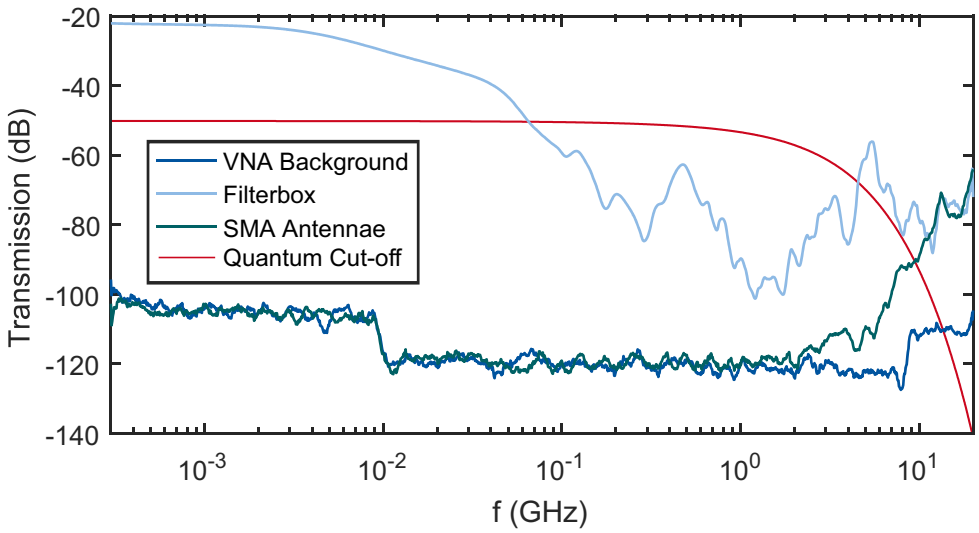

Figure 4.5.: Transfer functions of the full CuP-RC-filter-box, two non-terminated SMA cables for capacitively coupled SMA cables with face-to-face male connectors at a pin spacing of 1 mm and vector-network-analyzer background. The filter box shows high-order attenuation and resonances in the GHz band, comparable to [51] versions with the same powder composition (and without Eccosorb, which is not suitable for high magnetic fields), and capacitive coupling of SMA cables above 10 GHz. Over the entire measurement range, the signal exceeds the background level, so additional insulation is required to achieve a thermalization of 10 mK by understanding the limiting effects.

not compatible with the high magnetic fields of our experiments. Alternative measures must, therefore, be investigated.

Test Box Evaluation, Identification of Limiting Effects, Improvement Concept

To identify the origin of the resonances and the test measures that improve the filter performance, I designed a centimeter-size copper test box with two SMA connectors (center pins reaching a few millimeters into the device), a single cavity closed by two copper lids with grooves. This setup shows the best-case achievable isolation between two ports. The evaluation includes the worst-case reference where the transmission was measured without a lid (Figure 4.6 - "no lid"), resulting in significant crosstalk above 2 GHz exceeding 50 dB at 6 GHz.

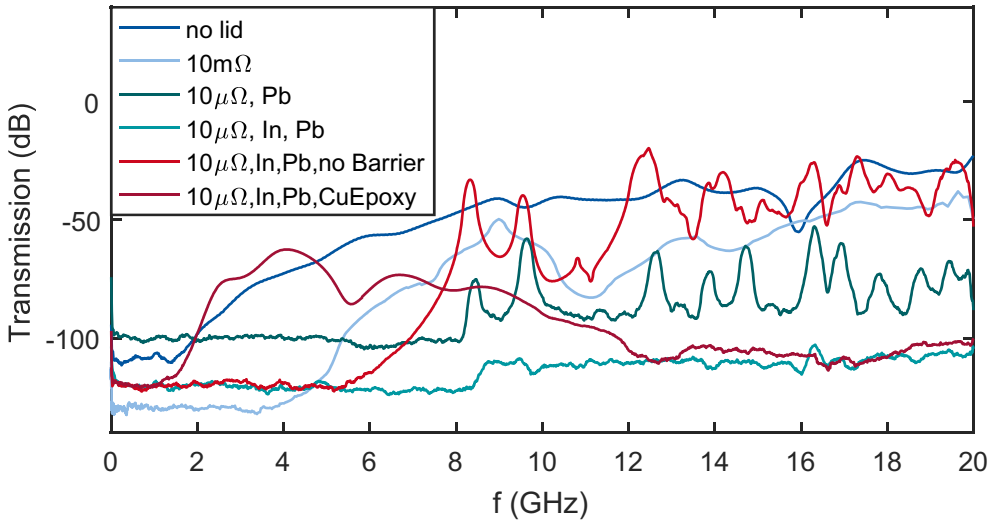

Figure 4.6.: Measures to ensure 20-GHz insulation: 'No lid' - Open copper box; '10mΩ' - Box with copper barrier and untreated lid; '10$\mu\Omega$, Pb' - Box with a copper barrier, polished lid, and soldered joints; $\mu\Omega$, In, Pb' - Box with a copper barrier, polished lid, soldered joints, indium-sealed lid; '10$\mu\Omega$, In, Pb, no barrier' - Box without copper barrier, polished lid, soldered joints, indium sealed lid; '10$\mu\Omega$, In, Pb, CuEpoxy' - Box without copper barrier, polished lid, soldered joints, indium-sealed lid, and filled with copper-powder epoxy.

The main improvements to create housing with sufficient shielding were:

- The introduction of two isolated chambers by closing the lid and dividing the cavity into two by a copper plate ('10$m\Omega$') improves the attenuation to below 50 dB (compared to 'no lid') with a significant transmission above 4 GHz while creating sharper resonances. This setup resembles the design properties of the filter box.

- Reduction of the contact resistance from lid to box to 10$\mu\Omega$ by mechanical polishing of one lid

- The closing of micron gaps of the interfaces by soldering results in an additional attenuation of up to 50 dB, revealing sharp resonances in the range of expected wavelengths of the box standing wave modes (Figure 4.6 '10$\mu\Omega$', '10$\mu\Omega$, Pb')

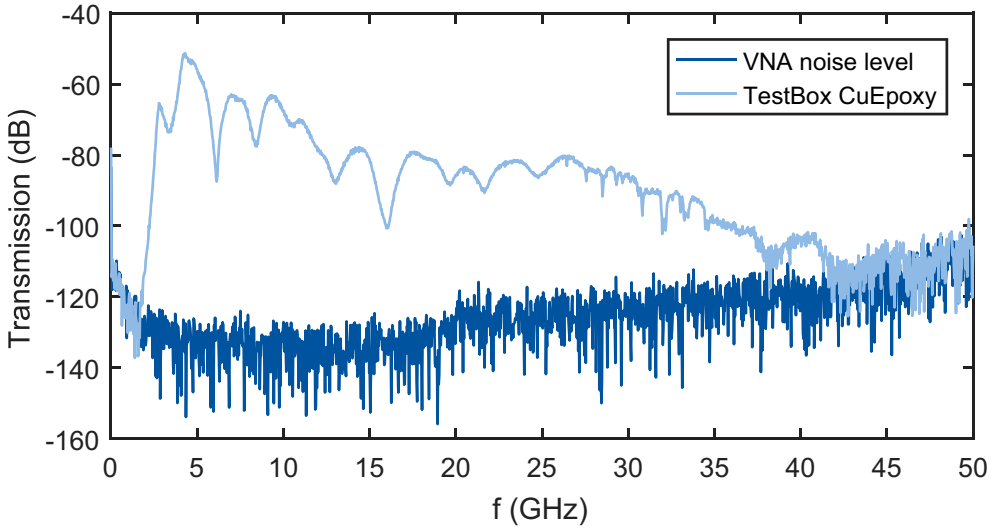

Figure 4.7.: Test box transfer function up to 50 GHz: The attenuation (without wiring) at 5 GHz is in the same range (55-60 dB) as for the Cu-powder box (including 1 m wire) and reaches -100 dB at 35 GHz limited by capacitive coupling (see Figure 4.6)

- The addition of an indium seal at the upper lid of the shielding of the two cavities achieves an attenuation greater than the VNA background at 120 dB over the entire measured spectrum (Figure 4.6 '10$\mu\Omega$, In, Pb').

Thus, only a low resistance and continuous contact along all interfaces reduce parasitic inductances to a sufficiently low level. The copper barrier was removed to characterize only the effect of the copper-powder resin compared to the insulated housing and uncured copper-powder epoxy was added. This increases the capacitive coupling in the 2-12-GHz interval, which is not critical for the quantum cut-offsults in resonance-free attenuation down to the measurement noise level. Thus, the copper powder-epoxy mixture alone with optimized shielding is sufficient for thermalization compared to the quantum cutoff cut-off10 GHz currently limited by the noise limit of the setup. After curing the resin, I characterized the optimized test box with the copper-powder epoxy up to 50 GHz (Figure 4.7). Attenuation is reduced from 2 to 12 GHz similar to the antennae in figure 4.5 likely due to the increased capacitance of the copper powder particles. The cured resin shows a minimal attenuation of ap-

prox. 50 dB at 5 GHz and reaches the frequency-dependent measurement noise levels of 100 dB at 35 GHz and 120 dB at 42 GHz. These steps towards the best achievable performance of the 2-port prototype, focusing on the attenuation of the filter with pure capacitive coupling (without connecting line), show a clear approach to produce an improved version of the filter box with our workshop.

4.4. Cryogenic Microwave Small-Scale Integration Platform

The interface between the cryostat sample holder, DC-wiring, AC coaxial lines on one side, and the device under test on the other is conventionally bridged by printed circuit boards (PCBs). Closely resembling their larger counterparts – graphics cards and motherboards – they support the quantum chip mechanically, anchor it thermally, and connect it electrically. They are designed and manufactured for a sample design to ensure proper line routing and impedance-matching for high bandwidth control and measurement. Future quantum computer architectures based on semiconductor spin qubits will depend on directing coherent microwave or complex pulse train signals to single qubits among millions. Signal distortions or crosstalk to unaddressed qubits lead to systematic gate errors that are difficult to determine and correct experimentally [55]. In the worst case of long-range crosstalk, which spreads over many qubits, a significant qubit overhead is required to correct errors. By creating a platform with high bandwidth and low crosstalk, the problem is solved at its source.

Furthermore, the introduction of a silicon interposer makes the first step from the conventional solution of routing signals from racks with room-temperature cabinet size over mm^2 footprint per coaxial line, which is limited by thermal stress and unrealistic footprints for even mid-size integration, to a scalable architecture. The integration of chip-size control electronics (like cryogenic voltage-controlled oscillators [56]) and quantum chips in one cryogenic environment, or even on one chip, medium to large integrated systems could be the next steps toward larger-scale integration [57, 58]. This step can be re-

alized by reducing the pad size of the interconnects (currently around 100 μm by an order of magnitude with existing scientific solutions [59]).

The following sections will develop the concept of the multilayer interposer and its most important functional parts (microwave-bandwidth coplanar waveguides, crosstalk-mitigating microstrip lines) and revise the group efforts in interposer fabrication. This microstrip creates a low-pass filter, which dissipates energy at high frequencies, thereby reducing the transmitted power. Improvements to the bandwidth of the integrated PCB interposer platform by removing parasitic inductance from bond wires, paving the way to coherent spin control up to magnetic fields of 1 T, and a proof-of-principle experiment on the crosstalk mitigation by microstrip lines conclude the discussion.

Concept for a Versatile, Low-crosstalk, Microwave-bandwidth Platform

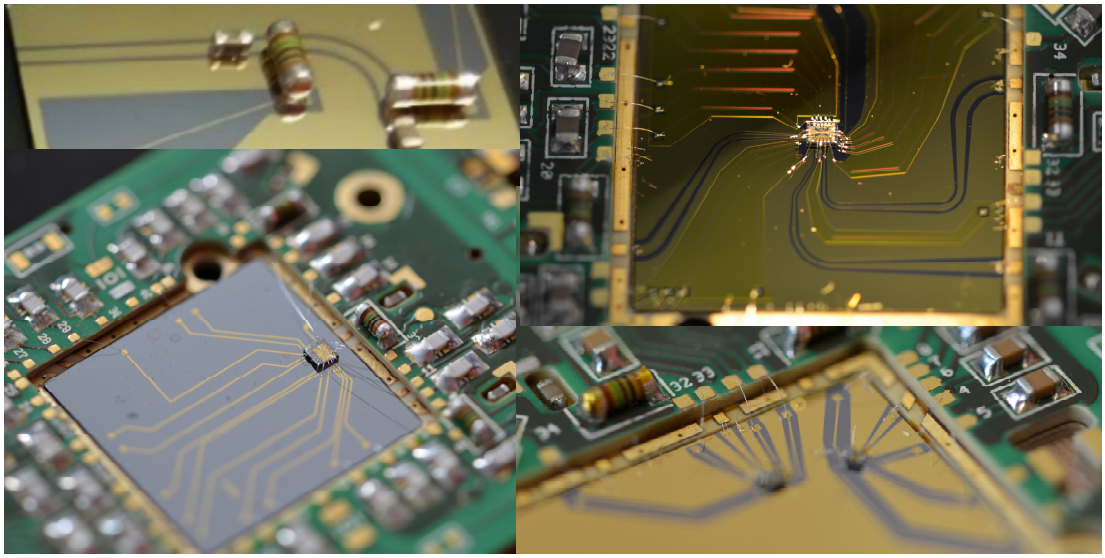

Figure 4.8.: Silicon-based microwave-bandwidth cryogenic integration platform: PCB-interposer implementations for a variety of experiments in our group – surface-mounted circuit elements on interposers for microwave bandwidth (e.g., bias tees), single-layer DC interposer for pre-characterization, multi-layer DC-AC interposer for EDSR qubit control and crosstalk reduction, single-layer interposer for microwave characterization of a voltage-controlled oscillator of 30 GHz.

Newer double quantum dot samples require less than 20 contacts, while future ones with multi-dot and bus systems will yield a number in the order of one hundred within the next five years. The high-bandwidth readout by radio-frequency reflectometry requires lines with minimal parasitic capacitance to ground to ensure correct impedance-matching and the right resonance frequency of the tank circuit. Furthermore, EDSR control in silicon requires a bandwidth of 20 GHz for typical fields of 0.5-1 T. Recent spectroscopic experiments at gigahertz frequencies show pronounced resonances that reduce the working range of the magnetic field [60]. The platform should provide surface-mount-device (SMD) compatibility for LCR elements of the low-pass filter, tank circuit, and bias tee elements.

A compact and high-bandwidth solution is multi-layer PCBs, which enable 3D-routing of lines [61]. These are specifically developed for a single-contact assignment (e.g., bias-tee microwave lines, DC lines, RF readout lines to sample pads) of similar sample types. The design and production of these prototype boards took my predecessor several months to reach an annual scale if process engineering and development were required. The introduction of a silicon interposer with all-optical lithography using commercially available plastic foil masks and 4-inch wafer production enables adapt these high-frequency sample holders to new samples on a week scale, creating flexibility in sample material and contact assignment, i.e., sample type, and opens up new ways to improve bandwidth (e.g., shortening or even removal of high-impedance bond wires by sample-specific design/flip-chip bonding or moving circuit elements in microwave lines very close to the sample). An exemplary layout can be viewed in Figure 4.9.

The PCB was designed by Jan Bussmann (v1), updated by Arne Hollmann (v2), and produced by Contag AG. It fits the pre-characterization 1K-setup "Bertha" and all cryogen-free mK-setups. It supports 8 microwave lines, 2 lines for RF readout, 40 DC lines, and SMD element ports for resistors and capacitors of bias tees, capacitors of all DC-line low-pass filters and inductances, resistors for the RF-readout lines as well as 3 pins for a laser diode (Figure 4.9). The layer stack contains one layer for microwave lines, located in the plane of the interposer surface to enable high-bandwidth-compatible short-wire bonds.

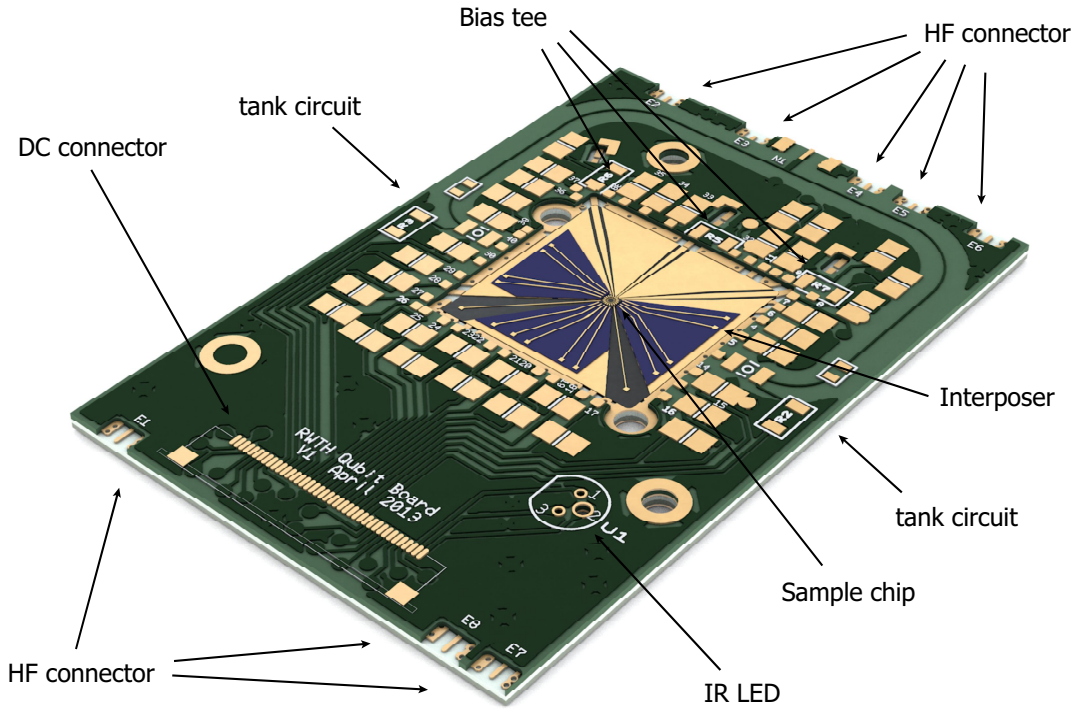

Figure 4.9.: The PCB-IP platform functional Layout of [62] designed in the [63] HF connector for EDSR/ESR experiments, DC connector for dot tuning lines and ohmics, tank circuit for RF readout, bias tee for DC+HF mixing, interposer for line routing, PCB-recycling, and bandwidth improvement.

This plane is shielded on both sides by ground planes and followed by two DC planes locally connected by vias. This enables the integration of SMD elements on the surface and 3D routing. Below the bottom DC plane, a ground plane is attached to the refrigerator for thermal anchoring. The detailed layer stack is shown in Figure 4.10. The low-power-dissipation ($\delta < 0.003$), high- and frequency-independent dielectric constant ($\epsilon_r = 4.55$) material Rogers was chosen for microwave bandwidth compatibility. Further details of the design for high bandwidths (T-junction shaping, via-fencing) are described in [63].

The silicon interposer proposed in [29] offers low-impedance microstrip DC lines for standing-wave resonance damping, crosstalk reduction from microwave to DC-lines, microwave control lines in coplanar waveguide layout up to the sample (10-micron fabrication resolution) to minimize the wire-bond

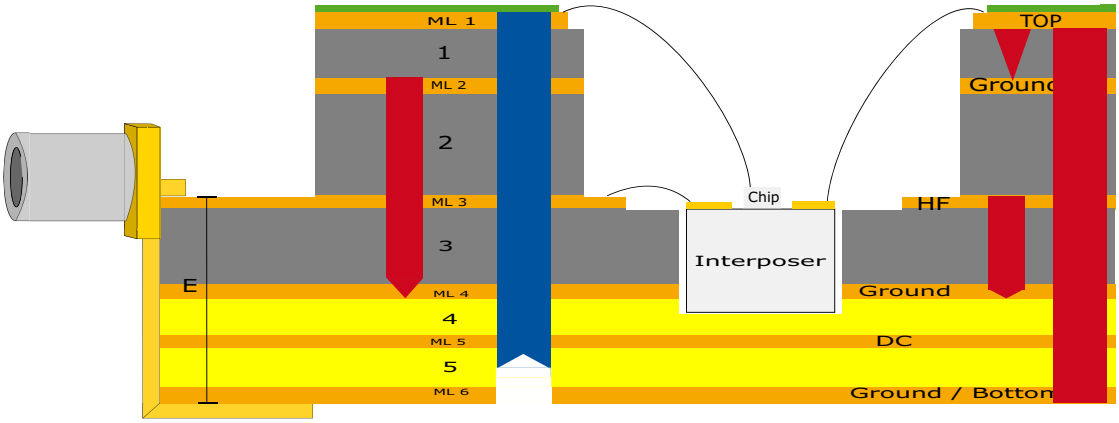

Figure 4.10.: Multilayer PCB layer stack. HF lines in plane with sample for improved bandwidth, multilayer DC for 40 connections, and RC-filter elements in sample vicinity, small footprint high-bandwidth RF connectors (left); Gray - Rogers HF dielectric; Yellow - Standard FR-4 dielectric; Orange - Conductive planes; Blue and red - Vias connecting the layers [63].

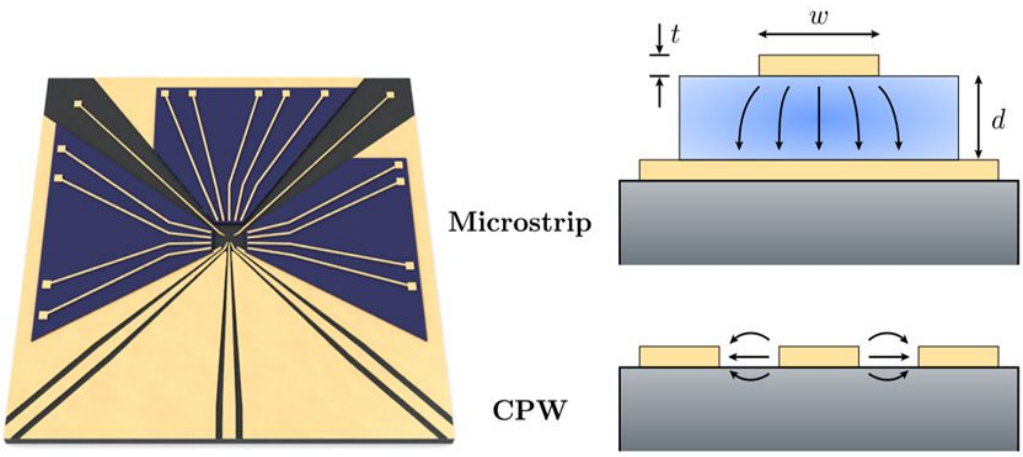

Figure 4.11.: Interposer with coplanar waveguides and microstrip lines: Left - Example of a layout with three CPW lines on the bottom side, two low-capacitance striplines for RF readout in the upper corners, and crosstalk-mitigating microstrips for the remaining DC-gates; Right - Layer stack of high-resistance silicon bulk (gray), gold (yellow) ground, and CPW plane, dielectric (blue), and microstrip plane gold (yellow).

length and the possibility for flip-chip interconnects by electroplated contact pads ($<$ 100-micron pitch) and thermocompression bonding. The layer stack of CPW and a ground-plane metal layer, the dielectric layer, and the microstrip metal layer, as well as a layout example, is shown in Figure 4.11.

The design of the CPW ensures a 50-Ω line-impedance matching by using CPW on isolator capacitance models from Simons [64] to determine the correct ratio of signal line width to gap and geometry variations (tapering, curvature) in the order of wavelength. The design, modeling, and implementation of microstrips for crosstalk reduction are discussed in the following subsections.

Physical Model for Interposer Microstrip Lines and Validation Experiment Design

The crosstalk between the low- and high-frequency lines results from capacitive coupling along the signal path. A significant part of this cross-coupling capacitance comes from the sample and interposer, where the lines are close and unshielded. Adding a shunt capacitance to ground the DC strip lines (C_{SL}) creates a capacitive voltage divider that reduces the voltage at the dot site V_{dot} by $C_{CC}/(C_{SL} + C_{CC})$, which is limited by resonances with parasitic inductances (e.g., of bond wires L_{chip}) or standing wave resonances due to reflections caused by impedance mismatch at the microstrip line ends). An analytical model, which describes the effects of the lumped elements and takes into account the phase variations along the stripline, was developed and implemented in Matlab by [29] and updated for changed material parameters in [62]. It is based on the ABCD-Matrix formalism, which models complex current and voltage signals in a two-port (input, output) network [65]:

$$\begin{pmatrix} V_{in} \\ I_{in} \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} V_{out} \\ I_{out} \end{pmatrix} \tag{4.2}$$

The original microstrip on the interposer model (Figure 4.12 Model a) includes the microstrip, which is characterized by specific resistance, length, cross-section, and capacitance per unit-length, bond wires to the PCB and sam-

ple, modeled by inductances, cross-coupling capacitance to sample, and PCB DC input, modeled by a high-impedance boundary condition. This model is insufficient to validate the assumptions and determine the crosstalk reduction in an experiment with direct transmission-type measurements through the stripline because the influence of the microstrip was not significant. This is due to the lack of high-impedance, high-frequency probes. A new method was developed by measuring the transmission of a CPW line that is restively coupled to the microstrip via a bond wire to access the effect with the 50 Ω probes. This circuit model is depicted in Figure 4.12 b). The microstrip generates a capacitive shunt that dissipates energy at high frequencies, thus reducing the transmitted power. At high frequencies, the increasing impedance of the inductance limits the attenuation.

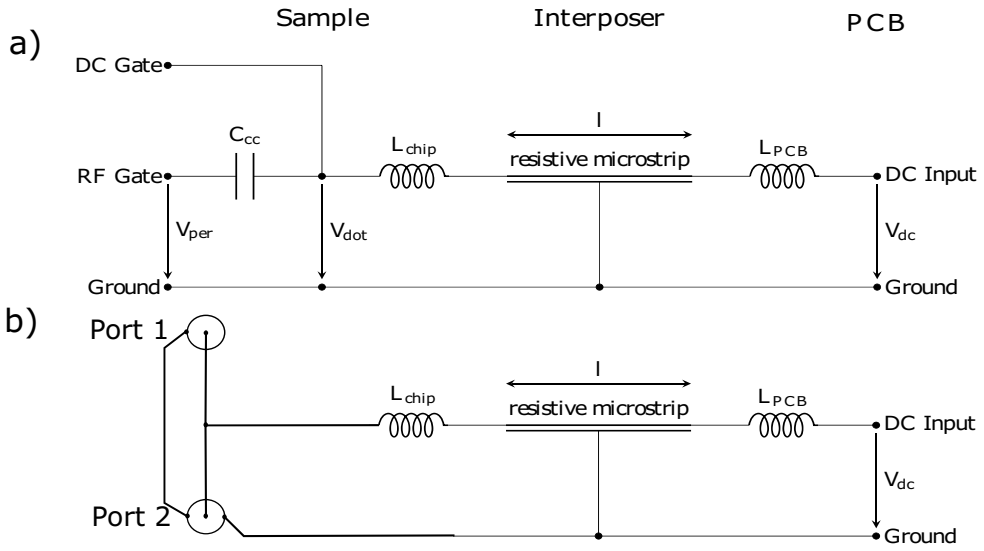

Figure 4.12.: Interposer with coplanar waveguides and microstrip lines: (a) Circuit model for sample microstrip PCB system, figure adapted from Neumann [62], (b) Circuit model for proof-of-principle transmission measurement for crosstalk reduction by microstrips.

Quantifying Crosstalk Suppression in Microstrip Proof-of-principle Experiments and Validation of the Microstrip Model

This paragraph motivates the design of an experiment using the 50 Ω probes to validate model b) and measure the characteristic values of the interposer chip instead of a direct measurement of the crosstalk reduction, which would require a high impedance high-frequency probe. These characteristic values enable estimates of the crosstalk reduction within the microstrips. The simulation in Figure 4.13 suggests an attenuation of more than 10 dB at approx. 500 MHz based on direct measurements of the stripline conductance ($1.03 \cdot 10^8 S/m$), the capacitance (70 pF), and a geometric estimate of 1 nH for the inductance. Furthermore, the influence of the microstrip can be clearly distinguished in the model from a stripline without ground and its standing wave resonance at a few gigahertz (Figure 4.13). This stripline resonance is an artifact of the 50 *Ohm* stripline in line of the measurement not existent in the signal line of the DC lines in the experiment. This measurement method validates the microstrip model and estimates the crosstalk reduction in the experiment.

The measurement and simulation of the crosstalk reduction of a microstrip line based on the same experimental parameters as the validation interposer is shown in Figure 4.14. In an unfiltered stripline (a metal strip on the substrate without an additional ground plane and width of the microstrip), due to the impedance mismatches at the bond wire, pronounced resonances occur above two gigahertz corresponding to standing waves at the interposer. In addition to the model prediction, the sample-IP bond wire and unknown parasitic capacitance create a resonance at 16 GHz ('Microstrip 100nm, wire-bonded 1 nH'), which is damped by the standing wave resonances on this 9.6-cm line. Microstrip lines with the same parameters as in the validation experiments attenuate 30 dB for low frequencies. This can be further improved by increasing the microstrip capacitance (low capacitance - 'Microstrip 450 nm' and increased capacitance - 'Microstrip 100 nm'). Standing wave resonances are damped as expected. The mentioned LC resonance can be shifted by two orders of magnitude if the wire bond is replaced with a flip-chip interconnect: [66] report 25 pH

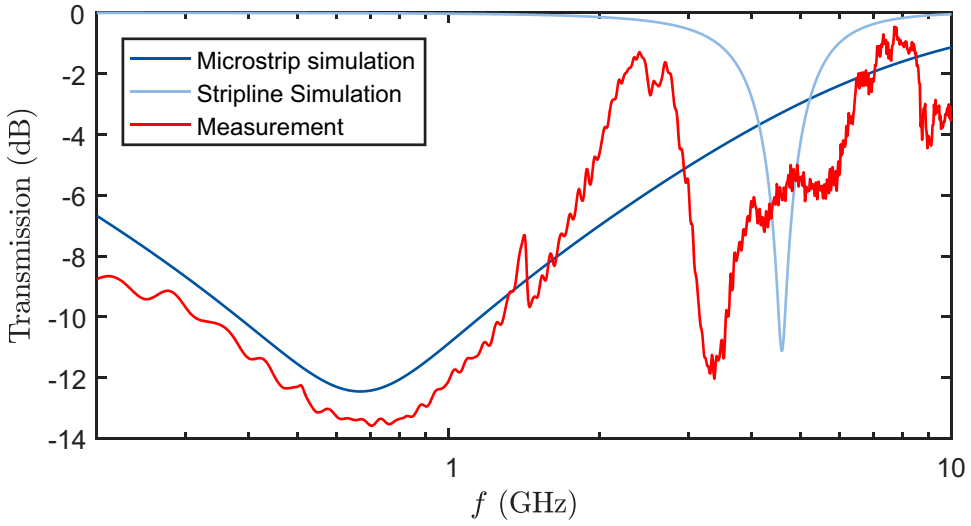

Figure 4.13.: Microstrip validation and proof-of-principle experiment: Comparison of simulated and experimental transmission of an interposer CPW bonded to a microstrip line. Simulation is based on the measured resistance and capacitance of the microstrip and geometric estimation of the bond-wire impedance.

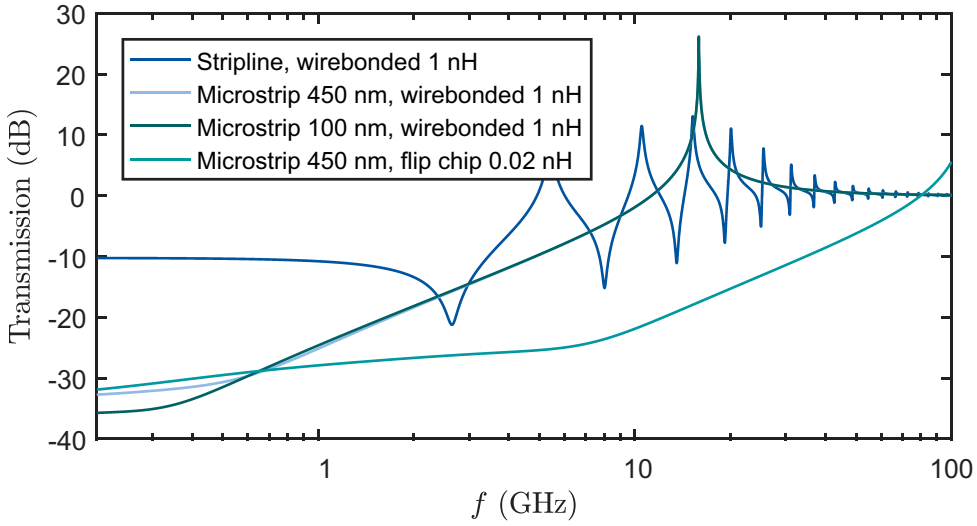

Figure 4.14.: Crosstalk reduction by microstrip: Simulated estimation of an interposer crosstalk and resonance reduction for the same parameters as the validation interposer (resist thickness 100 nm, 450 nm) and different interconnect technologies (i.e., different inductance)

inductances for 50-μm copper pillars ('Microstrip 450 nm, flip chip 0.02 nH'. Flip-chip tests at our institute by Sebastian Kindel and Foos [59, 67], using galvanically grown gold pads on the interposer and thermocompression bonding, showed mechanical stability and less than 2 Ω contact resistance at 4 K. The resulting crosstalk and resonance attenuation would exceed 25 dB up to 10 GHz compared to 15 dB amplification with the conventional stripline technique as our validated simulations in Figure 4.14 show.

Achieving Microwave Bandwidth with the Integration Platform

In order to increase the control power at the sample and to reduce the power dissipation, the signal transmission of the integration platform must be compared and improved with current solutions at the institute. Signal transmission in the high-frequency signal lines of the integration platform is impeded by reflections due to impedance mismatching or dissipation (e.g., via dielectric loss) on the way to the sample. The main sources of impedance mismatch on the PCB are sudden changes in the waveguide geometry. On our multilayer PCB, these are the SMPM connectors (geometry change: connector CPW to PCB-grounded CPW), bias tee (PCB-grounded CPW to DC via), and PCB-IP interface (PCB-grounded CPW to PCB CPW, PCB CPW to IP-CPW bond wire).

Measurements in the time domain reflectometry (TDR) reveal the mismatch position (determined from signal propagation time and dielectric constant) and the size of impedance mismatch:

- 10-15 Ω surplus on SMPM connectors varies with solder quantity
- 23-Ω insufficiency at the PCB bias tee, 10-12 Ω surplus at the PCB-IP Interface

Expected reflection coefficients are significant with $\Gamma = (Z_0 - Z_1)/(Z_0 + Z_1)$ in the range of 20-30% for each mismatch. A signal transmitted through the three mismatches accumulates a reflection of 55% up to the first order, resulting in an attenuation of two orders of magnitude, assuming a Fabry-Perot-type

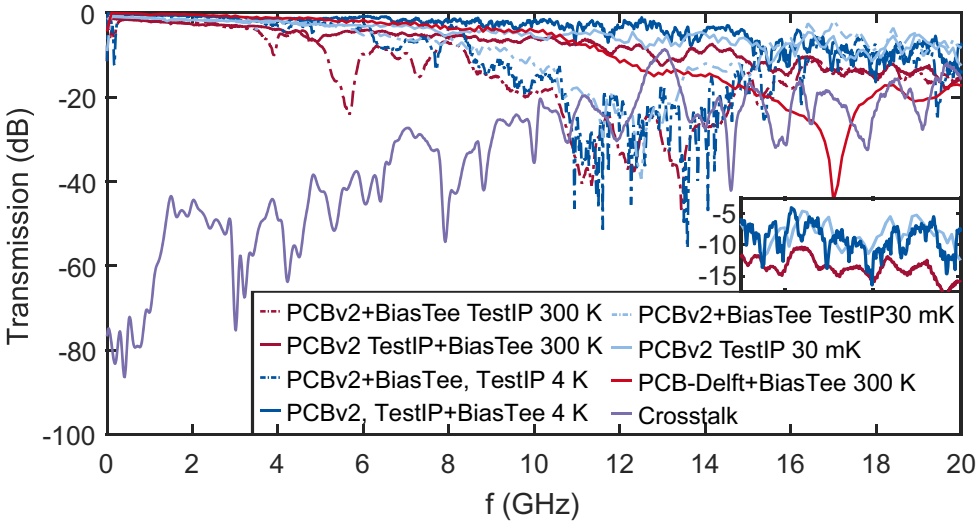

Figure 4.15.: Cryogenic Integration Platform Transmission: Transfer function for CPW paths - PCB-wirebond-Interposer-wirebond-PCB - at room temperature, 4 K, 30 mK with Bias Tee at PCB, IP and without Bias Tee (corrected for setup attenuation) and conventional PCB only platform path - PCB-wire-bond-PCB. The impedance mismatch on the PCBv2 Bias Tee line induces resonances, reducing the transmission by up to five orders of magnitude in the EDSR relevant 10-15 GHz band. Inset: Lines with/without Bias Tee on the IP yield less than 17 dB attenuation at room temperature and less than 12 dB at 30 mK outperforming the conventional PCB-only design.

resonance $P_t/P_i = 20\log(1-4\gamma/(1+\gamma)^2$. This assessment shows the need to improve the integration platform further. This hypothesis is confirmed by transmission measurements, which show resonances in the 10-15 GHz band with up to five orders of magnitude unintentional attenuation in Figure 4.15. These resonances only occur for lines with bias tees on the PCB. The resonance frequency correlates with the different path lengths between the mismatches on the PCB, which further supports the allocation of the mismatch.

Subsequent improvements significantly reduced the excess impedance:

- Placement of three flat bond wires or silver epoxy on each contact of the PCB-IP-CPW interface, which reduces the inductance and thus the mismatch to 7-9Ω Comment: Silver epoxy should not be used for the interposers used at cryogenic temperatures as different thermal expansion

coefficients of PCB and IP lead to cracks and chipping.

- The excess connector impedance can be reduced to 5-8 Ω by a thick solder blob on the inner conductor, which changes the CPW gap and thus increases the capacitance.

These improvements resulted in an overall attenuation of 15-17 dB over the entire PCB-IP-PCB setup (without bias tee) – shown in Figure 4.15 – on par with a conventional PCB-only solution at room temperature.
At cryogenic temperatures, the attenuation is 12-15 dB due to the reduced dielectric loss in the high-resistivity silicon [68]. The PCB-IP platform exceeds the PCB-only performance at millikelvin temperatures by at least a factor of 2. This is due to the temperature-independent dielectric loss of the PCB-only solution.
Bias tee attenuation performance has been improved by more than four orders of magnitude in the 10-14 GHz by fabricating interposers with SMD pads and bonding the circuit elements with silver epoxy resin [67]. The results of the fabrication, measurements at room temperature, and four Kelvin using Jacob Foos are shown in Figure 4.15. The magnitude of the crosstalk between microwave lines on the PCB and the interposer as an indicator of systematic gate errors due to residual Rabi drive is shown in Figure 4.15. As in [61], the crosstalk signal is reduced by only one to three orders of magnitude in the gigahertz band.

High-throughput Robust Interposer Microfabrication

The interposer should be a commodity that can be built quickly and does not delay the quantum experiments due to design and fabrication times or problems arising from process complexity. Therefore, the proposed fabrication process is based on commercially available high-resolution (3k-12kdpi) foil masks (days/week production time) and standard optical lithography. Interposer production on a wafer-scale 2 cm x 2 cm at the Central Laboratory for Micro- and Nanotechnology (CNMT) improves throughput. In our undoped silicon quantum chips, the failure of individual lines leads to the rejection of

the whole sample since each line is critical for dot tuning. The necessary implementation step, therefore, is the choice of dielectric and the development of a process that produces isolating layers that meet the requirements – withstanding experimental conditions, the achievement of desired electric properties for crosstalk reduction, and electrical insulation as discussed by [62, 69]: structurable by optical lithography, thin, high breakdown voltage (compared to experimentally used voltages -2 to 4V), low price, material and process parameters available and allowed in our institute clean rooms (central laboratory and Institute II clean room). Additionally, bonding to spin-on resists and cryo cycle stability proved to be complicated. The former can be handled by removing the dielectric underneath the bond pads and using positive-process optical lithography, which prevents resist undercuts and associated line tearing. Additionally, shorts between microstrip lines and the ground layer occurred at room temperature and increased in number after several cryo cycles for the proposed polyimide resist. An overview of the materials taken into consideration and investigated by [29, 38, 62, 69] (in chronological order) is listed as follows:

1. HSQ (hydrogen silsesquioxane)
    - High processing complexity and time – can only be structured by electron-beam lithography
2. LTC 9505 (polyimide)
    - Low process complexity (optical lithography)
    - Moisture-sensitive adhesive properties
    - Ageing effects and reproducibility problems as the layer thickness is strongly dependent on the solvent concentration
    - Cryocycle-induced insulation breakdowns
    - 100-mm wafer production is not possible due to adhesion problems (insufficient improvements with adhesion promoters bis(trimethylsilyl)amine (HDMS) or organosilane (VM651))
3. Aluminum oxide (Al_2O_3)

- High breakthrough voltage
- nm layer thickness
- High permittivity (8-10 [70])
- High processing complexity and time (nm/hour) of atomic layer deposition method
- Insulation breakdown (<100Ω) due to occasional pinholes for thicknesses of 40-50 nm limited by process engineering

4. SU-8 (bisphenol-A-novolac epoxy)
   - Low process complexity (optical lithography)
   - Frequent insulation breakdowns at 400 nm incidence with bubbles in the resist
5. Parylene C (Poly(P-xylylene) polymer)
   - Low insulation breakdown rate
   - Cannot be structured by optical lithography – additional photolithography and etching step required
   - cryo cycle-induced insulation breakdowns (tested up to a resist thickness of 700 nm)
6. Aluminum oxide (Al_2O_3 60 nm) + SU-8 (bisphenol-A-novolac epoxy 400 nm)
   - Insulation breakdowns 400 nm incident with bubbles in the resist
7. Aluminum oxide (Al_2O_3 60 nm) + Parylene C (Poly(P-Xylylene) polymer 250 nm)
   - Low insulation breakdown rate
   - Cannot be structured by optical lithography – additional photolithography and etching step required
   - Room-temperature insulation resistances in the order of 100 MOhm, no failures at 81x 1x1mm^2 intersections

- no cryo cycle insulation breakdowns after five cycles in liquid nitrogen

In summary, reliable microstrip insulation is currently limited by the technical implementation of faultless homogeneous dielectric deposition. This makes strip lines without microstrips the main choice for experiments with relaxed requirements on crosstalk. Thoroughly tested (multiple cryo cycles) microstrip interposers are in use for complex experiments (T1 measurements) described later. Possible sources are adhesion problems, bubbles in resist (bubble formation during spin-on and baking), fissures caused by thermal stress of spin-on resists, and imperfections in the aluminum oxide grown by ALD. The only combination of dielectrics that achieved sufficient quality was aluminum oxide with Parylene C, which, after five cooling cycles to liquid nitrogen temperatures, showed no failures from 81-millimeter-sized contact areas. This process is sufficient for the future production of prototype interposers suitable for experiments on quantum dots and qubits and for testing the performance of microstrip and microwave lines.

Conclusion

In conclusion, we have designed, produced, characterized, and improved a small- to medium-scale integration platform suitable for various electron-spin quantum computing platforms in GaAs and Si, for microwave control, and DC or RF readout of S-T0 or single-spin qubits and quantum buses, which meet the requirements on bandwidth, flexibility, and fast, cheap production. The main improvements in bandwidth were the bias tee on the interposer solution, which improves the attenuation by four orders of magnitude, and several optimizations at the critical interfaces, resulting in a 12-dB attenuation between two inputs of the PCB-IP platform at 20 GHz, achieving a bandwidth comparable to PCB-only solutions.

In addition, the microstrips remove standing wave resonances in the simulation based on experimental parameters and attenuate any crosstalk signal up to 10 GHz. In the next step, the performance of experiments needs to be validated. Finally, the technically feasible introduction of flip-chip bonding would

solve the problem of parasitic-capacitance bond wire resonance, which would result in a slowly increasing transfer function with up to four orders of magnitude improvement in crosstalk and standing wave resonance damping over the stripline interposer solution. Compared to a PCB-only solution, the microstrip interposer achieves an additional crosstalk reduction of 25 dB up to 10 GHz.

4.5. Control and Measurement Setup

Amplifier Evaluation for Spin Readout in Silicon

Experiments in quantum-dot systems mainly use two types of measurements: direct transport through the quantum-dot system and charge-sensing of the electron occupation of the quantum-dot system by a nearby current through a quantum point contact or quantum dot. Direct transport measurements are used in our system to test the functionality of the sample structures like gates and ohmics. In early measurements, the resistance of the sample is given by the ohmic contact resistance, limited by the implantation quality, in the order of a few kilohms. The resistances can reach more than a gigaohm with few electron-dot occupations and opaque barriers. Apart from the runtime of the experiment, there is no limitation in the timescale of a measurement. To determine the single electron occupation and spin readout, the QPC or quantum-dot sensors have resistances in the range 10-100 $k\Omega$, depending on the chosen resonance peak and the working point on the peak. For 100 μV to 1 mV biases, currents are measured in the nanoampere regime. Depending on the dot-sensor distance and the sensor's sensitivity, typical charge-sensing signals are in the range of 1-5 pA [31] for our designs in silicon. The limiting timescale for the final spin readout is the relaxation time T_1, which ranges from less than milliseconds to seconds, depending on the magnetic field working point [26]. If one avoids the relaxation hot spot, T1 of 100 ms, and more are realistic at magnetic fields where EDSR control is still possible.

The choice of the correct measurement setup, including a suitable amplifier stage, should be tailored to these experimental limitations.

demonstrated high bandwidth measurements reaching readout times of microseconds citeSchoelkopf1998 and are used in our group for doped gallium arsenide samples [5]. They use a radio frequency setup resembling a lock-in amplifier with a cold, high-bandwidth preamplifier matched to the charge sensor's impedance by an LC-tank circuit. Low parasitic capacitances in the line after the amplifier and the correct choice of the SMD inductance ensure that the resonance frequency of the tank circuit is in the range of the circulator and

amplifier bandwidth (220-240 MHz), and, at the same time,, the impedance is matched so that the reflected signal is sensitive to the change in sensor resistance. Tim Botzem was able to reduce further the 0.3 pF of the coil and PCB and 0.4 pF of the bonding and sample design to achieve sufficient sensitivity with an 820 nH inductor [5]. For undoped designs with large top gates (partially defined by optical lithography), as we use them for silicon devices, the capacitance is at least 2 pF from the micron-sized optical top-gate pads alone, which provides the connection to the e-beam features. To achieve similar performance, a floating top-gate isolated by a 500 $k\Omega$ resistance (large enough to decouple, but small compared to leakage resistances), an e-beam-structured implantation (with the risk of even higher ohmic resistances) or a split top-gate (effectively reducing the parasitic capacitance to ground) could achieve a sufficient reduction of the parasitic capacitance. This effort could allow a significant bandwidth to increase close to the reported readout times of >100 kHz.

A sufficient and less complex implementation is the DC readout. This subsection discusses the evaluation of the correct setup choice, which achieves a charge readout at 10-kHz bandwidth and a spin readout at 1-kHz bandwidth, comparable to state-of-the-art experiments [71].

Noise sources in the setup are, as discussed earlier, the resistor Johnson noise, the shot noise of the sensor signal due to the quantization of electron charges, and the current and voltage noise generated by the amplifier. For better comparability, the data sheets provide a cumulative noise spectral density related to the input – the input related to voltage/current noise e_n or i_n. Commercially available operational amplifiers can be divided into three leading technologies that result in different noise performances at varying sample resistances: Bipolar, MOSFET (metal-oxide-semiconductor field-effect transistor), and JFET (junction field-effect transistor). Bipolar is suitable for applications with high currents and resistance and yield pA/$\sqrt{Hz}$ current noise densities – too high for pA signals. The noise values of commercially available JFET operational amplifiers are in the fA/$\sqrt{Hz}$ and nV/$\sqrt{Hz}$ range, see Figure 4.16. Compact MOSFET are comparable but suffer higher 1/f noise due to the small gate dimensions. Figure 4.16 presents the most promising candidates (all JFETs) from a market research study in 2016. Besides integrated operational

amplifiers, it also represents the input-related noise of IV-converter solutions home-built at our institute using the OPA627 and the commercially available Femto DLPCA-200, as well as the SP983 IV-Converter of the University Basel, using an IF3602 JFET in a self-developed operational amplifier.

What are the dominant noise sources in the measurement circuit? The shot noise density of the sensor ($S_e = 2eI$) on picoampere signals is in the below $fA/\sqrt{Hz}$ regime and is therefore negligible compared to the amplifier noise. The same applies to the sample resistance at millikelvin temperatures. The feedback resistor of mega- up to gigaohm does not generate voltage noise within the bandwidth of the operational amplifier since any differential signal at the non-inverting input is corrected concerning the inverting input. The Johnson current noise of the feedback resistor of 100 MΩ to 1 GΩ is 13-1.3 $fA/\sqrt{Hz}$ at room temperature, thus in the appropriate order. The chosen amplifiers all deliver a similar current noise but are all voltage-noise limited for the expected range of 100 kΩ (1 nV corresponding to 10 fA – Figure 4.16). If the feedback resistance is chosen correctly, the input noise of the DC amplifier is the limiting source of measurement noise in our setup.

A detailed description of the noise spectra of all operational amplifiers in Figure 4.16, including tests with different sample and feedback resistances, can be found in [72]. Although spread in the noise performance of individual transistors induced by the fabrication process is typical, the tested operational amplifiers did not show any Hero device with improvements relevant to the performance placement compared to other types. The best choice for the expected sample resistance is the Basel IV-Converter SP983 with the IF3602 JFET stage, see Figure 4.16.

In order to assess whether this choice of amplifier is appropriate for spin readout, a model by [73] can be used: We want to resolve a signal amplitude of pA compared to the RMS noise. The RMS noise is calculated from the spectral density times the measurement bandwidth. The current spectral density for the amplifier is $S_i = e_n^2 R_S^2 + i_n^2$; the bandwidth ranges from the measuring frequency given by the integration time up to the acquisition frequency. The integration time is limited by T1 (100 ms) and the corner frequency (where 1/f and white noise amplitude are equal, below 10 Hz for the SP983)

– longer integration times do not yield a better signal-to-noise ratio due to spin relaxation and signal correlations that prevent a reduction of the standard error of the mean measured value. The acquisition frequency is limited by the setup bandwidth (10 kHz in our setup) or the bandwidth of the amplifier ($f = GBWP/(1 + R_f/R_s)$ – the product of the gain bandwidth divided by the voltage gain of the amplifier, 68 MHz in the case of the SP983, resulting in 68-kHz bandwidth at 100 M IV-gain). The resulting expected signal amplitude relative to the RMS noise is shown in Figure 4.16. Within T_1, most amplifiers achieve significant signals with multiple standard deviations from the background. Shorter integration times are preferable to resolve the step features of the Elzerman readout scheme. By increasing the measurement bandwidth by a factor of 10, only the OPA627, DLPCA-200, and SP983 remain, by a factor of 100, only the SP983. For spin measurements with kHz bandwidth, the SP983 is therefore the only viable choice. The institute's standard IV converter with OPA627 was used for pre-characterization of the samples.

Besides the right choice of the amplifier, the correct configuration is also necessary: The high-gain bandwidth product of the amplifier allows sufficient bandwidth with 0.1-GΩ feedback resistance for a 100 kΩ sample. At both amplifications, the output is not saturated (+/-10 V) at nanoampere currents. The final characterization of the setup is presented in Chapter 5.

Software Setup

The control and measurement software used for the experiments in this thesis was "special measure" a Matlab package with a command-line interface developed by Hendrik Bluhm. DC control and acquisition for pre-characterization, charge readout, and tuning to the few-electron regime is realized by software-controlled decaDAC voltage steps and single measurement point acquisition by the DMM or buffered ramps and readout of the devices triggered by software or hardware triggers (in cases where jitter is critical). For this purpose, the drivers of the DMM have been updated. During the multiple sample tests, a semi-automated standard process flow script was developed for sample testing up to tunnel barrier tuning.

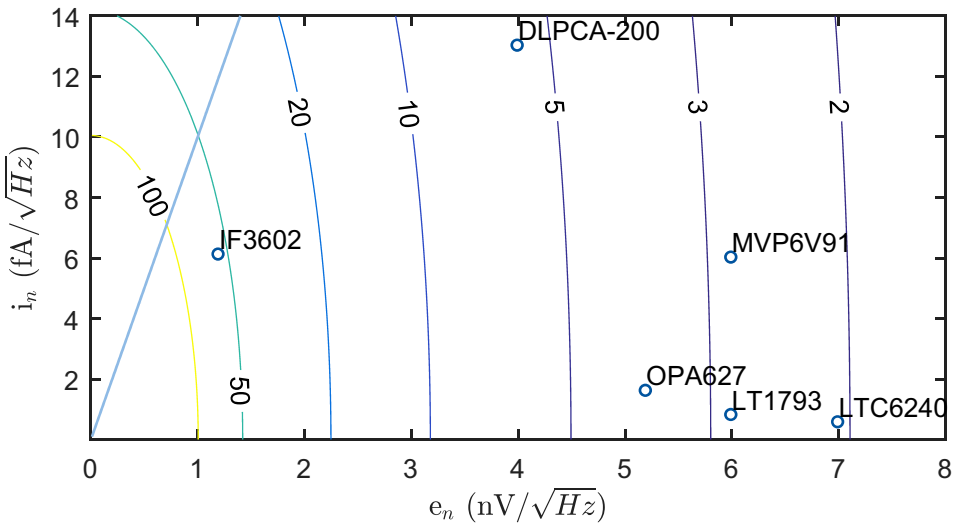

Figure 4.16.: The amplifier noise parameters and the resulting signal amplitude to RMS noise ratio: input-related current and voltage noise values for commercially available transistors (IF3602 used in the SP983 IV converter) and operational amplifiers (OPA627 used in home-built IV-converter, DLPCA-200 IV-converter from Femto), contour lines show the resulting signal amplitude-to-RMS-noise ratios for single-shot spin readout within 100-ms integration time for 100-kΩ sample resistance and 1-pA charge signal. The light-blue line indicates the optimal current-to-voltage noise ratio for a resistance of 100 kΩ.

For pulsed experiments and fast acquisition with the Alazar DAQ board, the qctoolkit Python package [74] with a Matlab interface written by Simon Humpohl was used, and scripts for tunnel-barrier tuning, Elzerman readout, and T1 measurements have been developed.

A data analysis package has been developed to support representation and reproducibility. It transforms the original data (e.g., by adding fine and coarse channels, rescaling, derivations or averages, updating the formatting for plots). It saves the normalized data together with the transformation parameters. The normalized data can then be used by analysis scripts and fed into a plotting routine with options for displaying experimental parameters and formatting for presentations or printing. Detailed descriptions of the developed packages and scripts follow with the respective experiments.

4.6. Cryostat Setups

Pre-characterization Setups

Devices with few contacts can be tested in probe stations that use movable measuring tips. More complex devices are wire-bonded to chip carriers and transferred to holders to apply voltage to many contacts simultaneously, thus testing many gates automatically.

For the pre-characterization of dots, mobile helium dewars with dipsticks for DC4 Kelvin is available. DC (48 lines) and high-frequency (6 lines) characterizations at cryogenic temperatures and magnetic fields of up to 6 T are available in the mobile dewar “Bertha”. The dipstick of the Bertha setup is large enough to accommodate the PCB-Interposer-Integration platform as an alternative to IC carriers. Unless otherwise specified, all pre-characterizations of the integration platform and the silicon quantum chips were performed in the Bertha setup.

30 mK low-frequency setup

The measurements on the doped silicon quantum dot R1940MV were performed in a Kelvinox wet-dilution refrigerator with a cold finger and filter design similar to the one used in [5], 6 T-magnet, and DC-only wiring. The cut-off frequency of the RC filters is 50 kHz ($R = 2\,k\Omega$, $C = 10\,nF$).

30 mK SHF setup

The "Kurt" setup is optimized to meet the challenges of silicon quantum computing in the coming years. It offers many high-frequency lines (8, with an option for an additional 6) and DC lines (96 in 4 looms). A highly stable magnet (<1ppm/hr) with 100 mm bore and 20 GHz bandwidth lines provides enough space, stability, and bandwidth for two-sample EDSR control in silicon-28. The option of a bottom loader could improve the throughput in the future.

The Triton 200 by Oxford Instruments plc delivers 3 µW of cooling power at 20 mK, 200 µW at 100 mK, and reaches 25-35 mK fully equipped in typical

experiments. For equipment sensitive to magnetic fields, such as circulators, a field cancellation coil on the mixing-chamber plate reduces the magnetic field to 100 Gauss for fields up to 7 T.

Thermal and electrical insulation is achieved by low-thermal-conductivity wiring – stainless steel boron and superconducting niobium-titanium high-frequency lines and phosphor-bronze DC lines, a breakout box with switchable voltage dividers, and RC filters (cut-off00 Hz see Appendix B) as well as pi-filters (cut-offMHz), a filter box with feedthrough resistors and capacitors in insulated chambers to reduce high-frequency resonances as shown in Figure 4.17.

Millikelvin temperatures are achieved in this dry-dilution refrigerator by a two-stage pulse-tube cooler. This helium pre-cooling line ensures sufficient heat exchange during cooling, and a He^3/He^4 circulation unit reaches the final base temperature. The pulse-tube coolers replace the liquid-nitrogen and helium baths and reach 4 K without moving parts at cryogenic temperatures, resulting in low vibration levels and a longer lifetime. [75]. It relies on the adiabatic expansion of helium gas and effective heat exchangers in the cold part of the pulse tube and the compression and cooling of an external heat exchanger. The technical implementation of the necessary pressure changes is carried out by a compressor with high- and low-pressure lines and a switching valve that operates cyclically between the two. To condense the helium mixture at 4 K, an additional compressor pump is added to the mixture cycle, which generates 3 bar pressure. The remaining parts resemble a wet mixing cryostat: Heat exchangers cool the incoming mixture in 0.7-K and 100-mK stages, which condenses in the mixing chamber. This reservoir is connected to a second reservoir, the "still" plate, at approx. 0.7 K, where the He^3 is pumped (distilled) from the mixing system. Heating the still to 0.7 K generates a high cooling power using a high evaporation rate, ensuring that the additional evaporation of He^4 does not limit the process.

The control and maintenance protocols developed in recent years can be found in Appendix B

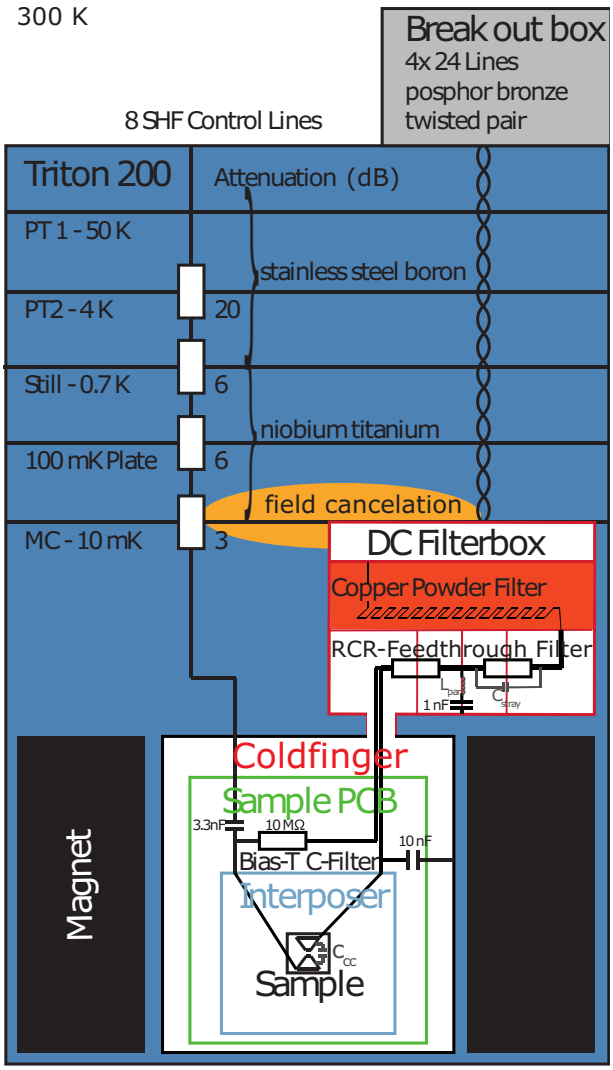

Figure 4.17.: Triton 200 "Kurt" - setup schematic: Wiring and filter concept for the dry refrigerator setup – DC wiring Pi-RC-filtered in the breakout box, 2-stage RC-filter, and metal-powder filter; the HF wiring includes 8 SHF control lines with superconducting niobium-titanium for below 1 K for thermal insulation; low-drift magnet for qubit control; two sample slots on the intermediate-scale integration platform with interposer and multilayer PCB. Detailed characteristics of the text are given in Appendix B

4.7. Dilution Refrigerator Setup "Kurt" Characterization

After discussing all design concepts, technology choices, and important parts of the system in the previous sections, we now examine the performance of the entire setup, gain an understanding of the most important technical noise contributions, and evaluate whether the setup is suitable for the control and measurements of spin qubits in scalable quantum chips. To simulate realistic conditions, the measurements were carried out at base temperature.

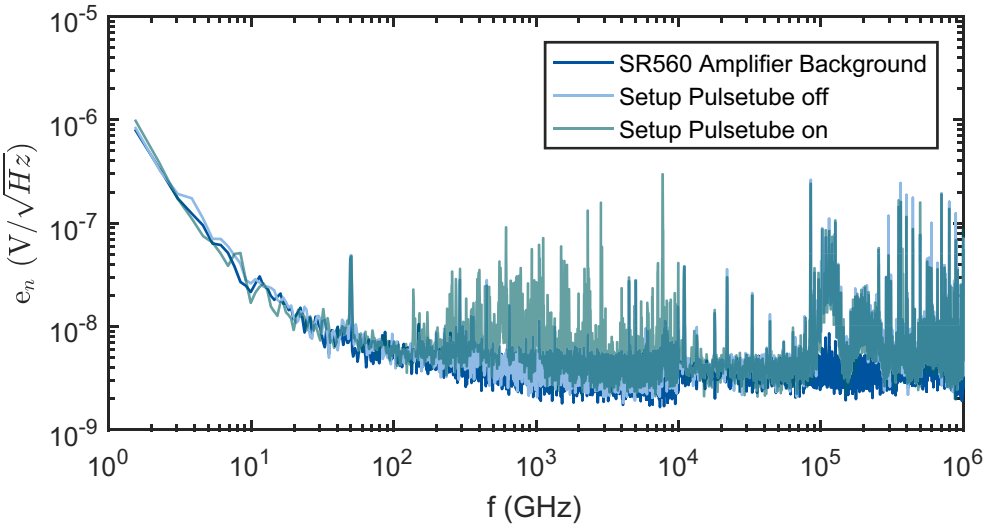

Figure 4.18.: Measurement voltage noise spectra without connected measuring equipment The low-frequency noise of the "Kurt" setup without connected measuring equipment generates additional hum, 1-10 kHz noise due to pulse tubes and >100 kHz noise probably originating from switching power supplies, compared to the SR560 preamplifier background.

The most straightforward measurement setup for determining the voltage noise spectrum of the refrigeration setup without any sample or electronics is to measure the voltage variations with a voltage preamplifier (SR560) and an oscilloscope (Tektronix DPO 7104C) to identify voltage noise sources at different frequencies. Given the sample resistance, this will give a first comparison with the IV converter current measurement. Figure 4.18 shows the Fourier-

transformed trace of the SR560 and shorted input to eliminate any influence of current noise. It shows the expected 3-nV/$\sqrt{Hz}$ noise floor and no additional interferences. If this measurement setup is combined with the refrigeration unit and the presented grounding concept, interference is generated at 50 Hz, at 300 Hz, as well as broader interference, which probably comes from switching power supplies in the range of 80-150 kHz and 180-300 kHz. The influence of the pulse tubes is significant in the range from 200 Hz to 30 kHz. Compared to the 8 μV contribution by hum, the contribution of the pulse tubes with 40 μV RMS noise is dominant. The RMS noise levels are given as numerically integrated contributions with a spectral resolution of at least 1/10 of the peak width.

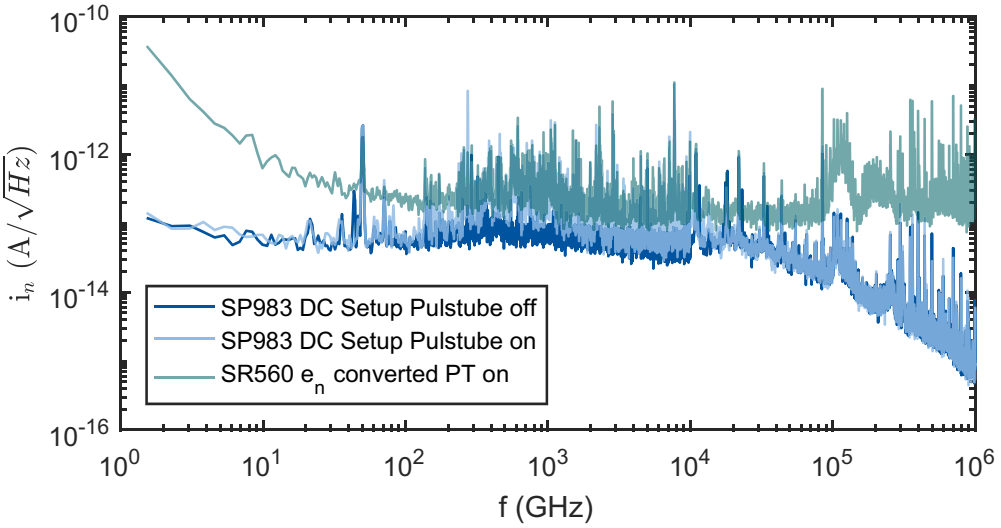

Figure 4.19.: Measurement current noise spectrum with IV Converter Corresponding to the lower background noise level and corner frequency, the background of the measurement setup is lower than the converted voltage noise background of the SR560. The cut-off corresponds to the filter setting, which is adapted to the bandwidth of the SP983 IV converter. The pulse tubes significantly increase the RMS current noise level. The converted voltage noise spectrum shows identical peak heights and a higher 1/f, white-noise background, as expected from the technical specifications of the SR560 amplifier.

After having established a baseline, the measurement setup can be evaluated with the SP983 IV-converter, a sample resistance in the range of the QPC or

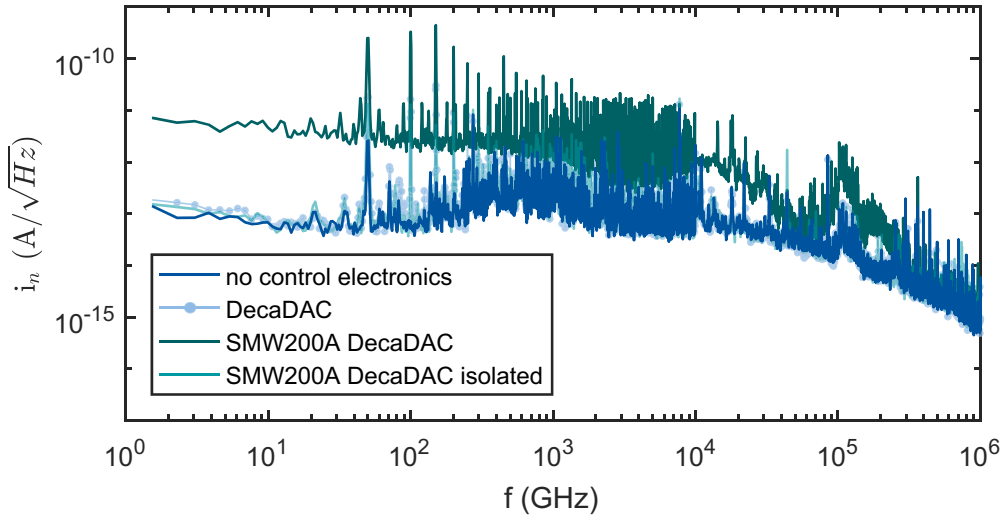

Figure 4.20.: Measurement current noise spectrum for different configurations of the control setup: The DecaDAC introduces higher harmonics of the power-line hum. The high-frequency sources only raise the background and interference levels if they are not thoroughly isolated (e.g., by an isolation transformer).

readout sensors (27 kΩ) is used in all measurements and an increasing number of setup electronics.

If no control electronics are connected, the resulting current noise of 50 fA/$\sqrt{Hz}$ noise level corresponds well to the 1.2 nV/$\sqrt{Hz}$ charge noise expected by the amplifier (Figure 4.19). The corner frequency is below 10 Hz, so a full 100 ms integration in the range of T_1 is possible. Compared to the SR560 converted voltage noise, the corner frequency is almost two orders lower. The background is also reduced. The amplifier's cut-offexpected for 1G amplification around 10 kHz. The resulting RMS noise in the corresponding measurement window for the desired spin readout within T_1 is 6 pA and increases to 20 pA with activated pulse tubes. The origin of the noise can be traced back to the voltage noise at the resistor since the amplitudes correspond to those of the converted voltage noise. The last plot (Figure 4.20) depicts the noise contributions of control electronics and occurring ground loops. The decaDAC voltage source induces higher harmonics of the hum and increases the RMS value by 5 pA. Adding a high-frequency source such as the SMW200A or TaborAWG,

background, and interferences are increased by two orders of magnitude, resulting in a 200-pA signal. The isolation transformer in the power supply line reversed this effect (24 pA).

The setup is fully equipped in this state, but is the noise performance sufficient for a spin readout? At 10-kHz acquisition and 100-ms integration times, the resulting RMS value fluctuation of the mean is 0.8 pA at 1-kHz measurement bandwidth 8 pA. With small measurement bandwidth, this signal is below the expected 1-5 pA signals, i.e., sufficient for spin readout. Additional software filtering of interferences and pulse-tube deactivation could push the readout to a higher measurement bandwidth.

Conclusion

This chapter reviewed and completed the group's efforts in the fabrication of interposers, PCB design, and testing. Developments in amplifier choice and testing, impedance matching, and the design and concept of an interposer-PCB integration platform result in a low-noise, high-bandwidth setup which, after initial characterizations, is sufficient for experiments on universal control in silicon quantum dots: The remaining dominant contributions are switching noise in the range 80-150 kHz and 180-300 kHz with 8 μV, power-line hum at 40 μV, and 200 Hz-30 kHz noise originating from pulse tubes. At 10 kHz acquisition and 100-ms integration times, the resulting RMS-variation is 0.8 pA, at 1 kHz measurement bandwidth 8 pA. For sub kilohertz measurement bandwidth, this signal is below the expected 1-5 pA charge sensor signals and is therefore sufficient for spin readout. Additional software filtering of interferences could push the readout to a higher measurement bandwidth. For single-spin qubit readout-critical thermalization, we have designed and produced multiple cryogenic filters for up to 192 DC lines with transmission characteristics comparable to less scalable PCB solutions. We have identified and resolved limitations in these designs, namely interface resistance and non-uniform contact. The fully integrated filter is as good in cut-off and attenuation as the state-of-the-art PCB metal powder [51] and has a smaller form factor, which improves scalability. In later experiments, the filters achieved thermalization

at 1.5 T, sufficient for Elzerman readout and approaching the intended working point of 1 T to maximize EDSR signal transmission. During prototype measurements, limiting effects (resistance and continuous contact of the enclosing box) were found. The resonances could be reduced to a background level. With a copper powder, an attenuation of 60 dB at 5 GHz, 80 dB at 12 GHz, and 100 dB at 35 GHz could be achieved. For sample-agnostic and future complex devices, we have designed, produced, characterized, and improved a small- to medium-scale integration platform suitable for various electron-spin quantum-computing platforms in GaAs and Si, for microwave control and DC- or RF-readout of S-T0 or single-spin qubits and quantum buses that meet the requirements on bandwidth, flexibility, and fast, low-cost production. The main improvements in bandwidth were the bias tee on the interposer solution, which improves the attenuation by four orders of magnitude (in the 10-14 GHz band), two orders in the 19-20 GHz band, and several optimizations at the critical interfaces, resulting in 12 dB attenuation between two inputs of the PCB-IP platform at 20 GHz and achieving a bandwidth comparable to PCB-only solutions. The microstrips also remove standing wave resonances in the simulation based on experimental parameters and attenuate any crosstalk signal up to 10 GHz. Finally, the technically feasible introduction of flip-chip bonding would solve the problem of parasitic-capacitance bond-wire resonance, which would result in a slowly increasing transfer function with up to four orders of magnitude improvement in crosstalk and standing-wave resonance damping via the stripline interposer solution. Compared to a PCB-only solution, the microstrip interposer achieves an additional crosstalk reduction of 25 dB up to 10 GHz.

Chapter 5.

Quantum-Dot and Sensor Tuning - Quantifying and Optimizing the Tunability of the Sample Design

One further challenge, which receives little attention in brief journal publications, is time efficient tuning and characterization measurement processes to identify and tune promising samples quickly. This work builds on standard methods published for doped systems like Botzem et al. [13] and it is intended as starting point towards less time-consuming and more scalable automated tuning like Baart et al. [76]. The following sections describe, for completeness, all steps towards tuning a single dot for relaxation time measurements, track variations of sample and heterostructure design, setup and experimental run parameters (see table on sample details Table 5, setup/cooldown details are covered in the appendix Table A.5) and their relations to measurement/tuning results. New tuning methods for undoped samples are introduced (e.g., 4K 2D pinch-offs, dot triangulation) to support future automation efforts and efficient scalable tune-up. As a result I developed a semi-automated tuning, visualization tool-kit, and analysis workflow based on the "special measure" toolkit (Appendix C) as well as a dot triangulation method. The results achieved regarding the specifications in the previous chapter are characterized. These efforts resulted in a single shot spin readout in an undoped silicon-28 sample with nanomagnet presented in the final section.

Heterostructure					Sample		
Doping	SiCap [nm]	SiQW [nm]	Wafer ID	Design	TG	Sensor	Device ID
doped	10	10	R1940	RBd1	global	| -	MV
undoped	3	10	R2104	ACud1		- -	P14
			R2104A8	RBud2			MII
					split	| -	MIII
			R2104B7			- -	MIV
					global	| -	MV
	1.5	12	R2152A12	RBud3	global/split		MI-IV
			R2159A7		global	- -	MI*
							MVI*
			R2160A7		split		MI*
					global		MII*
							MIV*

Table 5.1.: Sample Heterostructure Design Parameters: Overview of heterostructure- and sample-design parameters of samples evaluated in this thesis, which were motivated in Chapter 3: Heterostructures supplied by the group of Dominique Bougeard in Regensburg varied in doping, silicon cap (SiCap), and the width of the silicon quantum well (SiQW), with sample fine gate designs (Design) being fabricated in Aachen (design: ACud1) fabricated by Bernhard Klemt based on the fabrication recipe developed in this thesis. Floyd Schauer and Christian Neumann produced Regensburg samples (fine-gate design: RBd1, RBud2, RBud3 - Figure 3.2). Top-gate designs include split-gate and global-gate designs. Sensor designs varied between T-shaped ($|-$) and split-gate ($--$) designs. Multiple devices are considered for each combination of design parameters. * - Silicon-28 purified samples, gray - samples without accumulation signatures.

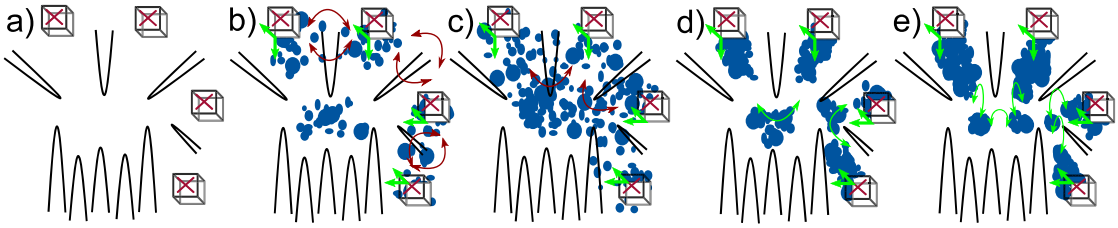

Figure 5.1.: Sketch of tuning protocol steps: (a) 0 V configuration without electron occupation, "x"-boxes - ohmic contacts, black - gates; (b) accumulation of charges (blue) in the 2DEG ensures conductivity between source and drain; (c) low-resistance linear I-V curves ensure homogeneous 2DEG between ohmics, fine-gate dependence near the dot region, green - current channels, red - parasitic channels; (d) 2D-pinch-offs with diagonal features prove transport through DQD and the sensor region; (e) fine-gate tuning establishes quantum dots, control of electron number, and barrier tuning.

5.1. Tuning Protocol and Tunability Measures - Dot and Sensor Functionality Across 12 Samples

Accumulation Functionality Test - Inducing a Homogeneous Stable Unhysteretic 2DEG

In our undoped samples with reduced gate pitch for increased gate number and control, fine gates screen the accumulation gate stronger. Changes in the fabrication process (e.g., fabrication ramp-up in Aachen, gate oxide, or new designs) require the testing of new voltage working regions while preventing sample damage by breakthroughs or recharging effects causing hysteresis and challenges in experiments with multiple repetitions and permuting pulse train elements. In the following, I establish working regions for the current sample designs and quantify detrimental effects and statistic variations to tuning, like hysteresis or inter- and intra-sample tuning parameter variations and their origins.

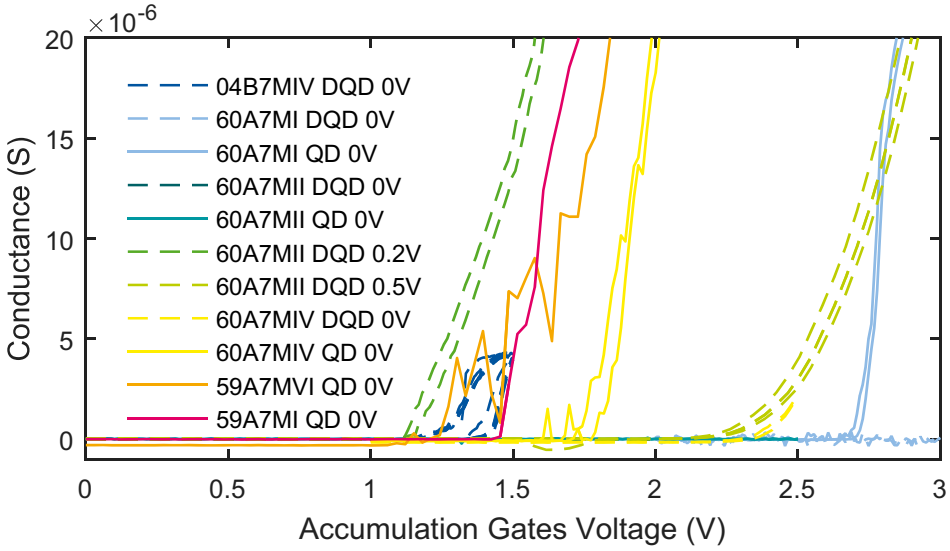

Figure 5.2.: Accumulation Characteristics at Base Temperature for multiple heterostructures (R21-"04B7", -"59A7", -"60A7"), designs (RBud2 - "04B7"; RBud3 - "60A7"& "59A7"), samples (R2104B7MIV, R2160B7MI, R2160B7MII, R2160B7MIV, R2159A7MI, R2159A7MVI), cooldowns details see Table 5.2, sensor ('QD' dashed lines) and double quantum dot current ('DQD' full lines), and fine gate voltages (0V, 0.2V, 0.5V). Not shown are samples that do not show a reaction within the depicted voltage interval because the sample or setup is compromised - R2152A12, R2104A8 MII, MIII, R2104B7MV. Curves show qualitative variations from peak structures to exponential-like onset and onset-voltage spread larger than typical onset-voltages of 1.5 V

Accumulation Voltage Working Ranges for Accumulation Gate and Fine Gates

Figure 5.2 shows the accumulation curves for different heterostructures, gate designs, DQD, and sensors ('QD') of multiple devices and cooldowns. A detailed overview is shown in Table 5.2. The starting points for the accumulation tests were the 0-3 V range for top gates and -1.5-0.2 V for fine gates as tested and proposed by cooperation partners in Regensburg. Bias voltages in the range of -1 to 1 mV, typically 0.1 mV, were applied. Except for the DQD in Sample R2160A7MI during its only cooldowns and the sensor, and DQD in R2160A7MII during cooldown 18, all remaining working samples showed induction within the range of 3 V. The sensor in R2160A7MII could be acti-

vated by ramping the sensor gates ('QN','QS') to 0.39(5) V. The double quantum dot could be activated at 0.5 V for all fine gates and at 2.7 V for the top gate. When the samples did not show a conduction onset until 3 V, all fine-gate voltages were increased up to a maximum of 0.5 V, resulting in onsets for multiple cooldowns of 60A7MII (Figure 5.2). The sample R2160A7MI showed some induction but broke at a potential difference of 3 V between the small and big top gate, causing permanent damage to all gates. Therefore, in future experiments, the two top gates were synchronized, and software safety checks were implemented. Tests up to 4 V at accumulation gates did not show improvements for non-reactive samples. All 7 remaining samples (R1940MV, R2104B7MIV, R2159MI, MVI, R2160A7MI, MII, MIV) are functional with regard to accumulation and hysteresis for the working range of -1.5-0.5 V for fine Gates and 0-3.5 V for the accumulation gates.

Hysteresis Quantification

To be able to reliably carry out experiments in the multidimensional gate space (e.g., resetting the qubit to readout, control, and other characteristic points in arbitrary order), it is necessary to check the device for hysteretic behavior. In one sample - R2104B7MIV DQD - a stronger effect was observed, which is not related to the voltage sweep but is due to a charging effect of the split top gates on the sample with a time constant of 2 seconds. The following possible sources can be excluded: the setup, which was reused in the same configuration for later samples, and the integrity of the metal gate structures since AFM measurements did not show any defects. As shown in Figure 5.2, the hysteresis between forward and reverse sweeps is less than 50 mV at large voltage sweeps of 3 V and sweep speeds of 0.1 V/s. In further dot-tuning and spin-lifetime experiments, this effect has never limited the tunability of our samples.

Variations in Accumulation Characteristics

Previous measurements show qualitative and quantitative variations (see Figure 5.2) of the accumulation curves in the range of more than one volt. The

onset voltages are determined oo understand the relevant causes of these variations and grouped in Table 5.2 by possible setup and sample causes. To determine the main source of these variations, Table 5.2 shows the onset voltages depending on sample and setup parameters: wafer number, (fine-gate) design, sample (ID), current path (through sensor or DQD), the voltage at all fine gates and cooldowns. The accumulation onsets are determined as the voltage at which the conductance is significantly above the typical currents of quantum dot resonances in our samples (0.1-0.2 µS). The resulting measurement uncertainties are in the 10 mV range and smaller than the observed variation in onset voltage. All wafers show minimum onsets in the 1.1-1.4 V range, for large sample sizes and heterostructure R2160A7 outliers of >3 V were observed, R2014B7, R2159A7 did not show outliers for a small sampling size. To make reliable statements about onset correlation on wafer numbers, larger sample sizes for R2014B7 and R2159A7 would be required. The same holds for the design choices ("design", "TG", "current path") supporting the design choices as viable options for further experiments. For each design root cause candidate, the mean value rms-variation is larger than the influence of the design parameter (e.g., the size change of the DQD dots compared to the sensor dot). These variations are limited to 3 out of 6 samples. For 2, thermal cycling could resolve the high onset (R2160B7MI, R2160B7MIV). For R2160B7MI, 2 cooldowns did not suffice to reset the sample to a normal state. With an increasing cooldown number, the onset voltages vary unsystematically. Therefore, deterioration of the setup as a root cause can be excluded. In summary, the observed variations in the accumulation characteristics are low-temperature-stable and vary between individual DQDs or sensors and cooldowns. This suggests local recharging at higher temperatures primarily influences the increased onset voltages. Eight samples showed no accumulation due to fabrication or setup limitations. All 7 intact samples showed accumulation during at least one cooldown and either in the sensor or the DQD. Details can be found in A of the appendix.

Candidate, State (Sample Size)	Min (V)	Mean	Max (V)	Max-Min (V)
Wafer				
R2104B7 (1)	1.2(4)	-	1.4(4)	0.2
R2160A7 (8)	1.1(3)	2.34± 0.65	**>3**	>1.8(7)
R2159A7 (2)	1.2(4)	-	1.4(6)	0.2
Design				
RBud2 (1)	1.2(4)	-	1.4(4)	0.2
RBud3 (10)	1.1(3)	2.14±0.71	**>3**	>1.8(7)
TG				
split (3)	1.3(4)	2.35±0.89	**>3**	>1.6(6)
global (9)	1.1(3)	1.96±0.68	**>3**	>1.8(7)
Current Path				
DQD (6)	1.1(3)	2.20±0.8	**>3**	>1.8(7)
Sensor (5)	1.2(4)	1.92±0.65	**2.7(2)**	1.4(8)
Sample				
R2104B7MIV (1)	1.2(4)	-	1.4(4)	0.2
R2160B7MI (2)	**2.7(2)**	-	**>3**	>0.2(8)
R2160B7MII (4)	1.1(3)	2.24±0.78	**>3**	>1.8(7)
R2160B7MIV (2)	1.6(2)	-	**2.4(0)**	0.1
R2159A7MI (1)	1.4(6)	-	1.4(6)	-
R2159A7MVI (1)	1.2(4)	-	1.2(4)	-
Cooldown				
9 (R2104B7MIV) (1)	1.2(4)	-	1.4(4)	0.2
15 (R2160B7MII) (2)	1.1(3)	-	**>2.5**	>1.3(7)
16 (R2160B7MI) (2)	**2.7(2)**	-	**>3**	>0.2(8)
18 (R2160B7MIV) (2)	1.6(2)	-	2.4(0)	0.1
18 (R2160B7MII) (1)	**2.3(0)**	-	**2.3(0)**	-
19 (R2160B7MII) (1)	**>3**	-	**>3**	-
20 (R2159A7MI) (1)	1.4(6)	-	1.4(6)	-
20 (R2159A7MVI) (1)	1.2(4)	-	1.2(4)	-
Fine Gate Voltage				
0.0 V (9)	1.2(4)	2.15±0.72	**>3**	>1.7(6)
0.2 V (1)	1.1(3)	-	1.1(3)	-
0.5 V (1)	**2.3(0)**	-	**2.3(0)**	-

Table 5.2.: Root cause candidates, property values, sample size and according statistical measures for accumulation-onset voltage. Outliers are marked in bold font. The mean value is given for sample sizes >3.

Ohmic Functionality Test - Constant Resistance as Measure for Channel Quality

In the pursuit of a homogeneous Fermi sea in the electron reservoirs and a single tunable tunnel barrier to the dot and view of the previously observed qualitative variations in the accumulation behavior, it is essential to investigate further the I-V_{bias} characteristic of the sample. Linear behavior is the first indicator for a path free of tunnel junctions or quantum dots. Furthermore, low ohmic resistances are relevant to ensure a significant change in conductance during charge readout. In early test samples without isotope purification, several combinations of the ohmics were measured to determine the resistance of each one. Later, this practice was changed to setting up the electronics only once before cooldown to avoid electrostatic discharge (ESD) damage by changing the switch configuration or removing equipment. Measured ohmic resistances after accumulation ranged from 2 kΩ to 73 kΩ after correcting for the room-temperature value of the filter 2 kΩ resistors (the values for low temperatures deviate by 5-35% from the specified values for the wire resistors used in the kΩ range). Figure 5.3 shows three characteristic curves from this interval. The characteristic of ohmic III in R2160A7MII, and ohmic I in R2104B7MIV could not be linearized (see 73 $k\Omega$ trace in Figure 5.3) within the safe voltage ranges and four cooldowns of the samples. These non-working ohmics are not linked to a wafer or the design choice (see Table 5.1). Further measurements in our samples revealed that all high resistances can be traced back to Coulomb blockade features (Coulomb diamond measurements e.g., see Figure 5.8). In working samples, fine gate voltages influenced the qualitative behavior of the I-V-curve. This observation shows that the current path constrictions are quantized electron systems near the dots - in the DQD, sensor, and reservoir regions. The conductance in our samples is sufficiently high for sensor tuning. In two cases and multiple cooldowns, it is limited by an inhomogeneous 2DEG for top- and fine-gate voltages within the safety intervals. This opens the possibility of filtering out these samples at 4-Kelvin pretests to save time and resources of dilution refrigerator trials. Disorder in the sample heterostructure near the dot sites is a possible candidate for this observation and may reduce tunabil-

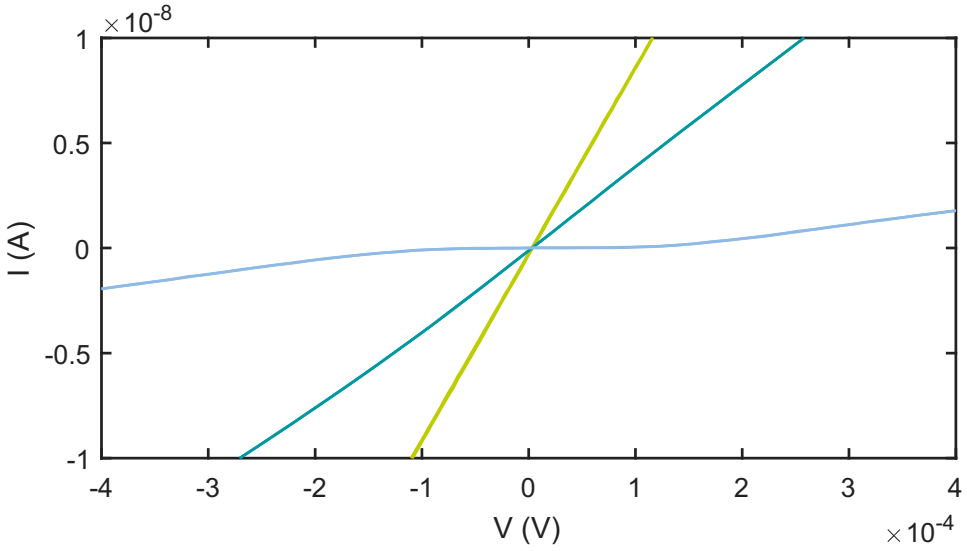

Figure 5.3.: Exemplary Ohmic Current-Bias-Voltage Characteristics: green - low resistance (3.(6) kΩ) linear characteristic; turquoise - higher resistance (11.(1) kΩ) characteristic; light blue - non-linear characteristic with clear plateau ($\Delta I/\Delta V$=73.(3) kΩ) indicating Coulomb blockade.

ity. With this test, it is not possible to identify the origin of the disorder and whether the current follows the intended path through the sensor and the double quantum dot (i.e., below fine gates). After testing the functionality of the gates, the next section on 2D pinch-offs will shed light on this issue.

Gate and Dot Charge Control Functionality Test - 1D and 2D Pinch-off as Charge Occupation Tunability Indicator

The ohmics and accumulation gates work, and the remaining functional part of the sample is the fine gates. Since fabrication and handling still result in samples with non-working ohmics or damaged gates due to transport, ESD, or sawing, a 4-K test reduces unnecessary 30-mK cooldowns and can be performed parallel to 30-mK measurements.

As a first and quick test of functionality, 1D-pinch-offs are an option. These measurements (shown exemplarily for sample R2104B7MIV in Figure 5.4) show significant variations in pinch-off voltage, which do not coincide with the expected distance relationship (pR pinch-off 0.3 V, shifted compared to pL

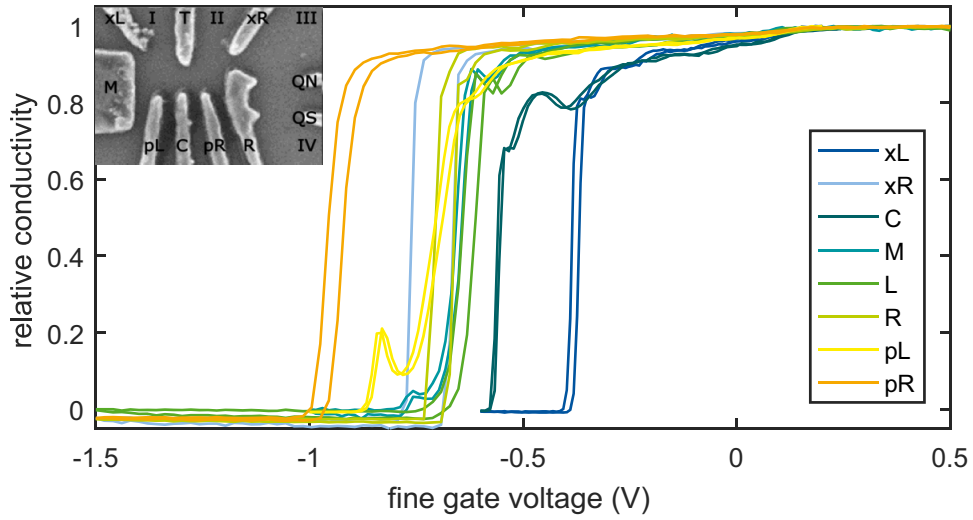

Figure 5.4.: 1D pinch-off characteristics for sweeps of T with a second gate specified in the legend (ordered by distance to the T-gate). All curves reach a non-conductive regime, indicating the gates' functionality. Large (0.3 V) offsets between pinch-offs of equally distant gates and missing Coulomb resonances or conductivity steps require further investigation of current paths and gate functionality.

despite the identical distance). Additionally, the accumulation onsets indicate variations in the working points of the fine gates. Furthermore, a 1D pinch-off does not indicate the current path through the dot regions. Establishing an indicator for an initial dot-tuning parameter set of the reference voltage(s) would help: The 2D-pinch-off method I introduce uses the T-gate as a reference since it divides the two DQD ohmics. This T-gate reference parameter (see Figure 5.5 yellow regions for T$>$ 0.1 V) is indicated by a sudden drop in conductance at the definition voltage related to the depletion under the fine gates' connections to the macroscopic contact pads as discussed by Barnes [77]. All other gates are swept against T, creating the 2D scans in Figure 5.5. The starting point in the voltage parameter space is given by the voltages generating linear characteristics in the aforementioned linearity test. These scans were implemented in all cooldown phases after R2104B7MIV, namely in the ^{28}Si samples R2160A7MII,MIV, and R2159A7MVI, MI, and all samples with identical gate design RBud3 and heterostructure design.

The scan in Figure 5.5 from a 4-K test of sample R2159A7MI showcases the

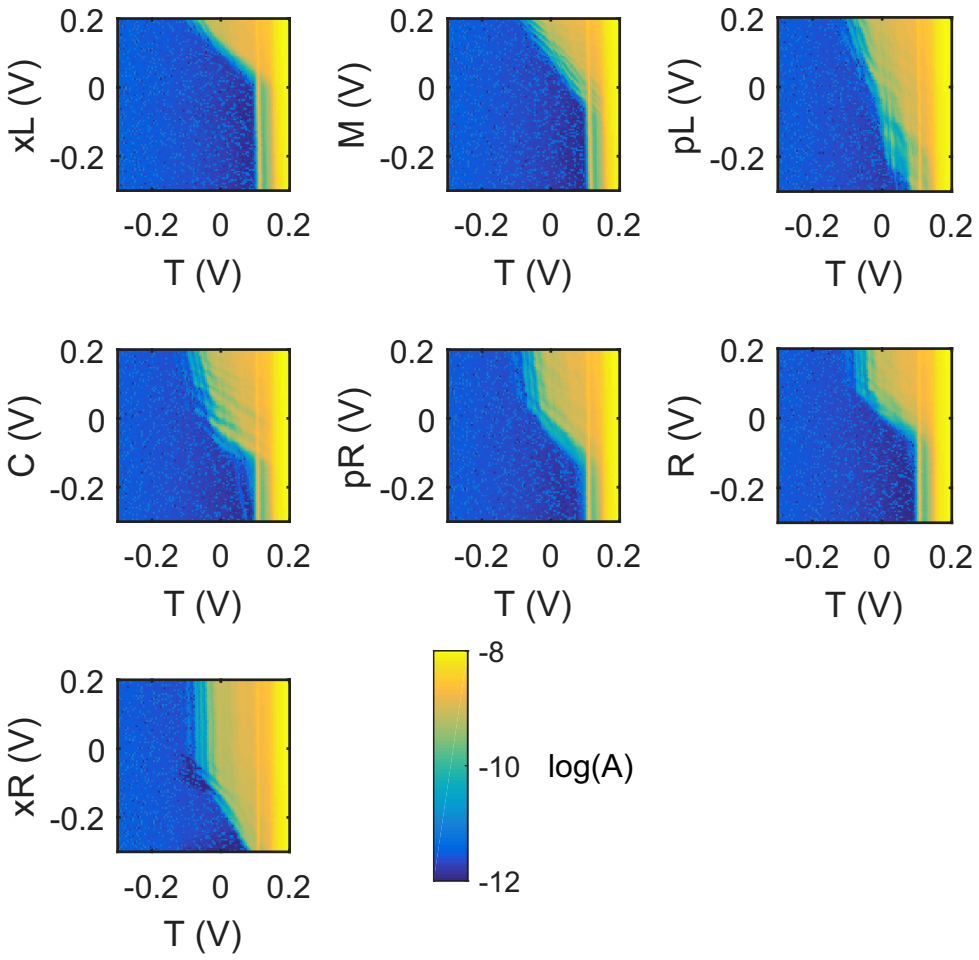

Figure 5.5.: 2D pinch-off characteristics: for sample R2159A7MI at 4 K, 0.2 V at fine gates, 2 V at the global accumulation gate. The pinch-off region is in blue. The rectangular yellow high-current region up to the definition voltage 0.1 V indicates the current below T. Triangular or trapezoidal regions with sinusoidal modulation indicates the current through quantum dots or paddles near the dot region.

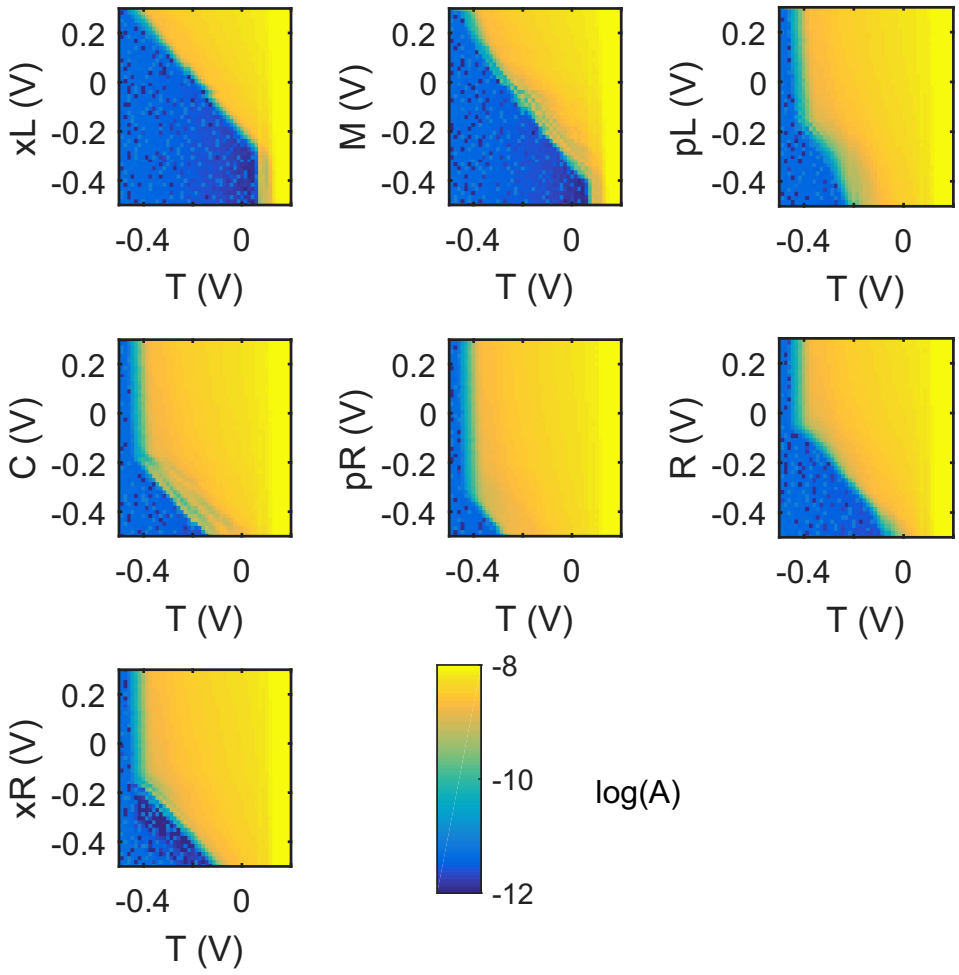

Figure 5.6.: 2D pinch-off characteristics: for sample R2159A7MI at 4 K, 0.3 V at fine gates, 3 V at the global accumulation gate. The pinch-off region is in blue. The rectangular yellow high-current region up to the definition voltage 0.1 V indicates current below T. Triangular or trapezoidal regions with sinusoidal modulation indicates the current through quantum dots or paddles near the dot region.

characteristic features and their support in tuning: The T-gate definition voltage of 0.1 V can be determined from the vertically-bounded region with the highest current, that is independent of the other gate voltages within and between 2D scans. After this point, the current flows only beneath the slim, fine gates but not beneath the large fan-out gate structures. Another conducting region stands out against the blue background of the pinch-off: Depending on the swept gate, its shape is triangular or trapezoidal, modulated by oscillations at the edges near the pinch-off. The vertical pinch-off corresponds to suppressing current beneath the T-fine-gate structures far from the other fine gates. The conductive regions shift with the fine-gate and accumulation-gate voltage, suggesting that these are the regions of transport near the DQD. C and pL scans show a less steep slope, indicating that the current limiting disordered reservoir is 'I'. This is either due to the asymmetrical design with the nanomagnet or to the cooldown/sample-specific disorder. The established starting point for a promising tuning region is thus at and beyond the diagonal (roughly 45) modulated edges (Figure 5.5), where both gates have a similar influence on the conductance. Increasing the accumulation gate voltage to 3 V and the fine gate voltage to 0.3 V, the modulations of the vertical-pinch-off edge disappear, and the edge rotates towards a vertical direction. This reduction in distinct oscillation slopes indicates that changes in T-voltage create fewer intermediate unintentional dots or located electron systems. Thus, a more homogeneous 2DEG in the electron reservoirs and a localized electron system close to the fine gates is achieved. Compared to the ohmic and 1-D pinch-off tests, this helps to localize remaining inhomogeneous regions in the electron reservoirs or unintentional tunnel barriers or dots. These measurements can be reproduced when samples are cooled in the 30-mK setup using the sensor path for sample safety (see Appendix A). Of 6 samples (out of 11) that reached the stage of 1D- and/or 2D-pinch-off, only two failed this test: R2159A7MVI showed one leaking gate due to dielectric damage, R2160A7MIV pL, pR lacked the influence on the 2D-pinch-off due to bias tee on interposer shorts (see Appendix A).

This is the starting point for dot-tuning towards the single electron regime, but it leaves open the need for a method to determine which samples are promising qubit candidates.

DC Sensor, Quantum Dot Tuning and Design Improvement

This paragraph sketches the next step of charge readout initialization for completeness and illustrates improvements in sensor design for increased working range. Resulting sensitivities will be discussed in section 5.3. Starting point of the sensor tuning is the xR-gate set to the definition voltage (xR-T-scan in Figure A.1) and the R-gate to the minimum voltage of the dot transport region to conserve the symmetric voltage tuning of the DQD. 2D scans of the two sensor barrier gates (QN,QS) repeated for step-wise reduced R-gate-voltage achieve Coulomb resonances as shown in Figure 5.7. The left-hand subplot shows the features of the previous design of sample R1940MV characterized in the Hell-setup at the early stages of this project. The triangular dot transport region shows only two resonances immersed in the vertical and horizontal definition regions. For decreased DQD voltages, these features absorb into the definition region, resulting in vanishing sensitivity. As countermeasure we increased the aperture angle between ohmic enclosing gates and the gate distance from 50 nm to 150 nm, resulting in scans with multiple Coulomb oscillations as shown on the right. As a worst-case example, the top right scan is of sample R2160A7MII with high ohmic resistance in ohmic III and the corresponding vertical and horizontal modulations resulting from the disorder-dominated lead without clear Coulomb resonances. These scans support the interpretation of the previous section and reproduce findings in disordered nanowires by Spruijtenburg et al. [44]. R2104B7MIV showed the best results with distinct diagonal Coulomb resonances of a single quantum dot (Figure 5.7 bottom right). This interpretation is supported by clear and distinct Coulomb diamonds in Figure 5.8 in contrast to R2160A7MII with overlapping smaller structures of different sizes corresponding to multiple larger quantum systems.

Further tuning of R2160A7MII with xR and R emptied unintentional dots and double dot features could be observed in Figure 5.9 so that all 4 functional samples with the new design achieved tunable sensor quantum dots in the sensors. Capacitive charge readout reproduces coulomb resonance positions from early direct transport measurements with a typical signal strength of a few picoamperes in Figure 5.9. Without transport measurements and in cases of

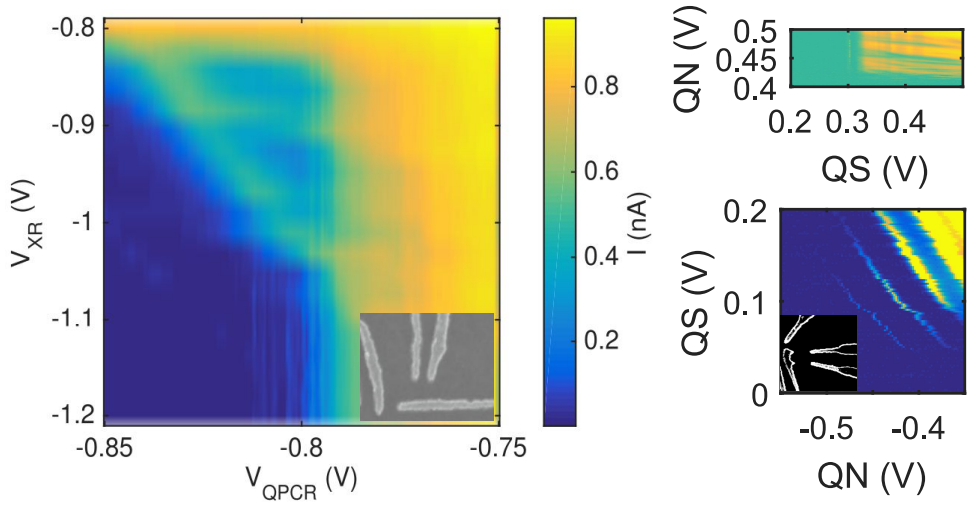

Figure 5.7.: 2D scan sensor: Charge sensor scans for R1940MV-doped sample 50 nm separation - left, disorder limited sensor in R2160A7MII (top right) and single dot sensor in R2104B7MIV (lower right) undoped samples at 150 nm separation.

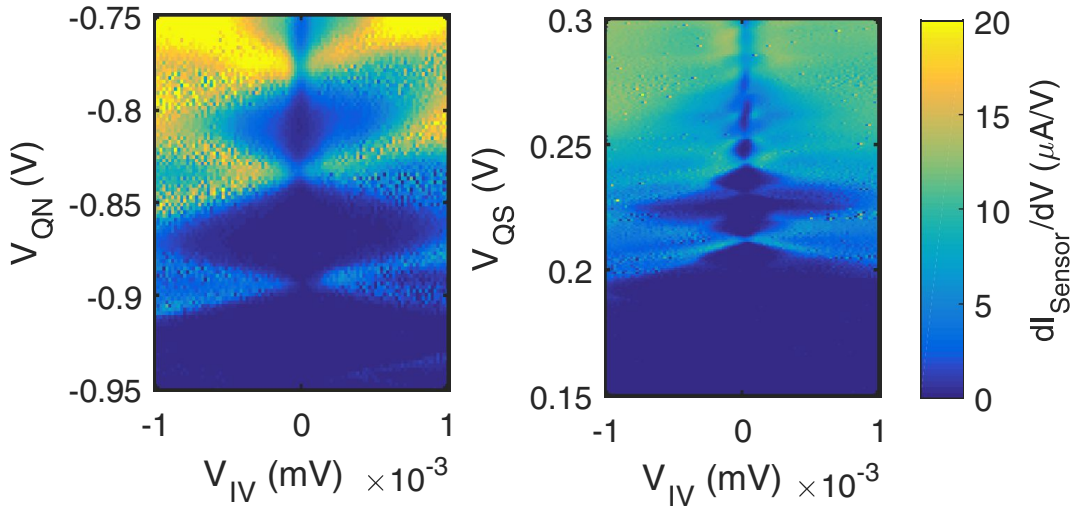

Figure 5.8.: Coulomb diamonds left - single dot charge sensor R2104B7MIV, right - multi-dot charge sensor R2160A7MII

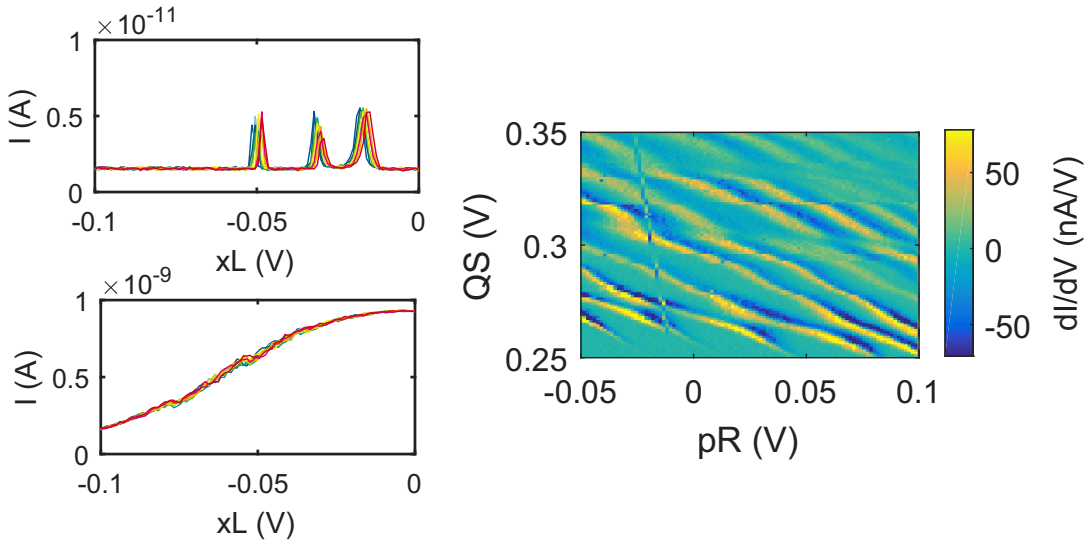

Figure 5.9.: Charge sensing top left - Coulomb resonances in dot transport; bottom left - corresponding charge sensor reaction with steps at resonances; right - 2D charge sensor sensitivity tuning and electron transition detection; high transconductance increases readout contrast, not all transitions are equal in the capacitive coupling, thus charge sensitivity, e.g., due to multiple dots with different positions.

unintentional multi-dot sensors (e.g., R2160A7MII), 2D scans with one sensor and one DQD gate proved to be helpful to identify sensitive sensor transitions (e.g., by stronger capacitive coupling of one of the sensor dots) and visualize quantum dot transitions (Figure 5.9). The transconductance was optimized by varying the sensor bias to improve the signal-to-noise ratio further. By these tuning methods, R2160A7MII achieved 15 nA/mV from an earlier 1 nA/mV, while R2104B7MIV achieved the highest transconductance of 45 nA/mV. All 4 functional samples could be tuned to find charge readout signals.

Few Electron Single Dot Tuning

The sensor activation and charge readout are the starting point for dot tuning to the single electron regime. It leaves open the need for a method to determine which samples are promising qubit candidates given the observed sample and cooldown variations. The goal was to tune a single quantum dot in the right

Gate	xL	T	xR	QN	QS	R	pR	C	pL	M	TG
Potential 1 (V)	-0.5	0.15	-0.08	-0.9	0.2	-0.14	0.5	-0.15	-0.2	-0.15	3.5
Potential 2 (V)	0.15	-0.1	-0.2	-1.8	-2.0	-0.2	0.3	0.18	0.3	-0.4	3.6
Potential 3 (V)	0.5	-0.3	-0.36	-0.83	-0.27	-0.25	0.4	0.14	-0.2	0.2	3.7

Table 5.3.: Gate configuration for R2159A7MI

point close to the sensor for maximum readout sensitivity. R2159A7MI shows three regimes towards this goal shown in Figure 5.10 and the corresponding potentials in Figure 5.11 originating from an electrostatic simulation validated in Appendix 5.3. The first simulation, with negative left-side gates, strongly confines the dot to the right side of the device. The second one shows a large dot over the entire width of the device, and the last one shows a weakly confined dot on the right side with a second dot about to localize on the left. The corresponding measurements show a multi-dot system for the strongly confined first configuration, double-dot features for the second, and isolated single-dot features for the last. One explanation for this behavior is an increasing homogeneity of the system as the accumulation gate voltages increase, starting from disorder-dominated dots in contrast to the predicted single dot, indicating disorder variations on length scales below 100 nm for configuration 1. With increased accumulation gate and left dot fine gate voltage (M,xL) for a homogeneous electron reservoir and negative T gate voltages to unload unintended dots on the left, an isolated single dot could be achieved in R2159A7MI for configuration 3. The occurrence of multiple transitions without signatures of opaque barriers (Appendix section 5.3) is a strong indicator of reaching the single electron occupation.

The tuning of two different designs, three different samples, and configurations allows comparisons in terms of reliability and evaluations of gate design: Figure 5.12 shows the voltages for all samples and configurations grouped by gate name. The accumulation gate voltage difference for the two designs is 1.75-2 V qualitatively agreeing with reduced accumulation gate capacitance to the dot due to reduced dot size. With the same design 'RBud3' and different cooldowns and samples, an increasing accumulation voltage led to an

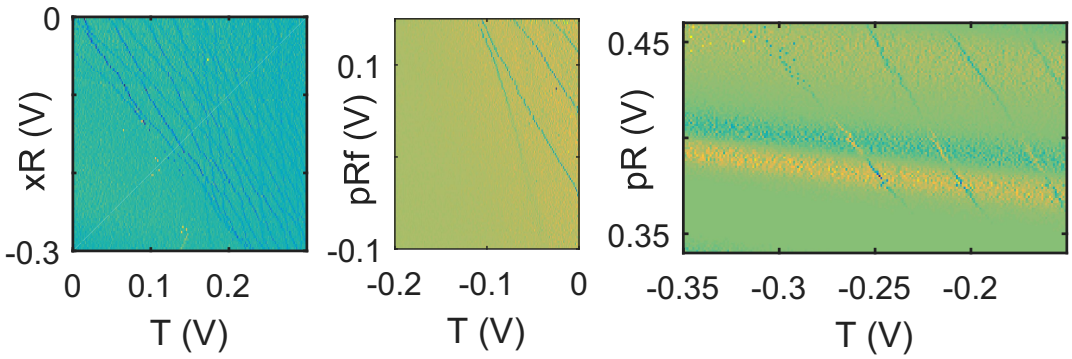

Figure 5.10.: **R2159A7MI Few-electron-regime** isolation of single dot charge transitions from a multi-dot system to increase the accumulation voltage and positive left side gates.

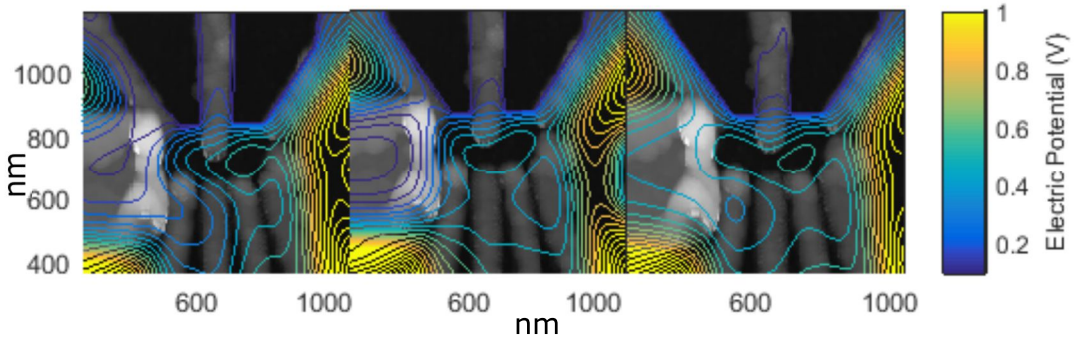

Figure 5.11.: **R2160A7MI electrostatic simulation** isolation of single dot charge transitions from a multi-dot system to increase the accumulation voltage and positive left side gates indicate a beneficial effect of occupying the left-dot region to avoid splitting into unintended dots and improve the loading of the right dot.

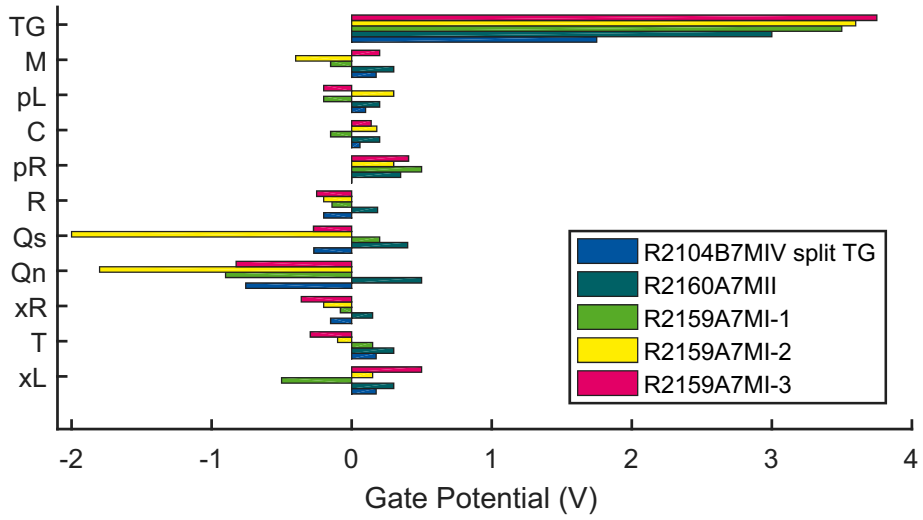

Figure 5.12.: Gate voltages for few-electron configurations for samples R2104B7MIV, R2160A7MII, R2159A7MI, designs RBud2, split accumulation gate (R2104B7MIV), RBud3 global accumulation gate (R2160A7MII, R2159A7MI); high positive accumulation voltages help tuning for RBud3; sensor voltages show strong variations during one cooldown

improved single dot tuning as indicated by the 3 configurations of sample R2159A7MI, with the limitation of increased instabilities for voltage levels close to 4 V tested in sample R2160A7MIV. An example of this trade-off is visible in configuration 2 compared to 1 and 3: Even within one sample and cooldown of R2159A7MI, the voltages varied between -2 V to 0.3 V, which is due to single large recharging events at high accumulation voltages (3-4 V) within the first days of the cooldown. Advantageously, these become increasingly rare (on a monthly scale) after refraining from the initial large voltage sweeps required for accumulation functionality tests.

All functional samples R2104B7MIV, R2160A7MII, and R2159A7MI could be tuned to the few-electron regime. The devices remained stable at fine-gate voltages of -2 to 0.5 V. Accumulation voltages above 4 V lead to saturation of the accumulation curve and instability in one device. The new designs can be tuned to single electron regimes for high accumulation gate voltages (3.6-3.75 V). The remaining influence of disorder indicated by electrostatic simulations can be quantified by determining the dot position and comparing it to the

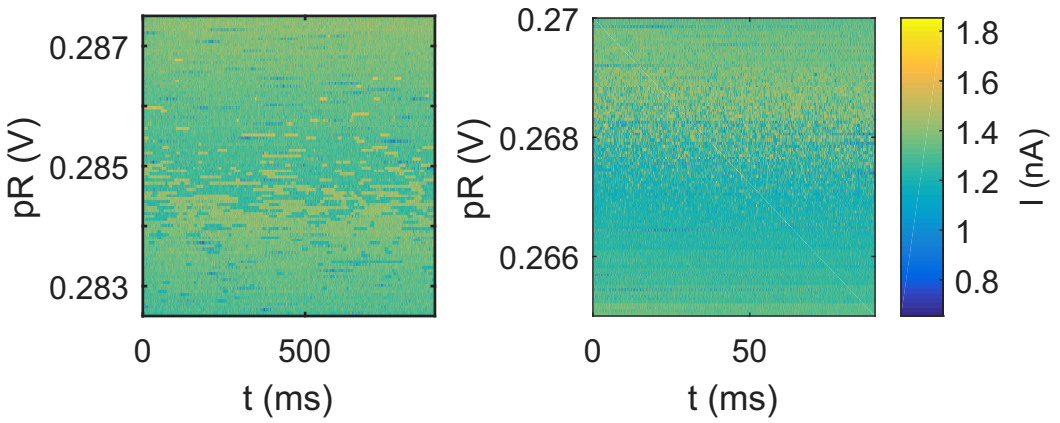

Figure 5.13.: Barrier tune: Time traces of single electron tunnel events for different gate voltage and tunnel timescales. Tunnel rates could be tuned over at least three orders of magnitude by 100 m V gate variations.

simulation results.

Reservoir Tunnel Coupling Control

The remaining dot charge control parameter as the basis for Elzerman spin readout is the tunneling rate. It is described in brief, as it is the basis for further pulsed experiments for lifetime and dephasing characterizations. For reduced trial times, the tunneling rate and the charge detection bandwidth should be as high as the current 10-kHz measurement bandwidth. To achieve full bandwidth, measurements were performed with a high-bandwidth Alazar PCIe data acquisition card instead of the 3-kHz bandwidth Agilent 34410A DMM. The data was recorded at full 100 MSPS (mega samples per second) and downsampled to 100 kSPS by the Python driver. The data stream was fed to special measure by an additional Python-MATLAB interface developed by Simon Humpohl. The SP983-IV Converter was set to 10-kHz bandwidth and 10E8 I/V-conversion. The gates chosen for barrier control are xL, T and xR directly at the end of the electron reservoirs. A simple method of evaluating the tuning range of the tunneling rate within the measurement bandwidth first

reduces the tunneling rate until it is comparable to the voltage scan rate in the order of seconds in a 2D scan. This results in probabilistic single electron tunneling with different transition positions in successive scan lines, further called transition fan-out (Figure 5.10). Subsequently, time-resolved measurements are carried out while stepping a gate with a high tunnel barrier lever-arm until the tunneling rate is sufficiently slow to detect Elzerman signatures described in chapter 2. 2 of 3 dots formed in the 3 examined samples showed a tunnel rate tunability from sub-second to 10 kHz range, sufficient for fast Elzerman readout through the expected gates (xR,R). In the third dot (formed in Sample R2160A7MII), the transition width is limited by the sensor bias within the tuning intervals limits, resulting in artificial broadening due to tunnel coupling to the reservoirs (see Appendix A including details on tuning parameters), which is larger than the expected Zeeman splitting and thus has a detrimental effect on the spin readout.

5.2. Quantifying the Influence of Disorder on Quantum Dot Position - Triangulation for Dot Identification and Spin readout Prospects

Several observations show that reliable tuning of a silicon quantum dot qubit in Si/SiGe heterostructure samples relies on high sample quality, which today is a non-trivial problem with an impact on scalability towards a functional quantum computer: The first implementation of a 2-qubit processor realized with silicon quantum dots by Watson et al. [33] depicts two quantum dots within an area designed for only one. Calculations by Jan Klos [78] (electrostatic 3D numeric simulations) and analytical estimates in this thesis (Chapter 3) suggest that charged defects in the silicon heterostructure or the gate oxide could produce potential variations, which have the same order of magnitude as the metal gate induced potentials. Furthermore, measurements in this thesis showed one quantum dot in each sample R2104B7MIV and R2160A7MII with only 1-2 tran-

sitions in the region where the charge readout and tunnel rates to the electron reservoirs are functional(Appendix section 5.3). This creates uncertainties regarding the clear discrimination of a quantum dot from multi-electron traps. The quantification of these influences and a test for excluding multiple electron charge traps located in the oxide would facilitate the understanding of disorder origins and potential improvements of the heterostructure stack. A common way to determine the dot positions is to estimate it from the various gate lever arms. As there are more gate combinations than independent variables, this provides overcomplete information, which is typically inconsistent due to various sources of errors and model inaccuracies originating for example from shape uncertainties like artificial broadening of features by atomic force microscopy. Here, I present a triangulation method for gate-defined quantum dots that systematically deals with redundant information in a mathematically motivated way. It determines the dot position from measurements of the relative lever arm of two metal gates on an electron transition in combination with a 3D electrostatic numerical model representing the complex capacitive couplings within the device. Combining both enables determining quantum dot positions within the device that agree with the observed lever arms regarding the relative capacitive coupling. Compared to previous work by Hollmann et al. [12], I extend the results by including a method to combine multiple relative lever arm measurements to a single dot-position, including uncertainty estimates based on Bayesian law for each measurement with numerical approximation of the non-analytical likelihood function. This likelihood function is determined for each gate combination including 3D model and measurement uncertainties. The key concept for the combined interpretation of several measurements is to accumulate the information gained from each lever arm via multiple Bayesian updates. This allows the different uncertainties arising from different gate combinations to be taken into account.

Dot Position Bayesian Estimator from Relative Lever Arm Measurements and Electrostatic Numerical Models

To determine the dot position, two preprocessing workflows were implemented for the input parameters of the Bayesian estimation. One is for the electrostatic model simulation and estimation of the impact of gate broadening by AFM imaging. It uses Comsol in combination with the Python interface "mph." The other is for automated fitting of the electron transition and determination of the relative lever arm.

Electrostatic Model and Automated Geometry Variation for Systematic Error Estimation

The electrostatic model workflow consists of two steps. First, the Comsol sample geometry and material model is generated from a ".mph"-format template file representing geometry and material properties based on the heterostructure layer definition. These parameters were chosen according to the sample provider and a geometry file from an AFM scan, which is generated with the add-in for "image to geometry" Comsol import. Precise scanning probe images would be preferred as they could reduce systematic errors of the dot position estimator. Due to suspected scanning electron microscopy charging and instability effects, our research group agreed on only non-invasive but broadened atomic force microscopy images. The gate structures extracted from these scans were reduced by the systematic difference between SEM and AFM gate feature sizes of similar samples, which is in the order of the AFM tip diameter. Secondly, a MATLAB-based Comsol wrapper is used for automated electrostatics simulation. This wrapper imports the sample template and runs the Comsol solver to extract what I call a basis set for generating potentials: One gate potential is set t,o 1 V, and all others are set to 0 V. This is repeated for all gates. This gives access to electrostatic potential solutions of the sourceless Laplace equation, linear in the gate voltages, by linear combinations of the basis set potentials. The model assumptions are identical to the previously described simulations in the dot tuning chapter, and validation details can be found in Appendix A.

Semiautomated Relative Lever Arm Estimation from 2D Charge Scans

I implemented a data analysis toolkit in MATLAB to preprocess the charge scan measurement data. All gate-pair combinations of the sample R2159A7MI were measured to enable insights into systematic errors of the method. The measurements were taken from scans with a series of more than three charge transitions, to reduce the probability of evaluating a charge trap in vicinity of the quantum dot. To ensure a stable device with a low occurrence of charge jumps interfering with signal-to-noise ratio or the correct identification of a transition, the transitions were measured weeks after the sample cooldown, days after the last global inducing gate voltage change, and within a comparatively small 200 mV 2D gate scan range. The full series of measurements was taken overnight and repeated in cases where the position of the transition changed. This excludes dot position changes and transition misidentification during the measurements. Additionally, the transition was placed centrally in the scan and the charge sensor was tuned to maximize the signal. This improves the precision of the lever arm estimation and correct detection in the automated processing pipeline. The 2D charge scan data was first mined for linear features by using the Hough transform (suggested by Simon Humpohl), which converts a binary image from Cartesian coordinates to a histogram over polar coordinates. It is an established standard technique for line detection in images sufficient for my purpose due to its computational efficiency and numerical stability (e.g., the Cartesian parametrization of a line creates numerical instabilities due to the infinite slope in the case of a vertical line, but the parameters in the polar representation of finite size images are bounded). I use the implementation provided by MATLAB, which is described in the documentation as follows: "The Standard Hough Transform (SHT) uses the parametric representation of a line: $\rho = x * cos(\theta) + y * sin(\theta)$ The origin of the coordinate system is assumed to be at the center of the upper-left corner pixel. The variable rho is the perpendicular distance from the origin to the line. The variable theta is the angle of the perpendicular projection from the origin to the line, measured in degrees clockwise from the positive x-axis. The range of theta is -90°$\leq \theta \leq$ 90°. The angle of the line itself is

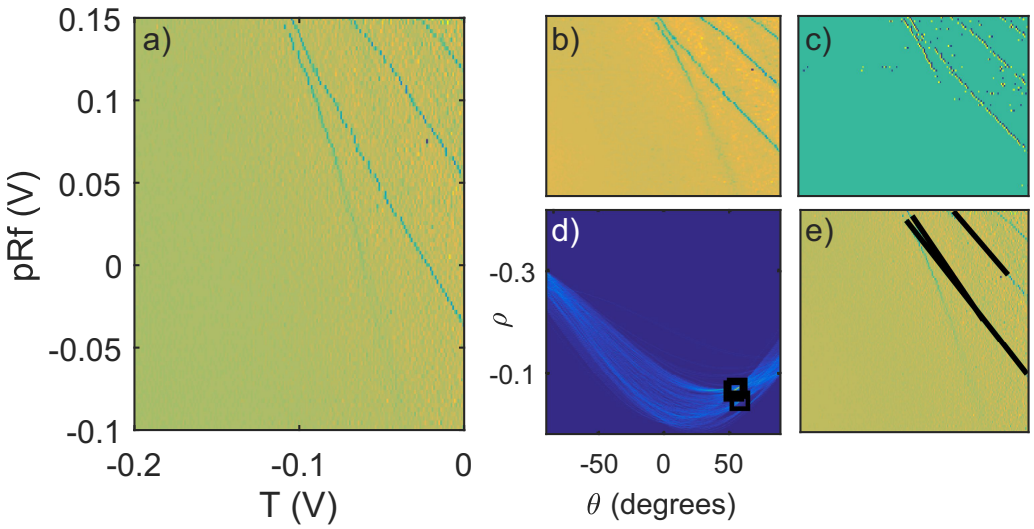

Figure 5.14.: Electron transition line detection: a) differentiated raw data, b) median filtered differentiated data, c) detected edges differentiated for jump rejection, d) Hough transform with detected peaks, e) original data with detected lines.

+90°, also measured clockwise with respect to the positive x-axis. The SHT is a parameter space matrix whose rows and columns correspond to rho and theta values, respectively. The elements in the SHT represent accumulator cells: Initially, the value in each cell is zero. Then, for every non-background point in the image, rho is calculated for every theta. rho is rounded off to the nearest allowed row in SHT. That accumulator cell is incremented. At the end of this procedure, a value of Q in SHT(r,c) means that Q points in the xy-plane lie on the line specified by theta(c) and rho(r). Peak values in the SHT represent potential lines in the input image. The Hough transform matrix, H, is n_{rho}-by-n_{theta} where: $n_{rho} = 2(\text{ceil}(D/\text{RhoResolution})) + 1$, and $D = \text{sqrt}((\text{numRowsInBW} - 1)^2 + (\text{numColsInBW} - 1)^2)$. Rho values range from -diagonal to diagonal, where $\text{diagonal} = \text{RhoResolution} * \text{ceil}(D/\text{RhoResolution})$. $n_{theta} = \text{length}(\text{theta})$" [Comment by the author: The MATLAB documentation uses MATLAB code formatting for mathematical expressions. Thus theta is an array of theta values $\theta_0..\theta_{n_{theta}}$] An additional step to determine these intersections by peak finder methods identifies the lines in panel e) of Figure 5.14.

The scope of a stable Hough transform output (panel d of Figure 5.14) requires a binary input. The following noise filter and binary transformer for edge detection was developed specifically for the 2D charge readout data, which represents electron transitions as a peak in each line of sensor current differentiated with respect to the gate voltage: Each scan line of a 2D scan was subtracted by second-degree polynomial background to filter out the non-linear sensor characteristic and telegraphic-noise-induced offsets in sensor current between consecutive scan lines (panel a of Figure 5.14). This slope reduction does not reduce the data quality regarding line detection, as the width of the lines is orders of magnitude smaller than the width of the background variations. Additionally, this background subtraction enables the application of a third-order median filter in the following step, without the risk of artificially broadening the lines due to sloped inputs to the median filter. The median filter (proposed by Simon Humpohl) filters fast and low amplitude (compared to the charge transition signal, which defines the lines) measurement noise and preserves the steps (panel b of Figure 5.14). The Sobel edge detection MATLAB routine converts the peaks into clear binary edges (panel c of Figure 5.14). The resulting data and the identified steps for configuration 2 of the sample R2159A7MI are shown in Figure 5.14. The method relies on transitions with significant transition signals (compared to the filtered background noise) and long lines (roughly 1/3 of the scan diagonal). The lines, which pass the filter stage and create clear peaks in the Hough transform are depicted in panel d of Figure 5.14. A sufficient scan resolution of 100x100 data points enabled reliable recognition of lines in panel e of Figure 5.14. The slopes of these lines give an estimate of the lever arm ratio of the two gates. After determining the lever arm ratio or relative lever arm corresponding to a gate capacitance ratio, the triangulation step translates this electric property to the geometric property of the dot position.

Synthesis of Measurement and Simulation Results for Systematic Uncertainty Sensitivity Analysis and Uncertainty Model

Before I introduce the method, which introduces the likelihood and Bayesian approach, I use the established method by Hollmann to motivate and validate the triangulation approach based on the synthesis of the electrostatic model and lever arm measurements. The first step is introducing the concept of equi-lever-arm curves, which mark positions in the 2D dot plane along a 1D curve agreeing with the observed lever arm and sample electrostatics: In the 3D simulation of the gate structure, the high conductivity reservoir's regions of the 2DEG are modeled by field-free plates at the lead potential. This assumption is valid if the 2DEG density is sufficient to screen external fields. Later on, I will evaluate the impact of this assumption on the validity of the triangulation method in numerical simulations. With this approximation, the Poisson equation reduces to the source-free Laplace equation, which is linear in the potentials applied to the metal gates. Thus it is possible to create all experimentally relevant potentials by a linear combination of potentials from the basis (abbreviated: basis potentials). The set of 2D potentials in the dot plane, where one gate is set to 1 V and all others are at 0 V in the 3D electrostatic model and iterated through all metal gates fulfills this requirement. The equi-lever-arm curves (the set of positions where the measured lever arm ratio matches the lever arm ratio of the electrostatic model) are determined by the following numerical approach: The basis potential of a gate "A" is subtracted from the basis potential of a second gate "B" weighted by the measured lever arm ratio. The equi-lever-arm curve (ELC) is given by the points at the zero-crossing and numerically implemented by using sign functions:

$$sgn_{\alpha_{i,j}}(x,y) = sgn(\phi_i(x,y) - \alpha_{i,j}\phi_j(x,y))$$

$$\delta sgn_{\alpha_{i,j}}(x,y) = sgn_{\alpha_{i,j}}(x,y) - sgn_{\alpha_{i,j}}(x+\delta x, y+\delta y)$$

$$ELC_{\alpha_{i,j}}(x,y) = \frac{\delta sgn_{\alpha_{i,j}}(x,y)}{\int_x \int_y \delta sgn_{\alpha_{i,j}}(x,y)dxdy}$$

with δy,δx the displacement by the numerical discretization increment of x,y. These lines mark the physical positions a point charge could occupy given the input parameters (e.g., the electrostatic model and lever arm measurement) are precise. The ELCs enable an initial sensitivity analysis of the different lever arm measurements with regard to the uncertainty in the reservoir geometry. ELCs are plotted for all gate combinations for gate configuration 3 of the sample R2159A7MI, where previously a transition could be unambiguously identified in all scans (Figure 5.15). This excludes measurements with global inducing gate variations as these coincide with regular charge state instabilities, which disturb and invalidate the time-intensive charge scans.

All gate pair combinations except the combination xR-xL and T-xL lead to physical solutions within the dot region. One possible explanation for the missing solution is a systematic error of the reservoir model: All combinations with gates in the vicinity of the reservoirs show large variations of >40 nm, when changing the geometry of the reservoir (see Figure 5.15). To give an upper bound on the systematic error of the lead-model-error, three models were evaluated: Model one does not have metallic plates as reservoirs, model two has reservoirs exactly up to the narrowest constriction between the gates surrounding the reservoirs - representing the two extreme cases - and model three includes an intermediate position with an 80 nm distance, that is in the order of dot distances in the devices with tunnel coupling strengths required for our measurement setup. To reduce the impact of systematic error on the result, only reservoir geometry-insensitive equi-lever-curve measurements are considered. Further sources of measurement uncertainty are the determination of the lever arm and systematic errors in the gate geometry due to the artificial broadening by the AFM tip in comparison with SEM measurements.

The artificial broadening of the gate features in the order of the AFM tip size at 20-30 nm (SEM images before the measurements were avoided to prevent possible sample charging). This systematic error was reduced by simulating a shrunken gate model. Due to geometric variations in the gate and tip topography, a remaining unknown systematic error exists. As an error for the gate model, I assume 8 nm as the difference between the designed gate width 45 nm and the 53 nm AFM scan width after AFM-broadening subtraction. Lift-

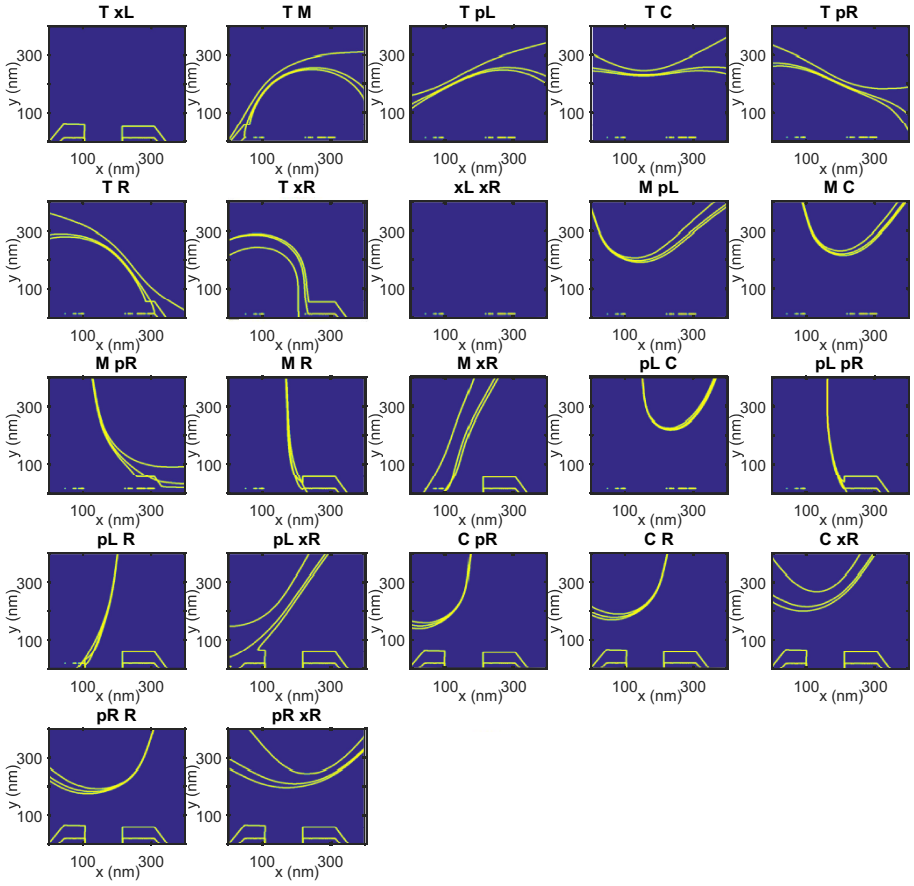

Figure 5.15.: Dot-triangulation reservoir position validation: Iso-lever-arm curves for R2159A7MI for three effective reservoir configurations ("without reservoir", "far" and "close") - "no reservoir" electron reservoirs to unfocused intersections and nonphysical solutions outside the dot region; curves are plotted with identical color to show the variations are in the order of systematic AFM tip broadening (10 nm).

off residue could further increase the uncertainty in AFM imaging. The high number of independent measurements of the lever arm will enable an evaluation of this assumption later on. These errors are included in the error propagation model by calculating the results for a shrunken and a broadened gate layout to propagate and estimate the systematic uncertainty regarding the dot position. The remaining and less significant error source is the uncertainty of the lever arm measurement. Assuming conservative errors due to the finite resolution of the 2D scan for the relative lever arms - 100x100 pixel resolution with ± 1 pixel error in the position - the errors are in the range of 1 % due to finite resolution of the charge scan. As the measurements have been taken at sufficient charge transition contrast for automated detection, far from additional transitions that introduce non-linearity and during stable operations to suppress telegraphic noise, the Hough transform identified transitions deviate insignificantly from the transitions shown in Figure 5.14, when compared to the scan resolution uncertainty. This overall conservative error estimation is assumed to achieve a first dot position estimation with the following Bayesian estimation method.

Numerical Bayesian Inference for the Dot Position Estimation

The previous method of using ELCs enables the identification of plausible dot position areas by repeating the calculation for uncertainty interval upper and lower boundaries, but it did not include statistical interpretations or synthesis across multiple measurements. Thus, in the following, I omit the ELC calculation and replace it with a Bayesian method using a non-analytical likelihood function. Based on the lever arms, basis potentials, and the error model above, creating a Bayesian estimator or posterior distribution is possible by iterative updates of a two-dimensional dot-position prior distribution. This approach is chosen because it offers a viable approach to incorporate the complex geometry, which can not be described by a closed-form expression, and the derivation of a single estimator for the dot position in the two-dimensional plane from more than a dozen measurements. Frequentist approaches like naively accumulating a histogram by sampling from the ELC curve distribu-

tion seem non-sensical as ELCs yield unphysical and inconsistent solutions far away from the intended dot positions for each get pair, which enter with the same weight as the ELC points closer to the intended dot position. A more informed weighted-means approach would require a sound approach for deriving weights, e.g., via error propagation. This is non-trivial due to the missing analytical expressions. A maximum likelihood approach would require a multivariate optimization over a sound parametrization for combining lever arm measurements. While this approach might be possible, I use Bayesian approach, which does not require an analytical form of the likelihood or explicitly defined measurement weights. I use a numeric approximation of the likelihood functions based on the previously described statistical models of the lever arm and geometry uncertainties. Due to the multiplicative updates of the prior distribution with several likelihoods, which are typically zero outside the region of interest, the ELC free Bayesian estimator is expected to suppress unphysical inconsistencies between measurements in contrast to the histogram of ELCs from several measurements. A comparison of the results with alternative approaches in the discussion section of this chapter will provide additional evidence regarding the advantages and limitations of the chosen method.

The Bayesian estimator $P(\overline{x}|\theta)$ is the probability of observing the dot at position $\overline{x}$ given the measured data θ by updates of a prior $P(\overline{x})$. The theorem of Bayes provides this posterior distribution:

$$P(\overline{x}|\theta) \propto L(\theta|\overline{x}) \times P(\overline{x}) \tag{5.1}$$

with the dot position vector $\overline{x}$ consisting of the x and y coordinate within the 2DEG and the likelihood function $L(\theta|\overline{x})$, which is a frequency function (sometimes called probability mass function, or probability up to a constant factor) depending on a model parameter θ given the realization $\overline{x}$ of a random variable $\overline{X}$. The numerically approximated likelihood function is derived as follows: The input is a statistical model representing measurement and model uncertainties based on the measurement uncertainty of the lever arm given by the charge scan resolution and approximated as a Gaussian probability density function with mean given by the measurement value $\mu_{\alpha i,j} = \alpha_{i,j}$ where the

combinations of i and j used are chosen by the experimenter and the standard deviation $\sigma_{\alpha i,j}$ as described before, the same holds for the model uncertainty of the geometry. The lever arms for a given dot position are numerically evaluated based on the basis potentials:

$$\alpha_{i,j}(\overline{x}) = \frac{\phi_i(\overline{x})}{\phi_j(\overline{x})} \tag{5.2}$$

Accumulating these inputs over one million samples for each lever arm measurement creates histograms, which assign frequencies of observing the lever arm value $\alpha_{i,j}$ to an equally distributed grid of x and y values. According to the definition of a likelihood $L(\alpha_{i,j}(\overline{x})|\overline{x})$ incorporating the abovementioned measurement uncertainties, these histograms yield a discretized frequency function when given a realization $\overline{x}$ of the discrete dot position random variable $\overline{X}$, as a function of the discrete lever arm parameter $\alpha_{i,j}$, which is well defined at the observed lever arm measurement values, thus constituting approximate likelihoods. Although this approach to creating the numerical likelihood estimates is well founded regarding the physical model describing the dependencies between dot position, geometry, and lever arms, as well as measurement and model uncertainties, further systematic model uncertainties or numerical errors can not be strictly excluded. In expectation of this, this study was conducted with far more measurements than necessary for the ideal case (two) to identify and eventually correct for potential remaining errors. The resulting likelihood estimates are depicted in Figure 5.16.

As expected, likelihood estimates with high sensitivities to the lever arm or geometry variations are broadened, especially far away from the gates (e.g., 'pR-R' in the region of 'xL'). As expected from the sensitivity analysis the likelihood estimates involving gates in the vicinity of multiple electron reservoirs are in many cases shifted outside the region of interest, and the remaining non-zero likelihoods are in close proximity to a region around (280 nm, 160 nm) or are significantly broadened resulting in a small impact on the Bayesian update. These observations support the model's validity for gate pairs away from the electron reservoirs. Before the results of the iterative Bayesian update on the prior are assessed, I want to stress the importance of this step of identifying and

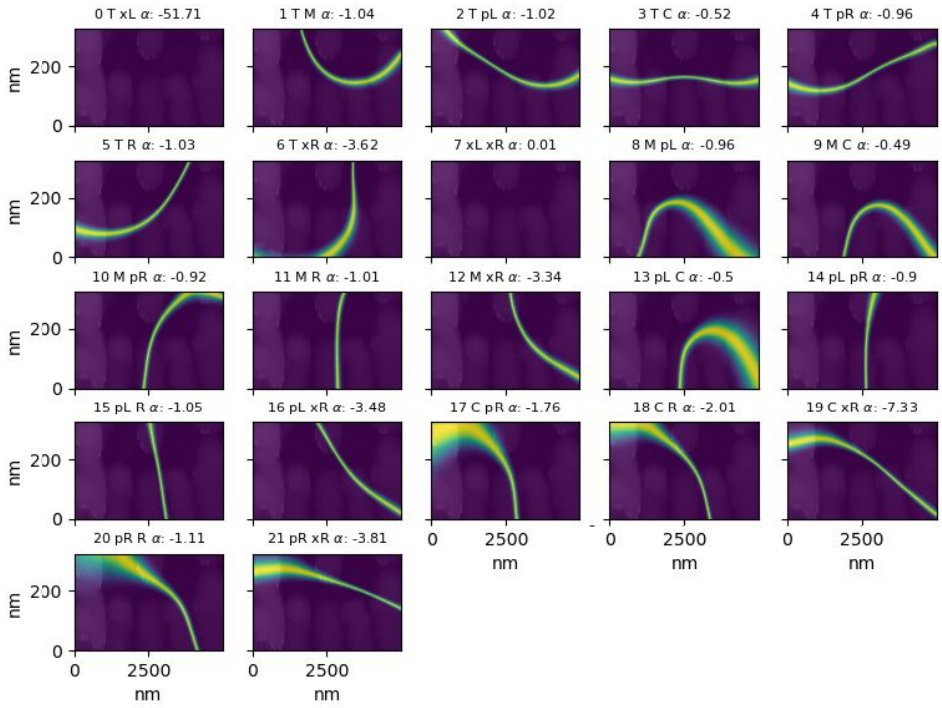

Figure 5.16.: **Likelihoods:** The conditional probability density functions exhibit broadening for measurements with high sensitivity to measurement uncertainties (e.g., for large differences in gate size) and at large distances to both gates. Gate pairs in the vicinity of multiple electron reservoirs ("xL","xR") exhibit systematic deviations (e.g., no solutions in the dot area or large offsets) as expected according to the sensitivity analysis and are omitted from further analysis.

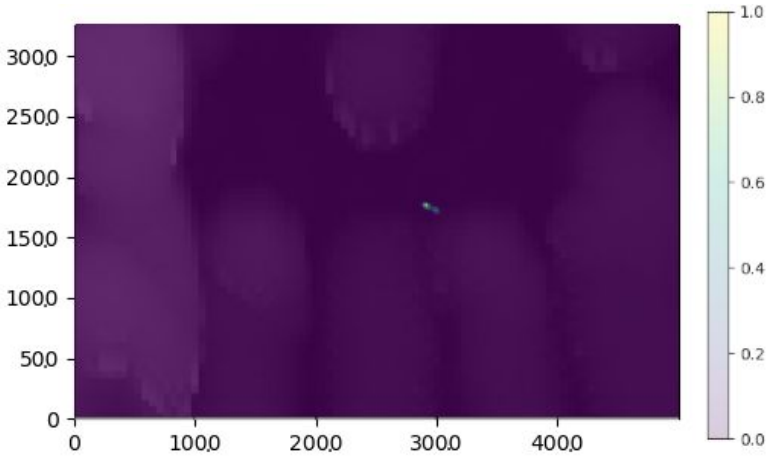

Figure 5.17.: Posterior Distribution: The posterior probability density function after Bayesian updates with all gates exhibits a non-physical multi-modal distribution due to systematic errors originating from reservoir-model uncertainties, confirming the assessment in the sensitivity analysis. In order to reduce these systematic errors gate pairs in the vicinity of multiple electron reservoirs ("xL", "xR") are omitted from further analysis.

removing inconsistencies due to systematic model or measurement uncertainties: The inconsistency created by taking into account lever-arm measurements with gates, which are very sensitive to the electron-reservoir-model-geometry-assumptions cannot be mitigated by the Bayesian model and does result in non-physical multi-modal posteriors Figure 5.18. Removing the measurements involving "x" gates based on the reasoning regarding the electrostatic model sensitivity results in single modal distributions indicating agreement with the assessment of systematic errors due to uncertainty of the electron reservoir positions and validating the conservative estimation of the error budget discussed before.

The posterior distribution, as my resulting estimation of the dot position, is determined by multiplying an equal distribution prior (over the entire simulated area) - chosen as a conservative state of no initial information and without loss of generality due to the large number of updates - by the remaining 15 likelihoods in Bayesian updates. The resulting distribution is normalized, and an estimator of likely positions is used in view of the observed lever arms and under the described model assumptions. I want to note that for simplic-

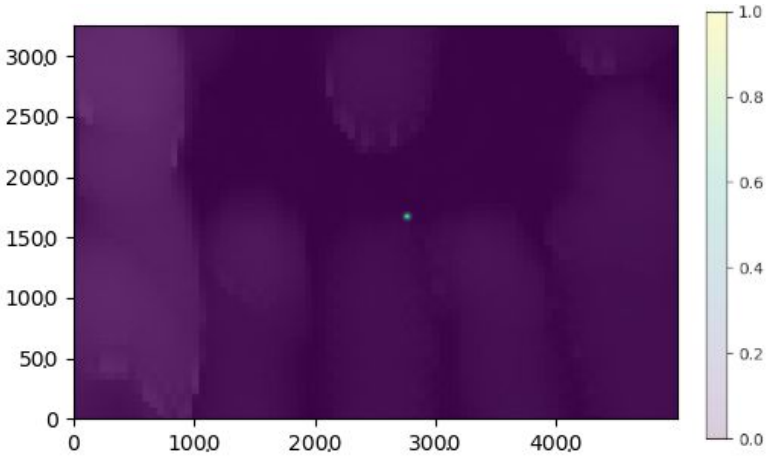

Figure 5.18.: Posterior Distribution: The posterior probability density function with an electron wave function mean (x,y)-position estimator of ($277 \pm_{stat} 2 \pm_{sys} 1$ nm, $162 \pm_{stat} 2 \pm_{sys} 5$ nm) with statistical error given by the variance of the posterior distribution and the systematic error estimated by determining shifts of the distribution due to reasonable gate size variation.

ity, we can assume the electrons are classical point particles, neglecting the spread of the wave function while still obtaining an insightful output: This output is interpretable as classical distribution arising from measurement and model uncertainties regarding the quantum mechanical expectation value of the electron's position.

The resulting posterior distribution for the dot position is depicted in Figure 5.18 resulting in a dot position mean value estimation of ($277 \pm_{stat} 2 \pm_{sys} 1$ nm, $162 \pm_{stat} 2 \pm_{sys} 5$ nm) given by the expectation x,y-values, standard deviation and a simulation of 53 nm plus and minus the systematic uncertainty of the gates (ca. 8 nm) each to propagate the systematic uncertainty. The result agrees with less precise methods of kernel density estimation based on single ELCs from the sensitivity analysis and the Monte Carlo method described in Appendix A, which does not assess the systematic uncertainty due to the geometric uncertainty.

Even with the conservative estimation of the measurement uncertainty of the dot position, the method is precise enough to support a significant deviation of the measured dot position in comparison to the potential minimum of the electrostatic simulation. The displacement of 50 ± 5 nm compared to the

minimum of the electric potential in both methods corresponds to a field of $1.8 \pm 0.2\,\mathrm{mV/nm}$ assuming a harmonic dot potential. It is greater than the electric fields generated by the metallic gates in the designs RBud3 0.165 mV/nm and ACud1 0.175 mV/nm calculated from simulations in Sushchyev [36] and a single charged defect stray field estimated by Klos et al. [78] 0.07 mV/nm at 34 nm heterostructure interface distance. Based on the analytical model of the electric field of a single charge, the resulting distance to the 2DEG can be estimated to be $10 \pm 1\,\mathrm{nm}$, with the field source placed inside the heterostructure. The interface and the oxide are outside the error margins even for 5 or respectively 10 strongly localized charges.

5.3. Setup and Sample Characterization for Qubit Readout and Control

Sample Isolation Test - Electron Temperature

Low electron temperature is a requirement for the Elzerman readout as discussed in Chapter 4. This parameter was determined by the base-temperature-dependent broadening of a charge transition measured by the charge sensor current during 1-d charge scans across the transition. The tunneling rate was chosen to be faster than the measurement rate, so multiple tunnel events probed the Fermi distribution to increase the sample size. Secondly, the transition should not be tunnel-broadened. By selecting a tuning location close to the maximum measurable 10-kHz tunnel rate, both requirements are met. The aim of these measurements is to determine a cumulative contribution of the high-frequency noise faster than the integration times of measurements as a measure of thermalization. This expands information gained on the low-frequency components by direct time trace measurements. Sweeps are performed at a maximum rate of 0.1 V/s over a small voltage range, sufficient to identify the transition but suppressing the low-frequency noise background. Typical times per trace are 100 ms and 1 kHz integration, resulting in 100 measurement points. Choosing a linear regime in the sensor characteristic facili-

tates the automation of the fitting routine.

The resulting curve (Figure 5.19) remains constant in a low-temperature interval as long as the electron temperature is limited by setup noise and ineffective thermalization and then asymptotically reaches a linear increase in the region of the dominant lattice temperature. The linear coefficient between temperature and transition width is called lever-arm α. The electron temperature can be determined by the phenomenological model that captures both asymptotic behaviors:

$$dV(T_b) = \alpha\sqrt{T_e^2 + T_b^2} \tag{5.3}$$

with dV - transition width, T_e - electron temperature, T_b - base and lattice temperature [31]. Alternatively, the y-axis offset can be converted into a temperature by the lever arm, which is determined by the slope of the asymptote.

Because of the high sweep rate, the measured single traces are comparatively noisy and occasionally accompanied by sensor tunnel events. To achieve sufficiently small errors in the final fit parameters, at least 200 scan lines per temperature were required, and an automated evaluation was required. A start-parameter-insensitive fitting algorithm was designed and implemented building on the Fit Suite wrapper by Pascal Cerfontaine. The Fit model is a Fermi-function parametrization that supports the determination of initial values from a sample scan line:

$$I(V) = (I_{amp} + \beta \cdot (V - V_0))\frac{1}{\exp{(V - V_0)/dV} + 1} + dI/dV \cdot (V - V_0) + I_{off} \tag{5.4}$$

where I_{amp} is the step amplitude, β is the difference in slope after the step, V_0 is the voltage offset of the step, dV is the width of the transition, dI/dV is the overall slope due to sensor characteristics, and I_{off} is the overall offset current.

Since any kind of averaging broadens the transition by slow electrical noise at the step position, the algorithm was optimized to adjust the original traces within parameter bounds of two orders of magnitude for the proportionality parameters and typical variations of offsets throughout the experiment (all lines, all temperatures). The evaluation function is a χ^2 function minimized by *fsolve* from the MATLAB library. In the first step, a filter omits traces with sen-

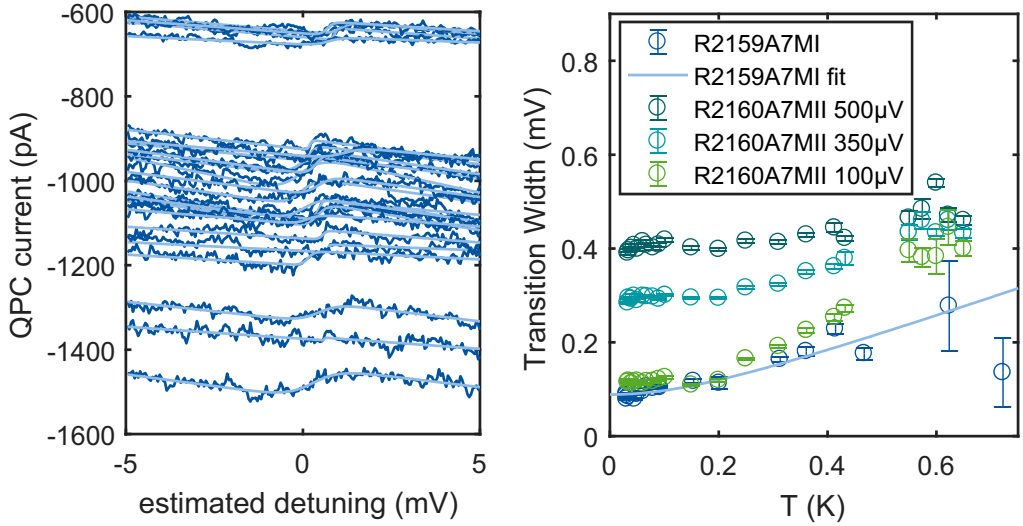

Figure 5.19.: **Electron temperature** left - results of the automated fitting for example traces of all temperatures, right - resulting transition widths versus temperature.

sor tunnel events (step jumps compared to the smoothed transition step), and traces outside the sensor's linear regime not covered by the model by comparing the current amplitude and smoothed gradient with results from the previous artifact free measurements. The resulting distribution of the transition width parameter gives the mean value and the variation of the transition for each temperature. For the sample R2160A7MII, the signals were large enough to fit all traces automatically. R2159A7MI showed a lower signal-to-noise ratio (SNR), resulting in large variations of the fit parameters. For these data, the same fit algorithm was used to determine the offsets, amplitude, and slope to normalize and average the traces for each temperature. The resulting curves were fitted using the same algorithm as before, with the extracted errors as weights (Figure 5.19). The resulting temperature is 0.2(2) K with a lever arm of 0.2(1) e for pR. This is consistent with the graphical interception point method Mueller et al. [51] results for low-biased sample R2160A7MII and R2159MI of $\tilde{2}$00 mK. This is significantly higher than in our Kelvinox setup (0.095 K) determined by Borjans [31]. Possible sources can be the coaxial lines, a less effective thermalization of the DC lines, artificial broadening by slow frequency noise,

or additional electrical noise from the pulse tubes. The broadening corresponds to less than 200 mT, which sets the lower limit for the spin readout.

Sample Charge Noise and Readout-Setup Sensitivity

We have observed in the previous passages that quantum dots show variations in positions that are influenced by the disorder. Typically, some of these defects are not static and produce 1/f-like flicker noise in transistors and quantum dots as observed by Takeda et al. [79]. These variations can lead to sudden changes in quantum dot charge states reported by Payette et al. [80], which requires the retuning of the device. The more important and limiting factor of fidelity in SiGe/Si quantum bits is the free evolutionary dephasing caused by 1/f charge noise over seven decades of frequency as reported for single qubit EDSR gates by Yoneda et al. [6]. Furthermore, the charge noise limits the fidelity of two-qubit gates that use the electron's charge for electric dipole Shulman et al. [81] or gate-controlled exchange coupling Petta et al. [82]. Finally, the overall noise of the sample and setup will limit the Elzerman readout sensitivity and the measurement bandwidth of our experiment.

Therefore, understanding and reducing the effects of defects in SiGe/Si samples is an important task to improve further the tunability, reproducibility, and fidelity of silicon qubits. Leading SiGe/Si qubit implementations, including those from Yoneda [6], are based on CVD-grown heterostructures. Our undoped MBE heterostructures are grown at lower temperatures and slower growth rates compared to CVD samples, which could lead to lower defect densities and noise levels Richmond et al. [83]. This section reports the first measurement of charge noise in these undoped MBE structures and the resulting sensitivity and bandwidth of our Elzerman readout.

The following measurements characterize low-frequency charge noise spectra by analyzing fast Fourier transforms (FFT) of the sensing dot current I_{Sensor} time traces sampled at 100 kHz. To distinguish current and voltage noise, I recorded time traces at maximum (0.5 nA/mV) and minimum (2 pA/mV) sensor transconductance (dI/dV). At minimal transconductance, voltage noise is thereby suppressed by a factor 250, which gives an estimate of the background

current noise.

At high dI/dV, the sample shows excessive $1/f^{\alpha}$ noise with $\alpha = 0.96 \pm 0.05$ up to kilohertz, which is due to potential fluctuations within the sample when compared to the low dI/dV case and the noise characteristic of the setup (Figure 4.19). Additionally, we observe an excess of current noise for both transconductance settings in the range of 1-100 kHz compared to the setup background noise (Chapter 4). Transforming the current noise into voltage noise by the transconductance shows that both curves show identical low-frequency voltage noise, which supports the correct transconductance measurement and the hypothesis of the dominant charge noise.

The RMS-voltage noise is determined by subtracting the current noise density background (low dI/dV) from the measurement of the high dI/dV. After integration, the current variance is converted into gate-equivalent voltage fluctuations, typically referred to as charge noise Buizert et al. [84]. The integration range is defined from 1 Hz as a typical lifetime to 49 Hz in literature due to setup limitations (power-line hum) Takeda et al. [79] for comparability reasons:

$$V_{rms} = \sqrt{\int_1^{49} i_n^2(f) - i_{n,BG}^2(f) df} \Big/ \frac{dI_{Sensor}}{dV_G} \tag{5.5}$$

This results in $V_{rms} = 1.8 \pm 1.1$ mV. The large relative error is due to the nonlinear sensor curve, resulting in dI/dV that variations of 60% for typical voltage variations. The RMS-charge noise matches the measurements of Borjans [31] and Takeda et al. [79] within the error range. A direct comparison with the spectrum of the sample with the highest reported fidelity in SiGe/Si heterostructures (Yoneda [6] 0.2 $\mu V/\sqrt{Hz}$) compared to $0.05 \pm 0.03\,\mu V/\sqrt{Hz}$ at 10 Hz with identical α shows a significantly lower flicker noise density in our MBE-grown heterostructures supplied by the group of D. Bougeard. This is the first reported measurement of charge noise in an MBE-grown, undoped SiGe/Si heterostructure. I would like to note that for an accurate comparison of sample fluctuations, the potential fluctuation at the quantum-dot site is the exact measure that is independent of the sample geometry. This fluctuation is determined by the gate-equivalent charge noise and the lever arm of the gate. Lever arms are typically determined by transport measurements

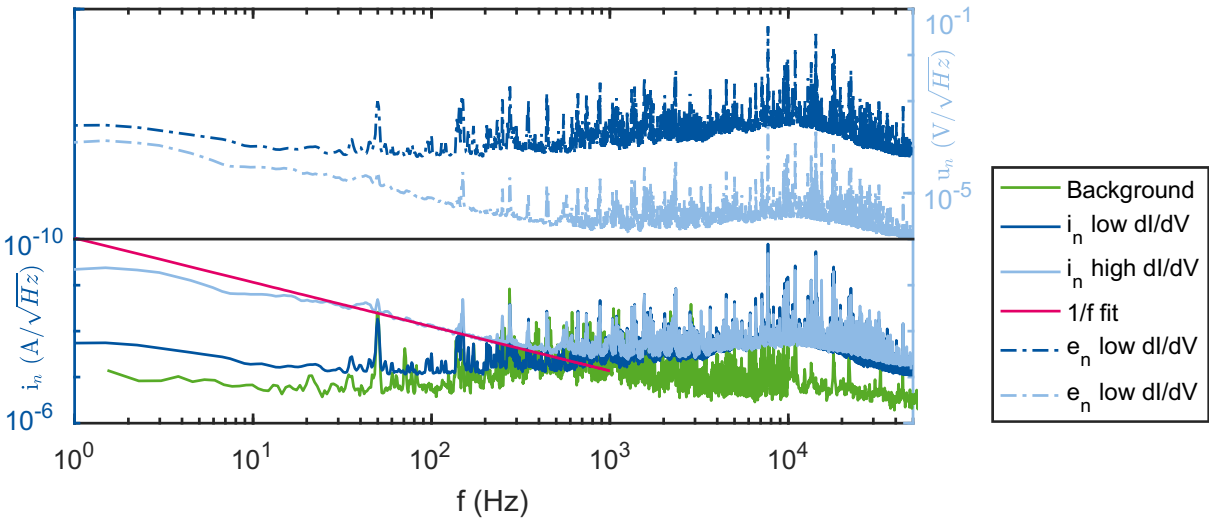

Figure 5.20.: Sample noise: continuous lines - current spectral density; dashed lines - gate-equivalent noise spectral density; magenta - $1/f^{\alpha}$ fit with $\alpha = 1.94 \pm 0.05$; green - setup background noise. The contributions in the low-frequency range increase with transconductance, indicating that charge noise is the source; the access sample noise in 1 kHz-100 kHz is transconductance-independent and points to the current noise source.

for multi-electron dots or in the context of electron temperature estimation. These measurements carry the risk of disturbing the sample tuning or cannot be performed for single electron dots. But since the lever arms in our shallow 2DEG samples (45-nm 2DEG depth) are similar or larger than in Yoneda et al. [6] with 2DEG depths (40 nm or 60 nm), the conclusions on gate equivalent noise in this chapter represent a conservative limit for comparisons of potential sample fluctuation.

Resulting electron sensitivities are determined to compare to literature-reported values by taking time traces at the single electron transition of the real-time electron tunneling and fitting two Gaussian peaks to determine the RMS current and signal strength at different setup bandwidths. This results in the SNR ratio for a given bandwidth and the electron sensitivity $(1/(SNR\sqrt{BW}))$ as given in Zajac et al. [85]. The time traces were taken for times longer than the timescale set by the 1/f corner frequency (also known as 1/f knee) To obtain a maximum SNR with fast acquisition. Integration beyond these times does not significantly improve the SNR due to 1/f-dependence

of the sample noise spectrum. The best-observed sensitivities after adjusting working points in the sensor bias and gate voltages for the highest transconductance are 2.7(0) me/$\sqrt{Hz}$ at 21.5 pA signal for the sample R2160A7MII and 11.(0) me/$\sqrt{Hz}$ at 15.9-pA signal for R2159A7MI for 1-kHz bandwidth. This is currently limited by the setup noise in the kilohertz interval, which sets the optimal bandwidth to 1 kHz, and the capacitive coupling of the sensor, which results in 10-20 pA amplitudes. Reducing the high-frequency noise to the white-noise level would rationalize using the full 10-kHz amplifier bandwidth to improve SNR or reducing the dot-to-sensor distance by using the techniques developed in Chapter 3 could increase the sensitivity to the best-reported levels for DC readout 0.8 me/$\sqrt{Hz}$ Zajac et al. [85], rfQPCs 0.6 me/$\sqrt{Hz}$ Barthel et al. [86] and below dispersive gate readout 6.3 me/$\sqrt{Hz}$ Colless et al. [87].

5.4. Elzerman Readout Test Measurements for T_1 Determination

The final step to the Elzerman readout was the setup of the Tabor-AWG and the implementation of pulse trains for the readout based on the library by Simon Humpohl. Since T_1 was expected to be in the range of 10 ms to 1 second and the Bias-Tee cut-off is 5 Hz, the tunneling rate was tuned to 1-10 ms to observe a clear spin blockade in the readout window. To avoid charging effects by the bias-tees, the average voltage of the pulse train and the readout level was set to 0 plus a pulse, the setup-dependent offset in the range of -2 to 2 mV, and the pulse-segment lengths were chosen in the range of 1-100 ms (readout bandwidth 1 kHz for best SNR). With R2160A7MII, no out-in-out events with subsequent blockade were observed up to 4 T at 350 μV sensor bias, which is required for sufficient readout contrast. This could be due to rapid relaxation in connection with valley hot spots or other relaxation channels as reported by Hollmann et al. [12]. After a thermal cycle to 3K due to the MC-temperature rise in the pre-cooling line, which left the sample unaltered in Configuration 2, R2159A7MI was tuned to Configuration 3 (increased accumulation gate voltage). A further increase of the top-gate voltage compared to Configuration 3

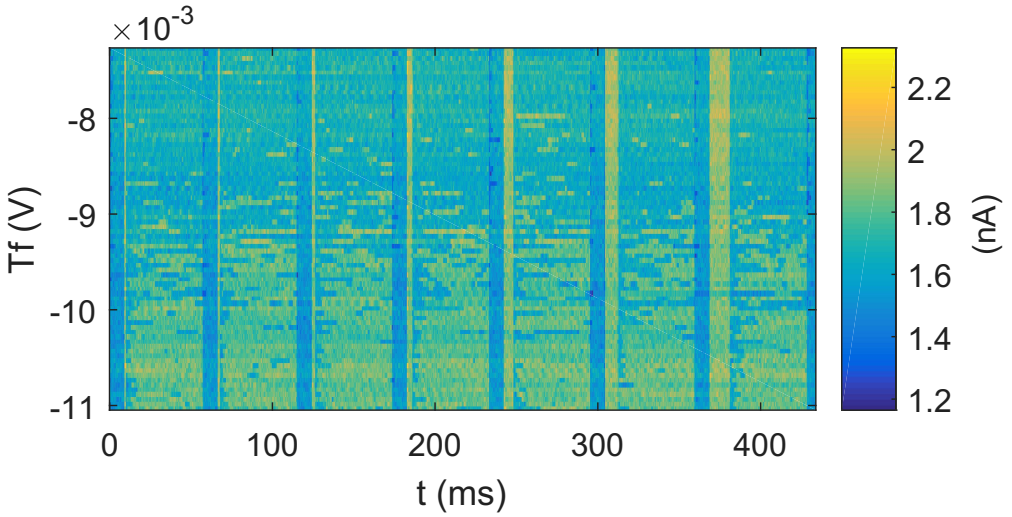

Figure 5.21.: T1 pulse train response: multiple cycles of Elzerman readout pulses (blue - unload; yellow - load; blue/yellow - read) with different load time from 2 ms to 45 ms in Configuration 3 (Figure 5.3) with out-in-out (blue-yellow-blue) signature candidates for spin-up readout events, followed by spin-down occupation and tunnel blockade.

enabled the detection of spin readout events for the previously implemented pulse trains with different load times. These measurements were performed and analyzed by Tom Struck, Arne Hollmann, and Lars Schreiber [88] with the following algorithm: Digitization of the data by line-by-line median subtraction, median filter (contrast of single peak events of >5 sample out-in-out events), 50-Hz filter based on FFT and Schmitt trigger (two hysteretic trigger levels), counting of the time-dependent up-counts resulted in the first T_1 measurement with a nanomagnet in undoped silicon-28 samples $T_1 = 35.6 \pm 0.8\,ms$, a spin-up fraction of $12.9 \pm 0.3\%$ at 1.5 T (Figure 5.22). Measurements by the same group resulted in measurements 4 T to below 0.3 T to identify dominant relaxation mechanisms in this system. These results agree with the setup design estimations, and characterization results and verify the setup's eligibility for single electron-spin physics experiments.

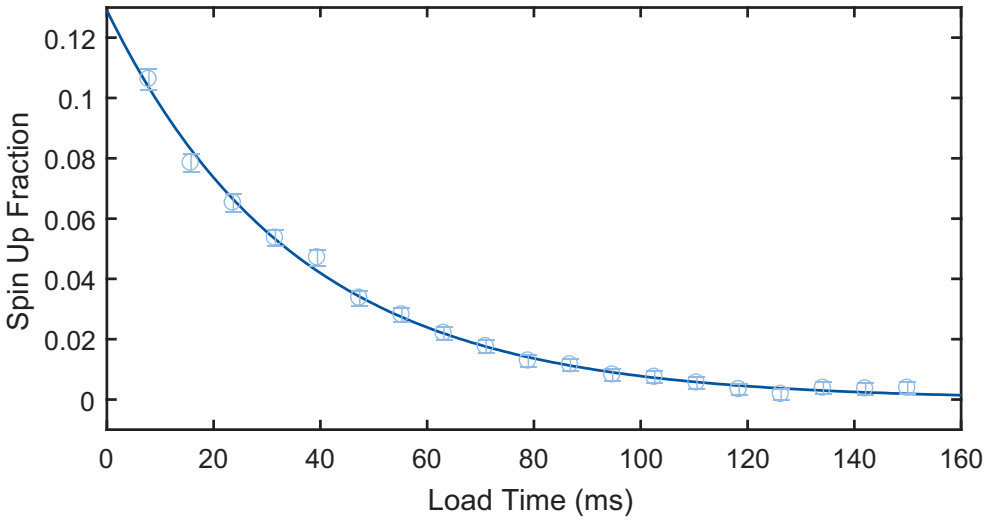

Figure 5.22.: T_1 spin decay: exponential decay of the observed spin-up fraction with $T_1 = 35.6 \pm 0.8\,ms$ and a spin-up fraction of $12.9 \pm 0.3\%$ at 1.5 T

Chapter 6.

Conclusion and Outlook

In this thesis, a measurement and control setup, silicon quantum dot samples and their fabrication were set up and optimized for Elzerman read-out and silicon spin qubit experiments like T_1 measurements with a focus on improving yield and efficient tune-up beneficial for scaling to multi-qubit systems.

The silicon quantum dot gate layout was improved by a split gate design to ensure a sufficient working range of the charge sensor and a reduced-pitch design to decrease defect numbers at dot-site by a factor of 3 for improved yield. A comprehensive study was conducted to determine limiting process parameters and generate lift-off gate patterns for 25-nm gate width and 50-nm pitch devices. This is the smallest single-layer pitch reported for silicon spin qubit devices and a basis for the realization of smaller dots or increased yield in multi-qubit devices and an increase of the number of free control parameters by two additional gates compared to state-of-the-art samples.

For the single spin qubit read-out critical thermalization of the 2DEG, I developed an integrated filter as good in cut-off and attenuation as state-of-the-art PCB metal-powder [51] at a smaller form factor for improved scalability. A copper-box-only prototype with purely capacitively coupled ports was characterized, and the attenuation-limiting effects turned out to be the interface resistance and continuous contact of the enclosing box. With copper powder, an attenuation of 60 dB at 5 GHz, 80 dB at 12 GHz, 100 dB at 35 GHz could be achieved as the basis for a second-generation integrated filter. In later experiments, our setup with these filters achieved a thermalization sufficient for Elzerman read-out at 0.3 T significantly below the intended 1 T to maximize

EDSR signal transmission.

For sample agnostic and future devices of higher complexity, I have created a small to medium-scale integration platform adaptable to different electron-spin quantum computing platforms in GaAs and Si, fast qubit-control, and high visibility across broad frequency range for resonance experiments and multi-qubit device control. The design improvements of a bias tee on interposer solution and impedance matching at interfaces result in a 12 dB attenuation between two inputs of the PCB-IP-platform at 20 GHz achieving a bandwidth comparable to PCB-only solutions, without their scalability limitations. To quantify the microstrip crosstalk- and resonance-mitigation, a new measurement method was developed for available 50 Ω equipment. Based on this, the microstrip model was validated. According to the model and assuming typical electrical properties of experimentally feasible flip-chip connections, crosstalk and resonance mitigation by microstrip lines are expected to exceed 25 dB up to 10 GHz compared to 15 dB amplification with the conventional stripline technique.

Samples tested in this thesis based on MBE grown $Si^{nat/28}$/SiGe undoped heterostructures exhibit significant variations in accumulation, pinch-off characteristics, and sensor and dot tuning voltages. I extended existing tuning protocols to track variations and identify viable samples for qubit experiments. It is worth mentioning that initially observed hysteresis < 50 mV for typical working ranges (-2 to 0.5 V for fine gates, < 4 V for accumulation gate) and sweep rates of the pre-tests did not limit charge tuning. Accumulation voltages above 4 V lead to saturation of the accumulation curve and instability in the one tested device, which is in agreement with energetically allowed tunnel events to states in the oxide or at the semiconductor-oxide interface of band-structure-simulations. By accumulation and fine gate voltage-dependent I-V characteristics, remaining variations can be traced to sample and cooldown-dependent local (on DQD, QD length scales) disorder potentials that are mobile-only at high temperatures and for high accumulation voltages. 8 samples showed no accumulation due to fabrication or setup limitations. All 7 intact samples showed accumulation during at least one cooldown and at least in the sensor or in the DQD. All functional samples could be tuned to the few-electron regime. 2 of 3 dots formed in the 3 examined samples showed a tunnel-rate

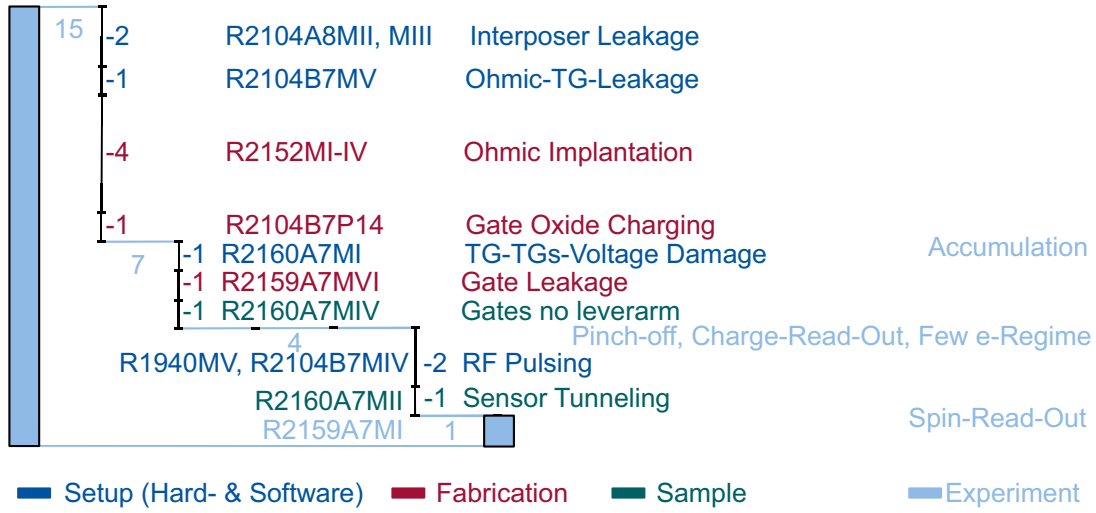

Figure 6.1.: Number of Samples reaching Tuning Protocol Steps: Number of samples and experimental steps indicated in bright blue, limitations by setup - blue, by fabrication - red, by sample - green

tunability from the sub-Hertz to 10 kHz range, sufficient for Elzerman readout. In a third dot (formed in Sample R2160A7MII), the transition width was limited by the sensor bias and preventing spin readout. The position required for this order of dot-to-sensor tunnel coupling indicates a significant shift into a typically depleted region under the fine gates.

To quantify unintentional dot displacements and support root cause analysis, I improved an existing triangulation method for gate-defined quantum dots, which estimates dot displacement and respective electric field strength, e.g., due to disorder charges. The resulting significant displacement indicates a rough disorder landscape generated by either single charges in close vicinity or multiply charged defects at a larger distance in comparison to the smooth confinement potential of the gates derived from analytical estimations and numeric simulations by Jan Klos et al. [78]. The precision of the method is in the single nanometer range. It can be further improved by replacing AFM scans of the gate geometry and resulting systematic broadening effects with an SEM scan after warming up the sample, as well as higher resolution charge scans and absolute lever arm measurements, that introduce additional measures of

absolute distance to the gates as the basis for the Bayesian approach. Based on the analytical model of the electric field of a single charge, the resulting distance to the 2DEG can be estimated to be 10 ± 1 nm, placing the source of the field inside the heterostructure for the probable case of a single or double charged origin. The interface and the oxide are only within the margin of error if highly charged or localized charged defects are expected. These findings provide empirical evidence supporting that MBE-grown Si/SiGe undoped heterostructures, sample fabrication, and the measurement setup are suitable for silicon qubit experiments and extend the foundation and direction to further improve reliability, tuneability, and fidelity of laterally defined qubits in undoped silicon heterostructures.

The measurement of low-frequency gate-equivalent noise within 10-kHz-measurement bandwidth in an MBE-grown, undoped SiGe/Si heterostructure is reported in this thesis is significantly lower in our sample than in previously reported CVD samples, which already allowed for 99.9% fidelity EDSR gates in silicon qubits. Since the lever arms in our shallow 2DEG samples (45 nm 2DEG depth) are similar or larger than in [6] with 2DEG depths (40 nm or 60 nm), the conclusion also holds for the hard-to-determine fluctuations of the electric potential at the quantum dot site.

The resulting best-observed charge-readout sensitivities achieved are $2.7(0)\,\mathrm{me}/\sqrt{Hz}$ at 1-kHz bandwidth, currently limited setup noise, and the capacitive coupling of the sensor. Reducing the high-frequency noise to the white-noise level or reducing the dot-to-sensor distance by using the techniques developed in this thesis could increase the sensitivity to the best-reported levels for DC readout $0.8\,\mathrm{me}/\sqrt{Hz}$ [85] at the time of the measurement. Later measurements by the same group performed in the interval from 4 T to below 0.3 T enabled the identification of dominant relaxation mechanisms with this setup. These results agree with the setup design estimations and characterization results, and they verify the setup's eligibility for single electron-spin physics experiments.

Appendices

Appendix A.

Dot Testing, Tuning and Sample Overview Tables

2D Pinch-offs at 30 mK

Since setup changes during cooldown bring with them the risk of disturbing the sample (some electrical equipment like DecaDAC and LockIns have up to 1-mV offset voltages on the inner/outer conductor of the output, which significantly increases the grounding level of the refrigerator), we tested the feasibility of the test for the final configuration, where the IV converter is only attached to the sensor, and all other ohmics are grounded. As shown in Figure A.1, features in the dot transport measurements are less obvious but modulate the sensor current significantly. At 30 mK, any changes to the setup can be avoided, thus reducing the risk of additional thermal cycles, while still being able to tests the gate functionality, and a starting parameter set for dot tuning can be estimated.

Single Electron Regime Tuning and Validation of Electrostatic Simulation

R2160A7MIV showed no transitions in cooldown 18 up to 4 V. R2104B7MIV, the only sample with split accumulation gates and larger dot diameter of the 'RBud2' design, could be tuned to the few-electron regime, indicated by the

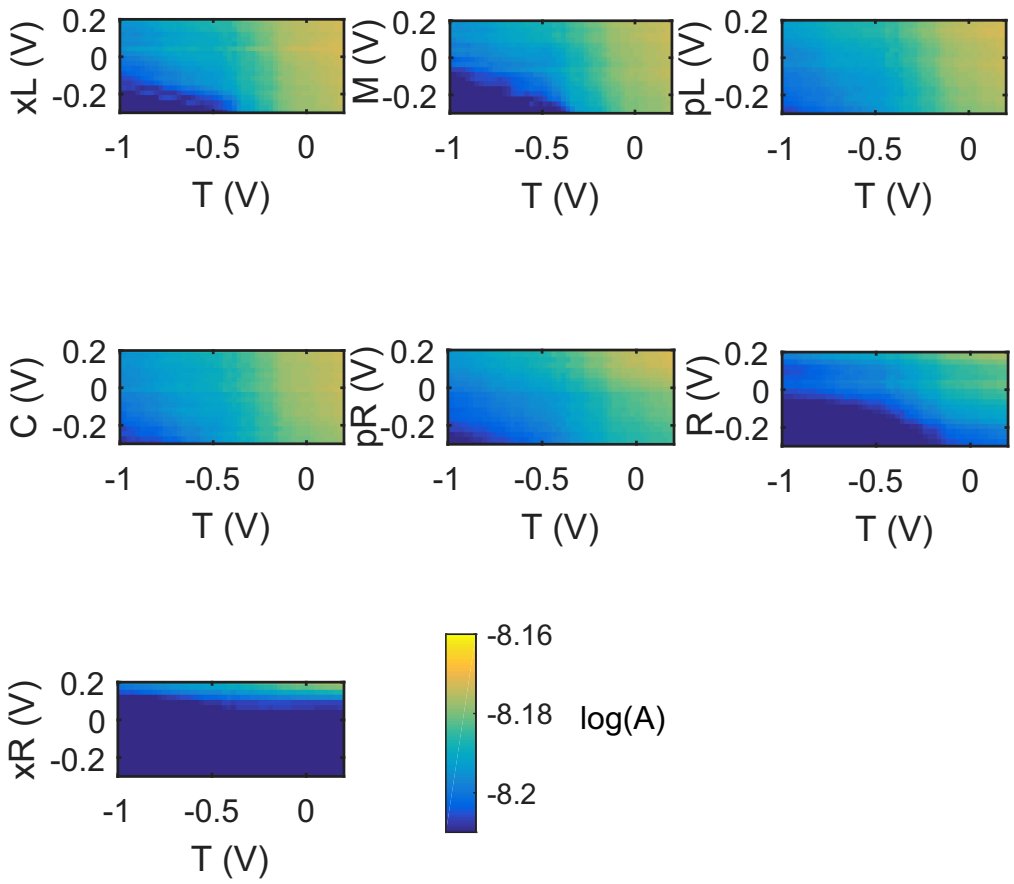

Figure A.1.: 2D pinch-off characteristics: current through ohmic IV on a logarithmic scale (6-7 nA) for sample R2159A7MI at 30 mK, 0.2 V at fine gates, 3 V at the global accumulation gate. The 6-nA current through the sensor is modulated with 1 nA through the DQD region and qualitatively reproduces the characteristics at room temperature.

lack of transitions for lower gate voltages as shown in Figure A.2 at fine-gate voltages in the range of -0.23 to 0.175 V at comparatively low accumulation voltages of 1.75 V for both gates. The occurrence of two vertical transitions does not distinguish decisively between a gate-defined quantum dot or a two-

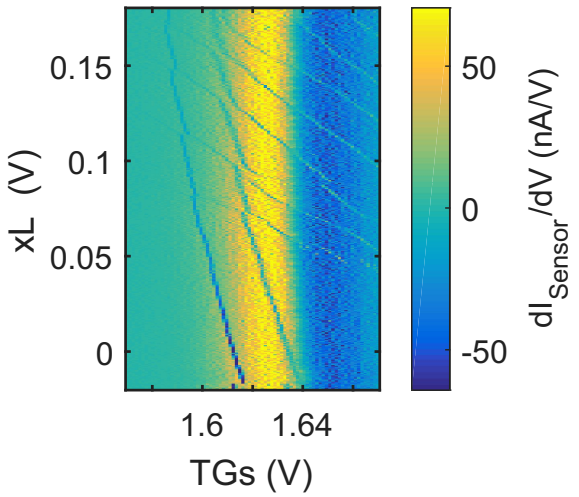

Figure A.2.: R2104B7MIV DQD Few-electron regime charge diagram for the double quantum dot system. The absence of further transitions in the charge-sensitive region of the sensor indicates a single-electron occupation.

Gate	xL	T	xR	QN	QS	R	pR	C	pL	M	TGs
Potential (V)	0.173	0.175	-0.15	-0.74	-0.23	-0.2	-0.2	0.06	0.0	0.175	1.75

Table A.1.: Gate configuration for R2104A7MIV

electron charge trap.

R2160A7MII showed double quantum dot-like features for fine gate voltages in the range of 0.15-0.5 V (Table A) near the safety limits of 0.5 V for an accumulation gate voltage of 3 V. This voltage is several 100 mV higher than the voltages for R2104B7MIV, either due to the larger dot diameter and thus higher lever arm for the accumulation gates or due to cooldown-specific charging. The bending of the lead transitions at the interdot transition and its broadening imply a tunnel coupling between close dots. Similar to the previous sample, one of the dots shows only one transition in the observed region. For voltages below 0.21 V at the R-gate, the mV-broad transitions turn into single tunneling events propagating along the sweep direction of V_{pR}. The spread increases with the reduction of V_R. This can be explained by increased tunneling times to the leads, reaching and overcoming the integration time per measuring point

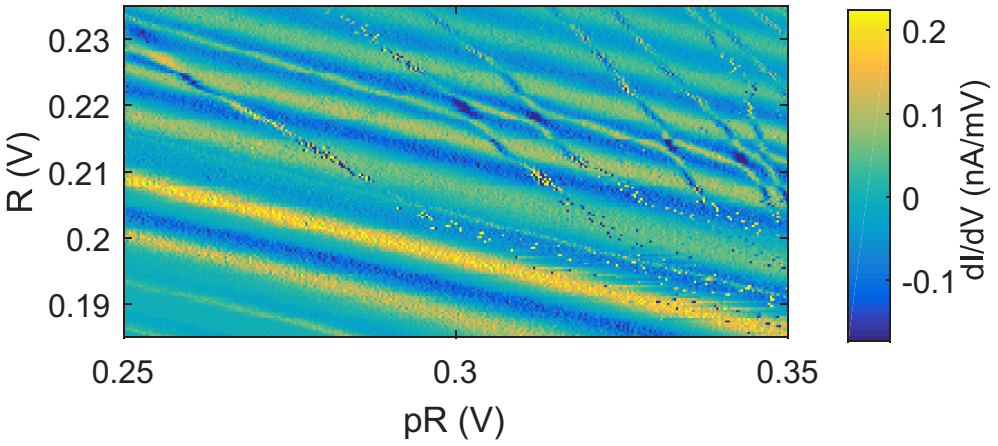

Figure A.3.: **R2160A7MII DQD Few-electron regime** charge diagram for the double quantum dot system. Variations in level spacing indicate the few-electron regime. The absence of further transitions in the charge sensitive region of the sensor indicates a single-electron occupation. A fan-out of the transitions toward the negative potential at "R" shows tunnel rates below the timescale of the measurements (20 ms).

Gate	xL	T	xR	QN	QS	R	pR	C	pL	M	TG
Potential (V)	0.3	0.3	0.15	0.5	0.4	0.185	0.35	0.2	0.2	0.3	3.0

Table A.2.: Gate configuration for R2160A7MII

(typically 10-100 ms). These features will be harnessed to control and measure the tunnel rate.

For the design used on the R2160 and R2159 wafers, the electrostatic simulation was validated (Section 5.2), and the resulting potential landscape is shown in Figure A.4 together with the electric field strength. The simulated potential suggests a single dot in the right quantum dot. This prognosis deviates from the measured double quantum dot features, indicating disorder variations on length scales below 100 nm.

Table A.3.: Overview of heterostructure- and sample-details

Heterostructure					Sample		
Doping	SiCap [nm]	SiQW [nm]	Wafer ID	Design	TG	Sensor	Device ID
doped	10	10	R1940	RBd1	global	| -	MV
undoped	3	10	R2104	ACud1		- -	P14
			R2104A8	RBud2			MII
					split	| -	MIII
			R2104B7			- -	MIV
					global	| -	MV
	1.5	12	R2152A12	RBud3	global/split		MI-IV
			R2159A7		global	- -	MI
							MVI*
			R2160A7		split		MI*
					global		MII*
							MIV*

Table A.4.: Overview of heterostructure- and sample-design parameters of samples evaluated in this thesis: Heterostructures supplied by the group of Dominique Bougeard in Regensburg varied in doping, silicon cap (SiCap) and silicon quantum well (SiQW) width, sample designs fabricated in Aachen (fine gate design: ACud1) fabricated by Bernhard Klemt based on the fabrication recipe developed in this thesis. Regensburg samples (fine gate design: RBd1, RBud2, RBud3) were produced by Floyd Schauer and Christian Neumann. Top gates designs include split gate and global gate designs. Sensor designs varied between T-shaped ($|-$) and split-gate ($--$) designs. Multiple devices are taken into account for each design parameter combination. * - Silicon-28 purified samples, gray - samples without accumulation signatures

Wafer ID	Device ID	IP	PCB	Setup	Cooldown	
					#	Date
R1940	MV	DC	v1	Hell 40 mK	1	2014-09
R2104A8	MII	AC, MS		Kurt 40 mK	4	2016-03
	MIII				3	2015-12
R2104B7	MIV	AC			6,7,8,9,10	2016-05,07,09
	MV				8,9	2016-07
R2152A12	MI-IV					2017-02
R2159A7	MI	AC, Bias Tee	v2		20,21	2017-11
				Bertha 2 K	-	2017-09
	MVI			Kurt 40 mK	20,21	2017-11
				Bertha 2 K	-	2017-09
R2160A7	MI			Kurt 40 mK	16	2017-06
	MII				14,15,18,19	2017-04, 05, 07, 09
	MIV				18,19	2017-07, 09
R2104	P14	-	-		18	2017-07

Table A.5.: Setup Configuration Parameters: Setup configurations and cool-down details for the samples evaluated in this thesis: Wafer and device ID as unique identifier; interposer type (IP): DC - gold strip-lines on silicon, AC - CPW and strip-lines on silicon, ACMS - CPW and micro-strip lines on dielectric on silicon, AC Bias Tee - CPW, strip-lines on silicon, Bias Tee on interposer; PCB version 1 and 2, Chapter 4; Setup: 40 mK Kurt (dry-system) Hell (wet-cryostat), 1-4 K Bertha; cooldowns number and date: The samples were cooled several times to allow reproducibility tests; gray - samples without accumulation signatures and leakage on interposer DC lines. Cooldowns for maintenance and revisions not depicted.

Table A.6.: Results of all cooldowns and limitations of all tested devices

Wafer ID	Device ID	Milestone	Limitation	Anomaly
R1940	MV	LD:last e-, RD: few e-*	sensor gapsize	-
R2104A8	MII	accumulation	IP shorts	-
	MIII	accumulation	IP shorts	-
R2104B7	MIV	single electron regime	RF attenuation PCBv2	R_{XI} large
	MV	-	XII TG leakage	-
	P14**	accumulation	recharging**	-
R2152A12	MI-IV	-	R_{XI-IV} large	-
R2160A7	MI	accumulation	TGb-TGs-Δ V-damage	-
	MIV	accumulation	pL, pR no lever arm	-
	MII	few electron regime	tunneling to sensor	R_{XIII} large
R2159A7	MVI	accumulation precharacterization	pR Leakage -	50 Hz noise -
	MI	Elzerman***, T_1*** precharacterization	- -	- -

Table A.7.: Wafer and Device ID of all samples evaluated in this thesis; milestones reached with the device (in multiple cooldowns); LD-left dot, RD-right dot; precharacterization - measured in 1-4 K system; * measured by Felix Borjans [31],** experiment and measurement routine implemented by the author, measurement by Bernhard Klemt, sample fabrication according to 3 by Bernhard Klemt, *** experiment and measurement routine implemented by the author, measurement and analysis by Tom Struck; gray - samples and setup damage preventing dot tuning, high-frequency operation or read-out

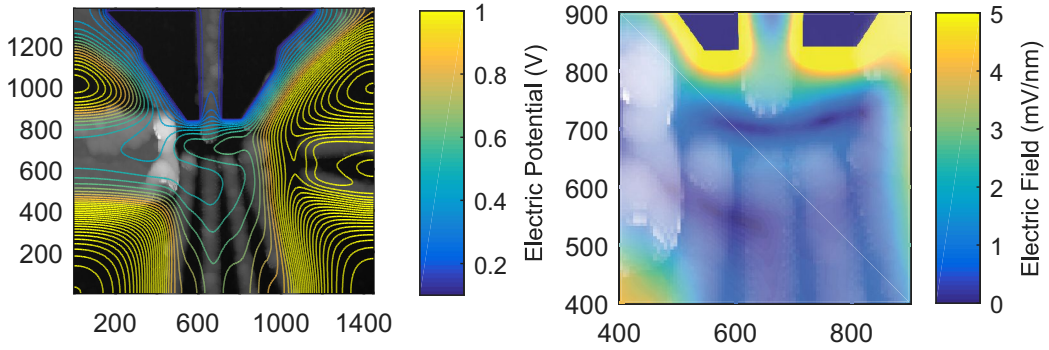

Figure A.4.: R2160A7MII electrostatic simulation: Electrostatic potential and electric field strength in the 2DEG plane for the voltage configuration in Figure A.3 predict a single-dot formation at the right dot. The ohmic position is validated in Section 5.2.

Numerical estimation of dot position

Based on the equi-lever-arm curves and the error model it is possible to create an estimator of the dot position by propagating the input data probability distributions according to the suggestions of the joint committee for guides in metrology [89]. The non-linear and non-closed-form of the ELCs described before, does not allow for the widely used analytical error propagation approach and the JCGM suggests to use the Monte Carlo method depicted in A.5 to estimate quantities of interest like the expected dot position and their uncertainties.

The input distributions are given by the previously quantified statistical properties the lever arm measurement error σ_α and the remaining broadening error σ_d on the width d of the gates. The models which transform the input distributions are the equi-lever-arm functions. The samples of the quantity of interest are numerically determined by ELC function evaluations on samples from the bi-variate Gaussian probability distribution and accumulation in a 2d-histogram in the 2DEG plane of the sample. The resulting dot position

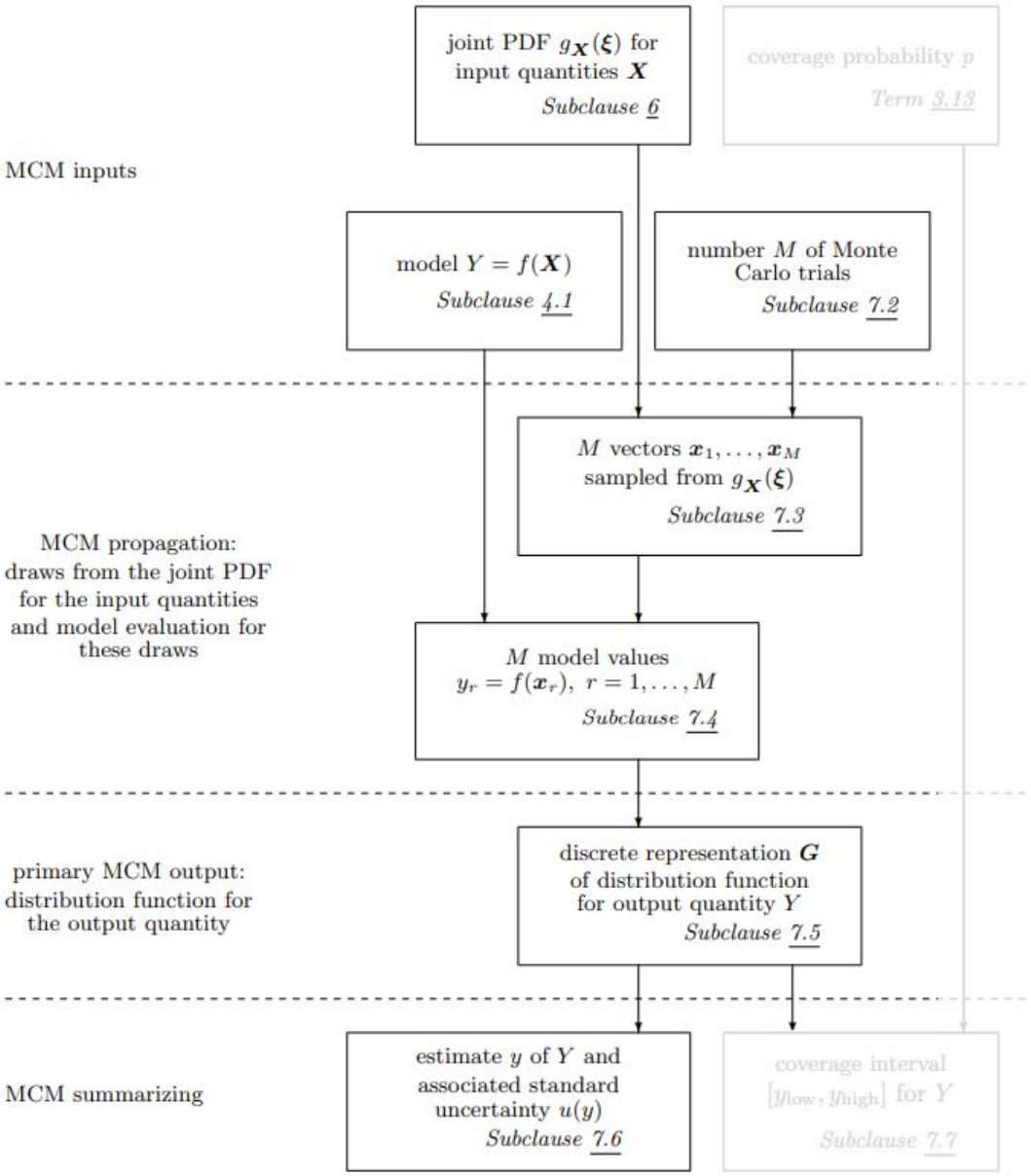

Figure A.5.: Monte Carlo Error Propagation Method: According to the Joint Committee for Guides in Metrology a valid method of evaluating the expectation value of a complex model is taking the probability density functions of the input quantities, the model which transforms these to the quantity of interest and random samples from the input quantities, to generate a discrete set of outputs used to estimate expectation values and uncertainties of the quantity of interest.

estimator is calculated by determining the bivariate expectation value of the histogram as approximation to the 2d discrete random variable frequency. It is an estimator of the expected value of the electron distribution, because the ELC's only represent relative couplings, which are invariant under symmetric expansion of the electron distribution towards the gate-pair under test. These choices create broad frequency distributions for ELC's with high sensitivity on measurement uncertainties (e.g. for lever arms of gate pairs with large differences in gate dimension or distance to dot of the involved gates), which correspond to small probability weights at positions of high uncertainty and subsequently minor shifts of the expectations value. A remaining gate dependant systematic error is the anisotropic broadening of gates due to AFM-tip shape-asymmetries and variations in gate height. This can be neglected if gate dimensions are large compared to metal grain sizes and lift-off build-up observed in SEM scans of previous samples but can be significant for varying gate heights e.g. of micromagnets.

Before discussing the results of the Monte Carlo sampling on estimator I want to stress the importance of the step of identifying and removing inconsistencies due to systematic model- or measurement-uncertainties: The inconsistency created by taking into account lever-arm measurements, that are very sensitive to the electron-lead-model-inaccuracies, is not captured by the ELC frequency distribution model and will result in estimator offsets and overestimated uncertainties. Another disadvantage of the model and the reason, why I use the Bayesian approach described in the main section is that a mathematically rigorous proof of the propagation of correlations between lever arm measurements from the geometry uncertainty is not straightforward and the method is thus unnecessarily complex and heuristic in nature. As results are in alignment with the Bayes results the approach is presented for future discussions and development.

In order to identify measurements of gate pairs with minimal systematic error figure A.6 shows error propagated histograms for all measured gate combinations. All but the one for the xL-xR gate combination cross the plausible region of the right quantum dot, where according to the gate voltage setting the minimum of the electrostatic potential should reside. This is in agreement with

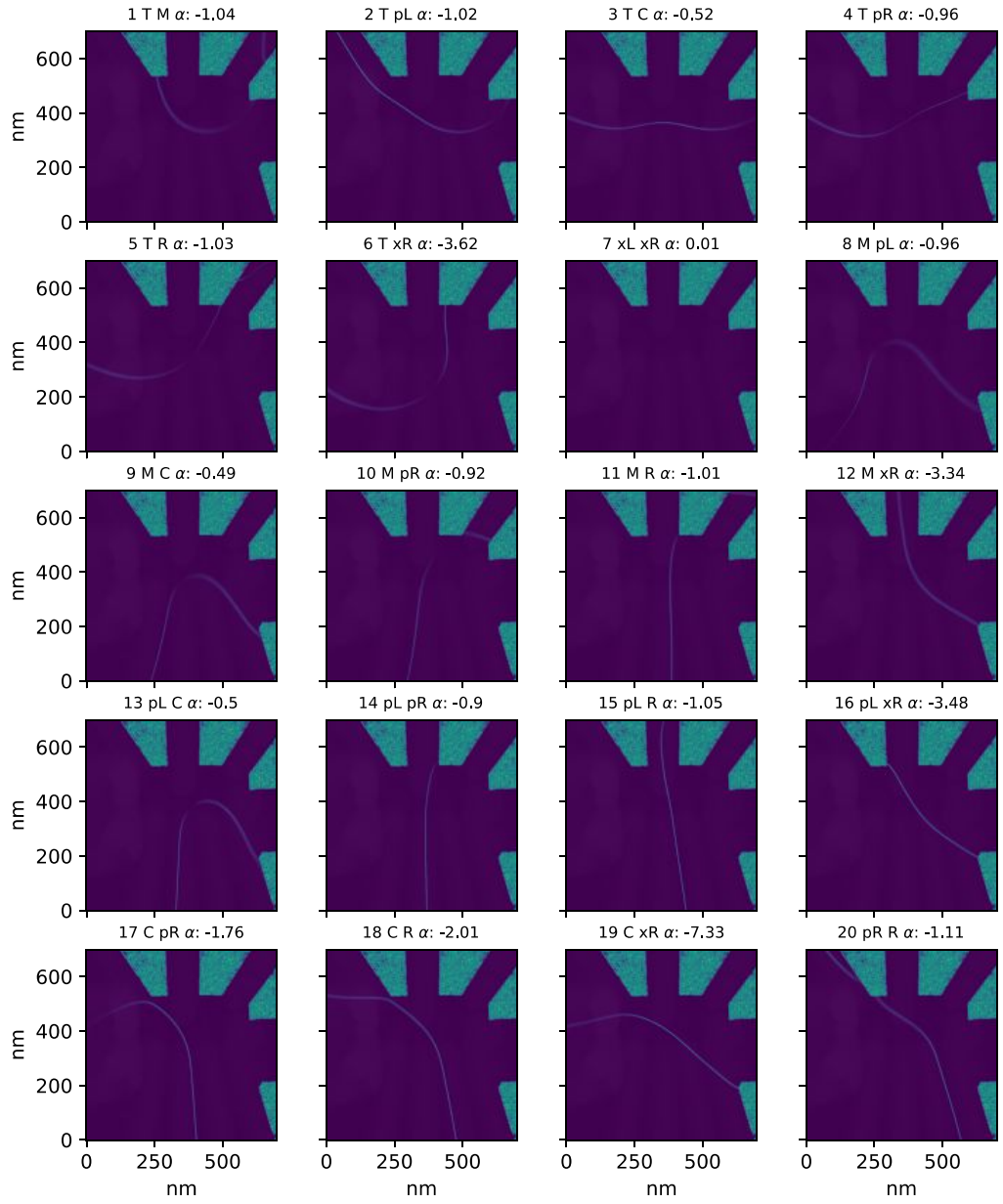

Figure A.6.: Likelihood estimators: The equi-lever-curve 2d histograms accumulated over 1000 samples from lever arm and geometry probability distributions exhibit broadening for measurements with high sensitivity to measurement uncertainties (e.g. for large differences in gate size). Electron leads appear bright as the potentials are fixed at 0 V creating additional zero-crossings in combination with numerical inaccuracies.

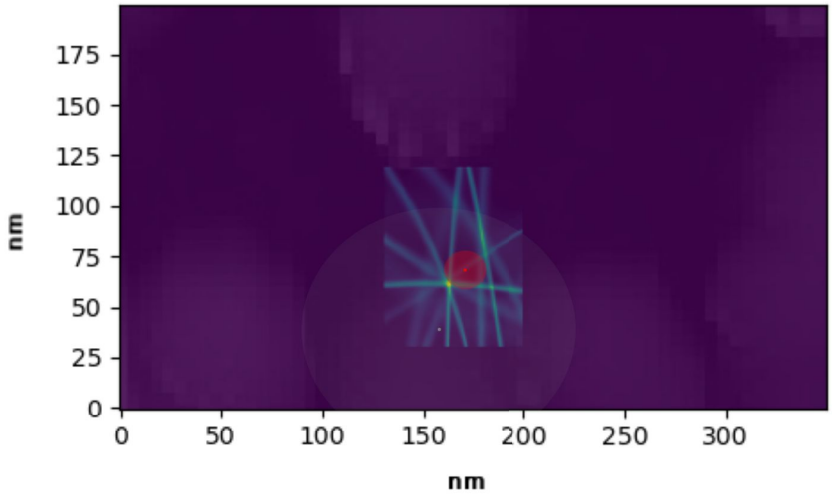

Figure A.7.: MC output histogram: These results with 100000 samples have been obtained by reducing the region of interest to 100x75 nm. Sharp frequency distributions are in good agreement meaning close proximity and displaced distributions are typically broad representing low certainty, with the only exception of pL-R. The dot position expectation value is (179 nm, 71 nm) with a standard deviation of (23 nm, 17 nm) and a correlation coefficient of -0.1 or a ca. 5 tilted covariance ellipse. The smaller sample size (1000 samples) simulation result is indicated by the gray spot and ellipse of the larger area the uncertainty is reduced by a factor of 7 and both values agree within the margin of error.

the assessment on systematic errors due to uncertainty of the electron leads positions and implies to treat lever arm measurements with gates in electron lead vicinity with caution. ELC sensitive to lever arm or geometry variations are broadened, especially for the asymmetric pairs (e.g. M and other gates), while symmetric gate pairs with similar dot distance (T,C), (pL,pR) show sharp features as expected by previous assessments. As second step of identifying systematic deviations the sum of the resulting error propagated frequency distributions of different gate pairs are presented in figure A.7. In order to reduce the sampling error by the discrete MC-method the sample size was increased from 1000 to 100000 and the sampling area was reduced to an area of interest with all crossings within the physically plausible area between the metal gates. The results in figures A.6, A.7 were created using the mathematical compilation and scan features of the Python library Theano, which reduced the runtime from several hours to a few minutes. As expected the most weight of the histograms is in close proximity (relative to their width) in a region around (170 nm, 70 nm) or are significantly broader resulting in a small influence on the estimator. One clear exception is visible for the combination pL-R resulting in a sharp feature at x=190 nm. Here the distance to the dot is asymmetric with pL being closer to the estimated dot position, while R being a significantly larger gate extending along the whole y-dimension. One reason for the systematic deviation could be the underestimation of the geometrical error due to increased broadening of the R gate in the AFM scan across lift-of residue. This shortcoming of the method could be addressed by a SEM scan of the sample at room temperature. Additionally one could include measurements of the lever arm of a single gate by coulomb diamond measurements in combinations with dot diameter estimates and thus involve estimations of the absolute distance of the dot to the gate. This would reduce the negative impact on the model histogram's variance by unphysically long tails of ELCs. As the sample was not available for new measurements I restrict the analysis to the sufficiently accurate method of using ELCs only. The resulting estimation for the dot position is depicted in figure A.7. Even with the conservative estimation of the measurement uncertainty of the dot position the method is precise enough to support a significant deviation of the measured dot position in comparison to

the potential minimum of the electrostatic simulation. The displacement of 65 ± 20 nm compared to the minimum of the electric potential induced by the gates according to the electrostatic model described previously corresponds to a potential variation in the order of 1 mV/nm assuming a harmonic dot potential. The comparison to electric fields generated by the metallic gates in the designs RBud3 0.165 mV/nm and ACud1 0.175 mV/nm calculated from simulations in [36] and the defect stray fields estimated by [78] 0.07 mV/nm at 34 nm distance indicate a rough disorder landscape generated by charges in close vicinity in comparison to the smooth confinement potential of the gates. Based on the analytical model of the electric field of a single charge, the resulting distance to the 2DEG can be estimated to be 17 ± 5 nm, with the field source placed inside the heterostructure. The interface and the oxide are not within the margin of error.

Barrier Tuning Details and Unintentional Tunnel Coupling to Sensor Leads

For the sample R2104B7MIV, 2D charge scans in the ranges TGs 1.5 to 1.75 V, xL -0.02 to 0.18 V showed no fan-out (FigureA.2), stepping L from 0.0 to -0.1 achieved a fan-out over the entire xL voltage-range indicating a strong relative lever arm of L on the barrier. This is unexpected as the L-gate is far from the expected potential barrier, indicating that local potential variations close to L create the limiting tunnel barrier.

For the sample R2160A7MII, 1D charge scans suggested high lever arms of pR,C,R. C in the range 0.1 to 0.3 V and pR in the range 0 to 0.1 V showed no transition fan-out in 2D scans, while small changes in R from 0.185 to 0.22 achieved fan-out over the entire range of pR (Figure A.3) indicating a strong lever arm of R. In contrast to the expected tunnel barrier to Lead II, the dot is likely to be tunnel-coupled to the sensor lead IV as the transition width shows a linear IV bias dependence (Figure A.8). R2159A7MI did not show this behavior, indicating that the bias dependence is not a setup- or design-specific problem but dot-specific tunneling to the leads. By changing R by

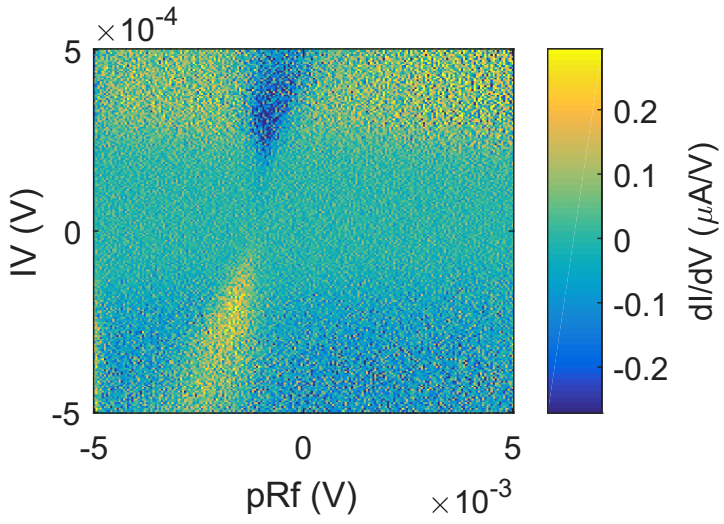

Figure A.8.: R2160A7MII Transition bias dependence: The bias dependence of the charge transition indicates heating effects or tunneling to the leads, inhibiting Elzerman readout.

10 mV and scanning pR, the measurements revealed single-electron tunneling event timescales from 100 ms to sub-milliseconds (Figure 5.13). At the higher bandwidths of the Alazar readout, the signal was dominated by pulse-tube blasts (Figure 5.13 blue features in the left plot). In the sample R2159A7MI, xR showed the expected modulation over the same timescales within a window of -0.206 to -0.134 V, i.e. a lever arm reduced by a factor of 7 compared to R in sample R2160A7MII.

Appendix B.

30 mK Setup "Kurt" Configuration and Protocols

Setup-Connection-Table, -Filter-Settings, -Characterization																	
Connection Table										Parameters&Characterization							
										(Ohm)	(kOhm)	(Ohm)	(Ohm)	(Ohm)			
Line #	FC #	Twisted Pair#	Loom#	PCB&Slot #	#FB CuP PCB	PCB/IC line #	Dot Gate	BoB	FB RCR	PCB C	IP Bias Tee	R through	R to GND Bob to FBox	R to GND Bob to FBoxend)	R to GND (BoB 2 Sample)	Function	
1	1	1	1	1	1	- -	5	1k 1nF(@mK) 1k	0 nF		-		>2E9	2.E+09	4.00E+07		
2	1	1	2	1	1	29 I	1	1k 1nF(@mK) 1k	1.2nF	-		2	>2E9	2.E+09	4.00E+07	ohmic	
3	1	2	3	1	1	40 II	1	1k 1nF(@mK) 1k	1.2nF	-		2	>2E9	2.E+09	4.00E+07	ohmic	
4	1	2	4	1	1	38 IV	1	1k 1nF(@mK) 1k	1.2nF	-		2	>2E9	2.E+09	4.00E+07	ohmic	
5	1	3	5	1	1	36 III	1	1k 1nF(@mK) 1k	1.2nF	-		2	>2E9	2.E+09	4.00E+07	ohmic	
6	1	3	6	1	1	27 xL	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
7	1	4	7	1	1	32 xR	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
8	1	4	8	1	1	25 M	35	1k 1nF(@mK) 1k	10nF	10 M		3	>2E9	2.E+09	4.00E+07	HF gate	
9	1	5	9	1	1	37 QN	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
10	1	5	10	1	1	- -	5	-	-	-	-		>2E9	2.E+09	4.00E+07		
11	1	6	11	1	1	35 QS	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
12	1	6	12	1	1	14 pL	35	1k 1nF(@mK) 1k	10nF	10 M		3	>2E9	2.E+09	4.00E+07	HF gate	
13	1	7	13	1	2	33 R	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
14	1	7	14	1	2	11 pR	35	1k 1nF(@mK) 1k	10nF	10 M		3	>2E9	2.E+09	4.00E+07	HF gate	
15	1	8	15	1	2	34 TG	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
16	1	8	16	1	2	8 C	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
17	1	9	17	1	2	- -	5	-	-	-			>2E9	short 19	4.00E+07		
18	1	9	18	1	2	30 T	1	1k 1nF(@mK) 1k	10nF			7	>2E9	2.E+09	4.00E+07	gate	
19	1	10	19	1	2	- -	5	-		-			>2E9	short 17	4.00E+07		
20	1	10	20	1	2	- -	5	-		-			>2E9	2.E+09	4.00E+07		
21	1	11	21	1	2	short 22 -	5	-		-		-	>2E9	2.E+09	4.00E+07		
22	1	11	22	1	2	short 21 -	5	-		-		-	>2E9	2.E+09	4.00E+07		
23	1	12	23	1	2	- -	5	-		-			>2E9	2.E+09	4.00E+07		
24	1	12	24	1	2	- -	5	-		-			>2E9	2.E+09	4.00E+07		
25	2	1	1	2	3	- -	5			-			>2E9	2.E+09	4.00E+07		
26	2	1	2	2	3	34 TG	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
27	2	2	3	2	3	short 27 -	5	-		-			>2E9	2.E+09	4.00E+07	short 27-28	
28	2	2	4	2	3	short 28 -	5	-		-			>2E9	2.E+09	4.00E+07		
29	2	3	5	2	3	38 IV	1	1k 1nF(@mK) 1k	1.2nF	-		2	>2E9	2.E+09	4.00E+07	ohmic	
30	2	3	6	2	3	36 III	1	1k 1nF(@mK) 1k	1.2nF	-		2	>2E9	2.E+09	4.00E+07	ohmic	
31	2	4	7	2	3	short 32 -	5	-		-			>2E9	2.E+09	4.00E+07	OK	
32	2	4	8	2	3	short 31 -	5	-		-			>2E9	2.E+09	4.00E+07	OK	
33	2	5	9	2	3	- -	5	-		-			>2E9	2.E+09	4.00E+07		
34	2	5	10	2	3	32 xR	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09			
35	2	6	11	2	3	33 R	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
36	2	6	12	2	3	30 T	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
37	2	7	13	2	4	37 QN	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
38	2	7	14	2	4	35 QS	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
39	2	8	15	2	4	11 pR	35	1k 1nF(@mK) 1k	10nF	10 M		2	>2E9	2.E+09	4.00E+07	OK	
40	2	8	16	2	4	14 pL	35	1k 1nF(@mK) 1k	10nF	10 M		2	>2E9	2.E+09	4.00E+07	OK	
41	2	9	17	2	4	29 I coldGN	1	1k 1nF(@mK) 1k	1.2nF	-		2	>2E9	2.E+09	4.00E+07	ohmic	
42	2	9	18	2	4	40 II coldGN	1	1k 1nF(@mK) 1k	1.2nF	-		2	>2E9	2.E+09	4.00E+07	ohmic	
43	2	10	19	2	4	11 pR	35	1k 1nF(@mK) 1k	10nF	10 M		3	>2E9	2.E+09	4.00E+07	HF gate	
44	2	10	20	2	4	14 pL	35	1k 1nF(@mK) 1k	10nF	10 M		3	>2E9	2.E+09	4.00E+07	HF gate	
45	2	11	21	2	4	- -	5	-	-	-			>2E9	2.E+09	4.00E+07	gate	
46	2	11	22	2	4	25 M	35	1k 1nF(@mK) 1k	10nF	10 M		3	>2E9	2.E+09	4.00E+07	HF gate	
47	2	12	23	2	4	27 xL	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	
48	2	12	24	2	4	8 C	4	1k 1nF(@mK) 1k	10nF	-		7	>2E9	2.E+09	4.00E+07	gate	

Table B.1.: DC Setup Settings Slot 1&2

	BoB		RC Filter				RC Cutoff	Function
Closed Switch	R in series	C to GND	R1	C1	R2	C2	(Hz)	Column1
1	1.00E+00	1.00E-12	1.00E+03	1.00E-09	1.00E+03	1.00E-08	7,954	Ohmic
34	8.33E+02	4.70E-08	1.00E+03	1.00E-09	1.00E+03	1.00E-08	4,065	khz Gate
35	5.00E+03	2.20E-05	1.00E+03	1.00E-09	1.00E+03	1.00E-08	1	HF Gate only if 10M Ohm at Bias tee
4	5.00E+03	4.70E-08	1.00E+03	1.00E-09	1.00E+03	1.00E-08	677	Gate, and HF Gate if 100kOhm at biastee

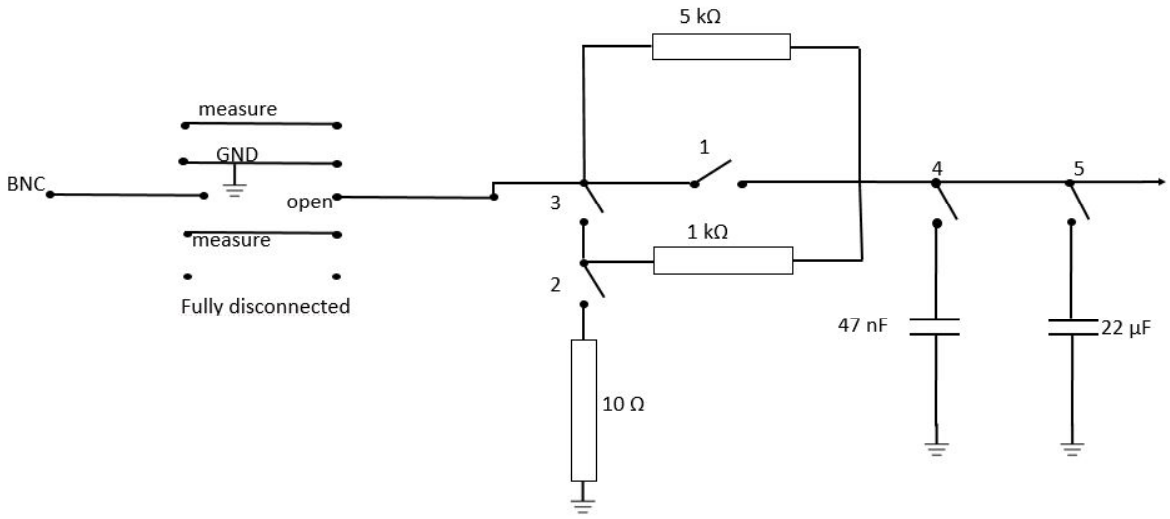

Table B.2.: Break-out-box configuration

Appendix C.

Measurement- and Control-Software-toolkit Overview

Source	Topic/Repository	Subtopic/-repo	Subtopic/-repo2	Subtopic/-repo3	Script/Function Name
Gitlab Qutech	Matlab	+comsolkit			
Gitlab Qutech	Matlab	+data_analysis			
Gitlab Qutech	Matlab	+fit_suite			
Gitlab Qutech	Matlab	+num_deriv			
Gitlab Qutech	Matlab	+simulation			
Gitlab Qutech	Matlab	+sm_scans	+kurt	+dataNPlotTools	NormPlotMultiFile.m
Gitlab Qutech	Matlab	+sm_scans	+kurt	+dataNPlotTools	pdfsave.m
Gitlab Qutech	Matlab	+sm_scans	+kurt	+dataNPlotTools	plot1DHystPinchOffs.m
Gitlab Qutech	Matlab	+sm_scans	+kurt	+dataNPlotTools	plot2DPinchOffs.m
Gitlab Qutech	Matlab	+sm_scans	+kurt	+dataNPlotTools	plotScan.m
Gitlab Qutech	Matlab	+sm_scans	+kurt	+dataNPlotTools	smDataNorm4Plot.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		Analyze2DDataLeverarm.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		AnalyzeElzerman.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		AnalyzePulseTubeAudioPowerSpectDensity.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		BarrierTune.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		ElectronTemp.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		fscanGateAlazar.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		fscanGates.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		fscanSnglGateHyst.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		NoiseSpectrSQD.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		plot1DHystScanFit.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		plot2DPinchOffs.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		plot2DScan.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		PlotMultiFileWithWildcards.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		R2160MIITuneUndopedSiDot201709.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		scanGateBufHardTrig.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		ScanScript1DHystPinchOff.m
Gitlab Qutech	Matlab	+sm_scans	+kurt		ScriptElzermanSteppedLoadTime.m
Gitlab Qutech	Matlab	+sm_scans			
Gitlab Qutech	Matlab	+sm_setups	+bertha		setup.m
Gitlab Qutech	Matlab	+sm_setups	+common		AlazarDefaultSettings.m
Gitlab Qutech	Matlab	+sm_setups	+common		install_atsaverage.m
Gitlab Qutech	Matlab	+sm_setups	+kurt		setup.m
Gitlab Qutech	Matlab	+sm_setups	+kurt		setup_qctoolkit.m
Gitlab Qutech	Matlab	+sm_setups	+kurt		setupKurtSi28.m
Gitlab Qutech	Matlab	+sm_setups	+kurt		smdata.mat
Gitlab Qutech	Matlab	+sm_setups	+kurt		startup.m
Gitlab Qutech	Matlab	+sm_setups			
Gitlab Qutech	Matlab	+util			
Gitlab Qutech	Python	qc-toolkit	doc	source	examples
Gitlab Qutech	Python	qc-toolkit			
Thesis Doc	NoiseSpectra	Kurt			DecaDACTestChannelRamp.m
Thesis Doc	NoiseSpectra	Kurt			testrampandtriggerDecaDAC.m
Thesis Doc	NoiseSpectra	Kurt			KurtNoiseSpectra.m
Thesis Doc	Dots	Accumulation			AccumulationComparison.m
Thesis Doc	Dots	DQD			Gatetuning_example.m
Thesis Doc	Dots	DQD			Gatetuning_Sample_R2160_ohmic2.m
Thesis Doc	Dots	Ohmics			OhmicsFigure.m
Thesis Doc	Dots	R1940MV			anaPwrSpctrlDnsty.m
Thesis Doc	Dots	R1940MV			EtempFitDataNormAvg.m
Thesis Doc	Dots	R1940MV			fermifn.m
Thesis Doc	Dots	R1940MV			plot1DHystScan.m
Thesis Doc	Dots	R1940MV			plot1DHystScanLinFit.m
Thesis Doc	Dots	SensorTune			ChargeReadout.m
Thesis Doc	Dots	SiGeR2160A7MITest			scanGates.m
Thesis Doc	Dots				pdfsave.m
Thesis Doc	Dots				pointcharge.m
Thesis Doc	Dots				R2159A7MI.m
Thesis Doc	Dots				R2159A7MVI.m
Thesis Doc	Dots				R2160A7MIV.m
Thesis Doc	ElectronTemperature				ScriptAnalyzeEtempFitSuite201701R1940MV.m
Thesis Doc	Filterbox	CuFilterBoxLineDesignTestCrosstalk			importfile.m
Thesis Doc	Filterbox				FBSMATestBoxVNAAnalysis2018032.m
Thesis Doc	IntegrationPlatform				TestIPBiasTeePCB_20GHzVNAS21_30mK.m
Thesis Doc	IntegrationPlatform				IPPCB_CPW_20GHzVNAS21_30mK.m
Thesis Doc	IntegrationPlatform				IntegrationPlattformVNA2018014.m
Thesis Doc	Measurement Setup				AmplifierChoice.m
Thesis Doc	NoiseSpec				AnalyzeSensorPowerSpecDensity20171002.m
Thesis Doc	NoiseSpec				SignalHist.m
Thesis Doc	Plot				TemplatePlot.m

Appendix D.

Quantum Dot Fabrication Run-sheets, Process Details

Si DQD Devices Log

10/2017

Sample Type: SiGe **Sample No.:**

Step & Process Parameters (facility)	Time & Comments
1. Sample Cut (HNF – Natalie Bruger) 1Day-1week	
Spin Coater - Protective resist	
Wafer Saw - Dice wafer into 10x10mm samples	
2. Marker Dry Etch (Optical lithography, dry etch) (HNF) 1-2 day	
CMOS WB OptLitho – Recipe: AZ5214_HNF neg. (Mask: MARKER)	
RIE 3 – Recipe: "CH1 IS Si SF6": SF6 25 sccm, 40mbar, 55mbar strike, 20°C, 50W, 7 Torr, He Backing; 0:25'→ 1000 nm (ca. 46nm/sec), check: Dektak	
Dektak check marker depth	
3. Ohmic Ion-Implantation (Optical lithography) (Jülich Mantl/Dresden) [5] 1 week- 2months	
CMOS WB OptLitho – Recipe: AZ5214_HNF neg. Implant recipe (Mask: IMPLANTATION)	
CMOS Implanter P 20keV 5E15 [cm^{-2}] 7° [4,9]	
Stripping resist - Aceton overnight	
RTP (**IHT**) : ramp 5 K/sec 700°C 15''	
4. Mesa Dry Etch (Optical lithography, dry etching) (HNF) 1-2 days	
CMOS WB OptLitho – Recipe: AZ5214_HNF pos. (Mask: MESA)	
RIE 3 – Recipe : "CH1 IS Si SF6 O2": 2'' → 100 nm Si, check: Dektak	
5. Ohmic Metallization (Optical Lithography) (HNF) 1 day	
CMOS WB OptLitho – Recipe: AZ5214_HNF neg. (Mask: OHMICS)	
CMOS WB HF Dip 30'' 1% (max. 1h time to ohmic evap due to H2 adsorption)	Ggf. 2 min for better passivation-> better contact?!
PVD PLS 570 - 5nm Ti 0.1nm/s 150nm Pt/Al 0.4 nm/s [8], Ac liftoff 5''US	
6. Depletion Gate Dielectric (Jülich – Torsten Rieger) (RWTH) 1 day-1 week	
ALD - ALD_Jülich_Template (Aceton IPA, Piranha, Al2O3 540 cycles 250°C) → 10nm	
PVD PLS 570 - 5nm Ti 0.1nm/s 15nm Pt/Al 0.4 nm/s [8], Ac liftoff 5''US	
Annealer (physics clean room) Forming gas, 350°C 15 min or higher	
7. First Fine Gate Metallization 2-3 days @ 50kV up to 1 month @100kV	
Vistec EBPG 5000plus Recipe: EbeamLitho_PMMA_100kV_HNF_Template Alternative Recipe: EbeamLitho_CSAR_100kV_HNF_Template	
PVD PLS 570 - 5nm Ti 0.1nm/s 15nm Pt/Al 0.4 nm/s [8], Ac liftoff 5''US	
8. Gates Metallization (Optical lithography (RWTH/HNF) 1 day per mask	
CMOS WB OptLitho – Recipe: AZ5214_HNF neg.. (Mask: GATESL1)	
PVD PLS 570 - 5nm Ti 0.1nm/s 150nm Pt/Al 0.4 nm/s [8], Ac liftoff 5''US	
CMOS WB OptLitho – Recipe: AZ5214_HNF neg. (Mask: GATESL2)	
PVD PLS 570 - 5nm Ti 0.1nm/s 150nm Pt/Al 0.4 nm/s [8], Ac liftoff 5''US	
9. Accumulation Gate Dielectric (Jülich – Torsten Rieger) 1day-1 week	
ALD - ALD_Jülich_Template (Aceton IPA, Al2O3 540 cycles 250°C) → 50nm	
10. Accumulation Gate Metallization (Ebeam Lithography) (RWTH!) 2-3 days @ 50kV up to 1 month @100kV	
Vistec EBPG 5000plus Recipe: EbeamLitho_PMMA_100kV_HNF_Template Alternative Recipe: EbeamLitho_CSAR_100kV_HNF_Template	
PVD PLS 570 - 5nm Ti 0.1nm/s 15 nm Pt/Al 0.4 nm/s [8], Ac liftoff 5''US	
11. Gates Metallization (Optical lithography) (RWTH/HNF) 1 day per mask	
CMOS WB OptLitho – Recipe: AZ5214_HNF neg. (Mask: MUMAGNET)	
PVD PLS 570 - 5nm Ti 0.1nm/s 150nm Pt/Al 0.4 nm/s [8], Ac liftoff 5''US	

12. Micro Magnet Metallization (Ebeam Lithography) (Jülich/RWTH) 2-3 days @ 50kV	
Vistec EBPG 5000plus Recipe: EbeamLitho_PMMA_50kV_Mumagnet	
PVD ESV2, 5nm Ti, Co 200nm, 10nm Au, Ac liftoff 5''US	
13. Device Cut (HNF – Natalie Bruger) 1Day-1week	
Spin Coater - Protective resist	
Wafer Saw - dice sample into 1.863x1.863mm devices	
14. Post fabrication anneal (RWTH)	
Annealer (physics clean room) Forming gas, 350°C 90 min	

Optional steps:
Complete oxidation of SiCap (RWTH/IHT) [5])
700°C 1-3 Min., dry process O2
Ellipsometry at sample edge
Determine Si oxide thickness (tradeoff: parallel channel vs. SiGe oxidization = > SiO2 +Ge)
(Jülich/IHT/RWTH)
Bondpad Al2O3 etch (Si-Ätzbank)
H3PO4 85% @ 55°C 1 min or RIE3 Cl2 O2

Sources:

[0] RWTH clean room procedure
[1] Electrical Characterization and Device (Schäffler Group Linz) – PhD Thesis - Sandersfeld
[2] Lateral Quantum Dots in Strained Si/SiGe (Linz) - PhD Thesis- Berer
[3] Low Dimensional Transport in Si/SiGe Heterostructures (Linz) –diploma thesis – Schmelz
[4] Eriksson Group (Wisconsin) – Jon
[5] Knoch Group (RWTH) – implantation, oxidization
[6] Lepsa (FZ Jülich) – cleaning, HF dip
[7] Materials and devices for quantum information processing in Si/SiGe - Sailer (WSI München)
[8] FZ Jülich clean room procedure
[9] Delft recipe – Walvoort, F. (2014). Fabrication and characterization of double quantum dots in an undoped Si-SiGe heterostructure.

Electron Beam Lithography Process

Date: 10.05.2016 **Sample type/no.:W2016-1M1P1-2, Y098 P1**
For Dose Test

PMMA ebeam lithography

Standard process flow	Comments
1. Cleaning: (WB 2.1 CMOS Solvent Bench);	15:00 (15 min)
1. Ultrasonic bath (Aceton, Isopropanol) each 5 min (US power: 1)	
2. N_2 blow dry	
2. Spin coating (Si Coating Bench)	15:15 (4 samples 1h; 8 samples 1.5h)
1. Preparations:	(10 min – during step 1.)
i. Prepare Hot Plates (continue with preheating)	180°C +/-1°C (dehyd.&prebake
ii. Prepare Spinner (clean with Acetone, use correct chuck, test vacuum)	
iii. Prepare Resist (warm up to RT , N2clean fill 1 ml Pipette)	
2. Dehydration:	
i. sample on clean Si wafer **180 °C for >5 min** (removes residual water)	Prog.: 180standby
3. 2x AR 639.04 (50k) spin on:	
i. Mount sample concentric; activate vacuum; **10sec N_2 clean&cool**	
ii. 1st droplet next to sample, **2 drop**letts in the middle of the sample	
iii. SolarSemi Covered Chuck Spin Coater Program **closed lid30sec 4k**	
iv. Bake at 180°C for 15 min	
Elipsometerresults: -	
~~4. Due to elipsom.rehyd. >= 5min prebake~~	
5. 1x AR 679.02 (950k) spin on:	
i. As 2.3. but bake only 5 min	
6. Clean up:	
i. Spincoater: sprinkle with Ac, clean in and outside with cr-towels	
ii. Cool Si wafer, clean with Ac and cr-towel	15 min
Elipsometer results: -	
3. Exposure: **SPL design dot 4 fields: basedose DL 1000 UL 1250 DR1500 UR 1750;** Factors: Coarse - ABCDE: 1.0*1.2^(n-1); SPL: 2.8 + (n-1)*0.18 * 5.3 -> ca.15-25mC/cm²;fine: **1 nm** coarse: **10nm stepping; 100pA , 100kV; no proximity**	
4. Development: 3 min IPA + US(power:1) @RT (2:50 US 2:55 out 3:00 H2O 3:15 2nd H2O)	
5. Evap: **PLS570 Ti 0.1 nm/sec 5nm** source pwr: 16% 43A **Pt 0.4 nm/sec 15 nm** 48% 264A	
6. Liftoff: Ac overnight, pipette flush, 2-30sec US burst power 1 , IPA rinse, dry blow	

Eidesstattliche Erklärung

Ich, Tim Leonhardt erkläre hiermit, dass diese Dissertation und die darin dargelegten Inhalte die eigenen sind und selbstständig, als Ergebnis der eigenen originären Forschung, generiert wurden. Hiermit erkläre ich an Eides statt

1. Diese Arbeit wurde vollständig oder größtenteils in der Phase als Doktorand dieser Fakultät und Universität angefertigt;
2. Sofern irgendein Bestandteil dieser Dissertation zuvor für einen akademischen Abschluss oder eine andere Qualifikation an dieser oder einer anderen Institution verwendet wurde, wurde dies klar angezeigt;
3. Wenn immer andere eigene- oder Veröffentlichungen Dritter herangezogen wurden, wurden diese klar benannt;
4. Wenn aus anderen eigenen- oder Veröffentlichungen Dritter zitiert wurde, wurde stets die Quelle hierfür angegeben. Diese Dissertation ist vollständig meine eigene Arbeit, mit der Ausnahme solcher Zitate;
5. Alle wesentlichen Quellen von Unterstützung wurden benannt;
6. Wenn immer ein Teil dieser Dissertation auf der Zusammenarbeit mit anderen basiert, wurde von mir klar gekennzeichnet, was von anderen und was von mir selbst erarbeitet wurde;
7. Kein Teil dieser Arbeit wurde vor deren Einreichung veröffentlicht.

List of Figures

List of Tables

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