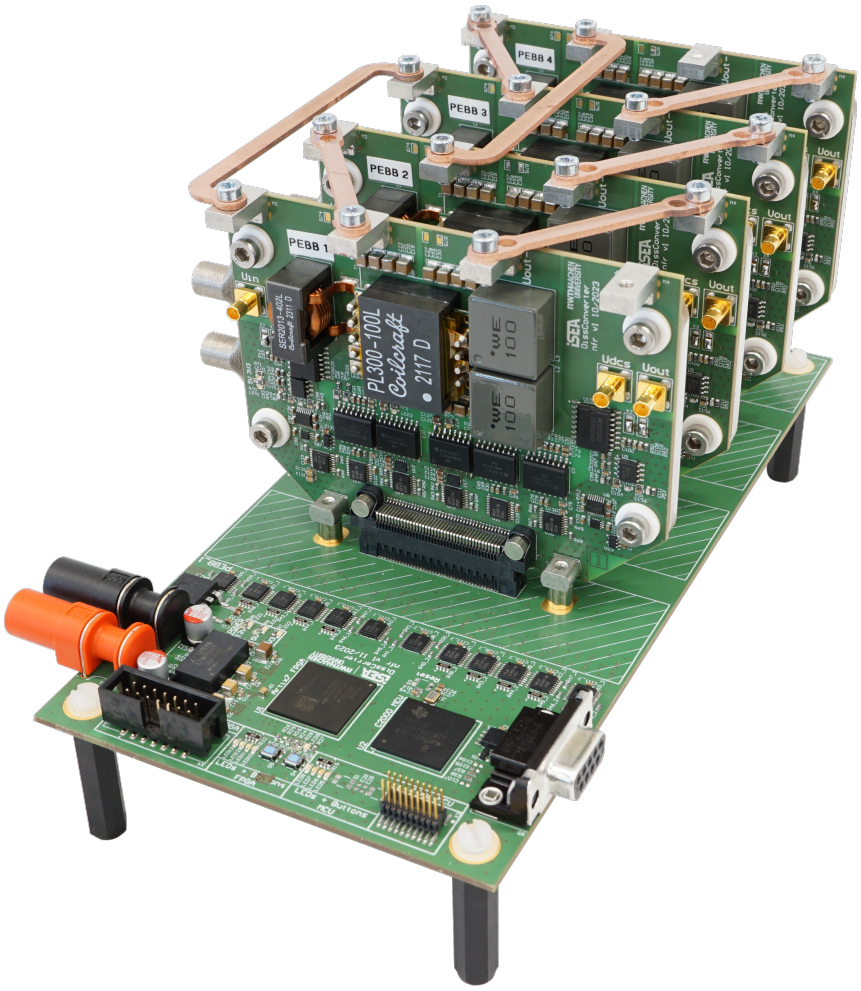
Jan Niklas Fritz

# Generalized Control Methodology for Modular DC-DC Converters




Aachener Beiträge des ISEA Band 186

# Generalized Control Methodology for Modular DC-DC Converters

**Von der Fakultät für Elektrotechnik und Informationstechnik der Rheinisch-Westfälischen Technischen Hochschule Aachen zur Erlangung des akademischen Grades eines Doktors der Ingenieurwissenschaften genehmigte Dissertation**

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Tag der mündlichen Prüfung: 19. September 2024

**AACHENER BEITRÄGE DES ISEA**
Vol. 186

Editor:
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ISSN 1437-675X

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I can live with doubt and uncertainty and not knowing.
I think it's much more interesting to live not knowing
than to have answers which might be wrong.

*Richard P. Feynman*

# Vorwort

Diese Dissertation entstand im Rahmen meiner Tätigkeit als wissenschaftlicher Mitarbeiter am Institut für Stromrichtertechnik und elektrische Antriebe (ISEA) der RWTH Aachen. Mein erster Dank gilt meinem Doktorvater, Professor Rik W. De Doncker, für die Möglichkeit einer Promotion am ISEA und das entgegengebrachte Vertrauen. Ebenso danken möchte ich Professor Antonello Monti für die Übernahme des Korreferats.

Das ISEA war für mich schon seit Studienzeiten ein großartiger Ort, an dem Zusammenhalt und Spaß ebenso wichtig wie die Arbeit sind. Für diese großartige Atmosphäre kann ich mich bei allen am ISEA und besonders der LEA-Gruppe gar nicht genug bedanken. Meinen Bürokolleginnen und -kollegen danke ich für unzählige lustige Stunden im Bahnbüro, in K128 und angrenzenden Räumen, der Skylounge und den Büros 113 und 518 im CARL. Ich danke für die Outdoor-Meetings, Wälzlagertests, Grillfeste, Doktorfeiern, Popcornsessions, Kartrennen, Klassenfahrten, Diss-Diskussionen, Quarterlys, Ringelpietze, Mittagskinos, die eine und die andere Olympiade, Kellerkonzerte, Nitro-Einspritzungen, Polsterreinigungen, Fußballfeste und insbesondere dem B12 für den gelungenen Einstieg in unzählige Wochenenden.

Ich möchte mich herzlich bei David Bündgen für die gute Zusammenarbeit bedanken. Sven Kalker danke ich für geteiltes Leid beim Schreiben unserer Dissertationen und die geteilten Pizzen. Schließlich danke ich Carsten Fronczek für den dafür notwendigen, kontrolliert aufgebauten Druck. Ich bedanke mich ebenso bei allen, die im Institut großartige Arbeit leisten, ohne die die wissenschaftliche Arbeit kaum möglich wäre, nämlich der Institutsverwaltung, den Sekretariaten, unserer Referentin, der IT sowie der elektrischen und mechanischen Werkstatt. Ganz herzlich möchte ich mich bei meinen Kolleginnen und Kollegen bedanken, die Kapitel dieser Arbeit gegengelesen haben, nämlich Paul Kowalewski, André Thönnessen, Sven Kalker, Vivien Grau, Christoph Lüdecke und insbesondere Lukas Ruppert und Rafael Goldbeck. Ein großer Dank gilt auch den Studierenden, die mich mit Abschlussarbeiten und als HiWis unterstützt haben, besonders Daniel Baggen.

Ich danke meinen Eltern ganz herzlich dafür, dass ihr mir das Studium ermöglicht habt, aber auch ganz allgemein für die Förderung und Unterstützung, ohne die ich es nicht bis hierher geschafft hätte. Meiner ganzen Familie und meinem Freundeskreis danke ich ebenso herzlich für euren Rückhalt. Schließlich danke ich dir, liebe Uta, ganz herzlich für dein Verständnis und deine Liebe.

Aachen, im September 2024 *Niklas Fritz*

# Acknowledgements

This dissertation was supported by the research project *ConverT*, funded by the German Federal Ministry for the Environment, Nature Conservation, Nuclear Safety, and Consumer Protection (BMUV) under funding code 16EM4009-2, and the research project *HyInnoLyze*, funded by the German Federal Ministry of Education and Research (BMBF) under funding code 03ZU1115AB, in the framework of the Hydrogen Clusters4Future. The responsibility for the content of this dissertation lies with the author.

The author would also like to thank IQ evolution GmbH for the manufacturing of 3D printed liquid coolers.

# Abstract

The increasing demand for power-electronic converters goes hand in hand with an increasing degree of modularity. Interconnecting existing products is often more feasible in terms of cost and time to market than developing a new product. This concept of power-electronic building blocks (PEBBs) is especially useful for galvanically isolated dc-dc converters, which can be flexibly interconnected in series or parallel. Advancing the PEBB philosophy not only benefits the suppliers, but also improves the scalability and interoperability of power electronics in general.

Despite these benefits, the modularization trend also comes with challenges regarding the control of such modular converters. Interconnecting PEBBs in series or parallel introduces cross couplings into the control loops. Hence, applying the same control methods designed for a single converter to a modular converter system instead will result in significantly worse performance. In some cases, a modular dc-dc converter system can be overdetermined, when the number of control variables exceeds the number of PEBBs, or even unstable. Solutions to these challenges have been proposed in literature, but only for specific interconnection schemes, sub-classes of topologies, control loop designs or modulation techniques.

This dissertation develops a generalized control methodology for modular, galvanically isolated dc-dc converters that ensures power sharing, control loop decoupling, and system stability. There is no restriction on the converter topology, and every possible interconnection is covered. The proposed methodology utilizes a linear transformation of the multi-converter state-space model into a coordinate system in which the cross couplings are completely removed, using the eigenvectors of the system matrices. By applying the theory by Lyapunov, also the stability of modular dc-dc converter systems is mathematically proven, even for overdetermined interconnections.

Rather than being mathematically abstract, the proposed solution is physically insightful because the found transformation matrices and eigenvectors have a physical meaning. Not only does it provide a fully decoupled system, it also inherently enables a power-sharing control and can be universally applied to any converter topology. This greatly facilitates the understanding of multi-converter systems using PEBBs and can be transferred to other power-electronic applications than dc-dc converters. Furthermore, the proposed solution is simple, robust, and easy to implement. It is validated experimentally by two case studies.

# Contents

# 1 Introduction

Climate change is the singular challenge of our generation, posing an unprecedented existential threat to humanity. More than half a century after the first observation of an increase of carbon dioxide in the atmosphere [1], the global community committed to limiting the global average temperature increase to 2 °C above pre-industrial levels in the Paris Agreement of 2015 [2]. However, as of 2022, global greenhouse gas emissions are on an all-time high [3]. Recent studies claim that the already induced emissions will cause economic damages that outweigh the costs of mitigating climate change to meet the 2 °C target by a factor of six [4]. Therefore, efforts to reduce carbon emissions in all sectors, especially power industry and transport, must be intensified dramatically.

Power electronics is the technology of efficient electrical energy conversion with low losses, high availability, high reliability, small size, light weight, and low cost using semiconductor switches [5]. Power electronics can be found at almost every electrical power interface, from 10 W smartphone chargers, which convert the 230 V alternating current (ac) grid voltage to 5 V direct current (dc), up to the converter stations of high-voltage dc transmission lines with voltages exceeding ±800 kV and power ratings beyond 10 GW. Power-electronic converters are key elements for renewable energy generation and can be found in every wind power plant or photovoltaic inverter. Moreover, the rise of electric mobility would not be possible without power-electronic traction inverters, on-board chargers (OBCs), and dc fast-charging stations [6]. The broad range of applications makes power electronics a key enabling technology in the effort of decarbonizing the world.

Hence, it is expected that the demand for efficient power-electronic converters will substantially increase. Meeting this demand will potentially pose significant challenges for the power-electronic industry. One key to handle this situation will be the modularization of power-electronic converters: the demands of a new application can be easily met by interconnecting already existing mass products to increase their current or voltage rating to the required level. This is, in many cases, more viable in terms of cost and time to market than the development of a completely new product. Also maintainability and redundancy are improved. Moreover, the partial-load efficiency can be increased by switching off some converter units, while operating the remaining ones closer to their peak efficiency. However, such efforts can only be successful when there is an easy, robust, and effective way to control modular power-electronic converters. This dissertation facilitates to exploit the benefits of a more-modular approach to power electronics by providing a generalized control methodology that can be used to improve the interoperability and hence, the scalability of galvanically isolated dc-dc converters.

## 1.1 Motivation and Background

The concept of power-electronic building blocks (PEBBs) was introduced by research conducted by the US Navy in the late 1990s [7–10]. The idea is simple — instead of relying on individual converter developments for every application, a universal building-block concept was promoted, in which a PEBB would act as a universal power processor. It would integrate the power semiconductor devices, sensors, and control hardware, it would be self-sensing the application that it is used in, and it would be flexible in performing various control tasks [10]. By interconnecting multiple PEBBs, any desired electrical power input could be changed to any desired output, regardless whether ac or dc. It was claimed that the cost benefits of high-volume production of such PEBBs would outweigh the obvious challenges that such a concept would pose [8].

Such a universal, plug-and-play approach would of course require a substantial standardization effort to ever be successful. Indeed, there have been various propositions by academia [11, 12] and even standardization efforts by the IEEE [13]. Some companies also introduced PEBB-based products in the 2000s [14]. Even today, the PEBB philosophy is explicitly mentioned in the most recent issue of the "IEEE Recommended Practice for the Design and Application of Power Electronics in Electrical Power Systems" by the IEEE Standards Association [15].

However, from today's point of view, it has to be admitted that the power-electronic industry is far from such an idealized scenario because the demand for universality is far too obstructive in terms of cost, control design, and the willingness of competitors to collaborate. Nowadays, the concept of PEBBs is interpreted in a broader fashion and mostly means taking a modular approach to the design of power electronics. This dissertation uses the term PEBB in this broader interpretation. Rather than calling for a universal power processor, any already existing product or sub-component could be used as PEBB by its manufacturer. An interconnection of such already existing products has obvious advantages over the development of a new product, namely

- lower development, engineering, investment, certification, and qualification cost,
- lower component cost due to high-volume production,
- shorter time to market,
- higher partial-load efficiency,
- facilitated re-configuration, maintenance, and repair,
- higher level of redundancy,
- and improved scalability of the product portfolio.

These benefits are known since the early days of power electronics [16] and have been applied ever since. The modular approach can be found in many stationary high-power applications, where the high system voltages exceed the voltage rating of any suitable

semiconductor technology, for example, in modular multilevel converters (MMCs) [17, 18], solid-state transformers (SSTs) [19], railway applications [20], or high-power battery storage systems [21]. But also for lower power ratings, literature demonstrates that modular, interconnected power-electronic converters can outperform single-stage designs in terms of power density and efficiency [22].

While the PEBB philosophy is attractive from the hardware point of view, it also comes with challenges regarding the control of interconnected systems. This dissertation addresses the control of modular, interconnected, galvanically isolated dc-dc converter systems consisting of multiple individual, galvanically isolated dc-dc converters connected in parallel and/or series on the input side, the output side, or both. In such systems, each interconnection scheme requires a different control design to regulate the delivered power precisely and to guarantee power sharing among the individual PEBBs. Moreover, the stability of the system must be ensured by balancing the state variables. In some cases, a modular dc-dc converter system can even be overdetermined, when the number of control variables exceeds the number of PEBBs. Even more, interconnecting multiple PEBBs to form a modular dc-dc converter system introduces cross couplings in their control loops. The use of control methods optimized for individual converters therefore often results in significantly worse performance for interconnected converters.

## 1.2 Research Objectives and Novelty

Solutions to the aforementioned challenges have been proposed in literature, but only for specific interconnection schemes, certain dc-dc converter topologies, specific control methods or specific modulation techniques. All these solutions lack the required degree of universality to truly exploit the benefits of modular dc-dc converter systems. The goal of this dissertation is to improve on the current state of the art by developing a novel, more generalized control methodology for modular, galvanically isolated dc-dc converter systems, which shall

- guarantee the independent, decoupled, and stable control of the power transfer and the power sharing in the interconnected converter,
- cover every theoretically possible interconnection variant,
- be completely independent of the converter topology and its operating principle,
- guarantee system stability also for overdetermined interconnection schemes,
- have global validity, e.g., by avoiding small-signal modeling or linearization of the control system model,
- be as simple and straightforward as possible,
- and be as physically insightful as possible.

Such a generalized concept for the control of modular dc-dc converter systems can easily be transferred to other applications and will facilitate the general understanding of modular power electronics and improve the scalability and interoperability of such systems.

## 1.3 Outline of This Work

This dissertation is structured as outlined in the following paragraphs. Each of the following chapters concludes with a short summary. Likewise, brief summaries are given at the end of every section.

**Chapter 2 — State of the Art Review:** First, an extensive literature review is provided, which discusses the existing approaches to the control of modular, interconnected dc-dc converter systems. This includes the simultaneous control of the power transfer and the balancing of the voltages and currents in interconnected dc-dc converter systems, the decoupling of these control loops, and the assessment of the system stability. This overview also highlights the limitations of the current state of the art that this dissertation addresses.

**Chapter 3 — Fundamentals:** The contributions of this dissertation rely on three different fields of research, namely control theory, linear algebra, and power electronics. While this dissertation aims to provide the most straightforward and simple solutions, some of the utilized concepts to derive them are often less familiar. Hence, this chapter compiles a toolbox of only those fundamental concepts that are immediately utilized in this dissertation, which also makes their application in later chapters more concise and more readable.

**Chapter 4 — Modeling and Control of a Dual DC-DC Converter System:** Before deriving a generalized control methodology for arbitrary interconnected dc-dc converter system, first this chapter addresses the simplest possible system, which consists of only two PEBBs. A real-world application, a galvanically isolated 200 kW OBC for a catenary truck consisting of two three-phase dual-active bridge (DAB) converters, each rated 100 kW, is used to contextualize the control tasks. After the design of current and voltage control loops for the individual converters, it is demonstrated that by the mere interconnection of the two converters, cross couplings are introduced in the control loops. A transformation matrix is proposed to transform the control variables into another coordinate system, in which the control loops are fully decoupled. Rather than being mathematically abstract, an insightful physical interpretation of the proposed transformation is also provided.

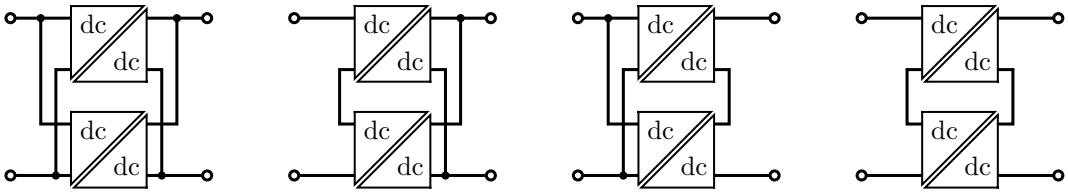
**Chapter 5 — Modeling and Control of Arbitrary, Modular DC-DC Converter Systems:** In the following, the decoupled control concept is extended to dc-dc converter systems that consist of an arbitrary number of PEBBs, of arbitrary topologies, with many different interconnection possibilities. While the considerations in the previous chapter were solely driven by physical considerations related to the target application, this chapter takes a mathematical approach, placing the found linear transformation concept on a solid theoretical foundation. After a thorough classification of the PEBB topologies and the associated interconnection variants, the transformation matrices are derived for every possible dc-dc converter system configuration. Since the decoupling concept should only be applied to either the input or output port of a dc-dc converter system, the stability of the uncontrolled port is analyzed using nonlinear stability theory. Finally, guidelines to design the control loops for an arbitrary modular dc-dc converter system are formulated.

**Chapter 6 — Experimental Validation:** Following the structure of the previous chapters, the proposed concepts for both two-converter and arbitrary converter systems are put into practice in two case studies. The special case of the decoupled control of a two-converter system as proposed in Chapter 4 is validated on the actual prototype of the 200 kW OBC for catenary trucks. To validate the generalized decoupled control methodology from Chapter 5, a low-power, modular, and flexibly re-configurable platform of four 200 W PEBBs is designed, built, and commissioned. Validation measurements are carried out for all interconnection scenarios from Chapter 5, as well as for the assessment of the system stability.

**Chapter 7 — Conclusions and Outlook:** The last chapter summarizes the key outcomes and contributions of this work and makes recommendations for follow-up research.

# 2 State of the Art Review

On the following pages, an overview of the existing literature on the control of modular dc-dc converter systems is given, illustrating the current state of the art. Literature mainly addresses interconnection variants called input-parallel output-parallel (IPOP), input-series output-parallel (ISOP), input-parallel output-series (IPOS), and input-series output-series (ISOS). For instance, IPOP interconnections of galvanically isolated dc-dc converter can be found in phase-modular on-board chargers (OBCs) [23], whereas ISOP interconnections are attractive for railway applications [24]. Figure 2.1 sketches those interconnection variants using the exemplary case of only two power-electronic building blocks (PEBBs); of course, the existing literature encompasses the extension of those interconnection variants to multiple PEBBs.




(a) IPOP (b) ISOP (c) IPOS (d) ISOS

Figure 2.1: Interconnection variants explored in existing literature

Since in any parallel interconnection, the PEBB voltages are equal, the current distribution is the critical control task, and either an active control has to be established or a passive balancing has to be ensured. Similarly, in any series interconnection, the PEBB currents are equal, and the voltage distribution between the PEBBs is the critical control task. In addition to this balancing control, also the overall power transfer of the dc-dc converter system has to be manipulable, for example through the control of the overall output voltage or current. Depending on the topology and interconnection, in many cases the number of these control tasks exceeds the number of PEBBs in the system, which poses the question how to guarantee the stability of such an overdetermined system. Additionally, in many cases the control loops that are used to achieve the aforementioned control tasks will exhibit cross coupling, which deteriorates the overall system performance.

Literature provides various solutions to the aforementioned challenges, which will be summarized in the following sections. An excellent overview of the topic is given in [25].

## 2.1 Balancing Control of Interconnected DC-DC Converter Systems

The following sections summarize the literature for the various interconnection variants from Fig. 2.1; IPOS interconnections are discussed together with ISOP interconnections.

**IPOP-Interconnected DC-DC Converter Systems** As already discussed, in IPOP interconnections, means of current sharing have to be provided. In most publications, an ideal input voltage source is assumed, and the balancing of the individual output currents is addressed. An overview of such control methods is given in [26]. On the one hand, droop methods can be implemented, which adjust the output voltage based on the load current in every individual PEBB, providing a virtual output impedance that balances the individual currents. Such a method is refined in [27] by implementing a piece-wise linear droop characteristic. On the other hand, active current sharing methods can be employed by providing centralized or decentralized control loops to balance the currents, resulting in many possibilities with their individual advantages and disadvantages [26]. For example, [28] proposes a master-slave control, in which one PEBB controls the power flow and the others control the current sharing. Master-less approaches also exist, for example through the implementation of a Gyrator behavior for the paralleled PEBBs [29]. Purely passive balancing mechanisms are reported in [30], which are however only available for specific topologies and modulation strategies. Apart from these classical approaches, also nonlinear approaches are suggested, for example using synergetic control [31] or communication graphs [32].

**ISOP-Interconnected DC-DC Converter Systems** For ISOP interconnections, the input-side balancing of the voltages as well as the control of the overall transferred power must be achieved. Since dc-dc converters are power-conservative, it is shown in [33] that achieving input-side voltage sharing implies achieving output-side current sharing. To achieve input-side voltage sharing, many concepts have been proposed.

Literature [34–36] proposes a purely passive "common duty ratio control" in which the input-side voltages are automatically balanced when applying the same duty cycle to all PEBBs. The naming already implies that this method is restricted to topologies using pulse-width modulation (PWM); in the case of [34, 36], flyback converters, and in the case of [35], phase-shifted full-bridge (PSFB) converters. Expanding this idea to dual-active bridge (DAB) converters, [37] shows that a passive "common phase shift" control can yield stable operation, however [38] shows that this balancing is quite weak. Hence, all purely passive methods rely on certain topology sub-classes or modulation strategies.

The alternative is an active control of the input-side voltage sharing. In [39], a proportional regulator on the input voltages is used to adjust the duty cycle command to

ISOP-interconnected PSFB converters. Literature [40] proposes a three-loop control structure, in which each PEBB has a cascaded control loop closed on its input voltage, with the inner loop controlling its output current. Additionally, a common output voltage controller manages the power transfer. Already, more control loops than PEBBs are present in the system, and it is explicitly mentioned that these control loops will interact; however, a stable system performance is achieved using flyback converters. An improvement of this method is made in [41] by selecting proper input midpoint voltage references. This method is widely used, one of many examples being [38], which implements the method for three-phase DAB converters, adding bidirectional capability. Instead of the three-loop control, [42] uses a master-slave control of forward converters with one PEBB controlling the output voltage and the other PEBBs balancing the input voltages.

In addition, droop-based approaches can be used to achieve input voltage sharing: If the output voltage of each PEBBs increases linearly with the input voltage, this behavior balances the input-side series connection [43], which is called positive output voltage gradient (POVG) control. This approach is also proposed in [44] under the name "inverse droop control". It can be implemented for various topologies, with [45] demonstrating it for the three-phase DAB.

ISOP systems have been extensively researched, and this overview cannot be exhaustive; [25] provides an excellent overview of the control of ISOP-interconnected dc-dc converters. The mentioned literature mainly relies on linear control theory; however, also nonlinear approaches have been proposed, such as hierarchical sliding-mode control [46] or even deep reinforcement learning [47, 48]. A pragmatic approach is the use of dedicated voltage balancing hardware as shown in [49], for example, which is however cost-intensive.

**ISOS-Interconnected DC-DC Converter Systems** In ISOS systems, the voltages of the series-connected PEBBs need to be balanced. Similar to ISOP systems, some purely passive, self-balancing mechanisms have been reported for single topologies and modulation strategies. In [50], an ISOS interconnection of flyback converters is reported to be stable by utilizing continuous conduction mode (CCM) operation for one PEBB dictating the power transfer and discontinuous conduction mode (DCM) operation for the other PEBBs, which evens out the voltage distribution. This gives the approach a master-slave characteristic. Similarly, [51] demonstrates that an ISOS interconnection of PSFB topologies can be stable without active control.

Naturally, also actively controlled approaches have been reported. For example, [52] adopts the three-loop control and applies it to an ISOS interconnection of two flyback converters, controlling the input voltages. In [53], a cascaded control approach is proposed to actively control the output voltages of an ISOS interconnection of PWM-based converters, and [54] proposes a master-slave control to balance the output voltages of an ISOS interconnection of forward converters. Finally, the feasibility of the POVG principle is also demonstrated for an ISOS system in [55]. Further insights are given in [25].

In summary, there is a vast number of publications addressing the balancing control of various dc-dc converter interconnections. Excellent overview papers are [26] for IPOP interconnections and [25] for all interconnections involving a series connection.

## 2.2 Control Decoupling in DC-DC Converter Systems

Most balancing control approaches from the previous section rely on individual, probably cascaded control loops for each PEBB. Already [40] acknowledges that those control loops will interact and may yield unwanted behavior.

In [33], a systematic picture of such interactions is developed for various interconnection variants of PWM-based topologies, and a decoupling branch is proposed that can either be added to a single PEBB or distributed over all PEBBs, eliminating the interactions between the power transfer and the balancing control. Also [56] addresses this topic for an ISOP interconnection of PSFB converters; it is demonstrated that the interactions are represented by fully occupied state-space matrices. By adding a similar decoupling branch as in [33] to one PEBB, implementing a master-slave-type structure, the decoupling of the control loops is demonstrated. Even more, this decoupling of this very specific dc-dc converter system was expressed as a linear transformation matrix, inspiring the generalized, direct use of linear transformations in this dissertation.

In [57–59], this approach is expanded to the ISOP interconnection of DAB converters, however, using linearized system models because the control directly acts on the modulation variables of the PEBBs, which influence the individual power transfer in a nonlinear fashion. Authors in [60] further improve on this by calculating the modulation from a given current command beforehand, which makes it possible for the closed-loop controllers to manipulate currents, which yields a linear system behavior and improved system responses. This idea is common in DAB converters and will be further discussed in Section 3.3.1.

In summary, the publications listed in this section accurately describe the interactions that arise between the control loops in interconnected dc-dc converter systems and propose add-on decoupling approaches that successfully compensate those interactions. In [56], this decoupled control is described using a linear transformation. It is also observed that with additional decoupling branches, the system decoupling reflects in diagonalized system matrices [57]. This dissertation picks up on these insightful results, generalizing these concepts for arbitrary topologies and providing a detailed mathematical context.

## 2.3 Stability of DC-DC Converter Systems

It is the very nature of dc-dc converters that they are power-conservative. Since a single converter can only influence one independent electrical quantity, either at its input or output side, the other side behaves like a constant-power element, either a constant-power source (CPS) or a constant-power load (CPL). These elements are inherently nonlinear, which poses some difficulties in assessing the system stability, especially for interconnected converter systems. Utilizing constant-power elements was the result of early efforts to develop canonical-form models for all possible PWM-based dc-dc converter topologies [61], leading to the introduction of CPS and CPL elements in [62]. All these techniques have been later compiled into textbooks, e.g., [63]. Nowadays, constant-power elements are essential for the modeling and stability analysis of dc microgrids [64, 65].

It has already been discussed that in modular dc-dc converter systems, there might be cases in which the number of state variables exceeds the number of PEBBs, resulting in an overdetermined system. In such cases, it has to be analyzed which state variables can be left uncontrolled without compromising the stability of the system. Many publications address this question and come to the conclusion that the state variables at the power input side of the dc-dc converter system are unstable and require a closed-loop control, whereas the state variables at the power output side of the dc-dc converter system are stable and can be left uncontrolled. Early examples of this rule of thumb are [39, 52], which are used in this dissertation as well. Also [41, 66] discuss the potential instability at the power input side of an ISOP interconnection due to the presence of a CPL, which is characterized by a negative differential resistance. The same result is found by [56] by analyzing the system equations of ISOP-interconnected PSFB converters, making the instability at the input side plausible. Finally, [33] makes more general statements about the stability of all interconnections from Fig. 2.1 by graphical analysis, formulating the aforementioned rule of thumb.

Moreover, mathematical stability evidence is provided. In [53, 67], linearized small-signal models of modular dc-dc converters are derived and classical approaches such as the Nyquist or the Routh-Hurwitz criteria are verified. Impedance-based stability analysis is carried out in [45, 68, 69], which also works with linearized models. More complex stability assessments are carried out in [70] for IPOP interconnections and in [71] for an ISOP system without decoupling.

In summary, literature has assessed the stability of modular dc-dc converter system by stating the rule of thumb that the state variables at the power input of the dc-dc converter system tend to be unstable, while the state variables at its power output tend to be stable. This claim is supported by convincing arguments or stability analysis of the linearized small-signal system models. However, a rigorous, large-signal, mathematical stability proof, which accounts for the nonlinear nature of the constant-power elements in the system models, has not been found.

## 2.4 Summary

The control of modular dc-dc converter systems has been extensively researched, mainly using the interconnection variants shown in Fig. 2.1. The goals are the control of the power transfer, as well as the balancing control of voltages in series connections and currents in parallel connections. Meanwhile, the cross couplings between these control goals have to be mitigated and the stability of the system has to be guaranteed. All these issues have been addressed in literature, and good overview papers are [25, 26, 33, 66].

The majority of the discussed publications addresses the control of modular dc-dc converter systems with a specific interconnection variant, a specific topology or topology sub-class, or a specific modulation strategy; many assume ideal power sources at the input side or resistive loads at the output side. Meanwhile, these publications often make general claims, e.g., a generalized control strategy for ISOS systems in [53], whereas it is only viable for buck-derived converters. Moreover, topologies with an input capacitor may behave differently in a series connection than topologies with an input inductor, however those differences are rarely pointed out explicitly. All this leads to contradictory statements about the decoupled control or the stability of some interconnection variant at first sight because the dc-dc converter topology and the system interconnection are rarely separated. Instead, most approaches have a bottom-up characteristic, developing a decoupled control for a certain interconnection of a certain topology, and then generalizing the approach, without properly stating the associated limitations.

A further trend in the discussed publications is that in many cases, such as the widely used three-loop control from [40], more control loops than PEBBs are provided, mostly forming cascaded control loops. Although providing many control loops to address all control goals in the modular dc-dc converter system evidently works, such pragmatic approaches often neglect the underlying physics of the system. The philosophy should rather be to base the design of the closed-loop control on a thorough physics-based modeling of the system.

Publications that are taking a top-down approach, starting from a general point of view, are much rarer but considerably more insightful. Publications [33, 66] take very systematic approaches to the control of modular dc-dc converter systems and provide very insightful statements about the system stability and the control requirements. Still, they rely on PWM-based converter topologies and linearized small-signal models.

This dissertation aims to further clear the picture, taking a systematic top-down approach, which requires the rigorous separation of the control of the PEBB topology and the control of its interconnection. Therefore, a level of abstraction needs to be introduced, classifying the PEBB topologies and condensing their behavior into generalized equivalent circuits. Such efforts have been made already in literature [72]. Furthermore, every consideration in this dissertation will be based on the physics of the system, which makes the derivation of decoupled control approaches much more insightful and less complicated.

# 3 Fundamentals

This chapter intends to compile the fundamentals, which are needed for the derivation of the generalized control methodology for modular dc-dc converters and its experimental validation. The selected fundamental concepts are summarized relatively concise and no claim is made for them to be complete; on the contrary, basic knowledge in control engineering, mathematics, and power electronics has to be assumed. Instead, the focus is put on those fundamentals that are immediately utilized in this dissertation, defining conventions and assembling a useful toolbox for the following chapters, improving conciseness and readability. This toolbox is organized in three sections addressing the fundamentals of control systems, linear algebra, and galvanically isolated dc-dc converters.

## 3.1 Linear and Nonlinear Control Systems

In the following sections, the fundamentals of control theory are reviewed. Apart from linear systems, also basic concepts regarding nonlinear systems are introduced because especially in power electronics, a closed-loop controlled dc-dc converter may behave like a constant-power load (CPL) or a constant-power source (CPS), elements that often introduce nonlinearity into the control loops. There is a wide range of literature on control engineering, and the fundamentals summarized in the following sections are taken from [73–78], where they can be explored in much greater detail.

### 3.1.1 Digital Control Systems

Control engineering is the science of modeling and actively influencing the behavior of dynamic physical processes. Some examples of control systems in everyday life include cruise control, keeping vehicles at a constant speed, heaters and air conditioners controlling the ambient temperature in buildings or cars, or any smartphone charger that must provide a well-regulated voltage of 5 V. Control systems rely on the principle of feedback, which means that a sensor, e.g., a thermometer, measures the control variable, e.g., the temperature, in the physical process, which is then compared to the desired value, the so-called control reference. Based on the difference between the reference and the measured value, the control law then computes a command, which is then forwarded to an actuator, e.g., a heater, which is able to manipulate the physical process. As this process

is repeated again and again, a closed loop of measurement, control law computation, and process manipulation is established. In contrast to closed-loop control systems, it is also possible to manipulate a physical process without using or even taking the measurements from the physical process, which is referred to as an open-loop control system. Despite being cheap, robust, and usually easy to implement, such control systems however cannot guarantee to make the physical process reach the reference value, and hence they require a very good model of the physical process to perform well.

Many modern-day control systems are executed on digital hardware, such as personal computers (PCs) or microcontrollers (MCUs). Therefore, any control system consists of two domains, the real, physical world, referred to as control plant, modeled in continuous time using continuous-time variables, and the digital world on the computer that executes the control laws. Figure 3.1 shows an exemplary, digital, closed-loop control system in the form of a so-called block diagram, which represents the signal flows. Many physical processes can be described mathematically through a linear time-invariant (LTI) ordinary differential equation (ODE) in the continuous time domain; using the LAPLACE transform, the transfer function $G_\mathrm{P}(s)$ of the plant can be derived as a model of the plant.[(i)] In turn, the control law can also be described mathematically using difference equations in the discrete time domain; using the $z$ transform, also the control law can be expressed as a transfer function $G_\mathrm{C}(z)$ in the discrete-time $z$ domain.[(ii)] The interface between the physical and the digital world are the sensor and the actuator. On the one hand, the control hardware picks up the measured sensor values only at discrete time instants, which is referred to as sample and hold (S/H); the time interval between the measurements is referred to as sampling time $T_\mathrm{s}$. The actuator, on the other hand, only receives one command per sampling period from the control hardware and applies it to the physical world for the entire upcoming sampling period, which can be modeled as a latch or zero-order hold (ZOH). On any digital platform, the execution of the control laws takes a certain time; usually, the command is applied to the actuator at the end of the sampling interval. This corresponds to one sample interval of delay, the so-called update delay, which is modeled by the transfer function $z^{-1}$. [78]

It should be differentiated between the manipulated inputs $u_\mathrm{m}$ to the system, which can be actively influenced by the actuator, and the so-called disturbance inputs $u_\mathrm{d}$ to the system, which cannot be influenced but also have an impact on the system output. For a cruise control application, for example, not only the motor may have an influence on the speed acting as actuator, providing torque to the system as manipulated input, but also headwinds or a steep slope may have an influence on the speed acting as disturbance inputs. Some disturbance inputs can be measured, while others may be entirely unknown; some effects, such as inaccuracies in the plant model $G_\mathrm{P}(s)$, may also be considered disturbance inputs. Additionally, the disturbance inputs can not only influence the system at the summation point shown in Fig. 3.1, but in various other ways.

[(i)] Note that the LAPLACE transform only exists for LTI systems, i.e., if the governing ODE is linear and time-invariant. Nonlinear systems have to be modeled differently.

[(ii)] Some control laws can also be nonlinear and hence, they cannot be expressed using a difference equation or a transfer function in the $z$ domain.

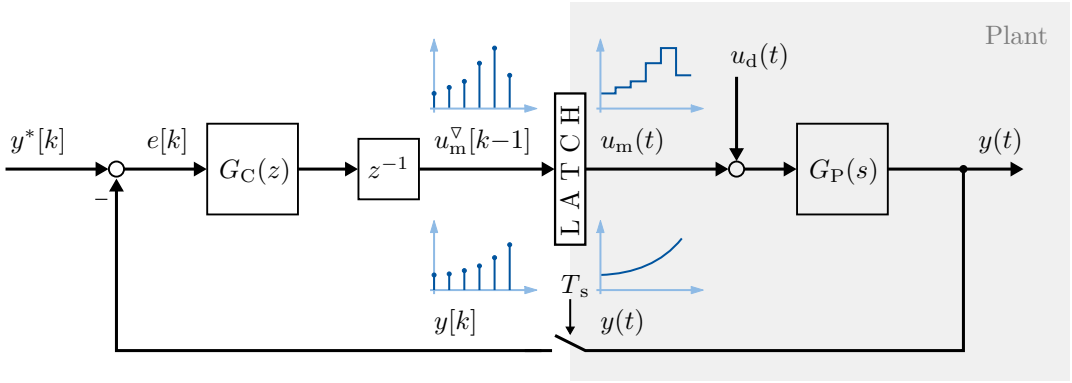



Figure 3.1: Block diagram of an exemplary, closed-loop digital control system [78]

The system output is denoted $y$ and is measured, sampled, fed back, and compared with the reference value $y^*$. In control theory, reference values are often denoted with a superscript asterisk. The difference between the reference and the feedback value, referred to as control error $e$, is fed into the control law $G_C(z)$. In this dissertation, the commanded quantity, which is applied to the actuator, is denoted with a superscript triangle $u_m^{\triangledown}$.

Two fundamental properties of control systems should be considered in any control design process: The command tracking property of the control system describes its ability to follow a given reference trajectory sufficiently dynamically and to eventually ensure a control error $e = 0$. On the other hand, the disturbance rejection property of a control system describes its immunity or stiffness against disturbances, ideally bringing the system back as quickly as possible to its state before the disturbance.

In summary, this section discussed the fundamental principles of digital control systems and introduced conventions in terms of vocabulary and notation using an exemplary block diagram of a generic control system.

### 3.1.2 State-Space Representation

In mathematics, it is well-known that an ODE of an order larger than one can be written as a system of ODEs of order one, their number being equal to the order of the original ODE. This can be applied to the differential equation of the exemplary LTI system that has been discussed in the previous section, which is called a single-input, single-output (SISO) system because it has only one manipulated input $u_m$ and one output $y$. Its LTI, but not necessarily first-order ODE can be written as a system of LTI, first-order ODEs. Extending this approach even further, it can also be applied to so-called multiple-input, multiple-output (MIMO) systems with multiple manipulated inputs, multiple disturbance inputs, and multiple outputs, which are then denoted as vectors. The result is the so-called state-space representation, which is a more detailed and more flexible way

of mathematically capturing the physics of a system:

$$\begin{aligned} \frac{\mathrm{d}\vec{x}}{\mathrm{d}t} &= \mathbf{A}\,\vec{x} + \mathbf{B_m}\,\vec{u}_{\mathrm{m}} + \mathbf{B_d}\,\vec{u}_{\mathrm{d}} \\ \vec{y} &= \mathbf{C}\,\vec{x} + \mathbf{D_m}\,\vec{u}_{\mathrm{m}} + \mathbf{D_d}\,\vec{u}_{\mathrm{d}}. \end{aligned} \tag{3.1}$$

The new vector $\vec{x}$ appearing in (3.1) is called state vector, it contains the so-called state variables. The dimension of the state vector, i.e., the number of state variables, is equal to the order of the system and hence, the order of its ODE. A vector $\vec{x}$ qualifies as state when, from its value at one specific time instant, it uniquely determines the future states and the future outputs of the system, given that the input vectors are known [73]. While this definition is somewhat abstract, usually the state variables represent the energy storages in the system [76], such as currents in inductors or voltages across capacitors. The first equation in (3.1) then describes how the energy in the system changes dynamically, either by its own dynamic behavior represented by the system matrix $\mathbf{A}$, or by manipulation from outside, represented by the input matrices $\mathbf{B_m}$ and $\mathbf{B_d}$. The second equation in (3.1) then describes how the measured system outputs $\vec{y}$ depend on the system state through the output matrix $\mathbf{C}$, or how they directly depend on the inputs through the feed-through matrices $\mathbf{D_m}$ and $\mathbf{D_d}$. In control theory, especially the interior system dynamics represented by the matrix $\mathbf{A}$ are of major interest because the eigenvalues of $\mathbf{A}$ correspond to the poles of the transfer function of the system in the Laplace domain.

In literature, the input matrices $\mathbf{B_m}$ and $\mathbf{B_d}$ are usually merged into one large input matrix, concatenating the manipulated input vector $\vec{u}_{\mathrm{m}}$ and the disturbance input vector $\vec{u}_{\mathrm{d}}$. Due to the fundamental differences between a manipulated input and a disturbance input, which have been discussed in the previous section, in this dissertation they are treated separately; a notation that can also be found in textbooks [73]. Consequently, the same applies to the feed-through matrices $\mathbf{D_m}$ and $\mathbf{D_d}$.

So far, only LTI systems have been addressed, which is why (3.1) can be expressed using matrices, i.e., linear mappings. However, also nonlinear[iii] systems can occur in reality, which can be modeled in state space as follows:

$$\begin{aligned} \frac{\mathrm{d}\vec{x}}{\mathrm{d}t} &= \vec{F}(\vec{x},\, \vec{u}_{\mathrm{m}},\, \vec{u}_{\mathrm{d}}) \\ \vec{y} &= \vec{G}(\vec{x},\, \vec{u}_{\mathrm{m}},\, \vec{u}_{\mathrm{d}}). \end{aligned} \tag{3.2}$$

Admittedly, (3.2) comes in a very generic form, which is of little use without the specific system equations. All that (3.2) expresses is that the dynamics of the state vector is some nonlinear function $\vec{F}$ of the state vector and the inputs, and that the output is also some nonlinear function $\vec{G}$ of the state and the inputs.

[iii] In this dissertation, time-variant systems are not addressed. Any system that is referred to as "nonlinear" is automatically considered time-invariant.

In summary, the state-space representation of a system is a useful, physically insightful, and detailed way of modeling a dynamic system. Especially the state variables of the system add physical meaning to a system model, as they usually represent the energy storages in a system.

### 3.1.3 Stability Criteria

Stability is one of the most important aspects when designing control systems. In a paraphrased definition, a system is stable if, without any control input, its overall stored energy tends to decrease over time, such that its state vector returns to an equilibrium point. It is, however, unstable if, without any control input, its energy increases over time, which may even lead to the destruction of the system. In contrast to the phenomenon of resonance, the destructive energy does not come from a control input, i.e., from outside the system, but comes from within the system itself. Many systems are unstable on their own, but stable inside a closed control loop. For example, military aircraft can be unstable with respect to one or more of the principal flight axes, and only a closed-loop flight control system ensures that they can resume a normal trajectory after a disturbance [79, 80]. Therefore, the ability to prove the stability of a closed-loop control system is of major importance.

Obviously, the paraphrased definition given in the last paragraph must be mathematically specified, before any mathematical way of proving stability or instability can be established. Indeed, there are multiple mathematical definitions of stability, each different in how strict the definition of stability is chosen and each with different methods of stability assessment. In this dissertation, the stability theory established by LYAPUNOV will be used. Its particular advantage is that it can even be applied to nonlinear systems. It is summarized in the following, based on [76, 77].

First, the definition of an equilibrium point shall be discussed. As already stated, in stability theory, often the absence of any control input to the system is assumed to assess its stability, excluding those cases in which the system is destroyed from outside. A more general case assumes that any control input to the system is constant over time, which can be mathematically reduced to the case that the inputs are zero [76, 77]. This assumption of zero inputs is made in the following. An equilibrium point $\vec{x}_{\mathrm{eq}}$ is defined as a state that does not change over time, hence its derivative is zero. Hence, the equilibrium points of a system can be identified by finding the solutions of

$$\vec{F}\left(\vec{x}_{\mathrm{eq}},\ \vec{0},\ \vec{0}\right) = \vec{0}\,. \tag{3.3}$$

While for LTI systems, stability is a property of the system itself, in the general case of nonlinear systems it is a property that is associated with a single equilibrium point. An equilibrium point is said to be attractive if every initial state $\vec{x}(0)$ that is sufficiently close

to the equilibrium point tends to converge into the equilibrium point. Mathematically formulated, an equilibrium point is attractive if there exists an $\epsilon > 0$ such that

$$\|\vec{x}(0) - \vec{x}_{\mathrm{eq}}\|_2 < \epsilon \quad \Rightarrow \quad \lim_{t\to\infty} \vec{x}(t) = \vec{x}_{\mathrm{eq}}. \tag{3.4}$$

Stability, however, is defined differently and does not necessarily imply attractivity. An equilibrium point is said to be stable in the sense of Lyapunov if for every $\delta > 0$ there exists an $\epsilon > 0$ such that

$$\|\vec{x}(0) - \vec{x}_{\mathrm{eq}}\|_2 < \delta \quad \Rightarrow \quad \|\vec{x}(t) - \vec{x}_{\mathrm{eq}}\|_2 < \epsilon \quad \text{for all} \quad t > 0. \tag{3.5}$$

Note that (3.5) does only state that any trajectory starting in a $\delta$-neighborhood of an equilibrium point will not leave an $\epsilon$-neighborhood of the equilibrium point, which does not imply attractivity; it is also possible that the state orbits the equilibrium point forever to be called stable. If, however, the equilibrium point is not only stable, but also attractive, it is called asymptotically stable, which guarantees the state to converge into the equilibrium point. Asymptotic stability, in turn, does not make any statement about how fast this convergence happens. Therefore, an even more strict definition is made, the so-called exponential stability, which requires exponential dynamics of the convergence. An equilibrium point is called exponentially stable if for every $\delta > 0$ there exist $\epsilon > 0$ and $\alpha > 0$ such that

$$\|\vec{x}(0) - \vec{x}_{\mathrm{eq}}\|_2 < \delta \quad \Rightarrow \quad \|\vec{x}(t) - \vec{x}_{\mathrm{eq}}\|_2 < \epsilon \cdot \mathrm{e}^{-\alpha t} \quad \text{for all} \quad t > 0. \tag{3.6}$$

Naturally, these definitions are of little use without an easy and straightforward criterion to prove them. Luckily, the so-called direct method by Lyapunov provides precisely such a criterion. First, a scalar-valued function of the state vector $V(\vec{x})$ needs to be found, a so-called Lyapunov function, which is differentiable in some neighborhood around the equilibrium point and, within that neighborhood, fulfills the conditions

$$\begin{aligned} &V(\vec{x}) = 0 \quad \text{for} \quad \vec{x} = \vec{x}_{\mathrm{eq}} \quad \text{and} \\ &V(\vec{x}) > 0 \quad \text{for} \quad \vec{x} \neq \vec{x}_{\mathrm{eq}}. \end{aligned} \tag{3.7}$$

Then, statements about the stability and also the instability[(iv)] of the equilibrium point can be made if the time derivative of the Lyapunov function satisfies the following condition for every $\vec{x}$ in the neighborhood around the equilibrium point:

$$\frac{\mathrm{d}V(\vec{x})}{\mathrm{d}t} \begin{cases} \leq 0 & \Rightarrow \text{stable}, \\ < 0 & \Rightarrow \text{asymptotically stable}, \\ > 0 & \Rightarrow \text{unstable}. \end{cases} \tag{3.8}$$

The time derivative of the Lyapunov function is easy to compute exploiting the chain

[(iv)] This Lyapunov instability theorem is less widely known, more information can be found in [77].

rule and (3.2):

$$\frac{\mathrm{d}V(\vec{x})}{\mathrm{d}t} = \left(\vec{\nabla}V\right)^{\mathrm{T}} \cdot \frac{\mathrm{d}\vec{x}}{\mathrm{d}t} = \left(\vec{\nabla}V\right)^{\mathrm{T}} \cdot \vec{F}\left(\vec{x},\ \vec{0},\ \vec{0}\right). \tag{3.9}$$

A similar theorem exists for proving exponential stability [77]. If a LYAPUNOV function can be found, which is differentiable in some neighborhood around the equilibrium point and, for some $\alpha > 0$, $\beta > 0$, and $0 < \delta_1 \leq \delta_2$, fulfills the conditions

$$\delta_1 \left\|\vec{x} - \vec{x}_{\mathrm{eq}}\right\|_2^\beta \leq V(\vec{x}) \leq \delta_2 \left\|\vec{x} - \vec{x}_{\mathrm{eq}}\right\|_2^\beta \quad \text{and} \tag{3.10}$$

$$\frac{\mathrm{d}V(\vec{x})}{\mathrm{d}t} \leq -\alpha\beta V(\vec{x}) \tag{3.11}$$

within that neighborhood, then the equilibrium point is exponentially stable, and the state converges with $\alpha$ being the rate of exponential decay according to (3.6).

The difficulty of the direct method and its equivalent to prove exponential stability is to initially find a LYAPUNOV function that satisfies (3.7) or (3.10), respectively. In many cases, a weighted sum of the squared deviations of the state variables from their value in equilibrium qualifies as LYAPUNOV function:

$$V(\vec{x}) = (\vec{x} - \vec{x}_{\mathrm{eq}})^{\mathrm{T}} \cdot \mathbf{diag}(\gamma_1,\gamma_2,\ldots) \cdot (\vec{x} - \vec{x}_{\mathrm{eq}}), \tag{3.12}$$

using positive constants $\gamma_1$, $\gamma_2, \ldots$ as weighting factors. Such a function is not only guaranteed to fulfill the conditions (3.7) and (3.10) with $\beta = 2$, it can also be interpreted physically: Whenever the state vector contains variables related to the energy storages of the system, such as voltages across capacitors or currents in inductors, a LYAPUNOV function as defined by (3.12) somewhat describes how far the system is away from its equilibrium point in terms of energy[v]. This immediately illustrates the direct method; a system can be considered stable if its stored energy, represented by $V(\vec{x})$, tends to decrease over time. In that light, also the condition from (3.11) is intuitively understandable because it is a linear, first-order ODE that demands the LYAPUNOV function to decay towards zero exponentially.

In the more specific case of LTI systems, the property of stability is not associated with a specific operating point, but with the entire system. Again assuming constant zero inputs to the system without loss of generality, the differential equation of an LTI system is

$$\frac{\mathrm{d}\vec{x}}{\mathrm{d}t} = \mathbf{A}\,\vec{x}, \tag{3.13}$$

and solving $\mathbf{A}\,\vec{x}_{\mathrm{eq}} = \vec{0}$ to find its equilibrium points gives either only one solution $\vec{x}_{\mathrm{eq}} = \vec{0}$ if the matrix $\mathbf{A}$ has full rank or infinitely many solutions if $\mathbf{A}$ is singular; multiple isolated equilibrium points are not possible. In contrast to nonlinear systems, (3.13) has a

[v] The LYAPUNOV function does not describe a real energy difference though, as this would have to be expressed using $\|\vec{x}\|_2^2 - \|\vec{x}_{\mathrm{eq}}\|_2^2$ rather than $\|\vec{x} - \vec{x}_{\mathrm{eq}}\|_2^2$. Therefore, without loss of generality, it is convenient to modify the state-space model such that $\vec{x}_{\mathrm{eq}} = 0$.

closed-form solution, which only contains exponential terms $e^{\lambda_p t}$, where $\lambda_p$ for $p = 1, 2, \ldots$ denote the eigenvalues of the matrix $\mathbf{A}$. If all eigenvalues of $\mathbf{A}$ have a negative real part, this immediately fulfills the definition of exponential stability in the sense of LYAPUNOV from (3.6), which is a well-known stability criterion for LTI systems and in many cases easier to prove compared to using the direct method. This implies that any LTI system that is asymptotically stable is also exponentially stable; the two have only to be distinguished for nonlinear systems.

In summary, the direct method by LYAPUNOV is a relatively simple way of proving the stability of equilibrium points of nonlinear systems, given that a suitable LYAPUNOV function can be found. The stability definition by LYAPUNOV is also compatible with the traditional methods to prove the stability of LTI systems.

## 3.2 Linear Algebra Toolbox

In the development of decoupled control approaches for modular dc-dc converter systems, state-space models according to Section 3.1.2 are derived. They contain large block matrices, which need to be handled mathematically; for example, the diagonalization of such matrices is a key element in deriving decoupled control approaches. However, to not lose generality, all matrices are derived for an arbitrary number of converters, making the size of the state-space matrices variable. To still be able to determine eigenvalues and eigenvectors, to invert, or to compute determinants of such block matrices of arbitrary size, some very useful tools in linear algebra are utilized. This section shall introduce those concepts and tools in linear algebra that are less widely known but required for the computations in later chapters, but shall presuppose fundamental knowledge of linear algebra. Hence it should be understood as a box of mathematical tools that is used in later chapters. In this dissertation, it suffices to only consider matrices of real numbers. The compiled tools are taken from textbooks [81–86], which can also provide a much bigger picture of the presented topics.

### 3.2.1 Right and Left Eigenvectors

The diagonalization of a square matrix via the so-called eigendecomposition requires the knowledge of its eigenvalues and (right) eigenvectors. Hence, this section briefly reviews the concept of eigenvalues and (right) eigenvectors, however also covering the less widely used concept of left eigenvectors. The presented concepts are taken from [81–84], where they can be explored in more detail.

When speaking of eigenvectors, usually right eigenvectors are meant. As widely known, a non-zero column vector $\vec{w}$ is called right eigenvector of a square $n \times n$ matrix $\mathbf{M}$ if it

satisfies

$$\mathbf{M}\vec{w} = \lambda\vec{w} \quad \Rightarrow \quad (\mathbf{M} - \lambda\mathbf{I}_n) \cdot \vec{w} = \vec{0}_{n\times 1}, \tag{3.14}$$

with $\lambda$ denoting its eigenvalue and $\mathbf{I}_n$ denoting the $n \times n$ identity matrix. Thus, an eigenvector is characterized by its property that its direction does not change when the linear transformation $\mathbf{M}$ is applied to it. Nevertheless, its length changes by multiplication with its corresponding eigenvalue. Equation (3.14) has non-zero solutions only if

$$\det(\mathbf{M} - \lambda\mathbf{I}_n) = 0. \tag{3.15}$$

This determinant is a polynomial in $\lambda$, the so-called characteristic polynomial, and finding its roots means finding the eigenvalues of $\mathbf{M}$[vi]. It is possible to have multiple roots of the same value, i.e., to find linear factors $(\lambda_p - \lambda)^q$ with integer $q$ in the characteristic polynomial. Then, the $p$'th eigenvalue $\lambda_p$ is said to have the algebraic multiplicity $q$.

For every identified eigenvalue $\lambda_p$, the eigenvectors can be computed by solving the right-hand side equation in (3.14). Hence, all possible solutions $\vec{w}$ are mapped to zero under the transformation $(\mathbf{M} - \lambda_p\mathbf{I}_n)$, i.e., they form the kernel of this matrix, which is also called eigenspace of the matrix $\mathbf{M}$ associated with the eigenvalue $\lambda_p$. The dimension of this eigenspace is called geometric multiplicity of the eigenvalue $\lambda_p$, and may be less or equal to its algebraic multiplicity.

This concept can be utilized when attempting to diagonalize the matrix $\mathbf{M}$, the so-called eigendecomposition. If a matrix $\mathbf{W}$ is assumed that contains a set of $n$ eigenvectors of the matrix $\mathbf{M}$ as columns, the multiplication of the two matrices yields

$$\begin{aligned} \mathbf{M} \cdot \mathbf{W} &= \mathbf{M} \cdot \begin{pmatrix} \vec{w}_1 & \vec{w}_2 & \dots & \vec{w}_n \end{pmatrix} \overset{(3.14)}{=} \begin{pmatrix} \lambda_1\vec{w}_1 & \lambda_2\vec{w}_2 & \dots & \lambda_n\vec{w}_n \end{pmatrix} \\ &= \mathbf{W} \cdot \mathbf{diag}(\lambda_1, \lambda_2, \dots, \lambda_n) =: \mathbf{W} \cdot \mathbf{\Lambda}. \end{aligned} \tag{3.16}$$

The matrix $\mathbf{W}$ is called (right) modal matrix of $\mathbf{M}$, while the resulting matrix $\mathbf{\Lambda}$ that contains the eigenvalues of the matrix $\mathbf{M}$ on its diagonal is called spectral matrix of $\mathbf{M}$. If the modal matrix is invertible, the equation can be left-multiplied with the inverse $\mathbf{W}^{-1}$, giving

$$\mathbf{W}^{-1} \cdot \mathbf{M} \cdot \mathbf{W} = \mathbf{\Lambda}, \tag{3.17}$$

which means that the matrix $\mathbf{M}$ has now been transformed into its diagonal equivalent, its spectral matrix $\mathbf{\Lambda}$, using its (right) eigenvectors as columns of the (right) modal matrix $\mathbf{W}$. Of course, this eigendecomposition only exists if the modal matrix $\mathbf{W}$ is invertible, which requires all $n$ eigenvectors to be linearly independent. Such a set of $n$ linearly independent eigenvectors can only be found if the dimensions of the corresponding eigenspaces, i.e., the geometric multiplicities, add up to $n$. Due to the fundamental theorem of algebra, the algebraic multiplicities of all eigenvalues add up to $n$, and as already discussed, the geometric multiplicity of an eigenspace is always less or equal than the algebraic multiplicity

[vi] In some textbooks, the characteristic polynomial is defined as $\det(\lambda\mathbf{I}_n - \mathbf{M})$, which differs from the shown definition by a factor $(-1)^n$. This however does not make a difference for the roots of the characteristic equation, i.e., the eigenvalues.

of the corresponding eigenvalue. Therefore, to obtain $n$ linearly independent eigenvectors, the geometric multiplicities must be equal to the algebraic multiplicities. This is, however, only a necessary condition because it only guarantees the linear independence of the eigenvectors corresponding to the same eigenspace. However, it can be proven that eigenvectors belonging to different eigenvalues must also be linearly independent [81], which makes the aforementioned requirement also a sufficient condition.

A very similar, but less widely known concept, is the concept of so-called left eigenvectors. A non-zero row vector $\vec{v}^{\mathrm{T}}$ is called left eigenvector[(vii)] of a square $n \times n$ matrix if it satisfies

$$\vec{v}^{\mathrm{T}}\mathbf{M} = \lambda \vec{v}^{\mathrm{T}}. \tag{3.18}$$

Transposing both sides of the equation results in

$$\left(\vec{v}^{\mathrm{T}}\mathbf{M}\right)^{\mathrm{T}} = \mathbf{M}^{\mathrm{T}}\vec{v} = \left(\lambda \vec{v}^{\mathrm{T}}\right)^{\mathrm{T}} = \vec{v}\lambda, \tag{3.19}$$

which by comparison with (3.14) means that any vector that is a left eigenvector of $\mathbf{M}$ is automatically a right eigenvector of the transposed matrix $\mathbf{M}^{\mathrm{T}}$. Hence, the corresponding eigenvalues are the roots of the characteristic polynomial

$$\det\left(\mathbf{M}^{\mathrm{T}} - \lambda \mathbf{I}_n\right) = \det\left(\mathbf{M}^{\mathrm{T}} - \lambda \mathbf{I}_n\right)^{\mathrm{T}} = \det(\mathbf{M} - \lambda \mathbf{I}_n) = 0, \tag{3.20}$$

which is exactly the same as for right eigenvectors. This means that the eigenvalues are unique to the matrix $\mathbf{M}$ regardless of whether they are associated with left or right eigenvectors.

An eigendecomposition of the matrix $\mathbf{M}$ can also be done using $n$ linearly independent left eigenvectors by arranging them in a left modal matrix $\mathbf{V}$ such that

$$\mathbf{V} \cdot \mathbf{M} = \begin{pmatrix} \vec{v}_1^{\mathrm{T}} \\ \vec{v}_2^{\mathrm{T}} \\ \vdots \\ \vec{v}_n^{\mathrm{T}} \end{pmatrix} \cdot \mathbf{M} \overset{(3.18)}{=} \begin{pmatrix} \lambda_1 \vec{v}_1^{\mathrm{T}} \\ \lambda_2 \vec{v}_2^{\mathrm{T}} \\ \vdots \\ \lambda_n \vec{v}_n^{\mathrm{T}} \end{pmatrix} = \mathbf{diag}(\lambda_1, \lambda_2, \ldots, \lambda_n) \cdot \mathbf{V} = \mathbf{\Lambda} \cdot \mathbf{V}. \tag{3.21}$$

Hence the left eigendecomposition using left eigenvectors is given by

$$\mathbf{V} \cdot \mathbf{M} \cdot \mathbf{V}^{-1} = \mathbf{\Lambda}. \tag{3.22}$$

Naturally, the condition to have $n$ linearly independent left eigenvectors, i.e., an invertible left modal matrix, still holds, which requires the geometric multiplicity of each left eigenspace to be equal to the arithmetic multiplicity of the corresponding eigenvalue.

An important special case are real, square, symmetric matrices $\mathbf{M} = \mathbf{M}^{\mathrm{T}}$. For such matrices, all eigenvalues must be real and, even better, all geometric multiplicities are equal to the respective algebraic multiplicities. This ensures that all such matrices have a

[(vii)] There are some alternative names for left eigenvectors such as eigenrows or co-eigenvectors.

set of $n$ linearly independent eigenvectors and that they all can be diagonalized [81]. Also, any left eigenvector is automatically also a right eigenvector of a symmetric matrix.

In summary, finding left and right eigenvectors of an $n \times n$ square matrix is a useful tool for its diagonalization via eigendecomposition. This requires to find $n$ linearly independent eigenvectors, which can be arranged into a so-called modal matrix. By multiplication with the modal matrix and its inverse, the original matrix can be brought to its diagonal form, the so-called spectral matrix, with the eigenvalues on its diagonal.

### 3.2.2 Block Matrices and the Kronecker Product

Any coherent block within a matrix can be considered as a sub-matrix. This section addresses such block matrices; the shown identities are taken from [85, 86]. For example, the matrix

$$\mathbf{M} = \begin{pmatrix} 1 & 2 & 0 \\ 3 & 4 & 0 \\ 0 & 0 & 5 \end{pmatrix} = \begin{pmatrix} \mathbf{M}_{11} & \mathbf{M}_{12} \\ \mathbf{M}_{21} & \mathbf{M}_{22} \end{pmatrix} = \begin{pmatrix} \mathbf{M}_{11} & \mathbf{0}_{2\times 1} \\ \mathbf{0}_{1\times 2} & \mathbf{M}_{22} \end{pmatrix} = \mathbf{diag}(\mathbf{M}_{11}, \mathbf{M}_{22}) \tag{3.23}$$

is subdivided into four blocks $\mathbf{M}_{pq}$ of different size. As the off-diagonal blocks contain only zeros, the matrix is called a block-diagonal matrix.

An efficient way of notating block matrices is the so-called Kronecker product, which is defined for any two matrices $\mathbf{M}$ and $\mathbf{N}$ as

$$\mathbf{M} \otimes \mathbf{N} := \begin{pmatrix} (\mathbf{M})_{11}\mathbf{N} & (\mathbf{M})_{12}\mathbf{N} & \cdots \\ (\mathbf{M})_{21}\mathbf{N} & (\mathbf{M})_{22}\mathbf{N} & \cdots \\ \vdots & \vdots & \ddots \end{pmatrix}, \tag{3.24}$$

where $(\mathbf{M})_{pq}$ denotes the entry of $\mathbf{M}$ in the $p$'th row and $q$'th column. For example,

$$\begin{pmatrix} 1 & 2 \\ 3 & 4 \end{pmatrix} \otimes \begin{pmatrix} 1 & 2 \\ 1 & 1 \end{pmatrix} = \begin{pmatrix} 1 & 2 & 2 & 4 \\ 1 & 1 & 2 & 2 \\ 3 & 6 & 4 & 8 \\ 3 & 3 & 4 & 4 \end{pmatrix}. \tag{3.25}$$

The Kronecker product is invariant to multiplication with a scalar $\gamma$,

$$(\gamma\mathbf{M}) \otimes \mathbf{N} = \mathbf{M} \otimes (\gamma\mathbf{N}) = \gamma(\mathbf{M} \otimes \mathbf{N}), \tag{3.26}$$

it is associative,

$$(\mathbf{L} \otimes \mathbf{M}) \otimes \mathbf{N} = \mathbf{L} \otimes (\mathbf{M} \otimes \mathbf{N}), \tag{3.27}$$

distributive,

$$\begin{aligned}(\mathbf{L}+\mathbf{M})\otimes\mathbf{N} &= (\mathbf{L}\otimes\mathbf{N})+(\mathbf{M}\otimes\mathbf{N})\\ \mathbf{L}\otimes(\mathbf{M}+\mathbf{N}) &= (\mathbf{L}\otimes\mathbf{M})+(\mathbf{L}\otimes\mathbf{N}),\end{aligned} \tag{3.28}$$

and the following rule can be derived for the mixed matrix product with the KRONECKER product, if the matrix dimensions agree:

$$(\mathbf{K}\otimes\mathbf{L})\cdot(\mathbf{M}\otimes\mathbf{N}) = (\mathbf{K}\cdot\mathbf{M})\otimes(\mathbf{L}\cdot\mathbf{N}). \tag{3.29}$$

In summary, the KRONECKER product is an efficient way of denoting large block matrices, and some useful identities exist to facilitate the mathematical handling of large block-matrix operations.

### 3.2.3 Special Determinants and Inverses

Especially with large matrices of arbitrary dimensions, it is difficult to analytically determine their eigenvalues, as this requires computing a determinant. The same is true for inverses. Fortunately, for special types of matrices, there are some identities that still allow computing their determinants and inverses. Therefore, this section collects those identities that are helpful in later chapters; they are taken from [84, 85].

First, the well-known rules for the determinant and the inverse of diagonal matrices,

$$\det(\mathbf{diag}(\gamma_1,\gamma_2,\ldots,\gamma_n)) = \gamma_1\cdot\gamma_2\cdot\ldots\cdot\gamma_n \tag{3.30}$$

$$(\mathbf{diag}(\gamma_1,\gamma_2,\ldots,\gamma_n))^{-1} = \mathbf{diag}\big(\gamma_1^{-1},\gamma_2^{-1},\ldots,\gamma_n^{-1}\big), \tag{3.31}$$

where $\gamma_1\ldots\gamma_n$ denote real numbers, do also apply to block-diagonal matrices [85]:

$$\det(\mathbf{diag}(\mathbf{M}_1,\mathbf{M}_2,\ldots,\mathbf{M}_n)) = \det(\mathbf{M}_1)\cdot\det(\mathbf{M}_2)\cdot\ldots\cdot\det(\mathbf{M}_n) \tag{3.32}$$

$$(\mathbf{diag}(\mathbf{M}_1,\mathbf{M}_2,\ldots,\mathbf{M}_n))^{-1} = \mathbf{diag}\big(\mathbf{M}_1^{-1},\mathbf{M}_2^{-1},\ldots,\mathbf{M}_n^{-1}\big). \tag{3.33}$$

Second, assuming a square $x\times x$ matrix $\mathbf{M}$ and a square $y\times y$ matrix $\mathbf{N}$, the following rules apply for the determinant and the inverse[(viii)] of a KRONECKER product:

$$\det(\mathbf{M}\otimes\mathbf{N}) = (\det\mathbf{M})^y\cdot(\det\mathbf{N})^x \tag{3.34}$$

$$(\mathbf{M}\otimes\mathbf{N})^{-1} = \mathbf{M}^{-1}\otimes\mathbf{N}^{-1}. \tag{3.35}$$

[(viii)] This requires $\mathbf{M}$ and $\mathbf{N}$ to be also invertible.

For the special case of $\mathbf{M} = \gamma$ being a real-valued scalar, (3.34) reduces to

$$\det(\gamma \mathbf{N}) = \gamma^y \cdot \det \mathbf{N}. \tag{3.36}$$

Furthermore, there are also identities for computing the determinant and the inverse of matrices that are of the form $\left(\mathbf{M} + \vec{a} \cdot \vec{c}^{\,\mathrm{T}}\right)$, where $\mathbf{M}$ is $n \times n$ and invertible, while $\vec{a}$ and $\vec{c}$ are column vectors of length $n$, which form a matrix that is added to $\mathbf{M}$ via the so-called outer product $\vec{a} \cdot \vec{c}^{\,\mathrm{T}}$. Computing the determinant of such a matrix is possible using the so-called matrix determinant lemma, stating

$$\det\left(\mathbf{M} + \vec{a} \cdot \vec{c}^{\,\mathrm{T}}\right) = \left(1 + \vec{c}^{\,\mathrm{T}} \cdot \mathbf{M}^{-1} \cdot \vec{a}\right) \cdot \det \mathbf{M}. \tag{3.37}$$

Similarly, the Sherman-Morrison formula gives the inverse of such a type of matrix:

$$\left(\mathbf{M} + \vec{a} \cdot \vec{c}^{\,\mathrm{T}}\right)^{-1} = \mathbf{M}^{-1} - \frac{\mathbf{M}^{-1} \cdot \vec{a} \cdot \vec{c}^{\,\mathrm{T}} \cdot \mathbf{M}^{-1}}{1 + \vec{c}^{\,\mathrm{T}} \cdot \mathbf{M}^{-1} \cdot \vec{a}}. \tag{3.38}$$

For the special case in which

$$\mathbf{M} + \vec{a} \cdot \vec{c}^{\,\mathrm{T}} = \gamma \mathbf{I}_n + \mu \vec{1}_{n\times 1} \cdot \left(\vec{1}_{n\times 1}\right)^{\mathrm{T}} = \gamma \mathbf{I}_n + \mu \mathbf{1}_{n\times n}, \tag{3.39}$$

with real-valued scalars $\gamma$ and $\mu$, the identities simplify significantly, resulting in

$$\det(\gamma \mathbf{I}_n + \mu \mathbf{1}_{n\times n}) = \gamma^n + n\mu\gamma^{n-1} \tag{3.40}$$

$$(\gamma \mathbf{I}_n + \mu \mathbf{1}_{n\times n})^{-1} = \frac{(\gamma + \mu n)\mathbf{I}_n - \mu \mathbf{1}_{n\times n}}{\gamma(\gamma + \mu n)}. \tag{3.41}$$

In summary, even for large square matrices of arbitrary dimension, some useful identities can be exploited to compute their determinants and inverses, such as the matrix determinant lemma or the Sherman-Morrison formula. This concludes the collection of useful tools in linear algebra, which is used in later chapters for the development of decoupled control strategies of modular dc-dc converters.

## 3.3 Galvanically Isolated DC-DC Converters

Although the control methodologies for modular dc-dc converters that are developed in this dissertation should be independent of a specific converter topology, they are validated in the experiments using actual dc-dc converter hardware. Therefore, this section introduces the converter topologies that are used in this dissertation. All of them are galvanically isolated, i.e., their primary and secondary sides do not share a common potential, which is usually realized by transferring the power through a high-frequency transformer.

The galvanic isolation useful to flexibly interconnect the primary and the secondary sides in series or parallel without creating short circuits. Additionally, all examined topologies are bidirectional, which is useful for validation purposes, but not essential for the developed control methodologies.

Apart from the topologies that are worked with in this dissertation, there obviously exists a multitude of other galvanically isolated dc-dc converter topologies, both resonant and non-resonant, which should all be available to use with the developed control methodologies. A classification of converter topologies is done in Section 5.1. The following sections, however, only discuss the topologies that are used in this dissertation for the experimental validation, which are suitable representatives of all possible topologies.

### 3.3.1 The Single-Phase Dual-Active Bridge

The single-phase dual-active bridge (DAB) is a bidirectional, galvanically isolated dc-dc converter first introduced in [87]; its schematic is shown in Fig. 3.2. A lot of scientific literature exists on this topology, covering nearly every aspect of the converter from modulation and control techniques, design optimization, and hardware-related aspects; a thorough overview is given in [88]. This section gives a brief overview, which is based on the publication [89].

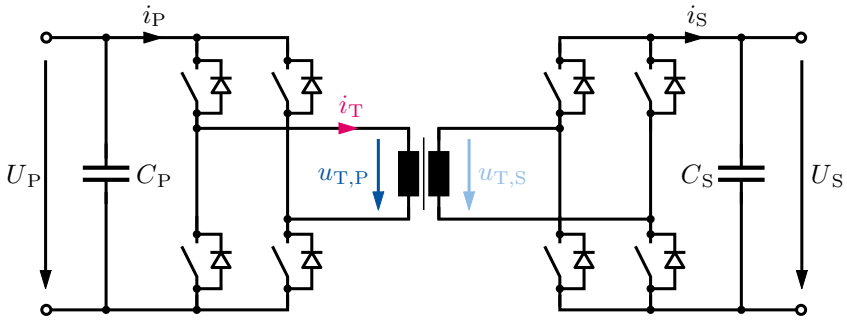



Figure 3.2: The single-phase DAB topology

The single-phase DAB consists of two dc ports each equipped with a full bridge of semiconductor devices, such as silicon (Si) or silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs), Si insulated-gate bipolar transistors (IGBTs) or gallium nitride (GaN) devices. The originally proposed modulation strategy for this converter is the so-called single phase shift (SPS) modulation [87], in which both full bridges operate at 50 % duty cycle. Figure 3.3 shows the operating waveforms of the single-phase DAB under SPS modulation. Within the full-bridge circuit, both half-bridge legs operate 180° out of phase, such that the resulting primary-side and secondary-side transformer terminal voltage waveforms, $u_\mathrm{T,P}$ and $u_\mathrm{T,S}$, are bipolar square waves. Introducing a phase-shift angle $\varphi$ between the primary and the secondary-side voltage patterns manipulates the voltage across the leakage inductance $L_\sigma$ of the transformer. The larger the phase-shift

angle, the longer lasts the high voltage drop across the parasitic inductance, making the transformer current $i_\mathrm{T}$ steeply rise. The steady-state transferred power $P_\mathrm{SPS,1ph}$ is directly manipulated by the phase-shift angle $\varphi$ according to

$$P_\mathrm{SPS,1ph} = \frac{U_\mathrm{P} U'_\mathrm{S}}{2\pi f_\mathrm{sw} L_\sigma} \cdot \varphi \cdot \left(1 - \frac{|\varphi|}{\pi}\right), \tag{3.42}$$

where $U_\mathrm{P}$ and $U_\mathrm{S}$ denote the dc voltages on the primary and secondary side, respectively, and $f_\mathrm{sw}$ the switching frequency. The notation $U'_\mathrm{S}$ indicates that this quantity is referred to the primary side of the transformer by scaling with the turns ratio. Note that the power transfer characteristic (3.42) also holds for negative values of the phase-shift angle $\varphi$ and therefore showcases the bidirectional nature of the single-phase DAB. The power transfer equation (3.42) is idealized, it assumes a completely lossless converter and zero dead times; hence, it can only serve as an estimate when using it inside a control system.

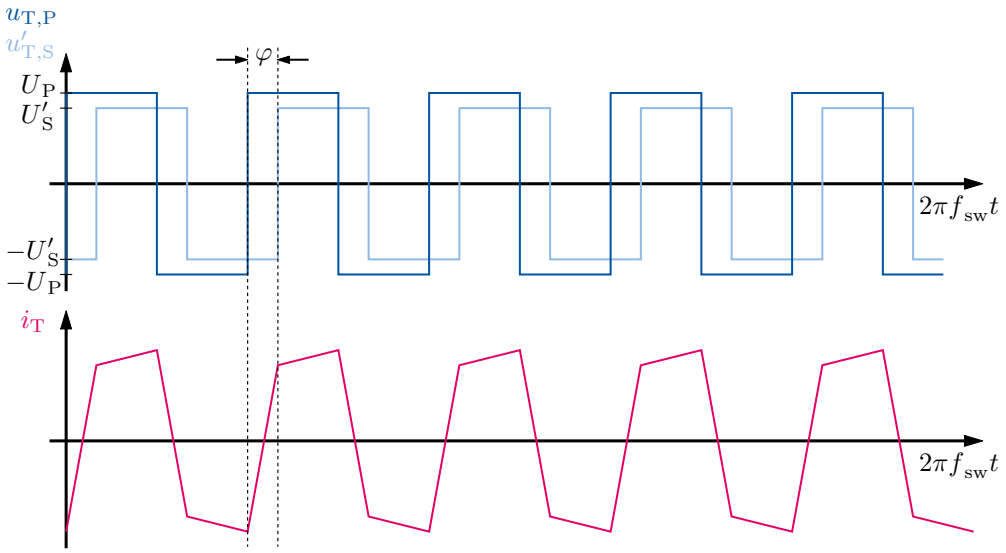



Figure 3.3: Waveforms of the SPS modulation for the single-phase DAB

It can easily be derived that the absolute value of the transferred power is maximal for phase-shift angles $|\varphi| = \pi/2$, which implies that for given primary-side and secondary-side voltages, the transferred power is inherently limited by the short-circuit reactance of the transformer measured at the switching frequency:

$$|P_\mathrm{SPS,1ph}| \leq \frac{U_\mathrm{P} U'_\mathrm{S}}{4 \cdot 2\pi f_\mathrm{sw} L_\sigma}. \tag{3.43}$$

Additionally, it becomes clear from (3.42) that the average primary-side rectified current $\bar{i}_\mathrm{P}$ only depends on the secondary-side dc voltage $U_\mathrm{S}$ because the power equation $P_\mathrm{SPS,1ph} = U_\mathrm{P} \bar{i}_\mathrm{P}$ must always hold, hence

$$\bar{i}_\mathrm{P} = \frac{U'_\mathrm{S}}{2\pi f_\mathrm{sw} L_\sigma} \cdot \varphi \cdot \left(1 - \frac{|\varphi|}{\pi}\right). \tag{3.44}$$

Naturally, the same also applies to the average secondary-side rectified current, which only depends on the primary-side dc voltage. This also implies that the short-circuit current on either side of the single-phase DAB is inherently limited, as it only depends on the voltage on the other side of the converter [90].

Another advantage of the SPS modulation strategy is its zero-voltage switching (ZVS) capability. Because of the two zero crossings of the transformer current in each switching period, the switches turn on under negative currents in most operating points, and thus, under almost zero voltage, as the anti-parallel diodes of the semiconductor switches are conducting. The turn-on process of a semiconductor device is usually associated with higher losses than the turn-off process [91], hence eliminating these turn-on losses is beneficial for converter efficiency. Nonetheless, the ZVS property is lost under partial-load conditions, when the ratio of the dc supply voltages does not match the transformer turns ratio. Additionally, the larger the phase-shift angle becomes, the larger is the ratio of the reactive power to the transferred power, making the conduction losses disproportionately rise [89]. Due to the absence of series capacitors as seen in resonant converters, dc offsets may occur in the winding currents and in the flux linkage waveforms in the transformer core. To avoid permanent dc bias or even saturation of the transformer core, the voltage-time areas applied to the primary-side and secondary-side windings have to be as symmetric as possible, which requires a sufficiently high resolution of the PWM signals, or passive measures against saturation such as an airgap in the transformer core.

These downsides are only exemplary reasons for the development of many other modulation strategies in literature, for example [92–96], each with its individual advantages and disadvantages. For example, a frequency-variable variant of the SPS modulation strategy called flux control modulation (FCM) has been proposed in [97]. It is based on the observation that the peak absolute value of the flux linkage waveform in the transformer core over one switching period decreases linearly with increasing phase-shift angle, which implies that the transformer core is designed for the no-load case. This allows for the switching frequency to be linearly reduced in the same manner, keeping the flux linkage at the level of the no-load case, but reducing the switching losses. This dissertation, however, only considers SPS modulation for the single-phase DAB because a robust way of operating this converter to validate higher-level control strategies is considered more important than a thoroughly optimized converter.

When abruptly transitioning from one phase-shift angle to another one in SPS modulation, dc offsets occur in the transformer currents, which reflects as severe oscillations in the primary-side and secondary-side rectified currents $i_\mathrm{P}$ and $i_\mathrm{S}$. As they decay with a large time constant, these dc offsets may even accumulate over time. To overcome this issue, the so-called instantaneous current control (ICC) has been proposed in [98, 99][(ix)] that allows for a smooth transition between two phase-shift angles, avoiding dc offsets. As two switching actions take place within one switching period, an intermediate phase-shift

[(ix)] The ICC and all related algorithms have originally been proposed for the three-phase DAB, however they are also suitable for the single-phase variant.

angle can be introduced in the middle of the upcoming switching period, before applying the new phase-shift angle at the end of the upcoming switching period. It has been shown in [98, 99] that if the intermediate angle is the arithmetic mean of the old and the new phase-shift angle, dc offsets in the phase current are fully eliminated. This is equivalent to introducing a discrete filter of the form

$$G_{\mathrm{ICC}}(z) = \frac{1 + z^{-1}}{2} \tag{3.45}$$

on the phase-shift angle, where one time step corresponds to half a switching period.

The ICC method, similar to the description of SPS modulation in (3.42), assumes an idealized, lossless converter. To adapt to more realistic scenarios, the ICC method has been improved over time, i.e., by accounting for the transformer winding resistance in the improved instantaneous current control (IICC) [100]. Furthermore, dc offsets not only occur in the transformer currents, but also in the flux linkage waveform in the transformer core. To also compensate these offsets and hence avoid saturation, the instantaneous flux and current control (IFCC) and improved instantaneous flux and current control (IIFCC) have been developed in [101] and [102], respectively, the latter also accounting for the winding resistances. These methods, however, require the switching actions to be shifted backward and forward in time, which makes the implementation more tedious. Therefore, the ICC method is used for the single-phase DAB converters in this dissertation because its implementation following (3.45) is very simple to realize and already allows a good compensation of current offsets. The family of ICC methods can also be transferred to multi-active bridge (MAB) converters [103, 104].

From a control perspective, the whole family of ICC algorithms allows a deadbeat-like transition between two operating points. However, taking the phase-shift angle as command variable is a sub-optimal choice because (3.44) describes a quadratic, and hence nonlinear relationship between the phase-shift angle $\varphi$ and the average primary-side rectified current $\bar{i}_{\mathrm{P}}$. Therefore, the SPS characteristic (3.44) is usually inverted in software to utilize the average primary-side rectified current directly as command variable, and calculating the required phase-shift angle from this commanded current [105, 106]. Naturally, this also can be realized for commanding the average secondary-side rectified current $\bar{i}_{\mathrm{S}}$, by using the other dc voltage in the inverse function of (3.44). The same idea can be applied also to other modulation strategies as seen in [60].

Figure 3.4 shows an exemplary, state-of-the-art, open-loop control for the single-phase DAB as seen in literature [103, 105]. The unit delay block models the update delay of the control system. The inverted SPS block represents the inverse of (3.44), calculating the required phase-shift angle from the commanded current. Acting as the interface between the control system and the plant, the ICC algorithm generates the PWM signals that are forwarded to the converter. For an idealized converter, these PWM patterns should evoke the exact same average rectified secondary-side current as commanded, however the inverted model (3.44) is idealized and will produce an error in a real application. This

error is modeled as a disturbance input $i_{\mathrm{err}}$ to the system. Condensing all the previous aspects into a single block labeled "DAB" describes the open-loop controlled DAB as a very dynamic, almost deadbeat-like controlled current source.

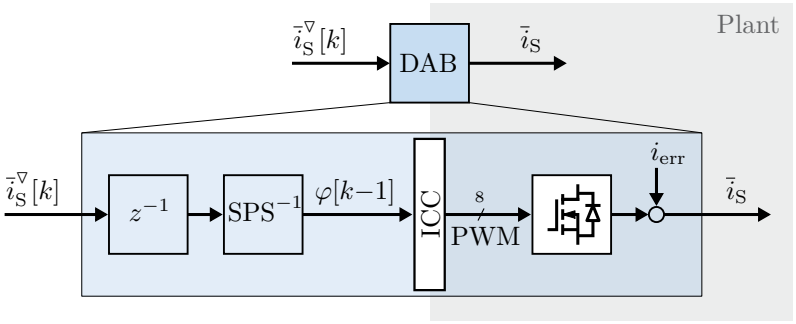



Figure 3.4: Exemplary open-loop control system for the single-phase DAB

In summary, this section introduced the single-phase DAB topology and a simple, straightforward method of operating it, compiled from state-of-the-art solutions proposed in literature. Using the SPS modulation strategy, the ICC to improve its transient response, and an open-loop control scheme, the single-phase DAB can be made to behave like a very dynamic, controlled current source.

### 3.3.2 The Three-Phase Dual-Active Bridge

Along with the single-phase variant, the three-phase variant of the DAB topology has been proposed in [87]; its schematic is shown in Fig. 3.5. Compared to the single-phase variant, the operating principle, the SPS modulation strategy, the family of ICC algorithms, and the open-loop control scheme are very similar, so that only the differences are pointed out in this section.

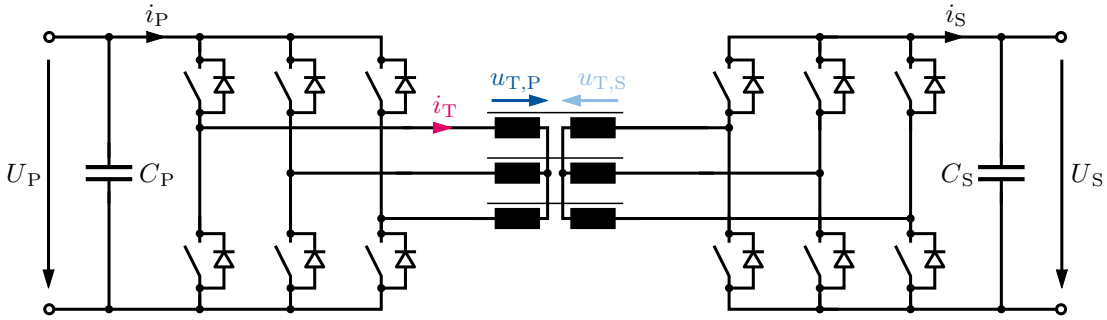



Figure 3.5: The three-phase DAB topology

Looking at the topology in Fig. 3.5, there are now three half bridges of semiconductor devices on each side of the three-phase high-frequency transformer. In SPS modulation, they still all operate at 50 % duty cycle, but shifted by 120° against each other. The voltage

waveforms generated by the half bridges, however, do not appear across the transformer windings like in the single-phase DAB, but the transformer windings form an inductive voltage divider due to the star connection of the transformer. In SPS modulation, two of the three windings are connected to either the positive or the negative dc rail, while the remaining winding is connected to the other dc rail. Therefore, the magnitude of the voltages across the transformer windings is either $\pm 1/3$ or $\pm 2/3$ of the respective dc voltage. The resulting six-step sinusoidal voltage waveforms across the transformer windings are shown in Fig. 3.6. The voltage patterns of the primary-side and secondary-side bridges are, again, phase-shifted in time by the angle $\varphi$, which manipulates the voltage across the leakage inductances of the transformer, which results in the following power equation:

$$P_{\mathrm{SPS,3ph}} = \frac{U_{\mathrm{P}} U'_{\mathrm{S}}}{2\pi f_{\mathrm{sw}} L_{\sigma}} \cdot \begin{cases} \varphi \cdot \left(\frac{2}{3} - \frac{|\varphi|}{2\pi}\right) & \text{for } |\varphi| \leq \frac{\pi}{3} \\ \varphi - \operatorname{sgn}\varphi \cdot \left(\frac{\varphi^2}{\pi} + \frac{\pi}{18}\right) & \text{for } \frac{\pi}{3} < |\varphi| \leq \frac{\pi}{2}, \end{cases} \tag{3.46}$$

$$|P_{\mathrm{SPS,3ph}}| \leq \frac{7}{36} \cdot \frac{U_{\mathrm{P}} U'_{\mathrm{S}}}{2\pi f_{\mathrm{sw}} L_{\sigma}}. \tag{3.47}$$

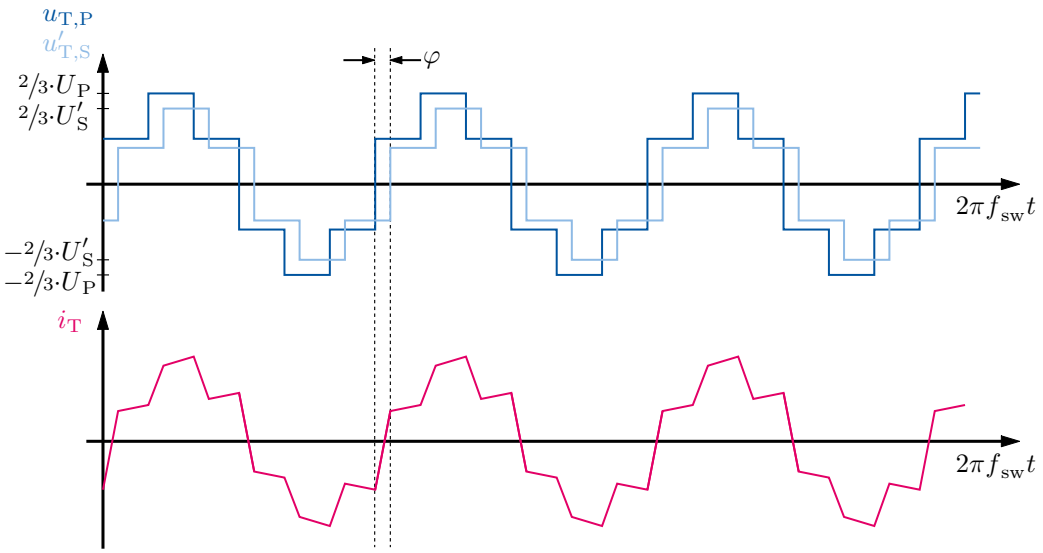



Figure 3.6: Waveforms of the SPS modulation for the three-phase DAB

The waveforms of the transformer currents as shown in Fig. 3.6 are more sinusoidal compared to those of the single-phase variant, which are more trapezoidal. This implies less harmonic content and hence lower conduction losses. The same holds for the flux linkage waveforms in the transformer legs. Even more, the peak flux linkage experienced in the three-phase DAB is significantly reduced compared to the peak flux linkage in the single-phase DAB for the same dc voltages and the same switching frequency [107]. It also decreases piece-wise linearly with increasing phase-shift angle, making the FCM modulation strategy also available for the three-phase converter [108]. As the switching states of each semiconductor bridge influence the current waveforms in all three phases, the current in the semiconductor devices are turned off at a lower value than the peak

phase current, saving switching losses. The turn-on transition, in turn, happens under ZVS condition, unless in partial load under asymmetric dc voltages, which is why a series of other modulation strategies has been proposed in literature to improve partial-load efficiency, e.g., the so-called asymmetric duty cycle control (ADCC) [109]. Finally, similarly to three-phase ac systems, the instantaneous power fluctuations are significantly reduced compared to those experienced in the single-phase DAB. This results in much less ripple content in the primary-side and secondary-side rectified currents, allowing a significant downsizing of the dc-link capacitors. A particular difficulty of the three-phase SPS modulation, however, is its susceptibility to transformer asymmetries. In three-leg transformer core configurations, the center leg usually exhibits a different parasitic inductance than the outer legs, resulting in an asymmetrically distributed power flow, which is however possible to compensate for [99, 110].

Just as for the single-phase DAB, the family of ICC algorithms is also available for the three-phase variant, compensating for transient dc offsets in the transformer phase currents and the flux linkage waveforms. Just as for the single-phase variant, these algorithms allow a fast transition between two operating points in no more than one switching period. Literature [111] also proposed so-called soft start-up and shut-down sequences for the three-phase DAB, avoiding dc offsets both in the phase currents and in the flux linkage waveforms when initially switching on the PWM, and avoiding remanent magnetization of the transformer core when switching off the converter.

The open-loop control system for the three-phase DAB is very similar to the one shown in Fig. 3.4 for the single-phase DAB and only requires replacing the inverted power transfer equation and the three-phase variant of either of the numerous ICC algorithms [105]. This also enables the three-phase DAB to act like a very dynamic, controllable current source.

In summary, this section highlighted the similarities and differences of the three-phase DAB compared to the previously discussed single-phase DAB in terms of topology, modulation strategies, and open-loop control. From a control perspective, both topologies can be operated as dynamic, controllable current sources.

### 3.3.3 Current-Fed Topologies

Proton exchange membrane (PEM) electrolysis or fuel-cell applications usually require a relatively low dc voltage and a high current that exhibits a very low, ideally zero ripple amplitude [112]. Addressing these requirements, a topology variant has been introduced in [113] for a single-phase resonant converter. However, this so-called current-fed structure is available for other converter topologies as well; Figure 3.7 shows a single-phase DAB similar to the one in Fig. 3.2, but with a current-fed secondary side.

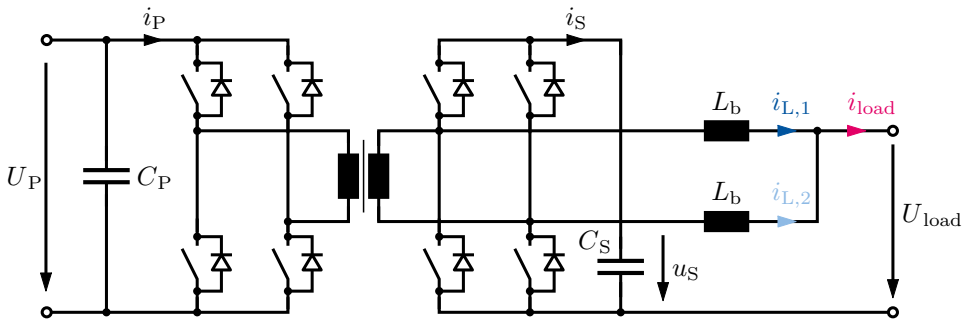



Figure 3.7: The current-fed, single-phase DAB topology

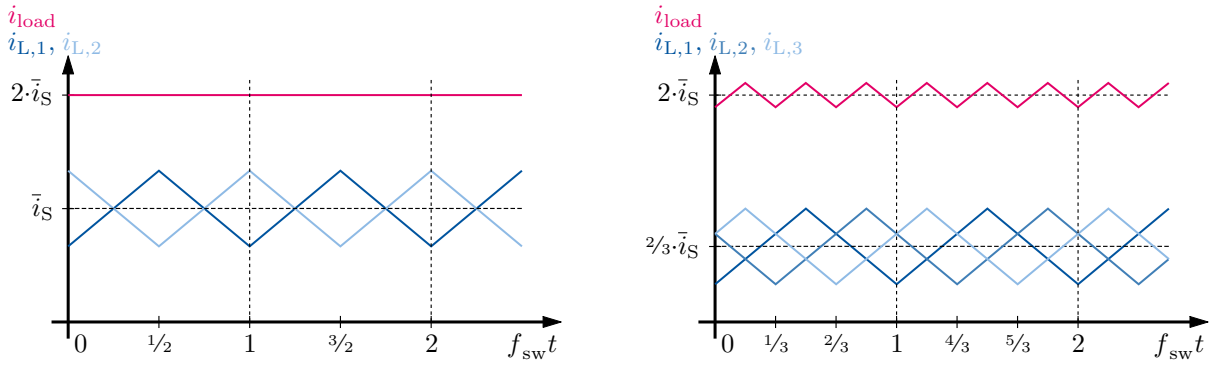
Instead of connecting the load to the dc-link terminals, it is connected to the midpoints of the full bridge through two series inductors $L_\mathrm{b}$. Hence, the inductors and the full bridge form two synchronous buck converters that are sharing the same semiconductor devices with the DAB topology. The synchronous buck structure allows a reduction of the load voltage $U_\mathrm{load}$ and an increase of the load current $i_\mathrm{load}$. For a duty cycle of 50 % as seen in SPS modulation, the average load current is twice the average rectified secondary-side current, $\bar{i}_\mathrm{load} = 2\bar{i}_\mathrm{S}$, while the load voltage is half the voltage $u_\mathrm{S}$ across the secondary-side dc-link capacitor, $U_\mathrm{load} = {}^1\!/_2 U_\mathrm{S}$, which makes the current-fed port behave similarly to a current-doubler rectifier [114].

Additionally, the synchronous buck converters operate in a phase-shifted manner due to SPS modulation, which is called “interleaving”, a common technique to reduce the current ripple [115] because the ripple components in the individual inductors partly cancel out when they add up at the common node. For an interleaved synchronous buck converter consisting of $\nu$ half bridges and switching at the duty cycle $d$, it has been shown in [116] that the peak-to-peak ripple component of the load current $i_\mathrm{load}$ is given by

$$\Delta I_\mathrm{load,pp} = \frac{U_\mathrm{load}}{f_\mathrm{sw} L_\mathrm{b}} \cdot \left(1 - \frac{\lfloor \nu d \rfloor}{\nu d}\right) \cdot (1 + \lfloor \nu d \rfloor - \nu d). \tag{3.48}$$

This implies that the load current ripple becomes zero whenever the quantity $\nu d$ is an integer. For the case shown in Fig. 3.7, the number of half bridges is $\nu = 2$ and the duty cycle is $d = 50\,\%$ due to SPS modulation. Therefore, the current-fed structure achieves ideally zero ripple current. In both inductors, triangular current waveforms denoted $i_\mathrm{L,1}$ and $i_\mathrm{L,2}$ with equal rise and fall times are generated, which add up to a pure dc current without any ripple at the common node. This scenario is illustrated in Fig. 3.8a. If the same structure is applied to the three-phase DAB, however, using $\nu = 3$ series inductors, the quantity $\nu d$ is not an integer and the remaining output current ripple is not zero anymore because the SPS modulation still operates at 50 % duty cycle. This scenario is illustrated in Fig. 3.8b.

A downside of the current-fed port is its increased component count and hence, higher cost. Therefore, literature proposes to integrate the current-fed inductors into the transformer




(a) Single-phase topology ($\nu = 2$) (b) Three-phase topology ($\nu = 3$)

Figure 3.8: Waveforms in current-fed topologies at 50 % duty cycle

[117, 118], which in turn makes its design more challenging. Moreover, the series inductors generate additional losses; not only do they experience a potentially significant dc current, but also potentially significant ripple components that generate high-frequency losses both in the winding and the core. As suggested by (3.48), these high-frequency losses are independent of the dc value of the load current, so they even occur in the no-load case and hence reduce the partial-load efficiency.

Apart from the steady-state operating principle, also the transient behavior of current-fed topologies is of interest because the inductors $L_{\mathrm{b}}$ and the dc-link capacitor $C_{\mathrm{S}}$ form a resonant network at the current-fed port. If the interleaved half bridges operating at 50 % duty cycle are assumed to ideally cut the voltage in half and double the current, the equivalent circuit shown in Fig. 3.9 is obtained. The equivalent inductance $L_{\mathrm{b,eq}}$ can be derived using the constraint of energy conservation:

$$\frac{1}{2}L_{\mathrm{b,eq}}\left(\frac{\bar{i}_{\mathrm{load}}}{2}\right)^2 = \nu \cdot \frac{1}{2}L_{\mathrm{b}}\left(\frac{\bar{i}_{\mathrm{load}}}{\nu}\right)^2 \quad \Rightarrow \quad L_{\mathrm{b,eq}} = \frac{4}{\nu}L_{\mathrm{b}}. \tag{3.49}$$

Whenever the current $\bar{i}_{\mathrm{S}}$ delivered by the DAB is abruptly changed, which is possible thanks to the ICC algorithm, it excites the resonant network at its resonant frequency

$$f_{\mathrm{res}} = \frac{1}{2\pi\sqrt{\frac{4}{\nu}L_{\mathrm{b}}C_{\mathrm{S}}}}. \tag{3.50}$$

Therefore, it has to be made sure that either sufficient damping is provided by choosing a particularly large dc-link capacitance, or that the resonant network is excited with minimal amplitude. This can either be achieved by avoiding step current changes, making sure that the exciting current contains minimal harmonic content at the resonant frequency, or by also introducing intermediate switching patterns that send the current-fed topology directly to its new steady-state operating point. Such an algorithm has been introduced in [119].

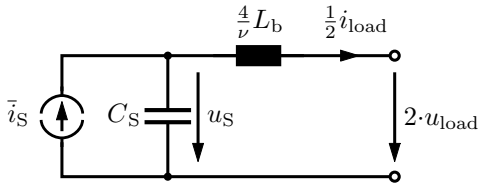



Figure 3.9: Equivalent circuit of a current-fed port

A very similar situation has to be considered when powering on the current-fed topology. Due to the antiparallel diodes of the semiconductor switches, the secondary-side dc-link capacitor is only pre-charged to the value of the load voltage $U_\mathrm{load}$. In steady state, however, twice the load voltage appears on the secondary-side dc-link capacitor. Hence, after switching on the PWM, the voltage is initially doubled, which also comes with a substantial transient exciting the resonant network. Additionally, the DAB portion of the converter is initially subjected to asymmetric dc voltages and therefore likely to operate outside its ZVS region. Literature [120] therefore proposes a dedicated start-up procedure to control the voltage across the secondary-side dc-link capacitor.

Switching to the control perspective, the equivalent circuit from Fig. 3.9 translates into the block diagram shown in Fig. 3.10. The resonant nature of the converter is visible from the inherent negative feedback loop and the two integrators.

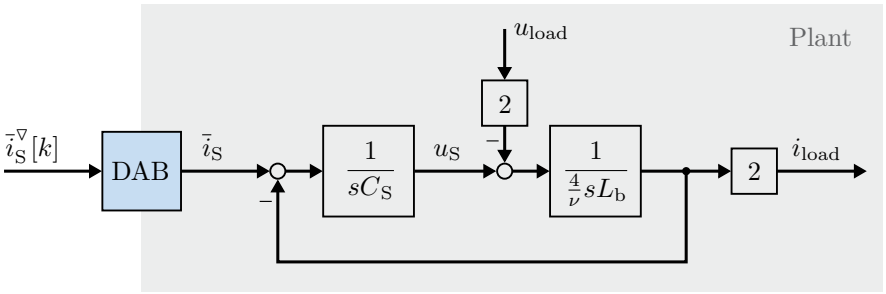



Figure 3.10: Block diagram of a current-fed converter port as control plant

In summary, this section introduced current-fed converter variants and discussed the operating principle to generate a high output current with low ripple amplitude. Based on the derivation of the equivalent circuit, the challenges in the practical application of these converters as well as possible solutions were highlighted, followed by a block diagram for control purposes.

## 3.4 Summary

The aim of this chapter was to compile a useful toolbox that is utilized in the following chapters to model, analyze, and decouple modular dc-dc converter systems. For this purpose, fundamentals from control theory, linear algebra, and power electronics have been reviewed.

After summarizing the basic concepts from digital control theory, the state-space representations of both LTI systems and nonlinear, time-invariant systems have been reviewed. Hereafter, the stability theory by LYAPUNOV has been reviewed, which applies both to LTI and to nonlinear systems. The direct method by LYAPUNOV has been introduced, which is a useful tool in assessing system stability for nonlinear systems. The reason for introducing means of system modeling and assessing system stability both for LTI and for nonlinear system is that in power-electronic systems, constant-power elements such as a CPS or a CPL are likely to occur, which are inherently nonlinear.

Developing the state-space models of modular, interconnected dc-dc converter systems in later chapters results in large systems of equations and hence, large block matrices. To facilitate the mathematical handling of these large matrices, basic concepts from linear algebra have been reviewed, such as the KRONECKER product, or the computation of non-trivial determinants and inverses using the matrix determinant lemma or the SHERMAN-MORRISON formula. Additionally, the concept of left eigenvectors has been reviewed and how it can be utilized to diagonalize matrices, which plays the key role in the decoupling of the control systems of modular, interconnected dc-dc converter systems in Chapter 5.

Finally, the power-electronic topologies that are used in this dissertation to validate the proposed decoupled control methods have been introduced, namely the single-phase and the three-phase DAB. Additionally, the so-called current-fed topology variant has been reviewed, which is encountered as a current-fed, single-phase DAB in the validation of the proposed control methods in Chapter 6. Apart from the schematics, the operating principles, and the modulation strategies, a special focus was put on the open-loop control of these topologies because making a topology behave in a well-defined and precise way is essential for a robust and well-behaved control design.

# 4 Modeling and Control of a Dual DC-DC Converter System

Before addressing the modeling and control of dc-dc converter systems consisting of arbitrarily many power-electronic building blocks (PEBBs), this chapter discusses the simplest possible modular dc-dc converter system consisting of only two PEBBs. The focus is put on a physics-based explanation rather than on a mathematical argumentation, which facilitates the understanding of the mathematical approach pursued in Chapter 5. Additionally, a realistic application scenario is addressed in this chapter, which is introduced in the first section. After that, the control design for an individual converter is discussed. When interconnecting two of these converters, however, cross couplings are introduced, which is illustrated using the state-space model of the interconnected system. Finally, the decoupling approach is presented, which is the basis for the more generalized approach pursued in Chapter 5. All steps are supported using simulations. The approach presented in this chapter has been published in [105, 121, 122].

## 4.1 Application: On-Board Charger for Catenary Trucks

While the decarbonization and electrification of the individual transport sector is already ongoing, the road-bound long-haul transport sector still produces about the same emissions as in 1990 [123]. One possible alternative to diesel trucks are so-called catenary trucks. They are equipped with a traction battery and two pantographs that are connected to overhead lines, which are partially installed on highways. In contrast to fully electrified trucks, this in-motion charging (IMC) approach reduces the size and cost of the traction battery and increases the possible operating hours of the trucks. However, the level of overhead-line electrification and the battery capacity have to be traded off carefully. Catenary trucks not only have the potential to significantly reduce the primary energy consumption, but also to achieve approximately equal life-cycle costs in comparison to pure diesel trucks [124, 125]. Test track installations use a dc voltage of 600 V as catenary voltage, while literature suggests higher catenary voltages of 1200 V or even more [126]. Due to the weak grounding of trucks, two overhead lines need to be installed to provide a current return path. For the same reason, a galvanic isolation of the overhead-line potential from the chassis potential must be established to prevent hazardous high voltage on the chassis in case of an isolation fault, a requirement that asks for a galvanically isolated dc-dc converter acting as on-board charger (OBC). The publicly funded

Table 4.1: Specifications of the three-phase DAB from the project "ConverT" [105, 122]

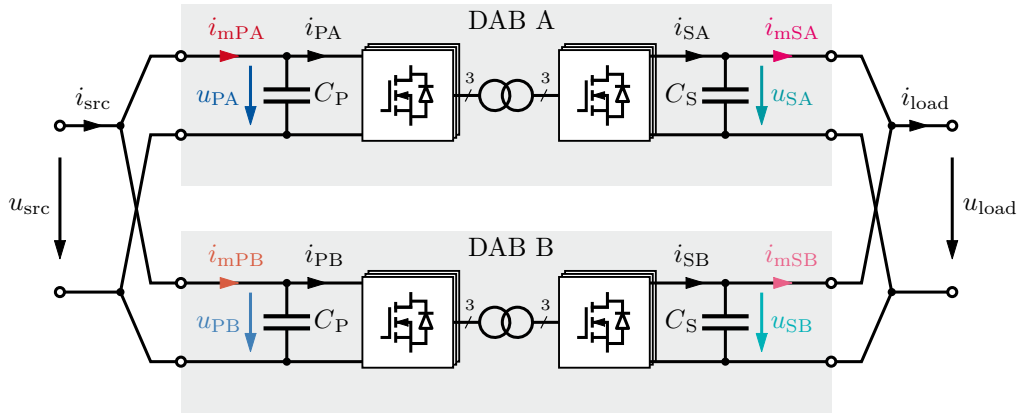
| Parameter | Value |
|---|---|
| Primary-side dc-link voltage range | 600 V…800 V |
| Secondary-side dc-link voltage range | 600 V…750 V |
| Nominal power | 100 kW |
| Switching frequency | 50 kHz |
| Transformer turns ratio | 1:1 |
| Transformer stray inductance, per phase | 4 µH |
| Primary-side dc-link capacitance | 120 µF |
| Secondary-side dc-link capacitance | 120 µF |
| SiC MOSFET modules | Infineon FF6MR12W2M1_B11 |
| Gate resistance | 1.8 Ω |
| Gate drive voltage | −5 V off, 15 V on |
| Dead time | 300 ns |
| Water coolers | IQ evolution IQ-Big53 |

research project "ConverT"[(i)] demonstrated a galvanically isolated, bidirectional OBC rated 200 kW for catenary trucks [105, 122, 127]. The control of this particular dc-dc converter is discussed in this chapter.

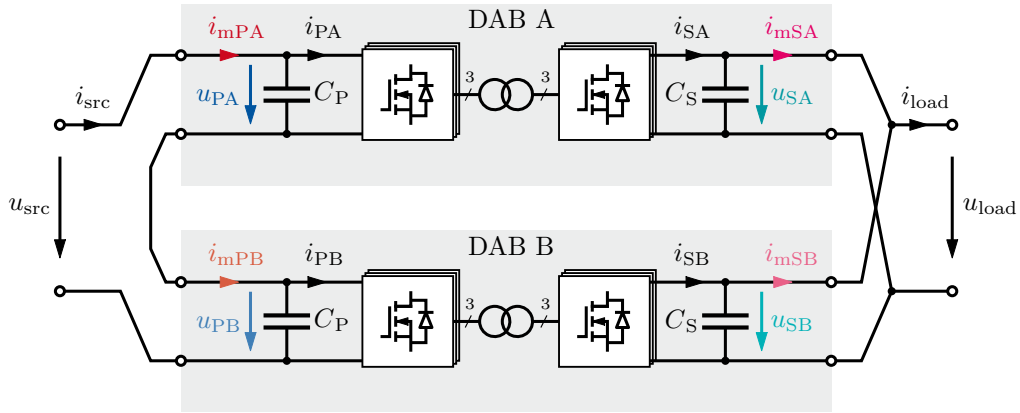
The dc-dc converter consists of two three-phase dual-active bridges (DABs) rated 100 kW each, acting as PEBBs. As semiconductor devices, 1200 V silicon carbide (SiC) MOSFETs are used, which enables a high switching frequency of 50 kHz. Further electrical parameters of a single PEBB are listed in Table 4.1. As the battery voltage is in the range of 600 V…750 V, both PEBBs are connected in parallel on the secondary side. To achieve compatibility with both 600 V and 1200 V catenary voltage levels, however, they can be either connected in parallel or in series on the primary side. These two interconnection variants are called input-parallel output-parallel (IPOP) and input-series output-parallel (ISOP), respectively, and Fig. 4.1 illustrates both configurations. To enable the control of the converter system, the electrical quantities highlighted in color in Fig. 4.1 are measured by sensors. The advantage of this modular hardware approach is not only that it is compatible with both catenary voltage levels, but also that one identical design of the semiconductor bridges can be used for both the primary and the secondary side.

The control design process described in this chapter is supported by simulations. For this purpose, the DABs are realized in the simulation software PLECS Blockset, embedded into Simulink. This simulation model and the control algorithms, which are implemented in C code, are executed within Simulink. This approach is called software in the loop (SiL). The advantage of the SiL approach is that the same software can be used in the subsequent experimental validation, in which it is executed not on the PC, but on the microcontroller (MCU) with the actual converter hardware. This approach eliminates sources of error when migrating from a Simulink model to C code. The three-phase DABs are operated under single phase shift (SPS) modulation exclusively using the open-loop

[(i)] Funded by the German Federal Ministry for the Environment, Nature Conservation, Nuclear Safety, and Consumer Protection (BMUV) under funding code 16EM4009-2, final report available online [122]




(a) IPOP interconnection




(b) ISOP interconnection

Figure 4.1: Interconnection variants of the two DABs in Chapter 4. Electrical quantities highlighted in color are measured

control regime from Fig. 3.4, making them behave like highly dynamic, controlled current sources. By implementing the instantaneous flux and current control (IFCC) and the soft start-up and shut-down algorithms from [101] and [111], respectively, any change of the operating point can be performed within one switching period.

In summary, the modular dc-dc converter under investigation is an OBC for catenary trucks consisting of two three-phase DABs rated 100 kW each. To achieve compatibility with both 600 V and 1200 V, a control method needs to be developed that allows the dc-dc converter system to operate either in IPOP or in ISOP interconnection.

## 4.2 The Back-to-Back Experiment

The so-called back-to-back (B2B) experiment is a commonly used method to commission and characterize dc-dc converters in the laboratory without the need for expensive high-power sources or loads. In this experiment, two converters are connected in IPOP interconnection and transfer power in opposite directions, such that a circulating power flow is established. This way, the power supply has to deliver only the losses to the system, which are usually at least one order of magnitude lower than the transferred power. Similarly, there is also no need to dissipate all the rated power in a load anymore. In many cases, the downside of this approach is that a second, potentially expensive, prototype has to be built to enable the circulating power flow.

The exact topology of this experiment varies, depending on the dc-dc converter topology, its voltage ratings at the input and output, and whether it is bidirectional or not. For the OBC discussed in this chapter, it consists of two three-phase DABs rated 100 kW each, which already eliminates the need for a second prototype to conduct a B2B experiment. Since the voltage ratings of the primary and the secondary side are equal as well, the simple IPOP interconnection shown in Fig. 4.1a can be exploited. Figure 4.2 shows the resulting interconnection. On the primary side, a single dc power supply can be used that only has to deliver the losses of the system. Both DABs operate in a way that they transfer currents of opposite signs, resulting in a circulating power. Hence, if both DABs transfer the rated power of 100 kW, this scenario is electrically equivalent to a full 200 kW charging process in an OBC because reversing the current direction in one DAB does not make an electrical difference due to the symmetry of the topology.

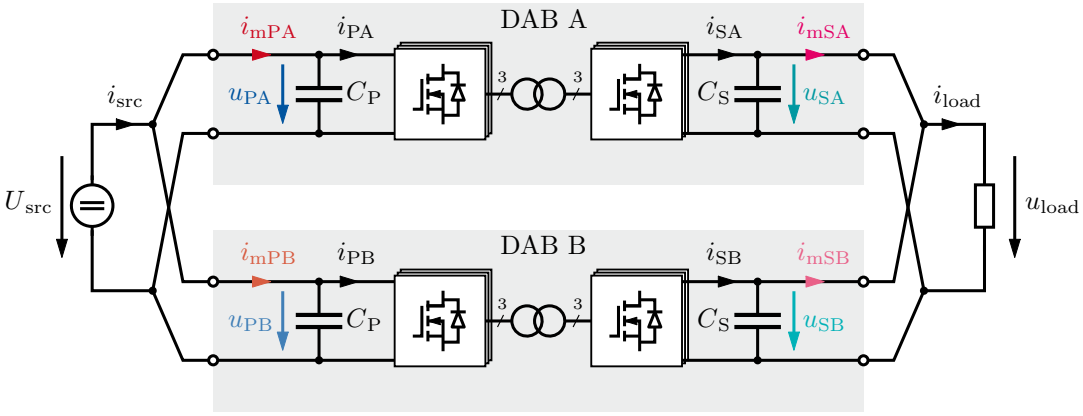



Figure 4.2: Schematic of a B2B experiment using the two DABs from Chapter 4

In the B2B experiment, also the current and the voltage have to be controlled, similarly to the OBC application, but simultaneously: On the one hand, the circulating current has to be controlled to the desired level to emulate a certain operating point of the OBC. On the other hand, the secondary side is connected to an unregulated load represented by a load resistance, which calls for a voltage control that precisely keeps the secondary-side

voltage at the desired level[ii]. Before addressing this simultaneous control, first individual current and voltage control loops shall be designed in the following section.

In summary, the B2B experiment is an efficient way to characterize dc-dc converters without the need for high-power dc sources or loads, by interconnecting two converters in IPOP configuration and establishing a circulating power flow that corresponds to the rated power. This way, only the losses have to be delivered to the system. The B2B experiment calls for both the control of the circulating current and the load voltage.

## 4.3 Individual Control Design

Before addressing the control of the interconnected OBC, individual control loops shall be designed. When charging a battery, usually a constant-current (CC) charging mode is employed, followed by a constant-voltage (CV) charging mode when the battery is almost fully charged. This requires the design of both a closed-loop current control and a closed-loop voltage control for the secondary-side current and voltage, respectively.

### 4.3.1 Current Control

First, the current control is considered. Figure 4.3 shows a mixed-domain block diagram, denoting a simplified version[iii] of the control law implemented in discrete time and a model of the physical plant in continuous time. To design a current control, some assumptions about the load have to be made. In the case of an OBC, the battery is modeled as an ideal voltage source that keeps the secondary-side voltage of the converter constant. Hence, the average rectified secondary-side current equals the battery charging current and therefore is the control variable. Acting as the interface between the digital and the physical world, the open-loop control from Fig. 3.4 is utilized, condensed into the block denoted "DAB". In this application, measurements are available at the beginning of every switching period. Hence, the sampling time is equal to the switching period.

To design the current controller, the physical plant from the mixed-domain block diagram in Fig. 4.3 has to be modeled in the $z$ domain, such that a unified model of the closed-loop system in the $z$ domain is obtained. As already discussed, the implemented IFCC algorithm applies any commanded current $\bar{i}_{\mathrm{S}}^{\triangledown}$ within one switching period, so that it can be measured in the following sampling instant. Therefore, the model of the plant

[ii] Usually, only a discharge resistor is used as load. However, for a load that varies over time, the load current $i_{\mathrm{load}}$ represents a disturbance input to the control system. To assess the disturbance rejection behavior of the developed control, non-negligible load currents are assumed in this chapter.

[iii] To preserve a good readability of the block diagram, anti-windup measures for the integral controller as well as command limiters are not shown.

is a simple unit delay in the $z$ domain. To model inaccuracies of the open-loop current control, a disturbance input $i_{\mathrm{err}}$ is added. Adding a second unit delay to model the update delay caused by the computation time of the control platform, the model in Fig. 4.4 is obtained.

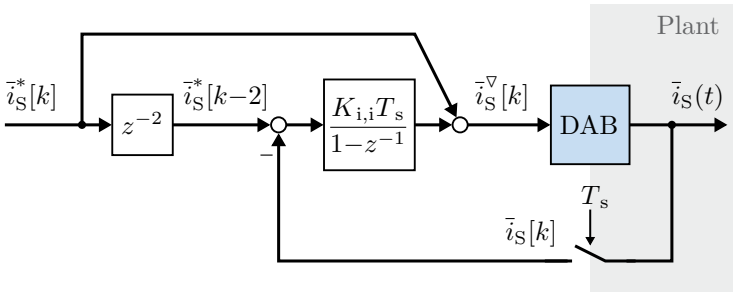



Figure 4.3: Mixed-domain block diagram of the current controller and the physical plant

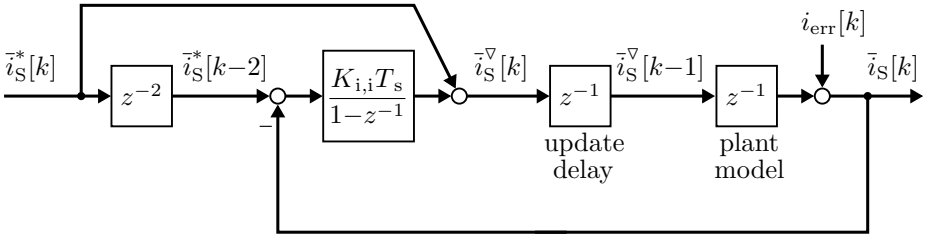



Figure 4.4: Unified discrete-time model of the closed-loop current control including the discrete-time plant model

The current control approach for a three-phase DAB is widely known and can be found in [105, 106], for example. As the open-loop current control from Fig. 3.4 is dynamic and precise, a command feedforward branch is implemented, which directly forwards the reference current to the actuator. It takes two sampling periods, namely one for the update delay and the second one for the IFCC algorithm, until the commanded current can be seen in the feedback branch. Hence, an additional delay of two unit steps needs to be inserted between the reference and the actual controller; otherwise, the comparison between the reference and the feedback value would produce a large error and cause the controller to react, when in reality, this error does not exist. Instead, adding the delay in the reference branch ensures that the reference and the feedback value are consistent with each other, appearing at the same time at the regulator.

An integral regulator with a feedback gain denoted $K_{\mathrm{i,i}}$ is used as feedback controller, which compensates for any error in the current. From Fig. 4.4, the following equation in the $z$ domain can be established for the closed-loop current control:

$$\overline{I}_{\mathrm{S}}(z) = I_{\mathrm{err}}(z) + z^{-2} \cdot \left( \overline{I}_{\mathrm{S}}^{*}(z) + \frac{K_{\mathrm{i,i}}T_{\mathrm{s}}}{1-z^{-1}} \cdot \left( z^{-2} \cdot \overline{I}_{\mathrm{S}}^{*}(z) - \overline{I}_{\mathrm{S}}(z) \right) \right). \tag{4.1}$$

From this equation for the closed-loop system, both the frequency-response function $FRF(z)$, describing the command tracking behavior, and the disturbance-response func-

tion $DR(z)$, describing the disturbance rejection behavior, can be derived:

$$FRF(z) = \left.\frac{\overline{I}_\mathrm{S}(z)}{\overline{I}^*_\mathrm{S}(z)}\right|_{I_\mathrm{err}(z)=0} = z^{-2}, \tag{4.2}$$

$$\begin{aligned} DR(z) &= \left.\frac{\overline{I}_\mathrm{S}(z)}{I_\mathrm{err}(z)}\right|_{\overline{I}^*_\mathrm{S}(z)=0} = \frac{1-z^{-1}}{1-z^{-1}+K_\mathrm{i,i}T_\mathrm{s}z^{-2}} \\ &= \frac{1-z^{-1}}{\left(1-z^{-1}\left(\frac{1}{2}+\sqrt{\frac{1}{4}-K_\mathrm{i,i}T_\mathrm{s}}\right)\right)\cdot\left(1-z^{-1}\left(\frac{1}{2}-\sqrt{\frac{1}{4}-K_\mathrm{i,i}T_\mathrm{s}}\right)\right)}. \end{aligned} \tag{4.3}$$

The frequency-response function (4.2) indicates deadbeat behavior as command tracking property, demonstrating the decoupling from the feedback controller through the additional two unit delays. The numerator of the disturbance-response function (4.3), in turn, demonstrates that the integral feedback can compensate the current error completely, while its denominator describes the dynamics of that compensation. To avoid complex conjugated pole pairs, an upper limit has to be introduced to the integral feedback gain. It also has to be greater than zero to avoid pole-zero cancellation and hence, the compensating property to be lost, effectively reducing the system to a pure open-loop system:

$$0 < K_\mathrm{i,i}T_\mathrm{s} \leq \frac{1}{4}. \tag{4.4}$$

In the case of only real poles, the slower, dominant pole, which is the one closer to $z = 1$, determines the time constant $\tau_\mathrm{d,i}$ of the disturbance rejection [128]:

$$\mathrm{e}^{-T_\mathrm{s}/\tau_\mathrm{d,i}} = \frac{1}{2}+\sqrt{\frac{1}{4}-K_\mathrm{i,i}T_\mathrm{s}} \quad\Rightarrow\quad \tau_\mathrm{d,i} = -\frac{T_\mathrm{s}}{\ln\left(\frac{1}{2}+\sqrt{\frac{1}{4}-K_\mathrm{i,i}T_\mathrm{s}}\right)}. \tag{4.5}$$

Note that the integral regulator is implemented using the Backward Euler method, exhibiting a direct feed-through and no additional delay. This is because the feedback and feedforward branches are already perfectly decoupled, and an additional unit delay in the integral regulator would only delay the disturbance compensation and introduce a third pole in (4.3), which is undesirable. The same holds for adding a proportional regulator; not only would it deteriorate the disturbance rejection dynamics due to a third pole, it would also be of little use, as the plant does not contain any physical integrator.

The current controller is simulated in a SiL simulation together with the model of one DAB. As integral feedback gain, $K_\mathrm{i,i} = 970\,1/\mathrm{s}$ is selected, which corresponds to a time constant of disturbance rejection of $\tau_\mathrm{d,i} = 1\,\mathrm{ms}$. Both the dc-link voltages on the primary and secondary side are set to 600 V. Figure 4.5 shows the simulation results. At $t = 0\,\mathrm{ms}$, a step change in the reference $\overline{i}^*_\mathrm{S}$ from 50 A to 100 A is applied to the system. Due to the feedforward branch and the excellent dynamics of the open-loop current control, an almost deadbeat behavior can be observed as suggested by (4.2). At $t = 3\,\mathrm{ms}$, a step change in the current error $i_\mathrm{err}$ from 0 A to 5 A is applied to the system; for this purpose,

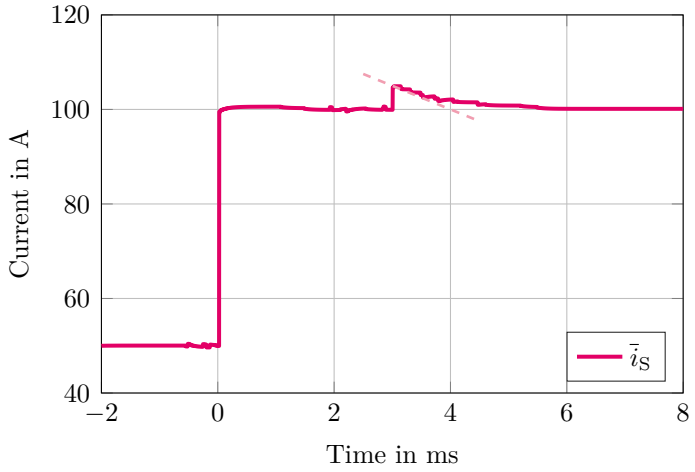



Figure 4.5: SiL simulation of the closed-loop current control, with a reference step from 0 A to 100 A at 0 ms and a disturbance step from 0 A to 5 A at 3 ms

a parasitic, controlled current source has been added to the model. It can be seen that the integral regulator quickly compensates this disturbance step; the time constant of this compensation is indeed approximately 1 ms, as indicated by the dashed line. Small fluctuations in the simulated current are due to the limited quantization of the PWM unit, which can only resolve phase-shift angles down to 4 ns. Other reasons are a limited resolution of the 16-bit floating-point computations of the compiled C code, and sample and hold (S/H) effects because for different phase-shift angles, the actual continuous-time current waveform looks differently, but is sampled at always the same time instant.

In summary, the closed-loop current control consists of a feedforward branch that ensures deadbeat command tracking behavior and an integral regulator to compensate for disturbances and model inaccuracies. The feedforward and the feedback portions of the current controller need to be decoupled to avoid interactions. The time constant of disturbance rejection can be tuned by adapting the integral feedback gain.

### 4.3.2 Voltage Control

In the case of a voltage controller, the secondary-side voltage is not constant, and the average secondary-side rectified current does not equal the load current anymore. Hence, the load current now acts as a disturbance input, which is however measured as Fig. 4.1 indicates. Figure 4.6 shows a mixed-domain model of the physical plant in the continuous time domain with a simplified block diagram of the voltage controller in the discrete time domain.

In contrast to the current controller, which acts dynamically due to the high bandwidth of the IFCC algorithm, the dynamics of the voltage control loop are much slower because

the dc-link capacitor represents a physical energy storage, which prevents abrupt voltage changes. In the following, it is assumed that the bandwidth of the closed control loop is at least a decade lower than the sampling rate, which is equal to the switching frequency. In such situations, the discrete-time voltage controller can even be modeled in continuous time, a so-called quasi-continuous model [76, 128]. Similarly, the open-loop current control with the IFCC algorithm, which acts as manipulated input to the system to manipulate the voltage, can be modeled as a direct feed-through. Again, the inaccuracies of the open-loop current control are modeled as a non-measurable disturbance input $i_{\mathrm{err}}$. The measurable disturbance input to the system, i.e., the load current, however, is measured and added to the output of the feedback controller, such that a disturbance input decoupling is realized. This mostly removes the influence of the load current from the closed-loop control; any remaining measurement errors can be included in the generic, non-measurable disturbance input $i_{\mathrm{err}}$. The result is the model of the closed-loop voltage controller in quasi-continuous time, shown in Fig. 4.7.

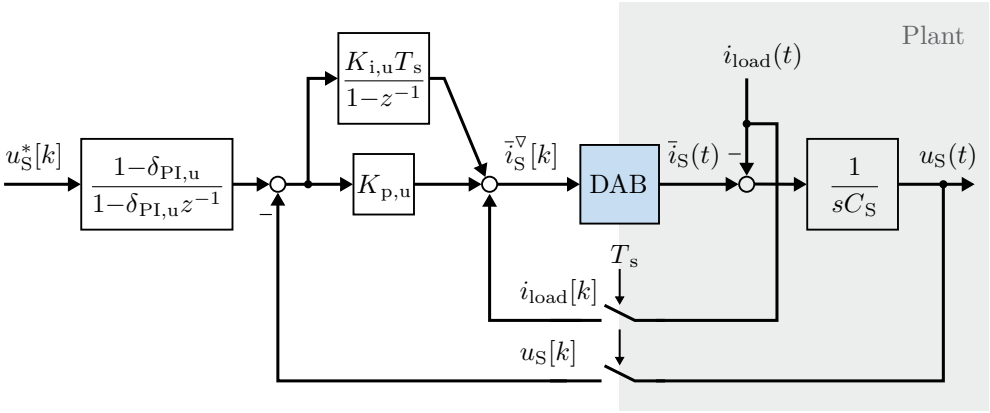



Figure 4.6: Mixed-domain block diagram of the voltage controller and the physical plant

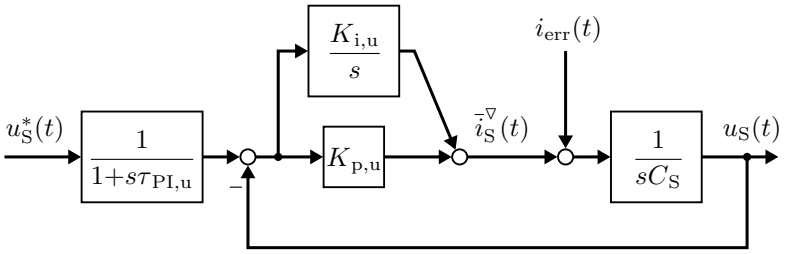



Figure 4.7: Unified continuous-time model of the closed-loop voltage control including the quasi-continuous-time controller model

The closed-loop voltage control shown in Fig. 4.7 is also widely known in literature [105, 106, 128]. It consists of a simple proportional-integral (PI) regulator with a proportional feedback gain denoted $K_{\mathrm{p,u}}$ and an integral feedback gain denoted $K_{\mathrm{i,u}}$. This controller commands a secondary-side rectified current $\bar{i}_{\mathrm{S}}^{\nabla}$ to manipulate the secondary-side voltage. However, PI regulators introduce a zero in the frequency-response function, which may cause overshoots [128]. Therefore, a first-order low-pass filter acting on the reference voltage is added, which exactly compensates that zero with a pole.

From the block diagram in Fig. 4.7, the following equation for the closed-loop voltage controller can be established in the LAPLACE domain:

$$U_{\mathrm{S}}(s) = \frac{1}{sC_{\mathrm{S}}} \cdot \left( I_{\mathrm{err}}(s) + \left( K_{\mathrm{p,u}} + \frac{K_{\mathrm{i,u}}}{s} \right) \cdot \left( \frac{U_{\mathrm{S}}^{*}(s)}{1 + s\tau_{\mathrm{PI,u}}} - U_{\mathrm{S}}(s) \right) \right). \tag{4.6}$$

From this equation, the frequency-response function $FRF(s)$ describing the command tracking properties of the closed-loop voltage controller and the dynamic stiffness function $DS(s)$ describing its disturbance rejection properties can be derived:

$$FRF(s) = \left. \frac{U_{\mathrm{S}}(s)}{U_{\mathrm{S}}^{*}(s)} \right|_{I_{\mathrm{err}}(s)=0} = \frac{K_{\mathrm{p,u}} s + K_{\mathrm{i,u}}}{(1 + s\tau_{\mathrm{PI,u}}) \cdot (C_{\mathrm{S}} s^2 + K_{\mathrm{p,u}} s + K_{\mathrm{i,u}})} \tag{4.7}$$

$$DS(s) = \left. \frac{I_{\mathrm{err}}(s)}{U_{\mathrm{S}}(s)} \right|_{U_{\mathrm{S}}^{*}(s)=0} = \frac{K_{\mathrm{i,u}}}{s} + K_{\mathrm{p,u}} + sC_{\mathrm{S}}. \tag{4.8}$$

The dynamic stiffness function is the inverse of the disturbance-response function and describes which magnitude of the disturbance input would change the output by 1 V at a specific frequency. A large value of the dynamic stiffness characterizes a control loop with good disturbance rejection. Figure 4.8 shows a qualitative plot of the dynamic stiffness with three asymptotes corresponding to each term in (4.8): At high frequencies, the capacitor provides passive disturbance rejection because of its low impedance. In the mid-frequency region, the proportional feedback gain provides disturbance rejection, while for the low-frequency region, the integral regulator provides stiffness. Due to the integration, the stiffness at zero frequency is infinitely high, which means that the closed-loop voltage controller is able to remove any steady-state control error.

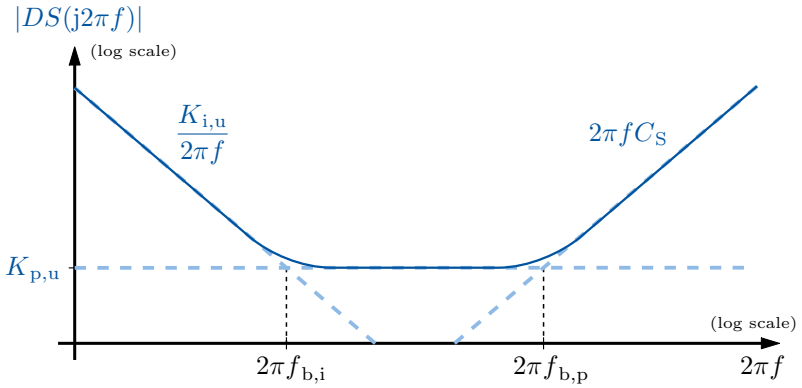



Figure 4.8: Qualitative dynamic stiffness plot of the closed-loop voltage control [128]

The control design is carried out by actively changing the vertical position of the low-frequency and mid-frequency asymptotes, modifying their intersections, a method that is highlighted in greater detail in [128]. The frequency at which the proportional gain is equal to the admittance of the secondary-side dc-link capacitor is called the bandwidth of the proportional feedback and denoted $f_{\mathrm{b,p}}$. In turn, the lower frequency at which the second intersection occurs is called the bandwidth of the integral feedback and denoted $f_{\mathrm{b,i}}$.

From these intersections, the following design equations can be derived:

$$\begin{aligned} K_{\mathrm{p,u}} &= 2\pi f_{\mathrm{b,p}} C_{\mathrm{S}}, \\ K_{\mathrm{i,u}} &= 2\pi f_{\mathrm{b,i}} K_{\mathrm{p,u}}. \end{aligned} \tag{4.9}$$

To achieve a perfect pole-zero cancellation in the frequency-response function (4.7), the time constant of the first-order reference filter has to be chosen equal to

$$\tau_{\mathrm{PI,u}} = \frac{1}{2\pi f_{\mathrm{b,i}}} = \frac{K_{\mathrm{p,u}}}{K_{\mathrm{i,u}}}. \tag{4.10}$$

Unfortunately, the feedback gains cannot be increased to arbitrarily high values to improve the stiffness of the system. Increasing the proportional feedback gain is limited by the limited bandwidth of the proportional regulator; it must stay a decade below the sampling frequency to not violate the assumption of a quasi-continuous system. If the proportional feedback gain was chosen higher, it would interact with the dynamics of the open-loop current control, which then would have to be incorporated into the control design. In turn, increasing the integral feedback gain is also limited, which can be seen by analyzing the system poles in (4.7), already assuming pole-zero cancellation:

$$\begin{aligned} FRF(s) &= \frac{1}{\frac{C_{\mathrm{S}}}{K_{\mathrm{i,u}}} s^2 + \frac{K_{\mathrm{p,u}}}{K_{\mathrm{i,u}}} s + 1} \\ &= \frac{\frac{K_{\mathrm{i,u}}}{C_{\mathrm{S}}}}{\left(s + \left(\frac{K_{\mathrm{p,u}}}{2C_{\mathrm{S}}} + \sqrt{\left(\frac{K_{\mathrm{p,u}}}{2C_{\mathrm{S}}}\right)^2 - \frac{K_{\mathrm{i,u}}}{C_{\mathrm{S}}}}\right)\right) \cdot \left(s + \left(\frac{K_{\mathrm{p,u}}}{2C_{\mathrm{S}}} - \sqrt{\left(\frac{K_{\mathrm{p,u}}}{2C_{\mathrm{S}}}\right)^2 - \frac{K_{\mathrm{i,u}}}{C_{\mathrm{S}}}}\right)\right)} \\ &\overset{(4.9)}{=} \frac{\frac{K_{\mathrm{i,u}}}{C_{\mathrm{S}}}}{\left(s + 2\pi f_{\mathrm{b,p}}\left(\frac{1}{2} + \sqrt{\frac{1}{4} - \frac{f_{\mathrm{b,i}}}{f_{\mathrm{b,p}}}}\right)\right) \cdot \left(s + 2\pi f_{\mathrm{b,p}}\left(\frac{1}{2} - \sqrt{\frac{1}{4} - \frac{f_{\mathrm{b,i}}}{f_{\mathrm{b,p}}}}\right)\right)} \qquad (4.11) \\ &\approx \frac{\frac{K_{\mathrm{i,u}}}{C_{\mathrm{S}}}}{\left(s + 2\pi f_{\mathrm{b,p}}\right) \cdot \left(s + 2\pi f_{\mathrm{b,i}}\right)} \quad \text{for} \quad f_{\mathrm{b,i}} \ll f_{\mathrm{b,p}}. \qquad (4.12) \end{aligned}$$

The last line (4.12) is obtained by using the TAYLOR series expansion of the denominator in (4.11) around $\frac{f_{\mathrm{b,i}}}{f_{\mathrm{b,p}}} = 0$. It demonstrates that whenever the proportional and integral feedback bandwidths are well separated, the system has two real poles, the dominant, slower pole corresponding to the integral feedback bandwidth. Hence, it is desirable to increase the integral gain to improve the system dynamics. According to (4.11), this however results in complex conjugate pole pairs and thus, overshoots or oscillatory system behavior. While this is to some extent acceptable [128], in this dissertation the poles will be kept on the real axis. Therefore, the integral bandwidth should be limited to

$$0 < f_{\mathrm{b,i}} \leq \frac{f_{\mathrm{b,p}}}{4}, \tag{4.13}$$

a similar condition compared to the one developed for the current control in (4.4).

Also the closed-loop voltage control is verified by a SiL simulation. The proportional feedback bandwidth is set to $f_{\mathrm{b,p}} = 2\,\mathrm{kHz}$, which is more than one order of magnitude below the sampling frequency, whereas the integral feedback bandwidth is set to $f_{\mathrm{b,i}} = 500\,\mathrm{Hz}$, which gives a double real pole at a frequency of 1 kHz in the frequency-response function according to (4.11). Again, a constant primary-side dc-link voltage of 600 V is used. Figure 4.9 shows the simulation results. At $t = 0\,\mathrm{ms}$, a step in the reference voltage $u_{\mathrm{S}}^*$ from 50 V to 600 V is applied to the system. It can be observed that the system responds quickly and without any overshoot. The corresponding step response of a system with two poles at 1 kHz is plotted in a dashed line as well, showing a good agreement with the simulation[(iv)]. At $t = 4\,\mathrm{ms}$, the load resistance is abruptly changed from 12 Ω to 9 Ω, which corresponds to a load current step of 16.67 A, drawing 10 kW more power than before. Although this disturbance is measured and decoupled, the controller cannot react immediately due to the update delay and the dynamics of the open-loop current control, and the resulting voltage dip is 5.1 V, i.e., less than 1 % of the load voltage.

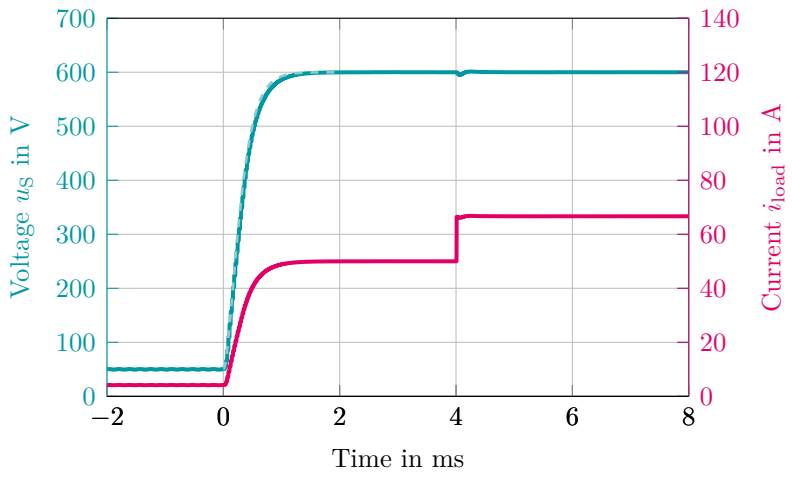



Figure 4.9: SiL simulation of the closed-loop voltage control, with a reference step from 50 V to 600 V at 0 ms and a load resistance step from 12 Ω to 9 Ω at 4 ms

In summary, the voltage controller consists of a simple PI regulator manipulating the average rectified secondary-side current, which directly manipulates the load voltage across the secondary-side dc-link capacitor. The proportional and integral feedback bandwidths are tuned in a way that they do neither interact with the open-loop current control nor cause complex conjugated pole pairs. As the load current is measured, a disturbance input decoupling is implemented. Additionally, a first-order low-pass filter on the reference input compensates for the zero of the PI regulator.

[(iv)] A system with a single pole at 1 kHz would have a time constant of 159 µs, however the simulated system is slower because it has a double pole.

## 4.4 Cross-Coupled Control

After the individual voltage and current controllers have been addressed, the control of a B2B experiment as introduced in Section 4.2 shall be envisaged, which requires a simultaneous control of the load voltage and the circulating current. In the following, the schematic from Fig. 4.2 is assumed for the B2B experiment. This scenario is similar to the CV charging phase of a battery, where the secondary-side voltage has to be controlled. However, a circulating current is only needed in the B2B scenario, which makes it more complex than the CV charging of the battery. In turn, a load resistor $R_{\mathrm{load}}$ is not necessary in a B2B experiment; it is nonetheless included to highlight the effect of the load current $i_{\mathrm{load}}$ on the control performance. Both the presence of the circulating and the load current helps to illustrate how the interconnection of two PEBBs that form a two-converter system influences their behavior as a control plant. The two PEBBs, in this case three-phase DABs, are distinguished by the letters "A" and "B" in the following.

The secondary-side average rectified currents of both DABs, $\bar{i}_{\mathrm{SA}}$ and $\bar{i}_{\mathrm{SB}}$, are selected as manipulated input variables to the system because they are able to manipulate both the load voltage and the circulating current. A straightforward approach when controlling two variables, namely the load voltage and the circulating current, would be to simply assign each control task to one of the two PEBBs. For instance, DAB A can be used to control the load voltage by implementing the voltage control loop from Section 4.3.2, acting on the average rectified secondary-side current of DAB A, $\bar{i}_{\mathrm{SA}}$. Meanwhile, DAB B can be used to control the circulating current by implementing the current control loop from Section 4.3.1, acting on the average rectified secondary-side current of DAB B, $\bar{i}_{\mathrm{SB}}$. Since both manipulated inputs manipulate both control variables, some sort of interaction between the control loops is expected. However, in many publications such allocations of control objectives to individual converters are indeed proposed [40], relying on the assumption that although the control loops interact, there will always be a possibly stable equilibrium point that the two-converter system will eventually reach.

The interaction of the two PEBBs can be mathematically described by analysis of the circuit in Fig. 4.2:

$$\begin{aligned} u_{\mathrm{load}} &= u_{\mathrm{SA}} = u_{\mathrm{SB}}, \\ 2C_{\mathrm{S}}\frac{\mathrm{d}u_{\mathrm{load}}}{\mathrm{d}t} &= \bar{i}_{\mathrm{SA}} + \bar{i}_{\mathrm{SB}} - i_{\mathrm{load}}, \\ i_{\mathrm{mSA}} &= \frac{1}{2}\cdot\left(\bar{i}_{\mathrm{SA}} - \bar{i}_{\mathrm{SB}} + i_{\mathrm{load}}\right) \\ i_{\mathrm{mSB}} &= \frac{1}{2}\cdot\left(\bar{i}_{\mathrm{SB}} - \bar{i}_{\mathrm{SA}} + i_{\mathrm{load}}\right) \end{aligned} \tag{4.14}$$

These equations indicate interactions between the two PEBBs, however this interaction becomes much more clear when they are transferred into the standard state-space representation of a control system as introduced in Section 3.1.2.

The only variable in the system qualifying as state variable due to its energy storing properties is the load voltage $u_{\mathrm{load}}$ because it is related to a stored capacitive energy in the secondary-side dc-link capacitors of both DABs. As already stated, the manipulated inputs to the system are the currents that both DABs deliver, denoted $\bar{i}_{\mathrm{SA}}$ and $\bar{i}_{\mathrm{SB}}$. The load resistor in Fig. 4.2 is just one possibility of an electrical load drawing some load current $i_{\mathrm{load}}$; hence, this load current is considered a disturbance input to the system. Finally, the quantities denoted in color in Fig. 4.2 are the variables that are measured in the system. For the secondary side, these are the dc-link voltages, which are equal to the load voltage, i.e., the state variable, and the terminal currents of both DABs, denoted $i_{\mathrm{mSA}}$ and $i_{\mathrm{mSB}}$, respectively. The terminal currents are considered as the system outputs. Since also the load voltage is measured, it could legitimately qualify as system output; however, in many control systems, the state variables are measured in any case. Including them in the system output vector would only increase the size of the matrix $\mathbf{C}$, adding an identity matrix block to it. For the sake of readability, therefore the state variables are automatically considered as measured and not included in the system output vector. These considerations result in the following definitions for the state, input, and output vectors of the system in state-space representation:

$$\vec{x} = u_{\mathrm{load}}, \quad \vec{u}_{\mathrm{m}} = \begin{pmatrix} \bar{i}_{\mathrm{SA}} \\ \bar{i}_{\mathrm{SB}} \end{pmatrix}, \quad \vec{u}_{\mathrm{d}} = i_{\mathrm{load}}, \quad \vec{y} = \begin{pmatrix} i_{\mathrm{mSA}} \\ i_{\mathrm{mSB}} \end{pmatrix}. \tag{4.15}$$

Using these definitions, the system equations (4.14) can be re-written into standard state-space notation:

$$\begin{aligned} \frac{\mathrm{d}u_{\mathrm{load}}}{\mathrm{d}t} &= \frac{1}{2C_{\mathrm{S}}} \cdot \begin{pmatrix} 1 & 1 \end{pmatrix} \cdot \begin{pmatrix} \bar{i}_{\mathrm{SA}} \\ \bar{i}_{\mathrm{SB}} \end{pmatrix} - \frac{1}{2C_{\mathrm{S}}} \cdot i_{\mathrm{load}} \\ \begin{pmatrix} i_{\mathrm{mSA}} \\ i_{\mathrm{mSB}} \end{pmatrix} &= \frac{1}{2} \cdot \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \cdot \begin{pmatrix} \bar{i}_{\mathrm{SA}} \\ \bar{i}_{\mathrm{SB}} \end{pmatrix} + \frac{1}{2} \cdot \begin{pmatrix} 1 \\ 1 \end{pmatrix} \cdot i_{\mathrm{load}}. \end{aligned} \tag{4.16}$$

Comparing with (3.1), the following state-space matrices can be identified:

$$\begin{aligned} &\mathbf{A} = 0, && \mathbf{B_m} = \frac{1}{2C_{\mathrm{S}}} \cdot \begin{pmatrix} 1 & 1 \end{pmatrix}, && \mathbf{B_d} = -\frac{1}{2C_{\mathrm{S}}}, \\ &\mathbf{C} = \mathbf{0}_{2\times 1}, && \mathbf{D_m} = \frac{1}{2} \cdot \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix}, && \mathbf{D_d} = \frac{1}{2} \cdot \begin{pmatrix} 1 \\ 1 \end{pmatrix}. \end{aligned} \tag{4.17}$$

Here, the matrix $\mathbf{A}$ is zero because the secondary-side dc-link capacitors represent a single, ideal integrator with a pole in the origin of the Laplace plane. Due to the absence of any energy-dissipating elements in the system model such as resistors, there are no dynamics of the open-loop system and the eigenvalue of $\mathbf{A}$ is zero. In turn, the dynamics of the closed-loop system will be determined by the control loop design. The $2 \times 1$ matrix $\mathbf{C}$ also contains only zeros because the measured terminal currents do not depend on the secondary-side dc-link voltage and the latter is not explicitly included in the system output, as already discussed. From the other state-space matrices in (4.17), the interaction

of the two PEBBs becomes mathematically clear. The fully occupied manipulated input matrix $\mathbf{B_m}$ suggests that both DABs contribute to changing the load voltage, therefore assigning this control task to one individual DAB does not make much sense. On the other hand, the measured terminal currents cannot be related to either individual DAB; the fully occupied feed-through matrix $\mathbf{D_m}$ suggests that both manipulated input currents are measurable by both sensors. The reason for both effects is that due to the parallel connection of the two secondary-side dc-link capacitors, any current delivered by one DAB would split and charge both capacitors. Therefore, a current delivered by DAB A is partly measured by the terminal current sensor of DAB B and vice versa. These measured terminal currents are used for the closed-loop circulating current control and for the disturbance input decoupling in the closed-loop voltage control. These obvious cross-coupling effects are even more visible when drawing a block diagram of the cross-coupled system from (4.16) together with a closed-loop voltage controller acting on DAB A and a closed-loop current controller acting on DAB B, shown in Fig. 4.10.

The cross-coupled scenario shown in Fig. 4.10, with DAB A controlling the load voltage and DAB B controlling the circulating current, is also simulated, and the results are shown in Fig. 4.11. The voltage and the current controllers are tuned in the exact same way as if they were controlling individual converters as shown in Fig. 4.5 and Fig. 4.9, respectively. A constant primary-side dc-link voltage of 600 V is assumed. The initial control references to the system are a reference load voltage of 50 V and a reference circulating current of 0 A. Initially, a load resistance of 6 Ω is applied. For $t < 0$ ms, both control goals are reached, as the load voltage matches its reference value and the measured terminal current of DAB B is indeed 0 A. Two reference steps and one disturbance step are applied to the system: At $t = 0$ ms, the load voltage reference is set to 600 V and at $t = 4$ ms, the circulating current reference is increased to 70 A. Additionally, at $t = 6$ ms, the load resistance is changed from 6 Ω to 4 Ω. Several observations can be made in Fig. 4.11: First, and most obviously, the waveforms exhibit significant oscillatory behavior, both on a reference and on a disturbance step, even though the tuning of the control loops is unchanged compared to the previous sections, where they have been designed to have only real system poles. Second, the control loops interact in such a way that they cannot guarantee satisfactory reference tracking; during the transient of the load voltage, for example, DAB B cannot control its terminal current to zero — which is not a surprise, as it has already been discussed that the capacitor charging current also charges the secondary-side dc-link capacitor of DAB B and hence becomes visible as a negative current at its terminal. Third, the simulation showcases that the control configuration is not viable for B2B experiments in which there is a considerable power flow to the load resistor. In such cases, DAB B does essentially not control the circulating current, but rather its measured terminal current; DAB A delivers whatever residual current is required by the load, which cannot guarantee a homogeneous power sharing between both converters, by design of the control loops. Aside from these drawbacks, the control loops are however able to reach their references and be stable.

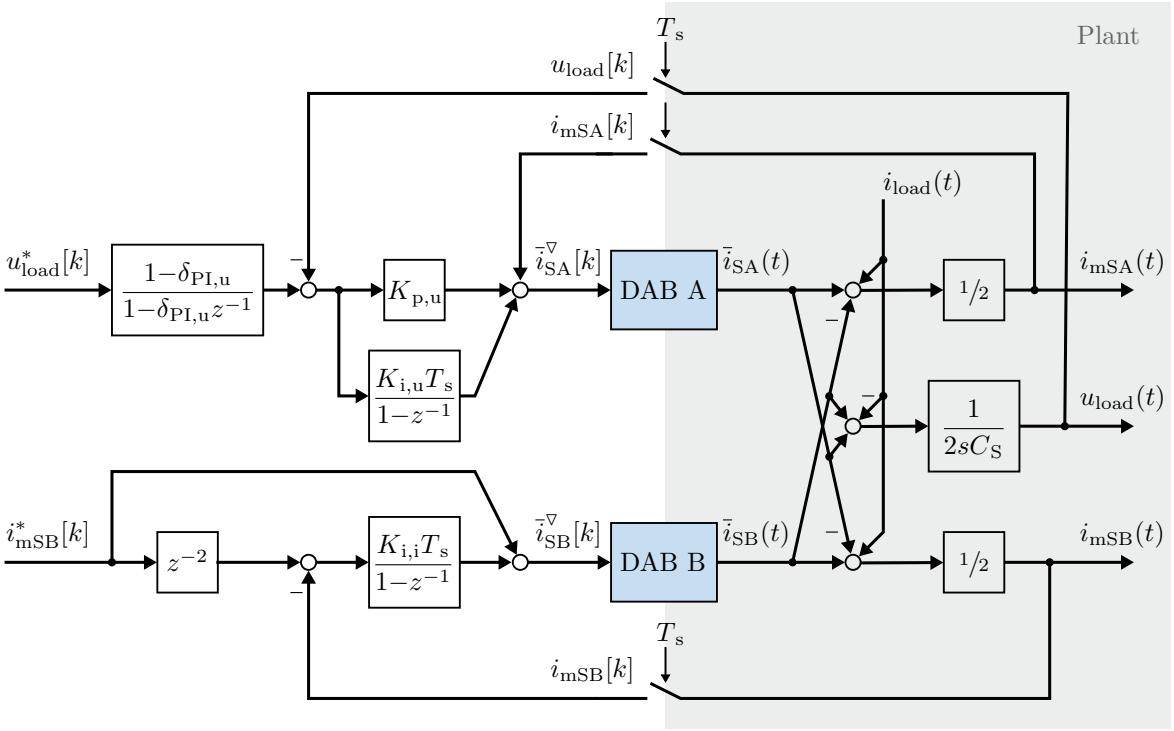



Figure 4.10: Block diagram of two IPOP-interconnected DABs in a B2B experiment, with DAB A controlling the load voltage and DAB B controlling the circulating current, exhibiting a massively cross-coupled plant

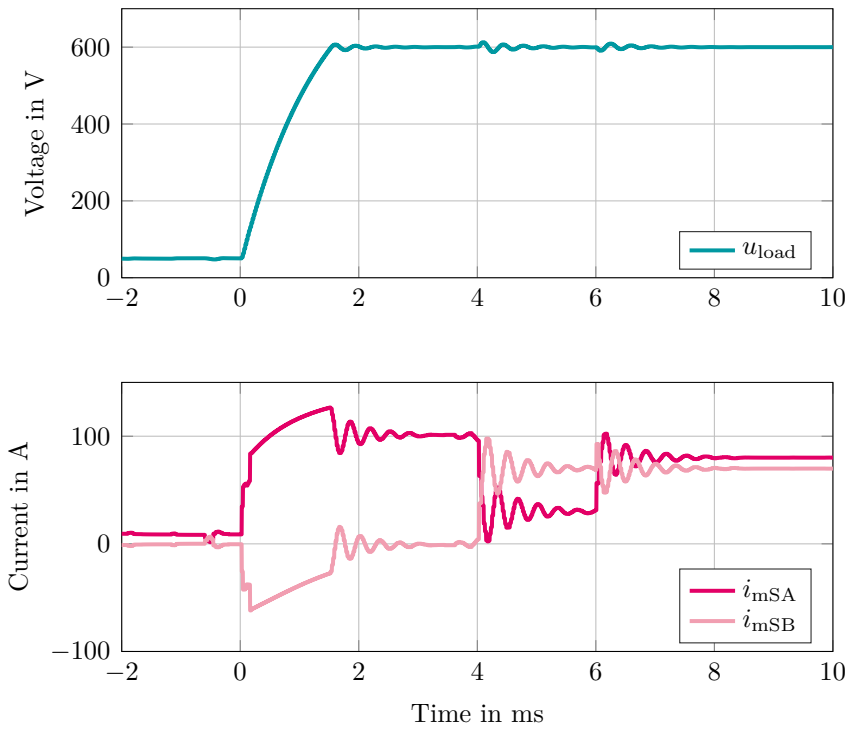



Figure 4.11: SiL simulation of the two IPOP-interconnected DABs in a B2B experiment, with DAB A controlling the load voltage and DAB B controlling the circulating current, exhibiting a massively cross-coupled plant

In summary, assigning individual control tasks to individual PEBBs in an interconnected dc-dc converter does not result in satisfactory control performance because by the mere interconnection of the PEBBs, cross-coupling effects are introduced into the plant model. This has been showcased for the B2B experiment of the OBC, which is discussed in this chapter by deriving the state-space model of the interconnected converter and SiL simulations.

## 4.5 Decoupled Control

It has been shown in the last section that a simple interconnection of two PEBBs to form a modular dc-dc converter creates heavy cross-coupling effects in the model of the control plant that lead to unwanted and oscillatory system behavior due to the interaction of the control loops. However, this way of describing the problem is one-sided because a physical interconnection, an act of hardware, has essentially nothing to do with the control world, which is a mathematical way of looking at the physical world and hence, theoretical. This leads to the suspicion that maybe the way of modeling an interconnected converter system, even though this way of modeling works for a single converter, should be entirely different for a multi-converter system. Now understanding that assigning individual control tasks to converters in a multi-converter system is not the go-to approach and that a multi-converter system has to be modeled under the assumption that all PEBBs act together as a unity, this section aims to develop the right perspective to look at the two-converter system from a control point of view.

Looking at the electrical network equations for the B2B experiment of the OBC in IPOP interconnection as they have been derived in (4.14), it is striking that the sum of the manipulated input variables, namely the average rectified secondary-side currents $\overline{i}_{\mathrm{SA}}$ and $\overline{i}_{\mathrm{SB}}$, appears in the equation for manipulating the load voltage, while the difference of the manipulated input variables appears in both the two equations for the measured terminal currents $\overline{i}_{\mathrm{mSA}}$ and $\overline{i}_{\mathrm{mSB}}$. The sum of the currents, which describes the net power transfer from the primary to the secondary side, directly manipulates the load voltage, while the difference of the currents only describes a power circulation, which cannot charge the secondary-side capacitors. Since any current delivered by one DAB splits and charges both capacitors, the sum of both currents is not measurable by the terminal currents because both partial currents flow in opposite directions in the respective sensor. In contrast, the difference of the currents is measurable at the DAB terminals. This is confirmed by the equations for the measured terminal currents (4.14), which contain the difference and not the sum of the individual currents. These considerations lead to the conclusion that considering both delivered currents $\overline{i}_{\mathrm{SA}}$ and $\overline{i}_{\mathrm{SB}}$ separately is a significantly inferior way of modeling the system compared to selecting the sum of these currents and the difference of these currents as manipulated input variables[(v)].

[(v)] Similar approaches are seen in the control of modular multilevel converters (MMCs) [17]

In the following, the new manipulated inputs to the system are called common-mode (CM) current for the sum of the average rectified secondary-side currents, denoted $\bar{i}_{\mathrm{S,CM}}$, and differential-mode (DM) current for the difference of the average rectified secondary-side currents, denoted $\bar{i}_{\mathrm{S,DM}}$. Mathematically, this process of choosing different manipulated input variables is a linear transformation, i.e., the multiplication of the manipulated input vector with a transformation matrix $\mathbf{T}$:

$$\begin{pmatrix} \bar{i}_{\mathrm{S,CM}} \\ \bar{i}_{\mathrm{S,DM}} \end{pmatrix} = \mathbf{T} \cdot \begin{pmatrix} \bar{i}_{\mathrm{SA}} \\ \bar{i}_{\mathrm{SB}} \end{pmatrix} = \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} \cdot \begin{pmatrix} \bar{i}_{\mathrm{SA}} \\ \bar{i}_{\mathrm{SB}} \end{pmatrix}. \tag{4.18}$$

As already discussed, the idea of considering the sum and the difference of the currents can be applied not only to the manipulated system inputs, but also to the system outputs, i.e., the measured terminal currents. If the transformation matrix $\mathbf{T}$ is applied to the measured currents, this results in

$$\mathbf{T} \cdot \begin{pmatrix} \bar{i}_{\mathrm{mSA}} \\ \bar{i}_{\mathrm{mSB}} \end{pmatrix} = \begin{pmatrix} \bar{i}_{\mathrm{mSA}} + \bar{i}_{\mathrm{mSB}} \\ \bar{i}_{\mathrm{mSA}} - \bar{i}_{\mathrm{mSB}} \end{pmatrix} \overset{(4.14)}{=} \begin{pmatrix} i_{\mathrm{load}} \\ \bar{i}_{\mathrm{S,DM}} \end{pmatrix}. \tag{4.19}$$

This shows that also the sum and the difference of the measured terminal currents makes physical sense. Obviously, the DM current, which can neither charge the capacitors nor flow to the load, is directly measurable. Instead of the CM current, which flows into the capacitors and cannot be measured, the load current is visible in the transformed system output. This already gives the hint that the transformation matrix $\mathbf{T}$ is not just an effective choice to solve an engineering problem, but is rather connected to some underlying, fundamental property of this very specific interconnection of two PEBBs.

Mathematically, it is interesting to derive the state-space system model in CM/DM coordinates to compare it to the cross-coupled version in (4.16). Using (4.18) and (4.19) in (4.16) gives the following version of the state-space model, now in CM/DM coordinates:

$$\begin{aligned} \frac{\mathrm{d}u_{\mathrm{load}}}{\mathrm{d}t} &= \frac{1}{2C_{\mathrm{S}}} \cdot \begin{pmatrix} 1 & 0 \end{pmatrix} \cdot \begin{pmatrix} \bar{i}_{\mathrm{S,CM}} \\ \bar{i}_{\mathrm{S,DM}} \end{pmatrix} - \frac{1}{2C_{\mathrm{S}}} \cdot i_{\mathrm{load}} \\ \mathbf{T} \cdot \begin{pmatrix} i_{\mathrm{mSA}} \\ i_{\mathrm{mSB}} \end{pmatrix} &= \begin{pmatrix} 0 & 0 \\ 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} \bar{i}_{\mathrm{S,CM}} \\ \bar{i}_{\mathrm{S,DM}} \end{pmatrix} + \begin{pmatrix} 1 \\ 0 \end{pmatrix} \cdot i_{\mathrm{load}}. \end{aligned} \tag{4.20}$$

As expected, the system is now perfectly decoupled because every matrix contains only one non-zero entry. This confirms that the CM/DM coordinate system is a superior way of mathematically modeling the physical reality.

The question now arises how to control such a plant that can be mathematically modeled in CM/DM coordinates, despite being physically the same as before. For the system outputs, i.e., the sensor signals, this question is already answered because the sensor signals just have to be transformed into the CM/DM coordinate system by multiplying them with the transformation matrix $\mathbf{T}$ just after sampling. The control laws are then executed in CM/DM coordinates. This means that a voltage controller is implemented as seen in Section 4.3.2, but its output is now a commanded CM current because only the CM

current manipulates the load voltage. In turn, a current control loop is implemented as seen in Section 4.3.1, and its output is a commanded DM current because this is precisely the circulating current that needs to be controlled, and it does not influence the load voltage. However, the output of both controllers are currents in CM/DM coordinates, whereas the actual hardware still requires individual current commands for each of the two individual DABs. Therefore, the commanded currents have to be transformed back by using the inverse of the transformation matrix $\mathbf{T}$.

The block diagram in Fig. 4.12 shows the complete system modeled in CM/DM coordinates. It can be seen that the commanded currents from both controllers are transformed back to individual commands using the inverse transformation matrix. Rather than putting the forward transformation block right after the S/H units, where in reality the transformation is performed, the whole system is shown transformed into CM/DM coordinates by placing the multiplication with the transformation matrix right after the commanded currents of both PEBBs. This way, the decoupling of the system, which only occurs in CM/DM coordinates, becomes visible. Also graphically, it becomes clear that all cross-coupling effects are removed because the two control loops do not share any common signal arrow.

To demonstrate the decoupling, the simulation from Section 4.4 is repeated, but now using the proposed CM/DM transformation, while the tuning of the control loops remains unchanged. Figure 4.13 shows the simulation results. While the second graph shows the measured terminal currents, i.e., the system output without having applied the transformation into CM/DM coordinates, the third graph at the bottom of Fig. 4.13 now shows the transformed system output according to (4.19). As before, two reference steps, one at $t = 0\,\mathrm{ms}$ for the reference load voltage and one at $t = 4\,\mathrm{ms}$ for the reference DM current, are applied to the system, followed by a step change of the load resistance at $t = 6\,\mathrm{ms}$. It can be seen that neither of the two reference steps has any influence on the respective other control variable, only the step change in the load resistance causes a disturbance on the load voltage, which is compensated by the voltage control, but not on the DM current. The small fluctuations in the measured terminal currents before $t < 0\,\mathrm{ms}$ are due to the limited resolution of the PWM unit and a minimum current command of 1 A, which is required to avoid numeric instabilities in the 16-bit floating-point calculations. Note that the DM current control can be utilized to guarantee power sharing between the two DABs when its reference is zero, i.e., for $t < 4\,\mathrm{ms}$.

Coming back to the OBC application, also other interconnection variants with different control tasks were introduced in Section 4.1 beside the B2B experiment. Hence, it shall be examined how to apply the same decoupling approach to another control scenario. For this, the ISOP interconnection from Fig. 4.1b with CC charging of the truck battery shall be considered. In this case, the primary sides share the same dc-link current due to the series connection, which means that any mismatch in the DAB currents will cause the midpoint voltage of the primary-side dc-link capacitors to drift. Therefore, besides the load current, also the midpoint voltage has to be controlled. As before, the CM current describes the net power flow from the primary to the secondary side, and

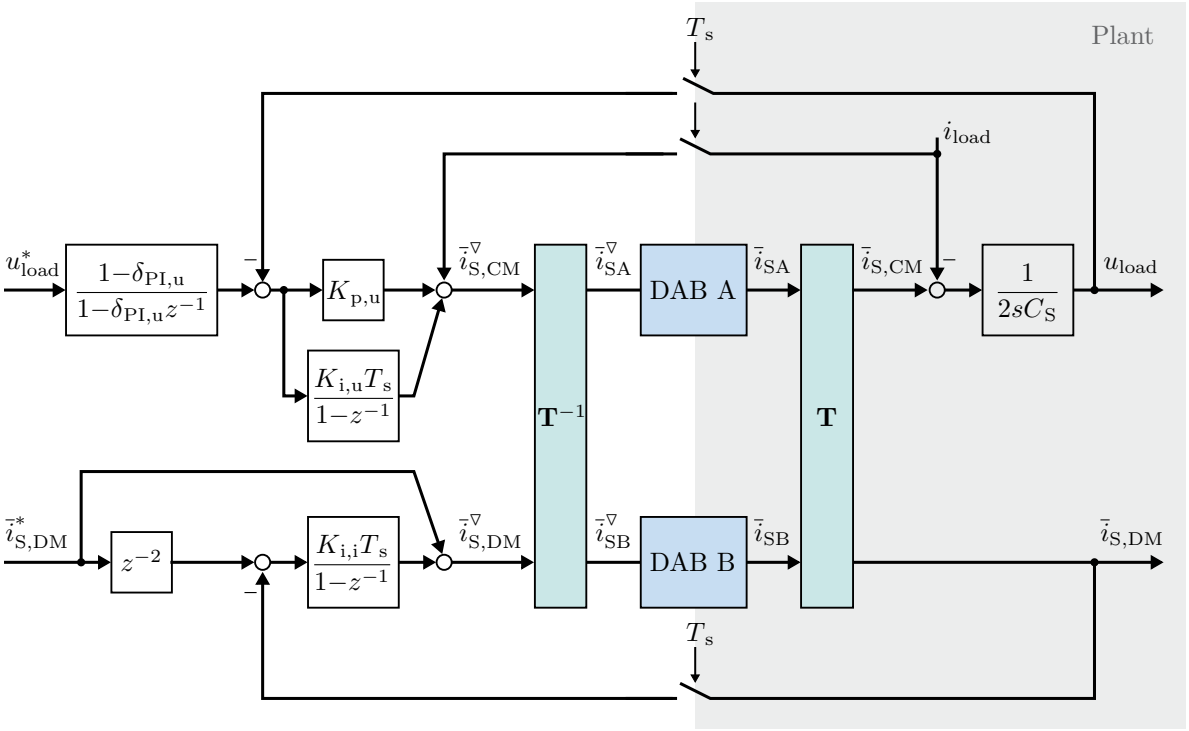



Figure 4.12: Block diagram of two IPOP-interconnected DABs in a B2B experiment in CM/DM coordinates, with a load voltage control loop closed on the CM current and a current control loop closed on the DM current

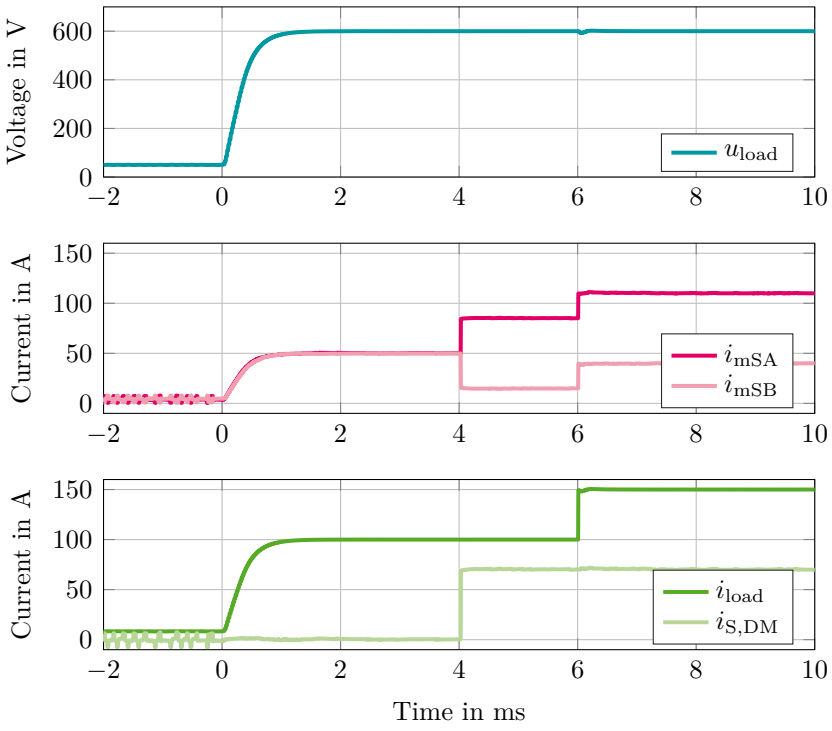



Figure 4.13: SiL simulation of the two IPOP-interconnected DABs in a B2B experiment in CM/DM coordinates, with a load voltage control loop closed on the CM current and a current control loop closed on the DM current

as such, it should be exactly equal to the load current, which is charging the battery. Moreover, a CM current alone causes the currents of both DABs to be identical, which cannot influence the primary-side midpoint voltage. In turn, the DM current describes a pure power circulation, which does not contribute to the battery charging process. Instead, a circulating current always charges one of the two series-connected primary-side dc-link capacitors, while discharging the other one. Hence, the DM current manipulates the primary-side midpoint voltage. This implies that the very same transformation into CM/DM coordinates also enables a decoupled control of the ISOP scenario.

Figure 4.14 shows the block diagram of the decoupled control of the ISOP scenario. Also in this block diagram, the decoupling becomes graphically clear. In the ISOP scenario with CC charging, the current controller now has to command a CM current, while the primary-side midpoint voltage controller now acts on the DM current. One important remark has to be made: the transformation into CM/DM coordinates is still carried out on the secondary-side measured terminal currents, and the transformation of the commanded currents by the controllers is also done with respect to individual secondary-side current commands, with both DABs implementing an open-loop current control of their secondary-side average rectified currents. However, the control variable in the DM loop is a primary-side quantity, which should be influenced by some primary-side DM current, which is yet to be defined, rather than the secondary-side current that is used in Fig. 4.14. Nevertheless, the primary-side and secondary-side circulating currents are related to each other. For equal primary and secondary dc-link voltages, for example, they are almost equal with the exception of the efficiencies of both DABs. For unequal primary and secondary dc-link voltages, however, there might be a considerably high dc offset between the primary and the secondary circulating current. In steady state, a primary-side circulating current of zero is always required to keep the primary-side midpoint voltage constant. However, if the primary-side midpoint voltage is not exactly half of the dc-link voltage, both DABs transfer unequal power, which implies unequal currents on the secondary side, i.e., a non-zero DM current. Nonetheless, this phenomenon can be treated as a disturbance input on the voltage control, which is more significant than the previously assumed disturbance input $i_{\mathrm{err}}$ reflecting model inaccuracies of the open-loop current control. In Chapter 5, this phenomenon is met with a more generalized approach.

In Fig. 4.15, a SiL simulation of the ISOP interconnection with CC battery charging is shown. On the primary side, a dc-link voltage of 1200 V is assumed, while on the secondary side, 600 V are applied to the system. To illustrate the operation of the primary-side midpoint voltage control, the reference primary-side midpoint voltage $u^*_{\mathrm{PB}}$ is initially controlled to 420 V, so well off center. Since the current of the series-connected primary sides must be equal, this results in an unequal power transmission by both DABs. Even though a steady-state condition is reached, which means that the primary-side circulating current is zero, the DM current on the secondary side is nonzero because of the unequal power flow, as explained in the last paragraph. At $t = 0\,\mathrm{ms}$, the reference primary-side midpoint voltage is changed to 600 V, ensuring equal power transmission of both converters. It can be seen that this control goal is achieved by manipulation of the circulating current, which is reflected by transients of opposite signs in the measured

terminal currents on the secondary side, and a transient of the DM current, while the CM battery charging current remains unaffected. After the transient, however, both DABs are transmitting the same power, and the steady-state primary-side circulating current of zero matches a secondary-side DM current of zero, indicating power sharing. At $t = 4\,\mathrm{ms}$, the reference CM current, i.e., the battery charging current, is increased to 100 A. Due to the highly dynamic open-loop current control, this current step can be reached very fast, and the transient does not have any influence on the voltage distribution on the primary side.

In summary, the proposed decoupling approach is effective in mitigating the cross-coupling effects observed in Section 4.4. The origin of these cross-coupling effects has been identified to be a sub-optimal choice of variables. Instead of the individual currents manipulated by both DABs, the sum and the difference of these currents, the CM and DM currents, are a much better option. This choice of manipulated input variables results in a fully decoupled model of the plant, and also applying the same transformation to the system output variables enables to implement fully decoupled control loops. Even more, the proposed coordinate transformation is not only viable for the B2B experiment, with both PEBBs connected in IPOP interconnection, but also for the ISOP interconnection.

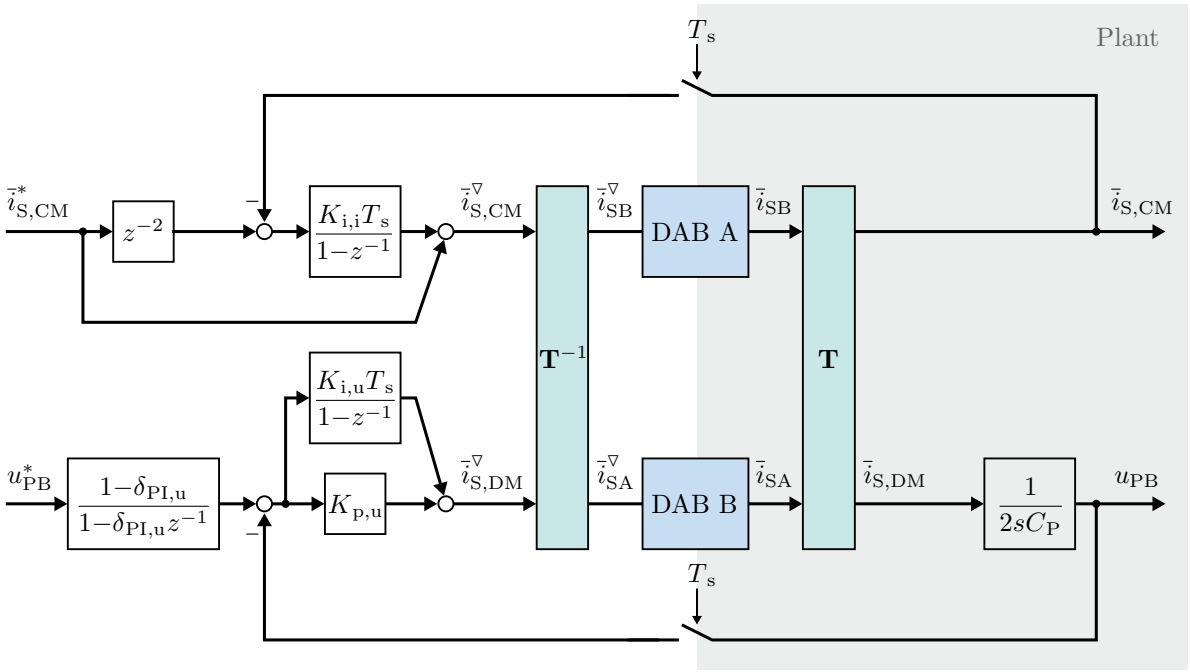



Figure 4.14: Block diagram of two ISOP-interconnected DABs with CC charging in CM/DM coordinates, with a current control loop closed on the CM current and a midpoint voltage control loop closed on the DM current

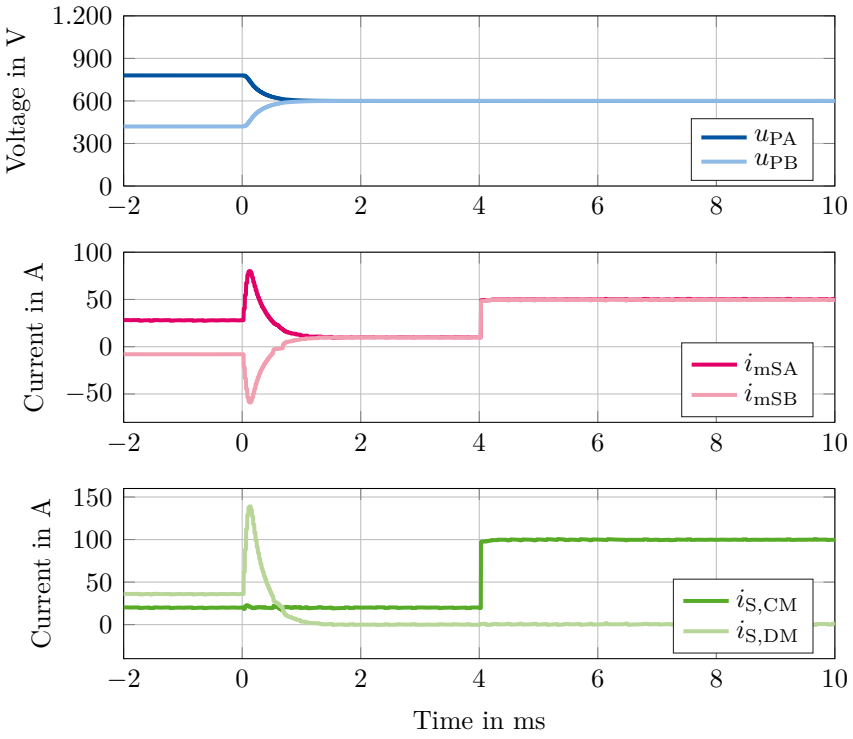



Figure 4.15: SiL simulation of the two ISOP-interconnected DABs with CC charging in CM/DM coordinates, with a current control loop closed on the CM current and a midpoint voltage control loop closed on the DM current

## 4.6 Summary

This chapter introduced an approach to decouple the control loops of a dc-dc converter system consisting of two PEBBs, namely three-phase DABs. As application scenario, a high-power dc-dc converter acting as an OBC for a catenary truck is considered, which consists of two three-phase DABs rated 100 kW each. The two DABs can either be connected in IPOP or ISOP interconnection for compatibility with catenary voltages of 600 V and 1200 V, respectively. Voltage and current control loops for the standalone operation of a DAB have been developed and validated using SiL simulations.

After this, the IPOP interconnection of both DABs has been analyzed during a B2B experiment. In this experiment, the primary-side voltage of both DABs is fixed, while the secondary-side voltage and the circulating current have to be simultaneously controlled. When each of the two control goals is assigned to an individual DAB, i.e., one controls the secondary-side voltage while the other controls the circulating current, the SiL simulation shows significant oscillations of the voltages and currents, although the tuning of the controllers is the exact same as with an individual DAB. Thus, the mere interconnection of two DABs introduces undesired effects in the control loops.

Analyzing the state-space models of the B2B experiment, cross couplings have been identified, making the state-space matrices fully populated. This indicates that the manipulated inputs to the control system, i.e., the currents delivered by both DABs, influence both control goals and also all measured system outputs. The main finding of this chapter is that the individual currents delivered by both DABs are not the right variables to accurately model the interconnected system because both DABs act together as a unity. Instead, the sum of the individual currents, the CM current, and the difference of the individual currents, the DM current, should be chosen as manipulated inputs. The CM current is linked to the net power transfer from the primary to the secondary side and only charges the secondary-side capacitors, while it does not contribute to any circulating current. In turn, the DM current is a purely circulating current, which is invisible to the secondary-side capacitors. Hence, selecting these new manipulated input variables is the optimal way of mathematically modeling a two-converter system.

If this transformation into CM/DM coordinates, which can be expressed as a matrix multiplication, is applied both to the manipulated system input and the measured system output, the system model fully decouples, which has been confirmed mathematically and by SiL simulations. Even more, the same transformation can also be applied to the ISOP interconnection of both DABs, in which the DM current is used to control the midpoint voltage of the series-connected primary-side capacitors to ensure power sharing of the DABs. This suggests that the CM and DM current patterns, which had been found from a purely physical consideration, might play some fundamental, underlying role for interconnections of two PEBBs. Therefore, the following chapter expands this idea to multi-converter systems and investigates the mathematical role of such coordinate transformations.

# 5 Modeling and Control of Arbitrary, Modular DC-DC Converter Systems

In the previous chapter, a control decoupling approach on the basis of a linear coordinate transformation has been discussed for a two-converter system in a physically insightful manner. This chapter extends this approach to an arbitrary number of power-electronic building blocks (PEBBs) forming a multi-converter system. Special emphasis is put on a thorough mathematical interpretation of the physics-based modeling and control of arbitrary, modular dc-dc converter systems. The first section addresses the classification of modular dc-dc converters, making sure that every theoretically possible dc-dc converter interconnection is covered. After this, the generalized state-space representation of a modular dc-dc converter system is discussed, and the role of the proposed coordinate transformation is mathematically contextualized. In the following, the transformation matrices are derived for all theoretically possible dc-dc converter interconnections. Finally, the control design process is discussed for arbitrarily interconnected dc-dc converter systems and the stability is assessed mathematically. Parts of this chapter are published in a condensed form in [129].

## 5.1 Modular Converter System Classification

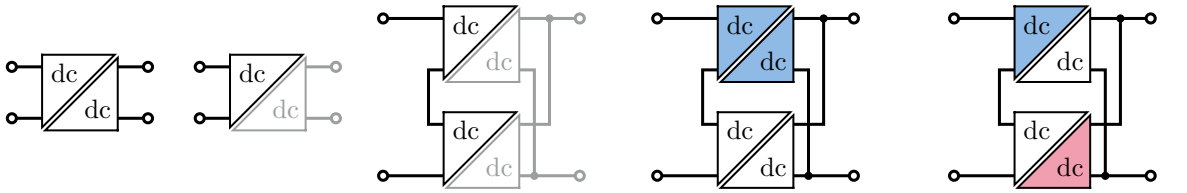
The first section of this chapter has the aim of classifying every possible interconnection variant of a dc-dc converter system consisting of multiple PEBBs. To develop a universal control methodology that is independent of the dc-dc converter topology, it is essential to introduce a layer of abstraction between the functionality of the individual converter unit and the control of the overall converter system. The following sections introduce this layer of abstraction by defining a nomenclature and a universal way of modeling all possible interconnection variants of any converter topology. The result is a classification of modular dc-dc converters into eight different configurations.

### 5.1.1 Modular Converter System Nomenclature

Modular dc-dc converter systems usually consist of many PEBBs, which are interconnected both on the primary and the secondary side. Hence, a nomenclature is useful to not lose oversight. The following wording is used in this dissertation:

- "Converter" or "PEBB" means a single galvanically isolated dc-dc converter with a primary and a secondary side, multiple of which are interconnected to form a "modular converter" or "converter system".
- "Individual converter port" means either the primary or the secondary side of a converter.
- An "interconnected converter port" describes the series, parallel, or mixed interconnection of multiple individual converter ports. An interconnected converter port exists on the primary side, consisting of the interconnection of all primary-side individual converter ports, and an interconnected converter port exists on the secondary side, consisting of the (possibly different) interconnection of all secondary-side individual converter ports.
- "Associated" individual converter ports belong to the same converter, being its primary and its secondary side. Each individual converter port in the primary-side interconnected converter port belongs to the same converter as one individual converter port in the secondary-side interconnected converter port.

These definitions are visualized by Fig. 5.1, using the example of an input-series output-parallel (ISOP) interconnection of two PEBBs. However, the nomenclature is of course applicable to any dc-dc converter system configuration.




(a) Converter or PEBB (b) Individual port (c) Interconnected port (d) Modular converter, marked ports are associated (e) Modular converter, marked ports are not associated

Figure 5.1: Nomenclature for modular dc-dc converter systems exemplified by an ISOP interconnection of two PEBBs

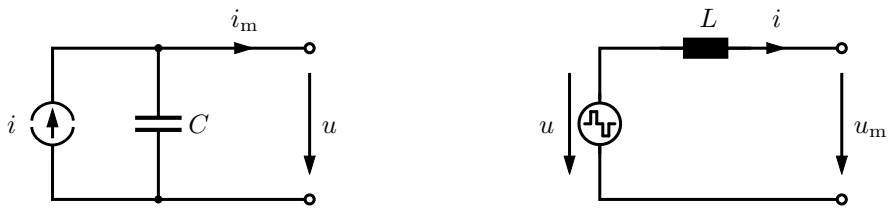
In summary, a comprehensive nomenclature has been defined, which facilitates the classification of any modular dc-dc converter system in the following sections.

### 5.1.2 MC and MV Ports

Previous decoupling approaches presented in the literature assume a certain class of dc-dc converters for the individual PEBB, such as "buck-derived" topologies [33]. This assumes a certain modulation strategy, in this case, PWM with a variable duty cycle acting as manipulated input, and a certain way of operation, i.e., that the average output voltage of the dc-dc converter is equal to its input voltage multiplied by the duty cycle. However, this limits the scope of topologies that can be addressed. In this dissertation, a generalized approach is pursued that comes without any restrictions. To overcome the aforementioned restrictions, a layer of abstraction needs to be introduced between the functionality of the individual PEBB and the control of the modular converter system.

This dissertation proposes a classification scheme for individual converter ports, which allows to model the primary-side or the secondary-side individual port of any dc-dc converter topology in a standardized fashion. Later, the decoupling technique will be developed for an interconnected converter port consisting of multiple of those standardized individual ports. This way, the overall number of interconnection schemes can be reduced significantly and a generalized way of modeling is established. Only at the end of this chapter, Section 5.4 addresses the control of the entire converter system, considering both interconnected ports on the primary and secondary side.

Two individual converter port types are distinguished in this dissertation, which are called "manipulated current (MC)" and "manipulated voltage (MV)" ports. Figure 5.2 shows the equivalent circuits. An MC individual converter port consists of a controlled current source feeding a shunt capacitor, while an MV individual converter port consists of a controlled voltage source feeding a series inductor. From a control perspective, the controlled current source in an MC port and likewise the controlled voltage source in an MV port are the manipulated input to the control plant. Similar classifications have been made in the literature, for example in [63, 67, 68, 72], but under different names, such as "Y-type" and "Z-type", "current-fed" and "voltage-fed", "current-source" and "voltage-source", or "Thévenin form" and "Norton form". This dissertation, however, sticks to the MC and MV nomenclature, for reasons that become clear in the following paragraphs.



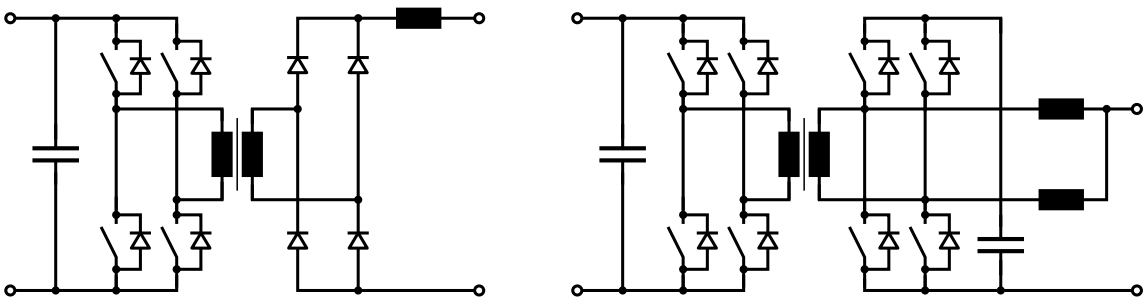

(a) MC port (b) MV port

Figure 5.2: Equivalent circuits of generic individual port types [129]

Determining whether an individual port of some dc-dc converter topology belongs to the MC or MV category is not always unambiguous, as exemplified by the two topologies

depicted in Fig. 5.3. The phase-shifted full-bridge (PSFB) converter shown in Fig. 5.3a consists of a full-bridge circuit at the primary side that switches at 50 % duty cycle, but with a phase-shift angle between the two half bridges. Usually, the parasitic elements of the transformer are neglected in the modeling of the PSFB converter, and a PWM waveform is obtained behind the diode rectifier [130]. Therefore, by changing the phase-shift angle, the average voltage behind the diode rectifier can be manipulated very precisely in an open-loop manner. Hence, the secondary side of the PSFB converter can be modeled as an MV port. In turn, the primary side resembles the equivalent circuit of an MC port from Fig. 5.2a. However, the magnitude of the current cannot be determined in an open-loop manner because it depends on the current in the output inductor. Therefore, making the primary side of the PSFB behave like an MC port is possible, but this would require an internal, closed-loop control of the output inductor current.

Figure 5.3b shows a current-fed dual-active bridge (DAB) converter as it has been introduced in Section 3.3.3. As discussed in Section 3.3.3, the average rectified currents in DAB converters have a nonlinear dependence from the phase-shift angle in single phase shift (SPS) modulation. By inversion of the SPS power transfer characteristic, however, the average rectified currents of the power stages can be manipulated quite precisely. Hence, if the open-loop current control from Section 3.3.3 is applied to the primary-side average rectified current, the primary side of the current-fed DAB converter can be modeled as an MC port. However, there is some ambiguity regarding the secondary side, whose equivalent circuit has been introduced in Fig. 3.9. Since the open-loop current control of a DAB converter can also be applied to the secondary-side average rectified current, which would then feed the secondary-side dc-link capacitor, the galvanically isolated portion of the converter could be legitimately modeled as an MC port as well. In this case, the two current-fed inductors would have to be considered as part of the load. This way of modeling could then be utilized to implement a closed-loop voltage control of the secondary-side dc-link capacitor, for example. Once this voltage is tightly controlled, the secondary side of the current-fed DAB could also qualify as an MV port because the current-fed inductors and the tightly controlled dc-link voltage form the equivalent circuit from Fig. 5.2b.



(a) PSFB converter (b) Current-fed DAB converter

Figure 5.3: Exemplary topologies showcasing MC and MV port classifications

The equivalent circuits in Fig. 5.2 hide a significant portion of the interior operation and the interior dynamics of the converter, which are usually complex. Instead, they

provide controlled current or voltage sources, which are linear circuit elements and hence, very convenient for control purposes. Much emphasis has to be put on the fact that the controlled current or voltage sources have to be directly manipulable; they have to be actively made to behave like current or voltage sources. In some cases, this requirement is easy to meet, but in other cases it may even require an interior closed-loop control. By no means, however, should these equivalent sources supply some imprecise voltage or current that technically results from manipulating some other variable; the supplied current or voltage has to be precise. This is the main reason why the nomenclature is consciously emphasizing the role of the current or voltage source as manipulated input to the exterior of the individual port.

Looking at the MC-type individual port in Fig. 5.2a from a control perspective, the controlled current source acts as a manipulated input to the control plant. The voltage $u$ across the dc-link capacitor is a state variable as it is related to an energy content in the capacitor. By convention, this state variable is assumed to be measured. It is directly manipulated by the controlled current source, i.e., the manipulated input variable. Applying KIRCHHOFF's current law (KCL) to the node in Fig. 5.2a shows, however, that besides the manipulated input, also the terminal current $i_\mathrm{m}$ influences the state variable. Hence, the terminal current $i_\mathrm{m}$ must be considered as a disturbance input to the control system. It is determined by a load that is attached to the port terminals, which can be a current source, a resistor, a constant-power element, or any other load.

For the MV-type individual port in Fig. 5.2b, the same logic applies. In this case, the voltage $u$ is the manipulated input to the system, and the current $i$ in the inductor is the state variable because of its energy-storing property. Applying KIRCHHOFF's voltage law (KVL) to the circuit in Fig. 5.2b shows that the terminal voltage $u_\mathrm{m}$ now plays the role as disturbance input variable. In this case, the load responds to the state variable $i$ with a load voltage $u_\mathrm{m}$. These relationships are summarized in Table 5.1.

Table 5.1: Roles of the electrical variables in MC-type and MV-type ports

| Port type | Manipulated input variable | State variable | Disturbance input variable |
|---|---|---|---|
| MC | Controlled current source $i$ | Capacitor voltage $u$ | Terminal current $i_\mathrm{m}$ |
| MV | Controlled voltage source $u$ | Inductor current $i$ | Terminal voltage $u_\mathrm{m}$ |

Since both MC and MV port types contain one energy storage element, they represent first-order systems from a control point of view. However, there is one important exception, which becomes relevant in later sections: It is possible that the load that is connected to the converter terminals reduces the system to a zero-order system. For an MC-type port, an ideal, constant dc voltage source fixes the voltage across the capacitor such that the terminal current $i_\mathrm{m}$ equals the manipulated input current $i$. In this case, the terminal current is not a disturbance input anymore. Moreover, the energy storage is virtually removed from the system because no current can flow into the capacitor at any time. For an MV-type port, the same logic applies if an ideal dc current source is connected to the port terminals. It removes the inductor as energy storage element, as its current cannot

be changed, and reduces the system to a zero-order system. Since no voltage can drop across the series inductor, the terminal voltage $u_\mathrm{m}$ is equal to the manipulated input $u$ and hence, $u_\mathrm{m}$ is not a disturbance input anymore.

In summary, an individual port of any dc-dc converter topology can be modeled as either a manipulated current source with a parallel-connected capacitor (MC-type port) or as a manipulated voltage source with a series inductor (MV-type port). This distinction is not always unambiguous. It has to be made sure that the current or voltage can be manipulated precisely, either by modulation or by an interior open-loop or closed-loop control scheme. This way of modeling masks the converter-specific behavior and its dynamics into controlled linear sources, which introduces a useful layer of abstraction.

### 5.1.3 Interconnection Schemes

After having discussed the modeling possibilities of an individual converter port, this section discusses the possible interconnection variants of individual converter ports. In a modular dc-dc converter system consisting of multiple galvanically isolated PEBBs, the interconnection of the primary-side individual ports can be completely independent from the interconnection of the secondary-side individual ports. Even more, each primary-side individual port can be associated with any secondary-side individual port; the number of combination possibilities increases dramatically with an increasing number of PEBBs. Therefore, the interconnection variants are explored separately for the primary-side and secondary-side interconnected converter ports.

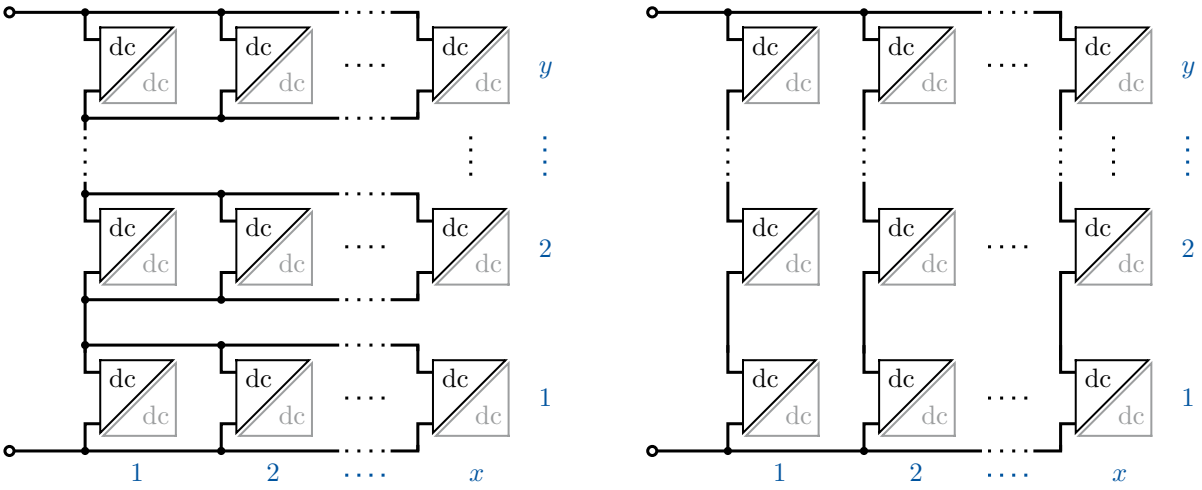
In each interconnected converter port, individual ports can be connected in series or in parallel. In the following, the number of individual ports in an interconnected port is denoted $n$, which is equal to the number of PEBBs. It makes sense to consider only those interconnections that are symmetric, i.e., that contain sub-units of the same number of individual ports connected in series or in parallel. For example, an interconnected port consisting of three individual ports in which one port is connected in series to a parallel connection of two ports would be asymmetric. In order for each port to transfer the same steady-state power, the voltages across the ports would have to be asymmetric. Usually, such configurations are undesired and hence not considered in this dissertation; in any case, the number of possible asymmetric interconnections of $n$ individual ports is very large and cannot be captured mathematically.

If only symmetric interconnection variants are considered, two general interconnection variants can be identified, independent of the number $n$ of individual ports, which are shown in Fig. 5.4. For the individual ports, dc-dc converter blocks are used as symbols; the interconnection variants are shown using the primary-side individual ports, while the interconnection of the secondary-side individual ports is not shown, therefore the secondary-side ports are grayed out. The interconnection variants are differentiated according to whether a parallel connection or a series connection is made first. A nomenclature

for these interconnection variants shall be used that is similar to the nomenclature of battery systems consisting of many battery cells connected in series or in parallel [131]. In an interconnection scheme denoted $x\mathrm{P}y\mathrm{S}$, the designators P and S identify the interconnection type, and the variables $x$ and $y$ determine how many individual ports are connected in parallel (P) or in series (S). The order in which the variables and the designators P and S appear in the nomenclature determines which type of interconnection is made first. For the $x\mathrm{P}y\mathrm{S}$ interconnection shown in Fig. 5.4a, first a number of $x$ individual ports is connected in parallel (P), and then a number $y$ of these units is connected in series (S). For the $y\mathrm{S}x\mathrm{P}$ interconnection shown in Fig. 5.4b, a number of $y$ individual ports is connected in series (S) first, before a number $x$ of those strings is connected in parallel (P). In this nomenclature, the order of the variables $x$ and $y$ as well as the designators P or S cannot be changed without altering the type of interconnection that is meant. For the overall number $n$ of individual ports, the relationship

$$x \cdot y = n \tag{5.1}$$

must always hold for symmetric interconnections. The trivial cases of all $n$ individual converter ports connected in parallel or in series are just special realizations of the aforementioned interconnection variants, where one of the variables $x$ or $y$ is set to one.




(a) $x\mathrm{P}y\mathrm{S}$ interconnection (b) $y\mathrm{S}x\mathrm{P}$ interconnection

Figure 5.4: Symmetric interconnection variants of one interconnected port

In theory, there are even more than two symmetric interconnection variants. They can be generated by alternately connecting the circuits from Fig. 5.4 in series or in parallel. For example, the $x\mathrm{P}y\mathrm{S}$ interconnection from Fig. 5.4a does not change in structure when multiple of those circuits are connected in series. However, if a number of $x\mathrm{P}y\mathrm{S}$ interconnected circuits is connected in parallel, a new structure arises, and if multiple of those new circuits are connected in series, another new structure is created. This alternating series and parallel stacking can be repeated until there are infinitely many interconnection structures. Aside from the fact that infinitely many interconnection structures cannot be analyzed in this dissertation, their practical use would be limited and it would be unlikely

to find such structures in a real application. However, the tools developed in this chapter prove useful in also covering such more complex interconnection variants.

In interconnected ports, the number of state variables depends on the type of interconnection. Connecting MC-type individual ports in parallel does not increase the number of state variables because the capacitors are connected in parallel. Similarly, connecting MV-type individual ports in series does not increase the number of state variables because the inductors are connected in series. Hence, an interconnected converter port in $x\mathrm{P}y\mathrm{S}$ or $y\mathrm{S}x\mathrm{P}$ configuration usually has less than $n$ states. As seen in the previous section, connecting a constant, ideal voltage source to the terminals of an MC-type individual port reduces the number of states by one, from one to zero. Similarly, attaching a constant, ideal voltage source to an interconnection of MC-type individual ports reduces the number of states by one. Without the ideal voltage source, all MC-type ports can influence the common dc-link voltage together, while attaching a constant, ideal voltage source removes this possibility. Similarly, if a constant, ideal current source is attached to an interconnection of MV-type individual ports, the number of states reduces by one as well. Table 5.2 lists the number of state variables for each of the aforementioned scenarios. For a $y\mathrm{S}x\mathrm{P}$ interconnection of MC-type individual ports without an ideal voltage source, for example, there are $(y-1)$ independent voltages in each of the $x$ series-connected branches, plus one common dc-link voltage, giving $x(y-1)+1$ state variables in total.

Table 5.2: Number of state variables for both interconnection variants of MC or MV ports and for different types of load [129]

| Port Type | Load | Interconnection Variant $x\mathrm{P}y\mathrm{S}$ | Interconnection Variant $y\mathrm{S}x\mathrm{P}$ |
|---|---|---|---|
| MC | ideal voltage source | $y-1$ | $x\cdot(y-1)$ |
| | other | $y$ | $x\cdot(y-1)+1$ |
| MV | ideal current source | $y\cdot(x-1)$ | $x-1$ |
| | other | $y\cdot(x-1)+1$ | $x$ |

Table 5.2 shows that eight different scenarios have to be considered, which is done later in this chapter. For each scenario, the state-space model is developed and a decoupling concept is proposed.

In summary, two generic interconnection structures called $x\mathrm{P}y\mathrm{S}$ and $y\mathrm{S}x\mathrm{P}$ have been identified for an interconnected port, with a nomenclature similar to one found in battery systems [131]. The interconnection variants are considered separately for the interconnected ports on the primary and on the secondary side because otherwise the number of possibilities to map each primary-side individual port with each secondary-side individual port would become too large. Considering the different types of individual converter ports and the different types of loads that can be attached to the interconnected converter port terminals, a grand total of eight different structures needs to be considered for the state-space modeling and the development of a decoupling approach.

## 5.2 Decoupling Concept for Interconnected Ports

The previous section addressed the classification of modular dc-dc converter systems, identifying two different individual converter port types, two different interconnection variants for an interconnected converter port, and two load scenarios. This results in eight different interconnected port configurations, for each of which a state-space model and a decoupling concept shall be developed. It is first examined how the coordinate transformation achieving system decoupling can be captured mathematically and how it can be integrated into the state-space model. Then, the role of the eigenvectors of the system matrices in finding the right coordinate transformation are explained. After these preparatory steps, the coordinate transformations of all eight scenarios are developed.

### 5.2.1 State-Space Representation of Interconnected Ports

The starting point for every state-space modeling is the standard state-space model from (3.1). In the following, a uniform definition of the input, state, and output vectors, along with the associated state-space matrices, is discussed for any interconnected converter port regardless of the specific interconnection variant.

As shown in Table 5.1, the manipulated inputs are the controlled current sources of all individual MC ports or the controlled voltage sources of all individual MV ports. For each interconnection, a coordinate system has to be defined by numbering the individual ports, which determines the order in which the controlled sources are arranged into the manipulated input vector $\vec{u}_{\mathrm{m}}$. Its dimension is $n$, the same as the number of PEBBs.

Usually, there is only one single disturbance input $\vec{u}_{\mathrm{d}}$ to an interconnected port. In case of individual MC-type ports, the terminal current of the interconnected port is a disturbance input, unless an ideal voltage source is connected, which reduces the number of state variables by one and also removes the disturbance input. The same applies for individual MV-type ports, where the disturbance input is the terminal voltage of the interconnected port, unless an ideal current source is connected. Hence, the disturbance input vector $\vec{u}_{\mathrm{d}}$ usually consists of only one variable, namely the terminal current or voltage of the interconnected port, or of no variable at all, depending on the load.

The number of state variables, which is denoted $n_x$ in the following, is clearly defined for every interconnection variant according to Table 5.2, however there is still some freedom in the actual choice of the state variables. For a series connection of $y$ MC-type ports without the presence of an ideal voltage source, for example, there are $y$ state variables. While all individual port voltages could be selected as state variables, it would also be possible to select the midpoint voltages as state variables, i.e., the voltages of each node against the negative rail of the interconnected port. Another possibility would be to select the average of all individual port voltages, giving one state variable, and the pair-wise differences

between neighboring individual port voltages, giving $(y-1)$ more state variables. With an ideal voltage source, the number of states reduces to $(y-1)$, where the terminal voltage of the interconnected port is fixed. In this case, the $(y-1)$ midpoint voltages could qualify as state variables, or the pair-wise differences between neighboring individual port voltages. Choosing the state variables often depends on the final application and the control goals that are attached to it, which is discussed further in Section 5.4. In any case, the number of state variables is less or equal to the number of PEBBs, i.e., $n_x \leq n$.

The system outputs are all quantities that are measured in the system. This dissertation assumes that all state variables are measured, however they are not listed again in the output vector $\vec{y}$; this would only add a unity matrix block to the matrix $\mathbf{C}$, which does not provide a lot of information. Table 5.1 shows that for an individual MC-type port, the terminal current $i_\mathrm{m}$ is a disturbance input, and hence it makes sense to measure it. Accordingly, the terminal currents of every individual MC-type converter port are assumed to be known. By using the same coordinate system to be found for arranging the manipulated input variables, these measured terminal currents are arranged into the system output vector $\vec{y}$. Likewise, if the interconnected port consists of MV ports, the measured terminal voltages form the system output vector.

From the previous considerations, the dimensions of the system matrices can be derived. First of all, it is assumed that all states are measured, but not listed in the output vector. Hence, the matrix $\mathbf{C}$ is of the size $n \times n_x$. The system outputs cannot depend on the state variables; in MC-type ports, for example, the capacitor voltage is the state variable, while the system input and output are currents. Due to the absence of resistors in the system and since the current source in an MC port can be controlled independently of any voltage, the states and the output must be independent, also for MV ports. Therefore, the matrix $\mathbf{C}$ contains only zeros, which is denoted $\mathbf{C} = \mathbf{0}_{n \times n_x}$. The matrices related to the disturbance input only exist when this scalar disturbance input exists. Then, the dimension of the disturbance input matrix $\mathbf{B_d}$ is $n_x \times 1$ and the dimension of the disturbance feed-through matrix $\mathbf{D_d}$ is $n \times 1$. In the case of ideal sources connected to the interconnected port, they do not exist. The dimensions of the matrices related to the $n$ manipulated inputs are easy to determine. The manipulated input matrix $\mathbf{B_m}$, which describes how the $n_x$ states are influenced by the $n$ manipulated inputs, has the dimension $n_x \times n$, while the manipulated feed-through matrix $\mathbf{D_m}$, which describes how the $n$ system outputs are directly affected by the $n$ manipulated inputs, has the dimension $n \times n$. Finally, the matrix $\mathbf{A}$ has the dimension $n_x \times n_x$ because it describes the dynamics of the $n_x$ states. However, in the equivalent circuits of MC and MV individual ports in Fig. 5.2, it can be seen that the state variables are only influenced by the manipulated and the disturbance inputs; with all inputs set to zero, there would be no dynamics in the system. Hence, the matrix $\mathbf{A}$ contains only zeros, i.e., $\mathbf{A} = \mathbf{0}_{n_x \times n_x}$. This makes sense because the capacitors in MC-type ports and the inductors in MV-type ports represent ideal integrators. Without any energy-dissipating elements such as resistors, the system state has no own dynamics and the open-loop system poles, i.e., the eigenvalues of $\mathbf{A}$, are all zero. Only implementing a closed-loop control moves the closed-loop system poles away from the origin of the LAPLACE plane to achieve the desired dynamic system response.

Since $\mathbf{A}$ and $\mathbf{C}$ are always zero, a reduced state-space model is used in the following:

$$\begin{aligned} \frac{\mathrm{d}\vec{x}}{\mathrm{d}t} &= \mathbf{B_m}\,\vec{u}_{\mathrm{m}} + \mathbf{B_d}\,\vec{u}_{\mathrm{d}} \\ \vec{y} &= \mathbf{D_m}\,\vec{u}_{\mathrm{m}} + \mathbf{D_d}\,\vec{u}_{\mathrm{d}}. \end{aligned} \tag{5.2}$$

In summary, the controlled current or voltage sources in the individual MC-type or MV-type ports are the manipulated inputs to the control system representing the interconnected port, while the measured terminal currents or voltages are the system outputs, respectively. The state variables are composed of the capacitor voltages of individual MC-type ports or the inductor currents of individual MV-type ports, however, there is a great freedom of choosing the state variables. If an ideal voltage or current source is connected to an interconnected port consisting of individual MC-type or MV-type ports, respectively, there is no disturbance input to the system, otherwise the terminal current or voltage is the only disturbance input. Finally, all entries of the matrices $\mathbf{A}$ and $\mathbf{C}$ have been shown to be zero, therefore a reduced state-space model is used going forward.

### 5.2.2 Coordinate Transformation Based on Eigenvectors

In order to mathematically contextualize the role of the coordinate transformation to decouple the state-space model, the example of the two-converter system from Chapter 4 is revisited. In Section 4.4, the following reduced state-space model was obtained for the back-to-back (B2B) experiment involving two PEBBs:

$$\begin{aligned} \frac{\mathrm{d}x}{\mathrm{d}t} &= \frac{1}{C}\cdot\begin{pmatrix}\frac{1}{2} & \frac{1}{2}\end{pmatrix}\cdot\vec{u}_{\mathrm{m}} - \frac{1}{2C}\cdot u_{\mathrm{d}} \quad = \mathbf{B_m}\,\vec{u}_{\mathrm{m}} + \mathbf{B_d}u_{\mathrm{d}} \\ \vec{y} &= \begin{pmatrix}\frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & \frac{1}{2}\end{pmatrix}\cdot\vec{u}_{\mathrm{m}} + \begin{pmatrix}\frac{1}{2} \\ \frac{1}{2}\end{pmatrix}\cdot u_{\mathrm{d}} = \mathbf{D_m}\,\vec{u}_{\mathrm{m}} + \mathbf{D_d}u_{\mathrm{d}}. \end{aligned} \tag{5.3}$$

Compared to (4.16), the notation is changed to comply with the notation that is used in this chapter; however, the PEBBs are still denoted "A" and "B". Since the topology of the PEBBs is a three-phase DAB, the individual ports can be modeled MC-type ports as shown in Fig. 5.2a, with the port capacitance denoted $C$. Therefore, the manipulated input vector $\vec{u}_{\mathrm{m}}$ consists of the controlled current sources in the MC-type ports, while the system output vector consists of the measured terminal currents:

$$\vec{u}_{\mathrm{m}} = \begin{pmatrix} i_{\mathrm{A}} \\ i_{\mathrm{B}} \end{pmatrix}, \qquad \vec{y} = \begin{pmatrix} i_{\mathrm{mA}} \\ i_{\mathrm{mB}} \end{pmatrix}. \tag{5.4}$$

Since the state-space matrices in (5.3) are fully occupied, every manipulated input variable influences every state variable and every output variable, which indicates cross coupling. To decouple the state-space model, a coordinate transformation has been proposed, which

was applied to the manipulated input vector $\vec{u}_\mathrm{m}$ and to the system output vector $\vec{y}$. This coordinate transformation was expressed by the matrix

$$\mathbf{T} = \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix}. \tag{5.5}$$

In the following, transformed system quantities are denoted with a tilde. Applying the transformation to the manipulated input vector $\vec{u}_\mathrm{m}$ and to the system output vector $\vec{y}$ yields

$$\begin{aligned} \tilde{\vec{u}}_\mathrm{m} &= \mathbf{T} \cdot \vec{u}_\mathrm{m} \\ \tilde{\vec{y}} &= \mathbf{T} \cdot \vec{y}. \end{aligned} \tag{5.6}$$

Inserting the unity matrix $(\mathbf{T}^{-1} \cdot \mathbf{T})$ into the reduced state-space model (5.2) and left-multiplying its second line with $\mathbf{T}$ gives

$$\begin{aligned} \frac{\mathrm{d}\vec{x}}{\mathrm{d}t} &= \mathbf{B_m} \cdot \left(\mathbf{T}^{-1} \cdot \mathbf{T}\right) \cdot \vec{u}_\mathrm{m} + \mathbf{B_d} \cdot \vec{u}_\mathrm{d} \\ \mathbf{T} \cdot \vec{y} &= \mathbf{T} \cdot \mathbf{D_m} \cdot \left(\mathbf{T}^{-1} \cdot \mathbf{T}\right) \cdot \vec{u}_\mathrm{m} + \mathbf{T} \cdot \mathbf{D_d} \cdot \vec{u}_\mathrm{d}. \end{aligned} \tag{5.7}$$

Applying (5.6) results in

$$\begin{aligned} \frac{\mathrm{d}\vec{x}}{\mathrm{d}t} &= \left(\mathbf{B_m} \cdot \mathbf{T}^{-1}\right) \cdot \tilde{\vec{u}}_\mathrm{m} + \mathbf{B_d} \cdot \vec{u}_\mathrm{d} \\ \tilde{\vec{y}} &= \left(\mathbf{T} \cdot \mathbf{D_m} \cdot \mathbf{T}^{-1}\right) \cdot \tilde{\vec{u}}_\mathrm{m} + \left(\mathbf{T} \cdot \mathbf{D_d}\right) \cdot \vec{u}_\mathrm{d}. \end{aligned} \tag{5.8}$$

Equation (5.8) is now a reduced state-space representation of the system transformed into the coordinates defined by the matrix $\mathbf{T}$. The new system matrices can be expressed using the original system matrices and the transformation matrix $\mathbf{T}$ as follows:

$$\begin{aligned} \tilde{\mathbf{B}}_\mathbf{m} &= \mathbf{B_m} \cdot \mathbf{T}^{-1}, & \tilde{\mathbf{B}}_\mathbf{d} &= \mathbf{B_d}, \\ \tilde{\mathbf{D}}_\mathbf{m} &= \mathbf{T} \cdot \mathbf{D_m} \cdot \mathbf{T}^{-1}, & \tilde{\mathbf{D}}_\mathbf{d} &= \mathbf{T} \cdot \mathbf{D_d}. \end{aligned} \tag{5.9}$$

If the actual values of the state-space matrices from (5.3) and the transformation matrix from (5.5) are inserted into the transformed state-space model (5.8), the following decoupled model is obtained:

$$\begin{aligned} \frac{\mathrm{d}x}{\mathrm{d}t} &= \frac{1}{2C} \cdot \begin{pmatrix} 1 & 0 \end{pmatrix} \cdot \tilde{\vec{u}}_\mathrm{m} - \frac{1}{2C} \cdot u_\mathrm{d} = \tilde{\mathbf{B}}_\mathbf{m} \cdot \tilde{\vec{u}}_\mathrm{m} + \tilde{\mathbf{B}}_\mathbf{d} \cdot u_\mathrm{d} \\ \tilde{\vec{y}} &= \begin{pmatrix} 0 & 0 \\ 0 & 1 \end{pmatrix} \cdot \tilde{\vec{u}}_\mathrm{m} + \begin{pmatrix} 1 \\ 0 \end{pmatrix} \cdot u_\mathrm{d} \quad = \tilde{\mathbf{D}}_\mathbf{m} \cdot \tilde{\vec{u}}_\mathrm{m} + \tilde{\mathbf{D}}_\mathbf{d} \cdot u_\mathrm{d}. \end{aligned} \tag{5.10}$$

The decoupled state-space model in (5.10) consists of only diagonal matrices[(i)], which

[(i)] Although the system also contains matrices that are not square, i.e., the matrix $\tilde{\mathbf{B}}_\mathbf{m}$, the term "diagonal" is meant to indicate that only the diagonal entries of the matrices are non-zero, a statement that can also be applied to non-square matrices.

means that every manipulated input variable influences only one variable in the system instead of all of them. The first element in $\tilde{\vec{u}}_{\mathrm{m}}$, for instance, only influences the state variable, while the second element in $\tilde{\vec{u}}_{\mathrm{m}}$ only influences one transformed system output variable. Hence, the multiple-input, multiple-output (MIMO) system from (5.3) decomposed into two independent single-input, single-output (SISO) systems in (5.10). To realize such a decoupling for every possible interconnection of individual converter ports, a universal method to find the transformation matrix $\mathbf{T}$ has to be found.

The multiplication of the transformation matrix $\mathbf{T}$ with the manipulated input vector $\vec{u}_{\mathrm{m}}$ in (5.6) shows that each row of $\mathbf{T}$ acts as a list of weighting factors for the manipulated input variables. For instance, the matrix $\mathbf{T}$ from (5.5) contains two row vectors, namely $\begin{pmatrix}1 & 1\end{pmatrix}$ and $\begin{pmatrix}1 & -1\end{pmatrix}$. When multiplied with the manipulated input vector containing the currents $i_{\mathrm{A}}$ and $i_{\mathrm{B}}$ of the MC-type converter ports, the first row vector $\begin{pmatrix}1 & 1\end{pmatrix}$ produces the sum of those currents, which was called common-mode (CM) current in Chapter 4. In turn, the second row vector $\begin{pmatrix}1 & -1\end{pmatrix}$ produces the difference of the currents when multiplied with $\vec{u}_{\mathrm{m}}$, which was called differential-mode (DM) current. Hence, it can be said that the rows of $\mathbf{T}$ define certain manipulated input patterns to the system.

As already discussed, decoupling is equivalent to diagonalization of the state-space matrices, and as it has been discussed in Chapter 3, diagonalization can be achieved through the left eigendecomposition using the left eigenvectors of the matrix in question. Indeed, looking at the equation for the transformed disturbance feed-through matrix $\tilde{\mathbf{D}}_{\mathbf{m}}$, which is highlighted in blue in (5.9), it can be seen that it is completely equivalent to equation (3.22), which defines the left eigendecomposition of a matrix as introduced in Section 3.2.1. Hence, the CM and the DM current patterns $\begin{pmatrix}1 & 1\end{pmatrix}$ and $\begin{pmatrix}1 & -1\end{pmatrix}$, i.e., the rows of $\mathbf{T}$, are the left eigenvectors of the disturbance feed-through matrix $\mathbf{D}_{\mathbf{m}}$. This makes $\mathbf{T}$ the left modal matrix of $\mathbf{D}_{\mathbf{m}}$. In turn, the diagonalized, or left eigendecomposed, matrix $\tilde{\mathbf{D}}_{\mathbf{m}}$, which is highlighted in blue in (5.10), contains the eigenvalues of $\mathbf{D}_{\mathbf{m}}$ on its diagonal because it is the spectral matrix of $\mathbf{D}_{\mathbf{m}}$. By comparison, it can be identified that the eigenvalue associated with the CM eigenvector is 0, while the eigenvalue associated with the DM eigenvector is 1.

In the B2B experiment that the state-space model describes, the CM current charges the capacitors $C$, hence it influences the states in the interconnected converter port. However, since it charges the capacitors, this CM current pattern cannot be measured at the terminals of the individual MC-type ports. This is reflected by its eigenvalue being zero; those manipulated current patterns in MC-type port interconnections that charge the capacitors, i.e., manipulate the system state, cannot be measured by the sensors. Hence, such current patterns are eigenvectors corresponding to the eigenvalue 0 of the manipulated feed-through matrix $\mathbf{D}_{\mathbf{m}}$, which describes which current patterns can be measured at the system output.

In turn, the DM current describes a purely circulating current in the B2B experiment, which cannot charge any capacitor, and hence it can be freely manipulated. Since it does not charge any capacitor, it can be measured at the terminals of the individual

converter port. Looking at (5.10), the fact that this manipulated current pattern is exactly reproduced by the measured terminal currents without any change in its amplitude confirms that it is an eigenvector of $\mathbf{D_m}$, and that its eigenvalue is 1.

It is expected that this decoupling strategy using left eigenvectors is applicable to any possible interconnected port, not just the B2B experiment. The individual converter ports should not be considered individually; if any individual port applies a manipulated input to the interconnected port, it will change various state variables and it will be measured by multiple sensors because the interconnected port is a cross-coupled system. Instead, all individual converter ports should be considered to operate together as a unity and apply certain patterns of manipulated inputs to the interconnected converter port. If these manipulated input patterns are left eigenvectors of the system matrix $\mathbf{D_m}$ corresponding to the eigenvalue 0, they will not be measurable at the system output, but rather manipulate the system state. In turn, if these manipulated input patterns are left eigenvectors of the system matrix $\mathbf{D_m}$ corresponding to the eigenvalue 1, these patterns will be reproduced without any change in amplitude in the measured system output vector. In the following, the eigenvectors that manipulate the system state, but are invisible at the system output are called "internal eigenvectors" and the corresponding eigenvalue of $\lambda_\mathrm{I} = 0$ is called "internal eigenvalue". In turn, the eigenvectors that do not manipulate the system state, but are replicated at the system output are called "external eigenvectors" and the corresponding eigenvalue of $\lambda_\mathrm{E} = 1$ is called "external eigenvalue".

The question now arises how to find the left eigenvectors of $\mathbf{D_m}$ to build the transformation matrix $\mathbf{T}$ for an arbitrary interconnection scheme. The mathematical approach is to first determine the eigenvalues of $\mathbf{D_m}$ and then, for every eigenvalue, the corresponding left eigenspace. Every base of this eigenspace is then a valid set of eigenvectors corresponding to the examined eigenvalue. However, there is a major inconvenience attached to this strategy: As only two distinct eigenvalues, namely 0 and 1, are expected, but the dimension of the matrix $\mathbf{D_m}$ is $n$, which is usually a large number, the algebraic and geometric multiplicities of the two distinct eigenvalues are expected to be large, too. Simply put, there is likely to be an overwhelming freedom in selecting a set of eigenvectors for each of the two eigenvalues. Hence, a physics-based approach to finding suitable eigenvectors is preferred in the following sections.

One way to find eigenvectors corresponding to the internal eigenvalue of $\lambda_\mathrm{I} = 0$ is already given, namely through the manipulated input matrix $\mathbf{B_m}$ of the system. As already discussed, internal eigenvectors are the manipulated current patterns that change the state variables in the system. However, those manipulated input patterns are given by the rows of the matrix $\mathbf{B_m}$, except for a scaling factor that is denoted $\gamma$. Looking at (5.3), this scaling factor is the capacitance $C$ of the MC-type individual ports. Since scaling factors do not change the property of an eigenvector as such, the port capacitance can just be omitted from $\mathbf{B_m}$ to obtain the internal eigenvectors. This also removes the physical unit from the matrix $\mathbf{B_m}$, and just weighting factors defining current patterns are left over. There must be as many internal eigenvectors $\vec{v}_{\mathrm{I}1}, \ldots, \vec{v}_{\mathrm{I}n_x}$ as system states, namely $n_x$, which must also be the algebraic multiplicity of the internal eigenvalue 0.

These internal eigenvectors can be arranged into the rows of the so-called internal left modal matrix

$$\mathbf{V}_\mathrm{I} = \begin{pmatrix} \vec{v}_{\mathrm{I}1}^{\,\mathrm{T}} \\ \vec{v}_{\mathrm{I}2}^{\,\mathrm{T}} \\ \vdots \\ \vec{v}_{\mathrm{I}n_x}^{\,\mathrm{T}} \end{pmatrix}. \tag{5.11}$$

Naturally, it has to be proven for every interconnected converter port that the vectors obtained from $\mathbf{B_m}$ are indeed internal eigenvectors of $\mathbf{D_m}$ by showing that

$$\mathbf{B_m} \cdot \mathbf{D_m} = \frac{1}{\gamma}\mathbf{V}_\mathrm{I} \cdot \mathbf{D_m} = \mathbf{0}_{n_x \times n}. \tag{5.12}$$

With a straightforward method to find suitable internal left eigenvectors, the question remains how to find the external left eigenvectors corresponding to the eigenvalue $\lambda_\mathrm{E} = 1$, i.e., those manipulated input patterns that are directly measurable at the system output. In the following sections, physically meaningful patterns for the manipulated inputs, just like the DM current, are identified for every interconnection variant. If it can be proven that they do not change after multiplication with the matrix $\mathbf{D_m}$, they can be confirmed as external eigenvectors. Since there are $n$ individual ports and $n_x$ states, it is expected that there are $(n - n_x)$ external eigenvectors denoted $\vec{v}_{\mathrm{E}1}, \ldots, \vec{v}_{\mathrm{E}(n-n_x)}$, which should also be the algebraic multiplicity of the external eigenvalue 1. They can be arranged into the rows of the so-called external left modal matrix

$$\mathbf{V}_\mathrm{E} = \begin{pmatrix} \vec{v}_{\mathrm{E}1}^{\,\mathrm{T}} \\ \vec{v}_{\mathrm{E}2}^{\,\mathrm{T}} \\ \vdots \\ \vec{v}_{\mathrm{E}(n-n_x)}^{\,\mathrm{T}} \end{pmatrix}. \tag{5.13}$$

The final step is to concatenate the internal and external eigenvectors in the internal and external left modal matrices, respectively, to build the transformation matrix $\mathbf{T}$:

$$\mathbf{T} = \begin{pmatrix} \mathbf{V}_\mathrm{I} \\ \mathbf{V}_\mathrm{E} \end{pmatrix}. \tag{5.14}$$

The diagonalization of the matrix $\mathbf{D_m}$ can be shown by using (5.11) and (5.13) in (5.9):

$$\begin{aligned} \tilde{\mathbf{D}}_\mathbf{m} &= \mathbf{T} \cdot \mathbf{D_m} \cdot \mathbf{T}^{-1} = \begin{pmatrix} \mathbf{V}_\mathrm{I} \\ \mathbf{V}_\mathrm{E} \end{pmatrix} \cdot \mathbf{D_m} \cdot \mathbf{T}^{-1} \\ &\overset{(3.18)}{=} \begin{pmatrix} \lambda_\mathrm{I}\mathbf{I}_{n_x} & \mathbf{0}_{n_x \times (n-n_x)} \\ \mathbf{0}_{(n-n_x)\times n_x} & \lambda_\mathrm{E}\mathbf{I}_{(n-n_x)} \end{pmatrix} \cdot \begin{pmatrix} \mathbf{V}_\mathrm{I} \\ \mathbf{V}_\mathrm{E} \end{pmatrix} \cdot \mathbf{T}^{-1} = \begin{pmatrix} \lambda_\mathrm{I}\mathbf{I}_{n_x} & \mathbf{0}_{n_x \times (n-n_x)} \\ \mathbf{0}_{(n-n_x)\times n_x} & \lambda_\mathrm{E}\mathbf{I}_{(n-n_x)} \end{pmatrix} \cdot \mathbf{I}_n \\ &= \begin{pmatrix} \mathbf{0}_{n_x \times n_x} & \mathbf{0}_{n_x \times (n-n_x)} \\ \mathbf{0}_{(n-n_x)\times n_x} & \mathbf{I}_{(n-n_x)} \end{pmatrix}. \end{aligned} \tag{5.15}$$

Even more, from the consideration that the internal eigenvectors are taken from the matrix $\mathbf{B_m}$ with the exception of only a scalar value $\gamma$ and the identity

$$\mathbf{I}_n = \mathbf{T} \cdot \mathbf{T}^{-1} \overset{(5.14)}{=} \begin{pmatrix} \mathbf{V}_\mathrm{I} \cdot \mathbf{T}^{-1} \\ \mathbf{V}_\mathrm{E} \cdot \mathbf{T}^{-1} \end{pmatrix} = \begin{pmatrix} \mathbf{I}_{n_x} & \mathbf{0}_{n_x \times (n-n_x)} \\ \mathbf{0}_{(n-n_x)\times n_x} & \mathbf{I}_{(n-n_x)} \end{pmatrix}, \tag{5.16}$$

it can also be shown that the manipulated input matrix $\mathbf{B_m}$ fully decouples under the transformation (5.9) because the first line in (5.16) suggests

$$\tilde{\mathbf{B}}_\mathbf{m} = \mathbf{B_m} \cdot \mathbf{T}^{-1} = \frac{1}{\gamma} \mathbf{V}_\mathrm{I} \cdot \mathbf{T}^{-1} = \frac{1}{\gamma} \cdot \begin{pmatrix} \mathbf{I}_{n_x} & \mathbf{0}_{n_x \times (n-n_x)} \end{pmatrix}. \tag{5.17}$$

Finally, besides the transformation matrix $\mathbf{T}$, also its inverse is needed. This is because all control loops are executed in decoupled coordinates and determine which eigenvectors should be applied to the system to achieve the desired response. However, from those commands, the individual manipulated inputs have to be reconstructed using the inverse transformation matrix. The inverse can only exist if $\mathbf{T}$ has full rank, hence all found eigenvectors must be linearly independent.

Nevertheless, this section still contains assumptions that have to be proven when actually deriving the state-space models and the transformation matrix for the different interconnected port configurations. Hence, the following step-by-step procedure is followed for every interconnected port configuration, making sure that all the shown identities and assumptions hold:

1. Derive the state-space model and show that the matrix $\mathbf{D_m}$ is real and symmetric, ensuring that there exists a set of linearly independent eigenvectors.
2. Find the eigenvalues of the matrix $\mathbf{D_m}$ and confirm that $\lambda_\mathrm{I} = 0$ is an eigenvalue with multiplicity $n_x$ and that $\lambda_\mathrm{E} = 1$ is an eigenvalue with multiplicity $(n - n_x)$.
3. Prove that the rows of the state-space matrix $\mathbf{B_m}$ are indeed internal eigenvectors by showing (5.12).
4. Find $(n - n_x)$ vectors and prove that they are external eigenvectors of $\mathbf{D_m}$.
5. Finish by constructing the transformation matrix $\mathbf{T}$ from the internal and external eigenvectors. Show that the selected eigenvectors are linearly independent, making sure that $\mathbf{T}$ is invertible.

In summary, decoupling the state-space model of an interconnected port means to diagonalize the state-space matrices, hence the transformation matrix $\mathbf{T}$ must contain eigenvectors of the system. External eigenvectors are manipulated input patterns that, if applied by all individual ports, can be measured at the location of the sensors, hence the external eigenvalue is 1. Internal eigenvectors are those current patterns that change the state of the system, for example, charge the capacitors, but cannot be measured at the location of the sensors, hence the internal eigenvalue is 0. A step-by-step procedure to apply this theory to decouple any converter interconnection has been developed.

## 5.3 State-Space Models and Coordinate Transformations

In the following sections, the step-by-step procedure developed in the previous section is used to find the state-space models and the associated coordinate transformations for every possible interconnection of the two individual converter port types with every possible type of load, as summarized in Table 5.2.

### 5.3.1 xPyS Interconnection of MC Ports

The first of eight interconnection variants to be analyzed is the $x\mathrm{P}y\mathrm{S}$ interconnection of MC-type converter ports without an ideal voltage source, which is shown in Fig. 5.5. In contrast to the equivalent circuit of an individual MC-type port shown in Fig. 5.2a, the directions of the currents have been flipped. This indicates that the interconnected port acts as the power input port to the modular dc-dc converter, which will be useful when analyzing the control of the entire dc-dc converter system in Section 5.4. In the following, the step-by-step strategy from Section 5.2.2 is followed to develop the state-space model and the decoupling matrix.

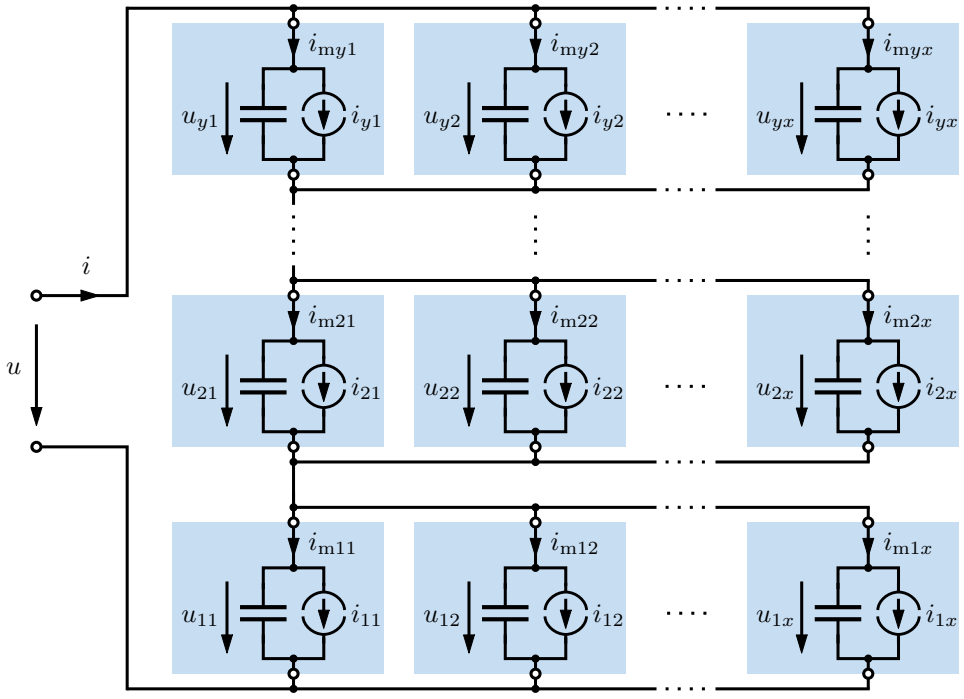



Figure 5.5: $x\mathrm{P}y\mathrm{S}$ interconnection of MC-type ports without ideal voltage source

**Step 1 — Derive the state-space model:** Figure 5.5 defines a certain coordinate system for all individual converter ports based on two indices, which is used for arranging the manipulated input variables and the output variables into their respective vectors. The manipulated inputs, for example, are denoted $i_{pq}$, where $q = 1 \dots x$ counts the individual ports that are connected in parallel, and $p = 1 \dots y$ counts the parallel-connected blocks that are stacked in series. For this interconnection, Table 5.2 suggests that there are $y$ different state variables because there are $y$ converter port blocks connected in series. Out of many possibilities to make a selection of state variables, the voltages across the series-connected blocks are considered the state variables of this interconnection. Since the voltages of all parallel-connected individual converter ports are equal, the following definition is made for simplicity:

$$u_p := u_{p1} = u_{p2} = \ldots = u_{px} \quad \text{for all} \quad p = 1 \dots y. \tag{5.18}$$

With the terminal current $i$ of the interconnected port being the only disturbance variable, the following system vectors are obtained:

$$\begin{aligned} \vec{x} &= \begin{pmatrix} u_1 & u_2 & \dots & u_y \end{pmatrix}^{\mathrm{T}}, \qquad \vec{u}_{\mathrm{d}} = i, \\ \vec{u}_{\mathrm{m}} &= \begin{pmatrix} i_{11} & i_{12} & \dots & i_{1x} & i_{21} & i_{22} & \dots & i_{2x} & \dots & i_{y1} & i_{y2} & \dots & i_{yx} \end{pmatrix}^{\mathrm{T}}, \\ \vec{y} &= \begin{pmatrix} i_{\mathrm{m}11} & i_{\mathrm{m}12} & \dots & i_{\mathrm{m}1x} & i_{\mathrm{m}21} & i_{\mathrm{m}22} & \dots & i_{\mathrm{m}2x} & \dots & i_{\mathrm{m}y1} & i_{\mathrm{m}y2} & \dots & i_{\mathrm{m}yx} \end{pmatrix}^{\mathrm{T}}. \end{aligned} \tag{5.19}$$

In the next step, the basic equations of the system are derived using KCL and the device equations of the capacitors in the system. It is assumed that all port capacitances $C$ are equal. The following equations are found:

$$C\frac{\mathrm{d}u_p}{\mathrm{d}t} = i_{\mathrm{m}p1} - i_{p1} = i_{\mathrm{m}p2} - i_{p2} = \ldots = i_{\mathrm{m}px} - i_{px} \qquad \text{for all} \quad p = 1 \dots y, \tag{5.20}$$

$$i = \sum_{q=1}^{x} i_{\mathrm{m}pq} \qquad \text{for all} \quad p = 1 \dots y. \tag{5.21}$$

Adding all equations from (5.20) together and using (5.21) gives

$$\sum_{q=1}^{x} C\frac{\mathrm{d}u_p}{\mathrm{d}t} = xC\frac{\mathrm{d}u_p}{\mathrm{d}t} \overset{(5.20)}{=} \sum_{q=1}^{x}(i_{\mathrm{m}pq} - i_{pq}) \overset{(5.21)}{=} i - \sum_{q=1}^{x} i_{pq} \quad \text{for all} \quad p = 1 \dots y$$

$$\Rightarrow \quad C\frac{\mathrm{d}u_p}{\mathrm{d}t} = \frac{i}{x} - \frac{1}{x}\sum_{q=1}^{x} i_{pq}. \tag{5.22}$$

This defines the matrices $\mathbf{B_m}$ and $\mathbf{B_d}$ of the reduced state-space representation from (5.2)

as follows, using the conventions (5.19):

$$\mathbf{B_m} = -\frac{1}{xC} \cdot \begin{pmatrix} 1 & 1 & \cdots & 1 & 0 & 0 & \cdots & 0 & \cdots & 0 & 0 & \cdots & 0 \\ 0 & 0 & \cdots & 0 & 1 & 1 & \cdots & 1 & \cdots & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & & \vdots & \vdots & \vdots & & \vdots & \ddots & \vdots & \vdots & & \vdots \\ 0 & 0 & \cdots & 0 & 0 & 0 & \cdots & 0 & \cdots & 1 & 1 & \cdots & 1 \end{pmatrix} = -\frac{1}{xC} \cdot (\mathbf{I}_y \otimes \mathbf{1}_{1\times x}), \tag{5.23}$$

$$\mathbf{B_d} = \frac{1}{xC} \cdot \begin{pmatrix} 1 \\ \vdots \\ 1 \end{pmatrix} = \frac{1}{xC} \cdot \mathbf{1}_{y\times 1}. \tag{5.24}$$

The notation from (5.23) using the KRONECKER product is convenient to save space; it shows that the matrix $\mathbf{B_m}$ consists of $y$ blocks of $x$ ones, which are highlighted in the original matrix. This suggests that every individual converter port in a parallel-connected block has to contribute the same current to change the voltage of the block, which resembles the idea of the CM current from Chapter 4. If the right parts of (5.22) and (5.20) are equated, the following expression can be obtained for the measured currents

$$i_{\mathrm{m}pq} = \frac{i}{x} + i_{pq} - \frac{1}{x}\sum_{r=1}^{x} i_{pr} \quad \text{for all} \;\; p = 1\ldots y \;\; \text{and} \;\; q = 1\ldots x, \tag{5.25}$$

which now defines the matrices $\mathbf{D_m}$ and $\mathbf{D_d}$ of the reduced state-space representation from (5.2) as follows, using the conventions (5.19):

$$\mathbf{D_m} = \frac{1}{x} \cdot \begin{pmatrix} x-1 & -1 & \cdots & -1 & & & \\ -1 & x-1 & \cdots & -1 & & \mathbf{0}_{x\times x} & \\ \vdots & \vdots & \ddots & \vdots & & & \\ -1 & -1 & \cdots & x-1 & & & \\ & & & & \ddots & & \\ & & & & & x-1 & -1 & \cdots & -1 \\ & \mathbf{0}_{x\times x} & & & & -1 & x-1 & \cdots & -1 \\ & & & & & \vdots & \vdots & \ddots & \vdots \\ & & & & & -1 & -1 & \cdots & x-1 \end{pmatrix} = \mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right), \tag{5.26}$$

$$\mathbf{D_d} = \frac{1}{x} \cdot \mathbf{1}_{n\times 1}. \tag{5.27}$$

Also here, the KRONECKER product is used to show that $\mathbf{D_m}$ is a block-diagonal matrix consisting of $y$ sub-matrices with the dimension $x \times x$. This shows that the matrix $\mathbf{D_m}$ is real and symmetric, which implies that there must be a set of $n$ linearly independent left eigenvectors forming an invertible transformation matrix $\mathbf{T}$ to diagonalize $\mathbf{D_m}$.

**Step 2 — Find the eigenvalues:** It is expected that $\mathbf{D_m}$ has the internal eigenvalue of 0 with multiplicity $y$, which equals the number of states, and the external eigenvalue of 1 with multiplicity $(n-y)$, which is shown in the following. Deriving the characteristic polynomial of the matrix $\mathbf{D_m}$ can be done by using various identities from Section 3.2:

$$\begin{aligned}
0 &\overset{!}{=} \det(\mathbf{D_m} - \lambda\mathbf{I}_n) = \det\left(\left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x}\cdot\mathbf{1}_{x\times x}\right)\right) - \lambda\mathbf{I}_n\right) \\
&\overset{(3.26)}{=} \det\left(\left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x}\cdot\mathbf{1}_{x\times x}\right)\right) + (\mathbf{I}_y \otimes (-\lambda\mathbf{I}_x))\right) \\
&\overset{(3.28)}{=} \det\left(\mathbf{I}_y \otimes \left((1-\lambda)\mathbf{I}_x - \frac{1}{x}\cdot\mathbf{1}_{x\times x}\right)\right) \overset{(3.34)}{=} \det\left((1-\lambda)\mathbf{I}_x - \frac{1}{x}\cdot\mathbf{1}_{x\times x}\right)^y \\
&\overset{(3.40)}{=} \left((1-\lambda)^x - x\cdot\frac{1}{x}\cdot(1-\lambda)^{x-1}\right)^y = \left((1-\lambda-1)\cdot(1-\lambda)^{x-1}\right)^y \\
&= (-\lambda)^y \cdot (1-\lambda)^{n-y}. \qquad (5.28)
\end{aligned}$$

The roots of this equation are $\lambda_\mathrm{I} = 0$ and $\lambda_\mathrm{E} = 1$, which confirms the expected eigenvalues and their multiplicities.

**Step 3 — Internal eigenvectors:** The internal eigenvectors of the given system are those current patterns that change the voltages $u_p$ but cannot be measured by the sensors, i.e., they correspond to the internal eigenvalue 0. As already discussed, those patterns can be directly taken from the matrix $\mathbf{B_m}$ derived in (5.23). However, since the matrix $\mathbf{B_m}$ includes the capacitance $C$, all matrix entries represent capacitances. To define current patterns, however, scalar-valued weighting factors are needed, such that the results of their multiplication with the manipulated input current vector are still currents. Hence, $\mathbf{B_m}$ is multiplied by the scalar value $\gamma = C$ to obtain the internal left modal matrix of $\mathbf{D_m}$, leaving only scalar weighting factors that define the internal eigenvectors:

$$\mathbf{V}_\mathrm{I} = -\frac{1}{x}\cdot(\mathbf{I}_y \otimes \mathbf{1}_{1\times x}). \qquad (5.29)$$

It can be shown that $\mathbf{V}_\mathrm{I}$ is the internal left modal matrix of $\mathbf{D_m}$, using (5.26) and (5.29):

$$\begin{aligned}
\mathbf{V}_\mathrm{I}\cdot\mathbf{D_m} &= \left(-\frac{1}{x}\cdot(\mathbf{I}_y \otimes \mathbf{1}_{1\times x})\right)\cdot\left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x}\cdot\mathbf{1}_{x\times x}\right)\right) \\
&\overset{(3.26)}{=} \left(\mathbf{I}_y \otimes \left(-\frac{1}{x}\cdot\mathbf{1}_{1\times x}\right)\right)\cdot\left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x}\cdot\mathbf{1}_{x\times x}\right)\right) \\
&\overset{(3.29)}{=} (\mathbf{I}_y\cdot\mathbf{I}_y) \otimes \left(\left(-\frac{1}{x}\cdot\mathbf{1}_{1\times x}\right)\cdot\left(\mathbf{I}_x - \frac{1}{x}\cdot\mathbf{1}_{x\times x}\right)\right) \\
&= \mathbf{I}_y \otimes \left(-\frac{1}{x}\cdot\mathbf{1}_{1\times x} + \frac{1}{x^2}\cdot\mathbf{1}_{1\times x}\cdot\mathbf{1}_{x\times x}\right) \\
&= \mathbf{I}_y \otimes \left(\left(-\frac{1}{x} + \frac{x}{x^2}\right)\cdot\mathbf{1}_{1\times x}\right) = \mathbf{I}_y \otimes \mathbf{0}_{1\times x} = \mathbf{0}_{y\times n} = \lambda_\mathrm{I}\cdot\mathbf{V}_\mathrm{I}. \qquad (5.30)
\end{aligned}$$

This proves that the current patterns defined in (5.29) are internal eigenvectors of $\mathbf{D_m}$, i.e., they are not measurable by the sensors.

**Step 4 — External eigenvectors:** The external eigenvectors of the given system are those current patterns that can be measured by the sensors without any change, but do not influence the voltages $u_p$, i.e., they correspond to the external eigenvalue 1. These eigenvectors are not provided by any other system matrix, and there is a great freedom of choosing them. Here, DM current patterns shall be defined as the difference of neighboring, parallel-connected individual converter ports, which is reminiscent of the definition of the DM current from Chapter 4. Hence, there are $(x-1)$ DM currents for each of the $y$ series-connected blocks, giving $(n-y)$ DM currents in total, as required. They describe circulating currents that can be measured by the sensors, but cannot charge any capacitors in the interconnected port. The aforementioned definition of the DM currents can be expressed mathematically by defining the external left modal matrix as follows:

$$\mathbf{V}_\mathrm{E} = \mathbf{I}_y \otimes \begin{pmatrix} 1 & -1 & 0 & \cdots & 0 \\ 0 & 1 & -1 & \cdots & 0 \\ \vdots & & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 & -1 \end{pmatrix} =: \mathbf{I}_y \otimes \mathbf{V}_\mathrm{E}^{\square}. \tag{5.31}$$

Here, $\mathbf{V}_\mathrm{E}^{\square}$ is a $(x-1) \times x$ matrix defining the DM currents for one parallel-connected converter block, and the KRONECKER product with the $y \times y$ unity matrix repeats this pattern for all $y$ series-connected converter blocks along the diagonal of $\mathbf{V}_\mathrm{E}$. To prove that this matrix contains external eigenvectors of the matrix $\mathbf{D_m}$, it shall be left-multiplied with the matrix $\mathbf{D_m}$. Indeed,

$$\begin{aligned} \mathbf{V}_\mathrm{E} \cdot \mathbf{D_m} &= \left(\mathbf{I}_y \otimes \mathbf{V}_\mathrm{E}^{\square}\right) \cdot \left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right)\right) \\ &\overset{(3.29)}{=} \mathbf{I}_y \otimes \left(\mathbf{V}_\mathrm{E}^{\square} \cdot \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right)\right) = \mathbf{I}_y \otimes \left(\mathbf{V}_\mathrm{E}^{\square} - \frac{1}{x} \cdot \mathbf{V}_\mathrm{E}^{\square} \cdot \mathbf{1}_{x\times x}\right) \\ &= \mathbf{I}_y \otimes \left(\mathbf{V}_\mathrm{E}^{\square} - \mathbf{0}_{(x-1)\times x}\right) = \mathbf{I}_y \otimes \mathbf{V}_\mathrm{E}^{\square} \overset{(5.31)}{=} \mathbf{V}_\mathrm{E} = \lambda_\mathrm{E} \cdot \mathbf{V}_\mathrm{E}, \end{aligned} \tag{5.32}$$

which proves the DM current patterns to be external eigenvectors.

**Step 5 — Transformation matrix:** Finally, the transformation matrix $\mathbf{T}$ of the $x$P$y$S interconnection of MC-type ports without ideal voltage source can be built by concatenating the internal and external left modal matrices vertically according to (5.14):

$$\mathbf{T} = \begin{pmatrix} \mathbf{V}_\mathrm{I} \\ \mathbf{V}_\mathrm{E} \end{pmatrix} = \begin{pmatrix} 1 & 1 & 1 & \cdots & 1 & & 0 & 0 & 0 & \cdots & 0 \\ & & & & & \ddots & & & & & \\ 0 & 0 & 0 & \cdots & 0 & & 1 & 1 & 1 & \cdots & 1 \\ 1 & -1 & 0 & \cdots & 0 & & & & & & \\ 0 & 1 & -1 & \cdots & 0 & & & & & & \\ \vdots & & \ddots & \ddots & \vdots & & & \mathbf{0}_{(x-1)\times x} & & & \\ 0 & 0 & \cdots & 1 & -1 & & & & & & \\ & & & & & \ddots & & & & & \\ & & & & & & 1 & -1 & 0 & \cdots & 0 \\ & & & & & & 0 & 1 & -1 & \cdots & 0 \\ & \mathbf{0}_{(x-1)\times x} & & & & & \vdots & & \ddots & \ddots & \vdots \\ & & & & & & 0 & 0 & \cdots & 1 & -1 \end{pmatrix}. \tag{5.33}$$

Finally, the linear independence of the eigenvectors needs to be proven. This proof is not necessary for the linear independence between any pair of internal and external eigenvectors because eigenvectors corresponding to different eigenvalues are always linearly independent [81]. However, it still has to be shown that the internal eigenvectors are pair-wise linearly independent and that the external eigenvectors are pair-wise linear independent. Looking at the rows of $\mathbf{B_m}$ in (5.23), the linear independence of the internal eigenvectors is evident. Similarly, looking at the rows of $\mathbf{V}_\mathrm{E}$ in (5.31), the linear independence of the external eigenvectors is also evident.

In summary, the state-space model and the transformation matrix have been developed for the $x$P$y$S interconnection of MC-type converter ports without ideal voltage source. The internal eigenvectors have been selected in terms of the sum of the currents in a parallel-connected block of individual converter ports, manipulating their common voltage. The external eigenvectors have been selected in terms of the pair-wise current differences between neighboring individual converter ports in those parallel-connected blocks.

### 5.3.2 xPyS Interconnection of MC Ports with Ideal Voltage Source

The next interconnection variant of MC-type individual ports exhibits still the same $x$P$y$S structure, but this time with an ideal voltage source connected to the terminals of the interconnected port. This reduces the number of state variables by one. Figure 5.6 shows the schematic of this interconnection variant.

**Step 1 — Derive the state-space model:** There are two major differences between this case and the previously analyzed one without ideal voltage source. First, the number of state variables is reduced by one because the ideal voltage source fixes the voltage across the interconnected port terminals. This makes it necessary to find a new set of state

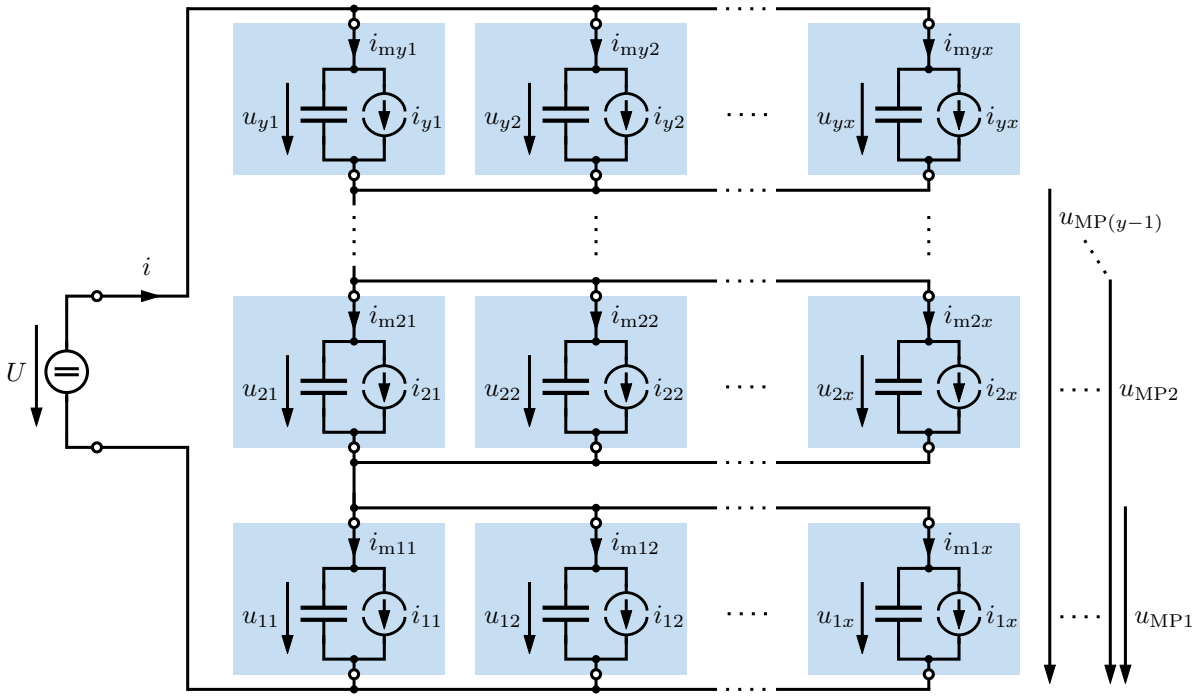



Figure 5.6: $x$P$y$S interconnection of MC-type ports with ideal voltage source

variables. In this case, the midpoint voltages $u_{\mathrm{MP}p}$ are used[ii], which are the accumulated voltages of the parallel-connected blocks according to (5.18):

$$u_{\mathrm{MP}p} := \sum_{r=1}^{p} u_r \quad \text{for all} \quad p = 1 \ldots (y-1). \tag{5.34}$$

These midpoint voltages are arranged in the new state vector as follows:

$$\vec{x} = \begin{pmatrix} u_{\mathrm{MP1}} & u_{\mathrm{MP2}} & \ldots & u_{\mathrm{MP}(y-1)} \end{pmatrix}^{\mathrm{T}}. \tag{5.35}$$

The second major difference is that the current $i$ at the terminals of the interconnected port is not a disturbance input anymore, which has already been discussed in Section 5.1.2; the terminal current is rather determined by all individual ports together. The definitions of the manipulated input vector and the output vector, however, remain as given in (5.19) because the same coordinate system can be applied.

Naturally, the basic equations of this interconnection developed in (5.20), (5.21) and (5.22) still remain valid; only an expression for the current $i$ has to be found. For this purpose, all voltages from (5.22) are added together, exploiting the fact that the overall dc-link

[ii] This is only one possibility to select $(y-1)$ states, as already discussed. Other choices such as the pair-wise differences between neighboring voltages of parallel-connected blocks would also be viable.

voltage is constant:

$$\sum_{p=1}^{y} C\frac{\mathrm{d}u_p}{\mathrm{d}t} = C\frac{\mathrm{d}}{\mathrm{d}t}\left(\sum_{p=1}^{y} u_p\right) = C\frac{\mathrm{d}U}{\mathrm{d}t} = 0 \overset{(5.22)}{=} \frac{y\cdot i}{x} - \frac{1}{x}\sum_{p=1}^{y}\sum_{q=1}^{x} i_{pq}$$
$$\Rightarrow i = \frac{1}{y}\sum_{p=1}^{y}\sum_{q=1}^{x} i_{pq}. \tag{5.36}$$

This result makes physical sense because it means that the load current is the average of the current sums of the parallel-connected converter blocks.

To obtain the system equations governing the matrix $\mathbf{B_m}$ (while the disturbance input matrix does not exist), the definition of the midpoint voltages (5.34) and the found expression (5.36) for the current $i$ have to be inserted into (5.22), giving

$$C\frac{\mathrm{d}u_{\mathrm{MP}p}}{\mathrm{d}t} = \frac{p\cdot i}{x} - \frac{1}{x}\sum_{r=1}^{p}\sum_{q=1}^{x} i_{rq} \overset{(5.36)}{=} \frac{p}{n}\sum_{r=1}^{y}\sum_{q=1}^{x} i_{rq} - \frac{1}{x}\sum_{r=1}^{p}\sum_{q=1}^{x} i_{rq}$$
$$= \frac{p}{n}\sum_{r=p+1}^{y}\sum_{q=1}^{x} i_{rq} - \frac{y-p}{n}\sum_{r=1}^{p}\sum_{q=1}^{x} i_{rq} \quad \text{for all} \quad p = 1\ldots(y-1). \tag{5.37}$$

The same can be done to obtain the system equations governing the matrix $\mathbf{D_m}$ (the disturbance feed-through matrix does not exist) by inserting (5.36) into (5.25):

$$i_{\mathrm{m}pq} = i_{pq} - \frac{1}{x}\sum_{r=1}^{x} i_{pr} + \frac{1}{n}\sum_{r=1}^{y}\sum_{o=1}^{x} i_{ro} \quad \text{for all} \quad p = 1\ldots y \quad \text{and} \quad q = 1\ldots x. \tag{5.38}$$

Using these equations as well as (5.35) and (5.19), the matrices $\mathbf{B_m}$ and $\mathbf{D_m}$ can be found:

$$\mathbf{B_m} = \frac{1}{nC}\cdot\begin{pmatrix} 1-y & \cdots & 1-y & 1 & \cdots & 1 & \cdots & 1 & \cdots & 1 & 1 & \cdots & 1 \\ 2-y & \cdots & 2-y & 2-y & \cdots & 2-y & \cdots & 2 & \cdots & 2 & 2 & \cdots & 2 \\ \vdots & & \vdots & \vdots & & \vdots & \ddots & & & & \vdots & & \vdots \\ -1 & \cdots & -1 & -1 & \cdots & -1 & \cdots & -1 & \cdots & -1 & y-1 & \cdots & y-1 \end{pmatrix}, \tag{5.39}$$

$$\mathbf{D_m} = \frac{1}{n}\cdot\begin{pmatrix} 1-y+n & 1-y & \cdots & 1-y & & & & \\ 1-y & 1-y+n & \cdots & 1-y & & & & \\ \vdots & \vdots & \ddots & \vdots & & & \mathbf{1}_{x\times x} & \\ 1-y & 1-y & \cdots & 1-y+n & & & & \\ & & & & \ddots & & & \\ & & & & & 1-y+n & 1-y & \cdots & 1-y \\ & & \mathbf{1}_{x\times x} & & & 1-y & 1-y+n & \cdots & 1-y \\ & & & & & \vdots & \vdots & \ddots & \vdots \\ & & & & & 1-y & 1-y & \cdots & 1-y+n \end{pmatrix}$$
$$= \frac{1}{n}\cdot\mathbf{1}_{n\times n} + \left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x}\cdot\mathbf{1}_{x\times x}\right)\right). \tag{5.40}$$

The matrix $\mathbf{B_m}$ consists of horizontal blocks of the dimension $1 \times x$, which are concatenated in a staircase-shaped form, as highlighted in (5.39). In turn, the matrix $\mathbf{D_m}$ is a real symmetric matrix, which proves that a base of $n$ linearly independent eigenvectors must exist. Compared to its counterpart in the case without ideal voltage source, it is considerably less sparse; the only difference is that the term $\frac{1}{n}$ is added to every entry of the matrix. This also makes physical sense because every sensor measures a fraction of $\frac{1}{x}$ of the terminal current $i$ of the interconnected port, since $x$ converters are connected in parallel. Together with the factor $\frac{1}{y}$ from the equation for $i$ in (5.36), this explains the structure of the matrix $\mathbf{D_m}$ also from a physical perspective.

**Steps 2–4 — Eigenvalues and Eigenvectors:** Since the matrix $\mathbf{D_m}$ is considerably less sparse than its counterpart from the previous section, the analysis of the eigenvalues and eigenvectors becomes more tedious than before. For the sake of conciseness, the steps 2–4 of the step-by-step procedure are only sketched without the proper mathematical proofs, which are moved to Appendix A.1. This way, more emphasis can be put on the physical contextualization of the found results.

It is expected that $\mathbf{D_m}$ has the internal eigenvalue 0 with multiplicity $(y-1)$, which equals the number of states, and the external eigenvalue 1 with multiplicity $(n-y+1)$. The characteristic polynomial is derived in Appendix A.1, with the result

$$0 \stackrel{!}{=} \det\left(\frac{1}{n}\mathbf{1}_{n\times n} + \left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\right) - \lambda\mathbf{I}_n\right) = \ldots = (-\lambda)^{y-1}\cdot(1-\lambda)^{n-y+1}. \quad (5.41)$$

This proves the stated expectations, i.e., that the number of internal eigenvalues has been reduced by one compared to the number of internal eigenvalues in the case without ideal voltage source, while the number of external eigenvalues has been increased by one.

The internal eigenvectors are once again taken from the matrix $\mathbf{B_m}$ as suggested in Section 5.2 by multiplying it with the scalar value $\gamma = C$, resulting in

$$\mathbf{V}_\mathrm{I} = \frac{1}{n}\cdot\begin{pmatrix} 1-y & \cdots & 1-y & 1 & \cdots & 1 & \cdots & 1 & \cdots & 1 & 1 & \cdots & 1 \\ 2-y & \cdots & 2-y & 2-y & \cdots & 2-y & \cdots & 2 & \cdots & 2 & 2 & \cdots & 2 \\ \vdots & & \vdots & \vdots & & \vdots & \ddots & & & & \vdots & & \vdots \\ -1 & \cdots & -1 & -1 & \cdots & -1 & \cdots & -1 & \cdots & -1 & y-1 & \cdots & y-1 \end{pmatrix}. \quad (5.42)$$

In Appendix A.1, these $(y-1)$ row vectors are proven to be left eigenvectors of $\mathbf{D_m}$ corresponding to the internal eigenvalue 0.

Finally, the external eigenvectors need to be derived from sensible physical assumptions. The same DM current patterns as in the case without ideal voltage source are selected. However, the multiplicity of the external eigenvalue of 1 increased by one, hence for a real symmetric matrix $\mathbf{D_m}$, there also must be one more linearly independent external eigenvector, which is still missing. Therefore, the terminal current of the interconnected converter port $i$ is selected as this additional eigenvector. As already discussed, it is not

a disturbance input anymore because it is manipulated by all converter ports together. Since it does not charge any capacitor, i.e., it does not manipulate the state of the system, it must be measurable by the sensors. This current might be called CM current because it directly controls the power transmitted by the interconnected converter port. For this reason, it is also very significant for the control of the converter. Hence, the external left modal matrix containing the external eigenvectors of $\mathbf{D_m}$ is constructed as follows:

$$\mathbf{V}_\mathrm{E} = \begin{pmatrix} \frac{1}{y} & \frac{1}{y} & \frac{1}{y} & \cdots & \frac{1}{y} & \cdots & \frac{1}{y} & \frac{1}{y} & \frac{1}{y} & \cdots & \frac{1}{y} \\ 1 & -1 & 0 & \cdots & 0 & & & & & & \\ 0 & 1 & -1 & \cdots & 0 & & & & & & \\ \vdots & & \ddots & \ddots & \vdots & \cdots & & \mathbf{0}_{(x-1)\times x} & & & \\ 0 & 0 & \cdots & 1 & -1 & & & & & & \\ & & \vdots & & & \ddots & & & \vdots & & \\ & & & & & & 1 & -1 & 0 & \cdots & 0 \\ & & & & & & 0 & 1 & -1 & \cdots & 0 \\ & & \mathbf{0}_{(x-1)\times x} & & & \cdots & \vdots & & \ddots & \ddots & \vdots \\ & & & & & & 0 & 0 & \cdots & 1 & -1 \end{pmatrix}. \tag{5.43}$$

The CM current as defined by (5.36) is highlighted in green in the first row. The $(x-1)$ DM current patterns for each parallel-connected block, highlighted in magenta, form $(x-1)\times x$ block matrices, which are repeated diagonally for each of the $y$ series-connected converter port blocks. In Appendix A.1, it is proven that all these vectors are indeed external eigenvectors of $\mathbf{D_m}$.

**Step 5 — Transformation matrix:** The last step is to construct the transformation matrix by stacking the internal and external left modal matrices:

$$\mathbf{T} = \begin{pmatrix} \mathbf{V}_\mathrm{I} \\ \mathbf{V}_\mathrm{E} \end{pmatrix} = \begin{pmatrix} \frac{1-y}{n} & \cdots & & \frac{1-y}{n} & & \frac{1}{n} & \cdots & & \frac{1}{n} \\ & & & & \ddots & & & & \\ -\frac{1}{n} & \cdots & & -\frac{1}{n} & & \frac{y-1}{n} & \cdots & & \frac{y-1}{n} \\ \frac{1}{y} & \cdots & & \frac{1}{y} & \cdots & \frac{1}{y} & \cdots & & \frac{1}{y} \\ 1 & -1 & 0 & \cdots & 0 & & & & \\ 0 & 1 & -1 & \cdots & 0 & & & & \\ \vdots & & \ddots & \ddots & \vdots & & \mathbf{0}_{(x-1)\times x} & & \\ 0 & 0 & \cdots & 1 & -1 & & & & \\ & & & & & \ddots & & & \\ & & & & & 1 & -1 & 0 & \cdots & 0 \\ & & & & & 0 & 1 & -1 & \cdots & 0 \\ & & \mathbf{0}_{(x-1)\times x} & & & \vdots & & \ddots & \ddots & \vdots \\ & & & & & 0 & 0 & \cdots & 1 & -1 \end{pmatrix}. \tag{5.44}$$

Regarding the linear independence of the external eigenvectors, it is evident by looking at the external left modal matrix $\mathbf{V}_\mathrm{E}$ in (5.43) that all of its rows must be linearly independent. In turn, the internal left modal matrix $\mathbf{V}_\mathrm{I}$ in (5.42) contains constant rows of increasing numbers from 1 to $(y-1)$, from which a lower block triangular matrix full of $y$ entries is subtracted, indicated by the shaded area. This triangular structure renders all rows of the matrix $\mathbf{V}_\mathrm{I}$ linearly independent. As already stated, the linear independence

of the internal eigenvectors from the external eigenvectors does not need to be proven because they belong to different eigenvalues.

In summary, the state-space model and the transformation matrix have been developed for the $x\mathrm{P}y\mathrm{S}$ interconnection of MC-type converter ports with ideal voltage source. The internal eigenvectors have been selected to be those current patterns that manipulate the midpoint voltages of the parallel-connected converter blocks, which have been selected to be the state variables. The external eigenvectors consist of the current that flows through the terminals of the interconnected converter, representing the overall power transmission of the system, and the pair-wise current differences between neighboring individual converter ports of parallel-connected blocks.

### 5.3.3 ySxP Interconnection of MC Ports

The third interconnection variant to be analyzed is the $y\mathrm{S}x\mathrm{P}$ interconnection without ideal voltage source as shown in Fig. 5.7. In this case, the series connection is made first, resulting in $x(y-1)$ midpoint voltages, which form the state variables together with the overall dc-link voltage $u$, resulting in $(x(y-1)+1)$ state variables as suggested by Table 5.2. These are considerably more state variables compared to the number of states in an $x\mathrm{P}y\mathrm{S}$ interconnection because only the parallel connection reduces the number of states for MC-type converter ports.

Some minor changes have to be made to the nomenclature for the highest convenience in developing the system equations and matrices: First, the order of the variables $x$ and $y$ in the nomenclature $y\mathrm{S}x\mathrm{P}$ has been swapped compared to the $x\mathrm{P}y\mathrm{S}$ interconnection because it is assumed less confusing when the variable $x$ is always associated with a parallel connection and when $y$ is always associated with a series connection. Additionally, the coordinate system that defines the numbering of the variables has been changed in Fig. 5.7 compared to the coordinate system shown in Fig. 5.5 and Fig. 5.6. For the $x\mathrm{P}y\mathrm{S}$ interconnection, the second index $p$ of, for example, the currents $i_{1p}$ differentiated between the current sources of all the individual converter ports in the first block, while the first index differentiated between the series-connected blocks. This was useful because with the definitions of the system vectors in (5.19), the variables related to parallel-connected individual converter ports were grouped closely together, forming the block structures in the system matrices. For the $y\mathrm{S}x\mathrm{P}$ interconnection, however, not the parallel connection, but the series connection is now made first. Therefore, to preserve the definitions of the system vectors in (5.19) and to preserve the block structures in the system matrices, the second index of the variables now differentiates between series-connected individual converter ports.

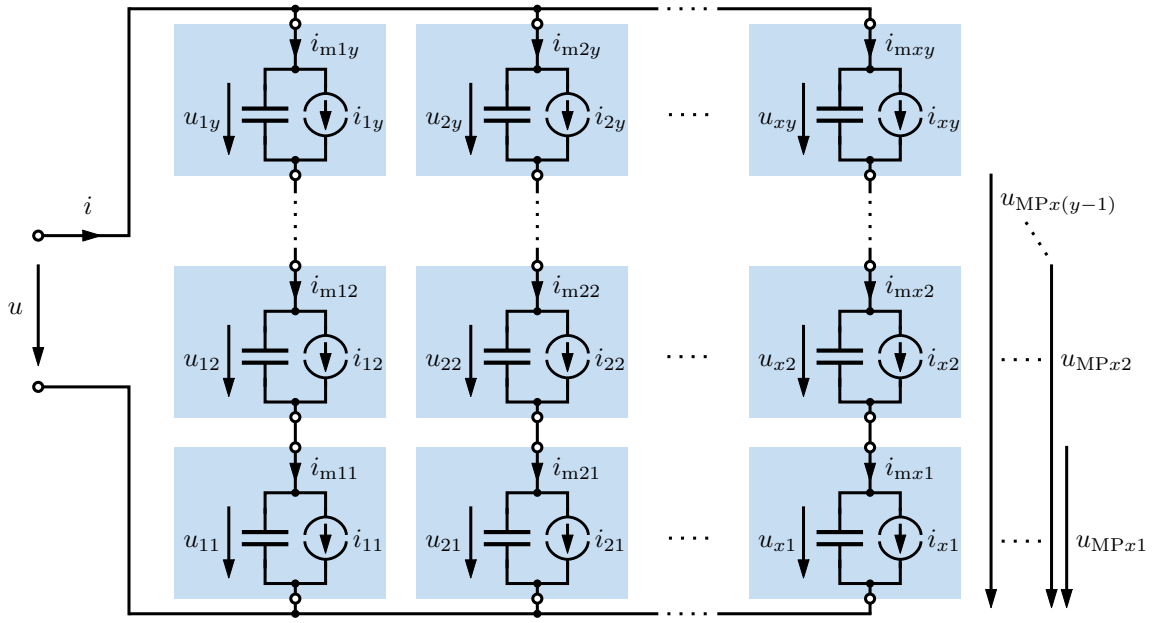



Figure 5.7: $y$S$x$P interconnection of MC-type ports without ideal voltage source

**Step 1 — Derive the state-space model:** The first task in deriving the state-space model of the $y$S$x$P interconnection is to define suitable state variables. Choosing the voltages of the individual converter ports would result in too many state variables because the common connection to one dc-link reduces the number of independent state variables. In turn, using the midpoint voltages of each series-connected branch would disregard the common dc-link voltage and hence produce one state variable less than required. Hence, the chosen state variables are the midpoint voltages in each branch, and additionally the common dc-link voltage. The midpoint voltages of each series-connected branch are defined as follows:

$$u_{\mathrm{MP}pq} := \sum_{r=1}^{q} u_{pr} \quad \text{for all} \;\; p = 1 \ldots x \;\; \text{and} \;\; q = 1 \ldots (y-1). \tag{5.45}$$

The state variables are arranged in the state vector as follows:

$$\vec{x} = \begin{pmatrix} u & u_{\mathrm{MP}11} & u_{\mathrm{MP}12} & \ldots & u_{\mathrm{MP}1(y-1)} & \ldots & u_{\mathrm{MP}x1} & u_{\mathrm{MP}x2} & \ldots & u_{\mathrm{MP}x(y-1)} \end{pmatrix}^{\mathrm{T}}. \tag{5.46}$$

The definition of the manipulated input vector, the system output vector, and also the disturbance input, are unchanged compared to the $x$P$y$S scenario as defined by (5.19). As no ideal voltage source is connected to the terminals of the interconnected converter port, the terminal current $i$ must be considered a disturbance input. One final simplification can be made because the current along each series-connected branch is the same. Hence, the measured current in each of those branches is denoted

$$i_{\mathrm{m}p} := i_{\mathrm{m}p1} = i_{\mathrm{m}p2} = \ldots = i_{\mathrm{m}py} \quad \text{for all} \;\; p = 1 \ldots x. \tag{5.47}$$

With these definitions of the system variables in place, the fundamental equations of the $y\mathrm{S}x\mathrm{P}$ interconnection can be derived using KVL, KCL and the device equation of the capacitors in the system:

$$C\frac{\mathrm{d}u_{pq}}{\mathrm{d}t} = i_{\mathrm{m}p} - i_{pq} \qquad \text{for all } \; p = 1\ldots x \;\text{ and }\; q = 1\ldots y, \tag{5.48}$$

$$u = \sum_{q=1}^{y} u_{pq} \qquad \text{for all } \; p = 1\ldots x, \tag{5.49}$$

$$i = \sum_{p=1}^{x} i_{\mathrm{m}p}. \tag{5.50}$$

When the equations from (5.48) are added along each series-connected branch, it can be found that

$$\sum_{q=1}^{y} C\frac{\mathrm{d}u_{pq}}{\mathrm{d}t} = C\frac{\mathrm{d}}{\mathrm{d}t}\sum_{q=1}^{y} u_{pq} \overset{(5.49)}{=} C\frac{\mathrm{d}u}{\mathrm{d}t} = y\cdot i_{\mathrm{m}p} - \sum_{q=1}^{y} i_{pq} \quad \text{for all } \; p = 1\ldots x. \tag{5.51}$$

The resulting equations from (5.51) can again be added along the parallel-connected branches, obtaining

$$\sum_{p=1}^{x} C\frac{\mathrm{d}u}{\mathrm{d}t} = xC\frac{\mathrm{d}u}{\mathrm{d}t} = \sum_{p=1}^{x} y\cdot i_{\mathrm{m}p} - \sum_{p=1}^{x}\sum_{q=1}^{y} i_{pq} \overset{(5.50)}{=} y\cdot i - \sum_{p=1}^{x}\sum_{q=1}^{y} i_{pq}. \tag{5.52}$$

This equation can already be used in finding the single row of the matrices $\mathbf{B_m}$ and $\mathbf{B_d}$ that relates to the derivative of the common dc-link voltage as state variable. If the expressions for this derivative from (5.52) and (5.51) are equated, expressions for the sensor currents can be found, which define the matrices $\mathbf{D_m}$ and $\mathbf{D_d}$:

$$\begin{aligned} C\frac{\mathrm{d}u}{\mathrm{d}t} &= y\cdot i_{\mathrm{m}p} - \sum_{q=1}^{y} i_{pq} = \frac{y}{x}\cdot i - \frac{1}{x}\sum_{p=1}^{x}\sum_{q=1}^{y} i_{pq} \\ \Rightarrow \quad i_{\mathrm{m}p} &= \frac{1}{x}\cdot i + \frac{1}{y}\sum_{q=1}^{y} i_{pq} - \frac{1}{n}\sum_{r=1}^{x}\sum_{q=1}^{y} i_{rq} \quad \text{for all } \; p = 1\ldots x. \end{aligned} \tag{5.53}$$

This result makes physical sense because the first term suggests that the load current flows in equal parts in all $x$ parallel branches, the second term suggests that the average manipulated current in each series-connected branch is also measured by the sensors, and the third term accounts for the fact that also the average manipulated current of all parallel branches is measured in all branches because they are connected to a common dc rail. The final missing part to construct the state-space matrices are the equations for the midpoint voltages $u_{\mathrm{MP}pq}$, which can be found by applying the definition (5.45) to (5.48)

and using the result for the measured currents (5.53):

$$C\frac{\mathrm{d}u_{\mathrm{MP}pq}}{\mathrm{d}t} = q\cdot i_{\mathrm{mp}} - \sum_{o=1}^{q} i_{po} \overset{(5.53)}{=} \frac{q}{x}\cdot i + \frac{q}{y}\sum_{o=1}^{y} i_{po} - \sum_{o=1}^{q} i_{po} - \frac{q}{n}\sum_{r=1}^{x}\sum_{o=1}^{y} i_{ro} \qquad (5.54)$$
$$\text{for all } \; p = 1\ldots x \;\text{ and }\; q = 1\ldots(y-1).$$

The state-space matrices of the system can now be derived using the definition of the manipulated input and output vectors (5.19), as well as the definition of the state vector (5.46) in conjunction with (5.52), (5.53) and (5.54):

$$\mathbf{B_m} = -\frac{1}{nC}\cdot \begin{pmatrix} y & y & \cdots & y & \cdots & y & y & \cdots & y \\ (1-x)+n & (1-x) & \cdots & (1-x) & & 1 & 1 & \cdots & 1 \\ 2(1-x)+n & 2(1-x)+n & \cdots & 2(1-x) & & 2 & 2 & \cdots & 2 \\ \vdots & & \ddots & \vdots & \cdots & \vdots & \vdots & & \vdots \\ (y-1)(1-x)+n & (y-1)(1-x)+n & \cdots & (y-1)(1-x) & & (y-1) & (y-1) & \cdots & (y-1) \\ & & & & \ddots & & & & \\ 1 & 1 & \cdots & 1 & & (1-x)+n & (1-x) & \cdots & (1-x) \\ 2 & 2 & \cdots & 2 & & 2(1-x)+n & 2(1-x)+n & \cdots & 2(1-x) \\ \vdots & \vdots & & \vdots & \cdots & \vdots & & \ddots & \vdots \\ (y-1) & (y-1) & \cdots & (y-1) & & (y-1)(1-x)+n & (y-1)(1-x)+n & \cdots & (y-1)(1-x) \end{pmatrix}, \qquad (5.55)$$

$$\mathbf{D_m} = -\frac{1}{n}\cdot \begin{pmatrix} 1-x & 1-x & \cdots & 1-x & \cdots & & \\ 1-x & 1-x & \cdots & 1-x & & & \\ \vdots & \vdots & & \vdots & & \mathbf{1}_{y\times y} & \\ 1-x & 1-x & \cdots & 1-x & & & \\ & & & & \ddots & & \\ & & & & & 1-x & 1-x & \cdots & 1-x \\ & & & & & 1-x & 1-x & \cdots & 1-x \\ & \mathbf{1}_{y\times y} & & & \cdots & \vdots & \vdots & & \vdots \\ & & & & & 1-x & 1-x & \cdots & 1-x \end{pmatrix}$$
$$= -\frac{1}{n}\cdot \mathbf{1}_{n\times n} + \left(\mathbf{I}_x \otimes \left(\frac{1}{y}\cdot \mathbf{1}_{y\times y}\right)\right), \qquad (5.56)$$

$$\mathbf{B_d} = \frac{1}{xC}\cdot \begin{pmatrix} y & 1 & 2 & \cdots & y-1 & \cdots & 1 & 2 & \cdots & y-1 \end{pmatrix}^{\mathrm{T}}, \qquad (5.57)$$

$$\mathbf{D_d} = \frac{1}{x}\cdot \mathbf{1}_{n\times 1}. \qquad (5.58)$$

The manipulated input matrix $\mathbf{B_m}$ consists of one line, highlighted in green, describing the manipulation of the common dc-link voltage governed by (5.52), followed by a structure of $(y-1)\times y$ sub-matrices. In the sub-matrices on the diagonal, which are highlighted in blue, all terms from (5.54) contribute entries, except for the term associated with the disturbance input, while in the off-diagonal sub-matrices, only the last term from (5.54) contributes entries. The disturbance input matrix $\mathbf{B_d}$ is constructed only by the first term in (5.54). The manipulated feed-through matrix $\mathbf{D_m}$ is governed by the second and

third term in (5.53), giving a block-symmetric structure, which again guarantees that a base of $n$ eigenvectors must exist. The matrix $\mathbf{D_m}$ consists of $x$ sub-matrices, each of $y \times y$ dimension with all entries being identical. This reflects the fact that all sensors in each series-connected branch measure the same current; indeed, (5.47) requires that every set of $y$ rows of the matrix $\mathbf{D_m}$ must be block-wise identical[iii]. Finally, the disturbance feed-through matrix $\mathbf{D_d}$ is governed by the first term in (5.53).

**Steps 2–4 — Eigenvalues and Eigenvectors:** As before, for the sake of conciseness, the steps 2–4 of the step-by-step procedure will only be sketched in the following without the proper mathematical proofs, which are moved to Appendix A.3. Deriving the characteristic polynomial of the matrix $\mathbf{D_m}$ to find its eigenvalues results in

$$0 \stackrel{!}{=} \det\left(-\frac{1}{n} \cdot \mathbf{1}_{n\times n} + \left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y}\right)\right)\right) = \ldots = (-\lambda)^{x(y-1)+1} \cdot (1-\lambda)^{x-1}. \quad (5.59)$$

As expected, the multiplicity of the internal eigenvalue 0 matches the number of state variables, also for this interconnection.

The internal left modal matrix $\mathbf{V}_\mathrm{I}$ is obtained by multiplying the matrix $\mathbf{B_m}$ in (5.55) with the scalar value $\gamma = C$; Appendix A.3 proves that this internal left modal matrix indeed contains internal eigenvectors of $\mathbf{D_m}$. However, the external left modal matrix, which should contain external eigenvectors of $\mathbf{D_m}$, is yet to be found. The multiplicity of the external eigenvalue of 1 found in (5.59) suggests that there are only $(x-1)$ external eigenvectors. Evidently, the pair-wise differences between the currents of neighboring series-connected branches can be chosen as external eigenvectors[iv]; more precisely, (5.53) suggests that it is the average current of a series-connected branch that is measurable by the sensors. Hence, the external left modal matrix is defined as

$$\mathbf{V}_\mathrm{E} = \frac{1}{y} \cdot \begin{pmatrix} 1 & \cdots & 1 & -1 & \cdots & -1 & 0 & \cdots & 0 & \cdots & 0 & \cdots & 0 \\ 0 & \cdots & 0 & 1 & \cdots & 1 & -1 & \cdots & -1 & \cdots & 0 & \cdots & 0 \\ \vdots & & \vdots & & & & & \ddots & & \ddots & \vdots & & \vdots \\ 0 & \cdots & 0 & 0 & \cdots & 0 & & \cdots & & 1 \;\cdots\; 1 & -1 & \cdots & -1 \end{pmatrix}. \quad (5.60)$$

In Appendix A.3, it is shown that $\mathbf{V}_\mathrm{E}$ indeed contains external eigenvectors of $\mathbf{D_m}$.

**Step 5 — Transformation matrix:** To form the transformation matrix $\mathbf{T}$, the final step is again to concatenate the internal and external left modal matrices vertically according to (5.14). The matrix $\mathbf{T}$ is not explicitly printed for the sake of conciseness. Regarding the linear independence of the eigenvectors, similar arguments can be made as in the

[iii] This would justify to remove all duplicate rows from $\mathbf{D_m}$, shortening the definition of the system output vector by the number of redundant measurements. However, eigenvectors and eigenvalues can only be found for square matrices, therefore the redundancy is maintained on purpose.

[iv] This choice is as good as any other choice of external eigenvectors, it is however consistent with the DM current patterns that are used multiple times in this dissertation.

previous sections. The external left modal matrix (5.60) very obviously has linearly independent rows. The linear independence of the eigenvectors contained in the internal left modal matrix $\mathbf{V}_\mathrm{I}$, on the other hand, can be deduced from a structural discussion using the originating matrix $\mathbf{B_m}$ in (5.55). Thus, it is easily verified that the same argument can be made as for the internal left modal matrix from Section 5.3.2: Since lower triangular matrices are added block-wise to blocks of otherwise linearly dependent rows, linear independence is guaranteed.

In summary, the state-space model and the transformation matrix have been developed for the $y\mathrm{S}x\mathrm{P}$ interconnection of MC-type converter ports without ideal voltage source. The internal eigenvectors have been selected as those current patterns that manipulate the midpoint voltages of the series-connected converter branches, and additionally the current pattern that manipulates the common dc-link voltage. The external eigenvectors have been selected as the pair-wise differences between the average currents of neighboring series-connected branches.

### 5.3.4 ySxP Interconnection of MC Ports with Ideal Voltage Source

For MC-type individual converter ports, only one variant is left to be analyzed, namely the $y\mathrm{S}x\mathrm{P}$ interconnection with ideal voltage source, which is shown in Fig. 5.8.

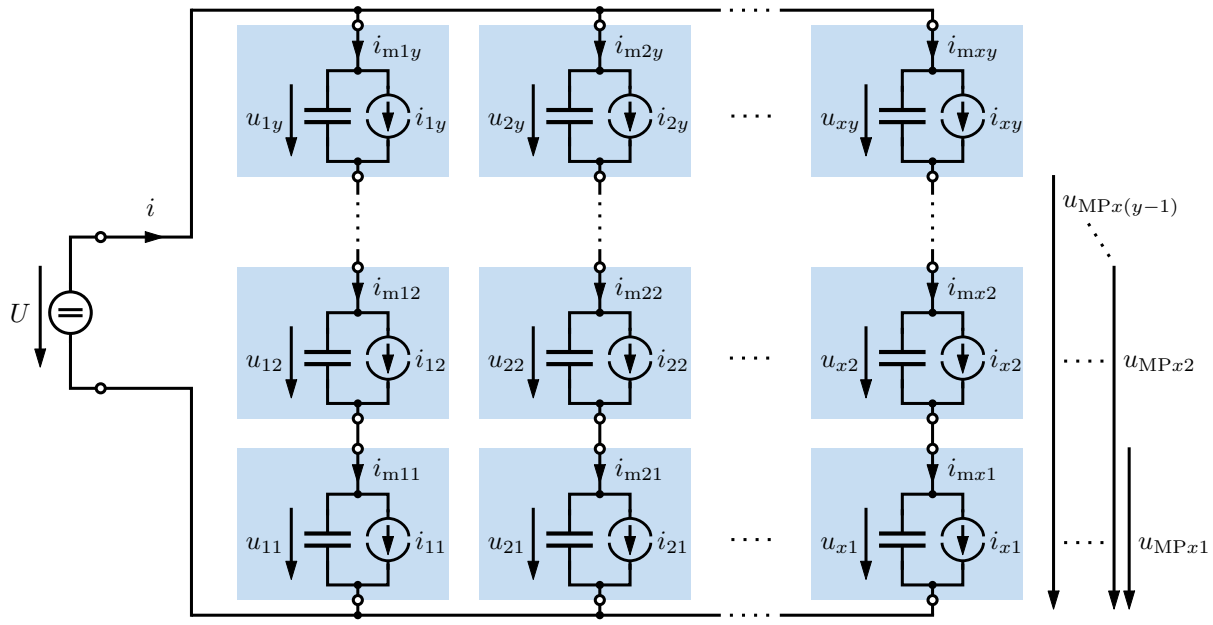



Figure 5.8: $y\mathrm{S}x\mathrm{P}$ interconnection of MC-type ports with ideal voltage source

**Step 1 — Derive the state-space model:** Connecting an ideal voltage source to the $y\mathrm{S}x\mathrm{P}$ interconnection somewhat simplifies the system equations, as it suppresses the in-

teractions between all series-connected branches and therefore eliminates exactly the common dc-link voltage from the vector of the state variables. Hence, there are only $x(y-1)$ midpoint voltages left as defined by (5.45), forming the state vector

$$\vec{x} = \begin{pmatrix} u_{\mathrm{MP}11} & u_{\mathrm{MP}12} & \dots & u_{\mathrm{MP}1(y-1)} & \dots & u_{\mathrm{MP}x1} & u_{\mathrm{MP}x2} & \dots & u_{\mathrm{MP}x(y-1)} \end{pmatrix}^{\mathrm{T}}. \tag{5.61}$$

In turn, the manipulated input and output vectors are still the same as defined in (5.19). The terminal current $i$ is again not a disturbance input anymore because it is not linked to a system state, i.e., it does not charge a capacitor. Instead, it is jointly manipulated by all converters and directly measurable by the sensors. Hence, neither a disturbance input vector $\vec{u}_{\mathrm{d}}$ nor the matrices $\mathbf{B_d}$ and $\mathbf{D_d}$ exist.

The remaining equations have already been prepared in Section 5.3.3, only the constant dc-link voltage requires further considerations. Setting the derivative of the common dc-link voltage $u$ in (5.52) to zero yields the following expression for the current at the terminals of the interconnected converter:

$$i = \frac{1}{y} \sum_{p=1}^{x} \sum_{q=1}^{y} i_{pq}. \tag{5.62}$$

This indicates that the terminal current is equal to the sum of the average currents of all $x$ converter branches, which makes physical sense. Using (5.62) in (5.53) yields an equation for the sensor currents,

$$i_{\mathrm{mp}} = \frac{1}{y} \sum_{q=1}^{y} i_{pq}, \tag{5.63}$$

which governs the manipulated feed-through matrix $\mathbf{D_m}$ as follows:

$$\mathbf{D_m} = \frac{1}{y} \cdot \begin{pmatrix} 1 & \cdots & 1 & & & \\ \vdots & & \vdots & & \mathbf{0}_{y\times y} & \\ 1 & \cdots & 1 & & & \\ & & & \ddots & & \\ & & & & 1 & \cdots & 1 \\ & \mathbf{0}_{y\times y} & & & \vdots & & \vdots \\ & & & & 1 & \cdots & 1 \end{pmatrix} = \mathbf{I}_x \otimes \left( \frac{1}{y} \cdot \mathbf{1}_{y\times y} \right). \tag{5.64}$$

Again, the matrix $\mathbf{D_m}$ is real and symmetric, making it diagonalizable. It consists of $x$ blocks, each $y \times y$ with all identical rows because all sensors in a series-connected branch measure the same current. Inserting (5.63) into the left part of (5.54) gives an expression for the derivative of the midpoint voltages,

$$C \frac{\mathrm{d}u_{\mathrm{MP}pq}}{\mathrm{d}t} = \frac{q}{y} \sum_{o=1}^{y} i_{po} - \sum_{o=1}^{q} i_{po} = \frac{q}{y} \sum_{o=q+1}^{y} i_{po} - \frac{y-q}{y} \sum_{o=1}^{q} i_{po}, \tag{5.65}$$

which governs the manipulated input matrix $\mathbf{B_m}$ as follows:

$$\mathbf{B_m} = \frac{1}{yC} \cdot \begin{pmatrix} \begin{matrix} 1-y & 1 & 1 & \cdots & 1 \\ 2-y & 2-y & 2 & \cdots & 2 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ -1 & -1 & -1 & \cdots & y-1 \end{matrix} & & \mathbf{0}_{(y-1)\times y} \\ & \ddots & \\ \mathbf{0}_{(y-1)\times y} & & \begin{matrix} 1-y & 1 & 1 & \cdots & 1 \\ 2-y & 2-y & 2 & \cdots & 2 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ -1 & -1 & -1 & \cdots & y-1 \end{matrix} \end{pmatrix}. \tag{5.66}$$

The found matrix $\mathbf{B_m}$ is a block-diagonal matrix consisting of $x$ diagonal blocks representing the parallel-connected converter branches. Each individual block has the dimension $(y-1) \times y$, which indicates that in every branch, $(y-1)$ midpoint voltages are manipulated. The off-diagonal blocks containing only zeros indicate that the ideal voltage source removes any interactions between neighboring port branches.

**Steps 2–4 — Eigenvalues and Eigenvectors:** For the sake of conciseness, the detailed derivation of the eigenvectors and eigenvalues of the matrix $\mathbf{D_m}$ is given in Appendix A.2. The characteristic equation of the matrix $\mathbf{D_m}$ is found to be

$$0 \overset{!}{=} \det\left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y}\right)\right) = \ldots = (-\lambda)^{x(y-1)} \cdot (1-\lambda)^x. \tag{5.67}$$

This confirms that the multiplicity $x(y-1)$ of the internal eigenvalue 0 corresponds to the number of states for this type of interconnection. As $\mathbf{D_m}$ is real and symmetric, there must exist an equal number of linearly independent internal eigenvectors. These can be found once again by multiplying the matrix $\mathbf{B_m}$ from (5.66) with the scalar $\gamma = C$ to form the internal left modal matrix $\mathbf{V}_\mathrm{I}$. Appendix A.2 delivers the proof that these current patterns defined by $\mathbf{B_m}$ are indeed internal eigenvectors of $\mathbf{D_m}$. As regards the external eigenvectors, $x$ vectors are still to be chosen. The current $i$ flowing into the terminals of the interconnected converter port, i.e., the CM current, is a physically meaningful variable as it determines the overall power transfer of the interconnected port. Therefore, it is selected as one external eigenvector according to its definition in (5.62). The remaining $(x-1)$ eigenvectors are again selected to be the DM currents, i.e., the pair-wise differences between the average currents of neighboring series-connected converter port branches. Hence, the external left modal matrix is defined as follows, with the CM current pattern highlighted in green and the DM current patterns highlighted in magenta:

$$\mathbf{V}_\mathrm{E} = \frac{1}{y} \cdot \begin{pmatrix} 1 & \cdots & 1 & 1 & \cdots & 1 & 1 & \cdots & 1 & \cdots & 1 & \cdots & 1 \\ 1 & \cdots & 1 & -1 & \cdots & -1 & 0 & \cdots & 0 & \cdots & 0 & \cdots & 0 \\ 0 & \cdots & 0 & 1 & \cdots & 1 & -1 & \cdots & -1 & \cdots & 0 & \cdots & 0 \\ \vdots & & \vdots & & & & & \ddots & & \ddots & \vdots & & \vdots \\ 0 & \cdots & 0 & 0 & \cdots & 0 & & \cdots & & 1 \;\cdots\; 1 & -1 & \cdots & -1 \end{pmatrix}. \tag{5.68}$$

In Appendix A.2, it is confirmed that $\mathbf{V}_\mathrm{E}$ is indeed an external left modal matrix of $\mathbf{D_m}$.

**Step 5 — Transformation matrix:** In the last step, the internal left modal matrix $\mathbf{V}_\mathrm{I}$, which is obtained from the matrix $\mathbf{B_m}$ (5.66) by multiplication with $\gamma = C$, and the external left modal matrix $\mathbf{V}_\mathrm{E}$ from (5.68) are concatenated vertically to form the transformation matrix $\mathbf{T}$ as defined by (5.14). All internal eigenvectors must be linearly independent because of the triangular structure of the sub-matrix blocks on the diagonal of $\mathbf{B_m}$. All external eigenvectors in the matrix $\mathbf{V}_\mathrm{E}$ defined in (5.68) are obviously linearly independent. Hence, the matrix $\mathbf{T}$ is invertible and can be used for a decoupled control.

In summary, the state-space model and the transformation matrix have been developed for the $y\mathrm{S}x\mathrm{P}$ interconnection of MC-type converter ports with ideal voltage source. The internal eigenvectors have been selected as those current patterns that manipulate the midpoint voltages of the series-connected converter branches. The external eigenvectors are composed of the CM current flowing at the terminals of the interconnected converter and the DM currents, which are given by the pair-wise differences between the average currents of neighboring series-connected branches.

### 5.3.5 Interconnections of MV Ports

In the previous sections, all four possible interconnection variants of MC-type ports have been analyzed following the step-by-step procedure from Section 5.2.2. The same process needs to be repeated for the four possible interconnection variants of MV-type ports. This is a tedious and lengthy process, which can be bypassed, however, by exploiting many dualities with MC-type ports. Indeed, the exact same state-space models can be found for the four MV interconnection variants as for the four MC interconnection variants; however, identifying the equivalent scenarios requires some deeper analysis of the duality between the MC and MV cases.

Looking back at the equivalent circuits of MC-type and MV-type individual converter ports from Fig. 5.2 in Section 5.1.2, it is evident that the roles of currents and voltages are swapped. For MV-type ports, the state variables are inductor currents instead of capacitor voltages, and the manipulated inputs as well as the measured system outputs are now voltages. Additionally, also the roles of series and parallel connections have been swapped because a series inductor replaces the shunt capacitor from the MC case. This also reflects in the total number of state variables as already analyzed in Table 5.2: For MV-type converter ports, it is the series connection that reduces the number of state variables because inductors are now connected in series. In contrast, the parallel connection of MV-type ports is now the more critical interconnection because the current distribution between those parallel-connected ports must be actively controlled. This is equivalent to the case of MC-type ports connected in series, where the midpoint voltages have to be actively controlled. Finally, the total number of state variables can be reduced by one if an ideal, constant current source is connected to the terminals of the MV-type interconnected port, in analogy to the connection of an ideal, constant voltage source to the terminals of an MC-type interconnected port.

With the dualities of voltages and currents, inductors and capacitors, as well as series and parallel interconnections in mind, it can be suspected that an $x$P$y$S interconnection of MC-type ports would be mathematically equivalent to an $x$S$y$P interconnection of MV-type ports. The same holds for the $y$S$x$P interconnection of MC-type converter ports being mathematically equivalent to the $y$P$x$S interconnection of MV-type converter ports. Additionally, the cases with ideal voltage source for MC-type ports would be equivalent to those with an ideal current source for MV-type ports. The notation of the dual MV case can be obtained by swapping the letters P and S in the notation of the MC case.

This postulation must of course be proven. For the sake of conciseness, this is only done for the $x$S$y$P interconnection of MV-type ports without ideal current source in the following, while the other interconnection variants are covered in Appendix B.

Figure 5.9 shows the schematic of the $x$S$y$P interconnection in question. The coordinate system in which the ports are numbered is once again changed; as in every case before, the second index counts those ports that are closely connected in a sub-group, in this case, the series-connected branches, while the first index counts the blocks of ports, in this case, the parallel-connected branches. While for MC-type converters, the quantity $x$ always referred to the parallel connection, it now refers to the series connection; this is mainly to obtain the same equations as before, but it also makes physical sense because these are equivalent interconnections that reduce the number of states. The variable $y$, in turn, now refers to the parallel connection instead of the series connection, but for MV-type ports, this is the interconnection that does not reduce the number of states and hence requires additional control. The equations for the numbers of state variables from Table 5.2 support that equivalence.

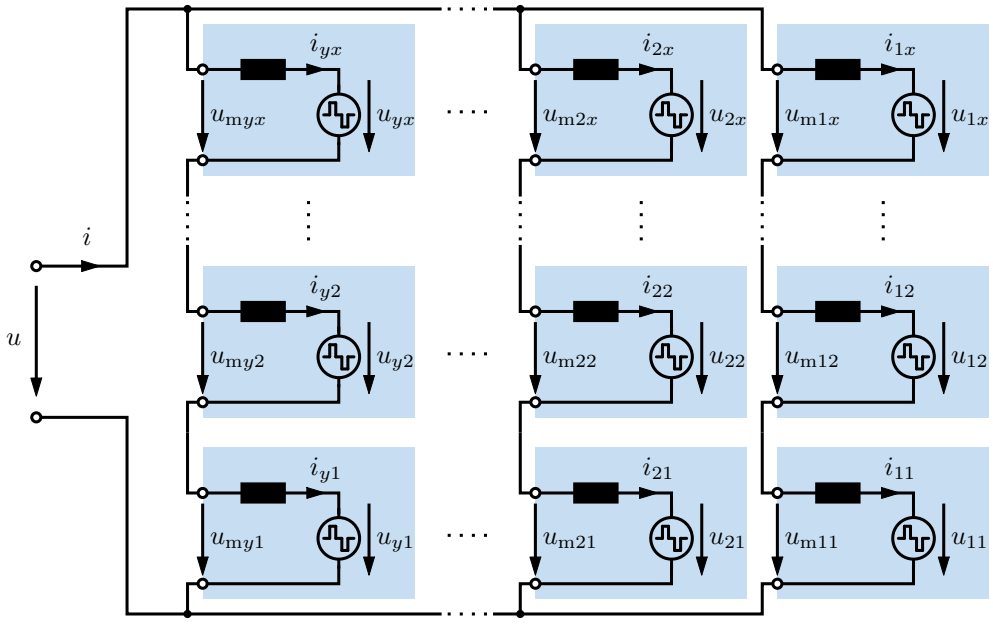



Figure 5.9: $x$S$y$P interconnection of MV-type ports without ideal current source

In the case of the $x$S$y$P interconnection in Fig. 5.9, the $y$ states are selected as the currents in each of the parallel-connected branches. This choice of state variables is equivalent to selecting the voltages of series-connected blocks in an $x$P$y$S interconnection of MC-type converters. Since the currents of all series-connected individual converter ports are equal, the following definition is made for simplicity:

$$i_p := i_{p1} = i_{p2} = \ldots = i_{px} \quad \text{for all} \quad p = 1 \ldots y, \tag{5.69}$$

which is the MV-type counterpart to the MC-type definition from (5.18). With this definition, the input, state, and output vectors of the system can be defined in analogy with (5.19) as follows:

$$\begin{aligned} \vec{x} &= \begin{pmatrix} i_1 & i_2 & \ldots & i_y \end{pmatrix}^{\mathrm{T}}, \qquad \vec{u}_{\mathrm{d}} = u, \\ \vec{u}_{\mathrm{m}} &= \begin{pmatrix} u_{11} & u_{12} & \ldots & u_{1x} & u_{21} & u_{22} & \ldots & u_{2x} & \ldots & u_{y1} & u_{y2} & \ldots & u_{yx} \end{pmatrix}^{\mathrm{T}}, \\ \vec{y} &= \begin{pmatrix} u_{\mathrm{m}11} & u_{\mathrm{m}12} & \ldots & u_{\mathrm{m}1x} & u_{\mathrm{m}21} & u_{\mathrm{m}22} & \ldots & u_{\mathrm{m}2x} & \ldots & u_{\mathrm{m}y1} & u_{\mathrm{m}y2} & \ldots & u_{\mathrm{m}yx} \end{pmatrix}^{\mathrm{T}}. \end{aligned} \tag{5.70}$$

Using KVL and the device equation of the inductors $L$ in the system, which are all assumed equal, the following basic equations are found:

$$L\frac{\mathrm{d}i_p}{\mathrm{d}t} = u_{\mathrm{m}p1} - u_{p1} = u_{\mathrm{m}p2} - u_{p2} = \ldots = u_{\mathrm{m}px} - u_{px} \qquad \text{for all} \quad p = 1 \ldots y, \tag{5.71}$$

$$u = \sum_{q=1}^{x} u_{\mathrm{m}pq} \qquad \text{for all} \quad p = 1 \ldots y. \tag{5.72}$$

Adding all equations from (5.71) together and using (5.72) gives

$$\begin{aligned} \sum_{q=1}^{x} L\frac{\mathrm{d}i_p}{\mathrm{d}t} = xL\frac{\mathrm{d}i_p}{\mathrm{d}t} = \sum_{q=1}^{x}(u_{\mathrm{m}pq} - u_{pq}) &\overset{(5.72)}{=} u - \sum_{q=1}^{x} u_{pq} \quad \text{for all} \quad p = 1 \ldots y \\ \Rightarrow \quad L\frac{\mathrm{d}i_p}{\mathrm{d}t} &= \frac{u}{x} - \frac{1}{x}\sum_{q=1}^{x} u_{pq}, \end{aligned} \tag{5.73}$$

and if (5.71) is substituted into (5.73), the following expression can be obtained for the measured voltages:

$$u_{\mathrm{m}pq} = \frac{u}{x} + u_{pq} - \frac{1}{x}\sum_{r=1}^{x} u_{pr} \quad \text{for all} \;\; p = 1 \ldots y \;\; \text{and} \;\; q = 1 \ldots x. \tag{5.74}$$

All of these equations have the same structure as the ones describing the $x$P$y$S interconnection of MC-type ports in Section 5.3.1. Equation (5.73) describes the influence of the input vectors on the system state, hence it defines the matrices $\mathbf{B_m}$ and $\mathbf{B_d}$. Since (5.73) is in perfect duality with (5.22), the matrices $\mathbf{B_m}$ and $\mathbf{B_d}$ must be the same as in the case of $x$P$y$S -interconnected MC-type ports. The same holds for (5.74), which is in perfect duality with (5.25), hence also the matrices $\mathbf{D_m}$ and $\mathbf{D_d}$ must be the same.

Since the state-space matrices of the $x$S$y$P interconnection of MV-type ports are identical to those of the $x$P$y$S interconnection of MC-type ports, the decoupling approach and the transformation matrix must be the same as well. Therefore, there is no need to repeat the step-by-step procedure to find suitable eigenvectors, as this has already been done. The same applies to the three other interconnection variants using MV-type ports, which all have a dual counterpart in terms of MC-type ports, which can be found by swapping the letters P and S in the interconnection description. To demonstrate this, all equations are elaborated in Appendix B.

Nevertheless, relying on the exact same model as with MC-type ports may also result in some minor inconveniences, as shall be pointed out in the following. As already stated, the selection of the state variables comes with a large degree of freedom, making it possible to select sums, differences, deviations from the mean value, and so on. This, in turn, fixes the system input matrices and therefore also the internal eigenvectors that are used for decoupling. Another large degree of freedom is the selection of suitable external eigenvectors, as long as they are indeed linearly independent eigenvectors of $\mathbf{D_m}$ corresponding to the external eigenvalue of 1. Until now, these degrees of freedom have been used to define sets of state variables and external eigenvectors that are the most physically insightful. For example, the midpoint voltages in a series connection of MC-type ports have been used, defined as the accumulation of the individual port voltages according to (5.34) or (5.45). Using the same definition for parallel-connected MV-type ports results in the accumulated port currents as state variables. This of course also has a physical meaning, but maybe the pair-wise differences in the currents of neighboring converters would be a more physically insightful choice of state variables. However, this would require a completely new derivation of the state-space models and a complete elaboration of the step-by-step procedure to find a transformation matrix. The same applies to the choice of external eigenvectors. In MC-type converters, the DM currents were used as external eigenvectors, i.e., the pair-wise differences between the manipulated input currents of parallel-connected ports. In the MV-type equivalent, these would now correspond to DM voltages, i.e., the pair-wise differences of manipulated input voltages of series-connected MV-type ports. Here again, other choices are possible, for example the accumulated manipulated input voltages. However, other choices than the ones made for MC-type converter ports are not addressed in this dissertation for the sake of conciseness. Nonetheless, it has to be emphasized that the proposed methodology following the step-by-step procedure is applicable to any possible choice of state variables and external eigenvectors and hence does not pose any limitations on the degree of freedom in system modeling.

In summary, the state-space models for $x$S$y$P and $y$P$x$S MV-type port interconnections turn out to be the same as for $x$P$y$S and $y$S$x$P interconnections of MC-type ports, respectively, if the coordinate system of the interconnection schematic is adapted properly. This has been demonstrated using the $x$S$y$P interconnection of MV-type ports without ideal current source, while the duality of the three other interconnection variants with corresponding MC-type interconnections is proven in Appendix B. Hence, all state-space models and all coordinate transformations are already known from the case of MC-type ports, as long as analogous state variables and external eigenvectors are chosen. While

selecting other state variables or external eigenvectors is generally possible, it requires re-calculating the step-by-step procedure from Section 5.2.2, which is avoided for the sake of conciseness.

## 5.4 Control Design

So far, the decoupling concept has only been addressed for a single interconnected converter port. Hence, a decoupled control can be implemented either on the primary side or on the secondary side of a modular converter system. However, not only can the interconnection of the primary-side and secondary-side interconnected ports be completely different, but each of the $n$ individual ports on the primary side can be associated to any of the individual ports on the secondary side. Over all, this increases the number of scenarios to an impractical level. Even more, when developing a decoupled control for one of the interconnected ports, $n_x$ state variables and $(n - n_x)$ external eigenvectors need to be controlled; since every converter can only influence one independent electrical variable, all $n$ degrees of freedom are already utilized. Thus, either the primary-side or the secondary-side interconnected port can be actively controlled, but never simultaneously.

To meet those challenges, this section provides a generalized control approach, which shall be applicable to any modular dc-dc converter system. The proposed decoupling technique is applied to only one of the interconnected ports, for which closed control loops on the state variables and external eigenvectors are designed, while the other interconnected port is left uncontrolled. This way, only one interconnected port needs to be considered in the control design, and only the eight scenarios from the previous sections need to be considered. However, the stability of the uncontrolled interconnected port must be guaranteed.

The first of the following sections addresses the control design for one interconnected port, which utilizes the transformation matrices from the previous sections. In a second step, the uncontrolled port is modeled, resulting in nonlinear systems, and the stability is assessed using the direct method by Lyapunov. Based on the results, it can be decided which of the interconnected ports can be safely left uncontrolled. In the last section, basic guidelines for control design are formulated.

### 5.4.1 Decoupled Control Design for an Interconnected Port

When implementing a closed-loop control for a modular dc-dc converter system, it has to be decided first for which of the two interconnected ports the active, decoupled control should be established. This must be done based on the stability considerations that will be discussed in Section 5.4.3; further guidelines will be given in Section 5.4.4.

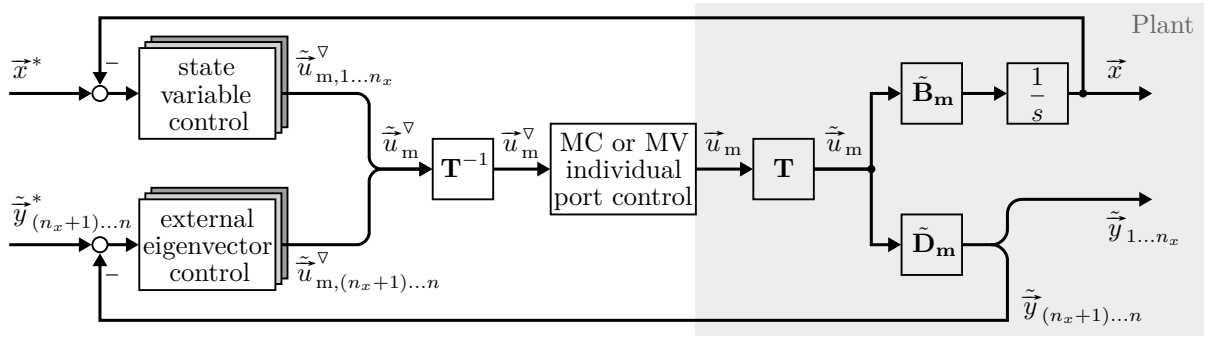



Figure 5.10: Decoupled control system for one interconnected converter port [129]

Figure 5.10 shows a decoupled, closed-loop control system for the actively controlled interconnected converter port. The first step in implementing the decoupling technique from the previous sections is to establish the MC-type or MV-type behavior of all individual ports, which guarantees that all current or voltage sources are actively and precisely manipulable, as already discussed in Section 5.1.2. This is shown in the block in the center of Fig. 5.10. It translates the commanded manipulated inputs $\vec{u}_\mathrm{m}^\nabla$ into actual manipulated inputs $\vec{u}_\mathrm{m}$ in the hardware.

The control plant, i.e., the interconnected port, is shown in decoupled coordinates, which is expressed by the multiplication with the suitable matrix $\mathbf{T}$ for the respective interconnection variant of the interconnected port. In transformed coordinates, $\tilde{\vec{u}}_\mathrm{m}$ now expresses manipulated input patterns that are applied to the system. Each of those manipulated input patterns either influences a single state through the diagonalized matrix $\tilde{\mathbf{B}}_\mathbf{m}$, if it is an internal eigenvector, or it influences a single output through the diagonalized matrix $\tilde{\mathbf{D}}_\mathbf{m}$, if it is an external eigenvector. Hence, all cross couplings are removed. For the sake of simplicity, a possible disturbance input is not shown in Fig. 5.10. As already discussed, the state variables $\vec{x}$ are assumed to be measured. The system outputs $\vec{y}$, which are also measured, must be transformed into decoupled coordinates by multiplication with the matrix $\mathbf{T}$ before they can be used as control feedback. This is already included in Fig. 5.10 since the entire plant is shown in decoupled coordinates; in a real system, however, this matrix multiplication must be executed as part of the control law.

Due to the diagonal structure of the matrix $\tilde{\mathbf{B}}_\mathbf{m}$ from (5.17), the applied internal eigenvectors, i.e., the first $n_x$ manipulated input patterns $\tilde{\vec{u}}_{\mathrm{m},1\ldots n_x}$ only manipulate the state variables $\vec{x}$. However, due to the diagonal structure of the matrix $\tilde{\mathbf{D}}_\mathbf{m}$ from (5.15), which contains the internal eigenvalue 0 on the first $n_x$ diagonal entries, those internal eigenvectors cannot be measured, hence the respective system outputs $\tilde{\vec{y}}_{1\ldots n_x}$ are zero as long as no disturbance input is present. In turn, the applied external eigenvectors $\tilde{\vec{u}}_{\mathrm{m},(n_x+1)\ldots n}$, i.e., the remaining $(n - n_x)$ manipulated input patterns, directly replicate at the output $\tilde{\vec{y}}_{(n_x+1)\ldots n}$ because the diagonalized matrix $\tilde{\mathbf{D}}_\mathbf{m}$ contains the external eigenvalue 1 on the respective diagonal entries. However, they do not influence the state variables as seen in the right-hand part of (5.17).

Since all cross couplings are removed, the control loops for each of the $n_x$ state variables and each of the $(n - n_x)$ eigenvectors can be designed separately and individually. If the individual ports are MC-type ports, the state variables are voltages and the external eigenvectors are current patterns, while the capacitors in the individual ports represent ideal integrators. In this case, all control loops of the state variables are the same as the voltage control loop that has been discussed in Section 4.3.2; the plant contains a single capacitance. Therefore, simple PI regulators can be used to control each of the state variables individually, the design process being the same as in Section 4.3.2. In turn, all control loops of the external eigenvectors are the same as the current control loop that has been discussed in Section 4.3.1; the plant is a direct feed-through. Therefore, a control loop can be designed for each external eigenvector individually as discussed in Section 4.3.1. In the case of MV-type individual ports, the roles of currents and voltages, as well as the roles of capacitances and inductances are swapped, respectively, but the control design process remains the same.

The outputs of the aforementioned controllers are commanded magnitudes $\tilde{\vec{u}}_{\mathrm{m}}^{\triangledown}$ for the associated internal and external eigenvectors. Before applying those commands to the plant, however, it is necessary to transform those eigenvector magnitudes back into individual commands $\vec{u}_{\mathrm{m}}^{\triangledown}$ for all interconnected ports. This is done by the multiplication with the inverse transformation matrix $\mathbf{T}^{-1}$, which must be included in the control law.

In summary, by designing the closed-loop control system in decoupled coordinates, each state variable and each external eigenvector can be controlled individually and without any cross couplings. The design process of those control loops is the same as in Section 4.3. Those controllers do not contain anything more complex than a PI controller. All that is required is to establish the MC or MV behavior of the individual ports, to multiply the system output $\vec{y}$ with the transformation matrix $\mathbf{T}$, and eventually to translate the control commands back to commands for the individual ports by multiplication with the inverse matrix $\mathbf{T}^{-1}$.

### 5.4.2 Modeling the Uncontrolled Interconnected Port

As already discussed, the decoupled control can be applied to only one of the interconnected converter ports, while the other one has to be left uncontrolled. The reason is that a single dc-dc converter can manipulate only one power flow, which happens at the individual port for which the MC or MV behavior is established. As dc-dc converters are power-conservative, the uncontrolled individual port is best modeled as a constant-power source (CPS) or constant-power load (CPL) with additional passive components. In the following, the schematic symbols from [62] as shown in Fig. 5.11 are used for the CPS and CPL elements. These circuit elements are inherently nonlinear, hence the uncontrolled port, together with the electrical load attached to it, forms a nonlinear system. Naturally, the question arises whether this nonlinear system is stable.

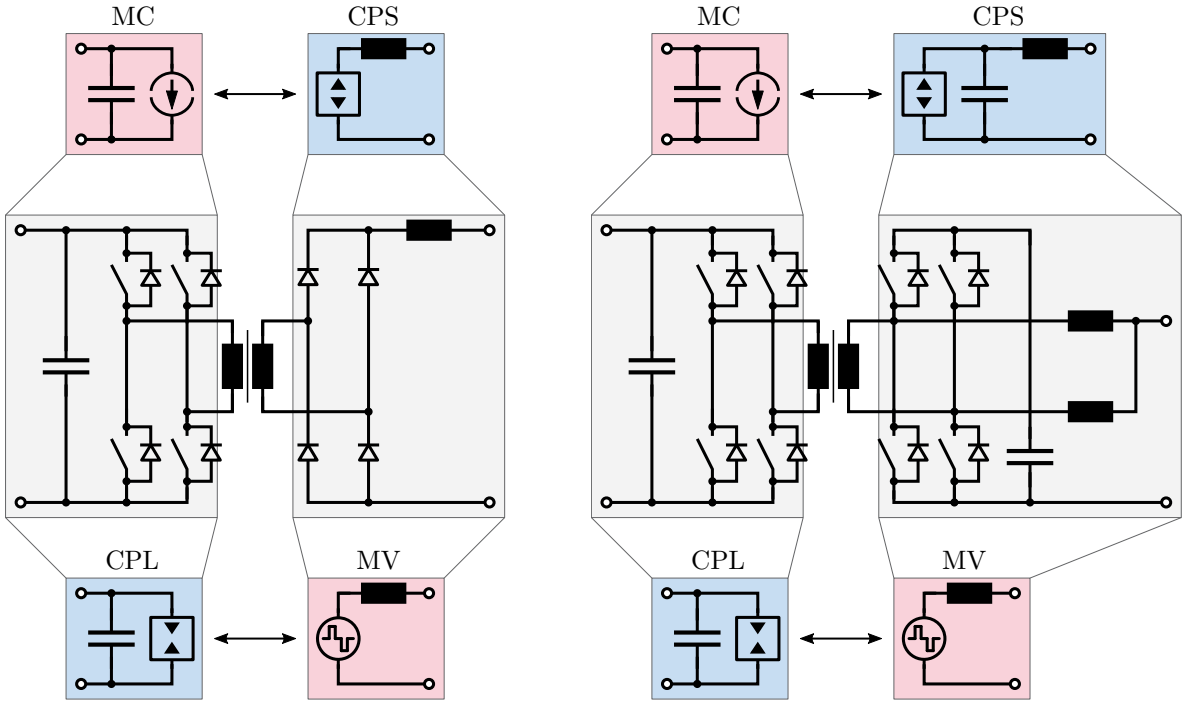

(a) CPS symbol (b) CPL symbol

Figure 5.11: Schematic symbols for constant-power elements as in [62]

It is important to note that the uncontrolled side of a single PEBB cannot be classified as MC-type or MV-type anymore because as explained in Section 5.1.2, this classification only applies to one port of the dc-dc converter being actively programmed to behave like a current or voltage source. The other, uncontrolled port, is purely passive. To illustrate the point, Fig. 5.12 shows the two exemplary topologies that have already been shown in Section 5.1.2, namely the PSFB and the current-fed DAB converter. The power flow is assumed in the direction from left to right, i.e., from the primary to the secondary side. For both topologies, either the primary or the secondary side can be made to behave like an MC-type or an MV-type port; this actively controlled side is shaded in magenta, while the uncontrolled port is shaded in blue. At the top, the equivalent circuits for an active control of the primary sides are shown, which results in MC-type primary-side ports for both topologies. In this case, the secondary sides are CPS circuits. At the bottom, the equivalent circuits for an active control of the secondary sides are shown, resulting in MV-type secondary-side ports for both topologies. In this case, the primary sides are CPL circuits. It has to be emphasized that for the uncontrolled ports, all passive components have to be included. For example, when the secondary side of the current-fed DAB is actively controlled, a closed-loop voltage control acts on the secondary-side dc-link capacitor, making it behave like a controlled voltage source and thus realize the MV characteristic; hence, the secondary-side dc-link capacitor does not appear in the equivalent circuit. If the secondary side of the current-fed DAB is left uncontrolled, however, the dc-link capacitor has to be included in the equivalent circuit, in full agreement with the open-loop model shown in Fig. 3.9 in Section 3.3.3.

Moving from a single dc-dc converter to a modular converter system consisting of $n$ PEBBs, the same way of modeling shall be applied. The approach to controlling the entire converter is to apply the coordinate transformations from Section 5.3 to either the primary-side or the secondary-side interconnected port and leave the other port uncontrolled. In this case, the uncontrolled interconnected port can be represented by an interconnection of CPS or CPL elements with passive components. Together with the electrical load attached to its terminals, a nonlinear system is created.

Controlling a modular dc-dc converter system should make it possible to manipulate the overall transferred power and to control all state variables. Applying the decoupling technique introduced in Section 5.3 to one interconnected converter port implies making all of its individual converter ports behave like MC-type or MV-type ports. The decoupling




(a) PSFB converter (b) Current-fed DAB converter

Figure 5.12: Complete model of exemplary dc-dc converter topologies, assuming a power flow from left to right. Top: The primary sides are actively controlled. Bottom: The secondary sides are actively controlled.

technique then provides control inputs that each manipulate only one state variable in this interconnected converter port, while not affecting all other state variables. This makes it possible to implement a closed control loop separately for every state variables, such as the midpoint voltages in series-connected MC-type ports. This seems, at first sight, absolutely mandatory for every state variable because in the example of series-connected MC-type ports, any current mismatch would cause the midpoint voltages to drift, hence an open-loop control seems to be inherently unstable. The same applies to the parallel connection of MV-type ports, where small voltage mismatches result in a current drift and an increasing current mismatch. However, applying the decoupling technique to only one interconnected converter port means leaving the other one completely uncontrolled, which seems impractical because the interconnections in this port may also require active balancing to avoid instability due to drifting of the state variables.

An intuitive solution might consist in applying the decoupling technique from Section 5.3 to both interconnected ports and not leaving any of them uncontrolled. However, in many cases this results in an overdetermined system, whenever the number of states of both interconnected ports added together exceeds the number of PEBBs, i.e., the number of manipulated inputs. In such a case, it would be impossible to find current patterns for the entire system that would each manipulate a single state variable because of the relationships between the primary-side and secondary-side ports. Inevitably, either

some state variables would have to be left uncontrolled or some states would have to be controlled simultaneously.

An example for such a case is the input-series output-series (ISOS) interconnection of two DABs, as shown in Fig. 5.13. It must be ensured that the midpoint voltages on the primary and the secondary side, highlighted in magenta, are equal to half of the respective dc-link voltage. On the primary side, for example, any current mismatch of the two DABs could cause the midpoint voltage $u_{\mathrm{PB}}$ to drift, rendering the system unstable. Additionally, the power transfer must be manipulable, e.g., through the source current $i_{\mathrm{src}}$, which is highlighted in blue. Hence, there are three control variables, but since there are only two PEBBs, only two manipulated inputs are available, which makes the system overdetermined. Insisting on the closed-loop control of each variable would categorically rule out such overdetermined interconnections. It would also make the modeling a lot more complex because both interconnected ports would have to be considered in a single state-space model, which had been avoided for good reason in Section 5.3.

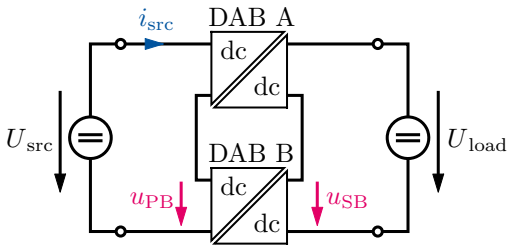



Figure 5.13: ISOS interconnection of two DABs

Instead, leaving one interconnected converter port uncontrolled, as proposed in this dissertation, is the only way to control such overdetermined systems. However, this can only work if all states in the uncontrolled port are stable, which may seem unlikely for state variables like the midpoint voltages of series-connected capacitors. Fortunately, uncontrolled converter ports can indeed be stable under certain circumstances, which is analyzed in the following section. Therefore, the decoupling technique from Section 5.3 should be applied to the interconnected port whose state variables would be unstable without a closed-loop control. The other port can be left uncontrolled if its stability can be proven. Therefore, the following section addresses the stability or instability assessment of uncontrolled interconnected converter ports.

In summary, to control the complete, modular dc-dc converter, the decoupling technique from Section 5.3 is applied to only one of the two interconnected ports, while the other one is left uncontrolled. This uncontrolled port can be modeled using constant-power elements, thus forming a nonlinear system together with the load that is attached to its terminals. In the following, it has to be analyzed under which circumstances the state variables of an interconnected port are unstable; the decoupling technique should then be applied to this interconnected port to enable closed-loop control of its state variables and thus to guarantee system stability. For the uncontrolled port, however, it must be proven that it is stable even without a closed-loop control.

### 5.4.3 Stability Assessment

As illustrated in the previous section, it is crucial to determine under which conditions an uncontrolled converter port is stable. Since it consists of nonlinear constant-power elements such as CPS and CPL, the stability concept and the direct method by LYAPUNOV as introduced in Section 3.1.3 are used.

The uncontrolled converter port of each dc-dc converter topology has an individual equivalent circuit, dependent on the passive elements that are present in that port. Exemplary equivalent circuits of uncontrolled converter ports are shaded blue in Fig. 5.12. These uncontrolled individual converter ports can then be interconnected in an arbitrary fashion to form an uncontrolled interconnected port. Because of the many possibilities for both the equivalent circuit and the interconnection scheme, it is impossible to cover all combinations using a generalized mathematical stability proof.

However, the methodology of proving the stability of an interconnected converter port using the direct method by LYAPUNOV can be utilized for every possible scenario. This methodology is formulated as a step-by-step procedure later in this section. Since all stability assessments made in this dissertation yield the same result, it is possible to formulate a generalized rule of thumb even without a universal mathematical proof.

One of the simplest possible networks is obtained if only one individual dc-dc converter is assumed; this network contains only one constant-power element and a parallel capacitor, as shown in Fig. 5.14. In the following, the stability is analyzed for both power flow directions, i.e., assuming the converter port to act either as a CPS or as a CPL. This does not yet represent an uncontrolled, interconnected port consisting of multiple PEBBs, which is addressed in a second step.


(a) With CPS (b) With CPL

Figure 5.14: Uncontrolled port of a single dc-dc converter with a shunt capacitor, considering both power flow directions

In a first step, the nonlinear state-space model of the system needs to be developed, with the power $P$ acting as manipulated input, the voltage $u$ being the state variable and the current $i$ representing the disturbance input. At first, the CPS case assuming positive power flow shall be analyzed:

$$C\frac{\mathrm{d}u}{\mathrm{d}t} = \frac{P}{u} - i. \tag{5.75}$$

As the state variable appears in the denominator of (5.75), this system cannot be expressed using matrices and hence, it is nonlinear. The second step is to find the equilibrium point $u_{\mathrm{eq}}$ of the nonlinear system, which can be found by setting all time derivatives to zero and solving for the state variable in equilibrium, giving

$$u_{\mathrm{eq}} = \frac{P}{i}. \tag{5.76}$$

To analyze whether this equilibrium point is stable in the sense of Lyapunov, a Lyapunov function needs to be found, which satisfies the conditions from (3.7). Hence, in a third step, the deviation $\Delta u$ of the state variable from the equilibrium point is defined as

$$\Delta u := u - u_{\mathrm{eq}}, \tag{5.77}$$

giving the following modified state-space model:

$$C\frac{\mathrm{d}\Delta u}{\mathrm{d}t} = \frac{P}{u_{\mathrm{eq}} + \Delta u} - i. \tag{5.78}$$

This models a case in which the system is away from its equilibrium point and undergoes a transient that, in the best case of asymptotic stability, ultimately moves it back into the equilibrium point. During this fictional transient, the inputs to the system, i.e., the manipulated input $P$ and the disturbance input $i$ are assumed constant as discussed in Section 3.1.3. To find out whether the system is stable, the following Lyapunov function is formulated, which satisfies all conditions from (3.7):

$$V(\Delta u) = \frac{1}{2} C \cdot \Delta u^2. \tag{5.79}$$

This also satisfies the condition from (3.10) for the exponential stability criterion with $\beta = 2$ and $\delta_1 = \delta_2 = \frac{1}{2}C$. Finally, the time derivative of the Lyapunov function can be computed using (3.9),

$$\begin{aligned}
\frac{\mathrm{d}V(\Delta u)}{\mathrm{d}t} = C\Delta u \cdot \frac{\mathrm{d}\Delta u}{\mathrm{d}t} &\overset{(5.78)}{=} \Delta u \cdot \left( \frac{P}{u_{\mathrm{eq}} + \Delta u} - i \right) = \frac{P\Delta u - \Delta u \cdot i(u_{\mathrm{eq}} + \Delta u)}{u_{\mathrm{eq}} + \Delta u} \\
&\overset{(5.76)}{=} \frac{P\Delta u - P\Delta u - i\Delta u^2}{u_{\mathrm{eq}} + \Delta u} \overset{(5.77)}{=} -\frac{i\Delta u^2}{u} \leq -\frac{i\Delta u^2}{u_{\max}} \\
&= -\frac{i}{C u_{\max}} \cdot 2 \cdot \left( \frac{1}{2} C \cdot \Delta u^2 \right) =: -\alpha\beta V(\Delta u),
\end{aligned} \tag{5.80}$$

where $u_{\max}$ denotes the maximum voltage during the fictional transient. If the coefficients $\alpha$ and $\beta$ are strictly positive, the condition (3.11) for exponential stability is fulfilled. The coefficient $\alpha$ is given by

$$\alpha = \frac{i}{C u_{\max}}. \tag{5.81}$$

Hence, $\alpha$ is strictly positive, given that the voltage in a dc-dc converter port must always be positive and assuming that the power flow $P$ and hence the current $i$ are nonzero and

positive. This ultimately proves that the equilibrium point is exponentially stable. In contrast to asymptotic stability, this is an even stronger statement because the coefficient $\alpha$ explicitly defines the dynamics of the exponential convergence into the equilibrium point according to (3.6). This result also makes physical sense because for a positive voltage deviation $\Delta u$, the CPS would deliver a smaller current in response, counteracting the voltage deviation.

The entire calculation can also be done for the case with a CPL, in which the signs of the manipulated input $P$ and the disturbance input $i$ are reversed. In this case, it is easy to see that the derivative of the LYAPUNOV function now must be positive at all times, which means that for a CPL, the system is proven to be unstable according to (3.8). This also makes physical sense because for a negative voltage deviation, the CPL would draw an even higher current in response, discharging the capacitor further.

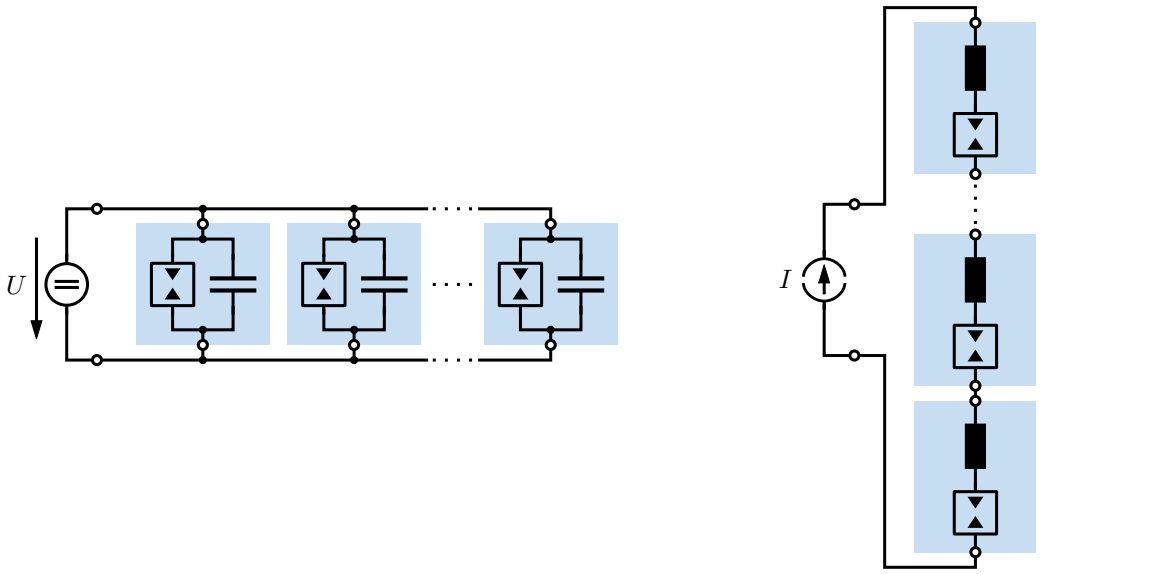
This leads to the rule of thumb that the power outlet port of a dc-dc converter, containing only CPS elements, tends to be stable, while the power inlet port of a dc-dc converter, containing only CPL elements, tends to be unstable. The decoupling approach from Section 5.3 should therefore always be applied to the interconnected port at the power inlet of a modular dc-dc converter system. In turn, the interconnected port at the power outlet can be left uncontrolled because it is stable. This result confirms earlier statements from the literature [33, 39, 41, 52, 66].

So far, the mathematical stability proof has only been carried out for a single dc-dc converter and only one passive network attached to the nonlinear constant-power element. Naturally, the stability proof has to be carried out for the specific interconnection scheme that is present at the interconnected port at the power outlet of a modular dc-dc converter system. As already stated, there are many combinations of interconnection schemes and passive networks, so this dissertation can only deliver the proof for a few examples. Nonetheless, the following step-by-step procedure can be followed for proving the stability of any desired interconnection:

1. Derive the nonlinear state-space model of the system
2. Find the equilibrium point
3. Re-formulate the state variables in terms of their deviation from the equilibrium point re-derive the state-space model
4. Define the LYAPUNOV function in terms of the deviation vector
5. Show that the derivative of the LYAPUNOV function is strictly negative to prove asymptotic stability, or show (3.11) to prove exponential stability.

It is important to note that some interconnection variants do not increase the number of states for nonlinear, uncontrolled port interconnections. As with linear MC-type ports, connecting multiple of the individual ports shown in Fig. 5.14 in parallel does not increase the number of states because this clamps the voltage across the involved capacitors to

the same value. This means that the shown stability proof also applies to multiple of the individual ports connected in parallel. Consequently, also the series connection of ports consisting of a constant-power element and a series inductor does not increase the number of states, similar to MV-type linear ports. It is even possible to reduce the number of states to zero, whenever the value of the state variable is fixed by an external, ideal source. Such cases with zero state variables are the most desirable interconnections because they are stable even with a CPL; the schematics are shown in Fig. 5.15.




(a) Parallel-connected CPL with shunt capacitor and ideal voltage source

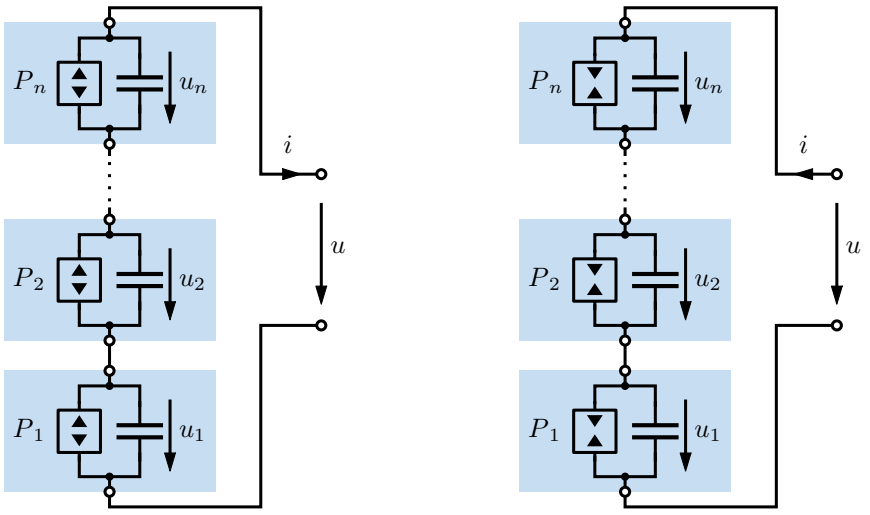
(b) Series-connected CPL with series inductor and ideal current source

Figure 5.15: Inherently stable interconnections of uncontrolled ports with a CPL and an ideal source

In the following, an example with more than one state variable shall be analyzed using the proposed step-by-step procedure. While the parallel connection of the ports from Fig. 5.14 does not increase the number of states, their series connection does. Hence, the next example is an uncontrolled interconnected port with $n > 1$ series-connected, capacitive individual ports. The equivalent circuits of this interconnection are shown for both power flow directions in Fig. 5.16.

Following the proposed step-by-step procedure, the nonlinear state-space model of the system with CPS elements is derived, using the voltages $u_p$ as states, the power sources $P_p$ as manipulated inputs, and the current $i$ as disturbance input:

$$C\frac{\mathrm{d}u_p}{\mathrm{d}t} = \frac{P_p}{u_p} - i \quad \text{for all} \quad p = 1 \ldots n. \tag{5.82}$$




(a) With CPS (b) With CPL

Figure 5.16: Uncontrolled interconnected port containing $n$ series-connected individual ports with shunt capacitors considering both power flow directions

The capacitance $C$ of each port is assumed equal. In the second step, the equilibrium point is found by setting the time derivative in (5.82) to zero, giving

$$u_{\mathrm{eq}p} = \frac{P_p}{i} \quad \text{for all} \quad p = 1 \dots n. \tag{5.83}$$

Defining $\Delta u_p$ as the voltage deviation from the equilibrium $u_{\mathrm{eq}p}$, the state-space model can be re-derived as

$$C\frac{\mathrm{d}\Delta u_p}{\mathrm{d}t} = \frac{P_p}{u_{\mathrm{eq}p} + \Delta u_p} - i \quad \text{for all} \quad p = 1 \dots n. \tag{5.84}$$

The Lyapunov function in step 4 is now defined as

$$V(\Delta u_1, \dots, \Delta u_n) = \sum_{p=1}^{n} \frac{1}{2} C \Delta u_p^2, \tag{5.85}$$

and its time derivative can be computed as follows:

$$\begin{aligned}
\frac{\mathrm{d}V}{\mathrm{d}t} &= \frac{\mathrm{d}}{\mathrm{d}t} \sum_{p=1}^{n} \frac{1}{2} C \Delta u_p^2 = \sum_{p=1}^{n} C \Delta u_p \cdot \frac{\mathrm{d}\Delta u_p}{\mathrm{d}t} \overset{(5.84)}{=} \sum_{p=1}^{n} \Delta u_p \cdot \left( \frac{P_p}{u_{\mathrm{eq}p} + \Delta u_p} - i \right) \\
&= \sum_{p=1}^{n} \frac{P_p \Delta u_p - \Delta u_p \cdot i(u_{\mathrm{eq}p} + \Delta u_p)}{u_{\mathrm{eq}p} + \Delta u_p} \overset{(5.83)}{=} -\sum_{p=1}^{n} \frac{i \Delta u_p^2}{u_p} \\
&\leq -\frac{i}{C \cdot \max\limits_{p} \{u_{\mathrm{max}p}\}} \cdot 2 \cdot \sum_{p=1}^{n} \frac{1}{2} C \Delta u_p^2 =: -\alpha\beta V.
\end{aligned} \tag{5.86}$$

Again, this proves exponential stability for the interconnection from Fig. 5.16a. If the case with reversed power direction from Fig. 5.16b using CPL elements is assumed, $P_p$ and $i_p$ all change signs, which makes the derivative of the LYAPUNOV function always positive, proving instability according to (3.8).

For the example of the ISOS interconnection of two DABs in Fig. 5.13, this means that the primary-side midpoint voltage should be controlled because since it acts as the power input, it would be unstable without a closed-loop control. If the primary-side midpoint voltage is controlled to half of the dc-link voltage, the power deliveries $P_p$ on the uncontrolled secondary side are equal with the exception of efficiency differences. Since the secondary sides operate as CPS elements, the secondary-side midpoint voltage is exponentially stable; its equilibrium-point value is determined by the power delivery $P_p$ of both PEBBs. It has to be noted explicitly that the power deliveries $P_p$ by the PEBBs do not have to be equal, i.e., power sharing is not a necessary condition for stability.

The same analysis can be repeated for other interconnection variants, for example the parallel connection of uncontrolled individual ports that consist of a constant-power element and a series inductor, or the parallel connection of uncontrolled current-fed ports. Both of these interconnections are used in the experimental part of this dissertation. For the sake of conciseness, however, those stability proofs are moved to Appendix C.

In summary, the stability of an interconnection of uncontrolled, nonlinear converter ports with constant-power elements can be assessed using the direct method by LYAPUNOV. For example, the exponential stability of series-connected ports represented by a CPS and a shunt capacitor was mathematically proven. However, this interconnection becomes unstable if the power flow direction is reversed, i.e., when the CPS is replaced by a CPL. The stability of further interconnections is addressed in Appendix C. In general, uncontrolled interconnected converter ports tend to be stable when they represent the power outlet of a dc-dc converter system. The interconnected port at the power inlet, however, tends to be unstable. Hence, the decoupled control should be applied to stabilize the input side of a dc-dc converter system, while the output side can be left uncontrolled.

### 5.4.4 Guidelines for Control Design

By now, the complete toolbox for modeling, decoupled control, and stability assessment of modular dc-dc converters is assembled. Apart from mandatory control goals, such as the requirement to guarantee system stability and the ability to regulate the overall transferred power, there might be a large number of additional control goals, such as equal power sharing between all PEBBs, some phase-shedding capability, or other control goals. Since these additional control goals are very individual to the target application, this dissertation focuses on the mandatory control goals and only provides guidelines on how to satisfy potential additional control goals. In the following, such basic guidelines for designing the control of a modular dc-dc converter are given. Some of them already

address the design phase of the converter because it is beneficial to consider the control of a modular dc-dc converter from the very beginning, but they can also be applied to already existing systems. It goes without saying that many of the following aspects are conflicting and hence have to be traded off carefully.

**Minimize the number of state variables:** As listed in Table 5.2, the number of state variables depends on the configuration of an interconnected port. For MC-type individual ports, for example, the $x\mathrm{P}y\mathrm{S}$ interconnection has significantly less state variables than the $y\mathrm{S}x\mathrm{P}$ interconnection. The overall number of state variables should be reduced whenever possible, for various reasons: First, if the considered interconnected port acts as the power input, the stability assessment from Section 5.4.3 shows that it can only be stable under a closed-loop control. Hence, the stability of the system depends on the reliability of the sensors and the control hardware. Reducing the number of state variables hence implies an enhanced reliability and lower computational control effort. Additionally, when applying the decoupled control technique from Section 5.3, having less state variables also means having a larger number of external eigenvectors and hence, a larger degree of freedom to address potential secondary control goals. Moreover, having many state variables usually means having less freedom to operate and less redundancy: In a series connection of MC-type ports, for example, all ports have to operate permanently to control the midpoint voltages, and a failure would affect the entire series connection. However, in a parallel connection, some ports may fail or be switched off intentionally while keeping the rest of the interconnected port still operational.

**Identify stable and unstable ports:** Stability is a necessary requirement for any modular dc-dc converter system. Hence, it is mandatory to determine which interconnected port of a modular dc-dc converter system could potentially become unstable. As a rule of thumb, the interconnected port at the power input usually is the unstable one, while the interconnected port at the power output is usually inherently stable, regardless of its interconnection. Therefore, in many cases it is the interconnected port at the power input that needs to be stabilized using closed-loop control. Nevertheless, the stability should always be mathematically assessed using the direct method by Lyapunov, following the step-by-step procedure proposed in Section 5.4.3. It can be possible that a modular dc-dc converter is stable even without any closed-loop control, for example a purely parallel connection of MC-type ports with an ideal voltage source at the power input, as shown in Fig. 5.15.

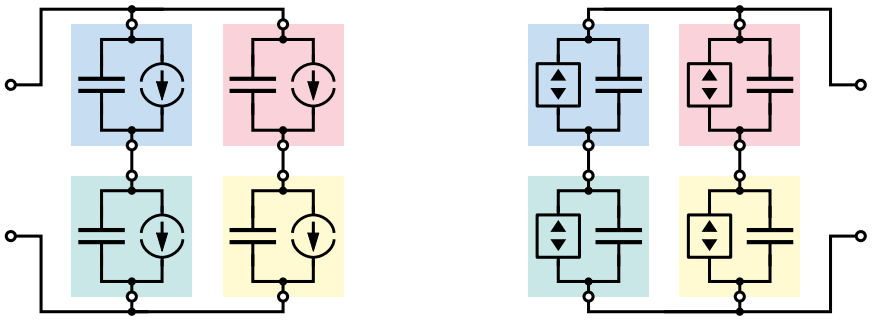
**Apply the decoupling technique where it makes most sense:** In many cases, the decoupling technique needs to be implemented for the interconnected port at the power input of the modular dc-dc converter in order to stabilize the system. However, when the power input port is stable, it is also possible to apply the decoupling technique to the power output port. This is the case for the interconnection variants shown in Fig. 5.15. If there is

a choice, the decision may depend on different factors: As stated in Section 5.1.2, making individual ports behave like MC-type or MV-type ports can be as easy as commanding a duty cycle in an open-loop manner, but it can also be complex and require a closed-loop control in itself, which requires additional sensor hardware. In many cases, it is much easier to make one port of a dc-dc converter topology behave like an MC-type or MV-type port than the other, which should be respected if there is a choice. Moreover, the target application may demand certain characteristics of one interconnected converter port. For example, it may request a precise steady-state voltage or current sharing at that specific port, or some specific transient behavior. Such requirements can in many cases only be fulfilled by a thoroughly designed closed-loop control, which requires the decoupling technique to be implemented at that specific port. The uncontrolled port, in turn, can only be assured to be stable, potentially also exponentially stable. However, no general statement can be made about a certain transient behavior, e.g., an overshoot. Also a voltage or current sharing cannot be guaranteed due to efficiency deviations between the PEBBs. There might be a lot more reasons to consider, which would all be very individual to the target application, such as requirements induced by norms and standards, the cost of the sensors, the availability of sensors in already existing PEBBs, and many more.

**Select state variables and external eigenvectors wisely:** As already stated in Section 5.3, there is a great degree of freedom in choosing the state variables and the external eigenvectors. For every interconnection variant, one of the many possibilities has been discussed; in the analysis of MV-type ports, the same definitions were used as with MC-type ports, although those definitions were less physically insightful. From the perspective of the target application, however, some definitions can be more useful than others, which should be considered in the control design process. Taking possible external eigenvectors of parallel-connected MC-type ports with an ideal voltage source as example, the CM and DM currents can be used to separately regulate overall power transmission and current sharing. Using accumulated currents instead could be helpful when realizing a phase-shedding function. Those choices should be driven by the target application, and one possible criterion could be the physical reference variables and the mathematical effort required to translate them into the actual reference variables for the control loops. In the best-case scenario, the control goals from the target application can all be expressed in terms of state variables and external eigenvectors so that they can be directly controlled.

**Minimize sensor count:** If stability considerations permit, some sensors can be saved at the uncontrolled port of the modular dc-dc converter, unless they are required for other reasons such as circuit supervision and protection. Even beyond, if a tight control of the external eigenvectors is not required, it may suffice to provide closed control loops only for the state variables to guarantee system stability, while controlling the external eigenvectors in an open-loop manner. In this case, there would be no need to measure the system output vector, and those sensors could be saved as well. This is only possible if the open-loop behavior of the controlled MC-type or MV-type ports is sufficiently precise.

**Choose sensible associations between primary and secondary sides:** The advantage of the proposed control approach is that the interconnected ports on both sides of the dc-dc converter system can be considered independently. In theory, the individual converter ports could be arranged randomly in the uncontrolled interconnected port, disregarding the port associations. However, for various reasons, the port associations should be considered nonetheless. Figure 5.17 shows an exemplary dc-dc converter system to illustrate this point. It consists of a 2S2P interconnection in both the controlled and the uncontrolled interconnected port, and its individual ports all contain capacitors. In this example, the ports that are connected in series in the controlled port are associated with ports that are also connected in series in the uncontrolled port, indicated by the color shading. This is beneficial in terms of redundancy; using the shown associations, the failure of a single PEBB would only cause one series-connected branch to stop operating in each interconnected port. Were the ports randomly associated, the failure of a single PEBB could render the whole dc-dc converter system nonfunctional. Moreover, the ports that are connected to the negative dc rail in the controlled port are associated with ports that are also connected to the negative dc rail in the uncontrolled port. This helps to uniformly distribute the isolation voltage across the galvanic isolation barriers of the series-connected PEBBs.

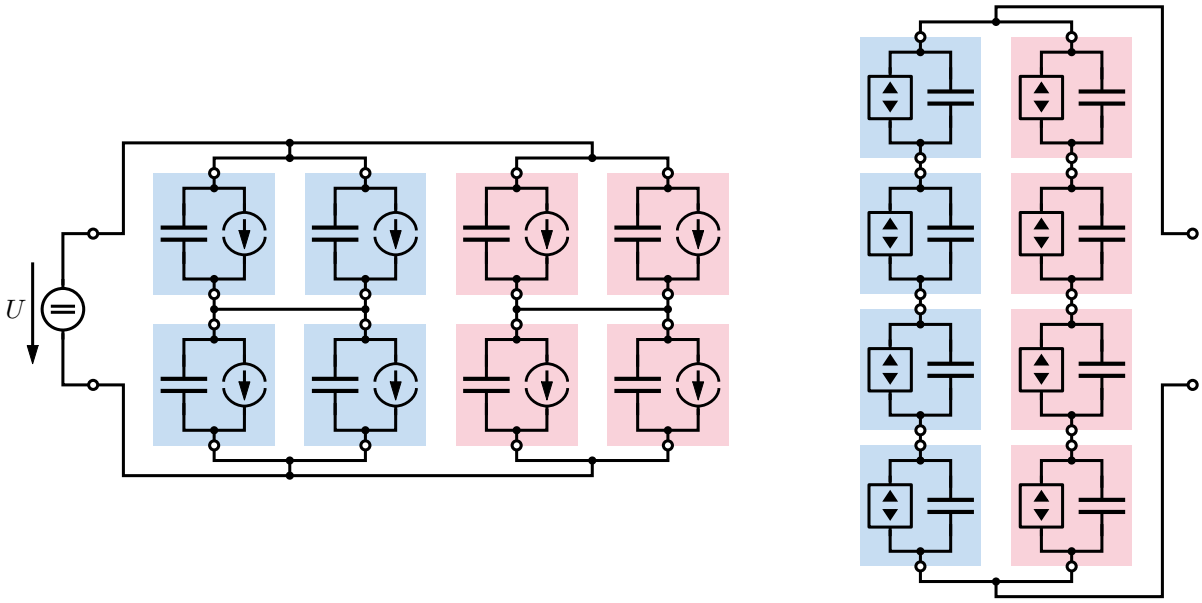


(a) Controlled interconnected port (b) Uncontrolled interconnected port

Figure 5.17: Modular converter system with 2S2P interconnections on both sides, associated ports are shaded in the same color

**Utilize converter partitioning possibilities:** As already mentioned, arranging the primary-side and secondary-side ports of the PEBBs similarly in both interconnected ports is beneficial in terms of redundancy, distribution of isolation voltage and phase-shedding capability. Even more, under certain circumstances it is possible to consider a large interconnected port as an independent interconnection of several smaller interconnected ports. This independence is given in the case of a parallel connection of small MC-type interconnected ports attached to an ideal voltage source, or in the case of a series connection of small MV-type interconnected ports attached to an ideal current source. For example, the complex dc-dc converter system shown in Fig. 5.18 could have been the result of an upgrade of an already existing converter system (ports are shaded in blue) by connecting a second, identical converter in parallel (shaded in magenta). Because of the ideal voltage

source at the controlled interconnected port, it is possible to treat the resulting structure as two independent 2P2S interconnections instead of a complex 2P2S2P interconnection. This not only avoids redeveloping the entire converter software, but also allows to keep the old software running on both dc-dc converter systems independently. If applicable, partitioning also makes complex interconnections that were not considered in Section 5.3 available to decoupling without additional efforts. This approach could also be applied to dc-dc converter systems that are designed in one run; partitioning a large system into smaller subsystems further improves redundancy and phase-shedding capability, but also reduces computational effort, since multiple small matrix multiplications are more efficient than a single large matrix multiplication.




(a) Controlled interconnected port (b) Uncontrolled interconnected port

Figure 5.18: Complex dc-dc converter system that can be modeled as an independent interconnection of two smaller dc-dc converter systems

**Be aware of limitations:** The mathematical approach to decouple the state-space model of an interconnected converter port has some practical limitations. First, making any dc-dc converter port behave like an MC-type or MV-type port is generally not ideal, i.e., there will always be deviations between the reference command and the actually applied current or voltage. These deviations will even vary from one PEBB to another. Hence, the applied internal and external eigenvectors will always be distorted and re-introduce some minor cross couplings to the system. Therefore, applying a specific eigenvector will introduce minor disturbances into other control loops. In many cases, the limited bandwidth of the current or voltage manipulation in MC-type and MV-type ports must be taken into account, especially when this manipulation requires an inner closed-loop control. Therefore, the bandwidth of the control loops for the state variables and the external eigenvectors should be kept well below the bandwidth of the MC or MV port

realization. Additionally, parasitic inductances or capacitances in any interconnected port will also re-introduce minor cross couplings. Likewise, the assumption of ideal sources is not realistic; while capacitors and batteries can be modeled as stiff voltage sources, stiff current sources are considerably less common. Hence, the characteristics of the load have to be taken into account in the control design process as well. Finally, the assumption of all PEBBs being identical is also idealized, especially with respect to the size of the port capacitances or inductances, which tend to vary within a certain tolerance. Any variation between these elements re-introduces cross couplings in the control loops, which have to be designed robustly to deal with those additional, parasitic disturbance inputs.

In summary, designing the control of a modular dc-dc converter system should be mainly driven by the requirements of the target application. While there are some mandatory rules to guarantee system stability, there might remain a large freedom for individual decisions. Those can be hardware decisions, such as choosing an interconnection variant with few state variables, minimizing the sensor count, or wisely arranging the ports on both sides of the converter system. Other degrees of freedom include modeling decisions, such as choosing state variables and external eigenvectors that are suited best for the target application, or making use of partitioning converter models.

## 5.5 Summary

This chapter proposed a thorough mathematical, yet physics-based framework to model, decouple, and control arbitrary, modular dc-dc converter systems. It not only extends the approach for two-converter systems from Chapter 4 to an arbitrary number of PEBBs, it also mathematically contextualizes the decoupling approach.

The basis for finding decoupling techniques for modular dc-dc converter systems is a thorough modeling of the individual PEBBs. While previous approaches from the literature only consider certain topology sub-classes such as PWM-based converters, this dissertation used a modeling approach that is much more universal. The classification of galvanically isolated topologies is done with respect to only one converter port, which is actively made to be have like a controlled current source with a parallel capacitor, referred to as MC-type port, or a controlled voltage source with a series inductor, a so-called MV-type port. Both port types can be represented by a simple equivalent circuit, and this classification is applicable to a wide range of galvanically isolated dc-dc converter topologies. The other port of the converter topology, which is not actively controlled, is power-conservative, hence it has to be modeled using a CPS or CPL.

Whenever multiple MC-type or MV-type individual converter ports are interconnected, a large interconnected converter port is formed. For both port types, four different symmetric interconnection variants are possible, all involving different numbers of state variables. For each of the resulting eight scenarios, the state-space models and coordinate transfor-

mations have been developed to enable the decoupled control of such interconnected ports. The four MC-type and MV-type interconnections have been found to be structurally equivalent when parallel interconnections are swapped for series interconnections.

In the mathematical analysis of the state-space models of interconnected converter ports, it has been found that the state-space matrices $\mathbf{B_m}$ and $\mathbf{D_m}$ contain valuable information about the structure of the interconnected converter port that can be utilized in the decoupling approach. While the matrix $\mathbf{B_m}$ describes which manipulated input patterns influence the state variables, the matrix $\mathbf{D_m}$ describes which manipulated input patterns are measurable at the system output, i.e., at the location of the sensors. It could be shown that the manipulated input patterns in the matrix $\mathbf{B_m}$ are all left eigenvectors of the matrix $\mathbf{D_m}$ corresponding to the eigenvalue 0. Thus, they form the kernel of the matrix $\mathbf{D_m}$, which means that the system input patterns that manipulate the system state cannot be measured at the system output. In turn, all remaining left eigenvectors of the matrix $\mathbf{D_m}$ are called external eigenvectors and correspond to the eigenvalue 1, which means that they can be measured at the system output. They do not manipulate any state variable and can be freely controlled. Based on those eigenvectors, the transformation matrix $\mathbf{T}$ can be derived, which diagonalizes the matrix $\mathbf{D_m}$. Also the manipulated input matrix $\mathbf{B_m}$ is reduced to its diagonal form. Having only diagonal state-space matrices means that the transformation $\mathbf{T}$ decouples the system model; in decoupled coordinates, each state variable and each external eigenvector can be influenced independently.

This decoupling technique can only be applied to one interconnected port because each individual dc-dc converter can only manipulate one independent electrical quantity. The other interconnected port therefore has to be left uncontrolled. Since all PEBBs are power conservative, it contains constant-power elements such as CPS and CPL, which are inherently nonlinear. The direct method by Lyapunov has been utilized to prove the stability of a variety of interconnections; it could be found that interconnected ports containing only CPS elements and hence acting as the power output, tend to be exponentially stable, while interconnected ports containing only CPL elements and hence acting as the power input tend to be unstable. The proof of exponential stability should raise the confidence to a wider use of converter interconnections that would previously have been considered overdetermined, such as the ISOS interconnection of DAB converters.

Finally, the control design of modular dc-dc converter systems has been addressed. The general approach is to apply the decoupling technique using the proposed eigenvector-based coordinate transformation to one interconnected converter port, while leaving the other interconnected converter port uncontrolled. This requires the uncontrolled interconnected converter port to be stable. For the decoupled port, control loops can be implemented independently for every state variable and every external eigenvector. However, there are still many degrees of freedom in the actual control design, and the actual control requirements are mostly driven by the target application. Hence, a series of guidelines has been proposed that facilitate pursuing the most robust, most physically meaningful, and most simple modeling approach to enable a very straightforward and simple eigenvector-based control of a large, modular dc-dc converter system.

# 6 Experimental Validation

In the previous chapters, the modeling, decoupling, and control of modular dc-dc converter systems has been addressed, first for a dc-dc converter system consisting of two power-electronic building blocks (PEBBs), then for an arbitrary number of PEBBs. This mostly theoretical work is put into practice in this chapter. Following the structure of the previous chapters, first a validation is carried out on an existing high-power two-converter system; this dc-dc converter is the galvanically isolated 200 kW on-board charger (OBC) that already has been used in the simulations in Chapter 4. Most experimental results on the decoupled control of this converter have been published in [105]. After this, a low-power, multi-PEBB system is designed, tailored to the validation of the higher-level decoupling and control techniques from Chapter 5. The experiments on this hardware cover the decoupled control of all eight possible interconnection variants of both manipulated current (MC) and manipulated voltage (MV) port types, as well as a validation of the stability analysis from Section 5.4.3.

## 6.1 Case Study: On-Board Charger for Catenary Trucks

Chapter 4 discussed the decoupled control of a modular two-converter system, a 200 kW OBC for a catenary truck, which consists of two three-phase dual-active bridges (DABs) rated 100 kW each. For compatibility with various dc voltage levels on the overhead lines, the primary sides of the two PEBBs can be connected either in parallel or in series. As the secondary sides are connected in parallel, either an input-parallel output-parallel (IPOP) or input-series output-parallel (ISOP) interconnection can be realized with this setup. For both variants, a decoupled control approach has been developed using the common-mode (CM) and differential-mode (DM) currents, as presented in Section 4.5. In the following sections, the proposed decoupled control in CM/DM coordinates from Chapter 4 is validated. First, the experimental setup is presented, followed by the measurement results. The results have been published in [105].

### 6.1.1 Experimental Setup

Figure 6.1 shows a photograph of the 200 kW OBC. Although the hardware development is not part of this dissertation, a short overview is given, whereas a detailed description can

be found in [105, 122, 127]. Since the OBC consists of two three-phase DAB converters, four dc links and four three-phase semiconductor bridges are needed, respectively. Using ultra-compact 3D-printed metal coolers, all four active frontends consisting of the semiconductor devices, the gate drivers, and the dc-link capacitors are arranged in a volume of only 8 L. This stack of active frontends is visible on the left-hand side of Fig. 6.1. On the right-hand side, the transformers are located; instead of two three-phase transformers, six identical single-phase transformers are used. Further design parameters can be found in Table 4.1 and [105, 122, 127].

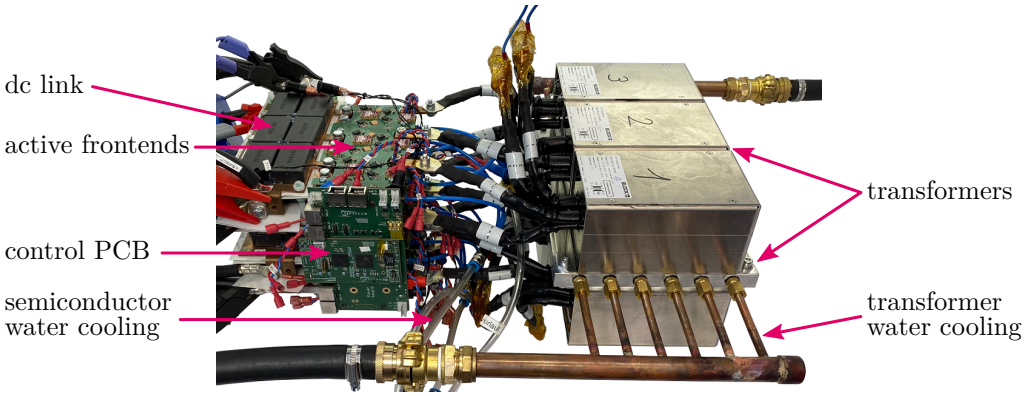
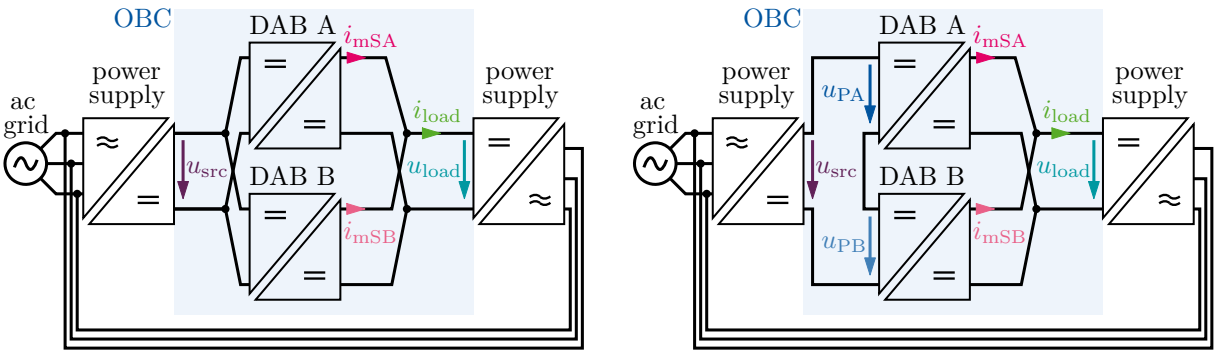



Figure 6.1: Prototype of the 200 kW OBC for catenary trucks [127]

The closed-loop control of the prototype is performed on a printed circuit board (PCB), which is visible in Fig. 6.1. It incorporates an Artix 7 field-programmable gate array (FPGA) by Xilinx/AMD and a dual-core C2000 microcontroller (MCU) by TI, the same set of chips that is used later in Section 6.2.2. The FPGA is used to generate the PWM patterns for the DABs and to acquire the data of all voltage and current sensors. On the MCU, the sensor data is evaluated, the transformation to CM/DM coordinates and back is performed, the control loops are executed, and the open-loop current control for the three-phase DAB according to Section 3.3.1 is implemented. The current and voltage control loops are realized in the same way as introduced in Section 4.3.1 and Section 4.3.2, respectively. For the open-loop current control, the instantaneous flux and current control (IFCC) algorithm from [101] is implemented, as well as the soft start-up and shut-down sequences from [111], which realizes dynamically controllable MC-type ports for both PEBBs.

To operate the prototype in IPOP and IPOP interconnection, it is connected to bidirectional dc power supplies of type EA-PSB 11500-60 from Elektro-Automatik both on the primary and the secondary side. These power supplies are rated 30 kW and can either supply or consume dc power, feeding it back into the ac grid. On the ac side, both power supplies are connected in parallel. For the measurement of the voltages, differential probes of type BumbleBee® from PMK are used in the following sections, while for the measurement of the currents, current probes of type N2781B from Keysight are used.

A schematic of the IPOP and ISOP interconnection of the two PEBBs with the bidirectional power supplies is shown in Fig. 6.2. In the IPOP interconnection shown in Fig. 6.2a, a constant-current (CC) charging of the truck battery can be emulated by setting the secondary-side power supply to constant-voltage mode. However, this is possible only up to the rated power of the power supplies. The secondary-side power supply can be also programmed to emulate a load resistor, realizing a back-to-back (B2B) experiment setup as discussed in Section 4.2. In IPOP interconnection, any commanded DM current circulates between both PEBBs and is only limited by the rated power of each PEBB. For the ISOP interconnection shown in Fig. 6.2b, the primary sides of both PEBBs are connected in series, and thus they share the same dc current. As discussed in Section 4.5, any circulating current causes the primary-side midpoint voltage to drift; hence, power can only be transferred by the CM current, limiting the overall possible power transfer to the power rating of the bidirectional power supplies.




(a) IPOP interconnection

(b) ISOP interconnection

Figure 6.2: Experimental setup of the OBC using bidirectional power supplies [105]

In summary, this section gives a brief overview of the hardware design of the 200 kW OBC. In the experiments, the prototype is used with bidirectional dc power supplies either in IPOP or ISOP interconnection, which allows to implement all scenarios from Chapter 4 in the laboratory.

### 6.1.2 IPOP Interconnection

First, the decoupled control of a B2B experiment shall be experimentally validated, following the decoupled control in CM/DM coordinates proposed in Section 4.5. For this purpose, both PEBBs are connected in IPOP interconnection as shown in Fig. 6.2a. The primary-side power supply provides a constant voltage of 600 V, while the secondary-side power supply is programmed to emulate a load resistance $R_{\mathrm{load}}$.

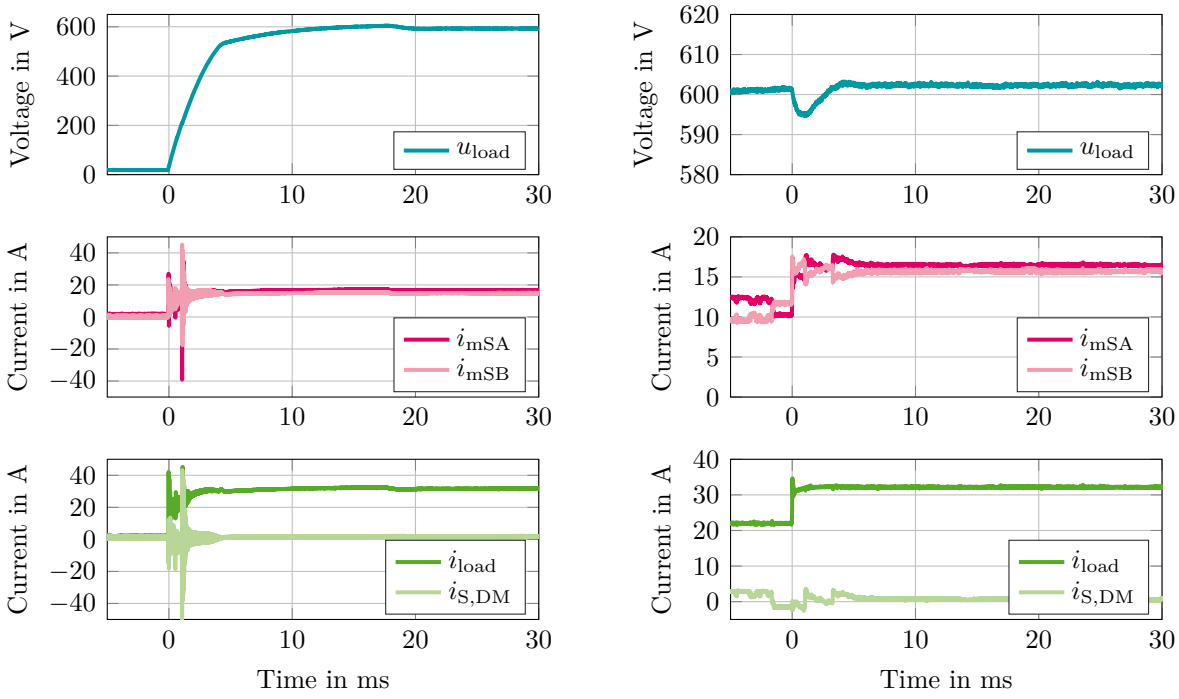
As discussed in Section 4.5, the control tasks for this setup are the closed-loop voltage control of the secondary-side load voltage $u_{\mathrm{load}}$ by manipulation of the CM current as well as the closed-loop control of the circulating DM current. Since the secondary-side

power supply emulates a load resistance, some load current $i_{\mathrm{load}}$ is present in the system, which in itself would not be necessary for the B2B experiment; however, the disturbance rejection properties of the closed-loop voltage controller can be validated this way.

The implementation of these two control loops is done according to Fig. 4.12. For the closed-loop current control acting on the circulating DM current, the integral feedback gain is set to $K_{\mathrm{i,i}} = 75\,{}^{1}\!/\!_{\mathrm{s}}$, which corresponds to an error compensation time constant of $\tau_{\mathrm{d,i}} = 13.3\,\mathrm{ms}$. However, the feedforward branch together with the highly dynamic open-loop current control using the IFCC algorithm allows for a very dynamic manipulation of the DM current. For the closed-loop control of the load voltage, which acts on the CM current, moderate proportional and integral feedback bandwidths of $f_{\mathrm{b,p}} = 50\,\mathrm{Hz}$ and $f_{\mathrm{b,i}} = 20\,\mathrm{Hz}$ are used, respectively.

First, the command-tracking and disturbance-rejection properties of the closed-loop voltage control are experimentally evaluated; the measurements have been published in [105]. Figure 6.3a shows the step response of the closed-loop voltage control. At $t = 0\,\mathrm{ms}$, the load voltage reference is set to the nominal voltage of 600 V, while the DM current reference remains zero. The emulated load resistance is set to $19.3\,\Omega$, which causes a load current of 31.1 A as the load voltage reaches 600 V. It can be seen that the voltage settles to the desired reference within 20 ms, with two distinct phases. For $0\,\mathrm{ms} \leq t < 4\,\mathrm{ms}$, the proportional feedback dominates the step response, before the integral feedback dominates the step response for $t \geq 4\,\mathrm{ms}$. The reason for the two distinct phases is the load resistance, which separates the system poles. It can be seen that the CM current manipulates the load voltage, while the DM current stays zero on average; however there are some oscillations shortly after 0 ms, which result from the inductance of the wiring that establishes the secondary-side parallel connection. Figure 6.3b shows the disturbance response of the closed-loop voltage control. While the load voltage is regulated to 600 V, the emulated load resistance is suddenly changed from $29\,\Omega$ to $19.3\,\Omega$, which corresponds to a load current step from 20.7 A to 31.1 A. Only a small undershoot of 6.7 V, i.e., about 1.1 %, can be observed, before the voltage returns to its reference value. The DM current remains at 0 A, while some deviations for $t \leq 6\,\mathrm{ms}$ are due to the small phase-shift angles of only a few degrees. A phase-shift angle of 1° corresponds to a time delay of only 70 ns at a switching frequency of 50 kHz; hence, the shape of the switching transients, the zero-voltage switching (ZVS) boundaries, and the deadtime interval all influence the currents, which is not modeled by the open-loop current control. Overall, the performance of the closed-loop voltage control is validated successfully.

In the next step, the decoupling of the load voltage and DM current control loops is validated; the measurement is also published in [105]. Figure 6.4 shows a measurement in which the load voltage is controlled to 600 V with a load resistance of $29\,\Omega$, while the DM current reference is changed from 0 A to 40 A, which corresponds to a power change of 12 kW in both PEBBs. Indeed, due to the dynamic open-loop current control, the initial transient of the DM reaches a value of approximately 45 A within 25 µs, which reflects in current changes of opposite signs in both measured terminal currents. Some short-lived oscillations are present for approximately 350 µs, caused by the inductance of the sec-




(a) Step response

(b) Disturbance response

Figure 6.3: Measurement of the closed-loop voltage control in a B2B experiment [105]

ondary-side parallel connection. After the transient, the integral regulator compensates the remaining current error until the DM current reaches the reference of 40 A. During the experiment, the load voltage changes by 1.7 %, which is suspected to be a result of a voltage drop caused by the circulating current. Overall, the measurement demonstrates the clean decoupling between the two control loops during a B2B experiment.

In summary, the decoupled control of a B2B experiment as proposed in Section 4.5 has been successfully validated. It could be shown that the closed-loop voltage control has good command-tracking and disturbance-rejection properties, and that the voltage and current control loops do not interact during a B2B experiment.

### 6.1.3 ISOP Interconnection

In the next step, the ISOP interconnection of the two PEBBs is experimentally evaluated, using the decoupled control in CM/DM coordinates proposed in Fig. 4.14. For this purpose, the OBC is configured as shown in Fig. 6.2b. In this experiment, the primary-side power supply provides a constant dc voltage of 800 V, while the secondary-side power supply provides a constant voltage of 400 V, which corresponds to the scenario discussed in Section 4.5.

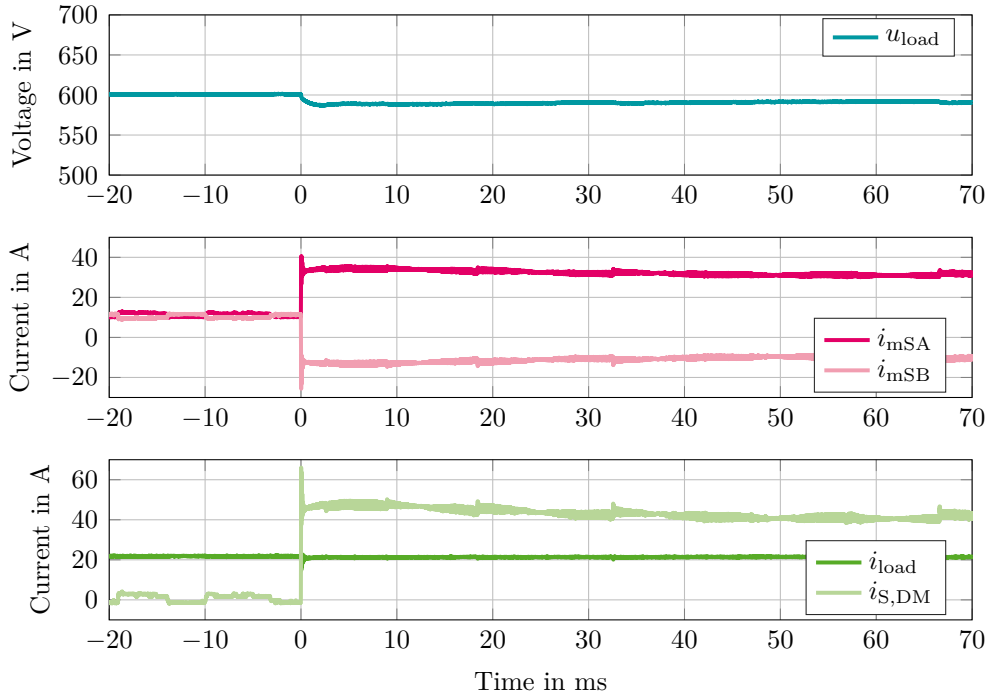



Figure 6.4: Decoupled control of the load voltage and the DM current, step response of the DM current [105]

As discussed in Section 4.5, a voltage control loop is implemented to keep the primary-side midpoint voltage at half of the primary-side dc voltage. This voltage controller acts on the DM current, which directly manipulates the midpoint voltage. The CM current, however, can be freely manipulated, since the secondary-side power supply is programmed to provide a constant voltage rather than emulating a load resistance. As keeping the primary-side midpoint voltage stable is a critical control task, the proportional and integral feedback bandwidths are increased to $f_{\text{b,p}} = 1\,\text{kHz}$ and $f_{\text{b,i}} = 400\,\text{Hz}$, respectively. Additionally, a first-order filter is added on the CM current reference because parameter mismatches in the open-loop current control could still introduce minor cross couplings and disturb the midpoint voltage control.

A resistive voltage divider connected to the primary-side series connection initially ensures asymmetric voltages, the initial midpoint voltage is 443 V. Figure 6.5 shows the measurement of the controlled ISOP interconnection. At $t = 0\,\text{ms}$, the experiment is started with a midpoint voltage reference of 400 V, which corresponds to half of the primary-side dc-link voltage, and a CM current reference of 50 A, which corresponds to a power transfer of 20 kW. Within 300 µs, the midpoint voltage is brought inside a tolerance band of ±5 % around the reference, which is accomplished by a transient of the DM current. In steady state, however, the DM current remains zero because otherwise it would cause the midpoint voltage to drift. In turn, the CM current rises until it also reaches the reference of 50 A. Overall, this demonstrates the stable operation in ISOP interconnection at 20 kW of transferred power. Further measurements are shown in [105].

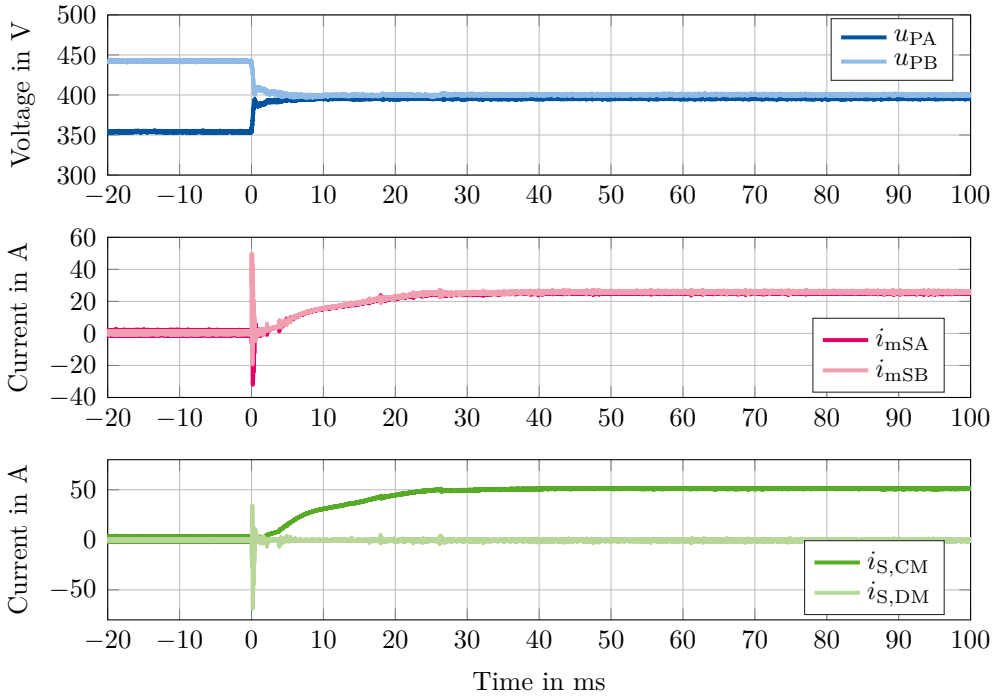



Figure 6.5: Decoupled control of the primary-side midpoint voltage and the CM current in an ISOP interconnection

In summary, the decoupled control of an ISOP-interconnected OBC as proposed in Section 4.5 has been successfully validated. The primary-side midpoint voltage is tightly controlled using the DM current, while the CM current is used to manipulate the transferred power.

## 6.2 Validation on Modular, Low-Power DC-DC Converters

The experiments from the previous section were successful in validating the decoupled control of a two-converter system, however on this hardware it is generally not possible to cover all converter configurations that have been explored in this dissertation. For one, the minimum number of PEBBs to distinguish an $x$P$y$S from a $y$S$x$P interconnection is four, which is more than the two 100 kW DABs that were used in the previous section. But even more, a three-phase DAB is best operated as a controlled current source, hence making either of its ports act as an MC-type port is very natural, while implementing an MV-type port on this topology would be complex, requiring at least a series inductor.

For these reasons, a platform of smaller scale is designed, built, programmed, and commissioned to cover all interconnection variants explored in Chapter 5. The platform consists

of a control PCB with an MCU and an FPGA as well as four sockets, each of which can hold a PEBB with 200 W rated power. By connecting the dc terminals of the four PEBBs using copper busbars, various series and parallel interconnections can be realized on both the primary and the secondary side.

The following sections first cover the design of this platform, followed by a brief description of the software. Then, the setup and the design of the experiments is discussed, before all configurations from Chapter 5 are tested experimentally.

### 6.2.1 Hardware Design

For the validation of the various decoupling approaches from Chapter 5, a flexible platform containing multiple PEBBs is to be designed. The requirements for the PEBBs are:

- A galvanically isolated topology should be selected that contains at least one port that can be operated as an MC-type port and also one that can be operated as an MV-type port. It also has to be bidirectional to assess the system stability when it acts as the power input or output.
- The entire topology including sensors, drivers, and peripherals should be accommodated on a single PCB of small physical size, to make the PEBB modules easy to attach to a common control platform via a single connector.
- Only off-the-shelf components should be used to allow easy re-configuration and replacement. The focus is put on a robust design rather than on efficiency optimization.
- The switching frequency should be maximized to enable relatively high control bandwidths.
- Sensors should be implemented in all places required to validate the decoupling of every interconnection variant from Chapter 5.

The topology that is chosen to meet these requirements is the current-fed, single-phase DAB as introduced in Section 3.3.3; its schematic is shown in Fig. 6.6. As discussed in Section 5.1.2, the secondary-side port can be operated as an MV-type port under a closed-loop voltage control, while the primary side can be operated as an MC-type port. Together with its bidirectional power transfer capability, it fulfills the aforementioned requirements. All quantities shown in color in Fig. 6.6 are measured using sensors, which enables to use all decoupling and control techniques from Chapter 5.

The targeted rated power of this converter is 200 W for rated voltages of 48 V on the primary side and 24 V on the secondary side[(i)]. The component selection for this topology,

[(i)] This implies 48 V secondary-side dc-link voltage due to the buck characteristic of the current-fed port.

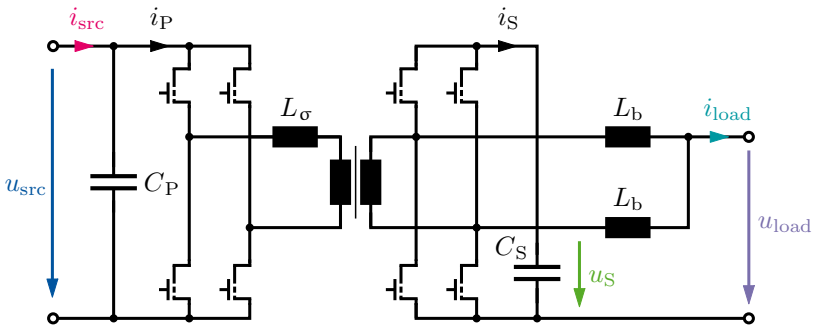



Figure 6.6: Current-fed, single-phase DAB as used in the experimental validation. All colored quantities are measured.

utilizing only off-the-shelf components, is summarized in Table 6.1. As power semiconductor devices, gallium nitride (GaN) half-bridge integrated circuits (ICs) by EPC are used, which already contain the required gate drivers. This not only simplifies the design, it also allows for a high switching frequency of 250 kHz and a deadtime of as low as 20 ns. The key element for galvanic isolation is a 300 W rated, planar transformer with multiple windings that are all connected in parallel on both the primary and the secondary side to realize a turns ratio of 1. As it has a negligible stray inductance, an external inductor of 4 µH is connected in series with the primary-side winding to limit the power transfer according to (3.44). For an operating point in which both the primary-side and the secondary-side dc-link voltages are 48 V, selecting this inductance results in the rated power of 200 W being transferred at a phase-shift angle of approximately 40°.

The voltage sensors are galvanically isolated delta-sigma ($\Delta\Sigma$) modulators that provide a 20 MHz digital bitstream, in which the rate of occurrence of logical ones and zeros corresponds to the measured voltage. This bitstream can be demodulated in software using a digital filter to obtain the voltage information. For the current, Hall effect-based transducers are used together with an analog-to-digital converter (ADC) that provides a digital serial interface. The PWM signals can be directly forwarded to the half-bridge ICs; only a galvanic signal isolation is required, which is established using digital isolator ICs. These also contain an isolated 5 V power supply for operating the half-bridge ICs. Both the sensor and PWM signals are transformed into differential signals using differential line drivers and receivers, to minimize disturbances in the communication with the control platform, which are likely in the presence of fast-switching GaN devices.

A photograph of the 200 W PEBB is shown in Fig. 6.7. While the top part of the PCB contains separated regions for the primary-side and secondary-side power stages, the bottom part connects to the low-voltage potential of the control PCB and contains all sensors and the circuitry to receive, transmit, and isolate the digital signals. A main connector is located at the bottom of the board to attach the PEBB vertically to the control platform, whereas at the top of the PCB, the power terminals of both the primary and the secondary side are located. In addition to the voltage sensors, coaxial connectors are provided for each of the measured voltages to attach active, differential probes and

Table 6.1: Component selection for the converter PCB

| Function | Qty. | Type | Manufacturer | Device |
|---|---|---|---|---|
| Semiconductor devices | 4 | GaN half bridge | EPC | EPC23102 |
| Transformer | 1 | planar, 1:1 | Coilcraft | PL300-100L |
| Current-fed inductors | 2 | 10 µH | Würth | 74439370100 |
| DAB inductor | 1 | 4 µH | Coilcraft | SER2013-402MLD |
| Dc-link capacitors | 16 | 10 µF, 100 V, X7S | Murata | GRM32EC72A106ME05 |
| Water cooler | 1 | 3D-printed | IQ evolution | IQ-Big 62 Automotive |
| Dc terminals | 4 | for PCB edges | Würth | 74622103 |
| Voltage sensor | 3 | ΔΣ modulator | TI | AMC3336 |
| Current transducer | 2 | Hall effect | Allegro | ACS37002LLAATR-015B5 |
| ADC (current sensor) | 2 | 16 bit | Analog Devices | LTC2311-16 |
| PWM isolator | 2 | integrated power | TI | ISOW7840DWE |
| Differential line drivers | 2 | 4 channels | TI | AM26LV31EIPWR |
| Differential line receivers | 4 | 4 channels | TI | AM26LV32EIPWR |
| Main connector | 1 | 80 positions | Samtec | ERF8-040-01-S-D-RA-L-TR |

record the voltage waveforms on an oscilloscope. The actual power stages cannot be seen in Fig. 6.7. The GaN half-bridge ICs, together with some local dc-link capacitors and some additional circuitry for the integrated bootstrap gate drivers, are grouped closely together on the bottom side of the PCB in an effort to minimize the inductance in the commutation loop. As shown in Fig. 6.8, this makes it possible to attach the semiconductor devices to a water cooler using an aluminum nitride (AlN) ceramic plate and thermal paste. The water cooler is a 3D-printed stainless-steel cooler by IQ evolution; while its power dissipation capability is way beyond the needs of this converter, it is still selected because of its small size.

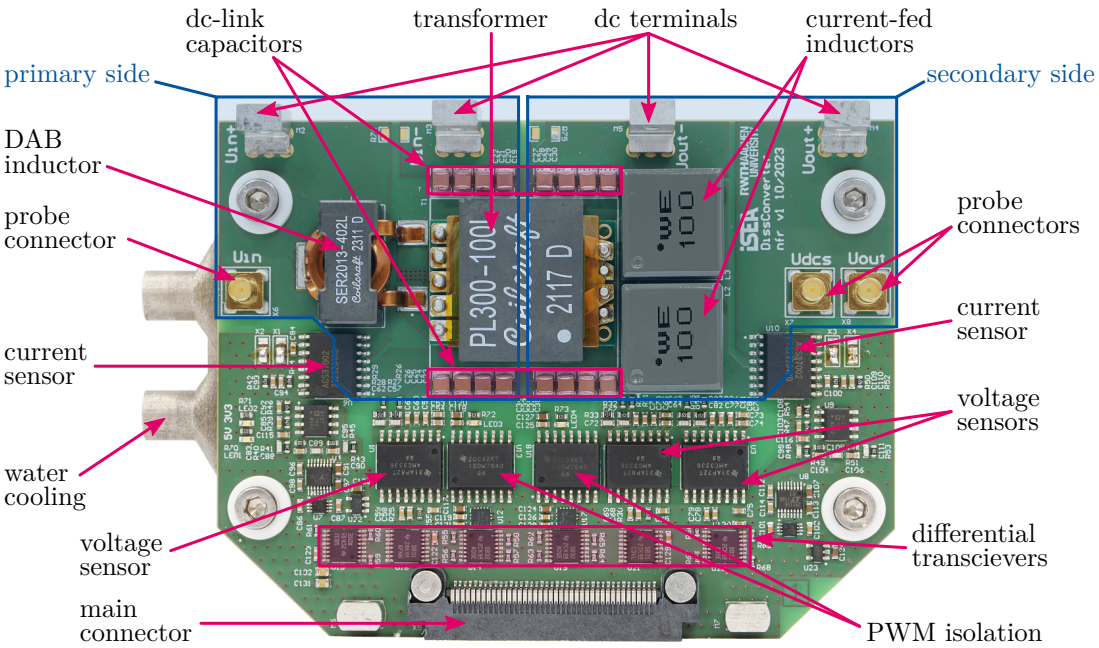
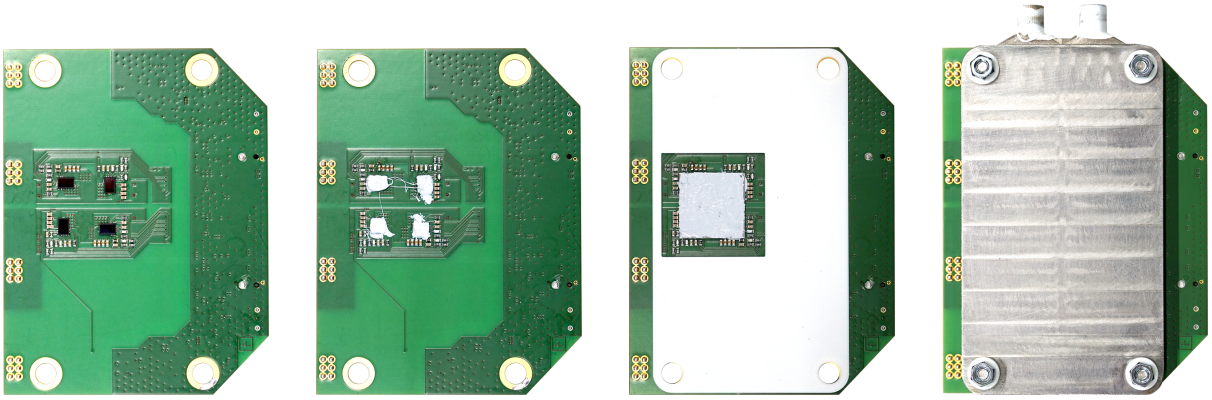



Figure 6.7: Photograph of the converter PCB [129]



(a) Bare PCB (b) Thermal paste on half bridges (c) AlN plate and spacer added (d) Heatsink mounted

Figure 6.8: Assembly of the cooling system on the bottom side of the converter PCB

A maximum of four PEBBs can be connected to a control PCB, which provides the embedded hardware to execute the control algorithms, receives the sensor signals coming from every PEBB and distributes the PWM signals to every PEBB in return. Figure 6.9 shows the control PCB. Four sockets for the converter PCBs, an MCU, an FPGA, and several peripherals can be seen. To handle the high number of digital signals and to enable a synchronous evaluation of all sensors, an FPGA is used; it allows a fast and simultaneous sensor evaluation, PWM generation, and even closed-loop control. The MCU, in turn, is best utilized for implementing control loops due to its superior computing hardware such as a floating-point unit (FPU). The two devices communicate via an external memory interface (EMIF), in which the address bus and the data bus of the MCU are forwarded to its physical pins and connected to the FPGA; any random access memory (RAM) that is implemented in the FPGA can thus be accessed by the MCU directly, merging the two devices virtually into a single device. Differential transceivers convert the PEBB signals back into single-ended signals. Moreover, some light-emitting diodes (LEDs) and buttons are provided, as well as joint test action group (JTAG) interfaces for debugging purposes. The whole board is powered via a 12 V input, which is converted into all other required, smaller voltages.

Finally, Fig. 6.10 shows the complete platform consisting of the control PCB and four attached converter PCBs. The last missing component is the means of realizing the various electrical interconnections such as $x\mathrm{P}y\mathrm{S}$ on the dc terminals of the PEBBs, which are now located at the top of the setup. For this purpose, copper busbars have been designed and custom made that can be screwed to the dc terminals, connecting the PEBBs in whatever required parallel or series interconnection. This makes the platform flexibly re-configurable for the validation of all interconnection variants from Chapter 5.

In summary, a platform consisting of four PEBBs and a control PCB has been designed. The PEBBs are 200 W single-phase, current-fed DABs rated 48 V on the primary side and 24 V on the secondary side, using GaN transistors switching at 250 kHz. These PEBBs

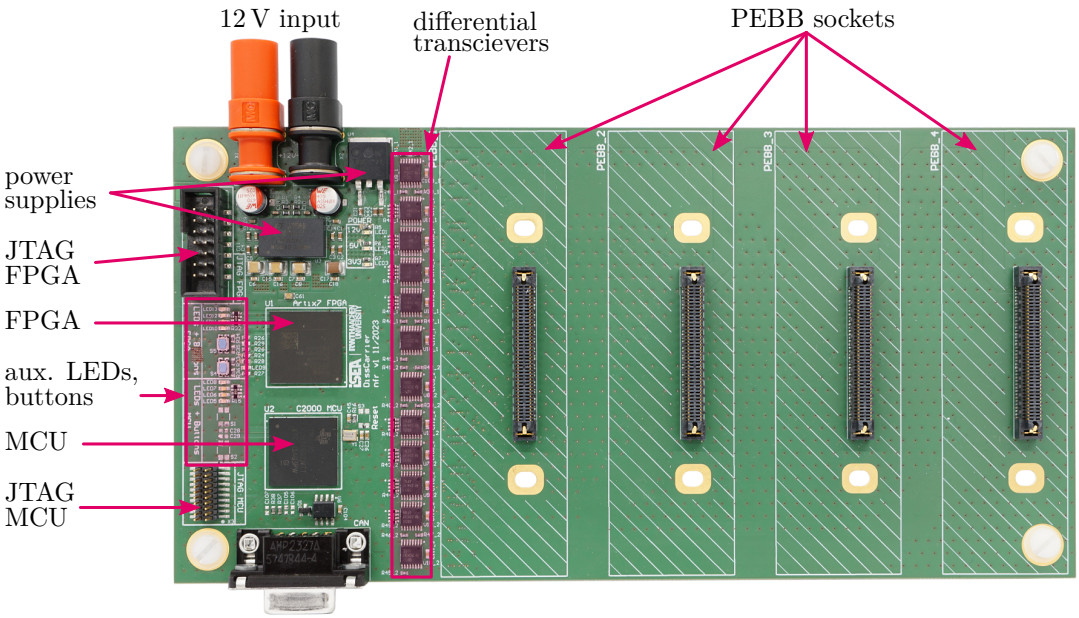



Figure 6.9: Photograph of the control PCB

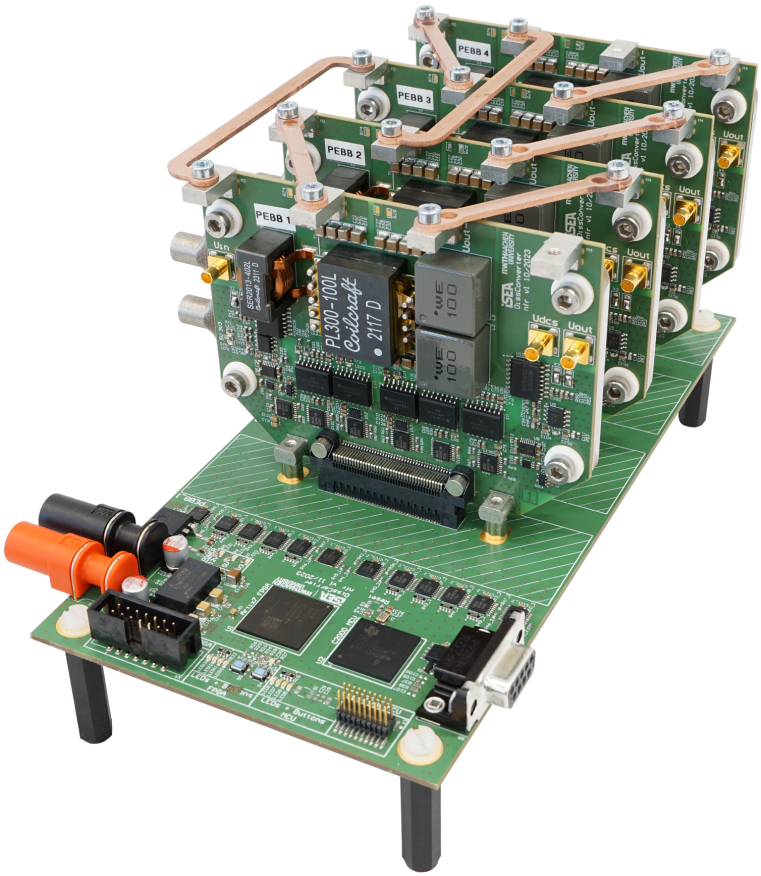



Figure 6.10: Photograph of the entire platform, four PEBBs are attached to the control PCB and copper busbars make the electrical interconnections

can be attached to a control PCB, which contains an MCU and an FPGA to execute the control laws. Any series or parallel interconnection of the PEBBs can be realized by connecting their dc terminals with custom-made copper busbars.

### 6.2.2 Software Design

In the software design, it is essential to distribute all control tasks, i.e., sensor evaluation, decoupling, control law execution, command calculation, actuation, and PWM generation, as efficiently as possible between the MCU and the FPGA. Moreover, this real-time, closed-loop, ever-repeating process needs to be embedded into some framework that can be operated by the user, allowing to start and stop an experiment and to provide control references. Additionally, safety features have to be implemented within the real-time portion of the software that automatically shut down the experiment if any measured sensor value exceeds a certain safety limit.

The MCU is a dual-core C2000 MCU by TI, which consists of two central processing units (CPUs) running at 200 MHz. It is programmed using the programming language C (standard C99) using the software Code Composer Studio, version 11. The FPGA is an Artix 7 FPGA by Xilinx/AMD; a main clock of 200 MHz is used in the design. It is programmed using the programming language VHDL (standard VHDL-1993) using the software Vivado, version 2020. Since the RAM of the MCU has a word size of 16 bit, this word size is used for all variables in the FPGA, too. The EMIF interface between the two chips has this data bus width as well. However, floating-point calculations in the MCU are done using standard 32 bit floating-point variables.

The key in control task distribution is to exploit the individual advantages of the MCU and the FPGA. Floating-point calculations are only possible on the MCU thanks to its FPU, which makes it well suited for calculating the closed control loops. However, it neither has enough PWM channels nor enough communication interfaces to acquire all sensor values. The FPGA, in turn, offers a great hardware flexibility to evaluate all sensors and generate all PWM patterns; however there is no support for floating-point calculations in the VHDL-1993 standard. Nonetheless, the FPGA contains digital signal processor (DSP) slices that are able to perform integer additions, subtractions, and multiplications in hardware in only a few clock cycles. This enables the FPGA to execute basic fixed-point calculations.

With these considerations in mind, the software structure shown in Fig. 6.11 is implemented. Inside the FPGA, modules for each of the four PEBBs are implemented, which contain the evaluation units for the sensors, a PWM generator, as well as every component that is needed to make one of the ports of the respective PEBB behave like an MC-type or MV-type port. Hence, from a control perspective, the FPGA manipulates all controlled current or voltage sources in the equivalent circuit of the controlled interconnected port. It also forwards all measured values to the MCU to enable the closed-loop

control of the state variables and external eigenvectors of the interconnected port. All hardware modules in the FPGA are synchronized with the PWM carrier; this allows to execute all control tasks in the FPGA at a sampling rate that is equal to the switching frequency of 250 kHz, corresponding to a sampling time of only 4 µs.

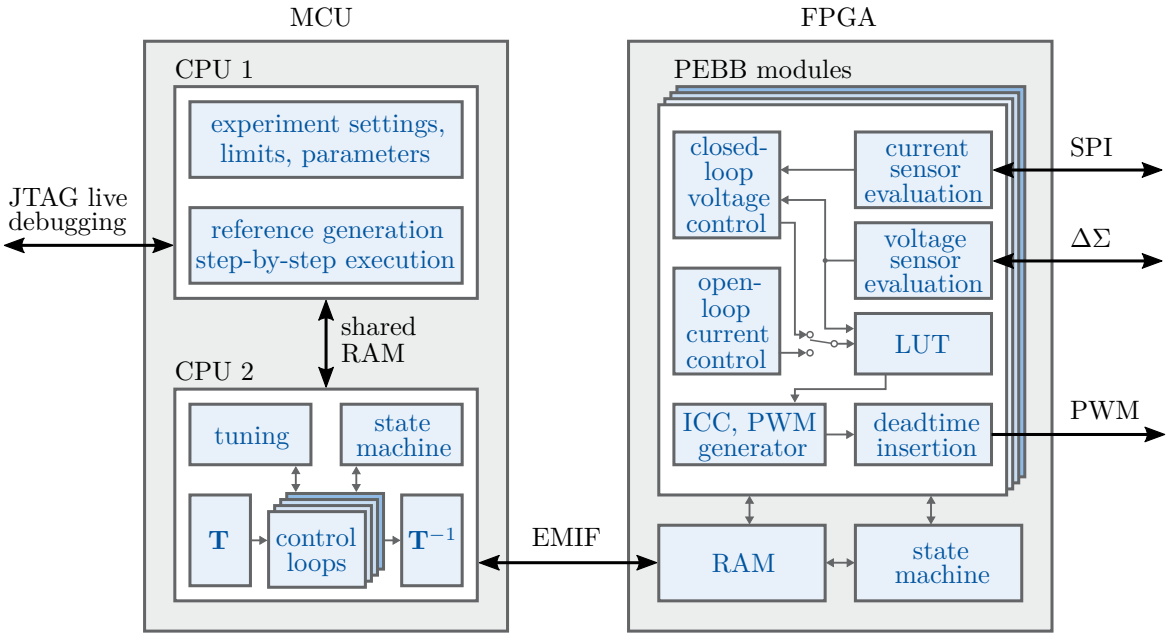



Figure 6.11: Overview of the software structure

From the perspective of the MCU, the FPGA provides access to all controlled voltage or current sources of one interconnected port. Hence, in the MCU, the sensor values have to be retrieved from the FPGA, extracting the state variables and multiplying the system outputs with the transformation matrix $\mathbf{T}$. After this, a control loop can be closed on every state variable to keep the interconnected port stable, the output of every control loop being an internal eigenvector command. Similarly, control loops can also be provided for the external eigenvectors, which can be manipulated freely in the interconnected port. This results in four control loops in total, with one portion of them acting on the state variables and the remaining loops acting on the external eigenvectors. In any case, the output of the control loops for both the state variables and the external eigenvectors are then multiplied by the inverse transformation matrix $\mathbf{T}^{-1}$ before commanding them to the FPGA. Due to the matrix calculations, the computational load of the four control loops, and the sequential execution of the C code on the CPU, the sampling rate cannot be kept as high as 250 kHz. Instead, the loop on the MCU is executed every ten switching periods, resulting in a sampling rate of 25 kHz and a sampling time of 40 µs.

The aforementioned control of the interconnected port is executed on CPU 2 of the MCU. In the experiments, it is run in real time without any debugging, using C code that is maximally optimized for speed. To ensure synchronous operation with the FPGA, two additional, dedicated signals are realized between the MCU and the FPGA. Every ten switching periods, the FPGA toggles one of these signals, triggering an interrupt in the

MCU, which initiates the execution of the control loops. When the MCU finishes writing the commanded values to the FPGA via the EMIF interface, it toggles the other signal to trigger the FPGA to fetch the new commands from its RAM. Along with the commands, several status bits are exchanged between the two ICs to indicate whether to activate the measurements or the PWM, as well as to indicate error states. Additionally, a request and a response bit are exchanged between the two ICs to detect whether one of them stopped working or responded too late, which triggers an error state in both devices.

Apart from the control loops, CPU 2 also implements a state machine of the whole experiment, which is sketched in Fig. 6.12. In the transition from the "uninitialized" to the "initialized" state, all software modules in the MCU are initialized and the RAM of the FPGA is filled with initial values. Transitioning into the "ready" state, the tuning of all control loops, the sensitivity and the safety limits of all sensors, as well as the frequency and deadtime of the PWM are set. In the "ready" state, all sensors are enabled and measurements are taken, but the control loops and the PWM are still disabled. Using the "start" and "stop" commands, the state machine can switch between the "ready" and "running" states, in the latter of which also the PWM and the control loops are activated. If any sensor value exceeds a predefined safety limit or if communication between the two ICs is lost, the state machine transitions into the "error" state, turning off the PWM immediately but keeping the measurements running.

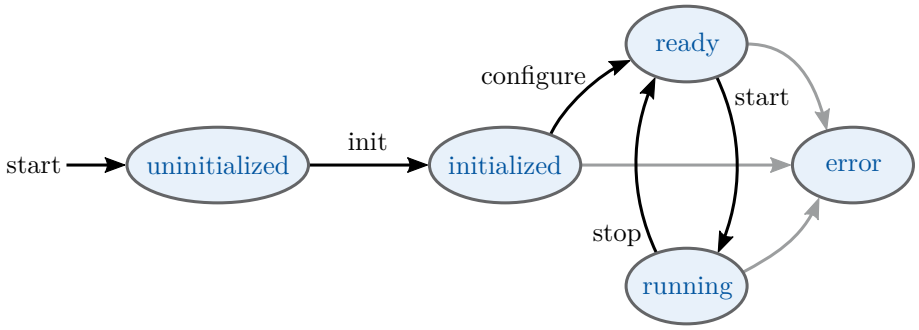



Figure 6.12: State machine running in CPU 2 of the MCU, controlling the experiment

CPU 1 of the MCU is not run in real time, but operated via a debugging interface by the user. It operates the state machine within CPU 2 via a shared RAM. For every experiment, a dedicated file with all the settings is compiled and initially forwarded to CPU 2 with the "configure" command. Apart from the commands of the state machine, also the control references are sent to CPU 2. This way, the user can execute the experiment procedure in a step-by-step fashion, e.g., starting an experiment, then providing reference step changes, then finally stopping the experiment, while CPU 2 runs in real time.

As already mentioned, the sensor evaluation is done in the FPGA. The ADCs measuring the currents of the PEBBs can be directly read using a serial peripheral interface (SPI). However, the obtained binary code only implicitly represents the current; not only does the reference voltage of the ADC have to be taken into account, but also floating-point variables are not used in the FPGA. Hence, a Q7.9 signed fixed-point representation is

selected according to [132], which denotes a 16 bit integer that is virtually split: The most significant 7 bit are considered to be before the comma, while the least significant 9 bit are considered to be behind the comma. This way, signed quantities can be represented with a resolution of $2^{-9} \approx 2 \cdot 10^{-3}$ in the range of $-64 \ldots (64 - 2^{-9})$. The range not only easily accommodates the expected voltages and currents in the PEBBs, but the resolution is also sufficient to precisely tune the controllers or scale the measured values. Both the measured currents and voltages are converted to the Q7.9 fixed-point integer format. To evaluate the voltage sensors, an averaging filter needs to be used on the $\Delta\Sigma$-modulated bitstream because the occurrence of binary zeros and one represents the measured voltage. For this purpose, a fourth-order cascaded integrator-comb (CIC) filter with a decimation ratio of 80 is used according to [133–135], which results in one voltage sample in every switching period and a sensor bandwidth of 79.8 kHz.

To ensure that the primary-side port of each PEBB behaves like an MC-type port, the open-loop current control for a single-phase DAB needs to be implemented as introduced in Fig. 3.4 in Section 3.3.1. While the instantaneous current control (ICC) according to (3.45) is easily realized, with the division by two just being a bit-shift operation, the inversion of the single phase shift (SPS) characteristic cannot be easily done on an FPGA because both a division by the measured voltage as well as taking a square root is required. For this purpose, a look-up table (LUT) is implemented as a RAM, individual for every PEBB. These LUTs contain the phase-shift angles for different voltages to obtain one specific primary-side current, which of course requires a calibration. The phase-shift values are saved for a grid of 64 voltage points ranging from 0 V…63 V and 32 current points ranging from −16 A…15 A; taking powers of two is convenient because then the LUT address can be computed from fixed-point integer values using only shift operations. The phase-shift angle of any requested primary-side current that lies in between the grid points defined by the LUT is calculated using the neighboring entries and a bilinear interpolation, which is implemented on the FPGA in fixed-point arithmetic. If the calibration of the LUT is done with sufficiently high precision using experimental data, the MC-type port of the PEBB can be made to behave like a very precise controlled current source.

To make the secondary-side port of each PEBB behave like an MV-type port, however, a closed-loop control of the secondary-side dc-link voltage is required. For this purpose, a generic PI controller using Q7.9 fixed-point integers is implemented in the FPGA. Figure 6.13 shows the corresponding block diagram, in which every shown parameter, i.e., the proportional and integral feedback gains $K_\mathrm{p}$ and $K_\mathrm{i}$, the zero of the first-order reference filter $\delta_\mathrm{z}$, and the lower and upper command limits $u_\mathrm{m}^\mathrm{min}$ and $u_\mathrm{m}^\mathrm{max}$, can be programmed from the FPGA RAM. If one of the limits of the commanded variable $u_\mathrm{m}^\triangledown$ is violated, the integrator is stopped[ii] as an anti-windup measure. The same structure is used to implement generic PI controllers in the MCU for controlling the state variables and external eigenvectors in the C language using floating-point operations.

[ii] More precisely, its absolute value is prevented from increasing. A decrease in absolute value is permitted.

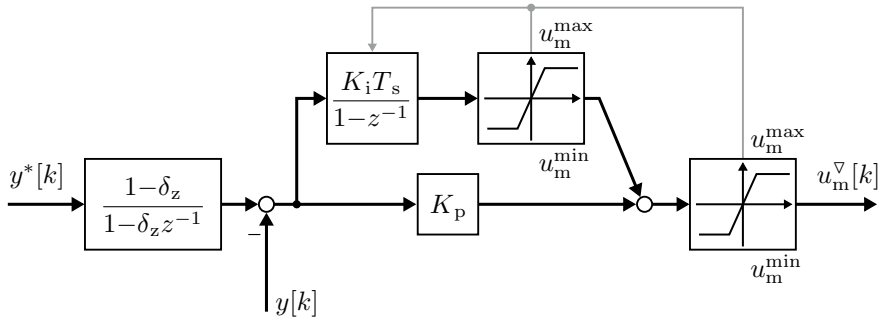



Figure 6.13: Generic PI controller as implemented both on the MCU and on the FPGA

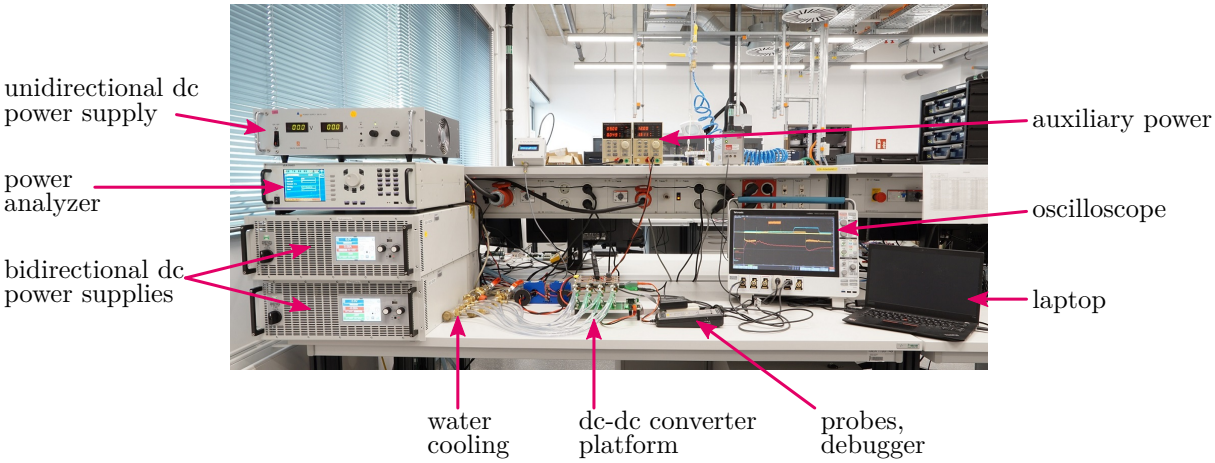
In summary, the FPGA controls every PEBB such that its primary-side port behaves like an MC-type port, implementing the open-loop current control for single-phase DABs from Section 3.3.1, or such that its secondary-side port behaves like an MV-type port, implementing a closed-loop voltage control using fixed-point integers. From the perspective of the MCU, this makes the voltage or current sources in an interconnected port directly manipulable. Hence, the MCU implements the decoupling of the sensor variables by multiplication with the transformation matrix $\mathbf{T}$, the control loops for the interconnected port in decoupled coordinates, and the subsequent conversion back to individual port commands by multiplication with $\mathbf{T}^{-1}$.

## 6.2.3 Commissioning

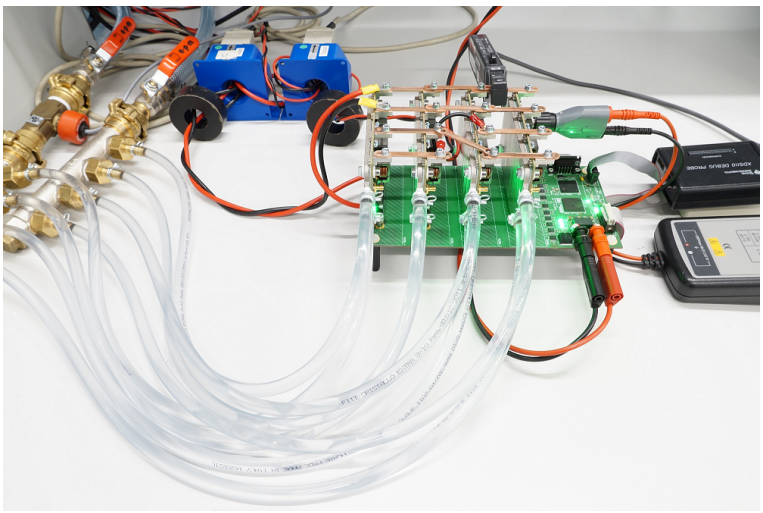
After the implementation of the hardware and the software, the converter PCBs are commissioned and evaluated in terms of efficiency. To enable the validation of the decoupled control strategies from Chapter 5, the MC-type port behavior for the primary sides and the MV-type port behavior for the secondary sides must be established and verified in a second step. These steps are described by the following sections.

### 6.2.3.1 Experimental Setup and Efficiency Characterization

In Fig. 6.14, photographs of the experimental setup are shown. A dc power supply and a load are required to operate the modular dc-dc converter platform. For this purpose, two bidirectional dc sources of type EA-PSB 11500-60 from Elektro-Automatik are used. Apart from their ability to act as power source and load, they can operate in constant-voltage as well as constant-current mode, which makes it possible to replicate ideal sources for interconnections of both MC-type and MV-type ports. In addition to the two bidirectional power supplies, another unidirectional power supply of type SM 70-45 D by Delta Elektronika is used optionally; in comparison to the bidirectional power supplies, its output voltage has significantly lower ripple and noise components.




(a) Overview



(b) Zoom on laboratory table

Figure 6.14: Laboratory setup of the low-power dc-dc converter platform

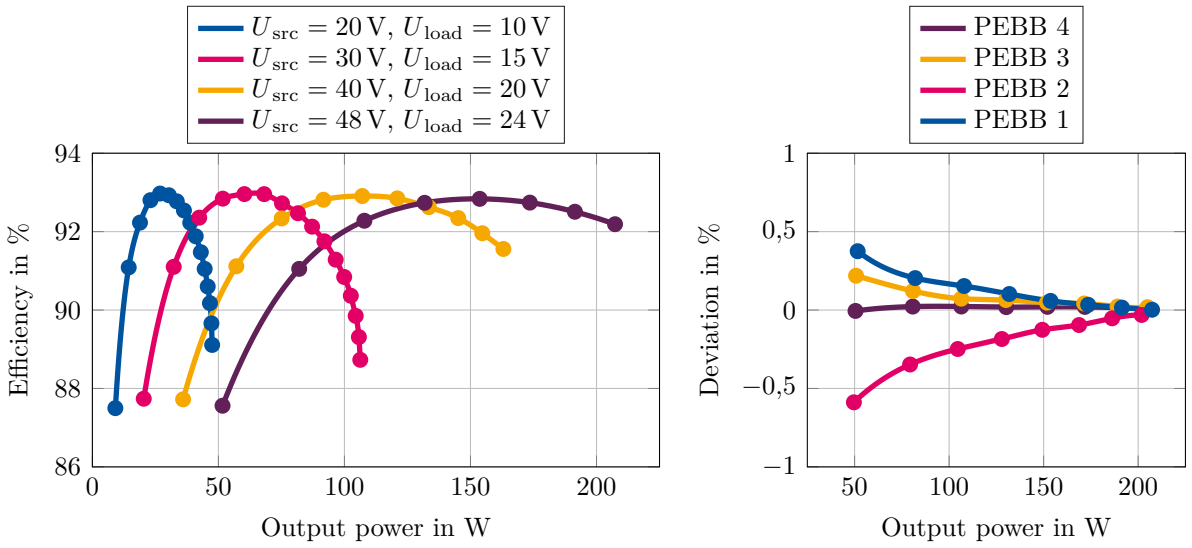
The modular dc-dc converter system is attached to the power supplies, and a power analyzer of type LMG500 by ZES Zimmer is used to measure the efficiency. The water coolers of the four PEBBs are attached to an in-house cooling system, which is regulated to 12 °C and provides a constant flow rate of 10 $^{\mathrm{L}}/_{\mathrm{min}}$ for the entire setup. The dc-dc converter platform is powered through a standard 12 V laboratory power supply.

While the control software utilizes the sensors on the converter PCBs, all relevant electrical quantities are also measured using voltage and current probes and an oscilloscope. The used oscilloscope is a six-channel, 1 GHz, 12 bit oscilloscope of type MSO56 from Tektronix. Only active differential voltage probes are used, listed in Table 6.2. The current probes are listed in Table 6.2 as well; the listed Rogowski coil is only used to measure the transformer current during the commissioning of the PEBBs. While the voltage probes are attached to the coaxial connectors provided on the converter PCBs, the current probes are directly clamped on the copper busbars interconnecting the individual PEBBs.

Table 6.2: Specifications of the used voltage and current probes

| Manufacturer | Probe | Type | Range | Sensitivity | Bandwidth |
|---|---|---|---|---|---|
| Testec | TT-SI 9101<br>TT-SI-9110 | voltage | ±70 V<br>±140 V | 100 mV/V<br>10 mV/V | 100 MHz |
| Keysight | N2783A | current | ±30 A | 100 mV/A | 100 MHz |
| Tektronix | TCP0030A | | ±30 A | 100 mV/A | 120 MHz |
| PEM | CWT 1B Ultramini | | ±300 A | 20 mV/A | 30 MHz |

At first, every PEBB is operated with a constant phase-shift angle to determine the efficiency using the power analyzer and also to characterize the power transfer characteristic of the implemented SPS modulation. For this experiment, the power supplies provide constant dc voltages for the source voltage $U_{\text{src}}$ on the primary side and for the load voltage $U_{\text{load}}$ on the secondary side. Figure 6.15a shows the efficiency characterization of PEBB 1 for different values of the source and load voltages, while Fig. 6.15b shows the difference of the efficiencies of all PEBBs from their average efficiency at 48 V source voltage and 24 V load voltage. The observed efficiency profiles have a typical shape, with a peak efficiency of approximately 93 %. Moreover, differences of less than 1 % among the efficiencies of all PEBBs are observed, which confirms that the design of the converter PCB together with the tolerances of the selected components produces satisfactorily consistent parameters.




(a) Efficiency of PEBB 1 for different source and load voltages

(b) Efficiency deviation of all PEBBs for $U_{\text{src}} = 48\,\text{V}$ and $U_{\text{load}} = 24\,\text{V}$

Figure 6.15: Efficiency characterization of the converter PCBs

Figure 6.16 shows a plot of the operating waveforms of PEBB 1 at 48 V source voltage, 24 V load voltage, and a phase-shift angle of 45°, which corresponds to the full-load operating point from Fig. 6.15. The maximum observed absolute value of the drain-source voltage waveforms is 58 V, which indicates a satisfactorily low-inductive design of the GaN

commutation cells. To verify the safe long-term operation in the full-load operating point, a thermal image of PEBB 1 has been taken after 10 min of operation at maximum output power; it is given in Fig. 6.17. The temperature of the series inductor of the single-phase DAB is in the range 100 °C…120 °C, which on the one hand is still within the specifications, but on the other hand implies significant losses. Hence, the series inductor is identified as the main loss contributor, preventing higher values of the efficiency. This is because the used inductors are not optimized for a 250 kHz, purely ac current waveform. However, a robust design using only off-the-shelf components to enable a quick replacement is prioritized over a thoroughly optimized converter.

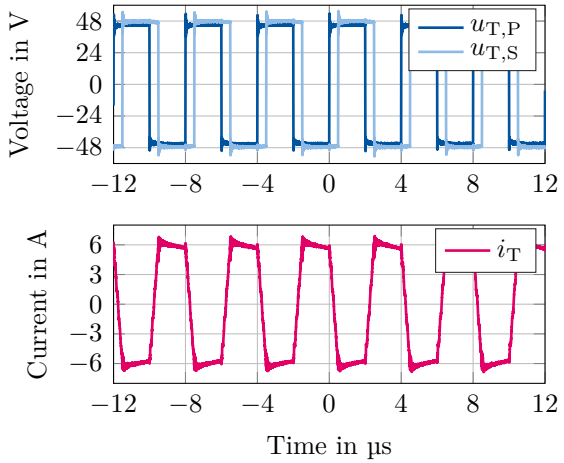



Figure 6.16: Waveforms of PEBB 1 at $U_{src} = 48\,V$, $U_{load} = 24\,V$ and $\varphi = 45°$

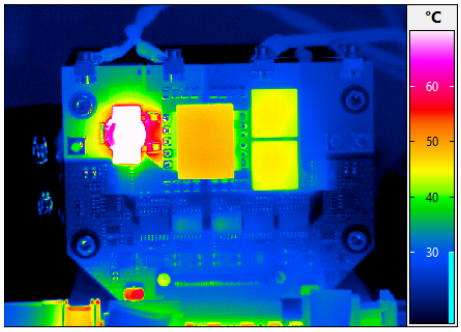



Figure 6.17: Thermal image of PEBB 1 running at $U_{src} = 48\,V$, $U_{load} = 24\,V$, and $\varphi = 45°$

In summary, the PEBBs have been successfully commissioned, running at constant dc voltages and constant phase-shift angles. Bidirectional dc power supplies are used on both interconnected converter ports, and voltage and current probes are used to record all relevant electrical quantities with an oscilloscope. The PEBBs reach a peak efficiency of about 93 %, and efficiency differences between the individual PEBBs are minor.

#### 6.2.3.2 MC-Type Port Realization and Verification

To realize the decoupled control of MC-type port interconnections from Section 5.3, the primary-side ports of all PEBBs need to be operated as controllable current sources. As introduced in Section 3.3.1, this can be done by inverting the power transfer characteristic of the SPS modulation strategy, calculating the required phase-shift angles from any current command, or in case of the FPGA, taking the required phase-shift angles to achieve a certain current at a given secondary-side voltage from the LUT. Hence, the strategy is to use the measurements from the previous section, which have been carried out at precisely known phase-shift angles, to fill the LUTs.

The SPS characteristic from (3.44) is idealized and does not account for the converter losses, device forward voltages, or deadtimes. Hence, an empirical extension of this equation is used, using additional, empirical offset variables $\varphi_0$ and $Y_0$ highlighted in blue:

$$\frac{\bar{i}_\mathrm{P}}{U_\mathrm{S}} = \frac{1}{2\pi f_\mathrm{sw} L_\sigma} \cdot (\varphi - \varphi_0) \cdot \left(1 - \frac{|\varphi - \varphi_0|}{\pi}\right) + Y_0. \tag{6.1}$$

If a set of estimated parameters $\hat{L}_\sigma$, $\hat{\varphi}_0$, and $\hat{Y}_0$ can be found, the LUTs in the FPGA can be filled with the following inverted equation for the estimated phase-shift angle $\hat{\varphi}$ for a commanded primary-side current $\bar{i}_\mathrm{P}^{\nabla}$ and a measured secondary-side voltage $U_\mathrm{S}$[iii]:

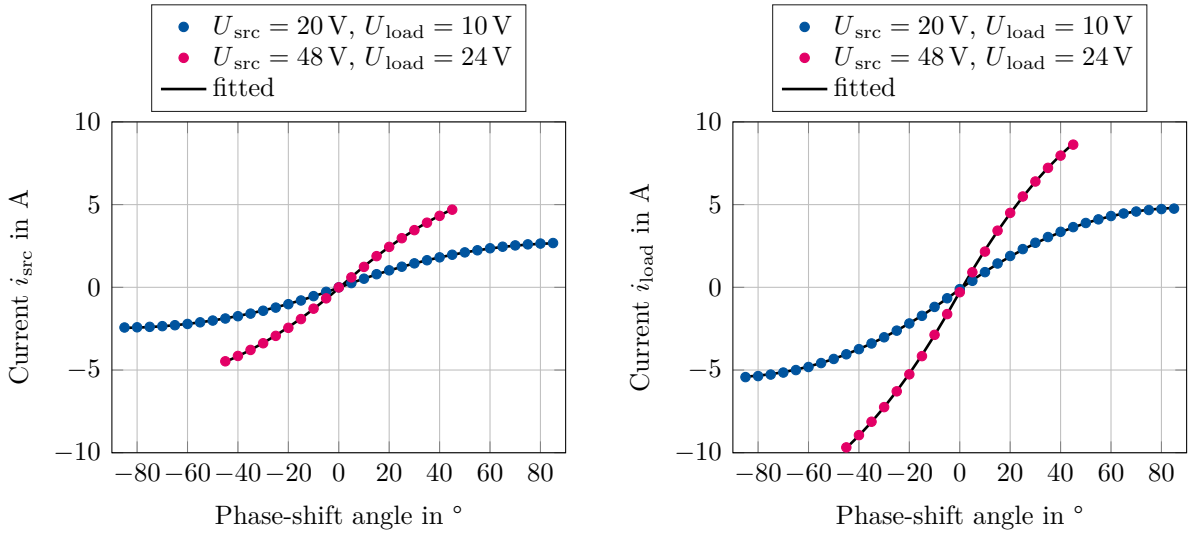
$$\hat{\varphi} = \hat{\varphi}_0 + \mathrm{sgn}\left(\frac{\bar{i}_\mathrm{P}^{\nabla}}{U_\mathrm{S}} - \hat{Y}_0\right) \cdot \left(\frac{\pi}{2} - \sqrt{\left(\frac{\pi}{2}\right)^2 - 2\pi^2 f_\mathrm{sw} \hat{L}_\sigma \cdot \left|\frac{\bar{i}_\mathrm{P}^{\nabla}}{U_\mathrm{S}} - \hat{Y}_0\right|}\right). \tag{6.2}$$

Calibration measurements must be made to estimate $\hat{L}_\sigma$, $\hat{\varphi}_0$, and $\hat{Y}_0$. Instead of the commanded primary-side current $\bar{i}_\mathrm{P}^{\nabla}$ and the measured secondary-side voltage $U_\mathrm{S}$, the same principle can be used with the commanded secondary-side current $\bar{i}_\mathrm{S}^{\nabla}$ and the measured primary-side voltage $U_\mathrm{src}$, which implements the open-loop current control for the secondary-side current. This results in a different set of parameters $\hat{L}_\sigma$, $\hat{\varphi}_0$, and $\hat{Y}_0$, which again have to be found using calibration measurements. The open-loop control of the secondary-side current is needed because the closed-loop control of the secondary-side dc-link voltage to realize an MV-type port manipulates the secondary-side current.

The measurements from the previous section were carried out at constant phase-shift angles and the power analyzer was used to record both the source and the load current, therefore these measured values are perfectly suitable as calibration measurements to estimate the parameters $\hat{L}_\sigma$, $\hat{\varphi}_0$, and $\hat{Y}_0$. The measured source and load currents of PEBB 1 are plotted as a function of the applied phase-shift angle in Fig. 6.18. Using this data, the parameter estimation is done for every PEBB using a nonlinear least-squares algorithm in MATLAB, separately for the primary-side and the secondary-side currents. The results are shown in Table 6.3. The modified SPS characteristic (6.1) using these fitted parameters is also plotted in Fig. 6.18, showing an accurate agreement with the measured values. Since every parameter set has been estimated using all calibration measurements that have been carried out at different primary-side and secondary-side dc voltages, it has to be noted that the modified SPS characteristic (6.1) accurately predicts the power transfer for arbitrary voltage levels only using three parameters.

It has to be checked whether the estimated parameters yield a precise current-source behavior even for pairs of dc voltages that have not been used during calibration. Hence, an experiment on PEBB 1 is carried out, filling the corresponding LUT with the estimated phase-shift angles obtained from the estimated parameters for PEBB 1. Different values of the source and load current are commanded for different sets of source and load voltages,

[iii] It has to be noted that $U_\mathrm{S}' = U_\mathrm{S}$ because the transformer has a turns ratio of 1.




(a) Primary-side source current

(b) Secondary-side load current

Figure 6.18: Source and load current of PEBB 1 as a function of the phase-shift angle, measurement and fitted SPS characteristic

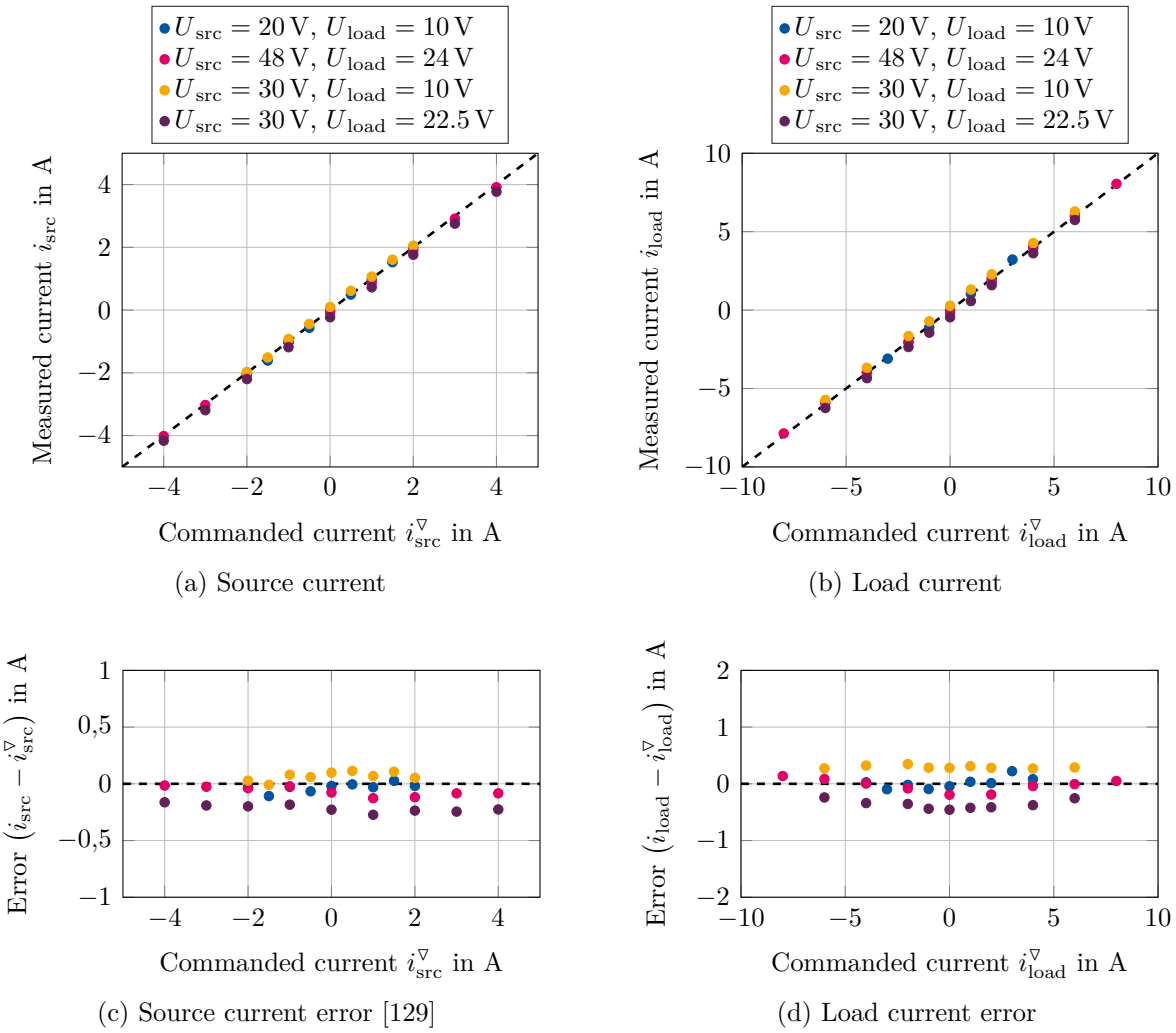
Table 6.3: Estimated SPS parameters to compute an estimated phase-shift angle for any current command

| PEBB | Primary-side current | | | Secondary-side current | | |
|---|---|---|---|---|---|---|
| | $\hat{L}_\sigma$ | $\hat{\varphi}_0$ | $\hat{Y}_0$ | $\hat{L}_\sigma$ | $\hat{\varphi}_0$ | $\hat{Y}_0$ |
| PEBB 1 | 3.898 µH | 2.425° | 5.677 mA/V | 3.910 µH | −1.770° | −7.835 mA/V |
| PEBB 2 | 4.000 µH | 2.384° | 5.419 mA/V | 4.007 µH | −1.720° | −7.786 mA/V |
| PEBB 3 | 3.941 µH | 2.463° | 5.740 mA/V | 3.954 µH | −1.736° | −7.696 mA/V |
| PEBB 4 | 3.927 µH | 2.571° | 5.829 mA/V | 3.941 µH | −1.613° | −7.636 mA/V |

including combinations that were not used before, particularly asymmetric dc voltages. This experiment is carried out for both the primary-side and the secondary-side current, using the individual parameters for these two scenarios.

Figure 6.19 shows the measurement results. In Fig. 6.19a, the measured source current is plotted as a function of the commanded current, and Fig. 6.19c shows the deviation of the measured source current from the commanded value. It can be seen that even for voltage ratios that have not been used in the parameter estimation, the measured current very precisely matches the commanded value. However, the deviation becomes larger for asymmetric dc voltages, with the maximum absolute error being 273 mA. The same is done for the measured load current in Fig. 6.19b and Fig. 6.19d. It has to be noted that the average secondary-side rectified current is commanded, but only the load current can be measured, which is twice as high due to the characteristics of the current-fed port; hence, all axes are scaled by a factor of two compared to Fig. 6.19a and Fig. 6.19c. Also for the load current, the resulting maximum absolute error of 457 mA is satisfactorily

small. All in all, using the estimated phase-shift angles in the LUTs in the FPGA allows for the PEBBs to be operated as fairly precise controlled current sources, which is the essential prerequisite for the decoupled control of an MC-type interconnected port.




(a) Source current

(b) Load current

(c) Source current error [129]

(d) Load current error

Figure 6.19: Measured source and load current of PEBB 1 as a function of the commanded current, at different symmetric and asymmetric dc voltages

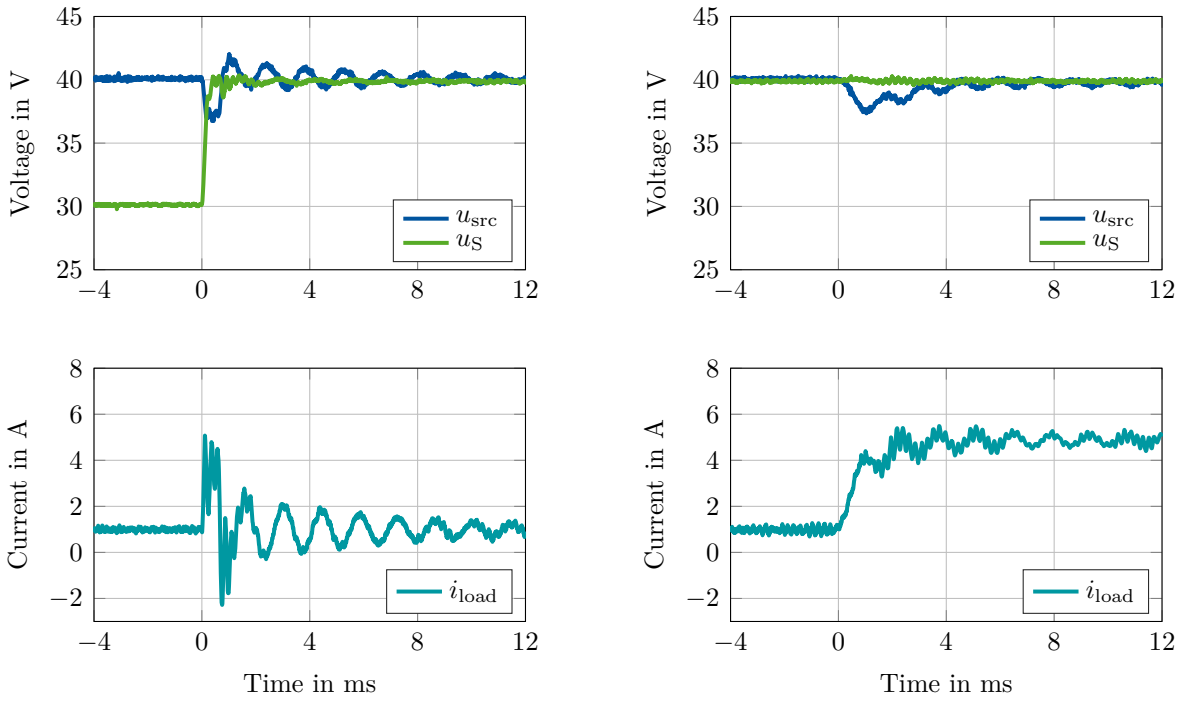
In summary, an open-loop control of the primary-side or secondary-side current of each PEBB has been implemented and validated. The parameters of the SPS modulation strategy have been fitted to the the measurements from the previous section. Using the fitted parameters, the LUTs of the PEBB are filled with estimated phase-shift angles for every possible pair of commanded current and dc voltage. In another experiment, it could be shown that when using these estimated phase-shift angles, the obtained currents are in good agreement with the commanded values, even for asymmetric dc voltages. This makes it possible to realize an MC-type port on the primary side of each PEBB, or to implement a closed-loop control of the secondary-side dc-link voltage of each PEBB, turning the secondary-side port into an MV-type port, which is discussed in the following.

#### 6.2.3.3 MV-Type Port Realization and Verification

After realizing a precise MC-type port behavior on the primary side, the MV-type port behavior has to be developed for the secondary side. Therefore, a closed-loop control of the secondary-side dc-link voltage is required. As shown in Fig. 6.11, this control loop is implemented on the FPGA, executing once every switching period, i.e., every 4 µs.

The closed-loop voltage control is developed in the exact same way as in Section 4.3.2. Considering the bandwidth of 79.8 kHz of the voltage sensors on the converter PCBs, the control bandwidths should stay at least one decade below that limit. Hence, the selected proportional and integral feedback bandwidths are $f_{\mathrm{b,p}} = 5\,\mathrm{kHz}$ and $f_{\mathrm{b,i}} = 1\,\mathrm{kHz}$, respectively. For the calculation of the controller gains, the value of the secondary-side dc-link capacitance has to be used. It has to be considered that its capacitance depends on the dc-link voltage in a nonlinear fashion because a class-2 ceramic is used. However, a constant capacitance of 24 µF is used in the calculations, which corresponds to the capacitance at 43 V. A first-order reference filter is implemented according to (4.10) to compensate the zero of the PI controller with $\tau_{\mathrm{PI,u}} = 159\,\mu\mathrm{s}$. In the discrete time domain with $T_{\mathrm{s}} = 4\,\mu\mathrm{s}$, this corresponds to a zero of $\delta_{\mathrm{z}} = 0.975$, see Fig. 6.13. The current that is commanded by this voltage controller is the average rectified secondary-side current; the open-loop current control developed in the previous section can be used to obtain the resulting estimated phase-shift angle using the LUT in the FPGA.

PEBB 1 is used to validate the performance of this closed-loop control. On the primary side, the dc power supply is set to 40 V, while on the secondary side, the voltage is determined by the closed-loop voltage control. Hence, the dc load on the secondary side is programmed to sink a constant load current of 1 A. The voltage waveforms are recorded using TT-SI 9101 probes, while the load current is measured using the N2783A probe. Figure 6.20a shows a scenario in which the reference secondary-side voltage is abruptly changed from 30 V to 40 V. It can be seen that the new reference value is reached within 500 µs. In the waveform of the load current, and even the waveform of the primary-side dc-link voltage, this transient increase of 5 W in transferred power causes oscillations due to the parasitic inductance of the wiring. This is however not a characteristic of the closed-loop voltage control, which keeps the secondary-side dc-link voltage tightly regulated, but rather the poor current control performance of the load. Apart from the command-tracking property, also the disturbance rejection property of the closed-loop voltage control is of interest. Figure 6.20b shows a measurement in which the secondary-side dc-link voltage reference is kept constant at 40 V, while the current sinked by the secondary-side bidirectional dc power supply is abruptly changed from 1 A to 5 A, corresponding to an increase of 80 W in transferred power. While this step change is not perfect due to the dynamics of the bidirectional power supply, the secondary-side dc-link voltage is tightly kept at 40 V without any significant undershoot. The primary-side dc-link voltage controlled by the primary-side dc power supply, however, experiences a significant undershoot. Overall, the closed-loop control of the secondary-side dc-link voltage shows excellent command-tracking and disturbance-rejection properties.




(a) 30 V to 40 V reference step

(b) 1 A to 5 A disturbance step

Figure 6.20: Performance of the closed-loop secondary-side dc-link voltage control

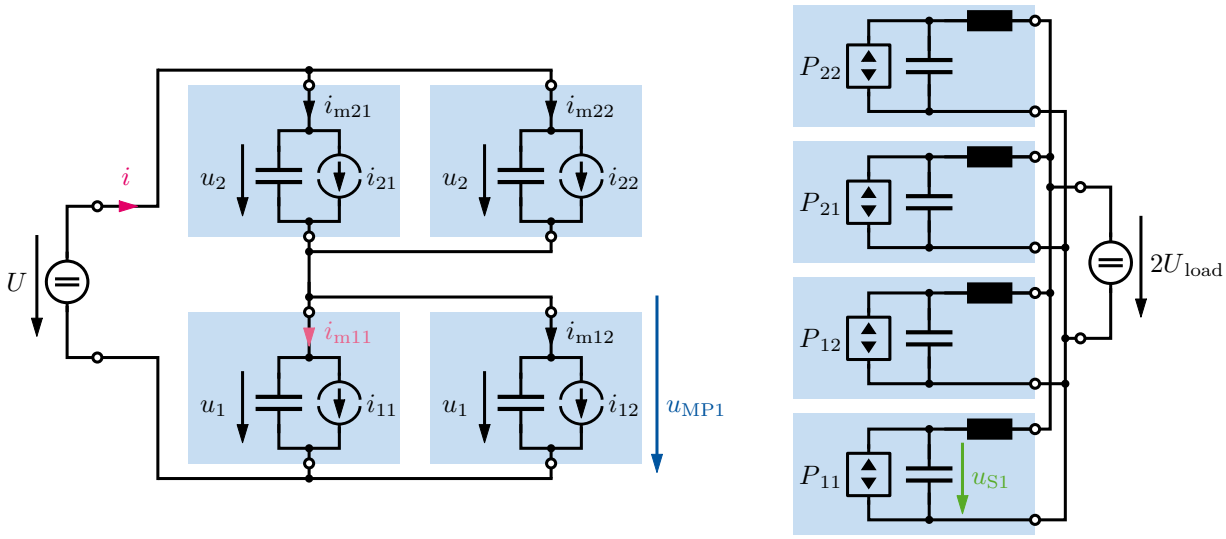
In summary, a closed-loop voltage control of the secondary-side dc-link voltage has been implemented in the FPGA using the procedure described in Section 4.3.2. The controller commands an average rectified secondary-side current, which is actuated by the open-loop current control that has been developed in the previous section. The performance of the voltage controller has been validated by experiment, showing excellent command-tracking and disturbance-rejection properties with a voltage settling time of about 500 µs.

### 6.2.4 Validation of Decoupled Control

After the preparatory steps of converter and control PCB design, commissioning, software development, and implementation of the MC-type and MV-type port behavior, the proposed decoupling and control strategies from Chapter 5 are validated. One interconnection variant of MC-type individual ports and one interconnection variant of MV-type individual ports are discussed in this section, while the measurements on the remaining six interconnection variants are moved to Appendix D for the sake of conciseness.

First, the decoupled control of the $x\mathrm{P}y\mathrm{S}$ interconnection of MC-type ports with ideal voltage source is addressed. As shown in Section 6.2.3.2, the primary sides of the used current-fed DAB converters can be programmed to behave like MC-type ports. With four

PEBBs available, both $x$ and $y$ are chosen to be two, resulting in a 2P2S interconnection of MC-type ports with ideal voltage source on the primary side. In turn, the secondary sides are all connected in parallel to an ideal voltage source. The primary and secondary sides of the converter PCBs are interconnected accordingly using the copper busbars. The decoupling technique from Section 5.3.2 shall be applied to this interconnection, which has a single state variable, namely the midpoint voltage $u_{\mathrm{MP1}}$. Figure 6.21 shows the equivalent circuit of the overall modular dc-dc converter system. The stability considerations from Section 5.4.3 demand that the power should be transferred from the primary to the secondary side because the secondary-side parallel connection is asymptotically stable only if it is the power outlet, as proven in Appendix C.




(a) Controlled primary side (b) Uncontrolled secondary side

Figure 6.21: Equivalent circuit of the dc-dc converter platform with the decoupled control applied to the primary-side 2P2S interconnection of MC-type converter ports with ideal voltage source

With the asymptotic stability of the uncontrolled secondary-side interconnection guaranteed, the decoupling and the control of the primary-side interconnection now comes into focus. From Section 5.3.2, the following transformation matrix $\mathbf{T}$ is obtained for $x = 2$ and $y = 2$,

$$\mathbf{T} = \begin{pmatrix} \vec{v}_{\mathrm{I}}^{\,\mathrm{T}} \\ \vec{v}_{\mathrm{E1}}^{\,\mathrm{T}} \\ \vec{v}_{\mathrm{E2}}^{\,\mathrm{T}} \\ \vec{v}_{\mathrm{E3}}^{\,\mathrm{T}} \end{pmatrix} = \begin{pmatrix} -\frac{1}{4} & -\frac{1}{4} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \end{pmatrix}, \tag{6.3}$$

listing the eigenvectors of this interconnection in its rows. The first row is the internal eigenvector that represents a current $i_{\mathrm{MP1}}$ that directly manipulates the state, namely the midpoint voltage $u_{\mathrm{MP1}}$. Hence, it must be used in a voltage control loop, keeping this midpoint voltage stable. The remaining three rows are external eigenvectors, which can be controlled freely. The second row in (6.3) represents the terminal current $i$ of the

interconnected port as derived in (5.36), which represents the overall transferred power. Finally, the last two rows in (6.3) are two DM current patterns denoted $i_{\mathrm{DM1}}$ and $i_{\mathrm{DM2}}$, i.e., the current differences within the two sets of parallel-connected ports, which can be used to manipulate the power sharing between the parallel-connected converter ports.

While the transformation matrix is used to compute the eigenvectors from the individual manipulated currents of each PEBB,

$$\begin{pmatrix} i_{\mathrm{MP1}} \\ i \\ i_{\mathrm{DM1}} \\ i_{\mathrm{DM2}} \end{pmatrix} = \begin{pmatrix} -\frac{1}{4} & -\frac{1}{4} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \end{pmatrix} \cdot \begin{pmatrix} i_{11} \\ i_{12} \\ i_{21} \\ i_{22} \end{pmatrix}, \tag{6.4}$$

its inverse is also needed to compute current commands for each PEBB from the eigenvectors commanded by the decoupled control loops:

$$\begin{pmatrix} i_{11}^{\triangledown} \\ i_{12}^{\triangledown} \\ i_{21}^{\triangledown} \\ i_{22}^{\triangledown} \end{pmatrix} = \mathbf{T}^{-1} \cdot \begin{pmatrix} i_{\mathrm{MP1}}^{\triangledown} \\ i^{\triangledown} \\ i_{\mathrm{DM1}}^{\triangledown} \\ i_{\mathrm{DM2}}^{\triangledown} \end{pmatrix} = \begin{pmatrix} -1 & \frac{1}{2} & \frac{1}{2} & 0 \\ -1 & \frac{1}{2} & -\frac{1}{2} & 0 \\ 1 & \frac{1}{2} & 0 & \frac{1}{2} \\ 1 & \frac{1}{2} & 0 & -\frac{1}{2} \end{pmatrix} \cdot \begin{pmatrix} i_{\mathrm{MP1}}^{\triangledown} \\ i^{\triangledown} \\ i_{\mathrm{DM1}}^{\triangledown} \\ i_{\mathrm{DM2}}^{\triangledown} \end{pmatrix}. \tag{6.5}$$

Also $\mathbf{T}^{-1}$ can be explained physically by looking at its columns. The first column is associated with the internal eigenvector: If the midpoint voltage controller aims to increase the midpoint voltage $u_{\mathrm{MP1}}$, it decreases the currents $i_{11}$ and $i_{12}$ as suggested by the first two entries in the first column, but increases the currents $i_{21}$ and $i_{22}$. This only manipulates the midpoint voltage, but neither the terminal current nor the current sharing between the parallel-connected ports. The second column of $\mathbf{T}^{-1}$ suggests that in order to increase the overall terminal current $i$, all four individual port currents have to be increased by equal amounts; however, since two ports are connected in parallel, each PEBB should only apply half of the commanded value $i^{\triangledown}$. Finally, the last two columns obviously generate circulating DM currents. By design of this decoupling, neither eigenvector interferes with any other.

With these considerations regarding the decoupling of this very specific primary-side interconnection variant in mind, the control can be developed. A mixed-domain block diagram of the physical plant in decoupled coordinates and the MCU and FPGA control loops is given in Fig. 6.22. In the FPGA, the open-loop current control of the current-fed DABs is activated as demonstrated in Section 6.2.3.2 to make the primary sides of all PEBBs behave like MC-type ports. Thus, the FPGA receives current commands in cross-coupled coordinates, individual for each PEBB, and the actual decoupled control is done in the MCU. As already discussed, only a single state variable must be actively controlled, hence a closed-loop voltage controller is implemented on the midpoint voltage $u_{\mathrm{MP1}}$; it commands the only internal eigenvector that directly manipulates this midpoint voltage. The design of the voltage controller is by no means different from the one developed in Section 4.3.2, using a simple PI regulator with the feedback bandwidths $f_{\mathrm{b,p}} = 2\,\mathrm{kHz}$

and $f_{\mathrm{b,i}} = 500\,\mathrm{Hz}$, as well as a command filter that compensates for the zero of the PI regulator. With the internal eigenvector used to implement the mandatory control of the midpoint voltage, the control of the three external eigenvectors is still missing. Since Section 6.2.3.2 demonstrated that the MC-type port realization produces very accurate currents, a purely open-loop control shall be utilized for the external eigenvectors for demonstration purposes, feeding the reference values directly into the inverse transformation matrix $\mathbf{T}^{-1}$. If a higher precision is needed, it is of course also possible to close the control loop.

Proceeding to the experiment, constant voltages of 60 V and 15 V are applied to the primary-side and secondary-side interconnected ports, respectively. With the primary-side series connection and the parallel-connected current-fed secondary sides cutting the voltage in half, these dc voltages match the transformer turns ratios of 1 for all PEBBs. In the primary-side interconnected port, the midpoint voltage $u_{\mathrm{MP1}}$ and the terminal current $i$ are measured as well as the current into PEBB 1 to assess the DM current $i_{\mathrm{DM1}}$. In the secondary-side interconnected port, the secondary-side dc-link voltage $u_{\mathrm{S1}}$ of PEBB 1 is measured to verify the stability of the uncontrolled secondary-side port.

Figure 6.23 shows the recorded waveforms of the experiment. It is started with a midpoint voltage reference set to 30 V, which is half of the primary-side dc voltage, and a terminal current reference set to 2 A, resulting in 120 W of transferred power for $t < 0\,\mathrm{ms}$. It can be seen that the state variable, i.e., the midpoint voltage $u_{\mathrm{MP1}}$, is regulated to the desired value of 30 V, and the same holds for the open-loop controlled external eigenvectors because the reference DM currents, which are set to zero, cause the current of PEBB 1 to be exactly half of the overall current.

Between $0\,\mathrm{ms} \leq t < 40\,\mathrm{ms}$, a pulse from 2 A to 4 A and back is applied to the terminal current reference $i^*$. This corresponds to an equivalent pulse from 120 W to 240 W and back in the overall transferred power. As a result, the secondary-side dc-link voltage of PEBB 1 experiences an overshoot and undershoot of 8.7 V peak amplitude on the rising and falling edges of the primary-side terminal current $i$. It however quickly converges back to an equilibrium, which confirms the asymptotic stability of the uncontrolled secondary side, which is assessed in Appendix C. On the primary side, it can be observed that the terminal current $i$ dynamically follows the reference values. Due to the parasitic inductance of the wiring between the interconnected port and the primary-side power supply, overshoots and short-lived oscillations are observable in the transients of the terminal current $i$, which settle within 200 µs. Also, the terminal current $i$ initially only reaches 3.75 A instead of the reference value of 4 A. This is due to the pure open-loop control, which is more accurate for equal primary-side and secondary-side dc-link voltages. As the secondary-side dc-link voltage however experiences a transient, the estimated phase-shift angles in the LUT of the FPGA are less accurate. Implementing a closed-loop control could compensate for this behavior; this experiment however is intended to demonstrate the accuracy of the open-loop control. Furthermore, it can be observed that the measured current of PEBB 1 follows half of the terminal current, which means that the DM current $i_{\mathrm{DM1}}$ is not affected and remains zero. Likewise, the midpoint voltage is barely affected

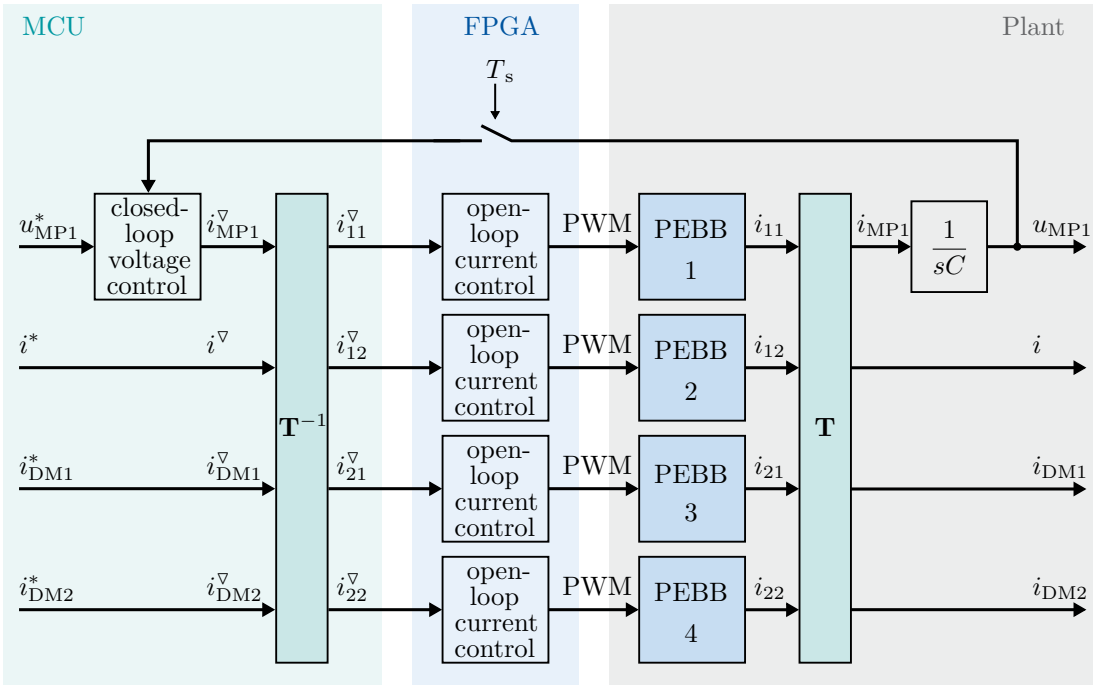



Figure 6.22: Block diagram of the decoupled control of the MC-type, 2P2S-interconnected primary-side port with ideal voltage source [129]

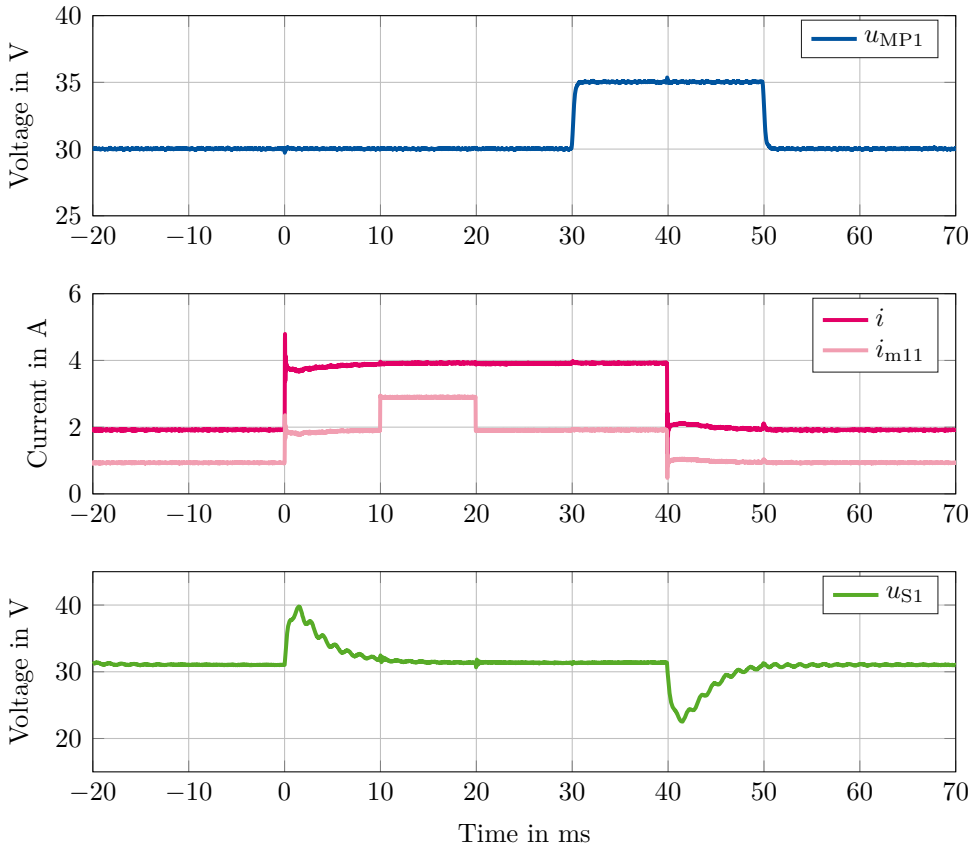



Figure 6.23: Measurement of the decoupled control of the MC-type, 2P2S-interconnected primary-side port with ideal voltage source [129]

by the large step of the terminal current; only deviations of less than 0.4 V are observed. Since the current manipulation of the PEBBs is not perfect as seen in Section 6.2.3.2, there remains a negligible cross coupling that still affects the midpoint voltage and can be interpreted as a disturbance input.

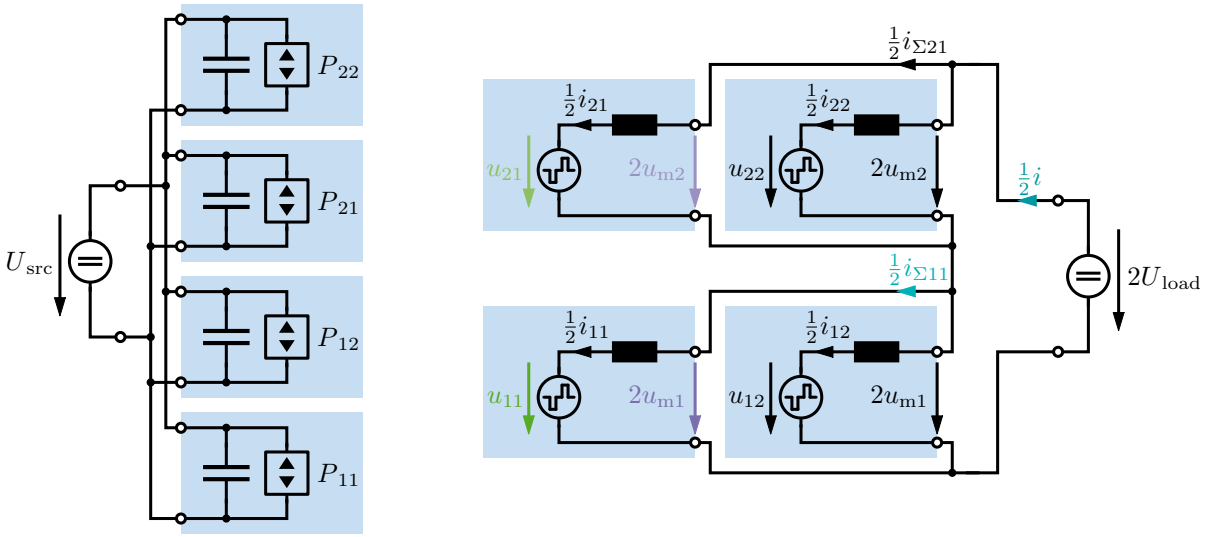
Between $10\,\text{ms} \leq t < 20\,\text{ms}$, a pulse from 0 A to 2 A and back is applied to both DM current references $i^*_{\text{DM1}}$ and $i^*_{\text{DM2}}$. This makes the current of PEBB 1 increase by 1 A; together with the current of PEBB 2 decreasing by 1 A, this corresponds to a current difference of 2 A, as required. Neither the overall terminal current nor the midpoint voltage are affected by this transient. Also the secondary-side dc-link voltage remains unaffected because the DM current does not contribute to any power transfer.

Finally, between $30\,\text{ms} \leq t < 50\,\text{ms}$, a pulse from 30 V to 35 V and back is applied to the midpoint voltage reference $u^*_{\text{MP1}}$, testing the command-tracking properties of the closed-loop control of the state variable. The desired voltage references are reached quickly, precisely, and without any overshoots. The internal eigenvector commanded by the voltage controller only manipulates the midpoint voltage and does barely interfere with the terminal current or the DM currents; at 50 ms, a deviation of only 150 mA can be observed in the terminal current.

Overall, it is confirmed by this experiment that the control of the primary-side interconnected port using its internal and external eigenvectors shows negligible cross couplings, allowing an independent control of the state variables and external eigenvectors.

In the following, a second scenario using an MV-type interconnected port shall be examined. Since Section 6.2.3.3 demonstrated that the secondary sides of the PEBBs can be programmed to act like controlled voltage sources using an interior closed-loop voltage control on the FPGA, the MV-type port behavior is established for the secondary-side interconnected port. The interconnection variant under investigation is the $y\text{P}x\text{S}$ interconnection without ideal current source; with four PEBBs, the choice of $x = 2$ and $y = 2$ is made like in the previous experiment, resulting in a 2P2S interconnection. All primary-side individual ports are connected in parallel, and the resulting primary-side interconnected port is left uncontrolled. If attached to an ideal voltage source, this uncontrolled primary-side interconnected port should be stable regardless of the direction of power flow, as discussed in Section 5.4.3. The equivalent circuit of the resulting dc-dc converter system is shown in Fig. 6.24.

With the secondary-side individual converter ports, there is one important caveat to be considered, which is related to the current-fed ports. As discussed in Section 3.3.3, the current-fed port contains two half bridges that switch at 50 % duty cycle. This results in the current to be doubled and the voltage to be cut in half. For this purpose, the equivalent circuit in Fig. 3.9 has been developed that looks at the single-phase current-fed DAB from the perspective of the secondary-side dc link. For this purpose, the load voltages have to be doubled and the currents have to be cut in half, which is consequently executed in the equivalent circuit in Fig. 6.24b. The shown inductances are all equal to the equivalent




(a) Uncontrolled primary side

(b) Controlled secondary side

Figure 6.24: Equivalent circuit of the dc-dc converter platform with the decoupled control applied to the secondary-side 2P2S interconnection of MV-type converter ports without ideal current source

inductance defined by (3.49). Hence, despite current-fed inductors of 10 µH are used according to Table 6.1, the control has to be designed for an equivalent inductance of $L_{\mathrm{b,eq}} = 20\,\mu\mathrm{H}$.

The decoupling of the secondary-side interconnected port now comes into focus. As discussed in Section 5.3.5 and Appendix B.2, the 2P2S interconnection of MV-type ports shares the same state-space model with the 2S2P interconnection of MC-type ports, hence the decoupling strategy from Section 5.3.3 can be used, which has been developed for MC-type ports. However, in all definitions, voltages have to be exchanged for currents and vice versa, which is worked out in detail in Appendix B.2. As suggested by (B.7), the state variables of the interconnected MV-type port are the overall terminal current $i$ as well as the accumulated currents in each parallel-connected converter block. Since in this case only two individual ports are connected in parallel, there is only one accumulated current for each block, which equals the inductor current of one of the individual ports. The two resulting accumulated currents are denoted $i_{\Sigma 11}$ and $i_{\Sigma 21}$, which are also shown in Fig. 6.24. This cumbersome definition is only used because it yields the same decoupling matrices as in the reference MC scenario; using other state variables would require to re-derive the entire state-space model. The three state variables need to be actively controlled in the given interconnection of four PEBBs by closed-loop current controllers, which are commanding the associated internal eigenvectors. Hence, only a single external eigenvector should remain to be freely controlled.

The transformation matrix for this interconnection variant is given by

$$\mathbf{T} = \begin{pmatrix} \vec{v}_{\mathrm{I1}}^{\mathrm{T}} \\ \vec{v}_{\mathrm{I2}}^{\mathrm{T}} \\ \vec{v}_{\mathrm{I3}}^{\mathrm{T}} \\ \vec{v}_{\mathrm{E}}^{\mathrm{T}} \end{pmatrix} = \begin{pmatrix} -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{3}{4} & \frac{1}{4} & -\frac{1}{4} & -\frac{1}{4} \\ -\frac{1}{4} & -\frac{1}{4} & -\frac{3}{4} & \frac{1}{4} \\ \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \end{pmatrix}, \tag{6.6}$$

listing the eigenvectors of this interconnection in its rows. The first row is the internal eigenvector that directly manipulates the first state, namely the terminal current $i$ of the interconnected converter. The second and third row in (6.6) list those internal eigenvectors that manipulate the accumulated currents $i_{\Sigma 11}$ and $i_{\Sigma 21}$, respectively. Finally, the last row in (6.6) is an external eigenvector, i.e., a voltage pattern that does not manipulate the system states and can be freely controlled. Obviously, it is the difference of the average port voltages in each parallel-connected converter block, i.e., the voltage difference between the lower two and the upper two PEBBs. This voltage does not manipulate any of the states; for example, the overall terminal current $i$ is not affected as only the voltage sum, not its difference, would cause it to change. In the following, this external eigenvector, the voltage difference, is called DM voltage $u_{\mathrm{DM}}$.

The inverse of the transformation matrix $\mathbf{T}$ as defined by (6.6) is given by

$$\mathbf{T}^{-1} = \begin{pmatrix} 0 & -1 & 0 & \frac{1}{2} \\ -1 & 1 & 0 & \frac{1}{2} \\ 0 & 0 & -1 & -\frac{1}{2} \\ -1 & 0 & 1 & -\frac{1}{2} \end{pmatrix}. \tag{6.7}$$

The columns of $\mathbf{T}^{-1}$ make physical sense in the context of the control of the interconnected port. To increase the terminal current $i$ but not any other control variable, the voltages $u_{12}$ and $u_{22}$ should be reduced. This voltage reduction lets the terminal current $i$ increase, but since the voltages $u_{11}$ and $u_{21}$ are not changed, the accumulated currents $i_{\Sigma 11}$ and $i_{\Sigma 21}$, i.e., the other state variables, remain unaffected. The second and third column in (6.7) describe the voltage patterns that only manipulate the accumulated currents: They can be manipulated by introducing a voltage difference between parallel-connected individual ports, which only affects the current distribution between them, but not the overall terminal current $i$. Finally, the last column is just the transpose of the last row in (6.6), confirming that the DM voltage $u_{\mathrm{DM}}$ is the difference between the voltage of the lower two and the upper two PEBBs, which is just how this DM voltage should be generated.

In the next step, the control is developed. A mixed-domain block diagram of the physical plant in decoupled coordinates and the MCU and FPGA control loops is given in Fig. 6.25. In the FPGA, the closed-loop control of the secondary-side dc-link voltage of the current-fed DABs is activated as demonstrated in Section 6.2.3.3 to make the secondary sides of all PEBBs behave like MV-type ports. The same proportional and integral

feedback bandwidths as in Section 6.2.3.3 are used to realize this MV-type port behavior, namely 5 kHz and 1 kHz, respectively. Thus, the FPGA receives voltage commands in cross-coupled coordinates, individual for each PEBB, and the actual decoupled control is done in the MCU. Since three state variables are present in the secondary-side interconnected port, three current control loops need to be established that manipulate the internal eigenvectors. It has already been discussed in Section 5.3.5 that a voltage source feeding a series inductance is mathematically equivalent to a current source feeding a parallel-connected capacitor; hence, the closed-loop current control can be designed in the exact same way as the closed-loop voltage control from Section 4.3.2. However, in the design equations (4.9), the equivalent inductance instead of the capacitance has to be used:

$$\begin{aligned} K_{\mathrm{p,i}} &= 2\pi f_{\mathrm{b,p}} L_{\mathrm{b,eq}}, \\ K_{\mathrm{i,i}} &= 2\pi f_{\mathrm{b,i}} K_{\mathrm{p,i}}. \end{aligned} \tag{6.8}$$

The feedback bandwidths are chosen $f_{\mathrm{b,p}} = 1\,\mathrm{kHz}$ and $f_{\mathrm{b,i}} = 250\,\mathrm{Hz}$, and a command filter is implemented, which compensates for the zero of the PI regulator. These bandwidths are lower compared to those in the previous section to avoid interaction with the inner closed-loop voltage control of the MV-type ports, which has a limited bandwidth. With the three internal eigenvectors used to implement the mandatory control of the interconnected port currents, the control of the remaining external eigenvector is still missing. Since the inner voltage control loops in the FPGA already guarantee a highly precise manipulation of the port voltages in the secondary-side interconnected port, it is not necessary to implement an additional closed-loop control; instead, it is perfectly sufficient to directly use the DM voltage reference to compute the individual voltage commands using the inverse transformation matrix $\mathbf{T}^{-1}$.

Proceeding to the experiment, constant voltages of 30 V are applied to both the primary-side and secondary-side interconnected ports. With the primary-side parallel connection and the current-fed secondary sides cutting the voltage in half, these dc voltages match the transformer turns ratios of 1 for all PEBBs. In the secondary-side interconnected port, the terminal current $i$ and the current into PEBB 1, which is equivalent to the state variable $i_{\Sigma 11}$, are measured. Also the dc-link voltages $u_{11}$ and $u_{21}$, which act as manipulated inputs to the system, are recorded. The experiment is repeated once, with the voltage probes instead measuring the terminal voltages $u_{\mathrm{m11}}$ and $u_{\mathrm{m21}}$.

Figure 6.26 shows the recorded waveforms of the experiment. It is started with a terminal current reference $i^*$ set to 4 A, both accumulated current references $i^*_{\Sigma 11}$ and $i^*_{\Sigma 21}$ set to 2 A, and a DM voltage reference $u^*_{\mathrm{DM}}$ of zero, which guarantees power sharing between all PEBBs. This results in 120 W of transferred power for $t < 0\,\mathrm{ms}$. It can be seen from Fig. 6.26 that those reference values are precisely tracked for $t < 0\,\mathrm{ms}$.

At $t = 0\,\mathrm{ms}$, the terminal current reference is increased to 6 A, which corresponds to a transferred power of 180 W, while the accumulated current references are not changed, which results in an unequal power sharing between the PEBBs. Then, at $t = 80\,\mathrm{ms}$,

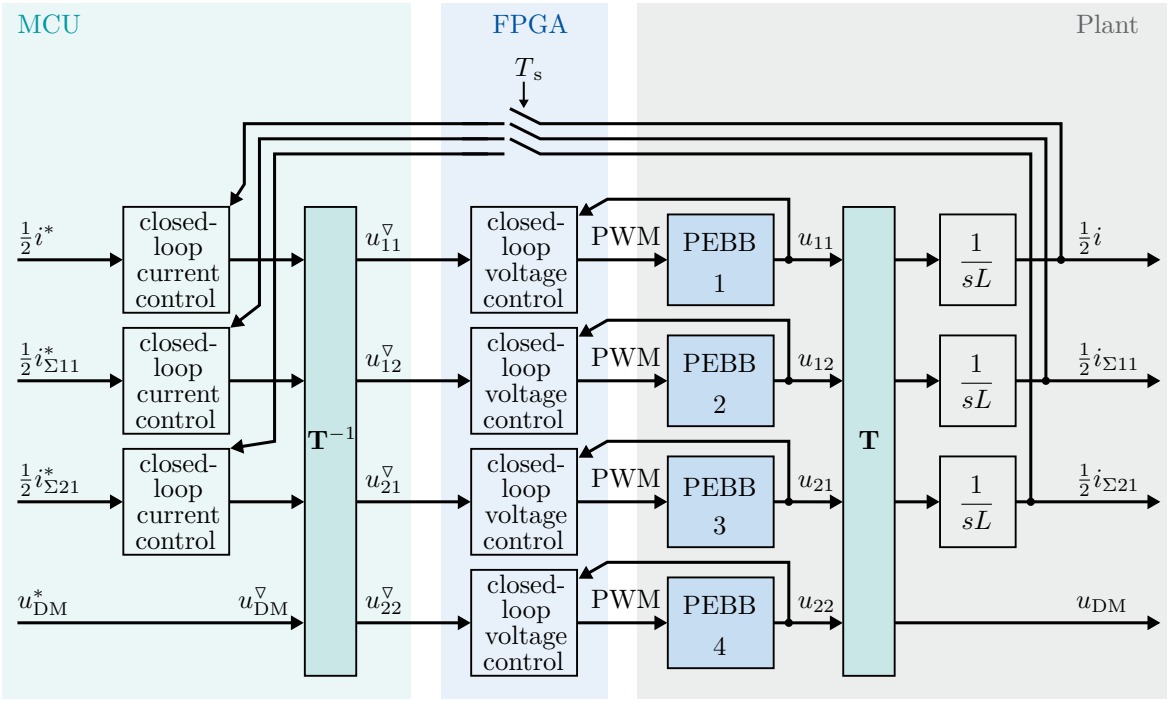



Figure 6.25: Block diagram of the decoupled control of the MV-type, 2P2S-interconnected secondary-side port without ideal current source

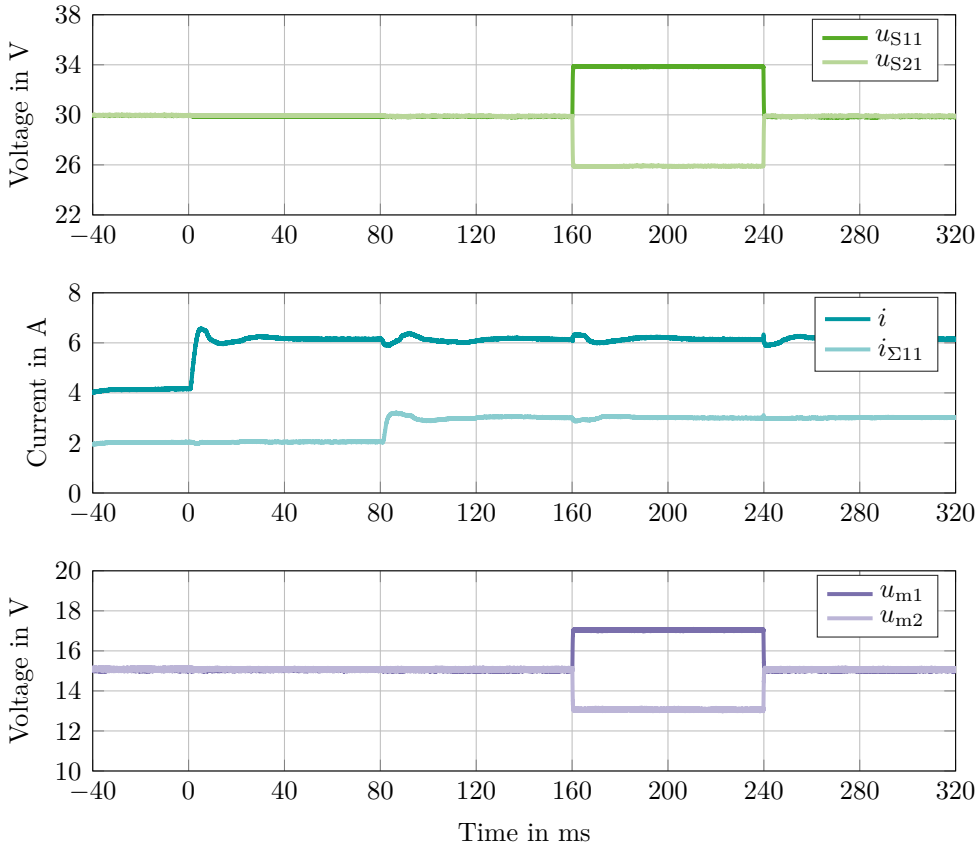



Figure 6.26: Measurement of the decoupled control of the MV-type, 2P2S-interconnected secondary-side port without ideal current source

the accumulated current references are both increased to 3 A, re-establishing equal power sharing. It can be seen from Fig. 6.26 that these current references are tracked satisfactorily, however with repeated deviations whenever another transient occurs in the system; the peak deviation is an overshoot of 560 mA in the terminal current shortly after 0 ms. The reason for this behavior originates from the limited bandwidth of the closed-loop current control: With a proportional feedback bandwidth of 1 kHz and an equivalent inductance of 20 µH, the value of the proportional gain $K_{\mathrm{p,i}}$ is only $126\,^{\mathrm{mV}}/_{\mathrm{A}}$ according to (6.8). This means that for a current deviation of 100 mA, the controller initially reacts with only 12.6 mV of compensating voltage. Hence, the small current deviations can be attributed to the limited resolution of the interior closed-loop control of the secondary-side dc-link voltage, or to a limited control bandwidth, or to the small value of the equivalent inductance, but not to the decoupling concept.

Between $160\,\mathrm{ms} \leq t < 240\,\mathrm{ms}$, a pulse from 0 V to 8 V and back is applied to the DM voltage references. This pulse is tracked very precisely by the interior closed-loop control in the FPGA, and aside from small deviations, it does not interfere with the port currents, which confirms the decoupling. In the measured terminal voltages, half of this amplitude is visible due to the characteristics of the current-fed port.

In summary, this concludes the validation of the decoupling approach from Chapter 5. It could be verified that the eigenvector-based modeling and control works in a real-world application, which has been verified using one interconnection of MC-type converter ports and one interconnection of MV-type converter ports. Observing the step responses of several state variables and external eigenvectors, the interactions between those variables could be almost completely eliminated. Measurements on the remaining six interconnection variants are also provided, but moved to Appendix D for the sake of conciseness.

### 6.2.5 Validation of Stability

In the previous section, it has already been shown that the uncontrolled parallel connection of the secondary sides of all PEBBs on a common voltage source is stable whenever the secondary sides act as the power output. This specific statement about the stability of an uncontrolled interconnected converter port is proven in Appendix C, and it follows the rule of thumb formulated in Section 5.4.3, which states that an uncontrolled interconnected converter port should always act as the power output to be stable. What is missing is the opposite scenario, proving that an uncontrolled interconnected converter port acting as the power input is unstable. Hence, two additional experiments are conducted to assess the stability of a modular dc-dc converter system in more detail.

For this purpose, only two PEBBs are used, which are connected in series on the primary side, forming a 1P2S interconnection. On the secondary side, they are connected in parallel, forming a 2P1S interconnection. The primary-side series connection requires the midpoint voltage to be stabilized, and the secondary-side parallel connection requires

both inductor currents to be balanced. Since three state variables are present, but only two PEBBs, i.e., only two manipulated system inputs, this interconnection variant is overdetermined. Hence, there is no choice but to rely on the stability of those state variables that cannot be actively controlled.

In the following, the decoupling and control techniques proposed in this dissertation are first applied to the primary-side interconnected port, and then to the secondary-side interconnected port. This should stabilize all state variables on the controlled interconnected port, while the stability of the state variables in the uncontrolled interconnected port are expected to depend on the direction of the power flow.

Figure 6.27 shows the equivalent circuit of the dc-dc converter system when the decoupled control is applied to the primary side, making the primary sides of the two PEBBs behave like MC-type ports. In this case, the midpoint voltage $u_{\mathrm{MP}}$ is the only state variable on the primary side, which can be controlled via a closed-loop voltage controller acting on the internal eigenvector; the tuning is the same as in the previous section. The terminal current $i$ is the external eigenvector and can be controlled in an open-loop manner. In the following experiment, the controlled interconnected port is operated as the power input first, controlling a positive terminal current. As already seen in the previous section, this should result in a stable operation because the uncontrolled secondary side acts as the power output. Then, the terminal current $i$ shall be reversed so that it becomes negative, making the uncontrolled secondary side suddenly act as the power input, which should yield instability.

Bidirectional power supplies are used on both the primary and the secondary side, with the primary-side dc voltage set to 40 V and the secondary-side voltage set to 10 V; the comparably low voltages leave enough safety margin for observing potential instabilities. The closed-loop controlled primary-side midpoint voltage $u_{\mathrm{MP}}$, both secondary-side dc-link voltages $u_{\mathrm{S1}}$ and $u_{\mathrm{S2}}$, and the open-loop controlled primary-side terminal current $i$ are measured.

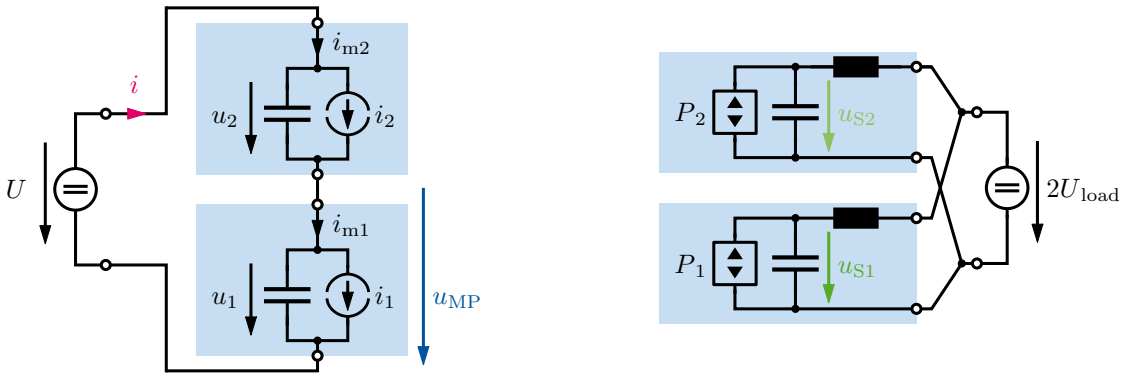
The results of this experiment are given in Fig. 6.28. For $t < 0\,\mathrm{ms}$, the terminal current reference $i^*$ is set to 1 A, making the secondary side act as the power output. The midpoint voltage reference $u^*_{\mathrm{MP}}$ is set to 20 V, which is half of the primary-side dc voltage and guarantees power sharing. At $t = 0\,\mathrm{ms}$, the terminal current reference $i^*$ is suddenly changed to $-1$ A, while the midpoint voltage reference $u^*_{\mathrm{MP}}$ stays at 20 V. As soon as the current crosses zero, it can be observed that the secondary side, which now acts as the uncontrolled power input, becomes unstable. The dc-link voltages $u_{\mathrm{S1}}$ and $u_{\mathrm{S2}}$ experience an undershoot because of the sudden power reversal; however, the secondary sides now act as constant-power load (CPL) elements. Hence, in the presence of a voltage undershoot, these CPL elements even draw a higher current, making the secondary-side dc-link voltages collapse even further and rendering them unable to return to an equilibrium, which can be seen in the measurements. This confirms the stability assessment from Appendix C.

The analogous experiment is performed when applying the decoupled control to the secondary-side interconnected port instead of the primary-side interconnected port. Figure 6.29 shows the equivalent circuits of this interconnection. As before, the decoupled control is used to establish a closed-loop control of the secondary-side terminal current $i$ and the current into PEBB 1, $i_1$; since two state variables are controlled using internal eigenvectors, no external eigenvectors exist. The tuning of the two closed-loop current controllers is the exact same as in the previous section. In the experiment, both currents are controlled in a way that the secondary side acts as the power input, observing the stability of the uncontrolled primary-side midpoint voltage. Then, the current direction is reversed, expecting the primary-side midpoint voltage to become unstable.

Again, the bidirectional power supplies are set to 40 V on the primary side and 10 V on the secondary side. On the secondary side, the terminal current $i$, the current into PEBB 1 $i_1$, and both secondary-side dc-link voltages $u_1$ and $u_2$ are measured. On the primary side, the midpoint voltage $u_{\mathrm{MP}}$ is measured.

The experimental results are shown in Fig. 6.30. For $t < 0\,\mathrm{ms}$, the secondary-side terminal current reference $i^*$ is set to 4 A, making the primary side act as the power output. This corresponds to the same transferred power as in the previous experiment, but now from the secondary to the primary side. The PEBB 1 current reference $i_1^*$ is set to 2 A, ensuring power sharing between the two PEBBs. This results in a stable operation, and the primary-side midpoint voltage $u_{\mathrm{MP}}$ stays at 20 V, i.e., half of the overall primary-side dc voltage, which reflects the successful power sharing also on the primary side. At $t = 0\,\mathrm{ms}$, the signs of both current references are changed, reversing the power flow. As seen in Fig. 6.30, the closed-loop current control reduces the currents toward their negative reference values by increasing the secondary-side dc-link voltages $u_1$ and $u_2$. However, as soon as the currents become negative at about 10 ms, making the primary side act as the uncontrolled power input, the primary-side midpoint voltage $u_{\mathrm{MP}}$ starts to exponentially increase, reaching 30 V shortly after. Crossing this limit, the software performs a safety shutdown of the experiment at 13.7 ms. This confirms the stability assessment of the primary-side interconnection from Section 5.4.3.

In summary, it could be experimentally shown that the assessment of the stability of uncontrolled interconnected converter ports made in Section 5.4.3 and Appendix C predicts the stability limits correctly. Two PEBBs were interconnected in series on the primary side and in parallel on the secondary side, which are those interconnections that increase the number of states, making the overall dc-dc converter system overdetermined. Applying the decoupled control to the primary side controlling the midpoint voltage, the uncontrolled secondary sides were stable as long as power was transferred from primary to secondary. Upon a sudden reversal of the direction of power transfer, the uncontrolled secondary sides became unstable. The same was observed when controlling the secondary side and observing the stability of the uncontrolled primary-side midpoint voltage. The rule of thumb from Section 5.4.3, which states that any uncontrolled interconnection of individual converter ports is stable if every port acts as a constant-power source (CPS), is confirmed by these experiments.




(a) Controlled primary side (b) Uncontrolled secondary side

Figure 6.27: Equivalent circuit of two PEBBs connected in series on the primary side and in parallel on the secondary side, with the decoupled control applied to the primary side

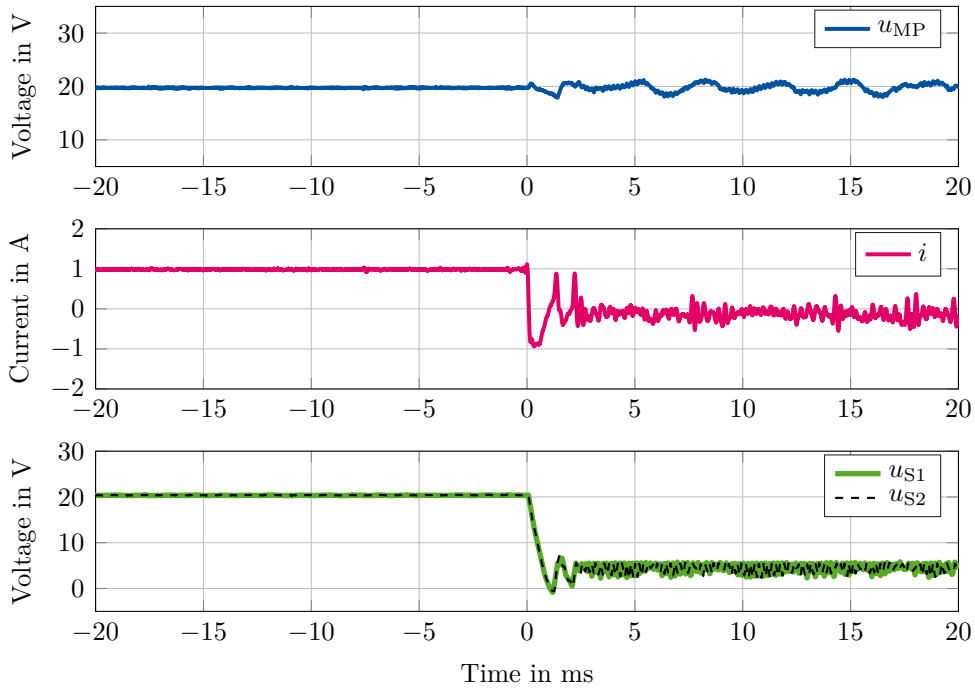
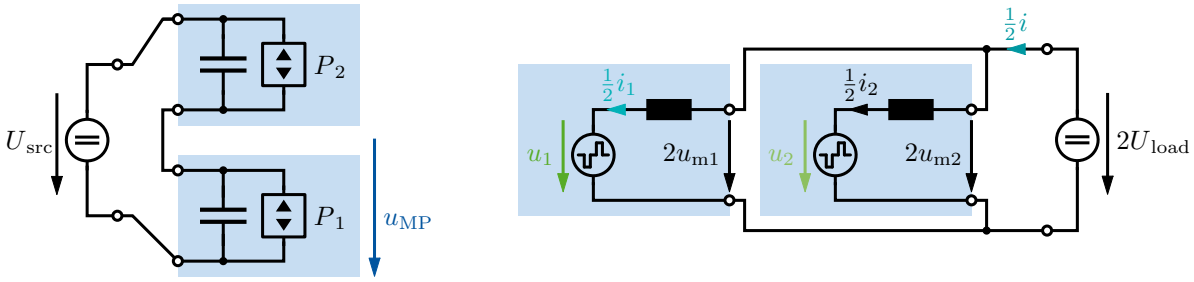



Figure 6.28: Measurement of the stability of the uncontrolled secondary-side interconnected port depending on the power flow direction




(a) Uncontrolled primary side

(b) Controlled secondary side

Figure 6.29: Equivalent circuit of two PEBBs connected in series on the primary side and in parallel on the secondary side, with the decoupled control applied to the secondary side

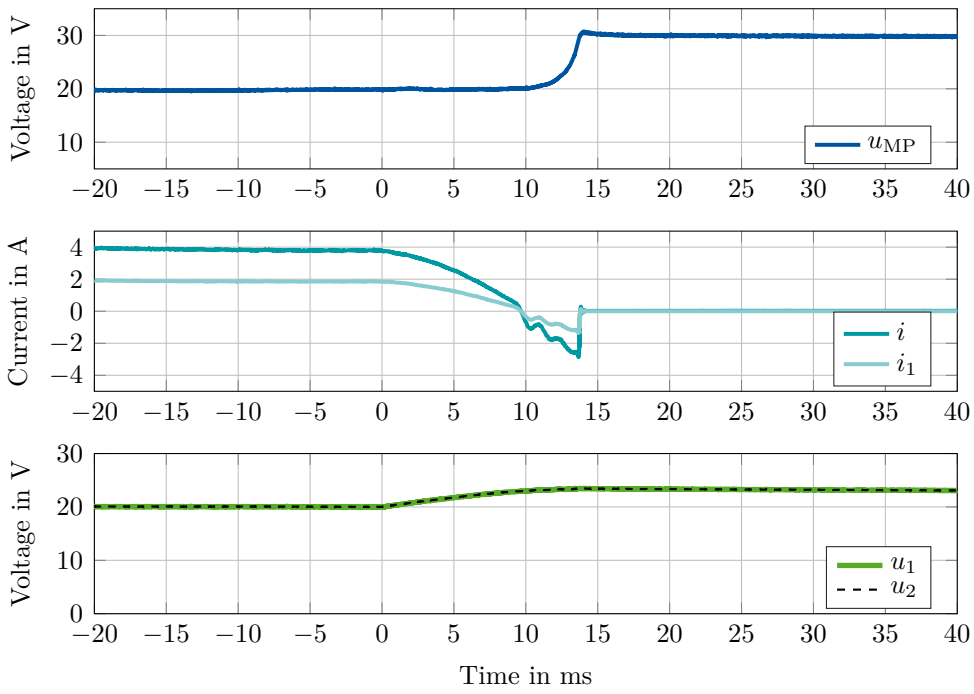



Figure 6.30: Measurement of the stability of the uncontrolled primary-side interconnected port depending on the power flow direction

## 6.3 Summary

In this chapter, the theoretical decoupling and control strategies from Chapter 4 and Chapter 5 were put into practice. First, the decoupled control of modular dc-dc converter systems consisting of two PEBBs from Chapter 4 was validated on a 200 kW dc-dc converter system. Then, the decoupled control of arbitrary dc-dc converter systems from Chapter 5 was validated on a low-power, modular, re-configurable dc-dc converter platform that was specifically designed for this dissertation.

For the validation of the decoupled control of a two-converter system, already existing hardware was used, namely a galvanically isolated, 200 kW OBC for catenary trucks, as it has been introduced in Section 4.1 and used in the simulations in Chapter 4. It consists of two three-phase DABs rated 100 kW each. Transient measurements were conducted both in IPOP and ISOP interconnection, using the decoupling approach in CM/DM coordinates. With the PEBBs in IPOP interconnection, a B2B experiment was carried out, which requires the closed-loop control of the secondary-side load voltage and the circulating current. It could be demonstrated experimentally that under CM/DM coordinates, the interaction of those two control loops could be reduced to a minimum, enabling simultaneous and dynamic control of both variables. The ISOP interconnection of the PEBBs, in turn, requires the closed-loop control of the load current and the primary-side midpoint voltage, which needs to be kept at 50 % of the primary-side dc-link voltage at all times. Hence, the stability of this interconnection relies on a closed-loop control. Also in this case, it could be demonstrated experimentally that the control in CM/DM coordinates is suitable and keeps the system stable.

For the validation of the decoupled control for arbitrary dc-dc converter systems, a modular, re-configurable platform consisting of four PEBBs and a control PCB was designed and commissioned. A current-fed, single-phase DAB was selected as topology because it allows to implement an MC-type port on the primary side and an MV-type port on the secondary side. Using GaN semiconductor devices, the PEBBs could be kept small and the control bandwidths could be maximized. With the four PEBBs attached to the control PCB, various interconnections could be established on the primary and secondary sides using custom-made copper busbars. The decoupling and control algorithms developed in Chapter 5 were implemented on an MCU and an FPGA on the control PCB. After the commissioning and efficiency characterization of the PEBBs, the MC-type and MV-type port characteristic was implemented and verified on the primary and secondary side, respectively. Finally, a decoupled control for all eight interconnection scenarios discussed in Chapter 5 was implemented and characterized experimentally. It could be shown that using the eigenvector-based control, the interactions between all control goals could be minimized, greatly facilitating the control of complex dc-dc converter system configurations. In a final step, the stability of modular dc-dc converter systems was experimentally verified, confirming that the decoupled control should always be applied to the power input port of a modular dc-dc converter system because any uncontrolled interconnected converter port is stable when it acts as the power output.

# 7 Conclusions and Outlook

To satisfy the increasing market demand for power-electronic converters, for example in automotive applications, the modularization of power-electronic converters is a key concept. In contrast to the development of a new product for each application, the parallel or series interconnection of already existing products to increase their current or voltage rating, respectively, has the advantage of lower development cost, shorter time to market, improved redundancy and maintenance, and higher partial-load efficiency. This concept of power-electronic building blocks (PEBBs) has the potential to greatly improve the scalability of power electronics in general.

Despite these advantages of the PEBB philosophy, the control of interconnected converter systems also poses challenges because the interconnection of multiple PEBBs to form a modular converter system introduces cross couplings in their control loops. Hence, the goal of this dissertation was to develop a generalized, decoupled control methodology for modular, galvanically isolated dc-dc converter systems, which should be independent of the PEBB topology or the interconnection variant, guarantee system stability, and be as simple and physically insightful as possible.

The following sections summarize the contributions and key outcomes of this dissertation and recommend future work.

## 7.1 Contributions and Key Outcomes

In this dissertation, the generalized, decoupled control methodology was derived in several steps; first for a system consisting of only two PEBBs, before expanding the idea to an arbitrary number of interconnected PEBBs. Both the more specific and the generalized concept were validated experimentally. The following paragraphs summarize the key outcomes of this dissertation.

**Decoupling and Control of Two-Converter Systems:** The two-converter system addressed in Chapter 4 was a 200 kW on-board charger (OBC) for next-generation catenary trucks, consisting of two 100 kW three-phase dual-active bridge (DAB) converters. Two interconnection variants were considered, namely the input-parallel output-parallel (IPOP) and the input-series output-parallel (ISOP) interconnection. It has been shown that the

voltage and current control loops that were developed for the standalone operation of one PEBB exhibited significantly worse performance when they were applied to the interconnected converter. Rather than assigning individual control tasks to each PEBB, they must be considered as a unity. Instead of selecting the individual currents delivered by each PEBB as the control inputs to the system, the so-called common-mode (CM) and differential-mode (DM) currents were defined, i.e., the sum and the difference of the individual currents. For both the IPOP and the ISOP interconnection schemes, the use of these new input variables results in a fully decoupled system model and yields the same control performance that had been observed for the standalone operation. In mathematical terms, this alternative selection of input variables is equivalent to applying a linear transformation to the state-space model using a transformation matrix. The approach was successfully validated on the prototype of the catenary truck OBC in Section 6.1, demonstrating the decoupled control both in IPOP and ISOP interconnection.

**Classification of Arbitrary Converter Systems:** The concept for two-converter systems was expanded to arbitrary interconnections of galvanically isolated dc-dc converter systems in Chapter 5. The decoupling technique should be applied to one port of a dc-dc converter, i.e., either its input or output side; the ports of the individual PEBB being called "individual ports" and their interconnection being called "interconnected port". It has been shown that either port of any power-electronic topology can be modeled in one of two ways, namely a manipulated current (MC) or manipulated voltage (MV) port. This way, the individual ports of any power-electronic topology can be condensed into an equivalent circuit. Then, eight different interconnection variants of those equivalent circuits were identified, i.e., eight different types of interconnected ports. This step is of major importance in the development of the generalized control methodology because it introduces a useful layer of abstraction by separating the interior operation of the PEBBs from their interconnection. This ensures the complete independence of the derived control methodology from the chosen topology, its operating principle, and its modulation strategy. Moreover, any PEBB topology can be used within this framework, and every theoretically possible interconnection variant is covered.

**Decoupling Technique for Arbitrary Converter Systems:** For each of the eight possible interconnection variants, the state-space models were derived. Those state-space models mostly contain fully occupied system matrices, which indicates the cross couplings between the individual ports. Following the idea of CM/DM currents from the two-converter system, similar input patterns needed to be found for large interconnected ports that would yield a decoupling of the state-space model. The found solution is to use the eigenvectors of the system matrices as input patterns, which diagonalize the system matrices and hence split the multiple-input, multiple-output (MIMO) system into multiple single-input, single-output (SISO) systems. It has been shown that the transformation matrix to achieve the decoupled control of any interconnected port can be composed of these eigenvectors. The resulting decoupled system model allows to manipulate all state

variables in the interconnected port as well as all available degrees of freedom, such as the transferred power, completely independently. Rather than being mathematically abstract, all found eigenvectors have a direct physical meaning, which makes the decoupling technique comprehensive and physically insightful.

**Stability Proof for Arbitrary Converter Systems:** Since this decoupling approach can only be applied to one interconnected port of the modular dc-dc converter system, the other one has to be left uncontrolled. Due to the power-conserving nature of dc-dc converters, it contains constant-power sources (CPSs) or constant-power loads (CPLs) and hence incorporates a nonlinear system. From literature, it is known that if this port acts as the power output, it tends to be stable, whereas for the case in which it acts as the power input, it tends to be unstable. However, a rigorous, large-signal, mathematical proof of this stability assessment that accounts for the nonlinear nature of the interconnected port and avoids model linearization and small-signal modeling had been missing. In this dissertation, the direct method by Lyapunov was utilized to provide such proofs, confirming at least asymptotic stability, but in most cases even exponential stability of the uncontrolled interconnected port that acts as the power output. These proofs have global validity throughout all operating points. Even overdetermined converter interconnections are covered, in which the number of state variables exceeds the number of PEBBs and hence relying on the stability of some state variables is inevitable. The provided stability proofs will potentially increase the confidence to rely on this asymptotic stability in future applications.

**Control Design Guidelines for Arbitrary Converter Systems:** Finally, a set of guidelines was formulated to realize the actual control of the decoupled interconnected converter port. Due to its decoupled nature, separate control loops can be provided for every state variable, which are guaranteed to minimize interactions with each other. The same can be done for all remaining degrees of freedom in the interconnected converter port, such as for the overall power transfer, or for circulating currents. In Section 6.2, the decoupled control has been validated experimentally using four 200 W PEBBs, which are attached to a common control platform and can be electrically interconnected in an arbitrary fashion. Using this setup, all eight possible interconnection variants could be successfully validated. With the found transformation matrices, which cause the system to decouple, there was no need for anything more complex than a simple PI regulator for each state variable.

In summary, the proposed generalized control methodology for modular dc-dc converter systems achieves the goals set out in Section 1.2 by ensuring the decoupled control of any interconnection of any dc-dc converter topology with guaranteed stability, while being easy to implement and physically insightful. It contributes to the general understanding of modular power electronics and has the ability to improve the scalability and interoperability of such systems, advancing the concept of power-electronic building blocks.

## 7.2 Recommended Future Work

Evidently, the proposal of the generalized control methodology in this dissertation can only be understood as a starting point, and several incremental improvements should be made in future work. This final section summarizes research questions that are yet to be answered and recommends starting points for future research topics.

An obvious recommendation is to apply the generalized decoupled control methodology to other applications to build experience and also explore possible limitations. It is particularly interesting how well the MC-type or MV-type behavior can be realized for other dc-dc converter topologies, maybe even multi-port topologies. Additionally, the approach could be realized on power-electronic hardware of higher power and voltage ratings, with a larger number of PEBBs.

From a theoretical viewpoint, it is particularly interesting to explore the limitations of the decoupling technique in more detail. As the decoupling strongly relies on the precision of the manipulated currents or voltages in MC-type or MV-type ports, respectively, minor cross-coupling effects cannot be avoided. Additionally, in many cases the MC-type or MV-type port behavior can only be realized with a limited bandwidth, which may cause interactions with the outer control loops. The robustness of the outer control loops against those effects should be researched and become one of the primary control design goals. Furthermore, since equal port capacitances and inductances were assumed in this dissertation, the robustness of the decoupled control approach with respect to component tolerances should be explored.

Moreover, the control design guidelines from Section 5.4 could only provide general recommendations because the control design is mainly driven by the target application. As not all of the given guidelines could be verified experimentally, it would be interesting to explicitly explore the consequences of different choices of state variables or external eigenvectors, of different associations of primary-side ports with secondary-side ports, and the possibilities of converter partitioning. The latter is especially interesting in order to partly decentralize the control methodology, improving redundancy.

The proposed procedure for stability assessment using the direct method by Lyapunov could be applied to more systems, maybe even beyond the scope of galvanically isolated dc-dc converters. It could also be expanded to more complex interconnection scenarios with other types of loads attached to the terminals of the interconnected converter.

As explored in Section 6.2.5, there are overdetermined converter interconnections that become unstable upon a reversal of the direction of power flow. If such configurations shall be operated in a bidirectional fashion, it would be necessary to dynamically apply the decoupled control to either the primary or the secondary side, depending on the instantaneous direction of power flow. The stability and dynamics of such switchover processes should be carefully explored.

Although the proposed control methodology operates on a linear transformation, the individual converter ports must still receive individual commands that have to be computed using the inverse transformation matrix. Usually, command limits are provided for every control loop, and anti-windup measures are implemented for the integrators if those limits are violated. In decoupled coordinates, anti-windup measures have to be rethought because they also undergo a coordinate transformation. An important exemplary case could be an interconnection in which a circulating current is controlled as external eigenvector: Apart from a limit that is imposed on the magnitude of this circulating current, also every individual port current must be limited to positive values in order to not compromise stability limitations. Hence, anti-windup should be incorporated into the mathematical framework of the proposed methodology.

Finally, it would be very interesting to investigate the extent to which the philosophy of abstracting dc-dc converters into standardized equivalent circuits and the utilizing the resulting eigenvectors for control purposes can be transferred to other areas of power electronics.

# Appendix

## A Eigenspace Analysis of Modular DC-DC Converter Systems

Carrying out the step-by-step procedure to find a transformation matrix for the various interconnection variants, some steps have been shown in an abbreviated fashion in Section 5.3 for the sake of conciseness, showing only the final results. More specifically, the complete derivation of the eigenvalues of the $\mathbf{D_m}$ matrices yet has to be carried out. Additionally, it has to be proven that the internal left modal matrices $\mathbf{V}_\mathrm{I}$ and the external left modal matrices $\mathbf{V}_\mathrm{E}$ contain left eigenvalues of $\mathbf{D_m}$ corresponding to the eigenvalues 0 and 1, respectively. The corresponding steps 2–4 are carried out in the following for those interconnection variants that were not completely covered in Section 5.3.

### A.1 xPyS Interconnection of MC Ports with Ideal Voltage Source

Analyzing the $x\mathrm{P}y\mathrm{S}$ interconnection of MC-type ports with ideal voltage source in Section 5.3.2, the manipulated feed-through matrix $\mathbf{D_m}$, and the internal and external left modal matrices $\mathbf{V}_\mathrm{I}$ and $\mathbf{V}_\mathrm{E}$ have been found/proposed as shown in the following lines. To execute the calculations in steps 2–4, it is useful to re-write the expressions for the matrices, the new representations are highlighted in blue:

$$
\begin{aligned}
\mathbf{D_m} &= \frac{1}{n} \cdot \begin{pmatrix}
1-y+n & 1-y & \cdots & 1-y & & & & \\
1-y & 1-y+n & \cdots & 1-y & & & & \\
\vdots & \vdots & \ddots & \vdots & & & & \\
1-y & 1-y & \cdots & 1-y+n & & & & \\
 & & & & \ddots & & & \\
 & & & & & 1-y+n & 1-y & \cdots & 1-y \\
 & & & & & 1-y & 1-y+n & \cdots & 1-y \\
 & & & & & \vdots & \vdots & \ddots & \vdots \\
 & & & & & 1-y & 1-y & \cdots & 1-y+n
\end{pmatrix} \\
&= \frac{1}{n} \cdot \mathbf{1}_{n\times n} + \left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right)\right) \\
&= \frac{1}{n} \cdot (\mathbf{1}_{y\times n} \otimes \mathbf{1}_{x\times 1}) + \left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right)\right),
\end{aligned}
\tag{A.1}
$$

$$\mathbf{V}_\mathrm{I} = \frac{1}{n} \cdot \begin{pmatrix} 1-y & \cdots & 1-y & 1 & \cdots & 1 & \cdots & 1 & \cdots & 1 & 1 & \cdots & 1 \\ 2-y & \cdots & 2-y & 2-y & \cdots & 2-y & \cdots & 2 & \cdots & 2 & 2 & \cdots & 2 \\ \vdots & & \vdots & \vdots & & \vdots & \ddots & & & & \vdots & & \vdots \\ -1 & \cdots & -1 & -1 & \cdots & -1 & \cdots & -1 & \cdots & -1 & y-1 & \cdots & y-1 \end{pmatrix}$$

$$= \frac{1}{n} \cdot \begin{pmatrix} 1-y & 1 & 1 & \cdots & 1 \\ 2-y & 2-y & 2 & \cdots & 2 \\ \vdots & \vdots & \ddots & & \vdots \\ -1 & -1 & -1 & \cdots & y-1 \end{pmatrix} \otimes \mathbf{1}_{1\times x} =: \mathbf{V}_\mathrm{I}^{\square} \otimes \mathbf{1}_{1\times x}, \tag{A.2}$$

$$\mathbf{V}_\mathrm{E} = \begin{pmatrix} \frac{1}{y} & \frac{1}{y} & \frac{1}{y} & \cdots & \frac{1}{y} & \cdots & \frac{1}{y} & \frac{1}{y} & \frac{1}{y} & \cdots & \frac{1}{y} \\ 1 & -1 & 0 & \cdots & 0 & & & & & & \\ 0 & 1 & -1 & \cdots & 0 & & & & & & \\ \vdots & & \ddots & \ddots & \vdots & \cdots & & \mathbf{0}_{(x-1)\times x} & & & \\ 0 & 0 & \cdots & 1 & -1 & & & & & & \\ & & \vdots & & & \ddots & & \vdots & & & \\ & & & & & & 1 & -1 & 0 & \cdots & 0 \\ & & & & & & 0 & 1 & -1 & \cdots & 0 \\ & & \mathbf{0}_{(x-1)\times x} & & & \cdots & \vdots & & \ddots & \ddots & \vdots \\ & & & & & & 0 & 0 & \cdots & 1 & -1 \end{pmatrix}$$

$$= \begin{pmatrix} \frac{1}{y} \cdot \mathbf{1}_{1\times n} \\ \mathbf{I}_y \otimes \begin{pmatrix} 1 & -1 & 0 & \cdots & 0 \\ 0 & 1 & -1 & \cdots & 0 \\ \vdots & & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 & -1 \end{pmatrix} \end{pmatrix} =: \begin{pmatrix} \frac{1}{y} \cdot \mathbf{1}_{1\times n} \\ \mathbf{I}_y \otimes \mathbf{V}_\mathrm{E}^{\square} \end{pmatrix}. \tag{A.3}$$

The $n \times n$ matrix $\mathbf{D_m}$ consists of a $y \times y$ grid of $x \times x$ sub-matrices. In turn, the internal left modal matrix $\mathbf{V}_\mathrm{I}$ is a $(y-1) \times n$ matrix and consists of a $(y-1) \times y$ grid of $1 \times x$ sub-matrices. Finally, the external left modal matrix $\mathbf{V}_\mathrm{E}$ consists of one line representing the CM current, concatenated with a block-diagonal matrix of $y$ blocks, each of the dimension $(x-1) \times x$. In the following, the calculations following steps 2–4 of the step-by-step procedure to find a coordinate transformation matrix $\mathbf{T}$ are shown.

**Step 2 — Find the eigenvalues:** The first step is to find the eigenvalues of the matrix $\mathbf{D_m}$. This is done by solving the characteristic polynomial

$$\begin{aligned} 0 &\overset{!}{=} \det\left(\frac{1}{n}\mathbf{1}_{n\times n} + \left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\right) - \lambda\mathbf{I}_n\right) \\ &= \det\left(\frac{1}{n}\mathbf{1}_{n\times n} + \left(\mathbf{I}_y \otimes \left((1-\lambda)\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\right)\right) \\ &\overset{(3.37)}{=} \left(1 + \frac{1}{n}\mathbf{1}_{1\times n}\left(\mathbf{I}_y \otimes \left((1-\lambda)\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\right)^{-1}\mathbf{1}_{n\times 1}\right) \det\left(\mathbf{I}_y \otimes \left((1-\lambda)\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\right), \end{aligned}$$

while the last line has been obtained by applying the matrix determinant lemma (3.37) introduced in Section 3.2.3. The determinant highlighted in blue is the characteristic polynomial of the matrix $\mathbf{D_m}$ in the case of $x\mathrm{P}y\mathrm{S}$ connected MC-type converters without ideal voltage source, as derived in (5.28),

$$\ldots \overset{(5.28)}{=} \left(1 + \frac{1}{n}\mathbf{1}_{1\times n}\left(\mathbf{I}_y \otimes \left((1-\lambda)\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\right)^{-1}\mathbf{1}_{n\times 1}\right) \cdot (-\lambda)^y \cdot (1-\lambda)^{n-y}$$
$$\overset{(3.33)}{=} \left(1 + \frac{1}{n}\mathbf{1}_{1\times n}\left(\mathbf{I}_y \otimes \left((1-\lambda)\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)^{-1}\right)\mathbf{1}_{n\times 1}\right) \cdot (-\lambda)^y \cdot (1-\lambda)^{n-y}.$$

The inverse highlighted in magenta can be resolved by applying the Sherman-Morrison formula for this special weighted sum of identity and unity matrix (3.41):

$$\ldots \overset{(3.41)}{=} \left(1 + \frac{1}{n}\mathbf{1}_{1\times n}\left(\mathbf{I}_y \otimes \left(\frac{\lambda\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}}{\lambda(1-\lambda)}\right)\right)\mathbf{1}_{n\times 1}\right) \cdot (-\lambda)^y \cdot (1-\lambda)^{n-y}$$
$$\overset{(3.26)}{=} \left(1 + \frac{1}{n\lambda(1-\lambda)}\mathbf{1}_{1\times n}\left(\mathbf{I}_y \otimes \left(\lambda\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\right)\mathbf{1}_{n\times 1}\right) \cdot (-\lambda)^y \cdot (1-\lambda)^{n-y}.$$

The product highlighted in blue of a matrix defined by a Kronecker product with a column vector full of ones can be interpreted as condensing the sum of all the rows of the matrix into a new column vector. In each of its lines, the matrix defined by the Kronecker product consists of one entry $\lambda$ on the diagonal and a number $x$ of entries all equal to $-\frac{1}{x}$, resulting each row to sum up to $\lambda - 1$:

$$\ldots = \left(1 + \frac{1}{n\lambda(1-\lambda)}\mathbf{1}_{1\times n} \cdot (\lambda - 1) \cdot \mathbf{1}_{n\times 1}\right) \cdot (-\lambda)^y \cdot (1-\lambda)^{n-y}.$$

The remaining expressions can be resolved easily:

$$\ldots = \left(1 - \frac{1}{\lambda}\right) \cdot (-\lambda)^y \cdot (1-\lambda)^{n-y} = \frac{1-\lambda}{-\lambda} \cdot (-\lambda)^y \cdot (1-\lambda)^{n-y}$$
$$= (-\lambda)^{y-1} \cdot (1-\lambda)^{n-y+1}.$$

This confirms the matrix $\mathbf{D_m}$ to have the internal eigenvalue of 0 with multiplicity $y-1$, which is equal to the number of states, and the external eigenvalue of 1 with multiplicity $n-y+1$.

**Step 3 — Internal eigenvectors:** As discussed in Section 5.2, it must be shown that

$$\mathbf{V}_\mathrm{I} \cdot \mathbf{D_m} = \mathbf{0}_{n_x\times n} \tag{A.4}$$

to prove that the matrix $\mathbf{B_m}$, which only differs by a scalar factor from the matrix $\mathbf{V}_\mathrm{I}$, contains internal eigenvectors of the matrix $\mathbf{D_m}$. For this purpose, the representations (A.2) and (A.1) of the matrices $\mathbf{V}_\mathrm{I}$ and $\mathbf{D_m}$ are used, respectively. This allows to evaluate

the identity (A.4) using the mixed KRONECKER and matrix product (3.29):

$$\begin{aligned}
\mathbf{V}_\mathrm{I} \cdot \mathbf{D_m} &= \left(\mathbf{V}_\mathrm{I}^{\square} \otimes \mathbf{1}_{1\times x}\right) \cdot \left(\frac{1}{n} \cdot (\mathbf{1}_{y\times n} \otimes \mathbf{1}_{x\times 1}) + \left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right)\right)\right) \\
&= \frac{1}{n} \cdot \left(\mathbf{V}_\mathrm{I}^{\square} \otimes \mathbf{1}_{1\times x}\right) \cdot (\mathbf{1}_{y\times n} \otimes \mathbf{1}_{x\times 1}) + \left(\mathbf{V}_\mathrm{I}^{\square} \otimes \mathbf{1}_{1\times x}\right) \cdot \left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right)\right) \\
&\overset{(3.29)}{=} \frac{1}{n}\left(\left(\mathbf{V}_\mathrm{I}^{\square} \cdot \mathbf{1}_{y\times n}\right) \otimes \left(\mathbf{1}_{1\times x} \cdot \mathbf{1}_{x\times 1}\right)\right) + \left(\mathbf{V}_\mathrm{I}^{\square} \cdot \mathbf{I}_y\right) \otimes \left(\mathbf{1}_{1\times x} \cdot \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right)\right) \\
&= \frac{1}{n}\left(\left(\mathbf{V}_\mathrm{I}^{\square} \cdot \mathbf{1}_{y\times n}\right) \otimes x\right) + \mathbf{V}_\mathrm{I}^{\square} \otimes \left(\mathbf{1}_{1\times x} - \frac{x}{x} \cdot \mathbf{1}_{1\times x}\right) \\
&\overset{(3.26)}{=} \frac{1}{y} \cdot \left(\mathbf{V}_\mathrm{I}^{\square} \cdot \mathbf{1}_{y\times n}\right) + \mathbf{V}_\mathrm{I}^{\square} \otimes \mathbf{0}_{1\times x} = \frac{1}{y} \cdot \left(\mathbf{V}_\mathrm{I}^{\square} \cdot \mathbf{1}_{y\times n}\right)
\end{aligned}$$

The remaining matrix multiplication suggests that every entry of the result consists of the sums of the rows of $\mathbf{V}_\mathrm{I}^{\square}$. However, by looking at (A.2), it is easily seen that all rows add up to zero, hence

$$\ldots = \mathbf{0}_{(y-1)\times n}$$

and the property of $\mathbf{V}_\mathrm{I}$ containing internal eigenvectors is successfully proven.

**Step 4 — External eigenvectors:** To prove that the external left modal matrix $\mathbf{V}_\mathrm{E}$ contains external left eigenvectors, its alternate representation (A.3) is used. Since the alleged left eigenvectors are the rows of $\mathbf{V}_\mathrm{E}$, it is sufficient to prove this property row-wise. For the first row, multiplying it by $\mathbf{D_m}$ means that the resulting vector contains the sum of all columns of $\mathbf{D_m}$, multiplied by $\frac{1}{y}$. Looking at $\mathbf{D_m}$, however, shows that the sum of its columns is all the same number for every column, i.e.,

$$\frac{1}{y} \cdot \mathbf{1}_{1\times n} \cdot \mathbf{D_m} = \frac{1}{y} \cdot \frac{1}{n} \cdot (n + x \cdot (1-y) + 1 \cdot x \cdot (y-1)) \cdot \mathbf{1}_{1\times n} = \frac{1}{y} \cdot \frac{n}{n} \cdot \mathbf{1}_{1\times n} = \frac{1}{y} \cdot \mathbf{1}_{1\times n},$$

which completely replicates the first row of $\mathbf{V}_\mathrm{E}$, confirming it to be an external eigenvector of $\mathbf{D_m}$. For the remaining rows of $\mathbf{V}_\mathrm{E}$, it can be found that

$$\begin{aligned}
\left(\mathbf{I}_y \otimes \mathbf{V}_\mathrm{E}^{\square}\right) \cdot \mathbf{D_m} &= \left(\mathbf{I}_y \otimes \mathbf{V}_\mathrm{E}^{\square}\right) \cdot \left(\frac{1}{n} \cdot \mathbf{1}_{n\times n} + \left(\mathbf{I}_y \otimes \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right)\right)\right) \\
&\overset{(3.29)}{=} \left(\mathbf{I}_y \otimes \mathbf{V}_\mathrm{E}^{\square}\right) \cdot \frac{1}{n}\mathbf{1}_{n\times n} + \left(\mathbf{I}_y \cdot \mathbf{I}_y\right) \otimes \left(\mathbf{V}_\mathrm{E}^{\square} \cdot \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right)\right) \\
&\overset{(3.26)}{=} \frac{1}{n}\left(\mathbf{I}_y \otimes \mathbf{V}_\mathrm{E}^{\square}\right) \cdot \mathbf{1}_{n\times n} + \mathbf{I}_y \otimes \left(\mathbf{V}_\mathrm{E}^{\square} - \frac{1}{x}\mathbf{V}_\mathrm{E}^{\square} \cdot \mathbf{1}_{x\times x}\right)
\end{aligned}$$

The expressions shaded in blue are taking the sum of the rows of the matrices $\left(\mathbf{I}_y \otimes \mathbf{V}_{\mathrm{E}}^{\square}\right)$ and $\mathbf{V}_{\mathrm{E}}^{\square}$, respectively; however, for both matrices it is evident that the sum of the rows is always zero because each row contains one entry 1 and one entry $-1$. Hence,

$$\ldots = \mathbf{0}_{(n-y)\times n} + \mathbf{I}_y \otimes \left(\mathbf{V}_{\mathrm{E}}^{\square} - \mathbf{0}_{(x-1)\times x}\right) = \mathbf{I}_y \otimes \mathbf{V}_{\mathrm{E}}^{\square},$$

proving also the remaining rows in $\mathbf{V}_{\mathrm{E}}$ to be external eigenvectors.

## A.2 ySxP Interconnection of MC Ports with Ideal Voltage Source

Analyzing the $y\mathrm{S}x\mathrm{P}$ interconnection of MC-type ports with ideal voltage source in Section 5.3.4, the manipulated feed-through matrix $\mathbf{D}_{\mathbf{m}}$, and the internal and external left modal matrices $\mathbf{V}_{\mathrm{I}}$ and $\mathbf{V}_{\mathrm{E}}$ have been found/proposed as shown in the following lines. To execute the calculations in steps 2–4, it is useful to re-write the expressions for the matrices, the new representations are highlighted in blue:

$$\mathbf{D}_{\mathbf{m}} = \frac{1}{y} \cdot \begin{pmatrix} 1 & \cdots & 1 & & & \\ \vdots & & \vdots & & \mathbf{0}_{y\times y} & \\ 1 & \cdots & 1 & & & \\ & & & \ddots & & \\ & & & & 1 & \cdots & 1 \\ & \mathbf{0}_{y\times y} & & & \vdots & & \vdots \\ & & & & 1 & \cdots & 1 \end{pmatrix} = \mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y}\right),$$

$$\mathbf{V}_{\mathrm{I}} = \frac{1}{y} \cdot \begin{pmatrix} 1-y & 1 & 1 & \cdots & 1 & & & & \\ 2-y & 2-y & 2 & \cdots & 2 & & \mathbf{0}_{(y-1)\times y} & & \\ \vdots & \vdots & \vdots & \ddots & \vdots & & & & \\ -1 & -1 & -1 & \cdots & y-1 & & & & \\ & & & & & \ddots & & & \\ & & \mathbf{0}_{(y-1)\times y} & & & & 1-y & 1 & 1 & \cdots & 1 \\ & & & & & & 2-y & 2-y & 2 & \cdots & 2 \\ & & & & & & \vdots & \vdots & \vdots & \ddots & \vdots \\ & & & & & & -1 & -1 & -1 & \cdots & y-1 \end{pmatrix}$$

$$= \mathbf{I}_x \otimes \frac{1}{y} \cdot \begin{pmatrix} 1-y & 1 & 1 & \cdots & 1 \\ 2-y & 2-y & 2 & \cdots & 2 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ -1 & -1 & -1 & \cdots & y-1 \end{pmatrix} =: \mathbf{I}_x \otimes \mathbf{V}_{\mathrm{I}}^{\square}, \tag{A.5}$$

$$\mathbf{V}_{\mathrm{E}} = \frac{1}{y} \cdot \begin{pmatrix} 1 & \cdots & 1 & 1 & \cdots & 1 & 1 & \cdots & 1 & \cdots & 1 & \cdots & 1 \\ 1 & \cdots & 1 & -1 & \cdots & -1 & 0 & \cdots & 0 & \cdots & 0 & \cdots & 0 \\ 0 & \cdots & 0 & 1 & \cdots & 1 & -1 & \cdots & -1 & \cdots & 0 & \cdots & 0 \\ \vdots & & \vdots & & & & & \ddots & & \ddots & \vdots & & \vdots \\ 0 & \cdots & 0 & 0 & \cdots & 0 & & \cdots & & 1 & \cdots & 1 & -1 & \cdots & -1 \end{pmatrix}$$

$$= \begin{pmatrix} & & \frac{1}{y} \cdot \mathbf{1}_{1\times n} & \\ \frac{1}{y} \cdot \begin{pmatrix} 1 & -1 & 0 & \cdots & 0 \\ 0 & 1 & -1 & \cdots & 0 \\ \vdots & & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 & -1 \end{pmatrix} & \otimes \mathbf{1}_{1\times y} & \end{pmatrix} =: \begin{pmatrix} \frac{1}{y} \cdot \mathbf{1}_{1\times n} \\ \mathbf{V}_{\mathrm{E}}^{\square} \otimes \mathbf{1}_{1\times y} \end{pmatrix}. \tag{A.6}$$

The matrix $\mathbf{D_m}$ consists of a $x \times x$ grid of $y \times y$ sub-matrices, resulting in an $n \times n$ matrix. The internal left modal matrix $\mathbf{V}_\mathrm{I}$ is a $(n-x) \times n$ matrix and consists of an $x \times x$ grid of $(y-1) \times y$ sub-matrices. Finally, the external left modal matrix $\mathbf{V}_\mathrm{E}$ consists of one line representing the CM current, concatenated with a $(x-1) \times n$ block matrix that consists of $1 \times y$ blocks that are repeated $(x-1) \times x$ times. In the following, the thorough calculations following steps 2–4 of the step-by-step procedure to find a coordinate transformation matrix $\mathbf{T}$ are carried out.

**Step 2 — Find the eigenvalues:** The first step is to find the eigenvalues of the matrix $\mathbf{D_m}$. This is done by solving the characteristic polynomial using the matrix determinant lemma for the weighted sum of identity and unity matrix (3.40),

$$\begin{aligned} 0 &\overset{!}{=} \det\left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y}\right) - \lambda \mathbf{I}_n\right) \overset{(3.28)}{=} \det\left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y} - \lambda \mathbf{I}_y\right)\right) \\ &\overset{(3.34)}{=} \det\left(-\lambda \mathbf{I}_y + \frac{1}{y} \cdot \mathbf{1}_{y\times y}\right)^x \overset{(3.40)}{=} \left((-\lambda)^y + y \cdot \frac{1}{y} \cdot (-\lambda)^{y-1}\right)^x \\ &= \left((-\lambda)^{y-1} \cdot (1-\lambda)\right)^x = (-\lambda)^{x(y-1)} \cdot (1-\lambda)^x, \end{aligned} \tag{A.7}$$

proving the matrix $\mathbf{D_m}$ to have the internal eigenvalue of 0 with multiplicity $n-x$, which is equal to the number of states, and the external eigenvalue of 1 with multiplicity $x$.

**Step 3 — Internal eigenvectors:** To show that the condition (A.4) holds, the representation (A.5) of the matrix $\mathbf{V}_\mathrm{I}$ is used, which allows the use of the mixed Kronecker and matrix product (3.29) as follows:

$$\begin{aligned} \mathbf{V}_\mathrm{I} \cdot \mathbf{D_m} &= \left(\mathbf{I}_x \otimes \mathbf{V}_\mathrm{I}^\square\right) \cdot \left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y}\right)\right) \overset{(3.29)}{=} \mathbf{I}_x \otimes \left(\mathbf{V}_\mathrm{I}^\square \cdot \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y}\right)\right) \\ &\overset{(3.26)}{=} \frac{1}{y} \cdot \mathbf{I}_x \otimes \left(\mathbf{V}_\mathrm{I}^\square \cdot \mathbf{1}_{y\times y}\right) = \frac{1}{y} \cdot \mathbf{I}_x \otimes \mathbf{0}_{(y-1)\times y} = \mathbf{0}_{x(y-1)\times n}, \end{aligned}$$

because the matrix product highlighted in blue takes the sum of the rows of $\mathbf{V}_\mathrm{I}^\square$, which is obviously zero when looking at (A.5). This proves that $\mathbf{V}_\mathrm{I}$ indeed contains internal eigenvectors of $\mathbf{D_m}$.

**Step 4 — External eigenvectors:** To prove that the external left modal matrix $\mathbf{V}_\mathrm{E}$ contains external left eigenvectors, its alternate representation (A.6) is used. For the first row in $\mathbf{V}_\mathrm{E}$, multiplying it by $\mathbf{D_m}$ means that the resulting vector contains the sum of all columns of $\mathbf{D_m}$, multiplied by $\frac{1}{y}$. Looking at $\mathbf{D_m}$, however, shows that the sum of its columns is all the same number for every column, i.e.,

$$\frac{1}{y} \cdot \mathbf{1}_{1\times n} \cdot \mathbf{D_m} = \frac{1}{y} \cdot \frac{1}{y} \cdot (1 \cdot 1 \cdot y) \cdot \mathbf{1}_{1\times n} = \frac{1}{y} \cdot \mathbf{1}_{1\times n},$$

which completely replicates the first row of $\mathbf{V}_{\mathrm{E}}$, confirming it to be an external eigenvector of $\mathbf{D_m}$. For the remaining rows of $\mathbf{V}_{\mathrm{E}}$, it can be found that

$$\begin{aligned}\left(\mathbf{V}_{\mathrm{E}}^{\square} \otimes \mathbf{1}_{1\times y}\right) \cdot \mathbf{D_m} &= \left(\mathbf{V}_{\mathrm{E}}^{\square} \otimes \mathbf{1}_{1\times y}\right) \cdot \left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y}\right)\right) \overset{(3.29)}{=} \left(\mathbf{V}_{\mathrm{E}}^{\square} \cdot \mathbf{I}_x\right) \otimes \left(\mathbf{1}_{1\times y} \cdot \frac{1}{y} \cdot \mathbf{1}_{y\times y}\right) \\ &= \mathbf{V}_{\mathrm{E}}^{\square} \otimes \left(\frac{y}{y} \cdot \mathbf{1}_{1\times y}\right) = \mathbf{V}_{\mathrm{E}}^{\square} \otimes \mathbf{1}_{1\times y},\end{aligned}$$

proving also the remaining rows in $\mathbf{V}_{\mathrm{E}}$ to be external eigenvectors.

## A.3 ySxP Interconnection of MC Ports

Analyzing the $y$S$x$P interconnection of MC-type ports without ideal voltage source in Section 5.3.3, the manipulated feed-through matrix $\mathbf{D_m}$, and the internal and external left modal matrices $\mathbf{V}_{\mathrm{I}}$ and $\mathbf{V}_{\mathrm{E}}$ have been found/proposed as shown in the following lines. To execute the calculations in steps 2–4, it is useful to re-write the expressions for the matrices, the new representations are highlighted in blue:

$$\begin{aligned}\mathbf{D_m} &= -\frac{1}{n} \cdot \begin{pmatrix} \begin{matrix} 1-x & 1-x & \cdots & 1-x \\ 1-x & 1-x & \cdots & 1-x \\ \vdots & \vdots & & \vdots \\ 1-x & 1-x & \cdots & 1-x \end{matrix} & \cdots & \mathbf{1}_{y\times y} \\ \ddots & & \\ \mathbf{1}_{y\times y} & \cdots & \begin{matrix} 1-x & 1-x & \cdots & 1-x \\ 1-x & 1-x & \cdots & 1-x \\ \vdots & \vdots & & \vdots \\ 1-x & 1-x & \cdots & 1-x \end{matrix} \end{pmatrix} \\ &= -\frac{1}{n} \cdot \mathbf{1}_{n\times n} + \left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y}\right)\right) \\ &= \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right) \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y}\right), \end{aligned} \tag{A.8}$$

$$\mathbf{V}_{\mathrm{I}} = -\frac{1}{n} \cdot \begin{pmatrix} \begin{matrix} y & y & \cdots & y \\ (1-x)+n & (1-x) & \cdots & (1-x) \\ 2(1-x)+n & 2(1-x)+n & \cdots & 2(1-x) \\ \vdots & & \ddots & \vdots \\ (y-1)(1-x)+n & (y-1)(1-x)+n & \cdots & (y-1)(1-x) \end{matrix} & \cdots & \begin{matrix} y \\ 1 \\ 2 \\ \vdots \\ (y-1) \end{matrix} & \begin{matrix} y \\ 1 \\ 2 \\ \vdots \\ (y-1) \end{matrix} & \cdots & \begin{matrix} y \\ 1 \\ 2 \\ \vdots \\ (y-1) \end{matrix} \\ \ddots & & & & \\ \begin{matrix} 1 \\ 2 \\ \vdots \\ (y-1) \end{matrix} & \cdots & \begin{matrix} (1-x)+n \\ 2(1-x)+n \\ \vdots \\ (y-1)(1-x)+n \end{matrix} & \begin{matrix} (1-x) \\ 2(1-x)+n \\ \vdots \\ (y-1)(1-x)+n \end{matrix} & \cdots & \begin{matrix} (1-x) \\ 2(1-x) \\ \vdots \\ (y-1)(1-x) \end{matrix} \end{pmatrix}$$

$$= \left( \begin{array}{c} -\frac{1}{x}\mathbf{1}_{1\times n} \\ \left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right) \otimes \left( \frac{1}{y} \begin{pmatrix} 1 & \cdots & 1 \\ 2 & \cdots & 2 \\ \vdots & & \vdots \\ y-1 & \cdots & y-1 \end{pmatrix} \right) - \mathbf{I}_x \otimes \begin{pmatrix} 1 & 0 & 0 & \cdots & 0 & 0 \\ 1 & 1 & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & & & \vdots \\ 1 & 1 & 1 & \cdots & 1 & 0 \end{pmatrix} \end{array} \right) \tag{A.9}$$

$$=: \begin{pmatrix} -\frac{1}{x}\mathbf{1}_{1\times n} \\ \left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right) \otimes \mathbf{V}_{\mathrm{I}}^{\square} - \mathbf{I}_x \otimes \mathbf{V}_{\mathrm{I}}^{\blacksquare} \end{pmatrix}, \tag{A.10}$$

$$\mathbf{V}_{\mathrm{E}} = \frac{1}{y} \cdot \begin{pmatrix} 1 & \cdots & 1 & -1 & \cdots & -1 & 0 & \cdots & 0 & \cdots & 0 & \cdots & 0 \\ 0 & \cdots & 0 & 1 & \cdots & 1 & -1 & \cdots & -1 & \cdots & 0 & \cdots & 0 \\ \vdots & & \vdots & & & & & \ddots & & \ddots & \vdots & & \vdots \\ 0 & \cdots & 0 & 0 & \cdots & 0 & & \cdots & & 1 \cdots 1 & -1 & \cdots & -1 \end{pmatrix}$$

$$= \frac{1}{y} \cdot \begin{pmatrix} 1 & -1 & 0 & \cdots & 0 \\ 0 & 1 & -1 & \cdots & 0 \\ \vdots & & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 & -1 \end{pmatrix} \otimes \mathbf{1}_{1\times y} =: \mathbf{V}_{\mathrm{E}}^{\square} \otimes \mathbf{1}_{1\times y}. \tag{A.11}$$

The matrix $\mathbf{D_m}$ consists is a block matrix consisting of $x \times x$ blocks, each of the size $y \times y$; it can be represented as the sum of a matrix in which all entries are equal and a block-diagonal matrix. The internal left modal matrix consists of one line representing the current that manipulates the common dc-link voltage $u$, concatenated with an $x \times x$ block matrix structure of $(y-1) \times y$ sub-matrices representing the currents that manipulate the midpoint voltages in the series-connected branches. The external left modal matrix $\mathbf{V}_{\mathrm{E}}$ has an overall dimension of $(x-1) \times n$, the rows of which represent the DM currents between the individual series-connected converter port branches; however, it also has a block structure and consists of $1 \times y$ sub-matrix blocks. In the following, the thorough calculations following steps 2–4 of the step-by-step procedure to find a coordinate transformation matrix $\mathbf{T}$ are carried out.

**Step 2 — Find the eigenvalues:** The first step is to find the eigenvalues of the matrix $\mathbf{D_m}$. This is done by solving the characteristic polynomial using the matrix determinant lemma (3.37):

$$\begin{aligned} 0 &\overset{!}{=} \det\left(-\frac{1}{n} \cdot \mathbf{1}_{n\times n} + \left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y}\right)\right) - \lambda \mathbf{I}_n\right) \\ &= \det\left(-\frac{1}{n} \cdot \mathbf{1}_{n\times n} + \left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y} - \lambda \mathbf{I}_y\right)\right)\right) \\ &\overset{(3.37)}{=} \left(1 - \frac{1}{n}\mathbf{1}_{1\times n}\left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y} - \lambda \mathbf{I}_y\right)\right)^{-1} \mathbf{1}_{n\times 1}\right) \cdot \det\left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y} - \lambda \mathbf{I}_y\right)\right). \end{aligned}$$

The determinant in blue is already known, it is the characteristic polynomial of the matrix $\mathbf{D_m}$ in the case of $y$S$x$P interconnected MC-type converters with ideal voltage source, as derived in (5.67):

$$\ldots \overset{(5.67)}{=} \left(1 - \frac{1}{n}\mathbf{1}_{1\times n}\left(\mathbf{I}_x \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y} - \lambda \mathbf{I}_y\right)\right)^{-1} \mathbf{1}_{n\times 1}\right) \cdot (-\lambda)^{x(y-1)}(1-\lambda)^x$$

$$\overset{(3.33)}{=} \left(1 - \frac{1}{n}\mathbf{1}_{1\times n}\left(\mathbf{I}_x \otimes \left(\frac{1}{y}\cdot\mathbf{1}_{y\times y} - \lambda\mathbf{I}_y\right)^{-1}\right)\mathbf{1}_{n\times 1}\right)\cdot(-\lambda)^{x(y-1)}(1-\lambda)^x.$$

The inverse highlighted in magenta can be computed using (3.41):

$$\ldots \overset{(3.41)}{=} \left(1 - \frac{1}{n}\mathbf{1}_{1\times n}\left(\mathbf{I}_x \otimes \frac{(1-\lambda)\mathbf{I}_y - \frac{1}{y}\mathbf{1}_{y\times y}}{(-\lambda)(1-\lambda)}\right)\mathbf{1}_{n\times 1}\right)\cdot(-\lambda)^{x(y-1)}(1-\lambda)^x$$
$$\overset{(3.26)}{=} \left(1 - \frac{1}{n(-\lambda)(1-\lambda)}\mathbf{1}_{1\times n}\left(\mathbf{I}_x \otimes \left((1-\lambda)\mathbf{I}_y - \frac{1}{y}\mathbf{1}_{y\times y}\right)\right)\mathbf{1}_{n\times 1}\right)\cdot(-\lambda)^{x(y-1)}(1-\lambda)^x.$$

The expression highlighted in blue takes the sum of the rows of the matrix defined by the KRONECKER product. In each row, one entry $(1-\lambda)$ can be found, as well as $y$ entries all equal to $-\frac{1}{y}$, giving a sum of $-\lambda$ for each row. Hence,

$$\begin{aligned}\ldots &= \left(1 - \frac{1}{n(-\lambda)(1-\lambda)}\mathbf{1}_{1\times n}\cdot(-\lambda)\cdot\mathbf{1}_{n\times 1}\right)\cdot(-\lambda)^{x(y-1)}(1-\lambda)^x \\ &= \left(1 - \frac{1}{1-\lambda}\right)\cdot(-\lambda)^{x(y-1)}(1-\lambda)^x = \frac{-\lambda}{1-\lambda}\cdot(-\lambda)^{x(y-1)}(1-\lambda)^x \\ &= (-\lambda)^{x(y-1)+1}(1-\lambda)^{x-1}.\end{aligned}$$

This proves the matrix $\mathbf{D_m}$ to have the internal eigenvalue of 0 with multiplicity $n-x+1$, which is equal to the number of states, and the external eigenvalue of 1 with multiplicity $x-1$.

**Step 3 — Internal eigenvectors:** To prove that the internal left modal matrix $\mathbf{V}_\mathrm{I}$ contains internal left eigenvectors, its alternate representation (A.10) is used. For the first row in $\mathbf{V}_\mathrm{I}$, multiplying it by $\mathbf{D_m}$ means that the resulting vector contains the sum of all columns of $\mathbf{D_m}$, multiplied by $-\frac{1}{x}$. Looking at $\mathbf{D_m}$, however, shows that the sum of its columns is all the same number for every column, i.e.,

$$-\frac{1}{x}\cdot\mathbf{1}_{1\times n}\cdot\mathbf{D_m} = \frac{1}{x}\cdot\frac{1}{n}\cdot((1-x)\cdot y + 1\cdot y\cdot(x-1))\cdot\mathbf{1}_{1\times n} = \mathbf{0}_{1\times n},$$

proving that the first row of $\mathbf{V}_\mathrm{I}$ is indeed an internal eigenvector of $\mathbf{D_m}$. For proving this property for the remaining lines in $\mathbf{V}_\mathrm{I}$, the alternate representation of $\mathbf{D_m}$ in (A.8) is used:

$$\begin{aligned}&\left(\left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\otimes\mathbf{V}_\mathrm{I}^{\square} - \mathbf{I}_x\otimes\mathbf{V}_\mathrm{I}^{\blacksquare}\right)\cdot\mathbf{D_m} \\ = \;&\left(\left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\otimes\mathbf{V}_\mathrm{I}^{\square} - \mathbf{I}_x\otimes\mathbf{V}_\mathrm{I}^{\blacksquare}\right)\cdot\left(\left(\mathbf{I}_x - \frac{1}{x}\cdot\mathbf{1}_{x\times x}\right)\otimes\left(\frac{1}{y}\cdot\mathbf{1}_{y\times y}\right)\right) \\ \overset{(3.29)}{=} \;&\left(\left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\cdot\left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\right)\otimes\left(\mathbf{V}_\mathrm{I}^{\square}\cdot\frac{1}{y}\mathbf{1}_{y\times y}\right) - \left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right)\otimes\left(\mathbf{V}_\mathrm{I}^{\blacksquare}\cdot\frac{1}{y}\mathbf{1}_{y\times y}\right)\end{aligned}$$

$$
\begin{aligned}
&= \left(\mathbf{I}_x - \frac{2}{x}\mathbf{1}_{x\times x} + \frac{x}{x^2}\mathbf{1}_{x\times x}\right) \otimes \left(\mathbf{V}_{\mathrm{I}}^{\square} \cdot \frac{1}{y}\mathbf{1}_{y\times y}\right) - \left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right) \otimes \left(\mathbf{V}_{\mathrm{I}}^{\blacksquare} \cdot \frac{1}{y}\mathbf{1}_{y\times y}\right) \\
&= \left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right) \otimes \left(\mathbf{V}_{\mathrm{I}}^{\square} \cdot \frac{1}{y}\mathbf{1}_{y\times y}\right) - \left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right) \otimes \left(\mathbf{V}_{\mathrm{I}}^{\blacksquare} \cdot \frac{1}{y}\mathbf{1}_{y\times y}\right) \\
&\overset{(3.28)}{=} \left(\mathbf{I}_x - \frac{1}{x}\mathbf{1}_{x\times x}\right) \otimes \left(\left(\mathbf{V}_{\mathrm{I}}^{\square} - \mathbf{V}_{\mathrm{I}}^{\blacksquare}\right) \cdot \frac{1}{y}\mathbf{1}_{y\times y}\right).
\end{aligned}
$$

The resulting matrix contains all zero entries if and only if the expression highlighted in magenta evaluates to all zeros. This expression takes the sum of the rows of the matrix $\left(\mathbf{V}_{\mathrm{I}}^{\square} - \mathbf{V}_{\mathrm{I}}^{\blacksquare}\right)$. The difference of the two matrices, which are both $(y-1) \times y$, is given according to (A.9):

$$
\mathbf{V}_{\mathrm{I}}^{\square} - \mathbf{V}_{\mathrm{I}}^{\blacksquare} = \frac{1}{y}\begin{pmatrix} 1 & \cdots & 1 \\ 2 & \cdots & 2 \\ \vdots & & \vdots \\ y-1 & \cdots & y-1 \end{pmatrix} - \begin{pmatrix} 1 & 0 & 0 & \cdots & 0 & 0 \\ 1 & 1 & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & & & \vdots \\ 1 & 1 & 1 & \cdots & 1 & 0 \end{pmatrix}.
$$

However, the row number $p$ in the left matrix contains $y$ entries all equal to $\frac{p}{y}$, while in the same row number $p$, the right matrix contains $p$ entries all equal to one. Hence, subtraction of the two matrices and taking the sum of the rows indeed yields all zeros, which finally proves that the matrix $\mathbf{V}_{\mathrm{I}}$ contains internal eigenvectors of $\mathbf{D_m}$.

**Step 4 — External eigenvectors:** To prove that the external left modal matrix $\mathbf{V}_{\mathrm{E}}$ contains external left eigenvectors, its alternate representation (A.11) is used:

$$
\begin{aligned}
\mathbf{V}_{\mathrm{E}} \cdot \mathbf{D_m} &= \left(\left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right) \otimes \left(\frac{1}{y} \cdot \mathbf{1}_{y\times y}\right)\right) \cdot \left(\mathbf{V}_{\mathrm{E}}^{\square} \otimes \mathbf{1}_{1\times y}\right) \\
&\overset{(3.29)}{=} \left(\mathbf{V}_{\mathrm{E}}^{\square} \cdot \left(\mathbf{I}_x - \frac{1}{x} \cdot \mathbf{1}_{x\times x}\right)\right) \otimes \left(\mathbf{1}_{1\times y} \cdot \frac{1}{y}\mathbf{1}_{y\times y}\right) \\
&= \left(\mathbf{V}_{\mathrm{E}}^{\square} - \frac{1}{x} \cdot \mathbf{V}_{\mathrm{E}}^{\square} \cdot \mathbf{1}_{x\times x}\right) \otimes \left(\frac{y}{y} \cdot \mathbf{1}_{1\times y}\right) = \left(\mathbf{V}_{\mathrm{E}}^{\square} - \mathbf{0}_{(x-1)\times x}\right) \otimes \mathbf{1}_{1\times y} \\
&= \mathbf{V}_{\mathrm{E}}^{\square} \otimes \mathbf{1}_{1\times y} = \mathbf{V}_{\mathrm{E}},
\end{aligned}
$$

where the expression highlighted in blue takes the sums of the rows of the matrix $\mathbf{V}_{\mathrm{E}}^{\square}$, which are of course all zero considering (A.11). This proves that $\mathbf{V}_{\mathrm{E}}$ is indeed an external left modal matrix of $\mathbf{D_m}$.

# B State-Space Models of MV Port Interconnections

In Section 5.3.5, the state-space models of MV-type ports were claimed to be the exact same than the state-space models of MC-type converters, whenever the letters P and S in the nomenclature were swapped. Indeed, it was proven in Section 5.3.5 that the $x\mathrm{S}y\mathrm{P}$ interconnection of MV-type ports without ideal current source yields the same state-space matrices as the $x\mathrm{P}y\mathrm{S}$ interconnection of MC-type ports without ideal voltage source. However, the duality between the state-space models of the remaining interconnection variants has yet to be proven, which is done in the following sections.

## B.1 xSyP Interconnection of MV Ports with Ideal Current Source

In the following, it has to be shown that the $x\mathrm{S}y\mathrm{P}$ interconnection of MV-type ports with ideal current source, as shown in Fig. B.1, yields the same state-space matrices as the $x\mathrm{P}y\mathrm{S}$ interconnection of MC-type ports with ideal voltage source, which have been derived in Section 5.3.2.

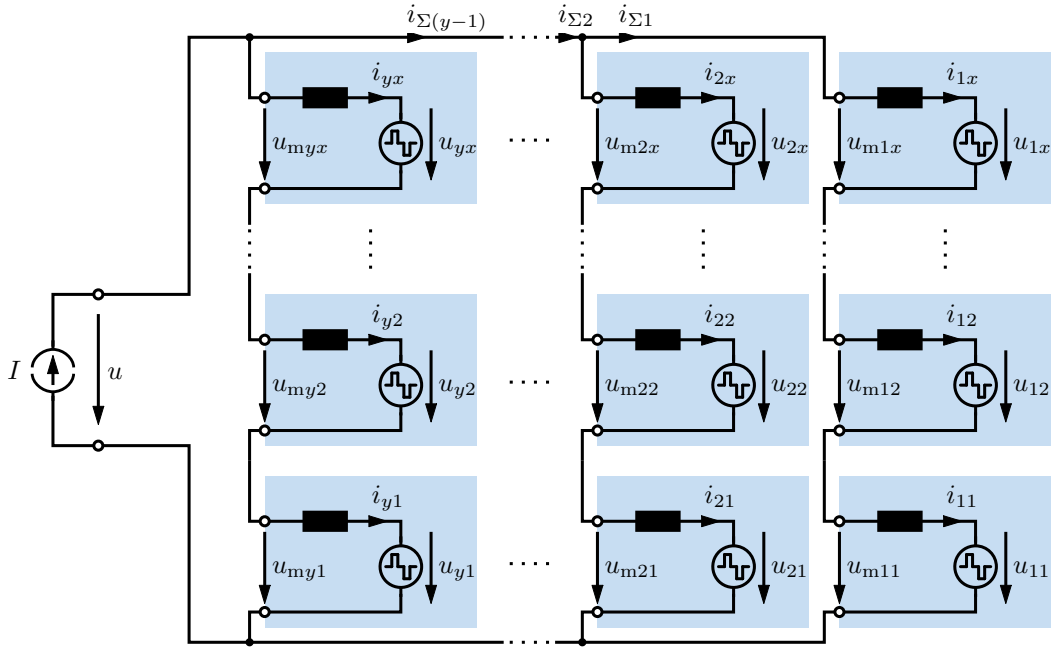



Figure B.1: $x\mathrm{S}y\mathrm{P}$ interconnection of MV-type ports with ideal current source

Since the ideal currents source reduces the number of state variables by one compared to the case without ideal current source, new state variables have to be found. For full equivalence with the reference MC-port case, an analogous definition to the midpoint voltages has to be used. Hence, accumulated currents $i_\Sigma$ are defined as follows, which are

also denoted in Fig. B.1:

$$i_{\Sigma p} := \sum_{r=1}^{p} i_r \quad \text{for all} \quad p = 1 \ldots (y-1). \tag{B.1}$$

These accumulated currents are arranged in the new state vector as follows:

$$\vec{x} = \begin{pmatrix} i_{\Sigma 1} & i_{\Sigma 2} & \ldots & i_{\Sigma(y-1)} \end{pmatrix}^{\mathrm{T}}. \tag{B.2}$$

The definitions of the manipulated input vector and the output vector, however, remain as given in (5.70).

Naturally, the basic equations of this interconnection developed in (5.71), (5.72), (5.73), and (5.74) still remain valid; only an expression for the terminal voltage $u$ has to be found, as it is not a disturbance anymore, but defined by all MV-type ports together. For this purpose, all currents from (5.73) are added together, exploiting the fact that the current source keeps the overall current constant:

$$\begin{aligned} \sum_{p=1}^{y} L\frac{\mathrm{d}i_p}{\mathrm{d}t} = L\frac{\mathrm{d}}{\mathrm{d}t}\left(\sum_{p=1}^{y} i_p\right) = L\frac{\mathrm{d}I}{\mathrm{d}t} = 0 = \frac{y \cdot u}{x} - \frac{1}{x}\sum_{p=1}^{y}\sum_{q=1}^{x} u_{pq} \\ \Rightarrow u = \frac{1}{y}\sum_{p=1}^{y}\sum_{q=1}^{x} u_{pq}. \end{aligned} \tag{B.3}$$

Insisting on the duality between voltages and currents in the MC and MV cases, the terminal voltage $u$ could legitimately be called CM voltage because it defines the power transfer of the interconnected port.

To obtain the system equations governing the matrix $\mathbf{B_m}$ (while the disturbance input matrix does not exist), the definition of the accumulated currents (B.1) and the found expression for the voltage $u$ (B.3) have to be inserted into (5.73), giving

$$\begin{aligned} L\frac{\mathrm{d}i_{\Sigma p}}{\mathrm{d}t} &= \frac{p \cdot u}{x} - \frac{1}{x}\sum_{r=1}^{p}\sum_{q=1}^{x} u_{rq} \overset{(B.3)}{=} \frac{p}{n}\sum_{r=1}^{y}\sum_{q=1}^{x} u_{rq} - \frac{1}{x}\sum_{r=1}^{p}\sum_{q=1}^{x} u_{rq} \\ &= \frac{p}{n}\sum_{r=p+1}^{y}\sum_{q=1}^{x} u_{rq} - \frac{y-p}{n}\sum_{r=1}^{p}\sum_{q=1}^{x} u_{rq} \quad \text{for all} \quad p = 1 \ldots (y-1). \end{aligned} \tag{B.4}$$

The same can be done to obtain the system equations governing the matrix $\mathbf{D_m}$ (the disturbance feed-through matrix does not exist) by inserting (B.3) into (5.74):

$$u_{\mathrm{m}pq} = u_{pq} - \frac{1}{x}\sum_{r=1}^{x} u_{pr} + \frac{1}{n}\sum_{r=1}^{y}\sum_{o=1}^{x} u_{ro} \quad \text{for all} \;\; p = 1 \ldots y \;\; \text{and} \;\; q = 1 \ldots x. \tag{B.5}$$

Equation (B.4) defines the matrix $\mathbf{B_m}$, however it is equivalent to (5.37) from the case of the $x\mathrm{P}y\mathrm{S}$ interconnection of MC-type ports with ideal voltage source. Similarly, (B.5)

defines the matrix $\mathbf{D_m}$, however it is equivalent to (5.38) from the case of the $x$P$y$S interconnection of MC-type ports with ideal voltage source. Hence, the state-space matrices are proven to be equal for these two cases.

## B.2 yPxS Interconnection of MV Ports

In the following, it has to be shown that the $y$P$x$S interconnection of MV-type ports without ideal current source, as shown in Fig. B.2, yields the same state-space matrices as the $y$S$x$P interconnection of MC-type ports without ideal voltage source, which have been derived in Section 5.3.3.

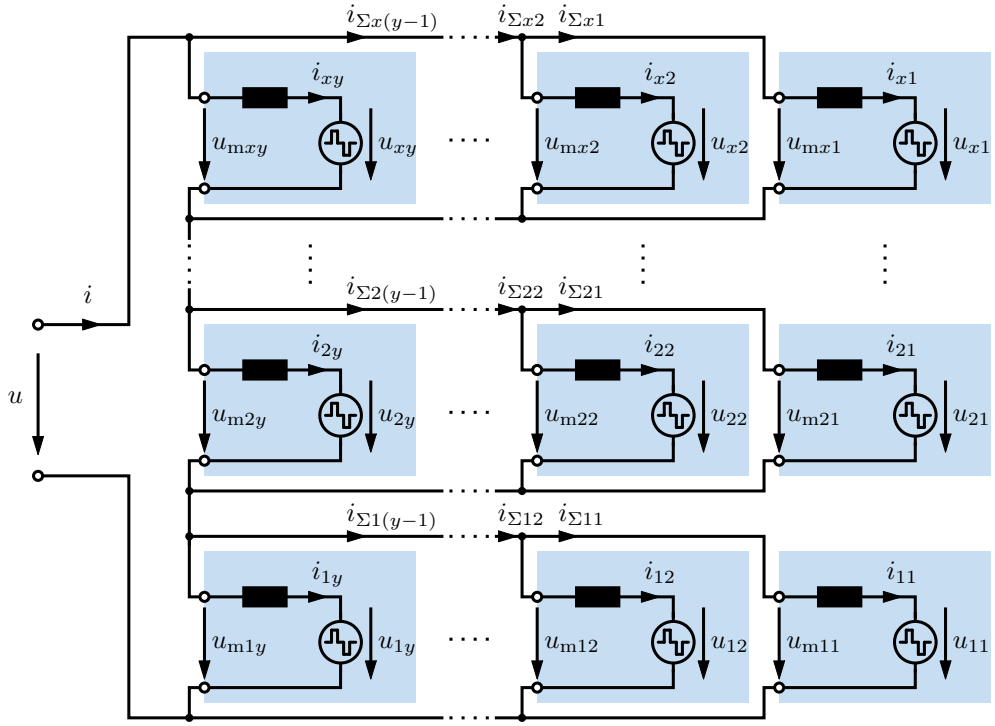



Figure B.2: $y$P$x$S interconnection of MV-type ports without ideal current source

In analogy with the reference interconnection of MC-type ports, the state variables are chosen the accumulated currents of each parallel-connected converter block, defined as

$$i_{\Sigma pq} := \sum_{r=1}^{q} i_{pr} \quad \text{for all} \quad p = 1 \ldots x \quad \text{and} \quad q = 1 \ldots (y-1), \tag{B.6}$$

and additionally the current $i$ at the terminals of the interconnected port. The states are arranged in the vector of the state variables as follows:

$$\vec{x} = \begin{pmatrix} i & i_{\Sigma 11} & i_{\Sigma 12} & \ldots & i_{\Sigma 1(y-1)} & \ldots & i_{\Sigma x1} & i_{\Sigma x2} & \ldots & i_{\Sigma x(y-1)} \end{pmatrix}^{\mathrm{T}}. \tag{B.7}$$

The definition of the manipulated input vector, the system output vector, and also the disturbance input, are unchanged compared to the $x\mathrm{S}y\mathrm{P}$ scenario as defined by (5.70). However, opposed to the $x\mathrm{S}y\mathrm{P}$ interconnections of MV-type ports, the coordinate system in Fig. B.2 has been changed, such that the second index counts those individual ports which are more closely connected, in this case, the parallel-connected ports. As no ideal current source is connected to the terminals of the interconnected converter port, the terminal voltage $u$ must be considered a disturbance input. One final simplification can be made because the measured voltages in each parallel connection of individual ports are equal, hence they are denoted

$$u_{\mathrm{m}p} := u_{\mathrm{m}p1} = u_{\mathrm{m}p2} = \ldots = u_{\mathrm{m}py} \quad \text{for all} \;\; p = 1 \ldots x. \tag{B.8}$$

With these definitions of the system variables in place, the fundamental equations of the $y\mathrm{P}x\mathrm{S}$ interconnection can be derived using KVL, KCL and the device equation for the inductors in the system:

$$L\frac{\mathrm{d}i_{pq}}{\mathrm{d}t} = u_{\mathrm{m}p} - u_{pq} \qquad \text{for all} \;\; p = 1 \ldots x \;\; \text{and} \;\; q = 1 \ldots y, \tag{B.9}$$

$$i = \sum_{q=1}^{y} i_{pq} \qquad \text{for all} \;\; p = 1 \ldots x, \tag{B.10}$$

$$u = \sum_{p=1}^{x} u_{\mathrm{m}p}. \tag{B.11}$$

When the equations from (B.9) are added along each parallel connection, it can be found that

$$\sum_{q=1}^{y} L\frac{\mathrm{d}i_{pq}}{\mathrm{d}t} = L\frac{\mathrm{d}}{\mathrm{d}t}\sum_{q=1}^{y} i_{pq} \overset{\text{(B.10)}}{=} L\frac{\mathrm{d}i}{\mathrm{d}t} = y \cdot u_{\mathrm{m}p} - \sum_{q=1}^{y} u_{pq} \quad \text{for all} \;\; p = 1 \ldots x. \tag{B.12}$$

The resulting equations from (B.12) can again be added along the series-connected converter blocks, obtaining

$$\sum_{p=1}^{x} L\frac{\mathrm{d}i}{\mathrm{d}t} = xL\frac{\mathrm{d}i}{\mathrm{d}t} = \sum_{p=1}^{x} y \cdot u_{\mathrm{m}p} - \sum_{p=1}^{x}\sum_{q=1}^{y} u_{pq} \overset{\text{(B.11)}}{=} y \cdot u - \sum_{p=1}^{x}\sum_{q=1}^{y} u_{pq}. \tag{B.13}$$

This equation can already be used in finding the single row of the matrices $\mathbf{B_m}$ and $\mathbf{B_d}$ that relates to the derivative of the dc-link terminal current $i$ as state variable. If the expressions for this derivative from (B.13) and (B.12) are equated, expressions for the

sensor voltages can be found, which define the matrices $\mathbf{D_m}$ and $\mathbf{D_d}$:

$$L\frac{\mathrm{d}i}{\mathrm{d}t} = y \cdot u_{\mathrm{mp}} - \sum_{q=1}^{y} u_{pq} = \frac{y}{x} \cdot u - \frac{1}{x}\sum_{p=1}^{x}\sum_{q=1}^{y} u_{pq}$$

$$\Rightarrow \quad u_{\mathrm{mp}} = \frac{1}{x} \cdot u + \frac{1}{y}\sum_{q=1}^{y} u_{pq} - \frac{1}{n}\sum_{r=1}^{x}\sum_{q=1}^{y} u_{rq} \quad \text{for all} \;\; p = 1 \ldots x. \tag{B.14}$$

The final missing part to construct the state-space matrices are the equations for the accumulated currents $i_{\Sigma pq}$, which can be found by applying the definition (B.6) to (B.9) and using the result for the measured voltages (B.14):

$$L\frac{\mathrm{d}i_{\Sigma pq}}{\mathrm{d}t} = q \cdot u_{\mathrm{mp}} - \sum_{o=1}^{q} u_{po} \overset{\text{(B.14)}}{=} \frac{q}{x} \cdot u + \frac{q}{y}\sum_{o=1}^{y} u_{po} - \sum_{o=1}^{q} u_{po} - \frac{q}{n}\sum_{r=1}^{x}\sum_{o=1}^{y} u_{ro} \tag{B.15}$$
$$\text{for all} \;\; p = 1 \ldots x \;\; \text{and} \;\; q = 1 \ldots (y-1).$$

Equation (B.15) defines the matrices $\mathbf{B_m}$ and $\mathbf{B_d}$, however it is equivalent to (5.54) from the case of the $y$S$x$P interconnection of MC-type ports without ideal voltage source. Similarly, (B.14) defines the matrices $\mathbf{D_m}$ and $\mathbf{D_d}$, however it is equivalent to (5.53) from the case of the $y$S$x$P interconnection of MC-type ports without ideal voltage source. Hence, the state-space matrices are proven to be equal for these two cases.

## B.3 yPxS Interconnection of MV Ports with Ideal Current Source

In the following, it has to be shown that the $y$P$x$S interconnection of MV-type ports with ideal current source, as shown in Fig. B.3, yields the same state-space matrices as the $y$S$x$P interconnection of MC-type ports with ideal voltage source, which have been derived in Section 5.3.4.

Connecting a voltage source to the $y$P$x$S interconnection simplifies the system equations, as now the interactions between all parallel-connected converter blocks are effectively demoved by the constant current, eliminating the current $i$ from the vector of the state variables. Hence, the state vectors is given by

$$\vec{x} = \begin{pmatrix} i_{\Sigma 11} & i_{\Sigma 12} & \ldots & i_{\Sigma 1(y-1)} & \ldots & i_{\Sigma x1} & i_{\Sigma x2} & \ldots & i_{\Sigma x(y-1)} \end{pmatrix}^{\mathrm{T}}. \tag{B.16}$$

The terminal voltage $u$ is again not a disturbance input, but jointly manipulated by all converters and directly measurable by the sensors because it is not linked to a system state anymore. Hence, neither a disturbance input vector $\vec{u}_{\mathrm{d}}$ nor the matrices $\mathbf{B_d}$ and $\mathbf{D_d}$ do exist.

The remaining equations have already been prepared in Appendix B.2, only the constant dc-link current $I$ has to be considered. Setting the derivative of the dc-link current $i$ in

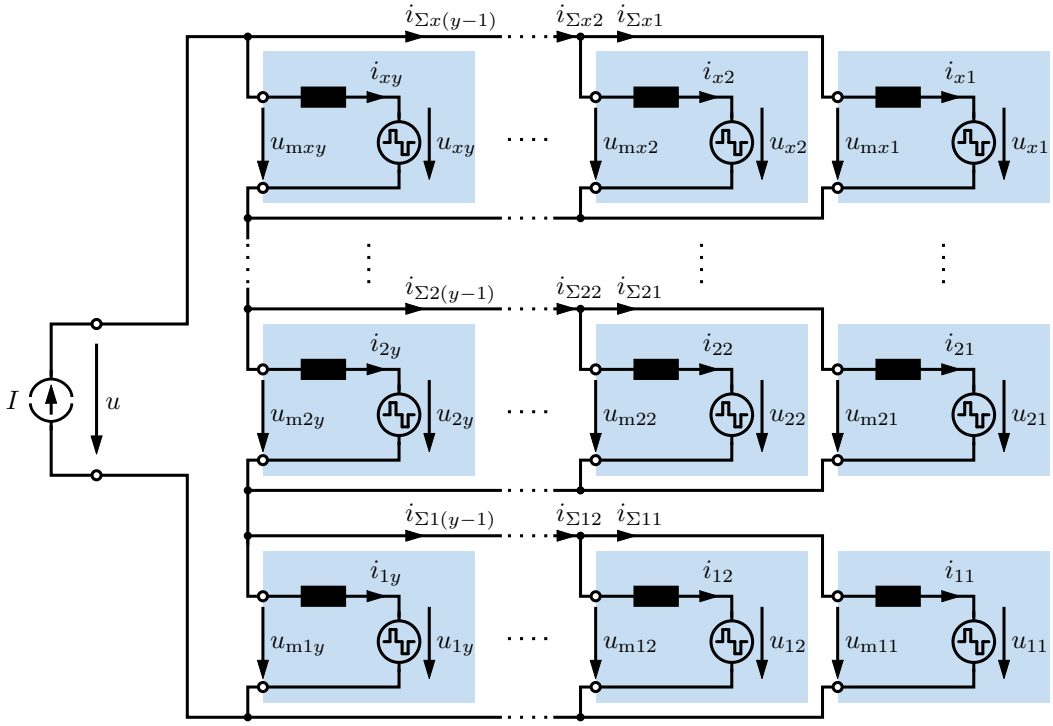



Figure B.3: $y\mathrm{P}x\mathrm{S}$ interconnection of MV-type ports with ideal current source

(B.13) to zero yields the following expression for the voltage $u$ at the terminals of the interconnected converter,

$$u = \frac{1}{y} \sum_{p=1}^{x} \sum_{q=1}^{y} u_{pq}, \tag{B.17}$$

indicating that this voltage is equal to the sum of the average voltages of all $x$ parallel-connected converter blocks. Using (B.17) in (B.14) yields an equation for the sensor currents,

$$u_{\mathrm{m}p} = \frac{1}{y} \sum_{q=1}^{y} u_{pq}. \tag{B.18}$$

Finally, inserting (B.18) into the left part of (B.15) gives an expression for the derivative of the accumulated currents,

$$L \frac{\mathrm{d}i_{\Sigma pq}}{\mathrm{d}t} = \frac{q}{y} \sum_{o=1}^{y} u_{po} - \sum_{o=1}^{q} u_{po} = \frac{q}{y} \sum_{o=q+1}^{y} u_{po} - \frac{y-q}{y} \sum_{o=1}^{q} u_{po}. \tag{B.19}$$

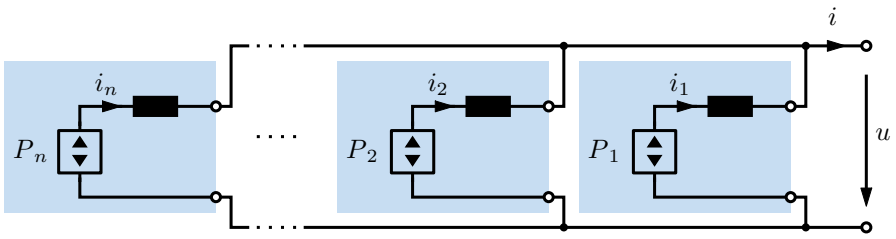
Equation (B.19) defines the matrix $\mathbf{B_m}$, however it is equivalent to (5.65) from the case of the $y\mathrm{S}x\mathrm{P}$ interconnection of MC-type ports with ideal voltage source. Similarly, (B.18) defines the matrix $\mathbf{D_m}$, however it is equivalent to (5.63) from the case of the $y\mathrm{S}x\mathrm{P}$ interconnection of MC-type ports with ideal voltage source. Hence, the state-space matrices are proven to be equal for these two cases.

# C Further Stability Analysis

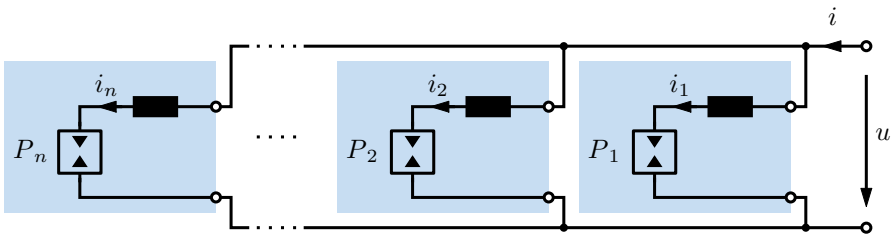
The following sections provide additional stability proofs for interconnections of uncontrolled ports, which are not shown in Section 5.4.3 for the sake of conciseness.

## C.1 Parallel-connected Ports with Series Inductor

In Section 5.4.3, the series connection of passive, uncontrolled ports with shunt capacitors has been analyzed with respect to its stability dependent on the direction of power. This section discusses the dual scenario, i.e., the parallel connection of passive, uncontrolled ports with series inductors. Figure C.1 shows this interconnection variant.




(a) With CPS




(b) With CPL

Figure C.1: Uncontrolled ports of $n$ parallel-connected PEBBs with series inductors considering both power flow directions

Following the step-by-step procedure from Section 5.4.3, the nonlinear state-space model of the system with CPS elements is derived, using the currents $i_p$ as states, the power sources $P_p$ as manipulated input, and the voltage $u$ as disturbance input:

$$L\frac{\mathrm{d}i_p}{\mathrm{d}t} = \frac{P_p}{i_p} - u \quad \text{for all} \quad p = 1 \dots n. \tag{C.1}$$

The inductances $L$ of the PEBBs are assumed equal. In the second step, the equilibrium point is found by setting the time derivative in (C.1) to zero, giving

$$i_{\mathrm{eq}p} = \frac{P_p}{u} \quad \text{for all} \quad p = 1 \dots n. \tag{C.2}$$

Defining $\Delta i_p$ as the current deviation from the equilibrium $i_{\mathrm{eq}p}$, the state-space model can be re-derived as

$$L\frac{\mathrm{d}\Delta i_p}{\mathrm{d}t} = \frac{P_p}{i_{\mathrm{eq}p} + \Delta i_p} - u \quad \text{for all} \;\; p = 1 \ldots n. \tag{C.3}$$

The LYAPUNOV function in step 4 is now defined as

$$V(\Delta i_1, \ldots, \Delta i_n) = \sum_{p=1}^{n} \frac{1}{2} L \Delta i_p^2, \tag{C.4}$$

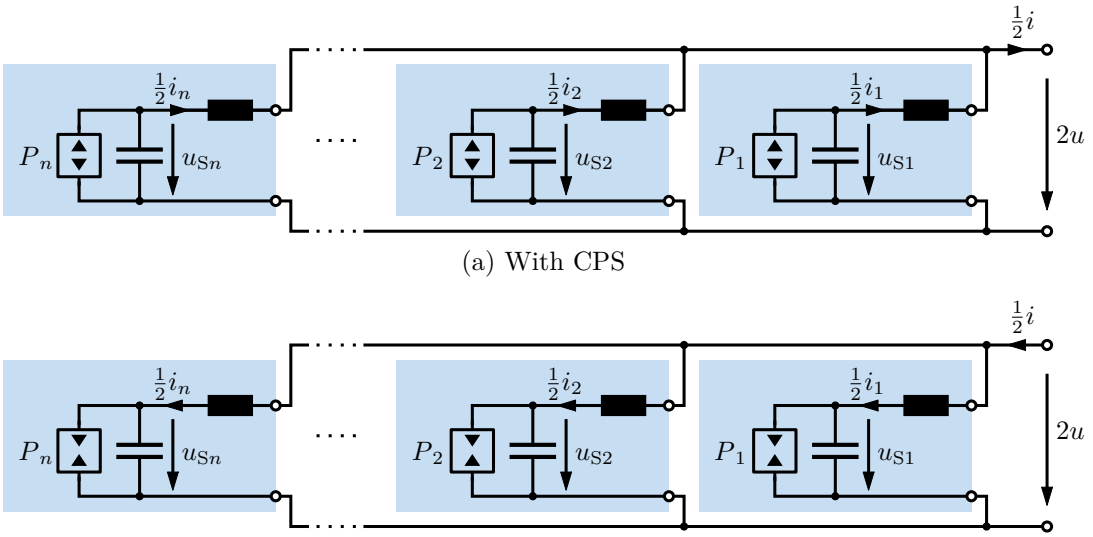
where the parameters of the exponential stability criterion (3.10) from Section 3.1.3 are given as $\beta = 2$ and $\delta_2 = {}^1\!/_2 L$. The time derivative of the LYAPUNOV function can be computed as follows:

$$\begin{aligned}
\frac{\mathrm{d}V}{\mathrm{d}t} &= \frac{\mathrm{d}}{\mathrm{d}t} \sum_{p=1}^{n} \frac{1}{2} L \Delta i_p^2 = \sum_{p=1}^{n} L \Delta i_p \cdot \frac{\mathrm{d}\Delta i_p}{\mathrm{d}t} \overset{(C.3)}{=} \sum_{p=1}^{n} \Delta i_p \cdot \left( \frac{P_p}{i_{\mathrm{eq}p} + \Delta i_p} - u \right) \\
&= \sum_{p=1}^{n} \frac{P_p \Delta i_p - \Delta i_p \cdot u (i_{\mathrm{eq}p} + \Delta i_p)}{i_{\mathrm{eq}p} + \Delta i_p} \overset{(C.2)}{=} -\sum_{p=1}^{n} \frac{u \Delta i_p^2}{i_p} \\
&\leq -\frac{u}{L \cdot \max\limits_{p} \{i_{\mathrm{max}p}\}} \cdot 2 \cdot \sum_{p=1}^{n} \frac{1}{2} L \Delta i_p^2 =: -\alpha\beta V.
\end{aligned} \tag{C.5}$$

Again, this proves exponential stability for the interconnection from Fig. C.1a according to (3.11). If the case with reversed power direction from Fig. C.1b using CPL elements is assumed, $P_p$ and $i_p$ all change signs, which makes the derivative of the LYAPUNOV function always positive, proving instability. It has to be noted explicitly that the power delivery $P_p$ by each PEBB does not necessarily have to be equal, i.e., power sharing is not a necessary condition for stability.

## C.2 Parallel-connected Current-Fed Ports

In the following, the stability of the parallel interconnection of uncontrolled current-fed ports is analyzed. This interconnection is used in the experimental validation in Section 6.2. Figure C.2 shows the equivalent circuits of this interconnection for both directions of power flow, which are based on the equivalent circuit developed in Fig. 3.9 in Section 3.3.3. Due to the half bridges switching at 50 %, the dc-link voltage is twice the terminal voltage and the output current is twice the dc-link current. Hence, the quantities have to be scaled accordingly when developing an equivalent circuit from the perspective of the dc link. Additionally, the equivalent inductance $L_{\mathrm{b,eq}}$ according to (3.49) has to be used. All equivalent inductances as well as all dc-link capacitances $C$ are assumed to be equal for all PEBBs.




(a) With CPS

(b) With CPL

Figure C.2: Uncontrolled current-fed ports of $n$ parallel-connected PEBBs considering both power flow directions

Following the step-by-step procedure from Section 5.4.3, the nonlinear state-space model of the system with CPS elements is derived, using the weighted currents $\frac{1}{2}i_p$ and the dc-link voltages $u_{Sp}$ as states, the power sources $P_p$ as manipulated input, and the weighted voltage $2u$ as disturbance input:

$$\begin{aligned} C\frac{\mathrm{d}u_{Sp}}{\mathrm{d}t} &= \frac{P_p}{u_{Sp}} - \frac{1}{2}i_p \quad \text{for all} \quad p = 1 \dots n, \\ L_{b,eq}\frac{\mathrm{d}\left(\frac{1}{2}i_p\right)}{\mathrm{d}t} &= u_{Sp} - 2u \quad \text{for all} \quad p = 1 \dots n. \end{aligned} \tag{C.6}$$

In the second step, the values is $u_{Sp}$ and $\frac{1}{2}i_p$ in equilibrium need to be found. They are denoted $u_{eqp}$ and $\frac{1}{2}i_{eqp}$, respectively, and obtained by setting the time derivatives in (C.6) to zero, giving

$$\begin{aligned} u_{eqp} &= 2u \quad \text{for all} \quad p = 1 \dots n, \\ \frac{1}{2}i_{eqp} &= \frac{P_p}{2u} \quad \text{for all} \quad p = 1 \dots n. \end{aligned} \tag{C.7}$$

Defining the deviations from the equilibrium point as follows,

$$\begin{aligned} \Delta u_p &:= u_{Sp} - u_{eqp} = u_{Sp} - 2u \quad \text{for all} \quad p = 1 \dots n, \\ \frac{1}{2}\Delta i_p &:= \frac{1}{2}i_p - \frac{1}{2}i_{eqp} = \frac{1}{2}i_p - \frac{P_p}{4u} \quad \text{for all} \quad p = 1 \dots n, \end{aligned} \tag{C.8}$$

the state-space model can be re-derived as

$$\begin{aligned} C\frac{\mathrm{d}\Delta u_p}{\mathrm{d}t} &= \frac{P_p}{2u+\Delta u_p} - \frac{1}{2}i_{\mathrm{eq}p} - \frac{1}{2}\Delta i_p \quad \text{for all } \; p = 1\ldots n, \\ L_{\mathrm{b,eq}}\frac{\mathrm{d}\left(\frac{1}{2}\Delta i_p\right)}{\mathrm{d}t} &= \Delta u_p \qquad\qquad\qquad\qquad\quad \text{for all } \; p = 1\ldots n. \end{aligned} \tag{C.9}$$

The LYAPUNOV function in step 4 is now defined as

$$V\left(\Delta u_1,\ldots,\Delta u_n,\, \tfrac{1}{2}\Delta i_1,\ldots,\tfrac{1}{2}\Delta i_n\right) = \sum_{p=1}^{n}\left(\frac{1}{2}C\Delta u_p^2 + \frac{1}{2}L_{\mathrm{b,eq}}\left(\frac{1}{2}\Delta i_p\right)^2\right), \tag{C.10}$$

and its time derivative can be computed as follows:

$$\begin{aligned} \frac{\mathrm{d}V}{\mathrm{d}t} &= \sum_{p=1}^{n}\left(C\Delta u_p\cdot\frac{\mathrm{d}\Delta u_p}{\mathrm{d}t} + L_{\mathrm{b,eq}}\left(\frac{1}{2}\Delta i_p\right)\cdot\frac{\mathrm{d}\left(\frac{1}{2}\Delta i_p\right)}{\mathrm{d}t}\right) \\ &\overset{(C.9)}{=} \sum_{p=1}^{n}\left(\frac{P_p\Delta u_p}{2u+\Delta u_p} - \frac{1}{2}i_{\mathrm{eq}p}\Delta u_p - \frac{1}{2}\Delta i_p\Delta u_p + \frac{1}{2}\Delta i_p\Delta u_p\right) \\ &\overset{(C.8)}{=} \sum_{p=1}^{n}\frac{P_p\Delta u_p - u\cdot i_{\mathrm{eq}p}\Delta u_p - \frac{1}{2}i_{\mathrm{eq}p}\cdot\Delta u_p^2}{u_{\mathrm{S}p}} \\ &\overset{(C.7)}{=} -\sum_{p=1}^{n}\frac{\frac{1}{2}i_{\mathrm{eq}p}\cdot\Delta u_p^2}{u_{\mathrm{S}p}} < 0. \end{aligned} \tag{C.11}$$

If CPS elements are in the circuit that all deliver nonzero power, all currents $i_{\mathrm{eq}p}$ are strictly greater than zero; also the dc-link voltages $u_{\mathrm{S}p}$ are assumed strictly positive. Under these circumstances, (C.11) is strictly negative, proving asymptotic stability of the parallel current-fed port interconnection from Fig. C.2a according to (3.8). If the case with reversed power direction from Fig. C.2b using CPL elements is assumed, $\frac{1}{2}i_{\mathrm{eq}p}$ all change signs, which makes the derivative of the LYAPUNOV function strictly positive, proving instability. Again, it has to be noted explicitly that the power delivery $P_p$ by each PEBB does not necessarily have to be equal, i.e., power sharing is not a necessary condition for stability.

# D Further Experimental Results

The validation of the decoupled control methodology has been validated for all eight interconnection variants from Chapter 5. However, Section 6.2 only presented one measurement for both MC-type and MV-type port interconnections. The following sections present measurements on the remaining six interconnections. For all interconnections, $x = y = 2$ is selected.

## D.1 xPyS Interconnection of MC Ports

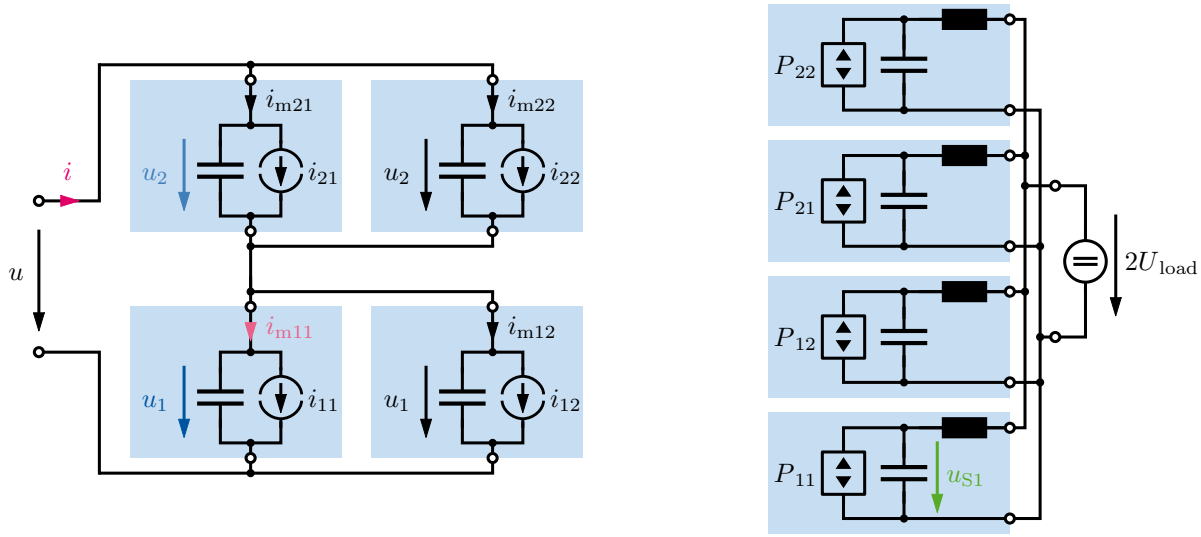
This section addresses the validation of the $x$P$y$S interconnection of MC-type ports. Hence, the decoupling technique is applied to the primary side. Figure D.1 shows the equivalent circuit of the resulting interconnection; all measured quantities are highlighted in color. The FPGA is programmed to activate the open-loop current control for each PEBB to implement MC-type port behavior. In turn, the MCU performs the decoupled control of the state variables and external eigenvectors. Table D.1 lists the transformation matrix, the internal and external eigenvectors, denotes which variables they influence, and how their respective control loop is designed.

Table D.1: Transformation matrix and tuning of the decoupled control of the MC-type, 2P2S-interconnected primary-side port without ideal voltage source

| Transformation matrix | Eigenvector type | Influencing the variable | MCU control | $f_{\mathrm{b,p}}$ | $f_{\mathrm{b,i}}$ |
|---|---|---|---|---|---|
| $\mathbf{T} = \begin{pmatrix} -\frac{1}{2} & -\frac{1}{2} & 0 & 0 \\ 0 & 0 & -\frac{1}{2} & -\frac{1}{2} \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \end{pmatrix}$ | internal | $u_1$ | closed-loop | 1 kHz | 250 Hz |
| | internal | $u_2$ | closed-loop | 1 kHz | 250 Hz |
| | external | $i_{\mathrm{DM1}}$ | open-loop | — | — |
| | external | $i_{\mathrm{DM2}}$ | open-loop | — | — |

Since this interconnection relies on the absence of an ideal voltage source, a bidirectional power supply is programmed to deliver a constant current of $i = 2\,\mathrm{A}$ and connected to the primary side. On the secondary side, all PEBBs are connected in parallel, and a bidirectional power supply provides a constant voltage of 15 V. Initially, both state variable references $u_1^*$ and $u_2^*$ are set to 30 V, ensuring a primary-side dc-link voltage of 60 V. The initial DM current references are set to zero.

Figure D.2 shows the measurement results. The initial references are reached for $t < 0\,\mathrm{ms}$. At 0 ms, both state variable references are decreased to 25 V. Between $10\,\mathrm{ms} \leq t < 20\,\mathrm{ms}$, both DM current references are temporarily set to 2 A. Finally, at 30 ms, the voltage reference $u_1^*$ is decreased to 20 V, while the voltage reference $u_2^*$ is increased to 30 V. It can be seen that all control references are precisely tracked with negligible interactions. An undershoot in the voltage control after 0 ms is attributed to the transient in the terminal current $i$, which acts as a disturbance input.




(a) Controlled primary side (b) Uncontrolled secondary side

Figure D.1: Equivalent circuit of the dc-dc converter platform with the decoupled control applied to the primary-side 2P2S interconnection of MC-type converter ports without ideal voltage source

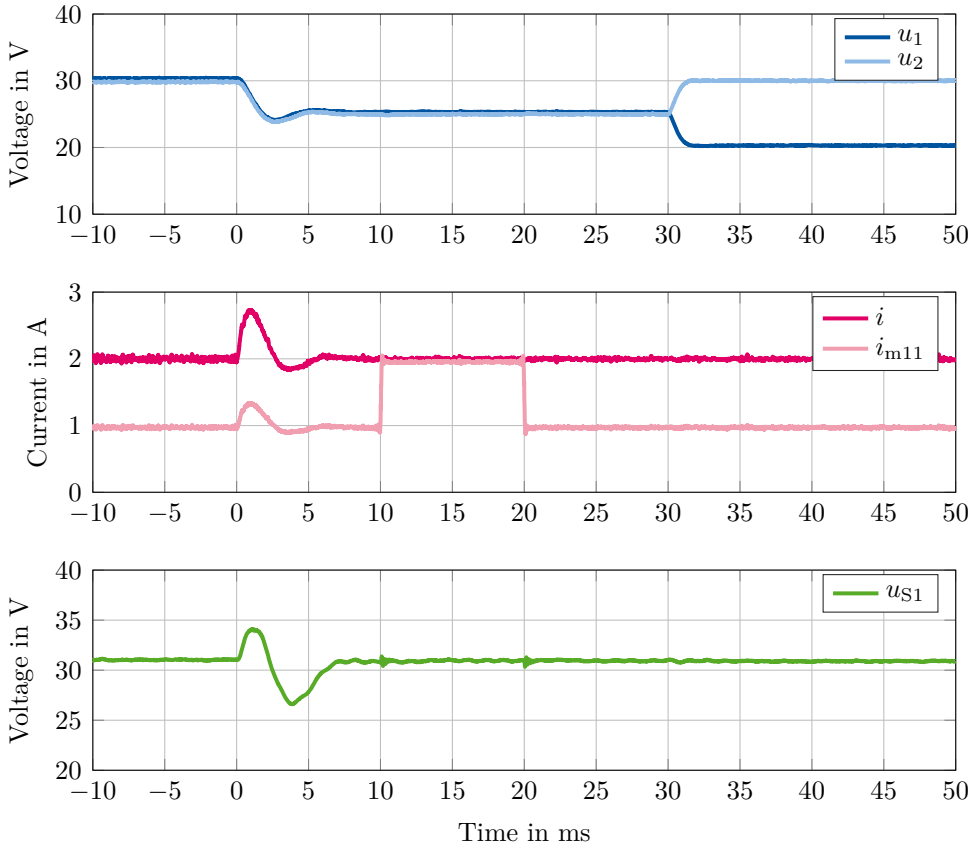



Figure D.2: Measurement of the decoupled control of the MC-type, 2P2S-interconnected primary-side port without ideal voltage source

## D.2 ySxP Interconnection of MC Ports

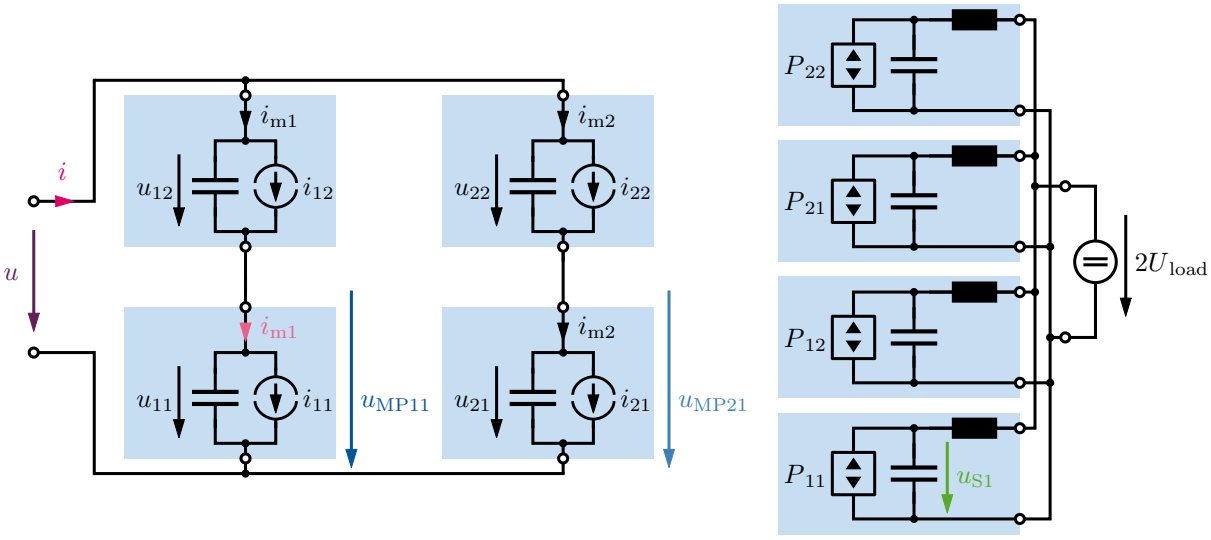
This section addresses the validation of the $y\mathrm{S}x\mathrm{P}$ interconnection of MC-type ports. Hence, the decoupling technique is applied to the primary side. Figure D.3 shows the equivalent circuit of the resulting interconnection; all measured quantities are highlighted in color. The FPGA is programmed to activate the open-loop current control for each PEBB to implement MC-type port behavior. In turn, the MCU performs the decoupled control of the state variables and external eigenvectors. Table D.2 lists the transformation matrix, the internal and external eigenvectors, denotes which variables they influence, and how their respective control loop is designed.

Table D.2: Transformation matrix and tuning of the decoupled control of the MC-type, 2S2P-interconnected primary-side port without ideal voltage source

| Transformation matrix | Eigenvector type | Influencing the variable | MCU control | $f_{\mathrm{b,p}}$ | $f_{\mathrm{b,i}}$ |
|---|---|---|---|---|---|
| $\mathbf{T} = \begin{pmatrix} -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{3}{4} & \frac{1}{4} & -\frac{1}{4} & -\frac{1}{4} \\ -\frac{1}{4} & -\frac{1}{4} & -\frac{3}{4} & \frac{1}{4} \\ \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \end{pmatrix}$ | internal | $u$ | closed-loop | 1 kHz | 250 Hz |
| | internal | $u_{\mathrm{MP11}}$ | closed-loop | 2 kHz | 500 Hz |
| | internal | $u_{\mathrm{MP21}}$ | closed-loop | 2 kHz | 500 Hz |
| | external | $i_{\mathrm{DM}}$ | open-loop | — | — |

Since this interconnection relies on the absence of an ideal voltage source, a bidirectional power supply that is programmed to deliver a constant current of $i = 2\,\mathrm{A}$ is connected to the primary side. On the secondary side, all PEBBs are connected in parallel, and a bidirectional power supply is used as load, setting a constant voltage of 15 V. Initially, the dc-link voltage reference $u^*$ is set to 60 V, while both midpoint-voltage references $u^*_{\mathrm{MP11}}$ and $u^*_{\mathrm{MP21}}$ are set to 30 V. The initial DM current reference is set to zero.

Figure D.4 shows the measurement results. The initial references are reached for $t < 0\,\mathrm{ms}$. At 0 ms, the dc-link voltage reference $u^*$ is decreased to 55 V. Between $10\,\mathrm{ms} \leq t < 20\,\mathrm{ms}$, the DM current reference is temporarily set to 2 A. Between $30\,\mathrm{ms} \leq t < 40\,\mathrm{ms}$, the midpoint voltage reference $u^*_{\mathrm{MP11}}$ is increased to 35 V, while the midpoint voltage reference $u^*_{\mathrm{MP21}}$ is decreased to 25 V. It can be seen that all control references are precisely tracked with negligible interactions. An undershoot in the dc-link voltage control after 0 ms is attributed to the transient in the terminal current $i$, which acts as a disturbance input.




(a) Controlled primary side (b) Uncontrolled secondary side

Figure D.3: Equivalent circuit of the dc-dc converter platform with the decoupled control applied to the primary-side 2S2P interconnection of MC-type converter ports without ideal voltage source

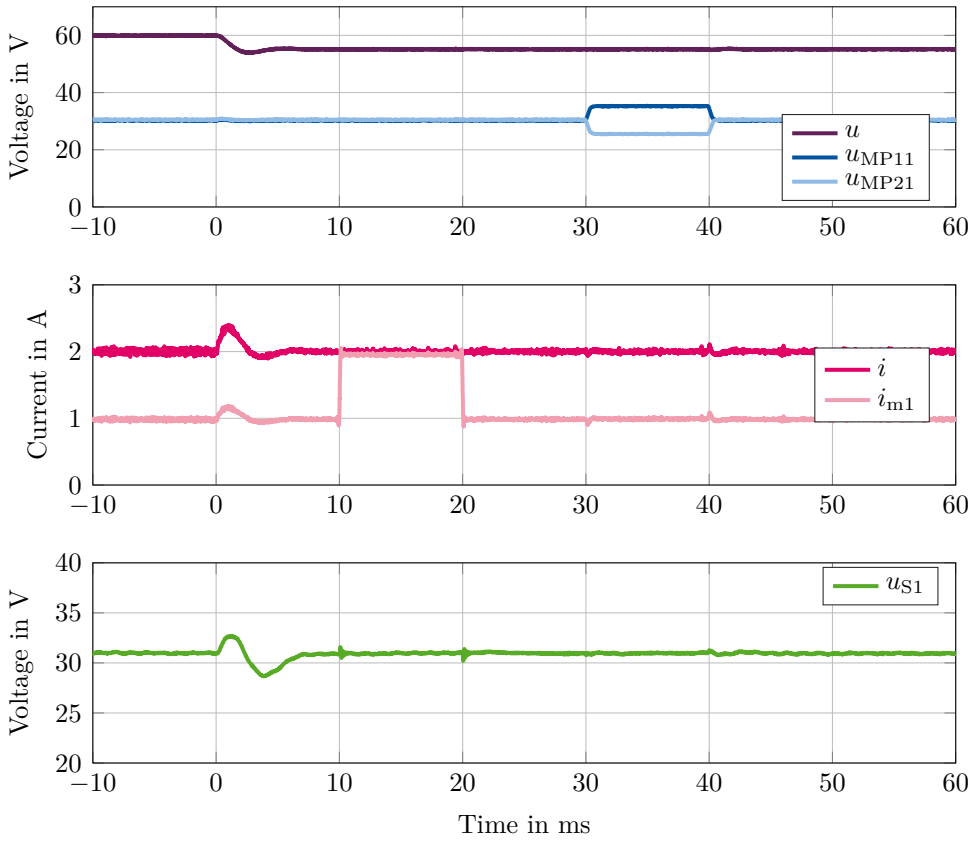



Figure D.4: Measurement of the decoupled control of the MC-type, 2S2P-interconnected primary-side port without ideal voltage source

## D.3 ySxP Interconnection of MC Ports with Ideal Voltage Source

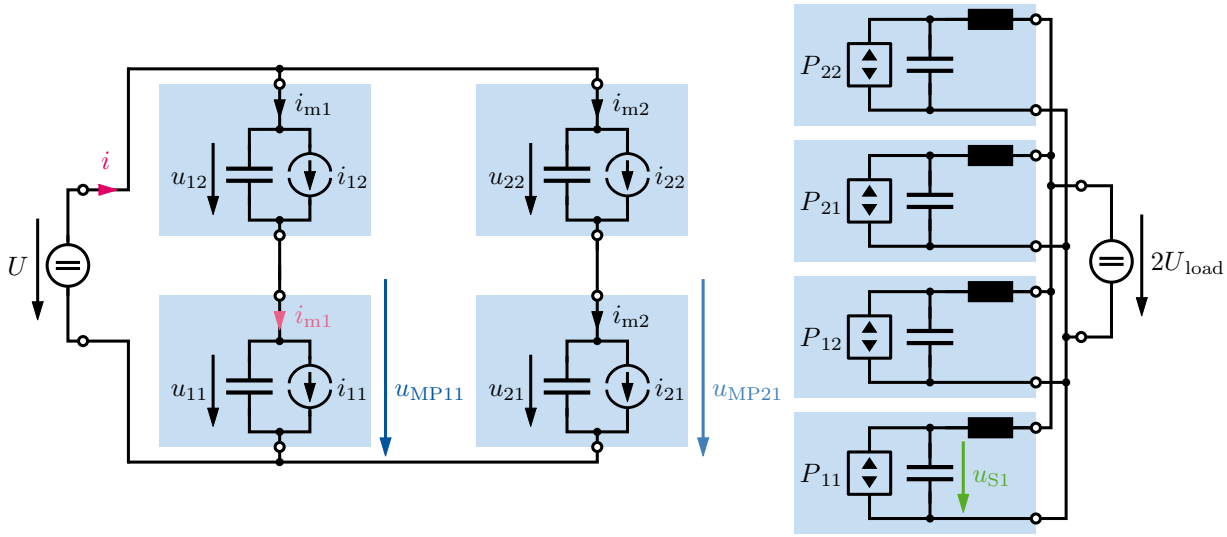
This section addresses the validation of the $y\mathrm{S}x\mathrm{P}$ interconnection of MC-type ports with ideal voltage source. Hence, the decoupling technique is applied to the primary side. Figure D.5 shows the equivalent circuit of the resulting interconnection; all measured quantities are highlighted in color. The FPGA is programmed to activate the open-loop current control for each PEBB to implement MC-type port behavior. In turn, the MCU performs the decoupled control of the state variables and external eigenvectors. Table D.3 lists the transformation matrix, the internal and external eigenvectors, denotes which variables they influence, and how their respective control loop is designed.

Table D.3: Transformation matrix and tuning of the decoupled control of the MC-type, 2S2P-interconnected primary-side port with ideal voltage source

| Transformation matrix | Eigenvector type | Influencing the variable | MCU control | $f_{\mathrm{b,p}}$ | $f_{\mathrm{b,i}}$ |
|---|---|---|---|---|---|
| $\mathbf{T} = \begin{pmatrix} -\frac{1}{2} & \frac{1}{2} & 0 & 0 \\ 0 & 0 & -\frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \end{pmatrix}$ | internal | $u_{\mathrm{MP11}}$ | closed-loop | 2 kHz | 500 Hz |
| | internal | $u_{\mathrm{MP21}}$ | closed-loop | 2 kHz | 500 Hz |
| | external | $i$ | open-loop | — | — |
| | external | $i_{\mathrm{DM}}$ | open-loop | — | — |

On the primary side, a constant dc-link voltage of 60 V is provided by a unidirectional power supply. On the secondary side, all PEBBs are connected in parallel, and a bidirectional power supply is used as load, setting a constant voltage of 15 V. Initially, both midpoint voltage references $u^*_{\mathrm{MP11}}$ and $u^*_{\mathrm{MP21}}$ are set to 30 V. The initial terminal current reference $i^*$ is set to 2 A, while the DM current reference is set to zero.

Figure D.6 shows the measurement results. The initial references are reached for $t < 0\,\mathrm{ms}$. Between $0\,\mathrm{ms} \leq t < 40\,\mathrm{ms}$, the terminal current reference $i^*$ is temporarily set to 4 A. Between $10\,\mathrm{ms} \leq t < 20\,\mathrm{ms}$, the DM current reference is temporarily increased to 2 A. Finally, between $30\,\mathrm{ms} \leq t < 50\,\mathrm{ms}$, the midpoint voltage reference $u^*_{\mathrm{MP11}}$ is increased to 35 V, while the midpoint voltage reference $u^*_{\mathrm{MP21}}$ is decreased to 25 V. It can be seen that all control references are precisely tracked with negligible interactions. As discussed in Section 6.2, due to the open-loop control of the port currents, the current references are not always tracked perfectly.




(a) Controlled primary side (b) Uncontrolled secondary side

Figure D.5: Equivalent circuit of the dc-dc converter platform with the decoupled control applied to the primary-side 2S2P interconnection of MC-type converter ports with ideal voltage source

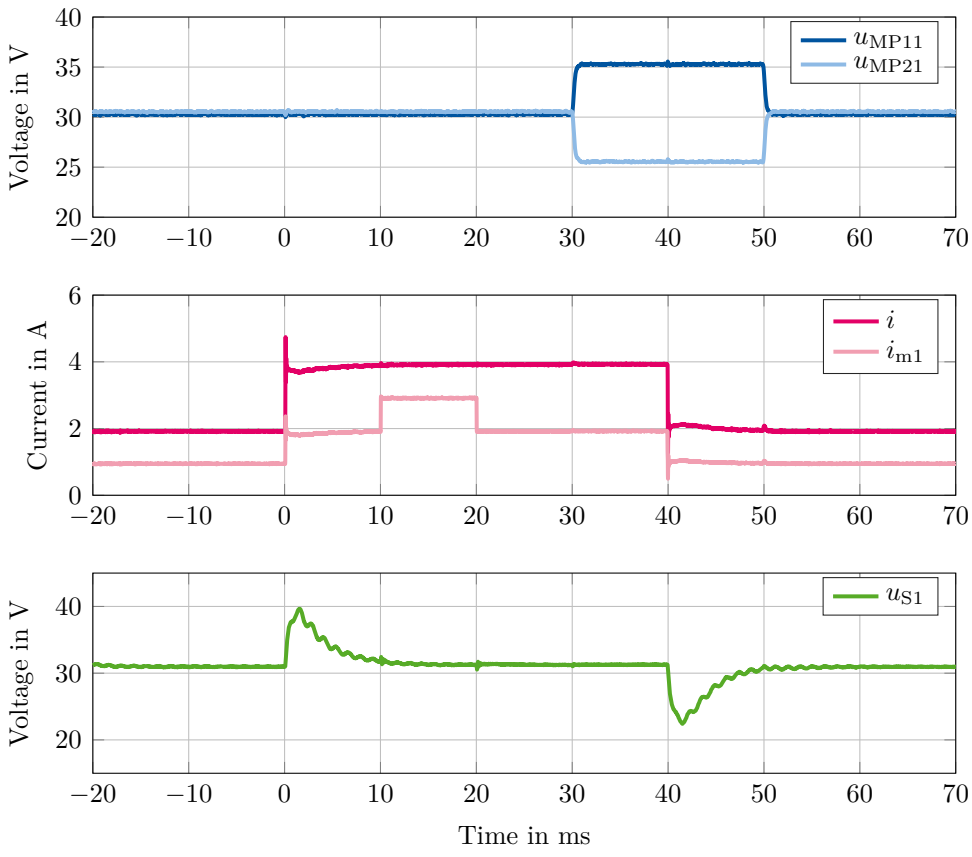



Figure D.6: Measurement of the decoupled control of the MC-type, 2S2P-interconnected primary-side port with ideal voltage source

## D.4 xSyP Interconnection of MV Ports

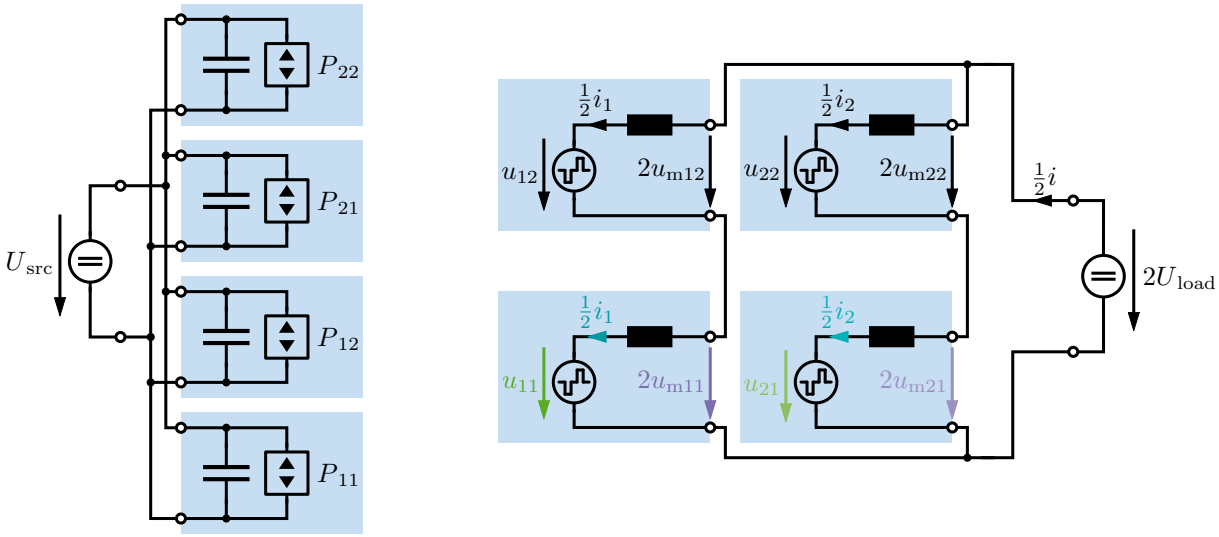
This section addresses the validation of the $x\mathrm{S}y\mathrm{P}$ interconnection of MV-type ports. Hence, the decoupling technique is applied to the secondary side. Figure D.7 shows the equivalent circuit of the resulting interconnection; all measured quantities are highlighted in color. The FPGA is programmed to activate the closed-loop secondary-side dc-link voltage control for each PEBB to implement MV-type port behavior as described in Section 6.2.3.3. In turn, the MCU performs the decoupled control of the state variables and external eigenvectors. Table D.4 lists the transformation matrix, the internal and external eigenvectors, denotes which variables they influence, and how their respective control loop is designed.

Table D.4: Transformation matrix and tuning of the decoupled control of the MV-type, 2S2P-interconnected secondary-side port without ideal current source

| Transformation matrix | Eigenvector type | Influencing the variable | MCU control | $f_{\mathrm{b,p}}$ | $f_{\mathrm{b,i}}$ |
|---|---|---|---|---|---|
| $\mathbf{T} = \begin{pmatrix} -\frac{1}{2} & -\frac{1}{2} & 0 & 0 \\ 0 & 0 & -\frac{1}{2} & -\frac{1}{2} \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \end{pmatrix}$ | internal | $\frac{1}{2}i_1$ | closed-loop | 1 kHz | 250 Hz |
| | internal | $\frac{1}{2}i_2$ | closed-loop | 1 kHz | 250 Hz |
| | external | $u_{\mathrm{DM1}}$ | open-loop | — | — |
| | external | $u_{\mathrm{DM2}}$ | open-loop | — | — |

On the secondary side, a constant dc-link voltage of 30 V is provided by a unidirectional power supply. On the primary side, all PEBBs are connected in parallel, and a bidirectional power supply is used as load, setting a constant voltage of 30 V. Initially, both current references $\frac{1}{2}i_1^*$ and $\frac{1}{2}i_2^*$ are set to 1 A, hence currents of 2 A are measured due to the current-fed port property. In turn, both DM voltage references are set to zero.

Figure D.8 shows the measurement results. The initial references are reached for $t < 0$ ms. At 0 ms, both current references $\frac{1}{2}i_1^*$ and $\frac{1}{2}i_2^*$ are increased to 2 A, which results in measurable currents of 4 A. Additionally, between 80 ms $\leq t <$ 160 ms, the DM voltage references are changed by $\pm$8 V in the two series-connected branches. It can be seen that all control references are precisely tracked with negligible interactions. As discussed in Section 6.2, due to the limited bandwidth of the closed-loop current control in the MCU, there are some deviations in the tracking of the state variable references.




(a) Uncontrolled primary side (b) Controlled secondary side

Figure D.7: Equivalent circuit of the dc-dc converter platform with the decoupled control applied to the secondary-side 2S2P interconnection of MV-type converter ports without ideal current source

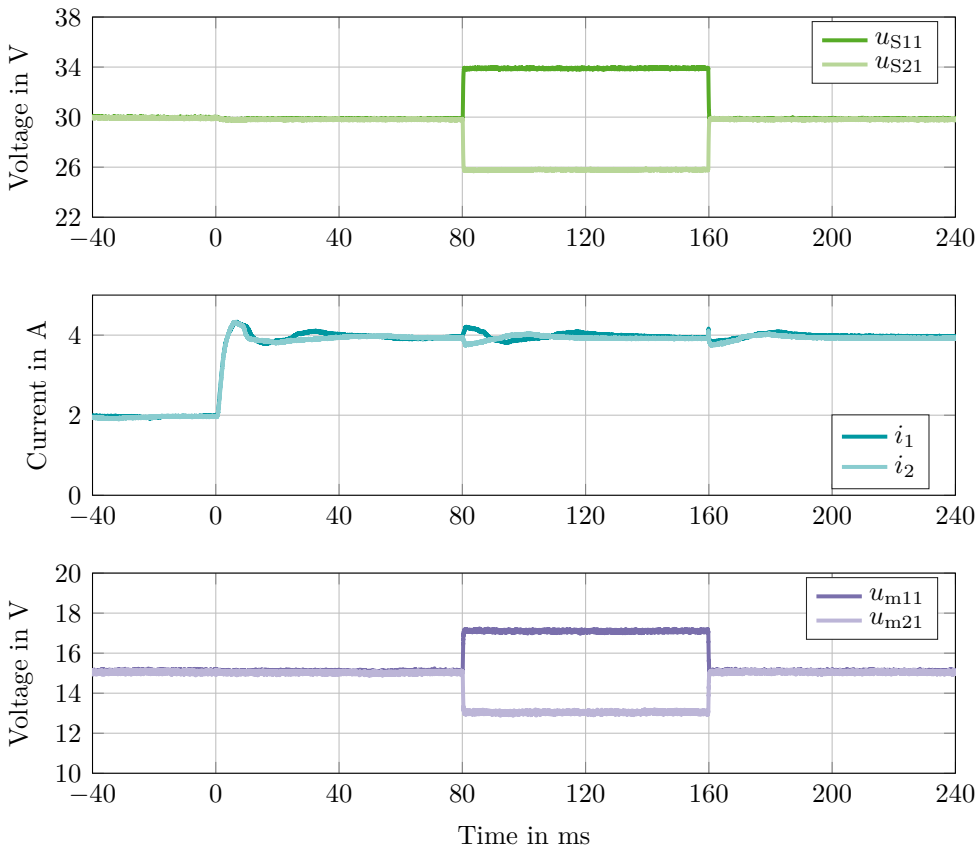



Figure D.8: Measurement of the decoupled control of the MV-type, 2S2P-interconnected secondary-side port without ideal current source

## D.5 xSyP Interconnection of MV Ports with Ideal Current Source

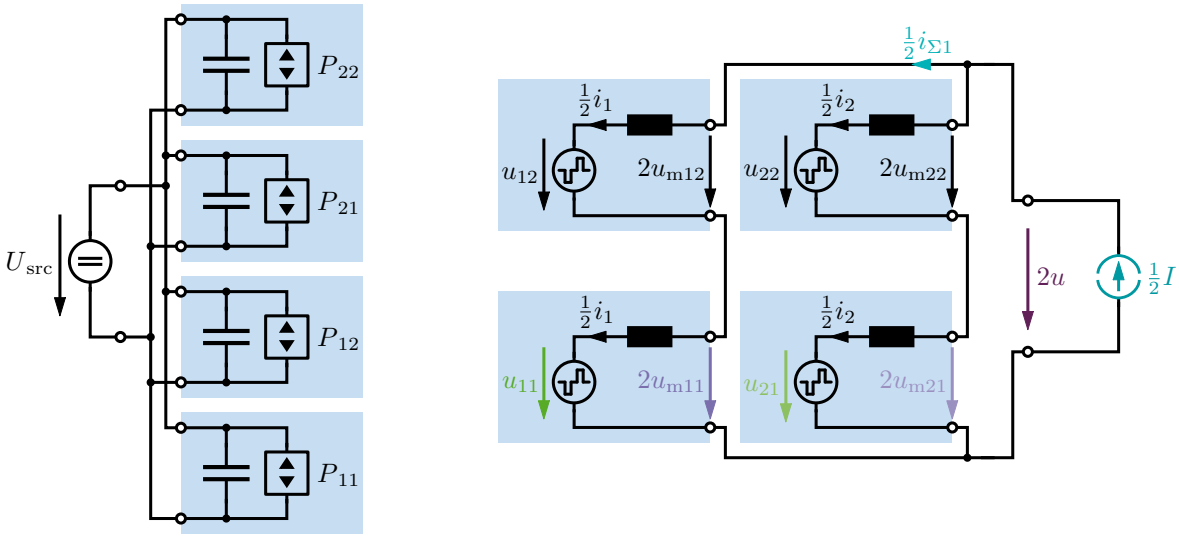
This section addresses the validation of the $x\mathrm{S}y\mathrm{P}$ interconnection of MV-type ports with ideal current source. Hence, the decoupling technique is applied to the secondary side. Figure D.9 shows the equivalent circuit of the resulting interconnection; all measured quantities are highlighted in color. The FPGA is programmed to activate the closed-loop secondary-side dc-link voltage control for each PEBB to implement MV-type port behavior as described in Section 6.2.3.3. In turn, the MCU performs the decoupled control of the state variables and external eigenvectors. Table D.5 lists the transformation matrix, the internal and external eigenvectors, denotes which variables they influence, and how their respective control loop is designed.

Table D.5: Transformation matrix and tuning of the decoupled control of the MV-type, 2S2P-interconnected secondary-side port with ideal current source

| Transformation matrix | | | | | Eigenvector type | Influencing the variable | MCU control | $f_{\mathrm{b,p}}$ | $f_{\mathrm{b,i}}$ |
|---|---|---|---|---|---|---|---|---|---|
| $\mathbf{T} =$ | $-\frac{1}{4}$ | $-\frac{1}{4}$ | $\frac{1}{4}$ | $\frac{1}{4}$ | internal | $\frac{1}{2}i_{\Sigma 1}$ | closed-loop | 1 kHz | 250 Hz |
| | $\frac{1}{2}$ | $\frac{1}{2}$ | $\frac{1}{2}$ | $\frac{1}{2}$ | external | $2u$ | open-loop | — | — |
| | 1 | $-1$ | 0 | 0 | external | $u_{\mathrm{DM1}}$ | open-loop | — | — |
| | 0 | 0 | 1 | $-1$ | external | $u_{\mathrm{DM2}}$ | open-loop | — | — |

On the secondary side, a constant terminal current $I$ of 4 A is provided by a bidirectional power supply. On the primary side, all PEBBs are connected in parallel, and a bidirectional power supply is used as load, setting a constant voltage of 30 V. Initially, the accumulated current reference $\frac{1}{2}i^*_{\Sigma 1}$ is set to 1 A, hence 2 A are measurable due to the property of the current-fed port. The secondary-side terminal voltage reference $2u^*$ is set to 60 V, which represents a measurable terminal voltage of 30 V due to the property of the current-fed port. In turn, both DM voltage references are set to zero.

Figure D.10 shows the measurement results. The initial references are reached for $t < 0$ ms. At 0 ms, the terminal voltage reference $2u^*$ is set to 52 V, which represents a measurable terminal voltage of 26 V At 40 ms, the accumulated current reference $\frac{1}{2}i^*_{\Sigma 1}$ is increased by 0.5 A, hence a step of 1 A is measured. Additionally, between 120 ms $\leq t <$ 160 ms, the DM voltage references are changed by $\pm 8$ V in the two series-connected branches. It can be seen that all control references are precisely tracked with negligible interactions. As discussed in Section 6.2, due to the limited bandwidth of the closed-loop current control in the MCU, there are some deviations in the tracking of the state variable references.




(a) Uncontrolled primary side (b) Controlled secondary side

Figure D.9: Equivalent circuit of the dc-dc converter platform with the decoupled control applied to the secondary-side 2S2P interconnection of MV-type converter ports with ideal current source

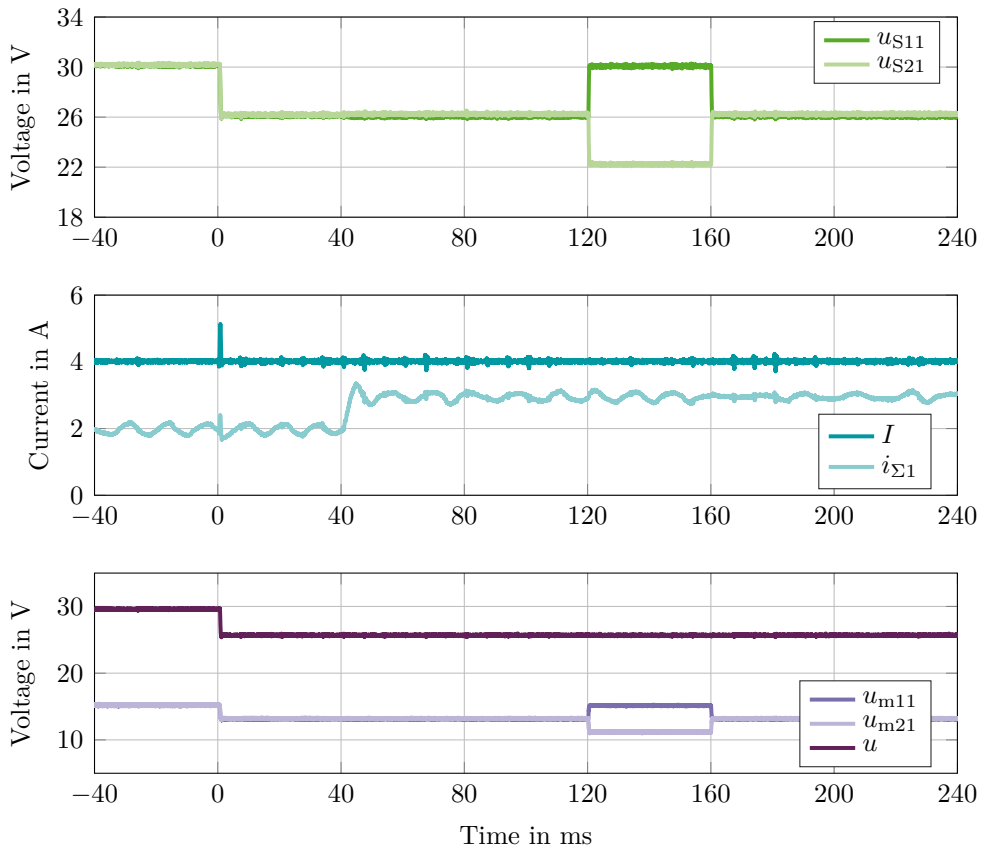



Figure D.10: Measurement of the decoupled control of the MV-type, 2S2P-interconnected secondary-side port with ideal current source

## D.6 yPxS Interconnection of MV Ports with Ideal Current Source

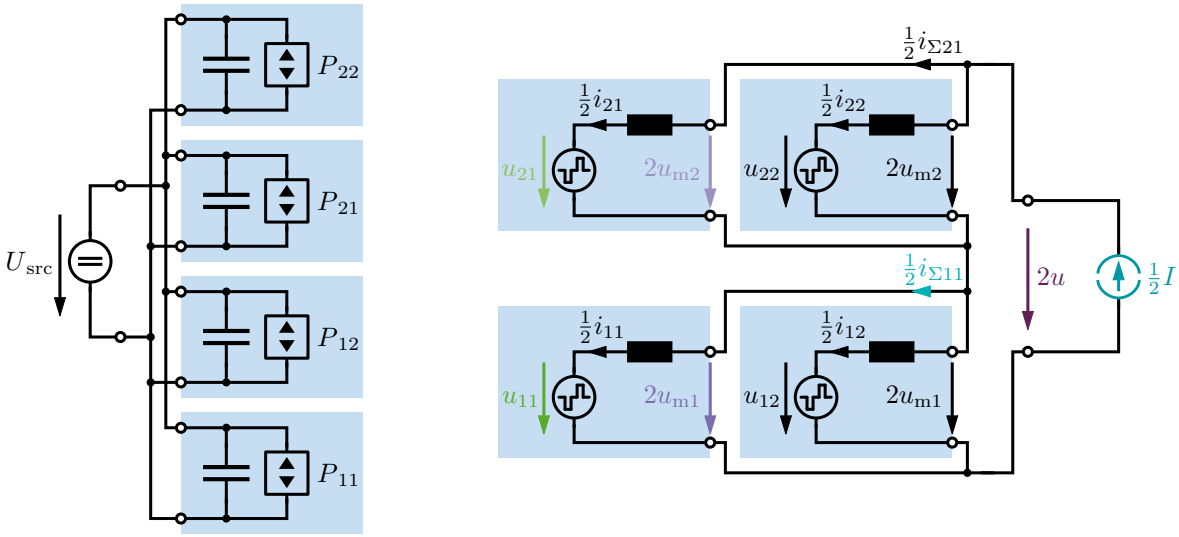
This section addresses the validation of the $y\mathrm{P}x\mathrm{S}$ interconnection of MV-type ports with ideal current source. Hence, the decoupling technique is applied to the secondary side. Figure D.11 shows the equivalent circuit of the resulting interconnection; all measured quantities are highlighted in color. The FPGA is programmed to activate the closed-loop secondary-side dc-link voltage control for each PEBB to implement MV-type port behavior as described in Section 6.2.3.3. In turn, the MCU performs the decoupled control of the state variables and external eigenvectors. Table D.6 lists the transformation matrix, the internal and external eigenvectors, denotes which variables they influence, and how their respective control loop is designed.

Table D.6: Transformation matrix and tuning of the decoupled control of the MV-type, 2P2S-interconnected secondary-side port with ideal current source

| Transformation matrix | Eigenvector type | Influencing the variable | MCU control | $f_{\mathrm{b,p}}$ | $f_{\mathrm{b,i}}$ |
|---|---|---|---|---|---|
| $\mathbf{T} = \begin{pmatrix} -\frac{1}{2} & \frac{1}{2} & 0 & 0 \\ 0 & 0 & -\frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \end{pmatrix}$ | internal | $\frac{1}{2}i_{\Sigma 11}$ | closed-loop | 1 kHz | 250 Hz |
| | internal | $\frac{1}{2}i_{\Sigma 21}$ | closed-loop | 1 kHz | 250 Hz |
| | external | $2u$ | open-loop | — | — |
| | external | $u_{\mathrm{DM}}$ | open-loop | — | — |

On the secondary side, a constant terminal current $I$ of 4 A is provided by a bidirectional power supply. On the primary side, all PEBBs are connected in parallel, and a bidirectional power supply is used as load, setting a constant voltage of 30 V. Initially, both accumulated current references $\frac{1}{2}i^*_{\Sigma 11}$ and $\frac{1}{2}i^*_{\Sigma 21}$ are set to 1 A, hence 2 A are measurable due to the property of the current-fed port. The secondary-side terminal voltage reference $2u^*$ is set to 60 V, which represents a measurable terminal voltage of 30 V due to the property of the current-fed port. In turn, the DM voltage reference is set to zero.

Figure D.12 shows the measurement results. The initial references are reached for $t < 0$ ms. At 0 ms, the terminal voltage reference $2u^*$ is set to 52 V, which represents a measurable terminal voltage of 26 V At 40 ms, the accumulated current references $\frac{1}{2}i^*_{\Sigma 11}$ and $\frac{1}{2}i^*_{\Sigma 21}$ are both increased by 0.5 A, hence steps of 1 A are measured. Additionally, between 120 ms $\leq t <$ 160 ms, the DM voltage reference is temporarily increased by 8 V. It can be seen that all control references are precisely tracked with negligible interactions. As discussed in Section 6.2, due to the limited bandwidth of the closed-loop current control in the MCU, there are some deviations in the tracking of the state variable references.




(a) Uncontrolled primary side

(b) Controlled secondary side

Figure D.11: Equivalent circuit of the dc-dc converter platform with the decoupled control applied to the secondary-side 2P2S interconnection of MV-type converter ports with ideal current source

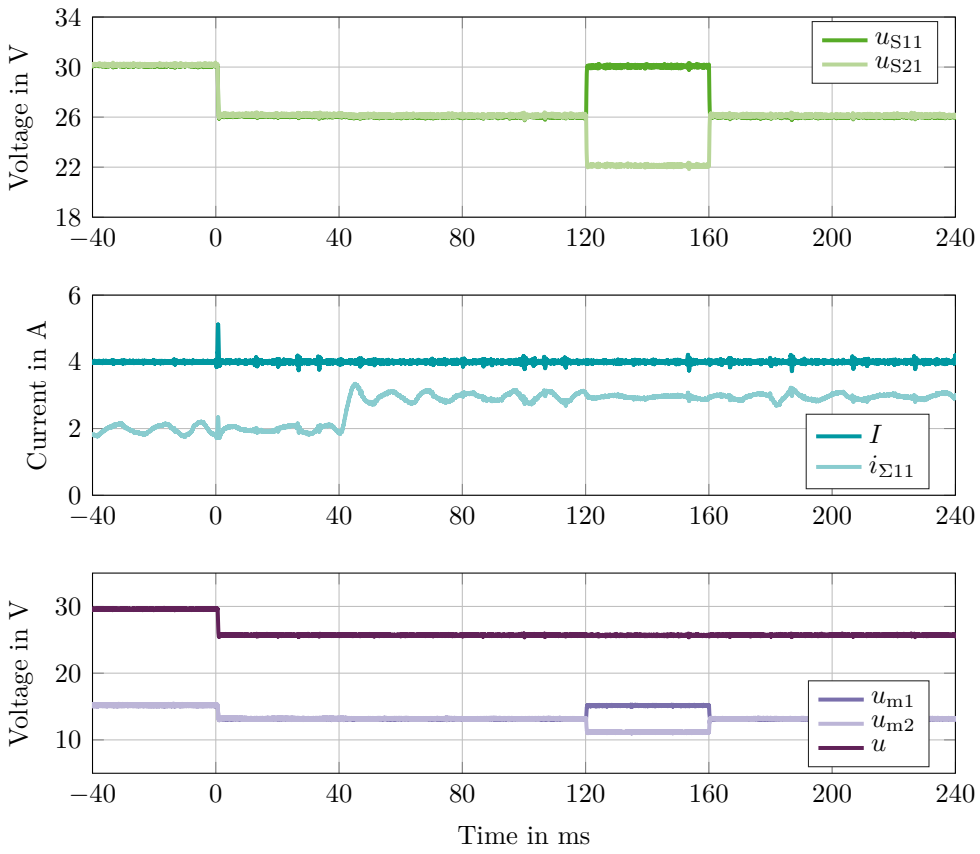



Figure D.12: Measurement of the decoupled control of the MV-type, 2P2S-interconnected secondary-side port with ideal current source

# List of Acronyms

| | |
|---|---|
| $\Delta\Sigma$ | delta-sigma |
| 3D | three dimensional |
| | |
| ac | alternating current |
| ADC | analog-to-digital converter |
| ADCC | asymmetric duty cycle control |
| AlN | aluminum nitride |
| | |
| B2B | back-to-back |
| | |
| CC | constant-current |
| CCM | continuous conduction mode |
| CIC | cascaded integrator-comb |
| CM | common-mode |
| CPL | constant-power load |
| CPS | constant-power source |
| CPU | central processing unit |
| CV | constant-voltage |
| | |
| DAB | dual-active bridge |
| dc | direct current |
| DCM | discontinuous conduction mode |
| DM | differential-mode |
| DSP | digital signal processor |
| | |
| EMIF | external memory interface |
| | |
| FCM | flux control modulation |
| FPGA | field-programmable gate array |
| FPU | floating-point unit |
| | |
| GaN | gallium nitride |
| | |
| IC | integrated circuit |
| ICC | instantaneous current control |
| IFCC | instantaneous flux and current control |

| | |
|---|---|
| IGBT | insulated-gate bipolar transistor |
| IICC | improved instantaneous current control |
| IIFCC | improved instantaneous flux and current control |
| IMC | in-motion charging |
| IPOP | input-parallel output-parallel |
| IPOS | input-parallel output-series |
| ISOP | input-series output-parallel |
| ISOS | input-series output-series |
| JTAG | joint test action group |
| KCL | KIRCHHOFF's current law |
| KVL | KIRCHHOFF's voltage law |
| LED | light-emitting diode |
| LTI | linear time-invariant |
| LUT | look-up table |
| MAB | multi-active bridge |
| MC | manipulated current |
| MCU | microcontroller |
| MIMO | multiple-input, multiple-output |
| MMC | modular multilevel converter |
| MOSFET | metal-oxide-semiconductor field-effect transistor |
| MV | manipulated voltage |
| OBC | on-board charger |
| ODE | ordinary differential equation |
| PC | personal computer |
| PCB | printed circuit board |
| PEBB | power-electronic building block |
| PEM | proton exchange membrane |
| PI | proportional-integral |
| POVG | positive output voltage gradient |
| PSFB | phase-shifted full-bridge |
| PWM | pulse-width modulation |
| RAM | random access memory |
| S/H | sample and hold |
| Si | silicon |
| SiC | silicon carbide |
| SiL | software in the loop |
| SISO | single-input, single-output |

| | |
|---|---|
| SPI | serial peripheral interface |
| SPS | single phase shift |
| SST | solid-state transformer |
| | |
| ZOH | zero-order hold |
| ZVS | zero-voltage switching |

# List of Symbols

## Notation

| | |
|---|---|
| $x^{\triangledown}$ | commanded quantity to the actuator in closed or open control loops |
| $(\mathbf{X})_{pq}$ | entry of the matrix $\mathbf{X}$ in row $p$ and column $q$ |
| $\mathbf{I}_x$ | identity matrix of the dimension $(x \times x)$ |
| $\mathbf{X}$ | matrix |
| $\mathbf{1}_{x\times y}$ | matrix of the dimension $(x \times y)$ containing only ones |
| $\vec{1}_{x\times 1},\ \vec{1}_{1\times y}$ | vectors of the dimension $(x \times 1)$ or $(1 \times y)$, respectively, containing only ones |
| $\hat{x}$ | estimated quantity |
| $x^*$ | reference quantity in closed or open control loops |
| $\mathbf{X}^{\blacksquare}$ | some submatrix of a block matrix $\mathbf{X}$ |
| $\mathbf{X}^{\square}$ | some submatrix of a block matrix $\mathbf{X}$ |
| $\vec{x}$ | vector |
| $\mathbf{0}_{x\times y}$ | matrix of the dimension $(x \times y)$ containing only zeros |
| $\vec{0}_{x\times 1},\ \vec{0}_{1\times y}$ | vectors of the dimension $(x \times 1)$ or $(1 \times y)$, respectively, containing only zeros |

## Operators

| | |
|---|---|
| $\lvert x\rvert$ | absolute value |
| $\det \mathbf{X}$ | determinant of a square matrix |
| $\mathbf{diag}(x_1, x_2, \ldots, x_n)$ | square, diagnoal $(n \times n)$ matrix with diagonal entries $x_1, x_2, \ldots, x_n$ |
| $\vec{\nabla} x$ | gradient |
| $\max_p\{x_p\}$ | maximum value |
| $\lfloor x \rfloor$ | floor function |
| $\mathbf{X}^{-1}$ | inverse of a square matrix |
| $\mathbf{X} \otimes \mathbf{Y}$ | Kronecker product of two matrices |
| $\ln x$ | natural logarithm (base e) |
| $\lVert \vec{x} \rVert_2$ | Euclidean norm of a vector |
| $\bar{x}$ | arithmetic mean value |

| | |
|---|---|
| $x'$, $X'$ | electrical quantity referred to the primary side of a transformer, scaling it with the turns ratio |
| $\operatorname{sgn} x$ | sign function |
| $\mathbf{X}^{\mathrm{T}}$ | transpose of a matrix |
| $\vec{x}^{\mathrm{T}}$ | transpose of a vector |
| $\tilde{\mathbf{X}}$ | matrix transformed into decoupled coordinates |
| $\tilde{\vec{x}}$ | vector transformed into decoupled coordinates |

## Variables

| | |
|---|---|
| $\alpha$ | positive real number |
| $\vec{a}$ | generic vector |
| $\beta$ | positive real number |
| $\vec{c}$ | generic vector |
| $\delta$, $\delta_1$, $\delta_2$ | positive real numbers |
| $\epsilon$ | positive real number |
| $\gamma$ | real number |
| $\mathbf{K}$ | generic matrix |
| $\lambda_p$ | $p^{\mathrm{th}}$ eigenvalue |
| $\lambda_{\mathrm{E}}$ | external eigenvalue |
| $\lambda_{\mathrm{I}}$ | internal eigenvalue |
| $\mathbf{L}$ | generic matrix |
| $\mathbf{\Lambda}$ | spectral matrix containing eigenvalues on its diagonal |
| $\mathbf{M}$ | generic matrix |
| $\mu$ | real number |
| $\mathbf{N}$ | generic matrix |
| $o$ | counter variable (integer) |
| $p$ | counter variable (integer) |
| $q$ | counter variable (integer) |
| $r$ | counter variable (integer) |
| $\vec{v}$ | generic left eigenvector |
| $\vec{v}_{\mathrm{E}p}$ | $p^{\mathrm{th}}$ external eigenvector |
| $\vec{v}_{\mathrm{I}p}$ | $p^{\mathrm{th}}$ internal eigenvector |
| $\mathbf{V}$ | left modal matrix containing left eigenvectors as rows |
| $\mathbf{V}_{\mathrm{E}}$ | external left modal matrix |
| $\mathbf{V}_{\mathrm{I}}$ | internal left modal matrix |
| $\vec{w}$ | generic right eigenvector |
| $\mathbf{W}$ | right modal matrix containing right eigenvectors as columns |
| $k$ | time variable in discrete systems (integer) |
| $s$ | Laplace variable (complex number) |
| $V(\vec{x})$ | LYAPUNOV function |

| | |
|---|---|
| $z$ | variable of the $z$ transformation (complex number) |
| $\mathbf{A}$ | system matrix of a linear control system |
| $\mathbf{B_d}$ | disturbance input matrix of a linear control system |
| $\mathbf{B_m}$ | manipulated input matrix of a linear control system |
| $\mathbf{C}$ | output matrix of a linear control system |
| $\mathbf{D_d}$ | disturbance feed-through matrix of a linear control system |
| $\mathbf{D_m}$ | manipulated feed-through matrix of a linear control system |
| $e$ | error in a control system |
| $\vec{F}$ | system function of a nonlinear control system |
| $\vec{G}$ | output function of a nonlinear control system |
| $\mathbf{T}$ | coordinate transformation matrix |
| $u_\mathrm{d}$ | disturbance input variable to a control system |
| $\vec{u}_\mathrm{d}$ | vector of disturbance input variables to a control system |
| $u_\mathrm{m}$ | manipulated input variable to a control system |
| $u_\mathrm{m}^\mathrm{max}$ | upper limit of the manipulated input variable to a control system |
| $u_\mathrm{m}^\mathrm{min}$ | lower limit of the manipulated input variable to a control system |
| $\vec{u}_\mathrm{m}$ | vector of manipulated input variables to a control system |
| $x$ | state variable of a control system |
| $\vec{x}_\mathrm{eq}$ | equilibrium point of a control system |
| $\vec{x}$ | vector of states variables of a control system |
| $y$ | measured output variable of a control system |
| $\vec{y}$ | vector of measured output variables of a control system |
| $\delta_\mathrm{PI,u}$ | $z$-plane zero of the discrete-time PI regulator in the voltage controller |
| $\delta_\mathrm{z}$ | $z$-plane zero of a discrete-time filter |
| $K_\mathrm{i}$ | integral feedback gain of a generic controller |
| $K_\mathrm{i,i}$ | integral feedback gain of a current controller |
| $K_\mathrm{i,u}$ | integral feedback gain of a voltage controller |
| $K_\mathrm{p}$ | proportional feedback gain of a generic controller |
| $K_\mathrm{p,i}$ | proportional feedback gain of a current controller |
| $K_\mathrm{p,u}$ | proportional feedback gain of a voltage controller |
| $\tau_\mathrm{PI,u}$ | time constant of the PI regulator in the voltage controller |
| $DR(z)$ | disturbance-response function |

| | |
|---|---|
| $DS(z)$ | dynamic stiffness function |
| $FRF(z)$ | frequency-response function |
| $G_{\mathrm{C}}(z)$ | transfer function of the controller in a control system |
| $G_{\mathrm{ICC}}(z)$ | transfer function of the ICC method |
| $G_{\mathrm{P}}(z)$ | transfer function of the plant in a control system |
| | |
| $I_{\mathrm{err}}(s)$ | LAPLACE transform of the current error |
| $I_{\mathrm{err}}(z)$ | $z$ transform of the current error |
| $\overline{I}_{\mathrm{S}}(z)$ | $z$ transform of the average secondary-side rectified current |
| $\overline{I}^{*}_{\mathrm{S}}(z)$ | $z$ transform of the reference average secondary-side rectified current |
| $U_{\mathrm{S}}(s)$ | LAPLACE transform of the secondary-side dc-link voltage |
| $U^{*}_{\mathrm{S}}(s)$ | LAPLACE transform of the reference secondary-side dc-link voltage |
| | |
| $n$ | integer representing the total number of interconnected converters |
| $n_x$ | integer representing the total number of states in an interconnected converter |
| $x$ | integer representing the number of serial or parallel interconnected converters |
| $y$ | integer representing the number of serial or parallel interconnected converters |
| | |
| $C$ | port capacitor of a PEBB with an MC port |
| $C_{\mathrm{P}}$ | primary-side dc-link capacitance |
| $C_{\mathrm{S}}$ | secondary-side dc-link capacitance |
| | |
| $L_{\mathrm{b}}$ | inductance of the current-fed series inductors |
| $L_{\mathrm{b,eq}}$ | equivalent inductance in the equivalent circuit of a current-fed converter |
| $L$ | port inductor of a PEBB with an MV port |
| $L_{\sigma}$ | stray inductance of the transformer |
| | |
| $\Delta u$ | voltage deviation from an equilibrium point |
| $u_{\mathrm{DM}}$ | differential-mode voltage in series-connected MV-type ports |
| $u_{\mathrm{eq}}$ | equilibrium-point voltage |
| $U_{\mathrm{load}}$ | dc load voltage |
| $u_{\mathrm{load}}$ | instantaneous load voltage |
| $u_{\mathrm{m}pq}$ | measured terminal voltage of an MV port with the coordinates $p$ and $q$ |

| | |
|---|---|
| $u_{\max}$ | maximum voltage |
| $u_{\mathrm{MP}}$ | midpoint voltage in series-connected MC-type ports |
| $U_{\mathrm{P}}$ | primary-side dc-link supply voltage |
| $u_{\mathrm{P}}$ | instantaneous voltage across the secondary-side dc-link capacitor |
| $U_{\mathrm{S}}$ | secondary-side dc-link supply voltage |
| $u_{\mathrm{S}}$ | instantaneous voltage across the secondary-side dc-link capacitor |
| $U_{\mathrm{src}}$ | dc source voltage |
| $u_{\mathrm{src}}$ | instantaneous source voltage |
| $u_{\mathrm{T,P}}$ | primary-side voltage across the transformer winding |
| $u_{\mathrm{T,S}}$ | secondary-side voltage across the transformer winding |
| $U$ | some constant dc-link supply voltage |
| $u_{pq}$ | manipulated input of an MV port with the coordinates $p$ and $q$, or state variable of an MC port with the coordinates $p$ and $q$ |
| $\Delta i$ | current deviation from an equilibrium point |
| $i_{\mathrm{DM}}$ | differential-mode current |
| $i_{\mathrm{eq}}$ | equilibrium-point current |
| $i_{\mathrm{err}}$ | current error as disturbance input, representing model inaccuracies |
| $I$ | some constant dc-link supply current |
| $i_{pq}$ | manipulated input of an MC port with the coordinates $p$ and $q$, or state variable of an MV port with the coordinates $p$ and $q$ |
| $i_{\mathrm{L},k}$ | current in the $k^{\mathrm{th}}$ current-fed inductor |
| $i_{\mathrm{load}}$ | instantaneous load current |
| $\Delta I_{\mathrm{load,pp}}$ | peak-to-peak ripple component of the load current in current-fed converters |
| $i_{\mathrm{m}pq}$ | measured terminal current of an MC port with the coordinates $p$ and $q$ |
| $i_{\max}$ | maximum current |
| $i_{\mathrm{MP}}$ | current that manipulates a midpoint voltage in series-connected MC-type ports |
| $i_{\mathrm{mP}}$ | measured primary-side terminal current |
| $i_{\mathrm{mS}}$ | measured secondary-side terminal current |
| $i_{\mathrm{P}}$ | primary-side rectified current |
| $i_{\mathrm{S}}$ | secondary-side rectified current |
| $i_{\mathrm{S,CM}}$ | common-mode secondary-side rectified current |
| $i_{\mathrm{S,DM}}$ | differential-mode secondary-side rectified current |
| $i_{\mathrm{src}}$ | instantaneous source current |
| $i_{\Sigma}$ | accumulated branch current in parallel-connected MV-type ports |
| $i_{\mathrm{T}}$ | current in the transformer winding |

| | |
|---|---|
| $f_{\mathrm{b,i}}$ | bandwidth of the integral feedback loop |
| $f_{\mathrm{b,p}}$ | bandwidth of the proportional feedback loop |
| $f$ | frequency variable |
| $f_{\mathrm{res}}$ | resonant frequency |
| $f_{\mathrm{sw}}$ | switching frequency |
| | |
| $T_{\mathrm{s}}$ | sampling time |
| $\tau_{\mathrm{d,i}}$ | time constant of disturbance rejection of a current controller |
| $t$ | time variable |
| | |
| $\varphi$ | phase-shift angle in SPS modulation |
| $\varphi_0$ | empirical offset phase-shift angle in SPS modulation |
| | |
| $d$ | duty cycle |
| $\nu$ | number of half-bridge legs in an interleaved buck converter |
| $R_{\mathrm{load}}$ | load resistance |
| $Y_0$ | empirical offset admittance in SPS modulation |
| | |
| $P_{pq}$ | active power of a constant-power port with the coordinates $p$ and $q$ |
| $P_{\mathrm{SPS,1ph}}$ | transferred power of the single-phase dual-active bridge converter |
| $P_{\mathrm{SPS,3ph}}$ | transferred power of the three-phase dual-active bridge converter |

# List of Figures

# List of Tables

# Bibliography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# Curriculum Vitae

## Jan Niklas Fritz

### Personal Information

| | |
|---|---|
| Date of birth | January 3, 1992 |
| Place of birth | Aachen, Germany |
| Nationality | German |

### Education

| | |
|---|---|
| 2011–2017 | Studies in Electrical Engineering and Information Technology at RWTH Aachen University; Bachelor and Master of Science Degree |
| 2002–2011 | Bischöfliches Pius-Gymnasium Aachen (high school) |

### Work Experience

| | |
|---|---|
| 09/2018–today | Research Associate at the Institute for Power Electronics and Electrical Drives (ISEA) of RWTH Aachen University under the supervision of Prof. Rik W. De Doncker in the Research Group Power Electronics; Group Leader since 10/2021; Chief Engineer since 05/2024 |
| 10/2016–03/2017 | Visiting research scholar at the Power Electronics, Machines and Control Group (PEMC) of the University of Nottingham, UK, under the supervision of Prof. Pat Wheeler |
| 04/2016–08/2016 | Internship at Futavis GmbH, Aachen |
| 2013–2016 | Student research assistant in the Power Electronics Group of the Institute for Power Electronics and Electrical Drives (ISEA), RWTH Aachen University |
| 2012–2013 | Teaching assistant at the Institute of Imaging and Computer Vision (LfB) and the Institute for Power Electronics and Electrical Drives (ISEA) of RWTH Aachen University |

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The increasing demand for power electronic converters goes hand in hand with an increasing degree of modularity. Interconnecting existing products is often more feasible than developing a new product, which benefits the suppliers and improves the scalability of power electronics in general.
Despite these benefits, the modularization trend presents challenges in controlling such modular converters. Interconnecting converters in series or parallel introduces cross coupling into the control loops. Applying the same control methods designed for a single converter to an interconnected converter instead will result in significantly worse performance. The control of a modular converter may even be overdetermined or unstable, when the number of control variables exceeds the number of converters.
This dissertation develops a generalized control methodology for modular, galvanically isolated dc dc converters that ensures power sharing, control loop decoupling, and system stability, even for overdetermined interconnections. There is no restriction on the converter topology, and every possible interconnection is covered. The proposed methodology utilizes a linear transformation of the multi converter state space model into a coordinate system in which the cross coupling is completely removed, using the eigenvectors of the system matrices. Instead of being mathematically abstract, the proposed solution is physically insightful, because the eigenvectors have physical meaning. Furthermore, the solution is simple, robust, and easy to implement. It is experimentally validated in two case studies.

ISSN 1437-675X