

# Digital-Centric Multi-Standard Transmitters for Advanced Wireless Communication Standards

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Successful men and women keep moving. They make mistakes, but they do not quit.

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*Conrad Hilton*



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## Abstract

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The rapid growth in the number of wireless-connected devices and the demand for higher data rates in modern communication systems have led to increasing spectrum scarcity and more complex modulation schemes, which necessitates more power-efficient and highly-linear transmitters. Advanced wireless communication standards demand strict out-of-channel and out-of-band emission control, use of enhanced modulation schemes with denser constellation points, and operation in mm-wave frequencies to achieve larger data bandwidths. Furthermore, with more flexibility and reconfigurability of digital circuits, which benefit higher-speed and smaller area of CMOS down-scaling, there is a desire to move functionalities of a transmitter as much as possible into the digital domain. Digital-Centric Multi-standard Transmitters (DCMTs) emerge as a promising solution for Software-Defined Radio (SDR), offering enhanced flexibility and reconfigurability through digital signal processing. This dissertation investigates the design and implementation of two novel DCMT architectures that address the key challenges in system design aspects and analog implementation in order to achieve a decent performance. Therefore, certain techniques and solutions have been established to improve weaknesses of the proposed architectures. Proof-of-concept prototypes are developed to validate the proposed architectures, demonstrating their potential for modern communication standards.

The first architecture introduces an I/Q digital-centric transmitter with a 25% duty-cycle which is developed and fabricated in a 65-nm CMOS technology to operate for a number of target standards such as IEEE 802.11ac at its 2.4 GHz band. The concept and its system design are explained in details. Then, circuit design and implementation are presented. And at the end, Measurement results are provided to prove its feasibility and potential performance. Despite some nonlinearity challenges in the DPA frontend, the transmitter successfully meets the WLAN requirements while indicating the effectiveness of a 25% LO duty cycle in enhancing power efficiency.

The second architecture focuses on a Multi-Level LINC (ML-LINC) transmitter with I/Q RF-DAC frontends, implemented in a 28-nm CMOS technology. An ML-LINC transmitter provides a high linearity and a relatively good power efficiency compared to simple LINC transmitters. As a result, it can be a good candidate for modulation schemes with larger number of constellation points. The transmitter of this work targets 160-MHz channels in the 5-GHz band of IEEE 802.11ac, emphasizing high linearity and power efficiency through innovative outphasing techniques. A major challenge is achieving outphasing vectors out of the transmitter frontend in I/Q form without losing accuracy of the transmit signal as a result of bandwidth expansion due to Cartesian/Polar conversions.

The design incorporates an I/Q unitcell-sharing [RF-DAC](#) structure with optimized phase and amplitude generation. Simulations confirm its ability to maintain signal integrity even under frontend imperfections.

In a nutshell, this work presents system aspects and circuit implementations as well as post-silicon validation of the proposed transmitters. Systematic requirements of the transmitters to meet specifications of target communication standards are derived. Simulations and Measurement results validate the proposed designs, highlighting key areas for improvement, including frontend linearity and system efficiency. The weaknesses are addressed and solutions are discussed. The findings pave the way for more advanced [Software-Defined Radio \(SDR\)](#) solutions that can adapt to evolving wireless standards with minimal hardware modifications.

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## Acronyms

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<b>3GPP</b>	3 <sup>rd</sup> Generation Partnership Project
<b>AC</b>	Alternating Current
<b>ACLR</b>	Adjacent Channel Leakage Ratio
<b>ADC</b>	Analog-to-Digital Converter
<b>ADPLL</b>	All-Digital Phase-Locked Loop
<b>AltCLR</b>	Alternate Channel Leakage Ratio
<b>AM</b>	Amplitude Modulation
<b>ASIC</b>	Application-Specific Integrated Circuit
<b>ASK</b>	Amplitude Shift Keying
<b>ASRC</b>	Arbitrary Sampling-Rate Conversion
<b>BBIC</b>	Baseband Integrated Circuit
<b>BER</b>	Bit Error Rate
<b>BPSK</b>	Binary Phase Shift Keying
<b>CDC</b>	Clock Domain Converter
<b>CDMA</b>	Code-Division Multiple Access
<b>CIC</b>	Cascaded Integrator-Comb
<b>CML</b>	Current-Mode Logic
<b>CMOS</b>	Complementary Metal-Oxide-Semiconductor
<b>CORDIC</b>	COordinate Rotation DIgital Computer
<b>CP</b>	Cyclic Prefix
<b>D-FF</b>	D Flip-Flop
<b>DAC</b>	Digital-to-Analog Converter
<b>DC</b>	Direct Current
<b>DCMT</b>	Digital-Centric Multi-standard Transmitter
<b>DCO</b>	Digitally-Controlled Oscillator
<b>DDR</b>	Dual Data Rate
<b>DDRC</b>	Direct Digital-to-RF Converter
<b>DET</b>	Digital-Enhanced Transmitter
<b>DFT</b>	Discrete Fourier Transform
<b>DLL</b>	Delay-Locked Loop
<b>DNL</b>	Differential NonLinearity
<b>DNW</b>	Deep N-Well
<b>DPA</b>	Digital Power Amplifier
<b>DPD</b>	Digital PreDistortion
<b>DSP</b>	Digital Signal Processing

<b>DSSS</b>	Direct Sequence Spread Spectrum
<b>DUT</b>	Device Under Test
<b>DWA</b>	Data-Weighted Averaging
<b>E-UTRA</b>	Evolved UMTS Terrestrial Radio Access
<b>EER</b>	Envelope Elimination and Restoration
<b>EIRP</b>	Effective Isotropically Radiated Power
<b>EM</b>	Electromagnetic
<b>ESL</b>	Element Selection Logic
<b>ET</b>	Envelope Tracking
<b>EVM</b>	Error-Vector Magnitude
<b>FDD</b>	Frequency-Division Duplex
<b>FDMA</b>	Frequency-Division Multiple Access
<b>FFT</b>	Fast Fourier Transform
<b>FIFO</b>	First In, First Out
<b>FIR</b>	Finite Impulse Response
<b>FMC</b>	FPGA Mezzanine Card
<b>FoM</b>	Figure of Merit
<b>FPGA</b>	Field-Programmable Gate Array
<b>FSK</b>	Frequency-Shift Keying
<b>FSM</b>	Finite-State Machine
<b>GI</b>	Guard Interval
<b>GPIB</b>	General-Purpose Interface Bus
<b>I/Q</b>	In-phase and Quadrature component
<b>IC</b>	Integrated Circuit
<b>ICI</b>	Inter-Channel Interference
<b>IEEE</b>	Institute of Electrical and Electronics Engineers
<b>IF</b>	Intermediate Frequency
<b>IFFT</b>	Inverse Fast Fourier Transform
<b>IIP3</b>	third Input Intercept Point
<b>IM3</b>	Inter-Modulation 3
<b>IoT</b>	Internet-of-Things
<b>IRR</b>	Image-Rejection Ratio
<b>ISI</b>	Inter-Symbol Interference
<b>ISM</b>	Industrial, Scientific, and Medical
<b>IUSR</b>	Inverted UpSampling Ratio
<b>LDO</b>	Low Drop-Out
<b>LINC</b>	Linear amplification with Nonlinear Components
<b>LO</b>	Local Oscillator
<b>LSB</b>	Least-Significant Bit
<b>LTE</b>	Long-Term Evolution

<b>LUT</b>	Look-Up Table
<b>LVDS</b>	Low-Voltage Differential Signaling
<b>LVS</b>	Layout Versus Schematic
<b>MAC</b>	Media Access Control
<b>MCS</b>	Modulation and Coding Scheme
<b>MIMO</b>	Multiple-Input Multiple-Output
<b>ML-LINC</b>	Multi-Level LINC
<b>ML-SCS</b>	Multi-Level Signal Component Separator
<b>MOS</b>	Metal-Oxide-Semiconductor
<b>MPW</b>	Multi-Project Wafer
<b>MSB</b>	Most-Significant Bit
<b>OFDM</b>	Orthogonal Frequency-Division Multiplexing
<b>OFDMA</b>	Orthogonal Frequency-Division Multiple Access
<b>OIP3</b>	third Output Intercept Point
<b>OSR</b>	Over-Sampling Ratio
<b>PA</b>	Power Amplifier
<b>PAE</b>	Power-Added Efficiency
<b>PAPR</b>	Peak-to-Average Power Ratio
<b>PCB</b>	Printed-Circuit Board
<b>PHY</b>	Physical Layer
<b>PLL</b>	Phase-Locked Loop
<b>PMU</b>	Power Management Unit
<b>PSD</b>	Power Spectral Density
<b>PSF</b>	Pulse-Shaping Filter
<b>PSK</b>	Phase-Shift Keying
<b>PSN</b>	Power Supply Noise
<b>PVT</b>	Process-Voltage-Temperature
<b>QAM</b>	Quadrature Amplitude Modulation
<b>QFN</b>	Quad Flat No-leads
<b>QPSK</b>	Quaternary Phase-Shift Keying
<b>RA-DWA</b>	Reduced-Activity Data-Weighted Averaging
<b>RB</b>	Resource Block
<b>RDL</b>	ReDistribution Layer
<b>RE</b>	Resource Element
<b>RF</b>	Radio Frequency
<b>RF-DAC</b>	Radio-Frequency Digital-to-Analog Converter
<b>RFIC</b>	Radio Frequency Integrated Circuit
<b>RLAN</b>	Radio Local-Area Network
<b>RMS</b>	Root Mean Square
<b>RX</b>	Receiver

<b>SC</b>	Subcarrier
<b>SC-FDMA</b>	Single Carrier – Frequency Division Multiple Access
<b>SCS</b>	Signal-Component Separator
<b>SDR</b>	Software-Defined Radio
<b>SMA</b>	Sub-Miniature version A
<b>SMB</b>	Sub-Miniature version B
<b>SMT</b>	Surface Mount Connector
<b>SNR</b>	Signal-to-Noise Ratio
<b>SRAM</b>	Static Random-Access Memory
<b>SSB</b>	Single-Side Band
<b>TD-SCDMA</b>	Time Division Synchronous Code Division Multiple Access
<b>TDD</b>	Time-Division Duplex
<b>TDMA</b>	Time-Division Multiple Access
<b>THD</b>	Total Harmonic Distortion
<b>TSMC</b>	Taiwan Semiconductor Manufacturing Company
<b>TSPC</b>	True Single-Phase Clock
<b>TX</b>	Transmitter
<b>UART</b>	Universal Asynchronous Receiver Transceiver
<b>UE</b>	User Equipment
<b>UMTS</b>	Universal Mobile Telecommunications System
<b>USB</b>	Universal Serial Bus
<b>USR</b>	UpSampling Ratio
<b>UWB</b>	Ultra-WideBand
<b>VGA</b>	Variable-Gain Amplifier
<b>WCDMA</b>	Wideband Code-Division Multiple Access
<b>WLAN</b>	Wireless Local-Area Network
<b>ZOH</b>	Zero-Order Hold

# Chapter 1

## Introduction

In today's world, wireless communications are essential and inevitable parts of our lives. Every day, a notable number of wireless devices are being produced and brought into play across the world. These include a wide range of devices such as smartphones, smartwatches, medical devices, automotive sensors, lights, home appliances, and numerous other types of devices that are connected through their [Internet-of-Things \(IoT\)](#) compatibilities. As a result, the number of wireless-connected devices increases remarkably year by year. Fig. 1.1 shows the number of connected devices of 4 different categories from 2014 to 2022 across the world according to the Ericsson mobility report [1]. It can be seen that in a span of eight years, the number of connected devices is doubled from 11,964 million in 2014 to 23,590 million in 2021. In other words, each year, several billion devices are added to the world around us, each requiring a frequency bandwidth of wireless communications. This trend is expected to continue as it is foretasted up to 2028 in Fig. 1.1. The huge number of wireless connections leads to scarcity of spectrum due to limited frequency bands. Therefore, the frequency spectrum needs to be utilized more efficiently.

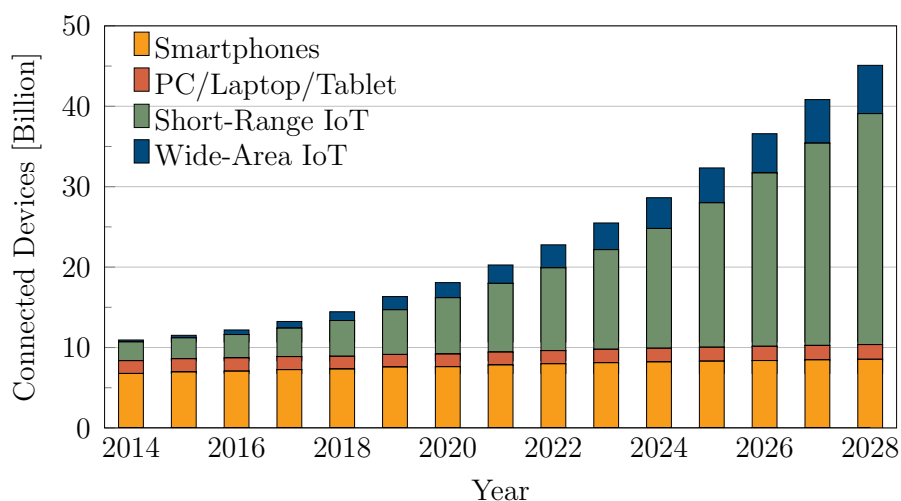


Figure 1.1: Estimated number of wireless connections per year [1].

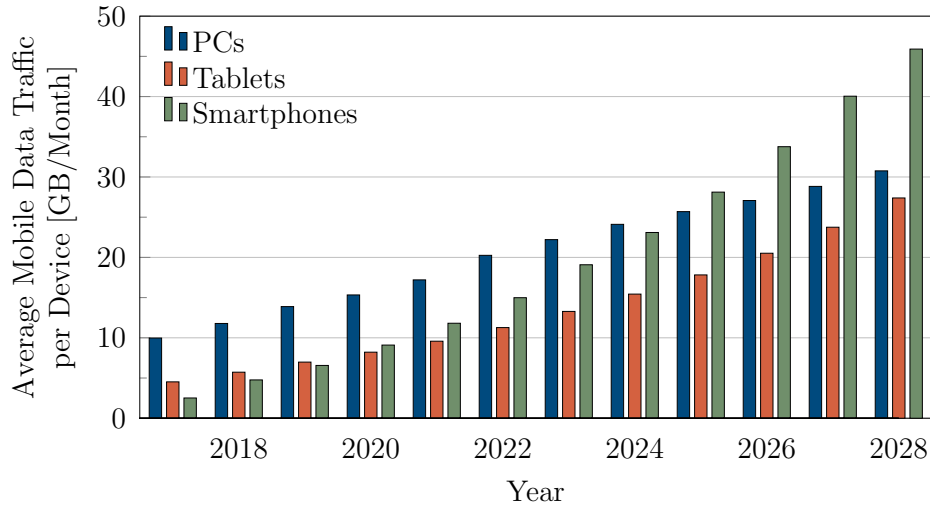


Figure 1.2: Average mobile data traffic across the world [1].

Furthermore, there is a trend of evolution of wireless communication towards higher data rates. Fig. 1.2 shows the average mobile data traffic per device per month for PCs, tablets, and smartphones from 2017 to 2022 as well as the forecast of this trend till 2028 [1]. The average data traffic of smartphones, which are the most popular connected devices nowadays, has increased from less than 2.5 GB/month to more than 15 GB/month, which implies up to six times higher data rates in 5 years. This is expected to grow in the same direction in the coming years as there is a never-ending demand for higher data rates. Higher data rates require larger modulation bandwidths. However, with a huge number of communication devices, the standard frequency bands are pretty occupied. As a result, more complicated modulation schemes with high spectrum efficiency and higher data rates are emerging and finding their way into frameworks of advanced communication standards such as 5G. On the other hand, the transmit frequencies are also getting shifted towards mm-wave frequencies, where larger data bandwidths can be realized. 5G, as an example, is intended to cover transmission frequencies up to 7.125 GHz in its frequency range 1 and up to 71 GHz in its frequency range 2 [2]. Also, the WLAN standard is already covering wireless transmission at 5 GHz band in 802.11ac and at 6 GHz band in 802.11ax [3].

Higher transmit frequencies and higher modulation bandwidths require significantly higher power consumption. However, the power budget of advanced mobile devices is clearly limited to allow for longer battery lives. This requires much more attention towards power efficiency of the whole communication system. In particular, transmitters as the most power-consuming parts of communication systems, need to cope with this trend as well. On the other hand, with more complicated modulation schemes, a transmitter should provide a sufficiently high performance in terms of linearity and signal quality despite delivering high output power levels as defined by the standard. In

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modulation schemes with higher throughput such as 1024-QAM, the separation between constellation points is reduced. This obligates a much higher in-band transmit accuracy in order to be able to achieve a communication link with a low Bit Error Rate (BER). Also, depending on the communication standard, the out-of-band spurs of the transmit signal have to be limited to avoid interference for the neighboring frequency channels. These together present significant challenges to the architecture and design of a transmitter for upcoming high-bandwidth communication standards.

The most broadly operated wireless devices, smartphones, need to support a number of well-established wireless communication standards such as WLAN, LTE, and Bluetooth, which are the most essential standards to be supported all over the world. In recent years, new standards such as UWB and, last but not least, a wide range of standards of 5G have also been introduced to the smartphone industry. Apart from these, legacy standards such as 3GPP UMTS should still be supported in a number of countries. As a result, with all these communication standards to be covered by a single mobile device, multiple transmitter systems and RFICs have been employed, each corresponding to one of the applications required. Combining a number of these transmitter systems in one single reconfigurable multi-standard system helps to reduce area, implementation efforts, cost, and power consumption significantly. For modern applications, such transmitters should be capable of providing modulation bandwidths from sub-megahertz range to several gigahertz and transmit frequencies up to the mm-wave frequency range. Furthermore, their linearity and power efficiency need to be sufficiently high to meet the requirements of the most stringent targeted communication standards and applications.

In recent decades, the CMOS technology has been scaled down from few micrometers in the 1970s to few nanometers as predicted by the Moore's law [4]. The downscaling has benefited the digital circuitry remarkably. On the one hand, smaller technology nodes allow for the integration of more digital functionalities in less die area. On the other hand, the transit frequency of devices is increased by smaller channel lengths, which results in a higher speed for Digital Signal Processing (DSP) [5]. However, for analog circuitry, nanometer downscaling is not as gainful as for digital, given that in deep-submicron technology nodes, short-channel effects such as velocity saturation get dominant with smaller gate lengths [6]. Furthermore, digital circuitry provides more flexibility and configurability, which is relevant towards Software-Defined Radio (SDR). Therefore, especially for a transmitter, it is of interest to move functionalities as much as possible into the digital domain.

The main objective of a transmitter in wireless communication is to transform the baseband signal from digital to analog domain, upconvert it to the carrier frequency, and provide a sufficient output power level while maintaining a satisfying signal quality. In a conventional transmitter system, the digital baseband data is first converted to analog through a Digital-to-Analog Converter (DAC) followed by a frequency mixer translating it to the carrier frequency and a Power Amplifier (PA) providing sufficient

output power. Typically, a number of filters are also included to suppress unwanted emissions. These include an anti-aliasing low-pass filter after the DAC, which suppresses sampling replicas of the input signal and a band-select filter at the output which suppresses out-of-band emissions. Within a reasonable area and cost criteria, these analog blocks usually do not offer much flexibility to be adapted for different applications and communication standards. Furthermore, due to their analog nature, they do not benefit from the improvements of advanced nanometer CMOS technology nodes.

In order to overcome the shortcomings of conventional analog transmitter systems in achieving flexibility and ease of integration for SDR, Digital-Centric Multi-standard Transmitters (DCMTs) have been introduced and developed widely in recent years [7, 8, 9, 10, 11, 12]. In this approach, it is attempted to push the signal processing operations as much as possible into the digital domain while the DAC and the mixer are combined in a single frontend block called Direct Digital-to-RF Converter (DDRC). As a result, the signal processing and filtering functions that are implemented in the digital domain can be adjusted and programmed according to the requirements of the communication standard. Although such structures alleviate the reconfigurability of the transmitter system, they introduce challenges to the design and implementation of the transmitter components.

### 1.1 Goal of This Work

This work aims to investigate techniques and structures to develop highly linear and power-efficient multi-standard transmitters, which can be used for advanced modulation schemes of modern wireless communication standards. Digital-Centric Multi-standard Transmitters (DCMTs) provide excellent levels of flexibility and reconfigurability for multi-standard operation. However, as mentioned earlier, they impose special requirements on the transmitter system. Hence, system design and analog implementation are both challenging to achieve decent performance, which necessitates specific techniques and solutions to be established in order to improve the weaknesses of the proposed architectures. For this reason, prototypes of DCMTs are to be designed and implemented in the target CMOS technology nodes.

In a first transmitter prototype of this work, an I/Q digital-centric Transmitter with 25% duty-cycle is developed to operate for a number of target standards such as IEEE 802.11ac 2.4 GHz band. The main focus is on the design of a current-mode 12-bit DPA with 25% duty cycle of LO signals as the DDRC. Using a high-resolution high-speed DPA requires special attention to its analog design and the implementation of the layout. The required digital signal processing steps for achieving proper performance are to be adopted and reviewed. The transmitter system design and its fabrication in a 65-nm CMOS technology

are presented and measurement results are provided to prove its feasibility and potential performance.

A main focus of this effort is to implement a complete chain of a **Multi-Level LINC (ML-LINC)** transmitter to achieve a superior linearity with the help of I/Q-based **RF-DAC** frontends. An **ML-LINC** transmitter provides a high linearity and relatively good power efficiency. As a result, it can be a good candidate for modulation schemes with a larger number of constellation points. The transmitter of this work targets to communicate data through 160-MHz channels of IEEE 802.11ac standard at its 5-GHz band. A major challenge to name is achieving outphasing vectors out of the transmitter frontend in I/Q form without losing the accuracy of the transmit signal as a result of bandwidth expansion due to Cartesian/Polar conversions of the **Signal-Component Separator (SCS)**. The Development of such a transmitter in a 28-nm **CMOS** technology with 1 V core supply voltage imposes significant challenges, especially on the design of the **RF** frontend. In this regard, systematic requirements of the transmitter to meet the specifications of target communication standards are to be derived. The different weaknesses shall be addressed and solutions need to be discussed.

## 1.2 Thesis Structure

The rest of the thesis is structured as follows.

Chapter 2 overviews the fundamentals of wireless communication. The Basics of digital wireless communications, from input data bit streams to transmission through the air channel, are shortly presented. Digital Modulation techniques such as **QAM** and **OFDM** are reviewed and multiple access techniques such as **OFDMA** and **SC-FDMA** are discussed. Next, performance metrics of a transmitter system are introduced. Finally, the characterizations of a number of key communication standards are summarized and the chapter is concluded with a brief comparison between multi-standard and single-standard systems.

Chapter 3 goes through transmitter structures and sheds light on different types of **DCMTs**. Conventional analog-intensive transmitters are briefly reviewed and their strengths are pointed out. The underlying principles of **DCMTs** are introduced and their special system requirements to incorporate **DDRCs** are presented. Also, a number of the most outstanding implementations of **DDRC** in the literature are reviewed. Next, three common transmitter system architectures of I/Q, polar, and **LINC** are studied and their benefits as well as their drawbacks are highlighted. The chapter is then concluded with a brief comparison of analog-intensive and digital-centric transmitters.

In order to develop a complete chain of a **DCMT** system, a digital part should be implemented, which receives the baseband data from off-chip and applies a number of signal

processing steps on it to be prepared for the **DDRC**. This is the focus of Chapter 4. It describes the implementation of the digital high-speed interface as well as an advanced version of it with two times faster data rates for higher-bandwidth transmit channels. Next, different upsampling and filtering blocks that are required for the **DCMT** are presented. Due to imperfections that are originated in a **DDRC**, a number of compensating steps are also described.

Chapter 5 presents **PalleonTX**, which is a prototype of a complete chain of a digital-centric I/Q transmitter. The concept and its system design are explained in detail. Then, circuit design and implementation are presented. At the end, measurement results are presented and compared to the literature.

In chapter 6, an I/Q-based **ML-LINC** transmitter, called **Chameleon**, is introduced in order to achieve a high linearity compared to the previous I/Q transmitter prototype, **PalleonTX**. According to target applications, the system design is presented and system simulations justify the adequate performance despite the imperfections of its **DDRC** frontend, which is an **RF-DAC**. The **RF-DAC** implementation and its challenges in the provided advanced 28-nm **CMOS** technology are investigated and the results are analyzed.

Finally, the thesis is concluded in chapter 7 with a brief summary of what has been done and presented.

# Chapter 2

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## Fundamentals of Wireless Communication for Transmitters

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Each transceiver system is based on certain communication concepts. In order to develop a transmitter system, which is the scope of this work, one needs to review the underlying communication theory behind it in the first place. For this purpose, this chapter describes a number of essential concepts of wireless transmission, which have evolved tremendously through ages. Section 2.1 reviews how a bit stream of data is processed and modulated and how a transmitter uses the transmission channel through different access techniques. In section 2.2, the main performance metrics of a transmitter system are presented. Finally, section 2.3 goes through a number of common wireless standards and reviews the requirements of a transmitter system operating under these specific standards.

### 2.1 Digital Wireless Transmission

A transmitter receives a bit stream of data and needs to send it over the air transmission interface through the antenna in a way it can be received as error-free as possible by receivers. For this purpose, in the first step, each  $N$  bits of the incoming input data stream are grouped together to form a Symbol. In this way, each symbol carries information of  $N$  data bits, which results in  $2^N$  different states [13]:

$$\begin{aligned} \text{bit stream: } b_{data} = \{b_1, b_2, \dots, b_K\} \implies \text{symbol stream:} \\ \begin{aligned} s_1 &= \{b_1, b_2, \dots, b_N\}, \\ s_2 &= \{b_{N+1}, b_{N+2}, \dots, b_{2N}\}, \\ &\vdots \\ s_{K/N} &= \{b_{K-N+1}, b_{K-N+2}, \dots, b_K\}. \end{aligned} \end{aligned} \quad (2.1)$$

Such a symbol manipulates one of the three parameters of a carrier signal which are  $A(t)$ ,  $\omega(t)$ , and  $\phi(t)$ :

$$s(t) = A(t)\cos(\omega(t)t + \phi(t)). \quad (2.2)$$

In other words, each symbol modulates the carrier signal by changing its amplitude, frequency, or phase in a way that it can be detected on the receiver side.

### 2.1.1 Digital Modulation

The simplest digital modulation schemes are achieved when only one of these three is affected by symbol states. This results in one of [Amplitude Shift Keying \(ASK\)](#), [Frequency-Shift Keying \(FSK\)](#), and [Phase-Shift Keying \(PSK\)](#), which are corresponding to changes in amplitude, frequency, and phase, respectively. However, there exists also more complex modulation schemes that are resulted from combining these three. A few of such modulations are described in the following sections.

#### 2.1.1.1 Quadrature Amplitude Modulation (QAM)

[Quadrature Amplitude Modulation \(QAM\)](#) is a family of the most widely used digital modulation schemes, which can provide a rather high data throughput by combining [ASK](#) and [PSK](#) in a Cartesian coordinate. Such 2-dimensional symbols can be constructed on two carrier signals with a 90-degree phase shift, which are mathematically orthogonal and provide the coordinate axes. In this way, the output [RF](#) signal is resulted by:

$$V(t) = S_I(t)\cos(\omega_c t) + S_Q(t)\sin(\omega_c t), \quad (2.3)$$

where  $\omega_c$  is the carrier angular frequency and  $S_I(t)$  and  $S_Q(t)$  are the in-phase and the quadrature components of the symbols, respectively [13]. Such symbols are commonly represented by a complex notation:

$$S(t) = S_I(t) + j \cdot S_Q(t). \quad (2.4)$$

As a result, by a multi-level [ASK](#) modulation with  $K$  states for each of the two carriers,  $M = K^2$  symbol states are achieved, which results in an [M-QAM](#) modulation. Fig. 2.1 shows a so-called constellation diagram of a [16-QAM](#) modulation scheme where all possible states are plotted in the complex plane with In-phase (I) and Quadrature (Q) components as the axes. If a coding rate of 1 is applied, each 4-bit packet of the incoming data stream is mapped to one of these symbol states of the depicted [16-QAM](#).

Obviously, a higher-order [QAM](#) modulation scheme such as [64-QAM](#), [256-QAM](#), or [1024-QAM](#) results in much higher data throughputs. However, for a given transmit power, a higher number of constellation points makes the detection more sensitive to noise as these points are closer to each other [14]. Therefore, it requires a better performance out of the transceiver system, most importantly, a higher [SNR](#) of the transmitted signal.

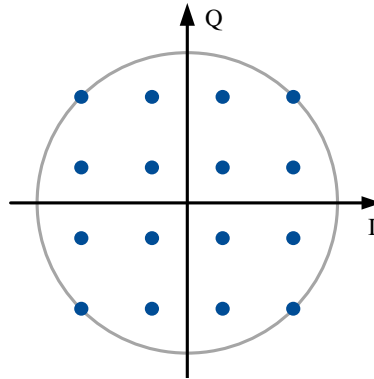


Figure 2.1: 16-QAM constellation diagram.

### 2.1.1.2 Orthogonal Frequency-Division Multiplexing (OFDM)

The transmitted RF signal propagates to the receiver through the air interface. As a result, it is transferred through not only one path but numerous of paths, which leads to producing various propagated versions of the signal with different delay and attenuation characteristics [15]. Such a multipath fading introduces distortion and **Inter-Symbol Interference (ISI)** to the transmitted data [13]. Furthermore, the Doppler frequency shift of a moving object contributes to the signal distortion by shifting the carrier frequency. This leads to a partially random envelope of the received signal [16]. In order to reduce the error rate due to multipath fading and Doppler effects as well as to construct a more robust communication, the symbol time should be sufficiently long. Consequently, a higher symbol rate cannot be achieved with simple one-carrier modulations such as QAM.

**Orthogonal Frequency-Division Multiplexing (OFDM)** introduces the possibility to transfer a number of symbols in parallel, leading to higher data rates while benefiting the reliability of long symbol times [13]. For this purpose, a certain number of symbols with different modulation schemes such as QAM are clustered together:

$$S = [S_{-N_s/2}, \dots, S_{-1}, S_0, S_1, \dots, S_{N_s/2}] , \quad (2.5)$$

where  $N_s$  represents the number of these so-called subsymbols. The subsymbols are then assigned to a set of the same number of subcarriers with a fixed frequency distancing between them. As a result, the achieved OFDM signal can be expressed as the sum of all subsymbols mixed with their corresponding subcarrier:

$$S(t) = \Re \left\{ \sum_{k=-N_s/2}^{N_s/2} S_k \cdot e^{j2\pi f_k t + \phi_k} \right\} , \quad (2.6)$$

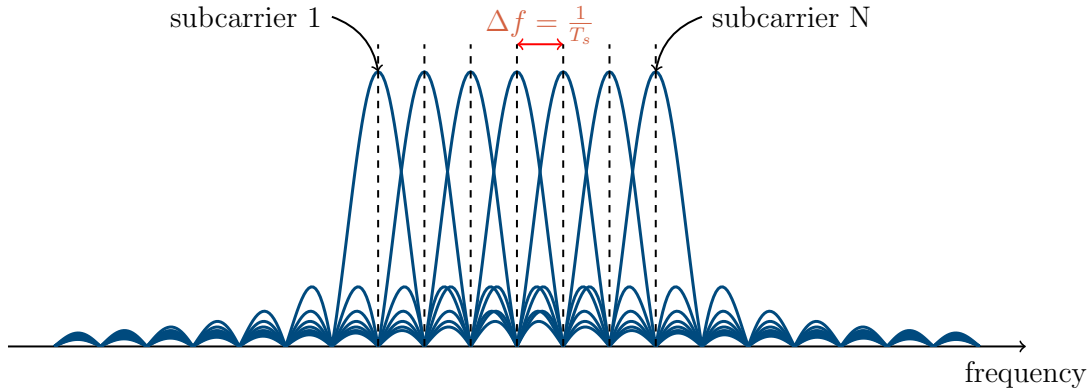


Figure 2.2: Orthogonality of sinc waveforms of OFDM subcarriers.

where  $f_k$  and  $\phi_k$  are the frequency and phase of the  $k^{th}$  subcarrier. It can be noticed that (2.6) resembles **Inverse Fast Fourier Transform (IFFT)** on the set of subsymbols. Therefore, in order to implement such a modulation, **IFFT** is commonly used in the **DSP**. This is more practical than using an I/Q mixer for mixing each subsymbol with its corresponding subcarrier.

Each subcarrier carrying a subsymbol will be seen as a sinc function in the frequency domain. Consequently, the **OFDM** signal is constructed out of a number of sinc waveforms with the same center frequencies of subcarriers. The amplitude and the phase of each sinc function depend on its corresponding subsymbol and its modulation. In order to receive this signal correctly and detect each subsymbol without **Inter-Channel Interference (ICI)**, the subcarriers should be orthogonal to each other [17]. This can be simply guaranteed by selecting the frequency spacing of the subcarriers to be:

$$\Delta f = \frac{1}{T_s}, \quad (2.7)$$

with  $T_s$  representing the symbol time. Fig. 2.2 shows a number of orthogonal subcarriers. Although these subcarriers are overlapping in the frequency domain, the sinc function of the other subsymbols will be zero at each subcarrier center frequency.

As mentioned earlier, the existence of different transmission paths of the signal leads to an unknown spread of delay at the receiver side. Since a delay of the signal in the time domain appears as a rotation in the frequency domain, the whole **OFDM** symbol at the **RX** will be a sum of differently attenuated rotated versions of the transmitted signal in the frequency domain. As a result, the signal in the frequency domain is received with a transfer function out of all these paths and the correct signal can still be obtained. However, as the stream of **OFDM** symbols has discontinuity at the end of each symbol in the time domain, the sampling window at the receiver side cannot observe the complete

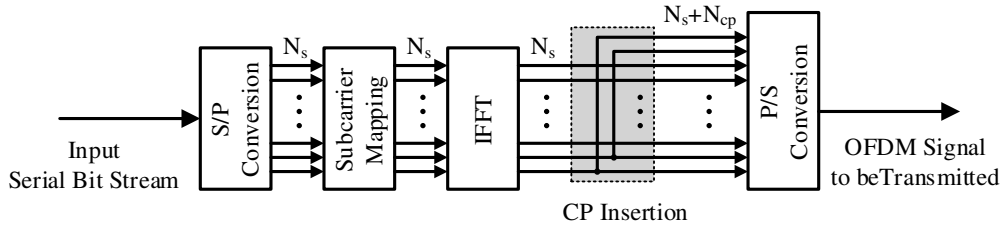


Figure 2.3: Construction of an OFDM signal through IFFT.

cycle of all delayed versions of the symbol. In order to solve this problem, a part of the end of each OFDM symbol is appended to its beginning so that even the most extreme delayed versions still include one complete cycle of that symbol in the FFT sampling window. This additional Guard Interval (GI), which prevents ISI by extending each OFDM, is also called **Cyclic Prefix (CP)** [13]. Fig. 2.3 depicts the creation of an OFDM signal. The bit stream is first converted into parallel groups of bits, which are then mapped to subsymbols. In the next step, the OFDM time-domain signal, which is also called an OFDM symbol, is generated by applying IFFT on the subsymbols. The resulting signal is then extended through CP and it is then mixed up with the carrier signal like single symbols.

One of the main disadvantages of OFDM-based transmitter systems is the high **Peak-to-Average Power Ratio (PAPR)** of the transmitted signals. For a single complex sinusoidal signal of  $Ae^{j \cdot 2\pi f_k t}$ , the average signal power and the maximum signal power are both  $A^2$ , which results in a PAPR of 0 dB [15]. This is the case for single-carrier constant-envelope modulations such as QPSK. If instead of a constant amplitude, it is modulated by  $A(t)$ , the average power,  $A_{rms}^2$ , depends on the characteristics of  $A(t)$  while the peak power remains the same as  $A_{max}^2$ . On the other hand, for an OFDM signal constructed out of  $N_s$  subcarriers, the maximum power occurs in the case that all subcarriers have the same amplitude at its maximum, resulting in a power of  $N_s \cdot A_{max}^2$  [18]. However, this case is clearly rare while most of the time the signal power is around the average, which depends on the statistics of subcarriers' modulations. This leads to a relatively high PAPR proportional to  $N_s$ , which is for example round 15 dB for  $N_s \geq 64$  in a WLAN transmission [13]. Such a high PAPR requires a highly linear RF frontend with a large dynamic range to cover this signal power difference accurately.

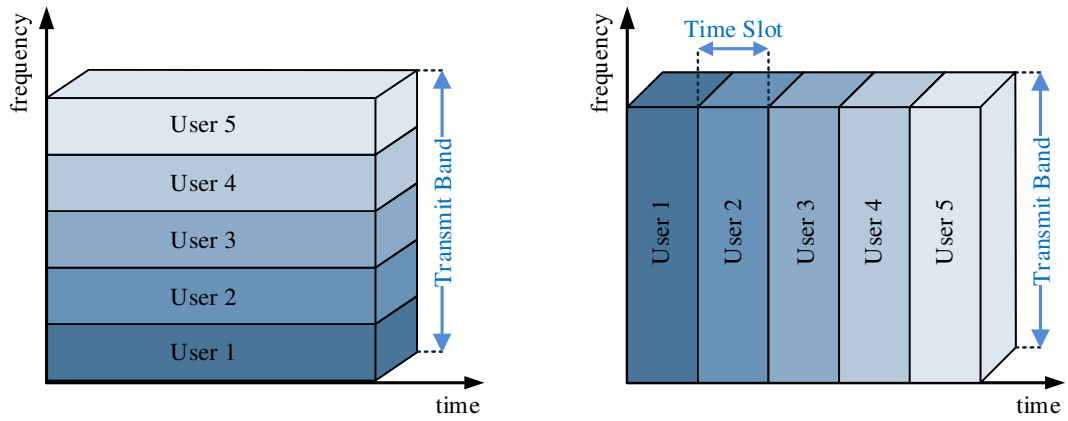
### 2.1.2 Multiple Access Schemes

In order to allow multiple transceivers to communicate in parallel, a so-called multiple access scheme should be adopted. This section first describes the long-established multiple-access techniques, which are required to understand basics of a communication system.

The simplest multiple access technique, which is the basis of cellular networks, is **Frequency-Division Multiple Access (FDMA)**, where different users communicate in separate frequency channels of the electromagnetic spectrum constructed by a range of selectable carrier frequencies. Fig. 2.4a illustrates this technique. The channel allocated to each transmitter remains the same and does not change with time until its corresponding communication is terminated and the channel becomes available to other users [14]. With **FDMA**, a problem that might occur is interference from each transmitter to other channels due to finite filtering attenuation at the edges of the transmit channel. This is characterized by **Figure of Merits (FoMs)** such as **Adjacent Channel Leakage Ratio (ACLR)** and **Alternate Channel Leakage Ratio (AltCLR)**, which are described later in section 2.2.

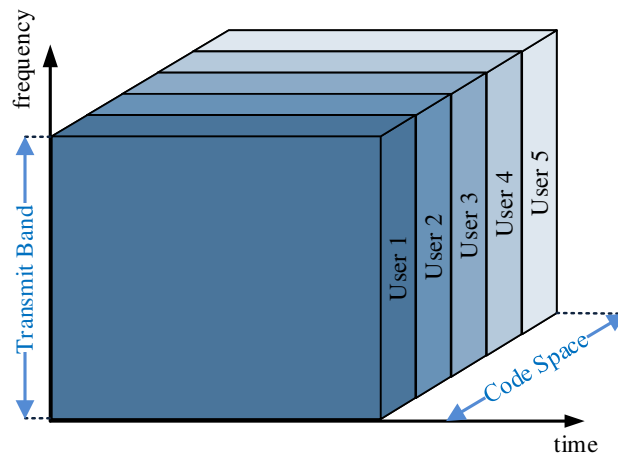
Another access scheme, shown in Fig. 2.4b, is **Time-Division Multiple Access (TDMA)** in which each transmission is scheduled to be performed during specific non-overlapping time intervals. In other words, each of the transceivers is allowed to use the same frequency band for a specific time slot, which is usually granted to them periodically [14]. A sync command synchronizes all stations to send data in subsequent time slots of a frame. After sending data, each station has to wait until its allocated time slot in the next frame. A **Guard Interval (GI)** might be integrated after each time slot so that problems with timing uncertainty and random multipath propagation delays as well as issues with settling of the power through ramping it down and up are avoided [13].

As shown in Fig. 2.4c, **Code-Division Multiple Access (CDMA)** is another multiple access method to share a frequency channel simultaneously between several users by using a set of orthogonal codes. It is based on a **Direct Sequence Spread Spectrum (DSSS)** technology, which spreads the signal over a much wider bandwidth than its own bandwidth by coding it. Each code, which is also called the spreading sequence, is assigned specifically to a pair of transmitter and receiver. The signal can be decoded only when the receiver uses the same code as the one used by the transmitter. When the spreading sequence, which consists of a number of higher-frequency pulses, called chips, is mixed with the transmit signal, it spreads the signal over a wider frequency bandwidth. On the receiver side, there would be many spread-spectrum signals from different transmitters in the network. However, only the signal which corresponds to the same spreading sequence as the receiver is decoded and demodulated, while due to orthogonality of the codes, rest of the signals are not decoded and their spread spectrum signals only contribute to increasing the noise floor. An advantage of **CDMA** is its possibility of changing the user capacity, whereas in **TDMA** and **FDMA** techniques, the maximum number of users is fixed [14]. However, with a high number of users, the near/far interference effect is more severe than that of other multiple access schemes. This requires a precise power control to reduce the power of interfering closer transmitters so that all signals are received with similar power levels [19].



(a) Frequency-Division Multiple Access (FDMA)

(b) Time-Division Multiple Access (TDMA)



(c) Code-Division Multiple Access (CDMA)

Figure 2.4: Illustration of conventional multiple access schemes.

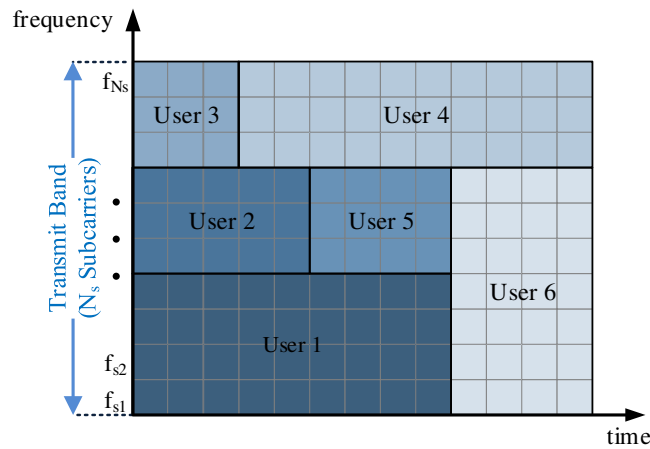


Figure 2.5: Allocation of subcarriers to different users in an OFDMA system.

### Orthogonal Frequency-Division Multiple Access (OFDMA)

Orthogonal Frequency-Division Multiple Access (OFDMA) is a variant of FDMA access technique where a subset of OFDM subcarriers are assigned to each user. The whole transmit band is composed of orthogonal OFDM subcarriers and a number of them are assigned to each user depending on its bandwidth. As depicted in Fig. 2.5, thanks to orthogonality of the subcarriers, signals of different users can be modulated on adjacent groups of subcarriers with no much additional spacing. Only a few null subcarriers are used as guard bands at the edges of the modulated data spectrum to reduce adjacent channel interference and out-of-band emissions [20]. This provides a flexible bandwidth selectivity for each user as well as a much more efficient use of the transmit band, in contrast to a channelized FDMA system where users are assigned to fixed frequency channels with sufficient spacing in between them.

A challenge in OFDMA is that the orthogonality of subcarriers needs to be guaranteed. This requires extensive synchronization between all the transmitters in the system, which is not feasible in practice. As a result, the use of OFDMA is reasonable only when the subcarriers are generated through the same transmitter. This is the case for downlink transmissions of base stations in LTE [21].

### Single Carrier – Frequency Division Multiple Access

Single Carrier – Frequency Division Multiple Access (SC-FDMA) is a variant of OFDMA where the high PAPR of OFDM signals is avoided by scrambling subcarriers. In other words, a spreading technique is employed by applying DFT on symbols before IFFT. As a result, DFT and IFFT virtually cancel each other out and a lower PAPR similar to that

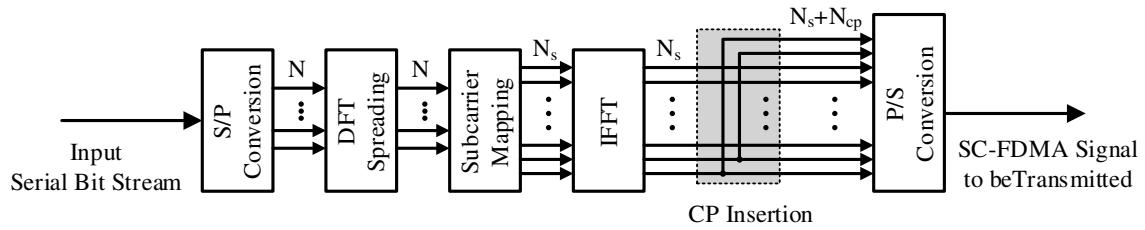


Figure 2.6: Construction of an SC-FDMA signal.

of a single-carrier modulation is achieved [17]. Fig. 2.6 shows the construction of an SC-FDMA signal. All the  $N$  parallel symbols go through an  $N$ -point DFT. The result is then mapped to  $N$  subcarriers assigned to the user out of all  $N_s$  available ones of the whole transmit band and other subcarriers are filled with zero. Similar to OFDM, subcarriers are converted back to time domain through IFFT and a CP is inserted as GI. In this way, each subcarrier carries a combination of components of all data symbols [22].

However, the main drawback of SC-FDMA is that it requires intensive signal processing at both of transmit and receive sides [21]. Furthermore, PAPR reduction also depends on subcarrier mapping to users. It can be proved that in case a uniformly distributed mapping is applied, a lower PAPR can be achieved compared to a localized mapping, where all subcarriers of a user are assigned next to each other [17].

SC-FDMA is used for uplink communication in LTE, where lower PAPR helps designing efficient PAs for mobile stations.

## 2.2 Performance Metrics

In order to be able to evaluate the performance of a system, a number of performance metrics are introduced. This section describes the most relevant ones for a transmitter system.

### Output Power and Efficiency

Each transmitter system is required to be able to transmit an output signal with a sufficiently high power level that can be received with a sufficiently low error rate at the furthest distance possible according to the standard. Furthermore, depending on the modulation scheme, it might need to adjust its power in fine steps across a defined range. As a result, performance metrics such as a maximum allowed output power, a minimum

power, a power control range, and a power control resolution might be specified for a transmitter according to its intended application.

Since the **Power Amplifier (PA)** of a transmitter is the most power-hungry part of the whole communication system, it needs to meet required levels of efficiency. There are a number of different **Figure of Merits (FoMs)** defined for the power efficiency of a transmitter. The drain efficiency is defined as:

$$\eta_{drain} = \frac{P_{out}}{P_{supply,pa}}, \quad (2.8)$$

where  $P_{out}$  is the transmitted signal power and  $P_{supply,pa}$  is the **DC** power consumption of the output stage of the **PA**. Taking the whole power of the transmitter system into account, system efficiency is similarly defined as:

$$\eta_{system} = \frac{P_{out}}{P_{supply,sys}}. \quad (2.9)$$

Another efficiency measure, which is mostly relevant to the **PA** by taking its input power as well, is the **Power-Added Efficiency (PAE)**:

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{P_{supply,PA}}. \quad (2.10)$$

## Linearity

In modulation schemes with higher throughput, envelope modulation is typically inevitable and as a result, the RF frontend is required to be highly linear to transmit the signals accurately. Few **FoMs** are defined for assessing the linearity. 1 dB compression point, denoted by  $P_{1dB}$ , is the output power where it drops by 1 dB compared to the linearly extrapolated output power. When it comes to the distortion behaviors of the output signal, third intercept points for output and input are defined, which are denoted by **OIP3** and **IIP3**, respectively.  $P_{OIP3}$  is the output power where the linearly-extrapolated third-order intermodulation product of the output signal, IM3, reaches that of the output signal fundamental component. The input power at this point is denoted by  $P_{IIP3}$ , which is relevant for **PAs** with analog input. These performance metrics are listed below:

$$P_{1dB} = P_{out} |_{P_{out}=P_{out,linear}-1dB}, \quad (2.11)$$

$$P_{OIP3} = P_{out} |_{P_{IM3}=P_{fundamental}}, \quad (2.12)$$

$$P_{IIP3} = P_{in} |_{P_{IM3}=P_{fundamental}} \cdot \quad (2.13)$$

## Error Vector Magnitude

**Error-Vector Magnitude (EVM)** is an FoM used to determine the in-band performance of a transmitter by evaluating the accuracy of symbol transmissions. Considering an I/Q constellation plane, EVM shows the extent of vector deviation of the sampled symbols at the output of a transmitter to their corresponding ideal symbol vectors. As a result, it is affected by noise, nonlinearity, and interference. The RMS value of EVM, which is typically expressed in percentage or dB, is achieved by normalizing the average power of error vectors to the average power of ideal symbol vectors over a certain number of symbols of length N:

$$EVM_{RMS} = \sqrt{\frac{\frac{1}{N} \sum_{k=1}^N |S_{ideal,k} - S_{real,k}|^2}{\frac{1}{N} \sum_{k=1}^N |S_{ideal,k}|^2}}. \quad (2.14)$$

## Power Leakage and Spectral Mask

Unwanted emissions of a transmitter due to its nonlinearity might cause interference and disturb signals of adjacent channels or even other bands. Therefore, it is necessary to limit such unwanted radiations of each transmitter. In practice, most communication standards specify a transmission spectral mask that must not be exceeded by the **Power Spectral Density (PSD)** of the transmitted signal. The mask is generally specified depending on the frequency offset from the desired signal channel. Fig. 2.7 illustrates this with the spectral mask for a 5 MHz channel in FDD mode of UMTS for User Equipment (UE) [23].

In addition to the PSD limitation introduced by the spectral mask, power leakage ratios to the neighboring channels are also commonly used to assess the disturbance to other channels. **Adjacent Channel Leakage Ratio (ACLR)** specifies the ratio of signal power in the adjacent channels to the signal power in the desired channel:

$$ACLR = \frac{P_{adj,ch}}{P_{main,ch}}. \quad (2.15)$$

If instead of the adjacent channels, the next alternative channels are taken into account,

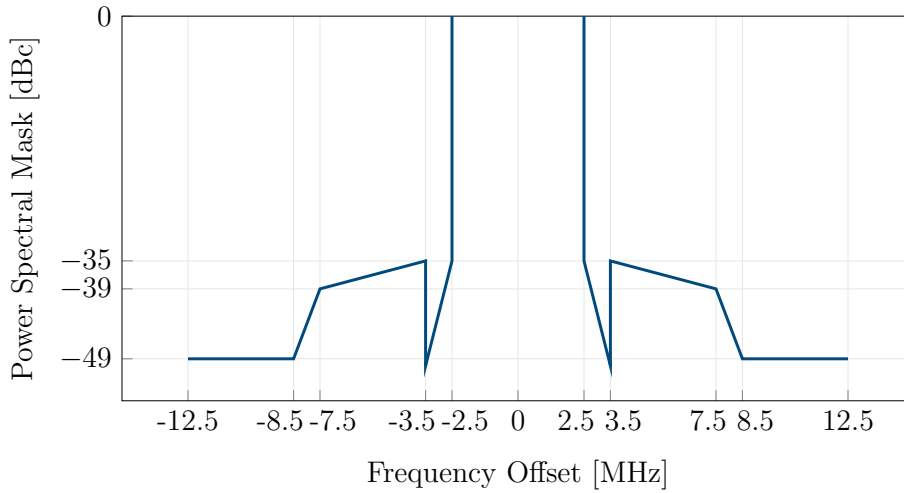


Figure 2.7: Spectral mask requirement of UMTS FDD for UE.

it is denoted as **Alternate Channel Leakage Ratio (AltCLR)**:

$$AltCLR = \frac{P_{alt,ch}}{P_{main,ch}} . \quad (2.16)$$

## 2.3 Wireless Standards

A multi-standard transmitter, which is targeted in this work, needs to provide the most stringent performance requirements of communication standards for which it is employed. Although such a transmitter is typically used to cover modern high-data-rate communication standards such as **LTE** and advanced **WLAN** standards, it needs to cope with the legacy ones such as **3GPP UMTS** as well. As a result, a benchmark out of a combination of all requirements is set, which must be met by the transmitter system. In order to give an insight into such requirements, those of **WLAN** and **LTE** are discussed in the following sections.

### 2.3.1 WLAN

The IEEE 802.11 family of **Wireless Local-Area Network (WLAN)** [24] is a common standard with strict requirements for which multi-standard transceiver systems can be employed. It provides a high data rate within a limited area, which is of interest for computer and internet networks as well as high-speed cyber-physical systems. **WLAN** consists of a number of different categories of specifications for **Physical Layer (PHY)** and **Modulation and Coding Scheme (MCS)**, of which those of **IEEE 802.11g** and **802.11n** based

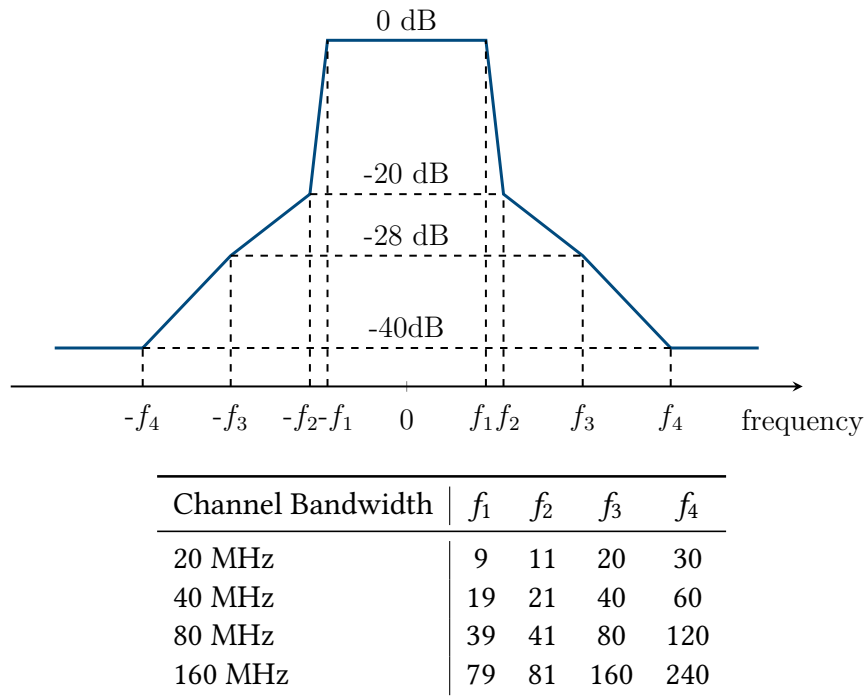


Figure 2.8: The spectral mask requirements of the **WLAN** standard with different channel bandwidths.

on **OFDM** with 20 MHz bandwidth are the most common for high-throughput networks. In general, **WLAN** standard imposes strict **EVM** requirements for the transmitted signal, especially for **MCSs** with higher data rates. For the power specifications, it does not demand requirements on power control and minimum power. However, the **Effective Isotropically Radiated Power (EIRP)** of the antenna should not exceed 20 dBm for 2.4 GHz band while there are different **EIRP** requirements for different sub-bands of the 5 GHz band. Besides, the **WLAN** spectrum mask, shown in Fig. 2.8, is not very strict compared to **LTE**.

### **IEEE 802.11g**

**IEEE 802.11g** amendment [25] uses 64-**QAM OFDM** signals transmitted at 2.4 GHz **ISM** band. **OFDM** of **IEEE 802.11a/g** is composed of 64 subcarriers, including 4 pilot subcarriers with **BPSK** signals and 48 data subcarriers, each transferring a signal with **BPSK**, **QPSK**, 16-**QAM**, or 64-**QAM** depending on the **MCS** index as listed in table 2.1. The remaining 12 switched-off subcarriers include the one at the center of the channel, which guarantees a **DC-free** transmission, and 11 subcarriers at the edge of the channel as guard bands, which allow for enough frequency spacing to attenuate the shoulders of the channel and reduce **ACLR**. The subcarriers are spaced with a frequency distance of 312.5 kHz across

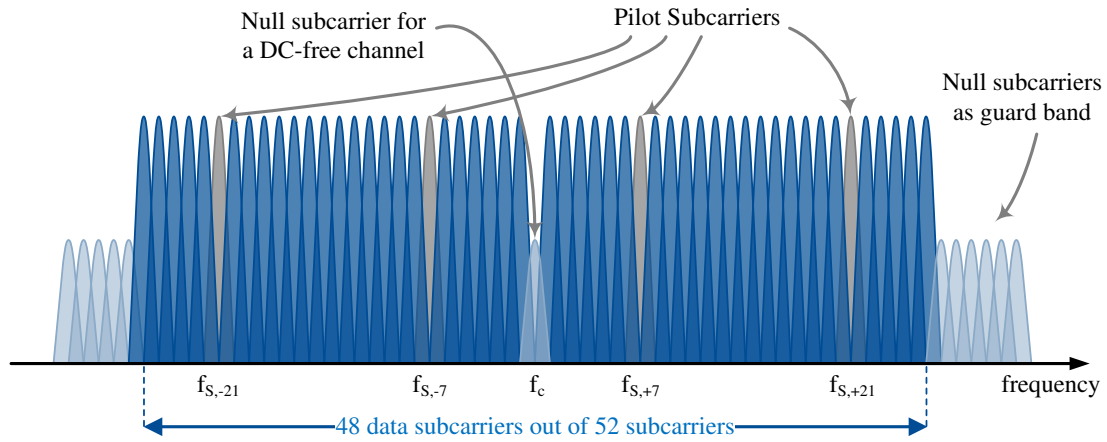


Figure 2.9: Arrangement of OFDM subcarriers in a 20 MHz channel of IEEE 802.11g.

the channel. As a result, the signal bandwidth consisting of 52 signal subcarriers and the null subcarrier at position 0 takes up to 16.6 MHz out of the 20 MHz bandwidth of the channel. Fig. 2.9 illustrates such an arrangement of subcarriers for IEEE 802.11a/g.

As described in section 2.1.1.2, the OFDM symbol can be achieved by using IFFT in the DSP. As a result, the whole OFDM data symbol time is  $1/312.5kHz$ , which is  $3.2 \mu s$ . Additionally, a guard interval of  $0.8 \mu s$  is considered to guarantee a low Inter-Symbol Interference (ISI) transmission of symbols.

Evidently, the maximum data rate of 802.11g is achieved with 64-QAM and a coding rate of 3/4:

$$\begin{aligned}
 R_{max} &= 6 \times 3/4 \frac{Bit}{Constl. Symbol} \times 48 \frac{Constl. Symbol}{OFDM Symbol} \times \frac{1}{4} \frac{OFDM Symbol}{\mu s} \\
 &= 54 Mbit/s .
 \end{aligned}
 \tag{2.17}$$

The other achievable data rates of WLAN with different settings, which are given in table 2.1 can be calculated similarly.

### IEEE 802.11n

IEEE 802.11n amendment [26], also known as the fourth generation WLAN, requires the use of the same 20 MHz channels of IEEE 802.11g operating at the legacy WLAN 2.4 GHz band and, alternatively, introduces support for optional 40 MHz channels and 5 GHz band. Furthermore, it allows using up to 4 antennas through Multiple-Input Multiple-Output (MIMO) technique in addition to employing frame aggregation in the Media Access Control (MAC) layer, which reduces the framing overhead to the user data.

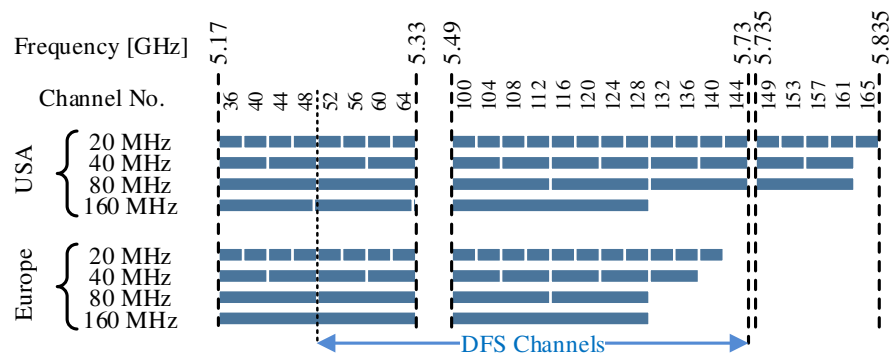


Figure 2.10: IEEE 802.11ac channel map of USA and Europe.

Furthermore, the guard interval of OFDM frames can be reduced to  $0.4 \mu\text{s}$  by operating in the short frame mode. These amendments, all together, allow for much higher data rates up to 600 Mbit/s. In a 20 MHz channel, the signal is transferred through 56 subcarriers, including 52 data subcarriers and 4 pilots, while the 8 remaining ones are switched off. With 4 additional data subcarriers as well as using 5/6 coding rate of 64-QAM, the data rate can be increased up to 72.2 Mbit/s compared to 54 Mbit/s of IEEE 802.11g. When 40 MHz channels are used, out of 128 subcarriers, 108 ones are assigned for data symbols, 6 subcarriers for pilots, and 14 subcarriers are switched off. This results in a maximum data rate of 150 Mbit/s per each 40 MHz channel with 64-QAM and a coding rate of 5/6. Clearly, with 4 spatial streams of MIMO, this can be increased to 600 Mbit/s.

### IEEE 802.11ac

IEEE 802.11ac [27], which operates only at the 5 GHz band, extends the data rates by introducing 80 MHz and 160 MHz channels as well as by supporting 256-QAM signals. Moreover, the number of spatial streams is increased from 4 to 8 while allowing multi-user transmission up to 4 users. As a result, by using 468 data subcarriers in a 160 MHz channel, the data rate can be scaled up to 866.7 Mbit/s for a single spatial stream, resulting in 6933.7 Mbit/s when all of 8 spatial streams are used. However, the number of non-overlapping higher bandwidth channels are limited. Fig. 2.10 depicts the channels of IEEE 802.11ac in the USA and Europe. Focusing on the 5 GHz channels in Europe, there are two sub-bands defined, which are RLAN band 1 from 5.17 GHz to 5.25 GHz and RLAN band 2 from 5.49 GHz to 5.73 GHz. In total, it can be configured in Europe to occupy non-overlapping channels out of nineteen 20-MHz channels, nine 40-MHz channels, or four 80-MHz channels, while there are only two 160-MHz channels available.

Table 2.1: Data rates and EVM requirements of WLAN configurations.

MCS	Modulation	Coding Rate	EVM [dB]	Maximum data rate for a single spatial stream [Mbit/s]									
				802.11a/g		802.11n				802.11ac			
				20 MHz 48 SC	20 MHz 52 SC	20 MHz 52 SC	40 MHz 108 SC	40 MHz 108 SC	20 MHz 52 SC	40 MHz 108 SC	80 MHz 234 SC	80 MHz 234 SC	160 MHz 468 SC
0	BPSK	1/2	-5	6	7.2	15	15	15	15	7.2	15	32.5	65
1	QPSK	1/2	-10	12	14.4	30	30	30	30	14.4	30	65	130
2	QPSK	3/4	-13	18	21.7	45	45	45	45	21.7	45	97.5	195
3	16QAM	1/2	-16	24	28.9	60	60	60	60	28.9	60	130	260
4	16QAM	3/4	-19	36	43.3	90	90	90	90	43.3	90	195	390
5	64QAM	2/3	-22	48	57.8	120	120	120	120	57.8	120	260	525
6	64QAM	3/4	-25	54	65	135	135	135	135	65	135	292.5	585
7	64QAM	5/6	-27	-	72.2	150	150	150	150	72.2	150	325	650
8	256QAM	3/4	-30	-	-	-	-	-	-	86.7	180	390	7850
9	256QAM	5/6	-32	-	-	-	-	-	-	-	200	433.3	866.7

Table 2.2: LTE channels.

Channel Bandwidth [MHz]	1.4	3	5	10	15	20
Sampling Frequency [MHz]	1.92	3.84	7.68	15.36	23.04	30.72
Number of RBs	6	15	25	50	75	100
Transmission Bandwidth [MHz]	1.08	2.7	4.5	9	13.5	18
Data Subcarriers	72	180	300	600	900	1200
FFT Size	128	256	512	1024	1536	2048

### 2.3.2 Long-Term Evolution

UMTS Long-Term Evolution (LTE) [28], commonly shorted to LTE, is the 4th generation of 3GPP mobile network technologies and is denoted by 4G. Through its air interface, called Evolved UMTS Terrestrial Radio Access (E-UTRA), LTE provides much more efficient data communication with higher data rates and reduced latency compared to its legacy UMTS of 3G. It uses OFDMA for the downlink transmission, where data is transmitted from base stations to User Equipments (UEs). Since OFDMA requires the use of a highly linear PA due to its high PAPR, SC-FDMA is used for the uplink transmissions, which results in a better cell-edge performance as well as a much lower PAPR while allowing for a much more power-efficient PA in the UE. Besides, LTE supports both FDD and TDD modes of operation. TDD brings a number of advantages such as changing the uplink/downlink capacity ratio dynamically according to demand as well as supporting legacy TD-SCDMA operators. However, FDD is the most widely used duplexing mode in LTE, which is reviewed here.

In the FDD mode, data is transferred within frames of 10 ms, each consisting of ten sub-frames, which are themselves divided into two slots of 0.5 ms. Each slot is structured by Resource Blocks (RBs), which is shown in Fig. 2.11. Each RB consists of 12 subcarriers with a frequency spacing,  $\Delta f$ , of 15 kHz, occupying an overall bandwidth of 180 kHz. As a result, each data symbol has a duration of  $1/\Delta f$ , which is  $66.7 \mu\text{s}$ . In the normal mode, an RB consists of 7 symbols per subcarrier, while it is reduced to 6 symbols in the extended Cyclic Prefix (CP) mode. The smallest unit of an RB, which is called a Resource Element (RE), consists of a subcarrier during one symbol duration. Each subcarrier carries QPSK or 16-QAM modulated symbols and should meet EVMs of 17.5 % or 12.5 %, respectively. A number of RBs are put together in the frequency domain to form channels with different bandwidths. For example, a 20 MHz channel of LTE consists of 100 RBs, which occupy 18.015 MHz of the channel bandwidth together with the DC subcarrier. These configurations of different defined channel bandwidths are listed in table 2.2.

Fig. 2.12 shows the spectral emission mask of a 20 MHz channel for the uplink. The output power is defined to be in the range of  $-40 \text{ dBm}$  to  $23 \text{ dBm}$  with minimum power

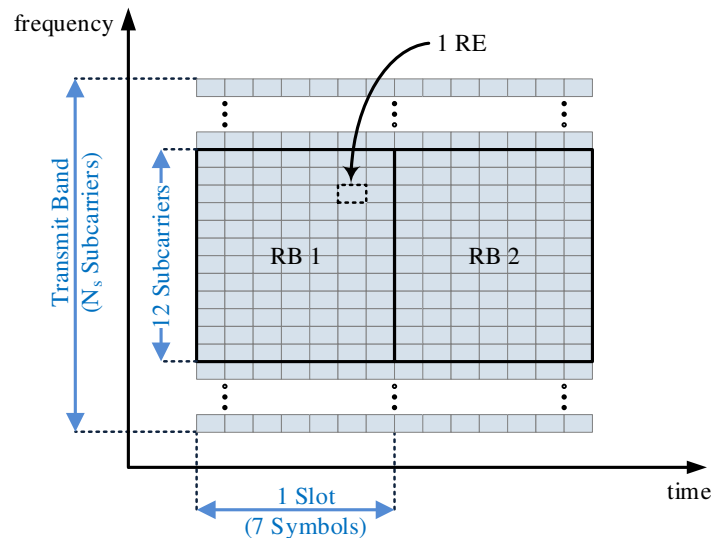


Figure 2.11: The structure of an RB in LTE.

control steps of 2 dB, which is relatively relaxed [16]. The LO leakage must be limited to  $-25$  dBc for output levels higher than 0 dBm,  $-20$  dBc for output powers between  $-30$  dBm and 0 dBm, and  $-10$  dBc for output levels smaller than  $-30$  dBm.

### 2.3.3 Multi-Standard Vs. Single-Standard

Since the beginning of radio transmission, transceiver systems have been developed to work under specific standards. However, with advances in modern CMOS technologies, particularly with higher speed DSP possibilities, digitally-assisted multi-standard radios that alleviate moving towards Software-Defined Radio (SDR) have emerged. Multi-standard operation requires the system to be highly configurable in order to be able to switch into different modes and fulfill requirements of all target standards. These systems typically benefit from easier reconfigurability, higher speed, and lower power consumption of digital circuitry by pushing more and more functions of the conventional bulky, power hungry, and less reconfigurable analog components into the digital domain. However, this usually brings up a number of challenges which might result in a degraded transceiver performance if not dealt with properly.

A radio system should meet several criteria to be used as a multi-standard system. In the first place, all components should be able to work in all the targeted frequency bands. This requires the components operating at RF to be either sufficiently wideband to cover the whole frequency range or to be switchable for different bands with a reasonable area overhead. Furthermore, different targeted standards use various sets of modulation

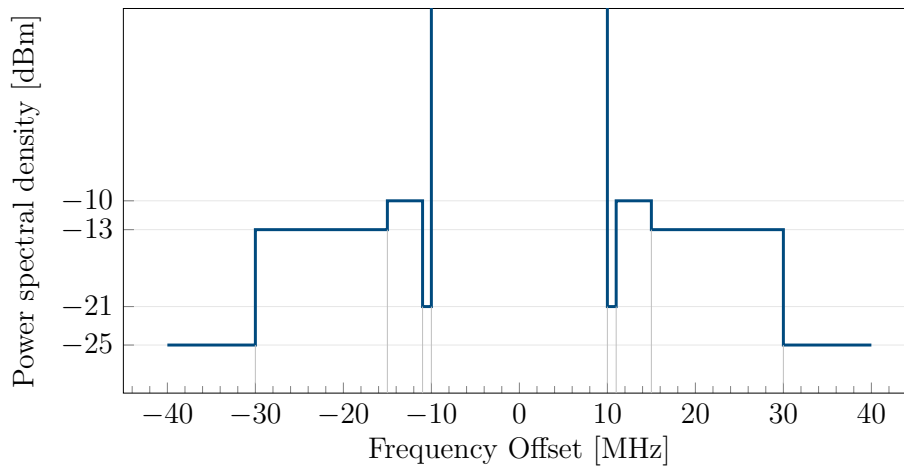


Figure 2.12: The spectral emission mask of a 20 MHz channel of LTE.

schemes and data rates, which need to be all supported by DSP. This further demands flexibility of the DSP to support different sampling rate conversions as well as to process different schemes for modulation or demodulation of the transmitted or received data.

Besides, since even in the most advanced digital-centric systems, the use of analog components such as RF frontends or ADCs is not avoidable, they also need to provide a level of configurability to be capable of adapting to the requirements of targeted standards. Furthermore, the Performance requirements and figure of merits of all standards should be met. This requires that the RF system can achieve the most stringent requirements of each of the standards. For instance, a multi-standard transmitter that is designed for WLAN, 3GPP UMTS, and 3GPP LTE should be able to meet the strict EVM requirements of WLAN, the power control requirements of UMTS, and the tight ACLR requirements of LTE [16].

A multi-standard system brings several benefits while introducing new challenges as well. An important benefit of multi-standard transceivers is reducing the number of chips included in a specific device, which results in a much more efficient use of available space. Such a reconfigurable system can be used for a number of initially targeted standards, while it might also be able to support other communication configurations thanks to its DSP flexibility. However, designing for more flexibility increases the complexity, area, and power consumption of the system. This also requires more time for design and verification before tapeout as well as more time for validation of the sample ICs in the laboratory.



# Chapter 3

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## Transmitter Architectures for Multi-Standard Systems

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This chapter gives an overview of different state-of-the-art transmitter architectures which can be used for a multi-standard system. The digital-centric alternatives, along with their advantages and their challenges are in the main focus. Section 3.1 begins with a brief review of analog transmitter architectures, including quadrature and polar alternatives. The digital-centric transmitter systems are followed in section 3.2, where their fundamentals are presented and their system architectures are discussed. Finally, section 3.3 summarizes the topic and presents a brief comparison between digital-centric transmitter architectures and analog-intensive ones by reviewing their strengths and weaknesses.

### 3.1 Analog-Intensive Transmitters

Analog transmitters have been there for a long time since the beginning of the radio system development. These systems provide rather good performance with the use of analog elements. In recent years, with the rise of demand for [Software-Defined Radio \(SDR\)](#), more effort has been made towards multi-standard transceivers. Although extensive research has been conducted in this area [29], employing analog components with limited reconfigurability restricts multi-standard implementations in small silicon areas. Digital-centric transmitters, which are introduced as alternatives, are based on the fundamentals of analog transmitters. Furthermore, noise and linearity performance of analog transmitters are still superior and their employment cannot be avoided for specific applications. Therefore, in the following sections, a few of the old-established analog transmitter systems, which are the base for digital-centric systems, are briefly reviewed.

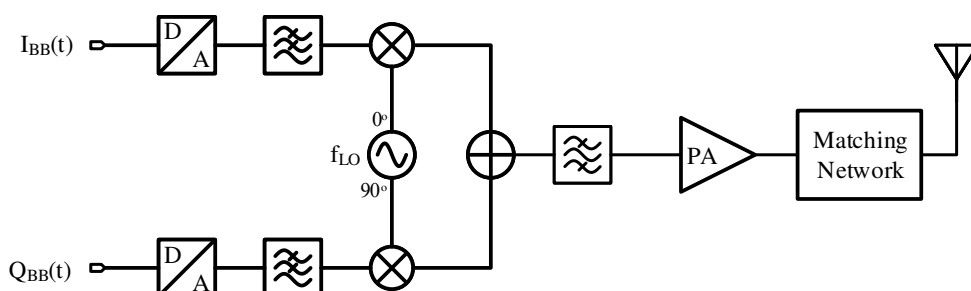


Figure 3.1: General block diagram of a direct conversion transmitter.

### 3.1.1 Direct-Conversion IQ Transmitter

Fig. 3.1 shows the block diagram of a direct-conversion I/Q transmitter. Both I and Q baseband signals, coming from digital blocks, are first converted to analog signals through DACs with adequate resolutions. The quantization noise of the D/A conversion should be sufficiently small so that the noise floor is suppressed and a higher SNR is achieved. Furthermore, the DACs need to be highly linear to meet the emission mask requirements of the communication standard. The DACs are followed by low-pass filters to eliminate aliasing replicas as well as to suppress unwanted emissions to adjacent channels [30]. The resulted I and Q baseband signals are then directly up-converted to the carrier frequency and summed up in an I/Q modulator. This RF signal can be expressed as in (3.1):

$$Y(t) = I_{BB}(t)\cos(2\pi f_{LO}t) - Q_{BB}(t)\sin(2\pi f_{LO}t). \quad (3.1)$$

The quadrature mixing operation helps to achieve a single side-band up-converted signal around the the carrier frequency. However, in practice, gain and phase mismatches between in-phase and quadrature paths results in appearance of an image signal. A formulation of mismatch between I and Q paths for a sinusoidal input, presented in [14], shows that the power ratio of the image signal to the desired signal is given by:

$$\frac{P_{Im}}{P_{Sig}} = \frac{(1 + \varepsilon)^2 - 2(1 + \varepsilon)\cos\Delta\theta + 1}{(1 + \varepsilon)^2 + 2(1 + \varepsilon)\cos\Delta\theta + 1}, \quad (3.2)$$

where  $\varepsilon$  and  $\Delta\theta$  represent gain and phase mismatches, respectively. The image power ratio needs to be smaller than the limits defined by communication standards.

The upconversion mixer plays an important role in the linearity of a transmitter. Passive mixers provide high linearity in exchange for huge power consumption. On the other hand, active mixers, which are the choice in most integrated applications, add

nonlinearity to the output by converting the baseband data from voltage domain to current through transconductance of MOS devices. Two-tone intermodulation analysis is usually performed to determine the linearity of the mixer. The spurs, generated due to third-order intermodulation of input tones, usually fall in the same band and can cause distortion of the signal and raise adjacent channel power. A bandpass filter can be placed after the I/Q modulator to filter out unwanted mixing harmonics of the LO signal.

The RF output of the I/Q modulator is further amplified through a PA to provide the power levels required by communication standards. In case a larger dynamic range is required by the communication standard, a Variable-Gain Amplifier (VGA) can also be placed before the PA to provide a dynamic range of output power up to 80 dB [31]. Since the RF signal contains envelope information, the linearity of the PA contributes significantly to the overall performance of the transmitter. Specifically, when the input of the PA gets close to its 1-dB compression point, higher nonlinearity is observed in the transmitted output signal. Furthermore, operating it in linear mode leads to a low overall efficiency of the PA. In some implementations, a matching network is also placed between the PA and the antenna to deliver the maximum possible power [14]. A band-pass filtering can also be included within the matching network or even separately to avoid unwanted emissions and harmonics [19].

Pulling of the Local Oscillator (LO) is another major challenge in direct-conversion transmitters [14]. In general, the required output power in most modern communication standards goes beyond 1 W, which results in a large voltage swing in the output of PA. This large voltage signal might be coupled to the oscillator through substrate, packaging, or even PCB, which can result in the appearance of a single tone close to the oscillator's center frequency and is called injection pulling. If it is not taken care of this properly, it causes periodic phase rotation in the output of the oscillator and increases the phase noise of the LO signal significantly. Increased LO phase noise and spurs contribute to degrading EVM and out-of-band emissions.

### 3.1.2 Two-Step IQ Transmitter

Performing upconversion in two steps helps to avoid the injection pulling of the oscillator [14]. Fig. 3.2 shows a block diagram of a two-step transmitter that is also called Heterodyne TX as it is complementary to the heterodyne receiver system. In the first stage, similar to the direct-conversion transmitter, a quadrature modulator up-converts the baseband digital input to a single side-band analog signal at an Intermediate Frequency (IF). Next, a second single-stage mixer up-converts this signal for a second time and translates it to the LO frequency. Band-pass filters are employed to remove unwanted harmonics of the mixers, while the second one should also remove the image of the IF signal. Obviously, a higher IF relaxes the filtering of the image at LO frequency.

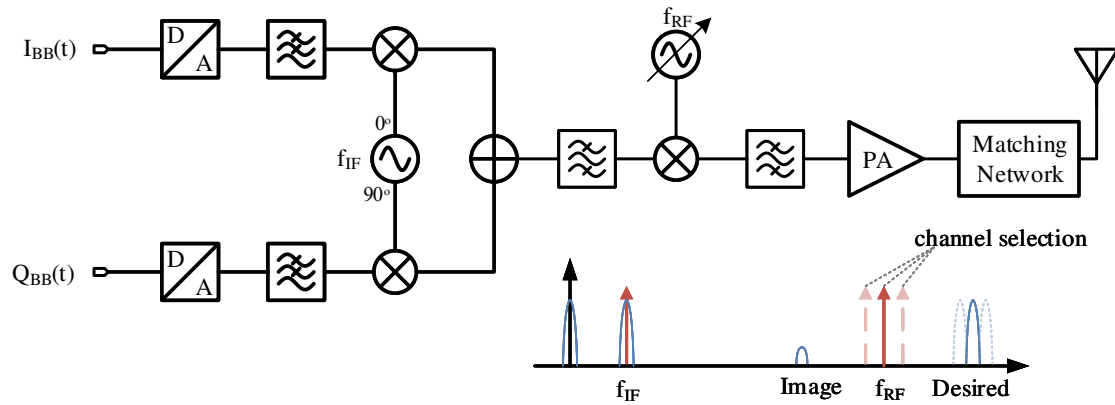


Figure 3.2: General block diagram of a two-step (Heterodyne) transmitter.

Another advantage of the two-step transmitter is that the IQ modulation is carried out at a much lower frequency. This alleviates the design for lower gain and phase mismatches between I and Q paths [14]. Furthermore, by using a narrowband channel filter, the noise and spurs of the IF can be significantly attenuated. However, the use of two mixers together can lead to spurs and harmonics at different frequencies, which are products of combining spurs of both mixers. This can even corrupt the desired RF signal and needs to be dealt with properly.

Despite the benefits, an increase in the number of analog components makes it less re-configurable for multi-standard applications [29]. Moreover, it consumes more power and occupies a larger silicon area compared to the direct-conversion TX. That is why, in many ordinary applications, a more straight-forward direct-conversion transmitter with a reduced number of filtering and simpler frequency planning is preferred.

### 3.1.3 Envelop Tracking

Linear **Power Amplifiers (PAs)** used in both of direct-conversion and two-step transmitter architectures are normally designed to deliver maximum efficiency at peak power. However, if such a PA is used to amplify an amplitude-modulated signal, the efficiency drops significantly at output back-off power levels as power is wasted due to additional voltage headroom at its drain. As a result, for a signal with high **PAPR**, which is the case for most high-throughput modern communication standards, the average PA efficiency would be small. In order to solve this problem, the drain modulation technique can be applied to maximize efficiency in output back-off power levels by optimizing the drain supply voltage of a linear PA. Such a transmitter system is called **Envelope Tracking (ET) TX** in the literature [32]. A Block diagram of an ET transmitter is shown in Fig. 3.3. A conventional IQ modulator produces the up-converted input signal of the PA, while a

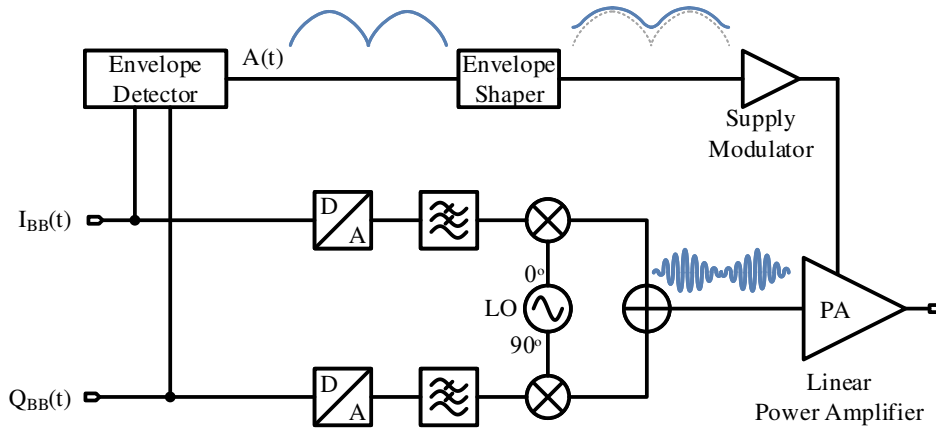


Figure 3.3: Block diagram of an ET transmitter.

baseband envelope amplifier modulates the drain voltage with the help of an envelope detection and shaping block.

For the purpose of power optimization, the supply modulator should adjust the drain voltage to the smallest level that the amplifier is still sufficiently linear. Even in some designs, the PA is driven to weak compression to achieve better efficiency in a trade-off with less linearity while the linearity is then recovered through predistortion of the baseband input signal in the digital domain [33]. Although the ET technique saves power loss in the drain of the PA, it is also important that the supply modulator itself is power efficient. Therefore, switching voltage regulators are employed for this purpose [34, 35]. Furthermore, the supply does not need to track the exact wideband envelope of the baseband signal, which requires higher power consumption. The drain voltage of the PA can be a slowly varying signal with reduced bandwidth to save power in the supply modulator [36].

Implementation of an ET transmitter requires a complex predistortion. Since the modulated drain voltage also affects the gain of the PA just like its input signal does, its AM-AM and AM-PM nonlinearity needs to be characterized under a sufficient number of supply voltages. As a result, the size of the LUT is increased significantly compared to that of a linear PA without ET. This results in a much higher power consumption as well as area for the predistortion of an ET PA [37, 38].

### 3.1.4 Polar Transmitters

Polar modulation can be used in TX systems as an alternative to IQ transmitter systems. This family of transmitters has been studied since long time ago, as in *Envelope Limi-*

**ation and Restoration (EER)** introduced by Kahn in 1952 [39]. With the evolution of on-chip digital signal processing and its integration with Analog/RF circuitry in advanced technology nodes, polar transmitters have become more and more popular in recent years. Smaller power consumption and hence higher efficiencies as well as low in-band distortion and out-of-band noise for low bandwidths makes it an attractive potential candidate to replace the IQ transmitter architecture for advanced wireless communication standards.

In order to get an overview of the principles of polar transmitters, it is first required to look into the polar representation of data samples. Each point of the constellation diagram can be represented in either Cartesian or polar coordinates:

$$S(t) = I(t) + j \cdot Q(t) = A(t) \exp^{j\theta(t)}, \quad (3.3)$$

where  $A(t)$  is the amplitude and  $\theta(t)$  is the phase of the baseband signal. These two signals are calculated as in (3.4):

$$\begin{aligned} A(t) &= \sqrt{I(t)^2 + Q(t)^2}, \\ \theta(t) &= \text{Arctan} \left( \frac{Q(t)}{I(t)} \right). \end{aligned} \quad (3.4)$$

In contrast to  $I(t)$  and  $Q(t)$  in IQ representation,  $A(t)$  and  $\theta(t)$  form the two uncorrelated orthogonal components of the polar plane.

Nonlinear Cartesian to polar conversion is usually performed through **COordinate Rotation Digital Computer (CORDIC)** [40, 41]. This conversion is carried out through a number of iterative simple shift/add operations. The output of **CORDIC** converges to the desired calculation value after a sufficiently large number of iterations. For a higher throughput in advanced communication standards, a pipeline **CORDIC** can be employed.

A major contrast of transmitter architectures with polar modulation to IQ transmitters is their difference of spectral properties of amplitude and phase signals compared to that of I/Q signals. The highly nonlinear Cartesian-to-polar conversion causes spectral expansion of both of amplitude and phase signals. After Cartesian-to-polar conversion through **CORDIC**, the amplitude and phase bandwidths are extended by different factors; for example, those of a **WCDMA** signal are extended with almost factors 4 and 10, respectively [42].

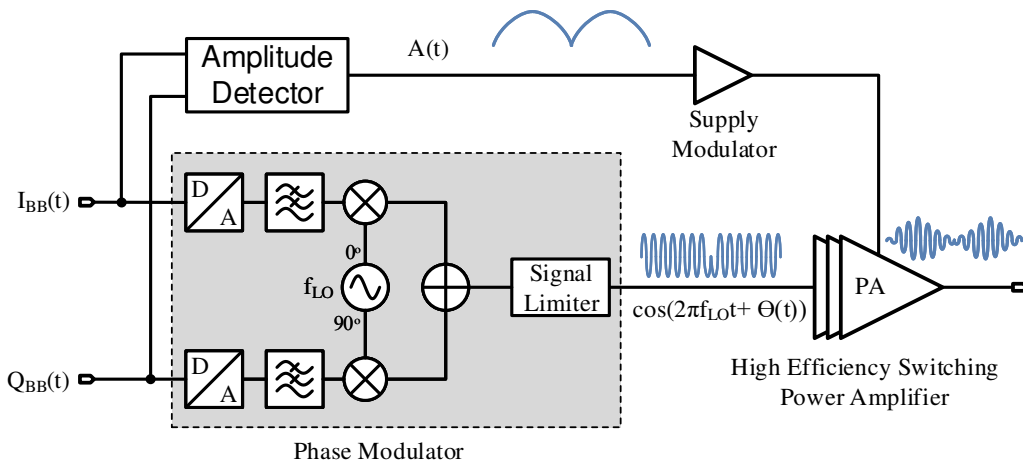


Figure 3.4: General block diagram of an **EER** architecture with polar modulation.

### Envelope Elimination and Restoration

As mentioned earlier, **EER** is the oldest and most common transmitter architecture with polar modulation. Fig. 3.4 presents a general block diagram of **EER** architecture. Input baseband I/Q signals are converted to signals carrying phase and amplitude information. A power-efficient switching mode **PA** is usually employed to amplify the constant-envelope phase-modulated signal while the amplitude modulation is applied through modulating its drain supply voltage. Avoiding linear mode **PAs**, which are typically used in IQ or **ET** transmitters, improves efficiency.

The spectral regrowth due to Cartesian-to-polar conversion raises the requirement of much higher bandwidth in paths of amplitude and phase signals before their recombination in the **PA** output. In practice, bandwidth limitations of the two paths as well as mismatches in spectrum expansion of signals can increase out-of-band distortions.

In an **EER** transmitter, since the whole amplitude modulation is performed through a supply modulator, it needs to be sufficiently wideband for the amplitude signal over a large dynamic range of output power levels. As a result, in contrast to an **ET** transmitter, **EER** has more stringent bandwidth requirements on the design of its supply modulator. This can be translated to higher power consumption in the supply modulator compared to the main power-efficient switching **PA**. Linear **Low Drop-Out (LDO)** regulators provide wideband operation and reduced output ripple [43, 44], while showing a degraded power efficiency. On the other hand, switching voltage converters provide a high efficiency in exchange with a lower bandwidth and higher ripples, which degrades the linearity of the transmitter. As a solution, hybrid versions of supply modulators with a combined use of linear and switching regulators have been reported in the literature [45, 46, 47]

In comparison with **ET**, **EER** transmitters can theoretically provide a better power efficiency due to the use of switching-mode **PA**. Furthermore, the predistortion algorithm can be less complicated since no multidimensional implementation, such as those required in **ET**, is needed. However, an **ET** system is more immune to timing misalignment between the envelope and the RF path [48]. On the contrary, the bandwidth of the envelope path can be reduced in **ET**, resulting in a more power-efficient design of the drain regulator, while the wideband operation requirement of the supply modulator can be the efficiency bottleneck of an **EER** system [49].

## 3.2 Digital-Centric Transmitters

In a trend in the last decade, intensive research has been reported in the literature towards digital implementation of state-of-the-art transmitter architectures. Modern CMOS technology nodes provide high digital processing speeds with low power and small area consumptions. Additionally, digital circuits can be easily migrated into newer technology thanks to their high integration capability. On the other hand, achieving decent analog performance is more challenging in smaller technology nodes due to short channel effects resulting in reduced intrinsic gains and reduced voltage headrooms along with the same threshold voltages and increased leakage currents [50]. As a result, further technology shrinking does not provide much benefits in reducing the area or power consumption of analog circuitry while maintaining a sufficient performance [51].

Furthermore, in order to develop a multi-standard transmitter, which is the scope of this work, one needs to guarantee reconfigurability in the first place. The digital domain provides such a reconfigurability through digital signal processing. In other words, bulky analog processing should be replaced with digital blocks as much as possible so that the transmitter becomes highly reconfigurable. In this way challenges in achieving high analog voltage resolutions are also traded for better timing accuracies of advanced **CMOS** technologies in digital circuitry. However, the interface to the analog and **RF** world still plays a significant role in achieving the desired performance out of the transmitter. For a reconfigurable solution, one needs to develop a reconfigurable **RF** frontend with sufficiently high performance to meet the requirements of targeted wireless communication standards. This has been achieved by the introduction of **RF-DAC** frontends in recent years.

Fig. 3.5 shows a general block diagram of a digital-centric transmitter system. The baseband signal is generated off-chip and is transferred to the **RFIC**, where it is processed. After a number of **DSP** blocks in the digital part, a **Direct Digital-to-RF Converter (DDRC)** converts the resulted digital signal to analog and mixes it with **LO** at the same time. As it is discussed in detail in the following section, such a TX architecture where fundamental analog filters are eliminated leads to a number of challenges which need to be addressed

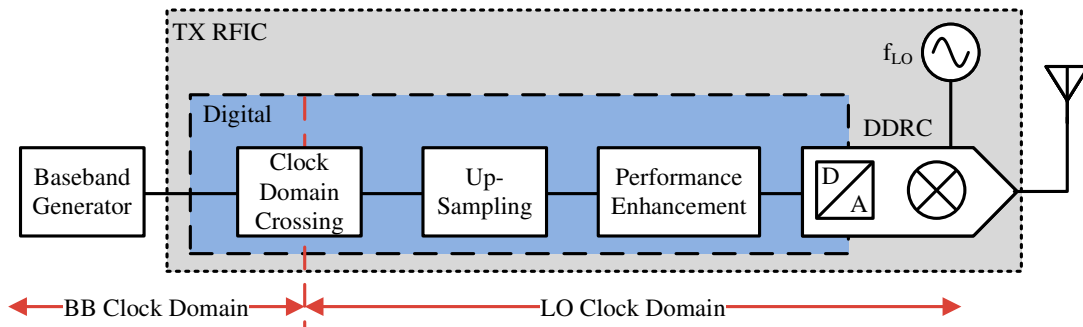


Figure 3.5: General block diagram of a digital-centric transmitter system.

through **DSP** and, hence, add up to the complexity of the digital part. Most importantly, the baseband signal has to be upsampled with a high **UpSampling Ratio (USR)** to a clock frequency that is achieved through dividing the carrier frequency by an integer factor. As a result, the digital part should first realize a clock domain crossing from the baseband sampling clock to the **LO** domain and then it should perform a number of upsampling steps. In addition, digitally-assisted enhancement of frontend performance, which includes compensation of non-idealities and generating required signals to drive it, should also be incorporated in the digital part. This implies that although the analog sections are reduced, the implementation of such a complex digital processing requires much more attention in order to achieve a desirable performance.

### 3.2.1 Direct Digital-to-RF Converter

The **DDRC** is the analog frontend of a digital-centric transmitter system, which modulates the digital baseband signal and converts it to the **RF** domain to be transmitted through the antenna. For this purpose, it needs to combine operations of both a DAC and an upconverting **RF** mixer of an analog-intensive transmitter. This is usually performed through a so-called **Radio-Frequency Digital-to-Analog Converter (RF-DAC)**. Similar to a low-frequency **Digital-to-Analog Converters (DACs)**, such a frontend consists of a number of unitcells that can be configured in a binary-weighted or unary-weighted scheme or a combination of both. According to the digital baseband data, a number of **DAC** cells are turned on to conduct the LO signal. In this way, D/A conversion and up-mixing are performed at the same time in each unitcell individually and the generated **RF** signals are summed up at the output.

In current-steering implementations of **RF-DAC**, which are pretty similar to current-steering **DACs**, each cell outputs a switching differential current that is produced through switching the constant tail current of the cell with a square-wave **LO** signal. In such **RF-DAC** frontends, which is illustrated in Fig. 3.6, all the cells are implemented in an open

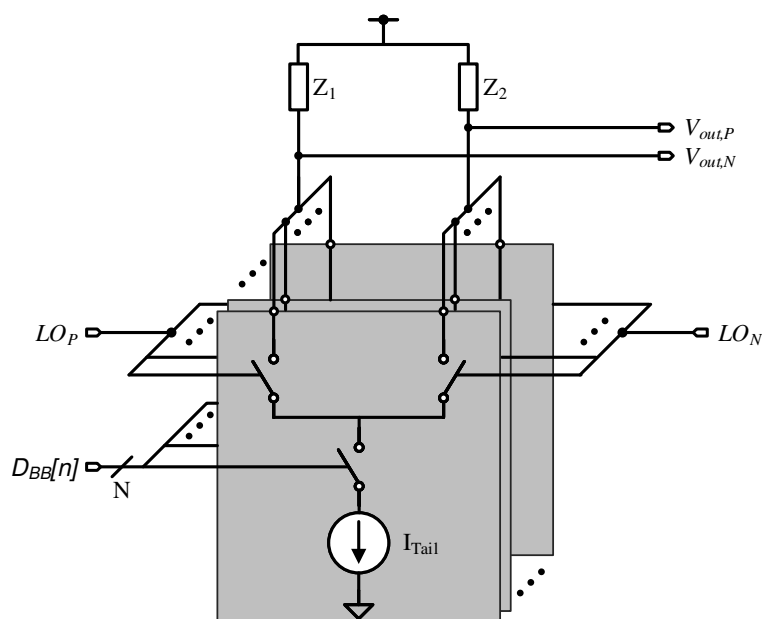


Figure 3.6: Current steering implementations of RF-DAC.

drain structure and their currents are summed up at the output node, which is biased externally by a supply voltage through RF chokes or baluns. The number of activated unitcells, which is determined by baseband data, decides the amplification of the LO signal in the output of the RF-DAC. Subsequently, the RF output signal is shaped by an envelope of digital baseband signal along with the carrier frequency of LO signal.

Due to a switch-mode mixing of a square-wave LO with the tail current, the mixing operation does not suffer nonlinear transconductance of MOS devices. This is contrary to conventional analog active mixers such as Gilbert cell [14, 52], where the input signal in the voltage domain is converted to current through  $g_m$  of MOS devices. As a result, mixing operation in such an RF-DAC is less sensitive to short-channel effects while it benefits higher  $f_t$  in smaller technology nodes.

There have been many different implementations of RF-DAC reported in the literature in recent years. Fig. 3.7 shows a number of these unitcell variants. The design shown in Fig. 3.7a, which is introduced in [10] for a polar transmitter system, is very similar to the general current-steering version depicted in Fig. 3.6. The tail current is provided through a current mirror and its bias voltage, which also allows power control. The data bit,  $D_{BB}$ , can enable or disable the current flow through a cascode transistor on top of the current source. The complementary LO signals,  $LO_p$  and  $LO_n$ , steer the current to one of  $Out_p$  or  $Out_n$  in each phase of the LO signal. Cascode transistors on top of LO switching increase the output impedance and reduce the coupling of LO signals to the output, which causes LO feedthrough. However, turning these cascodes on and

off with each LO phase causes slower transient performance and increases undesired harmonics of LO signal. Furthermore, enabling or disabling the current flow through a cascode switch transistor according to  $D_{BB}$  causes long settling times with each change in the baseband data. The former increases undesired harmonics of LO signal and causes mostly out-of-band spurs while the latter introduces harmonics of data frequency and deteriorates in-band linearity as well.

Another alternative design which is one of the very first versions of switch-mode unitcells is introduced in [9] and is shown in Fig. 3.7b. Very similar to a Gilbert-cell mixer, the tail current is switched to either of positive or negative branches according to the product of a multiplying LO and a data bit. Since the tail current is not turned off, such an implementation avoids the undesired start-up transient behavior of unitcells. However, constant-flowing tail currents degrade power efficiency at back-off levels significantly. This would be particularly an issue for signals with high PAPR.

In an effort in order to improve both transient performance and power consumption of the aforementioned designs, the unitcell shown in Fig. 3.7c is presented by [53] and [8]. A cascode current mirror provides biasing voltages for a cascode current source formed out of  $M1$  and one of  $M2a$  and  $M2b$ . Instead of using a cascode switch as in Fig. 3.7a, which slows it down, the gate voltage of the tail current source is switched between the biasing voltage and the ground for the purpose of enabling or disabling the current flow. Transistors  $M2a$  and  $M2b$ , which are part of the cascode current source, switch the current flow direction according to the sign of the baseband data so that a signed operation of the RF-DAC can be supported. On top of these, the LO-switching quad transistors are stacked to translate the baseband current of the cell to the carrier frequency. A drawback of this unitcell is that since the LO quad is located close to the output node, higher LO feedthrough can be expected compared to both of the former discussed versions. It should also be mentioned that similar to most other RF-DAC variants, thicker gate oxide MOS devices are employed for the upper transistors to allow higher supply voltages at the output. This even deteriorates the LO feedthrough due to bigger coupling capacitance to LO signals.

Another category of RF-DAC frontends, which are also called Digital Power Amplifier (DPA) in the literature, is shown in Fig. 3.8. The very simple unitcell shown in Fig. 3.8a is first presented by [7]. This unitcell consists of only two MOS devices stacked on top of each other. The lower transistor operates as a switch to enable current flow during high phases of the LO signal while the cascode one provides the current if the cell is activated by its corresponding data bit. As a result, it mixes LO and data bit by conducting current only when both are high. Since no cascode current source is considered for this cell, its output impedance is much lower compared to most of the other reported designs. Smaller output impedance is not desired as it increases the AM-AM and AM-PM nonlinearities. This will be discussed in more detail in the following sections.

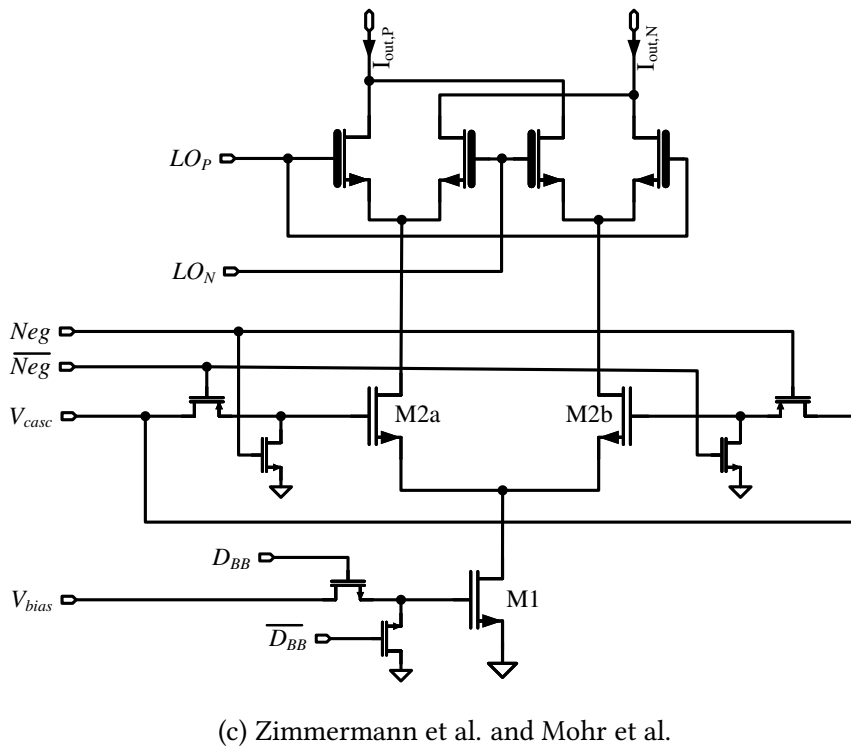
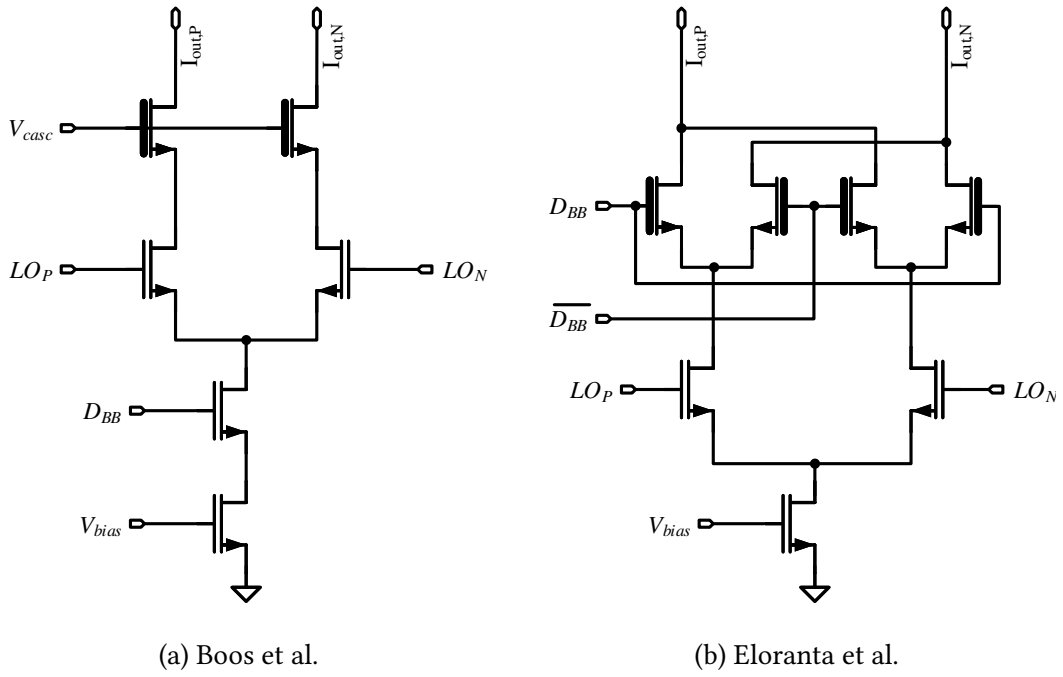


Figure 3.7: RF-DAC unitcell implementations in the literature.

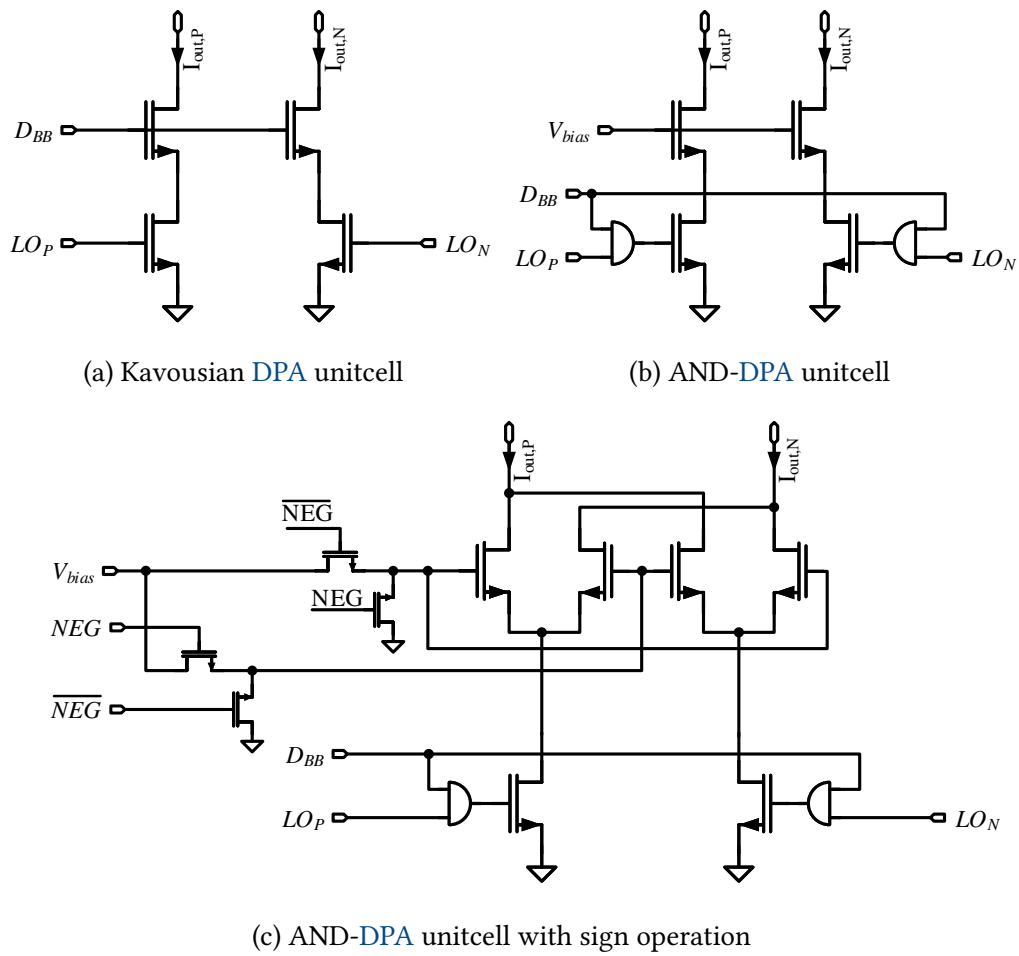


Figure 3.8: DPA unitcell for RF-DAC frontends.

Fig. 3.8b shows an AND-DPA, which was first introduced in [54] and used in many designs, including those reported in [55, 11, 56, 12]. Instead of mixing LO and  $D_{in}$  directly in the unitcell, an AND-gate is used to combine them prior to the current cell. The output of the AND-gate drives the enabling switch of the unitcell while the cascode transistor, which is biased separately, conducts current when the enabling switch provides a low-ohmic path to ground. The bias can be generated either with the help of a CMOS bandgap reference such as the one in [57] or a current mirror with the same structure. This provides the possibility to change the current of the cell by adjusting  $V_{bias}$  and applies a range of analog power control to the RF-DAC frontend. In [16], as depicted in Fig. 3.8c, a sign operation is added to the design by means of additional cascode transistors and switching their gate voltages between  $V_{bias}$  and ground. As a drawback of such an AND-DPA, the addition of a gate delay in each unitcell might increase the timing mismatch between unitcells of the frontend, which can degrade the linearity of the transmitter system and should be considered in the system design phase.

Although the use of DDRC in digital-centric transmitters alleviates the need to use bulky, power-hungry, and inflexible analog blocks, it brings up a number of challenges to deal with. These are discussed in the following sections.

### Lack of reconstruction filter

In a digital system, the signal spectrum is repeated at multiples of the sampling frequency,  $f_s$  [58]. In conventional analog-intensive transmitters, a low-frequency DAC is followed by reconstruction filters to attenuate and remove sampling replicas of the digital signal. However, in a digital-centric transmitter, there is no such possibility of providing low-pass filtering for the baseband signal. Using small unitcells, which combine bit-wise D/A conversion and up-conversion, does not allow for such filtering in the baseband domain. Furthermore, narrowband filtering at carrier frequency,  $f_{LO}$ , cannot be performed with a good quality factor at a low cost and it also reduces the reconfigurability of the transmitter system for multi-standard applications. As a result of lacking such a reconstruction filter, unwanted replicas of the baseband data will be seen at multiples of sampling frequency offsets from the carrier frequency, which will be  $f_{LO} \pm m \cdot f_s$ . These replicas cause out-of-band emissions and can fall in the frequency band of other communication standards, which is strictly forbidden.

In order to alleviate the problem of missing a reconstruction filter, ZOH behavior of the RF-DAC can be used. This comes from the fact that the baseband data is held constant during one full period of its sampling clock till the next digital sample is applied. Similar to ZOH transfer function in a low-frequency DAC [59], that of an RF-DAC can be written as:

$$H_{ZOH}(f) = \text{sinc}\left(\frac{f - f_{LO}}{f_s}\right) \cdot e^{-j\pi(f - f_{LO})/f_s}, \quad (3.5)$$

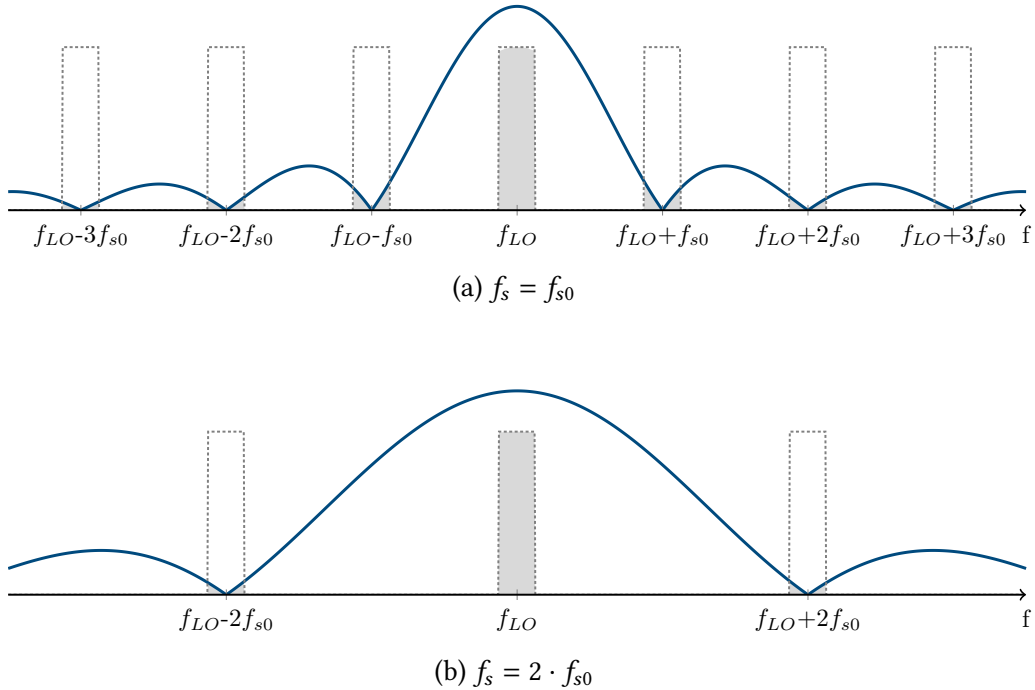


Figure 3.9: ZOH sinc transfer function of an RF-DAC frontend.

where the *sinc* function is zero at integer multiples of  $f_s$  away from  $f_{LO}$ . Fig. 3.9 shows this transfer function in the presence of signal replicas with two different sampling frequencies. It can be seen that if  $f_s$  is increased for the same baseband signal bandwidth, the replicas fall into areas of sinc function with higher attenuation. Consequently, a straightforward approach to reduce unwanted out-of-band emissions due to sampling replicas of the baseband signal is to increase the sampling frequency and, therefore, its ratio to the bandwidth of the baseband signal as much as possible. This also pushes sampling replicas farther from the desired signal, which facilitates the implementation of a band-pass filter at high frequencies since smaller filtering quality factor would be required. Therefore, digital upsampling of the baseband signal is desired to be applied with an **Over-Sampling Ratio (OSR)** as high as possible.

In addition to reducing unwanted emissions due to sampling replicas of the baseband signal, oversampling also helps to lower the noise floor by reducing quantization noise. Similar to a low-frequency DAC, oversampling increases the SNR by  $10\log(OSR)$  [60]. For instance, upsampling of a 20-MHz WLAN signal to 800 MS/s can improve the SNR by 16 dB.

### Clocking frequency requirements

In contrast to analog-intensive transmitters, where baseband sampling frequency is used in all steps towards mixing with LO, the clocking scheme is more complicated in a digital-centric transmitter. Since D/A conversion and mixing are combined in small unitcells with no possibility of reconstruction filter, glitches and spikes can occur. In order to avoid such glitches, it should be guaranteed that each new data sample becomes effective at zero-crossing points of its corresponding LO signal [53]. For this purpose, the sampling rate should be synchronized with the LO frequency in the first place. In other words, the sampling frequency,  $f_s$ , needs to be in the same clock domain as the LO signal, which means it should be derived through dividing  $f_{LO}$  by an integer number:

$$f_s = \frac{f_{LO}}{N}. \quad (3.6)$$

In addition, the negative image of the signal spectrum folds to positive frequencies at  $-f_{LO} + K \cdot f_s$  due to sampling replicas. As shown in Fig. 3.10a, these replicas might be close to the LO frequency, which can deteriorate the signal quality of the transmitter or, even worse, can fall into the receiver band and degrade its sensitivity [61]. By selecting the sampling frequency to be an integer fraction of the LO frequency, as in (3.6), aliased replicas of the negative image fall on the same replicas of the main signal and are suppressed by the *sinc* function of ZOH. This is shown in Fig. 3.10b.

In (3.6),  $N$  should be kept preferably small so that the resulted sampling frequency provides enough suppression of sampling replicas through ZOH as discussed earlier. However, the achievable maximum speed of the digital part depends on the technology node and the complexity of the operations that need to be done at this frequency. On the other hand, the baseband signal generator is typically not synced with LO signal. This requires that the baseband data is first transferred to the LO clock domain before it is processed and upsampled. Such a clock domain crossing should be carried out with sufficient precautions to prevent metastability and consequent errors.

### Matching of signal delays to/from different cells

One of the major challenges in implementation of an RF-DAC frontend is the timing alignment of its input signals as well as its output signals. Delay mismatch between the edges of output currents coming from different cells causes distortion in the transmitter's output where all these currents are summed up. As a result, the distribution of data bits and LO signals as well as outputs through different cells requires special attention. This problem is mainly originated in the layout because of different paths and parasitics of these signals to/from different cells. This challenge is even intensified with a higher-resolution RF-DAC which can also occupy a larger area.

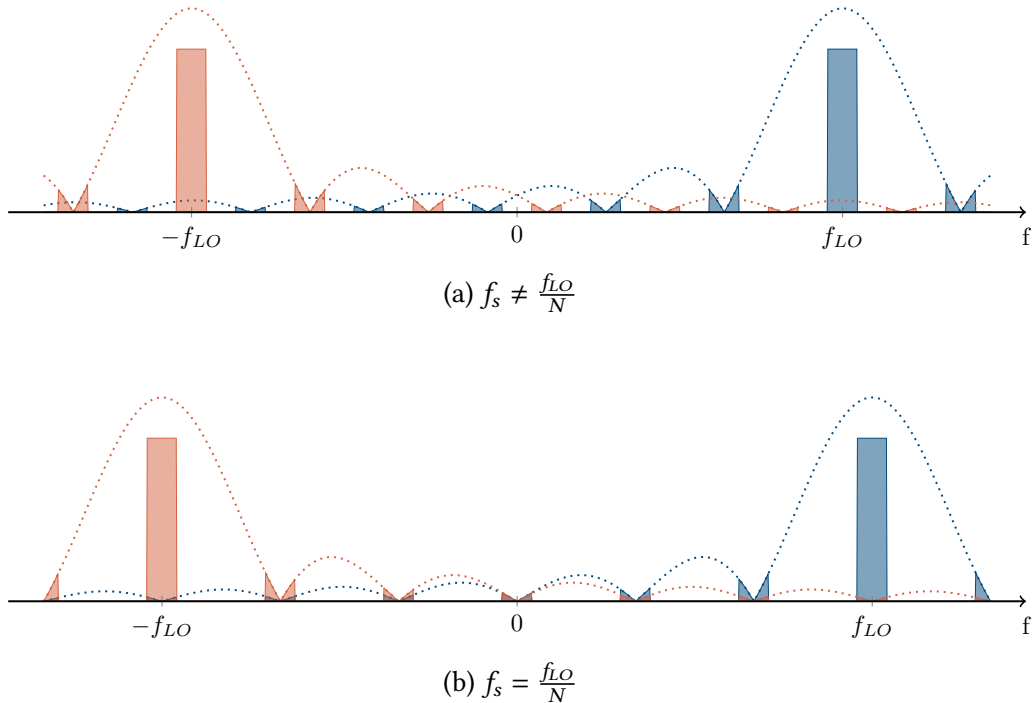


Figure 3.10: Folding of replicas of the negative image into the positive frequencies.

By deriving the sampling frequency from the LO signal, it can be guaranteed that data samples are fed to DDRC with a constant timing relative to the edges of LO. However, if the timing of data bits and LO edges arriving at each cell do not match with other cells, glitches in the time domain are produced, which gives rise to nonlinearity and spurs in the signal spectrum.

In practice, it is not feasible to match all signals across all cells. Instead, in most of the reported designs, LO and output signals, which consist of higher-frequency components, are taken care of to be distributed symmetrically in the whole frontend while data bits are then synchronized with LO through different techniques. This alleviates the distribution of data signals by allowing for a possible delay interval for bits of a new data sample to arrive at different cells. Furthermore, depending on the application as well as the desired performance, a margin can be found for delay mismatches in the edges of output currents from different cells. This margin is usually anticipated through system simulations prior to circuit implementation.

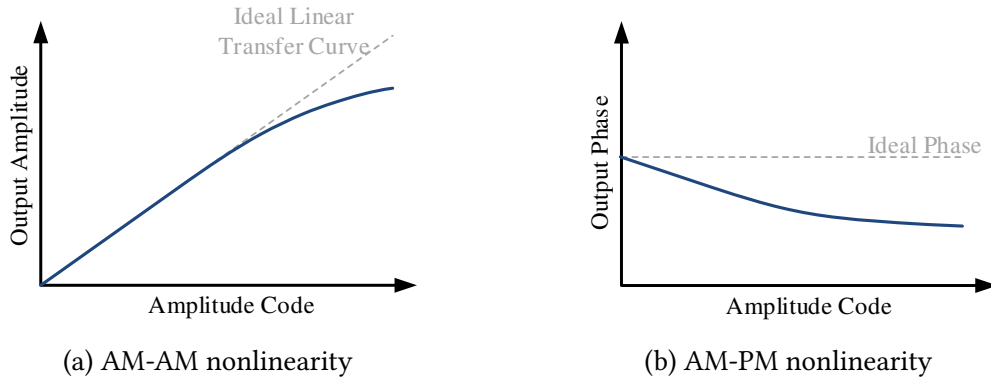


Figure 3.11: Nonlinearity of an RF-DAC frontend due to a finite output impedance.

### Limited output impedance of unitcells

Variation in the output impedance of an RF-DAC frontend at different output power levels can cause significant nonlinearity, which results in distortion and degrades the transmitter's EVM. In practice, when a cell is switched on, it acquires a finite output impedance, which is typically much smaller than that of the switched-off mode. In general, due to channel length modulation of MOS devices, the on-impedance of each cell is further reduced at higher output power levels where a larger voltage amplitude at the frequency of operation modulates its drain current. Furthermore, a larger number of cells need to be turned on in parallel to provide higher power levels, which leads to a significantly smaller impedance at the output of the frontend. Clearly, if the output impedance is reduced and becomes comparable with the load resistance, a smaller portion of the switching current amplitude is delivered to the load. This causes AM-AM nonlinearity as the output power does not increase linearly with increasing its input code. As a result, a transfer curve with compression at higher powers similar to the one shown in Fig. 3.11a is followed. It should be mentioned that since the output impedance is dominantly capacitive at high frequencies, this nonlinearity profile is highly dependent on the operation frequency.

In addition to compression in the amplitude transfer function, variation of the output impedance at the frequency of operation can also cause phase shifts in the output signal. By turning a cell on and off, the capacitance of its nodes varies as the operation modes of MOS devices change. For instance, the drain capacitance of the upper switching transistor, which is directly connected to the output node, is reduced by changing it from cut-off to saturation. Undoubtedly, when more number of cells are turned on, the change in output capacitance grows considerably. This causes a code-dependent phase shift in the output signal, which results in the AM-PM nonlinearity of DDRC. This is illustrated in Fig. 3.11b.

There are a few approaches that can be taken into consideration to reduce undesired AM-AM and AM-PM nonlinearities. In the first place, it is crucial to design unit cells with high on-mode impedance at the frequency of operation. Employing cascode transistors with larger channel lengths as well as a smaller current helps to increase the output resistance. However, larger transistors lead to a more considerable capacitance variation, which is the dominant part of impedance at higher frequencies. Furthermore, the input impedance of the matching network at the output of the frontend, which is the load of the **RF-DAC**, can be designed to be considerably smaller than the **RF-DAC** output impedance. On the other hand, a smaller load impedance means a smaller achievable output power with the same current. As a result, depending on factors such as resolution, linearity, current consumption, and required output power, a number of trade-offs need to be made in order to design an **RF-DAC** with an acceptable AM-AM/AM-PM nonlinearity profile.

**Digital PreDistortion (DPD)** can also be applied to compensate for AM-AM/AM-PM nonlinearity. In this technique, which is explained in more detail later in section 4.3.3, a reverse transfer function of the nonlinearity profile is applied to the sampled data so that an overall linear transfer function is achieved. For this purpose, each data sample is mapped to a new code in the digital signal processing and frontend compensation modules. Usually, a **Look-Up Table (LUT)**, which is filled through a calibration mechanism, is employed. The output corresponding to each code is processed through a power meter, which can be external or a simple integrated ADC such as [62] to read out a voltage that is generated according to the output amplitude of the frontend. Consequently, a proper correction is decided and filled in the **LUT**. However, it is desired to design the frontend with a sufficient linearity so that no complicated predistortion is required as it increases the complexity and requires additional calibration processes.

#### **Power Supply Noise**

Digital switching activities draw switching currents from the supply, which leads to **Power Supply Noise (PSN)**. Therefore, in the first place, there should be sufficient isolation between the digital supply and the analog supply of the frontend as well as their substrate connection. Furthermore, Digital modules are pretty sensitive to **PSN** as it introduces jitter. As a result, timing uncertainties are introduced to the signals driving the **DDRC**, which can affect its performance. In order to prevent it from affecting the performance of the transmitter, one can run a mixed-signal simulation by modeling the currents drawn by standard cells, which leads to **PSN** and accordingly find the timing uncertainty of output signals of the digital part as presented in [63]. This needs to be within the timing constraints with which the **DDRC** operates without noticeable degradation.

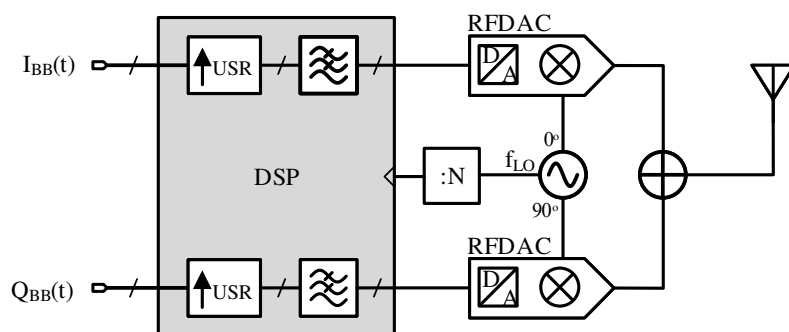


Figure 3.12: General block diagram of a digital-centric I/Q transmitter.

### 3.2.2 Digital-Centric I/Q Transmitter

Similar to the analog-intensive direct conversion IQ transmitter noted in section 3.1.1, its digital-centric variant can be implemented as illustrated in Fig. 3.12. The digital part receives in-phase and quadrature-phase data streams with the baseband data rate. After a number of stages of upsampling and digital signal processing, I and Q data samples are fed to two DDRCs, which mix the data with an LO signal with a 90-degree phase difference. As a result, by combining the outputs in a power combiner, the summation in (3.1) is achieved and the desired RF output is reconstructed. Depending on the implementation, power combining can be simply performed either by summing up the drain currents of both RF-DACs or through a more complicated circuit such as Wilkinson power combiner [64]. Clearly, the resolution and the linearity of RF-DACs play significant roles in achieving the required amount of image rejection and EVM. Furthermore, the mismatch between the paths can degrade the performance of the transmitter. This can be compensated to some extent through the DSP as is explained with more details in chapter 4.

#### IQ modulation with a 25 % LO signals

Square-wave LO signals with a 50 % duty cycle, shown in Fig. 3.13a, are commonly used in many designs. However, if used in an IQ modulator, a 50 % duty cycle is not the most efficient approach in terms of power consumption [65]. If the data samples remain constant, the main tone and harmonics of the differential current output signal, which is shown in Fig. 3.13c, are calculated through Fourier series as:

$$A_{n,50\%} = \frac{1}{T} \int_0^T I_{out,50\%}(t) e^{-j2\pi nt/T} dt = \frac{2I_0}{n\pi} \left[ \sin\left(\frac{n\pi}{2}\right) D_I + \sin^2\left(\frac{n\pi}{2}\right) D_Q \cdot j \right], \quad (3.7)$$

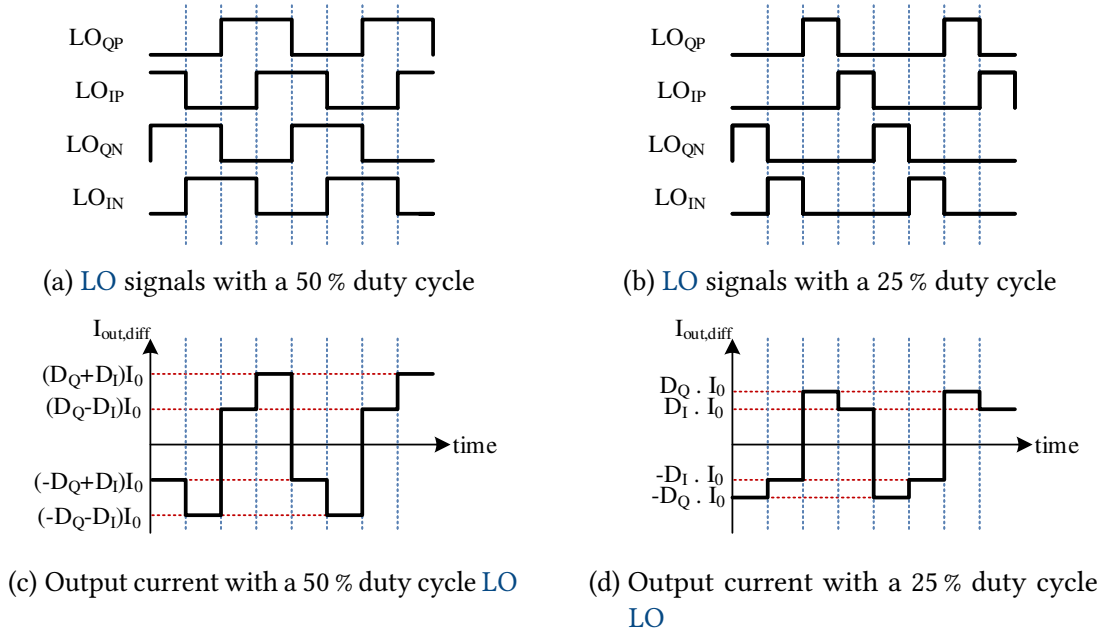


Figure 3.13: Effects of LO signals with duty cycles of 50 % and 25 % on an RF-DAC output.

where  $I_0$  is the tail current of each unitcell and  $D_I$  and  $D_Q$  are the number of activated cells for in-phase and quadrature samples, respectively. Consequently, the amplitude of the main tone of the output current is:

$$A_{h1,50\%} = \frac{2}{\pi} \sqrt{D_I^2 + D_Q^2} \cdot I_0. \quad (3.8)$$

As an alternative, non-overlapping 25 % duty-cycle LO signals, shown in Fig. 3.13b, can be also used. The resulting current waveforms are shown in Fig. 3.13d. In order to compare these two cases, the coefficients of the Fourier series for the output signal of this scheme are also calculated as follows:

$$A_{n,25\%} = \frac{1}{T} \int_0^T I_{out,25\%}(t) e^{-j2\pi nt/T} dt = \frac{I_0}{n\pi} \left[ \sin\left(\frac{n\pi}{2}\right) (D_I - D_Q) + \sin^2\left(\frac{n\pi}{2}\right) (D_Q + D_I) \cdot j \right]. \quad (3.9)$$

Therefore, the main tone is given by:

$$A_{h1,25\%} = \frac{\sqrt{2}}{\pi} \sqrt{D_I^2 + D_Q^2} \cdot I_0. \quad (3.10)$$

Obviously, the output power with the same number of cells turned on in each of the I and Q DACs is 3 dB higher with a 50 % duty cycle of LO. However, it can be shown that the drain current consumption is also much higher. The average current consumption in one period of LO can be calculated for comparison. With a duty cycle of 50 %, all the required cells conduct current in each of the DACs during a whole LO clock cycle. As a result, the average drain current is given by:

$$\overline{I_{drain,50\%}} = (D_I + D_Q) \cdot I_0. \quad (3.11)$$

While with a 25 % duty cycle, each of the I and Q DACs would conduct current only in half of a clock cycle, which results in an average current consumption of:

$$\overline{I_{drain,25\%}} = \frac{(D_I + D_Q)}{2} \cdot I_0, \quad (3.12)$$

which is half of that calculated in (3.11). Considering (3.8), (3.10), (3.11), and (3.12), it can be seen that with a duty cycle of 50 %, a 3 dB higher output power is achieved while it consumes 2 times more drain current compared to 25 % duty cycle. In other words, by increasing the unit current by a factor of  $\sqrt{2}$  and applying a duty cycle of 25 % for the LO signal, the same output power with less drain current consumption can be achieved.

Although a better power consumption can be achieved by using a 25 % duty-cycle LO signal, it might be more challenging to design the RF-DAC frontend. In each unitcell, since the current is cut off during 2 out of the 4 phases of the LO period, a slow transient response of turning on or turning off the tail current introduces glitches and spurs in the output signal and degrades the linearity. As a result, a tail current switching unitcell such as those in Fig. 3.7c or Fig. 3.7a is not consistent to be combined with a 25 % duty cycle. Instead, simpler DPA unitcells, as in Fig. 3.8, which are pretty fast with enabling or disabling current conduction, could be employed. However, such a design for a faster operation typically comes with the price of a lower output impedance, which should be dealt with properly.

### 3.2.3 Digital-Centric Polar Transmitter

In recent years, the polar transmitter architecture has been improved further by integration of RF-DAC frontend for the purpose of Amplitude Modulation (AM). In such digital-centric architectures, the envelope path is realized through a number of active RF-DAC cells. As a result, the complexity of an envelope modulator in the EER technique, as in [66, 48, 67, 47], can be avoided in a digital-centric polar transmitter [12, 68]. Furthermore, the problem with time mismatch between the paths of amplitude and phase signals, can be solved by clocked delay synchronization. Compared to an IQ-based digital-centric

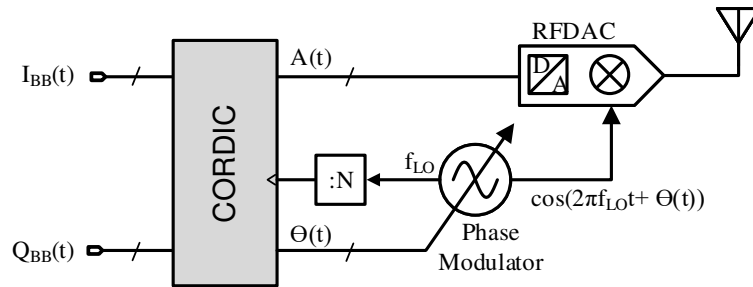


Figure 3.14: System block diagram of a digital-centric polar transmitter architecture.

transmitter, the polar variant requires only one DDRC for amplitude modulation while the phase is modulated separately in a prior circuit such as a PLL with 2-point modulation [69]. This alleviates the need to compensate the imbalances of IQ paths while leading to less area and power consumption of the frontend. Since only one single output vector is created to hit a specific point of the constellation, no power is wasted at the output for combining I and Q vectors. Depending on the signal phase, this can lead to up to 3 dB less power consumption at the output.

Fig. 3.14 shows a block diagram of a digital-centric polar transmitter. In the digital domain, I and Q baseband signals are upsampled and then processed by a CORDIC to generate amplitude and phase signals of the polar representation. The phase signal is fed into the phase modulator, which modulates the phase of the square-wave LO signal. The amplitude signal modulates the radiated output power.

### Phase modulation

An advantage of using advanced digital signal processing in modern CMOS technologies can be seen in the realization of phase modulation as well. Different phase modulation techniques are shown in Fig. 3.15. Traditionally, phase modulation has been performed through an amplitude-limited IQ modulation as in a conventional EER system shown in Fig. 3.4. However, just like a conventional analog direct-conversion IQ transmitter, described in section 3.1.1, it requires bulky and power-hungry off-chip filters. Furthermore, the quadrature mixer produces spurs and distortion, which should be avoided. Two-point modulation through a digital PLL introduced in [69] is commonly used for the purpose of phase modulation in a digital-centric polar transmitter. Such digital-friendly phase modulators can provide a very fine resolution with negligible spurs [11, 70]. However, due to the limited bandwidth of the PLL loop filter, there is a restriction on the bandwidth of the baseband phase signal, which is several times larger than the bandwidth of the I/Q baseband signal.

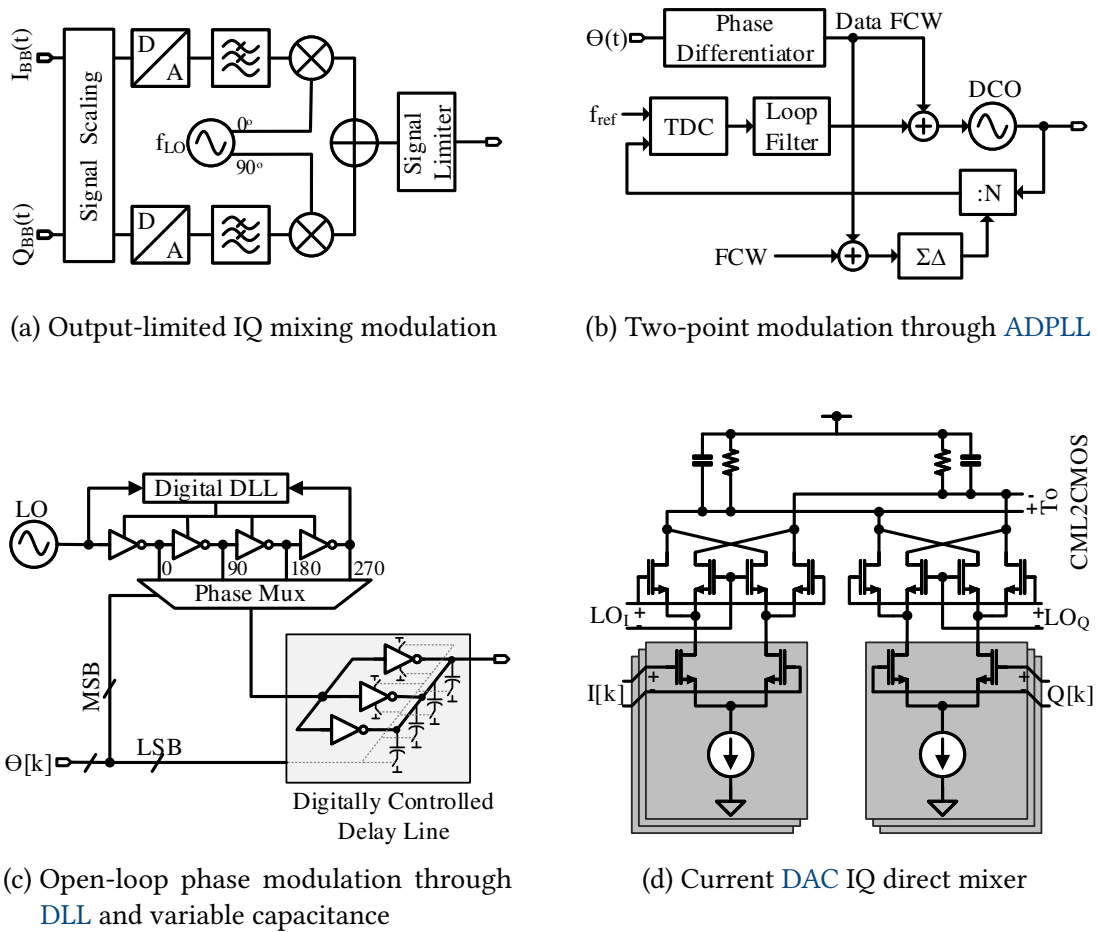


Figure 3.15: Different phase modulation techniques.

For a wide-bandwidth performance, as an alternative to two-point modulation with PLL, open-loop phase modulation can be adopted. In [71, 72, 73], as depicted in Fig. 3.15c, a segmented digital-to-time converter is employed where the MSB segment is implemented through a tapped DLL locked to the LO frequency and the LSB section is realized by a digitally-controlled delay line with switchable small capacitors. In [74], on the other hand, open-loop phase modulation is performed through current DACs with normalized I and Q signals while a Gilbert-cell quadrature mixer generates a constant-envelope phase-modulated output signal. This is shown in Fig. 3.15d. In both of the aforementioned open-loop phase modulation techniques, since the phase modulation is not integrated within the PLL, it can be optimized for phase noise with no need for gain and linearity calibration of the DCO. However, both methods introduce quantization noise, non-linearity, and spectral images and, therefore, need to be calibrated.

### 3.2.4 LINC Transmitter

Another digital-centric transmitter architecture with lots of attention drawn towards it in recent years is **Linear amplification with Nonlinear Components (LINC)** which is based on the outphasing principles. The outphasing modulation, which is the fundamental principle of the LINC architecture, has been studied since a long time ago as introduced in [75]. However, due to inefficient circuitry implementation at that time, it was not investigated much further. With the evolution of digital nano-scale CMOS technology nodes, complex time-domain signal processing can be performed with much higher clock rates, which allows for further development of outphasing transmitters.

LINC Transmitters are well-known for providing very high linearity with the use of two nonlinear PAs, each with a constant-envelope signal. Since constant-amplitude phase-modulated signals do not suffer intermodulation and distortion due to the nonlinearity of PAs, a very high-efficiency PA architecture such as switching-mode class-D can be used. Although this architecture presents a high drain efficiency at peak power, the efficiency drops significantly at power back-off levels. Furthermore, mismatches between its amplification paths can degrade its linearity far beyond the strict limits set by modern communication standards such as LTE and WLAN. In order to prevent these undesired effects, one needs to get a better understanding of the operation principles of outphasing, which is described in the following sections.

#### 3.2.4.1 Outphasing Fundamentals

Assuming a polar plane with a maximum amplitude of  $V_{max}$ , each signal  $V(t)$  can be decomposed to a linear combination of two outphasing signals,  $S_1(t)$  and  $S_2(t)$ , each with the constant envelope of  $V_{max}$ . A symmetrical decomposition of a signal vector into

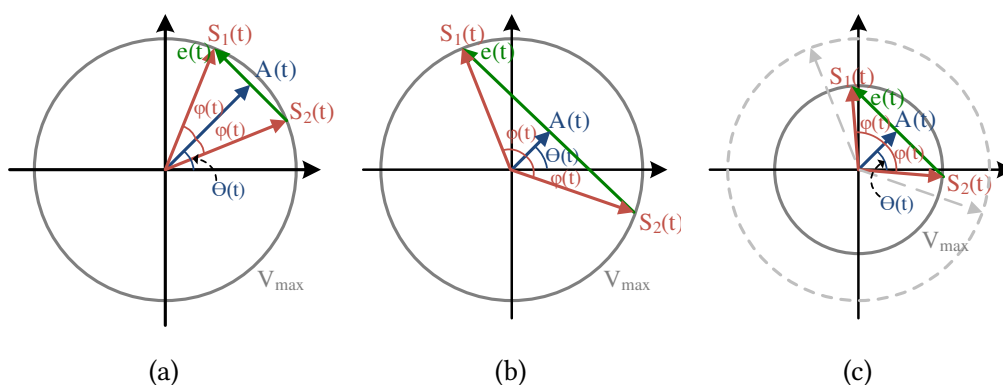


Figure 3.16: Outphasing signal representation of signals with different amplitudes.

outphasing vectors, which is the most common method in LINC transmitters, is shown in Fig. 3.16 for a few different signal amplitudes. As it can be seen, if the signal amplitude is close to  $V_{max}$ , the outphasing angle would be smaller. On the other hand, if the amplitude is decreased, the outphasing angle gets larger, which results in a much smaller efficiency as most of the power of the two outphasing signals is used to cancel out each other in the opposite direction. In the worst cases, when the signal amplitude is close to zero, the outphasing angle will be around  $90^\circ$  and as a result, a huge amount of the power of  $S_1(t)$  and  $S_2(t)$  is wasted to cancel out each other. Besides, as it is illustrated in Fig. 3.16c, if the same small vector of Fig. 3.16b is presented by outphasing vectors with a smaller  $V_{max}$ , a smaller outphasing angle can be used.

In order to describe the outphasing concept mathematically, the signal  $V(t)$  is considered in the polar plane with a phase,  $\Phi(t)$ , and an amplitude,  $A(t)$ :

$$V(t) = A(t)e^{j\theta} . \quad (3.13)$$

As a result, the outphasing vectors can be formulated as:

$$\begin{aligned} \varphi(t) &= \cos^{-1}\left(\frac{A(t)}{V_{max}}\right), \\ S_1(t) &= V_{max}e^{j(\theta(t)+\varphi(t))} , \\ S_2(t) &= V_{max}e^{j(\theta(t)-\varphi(t))} . \end{aligned} \quad (3.14)$$

The output signal of the transmitter after combining the outphasing signals will be their sum:

$$S(t) = S_1(t) + S_2(t) . \quad (3.15)$$

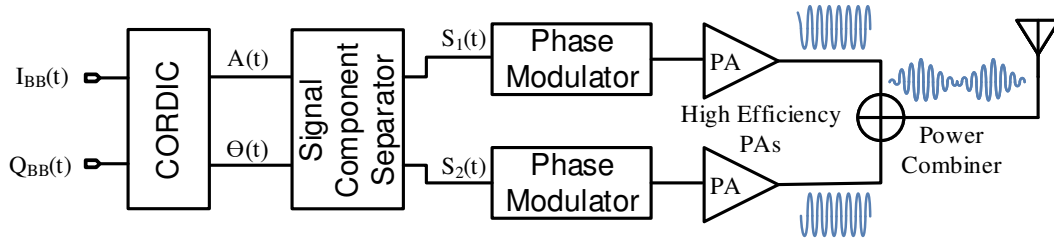


Figure 3.17: Simplified block diagram of a general LINC transmitter.

Fig. 3.17 presents a simple block diagram of a LINC transmitter. The input signal, which is represented by its phase and amplitude, is decomposed into outphasing signals  $S_1$  and  $S_2$  through a Signal-Component Separator (SCS) block. The resultant signals, which have constant envelopes and incorporate only phase modulation, are then up-converted and amplified by nonlinear highly-efficient PAs in two different paths. Then, the amplified signals are added up in a combiner with sufficient isolation between the two paths.

### Drawbacks and Benefits of Outphasing Transmitter

Clearly, with a high linearity, the outphasing architecture could be a good choice for transmitting LTE signals as it can provide good in-band accuracy and limited out-of-band emissions. Although the linearity of the combined high-frequency signal can be kept very high, non-linear PAs could be used. Since constant envelope signals are processed in each of the paths, the non-linearity of PAs does not play any role in the linearity of the whole transmitter system. On the other hand, the lower criteria for linearity of PAs allows to design them with a very high efficiency.

However, this single-level outphasing architecture has not been very successful in drawing much attention in practical designs. To begin with, mismatches between the two paths can reduce the linearity significantly. These can be phase, gain, or delay mismatches between the two paths. When such imbalances exist,  $S_1$  and  $S_2$  cannot cancel unwanted components of each other entirely. Therefore, such an incomplete vector cancellation leads to distortion in the reconstructed signal. In the frequency domain, one can interpret that the expanded spectrum of  $S_1$  and  $S_2$  do not cancel each other completely due to mismatches, which leads to out-of-band emission as well as in-band distortion. This results in decreased ACLR and increased EVM of the transmitted signal.

Another problem with an outphasing transmitter is that the input digital baseband data, which is generally in Cartesian I/Q coordinates, needs to be converted to Polar representation and then the outphasing vectors need to be generated through SCS. Therefore, in the first step, a CORDIC is required to convert the I/Q digital baseband

signal to polar coordinates. As a result, this system also suffers from the well-known problem with bandwidth expansion in Polar transmitters, explained in section 3.1.4. Additionally, the nonlinear operation of SCS in (3.14) adds up to the bandwidth expansion of CORDIC.

Furthermore, even with PAs with an efficiency of 100 %, the overall system efficiency drops significantly at output back-off power levels as more power is consumed in the combiner. In other words, when the signal amplitude is reduced, the outphasing angle gets larger and more power of  $S_1$  and  $S_2$  is wasted to cancel out unwanted parts of each other. The drain efficiency with ideal elements can be formulated as in (3.16):

$$\eta(t) = \cos^2(\varphi(t)) = \left(\frac{A(t)}{V_{max}}\right)^2. \quad (3.16)$$

In comparison to class B or class A PAs, the outphasing architecture provides 100 % efficiency at the peak power. However, with a normalized amplitude of lower than 0.8, it results in an efficiency lower than an ideal class B PA.

#### 3.2.4.2 Multi-Level LINC Transmitter

In order to increase the efficiency of an outphasing transmitter, the outphasing angle needs to be limited. For this purpose, additional amplitude levels can be introduced for a smaller output power. Fig. 3.18 illustrates such a technique for different signal amplitude levels. With multiple levels and for a symmetrical SCS, the decomposition algorithm does not change significantly. Compared to a single-level outphasing system, instead of  $V_{max}$ , the amplitude of outphasing signals,  $S_1$  and  $S_2$ , is selected to be the closest existing level larger than the primary input signal. As a result, with the additional levels, the outphasing angle is reduced and hence, less power is dissipated in the combiner. Such a technique can be simply implemented by modulating the supply of the switching PAs in Fig. 3.17. In contrast to that of a single-level outphasing transmitter, the peak efficiency is not different; however, at back-off power levels where larger outphasing angles would be required, the efficiency of the single-level version drops while switching to a smaller outphasing signal level in ML-LINC results in a much better efficiency performance.

#### Number and Positions of Levels

Evidently, the number of levels and their locations play important roles in the performance of the ML-LINC transmitter system. It can be easily reasoned that a higher number of levels can restrict the outphasing angle to smaller values, which leads to better drain efficiencies at output back-off power levels. For instance, assuming an ideal case of an

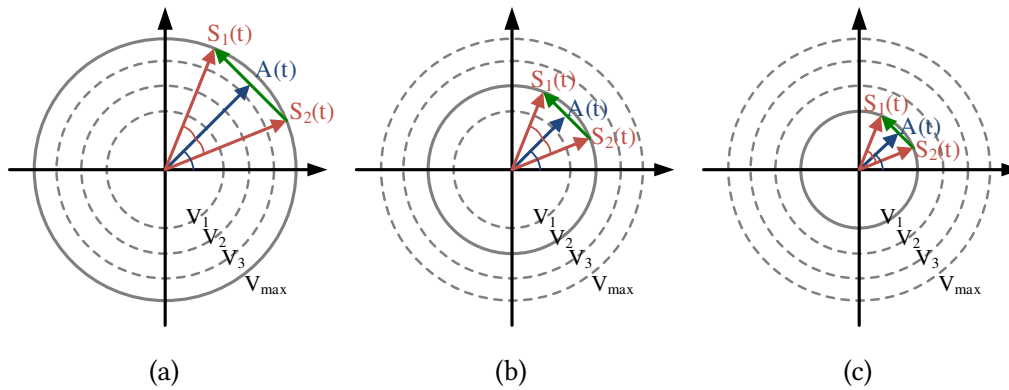


Figure 3.18: ML-LINC signal decomposition for different amplitudes.

infinite number of levels, both  $S_1$  and  $S_2$  would be the same as the original signal and therefore, no power is dissipated in the combiner. However, in practice, the number of levels is limited to the resolution of the digital signal as well as that of the analog frontend. With a finite number of levels, the location of levels also affects the efficiency of the transmitter system. The signal statistics vary depending on the input signal modulation scheme. Optimized positions of levels can be achieved in order to maximize the average **Power-Added Efficiency (PAE)**. The complexity of such an optimization problem does not allow for on-chip implementation. It is also important to note, however, that optimizing positions of levels does not contribute to achieving much higher average efficiency when the number of levels is very high. In other words, when there exist many levels for the same output power range, e.g. 1000, even with equally-distanced levels, the outphasing angle would be very small. This can result in a negligible change in the average efficiency with statistically optimized locations of levels. Clearly, the effect of optimized levels also depends on the dynamic range of the output power. In case a larger dynamic range is provided, the difference between levels gets larger in general.

In addition to the average efficiency, the number of levels affects the linearity of the **ML-LINC** transmitter as well. As mentioned earlier,  $S_1$  and  $S_2$  suffer 4 to 10 times bandwidth expansion due to Cartesian to Polar coordinate conversion through **CORDIC** and the nonlinear operation at **SCS**. Since the filtering characteristics of each path are different in practice, the out-of-band components of  $S_1$  and  $S_2$  cannot cancel each other in full. Therefore, As a consequence of a limited bandwidth of each amplification path, out-of-band emissions are raised, which results in degradation of **ACLR**. Provided that a higher number of levels exists, the outphasing angle becomes smaller and outphasing signals become more similar to the original signal, which does not suffer bandwidth expansion. In other words, since the phase difference of these signals becomes smaller, canceling out the out-of-band expansion would be less prone to the limited bandwidth of the paths.

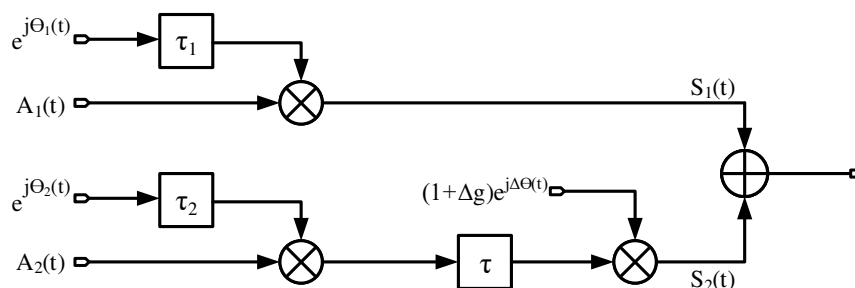


Figure 3.19: Time-domain model of impairments in an ML-LINC transmitter.

### Mismatch between the amplification paths

One of the important factors to consider during the system design of a transmitter is the effect of non-idealities of practical circuits on the performance of the system. Similarly, such practical imperfections can cause considerable degradation in the ML-LINC architecture as well. These include limited bandwidth and delay between amplitude and phase in each branch as well as mismatches between the two outphasing paths. The latter consists of static gain and phase mismatches, dynamic delay mismatch, and bandwidth differences.

Deriving analytical expressions for the effects of the mentioned imperfections on the transmitter linearity might help to get a better understanding. However, rather than complex equations with only one imperfection at a time, system simulations through models of these imperfections can give a better sense of their effects. According to simulation results, a number of constraints can be determined for each non-ideality so that the transmitter system performance remains within the acceptable limits specified by the communication standard or its application use case. For this purpose, a mathematical model of non-ideal effects, such as the one presented by [42], needs to be reviewed.

The outphasing principle equations of (3.14) and (3.15) are used as the base of this mathematical model. Fig. 3.19 presents such a model in the time domain. An AM/PM delay in each branch is modeled by delay values,  $\tau_1$  and  $\tau_2$ , in the path of the phase modulator in each branch. The delay mismatch between the two paths is modeled by a delay,  $\tau$ , which only exists in the path of  $S_2(t)$ . The gain and phase mismatches are also modeled by  $\Delta g$  and  $\Delta\theta$  in the second branch. As a result, the distorted output can be mathematically expressed by:

$$S'(t) = A_1(t)e^{j\theta_1(t-\tau_1)} + A_2(t-\tau)e^{j\theta_2(t-\tau_2-\tau)}(1+\Delta g)e^{j\Delta\theta}. \quad (3.17)$$

It is beneficial to derive a model in the frequency domain as well. A simple Fourier transform can do the job:

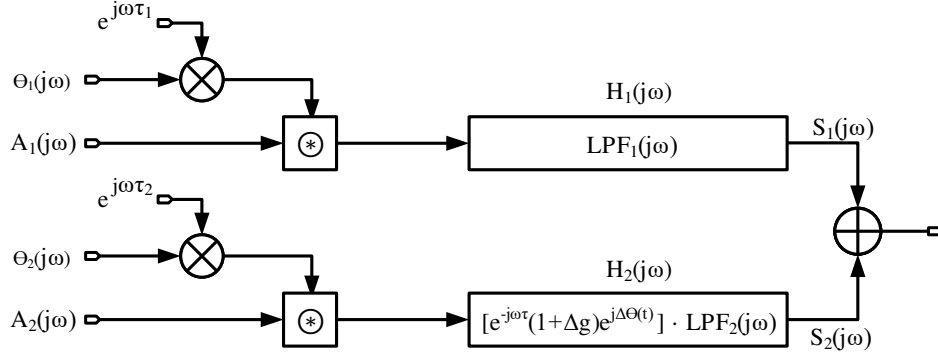


Figure 3.20: Frequency-domain model of impairments in an **ML-LINC** transmitter.

$$S'(j\omega) = A_1(j\omega) * (\Theta_1(j\omega)e^{-j\omega\tau_1}) + [A_2(j\omega) * (\Theta_2(j\omega)e^{-j\omega\tau_2})] e^{-j\omega\tau} (1+\Delta g)e^{j\Delta\theta}. \quad (3.18)$$

Fig. 3.20 depicts such a frequency model. Delays between amplitude and phase in each path appear as factors,  $e^{-j\omega\tau_1}$  and  $e^{-j\omega\tau_2}$ , to the phase of each path in the frequency domain. The rest of the impairments, including mismatches and delay between the two paths, appear through a transfer function in the path of  $S_2$  while that of  $S_1$  remains unity. An advantage of the frequency-domain model is that bandwidth limitations and differences can also be added. For this purpose, simply a low-pass transfer function with a corner frequency of  $\omega_0$  is added to the  $H_1$  while another one with a corner frequency of  $\omega_0 + \Delta\omega$  is added to  $H_2$ .

### 3.3 Conclusion

This chapter presented different transmitter architectures with the focus of digital-centric ones to be used for a multi-standard system. Analog direct conversion and two-step transmitters are based on I/Q modulation. Analog polar transmitters show a better power efficiency; however, the bandwidth expansion of phase and amplitude signals can cause spectral regrowth and increases out-of-band emissions. That is why polar systems are mostly used for lower-bandwidth signals. Furthermore, a timing mismatch between phase and amplitude can add up to out-of-band emissions.

Digital-centric transmitters have been developed to provide high reconfigurability and benefit higher speed and smaller area and power consumption of modern technology nodes where analog performance is degraded due to short-channel effects and reduced voltage headroom. However, such digital systems do not allow for reconstruction filters

in small unitcells of an **RF-DAC** frontend, which results in spectrum replicas of the baseband signal at **RF** and raises out-of-band emissions. As a result, a higher baseband signal sampling rate should be applied to shift the replicas away and suppress them further by the sinc transfer function of **ZOH** sampling in the **RF-DAC**. Furthermore, the data sampling clock frequency should be an integer fraction of the **LO** frequency, which requires a clock domain crossing from the baseband clock domain of the signal generator to the **LO** clock domain. These restrictions add to the complexity of the **DSP**. The frontend should be implemented with special attention to its nonlinearity due to the finite output impedance of unitcells as well as the timing mismatch between them, which requires careful symmetrical distribution of signals in the layout.

A Digital I/Q transmitter is implemented on the basis of I/Q modulation through employing two frontends with a  $90^\circ$  **LO** phase shift, where the use of **LO** signals with 25% duty cycle helps achieving a better power efficiency. In contrast to analog polar transmitters, their digital-centric alternatives benefit the better digital performance of advanced **CMOS** technologies in both AM and PM paths. Furthermore, the alignment of phase and amplitude path delays in the digital domain is way more straightforward compared to the analog domain. For a better linearity, digital-centric multi-level **LINC** transmitters, which produce two outphasing signals and reconstruct the desired one with recombination of these two, have been developed. However, the imperfections of such complex systems present a number of challenges to be addressed. The number and positions of levels affect the power efficiency as well as the linearity of the system to some extent. Moreover, the mismatch between the outphasing paths imposes a risk of degraded linearity in **ML-LINC** transmitters and needs to be considered carefully to meet the targeted linearity specifications.

# Chapter 4

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## Digital Modules of the Digital-Centric Transmitter

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Digital Signal Processing (DSP) of the baseband signal plays an important role in achieving a promising performance out of a digital-centric transmitter. Therefore, this chapter goes through different DSP blocks of the implemented transmitters in detail. A general view of digital modules of such a transmitter can be regarded as presented earlier in Fig. 3.5. Initially, data needs to be received from the baseband generator, which is usually a separated off-chip module. A clock domain crossing needs to be followed so that data are transferred from the baseband sampling clock to the LO clock domain. Furthermore, a number of upsampling steps should be included to push the sampling replicas farther away from the desired RF frequency ( $f_{LO}$ ) and provide a better ZOH attenuation of these replicas. Other than that, a few modules might be needed to enhance the performance of the RF frontend. Since only simple operations can be performed at higher sampling rates, these performance enhancement modules have to be implemented at an intermediate sampling rate. For this reason, the upsampling steps are divided into two parts and in between, the compensation operations are performed. Also, another module is needed to provide the right control signals for the frontend and it needs to be the last module of the digital signal path, which operates at highest sampling rate and directly feeds the frontend.

The chapter organization is as follows. First, the digital interfaces needed to transfer data and configuration bits are discussed in section 4.1. Then, section 4.2 introduces the different employed upsampling techniques, which are called pulse-shaping and CIC filters. Section 4.3 reviews the digitally-assisted compensation of frontend imperfections to enhance the transmitter performance. Next, the DDRC element selection techniques and their logic implementations are followed in section 4.4. It should be mentioned that many of these general digital modules were already developed and reported by [16]. However, these are adapted depending on the applications and requirements of this work; and a number of modifications or enhancements are applied to them, accordingly.

## 4.1 Interfaces

As a first step to transmit a signal sequence through the antenna, the baseband input data stream, which is usually generated in a separate baseband signal processing source such as a **Baseband Integrated Circuit (BBIC)** or a **Field-Programmable Gate Array (FPGA)**, needs to be transferred to the transmitter system **RFIC** through a data interface. Such an interface must establish a reliable high-speed data transmission link to support the input data rates of the transmitter system. Furthermore, configuration settings need to be transferred to the configuration register file of the **RFIC**. Due to the high-speed requirement, many general interface architectures cannot be employed for both of the aforementioned purposes. As a result, a high-speed synchronous interface with a **Clock Domain Converter (CDC)** is used to perform the data transmission through **Low-Voltage Differential Signaling (LVDS)**, which provides faster speeds with lower crosstalk impact due to lower voltage levels [76]. Due to the complexity of such an interface, a low-speed asynchronous interface called SerIAS is also included in the **RFIC** to support the main high-speed one as a backup solution. Since this **RF** transmitter is implemented for test and research purposes, instead of a **BBIC**, an **FPGA** is used to provide the required baseband signal to the **RFIC** through the interfaces as well as to configure the **RFIC** and control the measurement steps.

### 4.1.1 CAG/IOv2 High-Speed Data and Configuration Interface

Fig. 4.1 shows a block diagram of the CAG/IOv2 interface, which was originally used by [16] and is adapted to the applications of this work. The interface consists of two main serial lanes for transferring In-phase and Quadrature data from an **FPGA** to the Chip. This ensures that the data rate can be maximized as required by high-speed standards such as **LTE** or **WLAN**. Additionally, a lane is considered to transfer the serial synchronizing clock so that the necessity of having a complex clock recovery circuit on the **ASIC** side is eliminated. A fourth lane is also used to transfer required data from the **ASIC** back to the **FPGA**. This lane is required for initialization and establishing the interface link as well as for monitoring and debugging the operation of digital blocks.

As mentioned earlier, the connection is made through **LVDS**. The signal to be transferred is first converted to a differential current at the transmitter side and then is converted back to the voltage domain through a termination resistor at the receiver side. This helps the reliable transfer of serial data with a higher frequency while at the same time, the interference of digital switching noise into the RF domain is reduced. With 4 lanes, 8 pins are needed to connect the **ASIC** to the **FPGA** through this interface. A CML-to-CMOS converter circuitry is employed to provide a readable single-ended **CMOS** input for the digital part. With a constant current flowing to bias a **Current-Mode Logic (CML)**, which

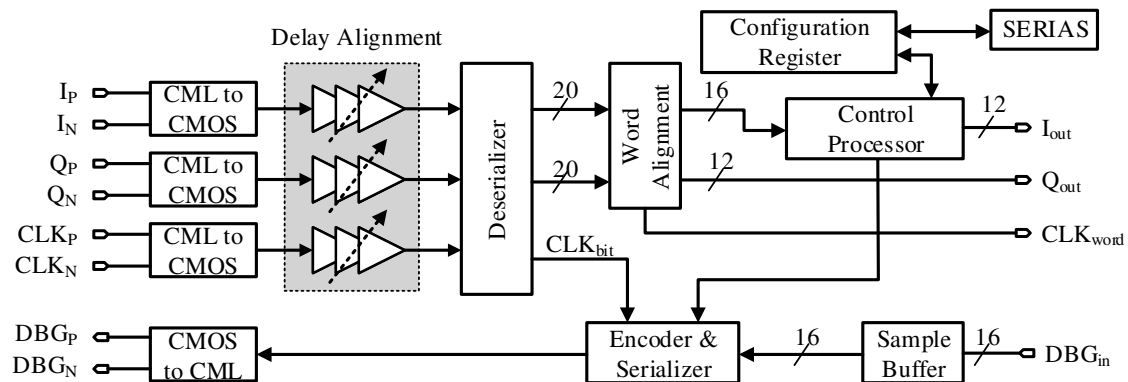


Figure 4.1: Block diagram of the CAG/IOv2 interface architecture.

sends and receives **LVDS** data through the pins rather than strong **CMOS** buffers, ground bouncing and supply sag are reduced [77].

Since no clock recovery circuit is implemented on the **ASIC** side, an adjustable delay line is considered for each of the three receiving lanes. This provides the possibility of bit alignment with an optimum timing for sampling of data as well as a minimum delay between I and Q paths. The bit-aligned data is deserialized, resulting in two parallel data words. These I and Q data words are then aligned with each other by detecting the data word boundaries. This also generates a word clock ( $CLK_{word}$ ) out of dividing the bit-aligned serial clock signal ( $CLK_{bit}$ ).  $CLK_{bit}$  is further used to transmit the debug data through the serializer. After word alignment, the I data is passed to the control processor as it can also contain a control command according to its header. This unit communicates with the configuration registers in addition to the SerIAS interface, which is only a backup interface for accessing these registers.

Using an **FPGA** board of Virtex 7 family, the interface on the **FPGA** side is implemented through GTX transceiver IP blocks provided by XILINX. The data bits are transferred with **Dual Data Rate (DDR)**, which means they are sampled by both rising and falling edges of  $CLK_{bit}$  in receivers. The delay of the clock lane is adjustable by a half-cycle resolution so that the transferred bits can be sampled with the best timing.

### Interface Protocol Through Characters

Every transfer of data is done with an 8b/10b encoding. For the control purposes, each transferred word is 20 bits, which consists of two 8b/10b control characters. These control characters are listed in Table 4.1. For the purpose of initialization of the link, first, the **FPGA** sends the INIT control word, which is only a serial clock pattern. The bit alignment blocks change the delays of both I and Q serial data and the interface logic compares the deserialized input word with the known pattern. In this way, it finds the

Table 4.1: Control characters of the CAG/IO interface.

Name	8b/10b characters
INIT	n.a. (xAAAAAA)
ALIGN_CHAR	K.28.5 K28.5
READY_CHAR0	K.28.4 K.28.4
READY_CHAR1	K.23.7 K.23.7
DATA_START	K.28.1 D.14.1
DATA_END	K.28.2 K.23.7
CTRL_WRITE	K.23.7 D.14.1
CTRL_READ	K.28.1 D.20.1
CTRL_END	K.28.2 K.28.0

minimum and maximum delays where the data pattern is received with no bit errors and consequently, adjusts the delay of each receiver lane to be the mean value in order to avoid metastability errors and guarantee correct sampling. Afterwards, the ASIC sends back the INIT word through the Debug lane.

On the FPGA side, after receiving the INIT pattern back from the ASIC, the FPGA transfers READY\_CHAR0 and ALIGN\_CHAR alternatively. The READY\_CHAR0 informs the ASIC to search for the ALIGN\_CHAR, which is a comma character and contains a bit pattern that is unique and cannot be seen in the data stream. Through this phase, the interface adjusts the boundaries of received data words on the ASIC side by detecting the ALIGN\_CHAR. In other words, the received deserialized input word is shifted bit by bit until this character is detected. In the next step, the ASIC sends READY\_CHAR1 followed by ALIGN\_CHAR repeatedly to the FPGA. In this way, the receiver of the FPGA adjusts itself and becomes ready for receiving data through the debug lane in the same way. This would establish the interface link and the transfer of data can be started next to that.

During the transfer of data or control configurations to the ASIC, the debug lane is not used. Therefore, it remains in an idle mode in which the ALIGN\_CHAR is repeatedly transferred to the FPGA.

As it can be seen in Table. 4.1, there are also a number of characters to specify whether data or control words are being transferred. When a data transfer is going to be started, first, a DATA\_START character is sent, which means infinite transfer of data words. However, the interface is also used to transfer control words to or from the control registers. For this purpose, a DATA\_END character ends the transfer of data and depending on the control word read or write direction, either of CTRL\_READ or CTRL\_WRITE is send to the ASIC. At the end of transferring the control word, a CTRL\_END indicates the end of the control frame and a data frame starts immediately afterwards.

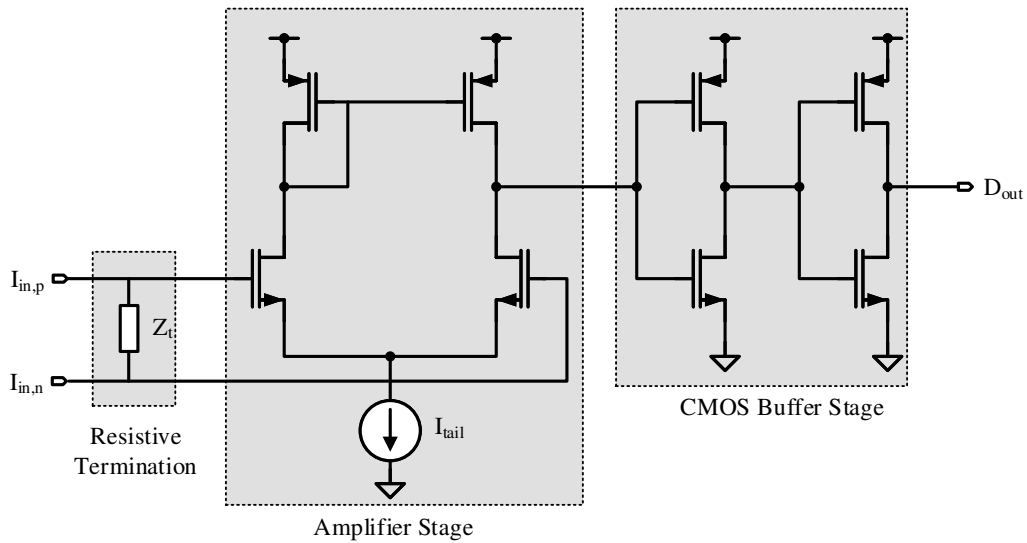


Figure 4.2: CML-to-CMOS converter circuit implementation.

### CML Converters As Input and Output Buffers

As mentioned earlier in this section, a current-mode **LVDS** is used to transfer data through the interface. This provides the possibility of operating at a higher frequency compared to **CMOS** [78] while it is also less prone to interference and coupling due to its differential nature [79]. Furthermore, although it has a higher static power consumption, CML logic can be more power efficient in higher data rates since the voltage swing can be much lower [80].

The schematic of CML-to-CMOS converters used for the CAG/IO interface in this work is depicted in Fig. 4.2. It consists of a  $100\Omega$  termination resistor that converts the differential input current to a low-swing differential voltage and then a single-ended amplifier which amplifies it. The output of the amplifier is fed to two **CMOS** inverters to buffer it and provide a full-scale **CMOS** output with a rail-to-rail swing.

For the reverse direction, which transfers the data from the **ASIC** to the **FPGA** through the debug lane, the CMOS-to-CML converter is realized with the circuit shown in Fig. 4.3 [81]. The current  $I_{bias}$  is always flowing to ground. However, the path would be different depending on the bit to be transferred. Considering the  $100\text{-}\Omega$  termination impedance on the **FPGA** side, when the input bit,  $D_{in}$ , is high, the current flows from  $I_{out,p}$  through the termination resistor to  $I_{out,n}$  and ground. This creates a positive voltage over the termination resistor. On the other hand, when the input bit is low, the current flows from  $I_{out,n}$  to  $I_{out,p}$ , which creates a negative voltage at the **FPGA** side.

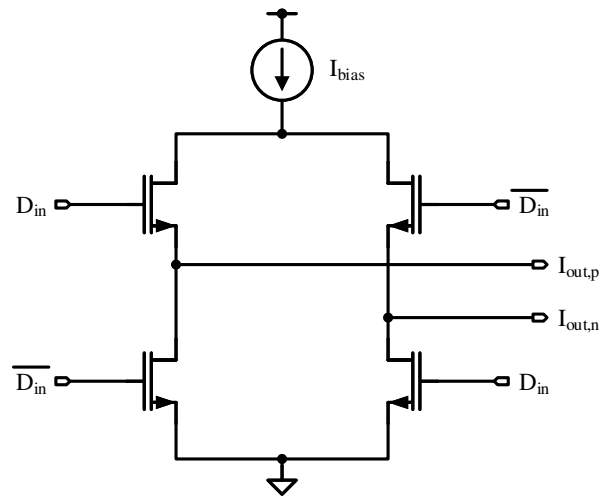


Figure 4.3: CMOS-to-CML converter circuit implementation.

### Delay Alignment

Each receiver lane of the interface includes an adjustable delay line in order to align it for the lowest errors through **DDR** sampling of serial bits. The delay line that is depicted in Fig. 4.1 consists of 16 delay elements. The desired output is selected through a 16-to-1 multiplexer, which is controlled with a 16-bit one-hot code. The optimum delay is adjusted in the alignment phase as the first step of initialization of the interface.

The delay elements are implemented by two cascaded inverters, creating a non-inverting buffer. Since the sampling of received bits is done in **DDR** mode, it is necessary for delay elements to have rather the same propagation delays for both rising and falling edges of the signal in all operating conditions. Therefore, the inverters are sized in a way that the delays match for different corners of the technology. Monte-Carlo simulations show that the delay of each element can be in the range of 16 ps to 29 ps. This means that the input can be delayed up to 256 ps in the fastest corner. Considering a maximum bit clock frequency of 1 GHz, the input can be delayed up to at least a quarter of the clock cycle, which would be sufficient to avoid avoiding sampling error in the receiver lanes. With these specifications of the delay line, it is expected that a correct bit alignment is feasible for baseband clock frequencies in the range of 80 Mhz to 120 Mhz.

### Digital Processor of the Interface

The Digital part of the interface, which is fully described in Verilog and VHDL, consists of a serializer, a deserializer, a word aligner, and a control processor. In both of the deserializer and the serializer, negative-edge-triggered registers offered by the technology

are used, which enable a **DDR** operation without inverting the clock [16]. The 8b/10b encoding is matched with the one performed on the **FPGA** side. The control processor takes care of a correct sequence of initialization steps and detection of data and control frames. It includes a number of **Finite-State Machine (FSM)** in different levels.

### Speed Consideration

The CAG/IOv2 interface is originally designed to transfer with data rates up to 1.6 Gbps per lane. Each 12-bit data word is extended with 4 bits header and then encoded with an 8b/10b encoding scheme, which results in 20 bits per data word. As a result, for a baseband sampling frequency of 100 MHz, a data rate of 2 Gbps per lane is required:

$$R = (12 + 4) \times \frac{10}{8} \times 100 \text{ MHz} = 2 \text{ Gbps} . \quad (4.1)$$

Taking the **DDR** sampling at the receiver side into account, this requires a serial bit-clock with a frequency of 1 GHz to be transferred. In practice, 1 GHz can be beyond the limit for the serializer, which is implemented through standard cells of the technology. Measurements of the prototypes, reported in [16], show that this interface provides a more robust performance and transfers the signals error-free with a lower serial bit-clock frequency of 800 MHz. This results in a baseband sampling frequency of 80 MHz, which is of interest for the first transmitter implemented in this work. For example, a WLAN signal with a bandwidth of 20 MHz can be upsampled with a **USR** of up to 4 and can be transferred error-free to the **ASIC**.

The 100 MHz data bandwidth limitation of the original CAG/IOv2 interface does not allow for higher signal bandwidths of more advanced communication standards such as 160 MHz signals in 802.11ac, which is of interest for the **ML-LINC** transmitter reported in this work. Alternatively, in order to transfer data with a higher data bandwidth, an improved version of the interface is also implemented by doubling the number of data lanes. The block diagram of this higher-speed interface is presented in Fig. 4.4. On the transmitting side, two consecutive data samples are buffered and transferred at the same time. Two lanes transfer the I data and two lanes transfer the Q data while the deserializer at the receiving side combines the data bits of each of these pairs to regenerate the transmitted parallel data samples. In this way, the interface can operate with a serial bit clock with the same frequency as that of the original version of CAG/IOv2 interface while a data-rate improvement of factor two is achieved.

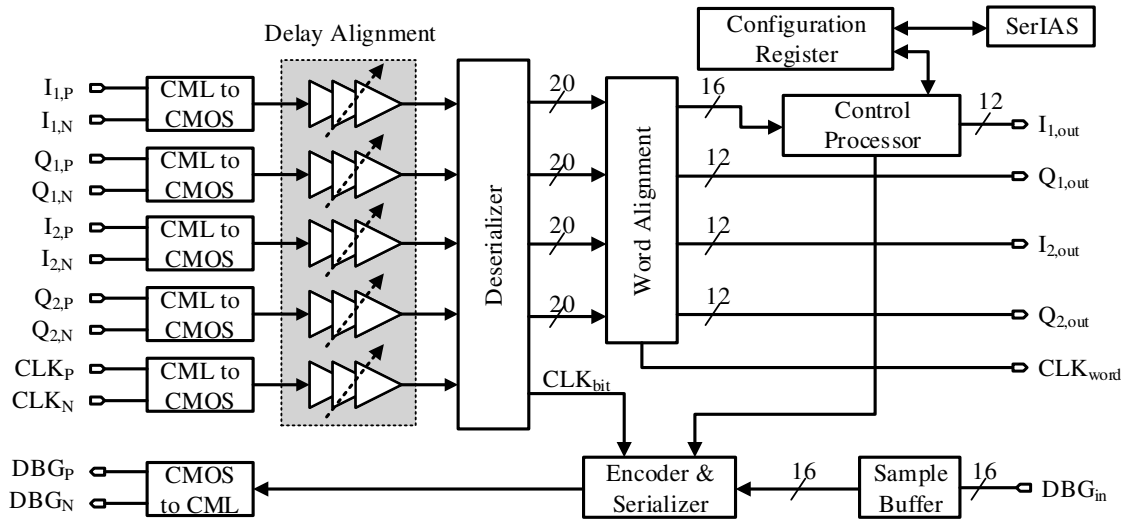


Figure 4.4: Block diagram of the CAG/IOv3 interface with a double speed configuration.

### 4.1.2 SerIAS Configuration Interface

Due to the high complexity of the CAG/IO interface, a backup solution called SerIAS has also been implemented. It is mainly a **UART**-based serial interface presented in [82], which is incorporated in the design in addition to CAG/IO in order to be able to transfer configuration data to the ASIC and read back from its register file. With the use of this interface, the PC can be directly connected to the **ASIC** through a **USB-to-UART** bridge.

The communication is initiated through a programming word from the PC and **ASIC** gives a response accordingly. Each programming word consists of a command, an address pointing to a register in the register file, and a number of data bits. There are eight commands provided by this interface that allow for setting a register, initializing it, or requesting its value as well as resetting the whole register file or even the whole **ASIC**. Depending on the programming command from the PC, the **ASIC** might send a response data in order to either confirm the operation or send a requested data.

## 4.2 Sampling Rate Conversion

A digital-centric transmitter should implement the requirements of the clocking frequencies explained in section 3.2.1. These include having a sampling frequency as high as possible, which needs to be derived from the **LO** signal. The input signal is received through the interface in the baseband clock domain that originates from a **BBIC** or an

**FPGA.** As a result, it needs to be upsampled to a much higher clock frequency in the **LO** domain. Furthermore, the upsampling should be adaptable to different clocking schemes depending on the communication standard so that a multi-standard system can be realized. For this purpose, first, the input baseband data is upsampled to an intermediate frequency, called **CLK\_SLOW**, where the signal processing operations can be applied to the input signal. A second sampling rate conversion is additionally required to upsample the data to **CLK\_FAST** that is the output sampling frequency of the digital to be mixed with **LO** in the frontend.

### 4.2.1 Pulse-Shaping Filter

Since the **LO** clock and the baseband clock come from different clock domains, there is always a need to synchronize the input data in the baseband clock domain with a divided version of **LO**. Consequently, an **Arbitrary Sampling-Rate Conversion (ASRC)** is needed. In some implementations of digital-centric transmitters, most signal processing steps are performed in the baseband clock domain, which requires a clock domain conversion at higher frequencies [10]. This would increase the power consumption and requires low-complexity operations in each clock cycle to avoid timing violations. The better approach is to perform the clock domain conversion directly at baseband. For this purpose, the **Pulse-Shaping Filter (PSF)** proposed in [83] is adopted. This architecture can perform a fractional **ASRC**, which is needed as the two clock domains can be completely unrelated.

The block diagram of the **PSF** upconverter is presented in Fig. 4.5. First, the input data is buffered in the clock synchronization block, which is simply a **FIFO**, in order to cross to **CLK\_SYNC** in the **LO** clock domain with a clock frequency as close as possible to **CLK\_IN**. This clock signal is generated through the timing control block by having the **Inverted UpSampling Ratio (IUSR)** from the configuration registers. However, since **CLK\_OUT** and **CLK\_IN** are unrelated and the resolution of **IUSR** cannot be infinite, there might be a frequency difference between **CLK\_SYNC** and **CLK\_IN**, which causes a clock shift. This results in errors in clock domain crossing when the read and write pointers of the clock synchronization **FIFO** reach each other. Even with this problem, depending on the size of the **FIFO**, it operates without any error for a period of time that is adjusted to be larger than a data burst time in the worst-case scenarios. With this regard, it is also taken care of that at the beginning of each data burst, the **FIFO** is reset so that enough time is provided in order to avoid errors. The resulting signal,  $D_{sync}$ , which is sampled with **CLK\_SYNC** is fed into the upsampling filter.

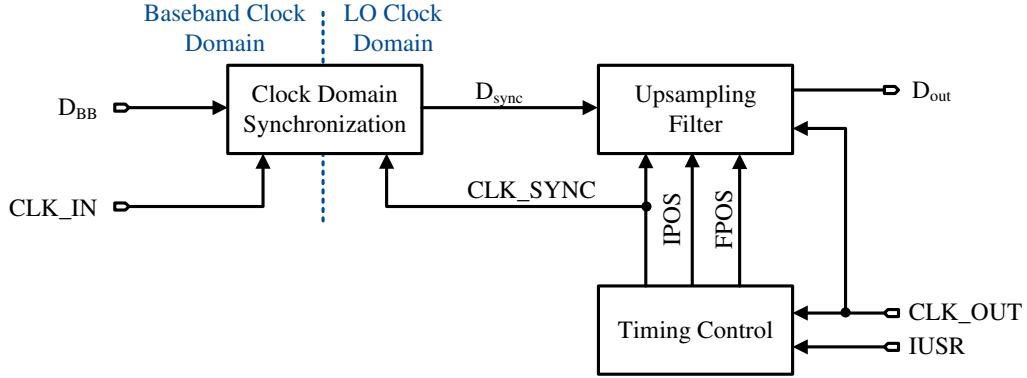


Figure 4.5: System architecture of the pulse-shaping filter.

### Modified Generalized Farrow Upsampling Filter

Farrow filters have been widely used to implement fractional upsampling [84]. However, poor image suppression of these filters degrades the performance of transmitter systems operating in today's LTE or WLAN standards. Polyphase filters implemented through a Finite Impulse Response (FIR) can be used alternatively. Yet, the implementation of an upsampling filter with a classical FIR structure limits the number of possible USRs, which is not favorable for a multi-standard system [85]. As a solution to overcome these limitations, a modified version of generalized farrow filters that combines both aforementioned structures is adopted from [83]. The block diagram of this filter is presented in Fig. 4.6. It can be seen that, like every other FIR upsampling filter with an order of  $K$ , the output can be written as the sum of a number of input samples each multiplied by the corresponding upsampling coefficient,  $c_k$ :

$$D_{out}[n] = \sum_{k=0}^{K-1} c_k \cdot D_{sync}[USR \cdot (n - k)]. \quad (4.2)$$

$K$  samples of the input data are provided through a shift register operating with  $CLK\_SYNC$ . For the purpose of using the features of a generalized farrow filter, at every time step, each upsampling coefficient,  $c_k$ , is a linear combination of two consequent FIR filter coefficients,  $h_i$  and  $h_{i+1}$ . This combination can be written as:

$$c_k = h_{k.N+IPOS} + (h_{k.N+IPOS+1} - h_{k.N+IPOS}) \cdot FPOS; \quad 0 \leq k \leq K - 1. \quad (4.3)$$

$N$  is the integer USR that determines the number of interleaved FIR coefficients for each of the upsampling filter coefficients,  $c_i$ . In other words, the USR can be any real value in the range:

$$N - 1 < USR \leq N. \quad (4.4)$$

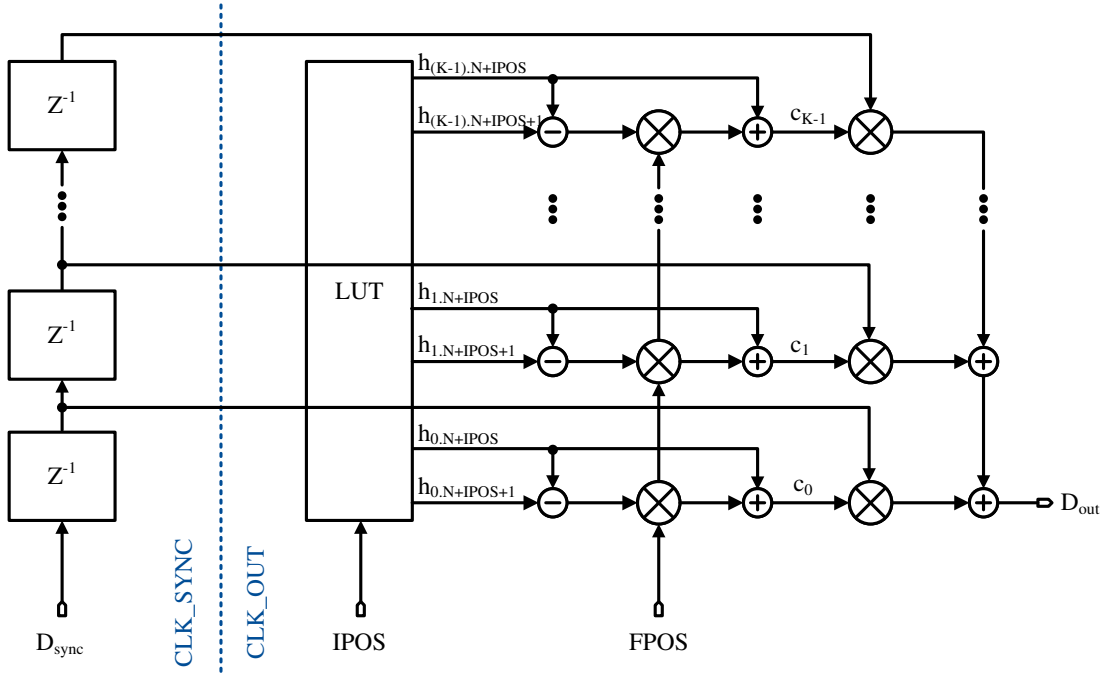


Figure 4.6: Modified generalized farrow upsampling filter.

IPOS and FPOS, which denote integer and fractional positions respectively, are both provided by the time control block with each CLK\_OUT cycle. Therefore, they are limited to the following ranges:

$$\begin{aligned} 0 \leq IPOS &\leq N - 1, \\ 0 \leq FPOS &< 1. \end{aligned} \quad (4.5)$$

It can be concluded that the number of required FIR filter coefficients,  $h_i$ , is given by:

$$I = N \cdot K. \quad (4.6)$$

In the context of transmitters implemented in this work, considering different standards in which the transmitter should be able to operate, the PSF is designed for an integer USR of  $N = 5$  with a filter order of  $K = 16$  which needs  $I = 80$  coefficients of the FIR filter impulse response,  $h_i$ .

It can be figured out that in the case of an integer USR, where FPOS is always 0, IPOS is generated through a counter with CLK\_OUT that counts repeatedly from 0 to  $N - 1$ . Therefore,  $c_k$  would be the result of interleaving 5 different coefficients, which results in achieving a USR of 5. For instance, for the first coefficient,  $c_0$ , in each CLK\_SYNC cycle, values of  $h_0, h_1, h_2, h_3,$  and  $h_4$  are output one after the other with a 5-time higher frequency of CLK\_OUT. For a non-integer USR, the combination of IPOS and FPOS

needs to count faster to result in a smaller **USR**. In this way, according to (4.3), the upsampling coefficients are calculated with a linear interpolation between the impulse response coefficients of the filter. For instance, assuming a **USR** of 4.5, coefficients must be output  $\frac{1}{9}$  faster in reference to **CLK\_OUT**. Therefore, starting from 0, the real value of  $IPOS + FPOS$  grows by  $\frac{10}{9}$  with each **CLK\_OUT** cycle. **FPOS** is directly output as achieved with this summation. However, since **IPOS** can only have values out of the set of  $\{0, 1, 2, 3, 4\}$ , it is reduced by 5 whenever the summation result overflows 5.

## 4.2.2 CIC Filter

After the signal processing tasks are carried out at an intermediate frequency, as mentioned earlier, it is required to perform another upsampling on the data signals to push **RF-DAC** output replica spectra as far as possible from the band of operation. Using a conventional **FIR** upsampling filter with lots of **LUTs** and multipliers for this purpose would consume a large area and a significant power to operate at a sufficiently high frequency which can be up to 800 MHz [16]. Furthermore, at such high frequencies, only simple **DSP** tasks can be carried out in one clock cycle. To overcome such challenges, a **Cascaded Integrator-Comb (CIC)** interpolator is developed for upsampling the data signal from **CLK\_SLOW** to **CLK\_FAST** with an integer **USR**. **CIC** filters eliminate the use of multipliers while only a limited number of storage blocks are used [86].

**CIC** filters are commonly used as anti-aliasing filters before decimation as well as anti-imaging filters for interpolation [87]. A **CIC** filter is based on the low-pass characteristics of a moving average filter, which averages the input over  $M$  consecutive samples:

$$y[n] = \frac{1}{M} \sum_{k=0}^{M-1} x[n - k]. \quad (4.7)$$

Implementation of such a filter requires a lot of adders, which are to be avoided because of area and power concerns. Ignoring the  $1/M$  factor, (4.7) can be rewritten with a recursive equation:

$$y[n] = y[n - 1] + x[n] - x[n - M]. \quad (4.8)$$

The resulting transfer function is:

$$H(z) = \frac{1 - z^{-M}}{1 - z^{-1}}, \quad (4.9)$$

which can be decomposed into an integrator and a comb:

$$\begin{aligned} H_I(z) &= \frac{1}{1 - z^{-1}}, \\ H_C(z) &= 1 - z^{-M}. \end{aligned} \quad (4.10)$$

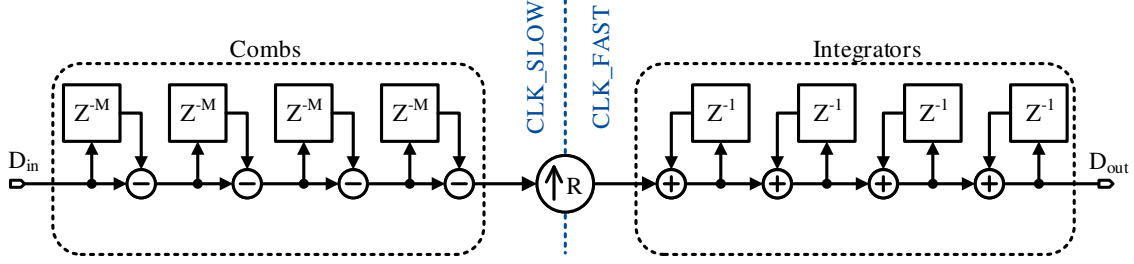


Figure 4.7: Block diagram of a CIC interpolation filter.

Each of these transfer functions can be easily implemented through only one adder and one delay element. A higher-order filtering can be achieved by cascading a number of first-order CIC filters. However, thanks to the flexibility provided by these filters, all integrators can be cascaded on one side while comb units are cascaded on the other side. When a CIC filter is used for interpolation or decimation, sampling rate conversion can be integrated within the filter by shifting all integrators to the higher frequency side and all the combs to the lower frequency side. Fig. 4.7 shows the block diagram of a CIC interpolator. The resulting transfer function of such a filter with an order of  $N$  and a sampling rate ratio of  $R$  can be written as:

$$H(z) = \left( \frac{1 - z^{-RM}}{1 - z^{-1}} \right)^N. \quad (4.11)$$

For an interpolating CIC, which is of interest for a digital-centric transmitter, the gain of the filter is  $(RM)^N$ . Therefore, the bit growth is  $\log_2 (RM)^N$  and the most significant bit of the filter output is calculated as in (4.12) [86]:

$$B_{max} = \lceil N \log_2 RM \rceil + B_{in} - 1. \quad (4.12)$$

In this work, a CIC interpolation filter with an order of 4 is adapted from [16]. First, there are 4 comb stages followed by an output register, all operating with CLK\_SLOW. Then, this output is up-converted to CLK\_FAST by adding zeros between samples. The zero-stuffed data is then fed into 4 stages of integrators to filter it and produce the final transfer function of this 4<sup>th</sup>-order CIC filter. As long as CLK\_SLOW is a divided version of CLK\_FAST with an integer division ratio, the CIC filter can be used for upsampling without any need to apply USR configurations to it.

The USR of this CIC upsampler is considered to be in the range of 2 to 10, which results in a range of possible values for bit growth. According to (4.12), by replacing  $N = 4$  and  $M = 1$ , the bit growth would be ranging from 4 up to 14 bits. This means that with a 12-bit data stream, the position of MSB after upsampling can be from the 16<sup>th</sup> bit to the 26<sup>th</sup> bit. The resulting 26-bit register should be truncated to 12 bits by using 12

more-significant bits. A gain configuration decides how many bits to shift it to the left before truncation. As a result, the output register is multiplied by  $2^{gain}$ .

However, this method of magnification cannot guarantee the highest possible maximum output power. The analog frontend is able to output a maximum power corresponding to  $2^{11} - 1$ , which is the maximum of a 12-bit signed data. With such a shifting magnification, the maximum truncated value might have any value from  $2^{10}$  to  $2^{11} - 1$ . The worst case scenario occurs when it is  $2^{10}$ . In this case, the maximum magnitude of the digital word would be as low as almost half of the magnitude, which results in the maximum power the frontend is designed to be able to deliver. This can be interpreted as a peak output power degradation:

$$P_{deg} = \left( \frac{2^{10}}{2^{11} - 1} \right)^2 \approx \frac{1}{4} = -6 \text{ dB} . \quad (4.13)$$

As a solution, a fractional boost stage is added before applying gain and truncation in order to perform a fractional amplification between 1 and 2. This stage multiplies the data by  $1 + \frac{boost}{2^3}$ , where boost is a 3-bit configuration register ranging from 0 to 7. With the boost stage, the worst case of power degradation can be compensated with a factor of 1.875:

$$P_{deg} = \left( 1.875 \cdot \frac{2^{10}}{2^{11} - 1} \right)^2 \approx (0.938)^2 = -0.56 \text{ dB} . \quad (4.14)$$

As it is clocked with CLK\_FAST, it should be taken into account that implementation of such a 3-bit multiplier must be fast enough to guarantee no timing violations. With this regard, it is implemented through a 2-stage pipelined multiplier.

## 4.3 Compensation of Imperfections

In practice, there are many undesired effects in the design of an RF frontend, which can impact and degrade the performance of a digital-centric transmitter. This section goes through a few of the performance degradation sources resulting from an imperfect frontend and reviews the techniques integrated in the transmitters of this work to deal with these issues.

### 4.3.1 LO Feedthrough

As mentioned earlier, LO feedthrough is one of the undesired effects a transmitter can suffer from. Each communication standard defines a criteria for an allowed amount of LO feedthrough in dBc unit. When the output spectrum is mixed down and demodulated at the receiver side or at measurement devices, LO feedthrough shows itself as a spike at DC. In the constellation diagram, it appears as a DC offset in both directions of I and Q, as

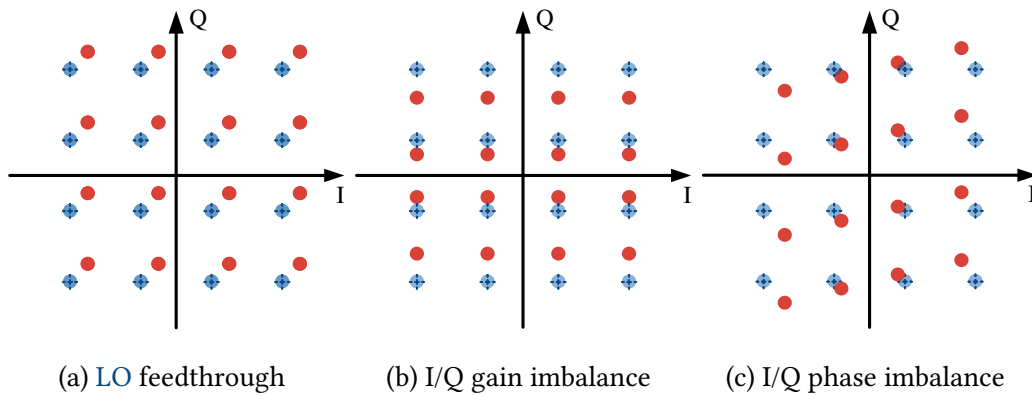


Figure 4.8: Effects of LO feedthrough and I/Q gain and phase imbalances on a 16-QAM constellation diagram.

illustrated in Fig. 4.8a for a 16-QAM constellation. This implies that it can be compensated by applying an opposite offset to each of I and Q data. Such a correction technique is implemented by [16] in the digital domain through an adder in each path of I or Q, similar to the way it is done in the analog domain in [88]. Two configuration registers,  $d_I$  and  $d_Q$ , are assigned for this purpose in the register file. However, it should be taken into consideration that this method does not account for dynamic LO feedthrough.

### 4.3.2 I/Q Gain and Phase Mismatch

I/Q imbalance plays an important role in degrading the performance of the transmitter besides LO feedthrough. I/Q gain imbalance is a common imperfection in quadrature transmitters due to the mismatch in I and Q paths. In lower-complexity modulation schemes like QPSK, a slight gain imbalance can be ignored as it does not result in an incorrect bit decision in most of the cases. However, with lower signal levels or in higher modulation schemes like 16-QAM or 64-QAM where neighboring constellation points result in very close power levels, an I/Q gain mismatch leads to a high EVM and even incorrect symbol detections due to increased density of constellation points. This can be seen in Fig. 4.8b, where the I axis has a positive phase offset towards the Q axis.

I/Q phase error can cause even more severe performance degradation than that of gain error. It can occur when the phase difference of LO signals for I and Q is different from  $90^\circ$  due to unequal path delays. Furthermore, a delay mismatch in the path of output currents of each of the I and Q RF-DACs can add up to this imperfection. It causes a trapezoid shape in the constellation diagram as shown in Fig. 4.8c.

In summary, LO feedthrough and I/Q gain and phase mismatches transform the output coordinate vectors of the transmitter as illustrated in Fig. 4.9. This can lead to a degraded

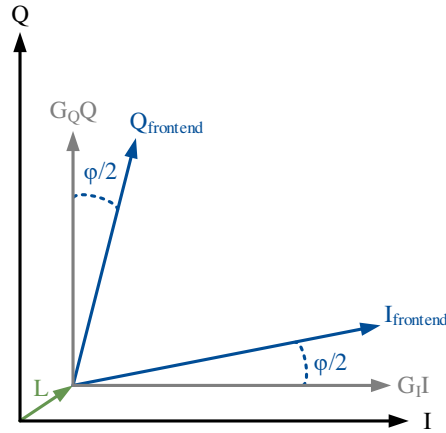


Figure 4.9: Effects of LO feedthrough and I/Q imbalances on the transmitter output vectors.

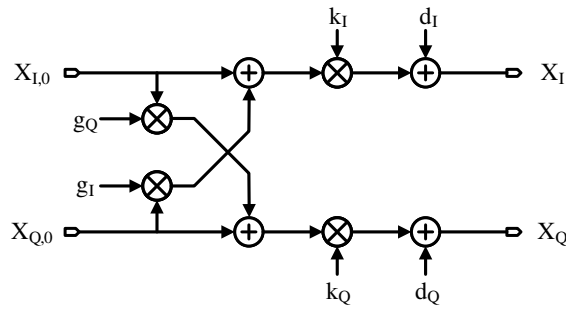


Figure 4.10: Block diagram of DET [16].

performance of an I/Q transmitter by increasing its EVM and symbol error rate. In order to compensate the effect of these imperfections, a digital module called **Digital-Enhanced Transmitter (DET)** is added to the design [16]. The output vector of the transmitter with regard to these imperfections can be expressed as in (4.15):

$$V_{out}(t) = e^{-j2\pi f_{LO}t} \cdot [(X_I(t) \cdot G_I + L_I) \cdot e^{j\frac{\varphi}{2}} + j \cdot (X_Q(t) \cdot G_Q + L_Q) \cdot e^{-j\frac{\varphi}{2}}], \quad (4.15)$$

where  $X = X_I + j \cdot X_Q$  is the input signal of the **RF-DAC**,  $L = L_I + j \cdot L_Q$  is the constellation offset due to **LO** feedthrough,  $G_I$  and  $G_Q$  are gains of each of the paths, and  $\varphi$  is the phase error from  $90^\circ$ .

Correction of gain error can be done by decreasing the gain of one of the paths in order to equalize the path gains and eliminate the mismatch. Phase error correction can be done by adding a fraction of one path to the other path and vice versa. The block diagram of the **DET** circuitry with which the mentioned imperfections are compensated is presented in Fig. 4.10 [16]. The output of this block can be written as:

$$X_I = d_I + k_I \cdot (X_{I,0} - g_I \cdot X_{Q,0}), \quad (4.16)$$

and

$$X_Q = d_Q + k_Q \cdot (X_{Q,0} - g_Q \cdot X_{I,0}). \quad (4.17)$$

The parameters of this correction scheme can be listed as:

$$\begin{aligned} d_I &= -\frac{L_I}{G_I}, & d_Q &= -\frac{L_Q}{G_Q}, \\ k_I &= \frac{1}{G_I} \cdot \frac{\cos(\frac{\varphi}{2})}{\cos(\varphi)}, & k_Q &= \frac{1}{G_Q} \cdot \frac{\cos(\frac{\varphi}{2})}{\cos(\varphi)}, \\ g_I &= g_Q = \tan(\frac{\varphi}{2}). \end{aligned} \quad (4.18)$$

The values of these parameters required to compensate imperfections cannot be calculated directly but are estimated by measurement during a calibration phase through a monotonic power meter. Such a measurement is performed in several steps. First, for calibrating the offset due to the LO leakage, a zero input data is applied to both I and Q and the power of the output spectrum at the LO frequency, which is the LO feedthrough, is monitored. To minimize it, first,  $d_I$  is swept and then, while  $d_I$  is set,  $d_Q$  is adjusted. Depending on the resolution of the RF-DAC, this procedure can be repeated few times until it converges to the most suppressed achievable LO feedthrough.

In the next phase, either of gain mismatch or phase error should be corrected. For this purpose, the transmitter is tested with a digital amplitude of  $A$  at different phases. The value of  $A$  should be large enough to allow for a sufficient precision while it should not be so large that it incorporates AM-AM and AM-PM non-linearities due to the finite output impedance of RF-DAC unitcells. It is recommended to begin with gain error by applying  $A$  and  $A \cdot j$  as inputs, which correspond to the I axis and Q axis, respectively. In this way, the gain of the axis with higher output can be reduced by adjusting  $k_I$  or  $k_Q$ .

In order to correct the phase error, inputs of  $A(1 + j)$  and  $A(1 - j)$ , which correspond to  $45^\circ$  and  $-45^\circ$ , are applied. If the output power at  $45^\circ$  is larger than that of  $-45^\circ$ , the phase error,  $\varphi$ , is positive. In this case,  $g_I$  is adjusted to minimize the difference between output power at  $45^\circ$  and  $-45^\circ$ . In case  $\varphi$  is detected to be negative,  $g_Q$  should be adjusted to correct the phase error.

The effects of LO feedthrough and I/Q mismatch can be visible with a Single-Side Band (SSB) input signal as well. When a sine signal and a cosine signal are given as inputs for I and Q, respectively, the image component should not exist in the output spectrum of the RF-DAC in the ideal case. However, due to the limited resolution of the frontend, the Image-Rejection Ratio (IRR) is limited. Furthermore, I/Q gain and phase errors reduce the IRR as the undesired sideband would grow with the imbalance of the two paths. Therefore, IRR can be considered as the measure to minimize the mismatch between I and Q paths of the transmitter. Clearly, LO feedthrough, which includes both

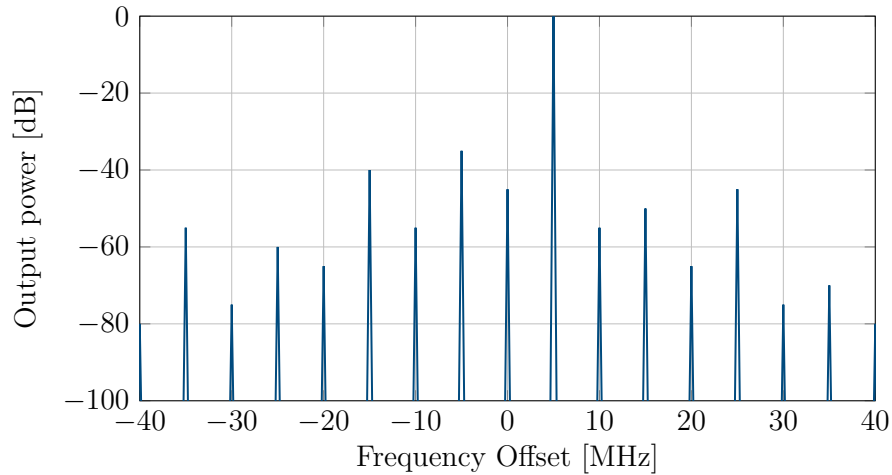


Figure 4.11: Effects of imperfections on SSB output spectrum.

dynamic and static components, is also measurable with an SSB input. Fig. 4.11 shows an example of the output power spectrum through a 5 MHz SSB test where spurs at different offset frequencies relative to  $f_{LO}$  can be seen. The signal spurs can be divided into two categories. The first one includes those at offset frequencies of 0,  $\pm 10$ ,  $\pm 20$ ,  $\pm 30$ , and  $\pm 40$ , which correspond to the effects of LO feedthrough. The spur at  $f_{LO}$  is the highest spur of this category as it includes both static and dynamic LO feedthrough while the rest are only due to dynamic LO feedthrough. Shifting the origin of the IQ coordinate by adding offsets to I and Q input signals cancels the static feedthrough and reduces the power of this spur. The spurs of the second category correspond to mixing products of harmonics of the 5 MHz input signal with the LO. These spurs occur due to the nonlinearity of the transmitter. The effect of I/Q imbalances contributes mostly to the image signal at a frequency offset of  $-5$  MHz. As a result, in order to compensate IQ gain and phase mismatches, one can observe this spur and reduce it through DET in a number of recursive steps as explained above. Although it makes the process of compensating nonidealities more complicated, SSB test provides a better precision as the input signal includes a range of different discrete points rather than only two points used in the simpler calibration technique.

### 4.3.3 Predistortion

An RF-DAC frontend or, more distinctively, a DPA would show a high amount of nonlinearity due to the limited output impedance of each unitcell when turned on. An example of a DPA profile with such a compressing nonlinearity is shown in Fig. 4.12. Since turning on more cells reduces the effective output impedance, the output power magnitude does not increase linearly and it results in an AM-AM nonlinearity. The impedance change

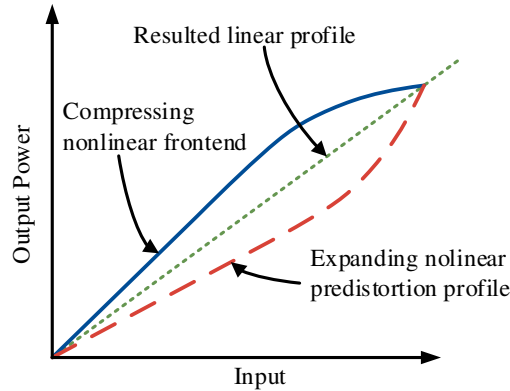


Figure 4.12: Examples of nonlinearity profiles of an RF-DAC and a DPD.

affects not only the magnitude but also the phase. The reason is that with more cells turned on, the capacitive load increases, which causes more delays. This translates into AM-PM nonlinearity in which the output phase does not remain constant by increasing the amplitude with a constant input phase. Consequently, it can be seen that the output amplitude and phase are functions of both I and Q inputs.

A Digital PreDistortion (DPD) block implements a reverse function of the nonlinearity of the RF-DAC frontend. In other words, it distorts the input by adding an expanding nonlinearity complementary to the compressing nonlinearity of the frontend so that they become linear when cascaded [89]. Such an expanding nonlinearity as the reverse function is illustrated in Fig. 4.12. The DPD is implemented through a Look-Up Table (LUT). Each input point specifies an address in this LUT where the corresponding output of the DPD is stored.

In conventional designs, 1-dimensional DPDs were implemented, which ignore the interaction between I and Q values on the output of RF-DAC [90]. The amplitude and the phase of output are functions of both I and Q inputs and, therefore, cannot be characterized independently. A better solution would be to implement a 2-dimensional DPD in which each complex input points to an element of the LUT with a specific complex output in the constellation diagram [56]. However, such a DPD requires a large LUT, which occupies a huge die area. For instance, for a 12-bit I/Q RF-DAC,  $N = 2^{12} \times 2^{12} = 2^{24}$  LUT cells with a word width of at least 24 bits for each cell are required, which is obviously not reasonable to be implemented on a transmitter die. Instead, it is reduced to  $N = 2^6 \times 2^6 = 2^{12}$ . In this case, for the points which are not available in the LUT a linear interpolation is performed. In other words, the LUT specifies square tiles in the constellation diagram, each with a particular gain and phase change.

For the purpose of creating such a DPD, a learning process should be employed in order to estimate the reverse nonlinearity function. The nonlinearity profile of the RF-DAC should be characterized. The estimation can be done through either of direct or indirect

structures [91]. In direct estimation, the **DPD** is implemented through a feedback loop that modifies elements of the **DPD LUT** directly during the operation of the transmitter. In indirect estimation, the **DPD** should perform an estimation process prior to the operation of the transmitter in order to build up the **LUT**.

Implementation of a complete chain of **DPD** on-chip, which requires a dedicated power meter as well as an estimator and an adaptive filter to build up the **LUT**, would require a high implementation effort along with a bigger die area. Instead, in this work, only the **LUT** and the interpolation function are adapted from [16] and implemented. The process of estimation and building up **LUT** elements can be performed with an indirect estimation in a loop through an off-chip power meter and an **FPGA**.

## 4.4 Element Selection Logic

The **Element Selection Logic (ESL)** has the responsibility to drive the control signals of the frontend. According to its input data, a number of current cells of the **RF-DAC** should be activated to generate a corresponding output current with **LO** frequency. The implementation of **ESL** is the same for each of I and Q data. In the first place, the magnitude of the input data is segmented into two parts for driving the binary-weighted **LSB DAC** and the unary-weighted **MSB DAC**. For the unary-weighted **DAC**, a further conversion to thermometer-coded data is required. In the first transmitter of this work, called **PalleonTX**, a 7-bit unary-weighted **MSB DAC** is implemented, which consists of 16 columns each with 8 **MSB** unitcells. Therefore, out of 7 bits of input data considered for this **DAC**, bits 0 to 2 are converted to thermometer-coded to control the rows and bits 3 to 6 are processed to control the columns.

The unary-weighted implementation of the **MSB DAC** relieves the degrading effects of mismatch to some extent but not completely. Accurate symmetric layout and proper use of dummy elements help to eliminate the systematic mismatch effects. However, random local variations, which cause a mismatch of transistors in different current cells, lead to a degraded linearity of the **RF-DAC** as in every other **DAC**. In order to further reduce this nonlinearity, a digital mismatch shaping algorithm can be merged into the implementation of **ESL** [92]. Such an algorithm randomizes the selection of the cells in each **CLK\_FAST** cycle so that the mismatch errors are averaged out in a busy signal with a lot of different signal levels. **Data-Weighted Averaging (DWA)** [93] and **tree-shaper** [94] are the most commonly used mismatch-shaping methods in the literature [95]. Due to its lower complexity of implementation in the high frequency clock domain, **DWA** is employed in this work.

In parallel to the unary-weighted data, the sign bit and the binary-weighted data are delayed to match the delay of other signals before being fed to the frontend. Clearly,

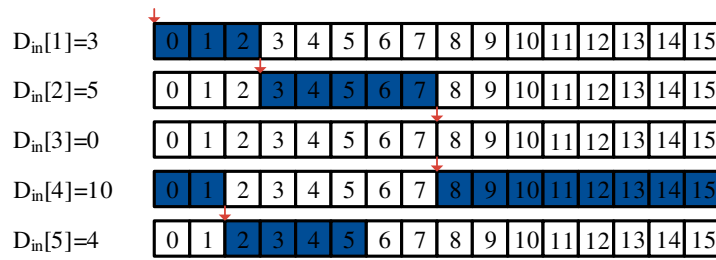


Figure 4.13: Illustration of DWA.

since the complexity of such operations is sufficiently low, there would be a less chance of timing problems when performing it with a high clock frequency of CLK\_FAST.

#### 4.4.1 Data Weighted Averaging

The DWA algorithm performs a first-order mismatch shaping to reduce the dynamic effect of mismatch errors in a unary-weighted DAC [93]. In this algorithm, with each new data cycle, the activated DAC cells are selected beginning from where selected cells ended in the previous data cycle.

Fig. 4.13 illustrates DWA for selecting cells in a 16-cell unary-weighted DAC. The input samples are consecutively “3”, “5”, “0”, “10”, and “4”. In this case, with the first input sample of 3, cells {0, 1, 2} are selected as the selection pointer points to cell 0 as the starting point. In the next data cycle, the selection pointer would be 3, which results in selecting cells {3, 4, 5, 6, 7} for an input sample of 5. An input of 0 would not change the selection pointer. Furthermore, the summation of the selection pointer with the input sample would be done in a modulo-16 way by going back to cell 0 after selecting cell 15. This can be seen for the fourth input sample, which is 10.

In this way, DWA is used for mismatch shaping of the quantization noise with the first-order noise transfer function of:

$$H_{N-DWA} = 1 - z^{-1}. \quad (4.19)$$

Due to the structure of columns and rows in the unary-weighted DAC of PalleonTX, in which only one column can have less than 8 cells activated, the use of the DWA structure is limited to the selection of the starting column out of 16 instead of the selection of a starting cell out of 128.

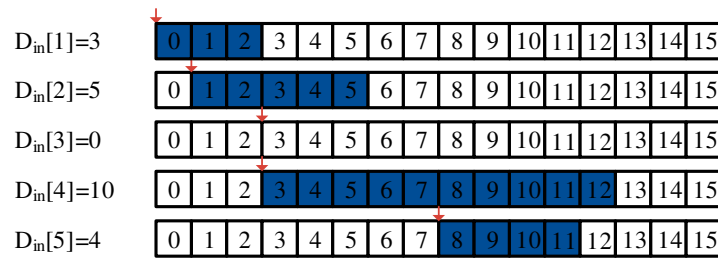


Figure 4.14: An example of RA-DWA algorithm with  $radwa\_fptr = 0.5$ .

## Reduced-Activity Data Weighted Averaging

A problem with the plain DWA algorithm is the increased switching activity [96]. This can lead to an increase in glitches and spikes as many of current cells are turned off and new ones are turned on in most of the cases. Ideally, the timing of turning on or turning off of a current cell should be synchronized with LO so that no glitch occurs with a new data sample. However, due to physical limitations which prevent a 100% symmetrical layout, this cannot be achieved perfectly. Also, non-ideal dynamics of current cells add up to the problem. Therefore, having fewer changes in activated current cells would be beneficial to reduce such spikes.

The Reduced-Activity Data-Weighted Averaging (RA-DWA) algorithm proposed in [97] provides the possibility to still benefit from the advantages of DWA while the number of cell switchings are reduced. In this algorithm, which is illustrated in Fig. 4.14 for a pointer factor of 0.5, instead of the data sample itself, a fraction of it is added to the pointer position to result in a new pointer position for the next sample. This means with a new sample, a number of cells used for the previous sample are still employed. In PalleonTX, a 5-bit signed register called  $radwa\_fptr$  specifies the fraction factor. In case a negative fraction is specified, the selection direction is reversed as in [98].

It is important to mention that in case an LUT DPD is used, applying DWA might be unnecessary and even unfavorable. In the presence of mismatch between unitcells, the learning sequence of the DPD depends on the exact cells that are turned on during the estimation of LUT elements. Therefore, alternating the turned-on cells might result in different output signals compared to those the DPD was calibrated with. Furthermore, having a calibrated DPD LUT can itself account for handling mismatches as existed during the estimation phase as well.

# Chapter 5

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## 12-bit I/Q Digital-Centric Transmitter with 25 % Duty-Cycle

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This chapter describes the implementation and measurement results of a digital-centric transmitter, called *PalleonTX*, which is fabricated in a 65-nm technology. The transmitter is based on the UMIC-TX3 transmitter presented by [16]. The digital blocks of the transmitter are described in detail in Chapter 4.

This chapter is organized in four different sections. In the first section, the system architecture of the transmitter is introduced and its clock frequency schemes corresponding to different communication standards are presented. In section 5.2, the circuit implementation of the main building blocks of the transmitter, including the *DPA* frontend and the clock dividers, are described and their practical implementation aspects, such as layouts, are reviewed. Section 5.3 presents the results of different measurements and validation tests performed on this transmitter and compares the results to the state-of-the-art transmitter systems in the literature.

### 5.1 System Architecture

The system block diagram of *PalleonTX* is presented in Fig. 5.1. As it can be seen, the data is first received through a high-speed data interface called *CAG/IOv2*. This interface consists of four lanes to communicate with an *FPGA*. These include one lane for receiving in-phase data, one lane for receiving quadrature data, one lane for receiving a synchronizing clock, and one lane for transmitting any required data back from the *ASIC* to the *FPGA*. The digital part of the interface has the responsibility of deserializing and decoding the receiving data as well as encoding and serializing the data to be sent back to the *FPGA*. In the first step after startup and taking the reset signal, the interface establishes a link to the *FPGA* by adjusting delays and making sure that data is transferred with a low error rate through the interface. Then, the input data can be used for either of register bank configuration or input baseband data. Further details about the implementation of this interface can be found in section 4.1.1

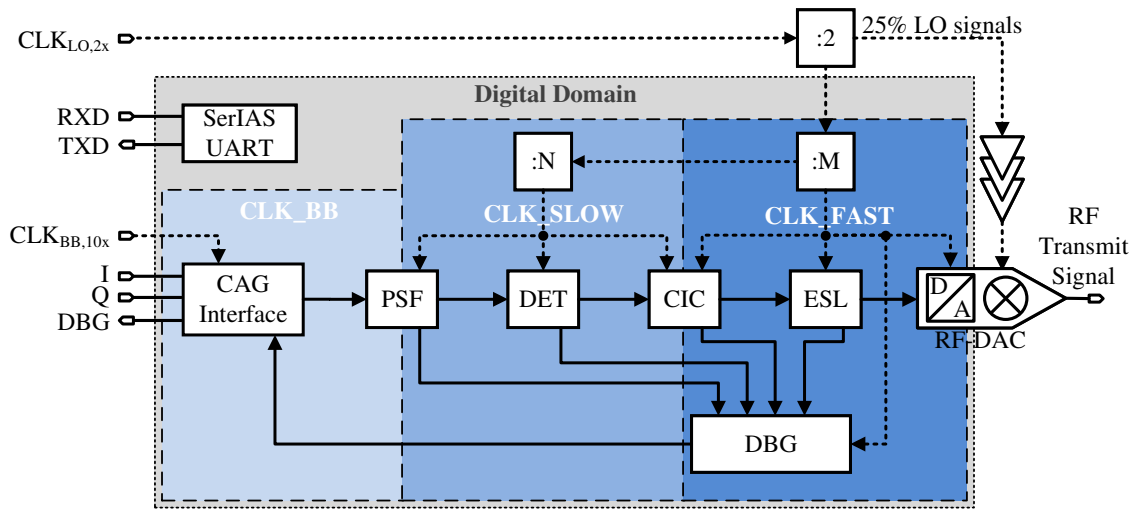


Figure 5.1: Block diagram of the PalleonTX transmitter system architectures.

As the next step after receiving the data through the interface, it must be processed within the digital part before being fed to the frontend. The first DSP block is the **Pulse-Shaping Filter (PSF)**. It performs a clock domain crossing as well as an upsampling with a fractional ratio from the baseband clock,  $CLK_{BB}$ , which is received by the interface, to the slow clock, called  $CLK_{SLOW}$ , which is a divided version of the LO. The ratio of upsampling through the PSF can be any fractional value between 4 and 5. This ratio is determined depending on the communication standard in which the transmitter is configured to operate. When the data is sampled with  $CLK_{SLOW}$ , signal processing steps can be applied. These include compensation of imperfections such as LO feedthrough and I/Q gain and phase mismatch as well as predistortion through a look-up table to compensate the AM/AM and AM/PM nonlinearities of the frontend as discussed in section 4.3. All these signal processing steps are performed in the DET block shown in Fig. 4.10.

In the next stage, the processed data is upsampled for a second time. This integer-ratio upsampling from the slow clock to the fast clock,  $CLK_{FAST}$ , is performed through a CIC filter. Since the frequency of  $CLK_{FAST}$  would be in the range of 500MHz to 800MHz, no significant signal processing steps can be performed in one clock cycle of this clock frequency. That is why it is preferred to perform most of the DSP steps in the lower frequency of  $CLK_{SLOW}$ . The only digital module of the signal path that operates in the fast clock domain is the ESL, which determines the signals that control the output power of the frontend. Furthermore, a Debug module is considered to provide the possibility of monitoring the performance of different digital modules discussed here. In case activated, it samples the data coming from the module selected to be monitored with  $CLK_{FAST}$  and transfers this data to the buffer of the serializer provided in the high-speed interface.

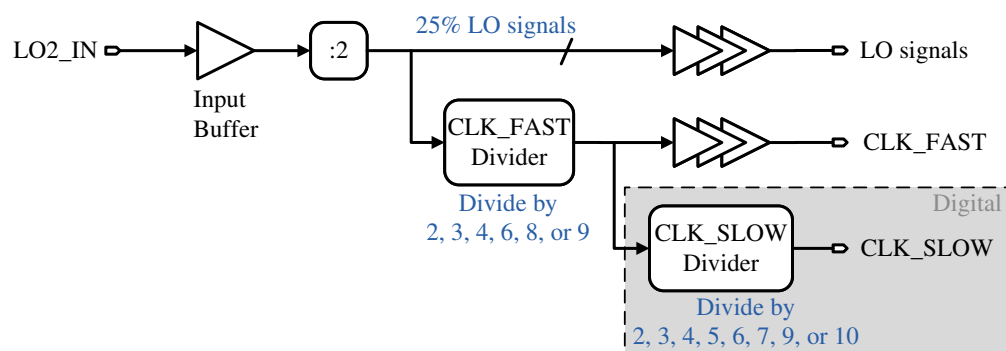


Figure 5.2: Clock distribution network of the transmitter.

Outside the digital part, the control signals are fed to the frontend to turn on a number of unitcells according to the upsampled data. As mentioned earlier, the frontend consists of a number of current cells, which draw current when both of the control signal and the corresponding LO signal are high. As a result, the frontend performs both D/A conversion and mixing of the upsampled data with the LO frequency.

Finally, as the last part to mention in this architecture, all the required clock signals are provided through an external Local Oscillator with a frequency of two times the carrier frequency required by the standard in which the transmitter is operating. A block diagram of the clock distribution of the RFIC is presented in Fig. 5.2. This differential clock with a frequency of  $2 \times f_{LO}$  is fed to an LO divider, which divides it by two and creates 4 different required phases of the LO clock, each with a duty cycle of 25 %. Then, these clocks are further divided by a specific integer factor according to the standard to result in CLK\_FAST, which is fed to the digital part of the chip. Similarly, CLK\_SLOW is generated through dividing CLK\_FAST by an integer ratio.

Table 5.1 presents the clocking scheme and division ratios used for different standards with different channel bandwidths. It needs to be taken into consideration that the frequency of CLK\_FAST needs to be high enough to sufficiently suppress the sampling aliases while not too high so that the digital modules can operate error-free and without timing violations.

## 5.2 Circuit Implementation

In order to achieve the expected performance out of the described transmitter system, special care has to be taken in circuit design and implementation. The provided 65-nm technology offers a robust high-speed performance for the digital circuitry that can operate at frequencies up to 1 GHz. However, the most challenging part of the implementation of the transmitter is its RF frontend and the clock distribution circuitry,

Table 5.1: Selection of clocking schemes.

Band	$f_{BB}$ [MHz]	$f_{LO}$ [MHz]	$f_{fast}$ [MHz]	CIC ratio	$f_{slow}$ [MHz]	PSF ratio
WLAN b/g/n/ax ch. 1 (I)	20.00	2412	804.00	10	80.40	4.02
WLAN b/g/n/ax ch. 1 (II)	20.00	2412	603.00	7	86.14	4.31
WLAN b/g/n/ax ch. 14 (I)	20.00	2484	828.00	10	82.80	4.14
WLAN b/g/n/ax ch. 14 (II)	20.00	2484	621.00	7	88.71	4.44
WLAN n 40MHz ch. 3	40.00	2422	807.33	5	161.46	4.04
WLAN n/ac ch. 36	20.00	5180	647.50	7	92.50	4.63
WLAN ac ch. 165	20.00	5825	728.13	9	80.90	4.63
WLAN ac 80MHz ch. 42	80.00	5210	651.25	2	325.63	4.07
WLAN ac 80MHz ch. 155	80.00	5775	721.88	2	360.94	4.51
3GPP Bd. 1, low	30.72	1920	640.00	5	128.00	4.17
3GPP Bd. 1, high	30.72	1980	660.00	5	132.00	4.30
3GPP Bd. 7, low	30.72	2500	625.00	5	125.00	4.07
3GPP Bd. 7, high	30.72	2570	642.50	5	128.50	4.18
3GPP Bd. 8, low	30.72	880	440.00	3	146.67	4.77
3GPP Bd. 8, high	30.72	915	457.50	3	152.50	4.96
Bluetooth (low)	24.00	2400	600.00	6	100.00	4.17
Bluetooth (high)	24.00	2484	621.00	6	103.50	4.31

which affect the transmitter's performance significantly. In the following sections, the design and implementation of critical analog/RF blocks of the transmitter are reviewed.

## 5.2.1 High-Speed Differential LO Clock Generation and Distribution

Since there is no [Phase-Locked Loop \(PLL\)](#) included in this design, an external differential clock signal from a [Local Oscillator](#) source with a frequency twice the carrier frequency is provided to the chip in order to generate all the required clock signals of the transmitter. For this purpose, several clock dividers and a number of buffers are implemented throughout the clock distribution network, which is shown in [Fig. 5.2](#).

### 5.2.1.1 Input LO buffer

In the first stage, a self-biasing Pseudo-differential LO buffer amplifies the signal received through the bare pads of the chip. The schematic of this buffer is presented in [Fig. 5.3](#) [53]. An AC-coupling capacitor allows for an external LO signal with no DC offset. A

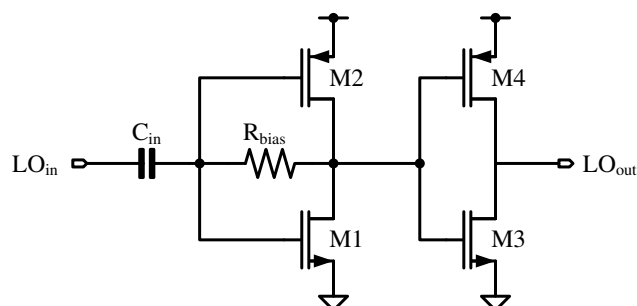


Figure 5.3: Input self-biasing pseudo-differential LO buffer.

self-biasing resistor guarantees that the input signal is biased at around half the  $V_{DD}$  as it would be a low-pass-filtered version of the first inverter's output. This is then followed by another inverter to shape a clean square waveform as the input of the LO divider.

### 5.2.1.2 Generation of LO Signals With a 25 % Duty Cycle

The buffered input clock signal is applied to a clock divider that divides the input clock frequency by 2 and generates four different phases of the carrier frequency,  $f_{LO}$ , each with a duty cycle of 25 %. For this purpose, a Razavi divider with the schematic shown in Fig. 5.4 is implemented [99]. It includes a leader latch and a follower latch in a negative feedback loop. Each latch consists of two sense devices ( $M_1$ ,  $M_2$ ,  $M_7$ , and  $M_8$ ), a regenerative positive feedback loop ( $M_3$ ,  $M_4$ ,  $M_9$ , and  $M_{10}$ ), and two pull-up transistors ( $M_5$ ,  $M_6$ ,  $M_{11}$ , and  $M_{12}$ ). Since the clock divider is sensitive to capacitive load, the same chain of CMOS buffers is inserted at each output. Furthermore, the layout, which is shown in Fig. 5.5, is done as symmetrically as possible so that no systematic offset is introduced to the LO divider. Since a Deep N-Well (DNW) is used, the NMOS devices are placed in the middle inside a P-well and the PMOS devices are placed in the N-well connected to the DNW.

An advantage of this divider is that it directly generates 25%-duty-cycle clock signals and does not require additional circuitry or higher LO frequencies such as the one employed in [12], which may increase the power consumption. By using wider transistors, at the expense of more power consumption, the operating frequency can be increased and the divider phase noise can be reduced. However, due to a flow of static current during the high clock phase of these latches, it consumes an excessive power consumption, which can be optimized by a proper sizing of the devices. In other words, the trade-off between a better phase-noise performance and a lower power consumption should be taken into account in sizing of the transistors.

Depending on the communication standard, the LO frequency of the transmitter can be as high as 2.5 GHz and therefore, the divider should work properly with an input

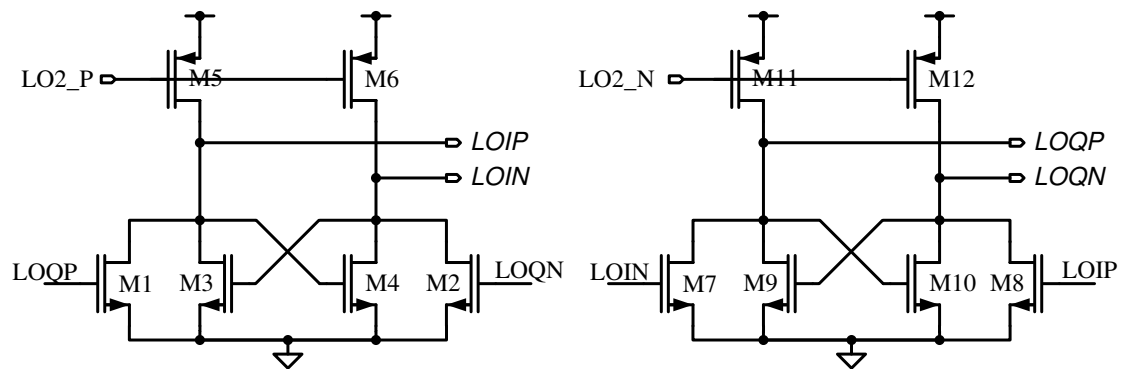


Figure 5.4: Schematic of the 25 % LO divider.

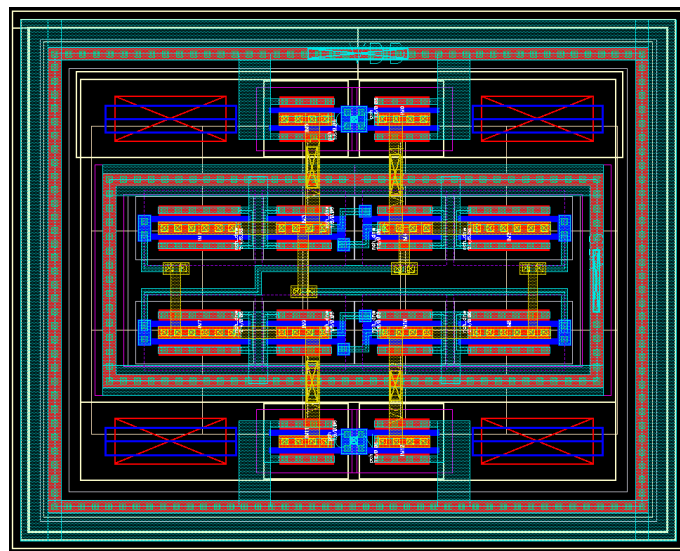


Figure 5.5: Layout of the 25 % LO divider.

frequency of up to 5 GHz under all possible process, voltage, and temperature conditions. Simulations show that the divider needs a very small input signal for injection locking. However, the phase noise would be increased if the input signal is small. The phase noise of the implemented divider is simulated with an extracted layout and the result is presented in Fig. 5.6. It can be seen that a phase noise of better than  $-151$  dBc/Hz is achieved at an offset of 10 MHz.

To name a disadvantage of the implemented LO divider, one can point out the high sensitivity of the duty cycle to mismatch. The problem arises from the fact that each of the LO phases does not reset to ground until the next LO phase goes high. For example, supposing LOIP is high, by the next phase of LO2, LOQP goes initially high, and then, this triggers LOIP to be discharged through M1. As a result, the LO phases will be overlap and the duty cycle of each phase is in practice more than 25 %. Furthermore, the duty

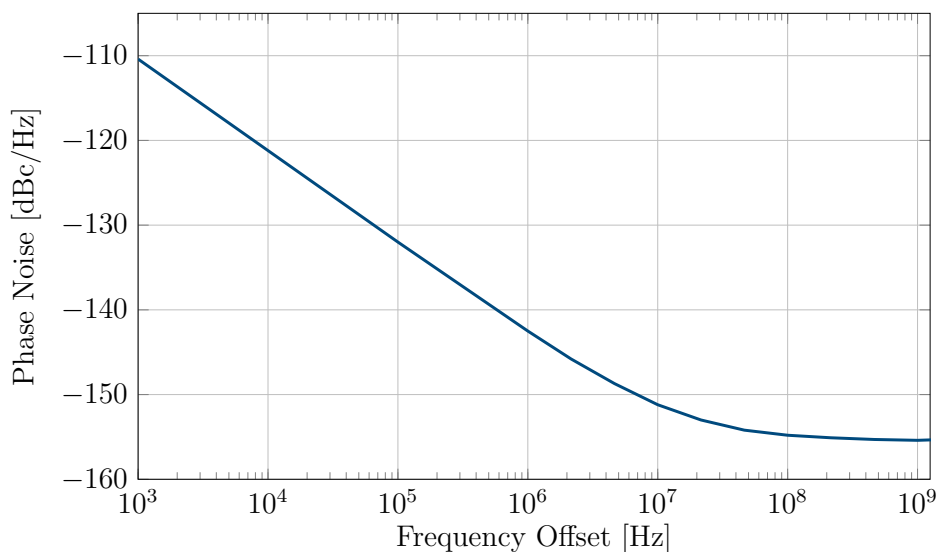


Figure 5.6: Phase noise of the LO divider.

cycle is highly susceptible to mismatch of the NMOS devices of the divider. Therefore, this can lead to a mismatch in the duty cycle of different phases, which deteriorates the precision of the transmitted signal by introducing I/Q gain and phase imbalances. In order to reduce this effect, wider devices with the cost of a higher power consumption can be used. However, since an I/Q mismatch compensation mechanism is implemented in the DET module of the digital part, such a requirement for a lower difference in the duty cycle of LO phases can be alleviated to some extent.

### 5.2.1.3 Generation of Digital Clocks

In order to synchronize the data stream and the carrier frequency as required, the clock of DSP parts as well as the frontend sampling clock should be derived from the LO clock. CLK\_FAST is the only clock input of the digital part in the LO clock domain and CLK\_SLOW is generated through a divider inside the digital part as stated earlier in Section 5.1. Furthermore, the signals controlling the RF-DAC cells are also sampled with CLK\_FAST so that they are synchronized with the LO clocks in all current cells. Therefore, a clock divider with an adjustable clock division ratio generates CLK\_FAST from LOIP after a sufficient number of buffers. As it can be seen in Fig. 5.2, the input buffer of this clock divider is added to paths of LOIN, LOQP, and LOQN so that they have the same load in the clock distribution network and the symmetry is maintained.

The block diagram of CLK\_FAST generator is presented in Fig. 5.7a. It consists of two cascaded dividers, each with a number of possible clock division ratios. The first divider, with the schematic presented in Fig. 5.7c, divides the input by a ratio of 2 or 3 while the

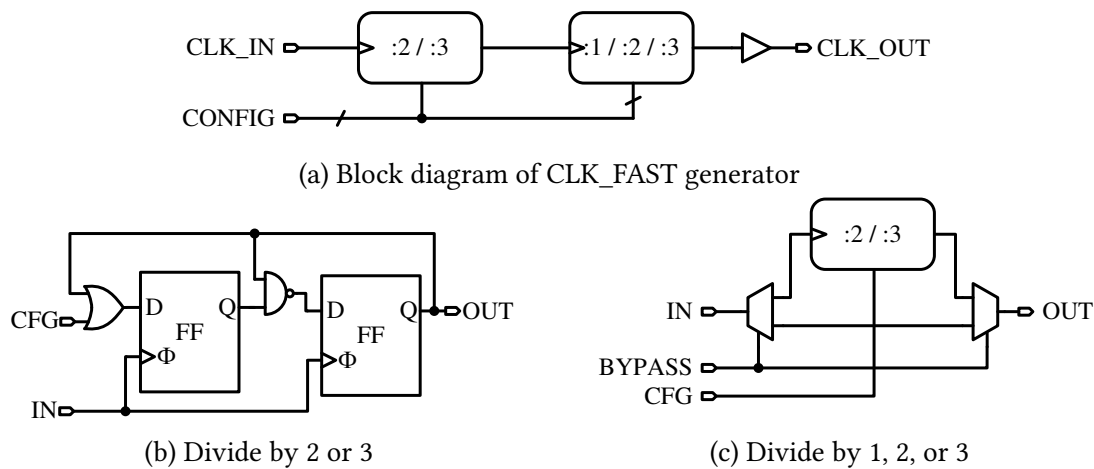


Figure 5.7: Programmable clock divider for generating CLK\_FAST.

second divider, depicted in Fig. 5.7b, can have a division ratio out of 1, 2, or 3. As a result, the overall division ratio, which is decided according to a 3-bit programmable register, can be set to 2, 3, 4, 6, or 9. As an illustration, for WLAN at the 2.4-GHz band, sampling frequencies in the range of 268 MHz to 1.242 GHz can be achieved. However, it should be noted that the implementation of the digital signal processing blocks in this technology limits the maximum sampling frequency to around 800 MHz. Therefore, reasonable division ratios for WLAN at the 2.4-GHz band can be 3 or 4 as listed in Table 5.1.

Another point to note about the CLK\_FAST generator is that in the case of a divide-by-9, the output cannot have a duty cycle of 50%. However, this does not affect the system as the digital signal processing blocks operating in the LO clock domain are not implemented with DDR mode and only use the rising edges of the clock signal.

True Single-Phase Clock (TSPC) latches are used to implement the dividers of Fig. 5.7. Fig. 5.8 shows the schematic of a TSPC latch which is used in this design [100]. This kind of dynamic latches can operate at higher frequencies with a lower power consumption compared to standard static latches as they do not incorporate a feedback loop. The lack of a positive feedback makes it necessary to refresh the stored data in the latch after a limited time in order not to lose them. This can be translated to a criterion of a minimum clock frequency when TSPC latches are used in a clock divider, which does not cause any problem for this work as the operating frequency is sufficiently high.

As mentioned earlier, CLK\_SLOW is generated from CLK\_FAST within the digital part. As it can be seen in Fig. 5.2 and table 5.1, division ratios of 2, 3, 4, 5, 6, 7, 9, and 10 should be provided for CLK\_SLOW. Therefore, in the first step, these division ratios are all generated and then, the output clock is selected through a multiplexer. This is depicted in Fig. 5.9.

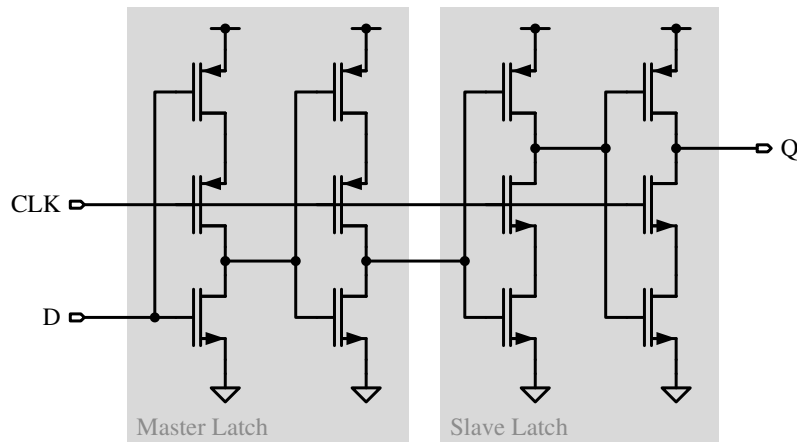


Figure 5.8: Schematic of a TSPC flip-flop used in the CLK\_FAST generator.

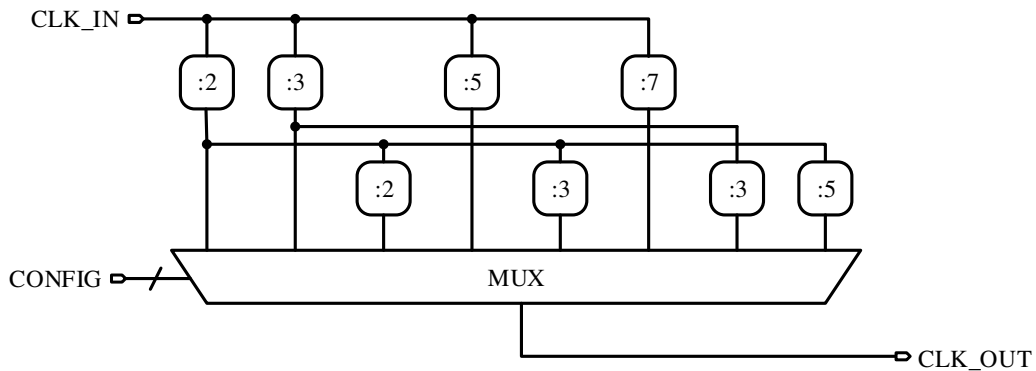


Figure 5.9: Block diagram of CLK\_SLOW generation.

## 5.2.2 Frontend Design

The DPA frontend consists of two similar DACs for each of the I and Q paths. Each DAC is implemented in a segmented way. A 4-bit DAC is designed for the LSB part with a binary-weighted switching scheme while for the MSB part, a 7-bit unary-weighted DAC with 128 MSB unitcells is implemented. Furthermore, the effect of the sign bit is implemented by switching the sequence of the LO phases.

### 5.2.2.1 Unitcells

In order to implement the current cells of the RF-DAC, a few kinds of unitcells have been considered. With a current switching cell like the one in Fig. 3.7c [16], the output impedance would be higher, which helps reduce AM-AM/AM-PM nonlinearities and it might eliminate the need for using a DPD. However, given an LO signal with a 25 % duty



cascode current branches as in [7]. However, with an AND gate prior to the current cascaded transistors, LO is one step further isolated from the output, which reduces the LO feedthrough. Furthermore, in this way,  $V_{DD,A}$  can be used more conveniently for analog power control.

With regard to noise perspectives, there are two different power domains in the implementation of each cell. The sampling of the data and its combination with LO are performed in the LO power domain with  $V_{DD,LO}$  and  $V_{SS,LO}$  as supply and ground voltages. This supply voltage is also used for LO buffers and other logics on the path of the data control signals of the RF-DAC frontend. Consequently, it incorporates switching noise with harmonics of LO and CLK\_FAST. That is why it should be separated from the analog power domain with  $V_{DD,A}$  and  $V_{SS,A}$  voltages, which directly affect output currents of unitcells.

The unitcell layout is implemented as symmetric as possible. The analog current parts are implemented in a DNW that isolates the bulk of the transistors from the noisy P-type substrate. The P-well is connected to  $V_{SS,A}$  while the middle N-well is biased with  $V_{DD,A}$ .

### 5.2.2.2 MSB DAC Structure

The 7-bit unary-weighted MSB DAC with 128 current cells is implemented in shape of 16 columns, each with 8 MSB unitcells. Fig. 5.11 shows the block diagram of each column. The activation of cells in a column is controlled through three signals called *col*, *full\_col*, and *row*. When *full\_col* is high, all MSB unitcells in the corresponding column are activated; otherwise, in case *col* is high for a column, *row* signals determine which cells of this column should be activated. Therefore, a simple decoder implementing a boolean logic of  $full\_col + col \cdot row$  is included in each cell to determine the data input. In this way, with each data sample, a number of columns are fully activated through *full\_col* signals and the *col* signal of another column is set to high so that a number out of the 8 cells in that column can be selected through *row* signals. In other words, out of the 7-bit input data of the MSB DAC, bits 0 to 2 correspond to *row* signals and bits 3 to 6 correspond to *ful\_col* signals.

Each column has a column driver block in addition to the current cells which provides the required LO signals. The schematic of the column driver is presented in Fig. 5.12. In the case of a negative data sign, the positive and negative LO signals are swapped instead of swapping the output current branch of the unitcells as in [16]. This task is performed in the column driver of each column. First, the sign signal is sampled with a version of CLK\_FAST, called CLK\_SIGN. Similar to the clock signal sampling the data in DPA current cells, CLK\_SIGN should sample sign bit during the time when both LOP and LON are low. The sampled version of the sign bit is used as the select bit of

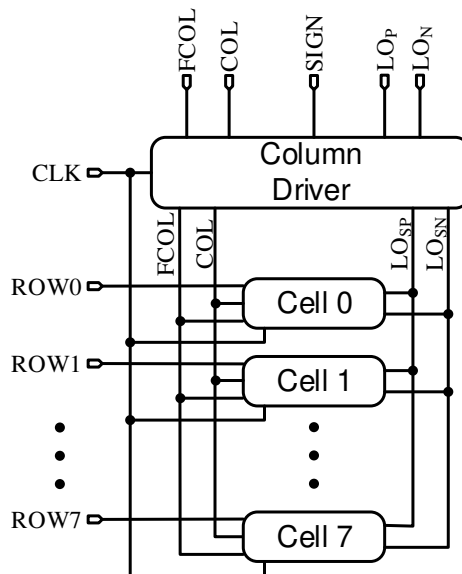


Figure 5.11: Block diagram of each column of the MSB DAC.

the multiplexer that swaps LO inputs through transmission gate switches as shown in Fig. 5.13.

The signed LO signals are then fed to a number of buffers, which can be deactivated in case none of the cells of the column are used. This helps to reduce the LO feedthrough as well as the average power consumption. For this purpose, an OR combination of *full\_col* and *col* is sampled through *CLK\_SIGN* and combined in a NAND gate. This is then followed by a simple CMOS buffer to reshape the LO signals and drive them through the column. These buffers should be sized properly so that the LO signals arriving at cells are sharp enough to eliminate unwanted effects of unsharp edges such as increased

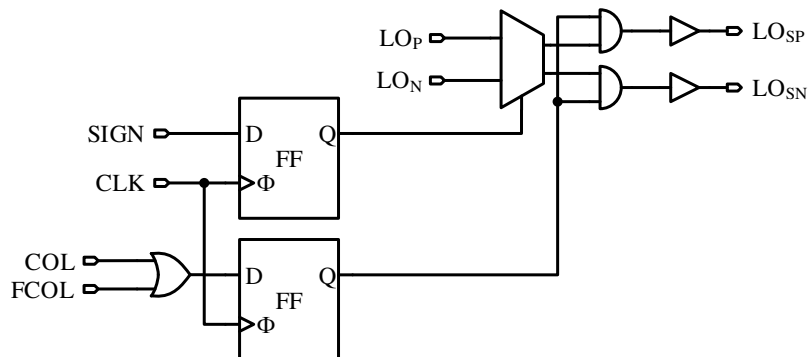


Figure 5.12: Schematic of the column driver in each of the columns of the MSB DAC.

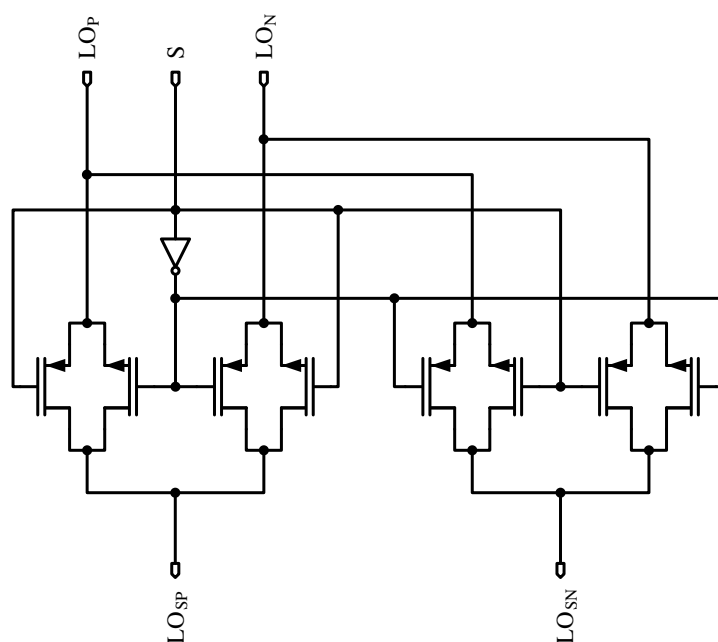


Figure 5.13: Schematic of LO multiplexer of the column driver.

phase noise and jitter. Moreover, with a strong buffer, the effects of mismatch in column drivers of different columns would be reduced. However, there is a trade-off between providing sharp signal edges and the power consumption of LO drivers, which should be taken into account as the LO distribution network corresponds to a significant part of the total power dissipation.

Clearly, multiplexing according to the sign bit and driving the cells in one column with the LO signals through the LO drivers creates a delay in the LO distribution. In each cell,  $CLK\_FAST\_I$  or  $CLK\_FAST\_Q$  should sample the data when the LO arriving at the cell is low while  $CLK\_SIGN\_I$  and  $CLK\_SIGN\_Q$  should be synched with the LO arriving at the column drivers. However, considering the delay of additional buffers driving  $CLK\_FAST\_I$  and  $CLK\_FAST\_Q$  from  $CLK\_SIGN\_I$  and  $CLK\_SIGN\_Q$ , it is cared that the delay added to LO signals in column drivers does not cause any problem in sampling the sign and column activation signals in column driver as well as sampling the data in each current cell.

### 5.2.2.3 LSB DAC Structure

The structure of the LSB DAC is much simpler as it consists of only 15 cells. The same circuit used as the column driver in the MSB DAC is used to provide the required LO signals for all LSB current cells. It should be mentioned that since the LSB cells provide

a current 16 times smaller than that of **MSB**, cells, the size of the **LSB** cells is much smaller, which dictates smaller buffers to reduce power consumption. Therefore, through simulations, it is decided that one column driver is enough for driving all 15 cells of this **DAC**. Besides, 4 latches are used to sample the 4-bit **LSB** binary data.

### 5.2.3 Layout Floorplan and Considerations

Implementation of the layout of an **RF-DAC** or a **DPA** is the most challenging part of its design. Since the timing of **LO** and sampling clock signals should be synchronized, the layout should be floorplanned in a symmetric way for distribution of these signals. Furthermore, the effect of mismatch should also be taken into account.

## 5.3 Measurement

PalleonTX is fabricated in a 65-nm low-power CMOS technology from **TSMC** with a core voltage of 1.2 V and an I/O voltage of 3.3 V. The technology allows the use of one layer of poly and 9 layers of copper metal with a metalization configuration of 9M\_6x2z plus 1 aluminum layer. Also, the triple-well feature of this technology is used to further isolate different voltage domains existing in this transmitter system, which is crucial in a mixed-signal IC with high-frequency signal paths.

This chip has a die size of  $1.875\text{mm} \times 1.875\text{mm}$ , which translates to an area of  $3.51\text{mm}^2$ . This is the minimum block size offered by the foundry. The die micrograph is presented in Fig. 5.14a. It can be seen that the die is not fully populated with integrated circuits and the whole transmitter circuit could be implemented in half of this size. The **DPA** frontend, which is the largest part of the chip, occupies an area of roughly  $0.55\text{mm}^2$  while the clock generation circuitry fills only  $0.21\text{mm}^2$ . The digital part occupies an area of  $0.415\text{mm}^2$  with a density of 69.1 %. And, as the smallest part, the analog part of the high-speed CAG/IO interface, which translates **CML** to **CMOS** signaling and vice versa, takes up an area of only  $0.027\text{mm}^2$ . The remaining area is filled with decoupling capacitors to provide more stable supply voltages with less noise.

The die is bonded to a **QFN-48** package with exposed pads, which provides a sufficient number of pins as shown in Fig. 5.14b. In order to decrease the parasitics in output paths, which can have a significant influence on the performance of the transmitter, it is desired that the output bond wires be as short as possible. That is why the die is not centered in the package and is displaced towards the output leads of the package.

In the following sections, validation measurement steps and their results are listed and discussed.

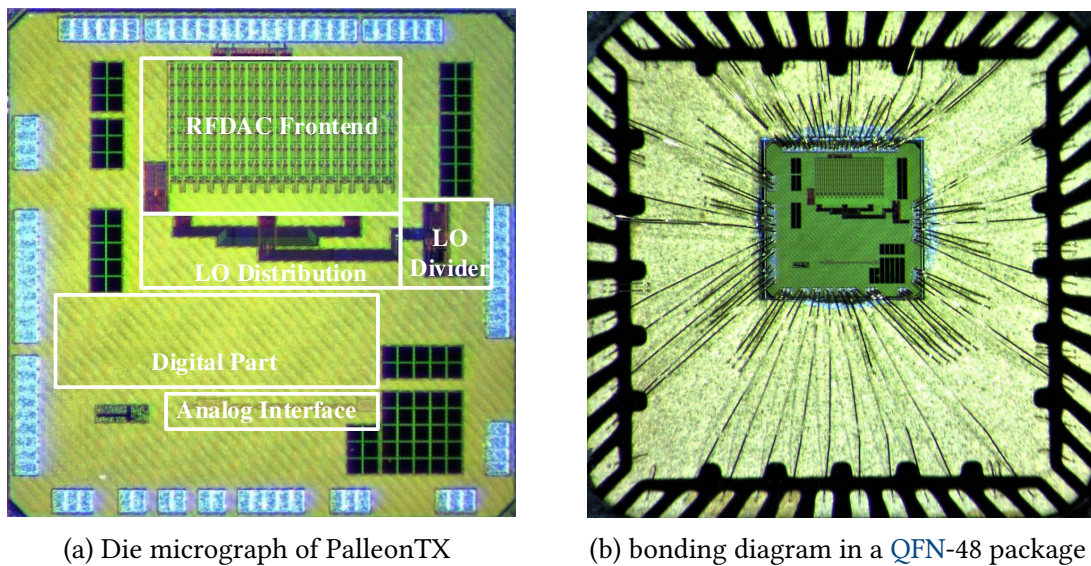


Figure 5.14: Photos of the fabricated chip.

### 5.3.1 Measurement setup

Fig. 5.15 depicts the measurement setup of PalleonTX. In the first place, the transmitter chip is soldered on a **Printed-Circuit Board (PCB)**. DC voltages and reference currents are directly connected to DC supply sources through the connectors on the PCB. In-phase and Quadrature input data of the transmitter, which are transferred from **FPGA** to **RFIC** through the CAG/IO interface, can be selected out of few different sources. The most trivial option is to give a constant input for either of I or Q to check the output level corresponding to different input values in each of the I or Q **DACs**. Furthermore, for an **SSB** sinusoid test, a sine-generator module is programmed in the **FPGA** through a look-up table where the frequency of the sinusoidal signal can be adjusted. At last, the most necessary option is to get modulated data from R&S®SMU200A through its digital baseband output and with the use of an R&S®EX-IQ-BOX.

In order to control the measurement steps, all measurement instruments are connected to the PC via **General-Purpose Interface Bus (GPIB)**. All of the equipments are synchronized through a 10-MHz reference clock from an FS725 Rubidium Frequency Standard. A CG635 clock synthesizer generates  $CLK\_FPGA$  with a default frequency of 80 MHz, which is given to the **FPGA** with 1.8-V **CMOS** signaling as its system clock and also with **LVDS** standard as the reference clock of its GTX transceivers. The EX-IQ-BOX receives input data samples with a lower-frequency baseband clock called  $CLK\_BB$  from R&S®SMU200A. In the **FPGA**, this data is sampled with  $CLK\_FPGA$  and is transferred with the same sampling rate to the **RFIC**. As described earlier, this oversampling is done in order to reduce the error rate during high-speed serial transfer of data. Obviously, the

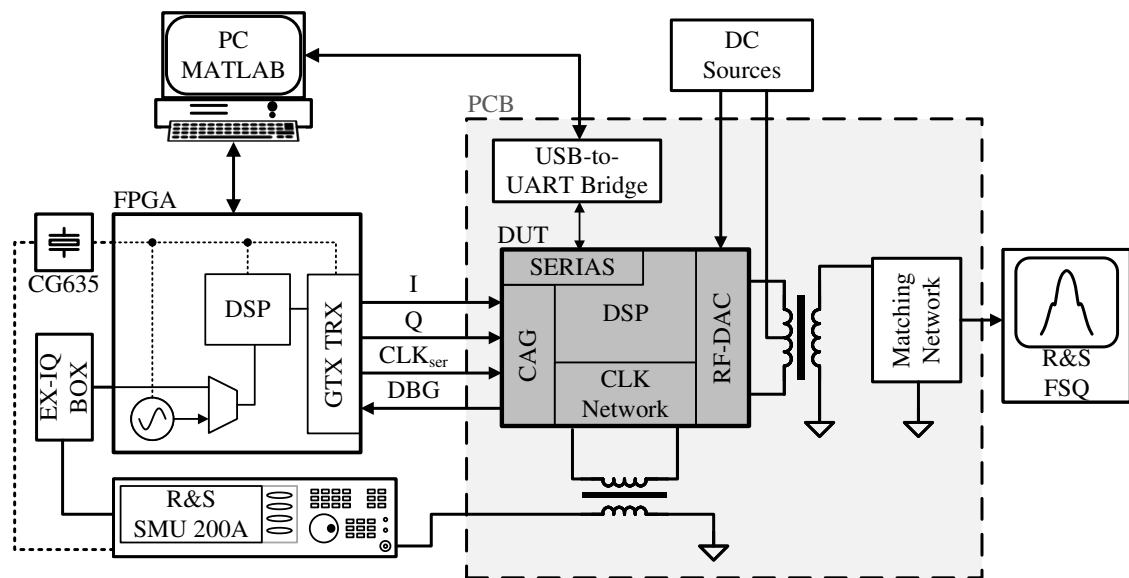


Figure 5.15: Measurement setup of PalleonTX.

frequency of  $CLK\_FPGA$  must be an integer multiple of that of  $CLK\_BB$ . For example, for a WLAN standard with a 20-MHz bandwidth,  $CLK\_BB$  is 20-MHz while  $CLK\_FPGA$  can be either of 80 MHz or 100 MHz.

A break-out board is used to provide a sufficient number of connectors of different types for the FPGA. It uses one of the FMC connectors provided on the FPGA evaluation kit for this purpose. The connection of the high-speed CAG/IO interface is done through 8 SMB connectors between the DUT PCB and the break-out board. The EX-IQ-BOX is also connected to the break-out board with two double-row socket assemblies through which the I/Q data is transferred to the FPGA using LVDS.

In the output of the transmitter, the differential open-drain outputs, which are biased with an external supply through RF chokes, are converted to a single-ended signal through a balun. A matching network is considered to tune the load of this signal and transfer its power to the 50-Ohm load of the measurement device. The combination of the balun and the matching network need to be sufficiently wideband to pass the modulated data. Clearly, a higher load for an open-drain buffer can lead to a higher output power. However, this increases the AM-AM and AM-PM nonlinearities caused by the limited output resistance of DPA unitcells. The reason is that since DPA output impedance is connected in parallel to the load, with a higher load impedance, an increase in the number of active cells and, consequently, a reduction in the output impedance of DPA would be more noticeable in the overall impedance at open-drain nodes. As a result, there is a trade-off between output power and linearity of the frontend when tuning the output load impedance. A load-pull analysis can be performed through a matching line

to find the optimum load.

### 5.3.2 Frontend

In this section, the measurement results of PalleonTX are presented and discussed. It should be mentioned that the maximum input value is limited in the range of  $-655$  to  $655$ . Because of having no possibility of a complete *LVS* run, which is caused due to the existence of the generated *SRAM* in the digital part, the connections of digital signals to the RF frontend could not be verified in the layout level within the tape-out time frame. This led to not detecting the errors made in these connections. However, the only problem caused in this tape-out is that a number of *MSB* columns are not working properly according to their control signals. This is caused by swapping the connection of *ful\_col* and *col* signals of these columns by mistake during the toplevel layout. As a solution for this problem, it is found out that out of 16 *MSB* columns in each of the I/Q *DACs*, 5 of them can be found, which are located after each other and work correctly with the digital control signals. Using the *ESL* and the debug lane of the interface, the starting column can be set to use 5 columns monotonically. However, in this way, data-weighted averaging, which was developed within the *ESL* module to perform a mismatch shaping cannot be used and verified. With 5 *MSB* columns each with 8 *MSB* unitcells as well as with the 4-bit *LSB DAC*, a maximum digital code of 655 can be used. This means almost 2 bits reduction of resolution. However, the *DPA* still shows a sufficient performance to give a sense of the concept as a purpose of this implementation.

#### Static Linearity

As the first step of verifying the performance of the chip, constant values are given to the *DUT* and the output power at carrier frequency is measured. Fig. 5.16 depicts the output power versus the input digital value. It is verified that the output power increases monotonically with an increase in the absolute value of digital magnitude and the *DNL* is kept rather low for all of the digital codes.

Since the load impedance is tuned through an impedance matching line to achieve a rather high fundamental output power, an AM-AM nonlinearity due to the limited output impedance of unitcells is unavoidable. This can be seen in Fig. 5.16b, where the *RMS* output current curve is derived out of the static output power in Fig. 5.16a by considering a standard  $50\ \Omega$  load impedance. It can be seen that the current does not change linearly for digital magnitudes that are higher than 500 or lower than  $-500$ .

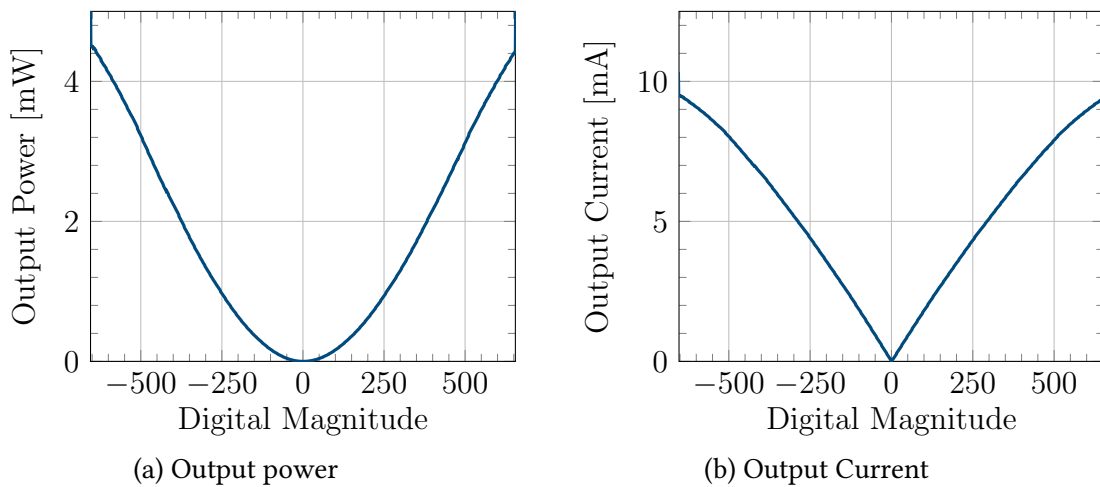


Figure 5.16: Static linearity of PalleonTX at a carrier frequency of 2.4 GHz.

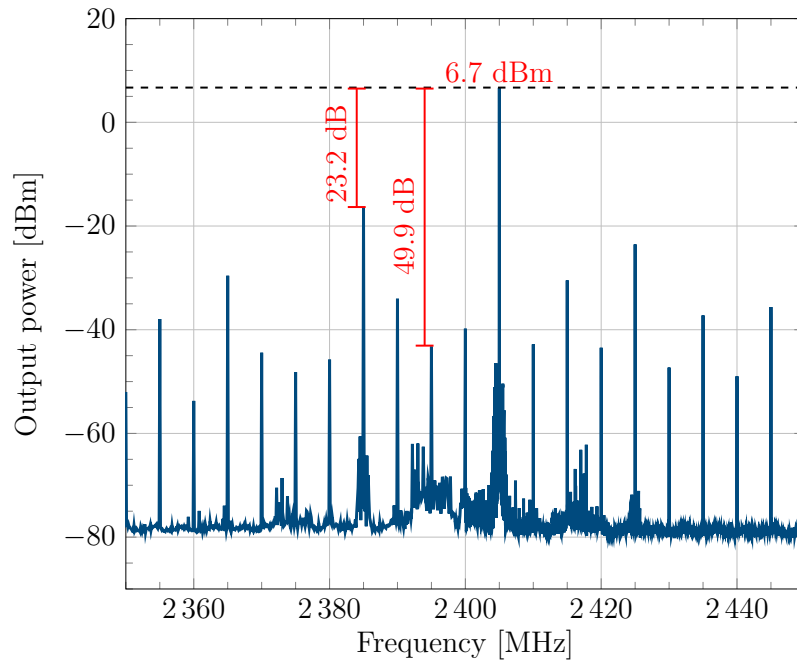
### 5.3.3 Transmitter System

In the next step, the whole transmitter system is tested by applying signals with different frequency contents, which are processed by the digital part and then transmitted by the DPA frontend.

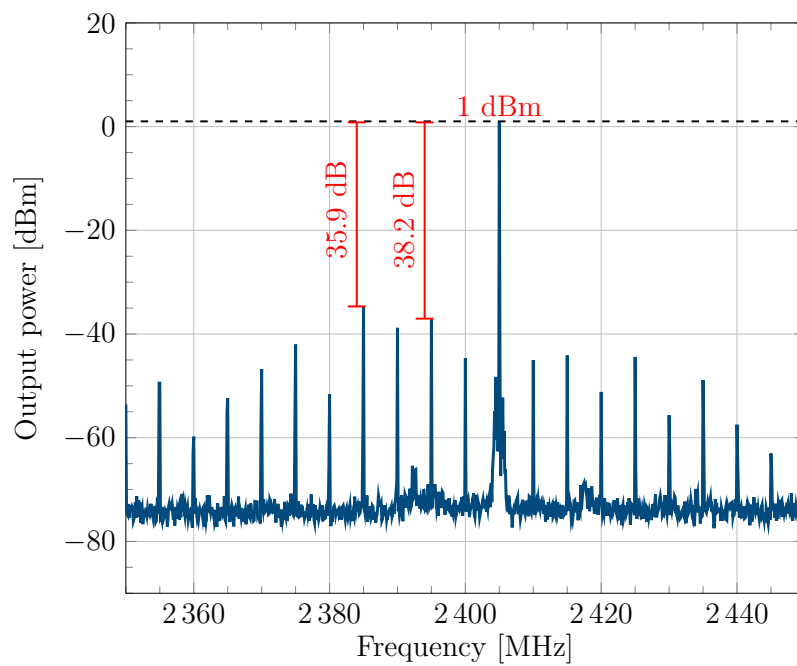
#### SSB Sinusoid Performance

In order to assess the dynamic performance of the DUT, an SSB sinusoidal signal is generated in the FPGA and is fed into the chip through the CAG/IO interface. The output spectrum with a 5-MHz SSB sinusoid input and a carrier frequency of 2.4 GHz can be seen in Fig. 5.17a. The peak power is measured to be 6.7 dBm while an IRR of 49.9 dB and an LO feedthrough of -39.8 dBm are achieved. This measurement result does not take into account the loss introduced by the balun and the cables.

It is evident that due to the limited output impedance of unitcells, there exist many spurs degrading the THD of the output signal. The third-order nonlinearity causes a spur of -23.2 dBc at 2.385 GHz. Clearly, these unwanted intermodulation components depend on both the output power and the load impedance. In order to get a cleaner output spectrum with much less intermodulation spurs, the transmitter can be configured to operate with a lower output power along with a PA, which can amplify it as much as required by the standard in which the transmitter is operating. In this way, although spurs of the output spectrum remain low, the system efficiency could be significantly improved as the PA can exhibit a far better efficiency for such a high output power. Fig. 5.17b shows the spectrum of the output signal during an SSB test with an attenuation of 5.7 dBm, which results in a fundamental output power of 1.01 dBm.



(a) 6.7 dBm peak output power.



(b) 1 dBm peak output power.

Figure 5.17: 5-MHz SSB sinusoid performance of PalleonTX.

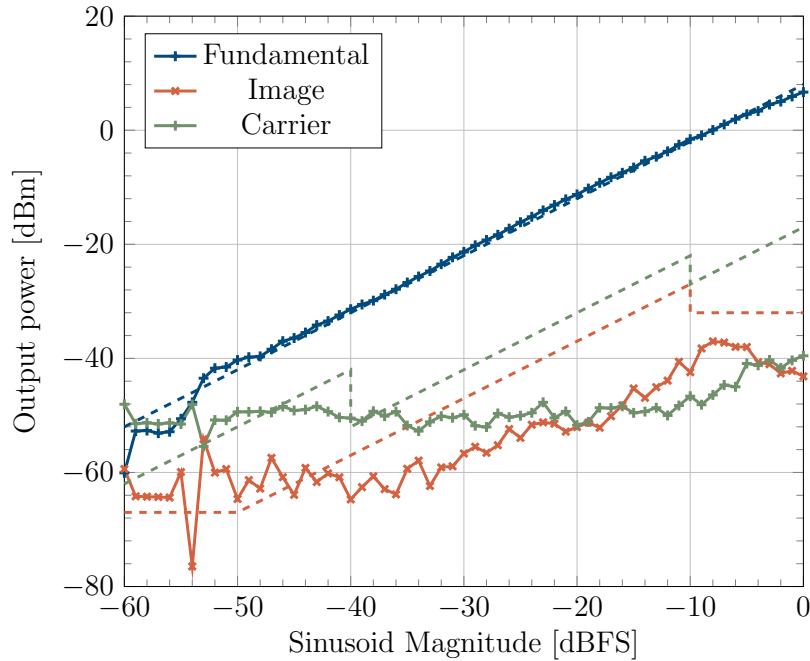


Figure 5.18: 5-MHz SSB power control of PalleonTX.

The problem of spurs due to the finite output impedance of the DPA can also be solved with the use of a 2-D DPD to linearize the transmitter instead of reducing the output power. As explained in section 4.3.3, such a technique applies the reverse nonlinear function of the frontend nonlinearity in the path of its input and leads to a linear transfer curve as a result of cascading the two nonlinear transfer functions.

A power sweep through digital attenuation of the input SSB signal has been run and the power of the desired output tone, the image, and the LO feedthrough are plotted in Fig. 5.18. It can be seen that the fundamental tone changes linearly, as expected, in accordance with the sinusoid magnitude. The carrier tone, which can be interpreted as the LO feedthrough, behaves similarly up to an input attenuation of  $-10$  dB as it is dominated by the dynamic LO feedthrough. However, when the input is further attenuated, it remains the same at around  $-50$  dBm as the static feedthrough becomes more dominant than the dynamic one. It can also be seen that the image tone gets closer to the desired tone which is expected. In other words, the attenuation of the image tone gets smaller as the main tone is reduced through input magnitude attenuation.

For the same sweep of input power discussed above, the power dissipation of the open-drain supply and the LO drivers are plotted in Fig. 5.19. With the peak SSB power, DPA draws a drain current of 21.8 mA from a 1.8 V supply while the LO drivers and frontend custom-designed logics consume a current of 67.3 mA from a 1.2 V supply. This results in a power consumption of 39.3 mW and 80.8 mW, respectively. Therefore, a peak drain

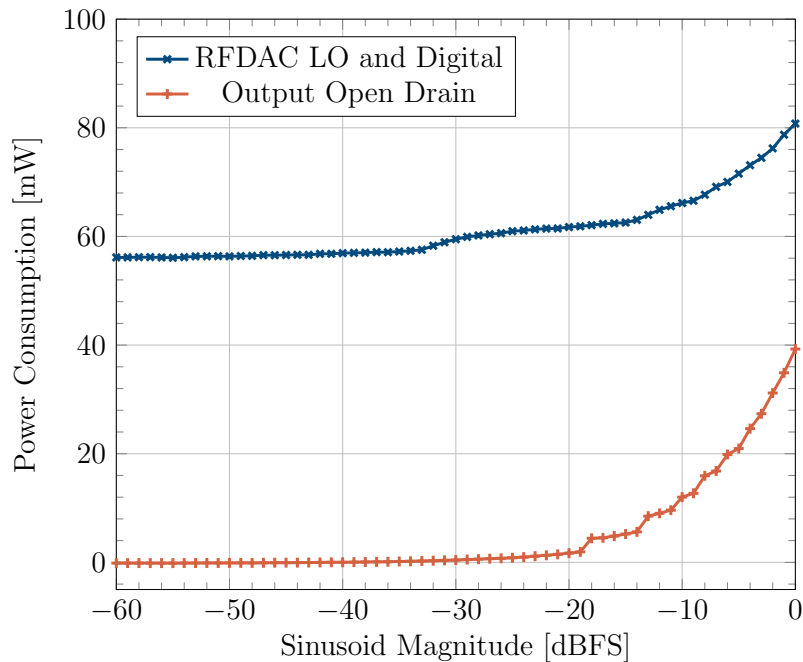


Figure 5.19: Power dissipation through power control of PalleonTX with a 5-MHz SSB signal.

efficiency of  $\eta_{drain,peak} = 11.9\%$  and a peak system efficiency of  $\eta_{sys,peak} = 3.9\%$  is achieved. At the 6-dB power back-off level, the power consumption drops to 19.8 mW and 70 mW for drain and LO driver supplies, respectively. As a result, the drain efficiency is almost halved to  $\eta_{drain,PBO} = 5.9\%$  and the system efficiency drops significantly to  $\eta_{sys,PBO} = 1.3\%$ . Power consumption of the digital part varies between 40 mW and 50 mW depending on the frequency scheme of CLK\_SLOW and CLK\_FAST.

## WLAN Performance

As the next step of validation of PalleonTX, its performance for WLAN communications has to be tested. For this purpose, a 54 Mbps 64QAM signal with a channel bandwidth of 20 MHz according to IEEE 802.11g is generated through R&S®SMU200A. As it is shown in Fig. 5.15, the signal burst data is passed through the EX-IQ-Box to the FPGA and from there, it is transferred through the CAG/IO interface to the transmitter chip. On the output of the transmitter, the RF signal goes through a balun, an SMT connector, and a coaxial cable to reach the spectrum analyzer, which add an overall attenuation of around 3.2 dB, measured separately at carrier frequency of 2.412 GHz. This external attenuation is added to the Settings of R&S®FSQ to compensate it and demonstrate the performance at the output of the transmitter.

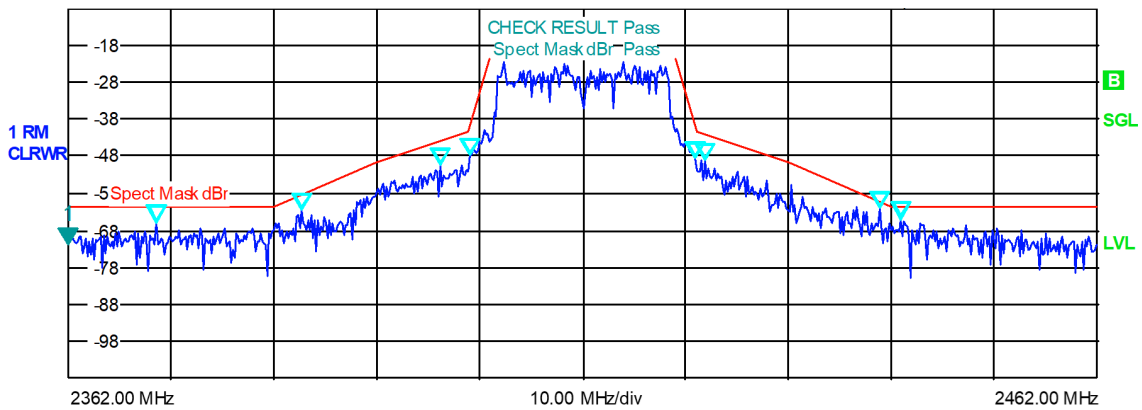


Figure 5.20: WLAN channel 1 spectral mask of PalleonTX.

Table 5.2: PalleonTX WLAN test result summary.

Frequency:	2.4 GHz	Signal Level:	-6.1 dB	External Att:	3.2 dB
Sweep Mode:	Single	Trigger Mode:	Free Run	Trigger Offset:	-10 $\mu$ s
Burst Type:	Direct Link	Modulation:	54 Mbps 64QAM	Data Symbols:	3/1366
Result Summary					
No. of Bursts	2 of 2				
	Min	Mean	Max	Limit	Unit
EVM All Carriers	5.31 -25.49	5.32 -25.48	5.32 -25.48	5.62 -25.00	% dB
EVM Data Carriers	5.35 -25.43	5.36 -25.42	5.36 -25.41	5.62 -25.00	% dB
EVM Pilot Carriers	4.83 -26.33	4.85 -26.28	4.87 -26.24	39.81 -8.00	% dB
IQ Offset	-34.13	-34.10	-34.06	-15.00	dB
Gain Imbalance	-0.38 -0.03	-0.38 -0.03	-0.38 -0.03		% dB
Quadrature Error	-1.23	-1.23	-1.22		$^{\circ}$
Burst Power	-4.78	-4.75	-4.75		dBm
Crest Factor	9.33	9.34	9.34		dB

With a full-scale input signal, the nonlinearities of the frontend dominate the performance, resulting in an *EVM* and a spectrum that violate the specifications of the 802.11g. In order to alleviate this, the input is scaled down by 3 dB. The achieved spectral mask at the output of PalleonTX configured for WLAN channel 1 is presented in Fig. 5.20. The spectrum of the transmit signal passes the spectral mask specification as there is a minimum margin of 3 dB to the mask limits. Table 5.2 lists a summary of the resulting performance of the WLAN transmit signal after being demodulated at R&S®FSQ signal

Table 5.3: Comparison to other works.

	This work	[8]	[12]	[56]
Technology [nm]	65	65	65	40
Architecture	IQ DPA	IQ RF-DAC	polar DPA	IQ DPA + DPD
TX Area [mm <sup>2</sup> ]	0.6	0.18	0.45	0.7
Supply [V]	1.2	1.2	1.2/1.8	1.2/1.8
Band [MHz]	2400	2400	2400	2400
EVM [%]	5.32	5.33	3.98	5.61
Burst Power [dBm]	-4.75	1	10.25	18.8
Drain Efficiency [%]	13.43	3.79	42	17
System Efficiency [%]	0.54	1.21	34	15.5

analyzer. The transmitter provides a burst output power of  $-4.75$  dBm with a PAPR of 9.34 dB, which results in a peak envelope power of 4.6 dBm, as expected according to the SSB test in the previous section. The power consumption of open-drain supply and DPA LO drivers are 2.49 mW and 58.5 mW, respectively. This results in  $\eta_{drain} = 13.43\%$  and  $\eta_{sys} = 0.54\%$ . With these settings, the transmitter realizes a decent performance with respect to IQ offset, gain imbalance, and quadrature error. However, EVM is passing the specification limits very marginally, which is due to high nonlinearities of the frontend.

Table 5.3 shows a comparison with the state-of-the-art transmitters. Although the output burst power is not as high, PalleonTX can achieve comparable EVM and drain efficiency. Since the analog power of LO and clock drivers does not increase significantly with higher output power levels, as in Fig. 5.19, the system efficiency could be improved in case much higher output power was provided such as in [56].



# Chapter 6

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## Digital-Centric Multi-Level LINC Transmitter

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As it has been highlighted throughout this thesis, the demand for ever-improving linearity and power efficiency has always been the key parameter in pushing towards higher communication data throughput being in 5G or 6G applications as well as in future standards that are yet to emerge. And to address this novel challenge, this chapter aims to study and design a **Multi-Level LINC (ML-LINC)** transmitter. As discussed earlier in section 3.2.4, an **ML-LINC** transmitter offers good linearity as well as a high average efficiency by keeping the outphasing angle of the **LINC** transmitter as small as possible. For the purpose of creating different levels for an **ML-LINC** architecture, a high-resolution **RF-DAC** frontend can be used. The high resolution of an **RF-DAC** brings more flexibility for optimization of the number of levels and their positions. However, the imbalance of the two paths can degrade the performance significantly and needs to be taken into consideration during the design of frontends. This might also require compensation with digital calibration. In the following sections of this chapter, the design and implementation of an **ML-LINC** transmitter in a 28-nm technology, called Chameleon, is described and the benefits and drawbacks of such a system in comparison to a simple **I/Q RF-DAC** transmitter are highlighted. In section 6.1, the system design and specifications are discussed. Section 6.2 presents **Multi-Level Signal Component Separator (ML-SCS)** as a key component of the transmitter system, allowing for calibration and optimization of amplitude levels as well as implementation of **DPD**. Next, the implementation of the frontends in the analog domain is followed in section 6.3. Section 6.4 goes through the achieved performance out of the transmitter.

### 6.1 System Perspective

Fig. 6.1 shows the block diagram of Chameleon, which has many parts in common with PalleonTX. The input data is received through a double-speed CAG/IOv2 interface, presented in section 4.1.1, with the capability of transferring data with a two times higher speed compared to that of PalleonTX. This provides the possibility of transferring **OFDM** signals of 802.11.ac with bandwidths up to 160 MHz, which is targeted in this work. As

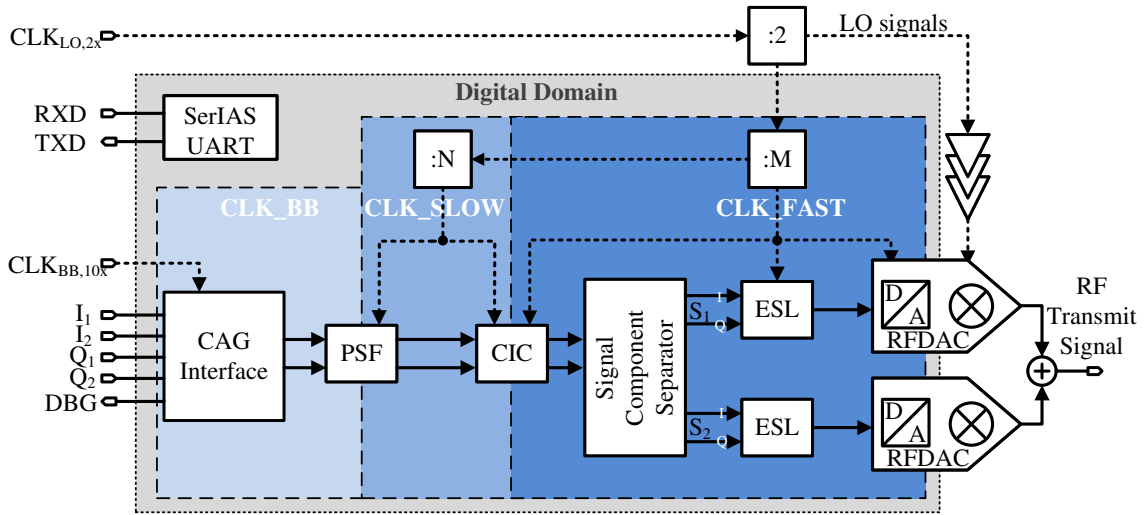


Figure 6.1: System block diagram of Chameleon ML-LINC transmitter.

depicted in Fig. 4.4, the interface requires using two input lanes with LVDS signals for each of I and Q data, one input lane for the baseband clock, and one output lane for the debug data, which results in 12 pins of the chip in total. Speed considerations in section 4.1.1 show that this interface can transfer data with sampling rates up to 200 MHz. The received data is then upsampled to CLK\_FAST in two steps through a PSF and a CIC upsampling filter.

The upsampled data is processed by ML-SCS, which converts it to polar coordinates and finds the next larger level by searching through a set of amplitude levels provided in the register file. Accordingly, outphasing angles are achieved by calculating the ratio of the input amplitude to the selected level and finding its corresponding  $\arccos$  through an LUT. A DPD is also included within the ML-SCS block. More details of this block can be found in section 6.2. In the next step, the outphasing signals, S1 and S2, are passed to the RF-DAC drivers where an ESL selects a corresponding number of RF-DAC unitcells to be activated. Clearly, the faster digital speed provided by the 28-nm technology alleviates the implementation of ML-SCS and ESL blocks with a sampling speed of CLK\_FAST. In spite of that, one still needs to keep the operations simple in each clock cycle to allow for higher speeds.

In the analog domain, for each of the outphasing signals S1 and S2, an I/Q RF-DAC outputs an amplitude of  $LO_I$  and an amplitude of  $LO_Q$  according to the input words. The upconverted outphasing signals are then combined in a power combiner to result in the desired RF transmit signal. Unlike PalleonTX, for each outphasing signal, I and Q paths are combined in one interleaved RF-DAC, which requires LO signals with a duty cycle of 50%. In other words, each unitcell is designed to be used for either of I or Q data. As a result, since the number of unitcells is limited to  $2^N$  for an RF-DAC with N

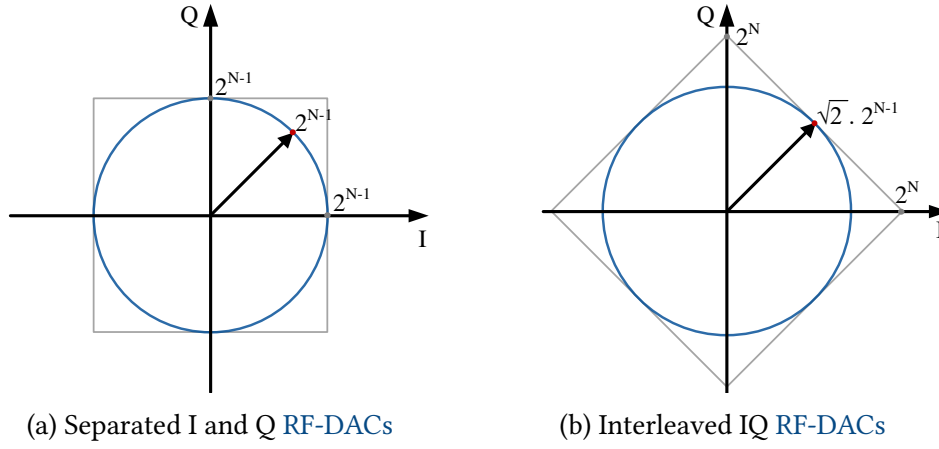


Figure 6.2: Constellation diagrams for digital-centric transmitters with separated RF-DACs and interleaved RF-DACs.

bits of magnitude resolution, the sum of activated I and Q unitcells cannot exceed  $2^N$  and the possible constellation points would be in a diamond shape as the one illustrated in Fig. 6.2b. In contrast to some conventional IQ digital-centric transmitters, where two RF-DACs generate outputs for I and Q data separately, an interleaved IQ RF-DAC can alleviate the mismatches between I and Q paths. Furthermore, with the same  $2^N$  overall number of cells, an interleaved RF-DAC can generate circles with constant constellation vector magnitudes up to  $\frac{2^N}{\sqrt{2}}$  while in the conventional version, the largest constellation circle would be  $\frac{2^N}{2}$ . This can be seen in Fig. 6.2, where the grey square shows the possible constellation vector of the RF-DAC and the circle shows the largest constellation circle of the transmitter system. Clearly, it can be concluded that interleaved RF-DAC can generate 3 dB higher output power with the same number of cells.

Another parameter to be figured out is the drain current of unitcells to achieve a required output power. It is supposed that each of frontends can provide a peak output power of around 8 dBm and therefore, a 6-dB back-off output power of 2 dBm. Considering the constellation diagram shown in Fig. 6.2b, the maximum power level, shown by the blue circle, is achieved when half of the cells are used for the I path and the other half is used for the Q path. As a result, according to (3.8), the peak power can be calculated with regards to the unitcell current and the resolution of the RF-DAC:

$$P_{out,peak} = \frac{R_{load} |I_{out,peak}|^2}{2} = \frac{2^{2N} R_{load}}{\pi^2} \cdot I_0^2, \quad (6.1)$$

where  $N = 11$  denotes the magnitude resolution of the RF-DAC,  $R_{load}$  is the 100- $\Omega$  differential termination load at the balanced side of the balun, and  $I_0$  is the tail current of each unitcell. Therefore, each unitcell needs to provide a current of around 12.18  $\mu$ A.

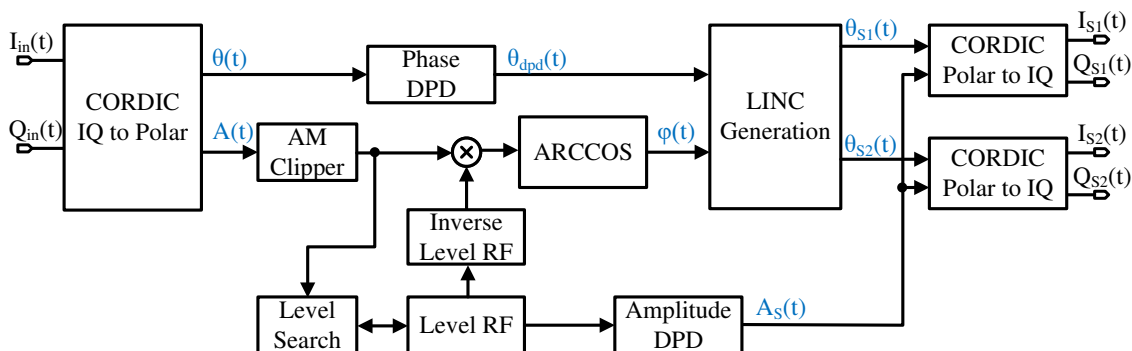


Figure 6.3: Block diagram of SCS of the Chameleon ML-LINC transmitter.

In order to compensate for losses, a typical unit current of  $15 \mu\text{A}$  is considered for the design of unitcells.

## 6.2 Multi-Level LINC Signal Component Separator

An ML-LINC transmitter requires conversion of each input sample to two outphasing vectors in the polar coordinate. For this purpose, a Signal-Component Separator (SCS) should be incorporated into the digital part of the transmitter chip. It is preferred to apply the SCS conversion at the very end stages in the CLK\_FAST domain, where no further upsampling is applied. The reason is that any manipulation in the outphasing signals, such as upsampling, can lead to a mismatch between these two vectors, which makes the result deviate from the desired output after the power combiner.

Fig. 6.3 presents the block diagram of the developed SCS of this work. Since all the computations are performed in polar coordinates, in the first step, the input I/Q signal needs to be converted to its polar representation. For this purpose, a pipelined CORDIC architecture is implemented, which uses a number of iterations of simple shift and add operations [42]. Generally, a higher number of iterations guarantees a smaller error of the calculated angle, which improves the ACLR of the transmitter. System simulations of [42] show that a minimum of 14 iterations are required to minimize the impact of the CORDIC on the ACLR. Accordingly, a CORDIC with 16 iterations is implemented in this work.

In the next step, the amplitude is clipped to a maximum value programmed in the register file. This would limit the AM signal to the boundaries of the frontend inputs. The clipped amplitude signal is fed to a level-search block which finds the next larger level. The set of levels as well as their inverse values are provided through the register file and can be programmed according to off-chip level optimizations. By having the amplitude

of outphasing signals, a **DPD** can be implemented to compensate for AM-PM and AM-AM nonlinearities. A phase **DPD** is also implemented to compensate phase-related nonlinearities.

In order to calculate the outphasing angle according to (3.14), the ratio of AM to the outphasing level is calculated by multiplying it by the inverse value of the outphasing level. Consequently, the outphasing angle,  $\varphi$ , is calculated by looking up the *arccosine* of the AM ratio in an **LUT** designated for it. Then, the phase output of the phase **DPD**,  $\Theta_{dpd}$ , and the calculated  $\varphi$  are summed and subtracted to achieve phases of the outphasing signals. In a final step, S1 and S2 are converted back from polar representation to I/Q coordinates. For this purpose, a **CORDIC** with 16 iterations similar to that of I/Q to polar conversion is employed.

It is worth to mention that all the data processing functions in the **SCS** block are performed on data words with a width of 16 bits and a resolution of 16 bits is used for both amplitude and phase signals. These are selected according to the study described in [42]. Furthermore, each step of signal processing on either of the phase or the amplitude is tied with applying a corresponding delay on the other one to match the delay. In contrast to the IQ digital-centric transmitter, an **ML-LINC** transmitter provides less flexibility for compensating **LO** feedthrough and the mismatches between I and Q paths of each **RF-DAC** separately. Since S1 and S2 signals need to reflect as small as possible mismatch, one cannot compensate the imbalances of these two paths independently.

## 6.3 Design and Implementation of RF-DAC Frontends

It can be claimed that the most important and most challenging part of this transmitter system would be design and implementation of its **RF-DAC** frontends as they affect the performance significantly. For this reason, careful considerations are taken into account for designing this part of the system.

### 6.3.1 Unitcells

As mentioned earlier, each unitcell should provide a current of approximately  $15\ \mu\text{A}$ , which is rather small. This makes it hard to implement it with simple kinds of current unitcells such as **DPA** since the mismatch would be high when very small devices are used. Furthermore, as discussed above, each cell should be able to be used with either of I or Q phases of the **LO** signal. This brings further complication to the custom-designed logic of each unitcell as will be discussed later.

Before the design of the unitcells is presented, it is important to look into their boolean current equation. For a simple unitcell of an **RF-DAC** like the one in Fig. 5.10, each cell

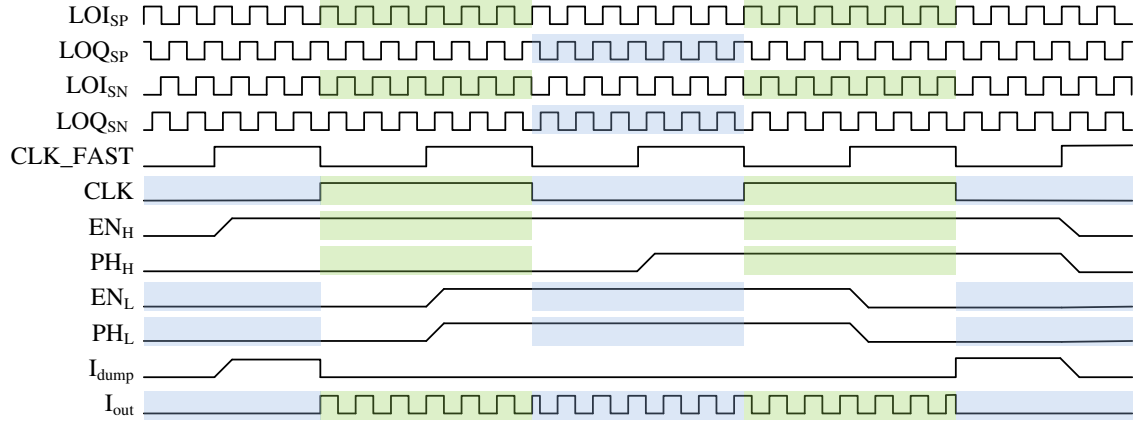


Figure 6.4: Illustration of alternative data sample phases for syncing them with LO.

needs a signal that activates the cell,  $EN$ , in addition to differential LO signals with the effect of sign bit, called  $LO_{SP}$  and  $LO_{SN}$ . Since the unitcells in Chameleon are going to be used for either of I or Q data, an LO phase-select signal,  $PH$ , is considered. If  $PH$  is 0, the cell is used for the I data while if 1, it is used for the Q data. As a result, the boolean logic equation of the normalized differential output current of a unitcell is given by the following equation:

$$\begin{aligned} I_{OUT,P} &= EN \cdot \left( \overline{PH} \cdot LO_{ISP} + PH \cdot LO_{QSP} \right), \\ I_{OUT,N} &= EN \cdot \left( \overline{PH} \cdot LO_{ISN} + PH \cdot LO_{QSN} \right), \end{aligned} \quad (6.2)$$

where  $LO_{ISP}$  and  $LO_{ISN}$  are differential LO signals for the I path, which are switched according to the sign bit as in Fig. 5.12 and  $LO_{QSP}$  and  $LO_{QSN}$  are those of the Q path.

A problem that should be dealt with is syncing the data signals generated by the digital core with the LO signals throughout all the unitcells of RF-DAC. In PalleonTX, a clock signal with the same frequency of  $CLK\_FAST$  was used to sync the data signals by sampling them at each unitcell. Here, it is implemented in a different way. The operation of unitcells is divided to a pair of timing phases through using a clock signal with half the frequency of  $CLK\_FAST$ , which is called  $CLK$  here for simplicity. In this way, two sets of data samples can be specified, one corresponding to the high phases of  $CLK$  and the other corresponding to its low phases. In other words, the digital core provides  $EN_H$  and  $PH_H$  to determine the data sample during the phases when  $CLK$  is high while  $EN_L$  and  $PH_L$  correspond to low phases of  $CLK$ . As shown in Fig. 6.4, the data samples of each phase should be available at unitcells before their corresponding edge of  $CLK$  and should be kept constant at least till the end of this phase of  $CLK$ . This brings the possibility of generating each data set with a half frequency and provides more time for their propagation delay compared to the previous method used in PalleonTX.

Looking into the logic equation corresponding to this method, one can rewrite (6.2) as:

$$\begin{aligned}
 I_{OUT,P} &= CLK \cdot EN_H \cdot \left( \overline{PH_H} \cdot LOI_{SP} + PH_H \cdot LOQ_{SP} \right) \\
 &+ \overline{CLK} \cdot EN_L \cdot \left( \overline{PH_L} \cdot LOI_{SP} + PH_L \cdot LOQ_{SP} \right), \\
 I_{OUT,N} &= CLK \cdot EN_H \cdot \left( \overline{PH_H} \cdot LOI_{SN} + PH_H \cdot LOQ_{SN} \right) \\
 &+ \overline{CLK} \cdot EN_L \cdot \left( \overline{PH_L} \cdot LOI_{SN} + PH_L \cdot LOQ_{SN} \right).
 \end{aligned} \tag{6.3}$$

In this version of RF-DAC, instead of switching LO signals according to the sign bit at column drivers, it is combined with the logic operation at each unitcell. Since the phase of each unitcell is selectable, both sign bits of I and Q data, called  $SI$  and  $SQ$ , respectively, should be available at unitcells. Furthermore, the requirement of two data sets for both phases of  $CLK$  makes it necessary to provide four signals of  $SI_L$ ,  $SQ_L$ ,  $SI_H$ , and  $SQ_H$  to all unitcells.

In this regard, it is important to derive the final logic description of each unitcell. The logic boolean equation of sign switching of LO signals, as in Fig. 5.13, is given by:

$$\begin{aligned}
 LO_{SP} &= \overline{S} \cdot LO_P + S \cdot LO_N, \\
 LO_{SN} &= \overline{S} \cdot LO_N + S \cdot LO_P,
 \end{aligned} \tag{6.4}$$

where  $S$  denotes the sign bit of data samples. As a result, by considering the four sign signals for different phases, (6.3) can be rewritten as:

$$\begin{aligned}
 I_{OUT,P} &= CLK \cdot EN_H \cdot \overline{PH_H} \cdot \left( \overline{SI_H} \cdot LOIP + SI_H \cdot LOIN \right) \\
 &+ CLK \cdot EN_H \cdot PH_H \cdot \left( \overline{SQ_H} \cdot LOQP + SQ_H \cdot LOQN \right) \\
 &+ \overline{CLK} \cdot EN_L \cdot \overline{PH_L} \cdot \left( \overline{SI_L} \cdot LOIP + SI_L \cdot LOIN \right) \\
 &+ \overline{CLK} \cdot EN_L \cdot PH_L \cdot \left( \overline{SQ_L} \cdot LOQP + SQ_L \cdot LOQN \right), \\
 I_{OUT,N} &= CLK \cdot EN_H \cdot \overline{PH_H} \cdot \left( \overline{SI_H} \cdot LOIN + SI_H \cdot LOIP \right) \\
 &+ CLK \cdot EN_H \cdot PH_H \cdot \left( \overline{SQ_H} \cdot LOQN + SQ_H \cdot LOQP \right) \\
 &+ \overline{CLK} \cdot EN_L \cdot \overline{PH_L} \cdot \left( \overline{SI_L} \cdot LOIN + SI_L \cdot LOIP \right) \\
 &+ \overline{CLK} \cdot EN_L \cdot PH_L \cdot \left( \overline{SQ_L} \cdot LOQN + SQ_L \cdot LOQP \right),
 \end{aligned} \tag{6.5}$$

where  $LOIP$ ,  $LOQP$ ,  $LOIN$ , and  $LOQN$  are four different phases of LO with a phase-shift

of 90°. This can be simplified by defining the following variables:

$$\begin{aligned}
 C_{L,IP} &= EN_L \cdot \overline{PH_L} \cdot \overline{SI_L}, & C_{H,IP} &= EN_H \cdot \overline{PH_H} \cdot \overline{SI_H}, \\
 C_{L,IN} &= EN_L \cdot \overline{PH_L} \cdot SI_L, & C_{H,IN} &= EN_H \cdot \overline{PH_H} \cdot SI_H, \\
 C_{L,QP} &= EN_L \cdot PH_L \cdot \overline{SQ_L}, & C_{H,QP} &= EN_H \cdot PH_H \cdot \overline{SQ_H}, \\
 C_{L,QN} &= EN_L \cdot PH_L \cdot SQ_L, & C_{H,QN} &= EN_H \cdot PH_H \cdot SQ_H,
 \end{aligned} \tag{6.6}$$

$$\begin{aligned}
 LOIP_{SP} &= LOIP \cdot \left( C_{H,IP} \cdot CLK + C_{L,IP} \cdot \overline{CLK} \right), \\
 LOIN_{SN} &= LOIN \cdot \left( C_{H,IN} \cdot CLK + C_{L,IN} \cdot \overline{CLK} \right), \\
 LOQP_{SP} &= LOQP \cdot \left( C_{H,QP} \cdot CLK + C_{L,QP} \cdot \overline{CLK} \right), \\
 LOQN_{SN} &= LOQN \cdot \left( C_{H,QN} \cdot CLK + C_{L,QN} \cdot \overline{CLK} \right),
 \end{aligned} \tag{6.7}$$

$$\begin{aligned}
 LOIN_{SP} &= LOIN \cdot \left( C_{H,IP} \cdot CLK + C_{L,IP} \cdot \overline{CLK} \right), \\
 LOIP_{SN} &= LOIP \cdot \left( C_{H,IN} \cdot CLK + C_{L,IN} \cdot \overline{CLK} \right), \\
 LOQN_{SP} &= LOQN \cdot \left( C_{H,QP} \cdot CLK + C_{L,QP} \cdot \overline{CLK} \right), \\
 LOQP_{SN} &= LOQP \cdot \left( C_{H,QN} \cdot CLK + C_{L,QN} \cdot \overline{CLK} \right).
 \end{aligned} \tag{6.8}$$

As a result, each of  $I_{OUT,P}$  and  $I_{OUT,N}$  can be written as an OR product of all variables in (6.7) and (6.8), respectively:

$$\begin{aligned}
 I_{OUT,P} &= LOIP_{SP} + LOIN_{SN} + LOQP_{SP} + LOQN_{SN}, \\
 I_{OUT,N} &= LOIN_{SP} + LOIP_{SN} + LOQN_{SP} + LOQP_{SN}.
 \end{aligned} \tag{6.9}$$

It can be argued that out of all 8 variables in both lines of the above boolean equations, only one can be 1 at each point in time. In other words, each of the four signals in each line of this equation would represent one of the four phases of the LO and data inputs  $EN_{H/L}$ ,  $PH_{H/L}$ , and  $SI/Q_{H/L}$  determine which LO phase should be redirected to each of positive and negative outputs with each data sample.

### Analog current switching

In order to implement the logic derived in (6.9), the analog part of each unitcell is designed as in Fig. 6.5. It consists of a current mirror that can be switched through 8 different output branches according to the data sample when the cell is turned on. An additional current branch is added so that the current mirror can be kept on even when the cell is not selected to contribute to the output. This is useful to eliminate the unwanted effect on the dynamic performance of the frontend due to turning the current mirror on and

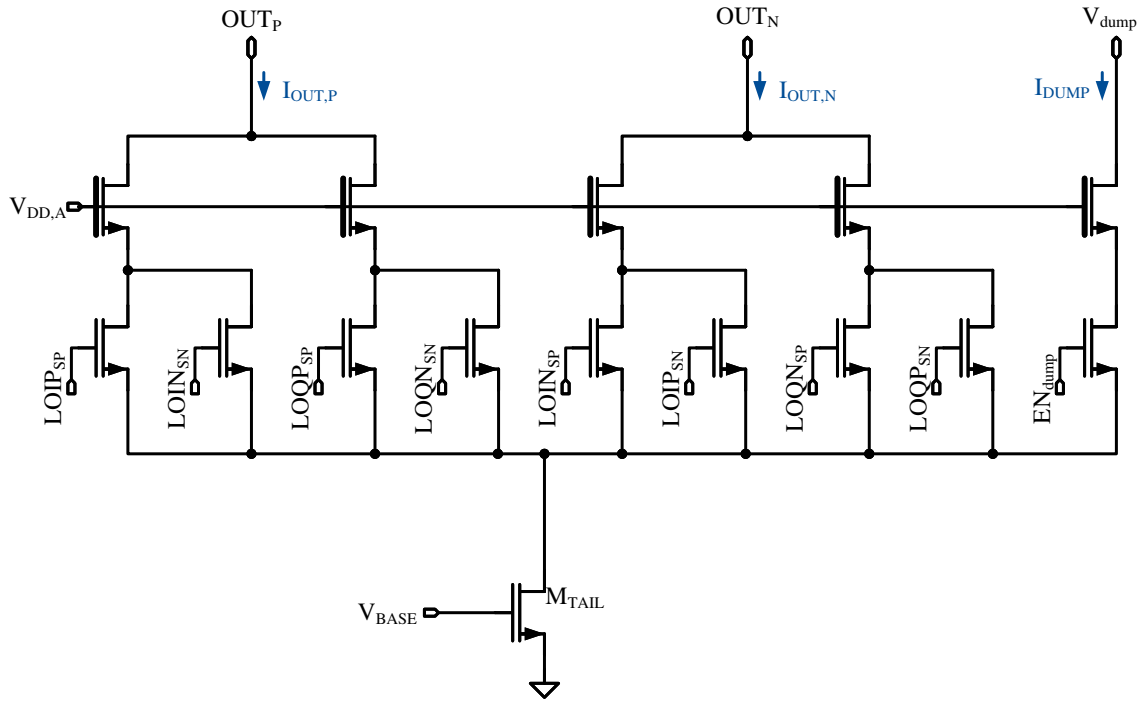


Figure 6.5: Analog current switching unitcell.

off. It guarantees that when a specific unitcell is going to be turned on with the next edge of  $CLK$ , the slow transient response of turning its current mirror on, which can take up to a few  $LO$  cycles, is passed beforehand.

When a cell is turned on according to the input data, the tail current is constantly switched between one of its positive and one of its negative branches with the  $LO$  signal. In order to explain this circuit more clearly, Fig. 6.6b shows an equivalent circuit for the operation of each branch. The tail current is provided by  $M_{TAIL}$ ,  $M_{SW}$  switches the tail current to this branch with  $LO$  signal, and  $M_{CASC}$ , which is a thicker oxide device, isolates the output from the  $LO$  switch. As mentioned earlier, the output is biased at 1.8 V,  $V_{DD,A}$  is 1 V, and  $V_{DD,D}$ , which is the supply voltage of custom-designed logic circuits as well as  $LO$  buffers, is also 1 V. As a result, when  $LO$  is high,  $M_{CASC}$  would be in Saturation while  $M_{SW}$  goes to triode and behaves just as a switch to conduct the tail current through  $M_{CASC}$ . During this phase,  $V_{D,MSW}$  would go down and  $M_{CASC}$  conducts all the tail current to the output node. In the next phase, when  $LO$  becomes 0 and the current is conducted through another branch,  $M_{CASC}$  does not conduct a significant current and therefore, its overdrive voltage is decreased significantly, which leads to an increase in  $V_{D,MSW}$ .

The cascode transistor helps to increase the output impedance, which is desired to reduce AM-PM and AM-AM nonlinearities. From the logic point of view, one cascode transistor

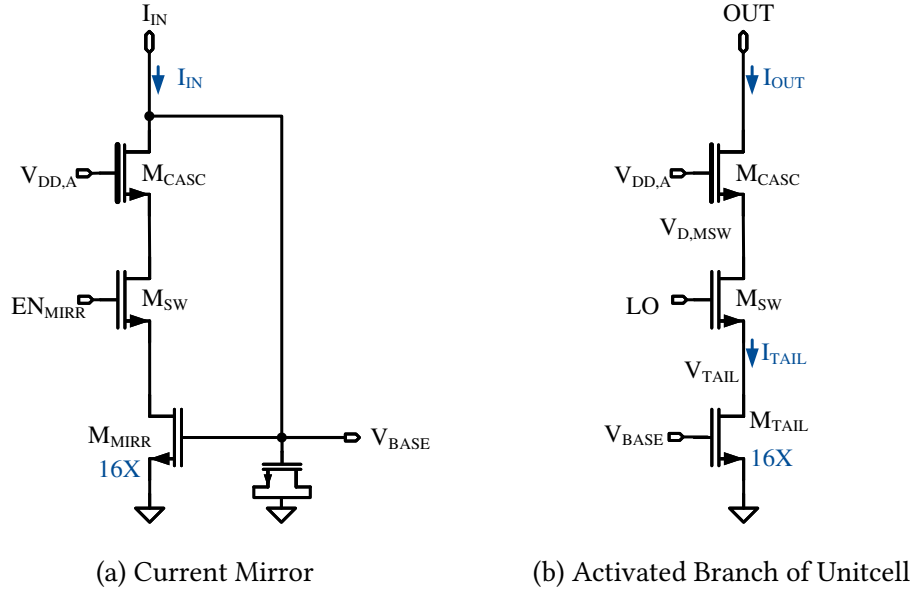


Figure 6.6: Equivalent circuit for branches of analog current switching.

can be shared for all 4 branches going to each one of the output nodes as only one can conduct current at each point in time. However, due to higher capacitance of sharing paths of all 4 switching transistors, the speed of the switching would be reduced. With this trade-off in mind, the cascode transistors are shared for every 2 branches.

The dumping branch is designed the same way as the output branches, with the only difference of its output bias voltage that is 1 V to reduce the power consumption. Considering the case that the unitcell is off while it should contribute to the output with the next data sample, the dumping branch should be activated in a sufficient time window before the switching edge of  $CLK$  so that the tail current settles to its normal operational point before switching  $LO$  signals are given to switching branches. This is shown in Fig. 6.4 as  $I_{dump}$ . In order to achieve such an operation, this branch can be enabled with the following boolean equation:

$$EN_{dump} = CLK \cdot (\overline{EN_H} \cdot EN_L) + \overline{CLK} \cdot (EN_H \cdot \overline{EN_L}). \quad (6.10)$$

Since the current mirror consists of a single transistor, current switching with  $LO$  frequency can induce switching noise into the tail current. To relieve this problem, more capacitance can be added to the drain of  $M_{TAIL}$ . However, this will make it slower and more power consuming to turn the tail transistor on as more current should flow from the dumping supply to  $V_{TAIL}$  to charge this capacitance. Furthermore, it is important to make sure that the  $LO$  signals as well as the enable signal of the dump branch are all symmetric in timing. Even a small overlap would be desirable so that the current is

switched from one branch to another without any timing gap in between.

As it can be seen in Fig. 6.6a, the current mirror consists of a biasing circuit similar to conventional wide-swing current mirrors except that it is stacked with the same transistor sizings as that of an LO switching branch of the MSB unitcell. In order to make the bias voltage more stable with regard to the switching spurs, an adequate number of MOS capacitors are added to this node. Also, it is worth mentioning that a programmable current mirror is considered on the toplevel of the frontend to provide current control in the range of 7.8  $\mu\text{A}$  to 25  $\mu\text{A}$ . This allows for additional analog control of the output power.

The implementation of bleeding currents has been investigated here as well. In order to make the switching faster, one can add bleeding currents to keep the cascode transistor on with a very small overdrive voltage even when the tail current is conducted through another branch of the unitcell. In this way, with the help of bleeding currents that are in the range of 10 % of the tail current, the current switching speed can be improved as the cascode transistor is not completely switched off and on with the LO signal. However, it does add additional capacitance and increases power consumption while the speed improvement is not significant in the case of the MSB unitcell of this design. Furthermore, bleeding currents can help to reduce the change of output capacitance of the unitcell by switching it on or off, which improves the linearity of the RF-DAC [102]. However, since the parasitics of the layout are dominant in this design, it does not improve the AM-PM linearity noticeably.

For LSB unitcells, which should conduct a current 16 times smaller than that of MSB unitcells, the same current biasing circuit is used while the tail transistor of the unitcell is 16 times smaller. Instead of using 16 multiples of the same transistor, as in the current biasing circuit and MSB unitcells, only one transistor is used along with enough dummy transistors around it. In other words, the current is mirrored with a ratio of 16 to 1 for the LSB unitcells. Since an LSB unitcell conducts a much smaller current, the sizing of switching and cascode transistors should shrink down to keep the same switching speed. In order to further decrease the capacitance of each branch, cascode transistors are not shared and each switching transistor is followed by an individual cascode transistor, resulting in 8 overall thick-oxide cascode transistors. One important design aspect is that each LSB unitcells produces the same output current phase and 16 times smaller current amplitude at the LO frequency. This shall be verified at all PVT corners and through Monte-Carlo simulations.

#### **Custom-designed digital logic of unitcells**

Given this structure for the analog part of unitcells, the required switching signals should be generated in a custom-designed logic circuit in each unitcell. Therefore, (6.7) and

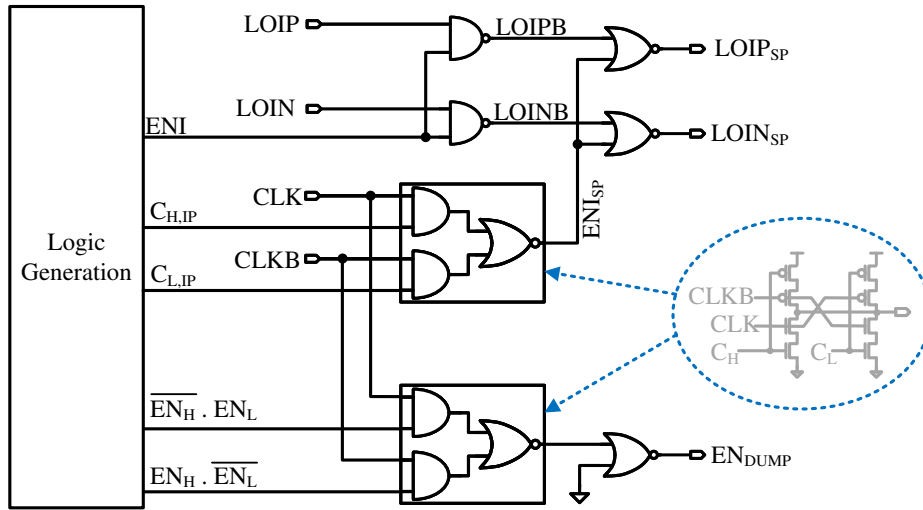


Figure 6.7: Custom-designed logic for generating  $LOIP_{SP}$  and  $LOIN_{SP}$ .

(6.8) should be implemented with careful considerations regarding the timing of  $LO$  signals as well as  $CLK$ . It is important to reduce the number of gates and propagation delays from  $LO$  signals and  $CLK$  to outputs of these equations as less mismatch should be introduced to the timing of these signals in different cells. With larger gates leading to faster switching and shorter rise and fall times, the effect of local circuitry mismatch on timing as well as added jitter of the gates would be smaller. For this reason, in the first step, variables given in (6.6) are generated through normal logic gates, and then these are combined with  $LO$  and  $CLK$  signals through low-threshold  $MOS$  devices to generate the final switching signals of the analog part.

Fig. 6.7 illustrates the digital logic implementation to generate  $LOIP_{SP}$  and  $LOIN_{SP}$ , which includes two stages of gates from either of  $CLK$  or  $LO$  signals to switching signals. In the first stage,  $CLK$  and  $\overline{CLK}$  are combined with variables given in (6.6) while  $LO$  signals are inverted through NAND gates. Then, in the second stage, a specifically-sized NOR gate combines these two to achieve the logics of (6.7) and (6.8). In order to generate  $EN_{dump}$  according to (6.10), the same gates of  $LO$  switching outputs are used with the exception that the second input of the NOR gate is connected to ground. This is necessary as  $EN_{DUMP}$  should have the same timing as switching  $LO$  signals at the edges of  $CLK$  and  $\overline{CLK}$ .

With this implementation, simulation results show that in the worst case, data sample signals should be available at each unitcell by about 100 ps prior to edges of  $CLK$  so that they cause no timing error for the switching  $LO$  signals. However, when considering the settling of the tail current through the dumping branch prior to using the cell, this setup time is increased. As a result, in practice, data input signals of  $EN_H$  and  $EN_L$  should be there at least 350 ps before the edges of  $CLK$ . This timing consideration of

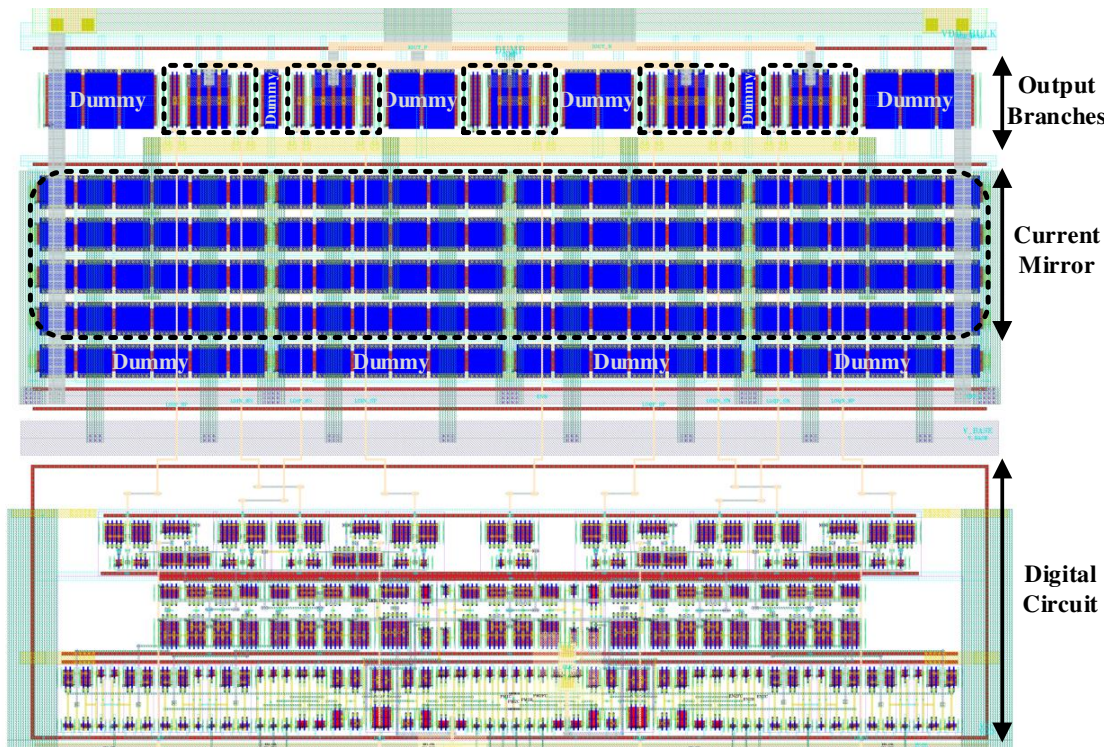


Figure 6.8: Layout of an MSB unitcell of the RF-DAC.

data inputs should be taken into account for routing these signals from the digital part to each unitcell of the RF-DAC.

### Layout of Unitcells

Fig. 6.8 shows the layout of an MSB unitcell of Chameleon. The tail transistor, which consists of 16 multiples of the same transistor, is laid out in 4 rows, each with 4 transistors. A row of dummy devices with the same dimensions is placed just below the tail transistor to isolate it from the empty space between the digital and the analog parts of the unitcell. The switching transistors and cascode transistors of the switching branches as well as the dumping branch are laid out symmetrically in one row on top of the tail transistor while enough dummy devices are placed in between to eliminate empty spaces. The whole analog part is implemented in a deep-N-Well with lots of guard rings to bias both of the N-Well and the P-Well inside it.

The custom-designed digital part of the unitcell is placed with a distance below its analog part. The logic digital circuits for generating variables given in (6.6) are placed in the lower row. The Data-clock combiner circuits of Fig. 6.8 are implemented in the second row and the final LO-enabling NOR gates are laid out on the upper row that is closer to

the analog part. Different guard rings and diffusion layers are placed in between these three rows to bias the circuits as well as their wells. It can be seen in Fig. 6.8 that thanks to the 28-nm minimum length of this technology, the custom-designed logic circuit is relatively small although it includes many different blocks.

The overall size of the unitcell layout is  $28\ \mu\text{m} \times 20\ \mu\text{m}$ , which is relatively small when compared to PalleonTX. The layout of **LSB** unitcells is also designed with the same size and arrangement. The custom-designed logic circuit is the same as that of **MSB**. In the analog part, out of 16 multiples of the same NMOS transistor, only one is used for the tail current while the rest of them are used as dummies and capacitors for  $V_{base}$ . The current biasing circuit of the tail current mirror is also implemented with a similar layout, whereas the custom-designed logic circuitry is replaced with the same size of **MOS** capacitors that are connected to  $V_{base}$ .

### Unitcell Performance

With the layout provided, one important aspect to be investigated is the output impedance of each unitcell and its changes through switching it on or off. Fig. 6.9 shows post-layout simulation results for output parallel capacitance and resistance of both **MSB** and **LSB** cells through corners around the frequency band of 5 GHz. It can be seen that in post-layout simulations, the output capacitance change between when the unitcell is completely off and when it is conducting current is not noticeable as it is less than 1.3 % in the worst case. Therefore, it does not contribute to a significant AM-PM nonlinearity while additional routing parasitics capacitance of the frontend output routing reduces this difference ratio as well. For AM-AM nonlinearity, one should check for the minimum output resistance when compared to the load resistance. The worst-case scenario occurs when a maximum number of unitcells are turned on. In this case, all 128 **MSB** unitcells and 32 **LSB** unitcells are turned on, which results in a minimum resistance of around 1.15 k $\Omega$  from each of the positive and negative outputs of the **RF-DAC** in the worst-case corners. The load resistance will be determined by a matching network that transfers the power to the 50  $\Omega$  load termination. Although it can be different depending on the matching network determined by a load-pull measurement, it can be approximated to be around 50  $\Omega$  termination load. A reduced output resistance of 1.15 k $\Omega$  in parallel to a load resistance of 50  $\Omega$  results in an overall resistance of 47.9  $\Omega$ , which would translate to around 0.19 dB attenuation of the output power relative to an absolutely linear performance. This is clearly much smaller than a 1-dB compression point.

Another important aspect of the design of unitcells is the output current amplitude generated by each unitcell. In the case of a perfect square waveform of current from each of the positive and negative branches, it is expected that in each **LSB** unitcell, each branch outputs a current amplitude of  $0.5 \times 15\ \mu\text{A} \times 4/\pi = 9.55\ \mu\text{A}$ . However, due to delays and slower edges, an amplitude of 8.8  $\mu\text{A}$  is achieved in the typical corner. The most

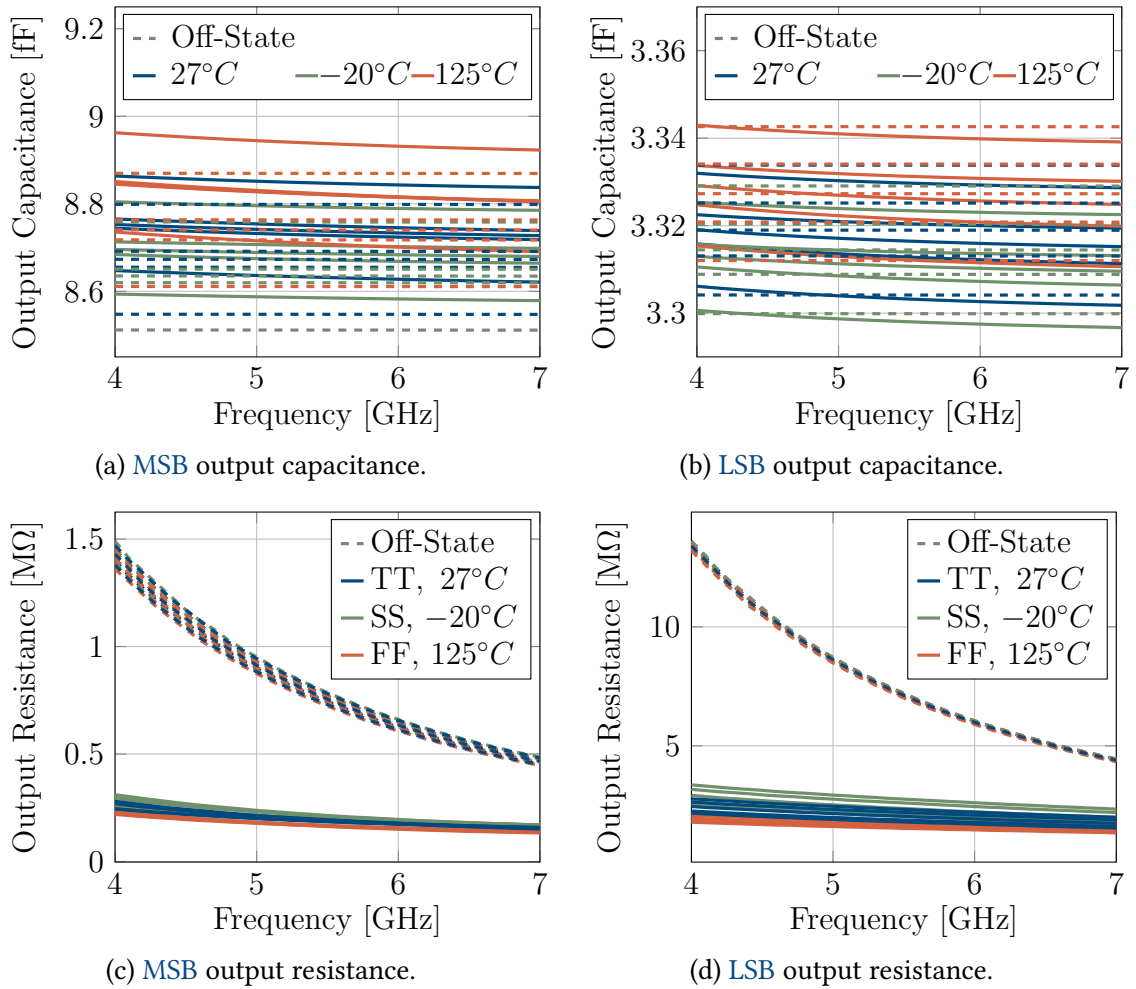


Figure 6.9: Post-layout output impedance of unitcells across frequency.

important aspect here is that the output current of **LSB** unitcells should match that of **MSB** ones to guarantee linearity of the frontend. For this purpose, the amplitude and the phase of 16 **LSB** unitcells can be compared to those of an **MSB** unitcell. Fig. 6.10 shows it across carrier frequency for all **PVT** corners, including 5 process corners, 3 temperature corners, and 3 supply voltage corners of  $\pm 5\%$ . In the worst cases, there is a difference of  $0.85^\circ$  in phase and 3.6 % in amplitude. Furthermore, a Monte-Carlo simulation with 1000 samples is run, which shows that the **DNL** of the case switching from 15 **LSB** unitcells to 1 **MSB** unitcell, does not exceed 70 % and the phase difference in this case is less than  $6.5^\circ$ .

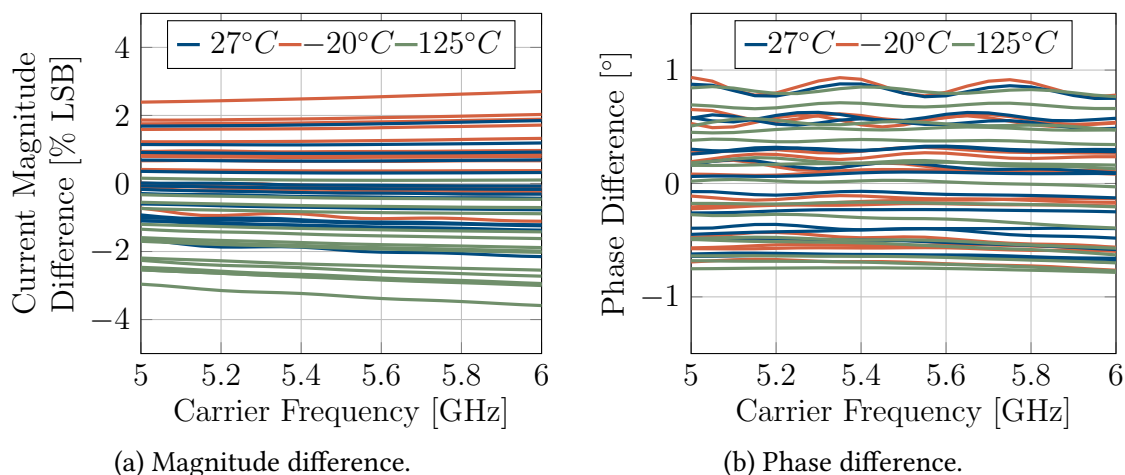


Figure 6.10: Output current of 16 **LSB** unitcells compared to that of 1 **MSB** unitcell with extracted netlist.

### 6.3.2 RF-DAC Structure

Each **RF-DAC** frontend used in Chameleon is structured in the form of columns and rows similar to that of PalleonTX. The **DAC** consists of 10 columns overall, including 8 **MSB** columns and 2 **LSB** columns, each with 16 unitcells. Therefore, it consists of a 7-bit **MSB DAC** with 128 unary-weighted elements and two 4-bit **LSB DACs**, each with 16 binary-weighted elements. Furthermore, a programmable current mirror is included in the frontend's toplevel, which can control the current of unitcells, providing an analog means of power control.

Each of the columns consists of 16 unitcells and 2 current mirror biasing circuits along with buffers for **LO** signals, *CLK*, and data sample signals. Routing data sample signals to each unitcell would not be practical due to a high number of signals needed for each **RF-DAC**. In the same way as in PalleonTX, for each of the data signals *EN<sub>H</sub>*, *EN<sub>L</sub>*, *PH<sub>H</sub>*, and *PH<sub>L</sub>*, signals of *row*, *col*, and *full\_col* are considered so that unitcells can be controlled with a minimum number of signal routings from the digital part to the frontends. Therefore, In order to determine the values of these four data sample variables, the custom-designed digital logic of each unitcell should also include four decoders to perform  $full\_col + col \cdot row$ . Sign signals *SI<sub>H</sub>*, *SI<sub>L</sub>*, *SQ<sub>H</sub>*, and *SQ<sub>L</sub>* are the same for all unitcells of the **RF-DAC**. As a result, there are in total 76 data sample signals routed in each column, which require the same number of buffers so that they do not cause timing problems due to propagation delays of connecting wires.

It is also important to shed light on how the unitcells are selected with each data sample. For **LSB** bits, it is straightforward as there are specifically 16 **LSB** unitcells for each of I and Q data. However, for the **MSB** data, 128 unitcells, numbered from 0 to 127, need to be

shared between I and Q. For this purpose, the I data selects unitcells in a chronologically increasing order from unitcell 0 while the Q data activates unitcells in a chronologically decreasing order from unitcell 127. In other words, the I data unitcell selection starts from column 0 and that of the Q data starts from column 7. In the case that more than 112 **MSB** unitcells shall be activated, one column is shared between I and Q data.

### 6.3.3 Layout and Implementation Considerations

As mentioned earlier, the layout of an **RF-DAC** frontend is a very important aspect to achieve the required performance out of it. Asymmetry and mismatch in the timing of signals can degrade the performance significantly as they introduce systematic phase offset for different unitcells. This becomes of great importance, especially when the **DAC** operates with higher carrier frequencies. Higher **LO** and data sampling frequencies imply that the same absolute timing mismatches degrade the performance further as they should be considered relative to the period of signals. Therefore, it is essential to design the layout in the best symmetric way regarding **LO** signals and **CLK**.

In order to get into the layout implementation of Chameleon, one should first have general information about the technology in which it is implemented. This transmitter system is designed in a 28-nm low-power technology, which is a high-performance and low-leakage technology with a core voltage of 1 V and I/O voltages of 1.8 V and 2.5 V. It allows for 1 layer of poly and 8 layers of copper metal with a metalization configuration of 1P8M\_5X1Z1U along with an Aluminum **ReDistribution Layer (RDL)** on top.

Clearly, in such a small technology node, digital circuitry would perform faster and occupy a much smaller area compared to the 65-nm technology in which **PalleonTX** is implemented. This is very advantageous for a digital-centric transmitter, which necessitates the use of many **DSP** modules. In particular, an **ML-LINC** transmitter imposes even more digital signal processing operations to calculate outphasing vectors in an efficient way. However, the design of analog circuits would be more challenging as transistor sizes shrink down in a new technology. For getting a better analog performance, the design rules and recommended guidelines, which would be more strict in smaller technologies as expected, should be followed so that the implemented circuit suffers less from the unwanted effects of technology shrinking.

In order to eliminate systematic mismatch in analog circuit design, both the devices and their surrounding environment should be identical [50]. A well-known technique to create an identical surrounding environment is to use enough dummy devices to fill the area around matched transistors in the same way. It is observed that in such a small technology node, it is very important to employ sufficient dummy fingers next to the outer fingers of a **MOS** device to keep its transconductance high enough. In the case, the number of similar dummy fingers is not enough, the outer fingers of a transistor

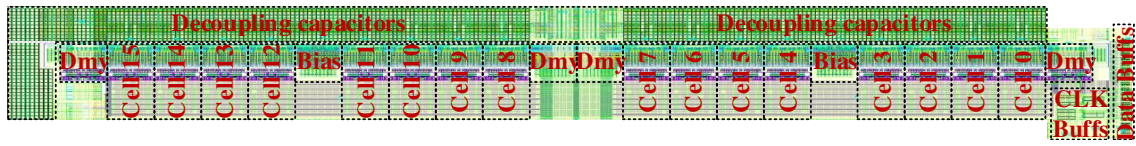


Figure 6.11: Layout of a column.

show smaller transconductance. Furthermore, these additional dummy fingers can also be used as MOS capacitors for decoupling between supply and ground.

### Column layout structure

Fig. 6.11 shows the structure of each column of the RF-DAC. By inserting symmetrically designed unitcells next to each other, the empty spaces are filled. In this way, in order to have identical surroundings for transistors of a unitcell, it is cared that the outer transistors of each unitcell have the same type of transistors with the same spacing next to them as other transistors that are not at the edge of unitcell. Furthermore, the bias circuits and the additional dummy cells are laid out very similar to unitcells except that their connections differ.

Data sample signals, which count to 76, are routed in parallel in a channel below the cells in Fig. 6.11 while 76 buffers drive them to meet their timing requirements as discussed earlier. Additionally,  $CLK$ ,  $\overline{CLK}$ , and  $LO$  signals are routed very low-ohmic with wide routings of metal layer M8. These signals are shielded with ground on metal layer M6 to reduce coupling to data sample signals, which are routed on metal layers M2 and M4. Due to limited space, it is not feasible to make a tree-shape symmetric clock and  $LO$  distribution routing. Instead, a wide width of  $2\ \mu\text{m}$  is applied for the routing of these signals across a length of  $560\ \mu\text{m}$  of a column while sufficient ground shielding layers are placed in between. These long clock lines are driven by 6 strong buffers, each driving around  $115\ \text{fF}$ , which is achieved by extracting RF-DAC columns. The clock lines are also simulated after extraction by an EM solver. The simulation result shows that in the worst case of SS corner with a temperature of  $-20\ ^\circ\text{C}$ , a maximum delay of  $0.6\ \text{ps}$  exists from  $LO$  signals at the inputs of the first unitcell to the inputs of the last unitcell of the column. This translates to a phase mismatch of around  $1.3^\circ$  at a carrier frequency of  $6\ \text{GHz}$  in the worst case.

On the output side, which can be seen on the top side of the column in Fig. 6.11,  $OUT_P$  and  $OUT_N$ , which are output nets of the RF-DAC, are routed with wide M8 tracks while shielded with M7. Additionally,  $V_{DUMP}$  and  $I_{BIAS}$  are routed under output nets on metal layer M4. A large number of decoupling capacitors are also placed on the upper side of the cells under the aforementioned routing layers of the output and supply nets on higher metal layers. Due to a lot of digital switching in the custom-designed logic circuits as

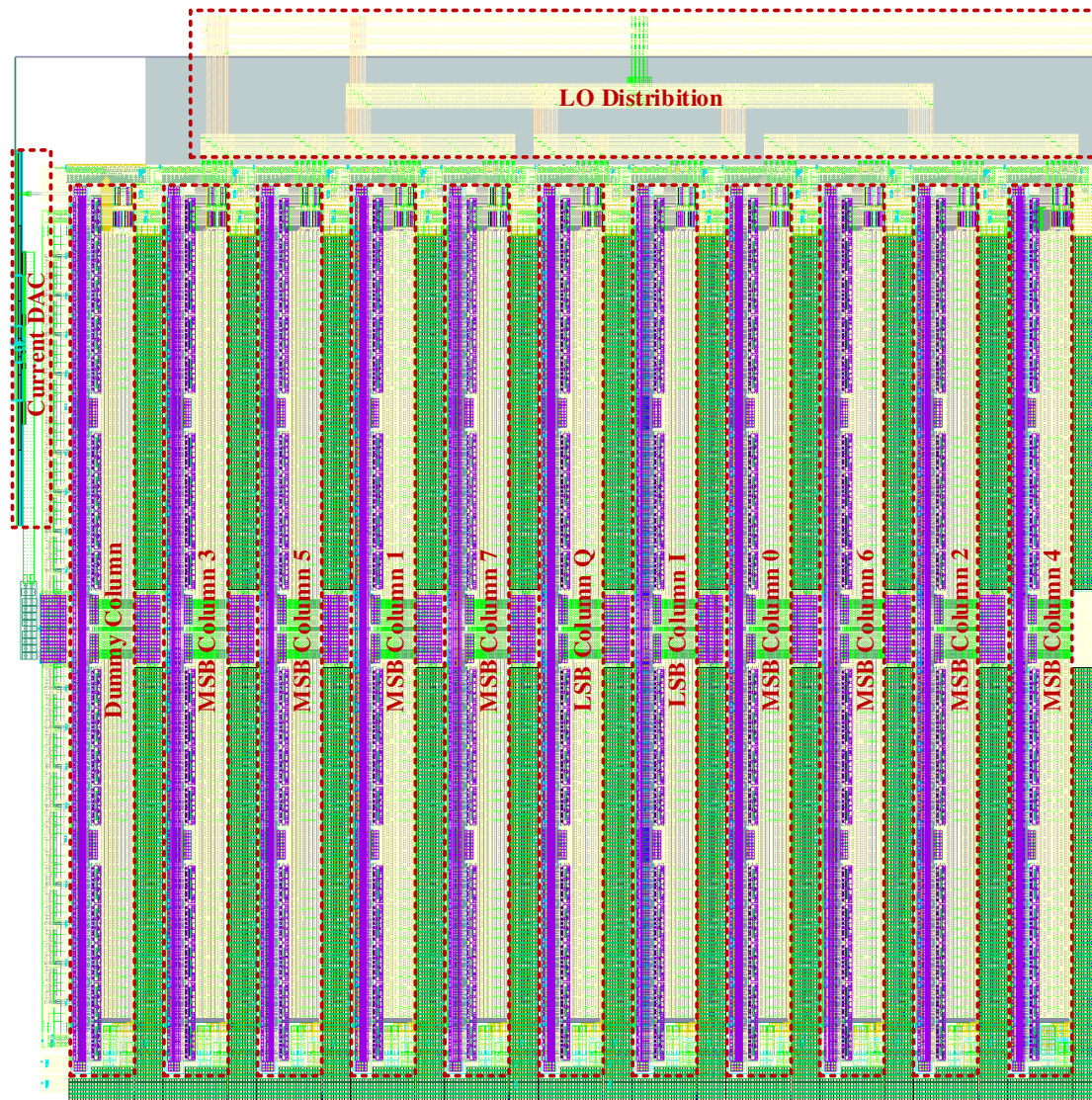


Figure 6.12: Toplevel layout of the RF-DAC frontend.

well as buffers, a considerable amount of switching noise is induced on the digital supply and this necessitates having big decoupling capacitors between  $V_{DD,Dig}$  and  $V_{SS,Dig}$ .

### Toplevel Layout

The final layout of the RF-DAC, which occupies an area of  $805 \mu\text{m} \times 785 \mu\text{m}$ , is presented in Fig. 6.12. All the 10 columns of the RF-DAC are placed next to each other. In order to arrange it more towards a common-centroid layout, the two LSB columns are placed in

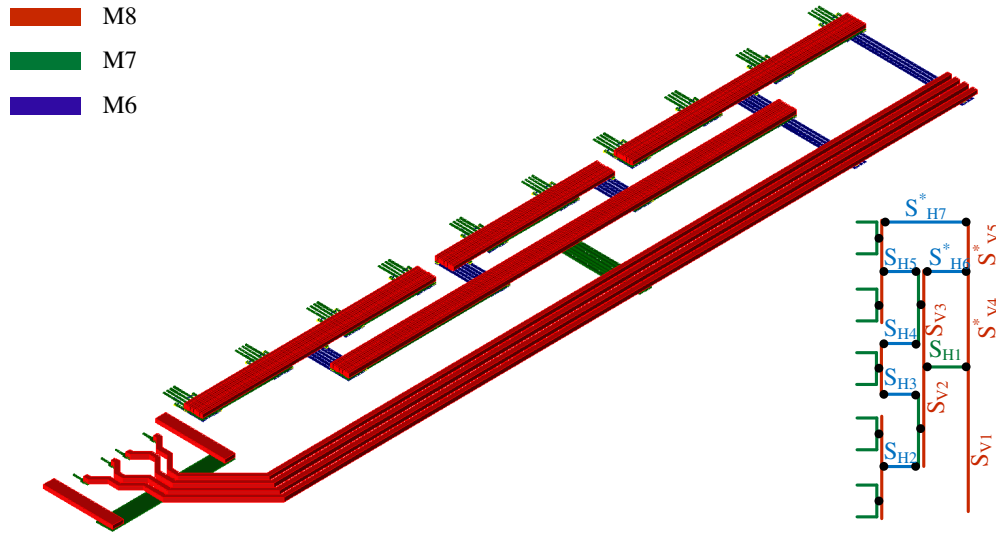


Figure 6.13: Toplevel input LO distribution of the RF-DAC frontend.

the middle, while the MSB columns are selected chronologically from the center. For the column selection, first, full columns of I and Q are considered. Columns are devoted to  $full\_col_I$  in increasing order from column 0 and to  $full\_col_Q$  in decreasing order from column 7. When all full columns are assigned, the next column in each direction is considered for the 4 less-significant bits of the MSB data. In case the sum of used full columns exceeds 7, only one column remains, which is used for both of the I and Q data together. Additionally, the programmable current DAC is inserted at the left side of the frontend and bias current is distributed across the current mirrors of each column.

An important aspect of the layout to be discussed here is the distribution of LO signals, which requires adequate care. Due to limitations imposed by the size of the chip, it is not possible to design a fully symmetrical layout with regard to LO signals and the outputs. However, it is attempted to achieve a distribution of these signals with minimum systematic mismatch introduced due to propagation delays. For this purpose, the LO tree shown in Fig. 6.13 is designed to deliver input LO signals and CLK signals from buffers of clock dividers to the clock buffers of all columns. Ignoring the segments named  $S^*$ , LO signals are delivered to the column buffers in a very symmetric manner resulting in the same parasitic resistance and capacitance across all paths. In other words, these signals would travel the same distance for all columns. However, due to Electromagnetic fields between segments, such as that of  $S_{V1}$  and  $S_{V2}$ , this does not hold. Through an experimental try and trial, it has been seen that by adding supplementary segments  $S_{V4}^*$ ,  $S_{V5}^*$ ,  $S_{H6}^*$ , and  $S_{H7}^*$ , a better LO signal routing can be achieved, where the phase mismatch of LO signals at LO buffers of columns is rather optimized.

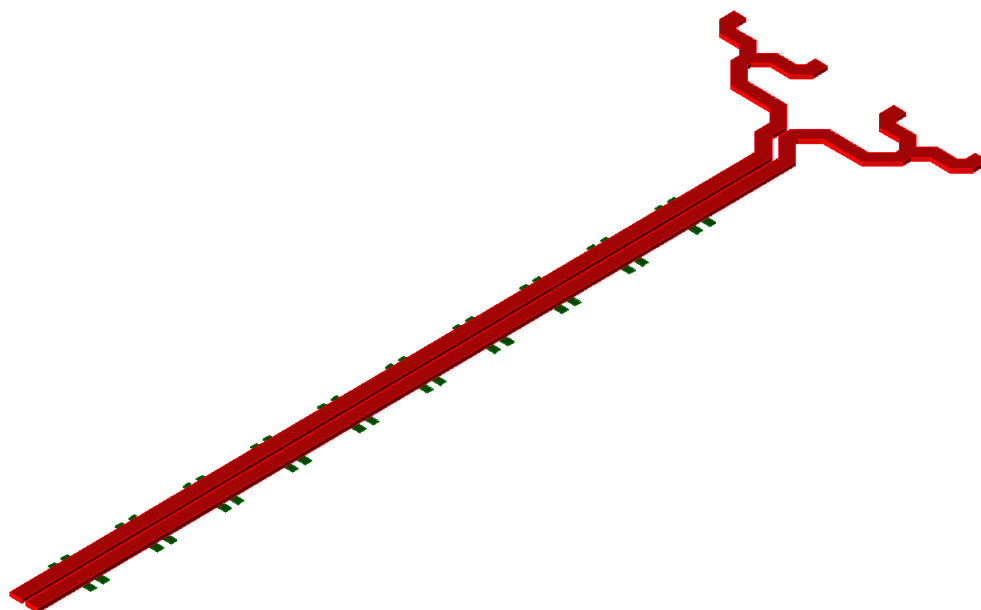


Figure 6.14: Toplevel differential output routing of the RF-DAC frontend.

In the middle of each column, a wide parallel track of M8 collects the differential output currents of columns and routes it to the output. This is depicted in Fig. 6.14. Two IO ports are dedicated to each of the output nets to reduce the undesired effects of the package and bond-wires. Furthermore the RF-DAC is placed as close as possible to these IO ports to reduce the routing distance.

### 6.3.4 Chip Integration and Validation Setup

The developed ML-LINC transmitter system is implemented in a Multi-Project Wafer (MPW) with a silicon area of  $2275 \mu\text{m} \times 1580 \mu\text{m}$  out of a die size of  $2488 \mu\text{m} \times 2948 \mu\text{m}$  where the bottom part of the die is used for another design. Fig. 6.15a presents a chip photo of the fabricated transmitter system. Two RF-DAC frontends are placed on top next to each other. On the right side of the chip, an on-chip balun is placed to receive a differential input clock up to 12 GHz. The output is fed to an LO divider that provides 4 phases of the LO signal, each with a duty cycle of 50%. To distribute these LO signals towards RF-DACs, a strong buffer is placed at the output of the divider, driving LO to the middle of the two RF-DACs. Another high-speed divider is designated to provide CLK\_FAST for the digital circuitry, which is located in the middle below the RF-DAC frontends. Additionally, a Power Management Unit (PMU), consisting of LDOs and bandgap reference generators, is integrated to provide the supplies that are required

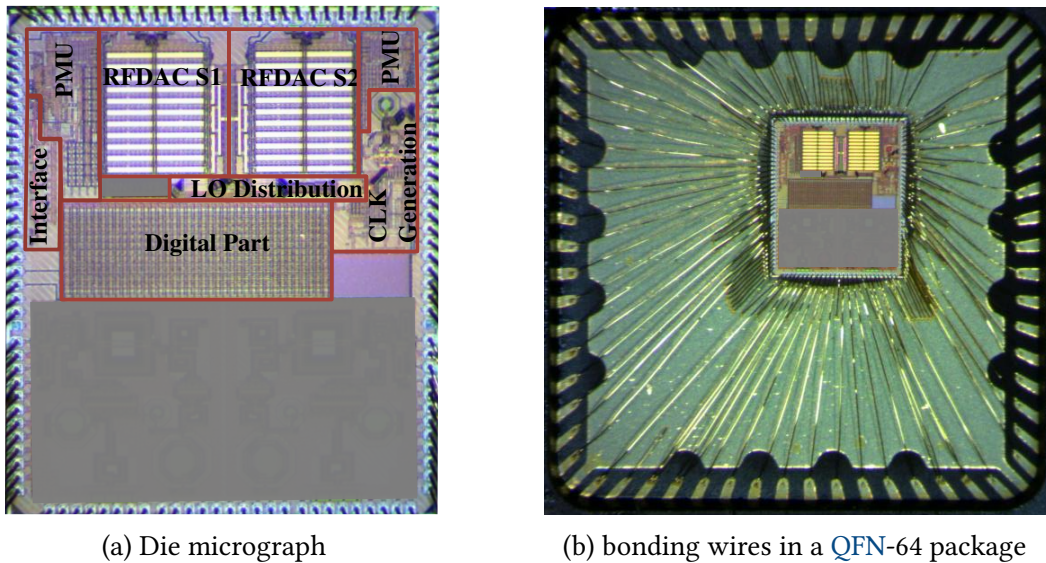


Figure 6.15: Photos of the fabricated Chameleon chip.

for the digital part as well as the LO distribution of the frontends. Fig. 6.15b shows the fabricated die within a QFN-64 package with its bonding wires. The die is shifted towards the output pads, similar to PalleonTX. This reduces the packaging parasitics and, most importantly, the bondwire inductance.

In order to begin the measurements, a number of received samples are mounted on test PCBs as in Fig. 6.16. The LO signal is given from the SMA pin on the right side of the board, where a balun is designated to convert it to a differential LO signal up to 12 GHz fed to the chip. On the left side of the board, one can see 12 pins for the CML inputs of the high-speed CAG/IOv2 interface with increased speed, which is discussed in section 4.1.1. A USB to serial UART conversion circuit for the backup UART interface is implemented on the bottom side. The RF outputs of the transmitter are routed towards a matching network on top of the PCB and then are given out through SMA pins. A second board is prepared to receive the outphasing RF signals, amplify them through PAs, and reconstruct the final RF signal in a power combiner.

## 6.4 Performance

With the layout implemented, a number of verification post-layout simulations are run to verify the performance of the implemented frontend and guarantee specifications required for the ML-LINC transmitter system. In order to find the optimum load of frontend and design a proper matching network, a load-pull simulation is run in the first place. The selected load should deliver sufficiently high power as required while

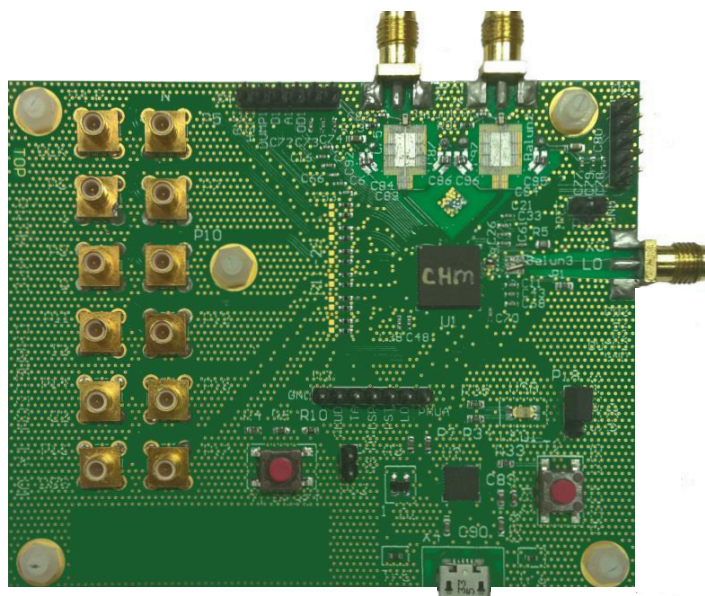


Figure 6.16: Test PCB of the Chameleon transmitter.

preventing noticeable AM-AM nonlinearity. If a larger output load is selected for the frontend, the peak power can be increased. However, a larger load leads to a more considerable attenuation of the output resistance when more unitcells are turned on, which increases the AM-AM nonlinearity. Furthermore, it is important to design the matching network so that the same peak power is delivered across the whole frequency band. The simulations show a peak power of around 12 dBm can be achieved, which is 4 dB higher than the required peak power of 8 dBm. Since such a higher peak power is not necessary for the requirement of this transmitter, one could select a load that results in a better frontend linearity with the cost of a reduced output power. Considering the loss due to the signal path through the PCB and the balun, a load is selected that delivers an output of 9.2 dBm with a maximum change of 0.02 dBm across the 5-GHz frequency band.

A first verification simulation is the linearity of the frontend across static input. For this purpose, harmonic-balance simulations are performed with a carrier frequency of 5.5 GHz while the digital input amplitude of the frontend is swept from 0 to 1448 and the I/Q phase is swept with steps of  $15^\circ$ . The result is shown in Fig. 6.17. The phase deviates, in the worst case, less than  $1^\circ$  from the target phase. However, for the phases that are multiples of  $45^\circ$ , this is smaller than  $0.5^\circ$ . The reason is the type of sweep applied here, which converts the amplitude and the phase to I and Q data by rounding to smaller integer numbers for each of them. In the real application, in case no DPD is employed in the SCS, the same result can be expected as there is a similar conversion from polar coordinates to cartesian coordinates. The amplitude might seem to be very linear at

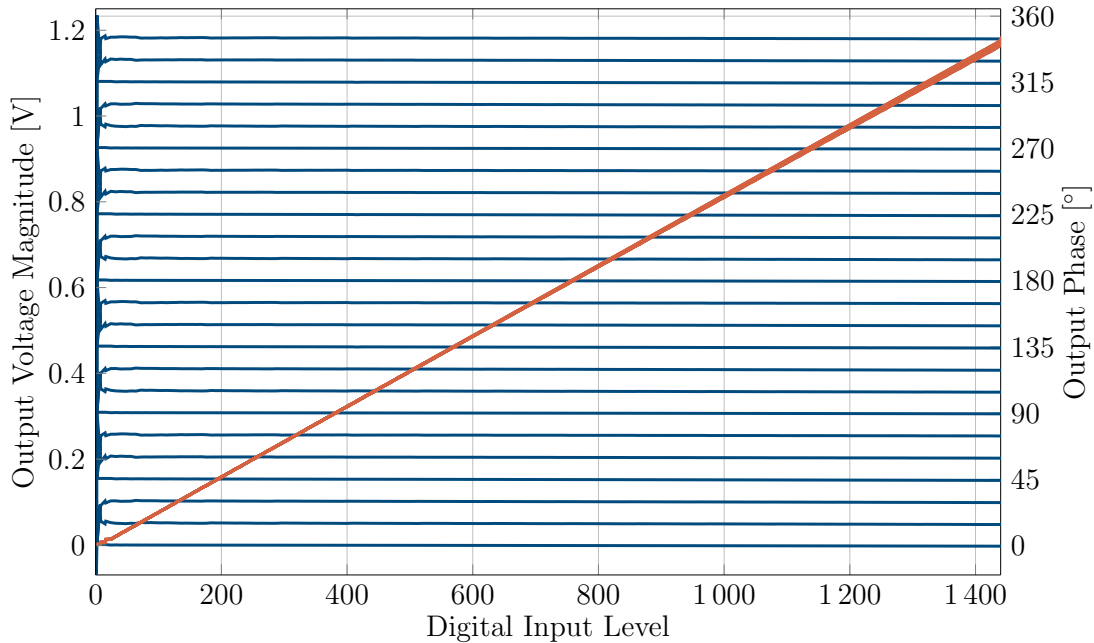


Figure 6.17: Static linearity of the frontend through amplitude and phase sweep at a carrier frequency of 5.5 GHz.

the first glance. However, it deviates from a linear line up to  $-0.14$  dB at the maximum power for the phases of  $45^\circ$ ,  $135^\circ$ ,  $225^\circ$ , and  $315^\circ$ , where the power I and Q power need to combine with a maximum interaction. For the phases of  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$ , and  $270^\circ$ , where only one of the phases of the LO signal goes to the output and there is no combination of I and Q data, this deviation at the maximum output is less than  $-0.05$  dB.

Another important performance measure that is discussed here is the SSB response of the frontend. To show a decent performance of this RF-DAC frontend, transistor-level simulations have been run for a 10-MHz sinusoidal with a maximum amplitude of 1448 at a carrier frequency of 5.6 GHz. For this purpose, the Cadence Spectre®RF simulator is used to converge into a periodic steady-state response. Clearly, the most precise result can be achieved with post-layout extraction of the frontend. However, due to a huge number of nets and, as a result, the netlist size with a extracted frontend, the simulation cannot converge within a reasonable time given the available resources. In order to reduce the simulation effort, the unitcells are post-layout extracted while the buffers and toplevel routings are taken as in the schematic. The result is presented in Fig. 6.18. A peak power of 5.5 dBm is achieved at the frequency of 5.61 GHz, while an image rejection of  $-57.3$  dB can be seen at 5.59 GHz. It can also be seen that the LO leakage is around  $-57.6$  dBm, which is pretty promising compared to what has been achieved in PalleonTX as well as in the literature. The nonlinearity of the frontend results in a  $3^{rd}$  order intermodulation product of  $-53.7$  dBc at 5.57 GHz. This is mainly

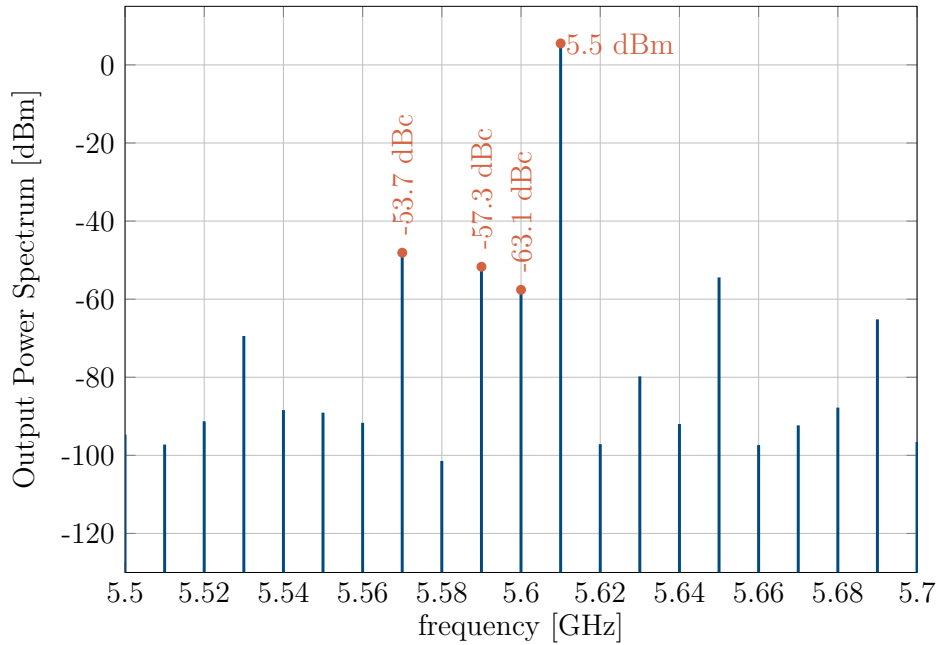


Figure 6.18: SSB performance of RF-DAC frontend with a 10-MHz sinusoid signal at a carrier frequency of 5.6 GHz.

there due to the AM-AM and AM-PM nonlinearity profile of the frontend.

In order to confirm the desired performance out of the transmitter, a number of efforts to measure the chip have been conducted. However, several attempts show that the transmitter system cannot be started up as desired. The issue has been further investigated to find the root cause. It is found out that the input LO divider is not functioning and draws a significant current. As a result, no LO is delivered to the frontend. Furthermore, CLK\_FAST is also not available to drive the digital part, which leads to an undefined state where no configuration bit can be adjusted through the interfaces. It is expected that the transmitter can be taped out again with a sufficiently robust LO interface, which results in a good-quality LO signal delivered to the RF frontend. This enables successful validation of the transmitter and confirming the promising results obtained through the post-layout simulations.



# Chapter 7

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## Conclusion

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In this work, the design and implementation of two **Digital-Centric Multi-standard Transmitters (DCMTs)** with different architectures and in different **CMOS** technology nodes are presented. The focus is mostly on the design of the **DDRC** frontend in order to achieve the desired system performance.

The thesis goes through the system, design, and implementation aspects of these transmitters. After a short introduction to the importance of digital-centric transmitters in Chapter 1, the basics of wireless communications are covered in Chapter 2. This provides a foundation for the next chapters and explains the important requirements of a transmitter system on which it shall be evaluated. The digital modulation schemes of **OFDM** for **WLAN**, as well as **OFDMA** and **SC-FDMA** for **LTE** require the transmitter to handle signals with a high **PAPR**. This dictates the need for a highly linear transmitter. **IEEE 802.11** standards require strict **EVM** performance, while **LTE** imposes more stringent requirements for out-of-channel emissions, i.e., **ACLR**. As a result, a multi-standard transmitter for **Software-Defined Radio (SDR)** needs to cope with all these requirements.

In order to provide a foundation of transmitter systems, Chapter 3 provides a survey of different architectures of transmitters with a focus on digital-centric ones. Starting with conventional analog-intensive transmitters, architectures of direct-conversion **IQ TX**, two-step **IQ TX**, envelope tracking, and polar **TX** are reviewed. Bulkiness and lack of flexibility of analog building blocks such as filters restrain these architectures from multi-standard operation within an affordable power, area, and cost budget. On the other hand, digital-centric transmitters benefit from the flexibility of digital signal processing as well as the effects of **CMOS** technology downscaling, including speed, area, and functionality. The core of such a transmitter includes a number of upsampling and digital signal processing steps that can be reconfigured according to the target standard, along with a **DDRC** frontend that performs both analog-to-digital conversion and upmixing to the carrier frequency at the same time. However, such a transmitter imposes a number of challenges, out of which the most important one is the lack of a reconstruction filter leading to replicas of the sampling frequency. There are three major architectures of digital-centric transmitters presented in this work. **IQ DCMTs** perform well for signals with larger bandwidths. Polar digital-centric transmitters require a fine phase modulator

and a high bandwidth of the frontends to be able to incorporate bandwidth expansion of polar coordinates. Last but not least, **ML-LINC** transmitters provide a high linearity through outphasing signals while requiring high-bandwidth frontends just like the polar architecture.

The digital building blocks of the transmitters of this work are presented in Chapter 4. First of all, a high-speed interfaces is needed to transfer the stream of data samples directly from the external baseband generator to the **RFIC**. For this purpose, the **CAG/IOv2** high-speed interface for 12-bit data samples is adapted from older designs. Using **LVDS** signaling, it can achieve data rates up to 2 Gbps per lane for each of the I and Q data streams, which translates to sampling rates up to 100 MHz for baseband data considering 4 additional header bits and 8b/10b encoding. In order to be capable of transferring data with sampling rates up to 200 MHz for standards with higher data rates such as 160-MHz channels of **IEEE 802.11ac**, another version of this interface is additionally developed in this work by using 2 lanes for each of the I and Q data. The received data is then upsampled in two steps. First, a **Pulse-Shaping Filter (PSF)** upsamples the data with an **Arbitrary Sampling-Rate Conversion (ASRC)** to an intermediate frequency where signal processing steps can be applied and then a **Cascaded Integrator-Comb (CIC)** filter upsamples the data to the final sampling rate before upmixing through the frontend. The **PSF** can perform upsampling with an integer ratio of 5 and fractional ratios between 4 and 5, while it has an order of 16 requiring 80 **FIR** coefficients. At the resulting intermediate frequency, a number of signal processing steps are carried out to compensate for the imperfections of the frontend. **LO** feedthrough is compensated with a shift in the IQ plane origin, IQ gain mismatch is corrected with gain stages in the path of each of I and Q data, and last but not least, IQ phase mismatch is canceled out by adding a fraction of I data to the q data or vice versa. Furthermore, a 2-dimensional **Digital PreDistortion (DPD)** module is implemented through an **LUT** of size  $N = 2^{12}$  to compensate for both of the AM-AM and AM-PM nonlinearities due to a finite output impedance of the **DDRC** frontends. After compensation of the frontend imperfections, the 4<sup>th</sup>-order **CIC** filter handles integer upsampling to the final sampling rate while an additional fractional boost stage is also included to minimize power degradation after truncating bit growth. Next, an **Element Selection Logic (ESL)** determines which unitcells of the frontend to use for each data sample. It has the capability of applying **Data-Weighted Averaging (DWA)** or **Reduced-Activity Data-Weighted Averaging (RA-DWA)** to randomize unitcell mismatches and average them out.

**PalleonTX**, a 12-bit IQ digital-centric transmitter with a 25 % duty cycle **LO**, is introduced in chapter 5 and its architecture and implementation as well as its measurement results are presented. The transmitter is implemented in a 65-nm **CMOS** technology with a supply voltage of 1.2 V. The digital part receives two parallel streams of data for In-phase and Quadrature components in the baseband domain and these are processed and upsampled to a division of carrier frequency. The output of digital drives two **DPA** frontends with a 90° phase shift, which perform similar to an IQ mixer in conventional

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analog transmitters. The frontend consists of 128 unitcells of **MSB** in the shape of 16 columns, each with 8 unitcells and 15 binary-weighted **LSB** unitcells, which results in an overall amplitude resolution of 11 bits for each of the I and Q data. The sign bit forms the 12<sup>th</sup> bit of the input data, which switches the polarity of the **LO** data accordingly. An external **LO** clock with a double frequency is fed into the chip while an **LO** divider divides it by 2 and generates 4 phases, each with a duty cycle of 25 %, which improves the efficiency of the transmitter compared to a similar transmitter with a 50 % duty cycle.

The **PalleonTX** transmitter is first validated through an **SSB** signal. It can achieve a power of 6.7 dBm with an **IRR** of 49.9 dB. However, the **DPA** frontend lacks sufficient linearity, which causes an **IM3** product of -23.2 dB. For a better linearity, digital power control is applied to reduce the output power to 1 dBm, which results in an **IRR** of 38.2 dB and an **IM3** of -35.9 dB. The validation of **PalleonTX** is followed by a **WLAN** transmission test with a 20-MHz **OFDM 64-QAM** signal at channel 1 of the 2.4-GHz band. The **TX** can achieve an **EVM** of 5.32 % with a burst power of -4.75 dBm. The resulting drain efficiency is 13.43 % and its system efficiency is around 0.54 %. In spite of a number of shortcomings, the transmitter can achieve the requirements of a **WLAN** transmission as expected. Also, this proof-of-concept design successfully demonstrates that the use of 25 % **LO** signals can improve drain efficiency compared to **UMIC TX3** [8], which uses a 50 % **LO** duty cycle with a pretty similar architecture.

There is a lot of room for improvement of **PalleonTX** for a future design. The **DPA** frontend lacks sufficient linearity. One important reason is the finite output impedance and its change at higher amplitudes. Since the capacitance dominates at the frequency of operation, the change of the output capacitance through activating a number of unitcells needs to be minimized. In a next design, more attention shall be paid to the output impedance of such a current-steering **DDRC** frontend. Furthermore, the digital implementation flow used in this work, particularly the integration of a custom-designed **SRAM**, does not allow a complete **LVS** check on the toplevel, which led to false connections of control signals of **MSB** unitcells. Since the columns of **MSB** cells need to be consecutive, only 5 **MSB** columns can be used, which results in a maximum of 655 unitcells in total. This limits the resolution to 9 bits. Also, lack of continuity prevents **DPD** and **DWA** from being employed in order to improve the effects of nonlinearities and mismatches in the design. In the absence of a sufficiently high output impedance of the frontend, a **DPD** could improve the overall transmitter linearity significantly. In future designs, it shall be guaranteed that sufficient verification with a right design flow prevents such problems. Also, the system efficiency can be increased, by improving the power consumption of clocks and **LO** drivers of the frontend. Since the design size is not optimized due to design time limitations, quite strong buffers are adopted to drive large routings of the **LO** signals. This helps to provide the **LO** signals with a minimum timing deviation across the frontend. However, it comes with the cost of a significantly higher power consumption.

Chapter 6 presents the system concept, design, implementation, and simulations of an **ML-LINC** transmitter called Chameleon, with a focus on the design of its **RF-DAC** frontends, which shall provide high linearity for advanced wireless standards such as 5G. Such a transmitter generates two outphasing signals with sufficiently small outphasing angles and reconstructs the desired output vector by combining them in the **RF** domain. The system consists of a digital signal processing block where the I and Q input data are received and processed from an off-chip **BBIC** or **FPGA**. A number of upsampling and signal processing steps are applied to convert these signals to a sufficiently high sampling rate in the **LO** frequency domain, which is an important requirement of **DCMTs**. A **Multi-Level Signal Component Separator (ML-SCS)** converts the IQ signal into phase and amplitude of polar coordinates and generates outphasing signals accordingly. The outphasing signals are converted into Cartesian coordinates and are upconverted to the **RF** band by means of two separate **RF-DAC** frontends. The upconverted outphasing signals are then combined in a power combiner in the **RF** domain to reconstruct the desired transmit signal.

According to the requirements specified for this transmitter, a number of system simulations are performed to resolve the requirements of each building block. Most importantly, it is established that an I/Q unitcell-sharing **RF-DAC** with a 12-bit resolution and a unitcell tail current of 15  $\mu\text{A}$  can achieve the required performance. As a result, an **RF-DAC** is developed, which consists of a 4-bit binary-weighted **LSB** part and a 7-bit unary-weighted **MSB** part besides a 1-bit **LO** sign switching. The design is implemented in a 28-nm **CMOS** technology node with a supply voltage of 1 V. The most challenging part of this work is to design the **RF-DAC** frontends, which should achieve the performance metrics required for the targeted standard. Boolean equations for the target unitcells are achieved and current steering unitcells are designed accordingly where important aspects such as output impedance and matching are taken into consideration. It is also ensured that unitcells have the capability of switching between I and Q output without significant latency. Besides, special attention has been paid to the toplevel architecture and layout of the **RF-DAC** frontend. It is implemented in the form of 10 columns, each with 16 unitcells. The two columns in the middle are considered for the **LSB** unitcells of the I and Q data while the rest are considered for **MSB**. One important aspect of the frontend design is the distribution of the **LO** signals and the routing of outputs to minimize the phase difference between signals from different unitcells at the output of the **RF-DAC**. For this purpose, optimized **LO** trees have been developed to deliver the signals as symmetrical as possible and have been verified through **EM** simulations. Simulations demonstrate that the **ML-LINC** transmitter can achieve the required functionality and performance. However, validation cannot be carried out due to an issue in the primary **LO** divider at the input of the chip.

In order to develop such a system further, one could bring the off-chip components, including the **PAs** and the power combiner, on-chip. Taking outphasing signals off-chip might introduce mismatches on the PCB as they need to go through the package, the

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PCB, and the matching networks as well. The losses introduced through this path can add to the mismatch between the outphasing vectors.



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## Curriculum Vitae

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10/2013–12/2013	RWTH Aachen University, Aachen Integrated Analog Circuits and RF Systems (IAS) Student Assistant
12/2012–02/2013	Technical University of Munich, Munich Institute of Technical Electronics (LTE) Student Assistant
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### Education

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