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TECHNICAL REPORT

# Irradiation tests of the OBDTv1 board at CHARM

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Abstract: The CMS Muon Drift Tube (DT) chambers require an upgrade of their on-detector electronics for operation in the High Luminosity LHC (HL-LHC) due to increased radiation, occupancy and trigger rates. The new On-Detector Board for Drift Tubes (OBDT) digitizes drift signals with a resolution of 0.8 ns and transmits them via high-speed optical links into the counting room, where the full detector information will be available to perform the trigger and event building logic. The prototype, OBDTv1, featuring a Microsemi PolarFire FPGA, underwent radiation testing at CERN's CHARM facility to validate its resilience in a full system test. Results confirmed the FPGA's robustness and also confirmed that the cross-sections obtained are comparable in reference tests and for the full final firmware. Few manageable Single Event Upsets (SEU) translate into rates below 0.24 SEUs/day in the full detector during operation at HL-LHC, ensuring reliable data acquisition. Resilient performance of all of the other components from the OBDTv1 board was also confirmed. The final OBDT will replace GBTx with lpGBT for enhanced speed and will use VTRX+ as optical transceivers, all of them radiation tolerant. Therefore, the results presented here demonstrate the readiness of the OBDT design for HL-LHC deployment.

Keywords: Front-end electronics for detector readout; Radiation damage to electronic components

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## Contents



## 1 Introduction

The on-detector electronics of the CMS Muon Drift Tube (DT) chambers [1] must be replaced for operation in the High Luminosity LHC (HL-LHC) [2] due to the increased occupancy and trigger rates, which exceed the capabilities of the current system [3]. The central component of this upgraded system is the On-Detector Board for Drift Tubes (OBDT), which is responsible for the time digitization of signals from the Drift Tube chambers signals for further transmission to the new Readout and Trigger electronics, which are located off-detector.

A total of 830 boards will be deployed to read out the 172,200 DT channels. The OBDT boards will be installed within aluminum profiles attached to the DT chambers, located inside the inner CMS wheels. Due to this placement, access for maintenance or repair will be highly restricted. These boards will measure incoming drift signals requiring a time resolution better than the $\sim 4$ ns time resolution of each individual drift cells. However, combination of drift cells allows to improve the timing and geometrical resolution by close to a factor 3, thus, the calibration of the time of flights and cable lengths needs to achieve resolutions at least 1.3 ns. The new electronics has been designed to use the same time bin as legacy ASICs (0.8 ns). This will allow a direct substitution of one system with the new one, being either case a time resolution well within the new electronics capability. To minimize the risk of information loss, no signal filtering or data reduction will be performed at the OBDT level. Instead, data will be multiplexed and transmitted via high-speed optical links. Additionally, the OBDTs will manage slow control tasks for the DT chamber system. The installation of this new system is scheduled for the LHC Long Shutdown 3 (LS3), planned for 2026–2029, just prior to the HL-LHC operational phase.

The region where the OBDTs will be installed is relatively shielded, as they are embedded within the steel of the yoke, which provides the return path for the CMS magnetic field. These radiation levels do not impose widespread use of radiation-hard ASICs. Nevertheless, all commercial components intended for use must undergo prior validation, given that future replacement or repair is highly impractical.



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Table 2 provides a summary of the radiation field expected throughout HL-LHC in the areas of the DT detector experiencing the highest doses and fluences. This radiation environment, characteristic of the LHC, is challenging to replicate accurately in most radiation testing facilities.

Several stages of prototyping for the OBDT board have been completed, including the development of the OBDTv1 [4], which was designed to digitize 240 DT channels and incorporated the final FPGA intended for use (Microchip PolarFire [5]). Although a radiation-tolerant version of this FPGA (RTPF500T) exists, the commercial-grade version was selected and tested. The primary difference between the OBDTv1 and the final OBDT design lies in the transceiver and optical chain, which were selected based on availability during the design phase. However, since the transceiver and optoelectronics intended for the final design are expected to be radiation-tolerant, the tests presented here will complete the validation of components for the final OBDT.

The radiation campaign took place at the CERN High-energy AcceleRator Mixed field (CHARM) [6] facility at CERN. This facility has a radiation field that is generated through the interaction of a 24 GeV/c proton beam extracted from the Proton Synchrotron (PS) with a metallic target and allows testing large scale systems. Our system was installed in an overhead conveyor inside CHARM which allowed to obtain a mixed-field radiation environment that resembles the one expected in the CMS experiment during HL-LHC [7].

## 2 The OBDTv1 board

The OBDTv1 board is based on a MicroSemi PolarFire FPGA (MPF300T-1FCG1152E), which digitizes up to 240 input signals, providing both coarse and fine time measurements for each signal. The coarse measurement is performed using a 12-bit counter driven by the 40.078 MHz LHC clock, corresponding to a time resolution of 24.95 ns per count. The dynamic range of the counter is reduced from 4096 to 3564 to ensure synchronization with the LHC orbit.

To achieve a fine time measurement, a dedicated firmware module is implemented for each of the 240 differential input channels. These dedicated modules operate at 640 MHz in DDR (Double Data Rate) mode, utilizing both the rising and falling edges of the clock signal, effectively achieving a sampling rate of 1.2 GHz. At this speed, the input signals are sampled to detect either a low or high level in time intervals of 0.83 ns. Using filtering logic, as a rising edge is identified, and the corresponding bit stream is encoded in up to 5 bits to represent the fine time measurement.

The coarse and fine time measurements of each signal are combined with the corresponding channel number to generate a 25-bit digital word. All time measurements are referenced to a periodic signal known as BC0 (Bunch Crossing 0), which is received externally and marks the start of an LHC orbit.

These digital time measurements performed by the OBDTv1 need to be merged into an output serialized stream that is sent through dedicated high speed optical links to the CMS DT backend.

Communication to and from the OBDT is implemented through two distinct methods. The first is the Slow Control link, which manages the reception of the LHC clock as well as configuration and monitoring commands. This link is bidirectional and uses transceiver ASICs specifically designed by CERN, that are guaranteed to be radiation tolerant. Due to its availability during the design phase, the Gigabit Transceiver (GBTx) [8] transceiver has been employed in the OBDTv1, while the final board is expected to use the Low Power Gigabit Transceiver (lpGBT) [9]. The use of this external transceiver instead of the internal FPGA´s transceivers, will allow performing remote reconfiguration of the Polarfire firmware.



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Conversely, the Readout links, responsible for transmitting the time digitization data, are implemented using the high-speed internal transceivers of the FPGA running at 10.24 Gpbs. The use of these transceivers facilitates having larger bandwidth by increasing the number of links without requiring additional external components.

In the final board both the Slow Control and Readout links will utilize radiation-tolerant optoelectronics developed by CERN. The intended module is the VTRX+ [10], designed to interface with the lpGBT. However, since the VTRX+ was not available during the design phase of the OBDTv1, commercial optoelectronic modules were used for this prototype. These commercial modules are not intended for the final OBDT board.

Another CERN ASIC utilized in the OBDTv1 is the SCA [11], which is responsible for monitoring voltages, currents, and temperatures. This device also supports the I2C protocol required for the gas pressure monitoring and alignment systems and facilitates the generation of calibration signals for the DT chamber. Proper level conversion of I2C lines is performed with dedicated circuits where required.

The OBDTv1 board is powered by two distinct sources to accommodate the significant differences in current consumption. A 5 V supply powers the calibration signals and I2C communication, with a current consumption of 0.8 A, while a 3.3 V supply powers the remaining components, with a current consumption of approximately 2.4 A. Several additional voltages required for the board's operation, including 2.5 V, 1.8 V, 1.5 V, and 1.05 V, are derived from the 3.3 V rail.

The architecture of the OBDTv1 board is shown in figure 1, while photographs of the board are presented in figure 2.

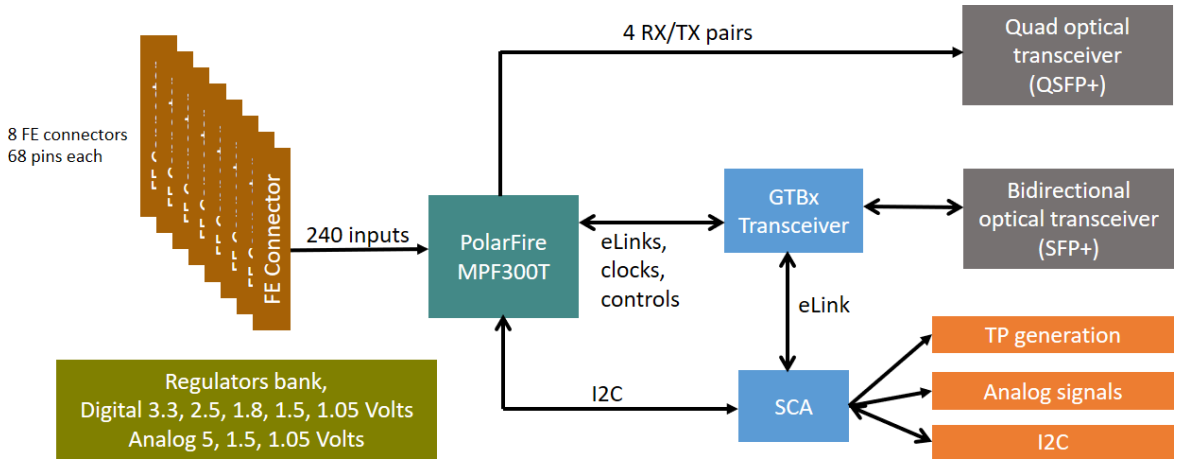


**Figure 1.** Drawing of the OBDT functionality and main components.

## 3 The test setup at CHARM

The radiation test setup consisted of two OBDTv1 boards with different firmware configurations, interconnected to transmit signals from one board to the other. The board running firmware similar to the design intended for HL-LHC operation is referred to as the OBDT. The second board, called PUlse Forwarding to OBDT (PUFO), was programmed with firmware dedicated to generating pulse hits, which were transmitted through 117 differential output channels to the input connectors of the OBDTv1. These pulses were sent periodically and synchronized with a reference signal occurring



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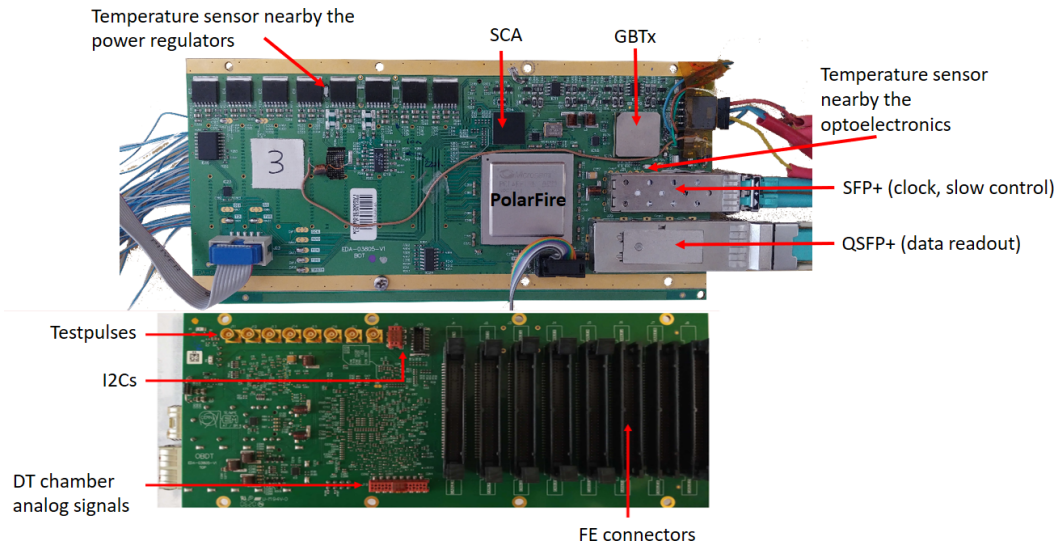


**Figure 2.** Image of the OBDTv1 board top and bottom.

once per LHC orbit (~ 11 kHz). Due to the use of High-Speed Input/Output (HSIO) bank pins in some of the PolarFire channels, it was not possible to generate LVDS outputs through those channels, limiting the number of utilized channels to 117 out of the 240 available.

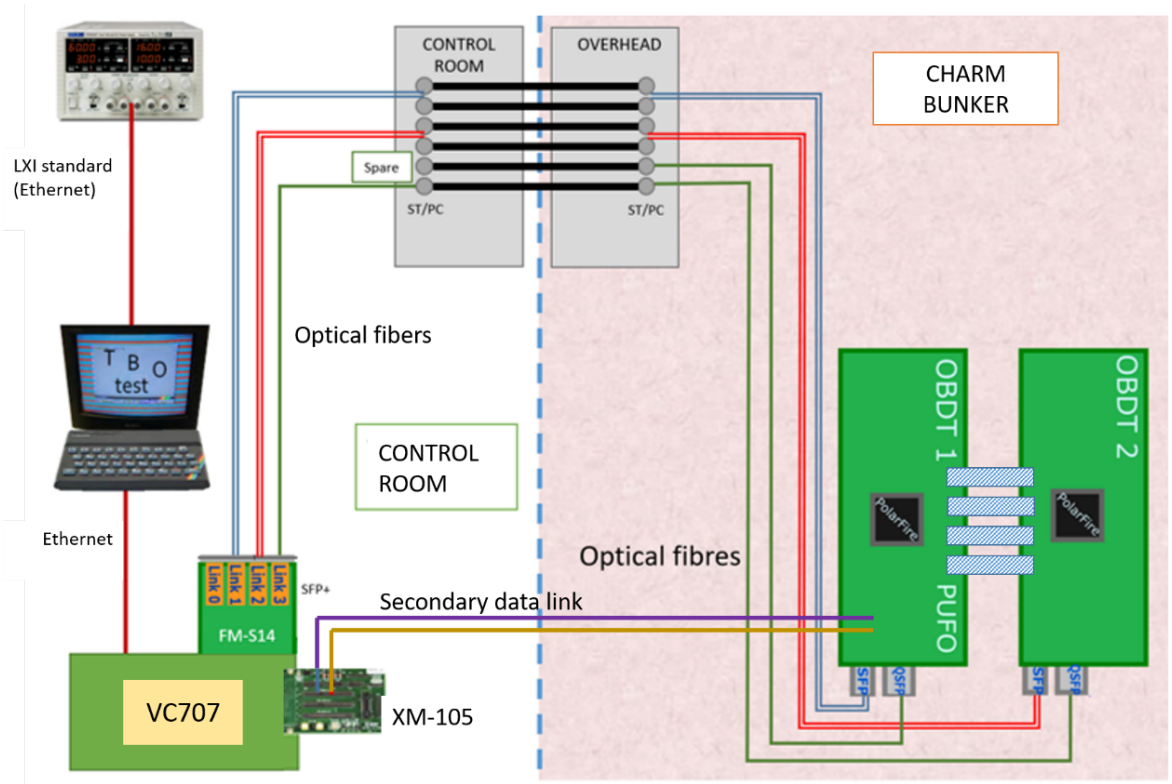


**Figure 3.** Drawing of the Test stand interconnections for the main test. OBDT and PUFO are located inside CHARM while VC707 is in the Control Room.



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A Xilinx VC707 evaluation board [12], equipped with a Faster Technology FM-S14 optical extension FMC board [13], was used to generate the system clock and manage slow control and monitoring of the entire setup via multiple optical links. Both boards were positioned outside the irradiation bunker. Figure 3 shows the electrical schematic detailing the architecture employed in this test.

The VC707 evaluation board receives the data stream from the OBDT board, which contains the time measurement information of the hits detected by the OBDT. Any discrepancies in the number of hits, their time values, or the associated channel information are flagged as errors. The total number of detected errors in the data stream is computed both internally by the OBDT and externally by the VC707 to enable cross-verification.

To ensure proper operation of the system even in the event of optoelectronics failure during testing, we included a copper link that guarantees communication with the FPGA and secure the acquisition of results. This custom electrical link allowed the measurement of the firmware Single Event Effects (SEUs) independently from the Bit Error Rates (BER) of the optical path.

**Table 1.** List of some of the main components that are part of the OBDTv1 and PUFO boards and that have been irradiated during this campaign.

| Part number | Manufacturer | Package | #/OBDT | Function |
|---|---|---|---|---|
| MPF300T-1FCG1152E | MICROSEMI | BGA1152 | 1 | PolarFire FPGA, 512 I/O, 300000 Logic Elements,1152-Pin FBGA, Extended Commercial Grade |
| MT25QL01GBBB8ESF-0SIT | MICRON TECHNOLOGY | SOIC16 | 1 | 1Gbit (128MB), 1.8 V, Multiple I/O Serial Flash Memory |
| SN74LVC2T45DCTT | TEXAS INSTRUMENTS | TSSOP8 | 1 | Dual-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs |
| LTC2052HVCS#PBF | LINEAR TECHNOLOGY | SOIC14 | 1 | Quad Zero-Drift Operational Amplifier |
| MM3Z5V6B | ON SEMICONDUCTOR | SOD-323F | 1 | 5.6 V 200 mW Zener Voltage Regulator |
| MM3Z12VB | ON SEMICONDUCTOR | SOD-323F | 1 | 12 V 200 mW Zener Voltage Regulator |
| 1N5819 | FAIRCHILD SEMICONDUCTOR | DO-41 | 3 | 40 V 1 A Schottky Barrier Rectifier |
| FXL4TD245BQX | ON SEMICONDUCTORS | QFN16 | 4 | 4-Bit Low-Voltage Dual-Supply Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-STATE Outputs |
| MIC69502WR | MICROCHIP TECHNOLOGY | S-PAK-7 | 8 | Adjustable Low VIN, Low VOUT LDO Regulator |
| P0K1.1206.2P.A | IST (INNOVATIVE SENSOR TECHNOLOGY) | 0805 | 2 | −50°C to 150°C, 100 Ohm at 0°C, SM Platinum Temperature Sensor |
| LM340MP-5.0/NOPB | TEXAS INSTRUMENTS | SOT223 | 1 | 5 V, 1 A Positive Voltage Regulators |
| GBT-SCA_REV 6.2 | CERN | BGA196 | 1 | Slow Control Adapter ASIC for the GigaBit Transceiver ASIC (GBT) |

Additionally, errors detected by the VC707 through the GBT link protocol, which includes an auto-correction mechanism, are recorded to determine the Bit Error Rate (BER) of the links. Furthermore, the VC707 monitors additional parameters of the OBDTs and PUFO, including voltages, currents, and temperatures.



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The operation of the set-up could be done fully remotely. A custom Python program was developed to manage monitoring and control, enabling configurations, power cycling and other operations. A continuously running routine monitored the status of the boards, logging the data to files and providing real-time status updates through a web interface.

At a maximum power consumption of 2.4 A, the OBDT requires cooling to maintain its temperature below 45°C. In the CMS environment, where the boards are embedded inside the CMS wheels and no air flow exists nor heating is allowed inside the detector, a water cooling system is needed to dissipate heat. At CHARM, two fans were incorporated into the setup to provide cooling with built-in redundancy.

Table 1 summarizes the list of integrated circuit part numbers from the OBDTv1 that were tested during the radiation campaign. Components not intended for use in the final OBDT but included in the validation are also identified.

### 3.1 FPGA SEUs monitoring specific logic

In addition to monitoring the expected OBDT firmware logic during the experiment, a dedicated firmware module was integrated into the Polarfire to enable a comparative measurement of the SEU rate, following methodologies outlined in the FPGA Radiation Test Guidelines [14]. The basic sensitivity of flip-flops to SEUs was evaluated using shift registers, which assess the chain output for the expected bit pattern. This logic was clocked continuously and errors were logged. The implemented logic comprised four flip-flop chains:

- FF All 1s: a chain where a logic "1" is propagated through 4096 flip-flops. Any deviation from the expected "1" is reported as an upset.
- FF All 0s: a chain where a logic "0" is propagated through 4096 flip-flops. Any deviation from the expected "0" is reported as an upset.
- CKBRD 40 MHz: an alternating data checkerboard pattern (1010101) is propagated through a chain of 4096 flip-flops clocked at 40 MHz. Any deviation from this pattern is recorded as an error.
- CKBRD 10 MHz: an alternating data checkerboard pattern (111100001111000011110000) is propagated through a chain of 4096 flip-flops clocked at 10 MHz. Any deviation from this pattern is recorded as an error.
- LSRAM: errors were monitored in 17-bit words stored in a 217 — position RAM. Memory addresses were written as values within the memory, and errors were detected by continuously scrubbing the entire RAM.

## 4 Results from the radiation tests

The dosimetry at CHARM includes the dose and the fluences and is obtained by a detailed calibration performed by the facility managers using the RadMon system [15]. Table 2 summarizes the total dose and particle fluence after the irradiation at CHARM as well as the dose and fluences expected at the location of the DT electronics. As shown, the radiation field significantly exceeds the expected levels for the OBDTs at the HL-LHC in terms of charged particles, neutrons, and total dose. The irradiation was performed with safety margins incorporating factors between 20 and 50 with respect the requirements.



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The irradiation period lasted 9 days, was performed using the copper target, and was divided into two periods with different shielding conditions. A first period where the shielding configuration included a block of iron and another one of concrete and a second period, with no shielding at CHARM. A total dose of 109.8 Gy was collected.

**Table 2.** Total dose and fluence received at CHARM during the irradiation and maximum dose and fluences expected at the location of the DT electronics in CMS after10 years of HL-LHC.

| **CHARM IRRADIATION** | |
|---|---|
| Dose (Gy) | 109.8 |
| High Energy Hadrons fluence ($cm^{-2}$) | $3.33\ 10^{11}$ |
| ThN fluence ($cm^{-2}$) | $6.37\ 10^{11}$ |
| 1MeVneq fluence ($cm^{-2}$) | $1.89\ 10^{12}$ |
| **DT ELECTRONICS AFTER HL-LHC** | |
| Neutrons $E > 100$ keV ($cm^{-2}$) | $8.9\ 10^{10}$ |
| Neutrons 1 MeV equivalent ($cm^{-2}$) | $9.8\ 10^{10}$ |
| Neutrons $E > 20$ MeV ($cm^{-2}$) | $1.87\ 10^{10}$ |
| Charged Hadrons ($cm^{-2}$) | $7.9\ 10^{8}$ |
| Total for SEE ($cm^{-2}$) | $1.95\ 10^{10}$ |
| Dose (Gy) | 2.10 |

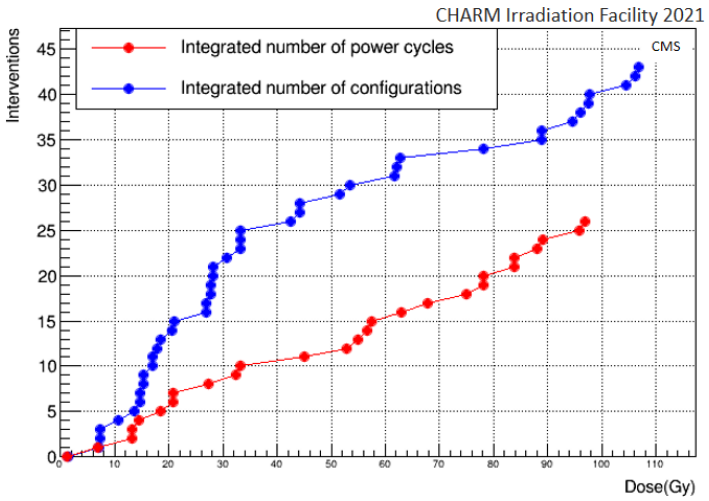


**Figure 4.** The accumulated number of power cycles and reconfigurations performed during the irradiation in both the OBDTv1 and PUFO board is presented.

The total number of power cycles and reconfigurations performed during the test is presented in figure 4. The power cycles are categorized into two types:

- Interventions: a total of 17 interventions were performed to recover from failures in commercial optical transceivers. These failures occurred when the link became unstable, resulting in incorrect data transmission. While some issues were resolved through board reconfiguration, the majority required a power cycle followed by a subsequent reconfiguration.



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- Shifter Actions: actions carried out by shifters to verify the system functionality, unrelated to any system malfunctions.

### 4.1 Results from the power supply distribution

The currents for the entire setup were measured via the power supplies for both the 5 V and 3.3 V rails. Monitoring was limited to the combined current of the OBDT and PUFO boards for each rail. The measured currents over the testing period are presented in table 3. Both currents exhibited a monotonic increase over time. This behavior has been previously observed during irradiation of similar regulators. On average, this corresponds to a system-wide current increase of approximately 3%, consistent across both power rails which will be imperceptible for DT at HL-LHC.

**Table 3.** Average variation of the test stand currents throughout the irradiation period. Note that the currents refer to the sum of both the OBDTv1 (2.4 A, 0.8 A) and the PUFO board (1.7 A, 0.8 A).

| | **3 V current** | **5 V current** |
|---|---|---|
| Current at the beginning of the irradiation | 4.127 A | 1.653 A |
| Current at the end of the irradiation | 4.256 A | 1.705 A |
| Total current increase | 129 mA | 52 mA |
| % current increase | 3.13 | 3.15 |

The linear regulators on the OBDT board generate various voltages, with the 1.05 V supply being used by the PolarFire FPGA. The trends for these voltages during the irradiation campaign are shown in figure 5. All voltages are provided by the Micrel MIC69502WR regulator, and as observed, there is an approximate 1% increase in voltage values over the irradiation period. This behavior is consistent with previous irradiation tests conducted on this technology.

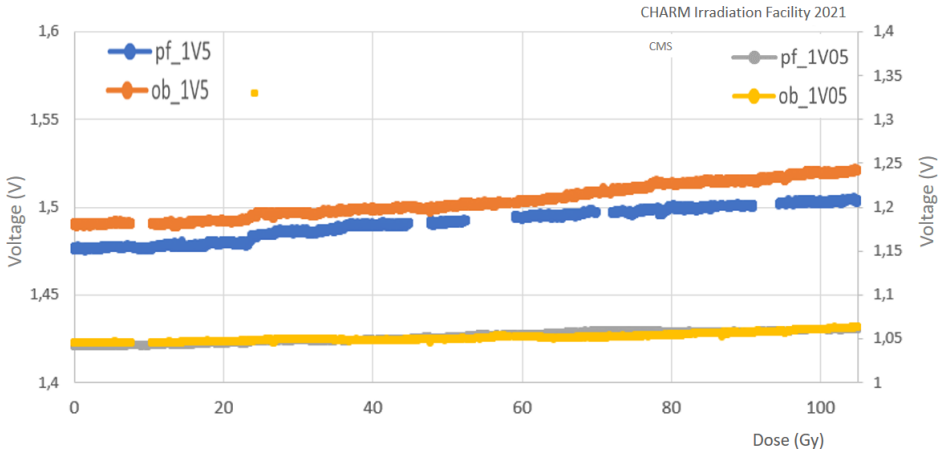


**Figure 5.** Output voltages of the MIC69502WR linear regulators on the OBDT and PUFO boards. The horizontal axis represents the accumulated dose up to a total of 109.8 Gy.

### 4.2 Results from the FPGA performance in the reference test

First, we present the results from the PolarFire firmware designed to perform the reference test described in section 3.1. The number of mismatches in the output values from the flip-flops was



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counted as SEUs, with the results for each board and test type summarized in table 4. The total dose and fluence used for the cross sections calculations are lower (70%) than the total received because we have removed the periods in which the monitoring was failing. The formula used to calculate the cross-section is provided in equation (4.1).

$$\sigma(\mathrm{cm}^2/\mathrm{bit}) = \frac{\#\mathrm{SEUs}}{\varphi((p)/\mathrm{cm}^2) \cdot \#\mathrm{bits}} \tag{4.1}$$

**Table 4.** Cross sections in the RAMs calculated for the SEU reference test both in the OBDT and PUFO board. Average values obtained from both boards are shown.

| | OBDT | PUFO | | | OBDT | PUFO | Average |
|---|---|---|---|---|---|---|---|
| | #SEUs | #SEUs | #FF or bits | Fluence ($p/cm^2$) | Cross-section ($cm^2$/bit) | Cross-section ($cm^2$/bit) | Cross-section ($cm^2$/bit) |
| **CKBD 40 MHz** | 60 | 71 | 4096 | 7,05E+11 | 2E-14 | 2E-14 | 2E-14 |
| **CKBD 10 MHz** | 33 | 25 | 4096 | 7,05E+11 | 1E-14 | 9E-15 | 1E-14 |
| **FF All 1s** | 16 | 20 | 4096 | 7,05E+11 | 6E-15 | 7E-15 | 6E-15 |
| **FF All 0s** | 29 | 22 | 4096 | 7,05E+11 | 1E-14 | 8E-15 | 9E-15 |

Additionally, the number of SEU errors detected in the internal RAMs was calculated by scrubbing the 17-bit words stored in a RAM with $2^{17}$ positions and results are shown in table 5. On rare occasions, the SEU counter displayed abnormally high values, characterized by erratic and uncontrolled increments. This behavior is likely caused by a SEU affecting the logic responsible for the SEU-reference counters and the calculation of the read address. These events are classified as Multiple Bit Upsets (MBUs).

**Table 5.** Number of SEUs measured in the OBDT and PUFO for the SEU reference test and corresponding calculated cross sections. Average values obtained from both boards are shown.

| | OBDT | PUFO | | | OBDT | PUFO | Average |
|---|---|---|---|---|---|---|---|
| | #SEUs or #MBUs | #SEUs or #MBUs | #FF or bits | Fluence ($p/cm^2$) | Cross-section ($cm^2$/bit) | Cross-section ($cm^2$/bit) | Cross-section ($cm^2$/bit) |
| **LSRAM SEUs** | 19414 | 16673 | 2228224 | 7,05E+11 | 1E-14 | 1E-14 | 1E-14 |
| **LSRAM MBUs** | 1 | 2 | 2228224 | 7,05E+11 | 6E-19 | 1E-18 | 1E-18 |

The cross sections have been averaged and are compared in table 6 with results from other radiation tests [16] performed on the PolarFire FPGA using similar logic implementations. The reference tests utilized radiation sources comprising 64 MeV protons and 1–800 MeV neutrons, whereas the CHARM radiation field encompasses a broader energy spectrum, including neutrons (1–10 GeV) and protons (0.1 MeV to 10 GeV).

CHARM cross-sections were determined using the combined fluence of high-energy hadrons and thermal neutrons as the total fluence for our test. This methodology considers the sensitivity of the Microsemi PolarFire FPGA to thermal neutron effects due to the presence of Boron-10. The cross-sections measured in this study (table 6) are slightly lower than those reported in other tests. These differences can be attributed to variations in particle types, energy spectra, clock frequencies, or specific firmware implementations. Despite these small differences, the results are very consistent between the tests, with closer similarity observed in the results obtained from neutron irradiation. This consistency validates the robustness of the methodology employed for determining the SEU results.



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**Table 6.** Cross sections obtained in our test at CHARM compared to results with other radiation sources.

| | **Our test at CHARM ($cm^2$/bit)** | **Reference [16] Neutron (1–800 MeV) ($cm^2$/bit )** | **Reference [16] Proton 64 MeV ($cm^2$/bit)** |
|---|---|---|---|
| CKBD 40 MHz | $2.27\ 10^{-14}$ | - | - |
| CKBD 10 MHz | $1.00\ 10^{-14}$ | - | - |
| FF All 1s | $6.23\ 10^{-15}$ | $1.06\ 10^{-14}$ | $8.46\ 10^{-15}$ |
| FF All 0s | $8.83\ 10^{-15}$ | $9.50\ 10^{-15}$ | $6.48\ 10^{-15}$ |
| LSRAM SEUs | $1.15\ 10^{-14}$ | $1.59\ 10^{-14}$ | $1.18\ 10^{-14}$ |
| SLRAM MBUs | $9.55\ 10^{-19}$ | $< 9.55\ 10^{-16}$ | - |

### 4.3 Results from the FPGA performance in the OBDT firmware test

As outlined in section 3, we monitored the number of SEUs potentially arising from mismatches in the time measurements of signals between the PUFO and the OBDTv1, simulating the expected behaviour of the logic during CMS operation. This firmware employed closely resembles the version intended for HL-LHC operations and incorporates Triple Module Redundancy (TMR) and Cyclic Redundancy Check (CRC) mechanisms in the RAMs. The only component not protected by TMR is the input logic of the TDCs and the high-speed transceivers. Errors in the transceivers are excluded from these measurements, as distinguishing them from errors in the optical transceivers is not feasible. To ensure reliable data transmission, the results reported here were obtained using the secondary electrical link.

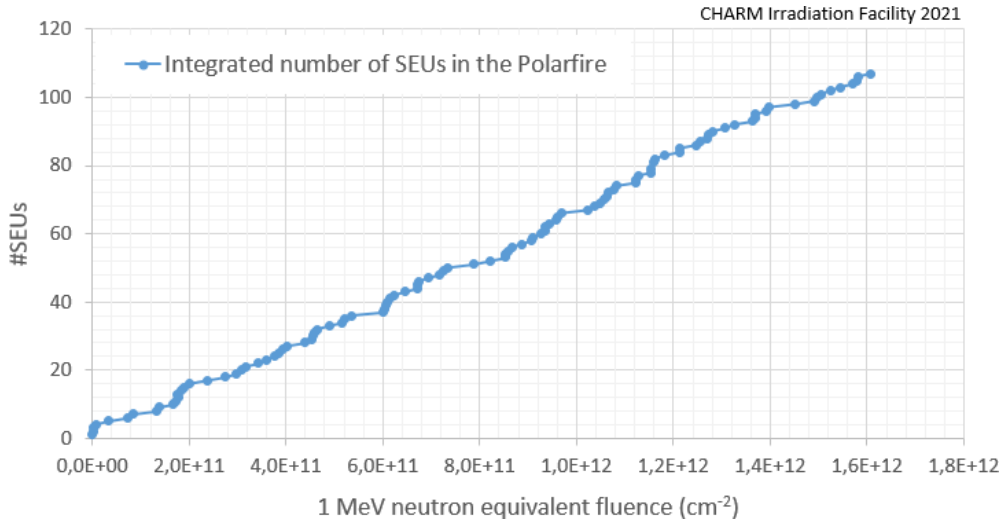


**Figure 6.** Results showing the number of SEUs measured in the test stand as a function of the accumulated fluence of 1 MeV equivalent neutrons during irradiation at CHARM.

The SEUs observed during the entire campaign were recorded and their distribution as a function of the 1 MeV equivalent neutron fluence is presented in figure 6. As can be seen, a very clear linear trend versus the fluence has been obtained. It is worth mentioning that all of these failures were automatically recovered, with no impact on the operational performance of the board. Additionally, there was no need to reprogram the FPGA at any point, indicating that the Flash memory of the



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FPGA was not affected. The results indicate a total of 107 SEUs observed throughout the irradiation campaign. Considering the amount of logic utilized in both devices during the test, the calculated cross-section for these failures is 2.33 $10^{-15}$ $cm^2$/bit.

This SEU cross-section obtained was compared to the values from the reference test outlined in section 4.3, showing comparable results. Notably, the final firmware intended for HL-LHC operations appears to exhibit slightly reduced susceptibility to SEU errors relative to the reference test. Comparisons of SEU measurements between reference architectures and final firmware do not always yield comparable results, making it crucial to ensure the failure rate in a realistic implementation of the system.

The extrapolation of this result to the anticipated SEU failure rates during the operation of the OBDTs in the HL-LHC has been performed by accounting for the differences in the expected radiation dose and the number of boards in the final system compared to the CHARM setup. Failures related to the optical transceivers were not extrapolated, as different devices will be used in the final system. The results are summarized in table 7.

Nevertheless, due to the non-uniform distribution of the radiation dose across the DT detector, average values do not accurately represent the actual failure rates that must be addressed from an operational perspective. Consequently, the extrapolation is also done separately for regions experiencing highest (external wheels MB1 type chambers) and lowest radiation (MB3 type chambers). As shown, the failure rates vary significantly between these regions. Nevertheless, even under the worst-case scenario, the projected rates remain within manageable levels.

**Table 7.** Extrapolation of the number of SEU failures in the OBDT board expected during HL-LHC based on the 107 failures observed at CHARM. The results provide the total projected failures across the entire DT system, as well as those specific to the most and least affected regions.

| | **Full DT system (830 OBDTs)** | **DT chambers on the highest radiation region (72 OBDTs)** | **DT chambers on the lowest radiation region (240 OBDTs)** |
|---|---|---|---|
| Average dose at HL-LHC (Gy) | 0.505 | 2.10 | 0.06 |
| #failures during HL-LHC | 241 | 86 | 8 |
| #failures/day (operating 100 days/year) | 0.24 | 0.09 | 0.01 |
| #days at HL-LHC between failures | 4.14 | 11.62 | 121.96 |

The results obtained in this study provide strong assurance that the OBDTs will perform reliably under radiation during operation at the HL-LHC.

## 5 Summary

The OBDTv1 prototype demonstrated the ability to digitize and transmit DT chamber signals with high time resolution ($\sim$ 0.8 ns) and meet the operational requirements of the HL-LHC environment. The radiation tests validated the robustness of key design elements, including the PolarFire FPGA, power distribution system, and slow control mechanisms, under realistic mixed-field radiation conditions. All of the components behaved perfectly apart from the optoelectronics. Measurable effects could



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be observed in the LDO regulators and in the FPGA. The expected current increase in the LDOs is negligible for our application and is not expected to impact the system's performance.

The FPGA results were also excellent, with the only radiation-induced effect observed being a certain number of SEU failures. SEU cross sections were measured for both a benchmark architecture and the final firmware implementation. The initial measurements confirmed the validity of the methodology and the reliability of the results. The second set of measurements produced results very similar to the reference, with no significant differences observed in the firmware implementation.

SEU results have been extrapolated to HL-LHC conditions to estimate the number of expected errors during the operation of the full DT system. The SEU effects in low and high dose regions are studied separately. The SEU results indicate that the system is well-suited to handle the anticipated radiation environment, with failure rates remaining manageable for operation stability.

The final OBDT board is expected to substitute the GBTx with the lpGBT ASIC to achieve higher speeds, though the functionality remains. Since both ASICs are designed to be radiation tolerant, no major difference in performance under radiation is expected.

In summary, the results demonstrate the readiness of the OBDTv1 prototype leading the way to the production of the final version of the boards for HL-LHC, where not only each individual component behaves properly under radiation but also the full board test confirms the reliability of the chosen architecture.

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