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Threshold switching in vertically aligned MoS_2/SiO_x heterostructures based on silver ion migration

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Threshold switching (TS) is a non-permanent change in electrical resistance controlled by voltage modulation in two-terminal devices. Silver (Ag) filament-based TS has been observed in two-dimensional transition metal dichalcogenides, which are promising due to their van der Waals gaps, facilitating ion migration and filament formation without disturbing covalent bonds. This work demonstrates the heterostructure growth of vertically aligned molybdenum disulfide ($VAMoS_2$) with an amorphous silicon oxide (SiO_x) layer after sulfurization. Ag ion migration through this material stack enables TS. Our $Ag/SiO_x/VAMoS_2/Au$ devices exhibit low switching voltages of ~0.63 V, high on-state currents over 200 µA, and stable switching exceeding 10^4 cycles. A physics-based dynamical model identifies two rate-limiting steps for filament formation, and the simulated switching kinetics align with experimental results. Our devices achieve fast switching in 311 ns and spontaneous relaxation in 233 ns. These findings advance understanding of switching mechanisms and highlight their potential for memory and neuromorphic computing applications.

Threshold switching (TS), also known as volatile resistive switching (RS), is a phenomenon in which electrical resistance temporarily changes in response to an applied electrical field[1]. TS devices have become highly relevant for emerging technologies, e.g., to be used as memory selectors, as artificial neurons and synapses in neuromorphic computing, and as true random number generators for security applications[2–10]. Memristive devices, typically composed of metal-insulator-metal two terminal structures, have gained attention as promising solutions for compact and energy-efficient technologies in the semiconductor industry[11–14]. They show TS primarily due to filament formation[15–17] achieved by ionic transport[18–20].

Recently, TS driven by the formation and disruption of conductive filaments from highly diffusive metal electrodes, such as silver (Ag) or copper (Cu) in two-dimensional (2D) materials, has gained considerable attention[21–26]. Reliable volatile RS, including high-speed switching and high endurance, is enabled by thin or weak filaments of the active metal ions in the switching layer[27,28]. The relaxation process, where filaments dissolve due to surface energy minimization or thermal diffusion, is influenced by the properties of the filament and the switching layer[28–31]. Material engineering strategies, such as a defected graphene layer at the Ag/insulator interface, have also been reported to influence the filament formation process[3,23,32,33]. In addition, the active metals enable the switching dynamics to be modulated by voltage amplitude, pulse duration, and temperature[5,8,23].

Ag or Cu filamentary threshold switches combined with 2D transition metal dichalcogenides (TMDs) are investigated for advanced brain-inspired neuromorphic hardware with fast switching speeds, high integration density, and low power consumption[15,34–38]. Among the 2D TMDs, molybdenum disulfide (MoS_2) is one of the most extensively studied switching layers in memristive devices[39], despite its relatively low bandgap (1.2–2.2 eV, depending on thickness)[40,41]. Monolayer MoS_2-based memristors have been demonstrated with stable, non-volatile RS while effectively suppressing leakage current[36]. It should be noted that the RS in MoS_2 primarily occurs via field-induced ion migration along van der Waals (vdW) gaps[16,20,42–44] or through grain boundaries and defects[15,18,36,45–47]. These findings suggest that intrinsic structural properties play a more critical role in RS behavior than the bandgap alone. MoS_2 films can be synthesized on wafer scale by thermally assisted conversion (TAC) from molybdenum (Mo) thin films into lateral or vertical MoS_2 layers via sulfurization[42,45,48]. Vertically aligned MoS_2 ($VAMoS_2$) layers are particularly promising for crossbar architectures,

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which rely on vertical electrical connections[16,17,20,49]. Their vertically oriented vdW gaps facilitate ion movement between two sandwiched electrodes for RS behavior[16,20,43]. In fact, volatile RS devices based on $VAMoS_2$ with an Ag active electrode have shown low threshold voltages from 0.18 V to 0.35 V and a high ON-OFF ratio of 10^6 [16,17,21,43]. However, the heterostructure of $VAMoS_2$ and an oxide layer remains underexplored, particularly regarding its impact on key device parameters such as switching voltages, variabilities, and the underlying switching mechanisms. Moreover, the time-dependent behavior and switching dynamics of such heterostructure-based devices have been rarely studied. More broadly, $VAMoS_2$-based and $VAMoS_2$/oxide heterostructure TS devices remain less understood than their widely investigated oxide-based counterparts[3,5,8,50,51]. Increased understanding of the switching dynamics in $VAMoS_2$/oxide heterostructure-based RS devices is therefore key for unlocking their potential applications.

In this work, we present TS devices that consist of an amorphous, substoichiometric silicon oxide (SiO_x) layer on $VAMoS_2$ below an active Ag electrode. The SiO_x layer was formed on top of $VAMoS_2$ during the sulfurization process. We show that Ag ions can travel through the material stack by applying long and short voltage pulses, leading to volatile RS. The switching performance is improved at lower switching voltages with a thinner SiO_x layer on top of the $VAMoS_2$ compared to a thicker SiO_x layer. The switching dynamics are analyzed theoretically using the JART ECM simulation model[52,53], which considers physics-based rate-limiting ionic processes, and are correlated with experimental observations.

Results

Device fabrication and material characterization of SiO_x/$VAMoS_2$-based RS devices

The two-terminal vertical devices studied in this work comprise a stack of SiO_x and $VAMoS_2$ layers sandwiched between an active Ag top electrode (TE) and an inert gold (Au) bottom electrode (BE). Figure 1a, b, respectively, show a schematic of the TS device and an optical microscopy image of the fabricated device with lateral dimensions of 4 µm × 4 µm. Figure 1c shows the fabrication process beginning with the preparation of inert Au BEs on Si substrates with 300 nm thermally grown silicon dioxide (SiO_2) using photolithography, electron-beam evaporation, and lift-off techniques. 6 nm Mo thin films were deposited on the pre-patterned Au BEs and subsequently converted into $VAMoS_2$ layers by TAC in a sulfur atmosphere in a chemical vapor deposition (CVD) system[20]. We fabricated SiO_x/$VAMoS_2$ devices with two different SiO_x layer thicknesses by placing the substrate either upright against the boat wall for thicker SiO_x and face-down on two overlapping boats for thinner SiO_x inside the CVD quartz tube (Fig. 1d). This resulted in 60 nm and 10 nm SiO_x on top of the $VAMoS_2$, as confirmed by ellipsometry. Finally, the active Ag TEs were deposited and structured similarly to the BEs (see Methods and Supplementary Fig. 1 for further details). The growth of the MoS_2 layer with a process-parameter-dependent SiO_x layer via sulfurization was further demonstrated using non-patterned Mo thin films deposited on SiO_2/Si substrates, as confirmed by high-resolution transmission electron microscopy (HRTEM) images (Supplementary Fig. 2). The corresponding growth parameters, resulting MoS_2 orientations, and SiO_x thicknesses are summarized in Supplementary Table 1. The material growth via TAC directly on the device substrate helps avoid defects such as wrinkles and folds, typically introduced during the transfer process of 2D materials[54]. A wrinkle-free surface after the device fabrication was confirmed by atomic force microscopy (AFM), as shown in Supplementary Fig. 3.

The device compositions and structures were verified using cross-sectional transmission electron microscopy (TEM), which confirmed the presence of an amorphous SiO_x layer on $VAMoS_2$ between the Ag and Au electrodes (Fig. 2a, b). The vertical orientation of the nanocrystalline MoS_2 layers was further verified by HRTEM (Fig. 2c). The initial few layers formed

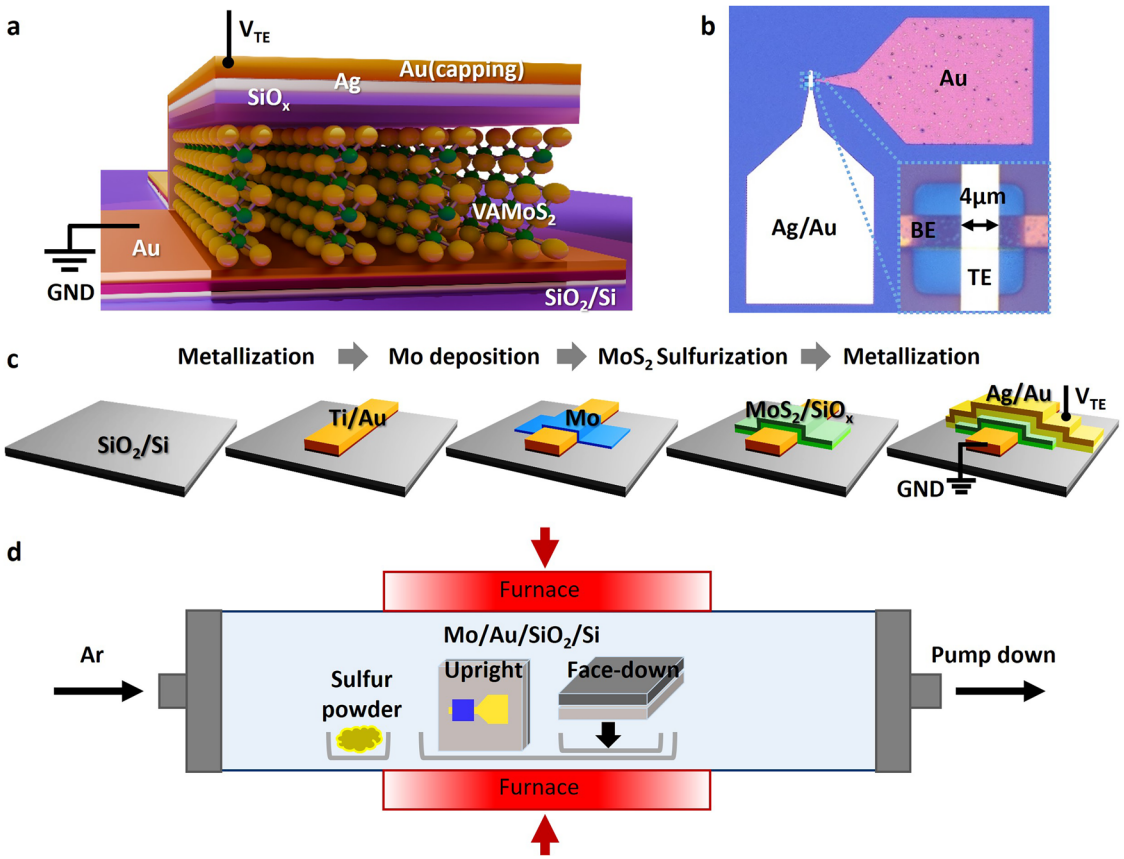

Fig. 1 | Ag/SiO_x/$VAMoS_2$/Au device structure and fabrication process. **a** Schematic drawing of the TS device. **b** Top-view optical microscopy image of the fabricated device, with the inset showing a zoomed image of the 16 µm^2 area where the top (TE) and bottom (BE) electrodes intersect. **c** Schematic of the fabrication process flow for a RS cross-point device. **d** Schematic of the sulfurization process for $VAMoS_2$ film in a horizontal tube furnace, with sulfur powder positioned upstream and sputtered Mo thin film on pre-patterned Au on SiO_2/Si substrate at the center of the tube.

on the Au surface tend to be laterally oriented, followed by the dominant formation of vertically aligned layers. This transition is attributed to surface alloying, where Mo atoms diffuse near the Au surface during the early stages of sulfurization[55]. In contrast, MoS_2 layers grown directly on the SiO_2/Si substrate appear predominantly vertically aligned (see Supplementary Fig. 4). Raman analysis was conducted on the as-grown MoS_2 film on the Au BE surface for 60 nm and 10 nm SiO_x/$VAMoS_2$ devices (Supplementary Fig. 5). The Raman spectra of the sulfurized MoS_2 films show the characteristic E^1_{2g} and A_{1g} peaks at 382 cm^{-1} and 407 cm^{-1}, respectively, in both devices. The Raman peaks correspond to the in-plane (E^1_{2g}) and out-of-plane (A_{1g}) vibrational modes, respectively[56,57], and confirm the synthesis of the 2H-MoS_2 phase. The data also provide insight into the vdW layer orientation, as their peak intensity ratio (E^1_{2g}/A_{1g}) of approximately 0.4, observed in both cases, indicates the formation of vertical MoS_2 layers, as reported in the literature[58]. The vertical MoS_2 growth from 6 nm Mo thin films is consistent with the literature, where vertical vdW orientation was reported for initial Mo thicknesses exceeding 3 nm (see Fig. 2d for details)[17,42,45,49,59–63].

The presence of the amorphous SiO_x layer was confirmed by high-angle annular dark-field (HAADF) imaging (Fig. 2e) and energy-dispersive X-ray spectroscopy (EDXS) elemental mapping (Fig. 2f) of the 10 nm SiO_x/$VAMoS_2$ device (see Supplementary Fig. 6 for the 60 nm SiO_x/$VAMoS_2$ device). We attribute the SiO_x layer formation to atomic diffusion of Si and O from the SiO_2/Si substrate at high temperatures during the Mo sulfurization process[49,64], potentially enhanced by the vdW gaps in the $VAMoS_2$ layer.

DC electrical performance

The SiO_x/$VAMoS_2$ devices initially exhibited a high resistance of more than 25 GΩ, which can be explained by the presence of the insulating SiO_x in the material stack. The RS characteristics of thick (60 nm) and thin (10 nm) SiO_x/$VAMoS_2$ devices were measured by 30 consecutive direct-current (DC) current–voltage (I–V) sweeps with a current compliance of I_{CC} = 1 μA (Fig. 3a, b). Both devices showed abrupt switching from the high resistance state (HRS) to the low resistance state (LRS) at certain positive on-threshold voltages ($V_{t,on}$) applied to the Ag TEs. The LRS was maintained for a positive bias beyond $V_{t,on}$. The transition from the LRS back to the HRS occurred during the reverse voltage sweep below the hold voltages (V_{hold}). Repeatable volatile RS was observed with an average $V_{t,on}$ of ~1.66 V for the 60 nm SiO_x/$VAMoS_2$ device and ~0.63 V for the 10 nm SiO_x/$VAMoS_2$ device, demonstrating that a thinner SiO_x layer on $VAMoS_2$ requires a lower switching voltage.

TEM imaging revealed residual traces of Ag in the SiO_x layer in the HRS (~1 MΩ) after 42 switching cycles (Fig. 3c). This suggests that applying a positive voltage to the TE induces Ag diffusion through the switching layer and the formation of a conductive filament bridging the top and bottom electrodes[21]. However, the Ag ions visible in the TEM do not form a complete filament because no external bias was applied during the measurement, and the device is in the HRS. Instead, the conductive filament required for the LRS has partly dissolved and ruptured as the voltage bias was removed due to interfacial energy minimization[17,27]. The volatile switching in our devices is thus governed by the formation and breakage of Ag conductive filaments within the SiO_x/$VAMoS_2$ stack, enabled by Ag ion movement in the SiO_x layer and along the vdW gaps of vertically oriented MoS_2 layers. Similar non-volatile switching with ion movement along the grain boundaries has been observed in laterally oriented MoS_2 layers[15,22,36,45].

We evaluated the variability of the devices based on SiO_x thickness by statistically analyzing $V_{t,on}$ and V_{hold} data from 30 consecutive cycles (Fig. 3d, e). The 60 nm SiO_x/$VAMoS_2$ device exhibited larger cycle-to-cycle standard deviations of 0.39 V for $V_{t,on}$ and 0.21 V for V_{hold}, compared to the 10 nm SiO_x/$VAMoS_2$ device with standard deviations of 0.16 V for $V_{t,on}$ and 0.09 V for V_{hold}, respectively. The thinner SiO_x layer on $VAMoS_2$ reduces variability and enables lower switching voltages. In addition, we analyzed $V_{t,on}$ and V_{hold} as a function of cycle number for both device types, which revealed no clear trend with increasing cycles (Supplementary Fig. 7). Additional DC I–V sweeps were performed on multiple devices to quantify the device-to-device variation. The results are shown in Fig. 3f, which plots $V_{t,on}$ and V_{hold} of the initial I–V traces of ten 60 nm and twenty 10 nm SiO_x/$VAMoS_2$ devices. The individual I–V sweeps corresponding to these data are provided in Supplementary Fig. 8, 9. The 60 nm SiO_x/$VAMoS_2$ devices exhibited standard deviations of 0.53 V for $V_{t,on}$ and 0.34 V for V_{hold}, while the 10 nm SiO_x/$VAMoS_2$ devices showed lower deviations of 0.21 V for $V_{t,on}$ and 0.13 V for V_{hold}, respectively. The lower cycle-to-cycle and device-to-device variability in the latter, combined with the lower switching voltages, favors thin SiO_x layers on $VAMoS_2$ for applications such as artificial neuron circuits[23]. The cycle-to-cycle variation for the 10 nm SiO_x/$VAMoS_2$ device was further evaluated using cumulative probability analysis over 384 consecutive cycles (Fig. 3g), with all I-V sweeps for the device plotted in Supplementary Fig. 10. Additionally, a yield was obtained to be 100% for the 60 nm SiO_x/$VAMoS_2$ devices and 95% for 10 nm SiO_x/$VAMoS_2$ devices, as detailed in Supplementary Section 10. The yield evaluation in this work is based on the initial functional performance of the devices, and does not include endurance statistics across multiple devices, which will be an important aspect of future studies. It is also noted that our as-grown 2D material fabrication process is transfer-free, effectively avoiding common transfer-related failures such as scratched lines and localized damage[65].

Pulsed voltage characteristics

We conducted pulsed voltage measurements to further elucidate the switching dynamics of the 10 nm SiO_x/$VAMoS_2$ devices, selected for their favorable DC switching behavior. We analyzed the transient current response to 100 μs voltage pulses with amplitudes ranging from V_{pulse} = 1.5 V to 4.5 V. The pulse width was chosen to capture the switching kinetics and to obtain measurable switching times across this voltage range. The devices switched to the LRS after a certain time which depended on V_{pulse}. After the pulse, the device returned to the HRS, and the state was read out with a read pulse of 0.3 V for 3 μs. Two typical transient current responses are shown in Fig. 4a, b, while all data is available in Supplementary Fig. 11. Supplementary Figure 12 presents enlarged views, clearly showing the transient from the LRS to the HRS. The on-switching time (t_{on}) was determined by extracting the midpoint value of the first significant non-capacitive current rise in the double logarithmic current-time (log(I)-log(t)) curves. This midpoint value also represents the steepest slope during this specific transient current rise. Figure 4c shows the extracted t_{on} values as a function of V_{pulse}, with an inset illustrating the voltage pulse waveform. As V_{pulse} increases, the log(t_{on}) decrease is mostly linear. However, at higher V_{pulse} values, the rate of decrease in log(t_{on}) reduces, resulting in a progressively flatter log(t_{on})-V_{pulse} curve, which indicates reduced sensitivity of the switching time change to further increased voltages. Similar observations were reported in volatile and non-volatile electrochemical metallization devices, where the switching kinetics are divided into three regimes based on the respective ionic rate-limiting step: (I) nucleation limited, (II) electron transfer limited, and (III) electron transfer and ion migration limited[8,52]. Considering these three distinct ionic processes under an applied bias enables a good prediction of switching times as a function of the electrical stimulus. The three processes become rate-limiting at three specific voltage regimes and are, therefore, responsible for the dynamic behavior of the device. Extensive experimental results have confirmed this observation[8,52].

We applied a well-established simulation model developed by Menzel et al. and Ahmad et al.[52,53] to gain a deeper understanding of the physical processes limiting the switching time in our Ag/SiO_x/$VAMoS_2$/Au devices. The full model is explained in Supplementary Section 12. The simulation results are plotted as a solid line with the experimental data in Fig. 4c. The fitting parameters are detailed in Supplementary Table 3. Two distinct regimes are evident from the data: At voltages below 3 V, the sharp linear slope on the logarithmic scale corresponds to the electron transfer-limited regime. Above 3 V, the flatter slope indicates that the rate-limiting factor shifts to a mixed regime of electron transfer and silver ion migration. Therefore, the voltage that drops across the device determines which of the ionic processes is/are the slowest and, thus, rate-limiting. This insight is obtained by analyzing the physics-based model, which describes the transient

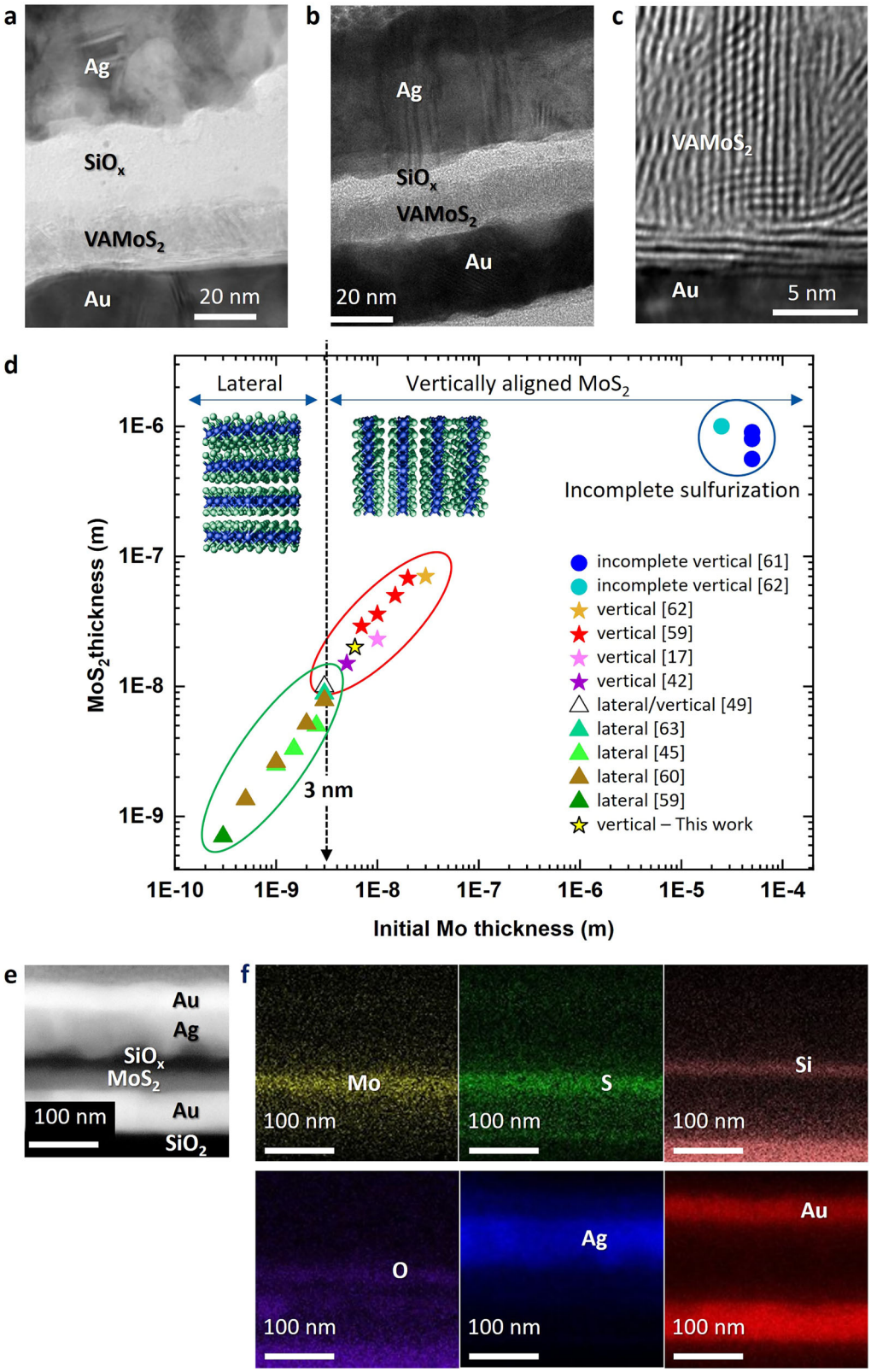

Fig. 2 | Cross-sectional analysis of the device structure and material characterization. a, **b** Cross-sectional TEM images displaying the vertical stack of SiO_x/$VAMoS_2$ between the top and bottom electrodes for devices with 60 nm (**a**) and 10 nm (**b**) SiO_x layers. The $VAMoS_2$ thickness is approximately 20 nm in both cases. **c** An enlarged HRTEM image of $VAMoS_2$ layers grown on Au. **d** MoS_2 orientation as a function of initial Mo layer thickness. When the initial Mo thickness is below 3 nm, laterally aligned MoS_2 layers are formed. As the Mo thickness increases, vertically aligned MoS_2 layers begin to dominate. In the bulk, incomplete sulfurization occurs after a certain amount of vertical layer formation[17,42,45,49,59–63]. **e**, **f** Cross-sectional HAADF image of the 10 nm SiO_x/$VAMoS_2$ device (**e**), and the corresponding EDXS elemental mapping of the device stack (**f**), showing Mo, S, Si, O, Ag, and Au.

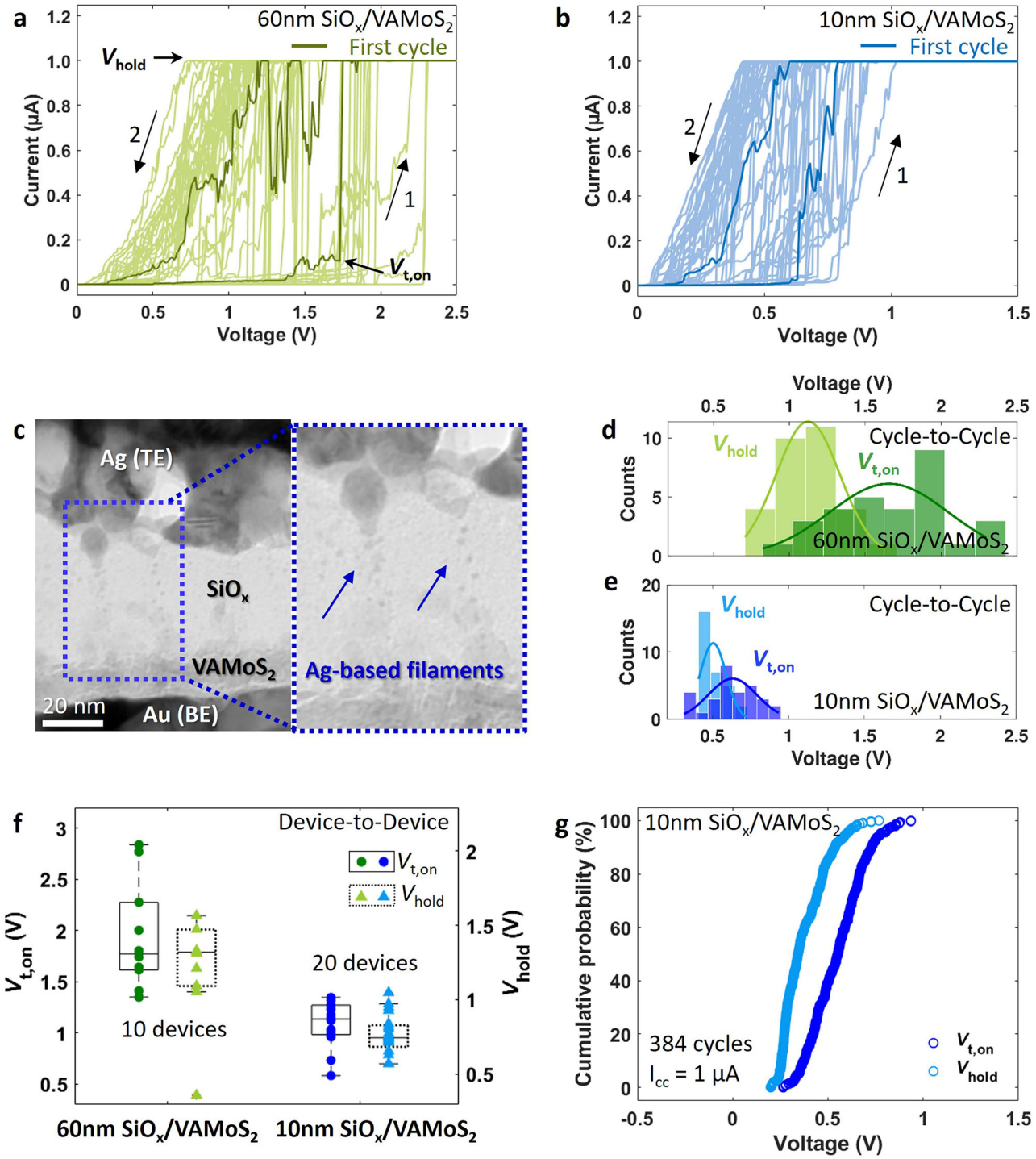

Fig. 3 | DC current-voltage (*I-V*) characteristics of Ag/SiO_x/$VAMoS_2$/Au devices. **a**, **b** 30 *I-V* switching cycles of a 60 nm and a 10 nm SiO_x/$VAMoS_2$ device, respectively. The devices exhibit TS with a positive voltage applied to the Ag top electrode. I_{CC} was set to 1 μA, and arrows 1 and 2 denote the voltage sweep direction. **c** Cross-sectional TEM image of the device after RS at low HRS after several RS cycles. The dotted blue rectangle is further enlarged on the right, showing Ag traces in the material stack. **d**, **e** Statistical distribution of switching voltages ($V_{t,on}$ and V_{hold}) for 60 nm and 10 nm SiO_x/$VAMoS_2$ devices, respectively. 30 RS cycles were evaluated per sample, with data extracted from (**a, b**). **f** Device-to-device distribution of $V_{t,on}$ and V_{hold} for 10 devices with 60 nm SiO_x/$VAMoS_2$ and 20 devices with 10 nm SiO_x/$VAMoS_2$. **g** Cumulative probability distribution of $V_{t,on}$ and V_{hold} in a 10 nm SiO_x/$VAMoS_2$ device over 384 RS cycles.

evolution of the gap between the active electrode and the filament tip and the transient evolution of voltage drops across the various ionic processes[52,53]. The model also includes a nucleation limited regime, which can typically be accessed with rather low voltages applied for rather long pulse durations, but which we did not see in this work's experimental data.

Next, we explored short voltage pulses of 1 μs to switch the SiO_x/$VAMoS_2$ devices. The voltage-dependent transients in Fig. 4d show a significant increase in on-state current upon 1 μs pulses of different voltages, up to 200 μA for 6 V. Such short pulses lead to reduced stress, which typically enhances the device endurance, a key performance parameter for TS devices besides fast switching time and high on-state current. We tested the endurance by applying short 2 μs voltage pulses of 4.5 V to switch a device from the HRS to the LRS, then returning it to the HRS, followed by a pulse of 0.1 V for 3 μs to read out the off-state current. The 10 nm SiO_x/$VAMoS_2$

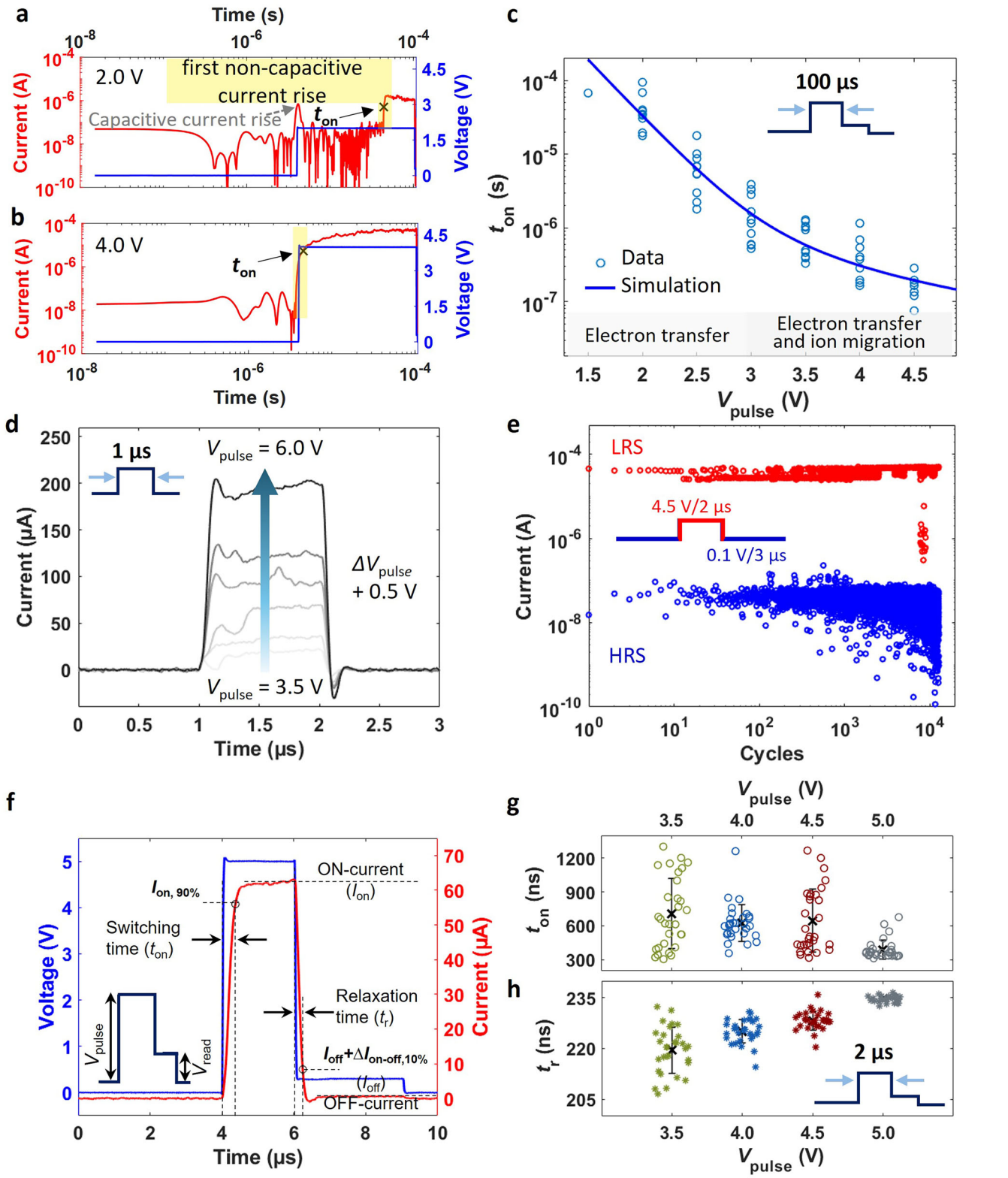

Fig. 4 | Pulsed voltage characteristics of Ag/10 nm SiO_x/$VAMoS_2$/Au devices. **a**, **b** Transient current response under V_{pulse} of 2.0 V (**a**) and 4.0 V (**b**) with a 100 µs duration in double logarithmic scale. t_{on} is marked with an "x", and the first non-capacitive current rise is highlighted in yellow. The initial capacitive current rise is also indicated with a grey arrow in (**a**). **c** Switching kinetics showing experimental data for t_{on} as a function of V_{pulse} (blue circles) and fitting data from the numerical simulation (blue solid line). The plot is divided into two regions: electron-transfer-limited and mixed control regimes. The inset displays the voltage pulse waveform. **d** Transient current response of 1 µs voltage pulses with amplitudes ranging from 3.5 V to 6.0 V (ΔV_{pulse}: +0.5 V). **e** Pulsed endurance showing over 10^4 cycles. Inset: programming pulse consisting of 4.5 V/2 µs followed by 0.1 V/3 µs. The LRS and HRS currents were extracted as the average of the values recorded during the second half of the 4.5 V and 0.1 V pulses, respectively. **f** Current response in the time domain under a voltage pulse of 5.0 V/2 µs, followed by a read pulse 0.3 V/3 µs. The inset shows the corresponding voltage pulse waveform. **g**, **h** Statistical distributions of t_{on} and t_r as a function of V_{pulse} in a short pulse of 2 µs for 30 repetitions, respectively.

device exhibits stable switching behavior after 10^4 cycles with an average ON-OFF ratio of 10^3, as shown in Fig. 4e. Additional DC resistance measurements were taken after every 10 consecutive voltage pulses to further validate the reliability of the device's volatility. The DC resistance values are plotted together with the extracted HRS and LRS resistance values in Supplementary Fig. 13, confirming consistent returns to the HRS after each set of 10 pulses. A pulsed endurance test was also performed without the DC resistance measurements to eliminate any potential influence from them. This device also demonstrated continued robust endurance of ~5800 cycles, with average resistance values of 166 kΩ for the LRS and 5 MΩ for the HRS (see Supplementary Fig. 14). Additional endurance results from two other devices are also provided in Supplementary Fig. 14.

Furthermore, we measured t_{on} and the relaxation time (t_r) of a 10 nm $SiO_x/VAMoS_2$ devices as a function of V_{pulse} for a fixed pulse time of 2 µs over 30 consecutive pulses. V_{pulse} values between 3.5 V and 5.0 V were chosen, where the switching time is determined by the electron-transfer and ion migration, enabling a rapid transition to the LRS. One example of a measured time-resolved current response to a 5 V pulse is shown in Fig. 4f. Here, t_{on} is defined as the time required to reach 90% of the LRS ON-current (I_{on}). t_r is defined as the time needed to decay from I_{on} to 10% of the difference between I_{on} and the HRS OFF-current (I_{off})[66]. All extracted t_{on} and t_r are plotted in Fig. 4g, h, with the inset in Fig. 4h showing the voltage pulse waveform. t_{on} decreases slightly with increasing V_{pulse}, similar to the behavior observed with the longer voltage pulses of 100 µs. The device then returns to the HRS through a self-relaxation process while the read voltage is applied. Unlike t_{on}, t_r increases with higher V_{pulse}. We assume that the stronger electric fields cause the formation of thicker, more robust filaments, which take longer to rupture. This assumption is supported by recent studies on oxide memristive devices[5,31]. The relaxation process thus reflects the history of the device, with t_r revealing whether the formed filament was thick or thin[8].

Our 10 nm $SiO_x/VAMoS_2$ device exhibits a fast switching of t_{on} = 311 ns and a spontaneous relaxation time of t_r = 233 ns using a voltage pulse of 5 V/2 µs and a read pulse of 0.3 V/3 µs. t_{on} and t_r are critical parameters for operating memristive devices and can be adjusted by the voltage pulse parameters in our devices. The optimization of the operating conditions is required to ensure reliable endurance and accurate device performance. Their tunability can be used for versatile applications in electronics, ranging from selectors for memories to synaptic devices for neuromorphic computing[3–6,8]. Our device shows promise for selector applications, which require high on-state currents and short relaxation times[4,67]. However, there is a tradeoff, as increasing the on-state current tends to increase the relaxation time.

Table 1 compares the TS performance of the present $SiO_x/VAMoS_2$ devices with data from previously reported studies in the literature[3,4,17,68,69]. Our devices demonstrate significantly lower switching voltages and faster switching speeds, particularly faster relaxation times, compared to pure SiO_x or SiO_2-based devices. Our $SiO_x/VAMoS_2$ devices exhibit 10 times higher V_{hold} than the SiO_2 devices[69] although they have similar $V_{t,on}$, which implies that weaker Ag filaments are formed. We attribute this to the rapid formation and dissolution of conductive filaments within the switching stack, particularly in the $VAMoS_2$ layer, where the vdW nature of MoS_2 enables ionic transport but also limits the filament growth. The relaxation time is mainly governed by the material stack, due to spontaneous conductive path rupture driven by atomic and ionic mass transport[29]. The SiO_x layer is known to promote the formation of strong conductive Ag filaments[70,71]. However, the presence of the $VAMoS_2$ layer in direct contact with the Au BE appears to suppress this strong filament growth in our $SiO_x/VAMoS_2$ devices. When comparing the $SiO_x/VAMoS_2$ and SiO_x-only devices, we found that the incorporation of the $VAMoS_2$ layer leads to more stable switching behavior by the confined formation of filaments. A detailed comparison of their pulsed voltage responses is provided in Supplementary Fig. 15, and the *I-V* characteristics of the SiO_x-only device are presented in Supplementary Fig. 16. Our findings highlight the potential to achieve fast switching by integrating a SiO_x layer with 2D TMDs and provide insight into switching dynamics for volatile RS devices.

Table 1 | Performance comparison of Ag-based threshold switches

Device	Material growth method	$V_{t,on}$	V_{hold}	$I_{ON/OFF}$ (DC)	On-state current		Endurance (cycles)		Switching speed		Pulsed voltage (V_{pulse}/duration)
					DC (I_{CC})	AC	DC	AC	Switching time	Relaxation time	
Ag/SiO_x/$VAMoS_2$/Au This work	**CVD (Sulfurization)**	**0.63 V**	**0.5 V**	**>10^3**	**1 µA**	**200 µA**	**384**	**>10^4**	**311 ns**	**233 ns**	**4.5 V/2 µs**
Ag/$VAMoS_2$/Au[17]	CVD (Sulfurization)	0.35 V	0.1 V	10^6	100 µA	N/A	>30	5 × 10^6	N/A	N/A	1.2 V/50 µs
Ag/MoS_2/Ag[68]	Aerosol-Jet Printer (Exfoliated flakes ink)	0.18 V-0.3 V	0.13 V	10^5	10 µA	1µA	100	N/A	N/A	50 µs	1.0 V/100 µs
Ag/DDG*/SiO_2/Pt[3]	Magnetron sputtering	0.6 V	—	5 × 10^8	500 µA	500 µA	100	10^6	100 ns	1 µs	2.0 V/2 µs
Ag/SiO_2/Au[69]	N/A	0.7 V	0.05 V	N/A	1 mA	40 mA	N/A	N/A	N/A	100 µs	1.3 V/1 ms
Ag/SiO_x/C** [4]	Electron-beam evaporation	1.75 V	1.5 V	10^7	50 µA	15 µA	N/A	N/A	10 µs	1 ms	5.0 V/100 µs

N/A not available, *DDG** discrete-defect graphene, *C*** graphitic carbon. The values shown in bold represent the results obtained in this work.

Discussion

We investigated Ag-based TS using a material stack comprising thin SiO_x layers on $VAMoS_2$ in a $Ag/SiO_x/VAMoS_2/Au$ configuration. Our devices demonstrated highly repeatable volatile RS at low switching voltages of 0.63 V, with a high on-state current exceeding 200 µA for $V_{pulse} = 6$ V and robust pulsed endurance over 10^4 cycles. Furthermore, our devices showed fast switching filament formation and dissolution speeds with both switching and relaxation times in a few hundred nanoseconds for $V_{pulse} = 5$ V. We analyzed the switching kinetics of the devices using the JART ECM model and identified the experimentally observed physical processes of electron-transfer-limited and electron-transfer/ion migration-limited switching. The observed SiO_x thickness and uniformity resulted from our solid source tube furnace setup, which was primarily designed for proof-of-concept studies rather than precise thickness control. While this method confirms the feasibility of growing $SiO_x/VAMoS_2$ heterostructures, it lacks the precision achievable with gaseous precursors in industrial fabrication techniques. Nevertheless, these findings advance the understanding of $SiO_x/VAMoS_2$-based RS devices and pave the way for their practical use in emerging memories and neuromorphic computing systems.

Methods

Device fabrication and material growth

The $Ag/SiO_x/VAMoS_2/Au$ cross-point devices, with dimensions of 4 µm × 4 µm, were fabricated on 300 nm SiO_2/Si substrates. First, the substrates were cleaned using acetone, isopropanol (IPA) and O_2 plasma to remove surface contaminants. Bottom electrodes (BEs) were defined by photolithography (using a Mask aligner EVG420 from EV GROUP) and deposited with a 5 nm titanium (Ti) adhesion layer and a 50 nm Au layer by electron-beam evaporation (Pfeiffer Balzers PLS 500), followed by lift-off in dimethyl sulfoxide (DMSO) heated to 80 °C. Next, a 6 nm thick patterned molybdenum (Mo) film was formed on the BEs by photolithography, direct-current sputtering (CREAMET S2, CREAVAC GmbH), and lift-off. A Mo target with a purity of 99.95% from EVOCHEM was used for the sputtering process. The sputtering was conducted with a power of 100 W under an Ar flow and a chamber pressure of $\sim 3 \times 10^{-3}$ mbar. The sulfurization process was performed in a chemical vapor deposition (CVD) tube furnace (RS 80/300, Nabertherm GmbH), where the patterned Mo film on $Au/SiO_2/Si$ substrate was heated in a sulfur atmosphere. This process was conducted at 800 °C for 30 min with an Ar flow rate of 20 sccm as the carrier gas at a pressure of 9.6×10^{-2} mbar to achieve a vertical orientation of the MoS_2 layers. Sulfur powder was placed upstream in the CVD furnace and heated to 150 °C. Sulfur diffused into the Mo film, creating ~20 nm thick MoS_2 layers. Finally, 30 nm Ag top electrodes (TEs) with a 30 nm Au capping layer were deposited using photolithography, electron-beam evaporation, and lift-off processes. The complete fabrication process flow and the sulfurization process are illustrated in Fig. 1c, d. Top-view optical microscopy images of the thick and thin $SiO_x/VAMoS_2$ cross-point devices are shown in Supplementary Fig. 1a, b, respectively.

Material characterization

Transmission electron microscopy (TEM) was employed to investigate the cross-sectional device structure, layer orientation, and chemical composition. TEM lamellae were prepared by focused ion beam (FIB) using an FEI Strata400 system. TEM imaging and energy-dispersive X-ray spectroscopy (EDXS) were conducted by JEOL JEM F200 at 200 kV. Raman spectroscopy was performed on the as-grown MoS_2 layer to analyze the phase formation. The Raman measurement was taken using a WITec alpha 300 R Raman system in mapping mode with a 532 nm excitation laser at 1 mW power and a 1800 g/mm grating.

Electrical characterization

Switching properties of the devices were measured at room temperature using a Lakeshore probe station connected to a semiconductor parameter analyzer (Keithley 4200S-SCS from a Tektronix company), equipped with two source measure unit cards (Keithley 4200-SMU) and preamplifiers (Keithley 4200-PA). A voltage stimulus was applied to the Ag top electrode while the Au bottom electrode was grounded. Under an applied electric field, Ag ions migrate through the material stack, namely the SiO_x layer and the $VAMoS_2$ layers, modulating the conductivity. The applied voltage was monitored in parallel on channel 2 from the Ag top electrode, and the output current was measured over time on channel 1 from the Au bottom electrode. For DC current–voltage (I–V) sweep measurements, the voltage was swept from 0 V to a positive maximum 3 V and back to 0 V, with the current limited by an external current limiter within the Keithley 4200-SCS. Pulsed voltage measurements were conducted using the pulse measure units (Keithley 4225-PMUs).

Data availability

The datasets generated and/or analyzed during this study are available from the corresponding author upon reasonable request.

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Author contributions

M.C.L. and A.D. conceived and designed the concept and supervised the project. J.L. carried out the material growth, characterization, device fabrication, and electrical measurements. J.L., S.C., D.B., and L.V. analyzed the electrical data and characteristics. R.W.A. performed the JART ECM simulations, and R.W.A. and S.M. supported the analysis of the electrical data. K.R. and V.M.A. conducted the TEM and EDSX analyses under the supervision of J.M.; J.L. prepared the initial manuscript draft, and all authors contributed to its revision and finalization. All authors have read and approved the final version of the manuscript.

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Competing interests

The authors declare no competing interests.

Additional information

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