Demonstration of Low Power and Multifunctional Neurons With Only Two or Five Ferroelectric SBFETs

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***Abstract*— This work demonstrates both artificial synapses and neurons based on a single type of ferroelectric Schottky barrier FET (Fe-SBFET). The Fe-SBFET features a 200-nm gate length, incorporating a ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) gate dielectric and an ultrathin Si_3N_4 interfacial layer. A single Fe-SBFET exhibits robust synaptic characteristics with low energy consumption of 28 fJ/state. Utilizing only two Fe-SBFETs, we realize an integrate-and-fire (IF) neuron with an energy cost of 0.67 pJ/spike. Notably, a five-transistor Fe-SBFET neuron circuit replicates thalamic neuron behavior, exhibiting leaky integrate and fire or burst (LIFB) functionality at 5.6 kHz, with an energy consumption of just 2.6 pJ/spike.**

***Index Terms*— Ferroelectric Schottky barrier FET (Fe-SBFET), $Hf_{0.5}Zr_{0.5}O_2$ (HZO), leaky integrate and fire or burst (LIFB), neuromorphic computing (NC), thalamic neuron.**

I. Introduction

THE energy consumption required for artificial neural networks is becoming increasingly challenging [1]. The goal of neuromorphic computing (NC) is to mimic the effectiveness of the brain by using artificial synapses and neurons based on semiconductor devices [2]. Synapses are responsible for transmitting information between neurons by releasing neurotransmitters, which can be either excitatory or inhibitory [see Fig. 1(a)]. There are different ways to implement these artificial synapses and neurons. The artificial synapse is fabricated with a device whose conductance can be modulated by an external stimulus, giving the synapse a certain plasticity. For example, conductive filaments can be generated in a memristor after applying a voltage [3], [4]. Another important property of the synapse is that the modulated plasticity remains either short-term or long-term after the external stimulus is removed, so the synapse has a memory function [5], [6]. The artificial neuron requires one part for integration and one part for spike generation. The integrating part can be realized with a capacitor that stores the charge from the synapse. In contrast,

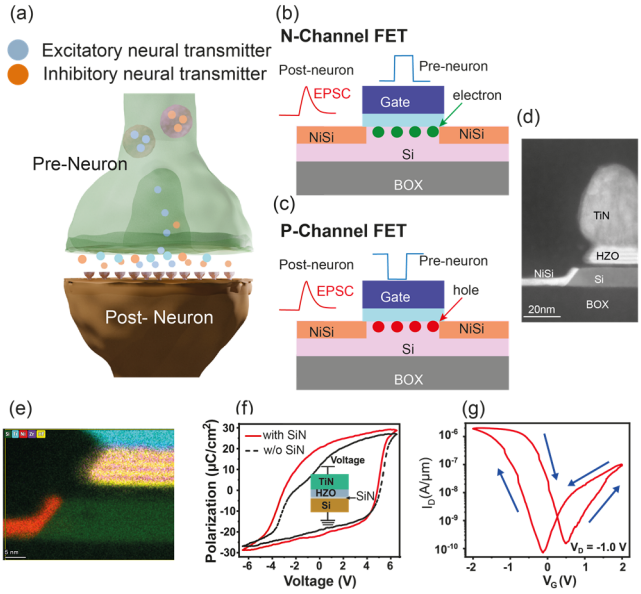

Fig. 1. (a) Illustration of biological synapses with excitatory and inhibitory neurotransmitters. Schematic of the ambipolar Fe-SBFET as (b) n-channel and (c) p-channel device, mimicking a synapse with different neural transmitters. (d) Cross-sectional TEM image of a fabricated device. (e) EDX mapping shows HfO_2–ZrO_2 superlattice structure. (f) *P–V* characteristics measured from a TiN/HZO/SiN/Si capacitor showing stronger polarization compared with the capacitor without a SiN interfacial layer. (g) I_D–V_G transfer characteristics of a fabricated Fe-SBFET with a channel length of 200 nm, showing ambipolar behavior and hysteresis.

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the spike generation part can be achieved with a memristor that generates a spike when the voltage across the capacitor exceeds the threshold [7], [8].

Most previously reported artificial synapses or neurons have, for example, high energy consumption or require many different devices, including capacitors that consume both area and energy [9], [10], [11], [12]. This makes integrating synapses and neurons more expensive and the NC less energy efficient with respect to machine learning in software. In [13] and [14], it was reported that one ferroelectric Schottky barrier FET (Fe-SBFET) can be used as a synapse and four Fe-SBFETs form a leaky integrate and fire (LIF) neuron (LIF-Neuron), which, in combination with an additional Fe-SBFET, implements a thalamic neuron. Only long-channel devices were demonstrated in [13] and [14], requiring high voltage bias and energy, whereas low-power short-channel devices are needed for practical applications.

In this work, we report artificial neurons with different functions based on only two or five optimized Fe-SBFETs with a gate length of around 200 nm, which can also be used as a synapse with multiple reconfigurable neural transmitters, allowing for easy fabrication of synapses and neurons. We demonstrate the improvement by device scaling, including lower energy consumption, with respect to the long gate device reported in [14].

II. Device Fabrication

Fe-SBFETs were fabricated on silicon-on insulator (SOI) substrates with a thin top Si layer (15-nm thick), as illustrated in Fig. 1(b) and (c). The SOI layer was etched into mesa structures. A very thin silicon nitride (SiN) layer, around 1.5 nm, was formed by controlled nitridation in NH_3 [15]. Then, a $Hf_{0.5}Zr_{0.5}O_2$ (HZO) layer with a thickness of 10 nm was grown by atomic layer deposition (ALD), followed by a 40-nm-thick TiN layer. The HZO layer was deposited in a superlattice structure by alternating ALD cycles of HfO_2 and ZrO_2. The growth of both oxides was calibrated on test samples prior to deposition on the device structures. Films with various HfO_2–ZrO_2 cycle ratios were deposited, and their thickness and composition were measured using X-ray reflectometry (XRR) and TEM to determine the corresponding deposition rates. An annealing at 450 °C for 30 s was performed to form the ferroelectric orthorhombic phase in the HZO layer. The thin SiN layer can improve the ferroelectricity, as confirmed by the polarization–voltage (P–V) measurements in a test capacitor [see Fig. 1(f)]. It shows a stronger remnant polarization in comparison to the device without SiN. The reason is that the interfacial quality is improved by the SiN interfacial layer. Furthermore, the SiN layer has a higher dielectric constant than SiO_x, which is otherwise formed in the HZO/Si interface for the reference sample with HZO directly deposited on Si. This means that a higher portion of the voltage is applied over the HZO layer in the HZO/SiN stack than in the HZO/SiO_x structure, resulting in a stronger remnant polarization of the HZO/SiN stack [16]. Further details on the SiN-layer-induced improvements in HZO ferroelectricity are provided in [17]. Thereafter, the gate-stack was patterned by e-beam lithography

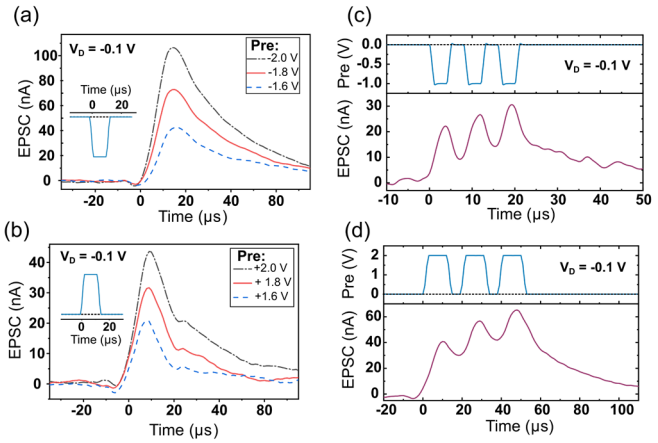

Fig. 2. (a) Negative or (b) positive applied presynaptic spike generates an EPSC spike at the source with different neurotransmitters. A higher absolute amplitude of the prespike generates an EPSC with a larger amplitude. (c) and (d) PPF characteristics of the synapse, where EPSC increases gradually with the number of pulses.

followed by dry etching of the TiN and HZO. The top 40-nm TiN was etched using reactive ion etching (RIE) CHF_3/O_2 plasma. This was followed by RIE etching of HZO and SiN layers in CHF_3/Ar plasma. NiSi was formed at the source/drain regions, with a self-aligned silicidation process by annealing an 8-nm-thick Ni layer at 500 °C. The final device structure is shown by a cross-sectional TEM image in Fig. 1(d). The HfO_2–ZrO_2 superlattice structure is confirmed by the energy-dispersive X-ray spectroscopy (EDX) mapping shown in Fig. 1(e). Finally, contact holes were etched, and a Pt layer was deposited to form contacts, connections, and circuits.

III. Synapse Based on a Single Fe-SBFET

Fig. 1(a) illustrates a biological synapse, where excitatory and inhibitory neurotransmitters differentially modulate the activity of the postsynaptic neuron. Leveraging its ambipolar characteristics, the Fe-SBFET can emulate such synaptic behavior by applying either a negative or positive presynaptic voltage spike to the gate, as shown in Fig. 1(b) and (c). This results in an excitatory or inhibitory postsynaptic current (EPSC), with holes or electrons serving as the charge carriers in the channel.

The ambipolar switching behavior of an FE-SBFET with a 200-nm gate length is presented in Fig. 1(g). The polarization of the ferroelectric HZO layer induces a clockwise hysteresis in the p-FET regime and a counterclockwise hysteresis in the n-FET regime. For p-FET operation, the device exhibits an ON/OFF current ratio exceeding four orders of magnitude and a memory window of 0.9 V. In the n-FET regime, an ON/OFF ratio of three orders of magnitude with a 0.7-V memory window is achieved. The lower ON-currents of the n-FET are caused by the higher Schottky barrier of NiSi to electrons than to holes. These results demonstrate that the Fe-SBFET can effectively operate as an artificial synapse, using either holes or electrons to mimic excitatory and inhibitory neurotransmission, respectively.

Fig. 2 shows the measured synaptic behavior of a single Fe-SBFET under negative [see Fig. 2(a)] and positive [see

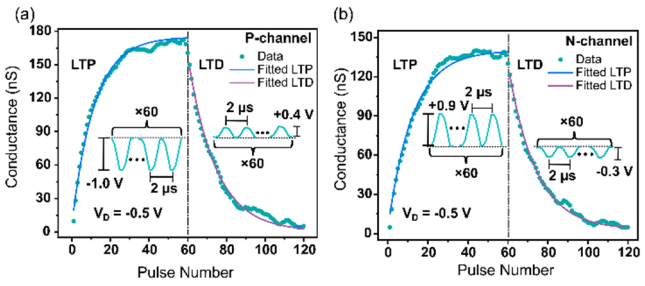

Fig. 3. (a) LTP/LTD characteristics of the synapse when (a) holes or (b) electrons, are the conductance carriers (neurotransmitter). LTP is achieved by applying (a) negative or (b) positive voltage pulses at the gate, while LTD is realized by applying a smaller pulse with opposite polarity to the LTP pulse.

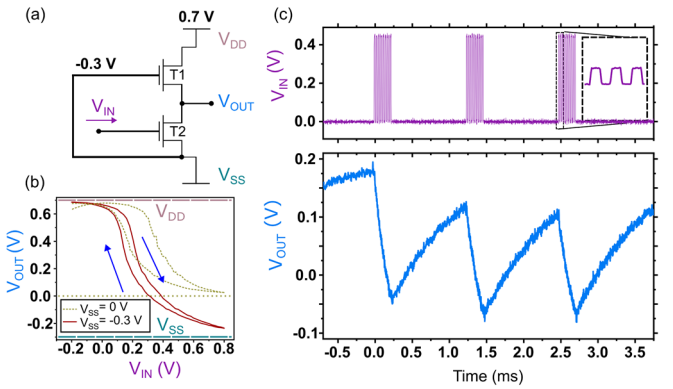

Fig. 4. (a) QIN circuit using only two Fe-SBFETs ($T1$ and $T2$), where the gate of $T1$ is connected to the source of $T2$, and the input voltage V_{IN} is applied to the gate of $T2$. (b) Measured VTC of the QIN circuit, with an increased V_{IN}, the output voltage V_{OUT} is switched from high to low for V_{SS} of −0.3 and 0 V. (c) Ten positive pulses with an amplitude of 0.44 V are applied at V_{IN}, (V_{SS} = −0.3 V) (zoomed-in view of the inset). A spike V_{OUT} from 0.18 to −0.05 V is generated. The neuron resets in ∼1 ms, and another ten pulses applied at V_{IN} can repeat the spike generation.

Fig. 2(b)] gate voltage spikes, applied as presynaptic stimuli. As observed in both figures, presynaptic spikes with higher amplitudes produce correspondingly larger EPSC responses, demonstrating effective synaptic weight modulation. When a series of closely spaced voltage pulses is applied, the EPSC gradually increases due to cumulative memory effects, as shown in Fig. 2(c) and (d) for a representative sequence of three pulses. This behavior is characteristic of short-term synaptic plasticity, specifically paired-pulse facilitation (PPF). The observed EPSC retention is attributed to the remnant polarization of the ferroelectric layer, which allows charge carriers to persist in the channel even after the presynaptic pulse is removed. This retention effect contributes to the enhanced EPSC, enabling memory-like behavior in the device.

The long-term potentiation and depression (LTP/LTD) characteristics of the Fe-SBFET synapse are demonstrated in Fig. 3(a) and (b), corresponding to operation in the p-FET and n-FET modes, respectively. An energy consumption as low as 28 fJ/state has been calculated, underscoring the high energy efficiency of the device. The energy consumption was calculated by multiplying the drain voltage and the drain current and integrating the value over the duration of the applied weight-update pulse at the gate. Then take the average of all weight updates during LTP and LTD over three complete cycles. By leveraging both p-type and n-type operation, the Fe-SBFET is capable of emulating excitatory and inhibitory neurotransmission. This mimics the functionality of biological synapses, which use neurotransmitters such as glutamate (excitatory) and gamma-aminobutyric acid (GABA) (inhibitory) to adaptively transmit signals based on environmental stimuli. Replicating this dual-mode functionality in artificial synapses is essential for developing advanced neuromorphic systems and adaptive robotics that can respond dynamically to different conditions [18]. Furthermore, this capability opens the door to designing more complex neuron circuits using Fe-SBFETs, enabling the realization of brain-inspired computing architectures with higher functional diversity and scalability.

IV. Neurons Based on Fe-SBFETs

A. IF-Neuron Based on Two Fe-SBFETs

We propose a compact neuron based on a quasi-inverter circuit, comprising only two Fe-SBFETs [see Fig. 4(a)]. In this quasi-inverter neuron (QIN) configuration, the gate of $T1$ is connected to the source of $T2$, such that only the conductance of $T2$ is modulated by the input voltage V_{IN}. As V_{IN} increases, the output voltage V_{OUT} correspondingly decreases toward V_{SS}. As shown in Fig. 4(b), the voltage transfer characteristics (VTCs) resemble those of a CMOS inverter, with performance dependent on the value of V_{SS}. At V_{SS} = 0 V (dashed curve), V_{OUT} transitions from 0.6 to 0.15 V, achieving a voltage gain of 1.7 V/V. When V_{SS} is reduced to −0.3 V, the transition improves significantly: V_{OUT} spans from 0.6 to −0.2 V, and the voltage gain increases to 2.3 V/V. Owing to the remnant polarization of the ferroelectric layer, the QIN exhibits a clockwise hysteresis loop with a memory window of 80 mV at V_{SS} = −0.3 V. Notably, the conductance of $T1$ is governed solely by V_{SS}; a more negative V_{SS} leads to a smaller switching voltage of $T2$, allowing a smaller transition voltage.

This behavior can be exploited in a neuron implementation, as illustrated in Fig. 4(c), where V_{IN} is applied as a series of pulses with an amplitude of 0.44 V, a duration of 10 μs, and an interpulse interval of 10 μs. The resulting output voltage spikes, V_{OUT}, progressively decrease from 0.18 to −0.05 V over 0.2 ms. This voltage decay behavior resembles that of an IF neuron, where V_{OUT} can be accurately modeled by a first-order exponential discharge of a capacitor

$$V_{OUT} = V_{DD}e^{-t/\tau} + V_0 \quad (1)$$

where V_{DD} is the spike output voltage, V_0 is the reset voltage, τ is the self-reset decay time constant, which was fit to a value of 1.05 ms. This results in a spike generation frequency of 0.81 kHz and an energy consumption of 0.67 pJ/spike. We show here only the results with V_{SS} = −0.3 V because the circuit shows a larger transition voltage range and voltage gain. A lower absolute value of V_{SS} and the voltage bias configuration as a normal inverter result in much lower output spikes. Furthermore, for the reset, any parasitic capacitances between $T1$ and $T2$ need to be discharged with the current

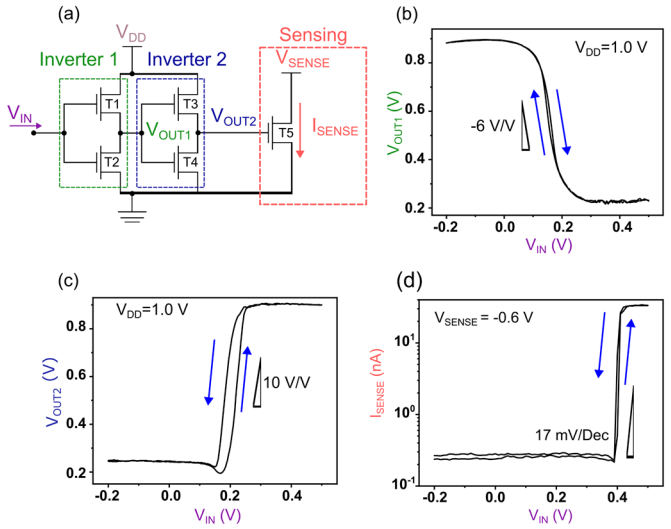

Fig. 5. (a) Schematic of a double inverter neuron circuit based on five Fe-SBFETs ($T1$–$T5$). Two inverters (inverter 1 with $T1$ and $T2$, inverter 2 with $T3$ and $T4$) and a sensing FET ($T5$) are connected in series. (b) Measured VTC for inverter 1 showing a gain of 6 V/V. (c) Inverter 2 showing a gain of 10 V/V, both at a V_{DD} = 1.0 V. (d) Transfer characteristics of the sensing current I_{SENSE} from $T5$ as a function of the applied input V_{IN}, showing very steep slope of 17 mV/dec due to the amplification of the double inverters.

through $T1$. A lower absolute voltage of V_{SS} decreases the current and thus limits the minimum reset time, which could make the reset time slower.

B. Thalamic Neuron Based on Five Fe-SBFETs

We fabricated a more advanced neuron circuit using multiple Fe-SBFETs to achieve more functions. Fig. 5(a) shows a double inverter neuron circuit schematic based on only five identical Fe-SBFETs ($T1$–$T5$) without capacitors and resistors. This circuit is based on inverters in comparison to the previous one. The neuron consists of a series connection of three components: double inverters ($T1$–$T4$) and a sensing FET $T5$. The inverter behaves similar to the conventional CMOS inverter. The output voltage of inverter 1 V_{OUT1} switches from high to low, as shown in the VTC in Fig. 3(b), with a voltage gain of 6 V/V. Compared with long-channel devices reported in [14], V_{DD} is lowered since the small gate length results in a larger voltage across the Schottky barrier.

Consequently, the inverter 2 inverts the V_{OUT1}, causing V_{OUT2} to switch from low to high. Fig. 3(c) shows the VTC of inverter 2, demonstrating a voltage gain of 10 V/V to V_{IN}. The gain of inverter 2 is further increased compared with inverter 1 due to the double amplification of the two inverters. Due to the remnant polarization of the ferroelectric layer, V_{OUT2} shows a clockwise hysteresis with a width of 50 mV, which is much smaller than that of a single Fe-SBFET because the two FETs operate complementarily. Furthermore, the applied voltages are far below the coercive field for completely switching the ferroelectric domains, resulting in a smaller hysteresis.

Next, V_{OUT2} is applied to the gate of $T5$ to modulate the conductance of the transistor. By applying a drain voltage V_{SENSE}, the conductive state is read out as the drain current I_{SENSE} in $T5$. Fig. 3(d) shows the I_{SENSE}–V_{IN} characteristics,

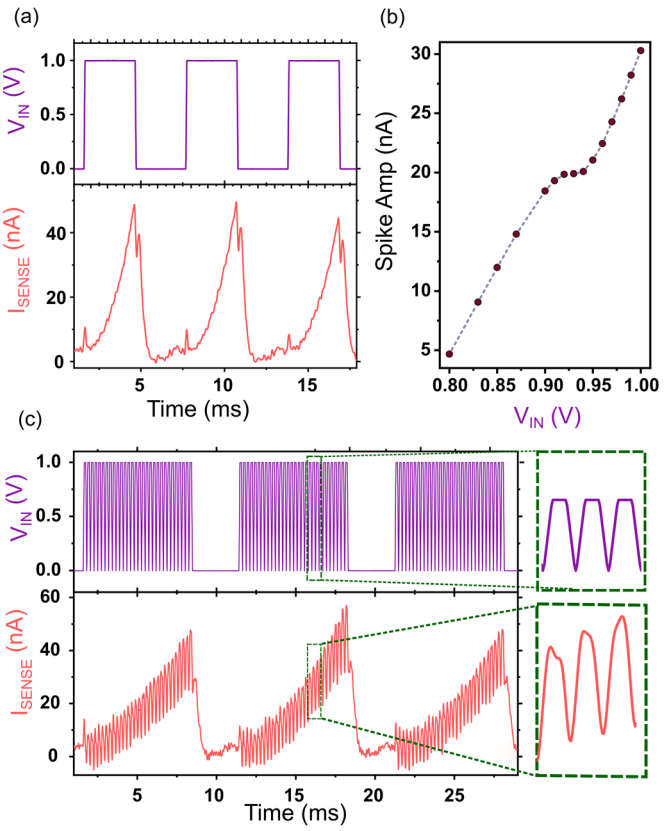

Fig. 6. (a) Long pulses with 3-ms pulsewidth and an amplitude of 1.0 V applied at the neuron's input result in LIF function of the neuron (tonic mode): an integration period followed by the generation of a spike when the I_{SENSE} reaches around 50 nA. After the pulse, the neuron resets. (b) Amplitude of the generated spikes increases with the amplitude of V_{IN}. (c) Shorter pulses with a width of 100 μs and an interval of 20 μs generate a burst of spikes, as demonstrated in the inset after a zoomed-in view of the I_{SENSE}.

displaying a very steep slope of 17 mV/dec, which is caused by the amplification of the double inverters. These properties, where the current can increase fast from one state to the other at a certain threshold, but otherwise remain stable, which is suitable for the spiking generation, combined with the memory needed for integration, are excellent for an artificial neuron.

In the following, we demonstrate that this five-FeFET circuit can function as an artificial thalamic neuron. The circuit is biased at V_{DD} = 1.0 V and V_{SENSE} = −0.6 V. As illustrated in Fig. 6(a), we first characterize the neuron characteristics by applying long voltage pulses at V_{IN}, each with a duration of 3 ms and an amplitude of 1.0 V. The applied input voltage pulse gradually switches the ferroelectric domains in $T1$ and $T2$, increasing polarization across the ferroelectric layer of $T2$ while depolarizing the HZO layer in $T1$. After a certain number of pulses, $T1$ switches OFF, and $T2$ turns on. Consequently, V_{OUT1} decreases and V_{OUT2} increases, activating $T5$ and generating a current spike in I_{SENSE}. The generated I_{SENSE} spikes show a LIF neuron function (tonic mode) with self-resetting taking place in 90 μs after the end of the input pulse. The self-resetting is caused by the exponential decay of the remnant polarization after removal of the applied voltage [19] as the applied voltage is below the coercive field. The endurance of a FeFET is linked to the resulting voltage applied

TABLE I
BENCHMARKING OF THE NEURONS IN THIS WORK WITH STATE-OF-THE-ART ARTIFICIAL NEURONS

	This Work		**[9]**	**[11]**	**[12]**	**[14]**
	Thalamic	**QIN**				
Device Type	Fe-SBFET		VCM	FeFET	FeFET Anti-Ferro	Fe-SBFET
CMOS Tech.	Yes		No	Yes	Yes	Yes
Circuit	5 Fe-SBFET	2 Fe-SBFET	3R-1C	2T-1Fe-FET-1R	8T-1 FeFET	4 Fe-SBFET
V_{IN} (V)	1.0	0.44	8	1.8	1.5	1.0 V
Energy Consumption	2.6 pJ	0.67 pJ	1.6 nJ	420 pJ	6 pJ	40 pJ
Freqency (kHz)	5.6	0.81	0.033	0.1	0.5	8.3
Function	LIFB/LIF	IF	LIF	LIF	LIFB	LIF

over the interfacial layer between the ferroelectric and channel. This means that an overall lower operating voltage results in increased endurance of synapses and neurons in this work [20]. The amplitude of the generated spikes increases almost linearly with the input amplitude if it is above the threshold for spiking generation, around 0.8 V, as shown in Fig. 6(b).

Applying shorter input pulses, each with a duration of 100 μs and an interval of 20 μs, induces bursting behavior in the neuron, as shown in Fig. 6(c). The neuron initially responds with small output current spikes to each input pulse, and the spike amplitude gradually increases until a full firing event occurs. The resulting spike generation during bursting has a frequency of 5.6 kHz. The neuron resets in 500 μs after the applied voltage pulses stop. Since more pulses are used than the tonic mode shown in Fig. 6(a), which results in more robust remnant polarization, the self-resetting time is longer.

In conclusion, the neuron can function as a LIF or burst (LIFB) neuron, similar to the thalamic neuron in the brain's thalamus cortex [21]. The biological thalamic neurons can generate bursts during sleep to classify certain events, and the information is less sensitive to noise. If persistent or strong enough external stimuli keep arriving, they can gradually depolarize the neuron. The single tonic spike can transport more detailed information. This allows the brain to rapidly detect and react to stimuli, which is essential for attention, perception, and decision-making in real time. Since biological thalamic neurons are essential, for example, for consciousness and movements, artificial thalamic neurons can be used in, for instance, microrobots and autonomous driving [22], [23].

V. CONCLUSION

In summary, neurons composed of two or five Fe-SBFETs have been demonstrated to exhibit IF and LIF/LIFB functionalities. Table I benchmarks the performance of our neuron circuits against state-of-the-art artificial neurons. Compared with other works, our design uses a minimal number of a single device type—without requiring additional capacitors (C), resistors (R), or conventional CMOS transistors (T), while achieving a broader range of neuron functions with lower energy consumption. Furthermore, we demonstrate that scaling down the Fe-SBFET and optimizing its gate-stack significantly reduces energy usage. Reducing the number of transistors from four to two not only lowers energy consumption but also minimizes the circuit area. The integration of both synaptic and neuronal behaviors in Fe-SBFETs presents a highly promising platform for future energy-efficient NC.

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