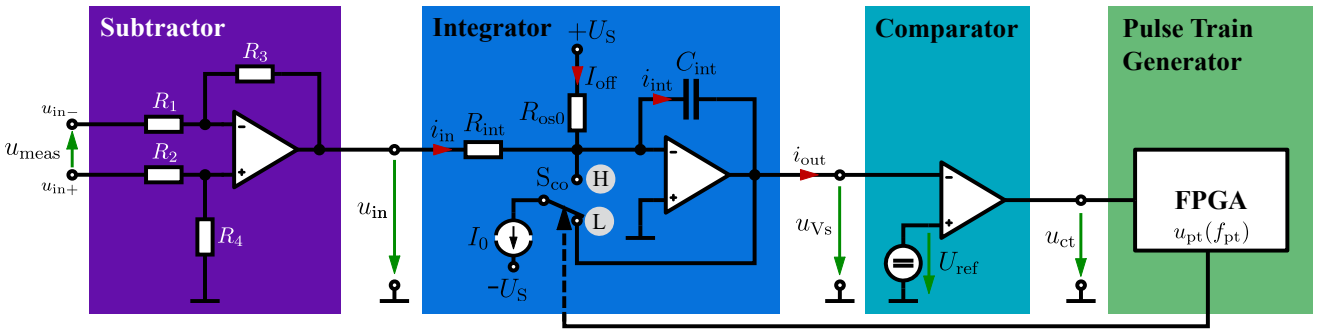
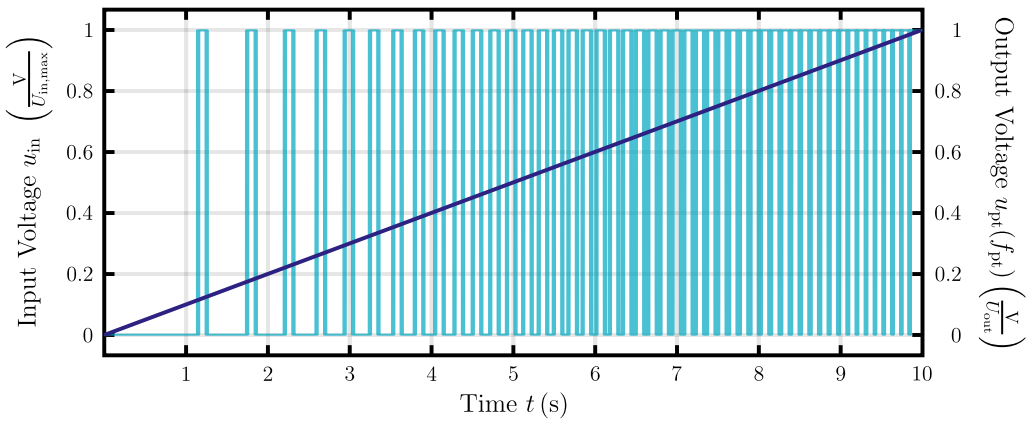
Anne von Hoegen

Precise and Instantaneous Flux-Linkage Sensing Methods in PWM Voltage-Source Inverters





Aachener Beiträge des ISEA Band 193

Precise and Instantaneous Flux-Linkage Sensing Methods in PWM Voltage-Source Inverters

Von der Fakultät für Elektrotechnik und Informationstechnik der Rheinisch-Westfälischen Technischen Hochschule Aachen zur Erlangung des akademischen Grades eines Doktors der Ingenieurwissenschaften genehmigte Dissertation

vorgelegt von
Anne von Hoegen, M.Eng.
aus Soller (Vettweiß)

Berichter:
Univ.-Prof. Dr. ir. Dr. h. c. Rik W. De Doncker
Univ.-Prof. Dr.-Ing. Stefan Heinen

Tag der mündlichen Prüfung: 30. Januar 2025

AACHENER BEITRÄGE DES ISEA
Vol. 193

Editor:
Univ.-Prof. Dr. ir. Dr. h. c. Rik W. De Doncker
Director of the Institute for Power Electronics and Electrical Drives (ISEA)
RWTH Aachen University

ISSN 1437-675X

Institute for Power Electronics and Electrical Drives (ISEA)
RWTH Aachen University
Campus Boulevard 89 • 52074 Aachen • Deuschland
Tel: +49 (0)241 80-96920
post@isea.rwth-aachen.de

Abstract

Precise knowledge of magnetic flux-linkage is a fundamental requirement for high-preformance control of electrical machines. Conventional estimation methods – whether based on current look-up tables or voltage integration – are prone to significant errors arising from steep PWM voltage slopes, high-frequency components, and inverter-related switching delays, particularly in SiC and GaN systems To address these limitations, this dissertation develops and evaluates novel volt-second sensor concepts that directly measure flux-linkage by combining continuous analog voltage sensing with FPGA-based digital processing.

The work introduces six new measurement architectures, including feed-forward voltage-distortion modeling for IGBT-based inverters as well as asynchronous and synchronous voltage-to-frequency converter designs These converters translate continuous phase-voltage signals into discrete volt-second values that can be processed in real time, overcoming the accuracy and implementation constraints inherent to purely analog or purely digital approaches.

A comprehensive comparative study evaluates fourteen measurement methods under varying operating points on an industrial half-bridge test bench. The analysis covers measurement accuracy, instantaneousness, and cost, and includes application-oriented validation on a traction-drive test bench The results demonstrate that the proposed sensor concepts enable precise and instantaneous determination of flux-linkage and corresponding phase voltage, while the underlying hardware can be flexibly adapted to different control algorithms through modifications in the FPGA-based evaluation logic.

Overall, the dissertation establishes a unified measurement framework that leverages complementary analog and digital technologies to overcome long-standing challenges in PWM voltage sensing. The introduced volt-second sensors provide a robust basis for enhancing control accuracy in modern electric-drive inverters and open new avenues for future research and technological advancement.

Contents

1 Introduction

1.1 Motivation, Goal and Task of this Work

Many control methodologies for electrical machines depend on the magnetic flux-linkage as a key variable. Most torque controllers are based on field-oriented control algorithms in which the amplitude and position of the flux-linkage is indispensable. This variable is typically calculated either utilizing current-based look-up tables (LUTs) or integrating the measured pulse width-modulation (PWM) voltage. Though, measuring pulse-modulated voltage accurately can be challenging due to its steep slopes, especially when dealing with silicon carbide (SiC) and gallium nitride (GaN) inverters. Additionally, high-frequency voltage components and time delays during switching further complicate this process especially in the low-speed range. Typical measurement methods for PWM voltages involve sample-and-hold (S&H) procedures with successive-approximation-register (SAR) analog-to-digital converters (ADCs), which may not effectively capture the applied phase voltage.

This dissertation focuses on direct, accurate, and instantaneous measurement of magnetic flux-linkage of electrical machines to prevent inaccuracies in voltage measurement or the conversion using LUT, respectively. This research aims to design and assess multiple volt-second sensors and a straightforward voltage-source inverter (VSI) simulation model that replicates volt-second inaccuracies if sensor technology is absent. Progress is made on the formulation of evaluation algorithms that utilize commercial voltage-to-frequency converter (VFC) integrated circuits (ICs), and, moreover, a design of an innovative volt-second sensor is presented merging the benefits of continuous voltage sensing of analog circuit technology with the execution of an field-programmable gate array (FPGA). A mathematical mapping of the simulation model enables its utilization as a feedforward measurement strategy.
The performances of the new volt-second evaluation approaches, the novel volt-second sensor, and the model-based approach are evaluated by contrasting them with conventional voltage measurement techniques. Therefore, the author conducts and appraises the measurement methodologies developed within this thesis, promising measurement methods in science, and industry-standard measurement procedures on the test bench for a comparative study. The main target is for the newly innovated volt-second sensor to outperform other partially already existing, partially newly developed measurement methods in terms of accuracy, instantaneousness, and cost effectiveness.

1.2 Major Scientific Contributions and Outline

The success of algorithms depends along with other things on the precision of their recorded control variable. If the actual variable is defective, achieving the desired reference value cannot be attained. Consequently, if the measured quantity is more precise, the control algorithm operates with higher accuracy. Therefore, many scientists focused on measuring instantaneous voltage for PWM VSIs to obtain an accurate average phase voltage value per PWM period for the control algorithm. Nevertheless, the direct sensing of the applied volt-second is not given appropriate attention. The contribution of this study effectively covers the gap in research, emphasizing the impact of small duty cycle and phase currents on volt-second deviation in the low-speed range.

The volt-second distortions of a VSI are examined comprehensively, mirroring findings from earlier research. However, this investigation revised common mathematical inaccuracies present in scholarly writings and subsequently validates the simulation model and its mathematical representation through measurements conducted on the test bench. Through this profound knowledge of the behavior of voltage trajectories in PWM VSIs, various approaches for measuring volt-seconds and voltages have been established. Initially, the author explores the characteristics of commercial VFCs by utilizing them for instantaneous voltage sensing before developing a specialized volt-second sensor to meet VSI requirements. This novel volt-second sensor combines both analog and digital technologies in a holistic measurement approach. The layout and design of the highest-performing volt-second sensor are presented based on various inverter-specific requirements. Moreover, the author details the deriving of the corresponding applied phase voltage from the measured magnetic flux-linkage if this quantity is necessary for the user. This determined phase-voltage is then juxtaposed in an unprecedented comparative study in terms of accuracy, standard deviation and cost. Afterward, the volt-second sensor is installed on a motor test bench to assess its capability in dielectric strength and electromagnetic compatibility (EMC) coupling. In conclusion, the author demonstrates how VFC-based measurement approaches serve to measure the flux-linkage of electrical machines for PWM-less control algorithms.

These major scientific contributions are elaborated across five chapters in the dissertation. Besides the introduction, the written version starts with the fundamentals of voltage sensing for electrical machines and focuses on two main components of the electrical drivetrain – inverter and electrical machine – as well as the basics of instantaneous voltage measuring. Additionally, the text describes the basic operating principle of VFCs as they are key features of the innovative volt-second sensor technology.
The core of the dissertation lies in the third chapter, where four novel measurement techniques for the magnetic flux-linkage and one for voltage are introduced and discussed. The opening section delves into accurately modeling of insulated-gate bipolar transistor (IGBT)-based three-phase VSIs and validates its mathematical model on the test bench. This feed-forward voltage-distortion model is implemented and combined with an ADC to assign the determined phase-voltage value for comparison. The second sec-

tion introduces measuring techniques applying the sensor family of VFCs. Asynchronous voltage-to-frequency converters (AVFCs) and synchronous voltage-to-frequency converters (SVFCs) rely on the following analog technology: They convert the continuously measured PWM voltage into discrete volt-second quantities that are passed to various developed evaluation logic implemented in the FPGA. While these approaches ensure high levels of accuracy, they have disadvantages in IC costs. Therefore, in the following section a discrete synchronous voltage-to-frequency converter (dSVFC) sensor is developed based on the working principle of the corresponding commercial SVFC IC. The dSVFC sensor is thoroughly synthesized, analyzed and optimized before incorporating it into the final measurements for comparison in Chapter 4.
An evaluation is conducted on 14 measurement methods examining accuracy, instantaneousness and cost. All measurement techniques are tested and evaluated on a standard industrial IGBT-based half-bridge with a constant phase current source as load. The construction of this evaluation setup is specifically intended to meet the requirements of a comprehensive and thorough investigation. All measurement circuits are tested regarding their preciseness in the range of low phase currents. Therefore, the established test bench allows for adjusting both the reference duty cycle and reference constant phase current to investigate the measurement deviation of the measurement circuits for different operating points (OPs). The assessment method for the measurement results is outlined in conjunction with the dedicated test bench. After this, a comprehensive review is undertaken on the 14 measurement methodologies to determine their measuring accuracy, and subsequently, they are directly compared based on statistical values. Additionally, the costs are examined for the investigated measurement techniques. Within this chapter, the author extensively studies the dSVFC for its potential utilization in volt-second sensing on a traction drive test bench evaluated in the next section. Therefore, two dSVFCs are implemented to measure the phase-to-phase voltage focusing on dielectric strength, EMC, and also precision. At the end of Chapter 4, the author also demonstrates how the same hardware sensor can be adjusted for PWM-less control algorithms by modifying the employed evaluation algorithm of volt-seconds.
Finally, the dissertation finishes with the conclusion and suggests remaining future tasks.

2 Fundamentals of Voltage Sensing for Permanent Magnet Synchronous Machines

This chapter introduces all fundamental topics required to understand the various topics of this thesis. At the beginning, it considers a model approach of the permament magnet synchronous machine (PMSM) and introduces the magnetic flux-linkage as an essential parameter for torque control and a wide variation of control methodologies. The benefits of having precise knowledge of flux-linkage are discussed along with state-of-the-art methods used to determine it. As VSIs provide the flux-linkages in the machine, the following section presents a standard three-phase inverter with its voltage distortion and demonstrates where to effectively measure the flux-linkage.
To demonstrate the method for measuring flux-linkage in this study, the author introduces the operating principle of voltage-to-frequency converters (VFCs) below as they will be the basis of novel developed volt-second measuring principles. This chapter concludes by explaining the concept of instantaneousness in relation to voltage and flux-linkage measurement methods.

2.1 Model and Control of Salient Permanent Magnet Synchronous Machines

This thesis focuses, without loss of generality, on modeling and controlling three-phase AC PMSMs. However, this concentration does not disregard other categories of electrical machines like e. g. induction machines (IMs) or switched reluctance machines (SRMs). In addition, the measurement approaches introduced and developed in this research have the opportunity that they are not limited to flux-linkage sensing for electrical machines but can be utilized across various types of flux-linkage and voltage measurements, respectively.

2.1.1 Dynamic Model of Salient Permanent Magnet Synchronous Machines

This first section focuses on modeling three-phase AC salient synchronous machines (SMs) with stator windings distributed in a quasi-sinusoidal manner. A popular type of salient

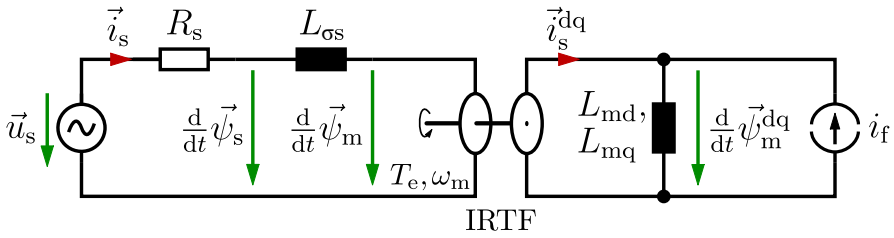


Figure 2.1: Synchronous machine model with salient rotor

SM is the interior permament magnet synchronous machine (IPMSM) which carries magnets within the rotor lamination. The machine model of the IPMSM is explained through the ideal rotating transformer (IRTF) model [1] shown in the rotor-oriented dq-frame in Fig. 2.1. Besides stator resistance R_s and stator leakage inductance $L_{\sigma\mathrm{s}}$, it incorporates the rotor-side magnetizing inductance L_md and L_mq of the machine.
When the inductance L_md is paired with the current source i_f, the rotor-side of the model displays the flux-linkage ψ_f of the permanent magnet excitation. Additionally, the rotor position affects the reluctance of salient SMs, such as IPMSMs with their magnets in the rotor lamination. For this reason, for PMSMs the real axis of the dq-reference frame is per definition locked to the direction of field flux-linkage ψ_f [2].

Rearranging the inductances $L_{\sigma\mathrm{s}}$, L_md, and L_mq of the symbolic model enables the deduction of the salient rotor-flux-based model in equation (2.1) consisting of stator voltage $\vec{u}_\mathrm{s}^{\,\mathrm{dq}}$ (equation (2.1a)), stator flux-linkage $\vec{\psi}_\mathrm{s}^{\,\mathrm{dq}}$ (equation (2.1b)), and electric torque T_e (equation (2.1c)) in dq-frame [3].

$$\vec{u}_\mathrm{s}^{\,\mathrm{dq}} = R_\mathrm{s}\vec{i}_\mathrm{s}^{\,\mathrm{dq}} + \frac{\mathrm{d}\vec{\psi}_\mathrm{s}^{\,\mathrm{dq}}}{\mathrm{d}t} + \mathrm{j}\omega_\mathrm{s}\vec{\psi}_\mathrm{s}^{\,\mathrm{dq}} \tag{2.1a}$$

$$\vec{\psi}_\mathrm{s}^{\,\mathrm{dq}} = L_\mathrm{sd} i_\mathrm{sd} + \mathrm{j}L_\mathrm{sq} i_\mathrm{sq} + \psi_\mathrm{f} \tag{2.1b}$$

$$T_\mathrm{e} = \underbrace{\frac{3}{2}\psi_\mathrm{f} i_\mathrm{sq}}_{\text{electromagnetic torque}} + \underbrace{\frac{3}{2}\left(L_\mathrm{sd} - L_\mathrm{sq}\right) i_\mathrm{sd} i_\mathrm{sq}}_{\text{reluctance torque}} \tag{2.1c}$$

The equation set basically relies on the knowledge of the stator current $\vec{i}_\mathrm{s}^{\,\mathrm{dq}}$, the stator resistance R_s, and the electrical angular frequency ω_s. The stator inductances L_sd and L_sq, along with the flux-linkage $\vec{\psi}_\mathrm{s}^{\,\mathrm{dq}}$, are not linearly dependent on the present stator current value $\vec{i}_\mathrm{s}^{\,\mathrm{dq}}$ due to saturation effects or temperature [1]. Thus, the stator inductances as well as the flux-linkage are typically established through finite element (FE)-simulations and then stored in LUTs [4].

The equation set is now adjusted to exclusively correlate with the stator flux-linkage $\vec{\psi}_\mathrm{s}^{\,\mathrm{dq}}$, which in turn depends on the stator current components i_sd and i_sq (equation (2.2) [5]).

$$\vec{u}_{\mathrm{s}}^{\,\mathrm{dq}} = R_{\mathrm{s}}\vec{i}_{\mathrm{s}}^{\,\mathrm{dq}} + \frac{\mathrm{d}\vec{\psi}_{\mathrm{s}}^{\,\mathrm{dq}}\left(i_{\mathrm{sd}}, i_{\mathrm{sq}}\right)}{\mathrm{d}t} + \mathrm{j}\omega_{\mathrm{s}}\vec{\psi}_{\mathrm{s}}^{\,\mathrm{dq}}\left(i_{\mathrm{sd}}, i_{\mathrm{sq}}\right) \tag{2.2a}$$

$$\vec{\psi}_{\mathrm{s}}^{\,\mathrm{dq}} = \left(L_{\mathrm{sd}} i_{\mathrm{sd}} + \psi_{\mathrm{f}}\right) + \mathrm{j}\left(L_{\mathrm{sq}} i_{\mathrm{sq}}\right) = \psi_{\mathrm{sd}}\left(i_{\mathrm{sd}}, i_{\mathrm{sq}}\right) + \mathrm{j}\psi_{\mathrm{sq}}\left(i_{\mathrm{sd}}, i_{\mathrm{sq}}\right) \tag{2.2b}$$

$$T_{\mathrm{e}} = \frac{3}{2} \cdot \left[\psi_{\mathrm{sd}}\left(i_{\mathrm{sd}}, i_{\mathrm{sq}}\right) \cdot i_{\mathrm{sq}} - \psi_{\mathrm{sq}}\left(i_{\mathrm{sd}}, i_{\mathrm{sq}}\right) \cdot i_{\mathrm{sd}}\right] \tag{2.2c}$$

By exclusively having information on the stator current $\vec{i}_{\mathrm{s}}$, the stator flux-linkage $\vec{\psi}_{\mathrm{s}}$, and the rotorposition θ_{r} for the Clarke and Park transforms, the acquired equation set allows for the torque calculation (equation (2.2c)). When the stator flux-linkage is − like the phase current − precisely measured, the determination of torque operates using only independent variables. In addition, the frequently utilized flux-linkage as a control variable can be directly accessed for control algorithms, which will be outlined in excerpts in the following subsection.

2.1.2 Determination of Stator Flux-Linkage

A powerful control technique is e. g. deadbeat (DB) direct torque and flux control (DTFC) that accurately regulate machine torque within one control interval [6]–[8]. In addition to controlling the torque, this strategy also regulates the flux-linkage, requiring the use of flux-observers like for SRMs [9], [10] or IMs [11], [12], especially at low-speed operation [13]. An extensively employed flux-observer is the gopinath-style flux-observer in both continuous [14]–[17] and discrete time [18] implementations. Hence, LUTs and flux-observers are obsolete if the magnetic flux-linkage is accessible, which preserves both computing capabilities and storage limits which compromise the preciseness of the calculated quantity [19]–[22].

The question now arises, how to ascertain the stator flux-linkage $\vec{\psi}_{\mathrm{s}}$ by installing a measuring instrument within the electric drivetrain. Since the stator flux-linkage $\vec{\psi}_{\mathrm{s}}$ is difficult to access physically, the stator voltage $\vec{u}_{\mathrm{s}}$ as the input quantity at the terminals of the machine will be the quantity of interest to determine the stator flux-linkage of the SM model. Accordingly, the volt-second sensor developed in this thesis is connected to the stator voltage $\vec{u}_{\mathrm{s}}$ to measure the flux-linkage $\vec{\psi}_{\mathrm{ph}}^{\,\Diamond}$ at the terminals of the machine (Fig. 2.2). It is common practice to quantify the stator resistance $R_{\mathrm{s}}^{\Diamond}$ (or the impedance of the machine, respectively) before commissioning and to measure the stator current $\vec{i}_{\mathrm{s}}^{\,\Diamond}$ in operation. Hence, the author proceed with the assumption that those three quantities are available through sensors at the test bench. These measurements enable the calculation of the stator flux-linkage $\vec{\psi}_{\mathrm{s}}$ like shown in equation (2.3).

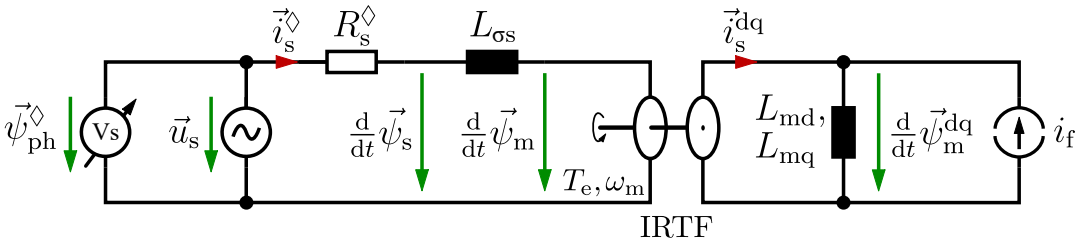


Figure 2.2: Synchronous machine model with measured terminal flux-linkage $\vec{\psi}_{\mathrm{ph}}^{\,\lozenge}$

$$\vec{\psi}_{\mathrm{s}} = \vec{\psi}_{\mathrm{ph}}^{\,\lozenge} - R_{\mathrm{s}}^{\lozenge} \int \vec{i}_{\mathrm{s}}^{\,\lozenge}\,\mathrm{d}t \tag{2.3}$$

At this point, it is essential to clarify the terminology; Fig. 2.2 and equation (2.3) show that the stator flux-linkage $\vec{\psi}_{\mathrm{s}}$ differs from the terminal flux-linkage or phase flux-linkage $\vec{\psi}_{\mathrm{ph}}$, while the stator voltage $\vec{u}_{\mathrm{s}}$ is equal the terminal voltage or phase voltage $\vec{u}_{\mathrm{ph}}$ (equation (2.4a)). Moreover, the stator current $\vec{i}_{\mathrm{s}}$ is equivalent to the phase current $\vec{i}_{\mathrm{ph}}$ at the terminals of the machine (equation (2.4b)).

$$\vec{u}_{\mathrm{s}} = \vec{u}_{\mathrm{ph}} \tag{2.4a}$$

$$\vec{i}_{\mathrm{s}} = \vec{i}_{\mathrm{ph}} \tag{2.4b}$$

In the context of electrical machines, the terminology of stator values are commonly used, whereas phase values are more prevalent related to VSIs, hence the need to introduce these distinct variables (equation (2.4)). The stator current $\vec{i}_{\mathrm{s}}$ and the stator voltage $\vec{u}_{\mathrm{s}}$ and, thus, the terminal flux-linkage $\vec{\psi}_{\mathrm{ph}}$ is commonly applied to the electrical machine and controlled by a VSI, which will be delved into the upcoming section.

2.2 Voltage-Source Inverters

VSIs as shown in Fig. 2.3, e. g. realized as IGBT-based VSI, control three-phase electrical machines by converting a direct current (dc) voltage U_{dc} into corresponding alternating current (ac) voltages that represents the terminal voltages $\vec{u}_{\mathrm{s}}$ of the electrical machine. This electric drivetrain is employed in a wide range of various applications. They begin at low power levels in microsystem technology, progress through e. g. household appliances, industrial robots, and traction drives in electric vehicles and reach high power categories such as railway systems and energy generation systems as wind turbines or hydroelectric power plants. The diversity of applications results in a broad spectrum of

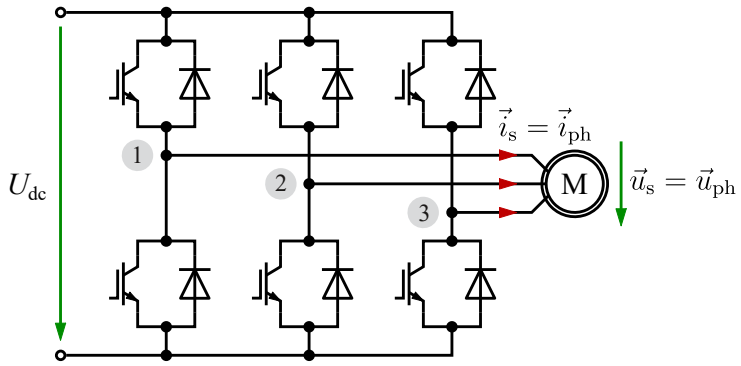


Figure 2.3: Voltage source inverter with three-phase machine

modeling techniques and control strategies. Notwithstanding, as mentioned above, the magnetic flux-linkage is an essential parameter in multiple methodologies in addition to the foundational torque, speed, and position control algorithms. The presence of (instantaneous) flux-linkage could be advantageous for emerging application fields e. g. as an additional quantity in verification of condition monitoring [23]–[25], or artificial intelligence (AI)-assisted or AI-based approaches, for example for temperature estimation [26], [27]. Control strategies like optimized pulse pattern (OPP) approaches, as in model predictive control [28] or flux trajectory control [29], or enhancing noise vibration harshness (NVH) of PMSMs through injection of flux-linkage harmonics [30] could also see improvements.

2.2.1 Phase-Voltage Determination

Conventional drive systems consist of a dc-link that is connected to the VSI. The drive system shown in Fig. 2.4 features a split dc-link on the left side, consisting of two capacitors of the same size connected in series, with a neutral point N located between them. As depicted before, six switching cells with IGBTs and anti-parallel diodes form the VSI. A series connection of stator inductance L_{s}, stator resistance R_{s}, and a voltage source $u_{\mathrm{e}i}$ ($i \in [1,2,3]$) representing electromotive force (EMF) is used to model the three machine phases on the right hand side. Furthermore, the measurable quantities phase current $\vec{i}_{\mathrm{ph}}$, supply voltages $u_{i\mathrm{N}}$ ($i \in [1,2,3]$), zero sequence component $u_{0\mathrm{N}}$, and phase-to-phase voltages u_{12} and u_{32} are declared.

The VSI is usally not able to specify the flux-linkage $\vec{\psi}_{\mathrm{ph}}$, but phase current $\vec{i}_{\mathrm{ph}}$ or phase voltage $\vec{u}_{\mathrm{ph}}$, since in general case the phase current $\vec{i}_{\mathrm{ph}}$ is directly measured and the phase voltage $\vec{u}_{\mathrm{ph}}$ can be determined by the supply voltages $u_{i\mathrm{N}}$ ($i \in [1,2,3]$) and the zero sequence component $u_{0\mathrm{N}}$. The magnetic flux-linkage is either calculated from LUTs or by software integration of the phase voltage. The latter leads to a more extensive discussion of determining the phase voltage.
The phase voltage is either determined through measurement or estimation [31]. Estimat-

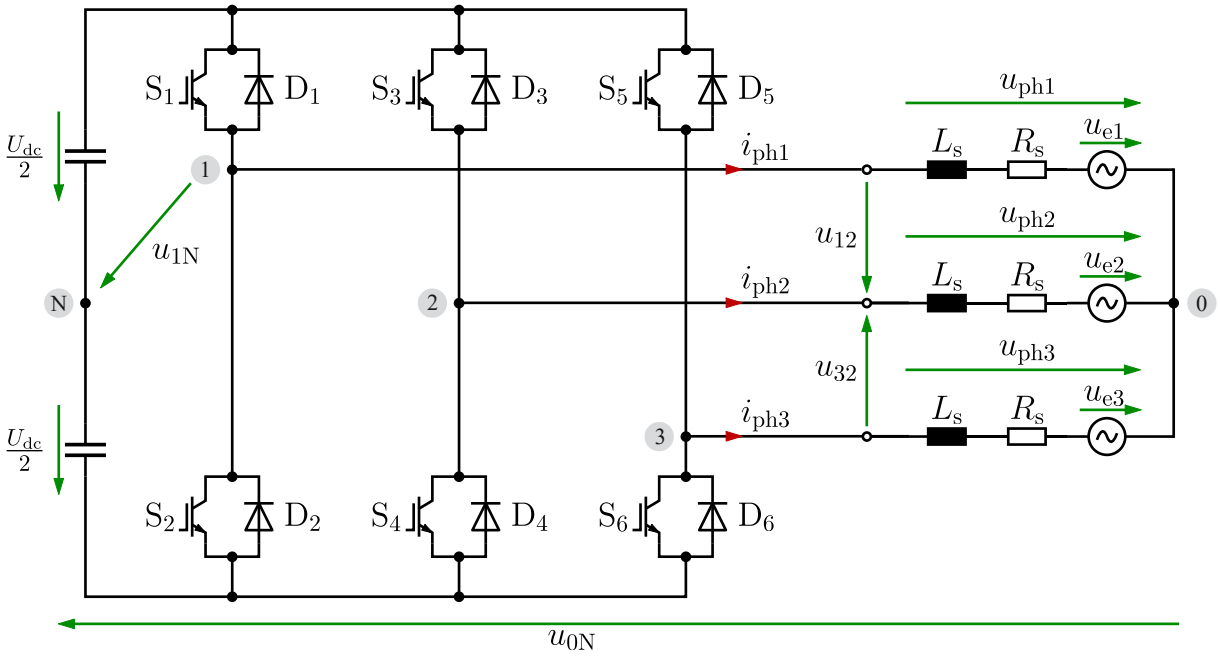


Figure 2.4: Electrical drive system with corresponding voltages

ing the phase voltage involves considering the inverter's switching state and the dc-link voltage [32], or it can be predefined by the reference voltage vector [33], thereby neglecting several effects causing volt-second errors. The dead time of the controller, the on-stage voltage drop of the semiconductor devices, and the nonlinearities of VSIs are all factors that contribute to these effects as outlined in detail later on.

VSIs vary frequency and magnitude of the output voltage by generating high-frequency pulses. There are manifold modulation schemes that are either continuous PWM (CPWM) [34] (e. g. carrier-based sinusoidal PWM (SPWM) [35], space-vector PWM (SVPWM) [36], or third harmonic injection PWM (THIPWM) [37]), or discontinuous PWM (DPWM) [38] as needed with overmodulation methods [39], [40] (like DPWM1, DPWM2, DPWM3). CPWM scheme is generated when the zero sequence component u_{0N} is continuous and, consequently, DPWM scheme is generated when the zero sequence component is discontinuous as there is a possibility for the modulator to have a phase segment that is clamped to either positive or negative dc-rails for a total of 120°, which means that there is no switching action within one phase segment over 120° electrical degrees.
Five specific evaluation criteria are mainly considered when deciding on the modulation scheme to be applied: current waveform quality, swichting losses, voltage linearity, common mode voltage, and overmodulation region performance. These guidelines indicate that CPWM, like SVPWM, is the preferred choice for low modulation ranges, whereas generalized DPWM (GDPWM) is advantageous for high modulation ranges [38].

Independent of the modulation method utilized, the following considerations are universally applicable to all strategies. The main objective is to obtain the terminal flux-linkage $\vec{\psi}_{\mathrm{ph}}$ as process variable for an arbitrary flux-linkage-based control algorithm. This control

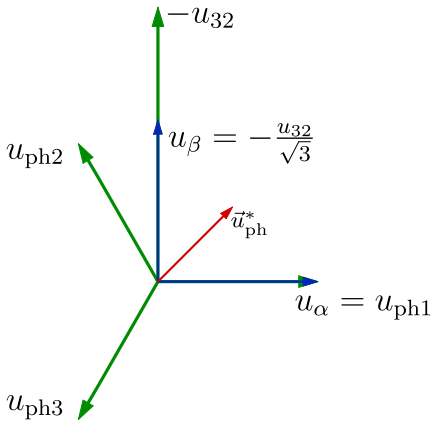


Figure 2.5: Space vector representation of symmetrical three-phase systems in $\alpha\beta$-plane

variable $\vec{\psi}_{\mathrm{ph}}$ is ascertained through the parallel connection to the stator voltage $\vec{u}_{\mathrm{s}}$, i. e. the phase voltage $\vec{u}_{\mathrm{ph}}$ (Fig. 2.2). Nevertheless, star point-connected machines are unable to metrologically achieve the phase voltage $\vec{u}_{\mathrm{ph}}$ due to the unavailability of star point 0. One potential approach is to measure either the three supply voltages $u_{i\mathrm{N}}$ − when assuming a symmetrical load − or two phase-to-phase voltages. Mainly for cost optimization, the decision is to implement two than three flux-linkage sensors. Hence, a deduction for the two phase-to-phase voltage or flux-linkages, respectively, conducts.
It is referred to Fig. 2.4, start by using three mash equations across the inverter and electrical machine, which are added in equation (2.5).

$$\sum_{i=1}^{3} u_{i\mathrm{N}} = \sum_{i=1}^{3} u_{\mathrm{ph}i} + 3 \cdot u_{0\mathrm{N}} \tag{2.5}$$

With the hypothesis of the load being symmetrical, the phase voltages $\vec{u}_{\mathrm{ph}}$ add to zero and the equation system with the switching states for a three-phase drive system in equation (2.6) results.

$$\begin{pmatrix} u_{\mathrm{ph1}} \\ u_{\mathrm{ph2}} \\ u_{\mathrm{ph3}} \end{pmatrix} = \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{pmatrix} \cdot \begin{pmatrix} u_{1\mathrm{N}} \\ u_{2\mathrm{N}} \\ u_{3\mathrm{N}} \end{pmatrix} \tag{2.6}$$

The representation of phase voltage (e. g. $\vec{u}^*_{\mathrm{ph}}$) can be depicted as a space vector in the $\alpha\beta$-plane shown in Fig. 2.5 as a combination of real part u_α and imaginary part u_β. The Clarke transformation in equation (2.7) now converts the amplitude invariant three-phase to two-phase system.

$$\begin{pmatrix} u_\alpha \\ u_\beta \end{pmatrix} = \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{pmatrix} \cdot \begin{pmatrix} u_{\mathrm{ph1}} \\ u_{\mathrm{ph2}} \\ u_{\mathrm{ph3}} \end{pmatrix} \tag{2.7}$$

Hereafter, the phase voltages $u_{\mathrm{ph}i}$ are substituted by two phase-to-phase voltages. Selecting phase 2 as reference voltage for both sensors is crucial to guarantee the functionality of two single-ended measuring volt-second sensors. This particular circuitry generates the necessary measurements of u_{12} and u_{32} and, thus, ψ_{12} and ψ_{32}, while eliminating the need for differential probes as demonstrated in a previous study [41]. While u_{ph1} is equal to u_α, the phase relationship of 120° between the phase voltages $u_{\mathrm{ph}i}$ causes the phase-to-phase voltage u_{32} to be perpendicular to u_{ph1} and differ in magnitude by a constant factor of $\sqrt{3}$ (equation (2.8)).

$$u_\alpha = u_{\mathrm{ph1}} \tag{2.8a}$$

$$u_\beta = -\frac{1}{\sqrt{3}} \cdot u_{32} \tag{2.8b}$$

The phase-to-phase voltage u_{12} is the focus for measurement, replacing the phase voltage u_{ph1}. In order to accomplish this objective, a system of equations (equation (2.9)) is formulated using three independent equations derived from the electric drive train mesh analysis, and subsequently solved to ascertain the phase voltage u_{ph1}.

$$u_{12} = u_{\mathrm{ph1}} - u_{\mathrm{ph2}} \tag{2.9a}$$

$$u_{32} = -u_{\mathrm{ph2}} + u_{\mathrm{ph3}} \tag{2.9b}$$

$$u_{\mathrm{ph3}} = -u_{\mathrm{ph1}} - u_{\mathrm{ph2}} \tag{2.9c}$$

When equation (2.9c) is inserted into equation (2.9b) and the phase voltage u_{ph2} is replaced with equation (2.9a), the space vectors u_α and u_β depending on the phase-to-phase voltages u_{12} and u_{32} in equation (2.10) remain.

$$\begin{pmatrix} u_\alpha \\ u_\beta \end{pmatrix} = \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} \\ 0 & -\frac{1}{\sqrt{3}} \end{pmatrix} \cdot \begin{pmatrix} u_{12} \\ u_{32} \end{pmatrix} \tag{2.10}$$

The space vectors can be calculated accordingly by measuring two phase-to-phase voltages, so it is unnecessary to use three sensors. Conclusions about the flux-linkage variables

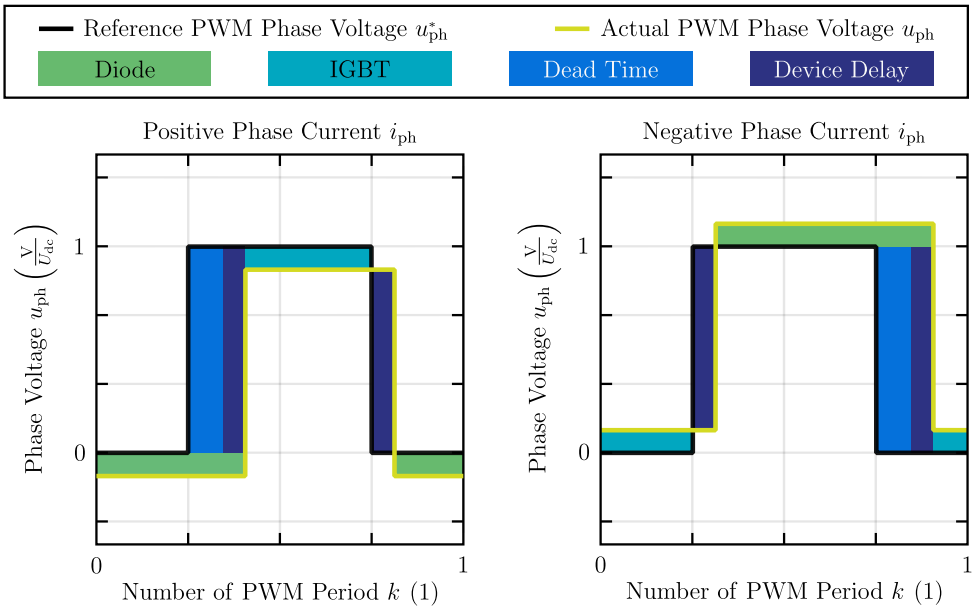


Figure 2.6: Volt-second error during one center aligned PWM period with $d = 0.5$

in the $\alpha\beta$-system and, consequently, the stator flux-linkage $\vec{\psi}_s$ can be inferred by analyzing the phase-to-phase flux-linkage measured.

2.2.2 Voltage Distortion of Voltage-Source Inverters

A related subject regarding VSIs pertains to devising a model for determining the resulting phase voltage u_{ph} in situations where obtaining the measured value is not feasible. The VSI applies the reference phase voltage u^*_{ph} to the electrical machine, yet the resulting phase voltage u_{ph} will deviate from a perfect rectangular shape due to nonidealities producing volt-second errors over a PWM-period. Nevertheless, IGBT-diode combinations as a switching cell of a inverter are often modeled as ideal switches although ideal switches neglect volt-second errors caused by the dead time T_{dt} of the controller, turn-on delay T_{on} and turn-off delay T_{off} of the devices, power devices on-stage voltage drops of the IGBTs U_{IGBT} and the diodes U_{diode}, as well as the limitied voltage gradient during commutation time as shown in Fig. 2.6. As a note, it should be stated here that the limited voltage slope is neglected in for the actual phase voltage u_{ph} since it depends on the phase current i_{ph} and therefore is discussed more in-depth in Section 3.1. Particularly at lower speeds, the volt-second error becomes significant, especially the dead time becomes relatively large in comparison to the on-time of a PWM-period [35]. Thus, either a precise model or volt-second compensation should be taken into account.

Literature explores diverse methods when aiming for a more accurate inverter model, including the enumerated deviations, than that provided by ideal switches. In 1988, the initial IGBT modeling method is introduced in the publication by A. R. Hefner and is

commonly referred to as the Hefner model [42]. His analytical model is the first to provide a consistent depiction of the IGBT's steady-state behavior and switching transients under loading conditions. He validated the accuracy of his model through practical experiments using devices with diverse parameter settings. Nonetheless, while his model is exact, it consumes a considerable amount of time. In [43] and [44], a model that is more practical but less precise than the Hefner model is presented over a decade later. The authors recommend retrieving information from datasheets and experimental configurations to establish the parameters of the analytical model. [45] suggests enhancing this model by optimizing the IGBT parameters using an algorithm to accelerate simulation in SPICE-based environments. The modeling method proposed by [46] accurately represents voltage distortion in IGBT and diode converters for advanced motor drives, which has been adopted in other studies like [47]–[51]. This methodology is also implemented in the investigation and interpretation outlined in Section 3.1. Novel techniques, such as self-identification through current injections [52] or online current- and voltage-sensor offset adation schemes [53], provide an accurate portrayal of the nonlinear characteristics of voltage distortion.
Furthermore, this author developed a modeling approach with regard to implementation in PLECS [54]. The software tool enables rapid simulation of power electronics at a system level and allows for seamless integration of these models into MATLAB/Simulink for designing control algorithms [55]. The accuracy of this model is verified by employing a test bench that is developed specifically for this task within this study and already introduced in [56].

Along with precise models for VSIs, there are the aforementioned multiple approaches to volt-second compensation aimed to counteract deviations. They start with (online) dead-time compensation [57]–[59], going to self-tuning dead-time compensation [60], feed-forward (offline) compensation of nonlinearities of IGBT inverters [61], [62], or direct dead-time effect compensation scheme [63]. With the intention of obtaining an accurate measurement of volt-seconds, these methods will not be pursued beyond this point.

2.3 Instantaneous Measuring Techniques

The terminology of *instantaneousness* is established, before discussing various measurement techniques. The measurement strategies outlined in the latter part of this section address direct or indirect voltage or flux-linkage measurements for power electronic circuits, whereby *instantaneous* signifies the sensing of averaged VSI output quantity (voltage $\bar{u}_{\mathrm{pwm}}$ or flux-linkage $\bar{\psi}_{\mathrm{pwm}}$) to precisely detect it for each (half) PWM period. This section supposes the sensing of phase voltage u_{ph} equal to u_{pwm} without loss of generality. Flux-linkage or volt-seconds, respectively, are a suitable description for PWM voltages because of its rectangular shape. As previously stated, having precise knowledge of the present volt-seconds is critical for controlling electrical machines effectively. A deviation by incorrect estimation or inaccurate measurement can affect the stability of the control

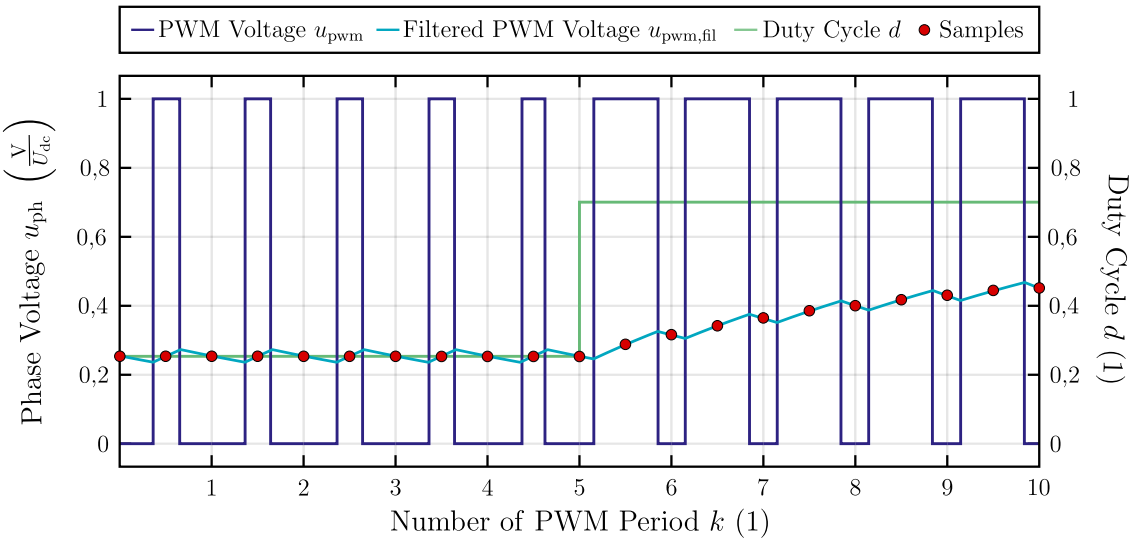


Figure 2.7: Filtered and sampled PWM voltage

[64]. Nevertheless, the challenging aspect lies in the measurement of the steep voltage slopes of a PWM signal [65].

The upcoming paragraph is an explanation of the conventional measurement methods for PWM trajectories in a general scope. Three main divisions exist for direct measurement techniques of PWM voltages: Filtering of the signal, analog integration, and digital integration of a PWM voltages.
One of the initial measurement methods involves the application of a low-pass filter to smooth the PWM voltage u_{pwm} and filtering out the high-switching components to extract the fundamental component. An almost ripple free voltage $u_{pwm,fil}$ output is achieved by employing a sufficiently high smoothing capacity. Subsequently, this voltage is sampled and digitally examined (Fig. 2.7). However, this technique results in an undesired and significant phase shift between the actual and the measured voltage [8]. Moreover, the filter can compromise the stability of the control system as voltage value changes are not instantaneously reflected in the sampled phase voltage for each switching period anymore. Therefore, the efficiency of this measurement method is diminished, and it is not regarded as instantaneous.
Various techniques apart from the filtering and sampling method involve analog or digital integration (Fig. 2.8, left, and Fig. 2.8, right) for establishing the average value of the PWM signal to counteract the drawback of low-pass filtered circuits. The analog integration technique requires a reset of the integrator operational amplifier circuit at the end of each PWM interval, causing a temporary loss of volt-seconds due to the interruption in input voltage detection. As will be introduced in Section 2.3.1, the literature presents a range of strategies for resolving this particular problem. To achieve digital integration, an ADC must sample the PWM voltage frequently, along with a computational logic that implements numerical integration methods like backward-euler, forward-euler, or the trapezoidal rule. The rate at which ADCs converts signals is of greater significance than

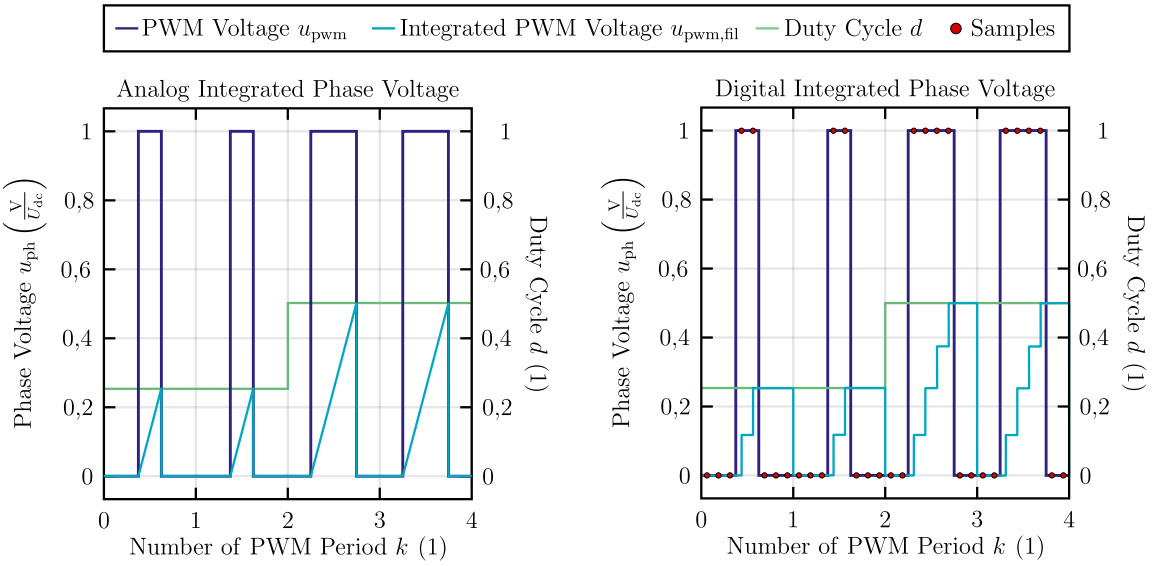


Figure 2.8: Analog and digital integration of PWM voltage

its accuracy, with research indicating that resolutions as low as 8 bits can be effective [66]. The preference for digital integration over analog integration is due to its ease of use, simplicity, high level of accuracy, and straightforward approach to signal processing.

In recent years, various techniques have emerged for precisely measuring PWM phase or line-to-line voltages in electrical machines. Instantaneous voltage and volt-second measurement techniques are explored in literature through analog and digital methods. The progress of the diverse measurement circuits is explained in the upcoming sections, along with a demonstration of the enhanced volt-second sensing developed in this thesis.

2.3.1 Instantaneous Voltage Measurement

A publication of 1997 marks the introduction of a technique for measuring instantaneous voltage accurately without employing a low-pass filter but an analog integrating circuit [65]. Two operational amplifiers measure the phase voltage in an alternating procedure using an integrator while evaluating and resetting the integrator capacitor of the other amplifier to overcome the loss of volt-seconds [67]. Nonetheless, this initial design demands a significant number of components due to the necessity of three operational amplifiers and eight switches for voltage measurement.
[68] utilizes the same measurement method in a modified arrangement requring only one analog integrator but complement a differential amplifier to reject the common-mode voltage of the PWM input. Thus, the output voltage of the inverter remains constant at low speeds, ensuring stable operation. An issue with this method is that the parallel switch resets the capacitor, resulting in a decrease in the average volt-seconds.

Another analog integration approach is presented in [64], in which the differential amplifier is substituted by an *RC*-circuit employing only one operational amplifier. In addition, it authorizes calculations on half of a symmetrical PWM-period starting at the midpoint to improve speed in applications. The main issue with this method is the lack of consideration for asymmetries induced by dead-time effects in system operation.
The specialized PWM voltage measurement apparatus in a US Patent [69] is designed for a three-phase electrical machine to measure and filter all phase voltages using a low-pass filter with a cutoff frequency below the output frequency. Voltage followers decouple the potentials, then an analog subtractor with an offset for bipolar supplies creates two line-to-line voltages, which are combined by an analog integrator. Through the implementation of analog buffering, a range of buffered voltage signals can be produced, allowing for reduced ADC sampling rates, albeit with the need for extensive analog circuit design.
A precise phase-voltage measurement technique using digital integration is introduced in [70]. This FPGA-based digital integrator is combined with high-speed high-cost ADCs for oversampling of the PWM-signal. An analog single-ended operational amplifier, similar to [69], determines the difference in incoming phase voltages to create two line-to-line voltages for a differential ADC driver.
A combination of filtering and oversampling of PWM phase voltage for instantaneous sensing is introduced in [71]. Utilizing the time-lag behavior of low-pass filtering intentionally reduces the slope of the PWM-signal, resulting in oversampling of the filtered voltage slope. As the volt-second area under a PWM-period remains unaffected by the filter, it can be used to shape the steep voltage gradient into exponential curves, which are subsequently sampled with an ADC.
A microcontroller-based voltage measuring method by obtaining the actual phase voltage based on the digital integration of PWM-voltage using the capture modulator in existing drive microcontrollers (MCUs) is presented in 2020 [72]. This method eliminates the need for separate ADC and communication hardware, despite the complexity of the signal processing software that follows.
The authors in [73] and [74] shift the utilization of commercial ICs for PWM-voltage detection. The second-order delta-sigma modulator (DSM) ADS1201 [75] and an asynchronous voltage-to-frequency converter (AVFC) VFC110 [76] are investigated for their effectiveness in voltage and current measurement in medium- and high-voltage inverters given their high signal-to-noise ratio (SNR). These ICs convert a range of voltages into a corresponding range of frequencies that increase in direct proportion to their input voltage. The output signal from both ICs consists of a digital pulse train that can be transmitted with minimal interference utilizing an optic fiber link. Additionally, the combined feature of both ICs prevents the loss of volt-seconds.
Owing to these advantages of converting a continuous PWM-voltage signal into a discrete digital pulse train by an AVFC, [56] also applies this IC as a key component of a measurement circuit. Moreover, VFCs in general address the integrator reset challenge by performing charge-balancing on the integrator capacitor rather than fully resetting it (see a more detailed explanation in the following Section 2.4). Although this measurement method is already more advantageous than the previously presented measurement circuits, the disadvantage is that a residual voltage remains on the capacitor at the end of each PWM period, which can be interpreted as quantization error. The authors sug-

gest sampling the residual voltage of the integration capacitor with a 12-bit successive-approximation-register (SAR) ADC to gain maximum accuracy. In Section 3.2, a more elaborate description of this measuring circuit is provided. In spite of this, the costly AVFC component acts as a barrier to the extensive adoption of this instantaneous measurement system, limiting its practical use to almost only laboratory applications.

In conclusion, the approaches of analog and digital integration still have two significant disadvantages when compared to the class of VFCs that are the preferred analog sensing technique in this work. Firstly, the limitation of linearity in these circuits stems from the fact that their transfer functions are influenced by varying capacitance values dependent on voltage, frequency, and temperature. Secondly, the analog integrated voltage requires conversion by an ADC for processing, whereas VFCs produce pulses that can be read as a 1-bit signal by a digital input. A more detailed explanation is outlined in Section 2.4.

2.3.2 Instantaneous Volt-Second Measurement

The advantage of this direct volt-second measurement method has been acknowledged by the authors of [77] as well. This time, instead of using a DSM or AVFC like described in the section before, another associate of the VFC-group − a synchronous voltage-to-frequency converter (SVFC) − is applied to extend the low speed range on the one hand and to improve disturbance rejection of back-EMF-based self sensing on the other hand [13], [78]. Their study indicates that their measurement strategy effectively deals with the problem of diverse back-EMF estimation methods, like integrating the terminal voltage [79]. Additionally, the researchers delve deeper into enhancing algorithms by illustrating techniques to increase the accuracy of torque [8], [80].

This innovative method avoids volt-second inaccuracies arising from various origins, such as inverter nonlinearity including dead time, voltage drops, dc-link voltage fluctuation and static error, ripple content, and poor SNR for controller bandwidth, while enabling negligent phase delay over each PWM period. These advantages are also approved for other machine types as the SRM in [81]. However, this measuring technique comes with the same significant drawback as the approach of sensing with an AVFC in [56]: Implementation of the high-expensive SVFC is limited to laboratory settings, as it is not feasible for utilization in industries like automotive. Although, the accuracy of measuring the $\pm 1.2\,\mathrm{kV}$ input voltage range (phase-to-phase voltage) with a resolution of $0.5\,\mathrm{V}$, which is equal to $0.02\,\%$, demonstrates remarkable precision. The resolution of volt-seconds requires accounting for either the PWM period T_{pwm} or the switching frequency f_{sw}, respectively. A volt-second quantum ψ_{ε} of $0.33 \cdot 10^{-3}\,\mathrm{Vs}$ at a quite low switching frequency f_{sw} of $1.5\,\mathrm{kHz}$ is stated within the study. These quantities will be evaluated in the subsequent Chapter 4.

The opportunities for improving a variety of algorithms is the motivation for this present study. It can be argued that this investigation has been greatly inspired by the innovative

work of those researchers from Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC), the technology center at the University of Wisconsin-Madison. The author's intention of this work is to revise the drawbacks employing a cost-intensive and fixed commercial SVFC by combining the advantages of analog integration, scalable and low-cost design, digital transmission, and adjustable evaluation by using already existing hardware. Therefore, a novel precision volt-second sensor for PWM VSIs is developed within this research, along with the previously measurement methods presented in [56]. The first prototype of this newly developed volt-second measurement instrument is already introduced in [82], [83] and, furthermore, stated as a WIPO Patent Cooperation Treaty [84].
In essence, the discrete synchronous voltage-to-frequency converter (dSVFC) is also founded on the charge-balancing process of VFCs, which is extensively discussed in theory, simulation, and measurement results in [83]. By implementing this procedure, an arbitrary input voltage range is converted into a digital pulse train with a certain propotional output frequency f_{pt}. It is explained how to dimension the transfer function of the dSVFC through this correlation and how to determine the instantaneuous volt-second value $\bar{\psi}_{\mathrm{pwm}}$ (also defined in this context as the average value over a PWM period). The further developement of the dSVFC with its analysis and evaluation is outlined in Section 3.3. Section 4.3 explores the performance of this method when contrasted with other measurement methodologies to provide a categorization of the sensor. Finally, two dSVFCs are installed on a traction drive application on a test bench to validate the measurement instrument by sensing phase-to-phase voltage in a range of $\pm 400\,\mathrm{V}$ in Chapter 4.4. Additionally, the author suggests how to adapt the evaluation algorithm to receive instantaneously a positive or negative volt-second quantum ψ_{ε} (instead of the average value $\bar{\psi}_{\mathrm{pwm}}$ of one PWM period), thus enabling the applicability for control algorithms like OPP.

2.4 Voltage-to-Frequency Converters

Delving further into the topic, this section focuses on VFCs that were previously introduced. Basically, a VFC converts an input voltage u_{in} into an output frequency f_{pt}. The output frequency f_{pt} is direct proportional to the input voltage u_{in} (Fig. 2.9). A VFC IC is consistent and has the capacity to operate with very low power consumption [85]. It has been noted that VFCs offer the advantages of a high linearity range in addition to a long transmission path without interference. Furthermore, they solve the integrator reset challenge, which was presented in the literature of instantaneous phase voltage measuring, by carrying out charge balancing on the integrator capacitor instead of discharging it entirely [86].
However, when it comes to VFCs, there are still inaccuracies like offset error, gain error, and (low) linearity error that must be considered. The dSVFC development in Section 3.3 will focus on addressing these three errors and demonstrating methods to minimize these three errors.

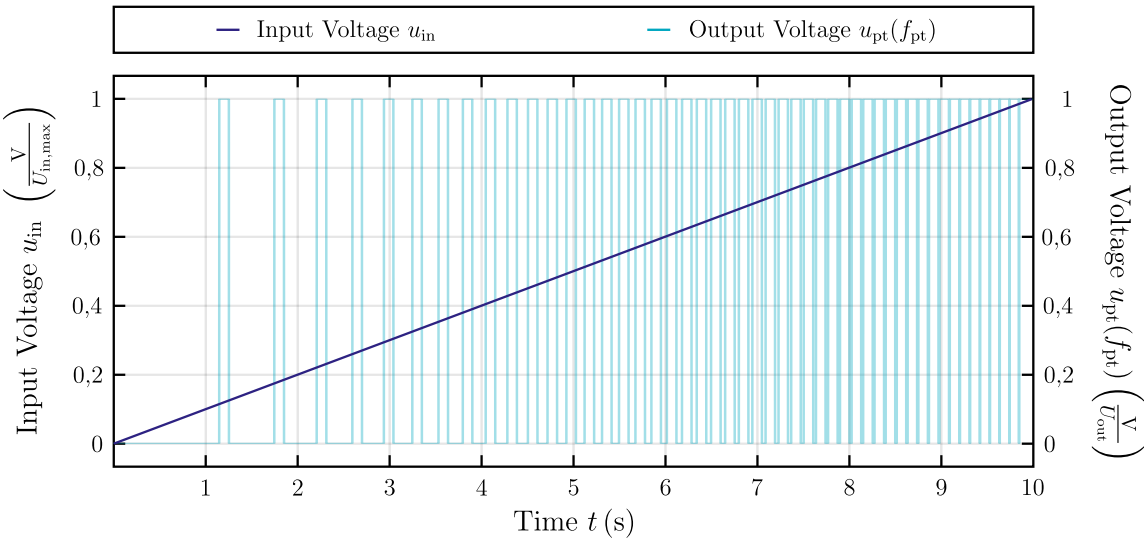


Figure 2.9: Correlation between input voltage u_{in} and output frequency f_{pt} of a VFC

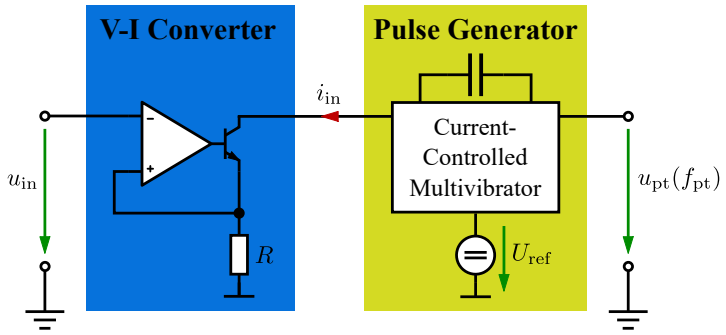


Figure 2.10: Current-steering voltage-to-frequency converter

Overall, VFCs can be classified into two primary groups: VFCs that use (current-steering) multivibrators and those that implement charge-balance strategies. A current-to-frequency converter, like the AD537 [87], changes the input voltage u_{in} into a current i_{in} that is responsible for charging and discharging a capacitor C, subsequently triggering a threshold (Fig. 2.10). The resulting voltage transient across the capacitor is a linear triangular shape. By using a stable reference voltage U_{ref}, the switching thresholds are established, leading to an output frequncy f_{pt} that correlates with the input voltage. Achieving linearities of around 14 bits is feasible using this approach. Comparator threshold noise, threshold temperature coefficient, and the stability and dielectric absorption of the capacitor (being generally a discrete component) are the factors that typically set the performance limits.
This type of VFCs is inexpensive even so less precise than the charge-balance type. In addition, multivibrators lack the capability to integrate negative input voltage, resulting in an inadequate volt-second measurement approach for this research, as the detection of phase-to-phase flux-linkage demands the ability to process negative input transients.

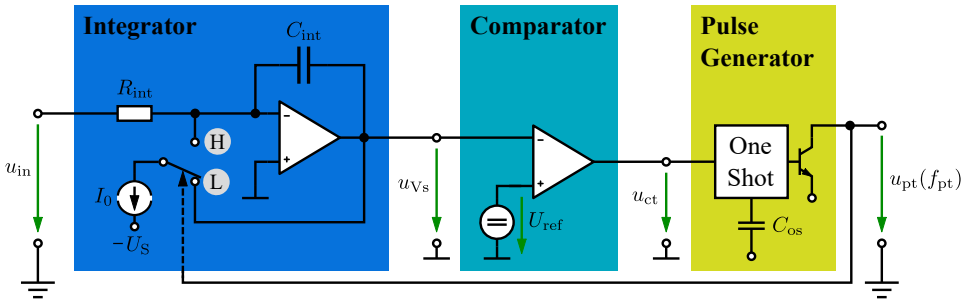


Figure 2.11: Asynchronous voltage-to-frequency converter

In 1988, [88] introduced the principle of charging-balancing through a switched capacitor realized as an IC. Concerning the charge-balance VFCs, such as the AD650 [89], these units are structured with three key elements: An integrator, a comparator, and a precision charge source. Consequently, this category of VFC presents increased complexity, higher requirements for supply voltage and current, but also superior precision with a linearity range between 16 to 18 bits. Two primary categories of charge-balancing VFCs exist: asynchronous VFCs and synchronous VFCs.

2.4.1 Asynchronous Voltage-to-Frequency Converters

The essential functionality is comparable to that of the multivibrator and illustrated in Fig. 2.11. The input voltage u_{in} is applied to an integrator whose capacitor C_{int} is charged. Reaching the threshold of the comparator, the precision charge source I_0 is triggered, and as a consequence, it removes a fixed and defined amount of charge. The key point lies on the uninterrupted flow of the input current i_{in} to ensure no input charge dissipates. The frequency at which the charge source is activated is dependent on the input to the integrator, ensuring that the removal rate of charge matches the supply rate and, consequently, the output frequency f_{pt} is proportional to the input voltage u_{in}. The operational concept of an AVFC and a SVFC remains consistent.
Considering an AVFC now (Fig. 2.11), similar to the VFC110 [76], the removed fixed charge is set by the precision current source I_0 and the pulse width of a precision monostable. The transient problem of the integrator is addressed by an single pole, double throw (SPDT) switch since on- and off-transients are eliminated and the output stage of the integrator perceives a constant load. AVFCs excel in promptly generating pulses, contrasting with SVFCs that exhibit minimal jitter through their bistable multivibrator. This benefit is utilized in innovative measurement techniques introduced in this study in Section 3.2 and also introduced in [56]. Nevertheless, dealing with the stability and transient response of the precision monostable proves problematic, but this issue can be solved by substituting the monostable with a clocked bistable multivibrator.

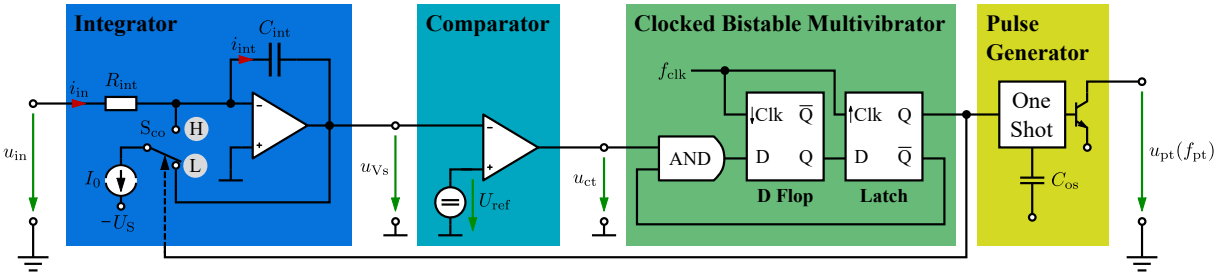


Figure 2.12: Synchronous voltage-to-frequency converter

2.4.2 Synchronous Voltage-to-Frequency Converters

Replacing the monostable with a bistable multivibrator, which is driven by an external clock, enhances both stability and linearity up to 18 bit with a steadiness in temperature stability (cf. equation (2.11)). The discharge event is now synchronized with this external clock to a defined pulse length, eliminating the instantaneous − also meaning arbitrary − discharging process. Connecting an SVFC, like the AD652 [90], to external control hardware benefits from the ease of handling synchronous data transfer in comparison to asynchronous transfer. The main benefit of synchronized output pulses is simultaneously unfavorable since significant jitter is mapped to the discharging pulses resulting in non-equidistant pulses. Moreover, nonlinearities in output frequency close to certain subharmonics of the clock frequency can be observed due to the coupling of the clock signal into the comparator as it causes the SVFC to behave as an injection-locked phase-locked loop (PLL). Nevertheless, there are design guidelines for the printed circuit board (PCB)-layout that can minimize these nonlinearities, which will be taken into consideration during the incorporation of sensors utilizing bistable multivibrators.

The subsequent discussion will provide a brief, yet detailed overview of how an SVFC operates, as the measurement methods devised in this study are rooted in this approach. (Fig. 2.12) depicts the basic circuitry of an SVFC (according to the topology of the AD652). The input voltage u_{in} is converted through the resistor R_{int} into the input current i_{in} that charges the integrator capacitor C_{int} and, thus, the integrator output voltage u_{Vs} increases (equation (2.11)) until it exceeds the reference voltage U_{ref}.

$$u_{Vs} = -\frac{1}{C_{int}} \cdot \int_{\tilde{t}=t_0}^{t} i_{int}\left(\tilde{t}\right)\, \mathrm{d}\tilde{t} + U_0\left(\tilde{t} = t_0\right) \tag{2.11}$$

If the input voltage u_{in} is larger than the reference voltage U_{ref}, the output voltage u_{ct} of the comparator is rising to its positive supply voltage and subsequently triggers the clocked bistable multivibrator. At this point, the synchronized output pulses f_{pt} are in operation since the bistable multivibrator is controlled by the external clock frequency f_{clk}. The clock-synchronized output pulses consistently have a duration equivalent to one clock period T_{clk}. The length of one pulse matches the clock period T_{clk} as the inverted output

of the latch is looped back to the D flop. The input signal D of the D flop switches to output Q on the falling slope of the clock signal f_{clk}. With the subsequent rising edge of the clock signal, the output signal Q of the D flop is switched to the output of the latch $\bar{\mathrm{Q}}$ and thereby setting the frequency of the output signal $u_{\mathrm{pt}}(f_{\mathrm{pt}})$. The maximum reachable output frequency f_{pt} of the pulse train lies at half of the clock frequency $f_{\mathrm{clk}}/2$.

Simultaneously, the output of the latch Q controls the position of the SPDT switch $\mathrm{S_{co}}$ with its default position L charging the capacitor C_{int}. Once the reference voltage U_{ref} is exceeded, a pulse is created at the multivibrator output causing the switch $\mathrm{S_{co}}$ to position L. Accordingly, the input current i_{in} is superposted with the current I_0 of the constant current source (equation (2.12)), discharging the capacitor C_{int} for the duration of the clock period T_{clk}.

$$i_{\mathrm{int}} = \begin{cases} i_{\mathrm{in}} = \frac{u_{\mathrm{in}}}{R_{\mathrm{int}}}, & \text{if } \mathrm{S_{co}} \text{ on L} \\ i_{\mathrm{in}} - I_0 = \frac{u_{\mathrm{in}}}{R_{\mathrm{int}}} - I_0, & \text{if } \mathrm{S_{co}} \text{ on H} \end{cases} \tag{2.12}$$

As the input voltage u_{in} increases, the charging current i_{int} also increases, leading to a direct correlation between the input voltage u_{in} and the output voltage u_{Vs} of the integrator circuit. As a result, the comparator's threshold voltage U_{ref} is exceeded at a faster rate, causing a rise in the pulse generation frequency f_{pt}. In summary, the input voltage u_{in} correlates directly with both the output frequency f_{pt} and the number of pulses in each PWM period. It is now apparent that there are limitations to how large the input current i_{in} and the constant current I_0 can be chosen. Section 3.3.1 will provide a thorough discussion of this topic when designing and dimensioning the dSVFC.

Different techniques are also employed in literature for the discrete or integrated application of SVFCs. Several publications have introduced this method at the complementary metal-oxide-semiconductor (CMOS) level [91]–[94]. Differential voltage measurements like in this study are carried out by a particular CMOS-based IC, which is configured with a preceding fully differential difference amplifier [95]. Two second-generation current conveyors are chosen over a differential difference amplifier in [96] for the realization of a differential VFC. Both techniques convert the differential input voltage into a current, which is utilized to control a subsequent logic circuit responsible for generating the pulse train. The main divergence in this work occurs in the realization at CMOS-level as the suggested measuring instrument is based on discrete components. In addition, the newly developed dSVFC is able to sense both positive and negative input voltages by adjusting its characteristic curve as will be presented in Section 3.3.2.

3 Voltage-Integration Measuring Techniques

This chapter introduces three new measuring techniques for instantaneous volt-second measurement according to which the chapter is also divided. The first approach presented involves precise model development of an VSI within PLECS and the calculation of voltage disturbance combined with a standard sample-and-hold (S&H) ADC installed on the test bench. The second and third methods are hardware-based volt-second measurement instruments. One category of measurement methods is based on a commercial AVFC. Multiple evaluation methodologies are established to determine voltage or volt-seconds, employing the identical sensor in place. The third approach is the elaboration of a novel volt-second sensor based on the working principle of an SVFC. The presentation includes an in-depth examination of the design process, and the subsequent hardware and software implementation is demonstrated. A comparison is conducted in Chapter 4 between these three approaches and common measurement techniques.

3.1 Accurate Voltage-Distortion Model of Voltage-Source Inverters

A detailed representation of the VSI is beneficial for both initial simulation studies and integration into a control algorithm for an electric traction drive. Precise representation of volt-second errors $\bar{\psi}_{\mathrm{pwm,err}}$ from nonidealities is crucial. Within this work, frist, an IGBT-based VSI voltage distortion model is implemented in PLECS and its typical characteristics are validated on a test bench. Second, an additional mathematical characterization for this model is added to represent influences of the phase current i_{ph} and the dc-link voltage U_{dc}. The objective of this precise modeling is to incorporate the mathematical results into a model-based feed-forward (MBFF) measurement approach, integrating them into the comparative investigation.

3.1.1 Voltage-Distortion Simulation Model

The PWM-period average $\bar{u}_{\mathrm{ph}}$ is the key quantity for most common control algorithms (see also the defintion of *instantaneousness* in Section 2.3). Once again, the focus is on a PWM-shaped phase voltage u_{ph} without loss of generality. The determination of the occurring

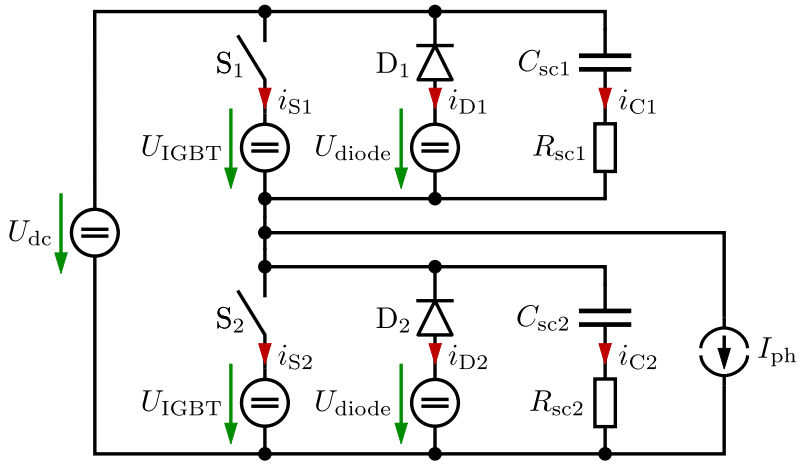


Figure 3.1: Model approaches of half-bridge with nonideal commutation cell in PLECS

voltage deviation during a PWM-period is based on a IGBT half-bridge model that will later be multiplied to a three-phase VSI. Basically, voltage drops across a conducting IGBT U_{IGBT} or diode U_{diode} cause a distortion in the amplitude of the actual phase voltage u_{ph}. Simultaneously, a time distortion through the dead time T_{dt} of the controller, which provides protection against half-bridge shoot-through, and delays in switch turn-on T_{on} and turn-off T_{off} occur. Additionally, due to the charging and discharging event of the IGBT's Miller-capacitance, the voltage gradient during commutation time is limited, which is investigated more extensively within this section.

The established method of using a parallel snubber capacitor C_{sc} with the switching cell is applied to limit the voltage slope during commutation and, thus, replicate an precise voltage distortion model of a half-bridge converter. A further equivalent series resistance (ESR) R_{sc} (of which its value is based on empirical factors) is connected to more accurately represent the current first order time lag behavior within the switching cell and prevent simulation errors. The voltage drops of the the semiconductors are simulated through respective voltage sources U_{IGBT} and U_{diode}, while time deviations are modeled through corresponding delays. Figure 3.1 illustrates the resulting voltage-distortion model for one inverter leg that is ready for immediate implementation transforming to a three-phase IGBT-based VSI in PLECS (Fig. A.1) as this author presents in detail in [54]. The carried-based SPWM utilized in this scenario is arbitrarily applied without any further consequences on the volt-second errors that are to be evaluated (Fig. A.2).

The required simulation parameters in Table 3.1 are on the one hand taken from the datasheet of the SEMIKRON trench IGBT module SKM 600GB066D [97] and on the other hand from the PWM-framework that is employed at a later stage during validation on the test bench (Section 3.1.3). The inductive load L_{s} is assumed to be infinite resulting in a approximated constant phase current I_{ph}. This strategy removes dependencies on the load and allows for the consideration of the phase current's influence.

A qualitative evaluation of the relevant simulated electrical quantities can be seen in

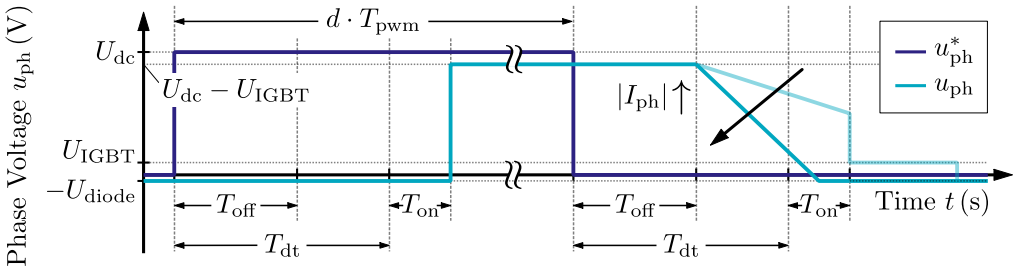
Table 3.1: Model parameters of VSI simulation in PLECS

IGBT Module				**PWM Parameters**				**Additional Capacitance**	
U_{IGBT}	U_{diode}	T_{on}	T_{off}	U_{dc}	f_{sw}	d	T_{dt}	C_{sc}	R_{sc}
1.45 V	1.4 V	270 ns	670 ns	60 V	5 kHz	0.5	3 µs	2.3 nF	10 Ω

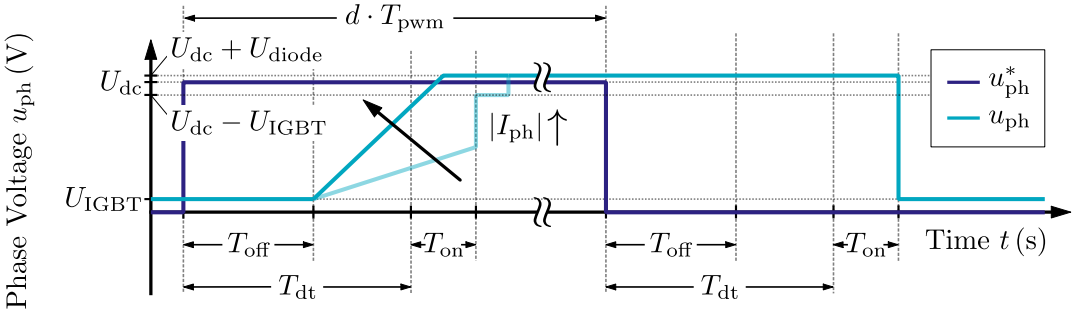
Fig. A.3 and Fig. A.4 in Section A.1. The first graph shows the reference gate signals for the upper and lower IGBT, the second graph indicates the dead time T_{dt} of the controller, while the third presents the actual gate signals including turn-on and turn-off delays. The resulting actual phase voltage u_{ph} with its deviation is then shown in Fig. 3.2a and Fig. 3.2b, respectively. It is necessary to establish a differentiation at this point since the phase voltage u_{ph} depends on the polarity and magnitude of phase current I_{ph}. Four distinct scenarios are noticeable. Two scenarios are observable in the voltage gradient for each polarity of the phase current I_{ph} Fig. 3.2: a pure linear response (dark blueish-colored trajectory) or a noticeable step within the phase voltage signal (bright blueish-colored trajectory) followed by a voltage drop U_{IGBT} across the IGBT. Whether the linear or nonlinear case occurs depends on the amplitude of the phase current I_{ph}. The voltage drop U_{IGBT} across the IGBT is also reflected in a current flow through each corresponding conductive IGBT (Fig. A.3 and Fig. A.4). Which semiconductor devices are utilized for current conduction is determined by the polarity of the phase current I_{ph}. The upper IGBT S_1 and the lower diode D_2 function as the conducting devices when the current I_{ph} is positive, while the upper diode D_1 and the lower IGBT S_2 take on this role in the case of a negative current I_{ph}.

Further, time distortions occurring at the rising slope at the beginning of the voltage pulse lead to a subtraction from the reference phase voltage u^*_{ph}, whereas at the falling slope at the end of the voltage pulse, time distortions result in an addition. The focus now shifts to examining the commutation periods more closely. Due to the ability of an IGBT to switch on and off independently of its current, commutation from a diode to an IGBT leads to an infinite voltage slope, while commutation from an IGBT to a diode results in a limited voltage gradient. The diode's takeover of current is associated with the additional parallel capacitance C_{sc} that needs to be charged and discharged adequately. If the magnitude of the phase current I_{ph} surpasses a predefined threshold $I_{\mathrm{ph,lim}}$, the phase voltage u_{ph} in this linear scenario decreases entirely before activating the second IGBT resulting in a commutation process for classical zero-voltage switching (ZVS).

If the magnitude of the phase current I_{ph} does not surpass the threshold current $I_{\mathrm{ph,lim}}$, the nonlinear case described earlier can be identified. The detailed explanation is provided including four sections utilizing a positive phase current that comes under the limit $I_{\mathrm{ph}} < I_{\mathrm{ph,lim}}$ (Fig. 3.3). In section (1), the upper IGBT is still conducting during turn-off delay time T_{off} and, consequently, the capacitance C_{sc1} is completely discharged, while capacitance C_{sc2} is fully charged with a voltage drop of U_{dc}. After the delay T_{off} has passed, both IGBTs are turned off in section (2), and a charge reversal of the additional capacitors C_{sc1} and C_{sc2} begins. Due to the identical impedance in both RC series cir-



(a) Volt-second error for positive current I_{ph}



(b) Volt-second error for negative current I_{ph}

Figure 3.2: Trajectories of disturbed phase voltage u_{ph} with additional capacitance (cf. [54])

cuits, the phase current I_{ph} is evenly distributed into half of the amount. In case the current falls beneath the threshold $I_{ph,lim}$, recharging will not be completed during dead time T_{dt} and switch-on time T_{on} of the lower IGBT. Thus, the second IGBT causes an infinitely high voltage slope at the transition to section (3) by turning on. Accordingly, the voltage U_{IGBT} of the IGBT is now applied to the load. The present current i_{C2} is now determined by the voltage U_{IGBT} and the components of the capacitance C_{sc2} and the resistance C_{sc2}. The first order time lag behavior of the current i_{C2} is reflected in both, the current i_{C1} flowing in the upper capacitor C_{sc1} and the current i_{S2} flowing in the second IGBT. When capacitor C_{sc1} is fully charged and C_{sc2} is discharged within the charge reversal time T_{cr}, diode D_2 initiates conduction in section (4) so that the commutation from IGBT S_1 to diode D_2 is successfully executed.

Knowing the threshold current $I_{ph,lim}$ is now of significance as the transition point between the distinct phase-voltage patterns can be established as calculations for the mathematical model will rely on this current limit. Two equations for charges serve as the foundation for the determination of the threshold current $I_{ph,lim}$. The electric charge Q as the product of current I_{ph} and time (equation (3.13a)), and simultaneously, the electric charge Q is equal to the product of applied voltage U_{dc} to the capacitors C_{sc} of both switching cells of the inverter leg (equation (3.13b)).

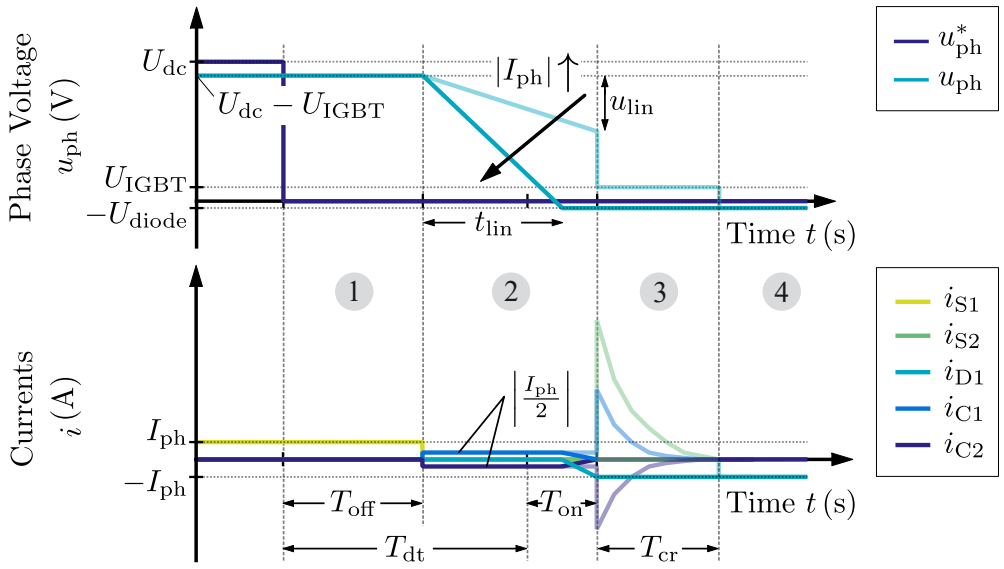


Figure 3.3: Simulated commutation at positive phase current I_{ph} (cf. [54])

$$Q = I_{ph} \cdot t \tag{3.13a}$$

$$Q = 2C_{sc} \cdot U_{dc} \tag{3.13b}$$

If the nonideal voltage values and also the respective time during the PWM-period are considered, the resulting limit current $I_{ph,lim}$ can be determined (equation (3.14)).

$$|I_{ph,lim}| = \frac{2C_{sc} \cdot (U_{dc} \pm U_{IGBT} \mp U_{diode})}{T_{dt} + T_{on} - T_{off}} \tag{3.14}$$

The mathematical model for an accurate volt-second error $\bar{\psi}_{pwm,err}$ during one PWM-period will now be developed on the basis of the simulation results.

3.1.2 Mathematical Model of Voltage-Distortion

The combination of voltage amplitude and time distortions enables the determination of distortion volt-second area $\bar{\psi}_{pwm,err}$, providing a detailed analysis of the switching properties of a IGBT-based half-bridge. The mathematical models yield three different levels of complexity that are related to each other. The initial and most basic model focuses solely on the divergent rectangular volt-second areas (cf. Fig. 2.6) and is therefore labeled

the *rectangular model*. The phase current I_{ph} is assumed to be infinite resulting in a volt-second area during commutation from an IGBT to a diode that is zero (cf. Fig. 3.3, phase voltage u_{ph}, section (2)). This results in equation (3.15) for volt-second error $\bar{\psi}_{\mathrm{pwm,err}}$ during one PWM-period

$$\bar{\psi}_{\mathrm{rect,err}} = \mp\Delta T \cdot \Delta U + \begin{cases} -T_{\mathrm{pwm}} \cdot \left(dU_{\mathrm{IGBT}} + (1-d)U_{\mathrm{diode}}\right), & \text{if } I_{\mathrm{ph}} > 0 \\ +T_{\mathrm{pwm}} \cdot \left(dU_{\mathrm{diode}} + (1-d)U_{\mathrm{IGBT}}\right), & \text{if } I_{\mathrm{ph}} < 0 \end{cases} \tag{3.15}$$

with the following summarized differences in equation (3.16) for the given voltages and time intervalls. These voltage and time differences were also depicted in the formular for the threshold current $I_{\mathrm{ph,lim}}$ in equation (3.14).

$$\Delta U = U_{\mathrm{dc}} + U_{\mathrm{diode}} - U_{\mathrm{IGBT}} \tag{3.16a}$$

$$\Delta T = T_{\mathrm{dt}} + T_{\mathrm{on}} - T_{\mathrm{off}} \tag{3.16b}$$

Equation (3.15) describes in the first term the volt-second losses due to commutation, and in the second term the volt-second errors during on- and off-state. Identification of the conducting semiconductor is easily accomplished through observation of the corresponding voltage drop.

The development of a more exact model during commutation time is based on the simulation results. This mathematical model is labeled as *full model*. For this purpose, the phase current is now assumed to be finite leading to volt-second errors during commutation that are dependent on the phase current (cf. Fig. 3.3, section (2)). A differentiation is established here by considering whether the phase current is under or over the threshold current $I_{\mathrm{ph,lim}}$, as previously outlined.
First, the absolute phase current value $|I_{\mathrm{ph}}|$ should be greater or equal than the limit current $|I_{\mathrm{ph,lim}}|$ resulting in the *linear case* in which commutation from IGBT to diode is completed within the time duration ΔT. The time t_{lin} needed to finalize the commutation process relies on the phase current I_{ph} and can be calculated utilizing equation (3.17).

$$t_{\mathrm{lin}}(I_{\mathrm{ph}}) = \frac{(U_{\mathrm{dc}} - U_{\mathrm{IGBT}}) \cdot C_{\mathrm{sc2}}}{I_{\mathrm{ph}}/2} \tag{3.17}$$

During this interval, the volt-second error $\bar{\psi}_{\mathrm{lin,err}}$ in equation (3.18) is being calculated. This result reveals that the volt-second error in the linear case is inversely proportional to the phase current.

$$\bar{\psi}_{\mathrm{lin,err}}(I_{\mathrm{ph}}) = \frac{(U_{\mathrm{dc}} - U_{\mathrm{IGBT}})^2 \cdot C_{\mathrm{sc2}}}{I_{\mathrm{ph}}} \tag{3.18}$$

Second, the absolute phase current value $|I_{\mathrm{ph}}|$ should be less than the limit current $|I_{\mathrm{ph,lim}}|$ resulting in the *nonlinear case*, i. e. the completion of the commutation process is unattainable within the given time ΔT. The deviating volt-second error $\bar{\psi}_{\mathrm{nonlin,err}}$ is now described by the difference between two volt-second areas. In this case, the height of the voltage step correlates with the phase current like equation (3.19) shows.

$$u_{\mathrm{lin}}(I_{\mathrm{ph}}) = \frac{\Delta T}{C_{\mathrm{sc2}}} \cdot \frac{I_{\mathrm{ph}}}{2} \tag{3.19}$$

In this nonlinear case, a linear correlation between the volt-second deviation $\bar{\psi}_{\mathrm{nonlin,err}}$ and the phase current I_{ph} results in equation (3.20).

$$\bar{\psi}_{\mathrm{nonlin,err}}(I_{\mathrm{ph}}) = (U_{\mathrm{dc}} - U_{\mathrm{IGBT}}) \cdot \Delta T - \frac{I_{\mathrm{ph}} \Delta T^2}{4 C_{\mathrm{sc2}}} \tag{3.20}$$

In addition to this deviation $\bar{\psi}_{\mathrm{nonlin,err}}$, the voltage-time-area error must be supplemented with the volt-second error $\bar{\psi}_{\mathrm{cr,err}}$ caused by the conducting IGBT during charge reversal of both additional capacitors C_{sc}. The transfer function (TF) is preferred for analyzing the switching cell with the current $I_{\mathrm{C2}}(s)$ flowing through the ohmic-capacitive impedance as output quantity and the voltage drop $U_{\mathrm{IGBT}}(s)$ across the conducting IGBT as output quantity. The inverse Laplace transform enables the equation of the derivative-element with first order lag in time domain (equation (3.21)).

$$\frac{I_{\mathrm{C2}}(s)}{U_{\mathrm{IGBT}}(s)} = \frac{s C_{\mathrm{sc2}}}{1 + s R_{\mathrm{sc2}} C_{\mathrm{sc2}}} \quad \overset{\mathcal{L}^{-1}}{\bullet\!\!-\!\!\circ} \quad i_{\mathrm{sc2}}(t) = \frac{u_{\mathrm{IGBT}}(t)}{R_{\mathrm{sc2}}} \cdot \mathrm{e}^{-\frac{t}{R_{\mathrm{sc2}} C_{\mathrm{sc2}}}} \tag{3.21}$$

The author assumes that the charge reversal process is completed once the current $i_{\mathrm{C2}}(t)$ attains zero. Within the scope of control theory, this occurs after the passage of five times the time constant. This time interval T_{cr} is dependent on passive components with fixed values. Thus, the voltage $u_{\mathrm{IGBT}}(t)$ of the IGBT solely influences the charge reversal, which, however, is also constant. The resulting volt-second error $\bar{\psi}_{\mathrm{cr,err}}$ in equation (3.22) is therefore a constant value.

$$\bar{\psi}_{\mathrm{cr,err}} = U_{\mathrm{IGBT}} \cdot T_{\mathrm{cr}} = U_{\mathrm{IGBT}} \cdot 5 R_{\mathrm{sc2}} C_{\mathrm{sc2}} \tag{3.22}$$

If these volt-second errors are finally totalized, the result of the total averaged volt-second $\bar{\psi}_{\mathrm{pwm,err}}$ depending on the phase current I_{ph} over one PWM-period is depicted by equation (3.23).

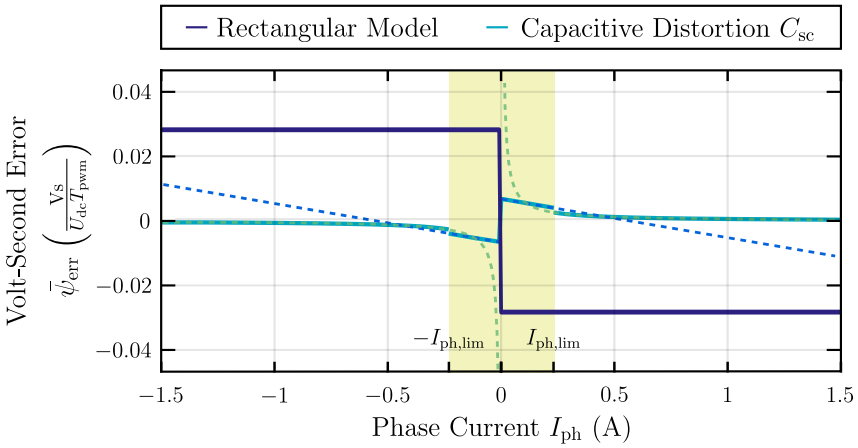


Figure 3.4: Volt-second erros $\bar{\psi}_{err}$ as a function of phase current I_{ph}

$$\bar{\psi}_{pwm,err}(I_{ph}) = \bar{\psi}^{\bigstar}_{rect,err} + \begin{cases} \bar{\psi}_{lin,err}, & \text{if } |I_{ph}| \geq |I_{ph,lim}| \\ \bar{\psi}_{nonlin,err} + \bar{\psi}_{cr,err}, & \text{if } |I_{ph}| < |I_{ph,lim}| \end{cases} \tag{3.23}$$

It is important to ensure that the time intervals, and thus, the volt-second distortion $\bar{\psi}^{\bigstar}_{rect,err}$ of the reactangular model is adapted since the time t_{lin} of the full model must be taken into account. In conclusion, it is important to highlight that the comprehensive development of the full model of an IGBT-based PWM VSI is conducted due to frequent inaccuracies or calculation errors identified in previous research.

Figure 3.4 illustrates both volt-second distortions, the volt-second error $\bar{\psi}_{rect,err}$ of the rectangular model, and the separated volt-second error caused by the additional capacitors C_{sc}. The impact of phase current I_{ph} on the volt-second error, taking into account the capacitive effect, is apparent. The yellow background color serves to highlight the linear case in which the phase current I_{ph} is lower than the threshold current $I_{ph,lim}$. The nonlinear case is in an inversely proportional relation to phase current I_{ph} is observable that causes the capacitively induced volt-second error to rapidly decay to zero. Dashed lines are utilized to demonstrate the continuation of volt-second distortion for the full range of the plot.

Combining both volt-second impacts demonstrates that the error reaches a steady state at a certain phase current magnitude (Fig. 3.5). In case where negative volt-second errors coincides with a positive phase current, the VSI output results with a reduced number of volt-seconds. Conversely, negative phase currents always exceed the desired average volt-second value. The minor influence of the capacitive effect on the average voltage-time area is readily apparent from the visual depiction of the derivated equations in Fig. 3.4 and Fig. 3.5, respectively. Even with low levels of current below $I_{ph,lim}$ (the nominal current of the module considered here numbers 760 A), the largest influence is almost negligible. Nevertheless, these particular influences at low currents and small duty cycles

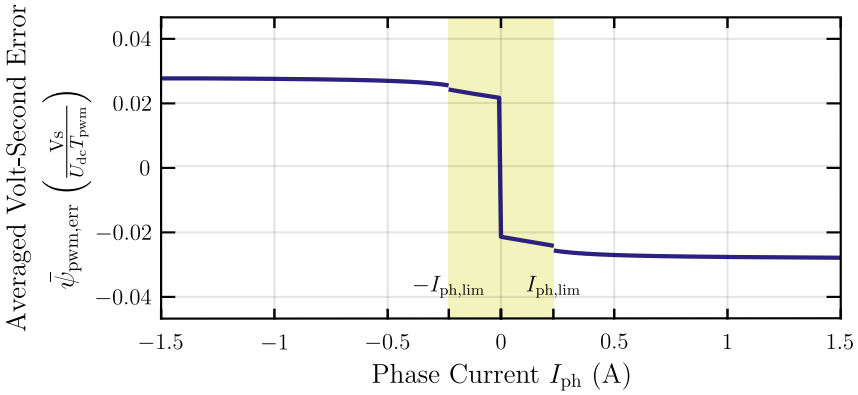


Figure 3.5: Averaged volt-second error $\bar{\psi}_{\mathrm{pwm,err}}$ over one PWM-period of full model

are a crucial part of this study, because a model that is accurate as possible is the overall goal regardless optimization of computational resources.

The evaluation of the influence of three variable input parameters is performed as part of the integration of the model into an MBFF measurement technique. The variable input parameters are the measured dc-link voltage $U_{\mathrm{dc}}^{\Diamond}$, the actual duty cycle d, and the measured phase current $i_{\mathrm{ph}}^{\Diamond}$.
The most significant parameter in this context is the phase current as the case differentiation is determined by this quantity (equation (3.23)). Figure 3.6 illustrates the impact of a superimposed current measurement inaccuracy on volt-second deviation within the full model. The most significant discrepancies (exceeding 4 % relative to the voltage-time area of dc-link voltage U_{dc} and PWM-period T_{pwm}) occur if the case differentiation inaccurately determines the polarity of phase currents. Hence, if the noise from the current sensor is higher than the phase current i_{ph} it is meant to detect, the full model will produce major inaccuracies, leading to unreliable results. Errors in volt-seconds below 0.5 % occur if the magnitude of phase current i_{ph} is overestimated, as indicated by the expressions that detail the effects of the capacitive distortion. At high phase current magnitudes, even a 0.5 A measurement noise is considered insignificant since the capacitive influence becomes negligible. In essence, precise identification of phase current polarity outweighs the significance of general current sensor accuracy.

It is common practice to combine volt-second error models or rather voltage distortion models with adaptation algorithms that incorporate feedback from the system that the model is applied to [51], [98], [99]. Additionally, the model's acquired data can be utilized in reverse to adjust system estimated parameters in real-time [53]. As the upcoming setup will not replicate the complete integration of this model into a three-phase drive system, thereby preventing the establishment of a feedback loop for model adjustments while in operation, the model is utilized in a feedforward approach.

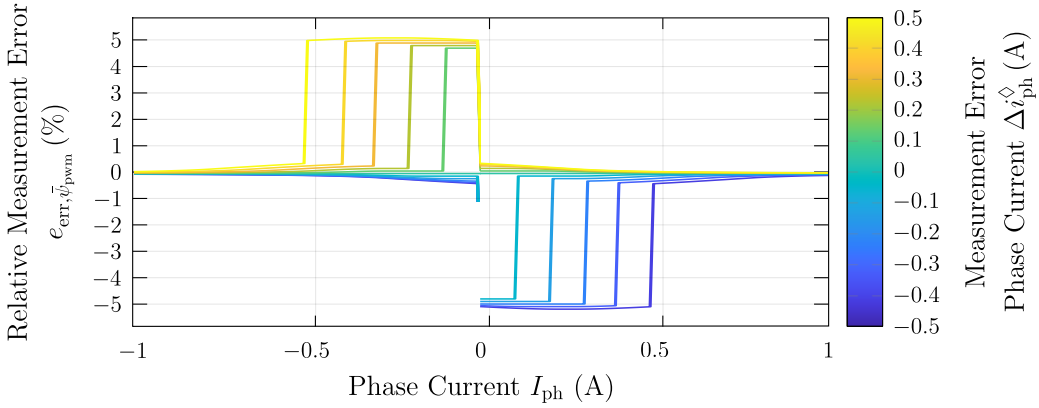
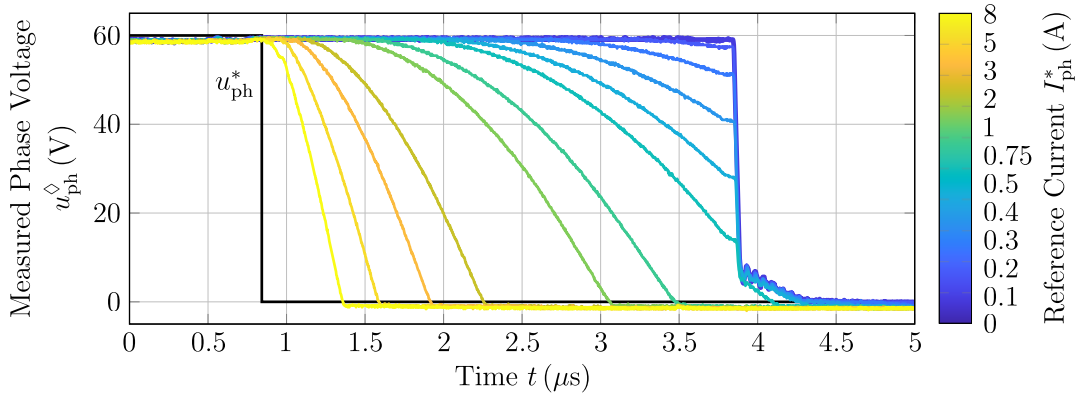


Figure 3.6: Impact of current measurement error on full-model accuracy

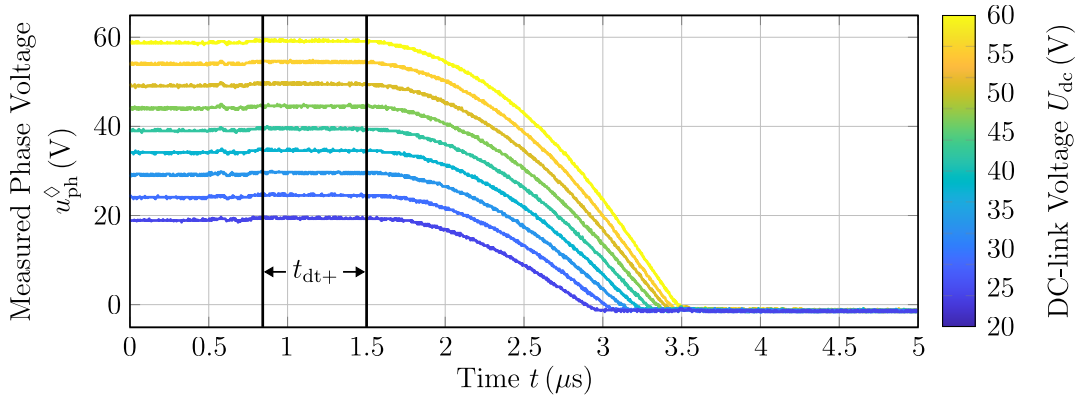
3.1.3 Validation of Voltage-Distortion Model

The evaluation of the simulative and mathematical model is conducted by measuring the analyzed SEMIKRON trench IGBT module SKM 600GB066D [97] on the test bench that will be introduced in detail in Section 4.2. The precision of the volt-second distortion model in replicating IGBT switching behavior of one module and, thus, a half-bridge is examined considering the trajectories of the phase voltage u_{ph}. Measurements for phase voltage u_{ph} are conducted with an oscilloscope for various dc-link voltage levels U_{dc}, and reference phase currents I_{ph}^{*} set with the load side current source. The current that is being examined is the constant reference phase current I_{ph}^{*} of the current source, not the measured phase current $i_{\mathrm{ph}}^{\diamondsuit}$, as will be explained in Section 4.2. It is important to note this discrepancy as the measured phase current $i_{\mathrm{ph}}^{\diamondsuit}$ may not consistently correspond with the reference current I_{ph}^{*}, especially for low current magnitudes. A total of 108 OPs is carried out for nine dc-link voltages U_{dc} from 20 V to 60 V, and 12 reference currents I_{ph}^{*} between 0 A and 8 A to analyze the capacitive effect during commutation. Measurements are constrained to a maximum of 60 V due to limitations in the available test bench equipment (cf. Section 4.2). The impact of these two parameters on the switching behavior of the IGBT half-bridge can be seen in Fig. 3.7. Fig. 3.7a shows a reference current sweep at a dc-link voltage of 60 V, while Fig. 3.7b depicts a dc-link voltage sweep at a reference phase current of 0.75 A.

The simulated phase voltage trajectory u_{ph} matches the measured phase voltage $u_{\mathrm{ph}}^{\diamondsuit}$ for almost the entire PWM-period. Yet, a more in-depth investigation needs to be conducted during commutation towards the diodes as Fig. 3.7 shows. Basically, the measurement results verify the case differentiation between the linear and nonlinear case since the voltage tail of the IGBT appears when the threshold current $I_{\mathrm{ph,lim}}$ is undershot and the IGBT S_2 conducts once the dead time T_{dt} elapsed. Despite this, there is a discrepancy regarding the characterization of the phase voltage waveform $u_{\mathrm{ph}}^{\diamondsuit}$ in section (2) (Fig. 3.3) using a linear equation that starts after the turn-off delay T_{off} of IGBT S_1 has ended. The measurements in Fig. 3.7a reveal that the reference phase current level I_{ph}^{*} impacts



(a) Measured phase voltage $u_{\mathrm{ph}}^{\Diamond}$ with variable I_{ph}^{*} and $U_{\mathrm{dc}} = 60\,\mathrm{V}$



(b) Measured phase voltage $u_{\mathrm{ph}}^{\Diamond}$ with variable U_{dc} and $I_{\mathrm{ph}}^{*} = 0.75\,\mathrm{A}$

Figure 3.7: Measured phase voltage $u_{\mathrm{ph}}^{\Diamond}$ trajectories

the start of phase voltage decrease and, additionally, the voltage gradient. Furthermore, the negative voltage gradient is more similar to a second-degree polynomial rather than a linear equation. The measurements in Fig. 3.7b illustrate that varying dc-link voltage U_{dc} does not impact the starting point when the phase voltage begins to decrease, even though a minor dependency on the voltage slope is recognizable, which needs further analysis.

The turn-off process of IGBT S_1 starts with a falling gate voltage u_{ge} reducing the channel current. Simultaneously, the gate-collector current i_{gc} starts charging the Miller capacitance C_{gc} and the quasi-parallel output capacitance C_{ce} that is equal to C_{sc1}. Afterwards, the voltage commutation starts slowly but barely detectable as the output capacitance C_{ce} decreases with increasing voltage drop u_{ce}. This confirms to the varying starting point of phase voltage decreasing since the charging process of the Miller capacitance C_{gc} and the output capacitance C_{ce} depends on the actual phase current i_{ph}.
As the gate voltage u_{ge} cannot be further reduced requiring the entire gate current to discharge the Miller capacitance C_{gc}, the gate plateau occurs when the channel current is nearly zero. At the same time, almost the entire phase current i_{ph} still charges the output capacitance C_{ce} of IGBT S_1, which is also reflected in the visible voltage drop of the phase voltage u_{ph}. It is a drawback that the simulation model cannot accurately

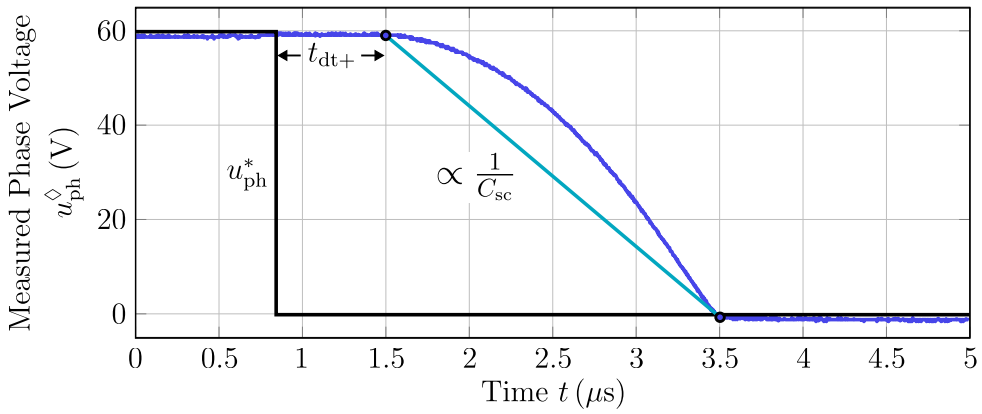


Figure 3.8: Modification of full model to measured phase voltage $u_{\mathrm{ph}}^{\diamond}$, $U_{\mathrm{dc}} = 60\,\mathrm{V}$, $I_{\mathrm{ph}}^{*} = 0.75\,\mathrm{A}$

depict this changing starting point $t_{\mathrm{dt+}}$.

Measuring the IGBT module enables the preciseness of the voltage distortion model through the utilization of LUTs during the commutation process. The rectangular model is retained and the corresponding functions $t_{\mathrm{dt+}}(I_{\mathrm{ph}}^{*}, U_{\mathrm{dc}})$ and $C_{\mathrm{sc}}(I_{\mathrm{ph}}^{*}, U_{\mathrm{dc}})$ are mapped instead of the linear or non-linear volt-second deviations. For this purpose, the commutation time interval is split into the additional time delay $t_{\mathrm{dt+}}$ and a linearized section with a variable and determined parallel capacitance C_{sc} (Fig. 3.8). The evaluation is performed based on the measurements of the previously mentioned 108 OPs for variantions of the dc-link voltage U_{dc} and the reference phase current I_{ph}^{*}. The results of both functions are shown in Fig. 3.9. The additional time delay $t_{\mathrm{dt+}}$ is solely influenced by the reference phase current I_{ph}^{*} (Fig. 3.9, left), as already seen by the dc-link voltage sweep in Fig. 3.7b. Regardless of the dc-link voltage levels, an analogous reduction in time delay $t_{\mathrm{dt+}}$ is observed as the reference phase current I_{ph}^{*} increases. The additional capacitance C_{sc} exhibits a dependency on both parameters, the dc-link voltage U_{dc} and the reference phase current I_{ph}^{*} (Fig. 3.9, right). Both rising dc-link voltage and reference current result in higher capacitance values. If the additional delay time $t_{\mathrm{dt+}}$ emains throughout the entire commutation section, the capacitance C_{sc} is equal zero. When linear behavior is observed, the determined capacitance is found to be significantly greater than the specified capacitance C_{oes} that equals 2.3 nF in the datasheet [97]. As conditions for output capacitance measurement in the datasheet are collector-emitter voltages u_{ce} of 25 V and a frequency of 1 MHz. It is improbable that the variance in output capacitance C_{oes} is due to difference in voltage levels between the dc-link voltage and the nominal voltage of the IGBT module. The capacitances of the datasheet might be biased by the high frequency, resulting in noticeable differences when compared to the measurements taken.

In conclusion, concerning modeling, it can be concluded that the goal of this study is to validate a precise simulation model that is straightforward to implement and rapid to execute. The PLECS model evaluation reveals that the quality of the simulated phase voltage trajectories align acceptably with the test bench measurements. The highly non-

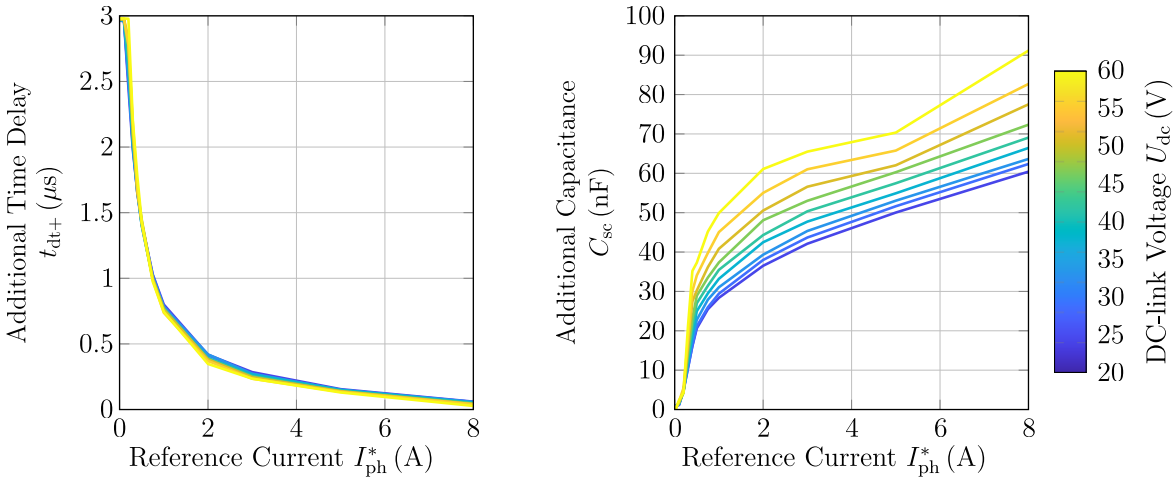


Figure 3.9: Evaluation of measured voltage distortion model parameter $t_{\mathrm{dt+}}$ and C_{sc}

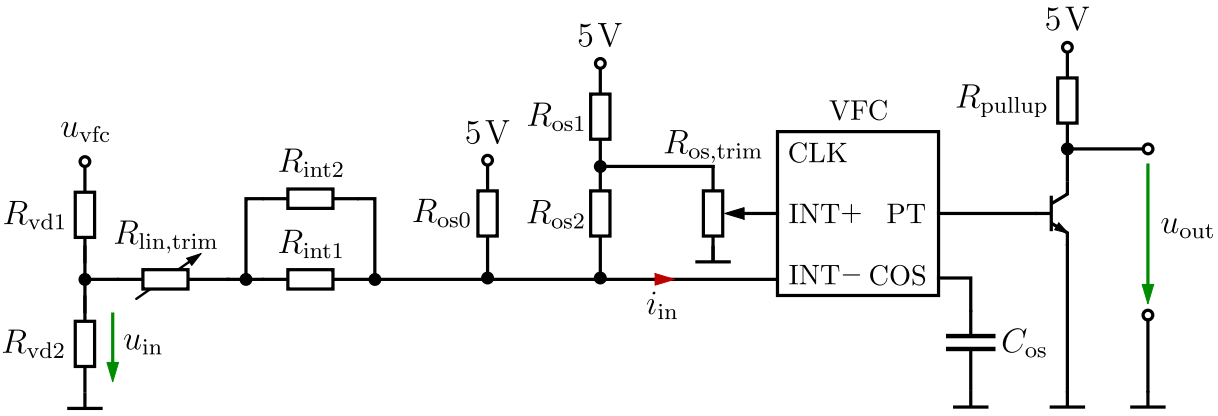
linear nature of the processes in the switching cell as described in [100] is not adequately depicted in this model. Nonetheless, the purpose of this modeling approach should not fullfil those requirements. Elaborate models like the three-capacity model are appropriate for this purpose but cannot be utilized in PLECS due to programming constraints as explained in [54]. The simulation model introduced in this section is therefore recommended for implementation in offline control appoaches for electrical drive trains. Finally, an analytical model is established using the simulation results, which will be employed for an online MBFF measurement technique later in this investigation (Section 4.3).
Outlined below are remarks concerning the measurement. The required dc-link voltage U_{dc} for this volt-second distortion MBFF approach is acquired by an averaged, possibly varying, dc-link voltage measurement over one switching period. The limited time averaging is utilized to reduce noise while maintaining the capability to respond to fluctuations in dc-link voltage between periods. The duty cycle d necessary for the model corresponds to the reference duty cycle established by the VSI's control algorithm. The most crucial quantity is also the most challenging to provide: the actual phase current i_{ph}. Accurate measurement is crucial for optimal results during commutation from IGBT and diode as the divergence of volt-seconds is influenced by the polarity of the phase current as discussed in this section. As the reference phase current I^*_{ph} of the current source is not accessible for the rapid control prototype (RCP)-system, a current transducer [101] and a current clamp [102] sample and average the measured phase current $i^{\Diamond}_{\mathrm{ph}}$ during commutation. Another approach would be to apply a dead-time current predictor that uses a PWM-period averaged phase current and machine parameters to reconstruct the phase current ripple, which for positive phase currents is at its maximum during dead time commutations toward diodes. The preferred strategy in this study is to apply current measurement.

3.2 Measuring Techniques with Voltage-to-Frequency Converters

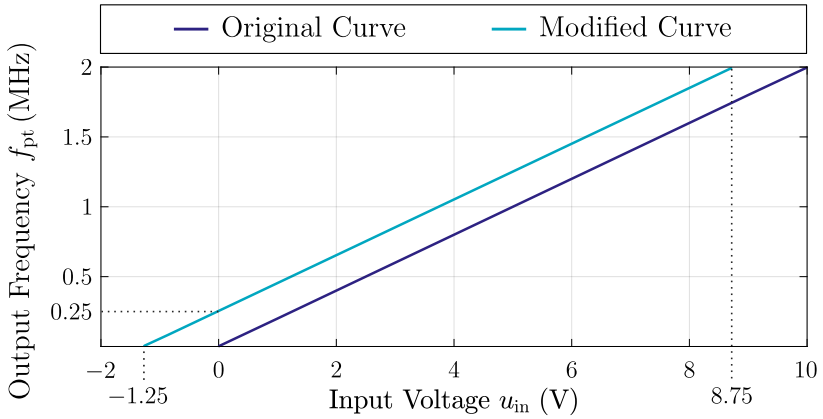
Commercial VFCs are considered as a further approach of direct volt-second measurement. The evaluation of phase voltage sensing is presented here as most common measurement methods refer to instantaneous voltage measurement and not volt-second measurement. Additionally, the reference measurement is employed on an oscilloscope and therefore voltage is the quantity of choice. Yet, it becomes apparent that the conversion from volt-seconds to volts during a PWM-period is only dependent on the scaling in relation to the switching frequency. All measurements are performed with the SEMIKRON trench IGBT module SKM 600GB066D [97] on a test bench that will be introduced in detail in Section 4.2.
The volt-second approaches are single-ended measurement techniques, which are compared to each other in Section 4.3. Section 3.1.1 demonstrated that positive and negative phase current i_{ph} behave very similarly to each other. There is a difference in semiconductor voltage drops between the two cases of positive and negative phase current, and capacitive dead-time effects are observed during the transition to the opposite phase voltage level. However, a different current polarity does not show significant differences in behavior, hence supporting the utilization of the outlined setup to focus on positive phase currents exclusively.

The basis of these measurement methods is on the one hand an AVFC and on the other hand an SVFC whose commonalities and differences are discussed in Section 2.4. This section presents various analysis methodologies for the determination of the instantaneous volt-second value ψ_{ph} over one PWM-period based on one commercial IC each. An identical external circuitry with its setting option, which is utilized for both ICs, is presented first before a detailed explanation on well-known and novel evaluation methods used for determining volt-seconds follows.

The manipulation of the input current i_{in} and subsequent adjustment of the input voltage range of VFCs can be achieved through various options as shown in Fig. 3.10a. Firstly, the obligatory input voltage divider brings the phase voltage u_{ph} in the range of acceptable IC input voltages u_{in}. The components preceding the VFC serve the purpose of modifying the characteristic curve to meet the desired design target (Fig. 3.10b). The resistor R_{os0} imposes a static offset to enable the detection of negative diode voltage drops, injecting an additional fixed offset input current that is 1/8 of the internal current source of the IC. A trim potentiometer $R_{\mathrm{lin,trim}}$ manipulates the total series input resistance of the VFC adjusting gain or linearity of the characteristic curve, respectively. Another potentiometer $R_{\mathrm{os,trim}}$ allows to elevate integrator bias voltage at the INT+ pin slightly above ground to fine-tune the static adjustment of the resistor R_{os0}. Only the SVFC offers the possibility of utilizing the clock input. Section 4.2.3 discusses the evaluation of the VFC measurement methodologies in detail. The signal processing of the RCP-system is presented for this objective.



(a) External circuity of VFCs



(b) Characteristic curve for measurements of half-brdige

Figure 3.10: Design for asymmetric bipolar voltage input range

3.2.1 VFC with Pulse Counting Calibration

As previously explained in Section 2.4 and also stated by its name, the VFC converts an input voltage into an output pulse train with a certain frequency that is proportional to the input voltage. The main contrast between an AVFC (Fig. 2.11) and an SVFC (Fig. 2.12) is that the output pulse width of the AVFC is solely defined by the one-shot block. The SVFC is superior to the AVFC in ensuring the precision of the output pulse width as the input clock frequency f_{clk} is considerably more precise than the one shot module. However, the advantage of the AVFC's solely dependence of the one shot module is a continuousness in generating output pulses, while the SVFC exhibits an intrinsic delay through the synchronization with the input clock frequency f_{clk}.
For this study, the selected AVFC IC is the VFC110 [76] and it is compared with the SVFC IC AD652 [90]. As stated before, the design objective illustrated in Fig. 3.10 is applied to both VFCs, even though the AVFC can produce frequencies of up to 4 MHz, albeit with lower anticipated linearity compared to the SVFC's maximum output frequency of 2 MHz. Consequently, the AVFC is designed for a 2 MHz frequency to ensure valid comparisons

Table 3.2: Components of SVFC circuit for pulse calibration

Voltage divider		Linearity				Offset				Output	
R_{vd1}	R_{vd2}	R_{int1}	R_{int2}	$R_{\mathrm{lin,trim}}$	C_{int}	R_{os0}	R_{os1}	R_{os2}	$R_{\mathrm{os,trim}}$	R_{pullup}	C_{os}
52.3 kΩ	7.5 kΩ	20 kΩ	2 MΩ	500 Ω	50 pF	80 kΩ	350 kΩ	20 kΩ	500 Ω	680 Ω	0 F

Table 3.3: Components of AVFC circuit for pulse calibration, pulse counting feed-forward, and pulse counting and frequency feed-forward method

Voltage divider		Linearity				Offset				Output	
R_{vd1}	R_{vd2}	R_{int1}	R_{int2}	$R_{\mathrm{lin,trim}}$	C_{int}	R_{os0}	R_{os1}	R_{os2}	$R_{\mathrm{os,trim}}$	R_{pullup}	C_{os}
52.3 kΩ	7.5 kΩ	100 kΩ	56 kΩ	1 kΩ	50 pF	144 kΩ	340 kΩ	20 kΩ	500 Ω	680 Ω	56 pF

between the two VFCs. The calibration of both VFCs, along with their external circuitry, follows the characteristic curve in Fig. 3.10b within the −1.25 V to 8.75 V input voltage range and the 0 Hz to 2 MHz output frequency range, enabling the storage of gain and offset parameters in the software. Consequently, the output frequency f_{pt} is correlated back to the input voltage u_{in} through the resulting linear function. The component values for both external circuitry are listed in Table 3.2 for the SVFC and Table 3.3 for the SVFC.

According to the datasheet of the VFC110, a precision monostable causes the SPDT switch to move to position L resulting in an output pulse whose length is defined by the one-shot capacitor C_{os} connected to the COS pin. While the SVFC outperforms the AVFC variant in terms of output pulse width, linearity, and precision, the latter does offer the advantage of advanced output pulse interpretation techniques due to its entirely continuous nature of the output frequency that are introduced in the following sections.

3.2.2 AVFC with Pulse Counting Feed-Forward

One pulse N of the VFC's output pulse train $u_{\mathrm{pt}}(f_{\mathrm{pt}})$ is the smallest amount of volt-seconds that is achievable. For this reason, it is commonly referred to as volt-second resolution or volt-second quantum ψ_ε (equation (3.24)). Section 3.3.2 and [83] cover the process of determining the volt-second resolution ψ_ε represented by one output pulse in detail.

$$\psi_\varepsilon := \frac{u_{\mathrm{in,range}}}{f_{\mathrm{pt,range}}} \tag{3.24}$$

The volt-second quantum ψ_ε is mapped to the volt resolution ψ_ε by scaling with the switching frequency f_{sw} of the VSI like shown in equation (3.25).

$$u_\varepsilon := \psi_\varepsilon \cdot f_{\mathrm{sw}} \tag{3.25}$$

After establishing the weight of a pulse, the number of pulses N in each PWM-period needs to be counted, which are then multiplied by the volt-second quantum ψ_ε or volt quantum ψ_ε to derive the averaged volt-second value $\bar{\psi}_{\mathrm{pwm}}$ (equation (3.26a)) or the averaged volt value $\bar{u}_{\mathrm{pwm}}$ (equation (3.26b)) over one PWM-period. Thus, in the pulse counting method, the resolution value of volt-second or volt, respectively, is predetermined establishing it as a feed-forward strategy.

$$\bar{\psi}_{\mathrm{pwm}} = N \cdot \psi_\varepsilon \tag{3.26a}$$

$$\bar{u}_{\mathrm{pwm}} = N \cdot u_\varepsilon \tag{3.26b}$$

The advantages of counting pulses are exemplary the simple provision of galvanic isolation, and the high noise immunity at transmission as well as the integrated voltage is readily available for digital signal processing without the need for another ADC.

3.2.3 AVFC with Pulse Counting and Time Sensing Feed-Forward

Since the output frequency f_{pt} of the AVFC is continuous, low frequencies and therefore long time durations between pulses can be measured additionally to solely counting the pulses over a PWM-period. The benefit of measuring time intervals Δt_{P2P} between two pulses instead of measuring pulses N themselves can be outlined as such: In case a high input voltage is applied to the VFC, it delivers accurate results, while achieving satisfactory resolution within a reasonable sample time is challenging for a slow running VFC generating only a few pulses. Therefore, it is more promising to measure the time Δt_{P2P} between two pulses. This measured time interval Δt_{P2P} can be inverted to its corresponding frequency f_{pt} and this in turn is converted back to an input voltage by utilizing the AVFC's characteristic curve illustrated in Fig. 3.10b. The determined input voltage represents the average voltage $\bar{u}_{\mathrm{in,P2P}}$ between these two pulses. This process of time measurement offers a different way to interpret the pulse train applying identical hardware.

The following analysis contrasts the pulse counting and time-sensing approach in resolution u_ε. Setting the sampling frequency f_{samp} of the digital input that processes the output pulse train $u_{\mathrm{pt}}(f_{\mathrm{pt}})$ equal 10 MHz, calculation of time sensing resolution is enabled. The resolution of the pulse counting method is carried out as explained in the section before; the calculated volt quantum u_ε is utilized by multiplying it by the number of pulses N (equation (3.26b)). Both resolutions are now compared within a PWM-period of a VSI in (Fig. 3.11). The resolution u_ε is normalized to a dc-link voltage U_{dc} of 60 V, the applied

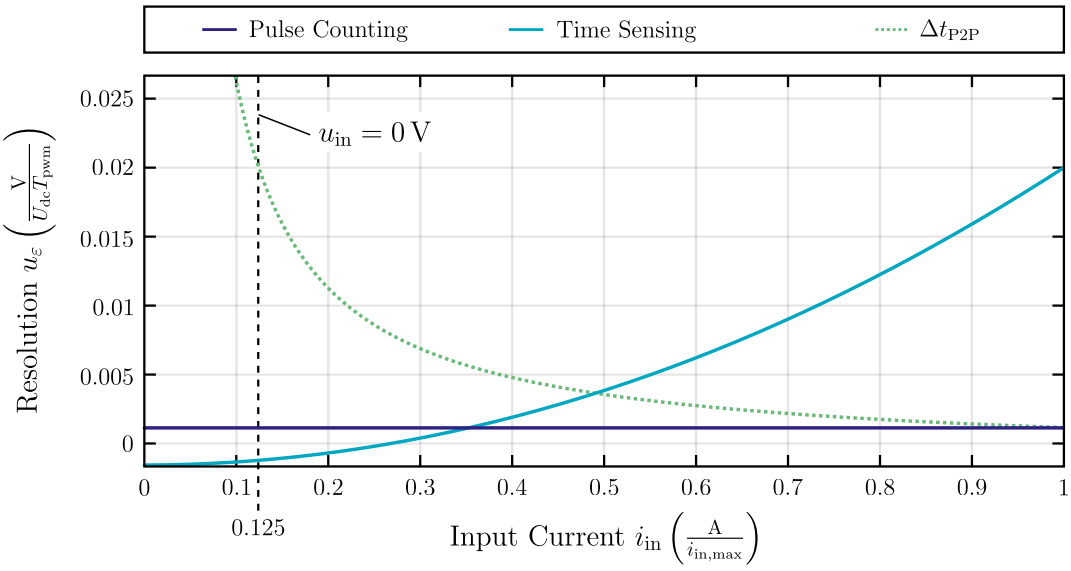


Figure 3.11: Resolution of pulse couting and time sensing of an AVFC

inverter switching frequency f_{sw} leading to a PWM-period of 0.2 ms, and an maximum input current i_{in} of the AVFC of 0.5 mA (cf. Fig. 3.10a).

The key motivation for incorporating both evaluation strategies lies in the ability to exploit the superior level of resolution in their best performing range. As already mentioned, Fig. 3.11 shows that the time sensing method is outstanding at low input voltages u_{in}, while the pulse counting method is superior at high voltage input u_{in}. As a consequence, the PWM-period is split into two parts: The first part is when the dc-link voltage U_{dc} is applied to the load and, thus, a high input voltage u_{in} results in a high input current i_{in}. Accordingly, the second part corresponds to the upper switch of the half-bridge opened resulting in a slightly negativ input voltage u_{in} for positive phase currents i_{ph}. Figure 3.12 further illistrates this concept of utilizing the method of pulse counting first, and time sensing second at a duty cycle d of 0.4. Combining these two methods yields the following equation (3.27) for the instantaneous voltage $\bar{u}_{\mathrm{pwm}}$:

$$\bar{u}_{\mathrm{pwm}}(N, \Delta t_{\mathrm{P2P}}) = N \cdot u_\varepsilon|_{u_{\mathrm{in,high}}} + \sum \bar{u}_{\mathrm{in,P2P}}(\Delta t_{\mathrm{P2P}})\Big|_{u_{\mathrm{in,low}}} \quad \text{with } \Delta t_{\mathrm{P2P}} = {f_{\mathrm{pt}}}^{-1} \tag{3.27}$$

Distinguishing between these two input voltage levels is achieved by implementing an edge detection that relies on the pulse train frequency defining a threshold for the time interval between two pulses. If this time threshold is exceeded, a low input voltage level is detected. It is essential to note that the interpretation of time measurement is based on the observation of two pulses occurring within one PWM-period. Therefore, left-aligned PWM is advantageous for this combined evaluation method maximizing the low level duration.
The design aim in Fig. 3.10b indicates that the combination of pulse counting and time

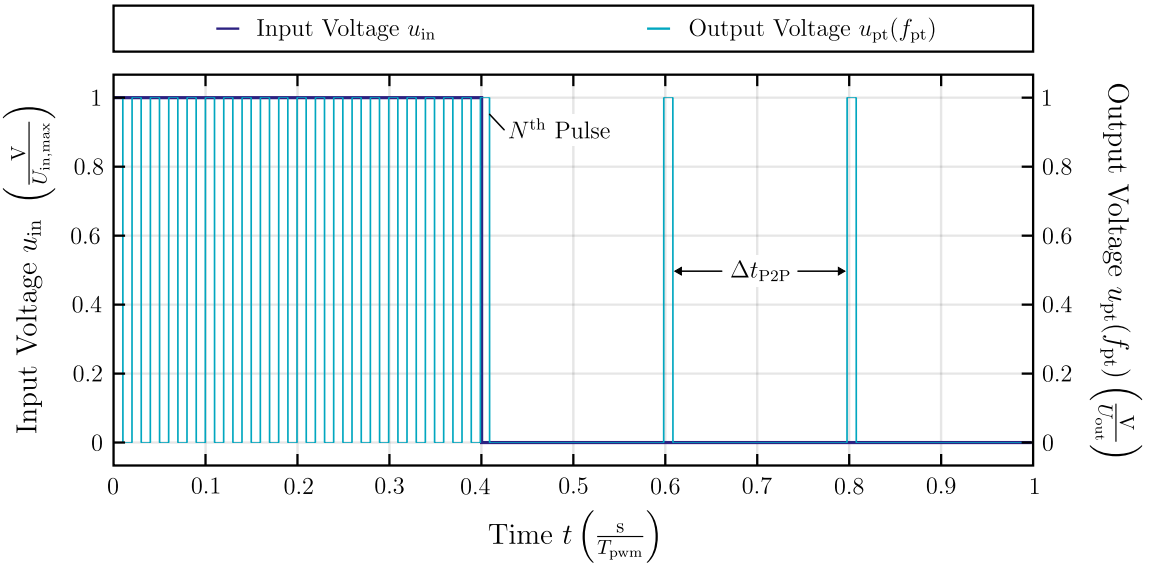


Figure 3.12: Concept of pulse couting and time sensing of an AVFC

sensing is anticipated to operate until a duty cycle of approximately 97 %, given that the time interval between pulses for small negative voltages must not exceed 3 % of the PWM-period T_{pwm} (Fig. 3.11). Since the external circuitry is designed to exhibit only a few pulses at a low input voltage level, the average voltage $\bar{u}_{\text{in,P2P}}$ between two pulses gained from the time measurement is extrapolated to be present during the whole detected low level duration. Additionally, counter/timer arrangement enables to measure the approximate output frequency f_{pt} of multiple cycles and maintain high resolution over a wide range of inputs. The pulse couting and time sensing method is also decribed as a feed-forward strategy since both parts of this technique are based on predetermined values like the volt quantum ψ_ε or the function represented through the characteristic curve.

3.2.4 Residual Voltage Sensing of AVFCs

Nonetheless, there is a distinct characteristic present in all measurement approaches utilizing VFC: Despite the accurate measurement by VFCs through the charge-balancing procedure, there will always be a discrepancy at the end of each period since residual voltage remains on the integrator capacitor C_{int} of the VFC. Figure 3.12 illustrate this (here maximum) quantization error as the integrator capacitor C_{int} is fully charged by the end of the PWM-period resulting in a pulse at the beginning of the next PWM-period although there is no voltage equivalent to charging a volt quantum u_ε yet. Thus, the residual voltage is equivalent to the quantization error. Another novel developed measuring technique is implemented to sense this residual voltage, thereby compensating the quantization error and increasing the instantaneous voltage. The primary recommendation for voltage sensing lies in the measurement of residual voltage, ensuring no disruption to volt-second-conversion process (equation (3.25)). This approach is thoroughly discussed

Table 3.4: Components of AVFC circuit for residual voltage sensing method

Voltage divider		**Linearity**				**Offset**				**Output**	
R_{vd1}	R_{vd2}	R_{int1}	R_{int2}	$R_{\mathrm{lin,trim}}$	C_{int}	R_{os0}	R_{os1}	R_{os2}	$R_{\mathrm{os,trim}}$	R_{pullup}	C_{os}
52.3 kΩ	7.5 kΩ	120 kΩ	180 kΩ	1 kΩ	50 pF	0 Ω	0 Ω	0 Ω	500 Ω	680 Ω	56 pF

in [56] and will be briefly outlined here.

Initially, the characteristic curve for the AVFC in Fig. 3.10b is adjusted to its original position by removing the offset injection setting R_{os0} equals zero. Three resulting cases during low level PWM are now depicted in Fig. 3.13 by showing an input voltage u_{in} of exactly 0 V (purple trajectories), a slightly negative input voltage $u_{\mathrm{in}-}$ (blueish trajectories), and a slightly positive input voltage $u_{\mathrm{in}+}$ (greenish trajectories). For clarification purposes, the author states that the pulse train $u_{\mathrm{pt}}(f_{\mathrm{pt}})$ is plotted as inverted function and right-aligned PWM is assumed.
First, the residual voltage for an ideal case of an input voltage u_{in} of 0 V is examined. The integrator output voltage u_{Vs} remains steady at a voltage level between 0 V and the reset reference voltage as zero input voltage u_{in} is applied and, thus, no input current i_{in} available that charges the integrator capacitor C_{int}. The voltage level where the plateau is observed corresponds to the residual voltage reflecting the discharge level at the end of PWM-period k without generating an additional output pulse. As stated before, there is consequently an excessive amount of charge on the integrator capacitor C_{int} at the beginning of the next PWM-period $k+1$.

Detecting the residual voltage becomes problematic when the low-level voltage is slightly negative or slightly positive in non-ideal situations. In case of negative low level input voltage $u_{\mathrm{in}-}$, the integrator capacitor C_{int} is charged, which usually only happens during resets when the comparator threshold voltage is surpassed. At positive low level input voltage $u_{\mathrm{in}+}$, the voltage gradient is notably less steep than at higher levels, although periodic pulses are still present. In both nonideal cases, the residual voltage is only detectable for a brief period right after the PWM voltage changes from high to low (cf. Fig. 3.13) rather than the entire duration of the full low level period of the constant voltage level being available. Continuous sampling of the integrator's output voltage u_{Vs} with a 12-bit ADC [103] is therefore essential for identifying residual voltage.
The objective of residual voltage measurement is to acquire the charge level of the integrator capacitor C_{int} through the use of an additional ADC as applied in Fig. 3.14, represented by a voltage measurement at the integrator output voltage u_{Vs}. It ensures an increase in precision by measuring the least significant bit (LSB) of the AVFC with the resolution of an ADC employing only one pulse. An implemented logic holds the sample value of the residual voltage as long as either a rising slope for consecutive sample values for negative low level voltage is true, or a change in a negative integrator output voltage slope is detected for positive low level voltage.

In conclusion, the residual voltage sensing method is a new inclusion in the measure-

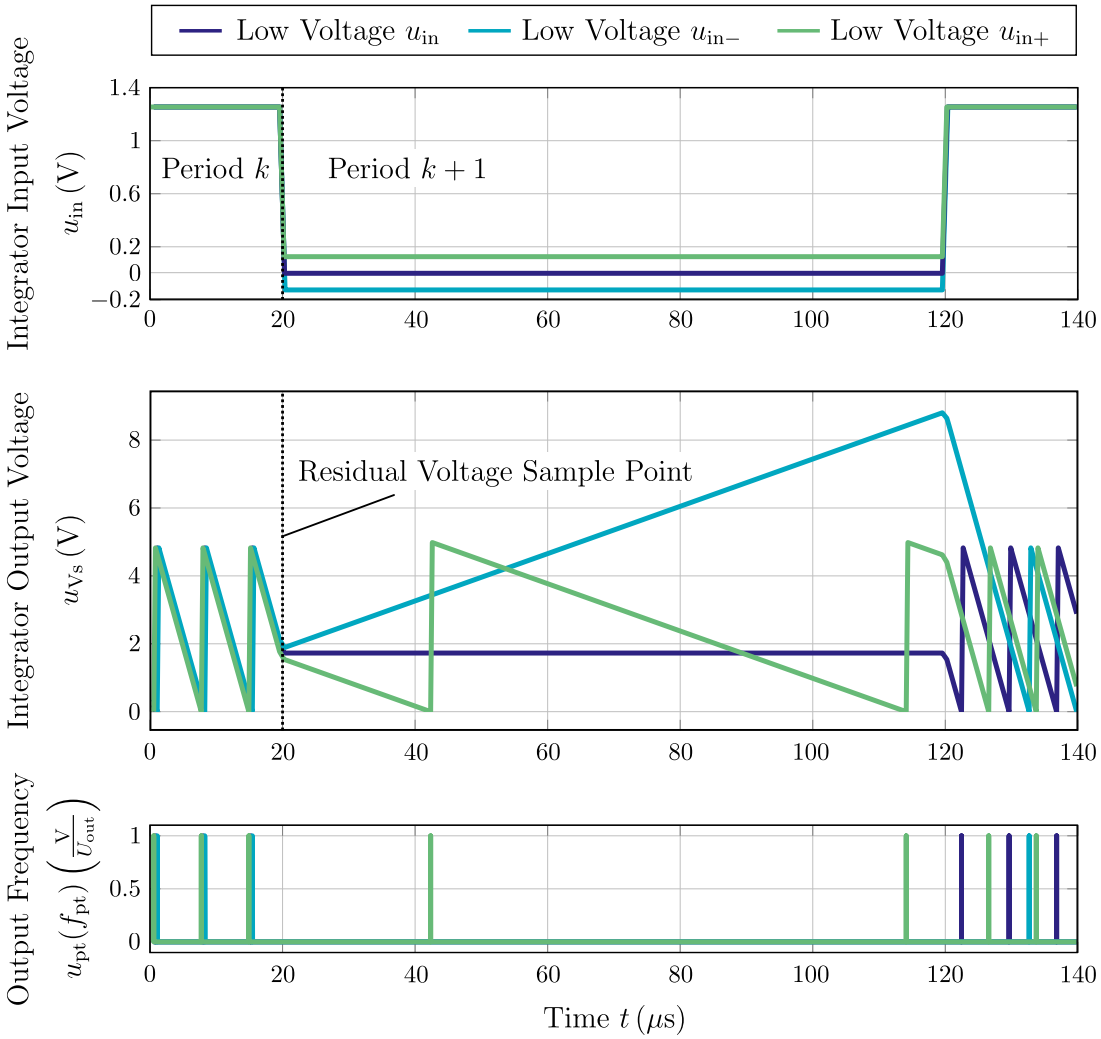


Figure 3.13: Simulated trajectories of residual voltages in AVFC (cf. [56])

ment approaches for AVFCs previously examined. Two residual voltage measurements are utilized to construct digits after the decimal point for the pulse count. Between two high levels of phase voltage u_{ph} in PWM period k and $k+1$, residual voltage always contains information that affect measurement evaluation for both PWM periods. The charge stored in the previous PWM-period k without pulse generation negatively impacts the digits after decimal point of the pulse count, while the charge of the following PWM-period $k+1$ positively impacts the digits as the charge is not sufficient for another output pulse. Consequently, pulse counting extends by including decimal values, determined by the quality of logic operations and the resolution of the utilized ADC.
Table 3.4 shows the parameter set for the residual voltage measurement technique. Increasing the total input resistance is essential to avoid saturation of the AVFC integrator guaranteeing charge-balancing to prevent any loss of charge.

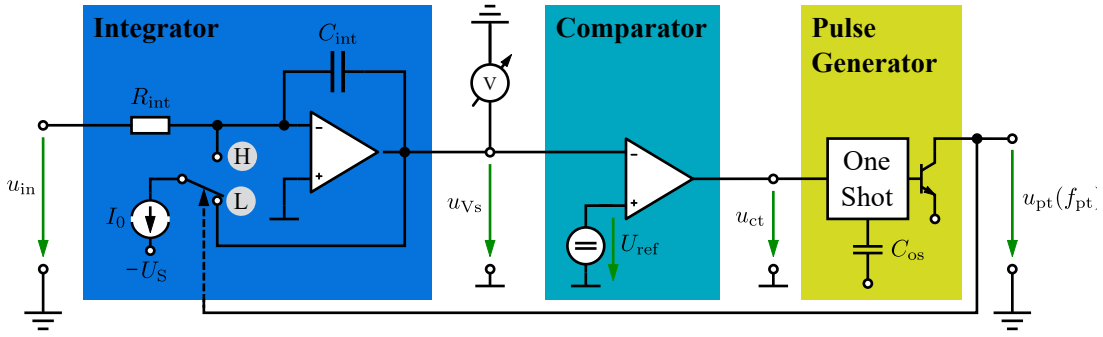


Figure 3.14: Block diagram of AVFC with additional ADC for residual voltage sensing

3.3 Discrete Synchronous Voltage-to-Frequency Converter

The promising results from the literature [8], [74], [77], [78], [81], conducted at WEMPEC and Institute for Power Electronics and Electrical Drives (ISEA), RWTH Aachen University, applying commercial VFCs for precise PWM voltage and volt-second sensing have one common disadvantage: the acquisition costs of VFC ICs (as compared in Section 4.3.3). With the development of a cost-optimized volt-second sensor, the author tackles that issue. At the same time, a comprehensive sensor layout is provided for the purpose of customization to meet each application's requirements for resolution and performance. Basically, the concept of the newly invented dSVFC is based on the working principle of an SVFC like the AD652 [90]. However, the clocked bistable multivibrator and the subsequent one-shot with its bipolar transistor (cf. Fig. 2.12) are substituted by already existing control hardware combining the advantages of analog circuit technology with the performance of an FPGA as depicted in the block diagram in Fig. 3.15. In addition to evaluating the pulses, the FPGA is also responsible for selecting the SPDT switch S_{co} which controls the charging process of the integrator capacitor C_{int}.
The measurement of bipolar voltages, like phase-to-phase voltages, is a necessary requirement of the dSVFC, as indicated by the assessment of the two commercial VFCs in Section 3.2.1. In this way, the dSVFC is expanded with an offset resistor R_{os0} to allow the measurement for negative input voltages through the injection of an additional input current I_{off}. The input voltage range to be measured should be distributed over a frequency range of 5 MHz. It is essential for the dSVFC to possess a bandwidth that allows for the measurement of inverter switching frequencies f_{sw} up to 20 kHz. Additionally, a preceding subtractor is supplemented enabling differential volt-second sensing as differential measurement has the main advantage over single-ended measurement regarding noise rejection.

The first prototype of the dSVFC was already presented in [82] and [83], and also published as a patent in cooperation with Mitsubishi Electric Corporation in [84]. A thorough explanation of the charge-balancing procedure is given, along with an overview of the fundamental method of counting volt-second pulses. Nevertheless, this first prototype is

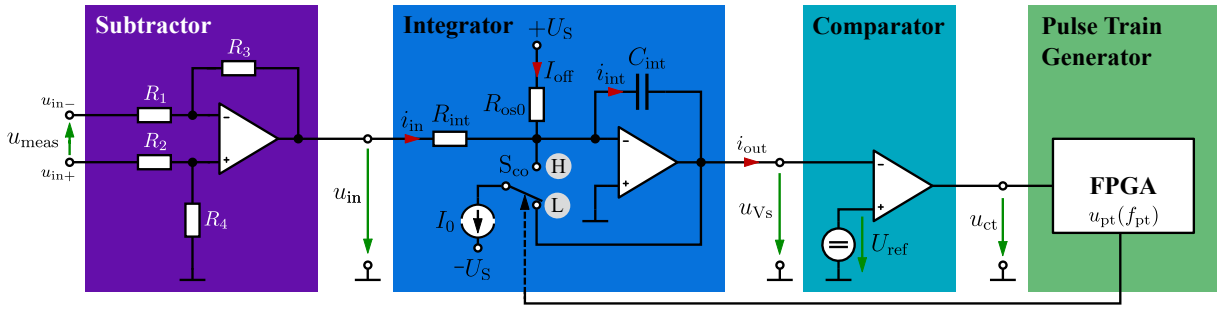


Figure 3.15: Block diagram of discrete synchronous voltage-to-frequency converter

limited to a clock frequency f_{clk} of 100 kHz and, thus, an output frequency f_{pt} of 50 kHz, and the proof of concept is conducted for an emulated switching frequency f_{sw} of only 1 kHz. This disqualifies the first prototype of volt-second sensor for employing on control algorithms for modern electrical drive trains e. g. in battery electric vehicles (BEVs) with switching frequencies greater than 10 kHz. The advancement of the volt-second measurement instrument presented here as dSVFC overcomes this lack of performance and resolution as the evaluation on a test bench with a 100 kW IPMSM powertrain confirms in Chapter 4.4.

3.3.1 Designing the Discrete Synchronous Voltage-to-Frequency Converter

At the heart of every VFC is the charge-balancing concept, which is managed by the integrator and the associated SPDT-switch S_1. The dimensioning of the charge-balancing process is determined by the currents within the dSVFC. The focus in the following will be on the design of each module of the dSVFC: the preceding subtractor, the integrator, and the subsequent comparator (Fig. 3.15). This also adequately fulfills the commitment to provide a comprehensive explanation of the working principle of an SVFC in Section 2.4.2.

First, the subtractor is applied to convert the differential measurement input voltage u_{meas} into a single-ended input voltage u_{in}. The response characteristic of the subtractor (equation (3.28)) is defined by the ratios of the resistors R_1 to R_4, which are chosen R_1 equals R_2 and R_3 equals R_4 resulting in a sufficiently high gain [104], [105]. Through selection of R_1 greater than R_3, the measured input voltage u_{meas} is also scaled down.

$$u_{\mathrm{in}}(u_{\mathrm{meas}}) = \frac{R_3}{R_1} \cdot u_{\mathrm{meas}} \tag{3.28}$$

While the input current i_{in} (equation (3.29a)) is defined through the integrator resistor R_{int} and the varying input voltage u_{in}, the injected offset current I_{off} (equation (3.29b)) is a

variable but fixed quantity dimensioned by the fixed positive supply voltage $+U_\mathrm{s}$ and the offset resistor R_os0.

$$i_\mathrm{in}(u_\mathrm{meas}) = \frac{u_\mathrm{in}(u_\mathrm{meas})}{R_\mathrm{int}} \tag{3.29a}$$

$$I_\mathrm{off} = \frac{+U_\mathrm{s}}{R_\mathrm{os0}} \tag{3.29b}$$

Consequently, equation (2.11) in Section 2.4.2 extends by the additional offset current I_off resulting in equation (3.30).

$$i_\mathrm{int}(u_\mathrm{meas}) = \begin{cases} i_\mathrm{in}(u_\mathrm{meas}) + I_\mathrm{off}, & \text{if } \mathrm{S_{co}} \text{ on L} \\ i_\mathrm{in}(u_\mathrm{meas}) + I_\mathrm{off} - I_0, & \text{if } \mathrm{S_{co}} \text{ on H} \end{cases} \tag{3.30}$$

Regardless of the SPDT-switch position $\mathrm{S_{co}}$, the output current i_out of the integrator circuit results in equation (3.31), which is why a constant load is present for the operational amplifier (OpAmp).

$$i_\mathrm{out}(u_\mathrm{meas}) = I_0 - I_\mathrm{off} - i_\mathrm{int}(u_\mathrm{meas}) \tag{3.31}$$

Once the dependencies of the currents within the dSVFC have been outlined, the next step is to determine suitable ranges for the related currents. The equivalent circuits of both switching states L and H in Fig. 3.16 are involved for this analysis. To ensure that the integrator's output voltage u_Vs oscillates around the the reference voltage U_ref, the discharge current $i_\mathrm{int,H}$ (Fig. 3.16a) of the constant current source I_0 must exceed the charging current i_in by a factor of two. If the input voltage u_in inceases to a level when the charging current $i_\mathrm{int,L}$ is exactly half of the constant current source I_0, the pulse train will be generated at an output frequency f_pt of halve of the clock frequency f_clk.

The constant offset current I_off is injected to the input current i_in ensuring an integrator current i_int that is always greater equal 0 A if a negative input voltage u_in is applied, while the SPDT-switch $\mathrm{S_{co}}$ is in position L. Accordingly, the offset current I_off is selected by the maximum input voltage u_in as follows in equation (3.32).

$$|I_\mathrm{off}| = \frac{|u_\mathrm{in}(u_\mathrm{meas})\,|_\mathrm{max}}{R_\mathrm{int}} \tag{3.32}$$

Determining the constant current I_0 of the precise current sourve requires calculating the chrage balance of both switches states H and L, i. e. the amount of charge during charging

(a) Equivalent circuit with S_{co} switching state L

(b) Equivalent circuit with S_{co} switching state H

Figure 3.16: Equivalent circuits of S_{co} switching states H and L of the dSVFC

process of the integrator capacitor C_{int} equals the amount of charge during discharging, while the SPDT-switch S_{co} is in position H. With the internal clock frequency f_{clk} of the FPGA as a reference, the switching state H is maintained for one clock period T_{clk}, while the switching state L can endure multiple clock periods n (equation (3.33)).

$$\left| \frac{i_{\text{int,L}} \cdot n \cdot T_{\text{clk}}}{C_{\text{int}}} \right| = \left| \frac{i_{\text{int,H}} \cdot T_{\text{clk}}}{C_{\text{int}}} \right| \tag{3.33}$$

Through the current equation (3.30), it is now viable to ascertain a specific factor n according to equation (3.34).

$$n = \left| 1 - \frac{I_0}{i_{\text{int}}(u_{\text{meas}}) + I_{\text{off}}} \right| \tag{3.34}$$

Consequently, this factor n serves as a requirement for the constant current value I_0 in equation (3.35). Interpretation of these equations will be clarified in Section 3.3.3 through simulations results.

$$I_0 \geq 2 \cdot \left(i_{\text{int}}(u_{\text{meas}}) + I_{\text{off}} \right), \text{ for } n \geq 1 \tag{3.35}$$

The component values for the designed dSVFC are listed in Table 3.5. Selection of resistors R_1 and R_3 results in a 1:12 ratio for the voltage divider of the voltage u_{meas} to be measured. This permits the detection of the dc-link voltage U_{dc} of $\pm 60\,\text{V}$ delivered by the test bench to the SEMIKRON trench IGBT module SKM 600GB066D [97]. This results in an input voltage u_{in} of the integrator of $\pm 5\,\text{V}$. The current values in Table 3.6 are derived from the definition of the components in Table 3.5.

Table 3.5: Components of dSVFC sensor

Subtractor		Integrator					Comparator
$R_1 = R_2$	$R_3 = R_4$	R_{int}	R_{os0}	C_{int}	$+U_{\text{s}}$	$-U_{\text{s}}$	U_{ref}
240 kΩ	20 kΩ	5 kΩ	5.5 kΩ	1 nF	5.5 V	−2.5 V	3.3 V

Table 3.6: Currents of dSVFC sensor

Constant Currents		Current Boundaries	
I_0	I_{off}	i_{in}	i_{int}
4 mA	1 mA	−1 mA...1 mA	−4 mA...6 mA

3.3.2 Characteristic Curve and Volt-Second Quantum

Following the circuit synthesis, the equation for the measured averaged volt-second over one PWM period $\bar{\psi}_{\text{pwm}}$ is determined by referring to the general characteristic curve of the dSVFC in Fig. 3.17.

This is also demonstrated in a comparable way in [83]. Throughout the process of deriving the instantaneous flux-linkage $\bar{\psi}_{\text{pwm}}$ in dependence of the output pulses N, various interpretations for the volt-second quantum ψ_ε are elucidated. The general characteristic curve of the dSVFC is described as already presented for the SVFC and AVFC in Section 3.2.1. The frequency of the output pulse train f_{pt} is linear proportional to the measured input voltage u_{meas} as illustrated in Fig. 3.17 and described mathematically in equation (3.36).

$$f_{\text{pt}}\left(u_{\text{meas}}\right) = \frac{f_{\text{pt}}|_{U_{\text{meas,max}}}}{U_{\text{meas,max}} - U_{\text{meas,min}}} \cdot u_{\text{meas}} + f_{\text{pt}}|_{u_{\text{meas}}=0\,\text{V}} \tag{3.36}$$

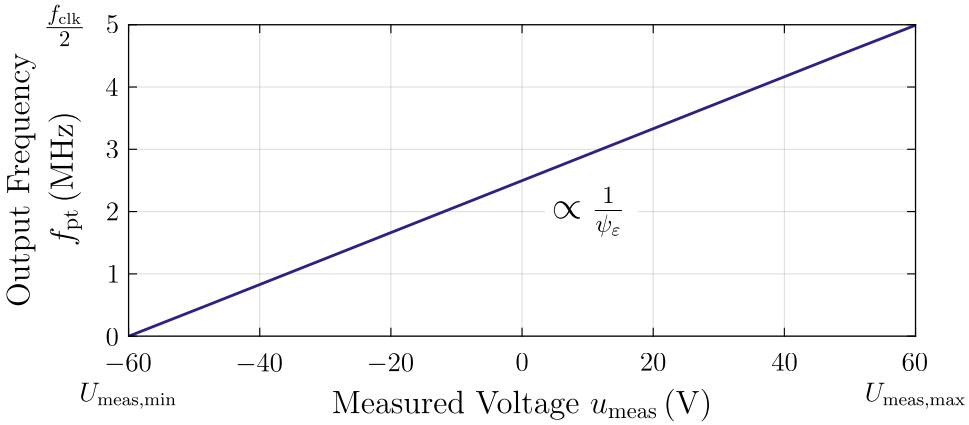


Figure 3.17: Characteristic curve design $f_{\text{pt}}(u_{\text{meas}})$ for dSVFC

The equation is reformulated to rely solely on the provided clock frequency f_{clk} and the defined minimum and maximum measured voltages $U_{\mathrm{meas,min}}$ and $U_{\mathrm{meas,max}}$. The maximum output frequency f_{pt} at maximum measured input voltage $U_{\mathrm{meas,max}}$ equals half of the FPGA's clock frequency f_{clk}, and the offset frequency of the characteristic curve at an input voltage of 0 V is determined utilizing the point-slope form. Therefore, two OPs are defined: The first is an output frequency f_{pt} of 0 kHz at the minimum measured voltage $U_{\mathrm{meas,min}}$, and the second is the maximum output frequency f_{pt} equals $1/2 f_{\mathrm{clk}}$ at an maximum measured voltage $U_{\mathrm{meas,max}}$. Consequently, the offset frequency of the characteristic curve results in equation (3.37).

$$f_{\mathrm{pt}}|_{u_{\mathrm{meas}}=0\,\mathrm{V}} = \frac{\frac{1}{2}\cdot f_{\mathrm{clk}}}{1+\frac{U_{\mathrm{meas,max}}}{U_{\mathrm{meas,min}}}} \tag{3.37}$$

As a result, the overall equation for the characteristic curve of a dSVFC is established with the variable but fixed parameter set of clock frequency f_{clk}, and the measured input voltage range from $U_{\mathrm{meas,min}}$ to $U_{\mathrm{meas,max}}$ for a specific application (equation (3.38)).

$$f_{\mathrm{pt}}\left(u_{\mathrm{meas}}\right) = \frac{\frac{1}{2}\cdot f_{\mathrm{clk}}}{U_{\mathrm{meas,min}}+U_{\mathrm{meas,max}}}\cdot\left(u_{\mathrm{meas}}+U_{\mathrm{meas,min}}\right), \quad U_{\mathrm{meas,min}}>0 \tag{3.38}$$

The inverse function in equation (3.39) now enables the determination of the input quantity of measured voltage u_{meas} depending on the output quantity of frequency f_{pt} of the sensor.

$$u_{\mathrm{meas}}\left(f_{\mathrm{pt}}\right) = \frac{U_{\mathrm{meas,max}}+U_{\mathrm{meas,min}}}{\frac{1}{2}\cdot f_{\mathrm{clk}}}\cdot f_{\mathrm{pt}} - \frac{U_{\mathrm{meas,max}}+U_{\mathrm{meas,min}}}{1+\frac{U_{\mathrm{meas,max}}}{U_{\mathrm{meas,min}}}} \tag{3.39}$$

The slope of this inverse function equation (3.39) equals the ratio of the entire measured input voltage range and the entire output range of frequency. Thus, the slope of the inverse function corresponds to the volt-second resolution ψ_ε of the sensor that is defined in equation (3.40). This is the also reasoning behind the defintion of the volt-second quantum in equation (3.24).

$$\psi_\varepsilon := \frac{U_{\mathrm{meas,max}}+U_{\mathrm{meas,min}}}{\frac{1}{2}\cdot f_{\mathrm{clk}}} \tag{3.40}$$

The volt-second quantum ψ_ε represents the proportionality factor between the measured input voltage u_{meas} and the output frequency f_{pt} and is therefore a constant value.

Nevertheless, this condition is only valid when a constant input voltage u_{meas} is applied. When measuring a dynamic input voltage like the PWM voltage of a VSI, it is necessary to measure various voltage levels and voltage transients as well. Hence, the assumption of a consistent output frequency f_{pt} is no longer tenable. Instead, it is possible to accumulate the quantity of pulses N per PWM period allowing for the determination of the instantaneous volt-second value $\bar{\psi}_{\mathrm{pwm}}$. The number of pulses N per PWM period results from the ratio of the output frequency f_{pt} and the switching frequency f_{sw} of the VSI in equation (3.41).

$$N = \frac{f_{\mathrm{pt}}}{f_{\mathrm{sw}}} \tag{3.41}$$

By counting pulses, the output frequency f_{pt} of a constant input voltage is reassigned from equation (3.39) to a dynamic input voltage within a specific time interval of in this case ${f_{\mathrm{sw}}}^{-1}$. Accordingly, equation (3.42) presents the general function of the instantaneous PWM voltage $\bar{u}_{\mathrm{pwm}}$.

$$\bar{u}_{\mathrm{pwm}}(N) = \psi_{\varepsilon} \cdot f_{\mathrm{sw}} \cdot N - \frac{U_{\mathrm{meas,max}} + U_{\mathrm{meas,min}}}{1 + \frac{U_{\mathrm{meas,max}}}{U_{\mathrm{meas,min}}}} \tag{3.42}$$

The voltage resolution u_{ε} varies with the switching frequency f_{sw} (cf. equation (3.25)), highlighting the absence of a fixed value like the volt-second quantum ψ_{ε} (equation (3.40)). Hence, increasing measurement accuracy is associated with larger time intervals T_{pwm} or lower switching frequencies f_{sw}, respectively, indicating a compromise between accuracy and speed.
The calculation of the instantaneous flux-linkage $\bar{\psi}_{\mathrm{pwm}}$ is finalized by scaling the PWM voltage $\bar{u}_{\mathrm{pwm}}$ with the VSI switching frequency f_{sw} resulting in equation (3.43). The result shows that the resolution and, thus, the gain of the function $\bar{\psi}_{\mathrm{pwm}}$ is independent of the switching frequency f_{sw}. In contrast to the determination of measured voltage $\bar{u}_{\mathrm{pwm}}$, where the gain varies with the switching frequency f_{sw}, in this case the offset shifts, resulting in undetectable volt-second below the defined resolution ψ_{ε}, which does not affect the resolution at all.

$$\bar{\psi}_{\mathrm{pwm}}(N) = \psi_{\varepsilon} \cdot N - \frac{U_{\mathrm{meas,max}} + U_{\mathrm{meas,min}}}{1 + \frac{U_{\mathrm{meas,max}}}{U_{\mathrm{meas,min}}}} \cdot \frac{1}{f_{\mathrm{sw}}} \tag{3.43}$$

In conclusion, the averaged volt-second $\bar{\psi}_{\mathrm{pwm}}$ over one PWM period is defined through the accumulation of the number of pulses N per PWM period weighted with the volt-second quantum ψ_{ε}. The negative offset derived demonstrates the feasibility of measuring negative volt-seconds. An extensive examination will be conducted based on the specified sensor requirements and the equations that have been formulated within this section.

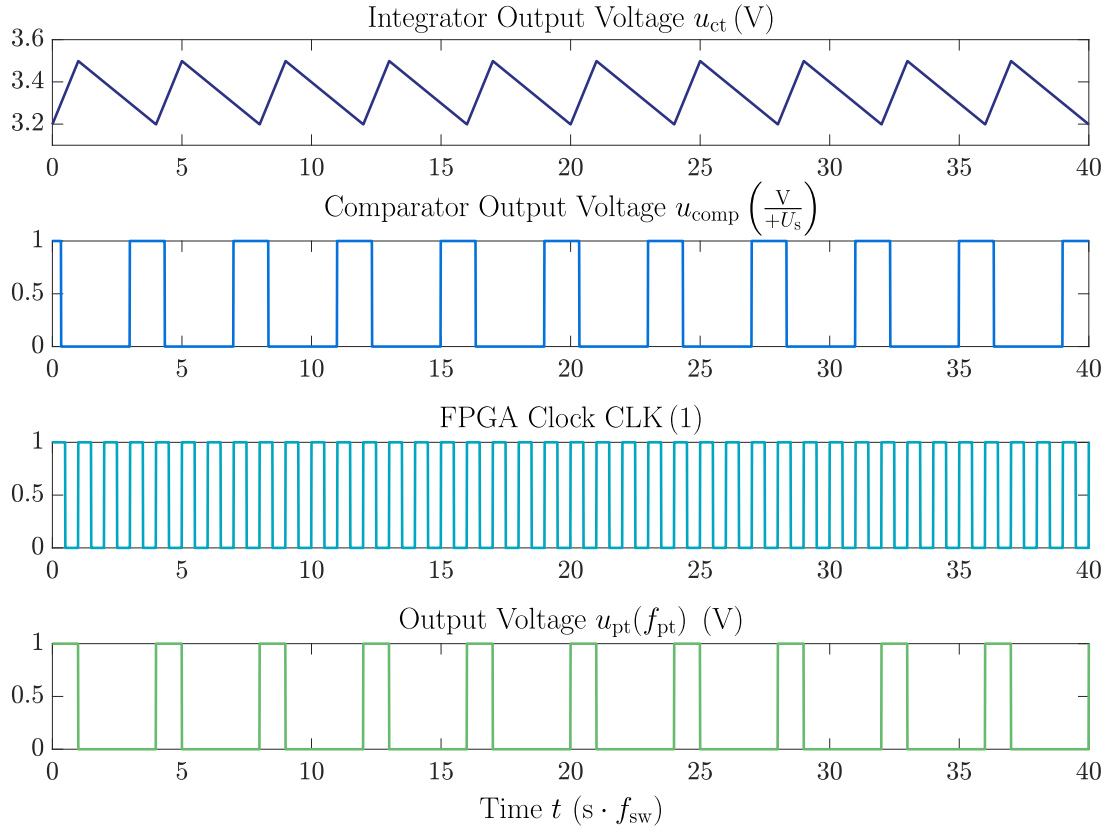


Figure 3.18: Simulation results for voltage trajectories of dSVFC for $u_{meas} = 0\,V$

3.3.3 dSVFC Simulation and Analysis

The working principle of the proposed volt-second sensor topology is validated with the simulation software PLECS. Figure A.5 shows the simulation model with the component values listed in Table 3.5 and the electrical quantities defined in the previous section. The FPGA source code is implemented as the clocked bistable multivibrator of the AD652 [90] since the FPGA code will be introduced in the next Section 3.3.4. As a demonstration, the results from two different measured input voltages u_{meas} are exhibited here to interpret the ratio n representing the ration of charge and discharge time of the integrator capacitor C_{int} in equation (3.34).
First, a measured input voltage u_{meas} of 0 V is applied whose simulation results are depicted in Fig. 3.18. An output frequency f_{pt} of 2.5 MHz occurs as expected since the input current i_{in} is 0 A and integrator capacitor C_{int} is only charged by the offset current I_{off}. In this case, the relation of the currents in equation (3.34) equals the integer 3, i. e. the charging duration is three times the discharging time of the integrator capacitor C_{int}. It follows that the output frequency f_{pt} is constant as the pulses are generated in time equidistant intervals.

If the current ratio in equation (3.34) results in a non-integer, then the integrator output voltage u_{Vs} shows irregular patterns in its macroscopic behavior due to the uneven

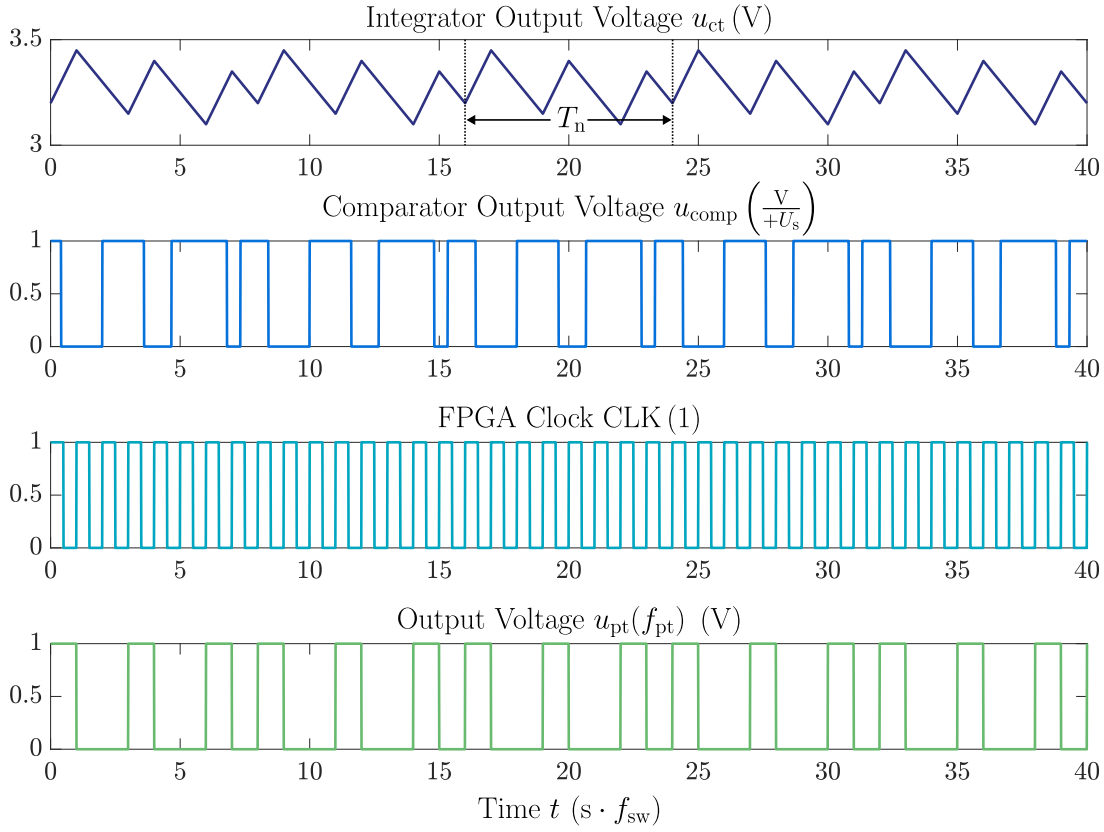


Figure 3.19: Simulation results for voltage trajectories of dSVFC for $u_{meas} = 30\,V$

distribution of output pulses. In case of a measured input voltage u_{meas} of 30 V, the multiple n is equal to $5/3$ resulting in deviation of charging and discharging time (Fig. 3.19). However, it is necessary for the charging intervals to be in multiples of the FPGA's clock period T_{clk}. As a result, there are two consecutive discharge events that occur at regular intervals followed by another discharge every two cycle periods. This pulse sequence can be associated with a specific period T_n. Averaging over the period duration T_n results in both the expected ratio of $5/3$ of the charging and discharging time and the calculated output frequency f_{pt} of 3.75 MHz. It should be noted that the rate of charging and discharging is influenced by the measured input voltage u_{meas} and the input current i_{in}, respectively (cf. equation (2.11)). The dependencies are outlined in equation (3.44). The greater the measured input voltage u_{meas}, the flatter the discharge curve and the steeper the charge curve – and vice versa.

$$u_{meas} \uparrow \Rightarrow \begin{cases} \left|\frac{du_{Vs}}{dt}\right| \uparrow, \text{ charging:} & S_{co} \text{ on L} \\ \left|\frac{du_{Vs}}{dt}\right| \downarrow, \text{ discharging:} & S_{co} \text{ on H} \end{cases} \tag{3.44}$$

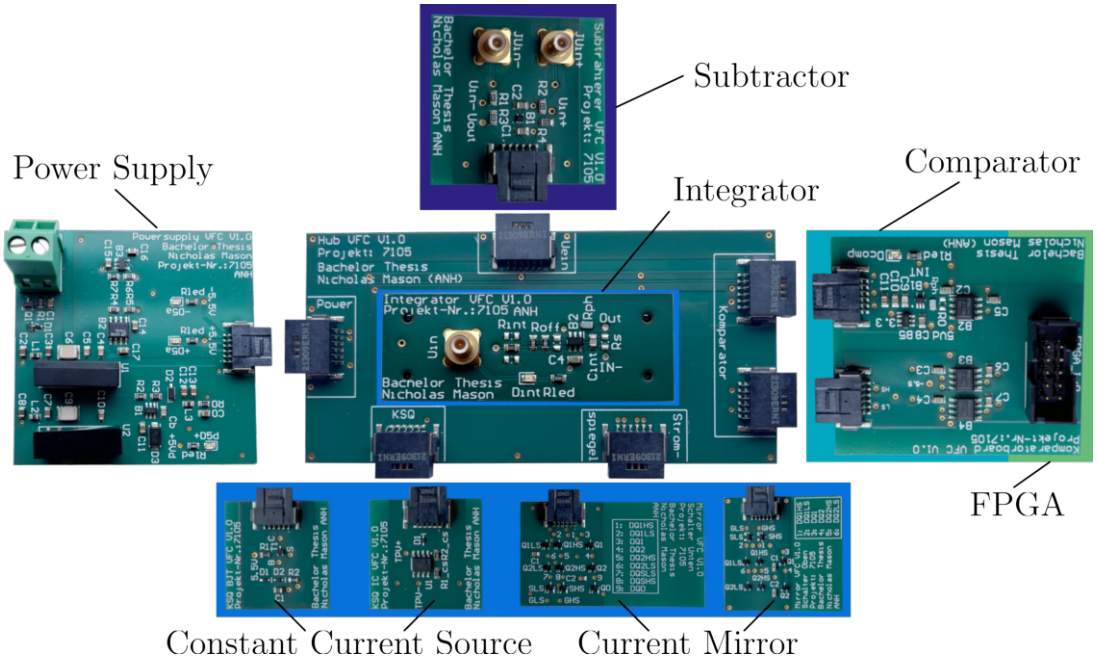


Figure 3.20: Printed circuit board of modular dSVFC

3.3.4 Modular Sensor Hardware Concept

The proof of concept of the hard- and software implementation is already introduced in [82] and [83]. The second dSVFC prototype presented in this section faces new requirements as stipulated at the beginning of Section 3.3. This time, the second prototype is designed with a modular approach as shown in Fig. 3.20. The center board is built by a PCB hub that connects all surrounded satellite PCBs realizing the different elements of the dSVFC. The benefits consist of the ability to commission and optimize independently and replace individual components with ease. The depiction in Fig. A.6 showcases the modular design concept and provides an overview of utilized electrical signal exchange between the hub and the satellite boards. Each satellite with its component of the dSVFC is described in the following. Additional information is available in [106] for a more thorough explanation.

The power supply PCB on the left ensures that all modules receive the appropriate voltage level (see also Table 3.7). It operates on a 24 V power source U_{sup} and converts it to 5.5 V and −2.5 V through a dc-dc converter and two Linear- and Low-Dropout-Controllers (LDOs) providing the analog parts of the sensor. The digital components of the sensor receive power from a 5 V supply converted by an additional isolated dc-dc converter and LDO. The analog and digital reference potentials are solely linked at the dc-dc converter, while being galvanically and physically isolated otherwise. The input of the power supply PCB is protected against reverse polarity.

The differential measured input voltage u_{meas} is connected via Mini-Bayonet Neill-Concelman (BNC) connectors to the subtractor, stepped down with the ratio 1:12, and

Table 3.7: Voltage levels of modular dSVFC sensor

U_{sup}	$+U_{\mathrm{s}}$	$-U_{\mathrm{s}}$	$U_{\mathrm{s,dig}}$	U_{ref}
24 V	5.5 V	−2.5 V	5 V	3.3 V

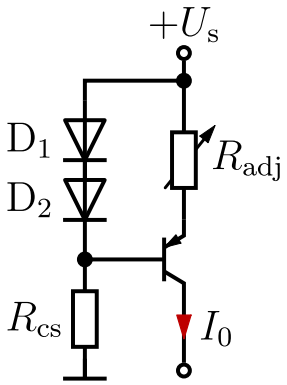
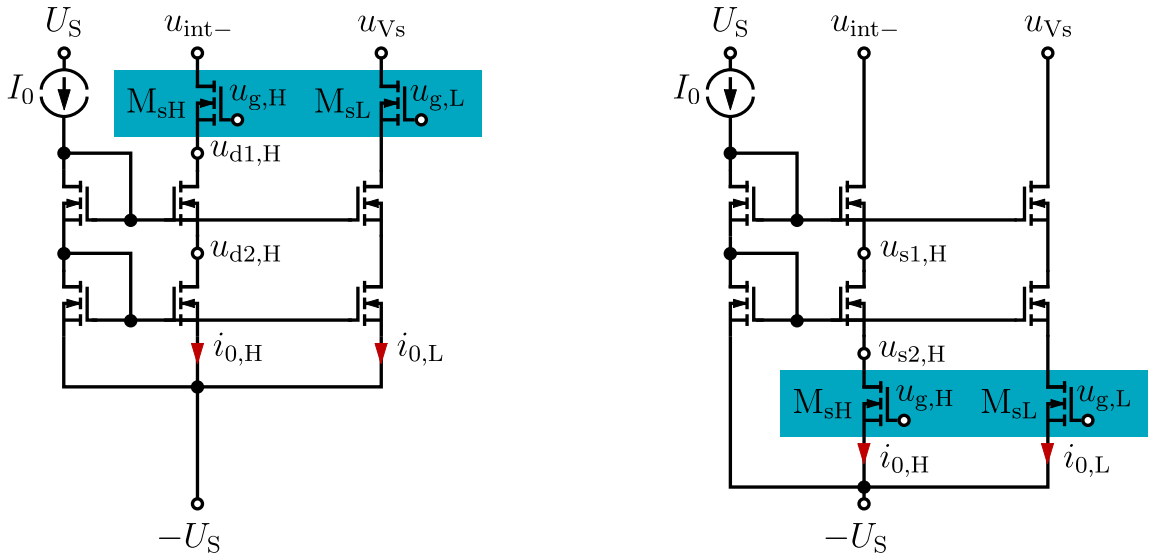


Figure 3.21: Discrete constant current source of dSVFC

converted into a single-ended signal. Several placeholders are provided to enable calibration of the integrator circuit; One located at the integrator resistor R_{int}, and another positioned at the offset resistor R_{os0}. One more placeholder is situated in parallel to the integrator capacitor C_{int} allowing for modification of the integrator's frequency response. As suggested in [86], a Teflon capacitor is employed to reduce dielectric absorption. In addition to handling the integrator output voltage u_{Vs}, the comparator satellite interfaces with the RCP system and the FPGA, respectively. Three digital isolators are in place to secure the RCP system inputs and outputs.

Two variations are available for both the constant current source and the current mirror, which implement the SPDT-switch $\mathrm{S_{co}}$, to examine their transient behavior in detail. The combination of both modules serves to discharge the integrator capacitor C_{int}. A comparison is made between the performance of the Texas Instruments LM334 IC [107] and a well-known discrete current source topology for the variable constant current source I_0 (Fig. 3.21). Due to its simplicity in adjusting current levels and lower price, the discrete current source is preferred over the commercial IC, as they both reliably deliver a constant current of 4 mA.

The evaluation and verification of the current mirror pose a greater challenge than the analysis of the constant current source. Since the current mirror functions as SPDT switch $\mathrm{S_{co}}$, three paths must be implemented as current mirror bank. The biasing-path corresponds to adjusting the OP with the reference current I_0 delivered by the constant current source, and to control the gate voltage of current mirror metal-oxide semiconductor field-effect transistors (MOSFETs). The constant current I_0 must be switched alternately between the negative input H and the output L of the integrator circuit to operate the sensor (cf. Fig. 3.15). The switching MOSFETs $\mathrm{M_{sH}}$ and $\mathrm{M_{sL}}$ activate and deactivate the two paths.



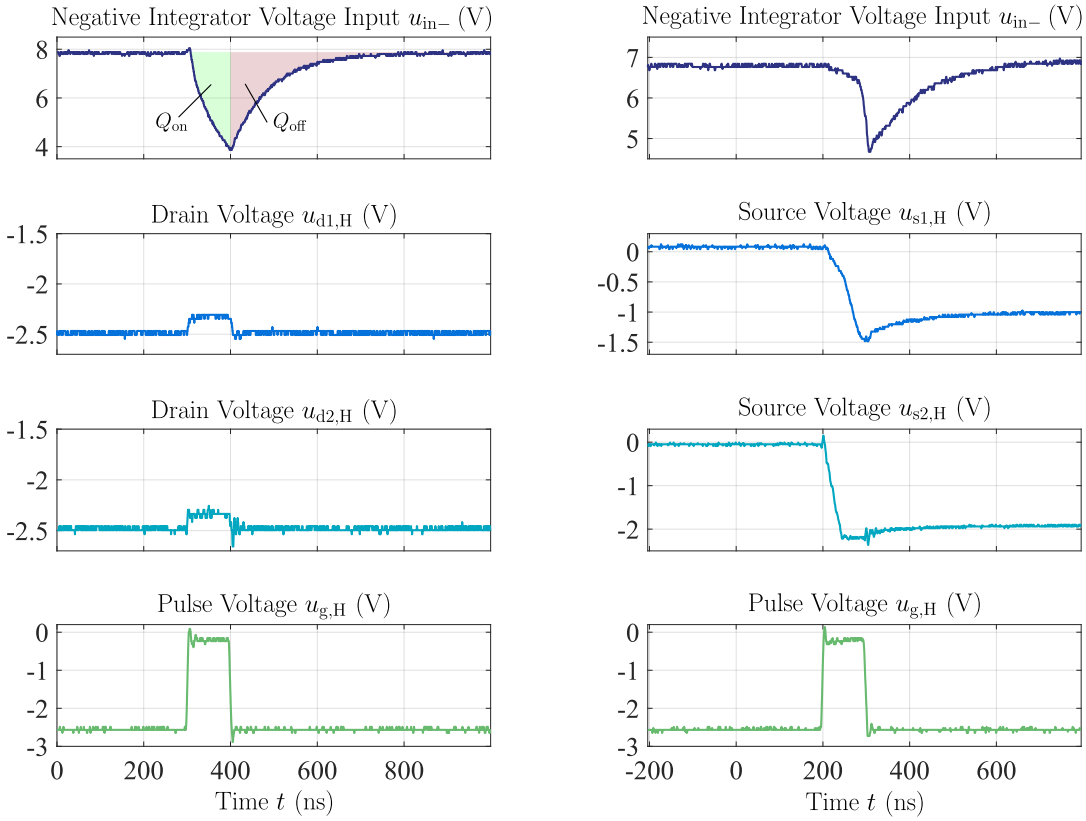
(a) Current mirror with switching MOSFETs above

(b) Current mirror with switching MOSFETs below

Figure 3.22: Current mirror with MOSFETs realizing the SPDT switch S_{co}

Figure 3.22 shows two various topologies realizing the current mirror bank. Figure 3.22a depicts the implementation with the switching MOSFETs M_{sH} and M_{sL} above the current mirror (highlighted in blue), while Fig. 3.22b illustrates them below the current mirror. Maintaining a negative potential $-U_s$ is essential due to the integrator circuit's negative input potential u_{int-} being set at 0 V. Therefore, the gate voltages applied to M_{sH} and M_{sL} are configured at 0 V and the negative potential $-U_s$, respectively, while generating pulses, and conversely in the alternate case. Investigation into the transient response of the current mirror paths is necessary as it result of the high-frequency switching events. To accomplish this goal, the generation of one pulse is examined. Besides the integrator input voltage u_{int-} that equals the current trajectory of $i_{0,H}$ due to an applied shunt measurement, the voltage performance of the MOSFETs is also under investigation. The examination of drain voltages $u_{d1,H}$ and $u_{d2,H}$ is conducted when the switching MOSFETs are placed above the current mirror, while the examination of source voltages $u_{s1,H}$ and $u_{s2,H}$ is conducted at the other case. Since the current $i_{0,L}$ in path L does not impact the output voltage behavior u_{Vs} of the integrator, the subsequent analyses focus solely on the current $i_{0,H}$ of the high side.

Figure 3.23 depicted the measurement results in path H related to GND of both current mirror variants. First, the trajectories of the current mirror with the switching MOSFETs above are considered in Fig. 3.23a. The high side path has both MOSFETs open before a pulse is activated, resulting in the drain voltages $u_{d1,H}$ and $u_{d2,H}$ being equivalent to the negative supply voltage $-U_s$. Consequently, the current $i_{0,H}$ is blocked causing an 8 V drop at the shunt resistor measuring the inverted integrator input u_{int-}. If a pulse is now triggered through switching MOSFET M_{sH} on, the drain voltages $u_{d1,H}$ and $u_{d2,H}$ of both



(a) Current mirror with switching MOSFETs above

(b) Current mirror with switching MOSFETs below

Figure 3.23: Measured voltage and current trajectories of current mirror

MOSFETs in the high path rises up to a constant voltage level of 15 mV. This marks the beginning of current conduction of $i_{0,\text{H}}$ with a simultaneous voltage decreasing of $u_{\text{int}-}$ as the MOSFETs are turned on. For the integrator to generate a linear output voltage curve u_{Vs}, it is crucial to maintain a constant current value of $i_{0,\text{H}}$, despite the observable time lag effect. This indicates a lack of speed of the switching behavior of the MOSFETs for the required pulse duration T_{pls}. Nonetheless, the accurate operation of the measuring circuit is sustained as long as the charge balance in equation (3.45) is secured during pulse generation.

$$Q_{\text{on}} = \int_{\tilde{t}=t_0}^{T_{\text{pls}}} \frac{u_{\text{int}-}}{R_{\text{shunt}}}\,\mathrm{d}t = \int_{\tilde{t}=T_{\text{pls}}}^{\Delta t_{\text{P2P}}} \frac{u_{\text{Vs}}}{R_{\text{shunt}}}\,\mathrm{d}t = Q_{\text{off}} = \text{const.} \tag{3.45}$$

In addition, the amount of charge Q_{on} must be large enough so that the integrator capacitor C_{int} is sufficiently discharged during the duration T_{pls} of the pulse.

Next, the trajectories of the current mirror with the switching MOSFETs below are considered in Fig. 3.23b. This topology is considered unsuitable as outlined below. The

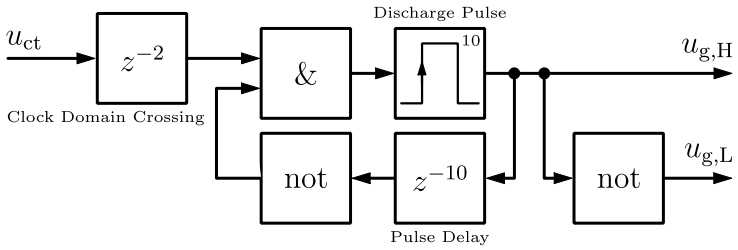


Figure 3.24: FPGA source code for control of current mirror of dSVFC

source voltages $u_{s1,H}$ and $u_{s2,H}$ are undefined voltage levels when not in the pulse duration. Hence, the conduction of the current $i_{0,H}$ is significantly delayed as the MOSFETs require time to become operational after MOSFET M_{sH} is activated. The current $i_{0,H}$ initiates once the pulse duration has already ended. The negative impact on integration behavior caused by the delay in discharge results in the exclusion of the topology with the switching MOSFETs below the current mirror for the subsequent phases of the study. Accordingly, the current mirror with the switches above as depicted in Fig. 3.22a is applied for the dSVFC.

Following the introduction of the hub and its satellites, the FPGA source code utilized for pulse counting and current mirror controlling is presented. As stated in the introduction of Section 3.3, the dSVFC applys already available control hardware by replacing the clocked bistable multivibrator of a commercial SVFC IC with FPGA source code that is illustrated in Fig. 3.24. Thus, the FPGA receives the comparator's output voltage u_{ct} and sets the gate signals $u_{g,H}$ and $u_{g,L}$ of the MOSFETs M_{sH} and M_{sL}, which are emulating the SPDT switch S_{co}. First, a delay of two clock cycles is present in the code to stabilize the read signal u_{ct}. If the AND gate produces a true output, a pulse with the duration of T_{pls} that equals 100 ns is generated. To prevent another pulse from happening within the next 100 ns after the initial pulse, it is sent and inverted to the AND gate during this time period. After the selection of each component within the modular dSVFC has been evaluated, the second prototype sensor is validated on the test bench in the next section.

3.3.5 Validation of Modular dSVFC Measurement Board

The real time (RT)-system of choice for the laboratory set-up is the MicroLabBox DS1202 provided by dSPACE GmbH [108]. It involves a Xilinx Kintex-7 FPGA with a clock frequency f_{clk} of 100 MHz, which evaluates the number of pulses N and, thus, the determination of the instantaneous volt-second value $\bar{\psi}_{pwm}$. Despite this, the MicroLabBox is incapable of controlling the SPDT switch S_{co} of the dSVFC due to a 120 ns output signal delay, which is too slow to guarantee a consistent pulse pattern for the discharging process of the integrator capacitor C_{int}. Therefore, an FPGA from Xilinx's Spartan 7 series [109] is employed to control the current mirror. The introduced FPGA source code

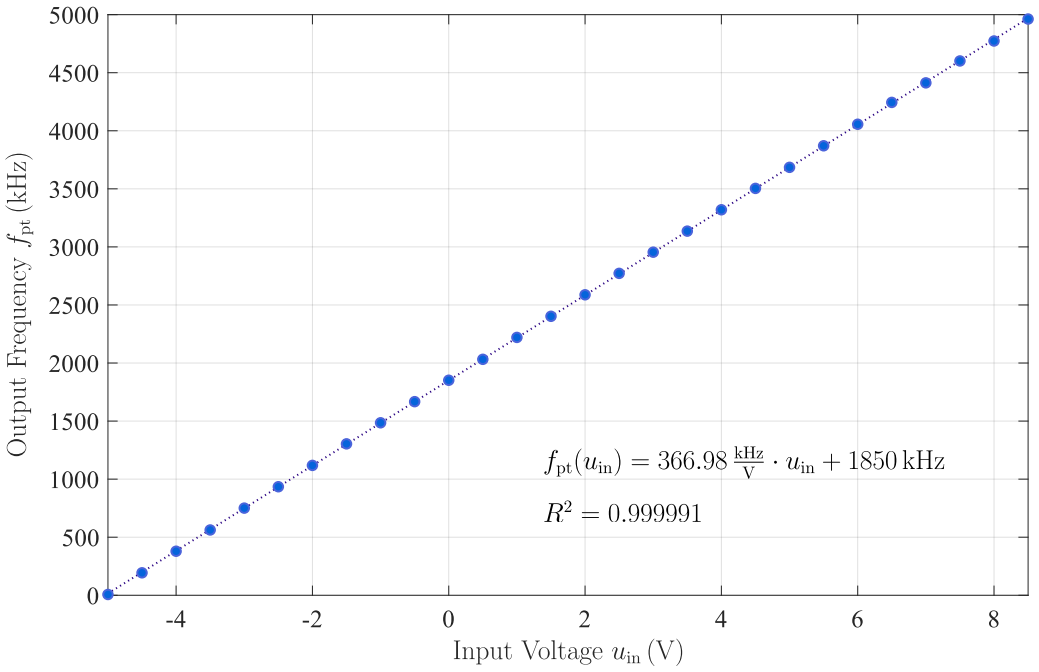


Figure 3.25: Measured characteristic curve of modular dSVFC

in Fig. 3.24 is implemented in very high-speed integrated circuit hardware description language (VHDL).
The initial step consists of determining the volt-second sensor's characteristic curve with the integrator input voltage u_{in} as input quantity and the frequency f_{pt} of the pulse train as output quantity. The characteristic curve then corresponds to that of commercial VFC ICs. The dynamic behavior with varying input voltage levels is examined with the third prototype – the integrated dSVFC – in the following Section 3.3.6. Subsequently, a more detailed examination is carried out on the voltage trajectories and they are compared with those of the commercial SVFC AD652.

The characteristic curve is established within the −5 V to 5 V integrator input voltage interval (corresponding to a measuring range of ±60 V with a divider ratio of 1:12), with increments of 0.5 V, mapped to the output frequency range from 0 Hz to 5 MHz. The measured OPs are presented in Fig. 3.25 along with the linear regression line for analysis. With a coefficient of determination R^2 approaching one, the dSVFC demonstrates a linear behavior in its operation. However, it is noticeable that the highest output frequency f_{pt} of 5 MHz is not achieved at an integrator input voltage u_{in} of 5 V, but rather at 8.5 V. According to equation (3.40), this results in a deviation of 1 % in volt-second resolution ψ_{ε} due to the larger input voltage range.

The sensor's modular adaptation alternatives to optimize the volt-second resolution are now demonstrated by utilizing this mismatch in the input-output ratio. In order to meet the design objective that is outline in Fig. 3.17, the volt-second resolution ψ_{ε} must be minimized, which increases the sensor's gain. Increasing the charging current $i_{\mathrm{int,L}}$ or

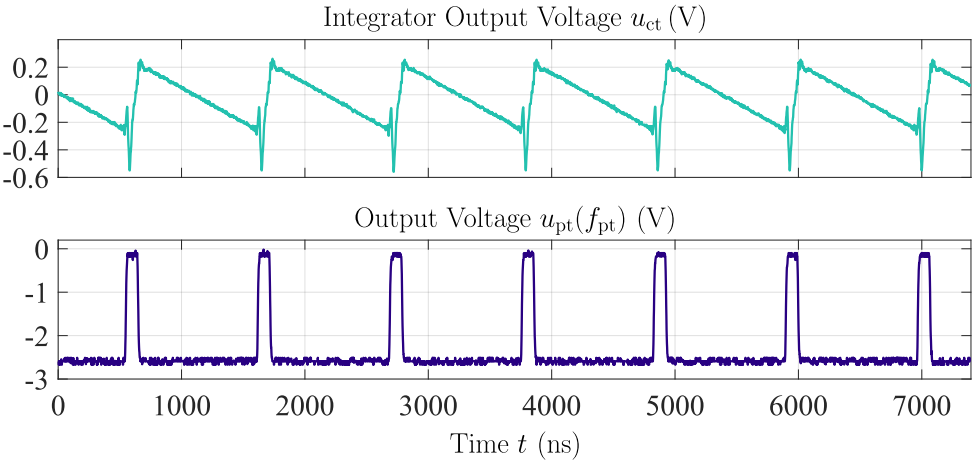


Figure 3.26: Measured integrator output voltage u_{Vs} and pulse train $u_{pt}(f_{pt})$ at $u_{in} = -2.5\,V$

reducing the discharging current $i_{int,H}$ (Fig. 3.16) accomplishes this requirement. When increasing the charging current $i_{int,L}$ through downsizing of the integrator resistor R_{int}, it must be ensured that the offset current is also adapted correcting the offset output of the sensor. When the charging current $i_{int,L}$ is increased by reducing the integrator resistor R_{int}, the offset current I_{off} needs to be correct adjusting the sensor's output offset. It should be emphasized that a drastic reduction in the discharge current $i_{int,H}$ diminishes the voltage oscillation of the integrator output voltage u_{Vs} causing the switching transients in the output voltage to become larger relative to the ac voltage component. This occurrence is observable in the trajectories of the integrator output voltage u_{Vs} in Fig. 3.26 and Fig. 3.27. In this situation, there is no guarantee of a continuous setting for the number of pulses N. Furthermore, the integrator output voltage u_{Vs} should not exceed the voltage supply U_{sup} to prevent saturation and the consequent loss of pulses.

The trajectories presented in the following are measurements in OPs taken from the characteristic curve in Fig. 3.25. Figure 3.26 depicts the measured integrator output voltage u_{Vs} and the corresponding output pulse train $u_{pt}(f_{pt})$ at a constant integrator input voltage u_{in} of $-2.5\,V$. The integrator output voltage u_{Vs} is displayed only in the ac-component reaching a 500 mV peak-to-peak value. The trajectory shows linear voltage gradients and also salient switching frequency caused by the switching MOSFETs of the current mirror. The output frequency f_{pt} of the pulse train equals 0.93 MHz. In Fig. 3.27, the maximum available integrator input voltage u_{in} of 8.5 V is applied to the dSVFC which cause an output voltage frequency f_{pt} of the previously discussed value 5 MHz. The charge and discharge duration matches in this OP as the output frequency f_{pt} here is exactly half of the FPGA's clock frequency f_{clk} and, therefore, the maximum reachable output frequency. The peak-to-peak value of the integrator output voltage u_{Vs} now approximately equals 200 mV, whereby the amplitude and duration the of switching transients are therefore relatively more significant. This has a pronounced effect on the linearity of the integrator's output voltage gradient, which, however, does not affect the working function of the dSVFC as the pulses are generated without errors. This completes the

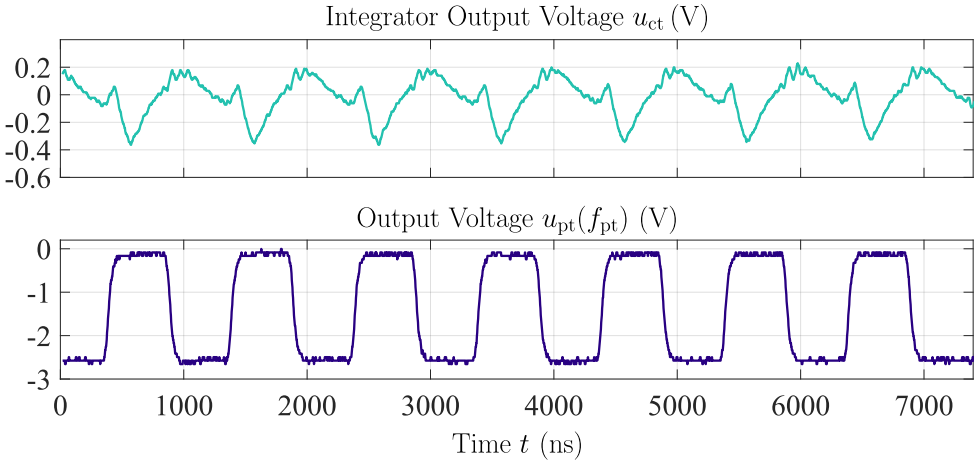


Figure 3.27: Measured integrator output voltage u_{Vs} and pulse train $u_{pt}(f_{pt})$ at $u_{in} = 8.5\,V$

successful validation of the modular dSVFC with constant integrator input voltages u_{in}.

3.3.6 Transient Analysis of dSVFC Sensor

After successful commissioning of the modular dSVFC, the conclusions drawn from the design objectives are utilized for the integration of the volt-second sensor onto a single PCB. The advantages of an integrated dSVFC sensor are the elimination of the contact resistances of the connectors from the satellites to the hub, the EMC-optimized design of the PCB and the arrangement of the components, a further reduction in costs and increased robustness against mechanical influences. Figure 3.28 shows the third integrated dSVFC prototype applied for further investigations. The design ensures that only one power supply is mandatory in addition to the direct phase conductor voltage connections. The connector is designed to plug directly to the connector of the Arty S7 board as shown in Fig. A.7 [109].

The study now incorporates an analysis of the the dynamic performance of the dSVFC, which is defined as the response to a variable input voltage, e. g. a PWM voltage input. Two different investigations are conducted. First, the correlation between the volt resolution u_ε and the switching frequency f_{sw} of a VSI in equation (3.25) is validated through measurements. Here, the PWM input voltage at the integrator input side u_{in} is emulated with a function generator. Second, the volt-second sensor's performance during commutation of a inverter half-brdige. These measurements are performed with the SEMIKRON trench IGBT module SKM 600GB066D [97] on a test bench that will be introduced in detail in Section 4.2.

The derivation of the volt-second quantum ψ_ε in Section 3.3.1 revealed its constancy as

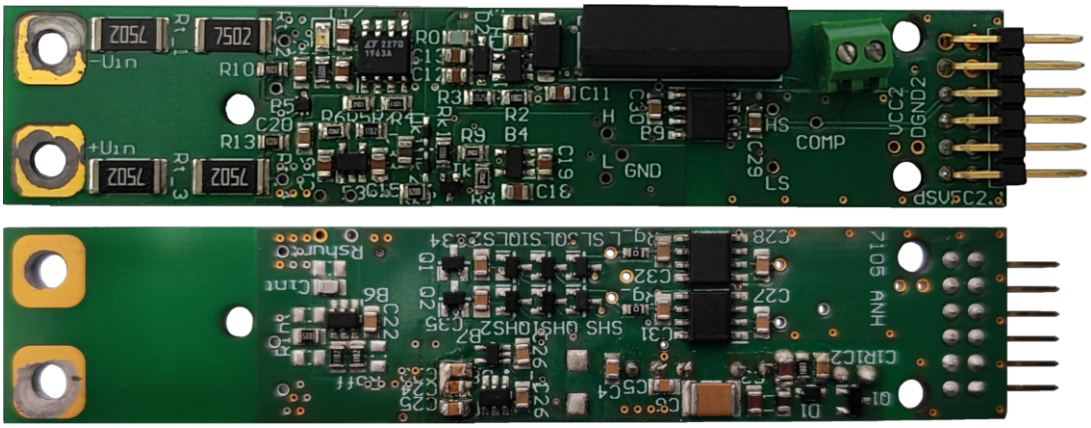


Figure 3.28: Front (top) and rear (bottom) view of the integrated dSVFC sensor, 96 mm×19 mm

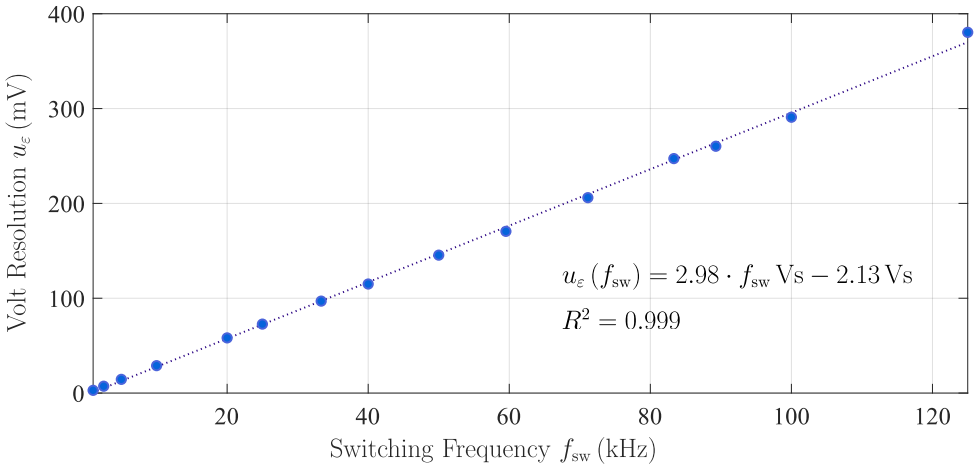


Figure 3.29: Measured resolution of modular dSVFC with regression function

it is solely defined by fixed requirement parameters, i. e. minimum and maximum input voltage $U_{\mathrm{meas,min}}$ and $U_{\mathrm{meas,max}}$, and the FPGA's clock frequency f_{clk} (equation (3.40)). However, this implies that the volt quantum u_ε linearly depends on the VSI's swichting frequency f_{sw} linked by the volt-second quantum ψ_ε as stated in equation (3.25). Therefore, a 125 kHz bandwidth is examined, starting at a switching frequency f_{sw} of 1 kHz, while maintaining a high PWM voltage level of 5 V. During each switching frequency, the duty cycle d of the PWM signal is increased in steps of 10 %. The average value of the number of pulses N within each PWM-period T_{pwm} is computed based on 100 PWM-periods. For the dynamic gain, the averaged pulses $\overline{N}$ must be considered relative to the period duration T_{pwm} of the switching frequency f_{sw}. Figure 3.29 presents the result of the conducted measurements. The linear correlation between swichting frequency f_{sw} and volt resolution u_ε validate a constant volt-second resolution ψ_ε. Nevertheless, this implies that as the switching frequency f_{sw} rises, the voltage resolution u_ε deteriorates. This is now confirmed by the calculation of the volt resolution u_ε utilized in this evaluation. The value of volt resolution u_ε is determined based on the ratio of averaged measured PWM

voltage $u_{\mathrm{ph}}^{\Diamond}$ and averaged measured number of pulses $\overline{N}$. Thereby, the difference of two various OPs is established for both voltage and pulse values. Given the linear relationship between pulses N and PWM voltage $u_{\mathrm{ph}}^{\Diamond}$, the choice of duty cycle values at 1 % and 99 % in equation (3.46) is without loss of generality.

$$u_{\varepsilon} = \frac{\bar{u}_{\mathrm{ph}}^{\Diamond}\Big|_{d=0.99} - \bar{u}_{\mathrm{ph}}^{\Diamond}\Big|_{d=0.01}}{\overline{N}\big|_{d=0.99} - \overline{N}\big|_{d=0.01}} \tag{3.46}$$

With an increase in switching frequency f_{sw}, there is a reduction in the number of pulses N within each period T_{pwm} and, consequently, a loss of volt resolution. Since the volt resolution u_{ε} is typically a measurement requirement like the measured input voltage range and the swichting frequency of the VSI, the demanded clock frequency f_{clk} of the FPGA determines the performance of the dSVFC (equation (3.47)).

$$f_{\mathrm{clk}}(U_{\mathrm{meas,min}}, U_{\mathrm{meas,max}}, u_{\varepsilon}, f_{\mathrm{sw}}) = \frac{2f_{\mathrm{sw}}}{u_{\varepsilon}} \cdot (U_{\mathrm{meas,max}} + U_{\mathrm{meas,min}}) \,,\, U_{\mathrm{meas,min}} > 0 \tag{3.47}$$

Finally, the transient behavior of the dSVFC is compared with the commercial SVFC AD652 [90]. The test bench that will be introduced in Section 4.2 is once again utilized in this measurement series. The measurements are applied at a dc-link-voltage U_{dc} of 40 V, a reference phase current I_{ph}^{*} of 0.75 A, a swichting frequency f_{sw} of 20 kHz and a duty cycle d of 50 %. A measurement section during commutation from IGBT S_1 to diode D_2 in the linear case (cf. Section 3.1.2) is presented. The measured phase voltage $u_{\mathrm{ph}}^{\Diamond}$ and the resulting output pulses N are displayed.
Figure 3.30 depictes the measurment results of the dSVFC. A clear correlation exists between the phase voltage decrease of $u_{\mathrm{ph}}^{\Diamond}$ and the reduction in pulse frequency f_{pt}. Additionally, the variation in frequency f_{pt} when changing the phase voltage level $u_{\mathrm{ph}}^{\Diamond}$ can be observed.
The relationship between the measured input voltage $u_{\mathrm{ph}}^{\Diamond}$ and the output pulses N generated by the SVFC is shown in Fig. 3.31. The basic operational procedure of the SVFC is clearly observable. However, both signals demonstrate an oscillation, contrasting with the dSVFC, which are likely attributed to the layout of the measurement board presented in Section 4.2. But it also points to the differential measurement input of the dSVFC that operates effectively.

In closing, the specifications of the innovative volt-second sensor are detailed. The first step involves a comparison of the volt-seond resolutions ψ_{ε} of the two sensors dSVFC (equation (3.48a)) and SVFC (equation (3.48b)) based on the maximum input voltage u_{in} of the integrator of 10 V. The dSVFC's resolution is enhanced by a factor of 2.5 due to its increased clock frequency f_{clk} of 10 MHz.

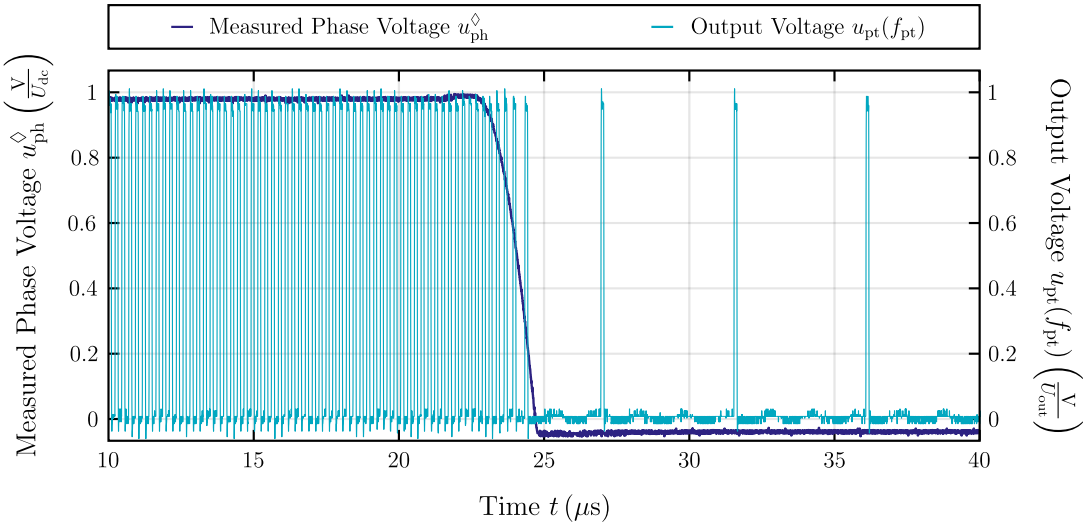


Figure 3.30: Measured phase voltage $u_{\mathrm{ph}}^{\Diamond}$ and pulse train $u_{\mathrm{pt}}(f_{\mathrm{pt}})$ of dSVFC

$$\psi_{\varepsilon,\mathrm{dSVFC}} = \frac{10\,\mathrm{V}}{1/2 \cdot 10\,\mathrm{MHz}} = 2\,\mu\mathrm{V\,s} \tag{3.48a}$$

$$\psi_{\varepsilon,\mathrm{SVFC}} = \frac{10\,\mathrm{V}}{2\,\mathrm{MHz}} = 5\,\mu\mathrm{V\,s} \tag{3.48b}$$

The volt resolution u_{ε} at corresponding switching frequencies f_{sw} is also determined for reference in the upcoming comparative study that will center on the measured phase voltage $u_{\mathrm{ph}}^{\Diamond}$. The input voltage range of the applied half-bridge equals 60 V at a dc-link-voltage U_{dc} of 60 V (including the on-stage voltage drop of IGBT and diode). This leads to a 12 µV s quantum ψ_{ε} (equation (3.49a)) conducting the calculation of the volt resolution u_{ε} for 5 kHz and 20 kHz in equation (3.49b). This equates to a 1 % relative resolution at a switching frequency f_{sw} of 5 kHz or 4 % at 20 kHz. The dSVFC is calibrated for the subsequent measurements, i. e. gain and offset are determined on the basis of the measured input voltage $u_{\mathrm{ph}}^{\Diamond}$ to the average of 12 periods of output pulses $\overline{N}$.

$$u_{\varepsilon} = 12\,\mu\mathrm{V\,s} \cdot f_{\mathrm{sw}} \tag{3.49a}$$

$$u_{\varepsilon}|_{5\,\mathrm{kHz}} = 60\,\mathrm{mV},\quad u_{\varepsilon}|_{20\,\mathrm{kHz}} = 240\,\mathrm{mV} \tag{3.49b}$$

The dSVFC's required power should be emphasized as a final point. Its power consumption P_{dSVFC} is in direct proportion to the input voltage level u_{in} it receives, and by extension, to the generated output pulse train $u_{\mathrm{pt}}(f_{\mathrm{pt}})$, necessitating the power evaluation

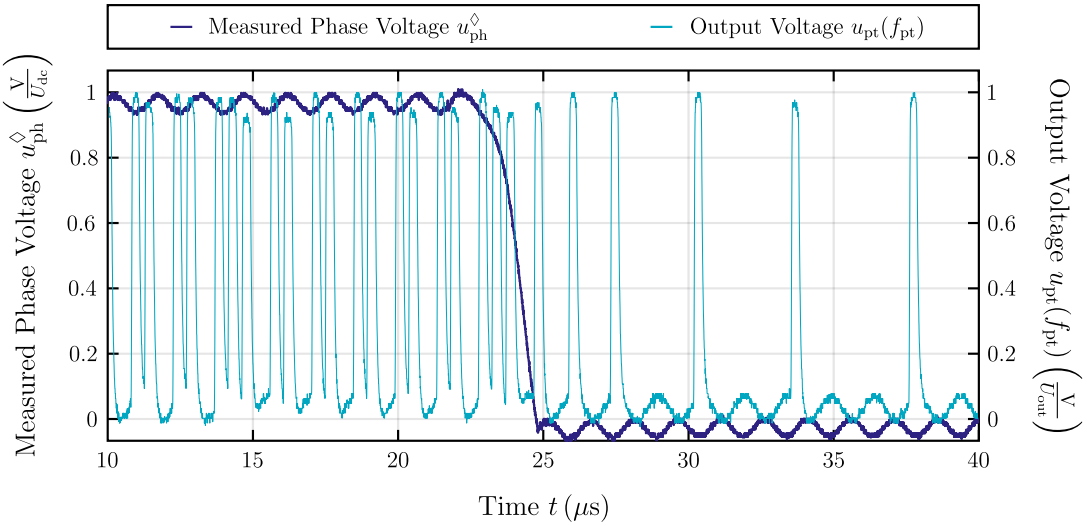


Figure 3.31: Measured phase voltage $u_{\mathrm{ph}}^{\Diamond}$ and pulse train $u_{\mathrm{pt}}(f_{\mathrm{pt}})$ of SVFC AD652

of different duty cycles d. In equation (3.50), these values recorded via the utilized the power supply are documented.

$$P_{\mathrm{dSVFC}}|_{d=0.07} = 500\,\mathrm{mW} \tag{3.50a}$$

$$P_{\mathrm{dSVFC}}|_{d=0.93} = 530\,\mathrm{mW} \tag{3.50b}$$

4 Comparative Study of Instantaneous Volt Sensing Approaches

The comparison of the measurement approaches evolved in this work is now being conducted alongside each other and, additionally, with broadly employed measurement techniques that are based on sample-and-hold (S&H) ADCs. The author chose the quantity of voltage for comparison over the volt-seconds as an oscilloscope for the reference voltage is employed. Additionally, the majority of typical measurement techniques are designed for instantaneous voltage measurement rather than instantaneous volt-second sensing, and the integrating element in the control algorithm should be excluded in this context. Figure 4.1 provides a complete overview of all measurement approaches that are part of the comparison.

A test bench is specially designed to meet the measurement criteria for testing all measurement techniques. The arrangement of this setup including all components and the handling of the measurement signals are explained. In order to address the accuracy of measuring volt-second distortions, a comparison of phase voltage measurements is specifically carried out within the low phase current range. Apart from the two dSVFC versions, all other measurement methods are executed on a single measurement board, which is introduced in this chapter. The comparison of measurement methods involves analyzing measurement errors in various OPs depending on the reference current and the duty cycle illustrated in a characteristic diagram, and average measurement errors including their standard deviations. Additionally, a cost analysis is conducted for the various measurement approaches. Ultimately, the dSVFC established in this investigation is employed on a 100 kW drivetrain for the purpose of voltage measurement and its subsequent evaluation. The author also proposes an approach for evaluating the volt-second quantum of arbitrary VFCs for PWM-less control methods such as OPP.

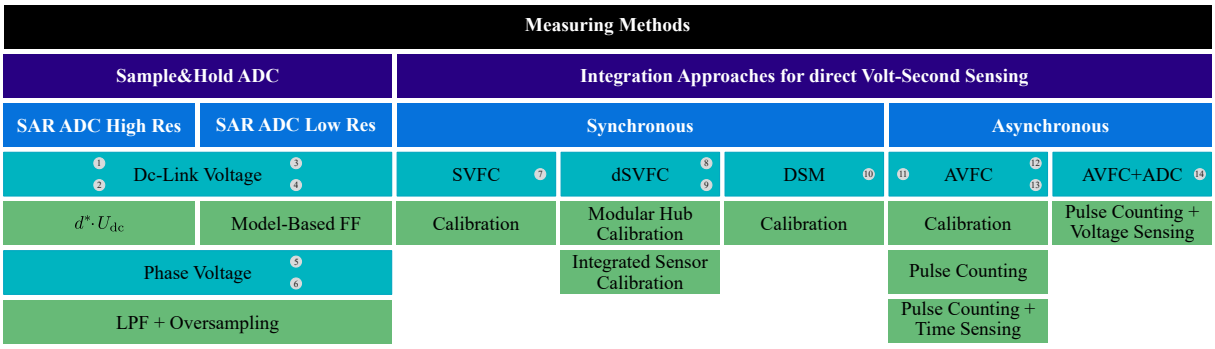


Figure 4.1: Overview of evaluated measurement methods

4.1 Sample-and-Hold Measuring Methods

In this section, the S&H methods utilized in the comparison are presented. The three measurement methods (dc-link measuring, voltage distortion model, and low-pass filtering with oversampling) are each applied to two different ADCs with a resolution of 12 bit [103] and 14 bit [110]. Both ADCs are based on the SAR architecture shown in Fig. 4.2. The SAR architecture is known to strike a good balance between conversion speed and accuracy [104], and also cost. The usual procedure involves the ADC sampling and holding the input voltage for a relatively brief acquisition time before converting it to a digital representation. Through an iterative process, the namesake approximation register is steadily converging towards its ultimate value by switching bits sequentially from the most significant bit (MSB) to the LSB. Subsequently, these bits are returned to the control unit utilizing a digital-to-analog converter (DAC). The subsequent content will present the two voltage methods that have not been introduced previously.

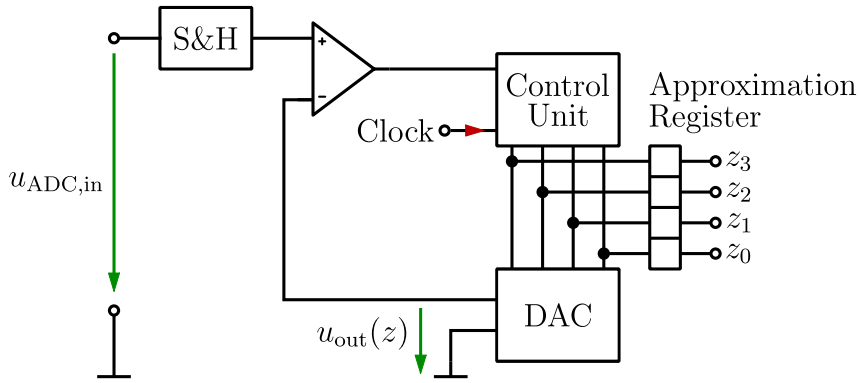


Figure 4.2: SAR ADC architecture (cf. [111])

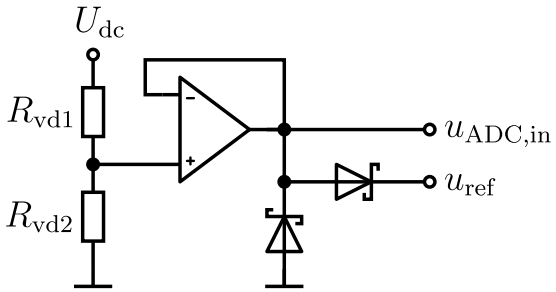


Figure 4.3: Dc-link measurement circuit

Table 4.1: Components of dc-link measurement circuit

Resistors	
R_{vd1}	R_{vd2}
56 kΩ	3.8 kΩ

4.1.1 Dc-Link Measuring Techniques

The dc-link measuring method is an indirect measurement technique as it involves sensing of other quantities and applying reference values to compute the actual phase voltage u_{ph}. It is the most basic measurement approach as it consists of the multiplication of the reference duty cycle d^* of a PWM-period by dc-link voltage U_{dc} (equation (4.51)). The dc-link voltage is acquired by an averaged, possibly varying, measured value $U_{\mathrm{dc}}^{\Diamond}$ over one PWM period. The reason behind implementing time-limited averaging is to minimize noise interference while still being able to adjust to changes in dc-link voltage $U_{\mathrm{dc}}^{\Diamond}$ between PWM periods.

$$\bar{u}_{\mathrm{pwm}} = d^* \cdot U_{\mathrm{dc}}^{\Diamond} \tag{4.51}$$

Figure 4.3 depicts the measurement circuit consisting of an input voltage divider R_{vd1} and R_{vd2}, an OpAmp buffer, and a dual Schottky diode to protect the subsequent ADC IC from negative input voltages or overvoltages. The corresponding values of the passive components are listed in Table 4.1.

Another benefit, in addition to its simplicity, is that dc-link measurement is typically accessible for other uses and only one measurement circuit is needed when utilizing reference duty cycles, regardless of the number of phases. One potential enhancement to employing the reference duty cycle d^* involves measuring the width of the PWM voltage pulse, a method demonstrated in [72]. By defining the duty cycle d more accurately, the issue of time distortion effects highlighted in Section 3.1.2 is resolved, yet amplitude distortions are not taken into consideration with this method.

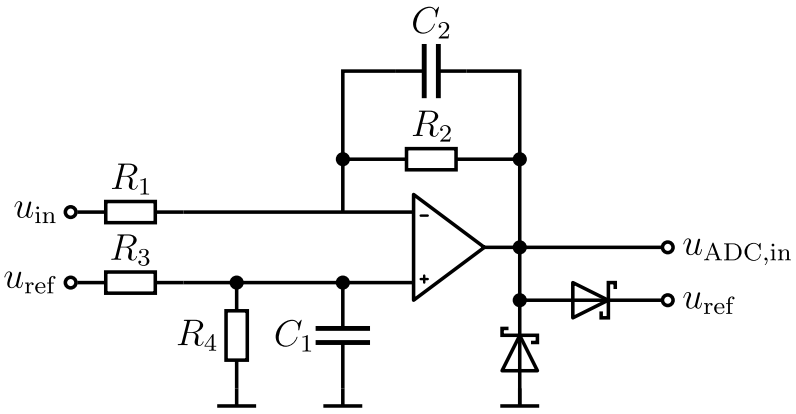


Figure 4.4: Inverting low-pass filter circuit for oversampling

4.1.2 Limiting Low-Pass Filter with Oversampling

This theory proposes a technique utilizing a time-delay characteristic of low-pass filtering to decrease the steepness of the voltage signal and subsequently sample it at a higher rate [71] as ADCs usually struggle with the very steep voltage gradients of PWM voltages as transients can occure between two sample points. As low-pass filtering causes a measuring error due to quantization and discretization errors, a design procedure that evaluates this error is presented. Parameters are chosen to optimize the low-pass filter's ability to smooth phase voltage slopes while keeping measurement phase delay minimal. Furthermore, the issue of steep phase voltage transients is magnified by digital signal processor (DSP) timer jitter, which can introduce discrepancies in sample timing [112], thus highlighting the necessity of employing low-pass filtering before data acquisition.
It is advantageous to position the low-pass filter in Fig. 4.4 on the high voltage side to minimize measurement noise. Equation (4.52) shows the TF of an inverting low-pass filter with offset [105]. Gaining insight into the design process according to [71] involves examining the component values specified for a design with a dc-link voltage U_{dc} of 75 V, comparable to the dc-link voltage U_{dc} of 60 V in this study.

$$U_{\text{ADC,in}}(s) = \underbrace{\frac{R_4\,(R_1+R_2)}{R_1\,(R_3+R_4)} \cdot U_{\text{ref}}(s)}_{\text{offset}} - \underbrace{\frac{R_2}{R_1}}_{\text{gain}} \cdot \underbrace{\frac{U_{\text{in}}(s)}{1+sT_{\text{LPF}}}}_{\text{LPF}}, \quad \text{with } T_{\text{LPF}} = R_2C_2 \tag{4.52}$$

Initiating the design process requires establishing the maximum fundamental stator frequency beforehand, a specification that is not accessible in this study. Therefore, the same value of 250 Hz is assumed. The second necessary parameter is the switching frequency f_{sw}, which is set at 5 kHz to enable the acquisition of 100 samples per PWM period. Subsequently, a provided graph enables the identification of the required filter corner frequency $1/T_{\text{LPF}}$ and expected error, whereas equation (4.52) highlights the surplus choices available in component selection. Selecting an appropriate resistor R_1 is crucial for limiting the input current in the low-pass filter circuit, while resistor R_2 is chosen to

Table 4.2: Components of dc-link low-pass filter measurement circuit

Resistors				Capacitors		Reference voltage
R_1	R_2	R_3	R_4	C_1	C_2	u_{ref}
56 kΩ	2 kΩ	330 Ω	3.6 kΩ	100 nF	600 pF	4.5 V

match the gain indicated in the 75 V design. The capacitor C_2 is distinctly determined by the previously established filter corner frequency $1/\tau_{\mathrm{LPF}}$, while the remaining elements are chosen to ensure that the offset reaches 95 % of the reference voltage u_{ref}. This allows for the detection of minor negative voltages of the measured PWM voltage $u_{\mathrm{ph}}^{\diamondsuit}$, like the voltage drop across the diode D_2 with positive reference phase current I_{ph}^{*}. The additional elements derived from this design process are listed in Table 4.2.

After a brief overview of the design of these two measurement circuits, the following section will present the test bench and the measurement board utilized to evaluate the various instantaneous measurement concepts.

4.2 Test-Bench Structure for Measuring Concept

This section provides an overview of both the test bench topology of supply and measurement instruments including the concept design of the measurement board, and the deployment of the RCP system. Additional information is available in [113] for a more thorough explanation.

4.2.1 IGBT-Based Half-Bridge with Reference Phase Current

A measurement setup must be established to validate the measurement methods discussed in the preceding sections. One inverter leg configuration, i. e. one half-bridge module, is satisfactory for assessing measurement techniques designed for single-ended measurements. As stated in the sections before, the SEMIKRON trench IGBT module SKM 600GB066D [97] is the module of choice, which is why the voltage distortion model in Section 3.1 is simulated based on its values. The setup requires a distinct specification of both the reference duty cycle d^{*} and reference phase current I_{ph}^{*}. The precision of measurements could be affected by the duty cycle, particularly when employing sample-based ADC methods that face challenges with extremely small PWM pulse widths. In order to maintain independence from dynamic phase current, a constant reference phase current I_{ph}^{*} is applied via constant current sources. This combination of reference values enables a thorough analysis of the impact of duty cycle and phase current on the accuracy of phase voltage measurement.

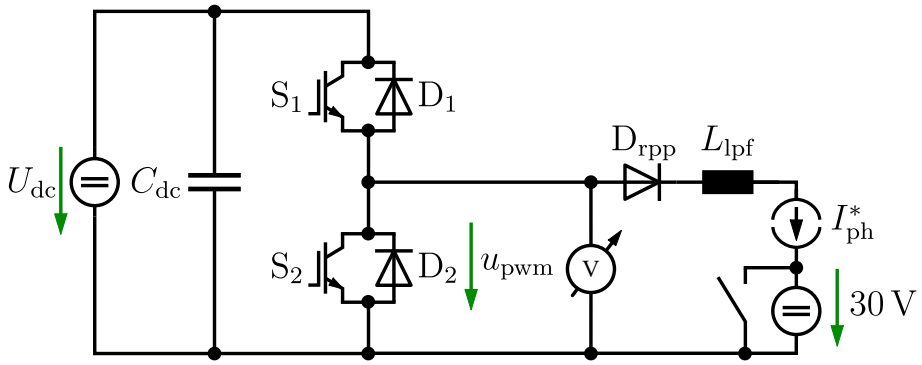


Figure 4.5: Measurement setup with variable reference duty cycle d^* and reference phase current I^*_{ph}

The test bench arrangement depicted in Fig. 4.5 satisfies these conditions (cf. [56]). The half-bridge consists of a 3 kW voltage source [114] supplying the IGBT module with a constant dc-link voltage U_{dc} of 60 V, which is stabilized by a capacitor bank C_{dc} [115]. The load path contains a smoothing inductance L_{lpf} with a value of approximately 4 mH, which will be elaborated in relation to the current sources employed. Additionally, a reverse polarity protection (RPP) diode $\mathrm{D}_{\mathrm{rpp}}$ [116] is installed allowing only positive phase currents protecting the dc-link voltage source that is incapable of sinking current. Without the RPP diode $\mathrm{D}_{\mathrm{rpp}}$ limiting power flow in the direction to the voltage source, the half-bridge might act similarly to a boost converter causing overvoltages at the dc-link source.

The half-bridge configuration is established utilizing a load that functions as a current source, two of which apply [117]. Their capacity includes both sourcing and sinking voltages within the range of -1 V to about 31 V, as well as currents of up to ± 8.2 A. This constraint is the rationale behind restricting the measurements to a maximum of 60 V. The first current source aims to apply the reference phase current I^*_{ph} for a given PWM period, while the second current source enables duty cycles of over 50 %. Utilizing only one current source would surpass the maximum voltage limit of 31 V due to the average phase voltage $\bar{u}_{\mathrm{pwm}}$ set by the half-bridge, causing a continuous positive voltage across the smoothing inductor L_{lpf} and leading to a continuous increase in positive phase current. The ability to maintain a constant current level I^*_{ph} is not always feasible because of superposition with the PWM voltage u_{ph} modulated by the duty cycle. At particular OPs, the current ripple induced by the inductor L_{lpf} is below half of the average phase current set by the first current source as the negative set voltage supplied by the device cannot be decreased any further reaching its limit. An increase in the duty cycle d and, consequently, the PWM voltage u_{ph}, intensifies this problem. Despite the less than optimal conditions, the inductor L_{lpf} enables the setting of the reference current I^*_{ph} in sufficiently small intervals. The accuracy of the setup is demonstrated to be sufficient to detect variations caused by the phase current even under limit operation and also for the highly current dependent model based feedforward technique at low phase current levels I^*_{ph}.

The voltage-distortion model in Section 3.1.1 already pointed out the similarities in behavior between positive and negative phase current I_{ph}. Semiconductor on-stage voltage drop may vary for each case, and the commutation process is present during the transition to the opposite phase voltage level, however, a change in current polarity does not fundamentally result in different behavior. Hence, it is considered acceptable to utilize the provided configuration and focus solely on analyzing positive phase currents. In case there is a desire to analyze the negative phase current I_{ph} with this measurement setup, it is possible to perform the procedure on the upper switching cell of the half-bridge employing a differential probe set at a 1:1 division ratio. However, it is crucial to note that the turn-on and turn-off delays are swapped, which is an important aspect for the model-based approach.

The test bench equipment, e. g. measurement equipment or auxiliary supplies, not affecting the electrical behavior of the test bench is detailed below. The determination of measurement error is enabled through the reference measurement of phase voltage $u_{\mathrm{ph}}^{\Diamond}$ applying a differential voltage probe [118] and an 200 MHz oscilloscope with 4 $^{\mathrm{GSa}}/_{\mathrm{s}}$ [119]. One capture will allow for 65,000 samples, with twelve PWM periods being evaluated for each OP in sequence, resulting in slightly over 5,400 samples per PWM period. Consequently, the reference measurement is sufficiently fast to outperform the ADCs of the various measurement approaches by over ten times in sample rate. Measurement of phase current I_{ph} is achievable by using a transducer [101] positioned at the center tap of the half-bridge, or a current clamp [102] connected to either the oscilloscope or RCP system (cf. Section 4.2.3), as external access is not provided by the current sources. An auxiliary 12 V power source [120] and 24 V power source [121] is employed to operate the gate drivers, and the measurement board. An overview of the arrangement is shown in Fig. A.23.

4.2.2 Voltage Measurement Board

A variety of measurement methods were outlined in the previous sections and must be implemented on a measurement board. As previously stated in the evolution of the dSVFC, neither the modular volt-second sensor nor the integrated dSVFC is considered in the measurement PCB. The measurement board itself is organized into distinct sections for general tasks like supply and reverse polarity protection, measurend dc-link voltage $U_{\mathrm{dc}}^{\Diamond}$ and phase voltage $u_{\mathrm{ph}}^{\Diamond}$ input, and a part dedicated to functionalities associated with the RCP system. Furthermore, the various measurement techniques like VFC measurement circuits [76], [90], 12 and 14 bit ADC measurement circuits [103], [110], and a DSM measurement circuit [122] are structured into segments. The measurement board including these sections are depicted in Fig. 4.6 and its schematics are accessible in Section A.3. It should be highlighted that the presentation of the measurement board in [56] is due to the fact that the residual voltage measurement at the AVFC is discussed in that research.

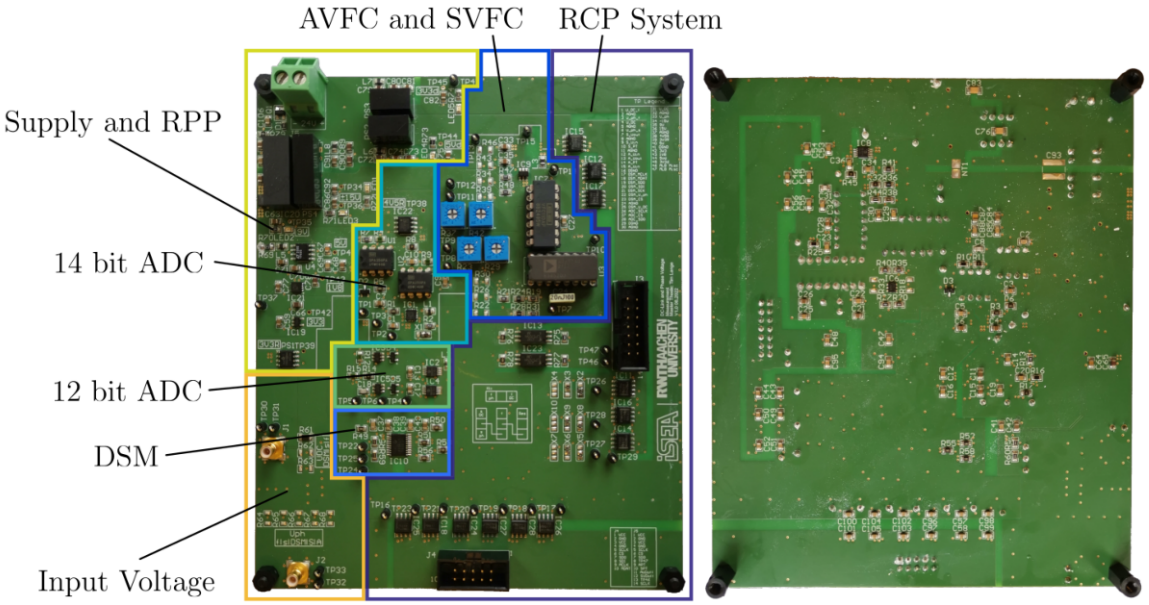


Figure 4.6: Front and back view of assembled measurement board (cf. [56])

Table 4.3: Supply voltage levels of measurement board

Type	Voltage Level	Application
Analog	±15 V	VFCs
Analog	9 V	Intermediate level
Analog	5 V	12 and 14 bit ADC
Analog	3.3 V	DSM
Analog	1.8 V	12 bit ADC
Digital	5 V	Pulse train of VFCs
Digital	3.3 V	12 and 14 bit ADC
Reference	4.5 V	12 bit and 14 bit ADC
Reference	3.3 V	DSM

Initially, the measurement board receives a 24 V supply voltage which passes through a reverse polarity protection. Following this point, the supply voltage splits off to multiple dc-dc converters and LDO regulators to convert it into the required supply voltage levels for the measurement circuits as listed in Table 4.3. As measurement circuits function as the connection point between analog and digital sectors, it is important to pay close attention to standard layout recommendations that are also addressed when laying out the dSVFC. All signals and supply voltages on the PCB are consequently spatially separated, and the top layer is predominantly reserved for power planes, while the top signal, bottom signal, and bottom layer accommodate the ground planes in the four-layer stack-up. A crucial element involves linking the dc-dc converters output grounds to the overarching analog and digital ground planes separately, except a single net tie connection for equalizing electrical potential at a singular star point. A variety of slots for jumpers allows for changing between measurement circuits that receive the measured input voltage u_{meas} ensuring to decouple the different measurement circuits. In general, the communication

can switch back and forth between the 14 bit ADC and three separate 12 bit ADCs utilized for, firstly, measuring dc-link voltage $U_{\mathrm{dc}}^{\Diamond}$ and, secondly, measuring voltage u_{meas} individually, as they are single channel devices unlike the 14 bit ADC. The third 12 bit ADC is provided for the residual voltage measurement of the AVFC.

Once the analog input voltage u_{meas} has been processed by the different measurement circuits, it must be transmitted to the RCP system discussed in the following section. Digital isolator ICs placed throughout the corresponding section on the PCB are implemented to protect the DSP system processing the measurements. In relation to the VFC measurement circuits, it is essential to consider that the AVFC is equipped with an internal integrator capacitor, whereas the integrator capacitor of the SVFC is situated externally to the IC. In this instance, the SVFC datasheet suggests utilizing a mylar capacitor or a similar variant with low dielectric absorption to ensure high linearity. The DSM is deemed to be the most configuration intensive because it entailed writing configuration registers with a serial peripheral interface (SPI) master that has slave data out (SDO) communication line capabilities to utilize it in the intended way for PWM voltage measurement.

4.2.3 Rapid Control Prototype System

An RCP system is employed to operate the half-bridge module and to evaluate the measurements taken from the measurement board. The same RT system is utilized as in Section 3.3.5: The MicroLabBox DS1202 provided by dSPACE GmbH [108]. The software structure of the MicroLabBox is categorized into a real-time processor (RTP) realized by a DSP and FPGA levels. The necessary functionalities for this work include analog and digital IO capabilities, and a sensor supply output to power the RCP side of the digital isolators on the measurement board. The lower FPGA level is as usual responsible for handling IO processing, while the higher DSP level is in charge of user interaction and communication with the host.

An overview of the RCP system's DSP level signal processing is depicted in Fig. 4.7. For a comprehensive list of all signals implemented, a more thorough description can be found in Fig. A.24. Through the human-machine-interface (HMI), the user sets input parameters for the entire RCP system, which are then processed at the DSP level and forwarded to the FPGA. The FPGA executes the signal processing with high speed requirements and IO handling and passes the output signal back to the DSP for operations, e. g. floating point multiplication and division, displaying the parameters in the HMI again.

The description of processing and evaluation in the subsequent part specifically targets the VFC measurement cicuits. Details on the processing and evaluation of the remaining measurement methods are explained in Section A.3.1. Internal evaluation of both VFC versions is performed by a VHDL unit, similar to the dSVFC setup. The established VFC evaluation unit helps in interpreting the VFC pulse train at the FPGA level. The unit

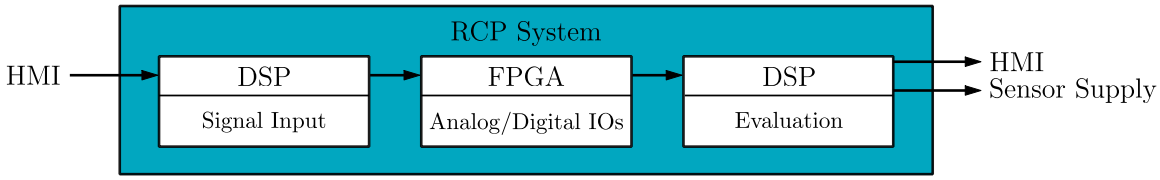
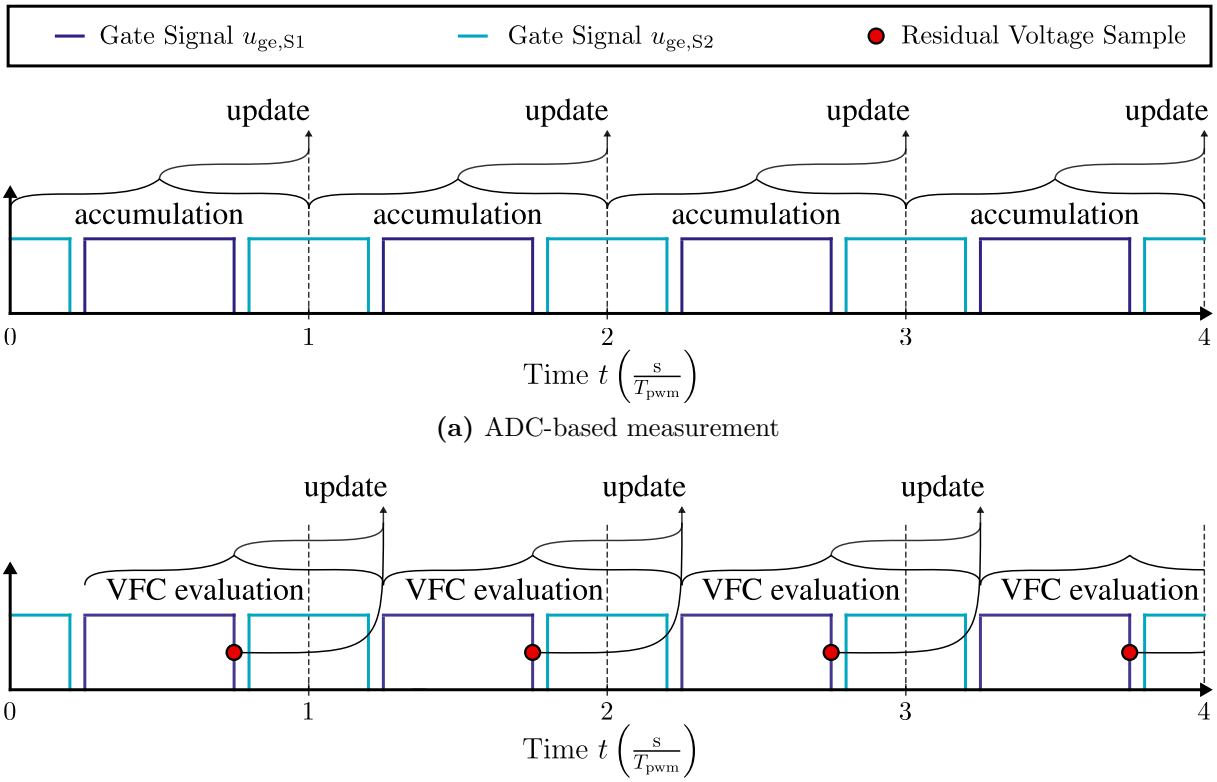


Figure 4.7: Signal flow diagram of RCP system

produces a counter that increments in accordance with the FPGA frequency f_{clk}, tracking both high and low PWM voltage levels (Fig. A.25, signal `hcnt` and `lcnt`), and associating them with their occurrence during high or low levels (Fig. A.25, signal `hpcnt` and `lpcnt`). The AVFC pulse counting with time sensing approach incorporates an additional FPGA clock frequency counter (Fig. A.25, signal `lbpcnt`) representing the duration between the last two accurately identified pulses. The DSP carries out the processing of the FPGA output signals as described in Section 4.3.1.
A problem arises as center-aligned PWM is the only type of PWM supported by the PWM half-bridge module. However, AVFC interpretation methods necessitate left-aligned for the pulse counting and time sensing method and right-aligned the for the residual voltage measurement technique. As the setup is not incorporated within an application employing PWM timings, an internal construct aligns the switching signals for the aforementioned approaches. The VFC evaluation module utilizes the upper gate signal $u_{\text{ge,S1}}$ to trigger the synchronous latching of outputs at the rising edge of the signal, rather than using the PWM trigger. Additionally, the upper gate signal $u_{\text{ge,S1}}$ is channeled to an impulse generator, which then transmits it to the evaluation module, as the residual voltage evaluation model's logic is discretely applied, not through a VHDL block. In this instance, the ADC is continuously acquiring samples. When there is a reduction in value detected by the ADC between two samples, the latest low sample is saved. However, if the ADC indicates a rising slope between two samples, the stored information is maintained and no further updates are executed. The successful filtering of residual voltage from the continuous samples is accomplished by applying this logic to the waveform from Fig. 3.13 for positive phase currents I_{ph} and negative low level input voltages u_{meas}. Subsequently, two registers in series are linked to store the ADC values of residual voltages for evaluation the current PWM period when the upper gate's rising edge impulse signal occurs.

An overview of the evaluation periods and update timing schemes is depicted in Fig. 4.8a for ADC based measurements and in Fig. 4.8b for VFC based measurements. As the ADC-based measurement methods aligns with the PWM modulators' output trigger, the signals from the ADC averaging unit are observed to latch symmetrically onto the center of the bottom gate switching signal $u_{\text{ge,S2}}$. As stated before, the PWM trigger is disregarded and updates occur at rising edge of the upper gate switching signal $u_{\text{ge,S1}}$ for the VFC-based techniques.

Once the test bench topology, measurement board, and signal processing of the RCP system have been clarified, it is important to describe how the final measurements will be executed for the various OPs in the upcoming Section 4.3. Therefore, the measurement



(a) ADC-based measurement

(b) VFC-based measurement

Figure 4.8: Evaluation periods and update timing schemes

trigger is explained further, as with this trigger via the HMI, a synchronization with the PWM trigger follows first, which is needed for recording the measurement data over one OP. Three measurement trigger signals are generated within the FPGA by considering a measurement window that consists of a total of 12 PWM periods.
The corresponding reference measurement is captured by the oscilloscope, which is connected to the half-bridge setup through a differential voltage probe, as previously indicated. The oscilloscope is triggered by a separate signal by connecting another oscilloscope channel to a test point on the measurement board that is connected to the RCP system. These two measurement trigger signals are utilized to initiate and terminate recordings in the RCP system, respectively. This guarantees the synchronization of the 12 PWM periods being analyzed between the measured data on the RCP system and the reference data on the oscilloscope. In the absence of any time-critical tasks other than measuring the PWM voltage, all values compared to the reference measurement are obtained between the PWM triggers in the middle of a PWM period. Despite VFC-based measurements being delayed compared to ADC-based measurements, both are accessible before half of the consecutive PWM period passed. Throughout all measurements – even at high duty cycles – the DSP is always fast enough to process all updates, and a sample to compare against reference measurement.

Table 4.4: Identifiers for investigated measurement appoaches

Identifier	Description
`dUdc12/14`	Dc-link measurement with 12/14 bit ADC multiplied by reference duty cycle
`MBff12/14`	Voltage-distortion model based feedforward with 12/14 bit ADC
`LPFOS12/14`	Low-pass filter with oversampling with 12/14 bit ADC
`DSMCal`	DSM calibrated to reference measurement
`AVFCPcCal`	AVFC total pulse counting calibrated to reference measurement
`AVFCPcff`	AVFC pulse counting feedforward
`AVFCPcTsff`	AVFC pulse counting and time sensing feedforward
`AVFCRes`	AVFCPcCal plus reference measurement for residual voltage measurement technique
`SVFCPcCal`	SVFC total pulse counting calibrated to reference measurement
`moddSVFC`	Modular dSVFC total pulse counting calibrated to reference measurement
`dSVFC`	Integrated dSVFC total pulse counting calibrated to reference measurement

4.3 Comparison of Various Measuring Approaches

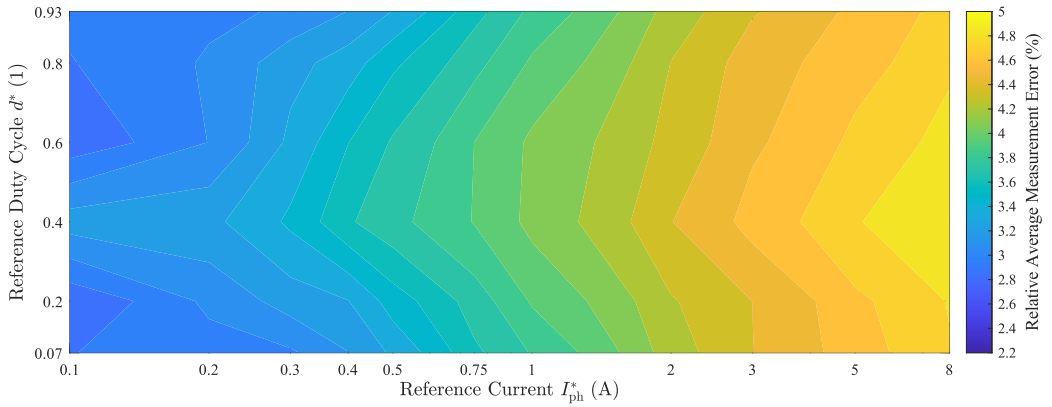
After outlining a comprehensive analysis of the complete test bench setup, the following section will discuss the evaluation of each introduced measurement approach. Table 4.4 serves as an overview of the 14 investigated methods being contrasted and their assigned identifiers. The key aspect is the accuracy of the measurements regarding the capture of an instantaneous PWM voltage. As stated before, the synchronization between the oscilloscope reference measurement and the measured PWM voltage for twelve consecutive PWM periods per capture is utilized. Following the examination of the accuracy of each individual measurement technique, they are compared with each other based on the selected operating range. Lastly, the costs of the individual measuring circuit devided into ICs and discrete components are contrasted.

The test bench introduced in Section 4.2 is employed to configure individually 72 OPs for each reference duty cycle d^* and reference phase current I^*_{ph} combination as listed in equation (4.53).

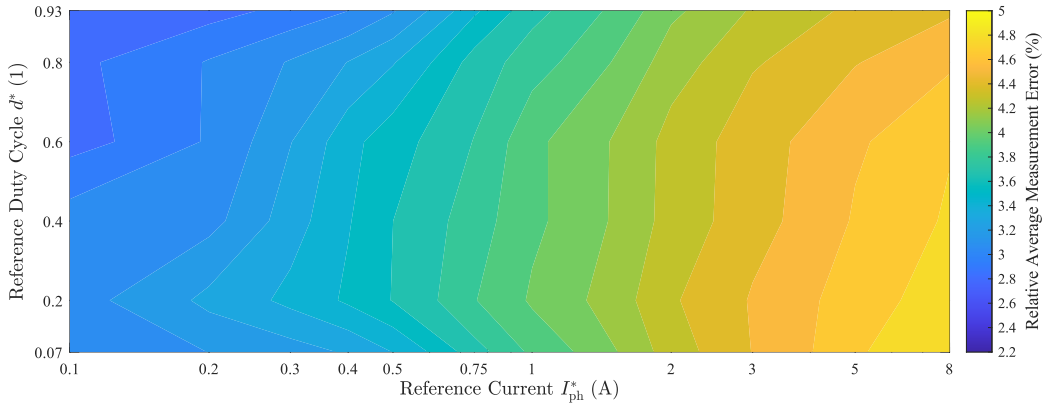
$$d^* = \{7\,\%, 20\,\%, 40\,\%, 60\,\%, 80\,\%, 93\,\%\} \tag{4.53a}$$

$$I^*_{\mathrm{ph}} = \{0\,\mathrm{A}, 0.1\,\mathrm{A}, 0.2\,\mathrm{A}, 0.3\,\mathrm{A}, 0.4\,\mathrm{A}, 0.5\,\mathrm{A}, 0.75\,\mathrm{A}, 1\,\mathrm{A}, 2\,\mathrm{A}, 3\,\mathrm{A}, 5\,\mathrm{A}, 8\,\mathrm{A}\} \tag{4.53b}$$

The boundary conditions represent the lower and upper limit of the reference duty cycle d^* that can practically exhibit switching actions with a chosen VSI switching frequency f_{sw} of 5 kHz and a dead time T_{dt} of 3 µs.



(a) Accuracy of dc-link voltage based method with 12 bit ADC: `dUdc12`



(b) Accuracy of dc-link voltage based method with 14 bit ADC: `dUdc14`

Figure 4.9: Accuracy of dc-link voltage based method

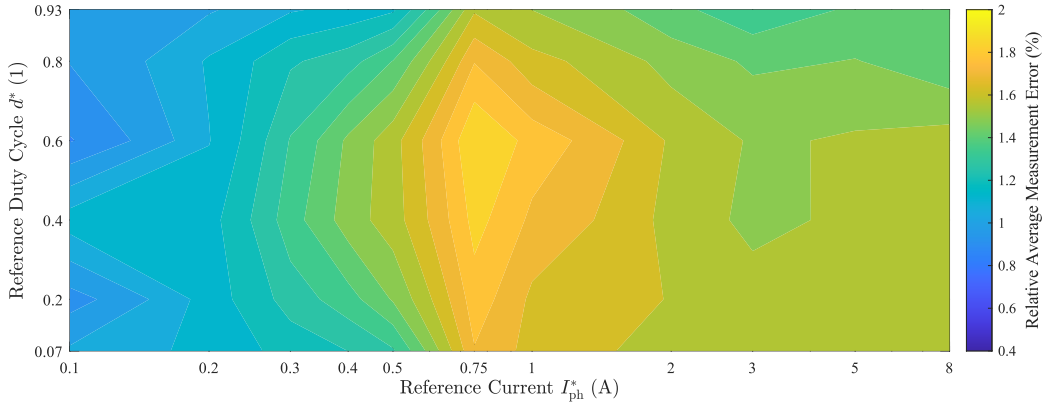
4.3.1 Evaluation of Measurement Accuracy

The relative average PWM voltage measurement error $e_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$ within the characteristic diagram serves as a metric for evaluating measurement accuracy. It is important to consider the various levels of the color bar in each contour plot as some measurement methods are overall more accurate than others. This depiction enables a precise evaluation of accuracy levels across the entire operating range and demonstrates potential correlations with the phase current I^*_{ph} or the duty cycle d^*. It is important to note that the analysis only considered the 72 OPs and the average voltage error values $e_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$ normalized to the reference dc-link voltage U_{dc} of 60 V are interpolated. In addition, when following this plot layout, the relative average voltage measurement error $e_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$ for each measurement approach is established by computing the average values for all 12 captures of PWM periods.

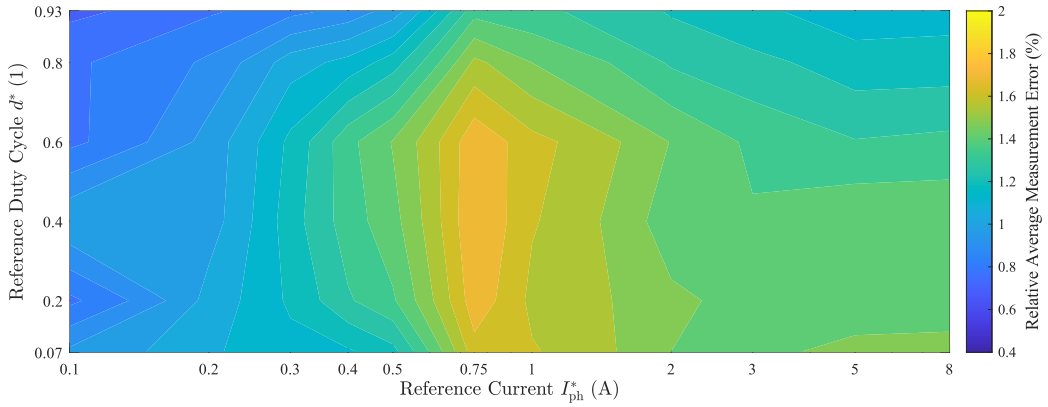
The accuracy plot shown in Fig. 4.9 represents the results obtained from the first measurement technique, which entails the multiplication of the reference duty cycle d^* by the

measured dc-link voltage $U_{\mathrm{dc}}^{\Diamond}$ for both 12 bit ADC (Fig. 4.9a) and 14 bit ADC (Fig. 4.9b). The commissioning and calibration of the 12 and 14 bit ADCs are verified solely for voltages around 60 V, as the complete measurement range is not essential for dc-link measurement. The measured PWM voltage u_{ph} is calculated according to equation (4.51) for both `dUdc12` and `dUdc14`. The measurement error in both the `dUdc12` and `dUdc14` techniques is predominantly attributable to the voltage distortions due to time delays like discussed in Section 3.1. As derived in Section 3.1.2 for positive reference currents I_{ph}^{*}, there are two voltage-distortion areas caused by time delays in every PWM period − one for IGBT and one for diode commutation. The first commutation consistently diminishes the reference PWM voltage, while the second commutation, including capacitive effects, increaes it (cf. Section 3.1.2). A high influence on the PWM voltage especially in the low phase current range is displayed in the measurements of the PWM voltage trajectories in Fig. 3.7a. In situations where reference phase currents I_{ph}^{*} are extremely low, the voltage-time area at the beginning and end of the high PWM voltage level effectively counteract each other, resulting in the most accurate OPs of `dUdc12` and `dUdc14`. When the phase current I_{ph}^{*} rises, less and less of the earlier volt-second area is neutralized by the subsequent dead time interval. This explains the dependence on the phase current I_{ph}^{*} of the resulting measurement error $e_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$ of this measuring technique. `dUdc12` displays a reduced dependency on reference duty cycle d^{*}, notably at 40 %, whereas `dUdc14` demonstrates an even weaker association at 20 % for even lower phase current levels. The difference in value between the two measurement series, as they operate similarly, is unlikely to be a result of technique error, but rather due to previous calibration. Furthermore, it is established that the measurements do not show any significant differences in their evaluation, as the choice of ADC for sampling the nearly constant dc-link voltage U_{dc} is of minimal significance.

In the examination of the voltage-distortion model that follows in Fig. 4.10, the current clamp [102] is employed due to its superior resolution compared to the available LEM transducers, which enhances the model's performance with precise measurement of low phase currents I_{ph}^{*}. Thus, the accuracy of measurements achieved should be seen as the highest level of precision attainable through the model-based feedforward technique `MBff12` (Fig. 4.10a) and `MBff14` (Fig. 4.10b), rather than expecting similar levels of accuracy in less precise implementations of current measuring in other applications. Since the model approach is also depending on the dc-link voltage and the duty cycle, the same value as before are utilzed, i.e. measured dc-link voltage and reference duty cycle. Considering that the model approach is also based on the dc-link voltage and duty cycle, the same values as previously are employed, i. e. the measured dc-link voltage $U_{\mathrm{dc}}^{\Diamond}$ and reference duty cycle d^{*}.
`dUdc12` and `dUdc14` exhibit a minimum error of 2 %, which is the largest error percentage found in the measurements obtained through the model-based appoaches `MBff12` and `MBff14`. For high reference phase currents I_{ph}^{*}, there are low dependencies on current and moderate average errors, whereas high current dependencies in the nonlinear case of the model are exhibited for low reference currents as expected. Nonetheless, the most notable deviation occurs at a phase current level slightly exceeding 0.75 A. The experimental results reveal that the limit current $I_{\mathrm{ph,lim}}$ is at 0.713 A and, thus, differing from the



(a) Accuracy of voltage-distortion model feedforward with 12 bit ADC: `MBff12`

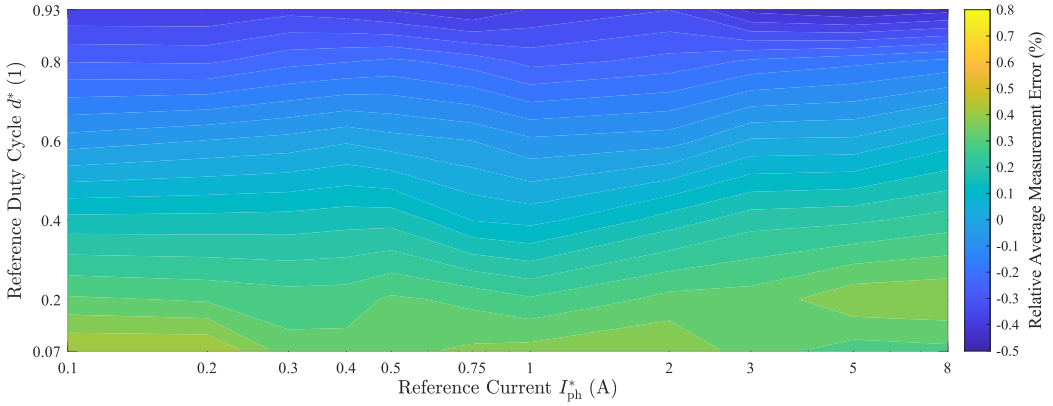


(b) Accuracy of voltage-distortion model feedforward with 14 bit ADC: `MBff14`

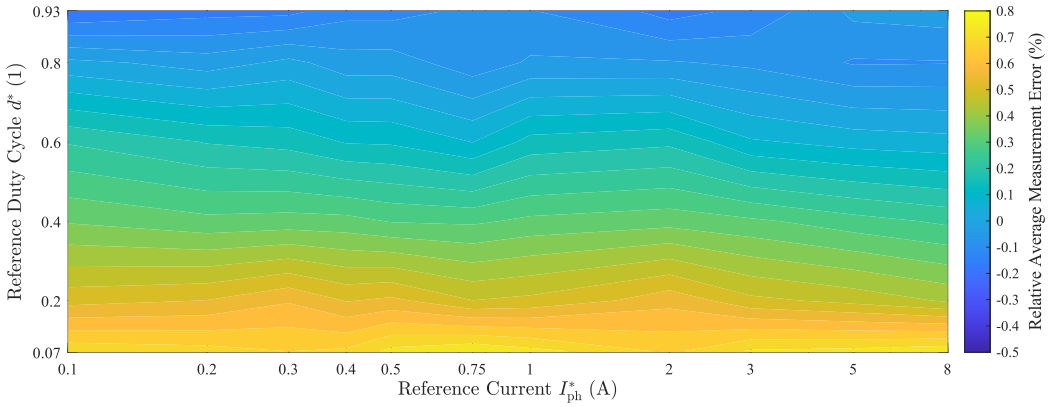
Figure 4.10: Accuracy of voltage-distortion model feedforward

theoretically expected limit phase current. The reason for this may be that when the phase currents are at this threshold value $I_{\mathrm{ph,lim}}$, the model switches abruptly between the linear and nonlinear case resulting in the highest measurement errors seen. Nevertheless, an average measurement error of well under 2 % can be obtained, which is satisfactory for a simplistic model that is not constructed based on any prior measurements but solely datasheet parameters (cf. Section 3.1). Improving the accuracy of the model approach could be a result of determining the limit phase current I^*_{ph} through measurements. Similar to `dUdc12` and `dUdc14`, the most effective operation of `MBff12` and `MBff14` is observed at lower phase currents, where the impact of dead time volt-second areas is nullified. As expected similar to the prior measurement series, there is no observable advantage to increasing the resolution of dc-link measurement.

The final investigated method for ADC-based measurements involves employing low-pass filtering and oversampling for both 12 bit ADC (`LPFOS12`) and 14 bit ADC (`LPFOS14`) in Fig. 4.11. Unlike dc-link measurement techniques, the average measurement error does not vary with the reference phase current I^*_{ph} but with the reference duty cycle d^*. A



(a) Accuracy of low-pass filtering with oversampling method with 12 bit ADC: `LPFOS12`



(b) Accuracy of low-pass filtering with oversampling method with 14 bit ADC: `LPFOS14`

Figure 4.11: Accuracy of low-pass filtering with oversampling method

decrease in reference duty cycle d^* corresponds to a higher average measurement error due to overestimation of the measurement circuit. Nevertheless, there has been a significant enhancement in the general precision of measuring instantaneous PWM voltage $u^{\Diamond}_{\mathrm{ph}}$. Once again, a reduction in resolution from 14 bit (Fig. 4.11b) to 12 bit (Fig. 4.11a) does not seem to influence the average measurement error, with only a slight variance in offset between the two ADCs noted, although the overall error range is nearly identical in both scenarios. In conclusion, low-pass filtering and oversampling measurement techniques are superior among the previously ADC-based approaches, though demanding one ADC per phase instead of just one overall ADC for dc-link measurement.

In the following, after the low-pass filter with oversampling measurement method, the second direct voltage measurement circuit is examined. The DSM is another ADC IC mainly employed in audio and measurement systems like precision digital multimeters, data loggers, and sensors. Typically, their application involves serving as sensors for temperature, pressure, acceleration, or magnetic field detection [123] to enable accurate and noise-free measurements. A DSM also produces a pulse train like a VFC as its output, converting

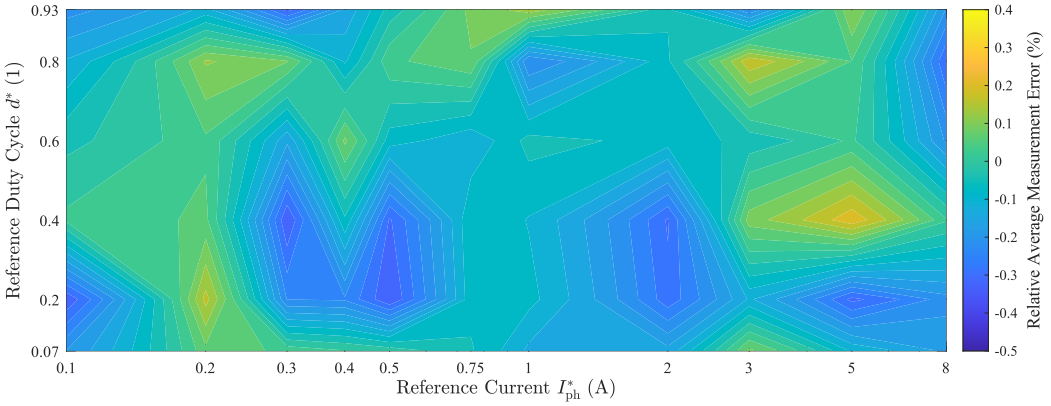
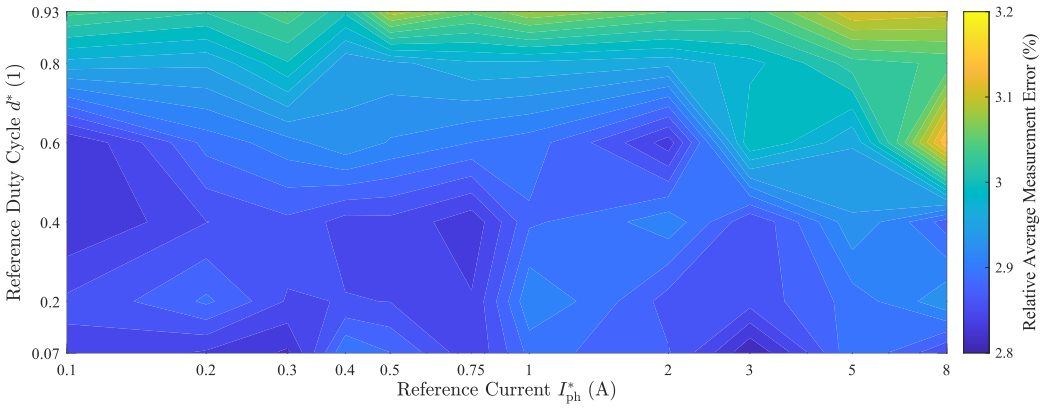


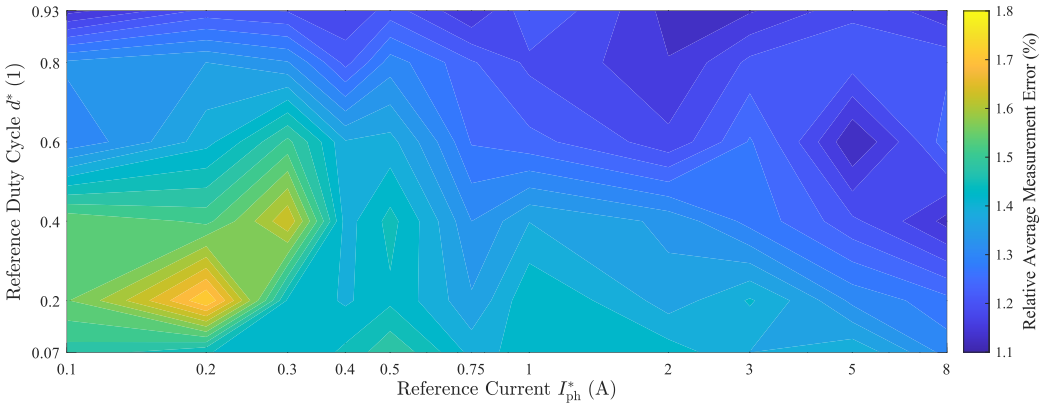
Figure 4.12: Accuracy of DSM measuring method: `DSMCal`

an analog input signal into a high-frequency digital bitstream. This pulse train represents the modulated signal, which is then converted into a precise digital signal through digital filtering and decimation.
Although the DSM configuration is challenging, measurements are conducted with it as displayed in Fig. 4.12. In the same manner as the VFC circuits to be examined subsequently, there is no dependency on reference phase current I^*_{ph} or reference duty cycle d^* throughout the entire characteristic diagram. Alongside the low-pass filter oversampling approach, this measurement method `DSMCal` covers a wide range where measurement imprecision is nearly nonexistent. This indicates that it outperforms all other measurement techniques analyzed thus far.

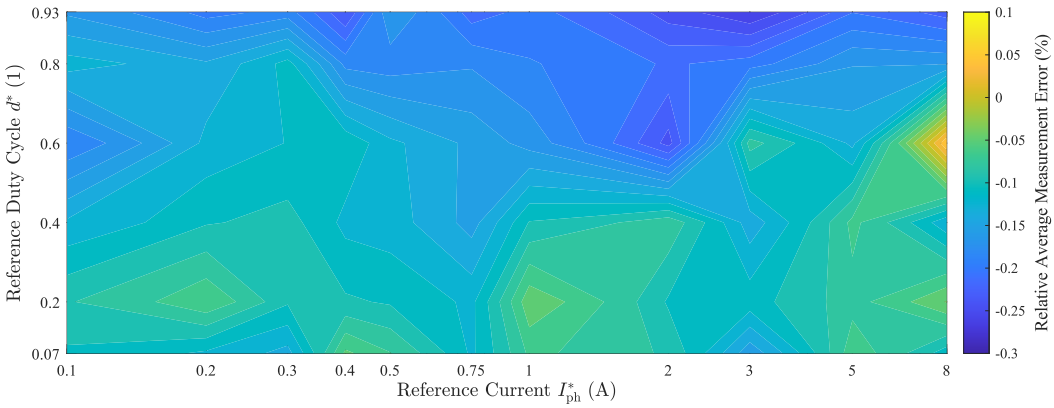
In the subsequent analysis, the focus shifts to the accuracy levels of the VFC-based measurement methods. Starting with the AVFC with pulse counting feedforward method (Fig. 4.13a), it is observable that this evaluation scheme `AVFCPcff` exhibits high measurement errors across the entire range. This direct measurement technique shows the weakest performance, even if the majority remains under a deviation of 3 %. The desired progress is attained through the additional integration of time sensing between pulses at low PWM voltage via edge detection leading to an approximate halving of measurement error (Fig. 4.13b). Yet, there is a clear positive discrepancy in the accuracies derived from both evaluation methods `AVFCPcff` and `AVFCPcTsff`. The performance of both feedforward techniques can suffer due to variations in input PWM voltage on the PCB and uncertainties in the voltage divider ratio. Similar to the `DSM`, there is no indication of any correlation on phase current or duty cycle.
Even though there is an enhancement in `AVFCPcTsff`, it is overshadowed by the notably superior results of the AVFC pulse counting calibration method `AVFCPcCal` depicted in Fig. 4.13c. Through the direct correlation of generated output pulses N and reference voltage measurement u^*_{ph}, it becomes possible to eliminate any unwanted influences and presumptions by means of calibration. As projected, the SVFC proves to be marginally more linear than its asynchronous alternative, consequently enhancing its precision. The SVFC outperforms other commercial VFC ICs due to its wide range of measurement er-



(a) Accuracy of AVFC with pulse counting feedforward: `AVFCPcff`



(b) Accuracy of AVFC with pulse counting and time sensing feedforward: `AVFCPcTsff`



(c) Accuracy of AVFC with pulse counting calibration: `AVFCPcCal`

Figure 4.13: Accuracy of AVFC measuring method

rors around 0 %, which is shown in Fig. 4.14. A significant observation is that the SVFC shows superior performance compared to the anticipated volt resolution u_ε of 0.25 % as per equation (3.25) during the evaluation of measurement errors. The cause of this occurrence is the phenomenon described in Section 3.3.3 where the number of pulses N

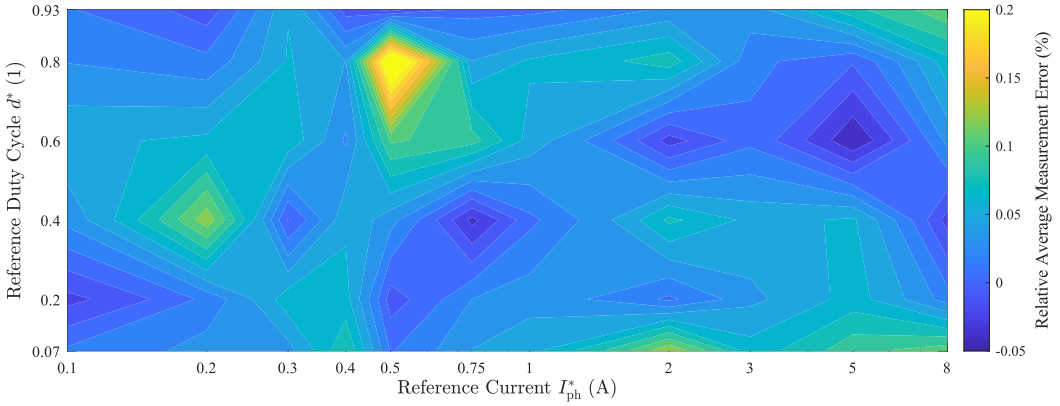


Figure 4.14: Accuracy of SVFC with pulse counting calibration: `SVFCPcCal`

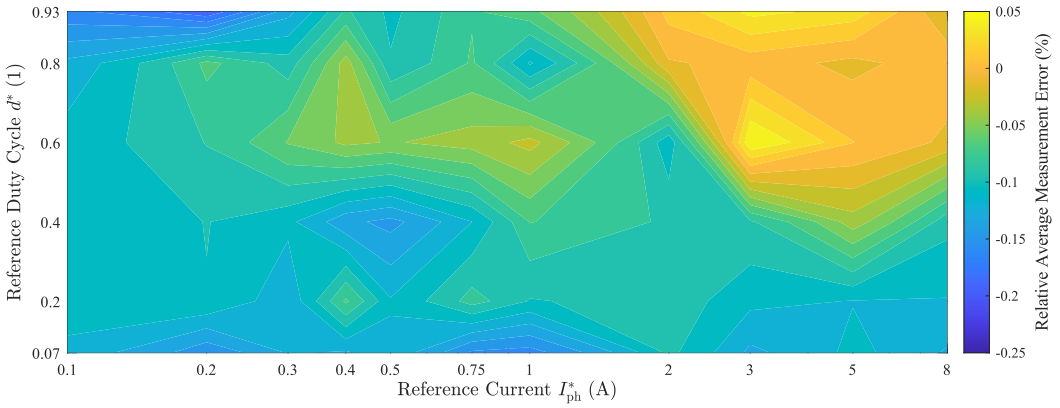
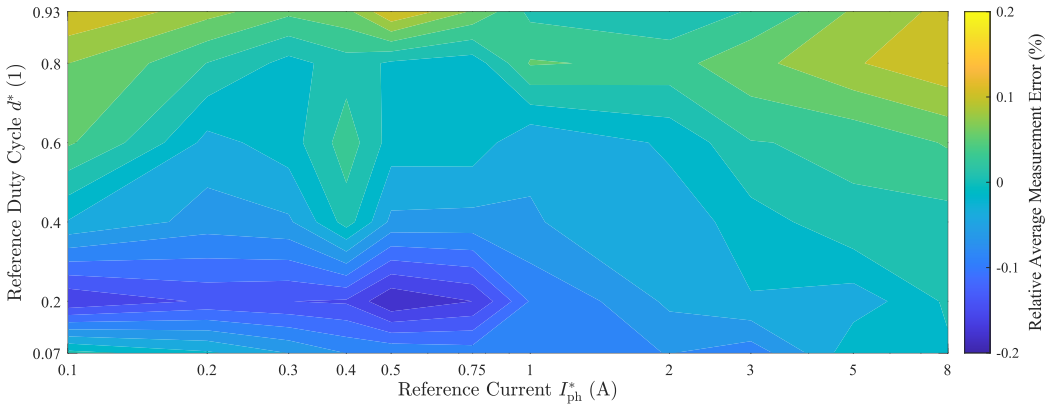


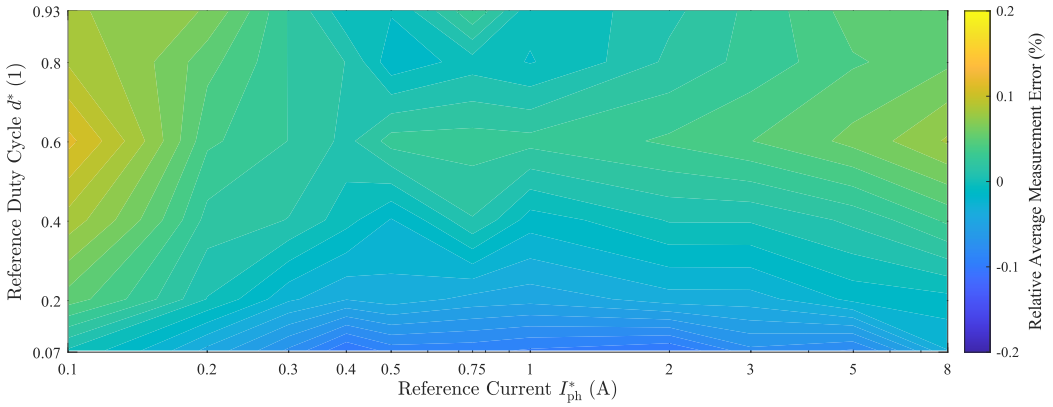
Figure 4.15: Accuracy of AVFC with residual voltage sensing (cf. [56]): `AVFCRes`

per PWM period varies based on the currents in the input node of the inverter circuit (equation (3.34)). Averaging over 12 PWM periods per OP contributes positively to minimizing the average measurement error of the SVFC. The investigation in Section 4.3.2 will indicate that the deviation is reflected in another statistical quantity: the standard deviation $\sigma_{\bar{u}_{\mathrm{pwm}}}$ of the calculated average measurement error $e_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$.

The last instantaneous measuring approach based on a commercial VFCs is to extend an AVFC extended with an additional ADC to sense the residual voltage once per PWM period. In order to effectively detect residual voltage, it is necessary to modify the offset circuit to prevent the integrator output voltage from saturating. This adjustment leads to the overall pulse count for one PWM period being halved, yet this has minimal impact on the precision of the AVFC, as extensively discussed in [56]. In addition to this near-constant resolution, the additional residual voltage sensing `AVFCRes` exceeds the accuracy of the AVFC calibration method `AVFCPcCal` as Fig. 4.15 depictes. Nevertheless, the combination of AVFC and ADC is still unable to surpass the precision of the highly linear SVFC.



(a) Accuracy of modular dSVFC: `moddSVFC`



(b) Accuracy of integrated dSVFC: `dSVFC`

Figure 4.16: Accuracy of dSVFC with pulse counting calibration

Lastly, an analysis is conducted on the newly created volt-second sensor dSVFC, considering both its modular `moddSVFC` and integrated variations `dSVFC`. Both versions are being examined to observe a possible impact on the measurement error due to the change of contact resistance of the connector or modified PCB design. Upon initial observation, there is a general alignment in the patterns of the measurement error within the operating range. By contrasting the measured deviations with the anticipated volt resolution u_ε of the dSVFC outlined equation (3.49b), it is proven that the calculated limits of 0.1 % are maintained throughout the majority of the measurement range. One exceedance at the result of `moddSVFC` occurs to reference phase currents I^*_{ph} below 0.7 A when operating at a 20 % reference duty cycle d^*. A first explanation is the assignment of the phase current range to the nonlinear case being less than the limit phase current $I_{ph,lim}$. Nevertheless, the correlation is dismissed due to the highest negative measurement error occurring in the `dSVFC` at a reference duty cycle d^* of 7 % and reference phase currents I^*_{ph} exceeding the limit current $I_{ph,lim}$. Basically, the characteristic diagram of the two types of volt-second sensors closely align the measurement error of the SVFC, differing only by a factor of 2.

4.3.2 Accuracy and Instantaneousness in Comparison

Comparing the individual measuring approaches can be challenging due to significant differences in both average measurement errors and varying dependencies on phase current or duty cycle, as demonstrated by characteristic diagrams. To address this difficulty, the average relative measurement error $\bar{e}_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$ is calculated across all OPs to evaluate the accuracy of each measurement method. It gives a condensed overview of the thorough analysis on average measurement error $e_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$ in Section 4.3.1.
Furthermore, the standard deviation $\sigma_{\bar{u}_{\mathrm{pwm}}}$ of the determined average measurement error $e_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$ is added as an additional statistical quantity. It is common knowledge that the standard deviation $\sigma_{\bar{u}_{\mathrm{pwm}}}$ relates to the degree of consistency in the measured value recorded per PWM period by the measurement circuit. This measured value per PWM period is exactly the measured instantaneous volt value $u_{\mathrm{ph}}^{\Diamond}$. Consequently, the standard deviation $\sigma_{\bar{u}_{\mathrm{pwm}}}$ serves as an interpretative indicator for the instantaneousness of a measurement circuit. Ideally, the standard deviation $\sigma_{\bar{u}_{\mathrm{pwm}}}$ would be zero if the measured instantaneous voltage value remained consistent at one OP. Thus, a more instantaneous measurement method results in a lower calculated standard deviation.

Figure 4.17 presents the results for the average relative measurement error $\bar{e}_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$ of all 72 OPs and the standard deviation $\sigma_{\bar{u}_{\mathrm{pwm}}}$ for each measurement method. The ADC-based measurement methods are characterized by two saliences: They exhibit the highest level of inaccuracy, yet consistently reflect this inaccuracy in every PWM period. The outcome is expected given that if the input variables, such as the reference duty cycle d^*, the constant measured dc-link voltage $U_{\mathrm{dc}}^{\Diamond}$, or the constant reference phase current I_{ph}^*, are held constant during the computation, the resulting PWM voltage will not change.
The VFC-based measurement methods − excluding the feedforward techniques − achieve a good average measurement error, yet an approximately ten times higher standard deviation than the ADC-based techniques. Averaging data over multiple PWM periods has a positive impact on reducing the average measurement error especially for the SVFC (which exhibits the smallest average measurement error), while deviations in each individual PWM period are stated through its high standard deviation. The developed residual measurement technique, which combines advantages from VFC-based and ADC-based methods, ensures low average measurement error and standard deviation. In direct comparison to the SVFC, it can be seen that the standard deviation of the residual voltage method is nearly five times lower and, thus, it is more reliable when requiring instantaneousness.
The comparison of the dSVFC indicates that the integrated volt-second sensor shows superior performance in average measurement error and standard deviation compared to its modular alternative. The measurement devation is nearly the same as the deviation of the residual measurement approach, even though its standard deviation is slightly worse. In contrast, it outperforms the commercial SVFC significantly in terms of standard deviation, making it equally suitable for instantaneous measurements like the residual measurement.

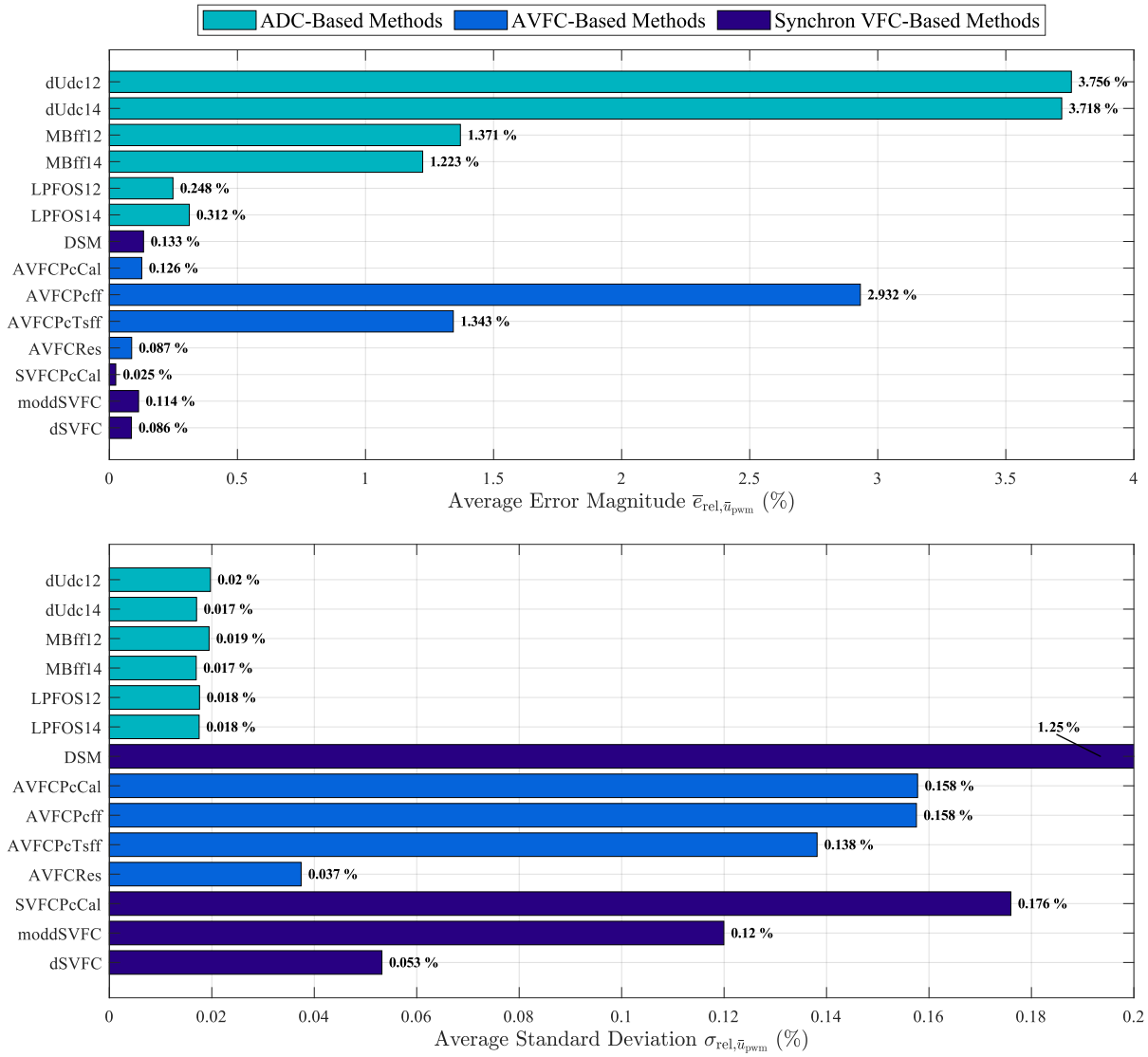


Figure 4.17: Average measurement error $e_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$ and standard deviation $\sigma_{\bar{u}_{\mathrm{pwm}}}$ of investigated measurement methods at $f_{\mathrm{sw}} = 5\,\mathrm{kHz}$

To conclude, commercial VFC-based methods are not ideal for instantaneous phase voltage assessment because of their high standard deviation. Increasing the VSI's switching frequency f_{sw} contributes to a degradation in volt resolution u_{ε}, thereby reducing the accuracy of the measured average PWM voltage across a single PWM period. This problem is solved through the implementation of the residual voltage measurement technique, which effectively enables the instantaneous measurement of phase voltage for AVFC. The dSVFC also demonstrates remarkable results when utilizing a 5 kHz switching frequency f_{sw} as the chosen test parameter. Its volt resolution also deteriorates with rising switching frequency f_{sw}, but the design principles developed in this study allow for its modification for higher switching frequencies; a feature that is not achievable with commercial VFCs. Moreover, every VFC-based approach possesses a key benefit that is absent in both the ADC-based methods and the residual voltage technique: they have the ability to mea-

sure volt-seconds directly, not just within a PWM cycle, but also in control systems that deviate from traditional PWM methods. An example demonstrating the application of hyper-instantaneous volt-second sensing is shown in Section 4.4.2 utilizing OPPs.

In reference to the DSM, it should be noted that the average measurement error $\bar{e}_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$ is very low, in line with expectations from the characteristic diagram in Fig. 4.12, and is comparable to that of the other VFC measurement methods in terms of magnitude. However, the DSM seems to demonstrate a considerable disparity in voltage measurements for each PWM period, what can be concluded from its high standard deviation $\sigma_{\bar{u}_{\mathrm{pwm}}}$. The author suggests that the reason for this could be the DSM's inadequate configuration, indicating that its measurement capabilities may be more potential than received by the results in this study.
Ultimately, it is important to highlight that a calibrated measurement approach is the preferred option over any feedforward measurement method as it produces the most accurate results.

In essence, the limitations experienced by control algorithms at low speeds become apparent when examining the results obtained from the conventional techniques of measuring the dc-link voltage and multiplying it by the reference duty cycle. By utilizing the conclusions of this study, a user can decide on the appropriate circuit for a specific use case.

4.3.3 Acquisition Costs of Sensor Technologies

If the cost of the measurement circuits is prohibitively high, an effective and reliable measurement technique is not implemented in field. Therefore, at the end of this section, a cost analysis of all the measurement techniques examined here will be presented. In the course of this, the cost evaluation is consistently based on a single sensor, even though some measurement methods would require multiple sensors to fully measure a three-phase VSIs. Thereby cost advantages associated with the measurement of multiple voltages using an IC (e. g. dc-link measuring technique) are disregarded. The expenses of each measurement circuit are subdivided into the prices of ICs and costs of further passive and active components. Calculations are done on basis of prices of 24$^{\mathrm{th}}$ March 2023 for full reel instead of single cut-tape. As PCBs, connectors, cables, FPGA or DSP or the like are determined by their application, they are not presented in this description. Furthermore, the prices for the substractor of the dSVFC and the measurement equipment for the model-based approach are not incorporated in cost calculations.

The accrued costs are visualized in Fig. 4.18. With the ADC-based technique, the 14 bit ADC is more cost-intensive than the 12 bit ADC. Since the resolution of the ADC does not have an impact on its accuracy, the additional costs here are not lucrative. The AVFC-based techniques are equal in price, due to being based on the same hardware and only varying in evaluation methods. Respectively, because of the additional ADC the residual measurement is more expensive than the related AVFC-based circuits. Thus,

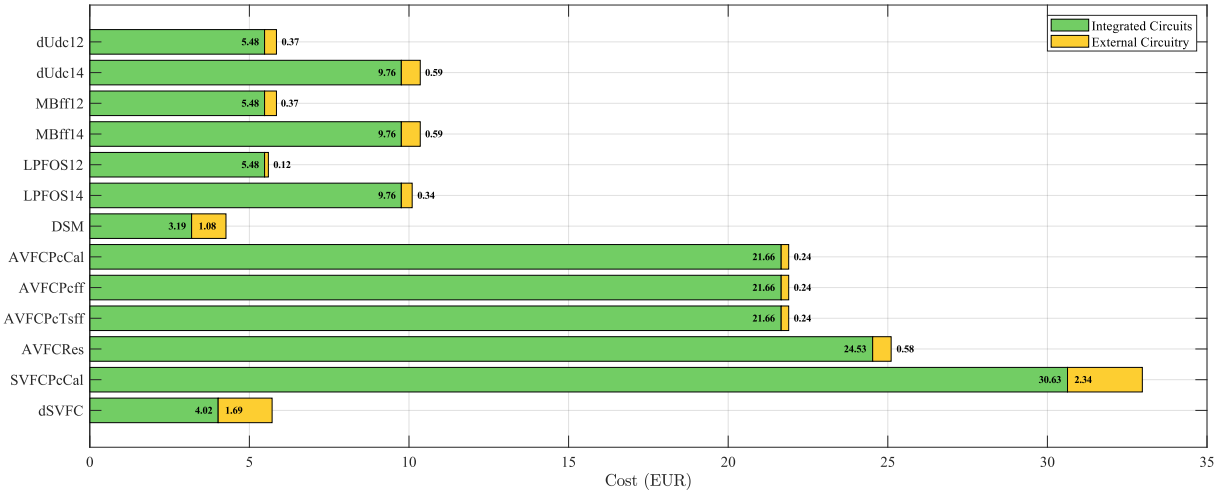


Figure 4.18: Costs of investigated measurement approaches

the higher costs result in an improvement of the accuracy The measuring accuracy due to the high linearity of the SVFC also entails correspondingly high acquisition costs; at a cost of over €30, it is by far the most expensive measuring circuit. The goal of cost optimization of the dSVFC has been successfully achieved, as it is one of the most cost-effective measuring circuits at just over €5, making it almost six times cheaper than its integrated SVFC variant. The dSVFC is clearly the best in cost-benefit efficiency at this point in view of the fact that it comes close to the measuring accuracy of the dSVFC and at the same time outperforms it in standard deviation. Only the DSM at less than €5 is even cheaper than the dSVFC.

4.4 Magnetic Flux Determination of Electrical Machines

Following the comprehensive analysis and contextualization of the dSVFC in the prior section, the volt-second sensor is evaluated for its appropriateness on a 100 kW electrical drivetrain. Investigation into the influence of EMC on measurement results is required, in conjunction with dielectric strength when measuring two phase-to-phase voltages with a peak-to-peak voltage value of 800 V_{pp}. Following the measurement of instantaneous phase-to-phase voltage, the author makes a proposal for employing the volt-second sensor in PWM-free control strategies.

4.4.1 Instantaneous Volt Sensing at a Three-Phase IPMSM

A 100 kW electric drive train on a motor test bench is equipped with two volt-second sensors, as specified in Section 2.2.1. The task of measuring one phase-to-phase voltage u_{12}

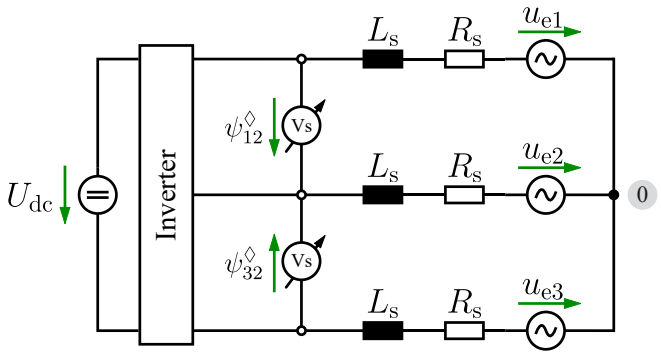


Figure 4.19: Sensing of phase-to-phase flux-linkages $\psi^{\diamond}_{12}$ and $\psi^{\diamond}_{32}$

and u_{32}, respectively, is assigned to each dSVFC sensor as depicted in Fig. 4.19. Pictures in the appendix displays both the motor test bench in Fig. A.34 and the dSVFC sensors that have been put into operation in Fig. A.35. The device under test is an IPMSM controlled by an field-oriented control (FOC) with an IGBT-based VSI. A swichting frequency f_{sw} of 10 kHz is applied to the VSI. After adjusting the voltage divider ratio to 1:80, calibration is carried out on both dSVFCs to enable an input voltage range u_{meas} of ± 400 V. Accordingly, the relative voltage resolution u_{ε} equals 0.2 % for this case of application.
The measurements are once more conducted using voltage sensing rather than flux-linkage sensing, as the reference measurement is performed using a four-channel LMG500 power analyzer manufactured by ZES Zimmer [124]. The voltage measurement capability of this device includes ports that allow direct measurement of voltages up to 1 kV. In this evaluation, the power analyzer measures the three-phase voltage and computes the phase-to-phase voltages u_{12} and u_{32}.

As an example measurement, the drive train is operated at an OP with an applied dc-link voltage of 200 V, mechanical speed at 2000 rpm, a flux-generating stator current component i_{sd} of -52 A, and a torque-generating stator current component i_{sq} of 89 A. Figure 4.20 depictes the measured PWM phase-to-phase voltages of both the reference measurement of the power analyzer u_{12} (top) and the instantaneous voltage sensing $u^{\diamond}_{12}$ of the dSVFC (bottom). The left-hand side trajectories illustrate two electrical periods of the electrical machine, each lasting 10 ms. The power analyzers' reference measurement shows the PWM-voltage u_{12} resulting from the subtraction of the corresponding phase voltages u_{ph1} and u_{ph2}. The bottom plot shows the associated instantaneous voltage measuring $u^{\diamond}_{12}$ of the dSVFC sensor, which successfully measures the average voltage $\bar{u}_{pwm}$ over one PWM period. For instance, upon examining the highest point of the trajectory, it is evident that the dSVFC voltage mirrors the decreasing mean amplitude of the dc-link voltage U_{dc}.
The graphs to the right offer an enlarged display, showcasing 10 PWM periods of the VSI, each lasting 0.1 ms. The fourth and fifth periods represent the zero-crossing of the PWM waveform, in which both negativ and positiv pulses in the reference measurement are recorded. These average values are also correctly detected by the volt-second sensor.

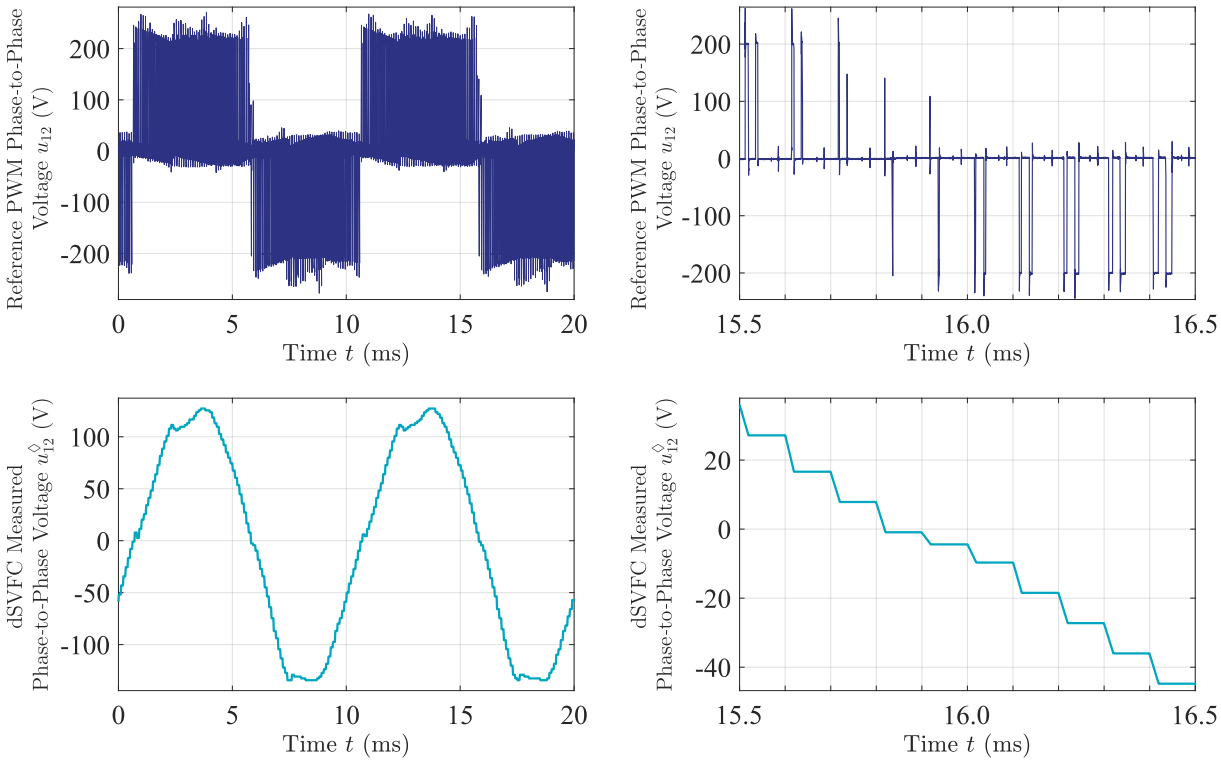


Figure 4.20: Measurement of reference PWM phase-to-phase voltage u_{12} (top) and measurement of dSVFC instantaneous phase-to-phase voltage $u_{12}^{\diamondsuit}$ (bottom), two electrical periods (left) and a zoom of 10 PWM-periods (right)

It should be emphasized that despite not measuring a peak-to-peak voltage value of 800 V in this example, both volt-second sensors were calibrated to an input voltage range of ±400 V and passed the calibration successfully. Furthermore, there are no weaknesses in the dSVFC regarding EMC sensitivity. Consequently, the author recommends the developed volt-second sensor within this work for instantaneous voltage of phase-to-phase voltage sensing in electric drive trains.

4.4.2 Volt-Second Sensing Approach per Pulse

The key benefit of VFC-based measurement circuits is their arbitrary but fixed volt-second quantum ψ_ε, which is solely determined by the measured input voltage range and the applied clock frequency as stated in equation (3.40). Consequently, the volt-second resolution ψ_ε is independent of quantities like dc-link voltage U_{dc}, phase current i_{ph}, duty cycle d, or VSI switching frequency f_{sw}. In the event that a single pulse N is produced, it is immediately linked to this unit of flux-linkage. The only variation is in the time intervals Δt_{P2P} between pulse generation.

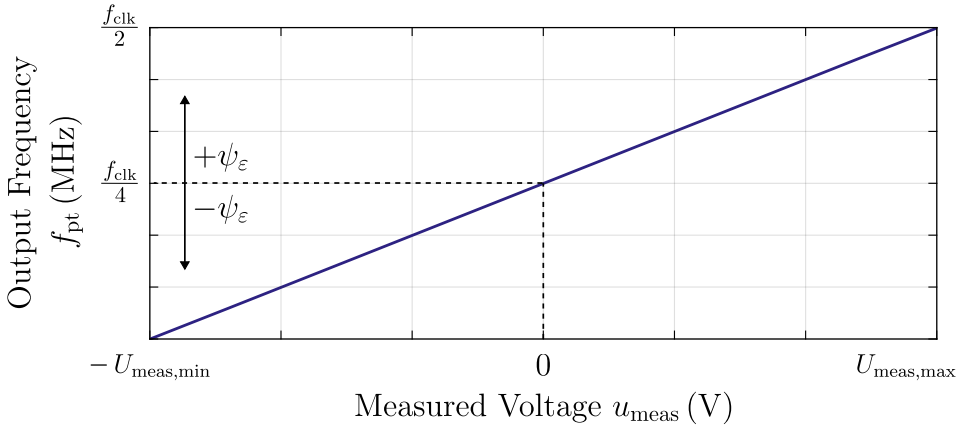


Figure 4.21: Characteristic curve for volt-second quantum counting

The same principles as the AVFC-based measurement technique Pulse Counting and Time Sensing (`AVFCPcTsff`) are utilized in the following approach. The information obtained from the time duration Δt_{P2P} between two consecutive pulses can be applied to interpret whether the input voltage is negative or positive, and thereby establishing if the flux component is negative or positive, as illustrated in the characteristic curve in Fig. 4.21. In the following example, a symmetrical bipolar input voltage, like the phase-to-phase voltage, is assumed without loss of generality. Since the maximum output frequency f_{pt} is half the applied clock frequency f_{clk}, the limit between negative and positive applied magnetic flux-linkage is exactly at a quarter of the clock frequency. The logic of equation (4.54) (for the special case of a symmetric input voltage) can assist in deciding whether the generated volt-second quantum ψ_ε needs to be incremented or decremented within the control algorithm.

$$\begin{aligned} &\text{if} \quad {\Delta t_{\mathrm{P2P}}}^{-1} < 1/4 f_{\mathrm{clk}}, \quad \text{then} \; -\psi_\varepsilon \\ &\text{if} \quad {\Delta t_{\mathrm{P2P}}}^{-1} > 1/4 f_{\mathrm{clk}}, \quad \text{then} \; +\psi_\varepsilon \\ &\qquad\qquad\qquad\qquad\qquad\quad \text{else } 0 \end{aligned} \tag{4.54}$$

The key point to consider is that the algorithm gains access to the volt-second quantum immediately after it has been recorded. By applying the dSVFC, the user is able to freely establish the quantum's value through adjusting the clock frequency. This strategy can be implemented for any input voltage ratio of negative and positive voltage mapping the corresponding ratio to the output frequency f_{pt}. This instantaneous volt-second sensing method is entirely independent of any PWM scheme, making it a suitable control algorithms like OPPs, where traditional PWM-based voltage measurement methods as discussed in this study are inadequate.

5 Conclusions and Future Work

Electrical drive trains require appropriate measured quantities for successful operating control algorithms. Accurate detection of the control variable flux-linkage or voltage, respectively, is particularly important, especially within the low-speed range when pulse widths of PWM voltage become relatively small. This dissertation has addressed key challenges in precise and instantaneous flux-linkage sensing methods in PWM VSIs. The findings presented in this study not only validate proposed measurement approaches but also provide opportunities for further investigations.

5.1 Conclusions

Volt-second distortions arise from the nonideal characteristics of the employed VSIs, thus becoming an inherent aspect of electrical drive trains. Understanding the origins of these distortions and their impact on the VSIs and electrical machine's performance is crucial. Therefore, an efficient simulation model for an IGBT-based VSI is developed to conduct an in-depth investigation of PWM voltages. The subsequent mathematical analysis reveals the voltage deviations and nonlinear characteristics that arise especially in the low phase current range due to the semiconductor devices. Thorough knowledge of voltage trajectory behavior allows for the development of volt-second sensing that meets the necessary criteria for effectively measuring PWM voltages.

The functionality of VFCs is well-adapted for a constant sensing of voltage-time areas in any voltage pattern. As a result, two different commercial VFCs are applied in the design of the measurement technology: An asynchronous VFC and a synchronous VFC. As a result of their immediate pulse response to a specific volt-second quantum, AVFCs are particularly well-suited for the design of various evaluation algorithms. which are presented within this work. The measurement reliability of the SVFC is attributed to its clock-controlled pulse output, which exhibits a high degree of linearity. Despite this, given its limitations in performance at common inverter switching frequencies of at least 10 kHz and its high cost, a new volt-second sensor is developed drawing inspiration from its operational principle. It is reasonable to split the features of an SVFC into an analog and a digital component. The SVFC internal clocked bistable multivibrator is replaced by a clocked FPGA as it is in place in most applications. The discrete structure of the analog part of the novel volt-second sensor dSVFC offers the benefit of being customizable to fulfill particular requirements. A comprehensive description of circuit synthesis and its

design requirements is provided in this study. Ultimately, to contextualize the newly devised measurement methodologies, they are assigned to a comprehensive comparative evaluation.

An evaluation test bench is established to assess individual measuring circuits according to phase current and duty cycle variations. The measuring accuracy and instantaneousness of each 14 circuits is evaluated in 72 OPs. Subsequently, a statistical examination is conducted to compare the measurement strategies in their average measurement error and standard deviation. The advantages of VFC-based measurement circuits over ADC-based methods are clearly demonstrated. In this comparison, the residual measurement technique and the dSVFC demonstrate the most effective performance. The results generally show that a calibrated measurement circuit surpasses all feedforward methods implemented in this study. Still, even with a reliable measuring circuit, its usage in the field will be limited by high costs. For this reason, the costs associated with obtaining all measurement strategies are presented, which highlights the dSVFC's superiority. As a result, the newly established volt-second sensor fulfills all specified requirements in terms of accuracy, instantaneousness, and costs. Subsequently, two dSVFCs are successfully implemented on a 100 kW motor test bench to establish their suitability for sensing a traction drive's instantaneous phase-to-phase voltage. The volt-second sensors accurately detect an 800 V_{pp} peak-to-peak voltage and show no sensitivity on EMC. In closing, a universal method is introduced for utilizing the inherent advantage of directly sensing volt-seconds in the dSVFC and other VFCs. This serves as proof that the dSVFC is suitable not only for precise instantaneous voltage measurement, but also for direct volt-second sensing techniques.

5.2 Open Issues and Future Work

Future studies should examine the IGBT-based simulation model for its applicability to other semiconductor components like SiC or GaN. Additionally, the author proposes the mathematical derivation of the model, incorporating the capacitor value of the output capacitance of the IGBT datasheet for the additional capacitor in the switching cell modeling. To distinguish between linear and nonlinear cases during commutation, it is necessary to employ a different capacity selection for determining the limit phase current, which is dependent on this capacitance. This adaption has the potential to improve the correlation with the measurend voltage graphs and, thus, also decrease inaccuracies in measurements based on the model. To evaluate the switching behavior of semiconductors at voltages near their nominal voltage level, the test bench needs to be modified to handle dc-link voltages higher than 60 V.

The DSM-based measurement circuit should be investigated for further improvement to instantaneous volt-second and volt sensing as its configuration has proven to be challenging. Due to its minimal expenses and existing integration as an IC, this measurement

method shows potential for practical application in industries.
The dSVFC arrangement is presumable limit to the time delay characteristics of the switching MOSFETs within the current mirror acting as SPDT switch. Exploring the possibility of substituting the existing current mirror with a MUX for switching the charging and discharging current is a promising area for study. These advancements could result in better performance through higher possible clock frequencies leading to improved sensor resolutions, a simplified layout, and further cost efficiencies.
In conclusion, the successful integration of the dSVFC into different control strategies is needed to demonstrate its performance and, thus, improve the behavior of electrical drive trains.

A Appendix

A.1 Simulation Results of Voltage-Distortion Model in PLECS

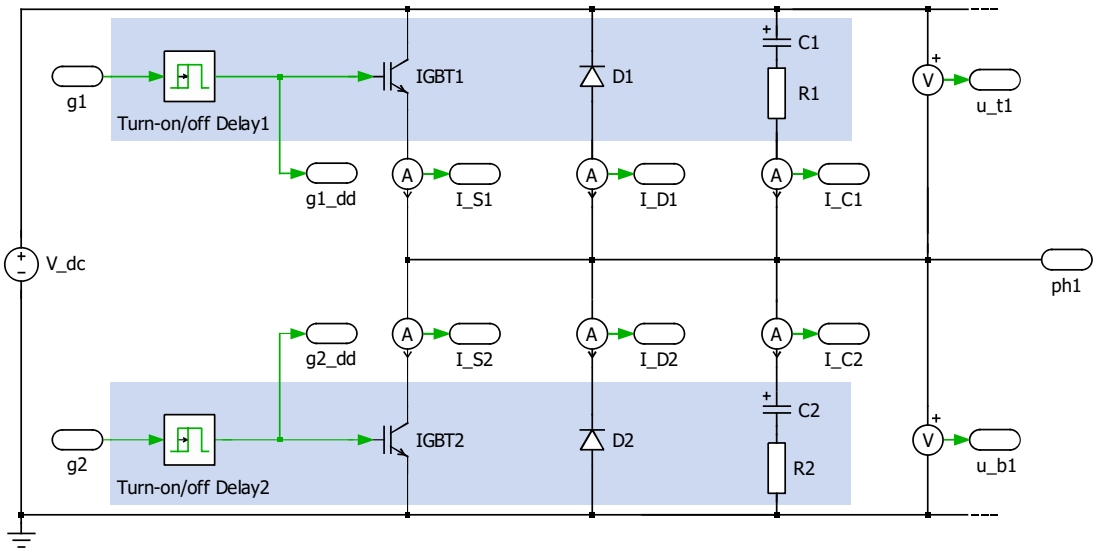


Figure A.1: Model approaches of half-bridge with nonideal commutation cell in PLECS (cf. [54])

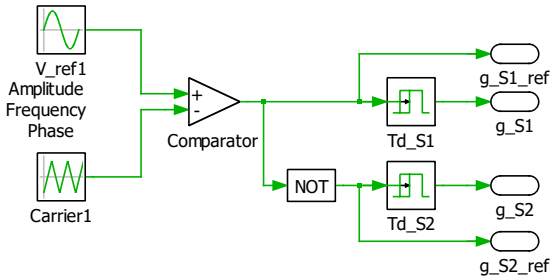


Figure A.2: Model approaches of driver with dead time T_{dt} in PLECS (cf. [54])

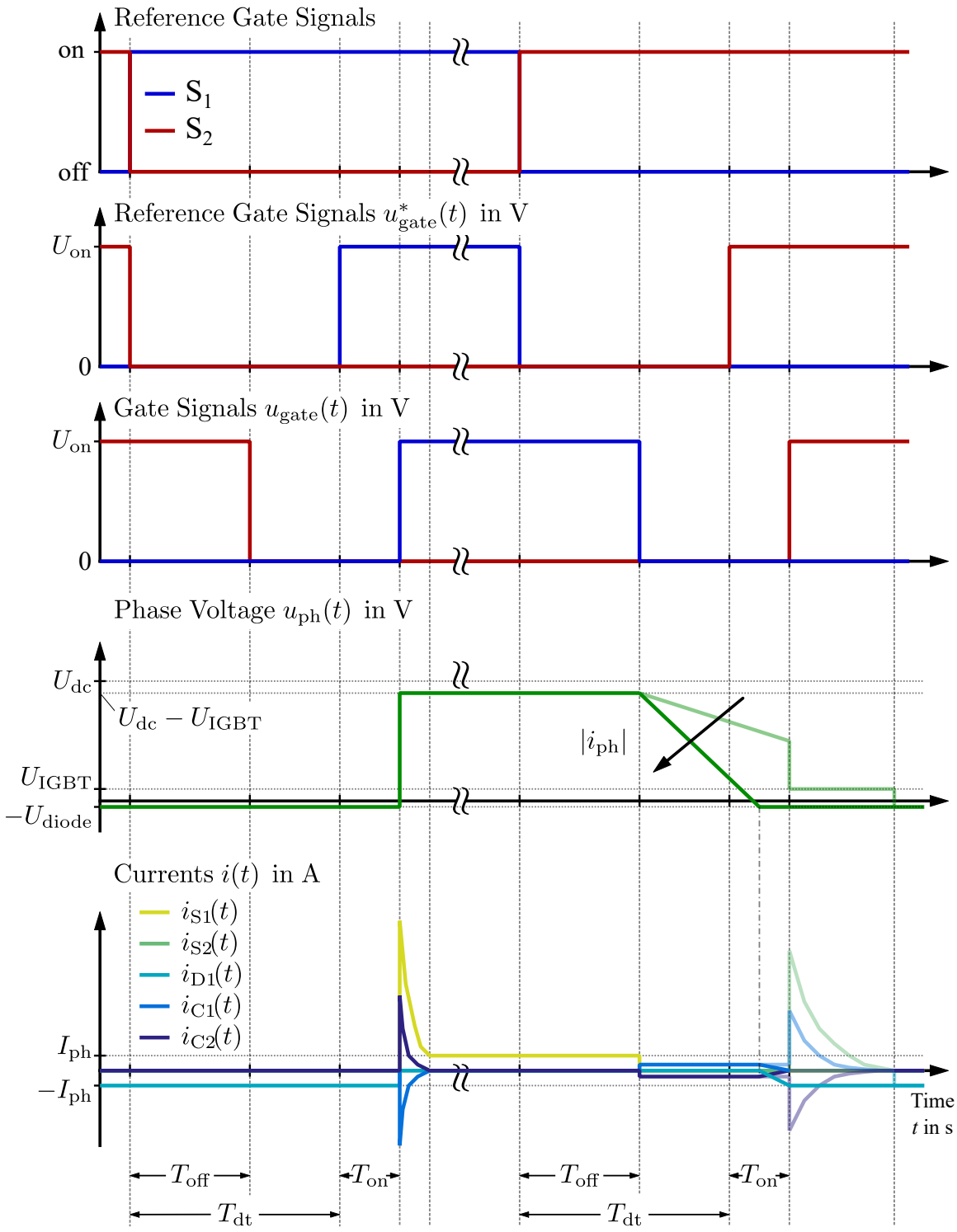


Figure A.3: Volt-second error for positive current I_{ph} (cf. [54])

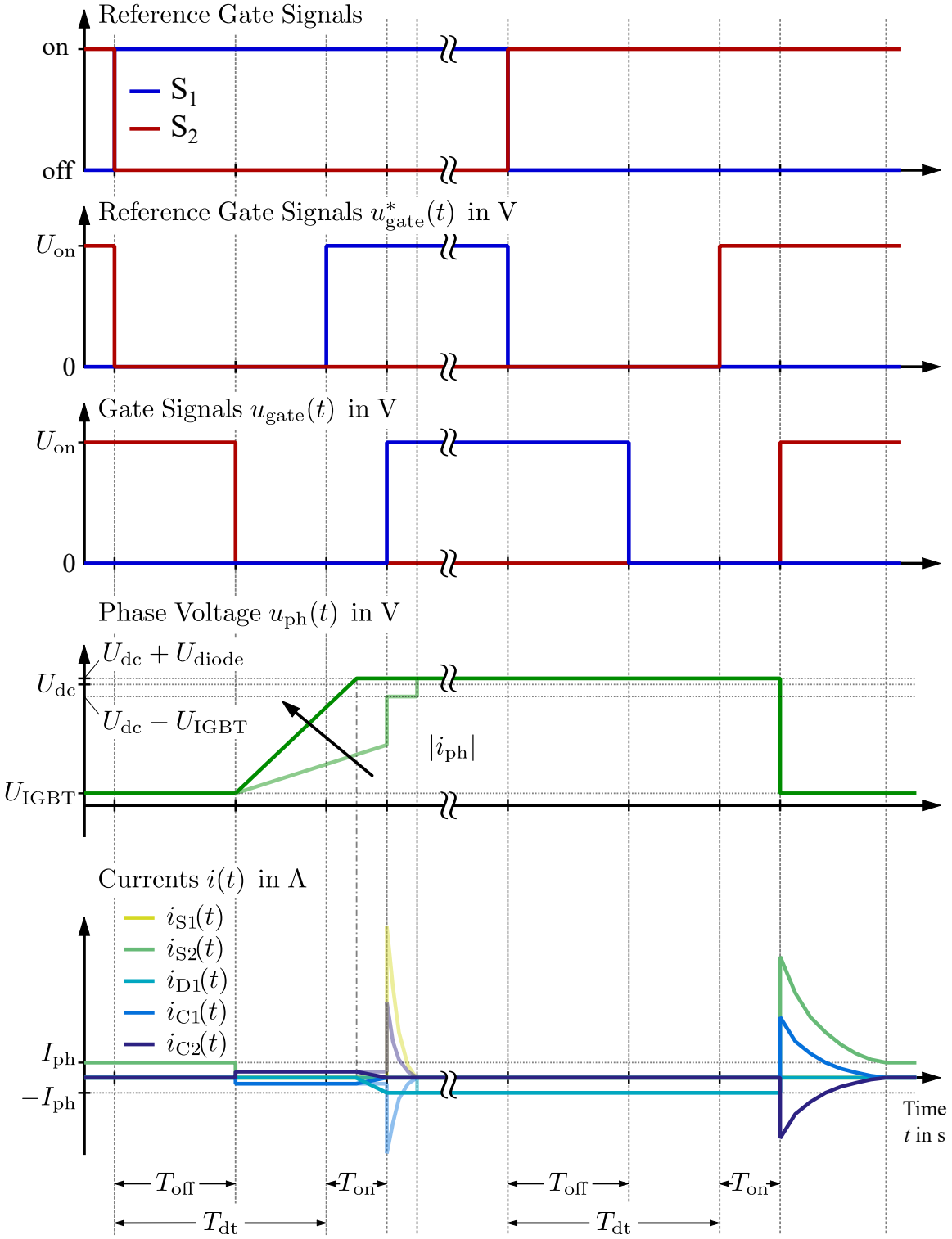


Figure A.4: Volt-second error for negative current I_{ph} (cf. [54])

A.2 Implementation Details and Schematics of dSVFC

A.2.1 Conceptualization of dSVFC

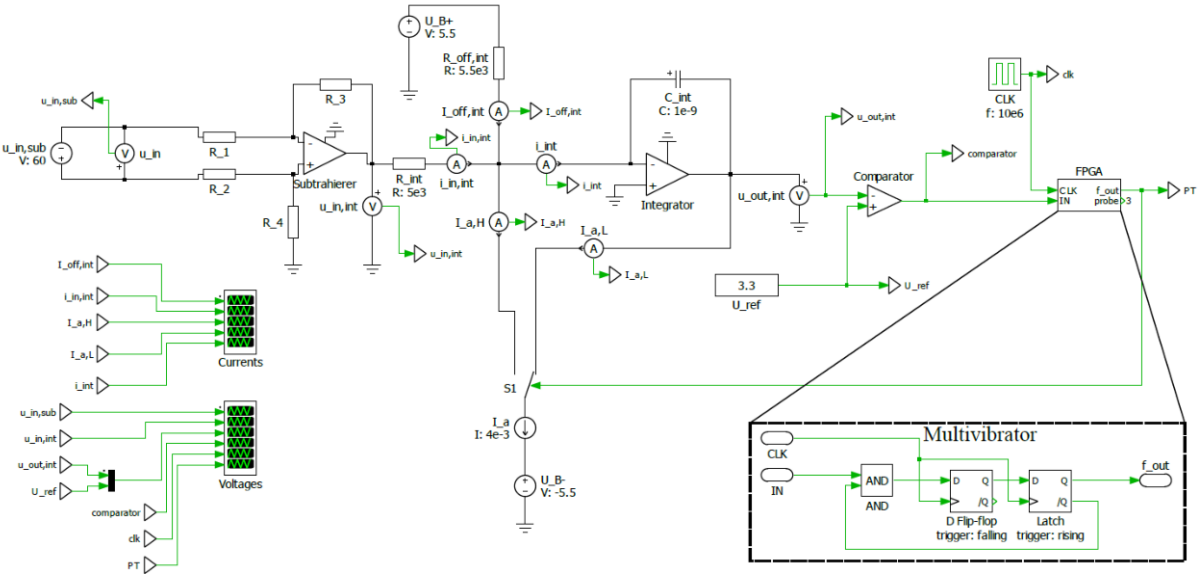


Figure A.5: Signal flow of dSVFC for PLECS simulation

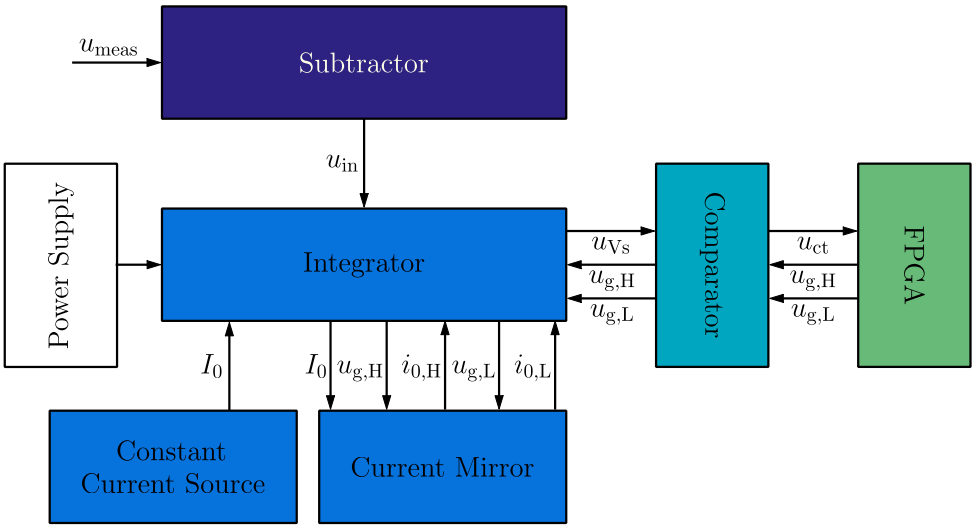


Figure A.6: Concept and signal transmission of modular dSVFC

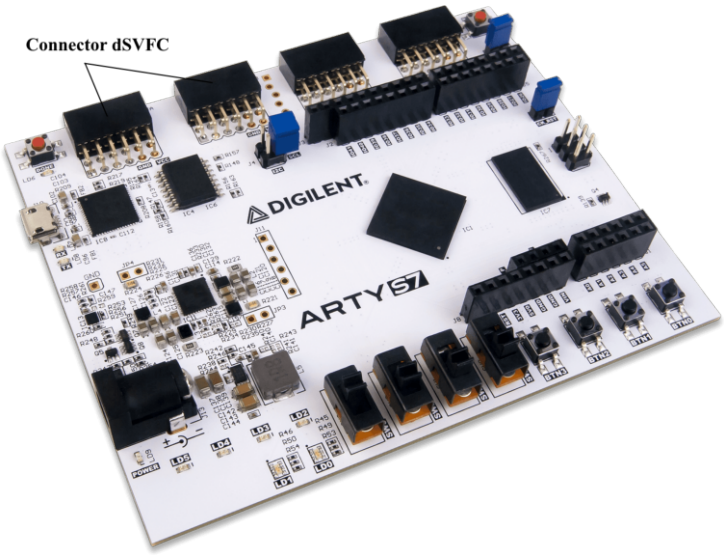


Figure A.7: Arty S7: Spartan-7 FPGA Development Board [109]

A.2.2 Schematics of dSVFC

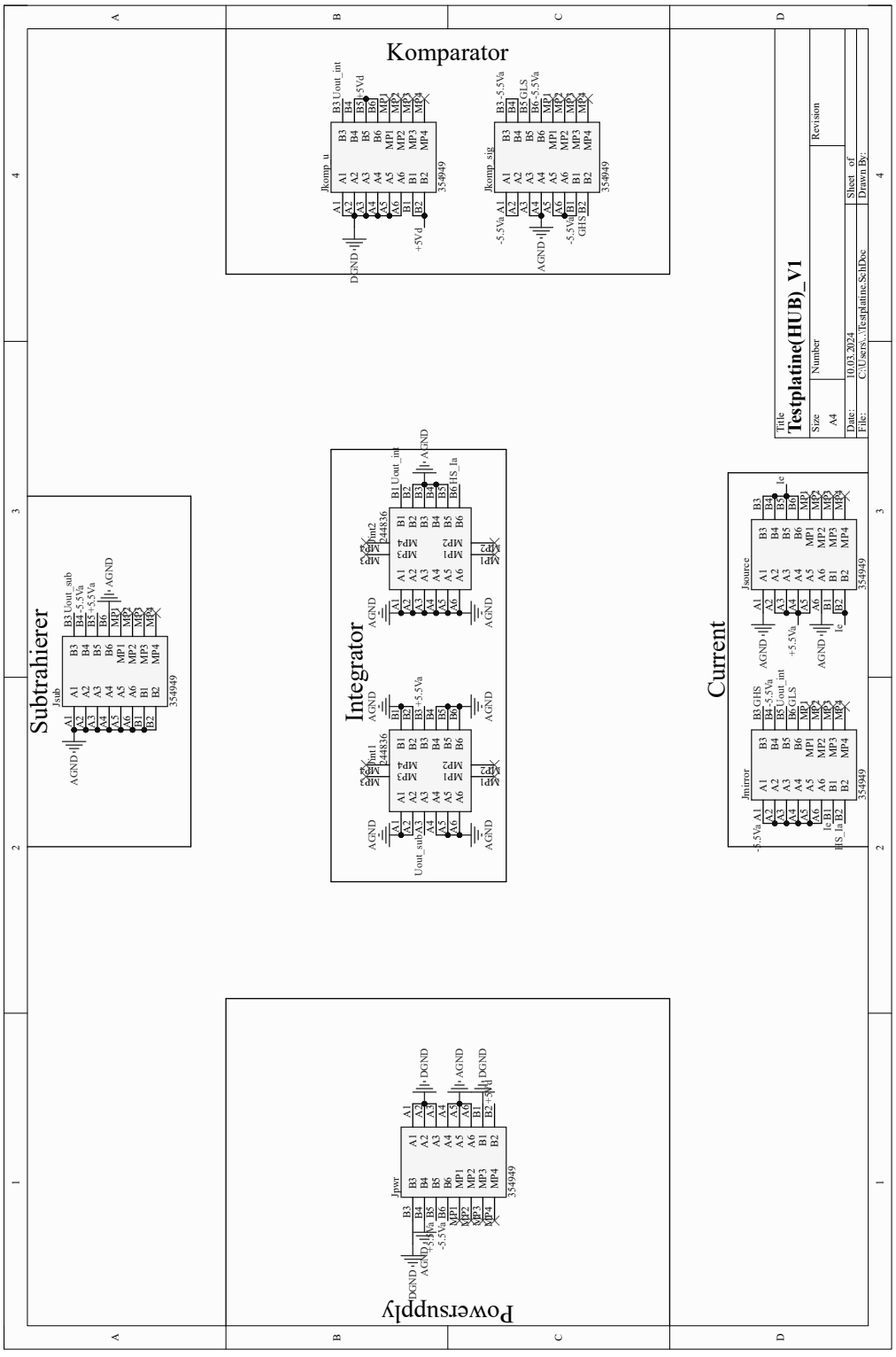


Figure A.8: Schematics modular dSVFC: connectors hub

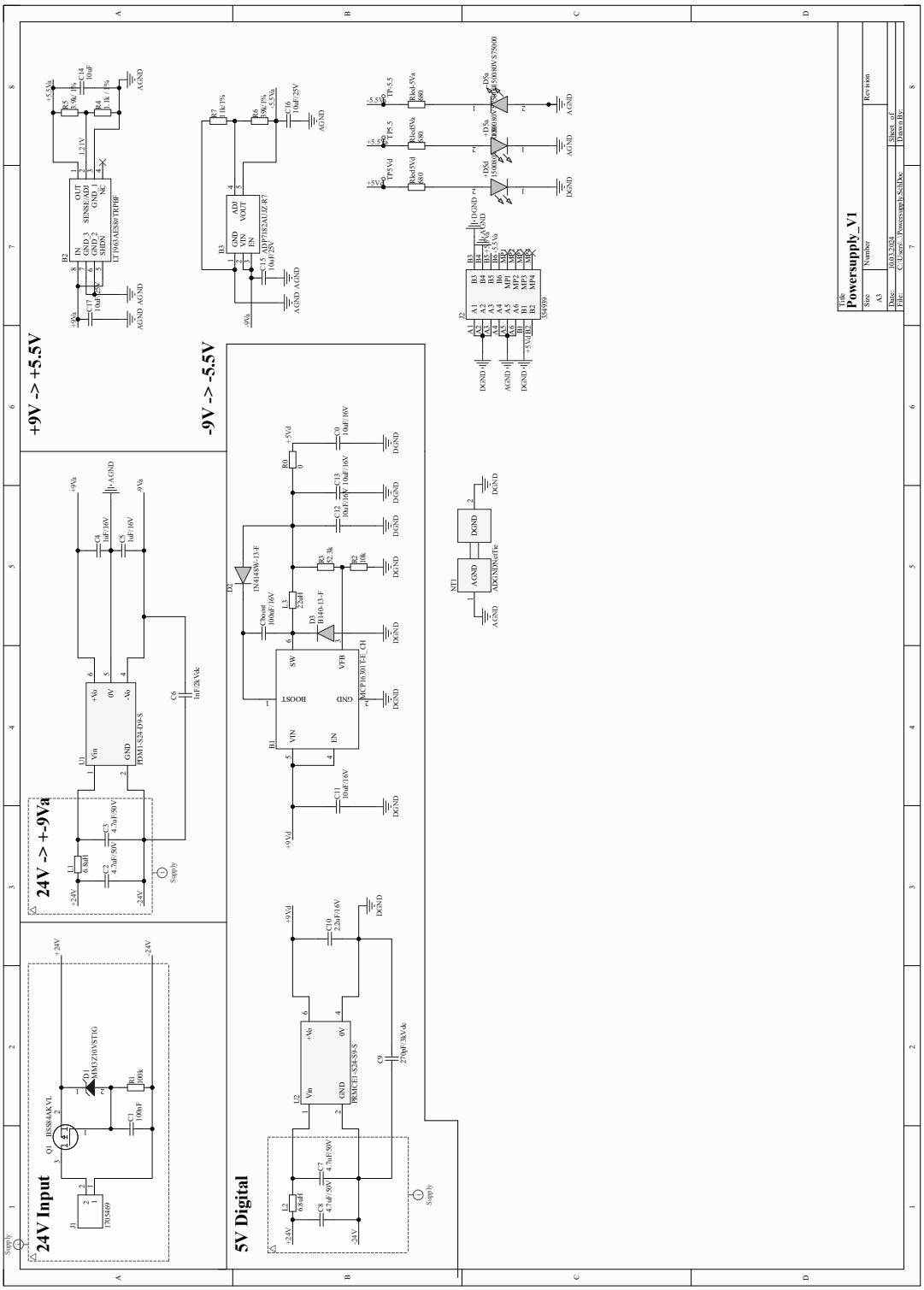


Figure A.9: Schematics modular dSVFC: power supply

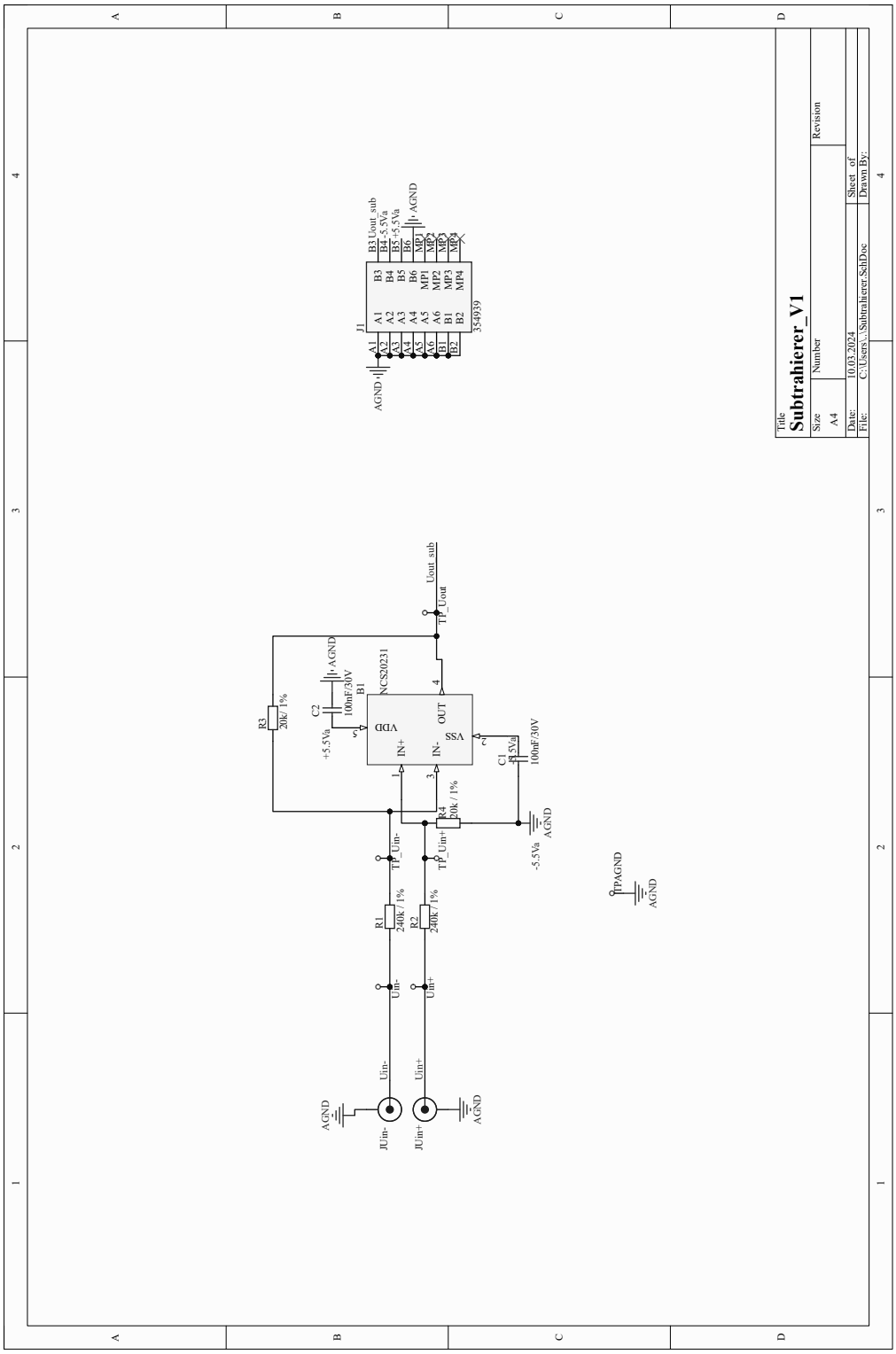


Figure A.10: Schematics modular dSVFC: substractor

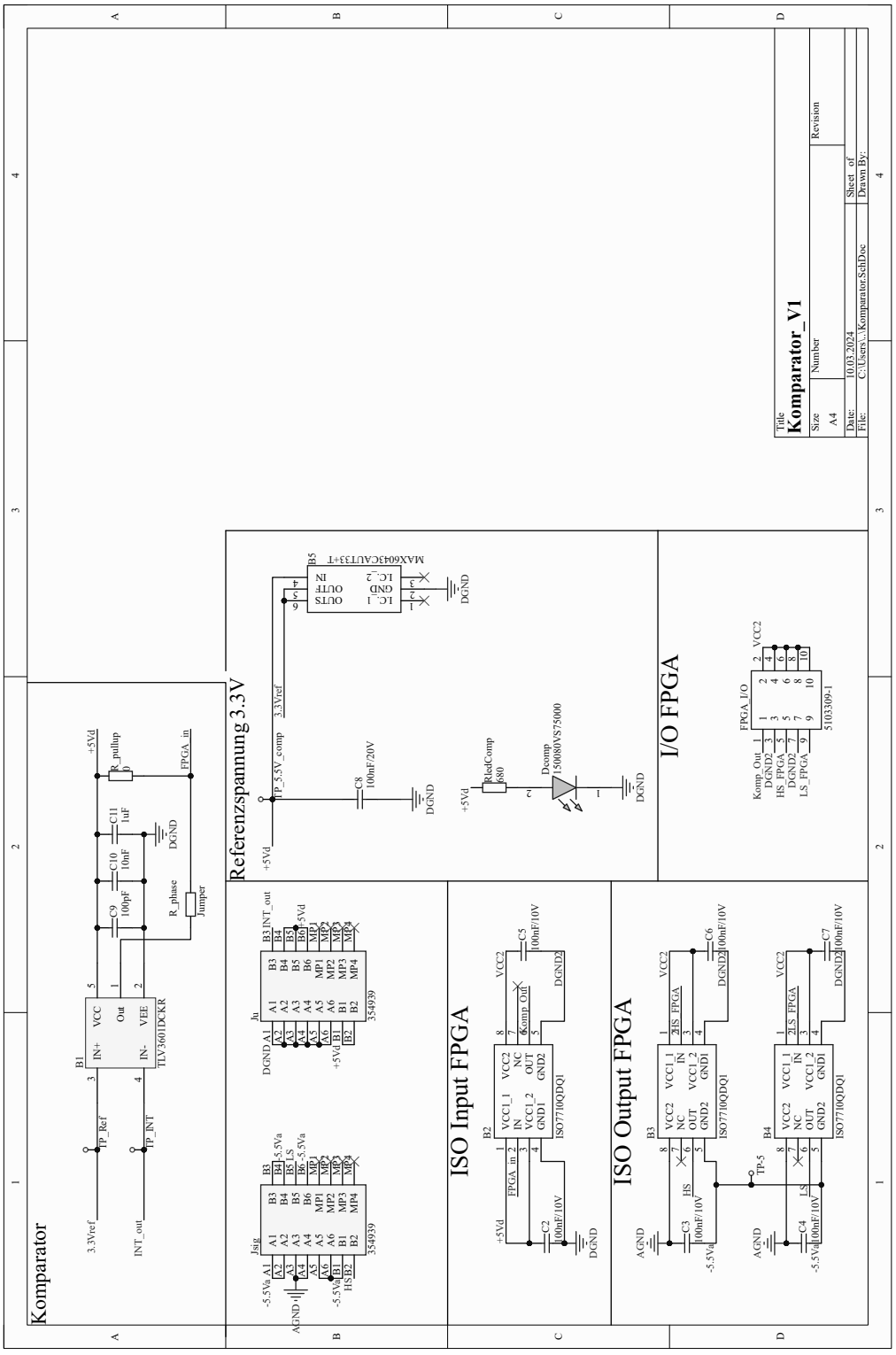


Figure A.11: Schematics modular dSVFC: comparator

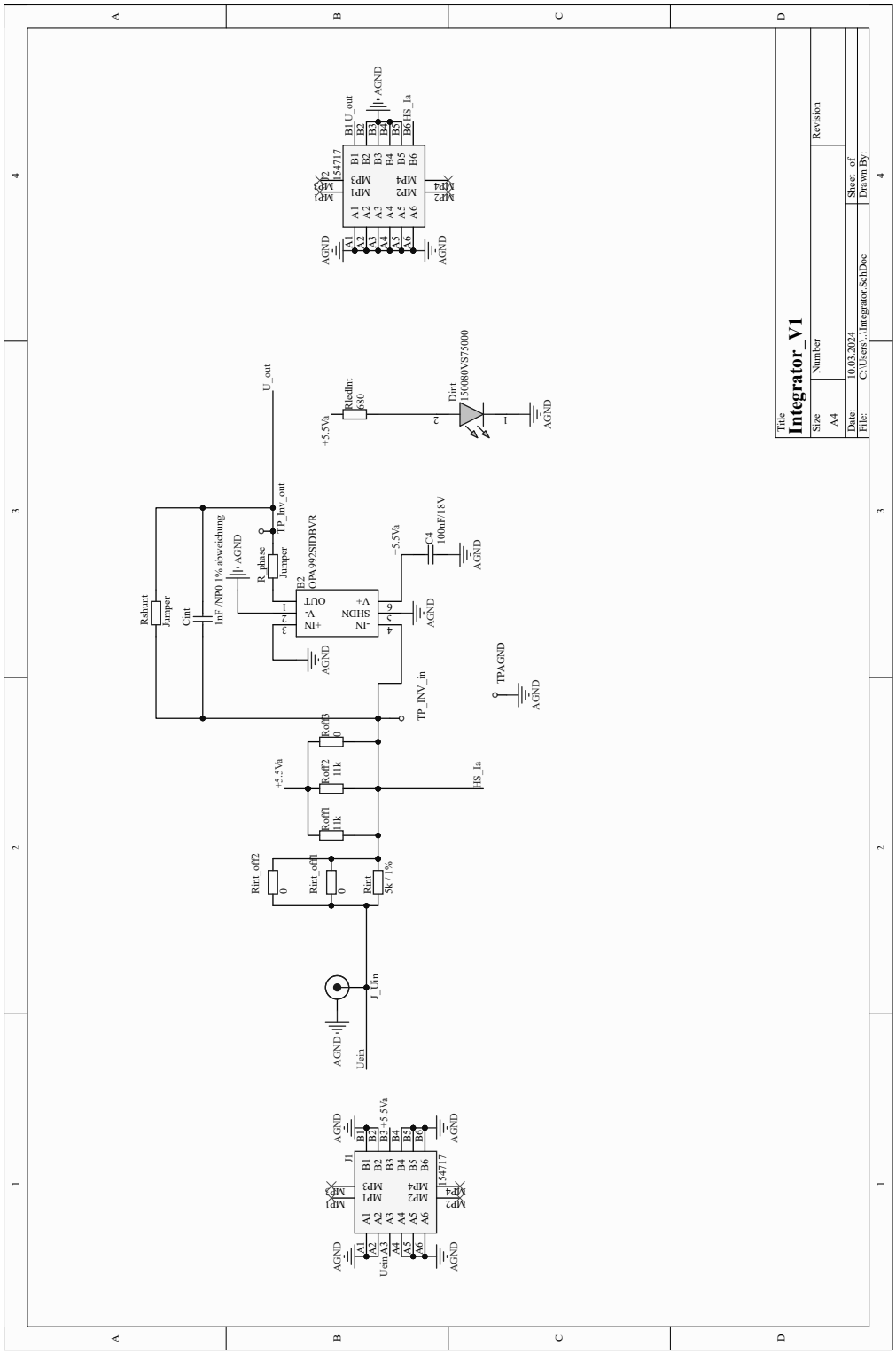


Figure A.12: Schematics modular dSVFC: integrator

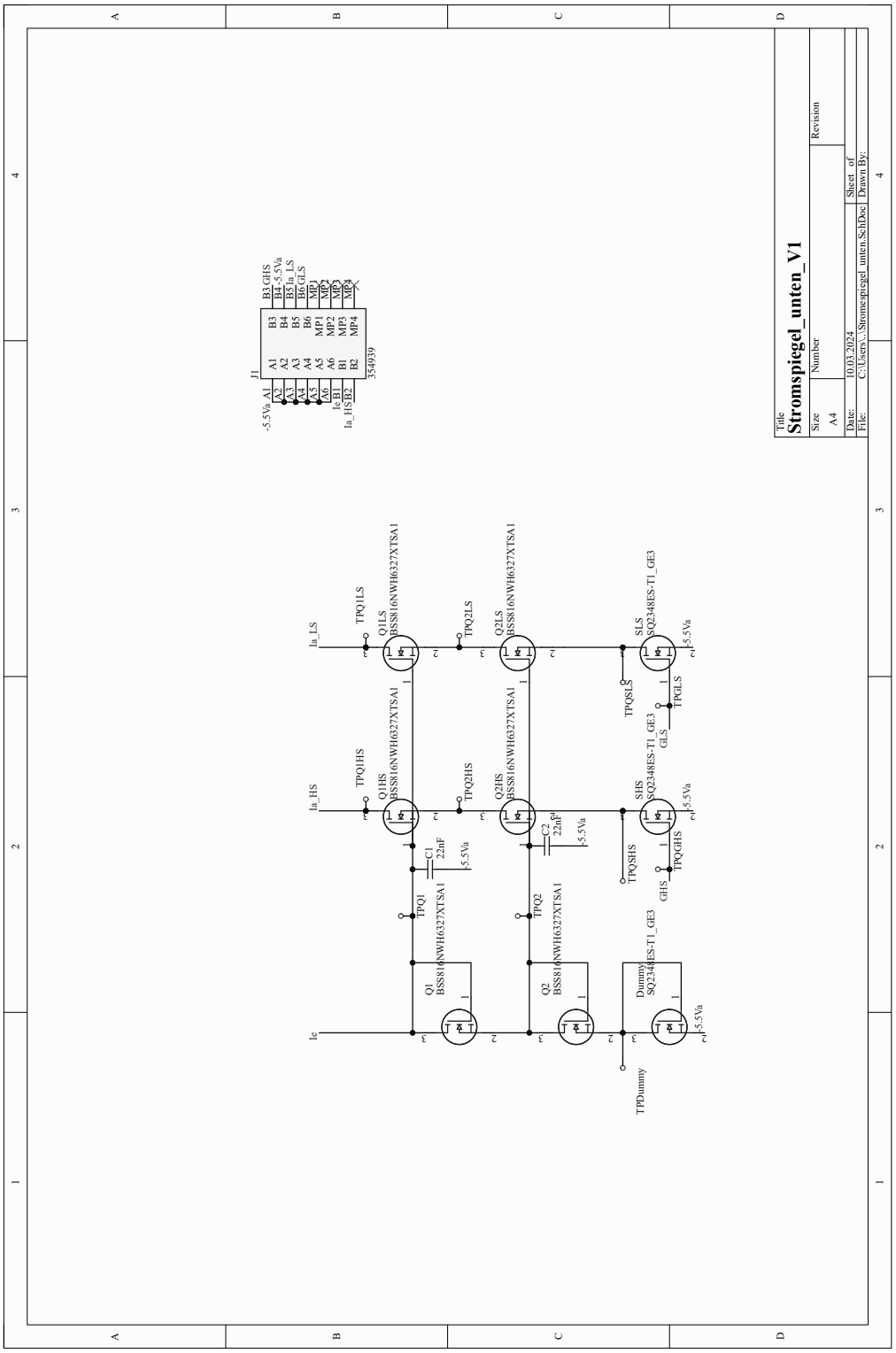


Figure A.13: Schematics modular dSVFC: current mirror, switches below

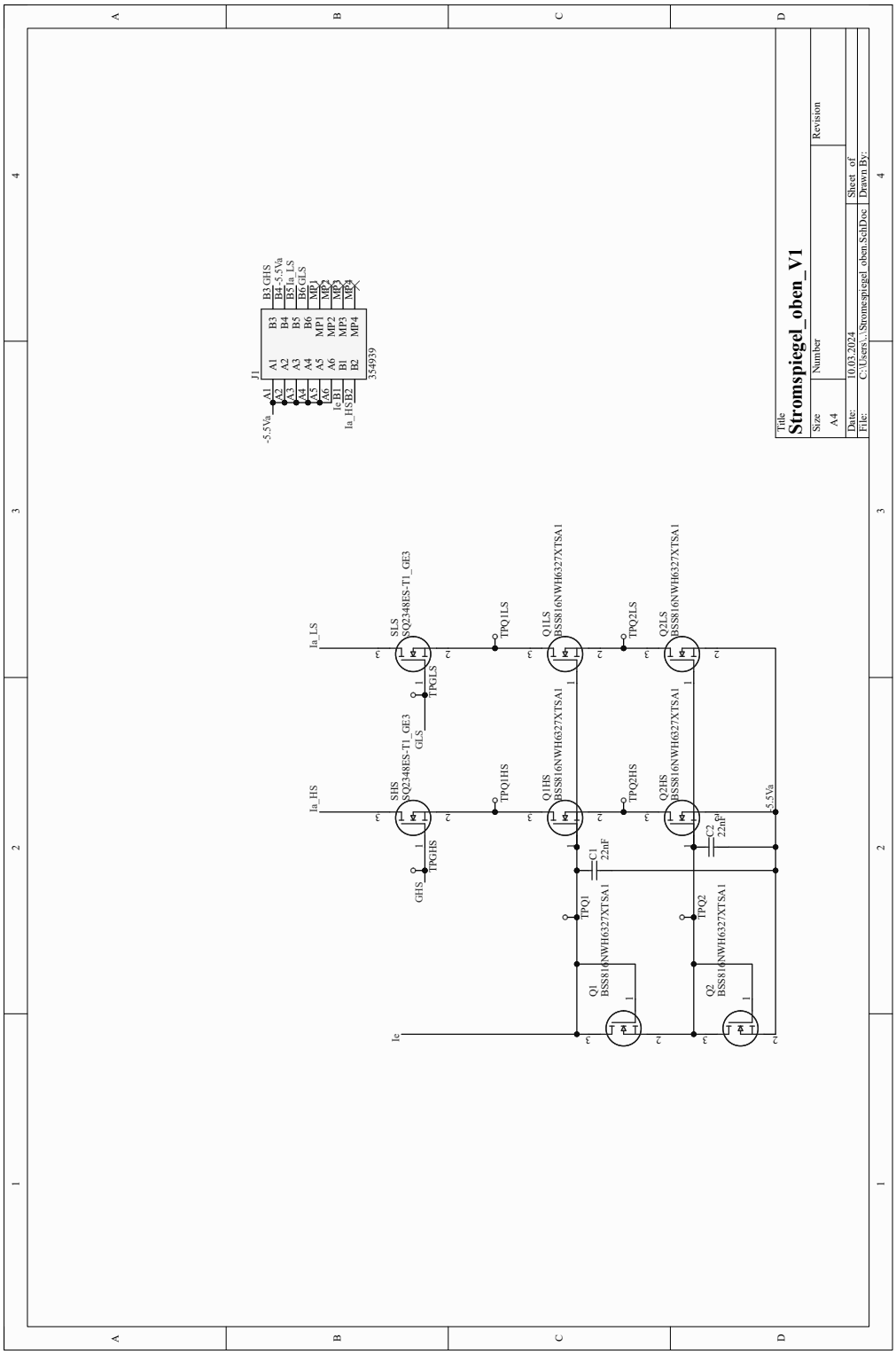


Figure A.14: Schematics modular dSVFC: current mirror, switches top

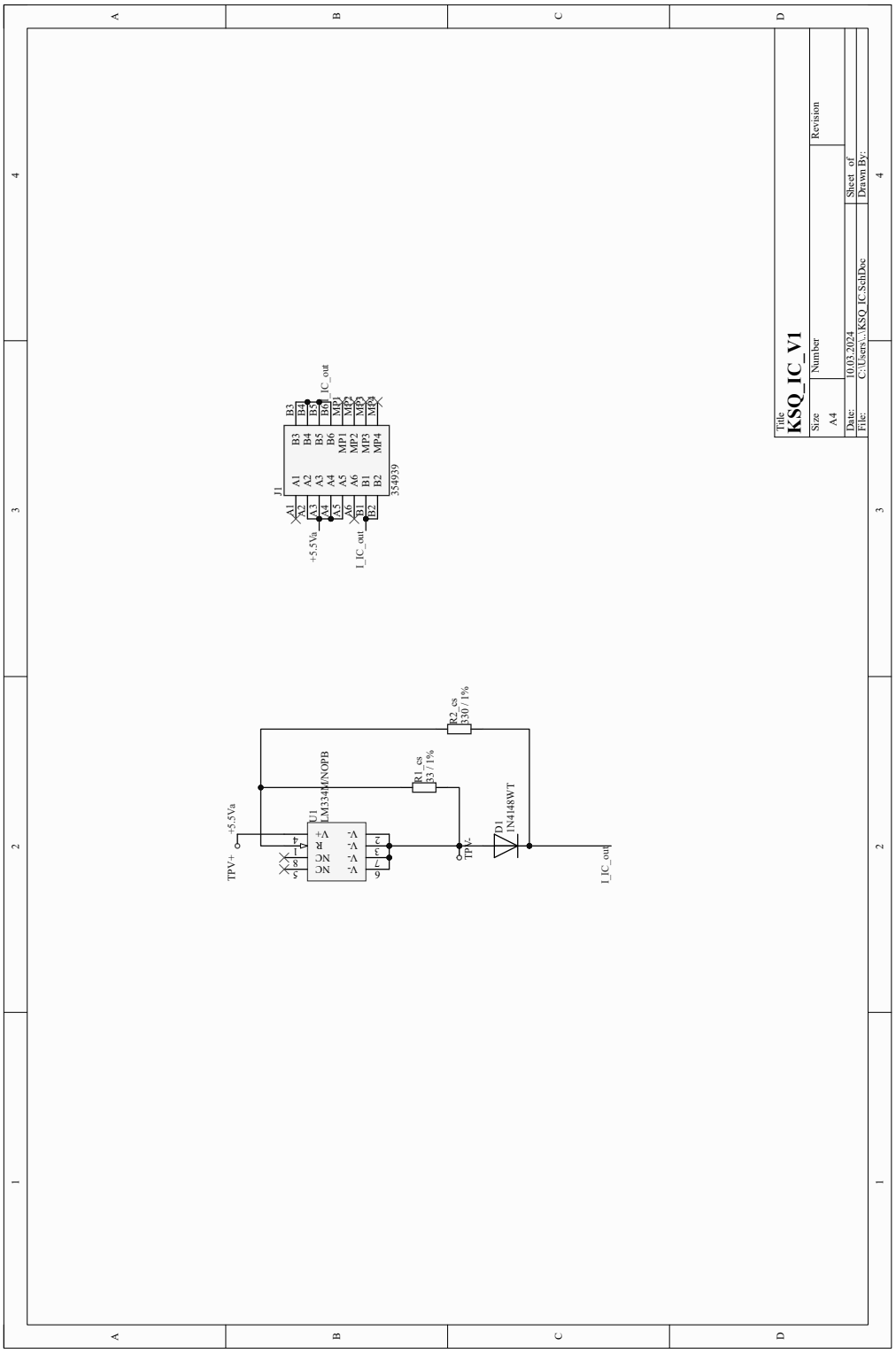


Figure A.15: Schematics modular dSVFC: constant current source, IC

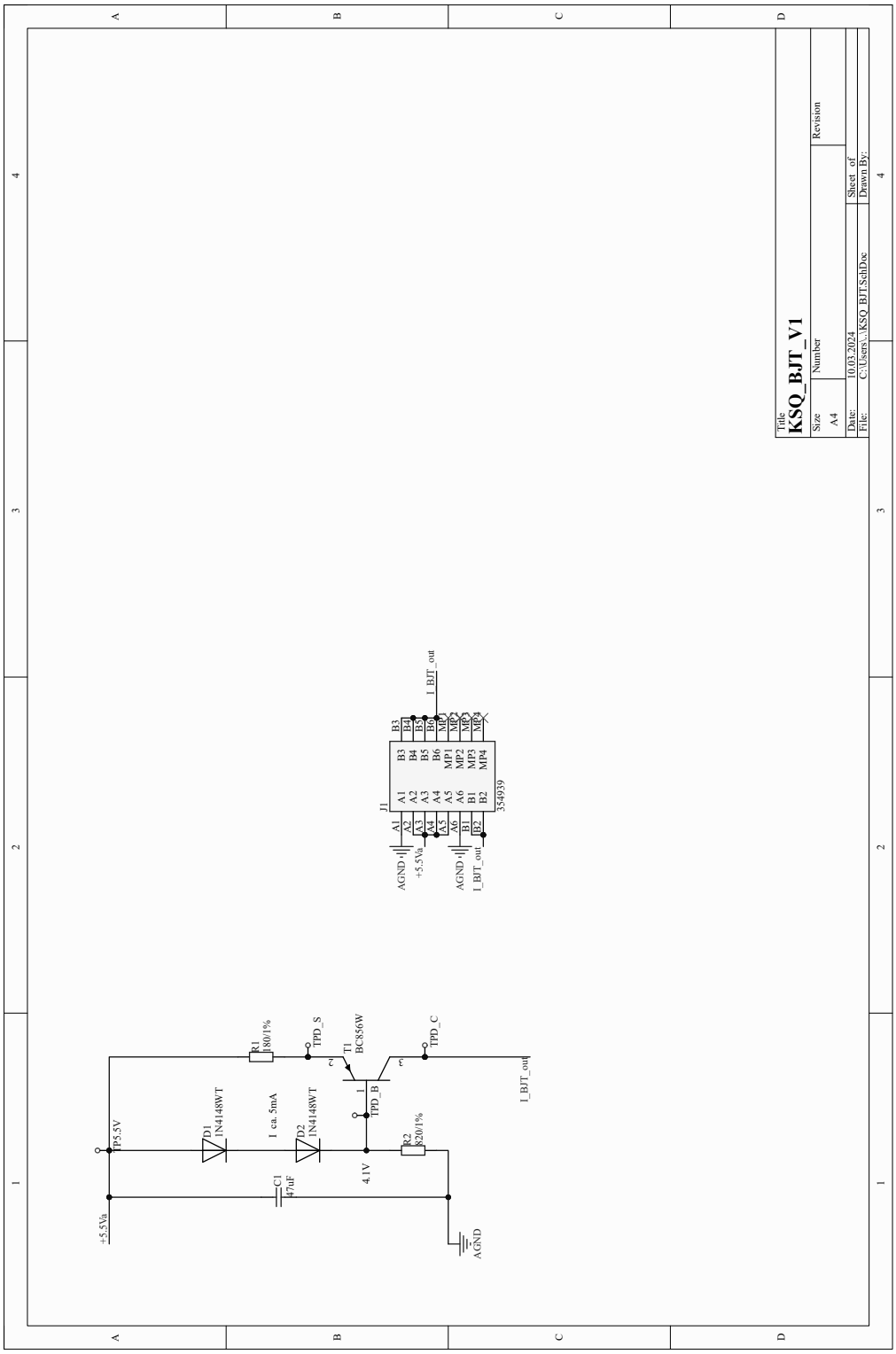


Figure A.16: Schematics modular dSVFC: constant current source, discrete

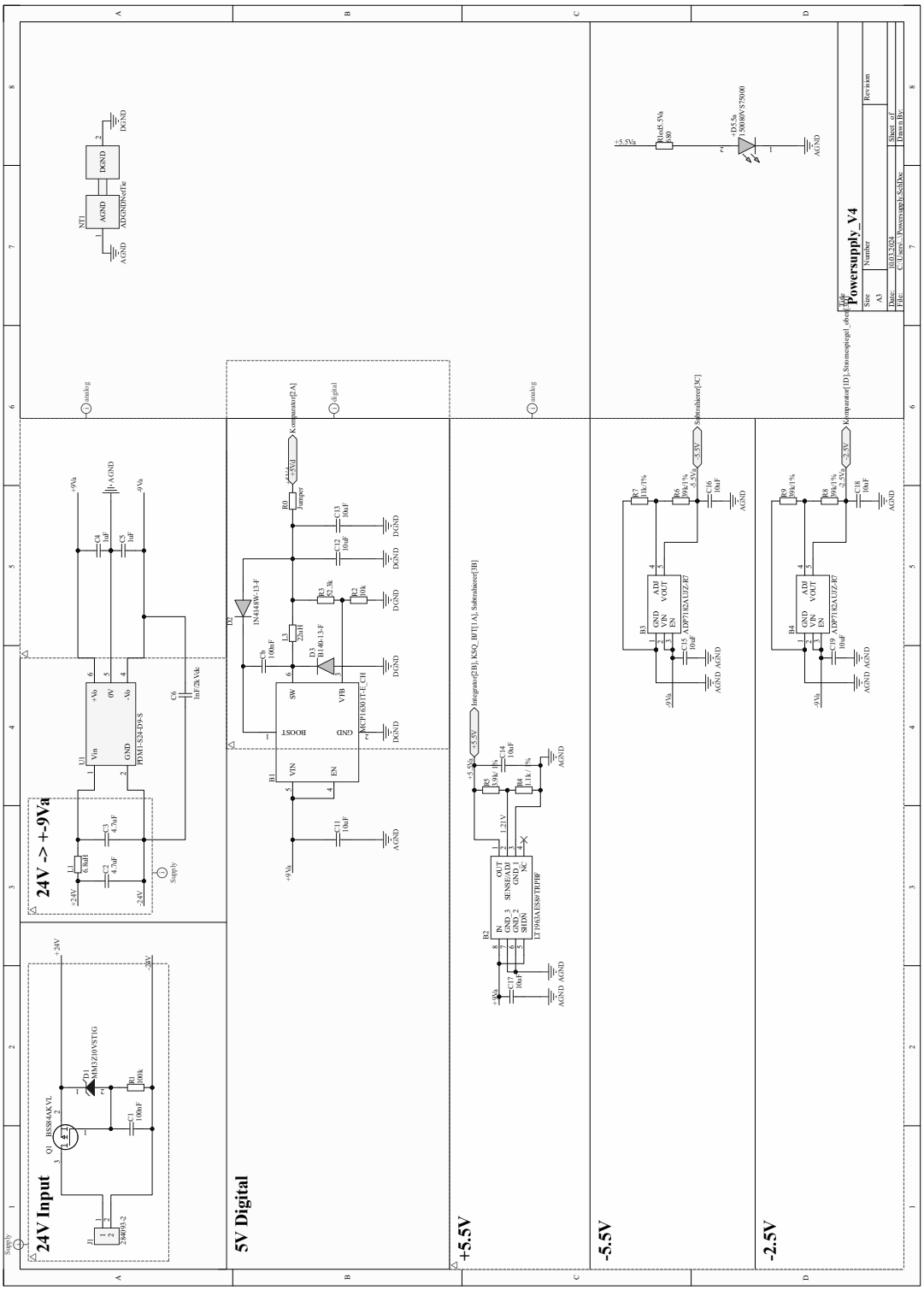


Figure A.17: Schematics dSVFC sensor: power supply

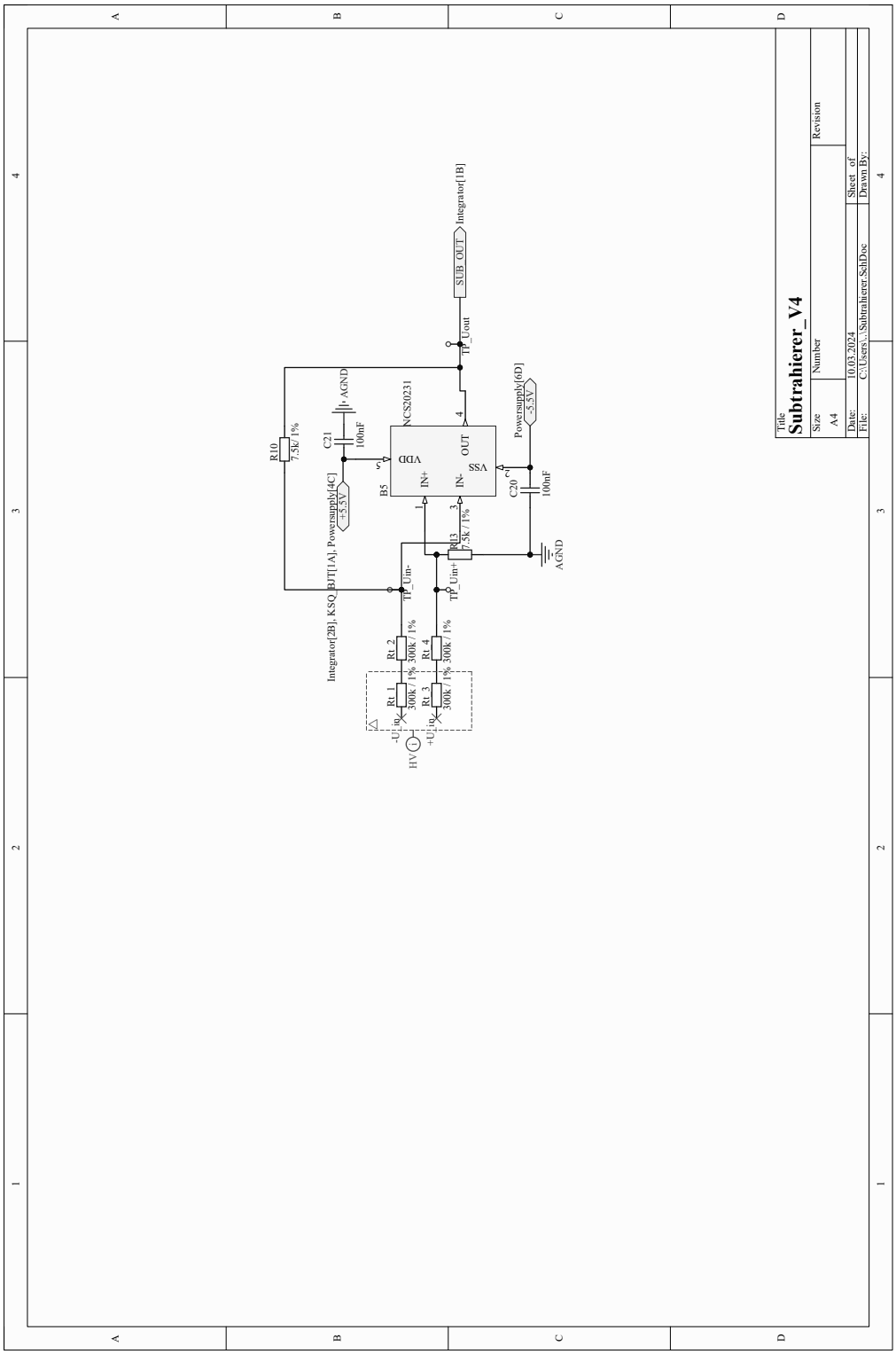


Figure A.18: Schematics dSVFC sensor: subtractor

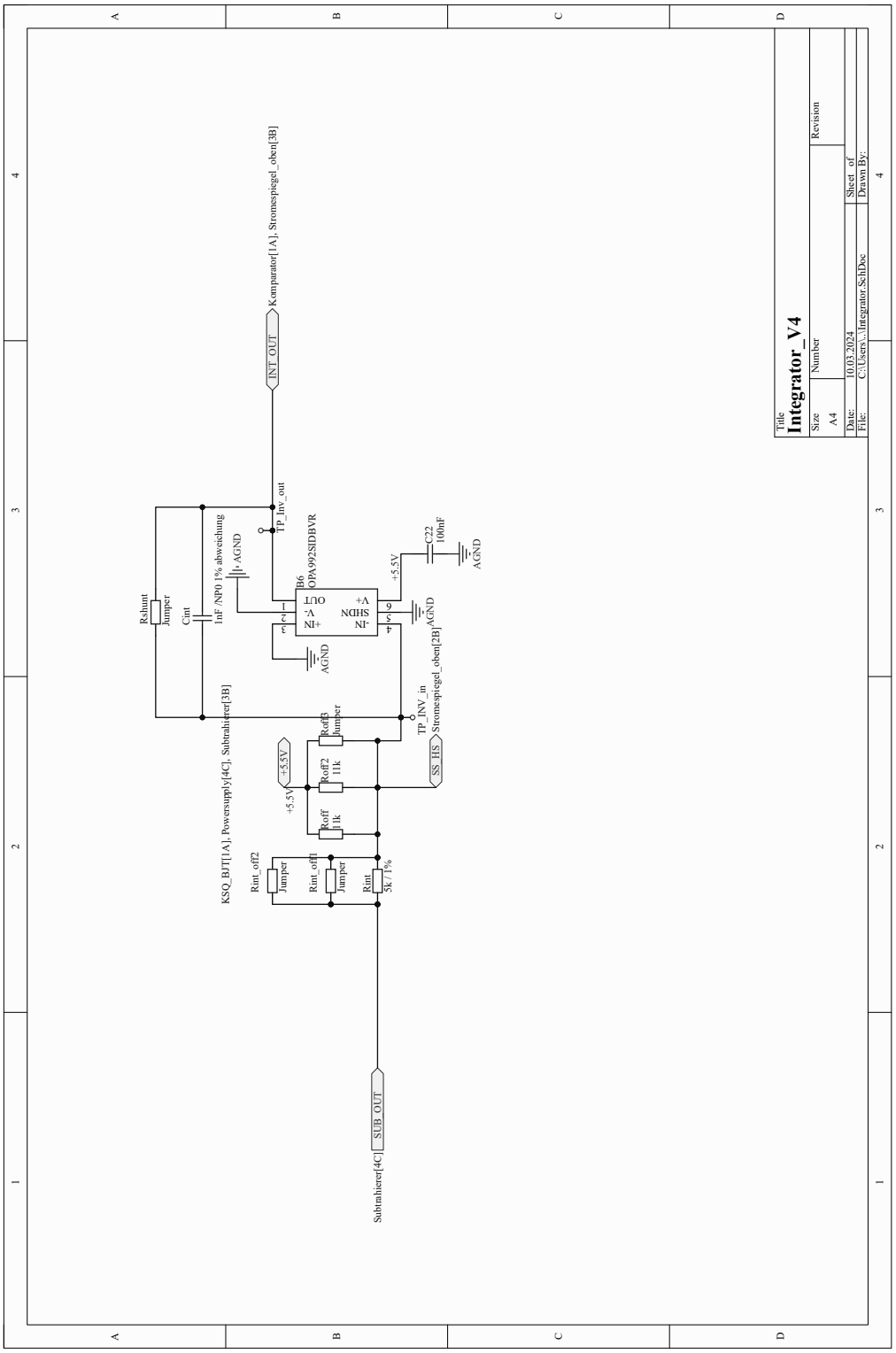


Figure A.19: Schematics dSVFC sensor: integrator

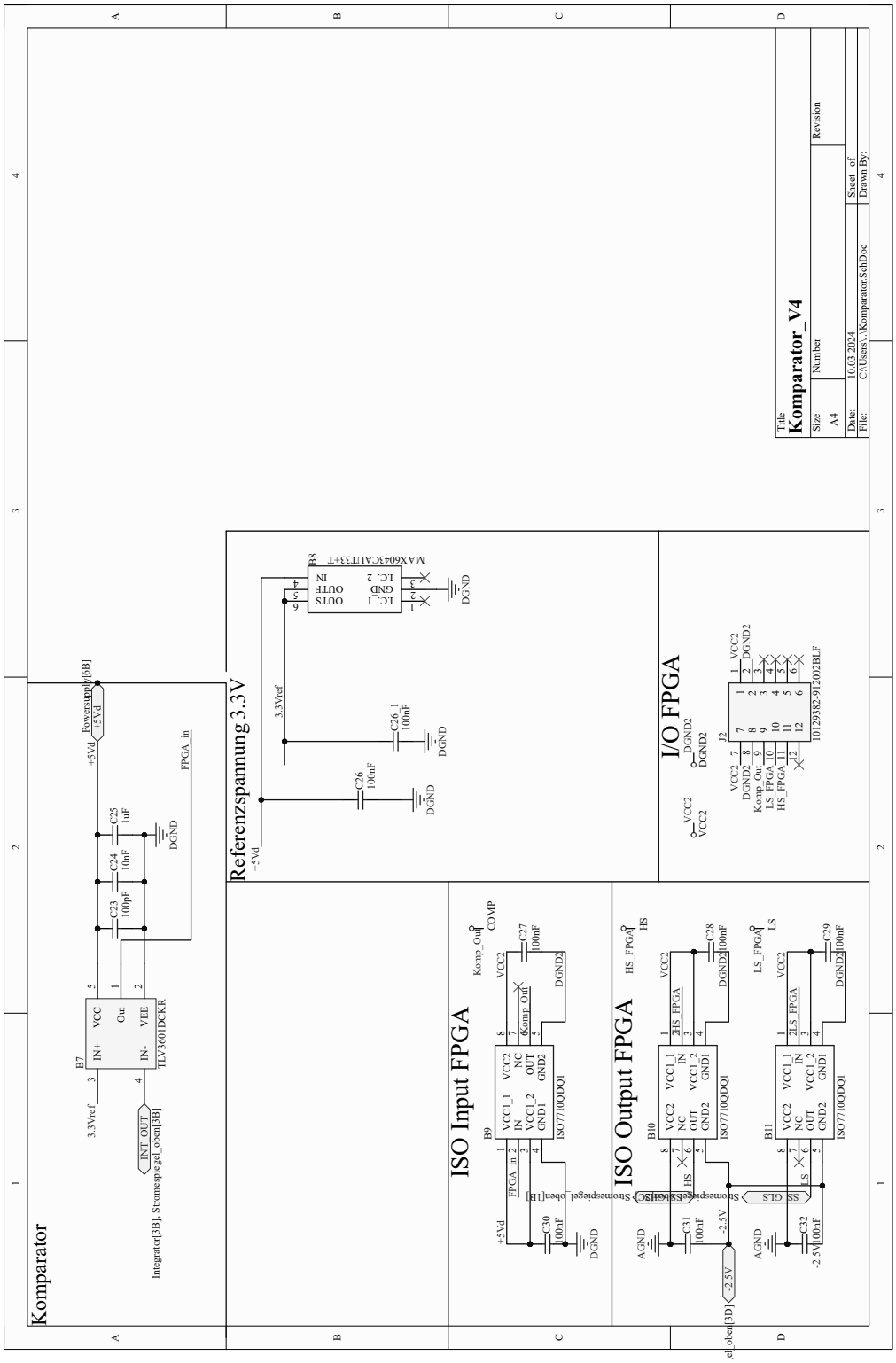


Figure A.20: Schematics dSVFC sensor: comparator

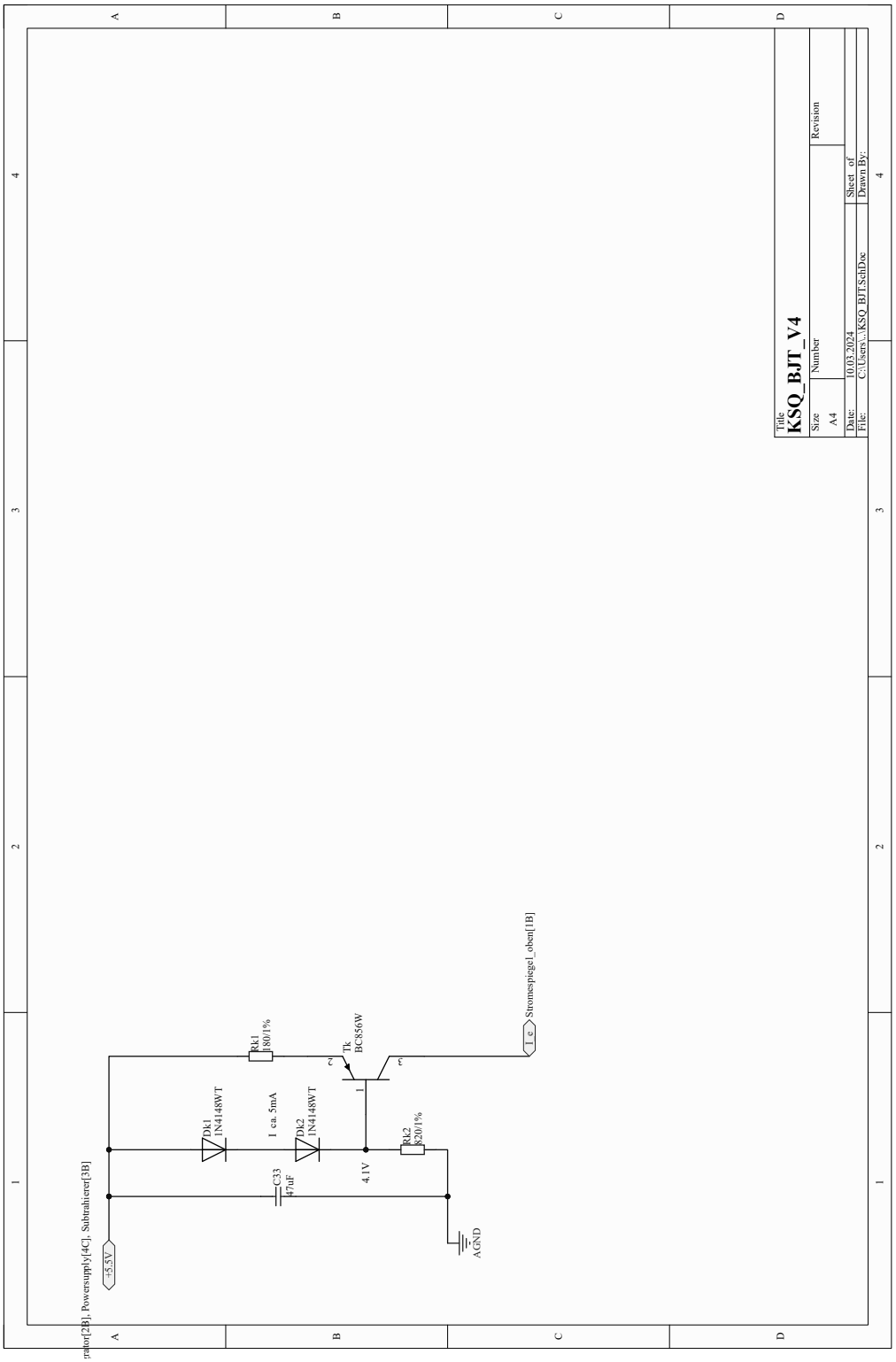


Figure A.21: Schematics dSVFC sensor: constant current source

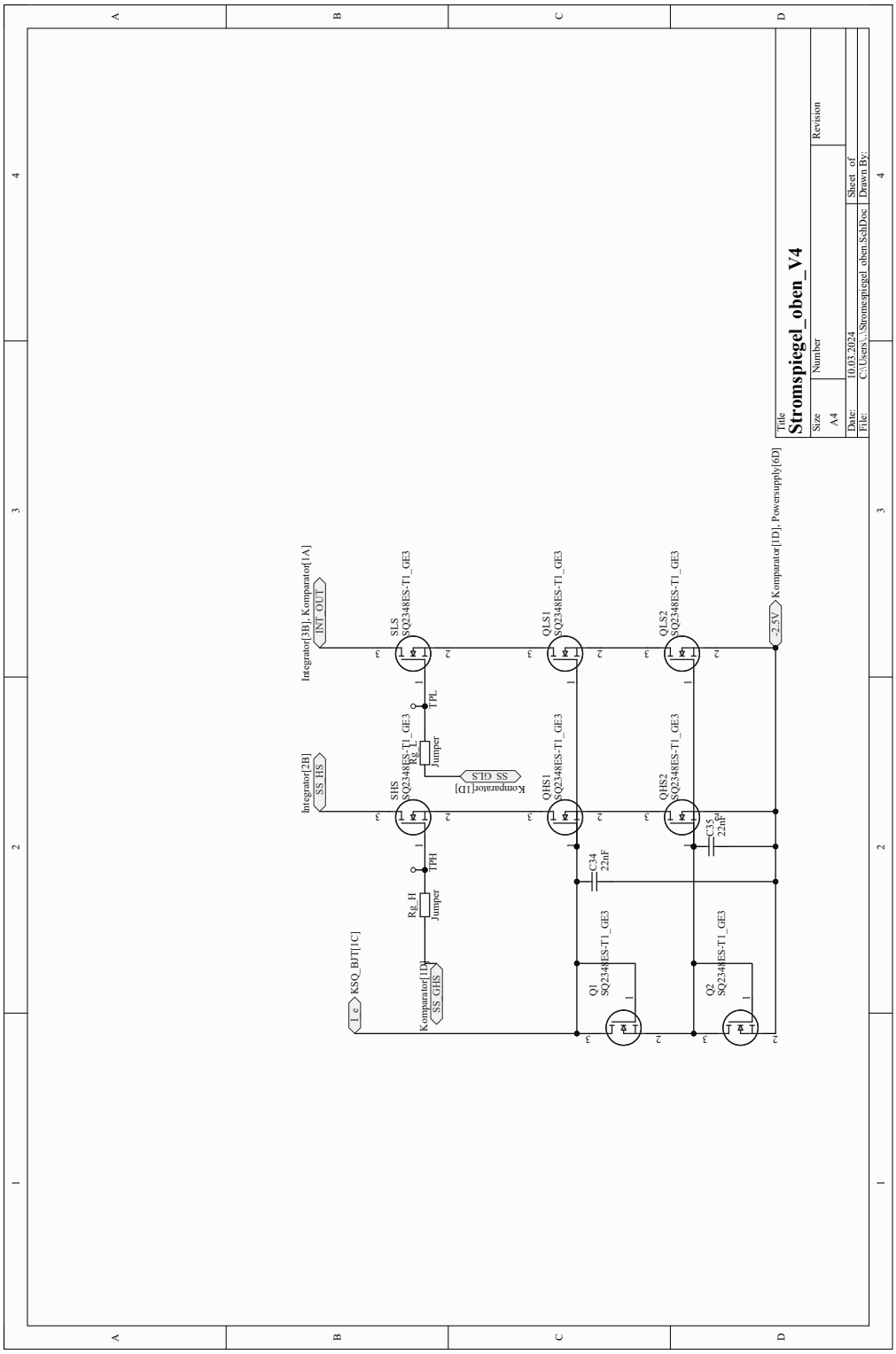


Figure A.22: Schematics dSVFC sensor: current mirror

A.3 Supplementary Description of Test Bench

A.3.1 Signal Processing of RCP System

A more detailed explanation of the entire RCP-system for the signals shown in Fig. A.24 is given in [113]. An overview and supplementary summary of the RCP-system can be found in the following lines.
SPI communication is parameterized for ADCs and the LEM current transducer with a delay and a channel select signal `ch_sel`. The delay variable denotes the dynamically adjustable length of a delay chain, which serves to synchronize internal communication signals with physical hardware components. This synchronization is achieved in discrete increments equivalent to the FPGA clock period, specifically 10 ns, within the FPGA architecture. For the 12 bit ADC, a delay value of 25 is determined to ensure optimal communication timing and accurate SPI word interpretation. Conversely, for the 14 bit ADC and the current sensor, a delay of 17 was identified as appropriate. Channel selection is exclusively employed for the current sensor, primarily because the output from the LEM transducer is routed to channel 2 of the ADC responsible for its evaluation. Communication can also be enabled or disabled via the HMI through an enable signal. This precautionary measure is implemented to prevent potential adverse effects on alternative measurement methodologies, which do not necessitate SPI communication, from the 10 MHz digital clock signal.
Concerning the PWM module, solely the duty cycle d is required as an input parameter. Furthermore, reset and enable functionalities are also furnished via dedicated input signals. The VFC edge detection threshold and delay constitute critical parameters for the edge detection mechanism within the AVFC pulse counting and time sensing measurement technique. The former is configured to $150 \cdot T_{\mathrm{clk}}$ of the FPGA, while the latter is established at $300 \cdot T_{\mathrm{clk}}$. Assuming a left-aligned PWM scheme for the AVFC pulse counting and time sensing methodology, with the objective of maximizing the coherent high and low level durations of the PWM voltage, a substantial temporal discrepancy persists between the rising edge of the gate signal (inclusive of dead time) and the actual PWM voltage output. To preclude erroneous triggering of the edge detection during this

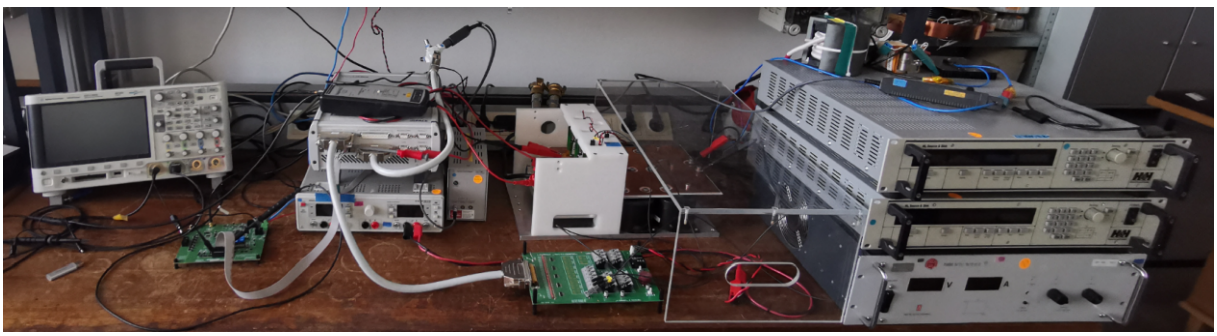


Figure A.23: Overview of measurement setup for various measurement approaches

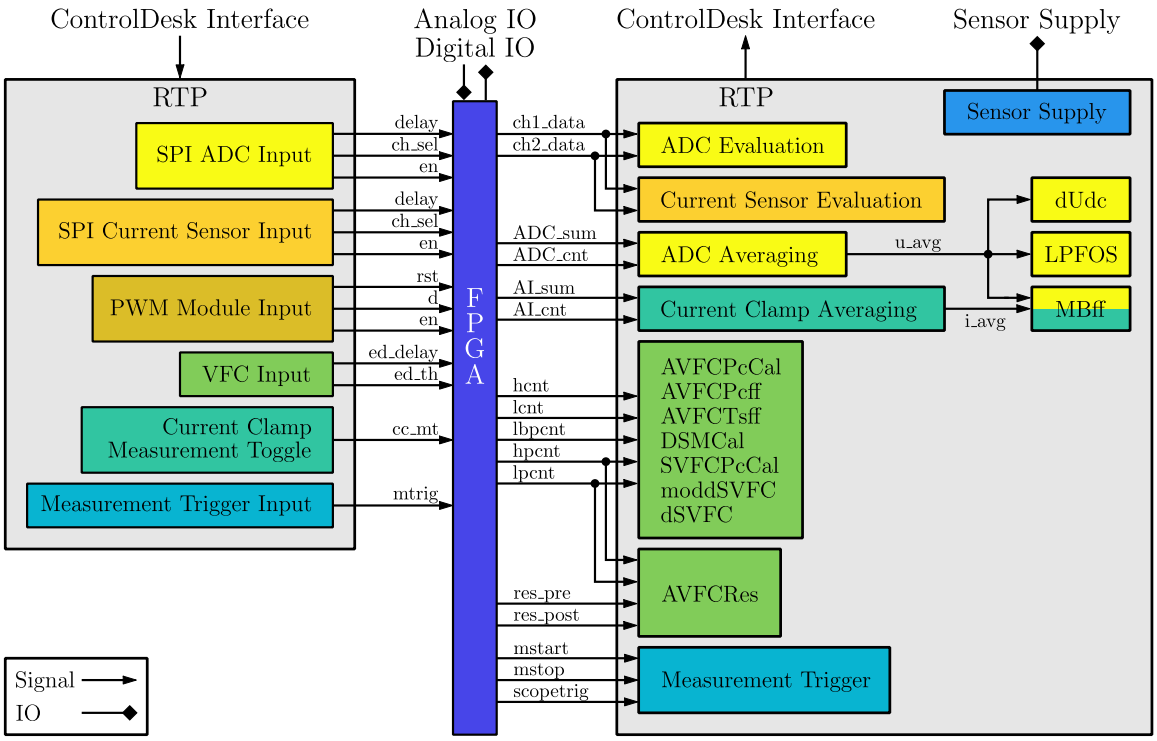


Figure A.24: Overview RTP level of RCP-system with all processing signals

interval, the delay parameter effectively deactivates the edge detection functionality for a predefined number of FPGA clock periods. Finally, a current clamp measurement toggle block relays an input from the HMI interface to alternate between continuous phase current measurement and precisely synchronized averaging pertinent to the MBFF control strategy. Continuous measurement is employed in conjunction with the demagnetization and consequent manual zero adjustment procedure to accurately calibrate the current clamp sensor.

As depicted on the right-hand side of A.24, FPGA output signals undergo subsequent processing by the RTP. ADC and current sensor evaluation blocks retrieve the interpreted SPI words, which are deposited into a shared register by the FPGA. While the comparatively slower cycle time of the RTP precludes the sampling of every interpreted SPI word, these blocks prove invaluable for debugging and fine-tuning functional delay parameters by providing instantaneous feedback. Averaging blocks for the ADCs and the current clamp fundamentally compute the arithmetic mean by dividing the aggregated measurement values by the total count of samples for each respective channel. These average values are subsequently supplied to the measurement evaluation blocks.

The sensor supply represents the sole hardware input/output (IO) related parameter managed at the RTP level. A comprehensive description of the measurement trigger input functionality was provided in Section 4.2.3, as its comprehension necessitates an understanding of both the RCP-system and software architectural levels. In the following, the FPGA-level details, as presented in A.25, will be expounded upon.

One SPI communication frame comprises 20 SPI clock cycles. To accommodate this, the SPI master block is appropriately configured to conform to the timing specifications stipulated in the corresponding datasheets for both the 12 bit and 14 bit ADC. PWM module inputs from the RTP are augmented by the `app_status` signal, which serves to deactivate switching signal outputs should the application executing on the RTP cease operation. Such an event may occur, for instance, if RTP constraints are violated, thereby entirely suspending RTP operation. Consequently, as a precautionary safety measure, switching signal outputs are inhibited. A center-aligned switching signal, denoted as s, inclusive of dead time, is generated by the PWM module for each of the three phases. Given that the current measurement configuration employs only a single half-bridge, the switching signal is demultiplexed into the distinct phases, and the IOs designated for top and bottom gate control are written to their corresponding IO channels.
The current clamp and ADC averaging units exhibit identical operational principles, hence the similar nomenclature for their output signals. ADC values are accumulated synchronously upon the assertion of the new data signal, in parallel with a counter that tracks the total number of rising edges of the new data signal. This process continues until the PWM trigger resets the accumulation and latches the sum and counter into a register for retrieval by the RTP. For the current clamp, the accumulated input is directly read from an analog IO channel of the MicroLabBox, while the reset and latch trigger is specifically designed to execute the measurement exclusively within the dead time constraints, when current commutates to a diode. This particular timing is essential for the voltage-distortion MBFF measurement technique. Since the current clamp value lacks a new data signal, it is accumulated continuously using sufficiently large registers to accommodate the extensive sample count. Lastly, the current clamp measurement toggle is capable of overriding the reset trigger, utilizing a multiplexer to favor a constant true signal for the previously described calibration of the current clamp.

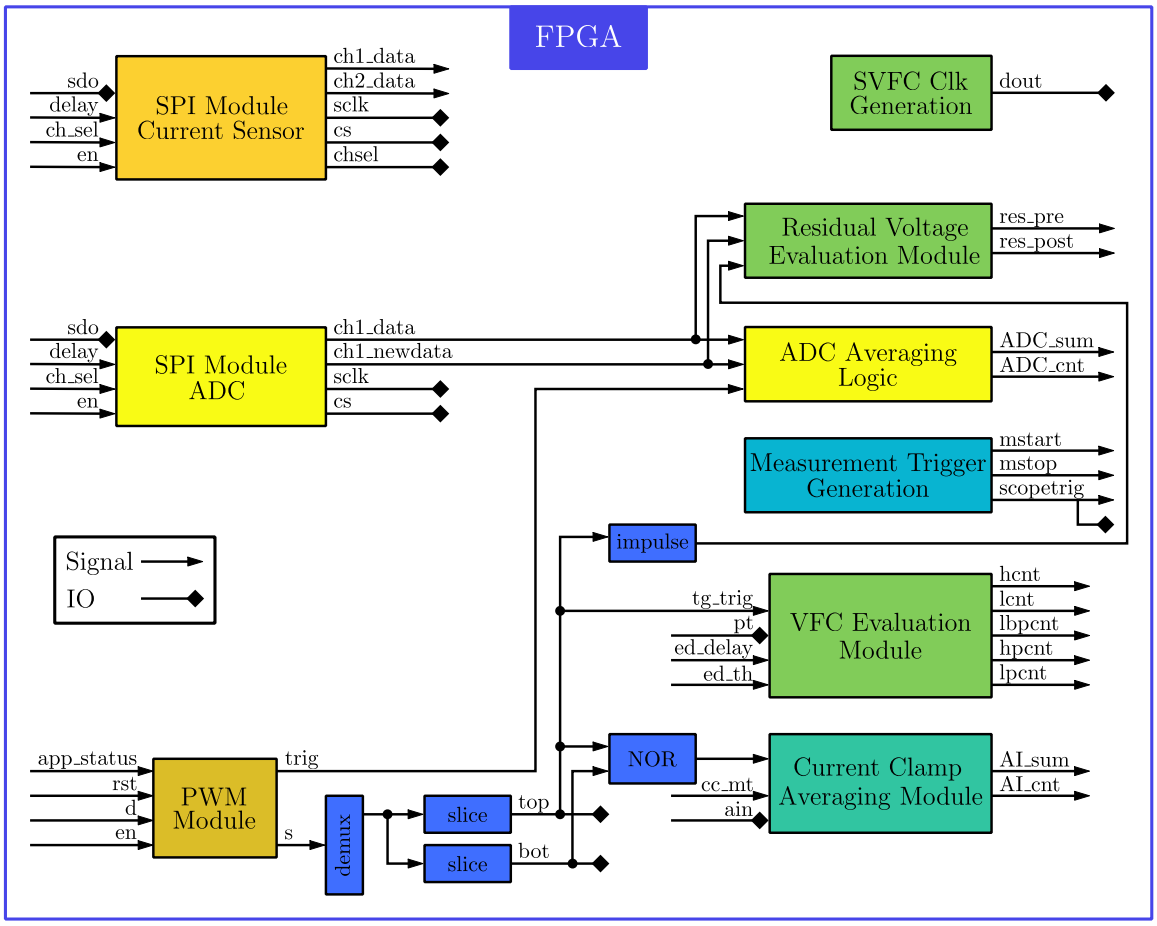


Figure A.25: Overview FPGA level of RCP-system with all processing signals

A.3.2 Schematics of Measurement Board

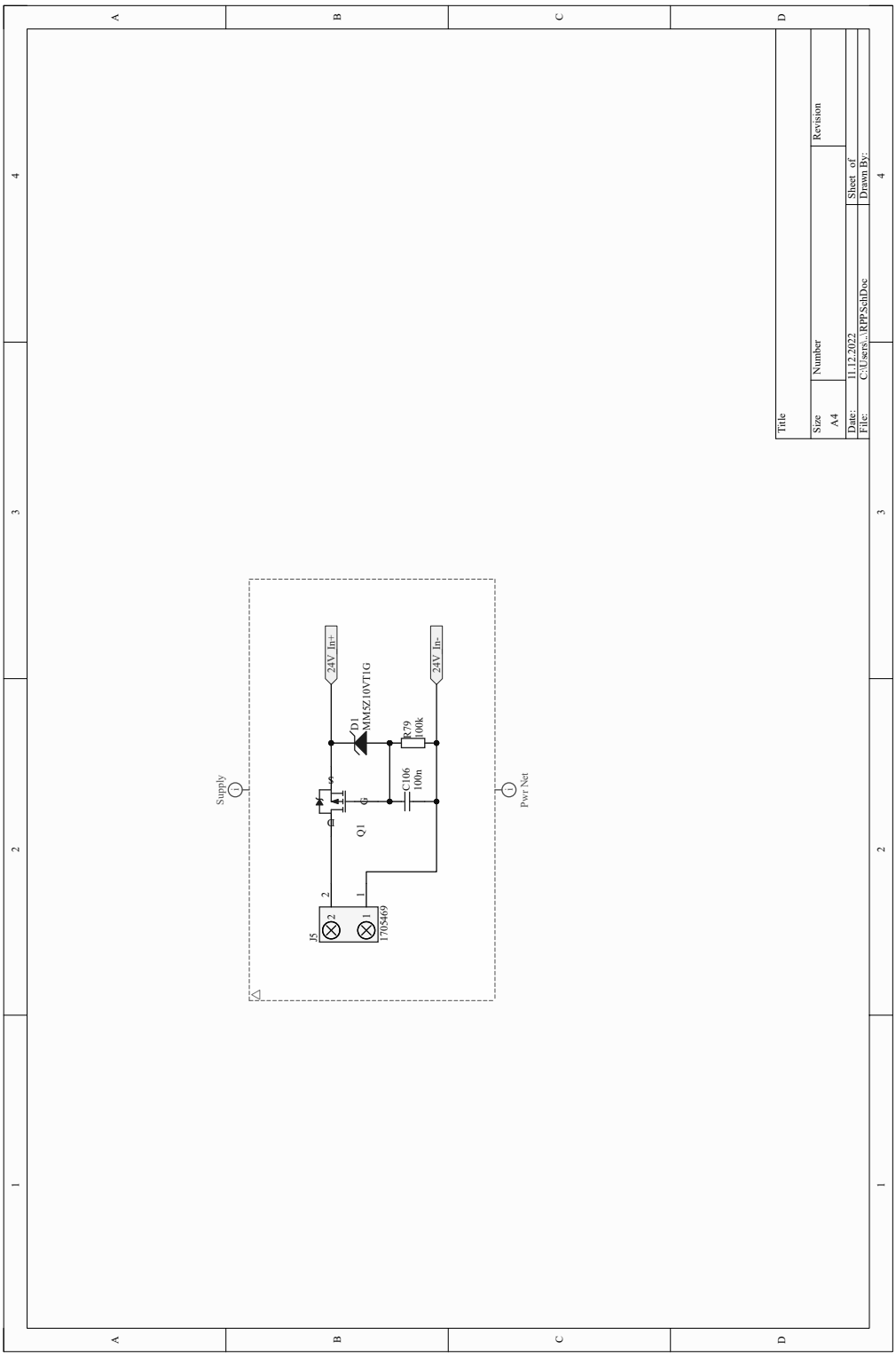


Figure A.26: Schematics measurement board: reverse polarity protection

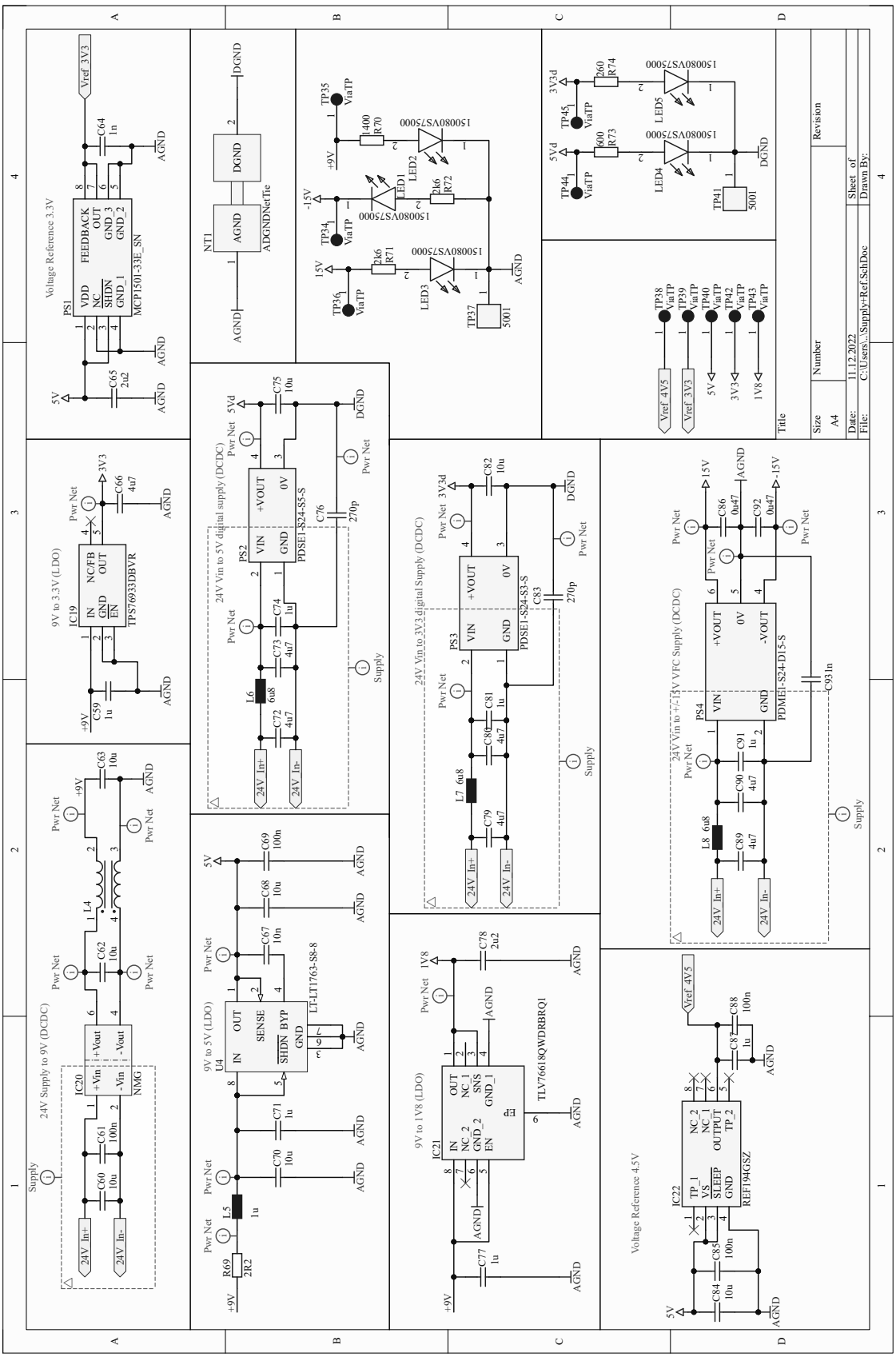


Figure A.27: Schematics measurement board: supply and reference voltage

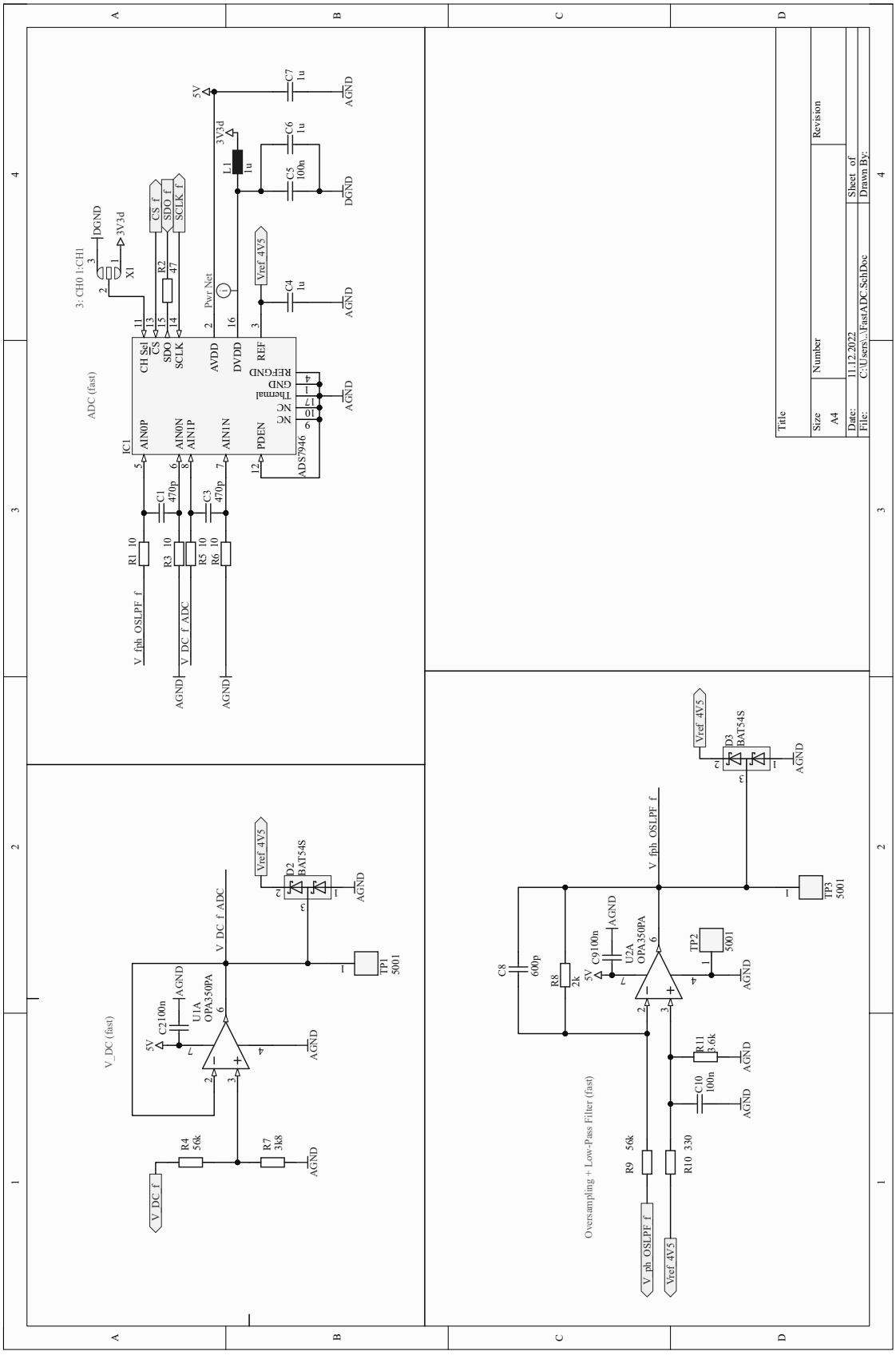


Figure A.28: Schematics measurement board: 14 bit ADC

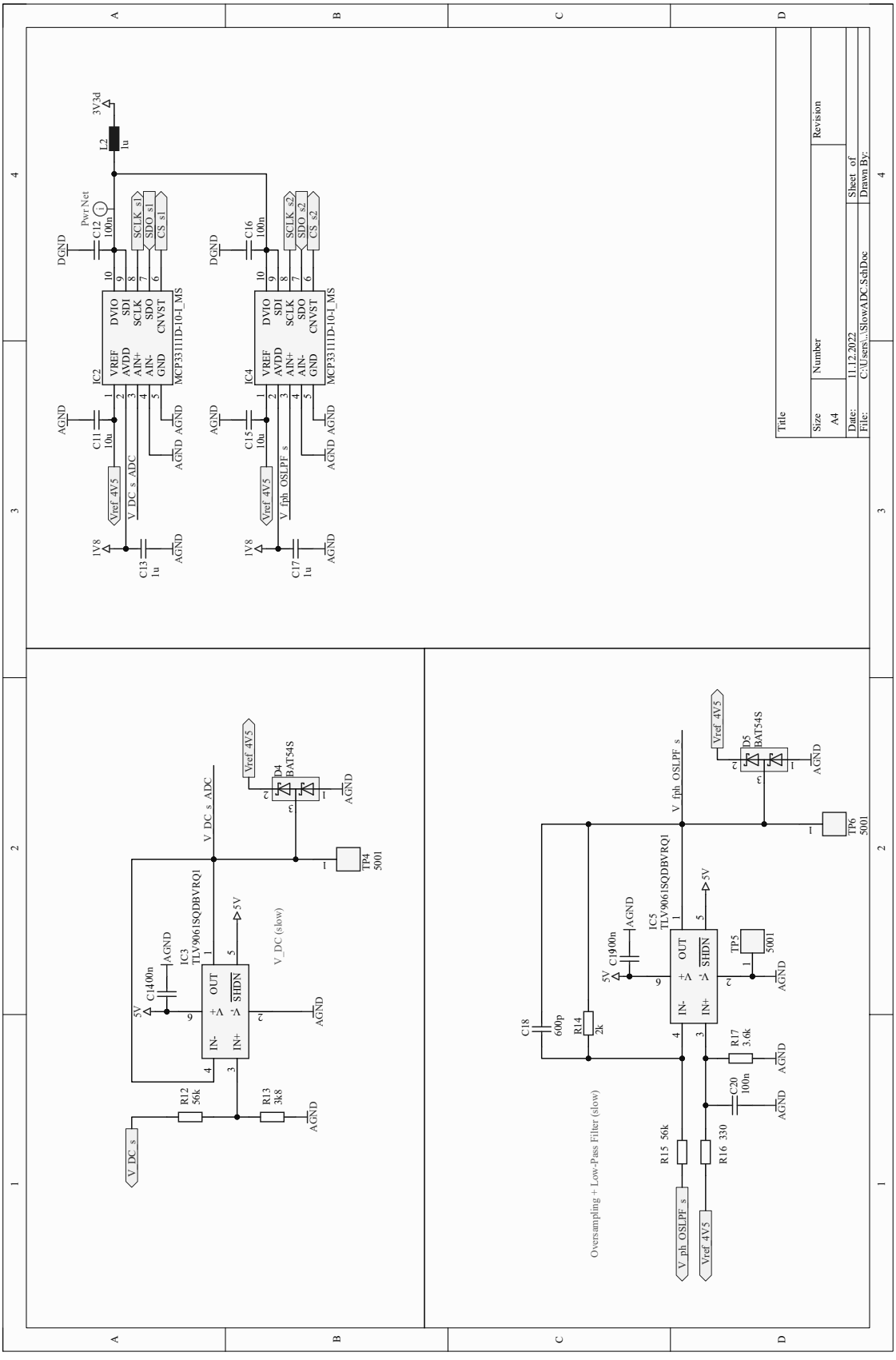


Figure A.29: Schematics measurement board: 12 bit ADC

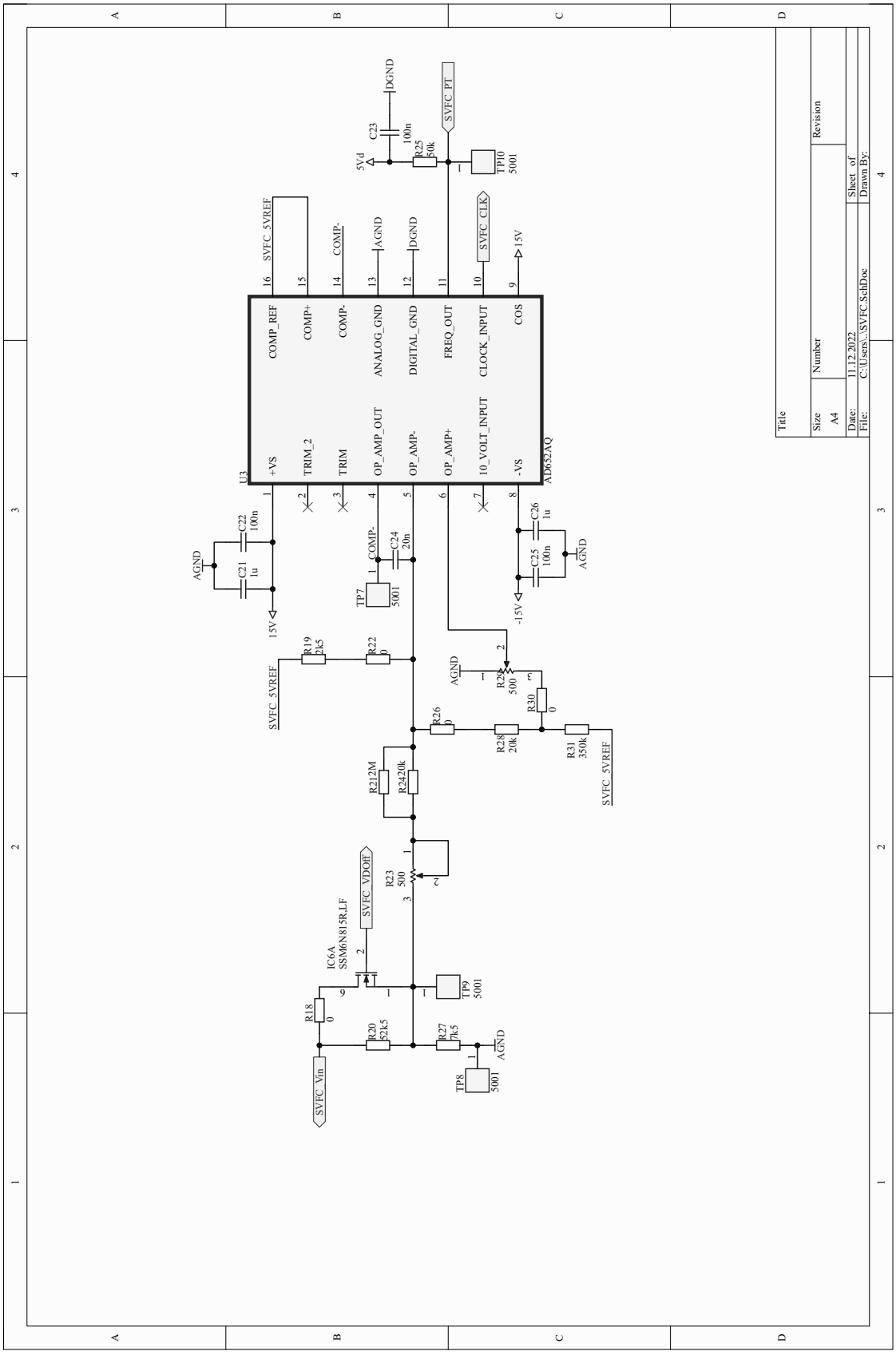


Figure A.30: Schematics measurement board: SVFC

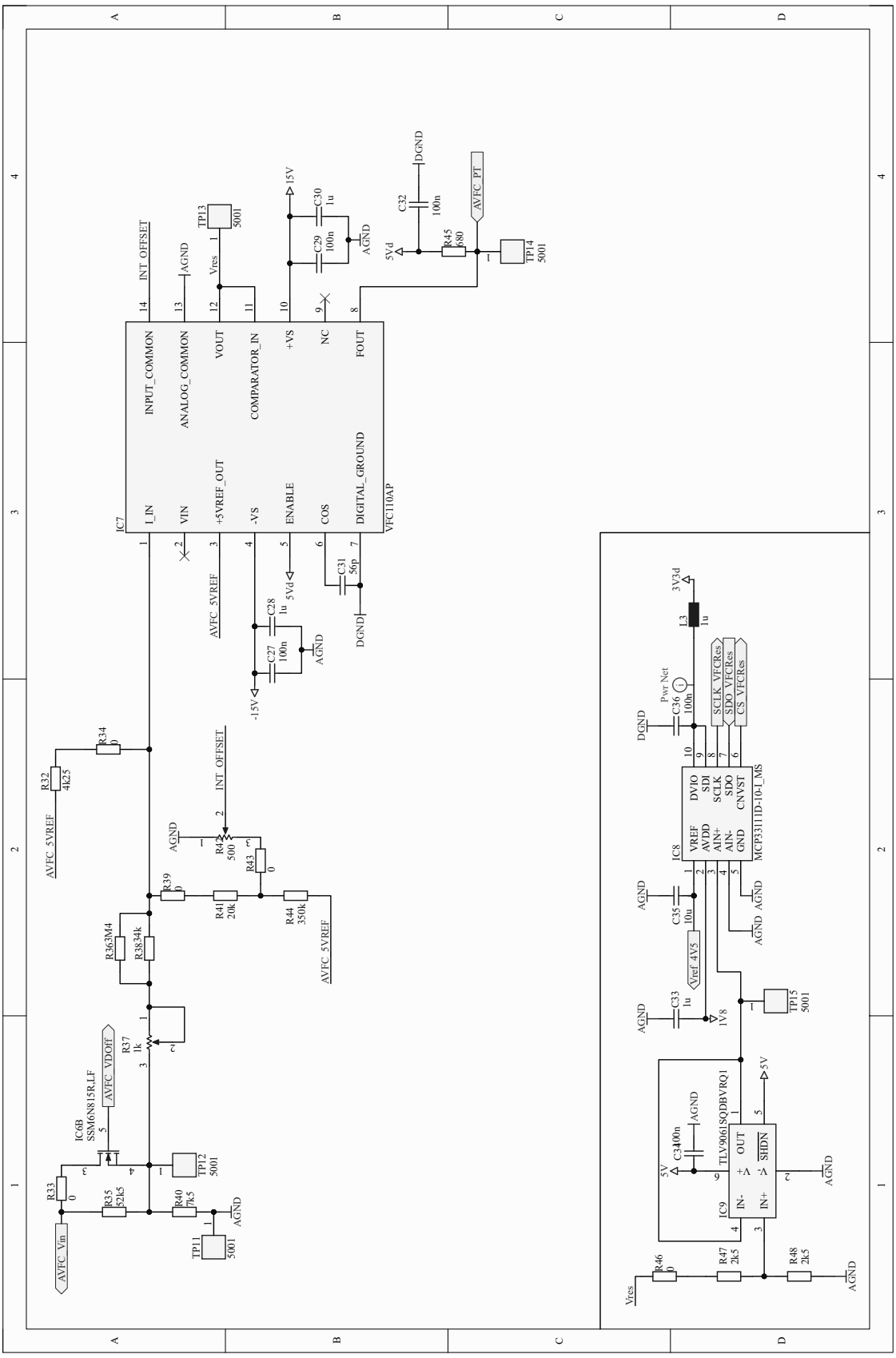


Figure A.31: Schematics measurement board: AVFC

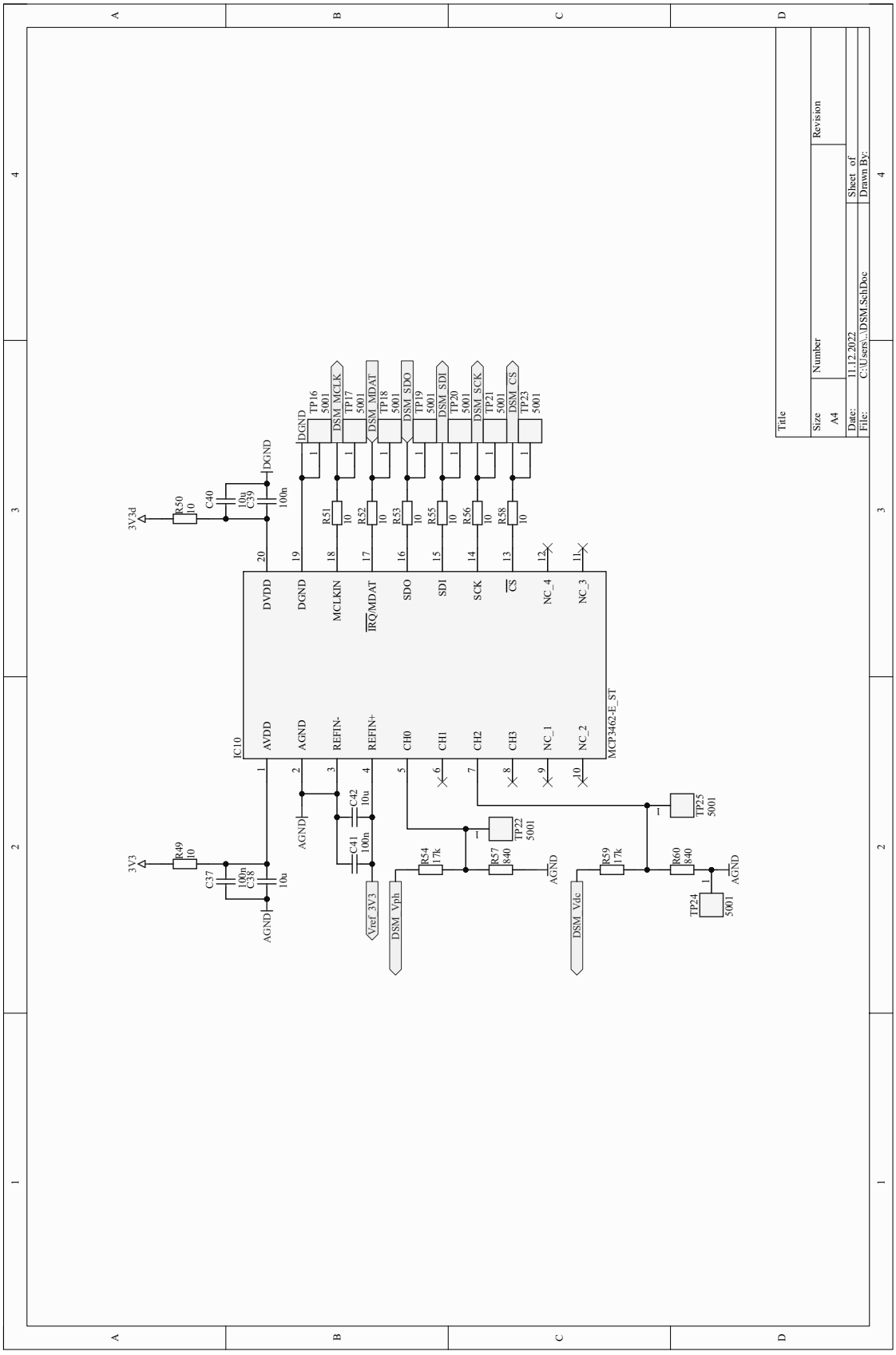


Figure A.32: Schematics measurement board: DSM

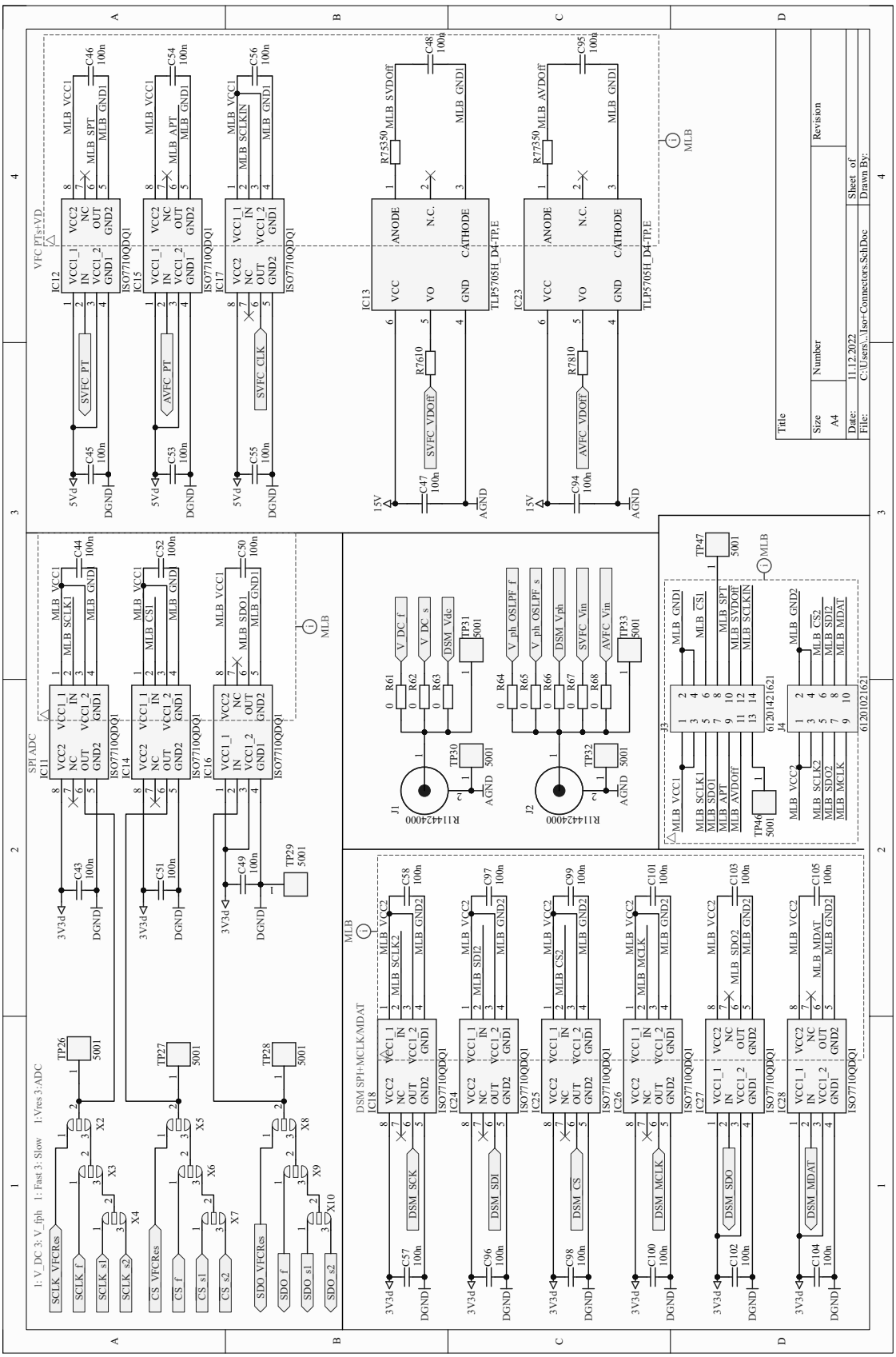


Figure A.33: Schematics measurement board: connectors and isolation

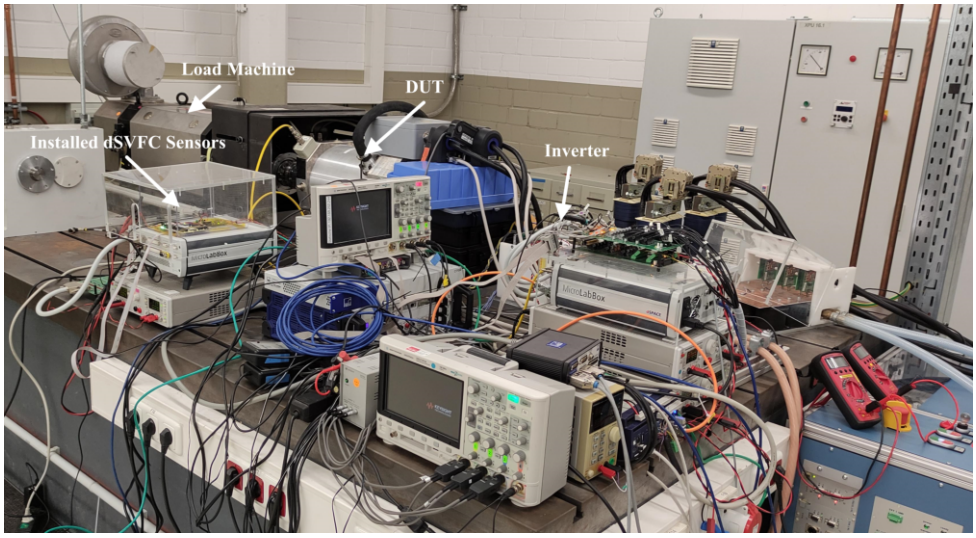


Figure A.34: Overview of electrical drivetrain test bench

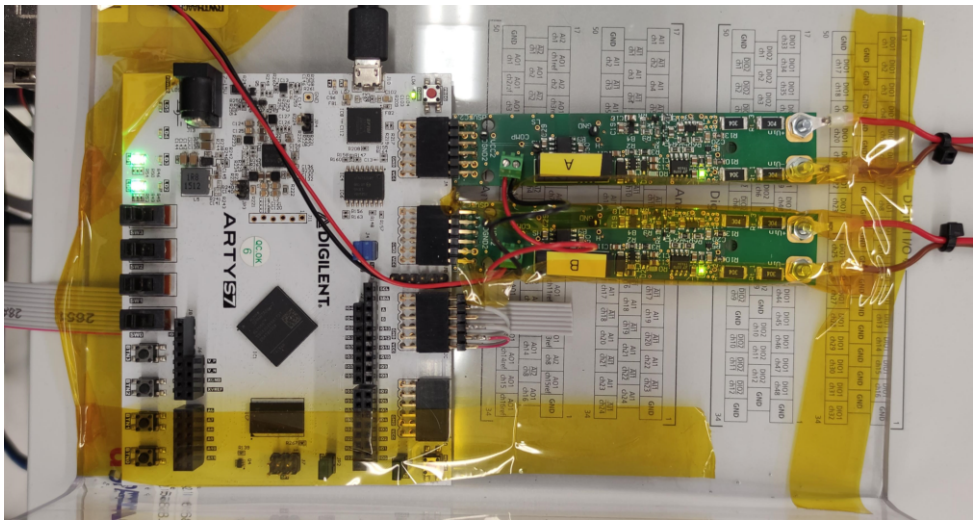


Figure A.35: Implemented dSVFC sensors for phase-to-phase measurement

B Acronyms

ac	alternating current
ADC	analog-to-digital converter
AI	artificial intelligence
AVFC	asynchronous voltage-to-frequency converter
BEV	battery electric vehicle
BNC	Bayonet Neill-Concelman
CMOS	complementary metal-oxide-semiconductor
CPWM	continuous PWM
DAC	digital-to-analog converter
DB	deadbeat
dc	direct current
DPWM	discontinuous PWM
DSM	delta-sigma modulator
DSP	digital signal processor
dSVFC	discrete synchronous voltage-to-frequency converter
DTFC	direct torque and flux control
EMC	electromagnetic compatibility
EMF	electromotive force
ESR	equivalent series resistance
FE	finite element
FOC	field-oriented control
FPGA	field-programmable gate array
GaN	gallium nitride
GDPWM	generalized DPWM
HMI	human-machine-interface
IC	integrated circuit
IGBT	insulated-gate bipolar transistor
IM	induction machine

IPMSM	interior permament magnet synchronous machine
IRTF	ideal rotating transformer
ISEA	Institute for Power Electronics and Electrical Drives
LDO	Linear- and Low-Dropout-Controller
LSB	least significant bit
LUT	look-up table
MBFF	model-based feed-forward
MOSFET	metal-oxide semiconductor field-effect transistor
MSB	most significant bit
NVH	noise vibration harshness
OP	operating point
OpAmp	operational amplifier
OPP	optimized pulse pattern
PCB	printed circuit board
PLL	phase-locked loop
PMSM	permament magnet synchronous machine
PWM	pulse width-modulation
RCP	rapid control prototype
RPP	reverse polarity protection
RT	real time
RTP	real-time processor
S&H	sample-and-hold
SAR	successive-approximation-register
SDO	slave data out
SiC	silicon carbide
SM	synchronous machine
SNR	signal-to-noise ratio
SPDT	single pole, double throw
SPI	serial peripheral interface
SPWM	sinusoidal PWM
SRM	switched reluctance machine
SVFC	synchronous voltage-to-frequency converter
SVPWM	space-vector PWM
TF	transfer function
THIPWM	third harmonic injection PWM
VFC	voltage-to-frequency converter

VHDL	very high-speed integrated circuit hardware description language
VSI	voltage-source inverter
WEMPEC	Wisconsin Electric Machines and Power Electronics Consortium
ZVS	zero-voltage switching

C Symbols

$\bar{e}_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$	Average relative error of averaged volt error over one PWM period
C_{ce}	Collector-emitter capacitance
C_{dc}	dc-link capacitor
C_{gc}	Gate-collector capacitance
C_{int}	Integrator capacitor
C_{oes}	Output capacitance of IGBT
C_{os}	One shot capacitor
C_{sc}	Additional capacitance of switching cell
D_1	Diode top switching cell
$\mathrm{D}_{\mathrm{rpp}}$	reverse polarity protection diode
D_2	Diode bottom switching cell
d^*	Reference duty cycle
$e_{\mathrm{rel},\bar{u}_{\mathrm{pwm}}}$	Relative error of averaged volt error over one PWM period
f_{clk}	Clock frequency
f_{pt}	Pulse train frequency
f_{samp}	Sample frequency
f_{sw}	Inverter switching frequency
$\vec{i}_{\mathrm{s}}^{\,\mathrm{dq}}$	Stator current dq-frame
i_{f}	Equivalent current of flux-linkage
i_{gc}	IGBT gate-collector current
i_{in}	Input current
i_{int}	Integrator current
$i_{\mathrm{int,H}}$	Integrator current with switch high side
$i_{\mathrm{int,L}}$	Integrator current with switch low side
I_{off}	Integrator offset current
i_{out}	Output current
I_{ph}	Constant phase current
$\vec{i}_{\mathrm{ph}}$	Phase current
i_{ph}	Actual phase current

$I_{\mathrm{ph,lim}}$	Constant phase current for transition in model approach
$i_{\mathrm{ph}}^{\Diamond}$	Measured phase current
I_{ph}^{*}	Reference constant phase current
$\vec{i}_{\mathrm{s}}$	Stator current
i_{sd}	Flux-generating stator current component
$\vec{i}_{\mathrm{s}}^{\Diamond}$	Measured stator current
i_{sq}	Torque-generating stator current component
I_0	Constant current of constant current source
$i_{0,\mathrm{H}}$	Mirrored current high side
$i_{0,\mathrm{L}}$	Mirrored current low side
L_{lpf}	Smoothing inductance
L_{md}	Quadrature main inductance
L_{mq}	Main inductance
L_{s}	Stator inductance
L_{sd}	Direct synchronous inductance
$L_{\sigma\mathrm{s}}$	Stator leakage inductance
L_{sq}	Quadrature synchronous inductance
$\mathrm{M_{sH}}$	Switching MOSFET high side of current mirror
$\mathrm{M_{sL}}$	Switching MOSFET low side of current mirror
N	Number of pulses
ω_{s}	Electrical anglular frequency
P_{dSVFC}	Power consumption of dSVFC
$\bar{\psi}_{\mathrm{cr,err}}$	Volt-second error during charge reversal
$\vec{\psi}_{\mathrm{s}}^{\mathrm{dq}}$	Stator flux-linkage dq-frame
ψ_{sd}	d-component stator flux-linkage
ψ_{f}	Permanent magnetic field flux-linkage
$\bar{\psi}_{\mathrm{lin,err}}$	Volt-second error in linear commutation process
$\bar{\psi}_{\mathrm{nonlin,err}}$	Volt-second error in nonlinear commutation process
$\vec{\psi}_{\mathrm{ph}}$	Terminal flux-linkage
ψ_{ph}	Actual terminal flux-linkage
$\vec{\psi}_{\mathrm{ph}}^{\Diamond}$	Measurend terminal flux-linkage
$\psi_{12}^{\Diamond}$	Measurend phase-to-phase flux-linkage (1-2)
$\psi_{32}^{\Diamond}$	Measurend phase-to-phase flux-linkage (3-2)
$\bar{\psi}_{\mathrm{pwm}}$	Measured averaged volt-second over one PWM period
$\bar{\psi}_{\mathrm{pwm,err}}$	Averaged volt-second error over one PWM period
ψ_{sq}	q-component stator flux-linkage
$\bar{\psi}_{\mathrm{rect,err}}$	Volt-second error in rectangular model
ψ_{ε}	Volt-second resolution

$\vec{\psi}_\mathrm{s}$	Stator field flux-linkage
Q	Electrical charge
Q_off	Charge during pulse off-stage
Q_on	Charge during pulse on-stage
R_int	Integrator resistor
$R_\mathrm{lin,trim}$	Trimmer to adjust linearity
$R_\mathrm{os}i$	Offset resistor i
$R_\mathrm{os,trim}$	Trimmer to adjust offset
R_pullup	Pull-up resistor
R_s	Stator resistor
R_sc	Additional resistor of switching cell
R_shunt	Shunt resistor
$R_\mathrm{s}^\lozenge$	Measured stator resistor
$R_\mathrm{vd}i$	Voltage divider resistor i
$\mathrm{S_{co}}$	SPDT switch
$\sigma_{\bar{u}_\mathrm{pwm}}$	Standard deviation of averaged volt error over one PWM period
$\mathrm{S_1}$	Switch top switching cell
$\mathrm{S_2}$	Switch bottom switching cell
T_clk	Clock period
T_cr	Charge reversal time
T_dt	Dead time
$t_\mathrm{dt+}$	Additional dead time during commutation
T_e	Electrodynamic torque
θ_r	Rotor angle
t_lin	Commutation time in linear case
T_n	Period of irregular pulse pattern
T_off	Turn-off delay
T_on	Turn-on delay
T_pls	Duration pulse on-stage
Δt_P2P	Time interval between two pulses of a pulse train
T_pwm	Period time of one PWM cycle
u_α	Real part 2D space vector
u_β	Imaginary part 2D space vector
u_ce	IGBT collector-emitter voltage
u_ct	Comparator output voltage
U_dc	Dc-link voltage
$U_\mathrm{dc}^\lozenge$	Measured dc-link voltage
U_diode	Diode on-stage voltage drop

$u_{\mathrm{d1,H}}$	Drain voltage of MOSFET
$\vec{u}_{\mathrm{s}}^{\,\mathrm{dq}}$	Stator voltage dq-frame
$u_{\mathrm{d2,H}}$	Drain voltage of MOSFET
$u_{\mathrm{e}i}$	Back-emf phase i
u_{ge}	IGBT gate-emitter voltage
$u_{\mathrm{g,H}}$	Gate voltage of MOSFET
$u_{\mathrm{g,L}}$	Gate voltage of MOSFET
U_{IGBT}	IGBT on-stage voltage drop
u_{ij}	Phase-to-phase voltage ij
$u_{i\mathrm{N}}$	i voltage sequence component
u_{in}	Input voltage
$\bar{u}_{\mathrm{in,P2P}}$	Averaged input voltage between to pulses of pulse train
$u_{\mathrm{int}-}$	Negative input integrator
u_{lin}	Commutation voltage in nonlinear case
u_{meas}	Measured voltage
$U_{\mathrm{meas,max}}$	Maximum measured voltage
$U_{\mathrm{meas,min}}$	Minimum measured voltage
$u_{12}^{\Diamond}$	Measured dc-link voltage
$\vec{u}_{\mathrm{ph}}$	Phase voltage
u_{ph}	Actual phase voltage
$\bar{u}_{\mathrm{ph}}$	PWM-period average actual phase voltage
$u_{\mathrm{ph}i}$	Voltage phase i
$u_{\mathrm{ph}}^{\Diamond}$	Measured phase voltage
u_{ph}^{*}	Reference phase voltage
$u_{\mathrm{pt}}(f_{\mathrm{pt}})$	Output pulse train
u_{pwm}	PWM voltage
$\bar{u}_{\mathrm{pwm}}$	Measured averaged voltage over one PWM period
$u_{\mathrm{pwm,fil}}$	Filtered PWM voltage
U_{ref}	Reference voltage
u_{ε}	Voltage resolution
$\vec{u}_{\mathrm{s}}$	Stator voltage
$U_{\mathrm{s,dig}}$	Digital supply voltage
$-U_{\mathrm{s}}$	Negative supply voltage
$u_{\mathrm{s1,H}}$	Source voltage of MOSFET
$+U_{\mathrm{s}}$	Positive supply voltage
$u_{\mathrm{s2,H}}$	Source voltage of MOSFET
U_{sup}	Supply voltage
u_{Vs}	Integrator output voltage

List of Figures

List of Tables

Bibliography

[1] R. De Doncker, D. Pulle, and A. Veltman, *Fundamentals of Electrical Drives*. Springer International Publishing, 2016.

[2] R. Richter, *Elektrische Maschinen*. Springer Basel, 1953.

[3] R. De Doncker, D. Pulle, and A. Veltman, *Advanced Electrical Drives*. Springer International Publishing, 2020.

[4] D. C. R. Pinto, H. Xu, and R. W. De Doncker, "Accurate fea-based modeling of ipmsms operating under high magnetic utilization," in *2022 25th International Conference on Electrical Machines and Systems (ICEMS)*, IEEE, Nov. 2022.

[5] S. Schüller and R. W. De Doncker, "AI-Assisted Torque Control of an Interior Permanent Magnet Synchronous Machine," in *2023 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*, IEEE, Nov. 2023.

[6] B. Kenny and R. Lorenz, "Stator- and rotor-flux-based deadbeat direct torque control of induction machines," *IEEE Transactions on Industry Applications*, vol. 39, no. 4, pp. 1093–1101, Jul. 2003.

[7] J. S. Lee, C.-H. Choi, J.-K. Seok, and R. D. Lorenz, "Deadbeat-direct torque and flux control of interior permanent magnet synchronous machines with discrete time stator current and stator flux linkage observer," *IEEE Transactions on Industry Applications*, vol. 47, no. 4, pp. 1749–1758, Jul. 2011.

[8] Y. Wang, Y. Xu, N. Niimura, B. Rudolph, and R. Lorenz, "Using Volt-Second Sensing to Directly Improve Torque Accuracy and Self-Sensing at Low Speeds," *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4472–4482, Sep. 2017.

[9] L. Ge, D. Zhang, J. Huang, and S. Song, "SMO-based Sensorless Control of Switched Reluctance Machines with Closed-loop Flux-linkage Observer," in *2022 25th International Conference on Electrical Machines and Systems (ICEMS)*, IEEE, Nov. 2022.

[10] G. Götz, J. Kolbe, A. von Hoegen, and R. De Doncker, "Control Parameter Analysis for an SRM Inverter for Range Extender Units with Integrated DC-DC Converter," *Journal of Electrical Engineering and Technology*, vol. 18, no. 3, pp. 1883–1892, Mar. 2023.

[11] G. Verghese and S. Sanders, "Observers for flux estimation in induction machines," *IEEE Transactions on Industrial Electronics*, vol. 35, no. 1, pp. 85–94, 1988.

[12] P. Jansen and R. Lorenz, "A physically insightful approach to the design and accuracy assessment of flux observers for field oriented induction machine drives," *IEEE Transactions on Industry Applications*, vol. 30, no. 1, pp. 101–110, 1994.

[13] Y. Xu, Y. Wang, R. Iida, and R. Lorenz, "Extending Low-Speed Self-Sensing via Flux Tracking With Volt–Second Sensing," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4405–4414, Sep. 2018.

[14] Y. Hori and T. Umeno, "Implementation of robust flux observer based field orientation (fofo) controller for induction machines," in *Conference Record of the IEEE Industry Applications Society Annual Meeting,*, IEEE, 1989.

[15] J.-H. Kim, J.-W. Choi, and S.-K. Sul, "Novel rotor flux observer using observer characteristic function in complex vector space for field oriented induction motor drives," in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, IEEE, 2001.

[16] H.-U. Rehman, M. Gilven, A. Derdiyok, and L. Xu, "A new current model flux observer insensitive to rotor time constant and rotor speed for dfo control of induction machine," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, ser. PESC-01, IEEE.

[17] K. Hurst, T. Habetler, G. Griva, F. Profumo, and P. Jansen, "A self-tuning, closed-loop flux observer for sensorless torque control of standard induction machines," in *Proceedings of PESC '95 - Power Electronics Specialist Conference*, ser. PESC-95, IEEE.

[18] N. T. West and R. D. Lorenz, "Digital implementation of both a stator and rotor flux linkage observer and stator current observer," in *2007 IEEE Industry Applications Annual Meeting*, IEEE, Sep. 2007.

[19] E. Reinhard, E. Garces, and J. Stauder, "Repeated look-up tables," *IEEE Transactions on Image Processing*, vol. 29, pp. 2370–2379, 2020.

[20] A. von Hoegen, A. Woerndle, and R. De Doncker, "Implementation of PWM-based Direct Instantaneous Torque Control with Duty Cycle Interlock for a Switched Reluctance Machine," in *2020 23rd International Conference on Electrical Machines and Systems (ICEMS)*, IEEE, Nov. 2020.

[21] B. Batkhishig, P. F. Da Costa Goncalves, B. Nahid-Mobarakeh, and A. Emadi, "Look-up table size reduction strategy for synchronous optimal pulse width modulation," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, IEEE, Oct. 2023.

[22] F.-Y. Lin and Y.-M. Chen, "Derivation of non-uniformly distributed look-up table for pmsm model simulation," in *2023 IEEE International Future Energy Electronics Conference (IFEEC)*, IEEE, Nov. 2023.

[23] A. Babel, A. Muetze, R. Seebacher, K. Krischan, and E. G. Strangas, "Condition monitoring and failure prognosis of IGBT inverters based on on-line characterization," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, IEEE, Sep. 2014.

[24] C. H. van der Broeck, R. D. Lorenz, and R. W. D. Doncker, "Methods for monitoring 3-d temperature distributions in power electronic modules," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, Mar. 2018.

[25] M. Schubert and R. D. Doncker, "Semiconductor Temperature and Condition Monitoring Using Gate-Driver-Integrated Inverter Output Voltage Measurement," *IEEE Transactions on Industry Applications*, vol. 56, no. 3, pp. 2894–2902, May 2020.

[26] W. Kirchgassner, O. Wallscheid, and J. Bocker, "Data-Driven Permanent Magnet Temperature Estimation in Synchronous Motors With Supervised Machine Learning: A Benchmark," *IEEE Transactions on Energy Conversion*, vol. 36, no. 3, pp. 2059–2067, Sep. 2021.

[27] S. Schüller, M. Azeem, A. von Hoegen, and R. De Doncker, "Temperature Estimation of a PMSM using a Feed-Forward Neural Network," in *2022 25th International Conference on Electrical Machines and Systems (ICEMS)*, IEEE, Nov. 2022.

[28] T. Geyer, N. Oikonomou, G. Papafotiou, and F. Kieferndorf, "Model Predictive Pulse Pattern Control," *IEEE Transactions on Industry Applications*, vol. 48, no. 2, pp. 663–676, Mar. 2012.

[29] N. Hartgenbusch, I. Ralev, R. D. Doncker, and T. Kojima, "Stator Flux Trajectory Control combined with Optimized Pulse Patterns for Interior Permanent Magnet Machines," in *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, IEEE, Aug. 2019.

[30] M. Harries, A. Woerndle, and R. De Doncker, "Low Vibrations and Improved NVH in Permanent Magnet Synchronous Machines Due to Injection of Flux-Linkage Harmonics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 2, pp. 1649–1657, Apr. 2022.

[31] M. Boesing, M. Niessen, T. Lange, and R. D. Doncker, "Modeling spatial harmonics and switching frequencies in PM synchronous machines and their electromagnetic forces," in *2012 XXth International Conference on Electrical Machines*, IEEE, Sep. 2012.

[32] T. Geyer, N. Oikonomou, G. Papafotiou, and F. Kieferndorf, "Model predictive pulse pattern control," in *2011 IEEE Energy Conversion Congress and Exposition*, IEEE, Sep. 2011.

[33] J. Lee, C. Choi, J. Seok, and R. Lorenz, "Deadbeat direct torque and flux control of interior permanent magnet machines with discrete time stator current and stator flux linkage observer," in *2009 IEEE Energy Conversion Congress and Exposition*, IEEE, Sep. 2009.

[34] A. Hava, R. Kerkman, and T. Lipo, "Simple analytical and graphical methods for carrier-based pwm-vsi drives," *IEEE Transactions on Power Electronics*, vol. 14, no. 1, pp. 49–61, Jan. 1999.

[35] J. Holtz, "Pulsewidth modulation for electronic power conversion," *Proceedings of the IEEE*, vol. 82, no. 8, pp. 1194–1214, 1994.

[36] H. van der Broeck, H. Skudelny, and G. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Transactions on Industry Applications*, vol. 24, no. 1, pp. 142–150, Jan. 1988.

[37] G. Buja and G. Indri, "Improvement of pulse width modulation techniques," *Archiv für Elektrotechnik*, vol. 57, no. 5, pp. 281–289, Sep. 1975.

[38] A. Hava, R. Kerkman, and T. Lipo, "A high-performance generalized discontinuous pwm algorithm," *IEEE Transactions on Industry Applications*, vol. 34, no. 5, pp. 1059–1071, 1998.

[39] A. Hava, R. Kerkman, and T. Lipo, "Carrier-based pwm-vsi overmodulation strategies: Analysis, comparison, and design," *IEEE Transactions on Power Electronics*, vol. 13, no. 4, pp. 674–689, Jul. 1998.

[40] A. Hava, S.-K. Sul, R. Kerkman, and T. Lipo, "Dynamic overmodulation characteristics of triangle intersection pwm methods," *IEEE Transactions on Industry Applications*, vol. 35, no. 4, pp. 896–907, Jul. 1999.

[41] M. Grubmuller, B. Schweighofer, and H. Wegleiter, "Development of a Differential Voltage Probe for Measurements in Automotive Electric Drives," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 2335–2343, Mar. 2017.

[42] A. Hefner and D. Blackburn, "An analytical model for the steady-state and transient characteristics of the power insulated-gate bipolar transistor," *Solid-State Electronics*, vol. 31, no. 10, pp. 1513–1532, Oct. 1988.

[43] P. Lauritzen, G. Andersen, and M. Helsper, "A basic IGBT model with easy parameter extraction," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, IEEE, 2001.

[44] R. Withanage, N. Shammas, S. Tennakoon, C. Oates, and W. Crookes, "Igbt Parameter Extraction for the Hefner IGBT Model," in *Proceedings of the 41st International Universities Power Engineering Conference*, IEEE, Sep. 2006.

[45] Y. Gao, N. Li, S. Guo, and H. Liu, "The Modeling and Parameters Identification for IGBT Based on Optimization and Simulation," in *Bio-Inspired Computational Intelligence and Applications*, Springer Berlin Heidelberg, 2007, pp. 628–638.

[46] N. Bedetti, S. Calligaro, and R. Petrella, "Accurate modeling, compensation and self-commissioning of inverter voltage distortion for high-performance motor drives," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, IEEE, Mar. 2014.

[47] K. J. Szwarc, A. Cichowski, J. Nieznanski, and P. Szczepankowski, "Modeling the effect of parasitic capacitances on the dead-time distortion in multilevel NPC inverters," in *2011 IEEE International Symposium on Industrial Electronics*, IEEE, Jun. 2011.

[48] M. Schubert, L. Jebe, M. Gossen, and R. W. D. Doncker, "Online phase current and voltage offset calibration using inverter voltage distortion," in *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*, IEEE, Dec. 2017.

[49] M. Schubert, *Hochpräzise Drehmomentregelung von Umrichter-gespeisten Asynchronmaschinen mit instantaner Phasenspannungsmessung*, en. RWTH Aachen University, 2018, vol. RWTH Aachen University, p. 2018.

[50] M. Schubert and R. W. D. Doncker, "Discrete Implementation Aspects for Online Current - and Voltage-Sensor Offset Calibration Based on Inverter Voltage Distortion," in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, IEEE, May 2019.

[51] W. Yang, Y. Wang, L. Yan, Z. Han, and D. Gerling, "Online Detection of Inverter Voltage Error Based on the Voltage Oversampling Measurement and Sigmoidal Function Model," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 303–312, Jan. 2022.

[52] S. Wiedemann and R. Kennel, "Accurate Self-Identification of Inverter Nonlinear Effects in AC Drives," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Jun. 2018.

[53] M. Schubert, D. Scharfenstein, and R. De Doncker, "A Novel Online Current- and Voltage-Sensor Offset Adaption Scheme Utilizing the Effect of Inverter Voltage Distortion," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6011–6017, Nov. 2019.

[54] A. von Hoegen, P. Tillmann, T. Kojima, and R. De Doncker, "Accurate Modeling of IGBT-Based Converters in PLECS," in *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, IEEE, Sep. 2022.

[55] J. Allmeling and W. Hammer, "PLECS-piece-wise linear electrical circuit simulation for Simulink," in *Proceedings of the IEEE 1999 International Conference on Power Electronics and Drive Systems. PEDS'99 (Cat. No.99TH8475)*, IEEE, 1999, 355–360 vol.1.

[56] T. Lange, A. von Hoegen, N. Hartgenbusch, G. Götz, and R. De Doncker, "Improvement of Phase-Voltage Measurement with Voltage-to-Frequency Converters via Residual-Voltage Sensing," in *2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe)*, IEEE, Sep. 2023.

[57] D. Leggate and R. Kerkman, "Pulse-based dead-time compensator for PWM voltage inverters," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 2, pp. 191–197, Apr. 1997.

[58] A. Munoz and T. Lipo, "On-line dead-time compensation technique for open-loop PWM-VSI drives," *IEEE Transactions on Power Electronics*, vol. 14, no. 4, pp. 683–689, Jul. 1999.

[59] L. Ben-Brahim, "On the Compensation of Dead Time and Zero-Current Crossing for a PWM-Inverter-Controlled AC Servo Drive," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 5, pp. 1113–1117, Oct. 2004.

[60] A. Cichowski and J. Nieznanski, "Self-Tuning Dead-Time Compensation Method for Voltage-Source Inverters," *IEEE Power Electronics Letters*, vol. 3, no. 2, pp. 72–75, Jun. 2005.

[61] H. Schmirgel and J. Krah, "Compensation of Nonlinearities in the IGBT Power Stage of Servo Amplifiers through Feed Forward Control in the Current Loop," in *2005 26th International Exhibition and Conference on Power Electronics, Intelligent Motion and Power Quality (PCIM)*, May 2005.

[62] J. Schellekens, R. Bierbooms, and J. Duarte, "Dead-time compensation for PWM amplifiers using simple feed-forward techniques," in *The XIX International Conference on Electrical Machines - ICEM 2010*, IEEE, Sep. 2010.

[63] D. Lee and J. Ahn, "A Simple and Direct Dead-Time Effect Compensation Scheme in PWM-VSI," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3017–3025, Sep. 2014.

[64] T. Batzel and M. Comanescu, "Instantaneous voltage measurement in PWM voltage source inverters," in *2007 International Aegean Conference on Electrical Machines and Power Electronics*, IEEE, Sep. 2007.

[65] T. Chin, M. Nakano, and T. Hirayama, "Accurate measurement of instantaneous voltage for power electronics circuits," in *Proceedings of Power Conversion Conference - PCC '97*, IEEE, Aug. 1997.

[66] J. Xia, W. Sun, Y. Yin, Z. Xing, and X. Yuan, "FPGA based direct measurement of PWM voltage and inverter disturbance," in *2016 19th International Conference on Electrical Machines and Systems (ICEMS)*, IEEE, 2016.

[67] T.-H. Chin, M. Nakano, and T. Hirayama, "Accurate measurement of instantaneous values of voltage, current and power for power electronics circuits," in *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196)*, IEEE, 1998.

[68] Y. Son, B. Bae, and S. Sul, "Sensorless operation of permanent magnet motor using direct voltage sensing circuit," in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, IEEE, 2002.

[69] R. Tallam, D. Busse, B. Brown, and R. Kerkman, "PWM output voltage measurement apparatus and method," patent US9374021B2 United States, 2016.

[70] L. Peretti and M. Zigliotto, "FPGA-based voltage measurements in AC drives," in *The XIX International Conference on Electrical Machines - ICEM 2010*, IEEE, Sep. 2010.

[71] M. Schubert and R. De Doncker, "Instantaneous Phase Voltage Sensing in PWM Voltage-Source Inverters," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6926–6935, Aug. 2018.

[72] G.-R. Chen and S.-C. Yang, "Phase Voltage Measurement for Permanent Magnet Machine Sensorless Drive Using Controller Capture Modulator," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 1, pp. 49–58, Jan. 2020.

[73] M. dos Santos, B. Cardoso Filho, and F. Vasconcelos, "Voltage and current measurement system for medium voltage inverters," in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, IEEE, 2002.

[74] J. Gottschlich, P. Weiler, M. Neubert, and R. W. D. Doncker, "Delta-sigma modulated voltage and current measurement for medium-voltage DC applications," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, IEEE, Sep. 2017.

[75] Texas Instruments. "Datasheet: High Dynamic Range Delta-Sigma Modulator: ADS1201." (2023), [Online]. Available: `https://www.ti.com/product/ADS1201`.

[76] Texas Instruments. "Datasheet: High Frequency Voltage-to-Frequency Converter: VFC110." (2023), [Online]. Available: `https://www.ti.com/product/VFC110`.

[77] Y. Wang and R. D. Lorenz, "Using volt-sec. sensing to extend the low speed range and the disturbance rejection capability of back-emf-based self-sensing," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, IEEE, Sep. 2016.

[78] Y. Xu, Y. Wang, R. Iida, and R. D. Lorenz, "Extending low speed self-sensing via flux tracking with volt-second sensing," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, IEEE, Oct. 2017.

[79] J. Holtz and J. Quan, "Sensorless vector control of induction motors at very low speed using a nonlinear inverter model and parameter identification," *IEEE Transactions on Industry Applications*, vol. 38, no. 4, pp. 1087–1095, Jul. 2002.

[80] Y. Wang, N. Niimura, B. Rudolph, and R. D. Lorenz, "Using volt-sec. sensing to directly improve torque accuracy and self-sensing at low speeds," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, vol. 39, IEEE, Sep. 2016, pp. 1–8.

[81] C. Dick, "Entwurf und Implementierung einer Sensorlosen Regelung für Geschaltete Reluktanzantriebe," M.S. thesis, Institute for Power Electronics and Electrical Drives, RWTH Aachen University, 2004.

[82] A. von Hoegen, G. Götz, N. Hartgenbusch, R. De Doncker, and T. Kojima, "Precise Volt-Second Measuring Instrument for Voltage-Source Inverters," in *2022 25th International Conference on Electrical Machines and Systems (ICEMS)*, IEEE, Nov. 2022.

[83] A. von Hoegen, G. Götz, N. Mason, N. Hartgenbusch, T. Kojima, and R. De Doncker, "Precise Volt-Second Measuring Instrument for PWM Voltage-Source Inverters," *IEEE Transactions on Instrumentation and Measurement*, vol. 73, pp. 1–15, 2024.

[84] A. von Hoegen, R. De Doncker, T. Kojima, and T. Suzuki, "Voltage Detection Device for Power Converter," WIPO Patent Cooperation Treaty WO/2023/181214, PCT/JP2022/013712, Sep. 28, 2023.

[85] Analog Devices. "Voltage-to-Frequency Converters by Walt Kester and James Bryant." W. Kester and J. Bryant, Eds. (2010), [Online]. Available: `https://www.analog.com/media/en/training-seminars/tutorials/MT-028.pdf`.

[86] Analog Devices. "Ask the Applications Engineer - 3." J. Bryant, Ed. (1989), [Online]. Available: `https://www.analog.com/media/en/technical-documentation/frequently-asked-questions/vol23n2.pdf`.

[87] Analog Devices. "Datasheet: Integrated Circuit Voltage-to-Frequency Converter: AD537." (2000), [Online]. Available: `https://www.analog.com/media/en/technical-documentation/data-sheets/AD537.pdf`.

[88] H. Matsumoto and K. Watanabe, "Switched-Capacitor Frequency-to-Voltage and Voltage-to-Frequency Converters based on Charge-Balancing Principle," in *1988, IEEE International Symposium on Circuits and Systems*, IEEE, Jun. 1988.

[89] Analog Devices. "Datasheet: Voltage-to-Frequency and Frequency-to-Voltage Converter: AD650." (2013), [Online]. Available: `https://www.analog.com/media/en/technical-documentation/data-sheets/AD650.pdf`.

[90] Analog Devices. "Datasheet: Monolithic Synchronous Monolithic Synchronous Voltage-to-Frequency Converter: AD652." (2004), [Online]. Available: `https://www.analog.com/%20media/en/technical-documentation/data-sheets/AD652.pdf`.

[91] D. McDonagh and K. Arshak, "Stable differential voltage to frequency converter with low supply voltage and frequency offset control," *IEEE Transactions on Instrumentation and Measurement*, vol. 47, no. 5, pp. 1355–1361, 1998.

[92] C. Wang, T. Lee, C. Li, and R. Hu, "An All-MOS High-Linearity Voltage-to-Frequency Converter Chip With 520-kHz/V Sensitivity," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 8, pp. 744–747, Aug. 2006.

[93] B. Calvo, N. Medrano, S. Celma, and M. T. Sanz, "A low-power high-sensitivity CMOS voltage-to-frequency converter," in *2009 52nd IEEE International Midwest Symposium on Circuits and Systems*, IEEE, Aug. 2009.

[94] T. Maneechukate, T. Yaonun, T. Kamsri, M. Julsereewong, and V. Riewruja, "Simple square-rooting voltage-to-frequency converter using opamps," in *ICCAS 2010*, IEEE, Oct. 2010.

[95] D. Arbet, M. Kovac, V. Stopjakova, and M. Potocny, "Voltage-to-Frequency Converter for Ultra-Low-Voltage Applications," in *2019 42nd International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO)*, IEEE, May 2019.

[96] W. Petchmaneelumka and A. Julsereewong, "Enhanced differential voltage-to-frequency converter for telemetry applications," in *Proceedings of SICE Annual Conference 2010*, Oct. 2010.

[97] Semikron Danfoss. "Datasheet: IGBT Module SKM600GB066D." (2009), [Online]. Available: `https://www.semikron-danfoss.com/products/product-classes/igbt-modules/detail/skm600gb066d-21915620.html`.

[98] Y. Park and S.-K. Sul, "A Novel Method Utilizing Trapezoidal Voltage to Compensate for Inverter Nonlinearity," *IEEE Transactions on Power Electronics*, vol. 27, no. 12, pp. 4837–4846, Dec. 2012.

[99] N. Urasaki, T. Senjyu, T. Funabashi, and H. Sekine, "Adaptive Dead-Time Compensation Strategy Taking Parasitic Capacitance Effects Into Account," in *2005 IEEE International Conference on Industrial Technology*, IEEE, pp. 1109–1114.

[100] N. Fritz, G. Engelmann, A. Stippich, C. Ludecke, D. A. Philipps, and R. W. D. Doncker, "Toward an in-depth understanding of the commutation processes in a sic mosfet switching cell including parasitic elements," *IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 4089–4101, Jul. 2020.

[101] LEM International SA. "Datasheet: Current Transducer HO-P series." (2020), [Online]. Available: https://www.lem.com/sites/default/files/products_datasheets/ho-p_series.pdf.

[102] Keysight Technologies. "Datasheet: https://www.keysight.com/us/en/product/N2893A/ac-dc-current-probe-100-mhz-15a.html." (2022), [Online]. Available: https://www.keysight.com/us/en/lib/resources/selection-guides/oscilloscope-probes.html#CurrentProbes.

[103] Microchip Technology Inc. "Datasheet: 1 Msps/500 ksps, 14/12-Bit Single-Ended Input SAR ADC: MCP33151/41-XX." (2019), [Online]. Available: https://ww1.microchip.com/downloads/en/DeviceDoc/MCP33151-XX-Family-Data-Sheet-DS20006220A.pdf.

[104] U. Tietze, C. Schenk, and E. Gamm, *Halbleiter-Schaltungstechnik*, 16th ed. Springer Vieweg, 2019.

[105] H. Lutz and W. Wendt, *Taschenbuch der Regelungstechnik*. Verlag Europa-Lehrmittel, 2021.

[106] N. A. Mason, "Sensorentwicklung zur instantanen Erfassung von Spannungszeitflächen für spannungsgeführte Wechselrichter," M.S. thesis, Institute for Power Electronics and Electrical Drives, RWTH Aachen University, May 17, 2023.

[107] Texas Instruments. "Datasheet: LM334 3-Terminal Adjustable Current Sources." (2013), [Online]. Available: https://www.ti.com/product/LM334.

[108] dSPACE GmbH. "MicroLabBox." (2022), [Online]. Available: https://www.dspace.com/de/gmb/home/products/hw/microlabbox.cfm#175_23630.

[109] Digilent, Inc. "Digilent Arty S7-25." (2023), [Online]. Available: https://digilent.com/shop/arty-s7-spartan-7-fpga-development-board/.

[110] Texas Instruments. "Datasheet: ADS7945, 14-Bit, 2MSPS, Dual-Channel, Unipolar, Differential, u-Power SAR ADC." (2011), [Online]. Available: https://www.ti.com/product/ADS7945.

[111] R. Lerch, *Elektrische Messtechnik, Analoge, digitale und computergestützte Verfahren*, 7th ed. Springer Vieweg, 2016.

[112] D. J. McKinnon, B. Karanayil, and C. Grantham, "Investigation of the effects of DSP timer jitter on the measurement of a PWM controlled inverter output voltage and current," in *The 4th International Power Electronics and Motion Control Conference, 2004. IPEMC 2004.*, 2004.

[113] T. Lange, "Instantaneous Phase Voltage Measurement for Flux Observers in Electrical Machines," M.S. thesis, Institute for Power Electronics and Electrical Drives, RWTH Aachen University, Nov. 16, 2022.

[114] Delta Elektronika BV, *Manual SM3000*. 2007.

[115] FISCHER AND TAUSCHE CAPACITORS. "Datasheet: Coax Caps." (2022), [Online]. Available: https://www.ftcap.de/fileadmin/user_upload/produktboxen/film_kondensatoren/webboxen/Coax_cap/CoaxCap.pdf.

[116] FAIRCHILD SEMICONDUCTOR. "Datasheet: RURG80100, Ultrafast Diode, 80 A, 1000 V." (2022), [Online]. Available: https://www.mouser.de/datasheet/2/308/1/RURG80100_D-2320112.pdf.

[117] Hoecherl und Hackl GmbH. "User Manual: NL Series, Source-Sink." (), [Online]. Available: https://pim.schulz-electronic.de/document/NL_HW_B_D-E.pdf.

[118] Testec Elektronik GmbH. "Datasheet: Differential-Tastköpfe TT-SI 9101." (2022), [Online]. Available: https://testec.de/de/produkte/differential-tastk%C3%B6pfe.html.

[119] Keysight Technologies. "InfiniiVision 3000A X-Series Oscilloscopes." (2020), [Online]. Available: https://www.keysight.com/de/de/products/oscilloscopes/infiniivision-2-4-channel-digital-oscilloscopes/infiniivision-3000a-x-series-oscilloscopes.html.

[120] HAMEG Instruments. "User Manual: Arbitrary Power Supply HM8143." (2015), [Online]. Available: https://cdn.rohde-schwarz.com/hameg-archive/MAN_HM8143_de_en_v009_20150624.pdf.

[121] ELV Elektronik AG. "Doppelnetzteil DPS 5315." (2012), [Online]. Available: https://de.elv.com/p/doppelnetzteil-dps-5315-teil-13-P203431/.

[122] Micorchip Technology Inc. "Datasheet: Two/Four/Eight-Channel, 153.6 ksps, Low Noise, 16-Bit Delta-Sigma ADC: MCP3461/2/4." (2021), [Online]. Available: https://ww1.microchip.com/downloads/aemDocuments/documents/APID/ProductDocuments/DataSheets/MCP3461-2-4-Two-Four-Eight-Channel-153.6-ksps-Low-Noise-16-Bit-Delta-Sigma-ADC-Data-Sheet-20006180D.pdf.

[123] R. Schreier, S. Pavan, and G. Temes, *Understanding Delta-Sigma Data Converter*. The Institute of Electrical and Electronic Engineers, Inc., 2017.

[124] ZES ZIMMER Electronic Systems GmbH. "LMG500 - 1 to 8 Channel Power Analyzer." (2023), [Online]. Available: https://www.zes.com/en/Products/Predecessor-Products/Energy-and-Power-Meters/LMG500.

Curriculum Vitae

Anne von Hoegen

Personal Information

Year of birth	1987
Place of birth	Düren, Germany
Nationality	German

Education

03/2013–08/2014	Master of Engineering in Automation and Electrical Drive Engineering at FH Aachen University of Applied Sciences
03/2010–02/2013	Bachelor of Engineering in Electrical Engineering with Internship Semester at FH Aachen University of Applied Sciences
07/1998–06/2007	Burgau-Gymnasium Düren

Work Experience

03/2024–today	Development Engineer with Mercedes-Benz AG, Sindelfingen, Germany
09/2018–12/2023	Research Associate at the Institute for Power Electronics and Electrical Drives (ISEA) of RWTH Aachen University under the supervision of Professor Rik W. De Doncker in the Research Group Electrical Drives
03/2015–02/2024	Freelance Lecturer in the field of Control and Automation Engineering

08/2013–08/2018	Scientific Assistant at the Faculty for Electrical Engineering and Information Technology of FH Aachen University of Applied Science under Professor Franz Wosnitza and Professor Ulrich Hoffmann
03/2012–08/2013	Student worker with DYNA-MESS Prüfsysteme GmbH, Stolberg (Rheinland), Germany
03/2011–07/2013	Student worker at the Faculty for Electrical Engineering and Information Technology of FH Aachen University of Applied Science
08/2008–10/2010	Student worker with PHOTON Europe GmbH and PHOTON Laboatory GmbH, Aachen, Germany

ABISEA Band 1
Eßer, Albert
Berührungslose, kombinierte Energie- und Informationsübertragung für bewegliche Systeme
1. Aufl. 1992, 129 S.
ISBN 3-86073-046-0

ABISEA Band 2
Vogel, Ulrich
Entwurf und Beurteilung von Verfahren zur Hochausnutzung des Rad-Schiene-Kraftschlusses durch Triebfahrzeuge
1. Aufl. 1992, 131 S.
ISBN 3-86073-060-6

ABISEA Band 3
Reckhorn, Thomas
Stromeinprägendes Antriebssystem mit fremderregter Synchronmaschine
1. Aufl. 1992, 128 S.
ISBN 3-86073-061-4

ABISEA Band 4
Ackva, Ansgar
Spannungseinprägendes Antriebssystem mit Synchronmaschine und direkter Stromregelung
1. Aufl. 1992, 137 S.
ISBN 3-86073-062-2

ABISEA Band 5
Mertens, Axel
Analyse des Oberschwingungsverhaltens von taktsynchronen Delta - Modulationsverfahren zur Steuerung von Pulsstromrichtern bei hoher Taktzahl
1. Aufl. 1992, 178 S.
ISBN 3-86073-069-X

ABISEA Band 6
Geuer, Wolfgang
Untersuchungen über das Alterungsverhalten von Blei-Akkumulatoren
1. Aufl. 1993, 97 S.
ISBN 3-86073-097-5

ABISEA Band 7
Langheim, Jochen
Einzelradantrieb für Elektrostraßenfahrzeuge
1. Aufl. 1993, 213 S.
ISBN 3-86073-123-8
(vergriffen)

ABISEA Band 8
Fetz, Joachim
Fehlertolerante Regelung eines Asynchron-Doppelantriebes für ein Elektrospeicherfahrzeug
1. Aufl. 1993, 136 S.
ISBN 3-86073-124-6
(vergriffen)

ABISEA Band 9
Schülting, Ludger
Optimierte Auslegung induktiver Bauelemente für den Mittelfrequenzbereich
1. Aufl. 1993, 126 S.
ISBN 3-86073-174-2
(vergriffen)

ABISEA Band 10
Skudelny, H.-Ch.
Stromrichtertechnik
4. Aufl. 1997, 259 S.
ISBN 3-86073-189-0

ABISEA Band 11
Skudelny, H.-Ch.
Elektrische Antriebe
3. Aufl. 1997, 124 S.
ISBN 3-86073-231-5

ABISEA Band 12
Schöpe, Friedhelm
Batterie-Management für Nickel-Cadmium Akkumulatoren
1. Aufl. 1994, 148 S.
ISBN 3-86073-232-3
(vergriffen)

ABISEA Band 13
v. d. Weem, Jürgen
Schmalbandige aktive Filter für Schienentriebfahrzeuge am Gleichspannungsfahrdraht
1. Aufl. 1995, 126 S.
ISBN 3-86073-233-1

ABISEA Band 14
Backhaus, Klaus
Spannungseinprägendes Direktantriebssystem mit schnelllaufender geschalteter Reluktanzmaschine
1. Aufl. 1995, 146 S.
ISBN 3-86073-234-X
(vergriffen)

ABISEA Band 15
Reinold, Harry
Optimierung dreiphasiger Pulsdauermodulationsverfahren
1. Aufl. 1996, 107 S.
ISBN 3-86073-235-8

ABISEA Band 16
Köpken, Hans-Georg
Regelverfahren für Parallelschwingkreisumrichter
1. Aufl. 1996, 125 S.
ISBN 3-86073-236-6

ABISEA Band 17
Mauracher, Peter
Modellbildung und Verbundoptimierung bei Elektrostraßenfahrzeugen
1. Aufl. 1996, 192 S.
ISBN 3-86073-237-4

ABISEA Band 18
Protiwa, Franz-Ferdinand
Vergleich dreiphasiger Resonanz-Wechselrichter in Simulation und Messung
1. Aufl. 1997, 178 S.
ISBN 3-86073-238-2

ABISEA Band 19
Brockmeyer, Ansgar
Dimensionierungswerkzeug für magnetische Bauelemente in Stromrichteranwendungen
1. Aufl. 1997, 175 S.
ISBN 3-86073-239-0

Aachener Beiträge des ISEA

ABISEA Band 20
Apeldoorn, Oscar
Simulationsgestützte Bewertung von Steuerverfahren für netzgeführte Stromrichter mit verringerter Netzrückwirkung
1. Aufl. 1997, 134 S.
ISBN 3-86073-680-9

ABISEA Band 21
Lohner, Andreas
Batteriemanagement für verschlossene Blei-Batterien am Beispiel von Unterbrechungsfreien Stromversorgungen
1. Aufl. 1998, 126 S.
ISBN 3-86073-681-7

ABISEA Band 22
Reinert, Jürgen
Optimierung der Betriebseigenschaften von Antrieben mit geschalteter Reluktanzmaschine
1. Aufl. 1998, 153 S.
ISBN 3-86073-682-5

ABISEA Band 23
Nagel, Andreas
Leitungsgebundene Störungen in der Leistungselektronik: Entstehung, Ausbreitung und Filterung
1. Aufl. 1999, 140 S.
ISBN 3-86073-683-3

ABISEA Band 24
Menne, Marcus
Drehschwingungen im Antriebsstrang von Elektrostraßenfahrzeugen - Analyse und aktive Dämpfung
1. Aufl. 2001, 169 S.
ISBN 3-86073-684-1

ABISEA Band 25
von Bloh, Jochen
Multilevel-Umrichter zum Einsatz in Mittelspannungs-Gleichspannungs-Übertragungen
1. Aufl. 2001, 137 S.
ISBN 3-86073-685-X

ABISEA Band 26
Karden, Eckhard
Using low-frequency impedance spectroscopy for characterization, monitoring, and modeling of industrial batteries
1. Aufl. 2002, 137 S.
ISBN 3-8265-9766-4

ABISEA Band 27
Karipidis, Claus-Ulrich
A Versatile DSP/ FPGA Structure optimized for Rapid Prototyping and Digital Real-Time Simulation of Power Electronic and Electrical Drive Systems
1. Aufl. 2001, 164 S.
ISBN 3-8265-9738-9

ABISEA Band 28
Kahlen, Klemens
Regelungsstrategien für permanentmagnetische Direktantriebe mit mehreren Freiheitsgraden
1. Aufl. 2002, 154 S.
ISBN 3-8322-1222-1

ABISEA Band 29
Inderka, Robert B.
Direkte Drehmomentregelung Geschalteter Reluktanzantriebe
1. Aufl. 2003, 182 S.
ISBN 3-8322-1175-6

ABISEA Band 30
Schröder, Stefan
Circuit-Simulation Models of High-Power Devices Based on Semiconductor Physics
1. Aufl. 2003, 123 S.
ISBN 3-8322-1250-7

ABISEA Band 31
Buller, Stephan
Impedance-Based Simulation Models for Energy Storage Devices in Advanced Automotive Power Systems
1. Aufl. 2003, 138 S.
ISBN 3-8322-1225-6

ABISEA Band 32
Schönknecht, Andreas
Topologien und Regelungsstrategien für das induktive Erwärmen mit hohen Frequenz-Leistungsprodukten
1. Aufl. 2004, 157 S.
ISBN 3-8322-2408-4

ABISEA Band 33
Tolle, Tobias
Konvertertopologien für ein aufwandsarmes, zweistufiges Schaltnetzteil zum Laden von Batterien aus dem Netz
1. Aufl. 2004, 148 S.
ISBN 3-8322-2676-1

ABISEA Band 34
Götting, Gunther
Dynamische Antriebsregelung von Elektrostraßenfahrzeugen unter Berücksichtigung eines schwingungsfähigen Antriebsstrangs
1. Aufl. 2004, 157 S.
ISBN 3-8322-2804-7

ABISEA Band 35
Dieckerhoff, Sibylle
Transformatorlose Stromrichterschaltungen für Bahnfahrzeuge am 16 2/3Hz Netz
1. Aufl. 2004, 147 S.
ISBN 3-8322-3094-7

ABISEA Band 36
Hu, Jing
Bewertung von DC-DC-Topologien und Optimierung eines DC-DC-Leistungsmoduls für das 42-V-Kfz-Bordnetz
1. Aufl. 2004, 148 S.
ISBN 3-8322-3201-X

ABISEA Band 37
Detjen, Dirk-Oliver
Characterization and Modeling of Si-Si Bonded Hydrophobie Interfaces for Novel High-Power BIMOS Devices
1. Aufl. 2004, 135 S.
ISBN 3-8322-2963-9

ABISEA Band 38
Walter, Jörg
Simulationsbasierte Zuverlässigkeitsanalyse in der modernen Leistungselektronik
1. Aufl. 2004, 121 S.
ISBN 3-8322-3481-0

ABISEA Band 39
Schwarzer, Ulrich
IGBT versus GCT in der Mittelspannungsanwendung - ein experimenteller und simulativer Vergleich
1. Aufl. 2005, 170 S.
ISBN 3-8322-4489-1

ABISEA Band 40
Bartram, Markus
IGBT-Umrichtersysteme für Windkraftanlagen: Analyse der Zyklenbelastung, Modellbildung, Optimierung und Lebensdauervorhersage
1. Aufl. 2006, 185 S.
ISBN 3-8322-5039-5

ABISEA Band 41
Ponnaluri, Srinivas
Generalized Design, Analysis and Control of Grid side converters with integrated UPS or Islanding functionality
1. Aufl. 2006, 163 S.
ISBN 3-8322-5281-9

ABISEA Band 42
Jacobs, Joseph
Multi-Phase Series Resonant DC-to-DC Converters
1. Aufl. 2006, 185 S.
ISBN 3-8322-5532-X

ABISEA Band 43
Linzen, Dirk
Impedance-Based Loss Calculation and Thermal Modeling of Electrochemical Energy Storage Devices for Design Considerations of Automotive Power Systems
1. Aufl. 2006, 185 S.
ISBN 3-8322-5706-3

ABISEA Band 44
Fiedler, Jens
Design of Low-Noise Switched Reluctance Drives
1. Aufl. 2007, 176 S.
ISBN 978-3-8322-5864-1

ABISEA Band 45
Fuengwarodsakul, Nisai
Predictive PWM-based Direct Instantaneous Torque Control for Switched Reluctance Machines
1. Aufl. 2007, 141 S.
ISBN 978-3-8322-6210-5

ABISEA Band 46
Meyer, Christoph
Key Components for Future Offshore DC Grids
1. Aufl. 2007, 187 S.
ISBN 978-3-8322-6571-7

ABISEA Band 47
Fujii, Kansuke
Characterization and Optimization of Soft-Switched Multi-Level Converters for STATCOMs
1. Aufl. 2008, 199 S.
ISBN 978-3-8322-6981-4

ABISEA Band 48
Carstensen, Christian
Eddy Currents in Windings of Switched Reluctance Machines
1. Aufl. 2008, 179 S.
ISBN 978-3-8322-7118-3

ABISEA Band 49
Bohlen, Oliver
Impedance-based battery monitoring
1. Aufl. 2008, 190 S.
ISBN 978-3-8322-7606-5

ABISEA Band 50
Thele, Marc
A contribution to the modelling of the charge acceptance of lead-acid batteries - using frequency and time domain based concepts
1. Aufl. 2008, 165 S.
ISBN 978-3-8322-7659-1

ABISEA Band 51
König, Andreas
High Temperature DC-to-DC Converters for Downhole Applications
1. Aufl. 2009, 154 S.
ISBN 978-3-8322-8489-3

ABISEA Band 52
Dick, Christian Peter
Multi-Resonant Converters as Photovoltaic Module-Integrated Maximum Power Point Tracker
1. Aufl. 2010, 182 S.
ISBN 978-3-8322-9199-0

ABISEA Band 53
Kowal, Julia
Spatially resolved impedance of nonlinear inhomogeneous devices: using the example of lead-acid batteries
1. Aufl. 2010, 203 S.
ISBN 978-3-8322-9483-0

ABISEA Band 54
Roscher, Michael Andreas
Zustandserkennung von LiFeP04-Batterien für Hybrid- und Elektrofahrzeuge
1. Aufl. 2011, 186 S.
ISBN 978-3-8322-9738-1

ABISEA Band 55
Hirschmann, Dirk
Highly Dynamic Piezoelectric Positioning
1. Aufl. 2011, 146 S.
ISBN 978-3-8322-9746-6

ABISEA Band 56
Rigbers, Klaus
Highly Efficient Inverter Architectures for Three-Phase Grid Connection of Photovoltaic Generators
1. Aufl. 2011, 244 S.
ISBN 978-3-8322-9816-9

ABISEA Band 57
Kasper, Knut
Analysis and Control of the Acoustic Behavior of Switched Reluctance Drives
1. Aufl. 2011, 205 S.
ISBN 978-3-8322-9869-2

Aachener Beiträge des ISEA

ABISEA Band 58
Köllensperger, Peter
The Internally Commutated Thyristor - Concept, Design and Application
1. Aufl. 2011, 214 S.
ISBN 978-3-8322-9909-5

ABISEA Band 59
Schoenen, Timo
Einsatz eines DC/DC-Wandlers zur Spannungsanpassung zwischen Antrieb und Energiespeicher in Elektro-und Hybridfahrzeugen
1. Aufl. 2011, 128 S.
ISBN 978-3-8440-0622-3

ABISEA Band 60
Hennen, Martin
Switched Reluctance Direct Drive with Integrated Distributed Inverter
1. Aufl. 2012, 141 S.
ISBN 978-3-8440-0731-2

ABISEA Band 61
van Treek, Daniel
Position Sensorless Torque Control of Switched Reluctance Machines
1. Aufl. 2012, 144 S.
ISBN 978-3-8440-1014-5

ABISEA Band 62
Bragard, Michael
The Integrated Emitter Turn-Off Thyristor. An Innovative MOS-Gated High-Power Device
1. Aufl. 2012, 164 S.
ISBN 978-3-8440-1152-4

ABISEA Band 63
Gerschler, Jochen B.
Ortsaufgelöste Modellbildung von Lithium-Ionen-Systemen unter spezieller Berücksichtigung der Batteriealterung
1. Aufl. 2012, 334 S.
ISBN 978-3-8440-1307-8

ABISEA Band 64
Neuhaus, Christoph R.
Schaltstrategien für Geschaltete Reluktanzantriebe mit kleinem Zwischenkreis
1. Aufl. 2012, 133 S.
ISBN 978-3-8440-1487-7

ABISEA Band 65
Butschen, Thomas
Dual-ICT- A Clever Way to Unite Conduction and Switching Optimized Properties in a Single Wafer
1. Aufl. 2012, 168 S.
ISBN 978-3-8440-1771-7

ABISEA Band 66
Plum, Thomas
Design and Realization of High-Power MOS Turn-Off Thyristors
1. Aufl. 2013, 113 S.
ISBN 978-3-8440-1884-4

ABISEA Band 67
Kiel, Martin
Impedanzspektroskopie an Batterien unter besonderer Berücksichtigung von Batteriesensoren für den Feldeinsatz
1. Aufl. 2013, 226 S.
ISBN 978-3-8440-1973-5

ABISEA Band 68
Brauer, Helge
Schnelldrehender Geschalteter Reluktanzantrieb mit extremem Längendurchmesserverhältnis
1. Aufl. 2013, 192 S.
ISBN 978-3-8440-2345-9

ABISEA Band 69
Thomas, Stephan
A Medium-Voltage Multi-Level DC/DC Converter with High Voltage Transformation Ratio
1. Aufl. 2014, 226 S.
ISBN 978-3-8440-2605-4

ABISEA Band 70
Richter, Sebastian
Digitale Regelung von PWM Wechselrichtern mit niedrigen Trägerfrequenzen
1. Aufl. 2014, 126 S.
ISBN 978-3-8440-2641-2

ABISEA Band 71
Bösing, Matthias
Acoustic Modeling of Electrical Drives - Noise and Vibration Synthesis based on Force Response Superposition
1. Aufl. 2014, 188 S.
ISBN 978-3-8440-2752-5

ABISEA Band 72
Waag, Wladislaw
Adaptive algorithms for monitoring of lithium-ion batteries in electric vehicles
1. Aufl. 2014, 232 S.
ISBN 978-3-8440-2976-5

ABISEA Band 73
Sanders, Tilman
Spatially Resolved Electrical In-Situ Measurement Techniques for Fuel Cells
1. Aufl. 2014, 126 S.
ISBN 978-3-8440-3121-8

ABISEA Band 74
Baumhöfer, Thorsten
Statistische Betrachtung experimenteller Alterungsuntersuchungen an Lithium-Ionen Batterien
1. Aufl. 2015, 157 S.
ISBN 978-3-8440-3423-3

ABISEA Band 75
Andre, Dave
Systematic Characterization of Ageing Factors for High-Energy Lithium-Ion Cells and Approaches for Lifetime Modelling Regarding an Optimized Operating Strategy in Automotive Applications
1. Aufl. 2015, 196 S.
ISBN 978-3-8440-3587-2

ABISEA Band 76
Merei, Ghada
Optimization of off-grid hybrid PV-wind-diesel power supplies with multi-technology battery systems taking into account battery aging
1. Aufl. 2015, 184 S.
ISBN 978-3-8440-4148-4

ABISEA Band 77
Schulte, Dominik
Modellierung und experimentelle Validierung der Alterung von Blei-Säure Batterien durch inhomogene Stromverteilung und Säureschichtung
1. Aufl. 2016, 165 S.
ISBN 978-3-8440-4216-0

ABISEA Band 78
Schenk, Mareike
Simulative Untersuchung der Wicklungsverluste in Geschalteten Reluktanzmaschinen
1. Aufl. 2016, 126 S.
ISBN 978-3-8440-4282-5

ABISEA Band 79
Wang, Yu
Development of Dynamic Models with Spatial Resolution for Electrochemical Energy Converters as Basis for Control and Management Strategies
1. Aufl. 2016, 188 S.
ISBN 978-3-8440-4303-7

ABISEA Band 80
Ecker, Madeleine
Lithium Plating in Lithium-Ion Batteries:
An Experimental and Simulation Approach
1. Aufl. 2016, 154 S.
ISBN 978-3-8440-4525-3

ABISEA Band 81
Zhou, Wei
Modellbasierte Auslegungsmethode von Temperierungssystemen für Hochvolt-Batterien in Personenkraftfahrzeugen
1. Aufl. 2016, 175 S.
ISBN 978-3-8440-4589-5

ABISEA Band 82
Lunz, Benedikt
Deutschlands Stromversorgung im Jahr 2050
Ein szenariobasiertes Verfahren zur vergleichenden Bewertung von Systemvarianten und Flexibilitätsoptionen
1. Aufl. 2016, 187 S.
ISBN 978-3-8440-4627-4

ABISEA Band 83
Hofmann, Andreas G.
Direct Instantaneous Force Control: Key to Low-Noise Switched Reluctance Traction Drives
1. Aufl. 2016, 228 S.
ISBN 978-3-8440-4715-8

ABISEA Band 84
Budde-Meiwes, Heide
Dynamic Charge Acceptance of Lead-Acid Batteries for Micro-Hybrid Automotive Applications
1. Aufl. 2016, 157 S.
ISBN 978-3-8440-4733-2

ABISEA Band 85
Engel, Stefan P.
Thyristor-Based High-Power On-Load Tap Changers Control under Harsh Load Conditions
1. Aufl. 2016, 156 S.
ISBN 978-3-8440-4986-2

ABISEA Band 86
Van Hoek, Hauke
Design and Operation Considerations of Three-Phase Dual Active Bridge Converters for Low-Power Applications with Wide Voltage Ranges
1. Aufl. 2017, 231 S.
ISBN 978-3-8440-5011-0

ABISEA Band 87
Diekhans, Tobias
Wireless Charging of Electric Vehicles - a Pareto-Based Comparison of Power Electronic Topologies
1. Aufl. 2017, 151 S.
ISBN 978-3-8440-5048-6

ABISEA Band 88
Lehner, Susanne
Reliability Assessment of Lithium-Ion Battery Systems with Special Emphasis on Cell Performance Distribution
1. Aufl. 2017, 184 S.
ISBN 978-3-8440-5090-5

ABISEA Band 89
Käbitz, Stefan
Untersuchung der Alterung von Lithium-Ionen-Batterien mittels Elektroanalytik und elektrochemischer Impedanzspektroskopie
1. Aufl. 2016, 258 S.
DOI: 10.18154/RWTH-2016-12094

ABISEA Band 90
Witzenhausen, Heiko
Elektrische Batteriespeichermodelle: Modellbildung, Parameteridentifikation und Modellreduktion
1. Aufl. 2017, 266 S.
DOI: 10.18154/RWTH-2017-03437

ABISEA Band 91
Münnix, Jens
Einfluss von Stromstärke und Zyklentiefe auf graphitische Anoden
1. Aufl. 2017, 171 S.
DOI: 10.18154/RWTH-2017-01915

ABISEA Band 92
Pilatowicz, Grzegorz
Failure Detection and Battery Management Systems of Lead-Acid Batteries for Micro-Hybrid Vehicles
1. Aufl. 2017, 212 S.
DOI: 10.18154/RWTH-2017-09156

ABISEA Band 93
Drillkens, Julia
Aging in Electrochemical Double Layer Capacitors:
An Experimental and Modeling Approach
1. Aufl. 2017, 179 S.
DOI: 10.18154/RWTH-2018-223434

Aachener Beiträge des ISEA

ABISEA Band 94
Magnor, Dirk
Globale Optimierung netzgekoppelter PV-Batteriesysteme unter besonderer Berücksichtigung der Batteriealterung
1. Aufl. 2017, 210 S.
DOI: 10.18154/RWTH-2017-06592

ABISEA Band 95
Iliksu, Merve
Elucidation and Comparison of the Effects of Lithium Salts on Discharge Chemistry of Nonaqueous Li-O_2 Batteries
1. Aufl. 2018, 160 S.
DOI: 10.18154/RWTH-2018-223782

ABISEA Band 96
Schmalstieg, Johannes
Physikalisch-elektrochemische Simulation von Lithium-Ionen-Batterien: Implementierung, Parametrierung und Anwendung
1. Aufl. 2017, 168 S.
DOI: 10.18154/RWTH-2017-04693

ABISEA Band 97
Soltau, Nils
High-Power Medium-Voltage DC-DC Converters: Design, Control and Demonstration
1. Aufl. 2017, 176 S.
DOI: 10.18154/RWTH-2017-04084

ABISEA Band 98
Stieneker, Marco
Analysis of Medium-Voltage Direct-Current Collector Grids in Offshore Wind Parks
1. Aufl. 2017, 144 S.
DOI: 10.18154/RWTH-2017-04667

ABISEA Band 99
Masomtob, Manop
A New Conceptual Design of Battery Cell with an Internal Cooling Channel
1. Aufl. 2017, 167 S.
DOI: 10.18154/RWTH-2018-223281

ABISEA Band 100
Marongiu, Andrea
Performance and Aging Diagnostic on Lithium Iron Phosphate Batteries for Electric Vehicles and Vehicle-to-Grid Strategies
1. Aufl. 2017, 222 S.
DOI: 10.18154/RWTH-2017-09944

ABISEA Band 101
Gitis, Alexander
Flaw detection in the coating process of lithium-ion battery electrodes with acoustic guided waves
1. Aufl. 2017, 109 S.
DOI: 10.18154/RWTH-2017-099519

ABISEA Band 102
Neeb, Christoph
Packaging Technologies for Power Electronics in Automotive Applications
1. Aufl. 2017, 132 S.
DOI: 10.18154/RWTH-2018-224569

ABISEA Band 103
Adler, Felix
A Digital Hardware Platform for Distributed Real-Time Simulation of Power Electronic Systems
1. Aufl. 2017, 156 S.
DOI: 10.18154/RWTH-2017-10761

ABISEA Band 104
Becker, Jan
Flexible Dimensionierung und Optimierung hybrider Lithium-Ionenbatterie-speichersysteme mit verschiedenen Auslegungs-zielen
1. Aufl., 2017, 157 S.
DOI: 10.18154/RWTH-2017-09278

ABISEA Band 105
Warnecke, Alexander J.
Degradation Mechanisms in NMC Based Lithium-Ion Batteries
1. Aufl. 2017, 158 S.
DOI: 10.18154/RWTH-2017-09646

ABISEA Band 106
Taraborrelli, Silvano
Bidirectional Dual Active Bridge Converter using a Tap Changer for Extended Voltage Ranges
1. Aufl. 2017, 94 S.
DOI: 10.18154/RWTH-2018-228242

ABISEA Band 107
Sarriegi, Garikoitz
SiC and GaN Semiconductors: The Future Enablers of Compact and Efficient Converters for Electromobility
1. Aufl. 2017, 106 S.
DOI: 10.18154/RWTH-2018-227548

ABISEA Band 108
Senol, Murat
Drivetrain Integrated Dc-Dc Converters utilizing Zero Sequence Currents
1. Aufl. 2017, 134 S.
DOI: 10.18154/RWTH-2018-226170

ABISEA Band 109
Kojima, Tetsuya
Efficiency Optimized Control of Switched Reluctance Machines
1. Aufl. 2017, 142 S.
DOI: 10.18154/RWTH-2018-226697

ABISEA Band 110
Lewerenz, Meinert
Dissection and Quantitative Description of Aging of Lithium-Ion Batteries Using Non-Destructive Methods Validated by Post-Mortem-Analyses
1. Aufl. 2018, 139 S.
DOI: 10.18154/RWTH-2018-228663

ABISEA Band 111
Büngeler, Johannes
Optimierung der Verfügbarkeit und der Lebensdauer von Traktionsbatterien für den Einsatz in Flurförderfahrzeugen
1. Aufl. 2018, 171 S.
DOI: 10.18154/RWTH-2018-226569

ABISEA Band 112
Wegmann, Raphael
Betriebsstrategien und Potentialbewertung hybrider Batteriespeichersysteme in Elektrofahrzeugen
1. Auflage 2018, 184 S.
DOI: 10.18154/RWTH-2018-228833

ABISEA Band 113
Nordmann, Hannes
Batteriemanagementsysteme unter besonderer Berücksichtigung von Fehlererkennung und Peripherieanalyse
1. Aufl. 2018, 222 S.
DOI: 10.18154/RWTH-2018-228763

ABISEA Band 114
Engelmann, Georges
Reducing Device Stress and Switching Losses Using Active Gate Drivers and Improved Switching Cell Design
1. Aufl. 2018, 195 S.
DOI: 10.18154/RWTH-2018-228973

ABISEA Band 115
Klein-Heßling, Annegret
Active DC-Power Filters for Switched Reluctance Drives during Single-Pulse Operation
1. Aufl. 2018, 166 S.
DOI: 10.18154/RWTH-2018-231030

ABISEA Band 116
Burkhart, Bernhard
Switched Reluctance Generator for Range Extender Applications - Design, Control and Evaluation
1. Aufl. 2018, 194 S.
DOI: 10.18154/RWTH-2019-00025

ABISEA Band 117
Biskoping, Matthias
Discrete Modeling and Control of a versatile Power Electronic Test Bench with Special Focus on Central Photovoltaic Inverter Testing
1. Aufl. 2018, 236 S.
DOI: 10.18154/RWTH-2019-03346

ABISEA Band 118
Schubert, Michael
High-Precision Torque Control of Inverter-Fed Induction Machines with Instantaneous Phase Voltage Sensing
1. Aufl. 2019, 221 S.
DOI: 10.18154/RWTH-2018-231364

ABISEA Band 119
Van der Broeck, Christoph
Methodology for Thermal Modeling, Monitoring and Control of Power Electronic Modules
1. Aufl. 2019, 290 S.
DOI: 10.18154/RWTH-2019-01370

ABISEA Band 120
Hust, Friedrich Emanuel
Physico-chemically motivated parameterization and modelling of real-time capable lithium-ion battery models – a case study on the Tesla Model S battery
1. Aufl. 2019, 203 S.
DOI: 10.18154/RWTH-2019-00249

ABISEA Band 121
Ralev, Iliya
Accurate Torque Control of Position Sensorless Switched Reluctance Drives
1. Aufl. 2019, 154 S.
DOI: 10.18154/RWTH-2019-03071

ABISEA Band 122
Ayeng'o, Sarah Paul
Optimization of number of PV cells connected in series for a direct-coupled PV system with lead-acid and lithium-ion batteries
1. Aufl. 2019, 114 S.
DOI: 10.18154/RWTH-2019-01843

ABISEA Band 123
Koschik, Stefan Andreas
Permanenterregte Synchronmaschinen mit verteilter Einzelzahnsteuerung - Regelkonzepte und Betriebsstrategien für hochintegrierte Antriebssysteme
1. Aufl. 2019, 158 S.
DOI: 10.18154/RWTH-2019-03446

ABISEA Band 124
Farmann, Alexander
A comparative study of reduced-order equivalent circuit models for state-of-available-power prediction of lithium-ion batteries in electric vehicles
1. Aufl. 2019, 214 S.
DOI: 10.18154/RWTH-2019-04700

ABISEA Band 125
Mareev, Ivan
Analyse und Bewertung von batteriegetriebenen, oberleitungsversorgten und brennstoffzellengetriebenen Lastkraftwagen für den Einsatz im Güterfernverkehr in Deutschland
1. Aufl. 2019, 158 S.
DOI: 10.18154/RWTH-2019-04698

ABISEA Band 126
Qi, Fang
Online Model-predictive Thermal Management of Inverter-fed Electrical Machines
1. Aufl. 2019, 154 S.
DOI: 10.18154/RWTH-2019-08304

ABISEA Band 127
Kairies, Kai-Philipp
Auswirkungen dezentraler Solarstromspeicher auf Netzbetreiber und Energieversorger
1. Aufl. 2019, 140 S.
DOI: 10.18154/RWTH-2019-06706

Aachener Beiträge des ISEA

ABISEA Band 128
Fleischer, Michael
Traction control for Railway Vehicles
1. Aufl. 2019, 162 S.
DOI: 10.18154/RWTH-2019-10570

ABISEA Band 129
Teuber, Moritz
Lifetime Assessment and Degradation Mechanisms in Electric Double-Layer Capacitors
1. Aufl. 2019, 150 S.
DOI: 10.18154/RWTH-2019-10071

ABISEA Band 130
Bußar, Christian
Investigation of Optimal Transformation Pathways towards 2050 for the Successful Implementation of a Sustainable Reduction of Carbon Emissions from Power Generation
1. Aufl. 2019, 204 S.
DOI: 10.18154/RWTH-2019-09975

ABISEA Band 131
Wienhausen, Arne Hendrik
High Integration of Power Electronic Converters enabled by 3D Printing
1. Aufl. 2019, 146 S.
DOI: 10.18154/RWTH-2019-08746

ABISEA Band 132
Kwiecien, Monika
Electrochemical Impedance Spectroscopy on Lead-Acid Cells during Aging
1. Aufl. 2019, 138 S.
DOI: 10.18154/RWTH-2019-09480

ABISEA Band 133
Titiz, Furkan Kaan
A Three-phase Low-voltage Grid-connected Current Source Inverter
1. Aufl. 2019, 128 S.
DOI: 10.18154/RWTH-2020-00458

ABISEA Band 134
Wünsch, Martin
Separation der Kathoden-alterung in Lithium-Ionen-Batteriezellen mittels elektrochemischer Impedanzspektroskopie
1. Aufl. 2019, 177 S.
DOI: 10.18154/RWTH-2019-11017

ABISEA Band 135
Badeda, Julia
Modeling and Steering of Multi-Use Operation with Uninterruptible Power Supply Systems - utilizing the example of lead-acid batteries
1. Aufl. 2020, 282 S.
DOI: 10.18154/RWTH-2020-05456

ABISEA Band 136
Kleinsteinberg, Björn
Energy Efficiency Increase of a Vanadium Redox Flow Battery with a Power-Based Model
1. Aufl. 2020, 163 S.
DOI: 10.18154/RWTH-2020-06092

ABISEA Band 137
Cai, Zhuang
Optimization of dimension and operation strategy for a wind-battery energy system in German electricity market under consideration of battery ageing process
1. Aufl. 2020, 144 S.
DOI: 10.18154/RWTH-2020-06525

ABISEA Band 138
Sabet, Pouyan Shafiei
Analysis of Predominant Processes in Electrochemical Impedance Spectra and Investigation of Aging Processes of Lithium-Ion Batteries with Layered Oxide Cathodes and Graphitic Anodes
1. Aufl. 2020, 136 S.
DOI: 10.18154/RWTH-2020-07683

ABISEA Band 139
Angenendt, Georg
Operation, Optimization and Additional Market Participation of Households with PV Battery Storage System and Power-to-Heat Application
1. Aufl. 2020, 221 S.
DOI: 10.18154/RWTH-2020-05200

ABISEA Band 140
Oberdieck, Karl Friedrich
Measurement and Mitigation of Electromagnetic Emissions of Propulsion Inverters for Electric Vehicles
1. Aufl. 2020, 181 S.
DOI: 10.18154/RWTH-2020-09215

ABISEA Band 141
Bubert, Andreas Martin
Optimierung des elektrischen Antriebsstrangs von Elektrofahrzeugen mit Betrachtung parasitärer Ströme innerhalb der elektrischen Maschine
1. Aufl. 2020, 215 S.
DOI: 10.18154/RWTH-2020-09556

ABISEA Band 142
Fleischer, Christian Georg
Model-Driven Software Development and Verification Solutions for Safety Critical Battery Management Systems
1. Aufl. 2021, 356 S.
DOI: 10.18154/RWTH-2021-00436

ABISEA Band 143
Arzberger, Arno
Thermografische Methoden zur zerstörungsfreien Messung der anisotropen Wärmeleitfähigkeit von Lithium-Ionen Zellen
1. Aufl. 2020, 131 S.
DOI: 10.18154/RWTH-2021-00479

ABISEA Band 144
Lange, Tobias
Oberwellenbasierte Modellierung, Regelung und Auslegung von Permanentmagnet- und Reluktanz-Synchronmaschinen
1. Aufl. 2020, S.
DOI: 10.18154/RWTH-2021-02537

ABISEA Band 145
Weiss, Claude
Fault Tolerant Switched Reluctance Machines with Distributed Inverters – Modeling and Control
1. Aufl. 2020, S.
DOI: 10.18154/RWTH-2021-02327

ABISEA Band 146
Huck, Moritz
Modelling the Transient Behaviour of Lead-Acid Batteries: Electrochemical Impedance of Adsorbed Species
1. Aufl. 2020, 151 S.
DOI: 10.18154/RWTH-2020-08362

ABISEA Band 147
Willenberg, Lisa
Volumenausdehnung und ihre Auswirkungen auf die Alterung einer zylindrischen Lithium-Ionen-Batterie
1. Aufl. 2020, S.
DOI: 10.18154/RWTH-2021-01906

ABISEA Band 148
Rogge, Matthias
Electrification of Public Transport Bus Fleets with Battery Electric Busses
1. Aufl. 2020, 161 S.
DOI: 10.18154/RWTH-2021-02146

ABISEA Band 149
Münderlein, Jeanette
Numerische Methodik zur Auslegung eines Hybriden Speichersystems mit Multinutzen“
1. Aufl. 2020, 221 S.
DOI: 10.18154/RWTH-2021-00867

ABISEA Band 150
Merten, Michael
Participation of Battery Storage Systems in the Secondary Control Reserve Market
1. Aufl. 2020, 187 S.
DOI: 10.18154/RWTH-2021-01029

ABISEA Band 151
Ge, Lefei
Performance Enhancement of Switched Reluctance Machines for High-speed Back-up Generators
1. Aufl. 2020, 152 S.
DOI: 10.18154/RWTH-2020-11546

ABISEA Band 152
Neubert, Markus
Modeling, Synthesis and Operation of Multiport-Active Bridge Converters
1. Aufl. 2020, 227 S.
DOI: 10.18154/RWTH-2020-10814

ABISEA Band 153
Schülting, Philipp
Optimierte Auslegung von hochintegrierten und bidirektionalen Onboard GaN-Ladegeräten
1. Aufl. 2020, 158 S.
DOI: 10.18154/RWTH-2020-09771

ABISEA Band 154
Sewergin, Alexander
Design Challenges and Solutions for the Practical Application of SiC Power Moduls – Exemplified by an Automotive DC-DC Converter. 1. Aufl. 2021, 154 S.
DOI: 10.18154/RWTH-2021-04498

ABISEA Band 155
Stippich, Alexander
Exploiting the Full Potential of Silicon Carbide Devices via Optimized Highly Integrated Power Modules
1. Aufl. 2021, 188 S.
DOI: 10.18154/RWTH-2021-08122

ABISEA Band 156
Gottschlich, Jan
Hilfsspannungsversorgungskonzepte für Mittelspannungs-DC/DC-Wandler
1. Aufl. 2021, 178 S.
DOI: 10.18154/RWTH-2021-11881

ABISEA Band 157
Hollstegge, Philipp
Injektion raumzeigerzerlegter Stromharmonischer zur Minderung tonaler Geräuschanteile in asymmetrisch sechsphasigen Permanentmagnetsynchronmaschinen
1. Aufl. 2021, 191 S.
DOI: 10.18154/RWTH-2021-11040

ABISEA Band 158
Grau, Vivien
Development of a Test Bench to Investigate the Impact of Steep Voltage Slopes on the Lifetime of Insulation Systems for Coil Windings
1. Aufl. 2021, 182 S.
DOI: 10.18154/RWTH-2021-09577

ABISEA Band 159
Ringbeck, Florian
Optimized Charging of Lithium-Ion Batteries with Physico-Chemical Models
1. Aufl. 2021, 174 S.
DOI: 10.18154/RWTH-2021-11038

ABISEA Band 160
Bank, Thomas
Performance and Aging Analysis of High-Power Lithium Titanate Oxide Cells for Low-Voltage Vehicle Applications
1. Aufl. 2021, 148 S.
DOI: 10.18154/RWTH-2021-10369

Aachener Beiträge des ISEA

ABISEA Band 161
Aupperle, Felix
Realizing High-Performance Silicon-Based Lithium-Ion Batteries
1. Aufl. 2022, 138 S.
DOI: 10.18154/RWTH-2022-05155

ABISEA Band 162
Schröer, Philipp A.
Entwicklung einer adaptiven Leistungsprognosefunktion für Starterbatterien mit Lithium-Titanat-Oxid-Anode als Grundlage zur sicheren Energieversorgung im Fahrzeug
1. Aufl. 2021, 187 S.
DOI: 10.18154/RWTH-2021-10819

ABISEA Band 163
Dechent, Philipp
Simulation and Real-Life assessment of cell-to-cell variation of ageing lithium-ion batteries
1. Aufl. 2022, 149 S.
DOI: 10.18154/RWTH-2022-09298

ABISEA Band 164
Li, Weihan
Battery Digital Twin with Physics-Based Modeling, Battery Data and Machine Learning
1. Aufl. 2022, 234 S.
DOI: 10.18154/RWTH-2022-02292

ABISEA Band 165
Thien, Tjark G. C.
Optimaler Betrieb von stationären Hybrid-Batterie-speichern am Beispiel des Projekts M5BAT
1. Aufl. 2022, 172 S.
DOI: 10.18154/RWTH-2022-00997

ABISEA Band 166
Lüdecke, Christoph
Compensating Asymmetries of Parallel-Connected SiC MOSFETs Using Intelligent Gate Drivers
1. Aufl. 2022, 166 S.
DOI: 10.18154/RWTH-2022-09587

ABISEA Band 167
Rahe, Christiane
Untersuchung von Batterieelektroden mit optischen Verfahren
1. Aufl. 2022, 214 S.
DOI: 10.18154/RWTH-2022-08794

ABISEA Band 168
Weber, Felix Martin
Stability of lithium electrolyte interphase enabling rechargeable lithium-metal batteries
1. Aufl. 2023, 168 S.
DOI: 10.18154/RWTH-2023-03565

ABISEA Band 169
Henn, Jochen
Gate Driver Integrated Closed-Loop Control for Electromagnetic Emissions and Switching Losses of Wide Bandgap Power Electronic Converters
1. Aufl. 2023, 169 S.
DOI: 10.18154/RWTH-2023-07726

ABISEA Band 170
Quabeck, Stefan
Modeling of Parasitic Currents and Fault Detection in Electrical Traction Drives
1. Aufl. 2023, 133 S.
DOI: 10.18154/RWTH-2023-10920

ABISEA Band 171
Hecht, Christopher
Usage overview, prediction, and siting optimization for electric vehicles public charging infrastructure with machine learning and big data methods
1. Aufl. 2023, 185 S.
DOI: 10.18154/RWTH-2024-01156

ABISEA Band 172
Kuipers, Matthias L. U.
Development of a Virtual Cell Design Tool for Objective Comparisons between State-of-the-Art Battery Cells and Next Generation Technologies
1. Aufl. 2023, 203 S.
DOI: 10.18154/RWTH-2023-11897

ABISEA Band 173
Brieske, Daniel Martin
Anwendungsbezogene Modellierung und Zustandsbestimmung von Lithium-Schwefel-Batterien
1. Aufl. 2023, 146 S.
DOI: 10.18154/RWTH-2023-10905

ABISEA Band 174
Teichert, Philipp
Einfluss der Degradation von nickelreichen $Li[Ni_xMn_yCo_z]O_2$ (NMC) Elektroden (mit $x \geq 0.6$) auf Vollzellalterung von Lithium-Ionen-Zellen
1. Aufl. 2023, 159 S.
DOI: 10.18154/RWTH-2024-01059

ABISEA Band 175
Kühnle, Hannes Sebastian
Optical and electrochemical investigations of fundamental lithium metal deposition processes on lithium surfaces
1. Aufl. 2023, 218S.
DOI: 10.18154/RWTH-2024-05806

ABISEA Band 176
Epp, Alexander
Multiphysical Models and Optimization for Conceptual Design of High-Voltage Battery Systems
1. Aufl. 2024, 256 S.
DOI: 10.18154/RWTH-2024-00430

ABISEA Band 177
Figgener, Jan
Data-driven battery aging analysis of home storage systems based on high-resolution field measurements
1. Aufl. 2024, 208 S.
DOI: 10.18154/RWTH-2024-10709

ABISEA Band 178
Meishner, Fabian
Untersuchung eines direktnetzgekoppelten stationären LTO-Speichersystems in einem 750 V DC Stadtbahnnetz
1. Aufl. 2024, 116 S.
DOI: 10.18154/RWTH-2024-06358

ABISEA Band 179
Frambach, Tobias
Anwendungsgerechte Dimensionierung und Betriebsstrategien von 48 V Plug-In-Hybridfahrzeugen
1. Aufl. 2024, 154 S.
DOI: 10.18154/RWTH-2024-03411

ABISEA Band 180
Goldbeck, Rafael
Model-Based Control of Three-Phase Dual-Active Bridge Converters for Dynamic Operation and Adaptive Compensation of Parameter Deviations
1. Aufl. 2024, 194 S.
DOI: 10.18154/RWTH-2025-00288

ABISEA Band 181
Götz, Georg Tobias
Bidirectional DC-to-DC Converter with Integrated Switched Reluctance Generator
1. Aufl. 2024, 192 S.
DOI: 10.18154/RWTH-2024-03854

ABISEA Band 182
Harries, Martin
Aktive Reduzierung der Vibrationen von Permanentmagnet-Synchronmaschinen durch adaptive Regler
1. Aufl. 2024, 144 S.
DOI: 10.18154/RWTH-2025-00626

ABISEA Band 183
Börner, Martin Florian
Ein prozessbasiertes Modell zur Berechnung der Kosten von Lithium-Ionen-Batteriezellen
1. Aufl. 2024, 163 S.
DOI: 10.18154/RWTH-2024-07853

ABISEA Band 184
Bihn, Stephan
Automatic Parameterisation of Electrical Equivalent Circuit Models for Virtual Battery Cell Design
1. Aufl. 2024, 226 S.
DOI: 10.18154/RWTH-2024-10636

ABISEA Band 185
Xu, Huihui
Thermal Modeling and Control of an Oil-Cooled Permanent Magnet Synchronous Machine: Initialization, Nonlinearity, and Controllability
1. Aufl. 2025, 156 S.
10.18154/RWTH-2025-01683

ABISEA Band 186
Fritz, Niklas
Generalized Control Methodology for Modular DC-DC Converters
1. Aufl. 2025, 222 S.
DOI: 10.18154/RWTH-2025-04395

ABISEA Band 187
Kalker, Sven
Toward Robust Monitoring of Power Electronic Devices: Challenges and Efficient Solutions
1. Aufl. 2025, 167 S.
DOI: 10.18154/RWTH-2025-06121

ABISEA Band 188
Wasylowski, David
Accelerating Battery Cell Design, Manufacturing, and Testing through Ultrasound Imaging
1. Aufl. 2025, 116 S.
DOI: 10.18154/RWTH-2025-00940

ABISEA Band 189
Steininger, Valentin
Aging analysis of lithium-ion batteries with field data
1. Aufl. 2025, 136 S.
DOI: 10.18154/RWTH-2025-00625

ABISEA Band 190
Jacqué, Kevin
Analyse der Belastungsprofile, der Alterung und der Wirtschaft-lichkeit eines Batteriespeichers im Primärregelleistungsmarkt aus realen Feldmessdaten
1. Aufl. 2025, 244 S.
DOI: 10.18154/RWTH-2025-04328

ABISEA Band 191
Hamzelui, Niloofar
Investigation of active materials and polymeric binders in silicon-based negative electrodes for lithium-ion batteries
1. Aufl. 2025, 148 S.
DOI: 10.18154/RWTH-2025-06437

ABISEA Band 192
Klever, Severin
High-Bandwidth Current Probing Techniques for the Dynamic Characterization of Wide-Bandgap Semiconductor Devices
1. Aufl. 2025, 158 S.
DOI: 10.18154/RWTH-2025-03518

Many control strategies for electrical machines rely on magnetic flux-linkage as a key variable, especially in torque controllers based on field-oriented control algorithms. This variable is commonly determined using current-based LUTs or by integrating the measured PWM stator voltage. However, accurately measuring pulse-modulated voltages is challenging - particularly with SiC and GaN inverters - due to steep voltage slopes, high-frequency components, and switching delays, which are especially problematic in the low-speed range.

This research addresses these challenges by developing direct, precise volt-second sensing methods. Central to the work is a novel sensor combining analog and digital technologies, leveraging voltage-to-frequency converters (VFCs) and FPGA-based logic for enhanced accuracy and cost-effectiveness. A simulation model replicates volt-second distortions, with its performance validated against conventional techniques. Fourteen measurement methods are systematically evaluated for accuracy, instantaneousness, and cost utilizing a specialized test bench. The study underscores the potential of the invented discrete synchronous VFC (dSVFC) sensor for electric traction drive applications and PWM-less control, demonstrating its adaptability and precision.

Key contributions include advancing knowledge of VSI voltage distortions, refining mathematical models, and introducing innovative sensors adapted to inverter-specific requirements. The dissertation compares traditional and novel approaches, paving the way for more accurate, efficient, and cost-efficient solutions in research and industry.

ISSN 1437-675X