Gate-Termination Frequency Adaptation in a Self-Synchronous Inverse Class-F Rectifier

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***Abstract*—Owing to the time-reversal duality principle, the circuit of a power amplifier (PA) can be used as a rectifier. Such a rectifier is called a self-synchronous rectifier. In this case, the drain-side network of a PA is fed by the RF-power and the drain bias, connected to a DC-load, obtains rectified dc voltage. When the drain-side network is properly laid out for PA operation, the same network is appropriate for rectifier operation. The gate-side network is crucial for proper rectification, as it provides the synchronous excitation to the transistor gate. Its ideal configuration, however, differs from that of the PA mode. In this paper, the effects of changing the gate-side parameters termination resistance and bias voltage on a class-F^{-1} self-synchronous rectifier are reported. We present, to the authors' best knowledge, for the first time a shift in the frequency at which maximum rectification efficiency is achieved from 2.28 GHz to 2.44 GHz by a change in the gate termination resistance from 0 Ω to an open circuit, while the frequency steadily increases with increasing resistance. Consequently, peak efficiency of the rectifier can be shifted and controlled.**

***Index Terms*—Class-F^{-1}, Gate Termination, Gate Bias, Self-Synchronous Rectifier, Time Reversal Duality**

I. Introduction

At low AC frequencies, like wireless charging applications, diode rectifiers can accomplish high-efficiency RF-to-DC rectification even at high power [1]. When the frequency increases to several gigahertz, the power handling capability of diode rectifiers is very limited, as either the breakdown voltage of the diode is too low, its parasitic elements too large, or its recovery time too long. To accomplish efficient rectification of gigahertz-frequency RF signals at high input power, rectifiers using transistors have gained interest in recent years [2], [3]. One way to establish rectification with a transistor device is by making use of the time-reversal duality principle [4]. This principle states that a power amplifier can be operated as a rectifier without changing any of the drain-side circuitry [5]. In power amplifier configuration, an RF input power is fed through a gate-side network to the gate of a transistor with a gate bias of V_G, as shown in Fig. 1a. The drain of the transistor is biased at a voltage V_D, which provides the dc input power, and the amplified RF output power is delivered to the load through the drain-side network. To operate the same circuit as a rectifier, as shown in Fig. 1b, the drain-side network is fed by the RF input power, and the gate is still biased at a voltage V_G, while the gate side network is terminated by a resistance R_G. The rectified dc output power is delivered to the drain bias point where the load resistance, R_L, is connected. The circuit depicted in Fig. 1b relies on the parasitic capacitance between the gate and the drain terminal of the transistor to couple some of the input power to the gate side. The operation mode is therefore called self-synchronous. A distinction is made between a self-synchronous and a synchronous rectifier [6]. In the synchronous rectifier power is purposefully fed to the gate via a coupler and a phase shifter, as shown in Fig. 1c. The successful realisation of self-synchronous rectifiers has been reported in numerous papers for several power amplifier classes, from linear amplifiers, like class-C [7], to switch-mode

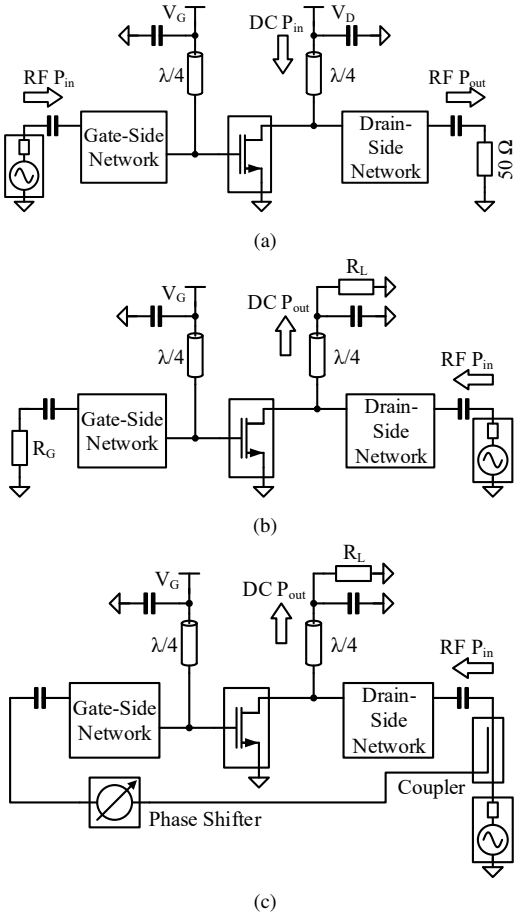

Fig. 1: Simplified diagrams of a transistor circuit operating as a power amplifier (a), as a self-synchronous rectifier (b) and a synchronous rectifier (c).

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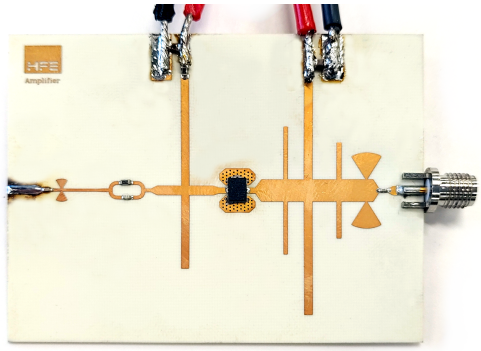

Fig. 2: Photograph of the self-synchronous rectifier. The board size is $69 \times 55.3\,\mathrm{mm}^2$.

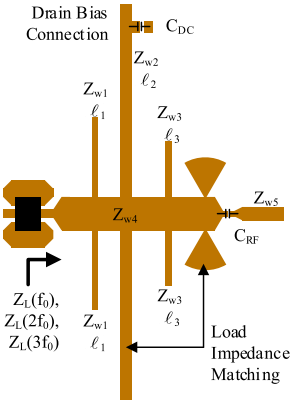

Fig. 3: The drain-side network.

amplifiers, like class-E [8], F [9] or F^{-1} [10]. As switch-mode designs usually can only deliver rectification at a narrow frequency band [7], the research on increasing the bandwidth for these devices is ongoing.

In this paper, a class-F^{-1} amplifier designed for a centre frequency of 2.45 GHz is used as a self-synchronous rectifier. We particularly investigate the effects of changes to the gate termination resistance, the gate bias voltage, as well as the load resistance over input power and frequency on the efficiency and output voltage of the rectifier. A shift in the frequency at which maximum rectification efficiency is achieved with a change in gate resistance is presented for the first time, to the authors' best knowledge. The gate termination resistance is increased from $0\,\Omega$ to an open circuit and a steady increase in this frequency is observed.

II. Class-F^{-1} Synchronous Rectifier

A photograph of the circuit board is shown in Fig. 2. The transistor used in this design is a surface-mount 6 W GaN-HEMT device, CGHV1F006S by Wolfspeed. At the gate-side a dampening circuit with a resistance of $47\,\Omega$ and a capacitance of 1 pF is encorporated. The RF connections are decoupled by 30 pF capacitors, C_{RF}, and the DC connections buffered by 1 nF capacitors, C_{DC}. The circuit is fabricated on a Rogers RO4350B substrate with 0.762 mm thickness and 17 μm copper thickness. The fabricated board size is $69 \times 55.3\,\mathrm{mm}^2$. The transistor source is connected to the backside ground plane with a via array to ensure a low inductance connection and proper thermal distribution. In Fig. 3 the drain-side network is depicted. The stubs Z_{w1} and Z_{w3} compose harmonic resonators to filter the second and third harmonic, respectively, obtaining class-F^{-1} operation. The characteristic impedances of the transmission lines, Z_{w1} to Z_{w5}, and electrical lengths, ℓ_1 to ℓ_3, are given in Table I. The bias network is realised via a quarter-wavelength transmission line and a bypass capacitor.

III. Measurement Setup

Fig. 4 gives an overview of the measurement setup. The RF signal generated by a vector signal generator is fed to the input of a driver amplifier, which outputs the desired power level, P_{in}. This power is then fed to the rectifier via a directional coupler, which allows the input power to be accurately measured by a power meter. Losses in the coupling measurement path are accounted for in measurement post-processing. The drain of the design is connected to an output load which is a resistance bank, R_L, composed of multiple resistors from Stackpole Electronics KAL 25 Watt series, via an ampere meter in series. A voltage meter measures the dc voltage across the load. Accurate output power measurement can be ensured by this way. A dc voltage source supplies the gate bias voltage, V_G. The gate termination resistances, R_G, from $0\,\Omega$ to $560\,\Omega$ are realised with SMD resistors. The measurement is carried out using Matlab with the GPIB communication protocol. The power efficiency, η, is calculated as

$$\eta = \frac{P_L}{P_G + P_{in}} = \frac{V_L \cdot I_L}{P_G + P_{in}} \approx \frac{V_L^2}{R_L \cdot (P_G + P_{in})}, \quad (1)$$

where P_L, P_G, and P_{in} are the load, gate bias, and input power, respectively, in W, V_L and I_L are the load voltage and current, and R_L is the load resistance. No mismatch compensation is included in the efficiency calculation.

TABLE I: Drain-side network parameters at $f = 2.45\,\mathrm{GHz}$.

Z_{w1}	ℓ_1	Z_{w2}	ℓ_2	Z_{w3}	ℓ_3	Z_{w4}	Z_{w5}
$80\,\Omega$	$\lambda/8$	$55\,\Omega$	$\lambda/4$	$75\,\Omega$	$\lambda/12$	$27\,\Omega$	$50\,\Omega$

IV. Measurement Results

To observe the effects on the performance of the self-synchronous rectifier by means of power efficiency and load voltage, the gate termination, R_G, the gate bias voltage, V_G, the load resistance, R_L, the input frequency, f, and the input power, P_{in}, were varied.

A. Gate Termination

The gate termination was varied from a short circuit to an open circuit on a purely real impedance scale while gate bias voltage, input power, and load resistance were kept

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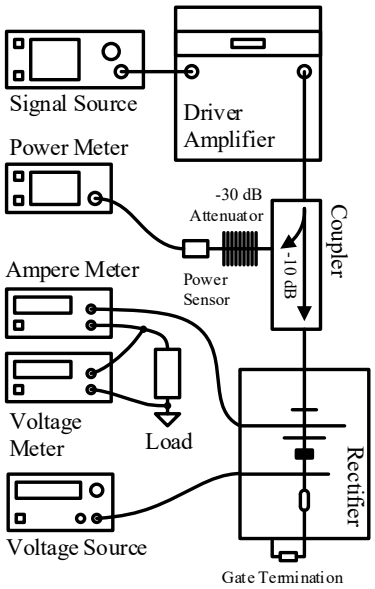

Fig. 4: Block diagram of the measurement setup.

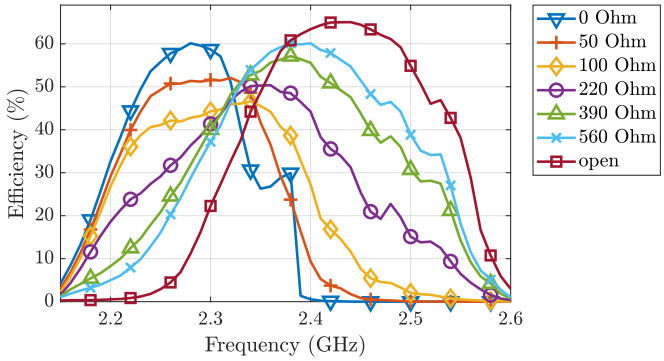

Fig. 5: Power efficiency over frequency for varying gate terminations at: $V_G = -4\,\mathrm{V}$, $P_{in} = 35.5\,\mathrm{dBm}$ and $R_L = 175\,\Omega$.

constant at $V_G = -4\,\mathrm{V}$, $P_{in} = 35.5\,\mathrm{dBm}$ and $R_L = 175\,\Omega$. Fig. 5 shows the power efficiency over the frequency for each of the termination values. At $R_G = 0\,\Omega$ the frequency range in which the efficiency is above 50 % is 2.23 GHz to 2.32 GHz. At $R_G = 390\,\Omega$ it has shifted to 2.33 GHz to 2.43 GHz, and at an open termination it lies between 2.35 GHz and 2.51 GHz. The sensible operational range is shifting to higher frequencies for higher ohmic gate termination values.

The results were rearranged and summarised as shown in Fig. 6. The frequency at which maximum efficiency is obtained for each termination resistance is plotted on the left y-axis. The frequency monotonically increases from 2.28 GHz to 2.44 GHz towards higher R_G values. On the right y-axis the maximum efficiency is given. The peak efficiencies of 60.1 % and 65.0 % are obtained at the short and open

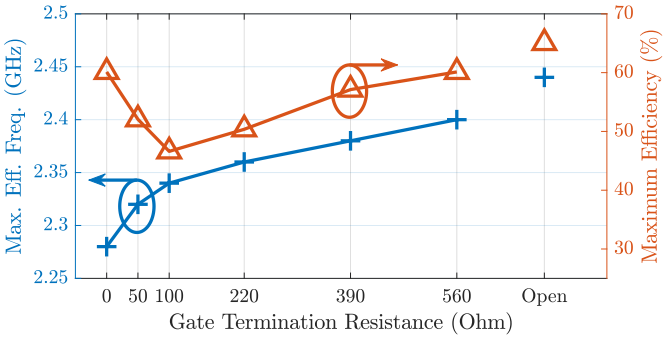

Fig. 6: Frequency of maximum efficiency (left axis) and according maximum efficiency (right axis) over gate termination at: $V_G = -4\,\mathrm{V}$, $P_{in} = 35.5\,\mathrm{dBm}$ and $R_L = 175\,\Omega$.

terminations, respectively. At $R_G = 100\,\Omega$ the maximum available efficiency drops to 46.6 %. However, in Fig. 5 it is visible that at this gate termination this comparatively low efficiency is reached over a broader frequency range. The measured data suggests that the operational range of the class-F^{-1} can be adapted by means of the termination of the gate port.

B. Gate Bias Voltage

The gate voltage was varied from -6 V to -3.5 V over an input power from 30 dBm to 40 dBm, while keeping the frequency and load resistance at $f = 2.45\,\mathrm{GHz}$ and $R_L = 175\,\Omega$ for the open gate termination case. Fig. 7 shows the efficiency over input power for the gate voltage values on the left axis and the respective load voltage on the right axis. The efficiency curve is the highest nearly over the whole input power range for a gate bias voltage of -4 V and for all gate bias voltages the maximum efficiency can be found at approximately 37 dBm input power. From -4 V to -3.5 V the efficiency drops steeply, while towards higher negative voltages the decay is slower. The load voltage increases steadily with increasing input power, as is expected. The highest voltages are measured at -4 V over nearly the whole input power range as well, which is reasonable according to (1). The highest efficiency was measured at $V_G = -4.2\,\mathrm{V}$ and $P_{in} = 37.2\,\mathrm{dBm}$ at 66.9 %. In [11] a shift in peak efficiency over input power due to changing the gate bias voltage has been reported for a GaAs HEMT rectifier. However, we haven't observed such a shift for the GaN HEMT self-synchronous rectifier in this design.

C. Load Resistance

The load resistance was varied from $50\,\Omega$ to $200\,\Omega$ at an open gate termination and $V_G = -4\,\mathrm{V}$. In Fig. 8 the measured output load voltage over frequency at an input power of 36 dBm is shown. No significant frequency shift can be observed. The maximum output dc voltage is at 2.4 GHz regardless of the output loads. Fig. 9 plots the measured

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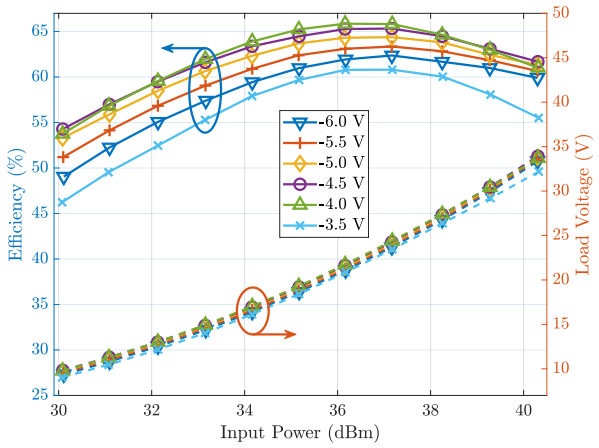

Fig. 7: Measured efficiency (left axis) and load voltage (right axis) over input power for varying gate voltages at: $f = 2.45\,\text{GHz}$, open gate termination and $R_L = 175\,\Omega$.

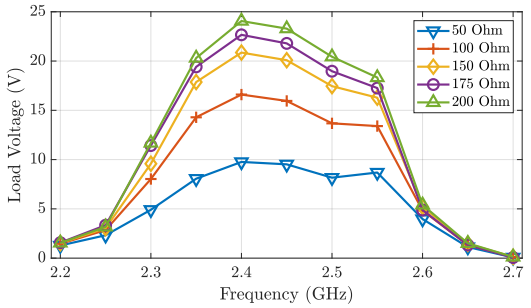

Fig. 8: Measured load voltage over frequency for varying load resistances at: $V_G = -4\,\text{V}$, open gate termination and $P_{in} = 36\,\text{dBm}$.

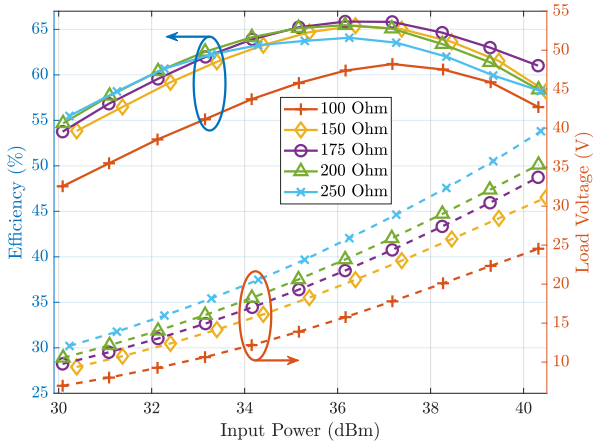

Fig. 9: Measured efficiency (left axis) and load voltage (right axis) over input power for varying load resistances at: $f = 2.45\,\text{GHz}$, open gate termination and $V_G = -4\,\text{V}$.

efficiency over input power on the left y-axis and the output load voltage on the right y-axis at a frequency of 2.45 GHz. The highest efficiency is obtained at $R_L = 175\,\Omega$. The load voltage rises with higher ohmic dc load.

V. Conclusion

We have presented the design and the measurement results for a class-F^{-1} self-synchronous GaN-HEMT rectifier under varying gate termination, gate bias, and dc load conditions. A frequency shift from 2.28 GHz to 2.44 GHz in the maximum achievable rectifier efficiency due to a change in the gate termination resistance has been reported for the first time, to the authors' best knowledge. This behaviour reveals the possibility for more broadband as well as reconfigurable designs of high-efficiency switch-mode self-synchronous rectifiers employing time-reversal duality in the future.

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