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Influence of Top Electrode Metal on Resistive Switching in Multilayer MOCVD MoS₂ Memristors

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ABSTRACT

Two-dimensional (2D) materials such as molybdenum disulfide (MoS₂) show promise for memristor applications. Most MoS₂ memristors use vertical metal/MoS₂/metal stacks with gold or silver active electrodes and rely on electron-beam evaporation; sputtering is seldom used. This study investigates palladium (Pd), nickel (Ni), and aluminum (Al) as electrodes and compares resistive switching (RS) performance for sputtered versus evaporated top electrodes. Pd acts as a passive electrode with minimal contribution to RS. Devices with Ni active electrodes exhibit very low initial resistance and a small RS window, consistent with deposition-induced damage to MoS₂. Sputtered Al yields highly reproducible RS in Pd/MoS₂/Al memristors, achieving 95% yield across 64 devices. In contrast, evaporated Al forms a parasitic oxide at the Al/MoS₂ interface that inhibits RS, even when deposited at a base pressure comparable to that of sputtered Al. Area scaling and temperature-dependent measurements indicate Al filament formation and dissolution via electrochemical metallization as the RS mechanism. Metal-specific energy barriers for filament formation explain the superior performance of sputtered Al. Overall, the results identify Al as an effective active electrode within the investigated device architecture and show that sputtering is a viable alternative for top-electrode deposition because it suppresses interfacial oxide formation.

1 | Introduction

Two-dimensional (2D) materials are emerging as key materials for next-generation electronic devices [1, 2, 3], including memristors [4–9, 10]. They offer several potential advantages for memristors, such as fast and low-power switching, large resistive switching (RS) windows, forming-free operation, utilization on arbitrary substrates by layer transfer, and ultimate thickness scaling [8–10, 11]. The transition metal dichalcogenide molybdenum disulfide (MoS₂) is one of the most extensively studied 2D

materials for memristors [7, 12–27, 28]. This is due to its early discovery [29, 30, 31], well-controllable growth methods [32, 33, 34], and a suitable bandgap [30].

The RS behavior in MoS₂ memristors has been explained by a filamentary mechanism. Metal atoms or ions supplied by the active electrode migrate and form a filament during the SET transition, switching the device from a high-resistance state (HRS) to a low-resistance state (LRS) [14, 19, 20, 22, 26, 27, 16, 35]. During the RESET process, the filament is dissolved again.

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The filaments are formed via metal atom or ion substitutions of sulfur vacancies, called conductive points, in monolayer MoS₂ [19, 26]. In the case of multilayer MoS₂, filaments are thought to be formed via metal ion diffusion through grain boundaries [14, 22, 16, 36], which is comparable to the electrochemical metallization (ECM) process described for oxide memristors [37, 38]. Therefore, the choice of metal for the active electrode plays a significant role in the RS behavior of multilayer MoS₂. Gold (Au), known for its inertness that prevents the formation of parasitic metal oxides in the device stack, and silver (Ag), recognized for its electrochemical activity, are predominantly used as active electrodes in MoS₂ memristors [7, 12, 13, 14, 16, 17, 19, 20, 24, 26, 28, 39–41, 42]. In contrast, other metals are more rarely explored [15, 21, 43–45, 46]. Additionally, electron-beam evaporation is widely used to deposit memristor electrodes, while sputtering is mostly avoided, due to its tendency to cause greater damage to 2D materials [47, 48, 49].

In this study, we investigate crosspoint-type memristors with multilayer MoS₂ grown by metal–organic chemical vapor deposition (MOCVD) as the switching material. We employ palladium (Pd) as the back electrode (BE) and explore Pd, nickel (Ni), and aluminum (Al) as top electrodes (TEs). Pd was used as the passive BE, similar to the more commonly used platinum [50] for all devices. Additionally, devices in which Pd served as both the BE and the TE were fabricated to investigate whether Pd can function as an active metal for filament formation in MoS₂. Al and Ni were investigated as active electrodes because they are reactive metals, low-cost, and widely available. Additionally, a recent simulation study demonstrated that Al exhibits beneficial energy barriers for metallic filament formation through grain boundaries in multilayer MoS₂ [36]. We systematically compare electron-beam evaporation and sputtering for Ni and Al to examine how different top electrode metals and deposition methods influence the device interface morphology and RS performance. All devices were fabricated using the same MOCVD-grown MoS₂ films, with identical bottom electrodes and device geometries, to isolate the influence of the top electrode metal and deposition method.

2 | Device Fabrication

We fabricated five types of vertical memristors with $\sim 20 \mu\text{m}^2$ active device areas by sandwiching multilayer MoS₂ between different metal electrodes. Figure 1a shows a schematic of the general device structure. All samples had Pd BEs, but the TE metal and deposition methods varied. We fabricated symmetric devices with a Pd-TE deposited by electron-beam evaporation, referred to as Pd_{ev}, to evaluate the role of Pd. In addition, we built devices with Ni- and Al-TEs deposited either by electron-beam evaporation, referred to as Ni_{ev} and Al_{ev}, or by direct current (dc) sputtering, referred to as Ni_{sp} and Al_{sp}. Exemplary microscope images of a device from the Al_{sp} sample are shown in Figure 1b,c. Microscope images of the other four samples are shown in the supplementary information (SI) Figure S1.

The multilayer MoS₂ for the memristors was grown on 2" sapphire wafers in an AIXTRON MOCVD reactor. An atomic force microscopy (AFM) surface scan of the as-grown MoS₂ on

sapphire (Figure 1d) reveals triangular and hexagonal crystal grains on a coalesced multilayer MoS₂ film. An AFM scan of the transferred MoS₂ on a SiO₂/Si substrate for device fabrication (Figure S2) shows a thickness of $6.9 \pm 0.9 \text{ nm}$ (~ 11 layers). The transferred MoS₂ film shows typical surface contamination, likely from polymer residues and wrinkles from transfer.

Figure 1e shows a Raman spectrum of as-grown MoS₂ with its two characteristic peaks. Further fabrication details and the MoS₂ growth process are described in the Methods section. Additional Raman spectroscopy results for all samples are presented in Figure S3. The results show no significant alteration of the material through the fabrication process. The Raman maps in Figure S4 validate the successful patterning of MoS₂ across all the samples.

3 | Results and Discussion

3.1 | Resistive Switching With Different TE Metals

This Section compares the initial resistance, resistive switching yield, and cycling behavior of MoS₂ memristors fabricated with different TE metals. The analysis identifies sputtered Al as the most suitable TE among those investigated and motivates the detailed characterization presented in subsequent Sections.

Initial resistance measurements with $V_{\text{read}} = 10 \text{ mV}$ (Figure 2) of at least 37 MoS₂ memristors per sample reveal strong TE-dependent differences. The Al_{ev} sample exhibits extremely high resistances (median 94 G Ω), indicating the presence of an insulating interfacial layer, as discussed later in the structural analysis (Section 3.3). Pd_{ev} devices show the second-highest resistances (median 76 k Ω), consistent with a van der Waals (vdW) interface formed between MoS₂ and the noble metal Pd and no interfacial reaction [51, 52, 53]. In contrast, both Ni-based samples, Ni_{ev} and Ni_{sp}, exhibit much lower resistances (median of 3 k Ω and 930 Ω , respectively). This is attributed to deposition-induced damage and penetration of Ni into the MoS₂ multilayer [47, 49, 54–56, 57]. Several Ni-TE devices show initial resistances below 1 k Ω , which indicates the formation of conductive clusters (filaments) directly after TE deposition. The Al_{sp} devices exhibit intermediate initial resistances (median 42 k Ω), comparable to Pd-based devices, and significantly higher than those observed for Ni-based samples.

We conclude that Pd evaporation and Al sputtering did not cause any significant damage to MoS₂. The seemingly contradictory result that highly energetic sputtering did not damage a 2D material can be explained by the low atomic weight of Al when compared to the other metals (Pd: 106.42 u, Ni: 58.69 u, Al: 26.98 u) [58], and a lower kinetic energy of sputtered Al compared to other metals [59].

Details on the electrical measurement setup for the initial resistance measurements and the following dc current-voltage (I - V) sweeps are included in the Methods Section.

Control devices without MoS₂ on each sample exhibit linear ohmic behavior, low resistances, and no RS (Figure S5), confirming clean metallic BE-TE contacts without parasitic layers.

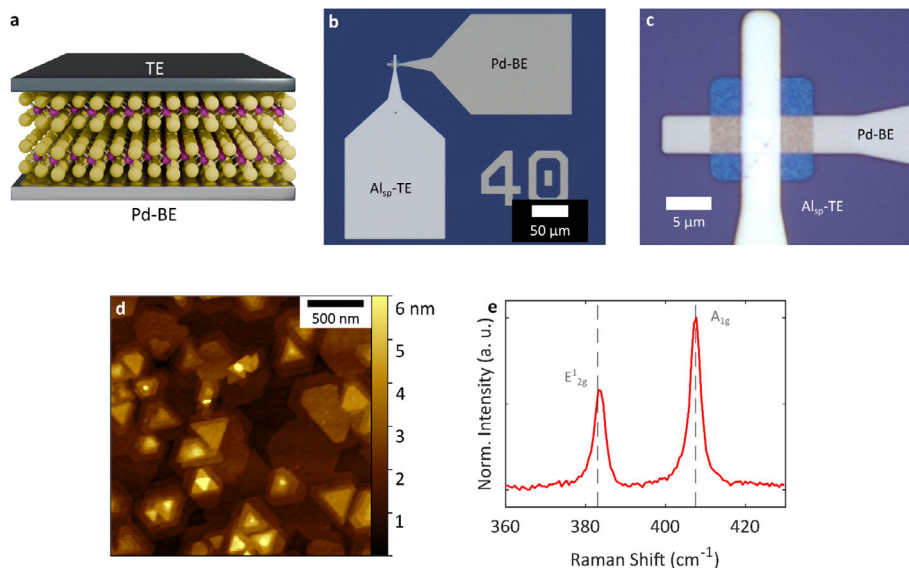


FIGURE 1 | Device structure and material analysis. (a) Schematic structure of the active area of the fabricated memristor devices. The metals used for the TE are Pd, Ni, and Al. (b) Microscope image of an Al_{sp} device showing the electrode contact pads. (c) Zoomed-in microscope image of the Al_{sp} device in (b), showing the active region. (d) AFM scan of the as-grown MOCVD MoS₂ on sapphire used for all devices in this study. (e) Raman spectrum of the as-grown MoS₂ showing the characteristic spectral fingerprint with the E'_{2g} and A_{1g} peaks.

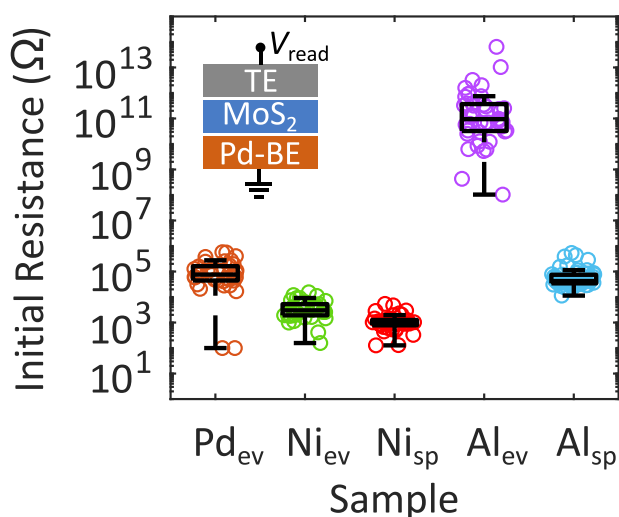


FIGURE 2 | Box plots of the initial resistances of MoS₂ memristors in each sample, measured with a read voltage (V_{read}) of 10 mV. The boxplots summarize 37 measurements for Pd_{ev} and both Ni samples, and 44 and 58 devices for Al_{ev} and Al_{sp}, respectively. The inset shows the schematic device structure and how the devices were biased.

Next, we applied dc I - V sweeps to the MoS₂ memristors in each sample to test the TE-dependent RS behavior. In each sample, 37 devices were tested, except for Al_{sp}, in which 64 devices were evaluated. Details on the testing routine are described in the Methods Section.

First, the number of devices exhibiting basic RS functionality was determined for each sample. For the yield analysis, a device was counted as showing RS if it transitioned from an HRS to an LRS and back at least once during dc I - V testing. The required

resistance ratio is $R_{\text{HRS}}/R_{\text{LRS}} \geq 5$. Several memristor studies with emerging materials use similar yield criteria [12, 13, 17, 60]. The RS yield of all samples, according to the aforementioned criteria, is visualized in the bar graph in Figure 3a. 3 out of 37 Pd_{ev} (8.1%), 12 out of 37 Ni_{ev} (32.4%), 4 out of 37 Ni_{sp} (10.8%), 4 out of 37 Al_{ev} (10.8%), and 61 out of 64 Al_{sp} devices (95%) showed at least one RS cycle with the minimum resistance ratio. A higher number of devices were tested for the Al_{sp} sample due to its superior initial performance. Most failed devices showed a breakdown to a permanent LRS after a single positive voltage sweep (three exemplary devices for each sample are presented in Figures S6–S10 for the details). This type of failure is typical for 2D memristors and has been associated with the irreversible formation of excessive conductive clusters in the switching layer from metal penetration [12]. In contrast, the majority of the failed Al_{ev} devices remained in a permanent HRS, even after applying high voltages up to ± 8 V (Figure S9), showing no controlled resistance change.

Figure 3b–f shows representative I - V characteristics of one RS device for each sample. The Pd_{ev} device exhibits one RS cycle but breaks down during the second SET transition. Both Ni-TE devices show low initial resistances and a narrow switching window. Ni_{ev} shows 14 RS cycles without failure. Due to low resistance values of the device in both resistance states, very high currents (~ 10 mA) flow during SET and RESET. This results in high power consumption, making the devices unsuitable for the envisaged memristor applications [61]. Hence, continued cycling was deemed unnecessary. The Ni_{sp} device showed one RS cycle but broke down during the second SET transition. The Al_{ev} device exhibits RS under comparatively high voltages, with the largest switching window of all samples, and stayed in a permanent HRS after only one cycle. In contrast, the Al_{sp} device shows stable, repeatable RS over 200

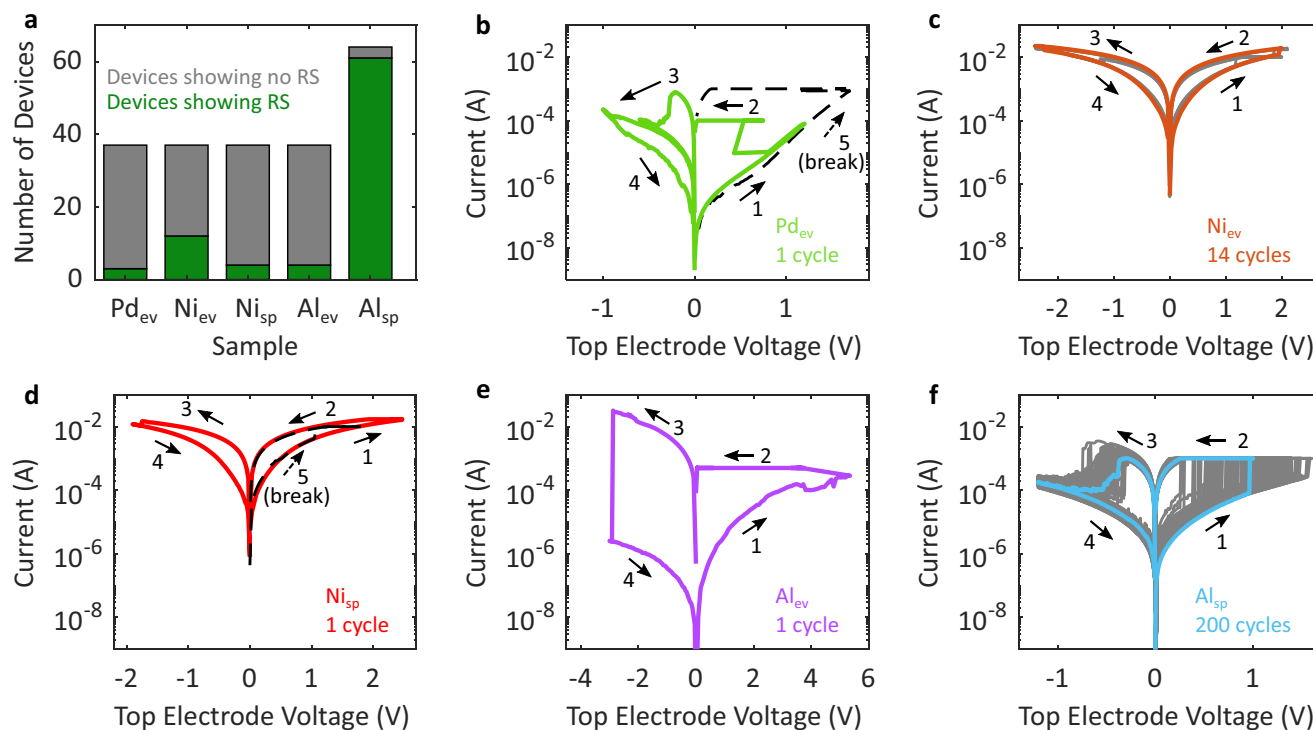


FIGURE 3 | Resistive switching (RS) results for different TE variations. (a) Bar graph summarizing the number of devices that showed RS out of all tested devices for each TE variation: 3 out of 37 for Pd_{ev}, 12 out of 37 for Ni_{ev}, 4 out of 37 for Ni_{sp}, 4 out of 37 for Al_{ev}, and 61 out of 64 for Al_{sp}. (b) One full RS cycle in a Pd_{ev} device, showing a two-step RESET process and subsequent breakdown (sweep number 5, indicated by the black dashed curve). (c) 14 RS cycles in a Ni_{ev}-TE device. (d) One RS cycle in a Ni_{sp}-TE device followed by breakdown during sweep number 5 (black dashed curve). (e) One RS cycle in an Al_{ev}-TE device. (f) 200 RS cycles in an Al_{sp} device. Note that the X-axis scales vary to accommodate the different voltage ranges required for each device, while the Y-axis scales are identical. Arrows and numbers indicate the sweep sequence and direction; the first cycle is colored.

consecutive cycles without breakdown. Additional *I-V* curves for all RS devices are provided in Figures S11–S17 and show behavior consistent with the representative devices shown in Figure 3.

In summary, only the Al_{sp} sample shows repeatable and stable RS behavior. Four more devices exhibiting over 100 RS cycles are illustrated in Figure S15. Many of the other tested devices were also evaluated over multiple RS cycles (Figures S16 and S17). Altogether, 1735 RS cycles in 61 devices were recorded for Al_{sp}, indicating consistent switching performance. None of the 61 Al_{sp} devices included in the yield assessment failed during dc *I-V* testing.

All other TE variations suffered from limitations such as low yield of RS devices, low cycling capability and early breakdown, excessive currents, or a too narrow switching window, making them unsuitable for practical memristor applications. Notably, the evaporated Al-TE sample (Al_{ev}), in contrast to Al_{sp}, shows a low RS yield and significantly higher resistances and switching voltages. Therefore, we focused on structural characterization of both samples and conducted additional electrical characterization [61, 62] on the Al_{sp} devices, identified as the most promising from the initial *I-V* measurements. The unusual difference between sputtered and evaporated Al will be further addressed in Section 3.3. The switching mechanism and the vast differences in the RS behavior and yield for the different TE-metals will be discussed in Section 3.4.

3.2 | Performance of the Sputtered Al-TE Sample

Table S1 in the SI compares the number of tested devices, the yield, the yield criteria, and the discussion of failed devices of our study to 19 vertical MoS₂ memristor studies in the literature [7, 12–17, 18, 20, 21, 23, 24, 39, 40, 43, 44, 46, 63, 64]. This comparison shows that our work achieves one of the highest reported yields among vertical MoS₂ memristors. More importantly, it provides the most comprehensive and explicitly defined dataset in terms of yield evaluation, including many tested devices, clearly stated yield criteria, and a discussion of failed devices. Such a level of explicit yield definition and failure analysis is not consistently reported in prior studies, where yield is either not mentioned, or the yield criteria are not clearly defined.

The device-to-device (D2D) and cycle-to-cycle (C2C) variabilities of eight devices exhibiting the highest number of dc switching cycles are visualized by boxplots of the resistances and the switching voltages in Figure S18. The devices include those shown in Figure 3f and Figure S15, along with three additional devices that completed 77, 75, and 53 dc cycles, respectively (the devices are labeled from 1 to 8). Significant D2D and C2C variabilities are visible.

A direct comparison with the literature is challenging, because only few studies provide numerical variability values [21, 24, 40, 43, 64], whereas most studies present it qualitatively via plots [7, 12–17, 18, 20, 23, 39, 44, 46, 63]. Calculating the coefficient of

variation (CV) of the switching voltages ($CV = \sigma/V_{\text{mean}}$) of the eight memristors with the most cycles (822 in total) results in the numerical C2C (V_{SET} : 29%; V_{RESET} : 24.4%) and D2D (V_{SET} : 24.3%; V_{RESET} : 20.5%) variabilities. Two previous studies report lower C2C variabilities [24, 43]. However, these values are obtained under substantially different experimental conditions. In reference [24], exfoliated MoS_2 was used, which provides near-ideal crystal quality but is not compatible with scalable fabrication, and the reported C2C variability is based on only 56 cycles measured in a single device. In reference [43], C2C variability is extracted from 100 cycles in one device employing large-area (200 μm) devices with a common BE, a configuration that is not representative for scalable memristor fabrication [61]. Consequently, while lower CV values are reported in these studies, the present work provides a more statistically robust assessment of switching variability under scalable material growth and device configurations, which is critical for evaluating the practical viability of MoS_2 -based memristors.

Regarding D2D variability, one study reports significantly lower values [64]. However, direct comparison is limited, as reference [64] employs large-area devices with a common back electrode, which is not representative of scalable memristor architectures. In contrast, two studies that fabricate scalable crossbar devices using CVD-grown MoS_2 and evaluate a statistically meaningful number of devices report D2D variabilities that are significantly higher [40] and slightly lower [21] than those observed in this work. These results indicate that the D2D variability reported here is within the typical range of values observed for scalable MoS_2 -based memristors.

The D2D variability is typically related to the fabrication conditions, for example, inhomogeneous interfaces that can appear because of the 2D material transfer process [61]. It can be reduced by improving the fabrication conditions. Overall, there is a need for more standardized metrics in 2D memristor publications to simplify comparison [61, 62, 65, 66].

The state retention was measured for two Al_{sp} devices to verify the non-volatility of the RS. Each device was first switched through for a full cycle and then SET to the LRS. The LRS resistance was continuously measured at a read voltage of 10 mV for 14 h. Afterward, the devices were stored under ambient condition for a week, after which the resistance was remeasured for 10 min. The same measurement protocol was then repeated for the HRS. Both devices showed stable state retention for at least 7 days (Figure 4a).

The endurance was evaluated by switching ten fresh Al_{sp} devices until breakdown, using both dc I - V sweeps and pulsed voltage stress (PVS). One device under dc operation showed an endurance of 677 cycles with stable resistance values (Figure 4b), while another device under PVS switched for 526 cycles with slightly higher resistance variations (Figure 4b). Eight additional PVS devices exhibited endurance values between 118 and 267 cycles, as depicted in Figure S19. All devices ultimately failed by irreversibly switching to the LRS, after which a RESET was no longer possible. During PVS, pulses with a width of 5 μs , rise and fall times of 500 ns, and a current compliance of $I_{\text{CC}} = 400 \mu\text{A}$ were used for the SET transition (see exemplary I - V - t plot in Figure 4c). The HRS and LRS resistances were measured

by applying a dc read voltage of 10 mV before and after each pulse.

A significant current overshoot up to 5 mA was observed during the SET transition before the voltage was regulated down to limit the current to 400 μA (Figure 4c). This overshoot and a limited controllability of current in the memristor in general are the main factors restricting the endurance of 2D material memristors [4, 67]. The overshoot happens because of the relatively slow current compliance response of commercial semiconductor parameter analyzers (SPA) [68]. Potential solutions for this issue include the use of specialized fast-response measurement setups [68] or integration of the memristor with complementary metal oxide semiconductor (CMOS) transistors [4, 5, 6].

The energy consumption of the Al_{sp} memristors was analyzed by PVS measurements. We switched two devices with the same parameters as shown in Figure 4c for 20 and 15 cycles, respectively (Figure S20a,b). The resulting energy consumptions are $E_{\text{SET}} = 1.1 \pm 0.1 \text{ nJ}$ and $E_{\text{RESET}} = 8.6 \pm 0.7 \text{ nJ}$, obtained by computing the electric power ($P = I \cdot V$) and numerically integrating P over the full duration of SET and RESET pulse, respectively. Both plots show a current overshoot before the voltage is reduced to limit the current to I_{CC} . Switching happens much faster than the applied voltage pulse width, which leads to unnecessary energy expenditure after the switching has already happened.

We applied the shortest possible voltage pulses, limited by our measurement equipment to $\sim 100 \text{ ns}$, to get the fastest accessible switching time and to reduce energy consumption. Figure 4d and Figure S20c show six consecutive fast switching cycles for one device each, respectively. The average switching times for both devices are $t_{\text{SET}} = 50 \pm 2 \text{ ns}$ and $t_{\text{RESET}} = 75 \pm 3 \text{ ns}$, with corresponding energy consumptions of $E_{\text{SET}} = 100 \pm 11 \text{ pJ}$ and $E_{\text{RESET}} = 513 \pm 36 \text{ pJ}$. Figure 4e shows the I - V plot of a representative pulse in Figure 4d that confirms that the SET and RESET transitions occurred. The resistances were measured via a dc read voltage of 10 mV before and after the pulses to confirm successful switching, as for the endurance measurements. Figure 4d and Figure S20c show no engagement of I_{CC} (400 μA) during the fast pulse. The currents reach up to 8 mA because the current compliance of the SPA is too slow for the nanosecond pulse [68]. Solutions to this issue are the same as those discussed previously for the limited endurance.

The average dc switching voltages of our Al_{sp} devices are 0.98 V (SET) and -0.81 V (RESET). A comparison to the dc switching voltages of vertical MoS_2 crosspoint memristors with other electrode metals [7, 12–20, 21, 23, 39, 40] shows that our switching voltages are among the lowest reported (Figure 4f). We directly attribute this to our use of Al, which has favorable energy barriers for filament formation compared to other metals, as we will discuss in Section 3.4.

Finally, the endurance, number of devices evaluated for endurance testing, retention, and switching time and energy consumption of the Al-TE memristors are benchmarked against previously reported vertical MoS_2 -based memristors in Table S2 [7, 12–17, 18, 20, 21, 23, 24, 39, 40, 43, 44, 46, 63, 64].

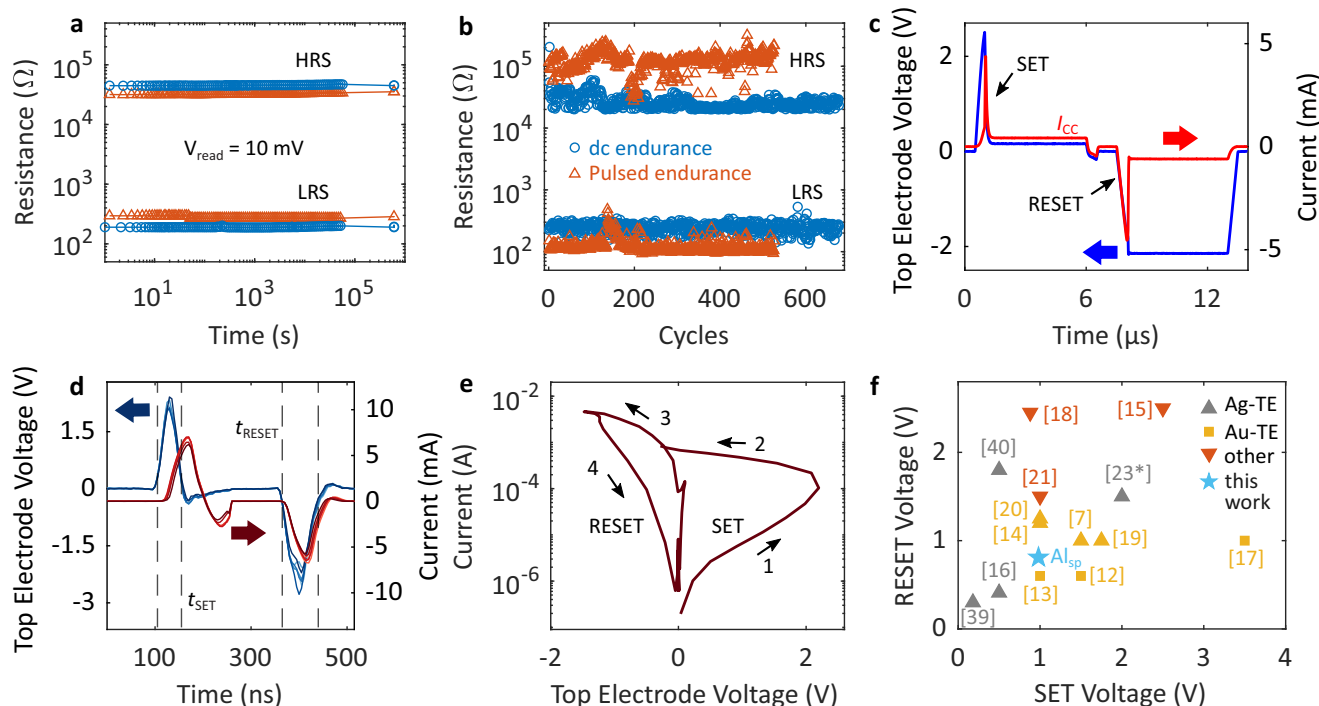


FIGURE 4 | Extended RS performance analysis of the Al_{sp} memristors. (a) Resistive state retention of two devices measured with a read voltage of 10 mV. Both devices show stable retention for at least a week. (b) Endurance of two devices, one measured with dc voltage sweeps showing 677 cycles, and another measured with pulsed voltage stress (PVS), showing 526 cycles. (c) I - V - t plot of an exemplary PVS switching cycle used for endurance testing. I_{CC} marks the current compliance level during the SET transition. The voltage pulse width was 5 μs , with rise and fall times of 500 ns. (d) Six consecutive switching cycles with nanosecond voltage pulses in a device. The extracted SET (t_{SET}) and RESET (t_{RESET}) times are indicated by dashed lines. (e) I - V plot of one exemplary switching cycle in (d), showing the non-volatile changes of the resistance. (f) Comparison of the average SET and RESET voltages of our Al_{sp} memristors with vertical MoS_2 crosspoint memristors using other electrode metals [7, 12–20, 21, 23, 39, 40] in the literature. The RESET voltages are absolute values. *Ag is the BE, but still the active electrode.

The comparison demonstrates that the Al -TE devices exhibit competitive endurance and retention. In addition, Table S2 highlights the limited and inconsistent reporting of switching times and switching energies in the literature, which complicates direct quantitative benchmarking of these metrics.

We focused further structural characterization on the two Al samples to understand the significant difference in RS behavior between Al_{ev} and Al_{sp} (Figures 3e,f).

3.3 | Structural Characterization of the Al -TE Samples

We analyzed the two Al -TE memristor samples, Al_{ev} and Al_{sp} , via cross-sectional high-resolution transmission electron microscopy (HRTEM). The bright field (BF) HRTEM images reveal the typical layered structure of MoS_2 , which is 5–7 nm thick and sandwiched between the top and bottom electrodes (Figure 5a,b). The Al_{ev} sample has a 5–8 nm thick amorphous layer at the Al - MoS_2 interface (Figure 5a), whereas the Al_{sp} sample has a relatively sharp interface between the MoS_2 and the TE (Figure 5b). Additional HRTEM images of both devices can be found in Figure S21. TEM images at lower magnification confirm the presence of the amorphous layer across the entire interface of Al_{ev} (Figure S22), whereas Al_{sp} exhibits a sharp Al - MoS_2 interface across large device sections (Figure S23).

Energy-dispersive X-ray diffraction (EDX) was used for the chemical characterization of both Al -TE devices (positions and widths of the analyzed areas are shown in Figure S24). The analysis revealed the presence of the expected elements Pd, sulfur (S), molybdenum (Mo), and Al, and two distinct oxygen (O) peaks (Figure 5c,d). The O peak at the surface of the Al -TE in both devices is attributed to the formation of native aluminum oxide upon exposure to air directly following TE deposition. The second O peak in both devices is located at the MoS_2 - Al interface. The intensity of the O peak at the MoS_2 - Al_{ev} interface (Figure 5c) is more than twice as high as the one on the aluminum surface. The position of the interfacial O peak overlaps primarily with the Al peak and, to a lesser extent, with the Mo and S peaks. We conclude that an aluminum oxide layer (AlO_x) formed at the interface during or after TE evaporation, consistent with the amorphous layer observed in the TEM images (Figure 5a, Figure S21 and S22). Moreover, the slight overlap of the O-signal with that of MoS_2 is attributed to the oxidation of sulfur vacancies on the MoS_2 surface due to ambient exposure (aging) [69–71, 72], since MoS_2 was stored for some time after growth and before processing.

Overall, HRTEM and EDX reveal a continuous interfacial AlO_x layer in the evaporated Al sample, whereas sputtered Al forms a sharp interface with MoS_2 without evidence of a continuous interfacial oxide. The following discussion addresses the origin of this interfacial oxidation.

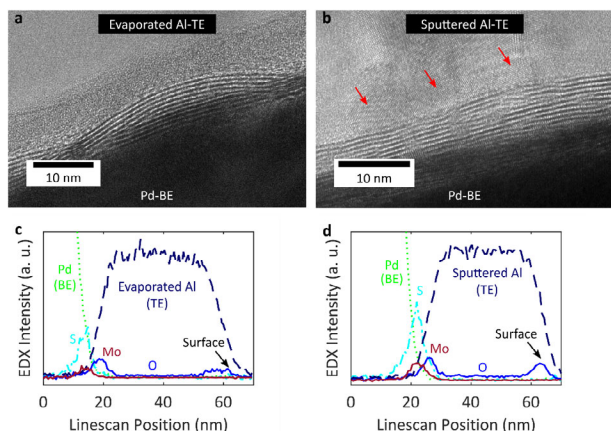


FIGURE 5 | HRTEM BF images and energy-dispersive X-ray spectroscopy (EDX) analysis of both Al-TE samples. (a) Cross-sectional HRTEM BF image of an evaporated Al-TE memristor showing the Pd-BE, layered MoS₂, the Al-TE, and a ~5 nm thick amorphous AlO_x layer at the Al-MoS₂ interface. (b) Cross-sectional HRTEM BF image of a sputtered Al-TE memristor showing the Pd-BE, layered MoS₂, and the Al-TE. Unlike in (a), no amorphous layer is observed at the interface. The red arrows show crystalline Al clusters near the Al-MoS₂ interface, indicating high metal quality. (c) EDX line scan intensities of the device depicted in (a), showing the expected elemental signals and two distinct oxygen (O) peaks. The EDX scan was performed on a wider region than the one shown in the HRTEM image in (a) and covered the Al-TE surface. (d) EDX line scan intensities of the device depicted in (b), showing the expected elements and two distinct O peaks. The EDX scan was performed on a wider cross-section than that visible in the HRTEM image in (b) and covered the surface of the Al-TE. The exact positions of the line scans depicted in (c) and (d) are shown in Figure S24.

In Al_{sp} (Figure 5d), the interfacial O peak has comparable intensity to the surface O peak and is narrower than in Al_{ev} (Figure 5c), while also showing greater overlap with Mo and S. The relative intensity of O compared to Mo and S is lower than for Al_{ev}. The interfacial O peak intensity of Al_{ev} is significantly higher than the surface peak. This indicates that the interfacial O signal in Al_{sp} arises primarily from oxidation of the MoS₂ surface because of aging rather than Al oxidation during processing. These trends are confirmed by EDX line scans of additional devices and elemental maps (Figures S25 and S26).

The amorphous AlO_x layer in Al_{ev} accounts for the higher resistances and voltages, as well as the reduced RS yield, compared to Al_{sp}. Previous studies attribute oxidation of reactive metals on MoS₂ [54] and tungsten diselenide (WSe₂) [73] during evaporation under high vacuum to residual oxygen in the chamber, while ultrahigh vacuum can suppress this effect [52, 53, 73]. Control devices on Al_{ev} with direct BE-TE contacts, which were not analyzed in the previous studies, show purely ohmic behavior (Figure S5), indicating that continuous oxide formation is specific to the MoS₂/Al interface. Both sputtering and evaporation in this work were performed under similar high-vacuum conditions (~10⁻⁷ mbar).

The confinement of oxidation to the Al_{ev}/MoS₂ interface indicates that it does not arise solely from the chamber ambient; otherwise, control devices would also exhibit an oxide layer. Instead, we

propose that highly reactive [74] evaporated Al reacted with O₂, H₂O and OH adsorbed on the MoS₂ surface [72, 75, 76, 77], which can persist even under high vacuum conditions [53]. In contrast, Al sputtering suppresses interfacial oxidation by removing these adsorbates through higher kinetic impact energies [78, 79], substrate heating [80], and UV radiation generated by the ionized sputtering gas [81–83, 84].

While the present results consistently indicate that interfacial oxide formation is linked to surface adsorbates on MoS₂, an in situ annealing step prior to Al evaporation could provide a more direct experimental validation of this interpretation. Such an approach could be explored in future studies to further decouple the effects of surface adatoms from those of the deposition method.

The effect of the higher energy of sputtered metal is also reflected in the larger overlap of the EDX peaks of S and Al (Figure 5c,d) in Al_{sp} when compared to Al_{ev}. The overlap shows that sputtered Al created surface defects in MoS₂ into which Al diffused, which is well known to arise when metals are deposited onto 2D materials [48, 55, 57]. While this can be problematic for monolayer films, multilayer MoS₂ is more robust to surface defects, especially in memristors [12]. TEM analysis shows that the vdW layers of MoS₂ in Al_{sp} devices are intact (Figure 5b, Figures S21 and S23). The high yield of functioning devices (Figure 3a), together with the second-highest initial resistances observed for Al_{sp} devices among all tested metals (Figure 2), both corroborate that Al sputtering did not cause modifications detrimental to memristor operation.

3.4 | Resistive Switching Mechanism

We analyzed the switching mechanism in Al_{sp} by measuring devices with a variable active area (Figure 6a). We measured the initial resistance state (IRS) before cycling and those after the SET or RESET sweeps with a read voltage of 10 mV. The HRS and LRS data points in Figure 6a represent the resistances of three devices per active area, averaged for at least five RS cycles per device. The IRS and HRS values are area-dependent. The LRS resistances do not exhibit area dependence. This behavior is typically observed for filamentary RS devices in the literature, where the current conduction in the LRS is dominated by one or a few nanoscale filaments [20, 85, 86, 87]. In contrast, in the HRS (and IRS), the entire active area of the device contributes to the current conduction. The passive role of Pd and the area independence of the LRS resistance indicate a filamentary RS mechanism in the Al_{sp} devices that is facilitated by Al.

We then performed temperature-dependent resistance (Figure 6b) and *IV* measurements (Figure 6c,d) on a device in the LRS to determine the conduction mechanism [88]. Details on these measurements and their setup are included in the Methods Section. The device resistance increased nearly linearly with increasing temperature (Figure 6b), and the current decreased with increasing temperature (Figure 6c), with a slope close to 1 when plotted on a double-logarithmic scale (Figure 6d). This strongly suggests ohmic (metallic) conduction as the dominant current conduction mechanism [88, 89]. Therefore, we conclude that our Al_{sp} devices switch via an ECM mechanism [90], where an Al filament is formed during the SET process, bridging

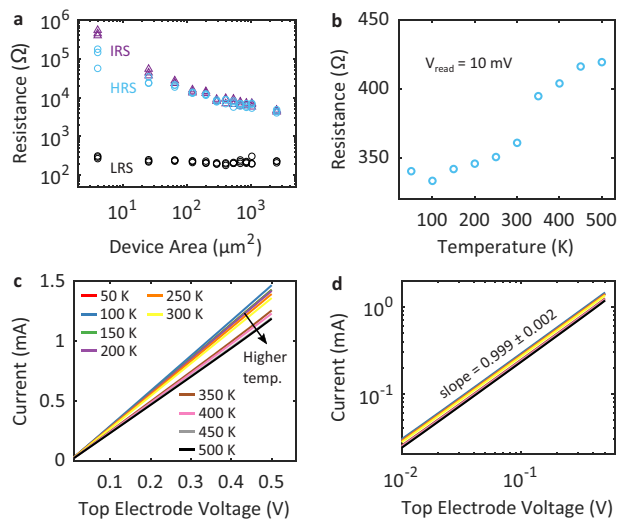


FIGURE 6 | Analysis of the switching mechanism of the Al_{sp} memristors. (a) Initial resistance state (IRS, purple triangles), high resistance state (HRS, blue circles), and low resistance state (LRS, black circles) of devices with variable active areas, ranging from $2500 \mu\text{m}^2$ down to $4 \mu\text{m}^2$. Each data point represents one device. The IRS was measured with a reading voltage of 10 mV in the pristine devices. The data points for the HRS and LRS represent the average resistances of at least five switching cycles per device. (b) Temperature-dependent (from 50 to 500 K in 50 K steps) resistance of a device in the LRS. The device was switched to the LRS at room temperature before the temperature-dependent measurements were conducted. The resistance was read at a voltage of 10 mV. (c) I - V sweeps of the device in the LRS from 0 to 0.5 V at different temperatures. (d) Double-logarithmic plot of the data in (c). The average slope of all sweeps from a linear fit with error is indicated in the plot and is very close to 1.

the MoS_2 between the BE and TE. The filament is dissolved again during the RESET process. This switching mechanism is consistent with the switching mechanisms reported in multilayer MoS_2 and h-BN memristors using other TE metals [14, 22, 16, 36, 88, 91].

In the following paragraphs, we use the theory of ECM RS devices to explain the variation in our devices with different TE metals (Figure 3). For this, we employed a modified dissociation-diffusion-adsorption (DDA) model proposed in the literature [19] for RS by filament formation in monolayer MoS_2 , and assumed four steps for our multilayer MoS_2 memristors: 1. Dissociation of metal ions from the bulk of the electrode [19, 92, 93]; 2. Adsorption of metal ions on the MoS_2 surface [19, 93, 94]; 3. In-plane diffusion of metal ions on the MoS_2 surface to reach a grain boundary [19, 93, 94]; and 4. Out-of-plane diffusion of metal ions through a grain boundary to form the filament [14, 22, 16, 36]. This last step is a modification, replacing the adsorption of metal atoms into sulfur vacancies in the monolayer MoS_2 of the original model. Note that a two-step process with dissociation from the bulk electrode directly followed by diffusion into a grain boundary is also possible [19]. Figure 7a provides a schematic representation of the filament formation steps.

The four steps of filament formation are governed by process and metal-specific energy barriers. These have been calculated in the

literature using density functional theory (DFT) [36, 93, 94] and are summarized in Table S3 for all metals used in this work and for Au and Ag for comparison. The energies for step 4 listed in the table are related to a grain boundary with a 22° tilt angle and serve as an example [36]. Energy values for other grain boundary types can be found in the source publication. Based on these considerations, the filament formation is expected to happen as follows:

(1) The dissociation and ionization probability of metal atoms from the electrode bulk is governed by their cohesive energy E_{coh} [19, 92], with lower cohesive energies corresponding to easier dissociation. Among the metals, Ag exhibits the lowest cohesive energy, followed by Al and Au, whereas Pd shows the second-highest value and Ni the highest. (2) After ionization, metal ions adsorb on the MoS_2 surface at metal-specific preferred sites [93, 94]. Pd, Ni, and Al favor adsorption on top of Mo atoms, whereas Au preferentially binds on top of S atoms and Ag above the center of the hexagonal MoS_2 ring. The adsorption energy E_{ads} increases from Ag to Au to Al, with Pd and Ni exhibiting the highest energies. (3) Subsequent filament growth requires lateral diffusion of metal ions toward grain boundaries, which can happen via an S-atom ($E_{\text{diff},1}$) or through the center of the hexagonal lattice ($E_{\text{diff},2}$) [93, 94]. Here, Au shows the lowest barrier energies, followed by Ag and Al, then Pd and Ni. (4) The final step involves out-of-plane diffusion of metal ions through MoS_2 along grain boundaries [14, 22, 27, 16, 36, 91]. Al exhibits the lowest out-of-plane diffusion barriers across all analyzed grain boundary types in a DFT study [36], followed by Ni, Au and Ag. No values were available for Pd. The bar graph in Figure 7b shows a visual representation of the energy barriers for each metal.

In summary, the model predicts the lowest energy barriers for Al-mediated filament formation in this study, which is consistent with the Al_{sp} devices exhibiting reliable switching at low voltages and low currents compared to the other tested samples (Figure 7b). The high device yield can be attributed to the reduced stress on the device and the MoS_2 during switching, which is enabled by the low power, and to fabrication conditions that minimized damage to the MoS_2 .

Pd has intermediate energy barriers relative to the other metals (Figure 7b). Hence, the RS behavior observed in the Pd sample (Figure 3b, Figure S11) indicated a full filament formation and dissolution but required higher voltages and higher currents for switching. This induced more stress on the devices, leading to breakdown after a single cycle. Most Pd devices failed after one SET transition without completing a full RS cycle (Figure S6). Pd_{ev} devices showed the highest initial resistances (Figure 2), indicating that damage from deposition can be mostly neglected.

Ni-based devices exhibit resistive switching behavior consistent with the highest modeled energy barriers and severe deposition-induced damage. The very low initial resistances (Figure 2) indicate the formation of metallic bridges prior to electrical measurements, which cannot be fully ruptured anymore due to the high diffusion barriers (Figure 7b), leading to a low yield. RS likely occurs via gradual modulation of filament geometry [37, 95] rather than abrupt formation and rupture, leading to a narrow switching window without abrupt transitions (Figure 3c,d and Figures S12 and S13). Similar electrical behavior has been reported

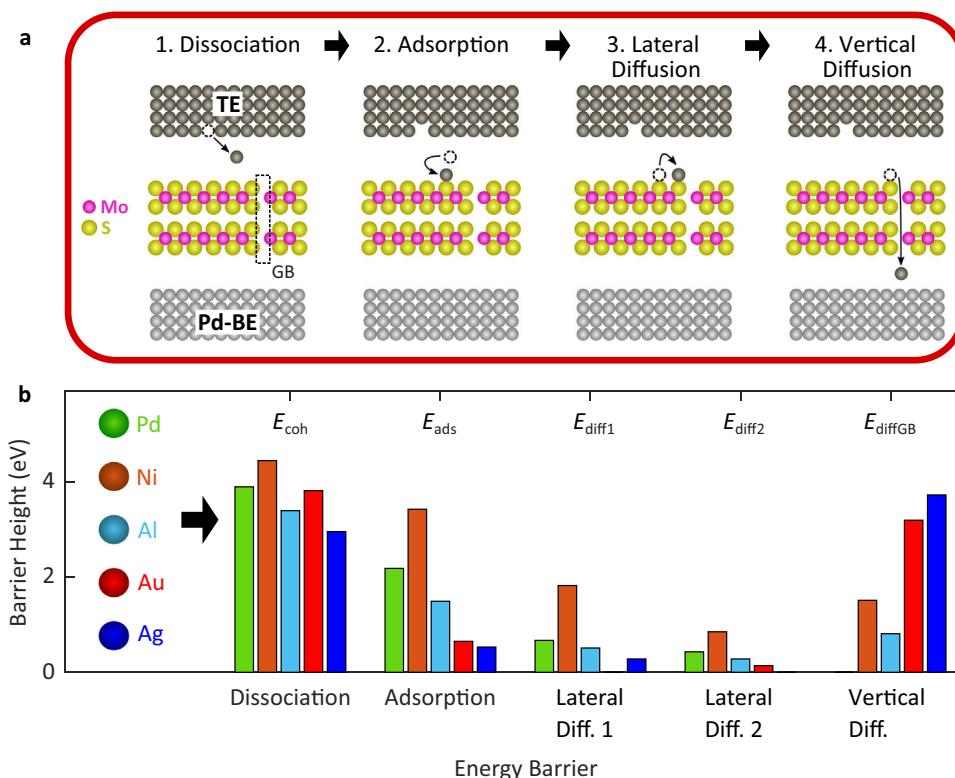


FIGURE 7 | Schematic representation of the resistive switching mechanism. (a) Step-by-step schematic of the filament formation process: (1) Dissociation of a metal ion from the bulk of the TE metal. (2) Adsorption of the metal ion onto the surface of MoS₂. (3) Lateral diffusion of the metal ion on the surface of MoS₂ toward a grain boundary (GB). (4) Diffusion of the metal ion through a GB in MoS₂. (b) Graphical representation of the energy barriers each TE metal has to overcome to form a conductive filament through MoS₂ [19, 36, 93, 94]. Each metal's energy barriers are represented in a different color (Pd green, Ni orange, Al light blue, Au red, and Ag dark blue). The relevant energy barriers are the cohesive energy (E_{coh}) for dissociation, the adsorption energy (E_{ads}) for adsorption, the diffusion barrier energies (E_{diff1} and/or E_{diff2}) on the surface of MoS₂, and the energy barrier for vertical diffusion (E_{diffGB}) through a grain boundary. A grain boundary with a tilt angle of 22° was chosen from the source publication to represent vertical diffusion [36]. The numerical values used for the graph are listed in Table S3.

for evaporated Ni electrodes on exfoliated MoS₂ [44], although quantitative comparison is limited due to the lack of statistical reporting in that study.

The evaporated Al sample is a special case due to the presence of the AlO_x interlayer (Figure 5a). This interlayer mostly prevents filament formation according to the discussed diffusion mechanisms, since Al is bound in the oxide. Consequently, only a few devices showed RS (Figure 3a,e, and Figure S14), and required much higher voltages. Switching may have occurred in the AlO_x instead of the MoS₂, as the voltage drop is expected to occur predominantly across the insulating oxide rather than the semiconducting MoS₂ due to its higher resistance. The high switching voltages led to high currents, increased stress on the device during the SET event, and a permanent breakdown after a single cycle. Most devices showed no reproducible resistance change, even after applying voltages up to ±8 V, highlighting the detrimental effect of the interfacial oxide on the RS behavior (Figure S9).

Finally, we applied these considerations to Au and Ag, which have mainly been used as active electrodes in the literature [7, 12, 13, 14, 16, 17, 19, 20, 24, 26, 28, 39–41, 42]. The energy barriers for filament formation are lower for Ag in steps 1, 2, and 3, while they are lower for Au in steps 2 and 3 (see Figure 7b) when compared

to Al. However, the out-of-plane diffusion barriers through grain boundaries (step 4) of Al are significantly lower than those of Au and Ag [36]. Nevertheless, the average SET and RESET voltages of our Al_{sp} memristors are comparable to or lower than those of MoS₂ memristors with Au and Ag active electrodes in the literature [7, 12–20, 21, 23, 39, 40] (Figure 4f). It appears that the higher barrier energies in steps 1 to 3 partially offset the lower barrier energy in step 4. Given the advantages of Al over Au and Ag concerning availability, cost, and ease of processing, it is an attractive option for scalable memristor fabrication. For example, reactive ion etching processes for patterning Al are well established and use standard gases and setups [96], while Au and Ag are more problematic to etch residual-free and often require specialized setups [97, 98, 99]. Last, Au and Ag are detrimental in front end of line CMOS processing [100], while Al is not [101, 102, 103], although it is no longer a standard metal in modern technology nodes.

4 | Conclusion

We investigated memristors with MOCVD MoS₂ as the active switching layer, Pd back electrodes, and five different top electrodes: Pd, Ni, and Al, the latter two deposited by sputtering or evaporation. Electrical measurements showed high initial

resistances for Pd-TEs, attributed to the vdW gap between the noble metal and MoS₂, and a low RS yield. Both Ni-TE samples exhibit very low initial resistances, confirming earlier reports that Ni deposition can damage MoS₂. Their RS yields are only slightly higher than those of the Pd sample, albeit with high currents and narrow switching windows. The sputtered Al sample exhibited high initial resistances comparable to those of the Pd sample, despite the use of high-energy sputtering. We attribute this to the low atomic weight and low sputtering energies of Al. The sample demonstrates reproducible RS with a high yield of 95% for 64 tested devices. Evaporated Al exhibited significantly higher initial resistances and a low RS yield, which we attribute to an amorphous AlO_x layer at the Al-MoS₂ interface, as determined by TEM and EDX analysis. A weak device area dependence of the LRS and its ohmic behavior confirm Al filament formation as the RS mechanism in the sputtered Al-TE sample. We discussed the RS behavior based on energy barriers for metal dissociation and diffusion on and in MoS₂ for filament formation obtained from DFT calculations reported in the literature. Our results demonstrate that sputtered Al electrodes lead to reliable resistive switching within the investigated Pd/MoS₂/Al device architecture and represent a viable and silicon technology-compatible method for fabricating active electrodes in 2D MoS₂-based memristors.

5 | Methods

5.1 | MoS₂ MOCVD

Multilayer MoS₂ was grown epitaxially in a commercial AIX-TRON planetary hot-wall reactor in a 10 × 2" configuration on c-plane sapphire substrates (with a 0.2° offcut toward the mplane). Initially, substrate desorption at 970°C in a pure hydrogen (H₂) atmosphere was performed. Afterward, growth was carried out at 750°C substrate temperature for 24 h, with nitrogen (N) as the carrier gas at a chamber pressure of 30 hPa. The precursor flows were set to 19 nmol/min for molybdenum hexacarbonyl (MCO) and 19 μmol/min for di-tert-butyl sulfide (DTBS). The multilayer nature was confirmed via TEM (Figure 5a,b).

5.2 | Device Fabrication

All samples were fabricated on 2 × 2 cm² silicon (Si) substrates with 300 nm thermally grown silicon dioxide (SiO₂) on top as insulation. The memristor BE was patterned via optical lithography using a double layer of lift-off resist LOR 3A (Micro Resist Technology GmbH) and AZ5214E photoresist (MicroChemicals). Then, 10 nm of titanium as an adhesion layer and 40 nm of Pd were deposited in an FHR.STAR 200 electron-beam evaporation system. Lift-off was performed in dimethyl sulfoxide (DMSO). All the samples presented in this work were fabricated via this BE process.

MoS₂ was transferred from the sapphire growth substrate to the prepatterned memristor substrates via potassium hydroxide (KOH)-assisted wet transfer with a PMMA support layer. The MoS₂ was then structured with a double layer of LOR 3A and AZ5214E JP photoresist on top of the PMMA [104]. The photoresist double layer was developed, and the PMMA was

removed in the exposed areas by low-power reactive ion etching (RIE) with oxygen plasma. MoS₂ was then etched via RIE in a chlorine, oxygen, and argon plasma. The LOR 3A and AZ5214E resists were subsequently stripped in DMSO at room temperature for 10 min, after which the remaining PMMA was stripped in acetone at 65°C for 20 min.

The TE was patterned with a negative lithography process using AZ5214E resist. The different TE metals of approximately ~50 nm were deposited as follows: The evaporated Pd_{ev} and Al_{ev} were electron beam evaporated in an FHR.STAR 200 system with a rate of 0.1 nm/s. Ni_{ev} was electron beam evaporated in a Balzers PLS 500 system with a rate of 0.1 nm/s. Ni_{sp} and Al_{sp} were deposited via direct-current (dc) sputtering in a von Ardenne CS 730S system with a rate of 0.27 nm/s and 0.83 nm/s, respectively. The base pressure of the two evaporation tools and the sputter tool ranged from 1·10⁻⁷ mbar to 5·10⁻⁷ mbar for all depositions. Lift-off was performed in acetone.

5.3 | Material and Device Characterization

Atomic force microscopy (AFM) measurements were performed with a Bruker Dimension Icon AFM in tapping mode. Raman spectroscopy was performed with a WiTec alpha300R Raman imaging microscope using an excitation laser wavelength of 532 nm with 1 mW laser power.

A dual-beam gallium-ion (Ga⁺) focused ion beam (FIB)—scanning electron microscope (SEM) FEI Strata 400 was used for the TEM lamella preparation of the crosspoint memristive devices. The cross-sectional (S)TEM and EDX measurements were conducted on a JEOL JEM-F200 TEM at an operating voltage of 200 kV. The (HR)TEM image acquisition and examination were made with the Gatan OneView Camera and Digital Micrograph software, respectively. The EDX spectrum recording and analysis were made with Oxford Instruments' Ultim Max TLE Silicon Drift Detector (SDD) and AZtecTEM software, respectively.

5.4 | Electrical Characterization

Electrical measurements were conducted in a LakeShore cryogenic probe station connected to a Tektronix 4200A-SCS semiconductor parameter analyzer (SPA) at room temperature under ambient conditions unless stated otherwise. Direct-current (dc) *I*-*V* characterization was performed via two Keithley 4200-SMU source measure units (SMU), each connected to a Keithley 4200-PA preamplifier.

Positive voltage sweeps induced a SET transition, that is, from the HRS to the LRS. The SET current was limited by a current compliance (*I*_{CC}) between 100 μA and 1 mA for the Pd and Al samples, whereas the Ni samples, owing to their low resistances, were switched with higher *I*_{CC} of 10 mA or no compliance at all. We increased the voltage successively if the device did not switch, and also, if needed, *I*_{CC}. When a SET transition was observed, we applied negative voltage sweeps without *I*_{CC} to RESET the devices from the LRS back to the HRS. The resistances of the devices under test were measured before and after each cycle to determine

their state (LRS or HRS) with a low read voltage of 10 mV to avoid accidental switching.

The same setup was used for the temperature-dependent electrical measurements shown in Figure 6b–d. All devices were initially switched for a full RS cycle under ambient conditions at room temperature to ensure that they were functional. Then, they were switched to the LRS, and the measurement chamber was evacuated and cooled to approximately 20 K with liquid helium (chamber pressure $\sim 1 \cdot 10^{-5}$ mbar). Temperature-dependent measurements were conducted, starting at 50 K. The sample was then heated in 50 K steps with a heating stage connected to a PID temperature controller up to a maximum of 500 K and electrically measured at each step.

Pulsed voltage measurements (Figure 4b–e, Figures S19 and S20) were performed with the same setup described above and an ultrafast pulse measurement unit (Keithley 4225-PMU), with each of the two PMU channels connected to a remote amplifier unit (Keithley 4225-RPM). Voltage pulses were applied to the TE while the BE was grounded.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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