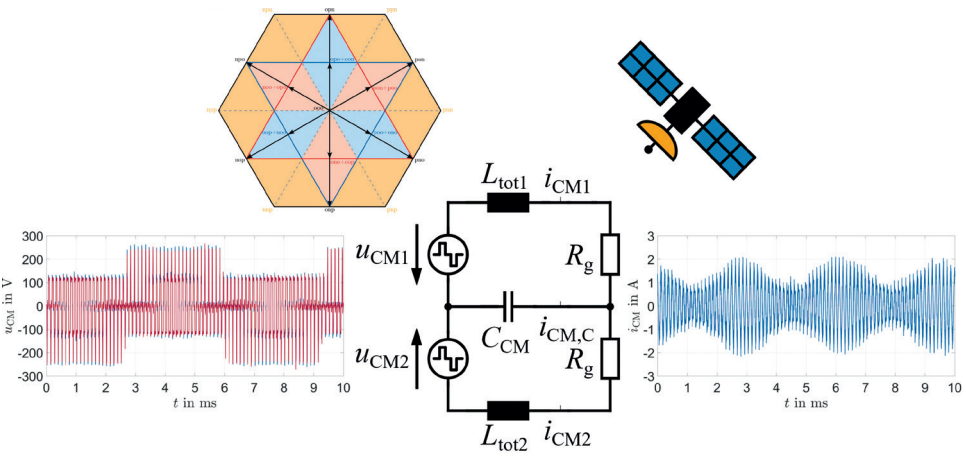
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Common-Mode Currents in Low-Voltage DC Underlay Grids with AC-Side Grounding

Fabian Herzog
Institute for Power Generation and Storage Systems



Common-Mode Currents in Low-Voltage DC Underlay Grids with AC-Side Grounding

Von der Fakultät für Elektrotechnik und Informationstechnik der Rheinisch-Westfälischen Technischen Hochschule Aachen zur Erlangung des akademischen Grades eines Doktors der Ingenieurwissenschaften genehmigte Dissertation

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Vorwort

Diese Arbeit entstand während meiner Zeit als wissenschaftlicher Mitarbeiter am Institute for Power Generation and Storage Systems (PGS) am E.ON Energy Research Center (E.ON ERC) der RWTH Aachen University. Die Arbeit befasst sich mit der Modellierung und Reduzierung von Gleichtaktströmen in unterlagerten Niederspannungsgleichstromnetzen mit wechselstromseitiger Erdung.

Zunächst möchte ich Professor Rik De Doncker für die Möglichkeit der Promotion am PGS sowie die Freiheit und Unterstützung bei dieser Arbeit danken. Außerdem möchte ich mich für das entgegengebrachte Vertrauen während meiner Zeit als Gruppenleiter und Oberingenieur bedanken. Darüber hinaus möchte ich Professor Hirofumi Akagi für die Übernahme des Koreferats und das Interesse an meiner Arbeit danken. Ebenso möchte ich mich für die gute interdisziplinäre Zusammenarbeit mit den anderen Instituten am E.ON ERC sowie am Center for Wind Power Drives bedanken.

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Abschließend möchte ich mich bei meiner Familie für die Unterstützung, auch bereits während des Studiums, bedanken. Ganz besonders danke ich meiner Frau Raveena für die bedingungslose Unterstützung während meiner gesamten Zeit am Institut, insbesondere in den letzten Monaten zum Abschluss der Arbeit.

Ohne euch hätte diese Arbeit nicht entstehen können. Danke.

Aachen, im Mai 2026 *Fabian Herzog*

Abstract

To counteract climate change, it is necessary to reduce the emission of greenhouse gases, such as carbon dioxide. The electrification of heating and transportation systems, as well as the installation of renewable energy sources (RESs), plays a central role in achieving this goal. However, this puts a strain on the low-voltage (LV) and medium-voltage distribution grids, because RESs, heat pumps, and charging infrastructure are primarily connected to them. This can result in the local overloading of transformers or cable systems.

DC underlay grids that support the existing LV AC grids are beneficial for integrating RESs and charging infrastructure because they are more efficient and require fewer components. They also enable vertical grid coupling between different AC grid sections with active power flow control, reducing local overloading by intelligently distributing loads. Previous studies assumed galvanic isolation between the LV AC and DC grids, which requires additional components and results in lower efficiency. Recently, a DC system with AC-side grounding was proposed that does not rely on galvanic isolation. However, this introduces certain challenges, especially when multiple infeed converters are used. The main challenges, which were identified, are increased common-mode (CM) currents and electromagnetic interference (EMI).

This work thoroughly analyzes these challenges and presents methods to mitigate their effects. At first, a CM model is derived to determine potential reduction measures. The CM choke is identified as the primary component for reducing CM currents. Therefore, a model-based design guide that limits the CM current to a specific value using the previously derived model and equations is presented. Additionally, the common-mode voltage (CMV) of the infeed converters and their switching alignment influence the CM currents. Thus, modulation strategies for three-level inverters are examined, and optimized modulation strategies with reduced CMV are evaluated. First, a discontinuous pulse width modulation (PWM) is developed that clamps the middle phase to the neutral point. This restricts the converter's linear modulation range, so the modulator is combined with sine-triangle pulse width modulation (SPWM). The result is a hybrid modulation strategy called hybrid-discontinuous sinusoidal pulse width modulation (HDSPWM). Second, middle phase opposition disposition (MPOD), a carrier

configuration that reduces the CMV, is proposed. MPOD opposes the carriers of the middle phase. While HDSPWM slightly reduces CMV at the given operating point, it does not reduce CM currents compared to SPWM. However, MPOD significantly reduces CMV and CM currents when combined with SPWM, space vector pulse width modulation, virtual space vector pulse width modulation, and HDSPWM, as compared to the conventional phase disposition and phase opposition disposition.

Furthermore, this work introduces the synchronization of locally distributed converters using the global navigation satellite system (GNSS) to align their switching without the need for additional communication. The maximum delay measured between two GNSS receivers is a few nanoseconds, which is sufficient for synchronization. Using this method, the reduction of circulating CM current is more than 80 %.

Finally, EMI measurements are performed. Different modulation waves significantly impact conducted EMI in the 9 kHz to 150 kHz frequency band. However, the carrier configuration does not impact EMI. Generally, the measured EMI is below the standard limit values regardless of the modulator or the number of converters.

Overall, this thesis demonstrates the feasibility of DC underlay grids with AC-side grounding. However, its contributions and concepts are not limited to this specific application. The optimized modulation strategies can be applied wherever CMV and CM currents must be limited. Examples include photovoltaic applications and drive systems. Additionally, the converter synchronization using GNSS is universally applicable when synchronizing multiple converters. Lastly, the EMI measurements can contribute to the standardization of DC grids.

Contents

Abstract v

1 Introduction 1

2 Low-Voltage DC Underlay Grid 11
2.1 Operation of DC Systems with AC-Side Grounding 11
2.1.1 Grounding Schemes 12
2.1.2 Operational Management 13
2.1.3 Protection of DC Systems with AC-Side Grounding . . . 15
2.1.4 Electromagnetic Compatibility 16
2.1.5 Stray Currents 19
2.2 Rectifier Topologies 19
2.2.1 Switching States 21
2.2.2 Common-Mode Voltage Profile 22
2.3 Demonstration Setup 23
2.4 Control of Three-Level Neutral-Point Clamped Inverter 26
2.4.1 Conventional Modulators 27
2.4.2 Neutral-Point Balancing 31
2.4.3 Influence of Dead Time 32

3 Modeling Common-Mode Currents 35
3.1 Single-Phase Model 35
3.2 Common-Mode Model 38
3.3 Model Extension for Multiple Front Ends 42
3.4 Model-Based Design of Common-Mode Choke 44
3.4.1 Structure and Components of Common-Mode Filters . . . 45
3.4.2 Design Guideline for Common-Mode Chokes in DC Systems with AC-Side Grounding 46
3.4.3 Construction of Common-Mode Choke for Experimental Analyses 49
3.5 Measuring Common-Mode Voltages 50
3.6 Summary 54

4 Optimized Modulation Strategies for Three-Level Inverters 57
4.1 Virtual Space Vector Pulse Width Modulation 57
4.1.1 Calculation of Duty Cycles 60
4.1.2 Active Neutral-Point Control 63
4.2 Hybrid-Discontinuous Sinusoidal Pulse Width Modulation 65
4.3 Carrier-Based Reduced Common-Mode Voltage Modulation . . . 68
4.3.1 Phase Opposition Disposition 69
4.3.2 Middle Phase Opposition Disposition 71
4.4 Evaluation of Modulation Strategies 74
4.4.1 Output Currents 75
4.4.2 DC Link Voltage Balancing 77
4.4.3 Common-Mode Voltage 79
4.4.4 Efficiency 83
4.5 Summary 85

5 Experimental Analysis of Common-Mode Currents 87
5.1 Synchronization of Locally Distributed Converters 87
5.1.1 Synchronization with Global Navigation Satellite System 88
5.1.2 Synchronization of Two Converters 90
5.2 Capacitive Common-Mode Currents 94
5.2.1 One Converter with Common-Mode Load 94
5.2.2 Increased Common-Mode Resonance Frequency 102
5.2.3 Two Converters with Common-Mode Load 104
5.3 Additional Simulative Considerations 112
5.4 Electromagnetic Interference Voltages 119
5.4.1 Introduction to Electromagnetic Interference Voltages . . 119
5.4.2 Measurement Settings and Setup 121
5.4.3 Measurement Results 122
5.5 Summary 126

6 Conclusions and Outlook 131

A Appendix 137
A.1 Differential Equation for Common-Mode Currents 137
A.2 Modulator Evaluation Measurements 138
A.3 Frequency Spectra of Common-Mode Current Measurements . . 151
A.4 Electromagnetic Interference Voltage Measurements 156

B Acronyms 163

C Symbols 165

List of Figures **169**

List of Tables **173**

Bibliography **175**

1 Introduction

Climate change is indisputably caused by the emission of greenhouse gases, such as carbon dioxide (CO_2), into the atmosphere. A substantial share of this emission is contributed by the production of electricity, the generation of heat, and the transportation sector. Consequently, a reduction of emissions, particularly in the aforementioned sectors, is of the utmost importance. This necessitates the electrification of heating and transportation systems, for instance, through the implementation of heat pumps and battery electric vehicles. Concurrently, the shift from conventional fossil fueled power plants to renewable energy sources (RESs) mitigates the global warming potential (GWP) of electricity production, thereby reducing the emissions of electrified systems.

In contrast to conventional power plants, the majority of RESs are integrated into the distribution grids [1, 2]. Large-scale systems, such as wind turbines and open-field photovoltaic (PV) systems, are connected to the medium-voltage (MV) grid, while rooftop PV is connected to the low-voltage (LV) grid [2]. This is already challenging for the existing grid infrastructure, as it was originally built to deliver electric energy from high voltage levels to lower voltage levels without infeed in the distribution grids. Additionally, the electrification of heat-

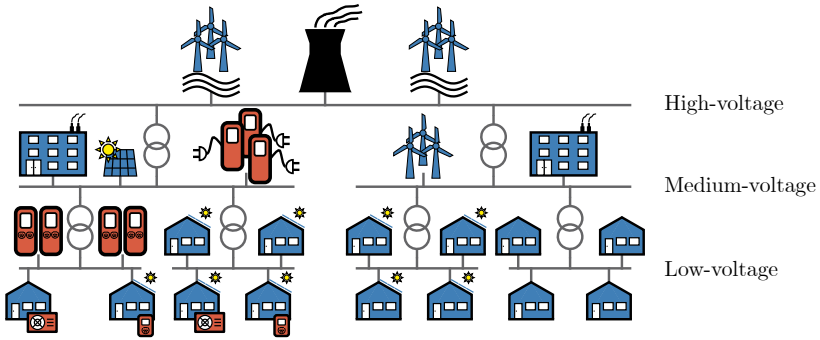


Figure 1.1: Exemplary grid structure showing a classical grid with consumers on the right side and a grid with many prosumers on the left side.

ing systems and transportation imposes substantial loads on distribution grids, potentially resulting in local overloading of transformers or cable systems [3–5]. Figure 1.1 presents an example grid to underscore the potential challenges in distribution grids. In the LV grid section on the right, the conventional structure is represented. It is visible that a number of households are connected to the distribution grid transformer without substantial loads, such as wallboxes or heat pumps, and with power supplied exclusively from the MV grid. A second grid section is located to the left of the aforementioned section. This section contains households that have rooftop PV panels installed. The challenge here is especially pronounced on a sunny weekday, as the low consumption from households is combined with the high electricity production of PV panels. Consequently, there is a substantial power flow from the LV to the MV grid. Due to the current flow, there is a voltage drop across the impedances, which leads to overvoltages because the MV side's voltage is mostly fixed. Moreover, in the event of an unfavorable scenario for the distribution grid operator, the generated electricity may not be consumed within the same MV grid section. Consequently, it is necessary to feed the electricity into the high-voltage transmission grid, which results in additional losses and costs. The left side of the figure presents additional challenging scenarios. While the right LV grid section has a substantial amount of rooftop PV installed, only a limited number of loads are available, particularly during daylight hours. However, the left grid section exhibits substantial loads, including charging infrastructure, while only a portion of the rooftop PV is utilized. In this scenario, the electricity generated on the right side must flow through the MV grid, which contains multiple transformers. This results in losses and increases the load on the grid infrastructure.

One solution that facilitates the distribution of electricity between two LV AC grids involves the implementation of solid-state transformers (SSTs), which enable active power flow control [5]. However, the necessity of a substantial number of components must be acknowledged. For instance, one particular solution utilizes two inverters and a three-phase dual-active bridge DC-DC converter [5]. Therefore, the construction of the SST necessitates the integration of four three-phase inverter modules, a medium frequency transformer, passive components, and additional auxiliary components. Furthermore, the main purpose of those SSTs is to regulate the power flow between two particular grid sections. A more efficient and flexible solution is to construct a DC underlay grid that can connect to multiple LV AC grid sections simultaneously. Furthermore, these DC underlay grids can efficiently connect large loads, such as charging infrastructure, PV systems, and battery energy storage systems (BESSs), given their inherent operational characteristics in DC [6, 7]. Consequently, rectifiers and inverters can be omitted when connected to a DC grid, enhancing efficiency while reducing cost and size. This is of particular importance in dense urban areas. Figure 1.2 illus-

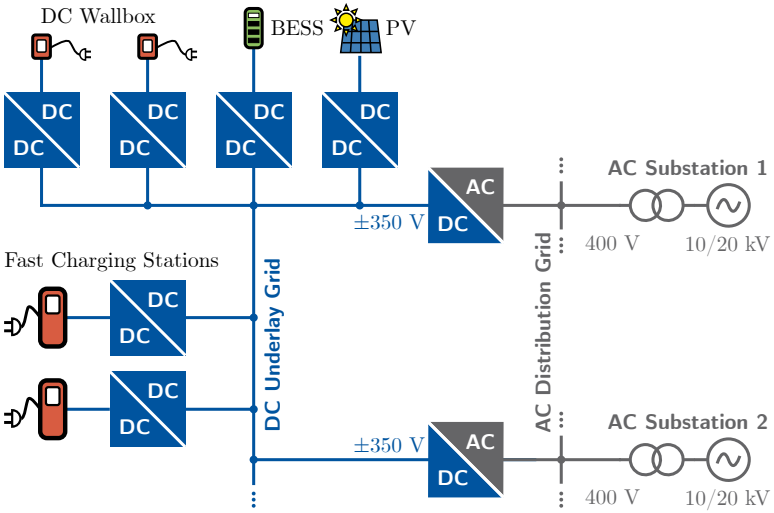


Figure 1.2: Exemplary DC underlay grid with two infeed converters connected to different LV AC grid sections.

trates an exemplary DC underlay grid supplied by multiple AC substations. It is evident that the DC grid functions as a complement to the AC grid; hence, it is underlaid [8]. It should be noted that only two infeed converters are depicted; however, the incorporation of additional converters is possible. This would result in an increase of the power rating of the DC underlay grid and the meshing between the AC grids. It should be mentioned that some of the necessary converters are not yet available as commercial products; however, they are currently under development. For instance, suitable DC-connected charging stations are only minimally available on the market. However, power hardware-in-the-loop test benches for their evaluation have already been developed [9].

Several studies have demonstrated the additional benefits of connecting charging infrastructure and PV to DC grids [10–12]. Depending on the size of the charging park, a reduction in GWP of up to 5.3 % was confirmed, with larger charging parks benefiting even more [13]. At the same time, the net present value was shown to increase by 2.9 %, despite the higher initial investment cost of the DC-connected charging park [13]. These results are primarily due to the higher efficiency of DC systems compared to AC systems. Especially on a large scale, DC grids can significantly reduce the GWP of charging infrastructure [14, 15].

The maximum load that can be connected to the DC underlay grid depends on the capacity available from the distribution grid transformers in the AC substations. Typically, the transformers' power ranges from 250 kVA to 630 kVA [16] and sometimes up to 1 MVA. However, these transformers' nominal power is typically not fully utilized. Distribution transformers supplying residential buildings, for example, have an average loading of only 15 % to 20 % [17]. In fact, they are often specified for an expected maximum load of 50 %, meaning half of the installed power is never used. With additional loads in the LV AC grids, this percentage may increase slightly, but overall utilization remains low. Historical reasons limit utilization to 50 %. If one substation fails, a transfer switch can be closed so a nearby substation can take over the full load of both grid sections. Experience has shown that these scenarios are extremely unlikely, leaving the installed power of distribution grid transformers unused most of the time.

There are several ways to connect a multi-terminal DC grid to existing AC grids. Common methods use an active front end (AFE) in combination with galvanic isolation, either with a line-frequency transformer or a medium-frequency SST [5, 15]. The maximum efficiency of a 250 kVA line-frequency transformer is around 98 %, whereas the maximum efficiency of a three-phase dual-active bridge depends on the system design and can be 97 % or higher [5, 18]. In theory, both methods can achieve an efficiency of more than 99 %, though this is typically only possible at specific operating points [19, 20]. Generally, the dual-active bridge requires much less material; a 250 kVA 50 Hz isolation transformer weighs over 700 kg, whereas the medium-frequency transformer of a dual-active bridge weighs only 50 kg, plus the weight of two inverters [5, 18]. This difference is also evident when analyzing the GWP of the production of a rectifier with a line-frequency transformer. A life cycle assessment (LCA) was performed on a three-level grid-connected inverter with an isolation transformer. The ecoinvent database was used with the software openLCA to gather the GWP during the production phase [21–23]. The LCA shows that the isolation transformer contributes around 31 % of the greenhouse gases produced, as shown in Figure 1.3. Furthermore, the transformer significantly contributes to the GWP during the use phase due to its limited efficiency. Therefore, a solution that does not rely on a galvanic isolation between the AC and DC grids can reduce losses, material usage, GWP, and cost, as well as save space.

A potential solution can be found in VDE SPEC 90037, which proposes a DC system with AC-side grounding [24]. With this grounding scheme, additional galvanic isolation is unnecessary; the ground reference of the AC system is used instead. However, the absence of galvanic isolation between the AC and DC grids poses challenges to the system. An electrical circuit between the AC substations closes through the DC underlay grid due to the grounding of the transformer

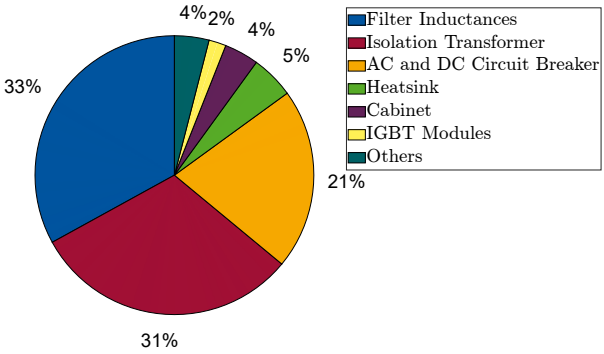


Figure 1.3: GWP percentage of various components of a three-level AFE.

star points [25]. This can lead to increased common-mode (CM) currents and circulating currents between the AC grids, which can increase losses and degrade the grounding components. It can also lead to protection issues in the AC distribution grid [26, 27]. Furthermore, there are concerns about unacceptably high electromagnetic emissions [27].

Aim of this Work

This work investigates the CM currents that arise in DC underlay grids with AC-side grounding to derive requirements for their implementation. First, the factors influencing the CM currents are determined by deriving a simplified model from the switching states of the AFEs and the grid configuration. Then, depending on the system configuration and the maximum permissible CM current, a design guide for the CM choke, which is the main component to mitigate CM currents, is developed.

Next, the converter control is examined and enhanced to minimize the common-mode voltage (CMV), which is identified as the excitation source of CM currents in this system. The modulation strategy significantly impacts the CMV; thus, existing modulation strategies are introduced and examined. Subsequently, novel modulation strategies for three-level inverters are developed to further reduce CMV and, consequently, CM currents. At the same time, the impact of the developed strategies on conducted electromagnetic interference (EMI) must be evaluated, as it is unclear whether the measures will have negative effects that

might necessitate further reduction efforts. To verify the validity of the developed models and concepts, a DC underlay grid with up to two infeed converters is constructed, and a series of measurements are performed and analyzed.

In summary, the overarching main objective is to identify the sources of CM currents in DC underlay grids with AC-side grounding and develop reduction methods through comprehensive analyses that enable the implementation.

Novelty of this Work

This work develops several novel contributions and concepts. First, a model based on the switching combinations of two three-level inverters is created. Next, this model is simplified into a CM model, which can be used to derive measures for reducing circulating CM currents. Then, the model is extended in multiple ways. Initially, CM capacitors in the DC grid are added. These capacitors may come, for example, from cable capacitances and EMI filters. Second, an extension to multiple infeed converters is made. Based on the derived models, a novel design guideline for CM chokes is developed that uses analytical equations to limit the CM currents to predefined values.

Furthermore, a novel method for synchronizing locally distributed converters without a direct communication connection is introduced. Since the models show that simultaneous switching or opposite switching can reduce the CM currents, synchronizing infeed converters is necessary. However, the use of additional wiring for communication links is generally undesirable. Therefore, using the time signal of the global navigation satellite system (GNSS) to synchronize converters is proposed. It is demonstrated that there is a delay of a few nanoseconds between two GNSS receiver signals. The delay is shown to be sufficiently short for the application at hand. Finally, the switching behavior and CM currents in a DC underlay grid are analyzed with two inverters synchronized with GNSS receivers.

Additional methods to reduce CM currents based on the control of three-level inverters are investigated. The models show that the CMV of the infeed converters excites the CM currents. Therefore, novel modulation strategies are developed to reduce the CMV of three-level inverters and, consequently, the CM currents. The first method focuses on adapting the modulation signal to ensure that only specific switching states are used. To accomplish this, one phase is clamped to the DC midpoint at all times. However, this significantly

restricts the converter's linear operating range. Therefore, a hybrid modulation scheme is adopted to counteract this issue. The second method modifies the carrier waves to enable reduced CMV operation with different modulators. This novel modulation scheme is tested with two inverters and is shown to reduce CM currents in combination with conventional sine-triangle pulse width modulation (SPWM), space vector pulse width modulation (SVPWM), virtual space vector pulse width modulation (VSVPWM), and the novel hybrid-discontinuous sinusoidal pulse width modulation (HDSPWM) in different configurations and operating points.

Finally, the techniques and requirements for testing conducted EMI in DC grids are investigated. Various standards regarding possible measurement methods for infeed converters in DC grids are examined. These findings are used to investigate and discuss the influence of different modulators and the use of multiple infeed converters on conducted EMI. They are also linked to previous findings on CM currents.

Outline of this Work

This work is divided into five main chapters. A brief introduction to these chapters is provided below.

Chapter 2: Low-Voltage DC Underlay Grid

This chapter introduces the LV DC underlay grid and describes its operation according to VDE SPEC 90037 and other applicable standards. Next, two-level and three-level inverters are introduced and compared. Then, the demonstration setup, built to resemble a DC underlay grid with AC-side grounding and two infeed converters, is presented. Lastly, the converter control for the three-level neutral point clamped (3L-NPC) converter used in the demonstration setup is introduced.

Chapter 3: Modeling Common-Mode Currents

Chapter 3 contains the derivation of an analytical model for the CM currents in a DC underlay grid with AC-side grounding. First, only one phase is considered

in order to establish a relation between the switching states, passive components, and CM currents. Then, this model is extended to consider all three phases, and a simplified, single-phase CM model is found. Subsequently, several additions are made to the simplified model to approximate the real system. Based on these models, a design guideline for CM chokes is developed to limit the CM currents to specified values. Finally, a measurement circuit for CMVs is introduced and implemented that captures high-frequency components and requires only a single voltage measurement.

Chapter 4: Optimized Modulation Strategies for Three-Level Inverters

This chapter introduces optimized modulation strategies for three-level inverters, beginning with VSVPWM, which ensures balanced DC link voltages at all operating points. The general pulse width modulation (PWM) model for three-level inverters is presented for the implementation of VSVPWM, which can be used to implement the modulator with a space vector approach while still generating switching signals with carriers. Next, a novel modulation strategy is derived that reduces the CMV by clamping one phase to the midpoint. However, this restricts the linear operating range. Therefore, a hybrid modulation scheme is implemented that seamlessly switches between SPWM and the discontinuous PWM, resulting in HDSPWM. Subsequently, carrier-based modulation strategies for reducing the CMV are investigated. First, the standard approach of phase disposition (PD) and the reduced CMV phase opposition disposition (POD) are introduced. Then, a novel carrier configuration called middle phase opposition disposition (MPOD) is proposed as an alternative method for carrier-based (CB) CMV reduction. Finally, SPWM, SVPWM, VSVPWM, and HDSPWM are combined with PD, POD, and MPOD, and the results are compared using test bench measurements.

Chapter 5: Experimental Analysis of Common-Mode Currents

Chapter 5 describes the experimental evaluation of CM currents in DC underlay grids and potential reduction strategies. First, the synchronization of locally distributed converters using a GNSS signal is analyzed, as well as its influence on circulating CM currents between two converters. Then, the use of one inverter with a capacitive CM load, representing cable-to-ground, PV panel capacitance, or EMI filter capacitors, is examined. The influence of different modulation strategies is evaluated and compared in this system. Next, a second converter is

added to the system, resulting in a realistic representation of a DC underlay grid with two infeed converters. Again, different modulation strategies are employed, and the resulting CM currents are analyzed. Additionally, simulation-based investigations are conducted to expand the scope of the measurement results to include other system configurations. Lastly, EMI measurements are performed with one and two converters to establish connections with the CM currents and to study the impact of various modulation strategies.

Chapter 6: Conclusions and Outlook

Chapter 6 provides a summary and conclusion of this thesis. Lastly, it offers an outlook on future research topics based on the presented concepts.

2 Low-Voltage DC Underlay Grid

The first chapter introduces the LV DC underlay grid system under investigation. Section 2.1 provides an overview of the system operation of DC grids with AC-side grounding based on VDE SPEC 90037 [24]. This section focuses on grounding schemes, voltage bands, protection, electromagnetic compatibility (EMC), and stray currents. Next, the two-level and three-level inverters are compared in terms of their CMVs. Section 2.3 introduces a demonstration setup of the DC underlay grid with two three-level inverters. This setup is used for all experimental investigations in this thesis. Lastly, the control strategy for the three-level inverters is presented, emphasizing conventional modulators, neutral point (NP) balancing, and dead time.

2.1 Operation of DC Systems with AC-Side Grounding

VDE SPEC 90037 [24] provides a broad overview of possible configurations for industrial DC systems. The VDE SPEC documents are technical guidelines and recommendations from the Verband der Elektrotechnik Elektronik Informationstechnik e.V. (VDE), but they are not yet standards. Therefore, they can be published more quickly and are more flexible, but they are not mandatory. VDE SPEC 90037 was developed in a collaboration with the *DC-INDUSTRIE* and *DC-INDUSTRIE2* project consortia and the Open DC Alliance (ODCA) [28, 29]. The document generally provides an overview of components, operational management, grounding concepts, protection, and EMC for DC installations. Some of this content was previously published in the book *Die Gleichstromfabrik*, which summarizes the *DC-INDUSTRIE* project's findings [30]. The following section introduces the most important aspects for this thesis. When appropriate or necessary, VDE SPEC 90037 is supplemented by existing standards.

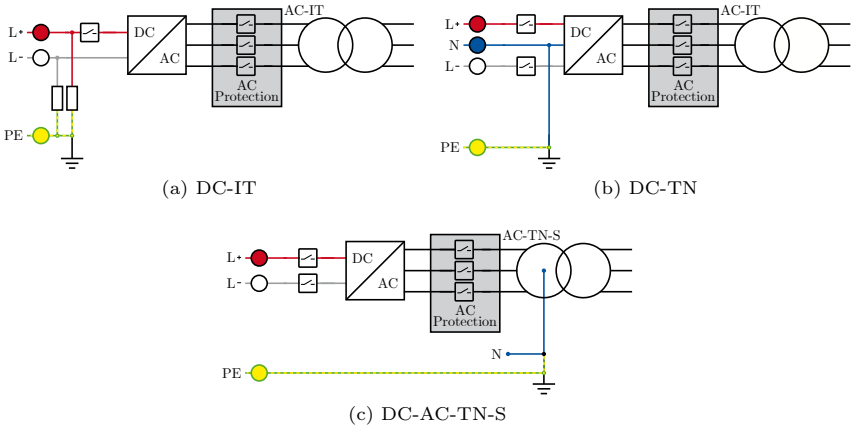
2.1.1 Grounding Schemes

VDE SPEC 90037 references three possible grounding schemes. According to the standard IEC 60364-1:2005, two of them are possible; however, the current version, IEC 60364-1:2025, added a DC system with AC-side grounding in Annex B for Germany, which contains notes concerning certain countries. In general, all systems are unipolar; bipolar grids are not considered in VDE SPEC 90037, as this would increase wiring work and complexity [24].

One possibility is to use an IT system that is galvanically isolated from the AC mains and uses high-impedance grounding, as shown in Figure 2.1 (a). Insulation monitoring devices are necessary to detect single-pole-to-ground faults, which can otherwise lead to an overloading of insulation and creepage paths. The advantages are that only one DC circuit breaker is required, fewer CM filters are needed, there is limited leakage current, and the risk of hazards is reduced. However, drawbacks include the necessity of galvanic isolation of the AC supply, symmetrization of the DC potentials against ground, difficult fault localization, and the necessity of galvanically isolated DC-DC converters for PV systems. [24]

The second possible grounding scheme is a DC TN-S system with a low-impedance grounding of the DC midpoint, as depicted in Figure 2.1 (b). This grounding scheme presents two major challenges. First, galvanic isolation between the DC and AC systems is necessary. Second, multiple earthing points can lead to significant DC balancing currents [24]. Therefore, VDE SPEC 90037 does not further analyze this grounding scheme. Nevertheless, this system has several advantages: it is similar to current LV AC installations; it theoretically allows for the use of the neutral line with half the DC voltage; and it has clearly defined potentials against ground. Furthermore, this grounding scheme is recommended in the technical rules of Current/OS, which aim to establish standards for DC distribution systems [31].

Lastly, the third possible grounding scheme is a DC system with AC-side grounding, as illustrated in Figure 2.1 (c). In this case, the star point of the AC system transformer is grounded, similar to the public LV distribution grid [25]. Unlike the other two concepts, the DC grid is formed without additional galvanic isolation. Therefore, this grounding scheme is advantageous in terms of cost, efficiency, and material usage, as it can operate with an existing AC-TN system. Furthermore, selective protection can easily be implemented due to high fault currents, similar to those in a DC TN-S system. However, disadvantages include the need for circuit breakers on both poles, substantial CM filtering, and



(a) DC-IT

(b) DC-TN

(c) DC-AC-TN-S

Figure 2.1: Possible grounding schemes in VDE SPEC 90037.

the prevention of DC stray currents. Additionally, using multiple infeed converters is challenging because it can lead to high CM currents, the main topic of this thesis. [24]

2.1.2 Operational Management

This summary covers various topics related to operational management, including voltage bands, power management, and stability. Precharging and discharging are not covered here. However, the requirements for devices can be found in VDE SPEC 90037.

VDE SPEC 90037 defines the voltage ranges in which different components can operate. The exact implementation is flexible and can be adapted as needed. Two nominal voltage bands are defined at 540 V and 650 V; however, these values do not correspond to the DC grid's no-load voltage. Depending on the voltage and how long these voltages are present, different operating states are defined and shown in Table 2.1. Generally, the red areas must be avoided, and devices are permitted to switch off; this also applies to the orange areas. Devices must continue working in the yellow areas but are allowed to reduce their power. Green areas indicate normal operating states. For example, if voltage band B4 is present for more than five seconds but less than 60 seconds, operating state

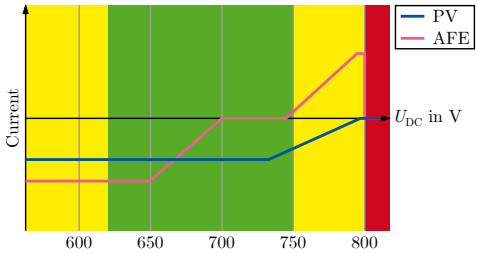


Figure 2.2: Exemplary droop curves in a DC grid according to VDE SPEC 90037.

Table 2.1: Operating states depending on system voltage and duration [24]

Upper voltage limit Ux in DC grid for nominal voltage 540 V / 650 V		**Voltage band**	S1: $t < 50$ µs	S2: 50 µs $\leq t \leq$ 1 ms	S3a: 1 ms $\leq t \leq$ 5 s	S3b: 5 s $\leq t \leq$ 60 s	S4: $t > 60$ s
Voltage	> 2000 V	B7	A7				
	880 V - 2000 V	B6	A6	A7			
	800 V - 880 V	B5	A4	A5	A5	A7	A7
	750 V - 800 V	B4	A3	A3	A3	A4	A5
	485 / 620 V - 750 V	B3	A3	A3	A3	A3	A3
	400 V - 485 / 620 V	B2	A4	A4	A2	A2	A2
	< 400 V	B1	A4	A2	A1	A1	

A4 is active. This means the device can reduce its power but must continue working. [24]

The system voltage is not fixed because droop curves are implemented to ensure a power balance between different devices. These curves adjust the current consumption or infeed depending on the voltage at the device. This also increases system stability as it acts as a virtual resistance. Furthermore, setting specific droop curves implements inherent power flow management. Figure 2.2 shows exemplary droop curves for different components in a DC grid. As can be seen, the PV system is always permitted to supply its maximum current until 730 V is reached; then, the current is reduced linearly to prevent further voltage increase. Conversely, the AFE begins feeding back current into the AC grid when the PV system reduces its current, thereby limiting the voltage. If the voltage drops below 700 V, the AFE begins to supply current from the AC grid. Other droop characteristics are also possible in principle, and must be evaluated based on the desired power flow and system behavior. [24]

2.1.3 Protection of DC Systems with AC-Side Grounding

A protection concept is necessary to ensure the safety of both components and people. This brief summary focuses on component protection. There are two possible fault scenarios: a ground fault, in which one or both lines are directly connected to ground, and a line-to-line fault. In the former, a low-impedance path emerges between one of the DC poles and the star point of the supplying transformer. This creates a current that flows through the freewheeling diodes of the AFE, primarily driven by the AC voltage. Thus, the time constant of the fault is in the millisecond range. Ideally, the fault clearance would happen selectively with a fast-switching device on the DC side, though it could also be switched off by an AC circuit breaker. Both DC lines must be protected because a ground fault can affect both poles. Regardless of how the fault is disconnected, the freewheeling diodes must withstand the fault current until it is cleared. [24]

In the second case, when both lines are connected due to a fault, the DC link capacitors discharge into the fault. Thus, the fault current slope and maximum value are limited only by the line and fault impedance. This results in very high fault currents that increase steeply. Once the capacitors discharge below the passive rectification voltage, the freewheeling diodes begin to conduct, increasing their thermal stress. Thus, the fault should be cleared shortly before or after this occurs. In summary, fast protection devices are necessary for both cases, and high fault currents ease fault detection and protection device tripping. [24]

As previously mentioned, it is possible for the AC transformer to disconnect in certain scenarios, such as when the AC circuit breaker interrupts the current. This results in a loss of ground reference for the system, causing it to behave like an IT system. However, since the protection concept is designed for high fault currents during ground faults, the system is no longer safe, as a ground fault on one DC line is no longer detectable. To prevent this, either the DC grid must be switched off, or additional insulation monitoring devices must be added so the system can operate as an IT system [24]. Redundant ground references are available when multiple AFEs with different transformer connections are used. Therefore, insulation monitoring devices are unnecessary; the DC grid is instead turned off if all ground references are lost which is less likely to happen the more connections are available.

In addition to overcurrents, overvoltages must also be limited. To this end, surge protection devices can be installed. However, traditional AC surge protection devices cannot be used for several reasons. There are specialized DC surge

protection devices for PV applications that can be used in DC grids if their specifications are sufficient. [24]

2.1.4 Electromagnetic Compatibility

Converters that operate at high frequencies can cause disturbances that lead to malfunction and interference with other components. Therefore, complying with EMC standards is necessary for all components in a grid to function without disturbance. There are existing limits and test procedures for AC grids that can also be applied to DC grids. VDE SPEC 90037 focuses on conducted emissions and only references some standards regarding radiated emissions. Therefore, the focus here is also on conducted emissions.

Three frequency spectra can be identified for conducted emissions: below 9 kHz, between 9 kHz and 150 kHz, and between 150 kHz and 30 MHz. The limit values for the last two ranges are adopted from existing AC standards. For the 9 kHz to 150 kHz frequency range, values from DIN IEC/TS 62578 are applied [32]. This standard describes the operating conditions and characteristics of active infeed converters, regardless of their technology or topology. It specifies limits for devices with nominal currents below and above 100 A. The 150 kHz to 30 MHz frequency range is adopted from DIN EN 55011, which specifies limit values for interference emissions of devices intended for industrial, scientific, medical, and household applications [33]. This standard distinguishes three power levels: below 20 kVA, 20 kVA to 75 kVA, and above 75 kVA. The limit values below 9 kHz were defined slightly above the interference voltage of an uncontrolled rectifier and via linear interpolation with the values from DIN IEC/TS 62578. Combining all these values yields the complete limits for interference voltages from 10 Hz to 30 MHz, as shown in Figure 2.3. [24]

Several components and measurement settings are necessary to measure EMI voltages. Line impedance stabilization networks (LISNs) are typically used to provide a defined termination impedance during EMI measurements. Versions for both AC and DC systems are available. There is a wide range of suppliers and models of LISNs for AC systems. However, DC-side LISNs are mostly used for PV systems, for which only a few LISNs are available, or for automotive applications, which have different impedance characteristics. DIN EN IEC 55016-1-2 mentions an alternative method for measuring EMI voltages without a LISN [34]. This method is based on CISPR 16-1-2 and is referenced in other standards, such as DIN EN 55011 and DIN IEC/TS 62578 [32, 33]. It uses a 1,500 Ω voltage probe consisting of a decoupling capacitor and a resistive voltage divider with a

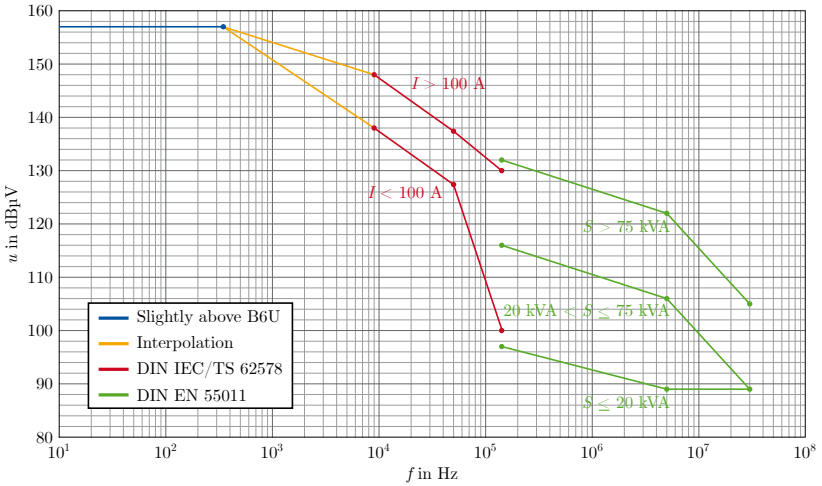


Figure 2.3: Quasipeak limit values for interference voltage between 10 Hz and 30 MHz [24].

minimum total resistance of 1,500 Ω between the line to be measured and ground. These probes are typically applicable to the entire frequency range from 9 kHz to 30 MHz. Although the standards and the manufacturers of these probes refer to this method, VDE SPEC 90037 only specifies its use in the 9 kHz to 150 kHz range [24]. For the frequency range from 150 kHz to 30 MHz, DIN EN 55011 proposes the use of a DC-LISN.

After installation, the measurement device is connected to an EMI test receiver according to the specifications of DIN EN IEC 55016-1-1 [35]. Unlike oscilloscopes, the device measures in the frequency domain rather than the time domain. EMI test receivers are also equipped with specialized inputs, such as hardware filters and mixers, as well as software that can perform measurements with different detector types and software filters. The EMI test receiver's software setup consists mainly of three components specified in DIN EN IEC 55016-1-1 and DIN EN IEC 55016-2-1: the resolution bandwidth (RBW), the step size, and the sweep time [35, 36]. The RBW is a Gaussian filter with a specified 6 dB bandwidth for measurements in different frequency spectra. For the frequency band from 9 kHz to 150 kHz, an RBW of 200 Hz is specified, and for the range from 150 kHz to 30 MHz, an RBW of 9 kHz is specified. Next, the step size must be defined, which is specified to be less than or equal to half the RBW. Thus, the frequency steps are 100 Hz and 4.5 kHz for the frequency bands from 9 kHz to

Table 2.2: EMI measurement settings with peak detector

Frequency band	RBW	Step size	Sweep time	Measurement time
9 kHz to 150 kHz	200 Hz	100 Hz	10 ms	14.1 s
150 kHz to 30 MHz	9 kHz	4.5 kHz	0.5 ms	2.985 s

150 kHz and from 150 kHz to 30 MHz, respectively. Finally, the sweep time per frequency step, which influences the total measurement time, is defined for the different frequency ranges, as well as for different detectors. The peak detector is generally recommended for evaluation or pre-compliance measurements, while the quasipeak detector is mandatory for final compliance measurements. One reason is the specified total measurement time. When using the quasipeak detector, the specified measurement times are 2,820 seconds and 5,970 seconds for the frequency bands of 9 kHz to 150 kHz and 150 kHz to 30 MHz, respectively. With the peak detector, these times are reduced to 14.1 seconds and 2.985 seconds, respectively. This yields sweep times with the peak detector of 10 ms and 0.5 ms, respectively. The measurement settings are summarized in Table 2.2.

If an external source is connected to the DC side of the converter during the measurements, a decoupling of the EMI produced by this source is necessary for precise results. Neither VDE SPEC 90037 nor the previously mentioned standards specify a suitable decoupling method. However, DIN EN 61000-4-6, which covers EMC testing and measurement techniques, provides a decoupling network for DC sources [37]. The network uses a combination of decoupling capacitors and low-frequency and high-frequency chokes to create a high asymmetric impedance across the entire frequency spectrum. The design of the decoupling capacitors is not specified in detail. Instead, the standard provides a typical value of 47 nF. Conversely, the inductance and impedance of the choke

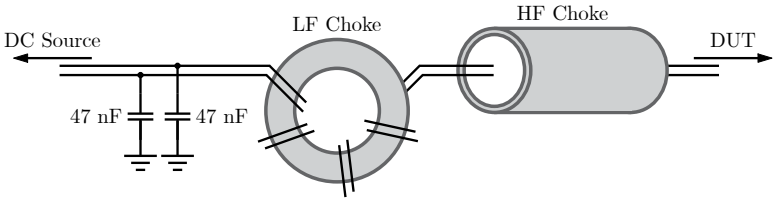


Figure 2.4: DC source decoupling network according to DIN EN 61000-4-6 [37].

are specified precisely: the minimum inductance at 150 kHz is 280 µH. Furthermore, the reactance should be greater than or equal to 260 Ω up to 24 MHz and greater than or equal to 150 Ω above 24 MHz. These requirements can be met by either a single choke or a combination of chokes.

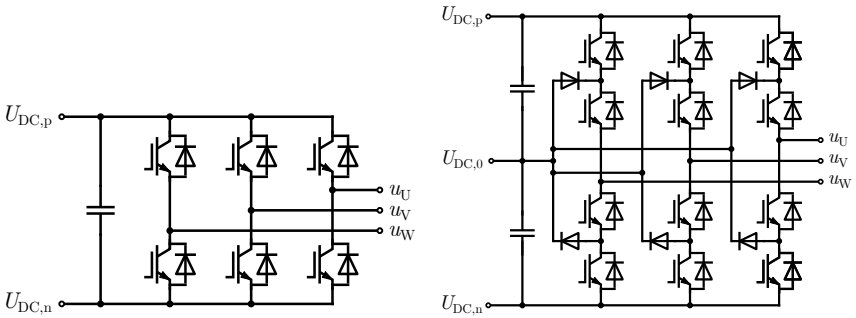
2.1.5 Stray Currents

Stray currents include leakage currents from EMI filters and parasitic capacitances, as well as currents that flow through the ground or other unintended paths. These stray currents must be avoided for several reasons, particularly in DC applications. They can cause corrosion under certain circumstances, as described in DIN EN 50162 [38]. Specifically, parasitic DC currents passing from a metal into an electrolytic medium, such as soil or concrete, can cause corrosion [24]. This can be dangerous for buildings with steel-reinforced concrete because the building's structural strength degrades over time. However, CM currents flowing through a capacitance to ground cannot lead to DC stray currents because the impedance is infinitely high impedance at 0 Hz. However, damaged insulation on cables or PV systems can lead to DC stray currents. These can be prevented by adding double insulation layers or shielding, or they can be detected by insulation monitoring devices. Using multiple AFEs in an AC-side grounded DC system can also lead to DC stray currents in specific cases.

Although AC stray currents do not cause corrosion, they can have other negative effects. For example, they can induce voltages in nearby systems that are actually zero-potential, and they can cause overheating [38, 39]. According to DIN EN 61008-1, a maximum value of 300 mA is permitted to prevent overheating, which can ultimately cause a fire [39].

2.2 Rectifier Topologies

Different topologies can be used to rectify AC to DC and feed the DC underlay grid. Line-commutated rectifiers that use diodes or thyristors are a low-cost, reliable solution. However, they require large filters and cannot offer grid services, fault ride-through capabilities, or bidirectional operation, which limits the use cases of the DC underlay grid. Therefore, only self-commutated and bidirectional topologies are considered.



(a) Two-level inverter (b) 3L-NPC inverter

Figure 2.5: Rectifier topologies considered as AFEs.

The two-level inverter, shown in Figure 2.5 (a), is the most popular topology that fulfills these requirements. It consists of six power electronic switches, such as insulated-gate bipolar transistors (IGBTs) with antiparallel diodes or metal-oxide semiconductor field-effect transistors (MOSFETs). The switches are arranged in three half-bridges, with one bridge assigned to each phase. Another possible topology is the 3L-NPC, shown in Figure 2.5 (b) [40]. This topology also consists of three half-bridges, but each half-bridge uses four switches with antiparallel diodes and two additional clamping diodes. Therefore, the 3L-NPC requires more components than the two-level inverter. Furthermore, control is more complicated because the number of active switches doubles, and ensuring the balance of DC link voltages is necessary [41, 42]. However, the increased number of switches provides several advantages to the 3L-NPC. First, since two devices are in series, each switch only has to block half of the DC link voltage. Additionally, the extra DC level decreases the distortion, allowing for smaller passive components or lower switching frequencies. Overall, these advantages can lead to higher possible efficiencies of the 3L-NPC [43, 44].

Another difference between the two converters is the CMV produced during operation. CMV can lead to distortions and unwanted CM currents, making CM filters necessary for reducing them. Thus, the following analysis details the CMV of two-level and three-level converters.

2.2.1 Switching States

First, the different switching states of the two topologies must be investigated. Considering only non-destructive switching states leaves $2^3 = 8$ states for the two-level and $3^3 = 27$ states for the 3L-NPC inverter. These numbers include two zero states for the two-level inverter and three zero states for the three-level inverter. Each switching state corresponds to one of the three phases connecting to the positive DC rail p, the negative DC rail n or to the midpoint o, which is only available for the 3L-NPC inverter. Thus, these switching states indicate the voltage at the three terminals u_{U}, u_{V}, and u_{W}. Finally, the converter's CMV u_{CM} can be calculated from these three voltages using Equation 2.1.

$$u_{\mathrm{CM}} = \frac{u_{\mathrm{U}} + u_{\mathrm{V}} + u_{\mathrm{W}}}{3} \tag{2.1}$$

Since the voltages are referenced to the midpoint of the DC link, the CMV can be normalized by dividing by $U_{\mathrm{DC}}/2$. Table 2.3 shows the resulting normalized CMV levels for the two-level and 3L-NPC inverters.

Only the normalized CMV levels of $\pm 1/2$ and $\pm 1/6$ are reached with a two-level inverter. For three-level inverters, the additional levels of $\pm 1/3$ and 0 appear. However, the $\pm 1/2$ voltage level is never reached during normal operation of three-level inverters because the switching states are not typically used with conventional modulators.

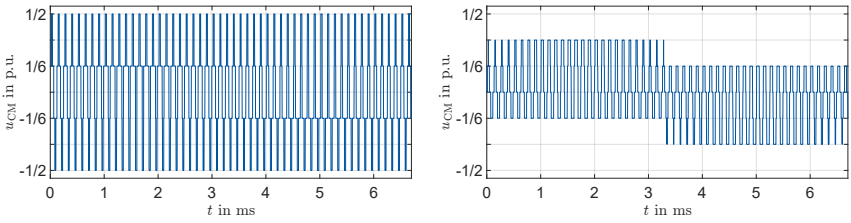
Table 2.3: Normalized CMV levels for all switching states of the two-level and 3L-NPC inverter

CMV	Two-Level Inverter	3L-NPC Inverter
$+1/2$	*ppp*	*ppp*
$+1/3$	-	*ppo*, *opp*, *pop*
$+1/6$	*ppn*, *pnp*, *npp*	*poo*, *opo*, *oop*, *ppn*, *pnp*, *npp*
0	-	*pon*, *opn*, *npo*, *nop*, *onp*, *pno*, *ooo*
$-1/6$	*pnn*, *npn*, *nnp*	*noo*, *ono*, *oon*, *pnn*, *npn*, *nnp*
$-1/3$	-	*nno*, *onn*, *non*
$-1/2$	*nnn*	*nnn*

2.2.2 Common-Mode Voltage Profile

As seen previously, the three-level inverter has more CMV levels, but the peaks are lower during normal operation. However, this does not necessarily mean that the three-level inverter produces less CMV. Therefore, a more in-depth analysis is carried out. Figure 2.6 shows the CMV profiles of a two-level and a three-level inverter with a modulation index of 0.8 using SVPWM. In this thesis, the modulation index is defined as one for three-quarters of a large vector, which corresponds to the linear modulation range of SPWM, as shown later in Figure 4.7. As expected, the CMV peak is higher for the two-level inverter than for the three-level inverter. Additionally, the CMV root mean square (RMS) value is 57 % higher, at 0.32 p.u. for the two-level inverter, compared to 0.20 p.u for the three-level inverter. The low-frequency components of the two frequency spectra are comparable, but the two-level inverter produces significantly increased frequency components at the switching frequency and its multiples. This can be seen in Table 2.3. During one switching cycle, the two-level inverter always switches between the two zero-states, producing a CMV of $\pm 1/2$, with steps of $1/3$. In contrast, the three-level inverter switches between $1/3$ and $-1/6$ or $-1/3$ and $1/6$, with steps of $1/6$. Since the step size and overall difference are smaller in each switching cycle, the CMV component at the switching frequency is much lower with the three-level inverter.

Furthermore, the three-level inverter provides more opportunities to reduce the CMV because it has multiple switching states that produce no CMV. These states can be utilized by adapting the modulator. Given these advantages, the 3L-NPC is chosen as the reference topology for this thesis. However, with slight adaptions, the general concepts and considerations of this thesis are applicable to two-level inverters and other active rectifier topologies.



(a) Two-level inverter (b) Three-level inverter

Figure 2.6: Exemplary CMV of two-level and three-level inverters.

2.3 Demonstration Setup

To validate the concepts in this thesis, a demonstration setup of a DC underlay grid with two AC terminals was built. Two 3L MiniSKiiP Evaluation Inverters from Semikron Danfoss are used as AFE converters [45]. Each inverter consist of three SKiiP 28MLI07E3V1 3L-NPC IGBT modules with gate drivers, an aluminum heat sink, two DC link capacitors in series with $2 \cdot C_{\mathrm{DC}} = 4.92$ mF each, three AC current sensors, and two DC link voltage measurements. Additional safety features are implemented to prevent a shoot-through and to detect overcurrents, overvoltages, and overtemperatures. With the given cooling system and gate drive units, a maximum AC current of 100 A and a switching frequency of up to 20 kHz are possible. However, a linear derating of the maximum allowed current is necessary, starting from 3 kHz down to 50 A at 20 kHz. To achieve a balance between losses and filter component size, a switching of $f_{\mathrm{sw}} = 8$ kHz was chosen, resulting in an AC current derating to 85 A. To remain below this threshold, the maximum current allowed for the inverters is 80 A, corresponding to a power of 50 kW at $U_{\mathrm{AC,N}} - 10$ %.

An LC filter was chosen for the differential-mode (DM) AC grid filter in the demonstration setup. The design of the AC grid side filter includes dimensioning of the inductance L_{f}, the capacitance C_{f} and the damping resistance $R_{\mathrm{f,d}}$. First, the minimum filter inductance value $L_{\mathrm{f,min}}$ is calculated based on the maximum current ripple Δi_{max}. Equation 2.2 provides an estimate of $L_{\mathrm{f,min}}$ [46].

$$L_{\mathrm{f,min}} = \frac{U_{\mathrm{DC}}}{24 \cdot \Delta i_{\mathrm{max}} \cdot f_{\mathrm{sw}}} \tag{2.2}$$

Assuming a maximum current ripple of 15 A, which corresponds to less than 20 % of the nominal current, and inserting the values for the given system yields a minimum inductance value of $L_{\mathrm{f,min}} = 243$ µH. Since a higher value than the theoretical minimum is recommended and different modulation strategies than those assumed in the design guide are allowed, an inductance of $L_{\mathrm{f}} = 480$ µH is chosen.

Next, the filter capacitance must be sized. This can be done using the resonance frequency f_{res} of the LC filter, which can be calculated with Equation 2.3.

$$f_{\mathrm{res}} = \frac{1}{2\pi} \cdot \sqrt{\frac{1}{L_{\mathrm{f}} \cdot C_{\mathrm{f}}}} \tag{2.3}$$

A low resonance frequency is preferable because the filter has an attenuation of $-40\ \frac{\mathrm{dB}}{\mathrm{dec}}$ beginning at the resonance frequency. Considering only Equation 2.3,

a high value of C_f seems beneficial. However, a capacitor increases reactive current, which increases losses in $R_\mathrm{f,d}$. It also affects the power factor, which must be corrected by the converter. Thus, a trade-off between reactive power and resonance frequency must be made. Using a capacitance value of $C_\mathrm{f} = 20\ \mu\mathrm{F}$ yields a resonance frequency of $f_\mathrm{res} = 1.6$ kHz, which is five times lower than the switching frequency. This value results in a reactive power of -1 kVA, corresponding to 2.5 % of the nominal power.

Finally, the damping resistor $R_\mathrm{f,d}$ must be sized, which affects the damping factor ζ, as defined in Equation 2.4, of the LC filter. For $\zeta > 1$, the system is overdamped, and for $\zeta < 1$, the system is underdamped. Thus, a higher value of ζ yields a lower resonant peak, reducing oscillations at the resonance frequency. If the damping is low, however, oscillations at the resonance frequency can occur. Conversely, if the damping is high, the LC filter behaves more like a regular L filter. The damping factor can be calculated using Equation 2.4.

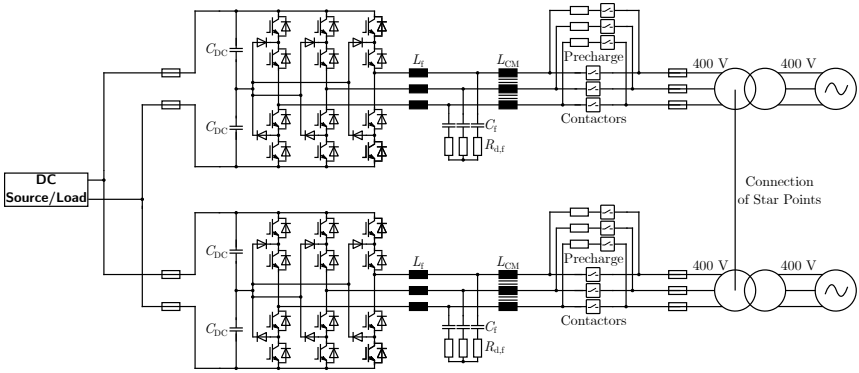
$$\zeta = \frac{R_\mathrm{f,d}}{2} \cdot \sqrt{\frac{C_\mathrm{f}}{L_\mathrm{f}}} \tag{2.4}$$

As can be seen, a higher $R_\mathrm{f,d}$ value increases the value of ζ. At the same time, this reduces the attenuation of the LC filter above the resonance frequency and increases losses in $R_\mathrm{f,d}$. To find a compromise, $R_\mathrm{f,d}$ is set to 2.7 Ω, yielding a damping factor of $\zeta = 0.28$. In addition to the DM filter, an AC CM choke L_CM is installed. The design of the CM choke will be shown in Chapter 3.

A set of contactors is added to disconnect the system from the AC grid and to precharge the DC grid. The 3L-NPC passively charges the DC grid through the freewheeling diodes up to the passive rectification voltage when the precharging contactors are closed. The 30 Ω resistors in the precharge path limit the high inrush currents that could otherwise destroy the inverter's freewheeling diodes. During normal operation, the main contactors close and conduct the AC current. Additionally, fuses with a nominal current rating of 80 A are installed on the AC and DC sides to protect the inverters. On the DC side, automotive fuses rated for a DC voltage of 1000 V are used.

Finally, two different Dyn5[(i)] isolation transformers are used to model distribution grid transformers, to which the AFEs are connected. The star points of both transformers are connected to simulate the grounding of the star points of real distribution grid transformers. However, the star points are not connected

[(i)] Dyn5 is a transformer connected in a delta configuration on the primary side and in a star (wye) configuration with a neutral wire on the secondary side. There is a phase shift of 150° between the primary and secondary sides.



(a) Schematic overview



(b) Real setup

Figure 2.7: Overview of the demonstration setup for experimental analysis.

to the public grid ground to precisely determine the CM current path and study different influencing factors. Thus, the transformer's star points act as a virtual ground potential, which may result in slight discrepancies compared to a DC underlay grid with AC-side grounding installed in the public distribution grid. Figure 2.7 (a) shows the schematic overview of the demonstration setup.

All components are built into the demonstration setup, as shown in Figure 2.7 (b). The transformers are located on the left side, outside the cabinet. In the bottom region, the inverters, the CM and DM filters, and the DC fuses are installed. The middle region contains the contactors, star point connection, and AC fuses. Additionally, the measurement equipment and control board are placed here. The auxiliary supply and the computer, which is used to connect to the control boards and oscilloscopes, are installed in the top region.

2.4 Control of Three-Level Neutral-Point Clamped Inverter

A general control strategy is implemented for the 3L-NPC inverters introduced in the previous section. Next, conventional modulators are described briefly, as they have a significant impact on the converter's behavior. Finally, two challenges of the converter control are discussed: NP balancing and dead time.

A standard control strategy for inverters is the cascaded model-based feedback control, consisting of an inner current control loop and an outer voltage control loop. These control loops are implemented in a synchronous reference frame (SRF), which rotates at the grid frequency f_g. The necessary grid angle is estimated by an SRF phase-locked loop (PLL). Finally, a modulator generates the switching signals for the IGBTs from the command voltage output of the current controller. Figure 2.8 shows a general overview of the controller [47].

The PI regulator of the PLL is set to a proportional gain of $2\pi \cdot 5$ and an integral gain of 0.001 [47]. To improve the PLL's response time, which is beneficial for fault ride-through capability, a higher proportional gain and thus a higher bandwidth should be used.

A model-based approach is used to design the main control loop parameters, which are then refined [48]. This approach yields current and voltage controller bandwidths of 400 Hz and 25 Hz, respectively. These values are then used to calculate the regulator's proportional and integral gains. Higher bandwidths are

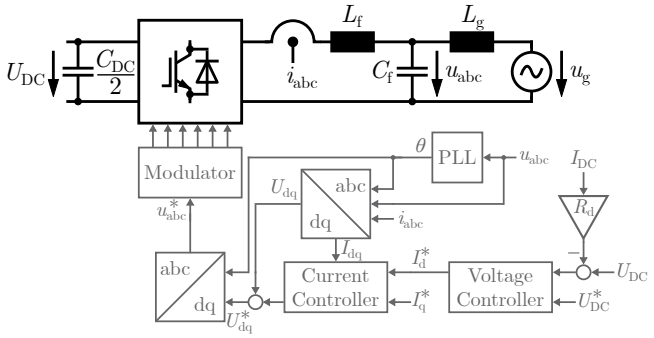


Figure 2.8: Block diagram of the converter controller.

possible, but they can negatively affect the total harmonic distortion (THD) of the output currents.

Additionally, a droop control is implemented alongside a regular inverter control to ensure stability of the DC grid [49, 50]. Furthermore, it enables more equal power sharing among multiple infeed converters [51, 52]. The droop resistance R_d for this controller is calculated based on the nominal current and an allowed voltage band of ± 7.5 %. This results in a droop resistance of $R_d = 735\text{m}\Omega$. The DC current which is used to calculate the droop voltage is derived according to Equation 2.5.

$$I_{DC} = \frac{U_d \cdot I_d}{U_{DC}} \tag{2.5}$$

Here, U_d and I_d represent the direct axis voltage and current components, respectively. Furthermore, harmonic controllers are implemented to improve the THD, though they are not shown in Figure 2.8 [47]. They also minimize the impact of dead time by reducing the harmonics it introduces. In addition to the Park transformation at the grid frequency, Park transformations are implemented for the negative fifth and seventh harmonic [47]. Subsequently, a slow I controller regulates the corresponding currents to zero.

2.4.1 Conventional Modulators

The modulator significantly influences the converter's output behavior and is the primary distinction in controlling two-level and three-level inverters. This thesis presents different PWM methods. One popular and simple method for

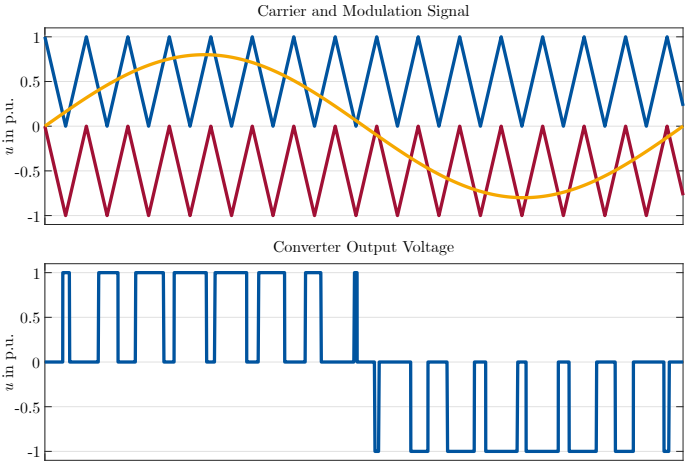


Figure 2.9: PD PWM carrier and modulation signal with the three-level output voltage.

generating switching signals from a modulation signal is using SPWM. The sinusoidal modulation signal, the controller's output, is compared to a triangular carrier signal. If the modulation signal is greater than the carrier signal, the output switches to '1'; otherwise it switches to '0'. For good reproduction of the modulation signal, the frequency of the carrier signal, which corresponds to the switching frequency of the converter, must be much higher than the fundamental frequency.

Two-level inverters only require one carrier per phase, as they need only a single output, which is provided as complementary signals to the two switches per phase. However, three-level inverters have four switches per phase and thus require double the switching signals. In general, an N-level inverter requires a minimum of N-1 carriers [53]. A beneficial multi-carrier method for multilevel inverters is PD PWM, which uses two carriers in phase but with vertical displacement [54, 55]. Figure 2.9 shows the general concept of PD PWM. As can be seen in the figure, the converter switches to the positive, middle, or negative DC bus, depending on how the modulation signal compares to the two carriers. PD PWM has two main advantages over other multi-carrier PWM methods: easy implementation and good harmonic output [53].

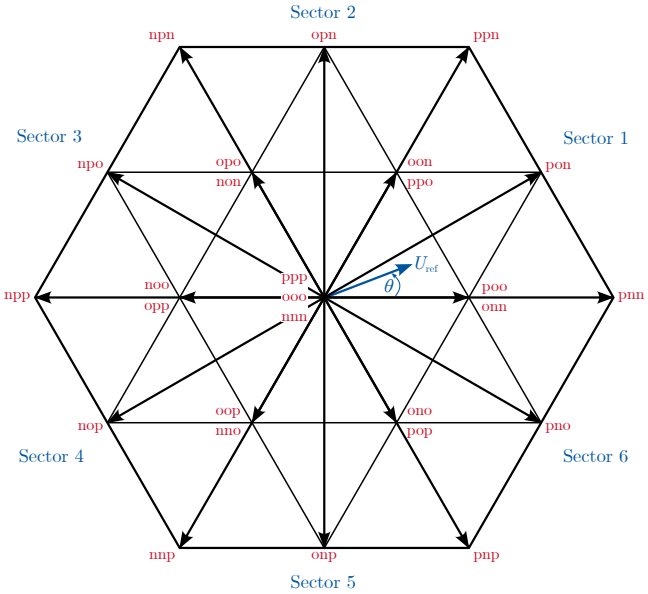
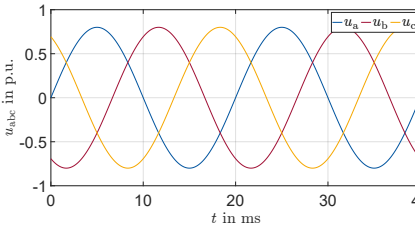


Figure 2.10: SVD of a three-level inverter.

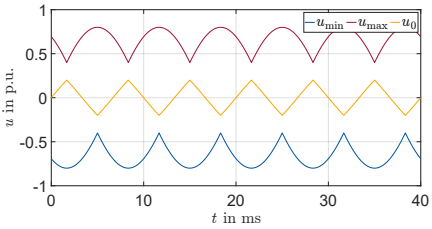
Another widely used PWM method is SVPWM, which offers several advantages over SPWM [56]. Specifically, it can improve the harmonic performance, decreases switching losses, and increases the linear modulation range [57, 58]. Furthermore, it provides better control over the switching state selection. However, SVPWM's general concept is vastly different from SPWM's. First, the modulation signal must be transformed into α-β coordinates using the Clark transformation shown in Equation 2.6.

$$\begin{pmatrix} u_\alpha(t) \\ u_\beta(t) \end{pmatrix} = \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{pmatrix} \cdot \begin{pmatrix} u_{\text{a}}(t) \\ u_{\text{b}}(t) \\ u_{\text{c}}(t) \end{pmatrix} \tag{2.6}$$

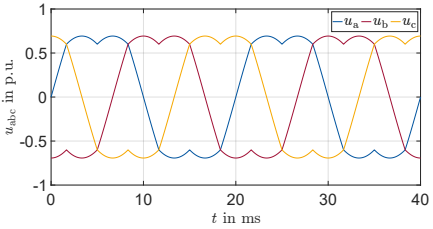
The resulting reference vector U_{ref} can be represented by its magnitude and angle θ. All of the switching states shown in Table 2.3 can be transformed into α-β coordinates, resulting in the space vector diagram (SVD) shown in Figure 2.10. The 27 switching states can be classified into three zero vectors, 12 small vectors, six medium vectors, and six large vectors. In the classical SVPWM approach, the three space vectors U_1, U_2, U_3 nearest to the reference vector are selected to recreate U_{ref} through vector addition. However, determining the three nearest



(a) Original modulation signals



(b) Calculation of u_0 with $u_{\min}$ and $u_{\max}$



(c) Modulation signal with zero-sequence

Figure 2.11: CB SVPWM generation with min-max injection.

vectors is not trivial, as the exact subsector must be found, which requires using both the magnitude and angle. Conversely, with a two-level inverter, only the angle is needed to find the three nearest vectors, and there are only six available subsectors. Then, the three vectors are applied for specific amounts of time – the dwell times T_1, T_2, T_3 – which respect the volt-second balance, as shown in Equation 2.7.

$$U_{\text{ref}} \cdot T_{\text{sw}} = U_1 \cdot T_1 + U_2 \cdot T_2 + U_3 \cdot T_3 \tag{2.7}$$

Here, T_{sw} is the switching period, which is equal to the inverse of the switching frequency. Furthermore, the sum of the dwell times must equal the switching period. Given these constraints, the dwell times are calculated within the SVPWM algorithm.

The output behavior of SVPWM can also be achieved using CB methods [58, 59]. The CB approach combines the advantages of SVPWM with the simple implementation of SPWM. To get a CB SVPWM representation, a suitable zero-sequence must be added to the modulation signal of each phase. The maximum and minimum voltage values of the original modulation signal $u_{\max}$ and $u_{\min}$

are used to calculate this zero-sequence u_0, as shown in Equation 2.8.

$$u_0(t) = \frac{U_{\mathrm{DC}}}{2} - \frac{u_{\min}(t)}{u_{\max}(t)} \tag{2.8}$$

Therefore, this method is also referred to as min-max injection [60]. As shown in Figure 2.11, the resulting zero-sequence voltage has a mean-free triangular shape with three times the fundamental frequency. Generally, more advanced strategies may require space vector-based modulation strategies because not all can be implemented using CB methods. Conversely, all CB methods can be implemented using a space vector approach because the exact vector sequence can be determined.

2.4.2 Neutral-Point Balancing

One challenge in controlling the 3L-NPC is maintaining a balanced DC link [41, 42, 61]. Otherwise, the DC link voltages could drift apart, leading to worse THD, instability, and component destruction. Two-thirds of the switching states in Figure 2.10 are associated with a current that increases imbalance by charging or discharging one of the two capacitors. This current is equivalent to the current flowing into the NP. Therefore, the zero and large vectors do not cause any imbalance in the DC link because they do not connect one of the phases to the midpoint. Conversely, the medium vectors cause a positive NP current because one phase is connected to o, and the small vectors cause a negative NP current with an amplitude equal to the phase current not connected to o. However, the actual current direction and value depend on the instantaneous phase current value of the specific phase. The switching states and their corresponding NP currents are shown in Table 2.4.

For a well-balanced DC link, the total NP current should be zero during one switching period. However, this is not the case for the modulators introduced in Section 2.4.1, which are only balanced for one-third of a fundamental cycle [62]. This results in a 150 Hz component in opposite directions on the individual DC link halves. Analyzing the vector sequences used in each sector of the SVD in Figure 2.10 can explain this. For each subsequent switching state, the NP current direction changes. Thus, there are six changes in the NP current direction in each fundamental cycle, corresponding to a third harmonic. Overall, the system remains stable, even with a low-frequency harmonic present on the DC link halves, and the total DC voltage is free of these harmonics, as they cancel each

Table 2.4: NP current of the 27 switching states

State	NP Current	State	NP Current	State	NP Current
ppp	0	poo	$-i_{\mathrm{a}}$	opp	i_{a}
ooo	0	oon	$-i_{\mathrm{c}}$	nno	i_{c}
nnn	0	opo	$-i_{\mathrm{b}}$	pop	i_{b}
pnn	0	noo	$-i_{\mathrm{a}}$	pon	i_{b}
ppn	0	oop	$-i_{\mathrm{c}}$	opn	i_{a}
npn	0	ono	$-i_{\mathrm{b}}$	npo	i_{c}
npp	0	onn	i_{a}	nop	i_{b}
nnp	0	ppo	i_{c}	onp	i_{a}
pnp	0	non	i_{b}	pno	i_{c}

other out. Nevertheless, this must be considered when designing the DC link capacitance, as it adds additional current stress and, consequently, heat.

2.4.3 Influence of Dead Time

A 3L-NPC half-bridge only permits certain switching states because the others are potentially or definitively destructive. Since the switching event of a semiconductor is delayed depending on the driver and the switch itself, directly forwarding the switching signals would lead to destructive switching states. Therefore, a turn-on delay, or dead time, is introduced to ensure the use of only the allowed switching states, summarized in Table 2.5 [63]. During main operation of the converter, the half-bridge switches between positive, neutral, and negative potentials by utilizing two transitional states. These states are only used during the dead time. The last allowed state is activated solely when the converter is in idle.

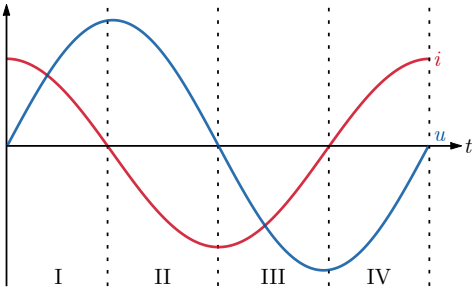
One drawback of dead time is that the converter output does not precisely match the desired output of the control algorithm. Instead, volt-seconds may be lost during the transition periods, leading to an increased THD [64, 65]. To analyze the converter behavior during dead time, one must analyze the current commutation path. Figure 2.12 (a) illustrates the four possible combinations of current and voltage during the converter operation. In this case, a positive current flows from DC to AC. However, the same sections occur during a reversed current flow, albeit in a different order.

Table 2.5: Allowed switching states of a three-level half-bridge

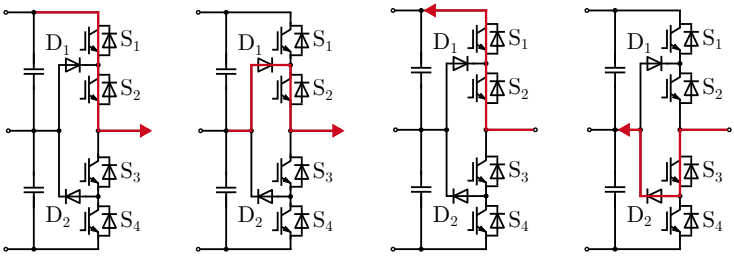
Switch	**Main**			**Transition**		**Idle**
S_1	1	0	0	0	0	0
S_2	1	1	0	1	0	0
S_3	0	1	1	0	1	0
S_4	0	0	1	0	0	0

As shown in Figure 2.12 (b) to (e), the current commutates between different diodes and switches in each section. In Section I, both the current and the voltage are positive. During the transition from p to o, switch S_1 turns off and switch S_3 is being turned on because they are complementary. However, current commutation to D_1 begins while S_1 is being turned off because there is no other possible path for the current than through D_1. Thus, during the dead time delay, the new switching state is reached, even though only S_2 is turned on. Conversely, when transitioning from o to p in Section I, the current begins to commutate when S_1 is turned on, which occurs after the dead time delay because S_3 is not conducting any current; thus, its switching state does not influence the current path. Therefore, volt-seconds are lost during this transition. The other sections can be analyzed analogously, with some transitions being influenced by the dead time delay and others not. Nevertheless, dead time does not lead to increased CMV levels, as it only delays transitioning to the next CMV state.

One exception to this may occur when reduced CMV modulation strategies, which limit CMV to $\pm 1/6$, are used and two half-bridges switch in a timely manner. In this case, switching states that are usually prohibited by these modulation strategies may be reached briefly. This can later be observed in some CMV measurements in Section 4. However, destructive states are still not activated, and the CMV of $\pm 1/3$ may only be active for a short time.



(a) Voltage and current waveform with sections



(b) Section I

(c) Section II

(d) Section III

(e) Section IV

Figure 2.12: Possible current paths of three-level inverters [65].

3 Modeling Common-Mode Currents

This chapter covers the modeling of CM currents in DC underlay grids with AC-side grounding to identify possible reduction techniques. Section 3.1 describes deriving a single-phase model for two inverters. This model is then extended to a three-phase model, which subsequently leads to a CM model. Next, the model is expanded to include more than two front end converters to investigate the behavior of a larger system. Section 3.4 shows the design of passive CM filters considering CM currents based on the analytical model. The final section presents a measurement method for an inverter's CMV that only requires a single voltage probe.

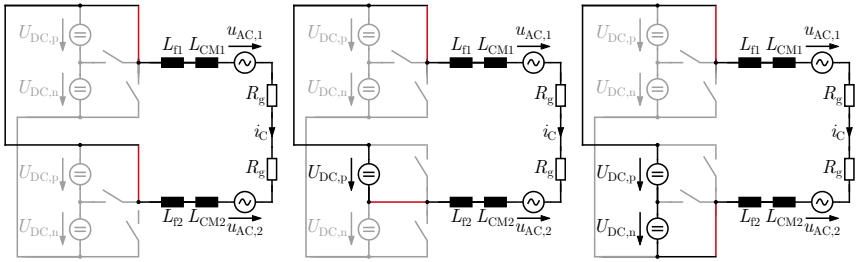
3.1 Single-Phase Model

A model of the DC underlay grid with two inverters is derived to estimate the resulting currents and identify suitable reduction strategies. The following simplifications are assumed to ease calculations and modeling:

- Only one phase is analyzed to understand the possible current paths of the two inverters' different switching combinations. The other two phases are omitted. This significantly reduces the number of possible switching combinations from $27 \cdot 27 = 729$ to $3 \cdot 3 = 9$.

- Ideal switches and inductors are used. Using these ideal components eliminates voltage drops across switching devices and winding resistances, both of which are expected to have a minor influence due to their low values. Additionally, the model simplifies switching events to have an infinite slope, which may affect high-frequency current components that are irrelevant to this model.

- Only an L filter instead of an LC filter is modeled. If their star point is not connected anywhere, the influence of the additional capacitors is expected to be low.



(a) State *pp* (b) State *po* (c) State *pn*

Figure 3.1: Current paths in simplified single-phase circuit with different switching combinations.

- An infinitely high DC link capacitance is used. Therefore, the capacitors can be replaced with ideal voltage sources, simplifying the system while introducing only minor deviations.

- Neither cable impedances nor CM and DM loads are included. The cable impedances are expected to be much lower than the filter impedances. Therefore, they can be omitted without altering the model's behavior. DM loads do not significantly influence the model, and a CM load will be added later.

- Perfectly symmetrical and balanced systems are assumed. In real systems, slight asymmetries may be present. However, their influence is expected to be minimal.

Figure 3.1 shows the simplified system. Examples of three different switching combinations and their associated current paths are presented. The following calculation determines the circulating current. To perform this calculation, differential equations are derived which result from the voltage change across the passive components. The full derivation of the circulating current can be found in Appendix A.1.

Analyzing Figure 3.1 (a), which shows the current path when both inverters are switched to the positive DC potential p, reveals that a current will only flow if there is a difference between the two AC voltages $u_{AC,1}$ and $u_{AC,2}$. Assuming the two AC grids are in phase and have similar amplitudes, the final value of the

CM current is zero. The same occurs for the other two switching combinations where both half-bridges are in the same switching state.

Figure 3.1 (b) shows the CM current path when the top inverter is switched to the positive DC potential p and the bottom inverter is switched to the NP potential o. Unlike the previous case, the positive DC voltage $U_{\mathrm{DC,p}}$ is switched across the passive elements, resulting in a non-zero final value for the CM current. To calculate the CM current, the inductances are summed as shown in Equation 3.1.

$$L_{\mathrm{tot}} = L_{\mathrm{CM1}} + L_{\mathrm{f1}} + L_{\mathrm{CM2}} + L_{\mathrm{f2}} \tag{3.1}$$

In Equation 3.2, the voltage sources are added together for a total voltage u_{tot}.

$$u_{\mathrm{tot}} = U_{\mathrm{DC,p}} - u_{\mathrm{AC,1}} + u_{\mathrm{AC,2}} \tag{3.2}$$

Finally, Equation 3.3 is used to calculate the circulating current.

$$i_{\mathrm{C}}(t) = \left(i_{\mathrm{C}}(0) - \frac{u_{\mathrm{tot}}}{2 \cdot R_{\mathrm{g}}} \right) \cdot \mathrm{e}^{-\frac{2 \cdot R_{\mathrm{g}}}{L_{\mathrm{tot}}} \cdot t} + \frac{u_{\mathrm{tot}}}{2 \cdot R_{\mathrm{g}}} \tag{3.3}$$

Even for unequal AC voltages, u_{tot} can be assumed to be constant because the switching frequency is much higher than the grid frequency, so $u_{\mathrm{AC,1}}$ and $u_{\mathrm{AC,2}}$ do not change significantly between two switching states. For the circuit in Figure 3.1 (c), only u_{tot} changes, as both DC voltages $U_{\mathrm{DC,p}}$ and $U_{\mathrm{DC,n}}$ must be added. Otherwise, Equation 3.3 remains the same. The other switching combinations that have not yet been analyzed generally behave similarly to those shown in Figure 3.1 (b) and (c). They switch either the positive or negative DC link voltage, or the sum of the two voltages, with a positive or negative sign across the other parts of the circuit. Therefore, u_{tot} is the only difference between the switching combinations. Equation 3.3 can be generalized with the new variables s_1 and s_2, which represent the switching state of the two half-bridges and can take the values 1, 0, and -1 for the switching states p, o, and n, respectively. This yields Equation 3.4 under the assumption that $U_{\mathrm{DC,p}}$ and $U_{\mathrm{DC,n}}$ are equal.

$$i_{\mathrm{CM}}(t) = \left(i_{\mathrm{CM}}(0) - \frac{(\mathrm{s}_1 - \mathrm{s}_2) \cdot \frac{U_{\mathrm{DC}}}{2} + u_{\mathrm{AC,1}} - u_{\mathrm{AC,2}}}{2 \cdot R_{\mathrm{g}}} \right) \cdot \mathrm{e}^{-\frac{2 \cdot R_{\mathrm{g}}}{L_{\mathrm{tot}}} \cdot t} + \frac{u_{\mathrm{tot}}}{2 \cdot R_{\mathrm{g}}} \tag{3.4}$$

Here, U_{DC} is the total DC link voltage, which is equal to the sum of $U_{\mathrm{DC,p}}$ and $U_{\mathrm{DC,n}}$. The initial condition $i_{\mathrm{C}}(0)$ is the circulating current at the switching instant, and this equation applies until the next switching action occurs.

Analyzing the simplified single-phase circuit yields key information about the circulating current i_{C}. If both inverters switch to the same DC potential, the

circulating current vanishes. Thus, these are the preferred switching combinations. Otherwise, the final value of the current depends on the voltage switched across the passive components and is limited only by the grounding resistance R_g. However, the sum of the inductances L_tot influences the time constant of the process, which is beneficial when different switching combinations are applied for a limited time.

3.2 Common-Mode Model

The single-phase model is used to derive a complete model of the three-phase system shown in Figure 3.2. All of the simplifications from the previous section remain valid except for the analysis of only one phase. Therefore, more switching combinations are possible, resulting in a parallel connection of three paths per converter. This parallel connection differs from Equation 3.4, which is only valid for a single-phase system. In the three-phase system, the circulating current splits up, so it is divided by three. However, all three phases contribute to the circulating current. The voltage switched across the system also changes and can be calculated using Equation 3.5, which sums the voltages of phases a, b, and c to the total three-phase voltage $u_{\mathrm{tot},3}$.

$$u_{\mathrm{tot},3} = \sum_{\mathrm{x=a,b,c}} \left((\mathrm{s_{1,x}} - \mathrm{s_{2,x}}) \cdot \frac{U_\mathrm{DC}}{2} - u_{\mathrm{AC,1,x}} + u_{\mathrm{AC,2,x}} \right) \tag{3.5}$$

Equation 3.5 and the single-phase Equation 3.4 are used to derive Equation 3.6.

$$i_\mathrm{C}(t) = \left(i_\mathrm{C}(0) - \frac{u_{\mathrm{tot},3}}{3 \cdot 2 \cdot R_\mathrm{g}} \right) \cdot \mathrm{e}^{-\frac{2 \cdot R_\mathrm{g}}{L_\mathrm{tot}} \cdot t} + \frac{u_{\mathrm{tot},3}}{3 \cdot 2 \cdot R_\mathrm{g}} \tag{3.6}$$

Here, L_tot consists of the two filter inductances L_f1 and L_f2, which are divided by three due to their parallel connection, as well as the two common mode inductances L_CM1 and L_CM2, which are not divided by three due to their coupling. The sum of the AC phase voltages and the switching states can then be simplified further. When the AC voltages are balanced, subtracting the two sums always yields zero, as demonstrated by Equation 3.7, regardless of the amplitudes or phases of the two AC grids.

$$u_{\mathrm{AC,1,a}} + u_{\mathrm{AC,1,b}} + u_{\mathrm{AC,1,c}} - u_{\mathrm{AC,2,a}} - u_{\mathrm{AC,2,b}} - u_{\mathrm{AC,2,c}} = 0 \tag{3.7}$$

Therefore, this part of Equation 3.6 can be omitted. Additionally, multiplying the sum of the inverter's switching states by half the DC link voltage and then dividing by three yields the CMV produced by the inverter, as shown in

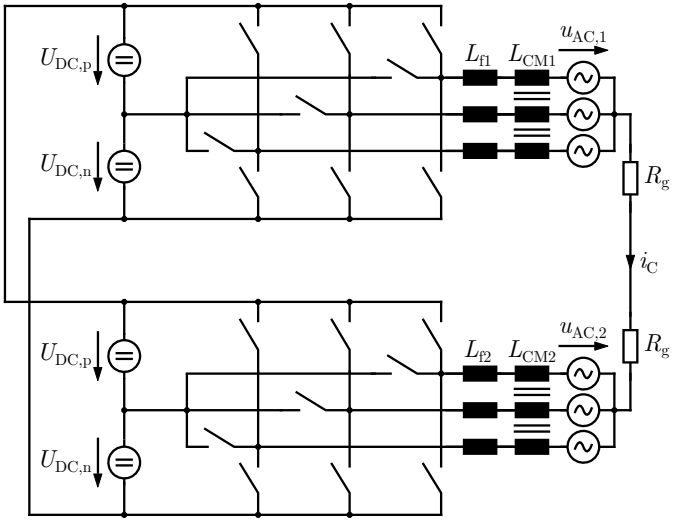


Figure 3.2: Simplified three-phase circuit for the analysis of circulating currents.

Equation 3.8.

$$\frac{\mathrm{s}_{1,\mathrm{a}} + \mathrm{s}_{1,\mathrm{b}} + \mathrm{s}_{1,\mathrm{c}}}{3} \cdot \frac{U_{\mathrm{DC}}}{2} = u_{\mathrm{CM1}} \tag{3.8}$$

The CMV of the second inverter u_{CM2} can be calculated analogously. Substituting Equations 3.7 and 3.8 into Equation 3.6 yields Equation 3.9 for the circulating CM current i_{CM}.

$$i_{\mathrm{CM}}(t) = \left(i_{\mathrm{CM}}(0) - \frac{u_{\mathrm{CM1}} - u_{\mathrm{CM2}}}{2 \cdot R_{\mathrm{g}}} \right) \cdot \mathrm{e}^{-\frac{2 \cdot R_{\mathrm{g}}}{L_{\mathrm{tot}}} \cdot t} + \frac{u_{\mathrm{CM1}} - u_{\mathrm{CM2}}}{2 \cdot R_{\mathrm{g}}} \tag{3.9}$$

Therefore, the system shown in Figure 3.2 can be simplified as presented in Figure 3.3. The other resistances and inductances that were omitted initially can be added to the existing passive components L_{tot} and R_{g}. To do so, the correct CM impedance must be used.

This model shows that the highest CM currents occur when u_{CM1} equals $-u_{\mathrm{CM2}}$. However, this scenario is only possible if u_{CM2} has a 60° phase shift against u_{CM1} and if both converters switch in the opposite direction. In principle, this is possible because different transformer vector groups are installed in the AC distribu-

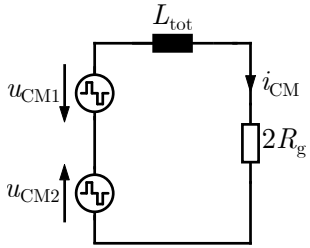


Figure 3.3: CM model for circulating currents [26].

tion grid, which can lead to a 60° phase difference between two LV distribution grids [25].

The CM model can be used to derive several measures to reduce the circulating CM currents. The circuit has four components: the grounding resistance R_{g}, the total CM inductance L_{tot}, and the two CMVs u_{CM1} and u_{CM2}. The grounding resistance cannot be influenced because it should be as small as possible to ensure the safety of the LV AC grid. However, L_{tot} can be modified by adding CM chokes to the inverters. Section 3.4 shows the calculation method for a suitable CM choke. Lastly, the two CMVs significantly impact the CM currents. Reducing the CMVs produced by the inverters or the difference between u_{CM1} and u_{CM2} is possible. This can be achieved by adapting the modulation strategy or by using simultaneous switching, both of which will be discussed in Chapters 4 and 5, respectively.

CM currents flow not only between two inverters in a DC underlay grid. Parasitic capacitances or bypass capacitors in EMI filters result in capacitive CM leakage currents to ground. PV modules, in particular, can have significant parasitic capacitances to ground because they have a large surface area in close proximity to ground [66]. Adding a CM capacitor creates a new current path, as shown in Figure 3.4. When the potential at point 0 changes, which occurs whenever u_{CM1} or u_{CM2} changes, the voltage across C_{CM} to the ground potential G changes. Without C_{CM}, this would result in rapid and significant changes in potential relative to ground, leading to high EMI voltages. However, the capacitor reacts with a current $i_{\text{CM,C}}$ and limits the voltage slew rate, which creates additional high-frequency CM current components in i_{CM1} and i_{CM2}.

The circuit shown in Figure 3.4 can be analyzed using the superposition principle. To do so, one of the sources is shorted, and then the current $i_{\text{CM,C}}$ is calculated. Next, the same is done for the other voltage source. For simplicity,

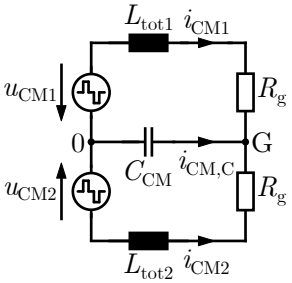


Figure 3.4: CM model including capacitive CM currents.

R_{g} is neglected in the following analysis. First, u_{CM2} is shorted, and then the resulting circuit is analyzed. With only u_{CM1} available, the inductance L_{tot1} is in series with the LC parallel circuit formed by C_{CM} and L_{tot2}. This creates a new pole in the system with a resonance frequency f_0 which can be calculated using Equation 3.10.

$$f_0 = \frac{1}{2\pi \cdot \sqrt{L_{\text{tot2}} \cdot C_{\text{CM}}}} \tag{3.10}$$

The frequency of the exciting source u_{CM1} is dominated by the converter's switching frequency f_{sw}. Therefore, when $f_{\text{sw}} < f_0$, the inductive component of the LC circuit prevails, making the circulating currents between the two converters dominant. However, when $f_{\text{sw}} > f_0$, the capacitance defines the behavior, reducing the impedance of the LC circuit, so only L_{tot1} limits the current slope. This results in the capacitive CM currents prevailing for large CM capacitances in the DC system. The condition for this is shown in 3.11.

$$C_{\text{CM}} > \frac{1}{(2\pi \cdot f_{\text{sw}})^2 \cdot L_{\text{tot2}}} \tag{3.11}$$

The reduction of CM currents through simultaneous switching is only viable if the condition in 3.11 is met. In this case, rather than reducing the difference between u_{CM1} and u_{CM2}, an opposing pattern would be more effective in reducing the sum of u_{CM1} and u_{CM2}, which would, in turn, reduce capacitive CM currents. However, the circulating current between the two inverters would be maximum with an opposing pattern.

Furthermore, if the switching frequency or its multiples align with the resonance point, the CM currents become large due to low damping in the system, even when resistances are taken into account. When the CM inductances L_{tot1} and L_{tot2} differ, two resonance points emerge. The resonance point of one converter's

CM inductance and C_{CM} creates high CM currents in the other converter's path. Thus, adding arbitrary components with CM capacitance can lead to instabilities and must be carefully evaluated. However, devices with these specific CM capacitances can be connected to the grid if an additional DC CM choke is placed on the grid side of these components or the AFEs. Adding a choke decouples the CM capacitance from the rest of the grid by shifting the resonance point and simultaneously adds damping to the resonance circuit.

Finally, the CM currents in this system can be estimated using the model. First, the CMV must be analyzed because it is the exciting source. If the middle phase voltage is positive, the CMV switches between $-U_{\mathrm{DC}}/6$ and $U_{\mathrm{DC}}/3$. Conversely, if the middle phase voltage is negative, the CMV switches between $U_{\mathrm{DC}}/6$ and $-U_{\mathrm{DC}}/3$. For a steady state of the CM currents, the volt-second product of the positive and negative CMV components must be equal. Therefore, the maximum possible volt-second product is $U_{\mathrm{DC}}/6$ for half a switching period $T_{\mathrm{sw}}/2$. When $f_{\mathrm{sw}} < f_0$, the difference between the CMVs significantly contributes to the CM current. This is contrary to the case when $f_{\mathrm{sw}} > f_0$, where the sum of the CMVs contributes to the CM current. In both cases, however, the maximum possible volt-second product is $U_{\mathrm{DC}}/6 \cdot T_{\mathrm{sw}}$. Combining this with the equivalent circuit shown in Figure 3.3 for $f_{\mathrm{sw}} < f_0$ yields Equation 3.12, which can be used to calculate the peak CM current.

$$\hat{i}_{\mathrm{CM}} = \frac{1}{2} \cdot \frac{T_{\mathrm{sw}} \cdot U_{\mathrm{DC}}}{6 \cdot (L_{\mathrm{tot1}} + L_{\mathrm{tot2}})} \tag{3.12}$$

The factor of $1/2$ arises from the conversion of the peak-to-peak current to the peak value. In the case of $f_{\mathrm{sw}} > f_0$, Equation 3.12 still holds, but only one inductance must be considered when calculating the capacitive CM current $\hat{i}_{\mathrm{C,CM}}$. However, the individual CM current peaks $\hat{i}_{\mathrm{CM1}}$ and $\hat{i}_{\mathrm{CM2}}$ are the same as in the case of $f_{\mathrm{sw}} < f_0$ because the current splits up equally between the two paths. Therefore, the CM currents cannot be reduced by the timing of switching actions when $f_{\mathrm{sw}} > f_0$.

3.3 Model Extension for Multiple Front Ends

In general, it is possible to have more than two AFEs in a DC underlay grid. Therefore, the CM model for two inverters must be extended. For this extension, the CM capacitance is again neglected. Figure 3.5 shows an exemplary system that models n inverters feeding a common DC grid. It is assumed that the inductances and resistances in each converter system are equal.

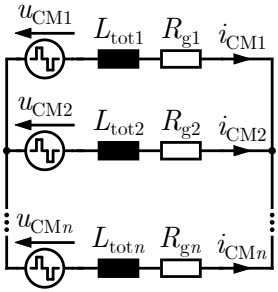
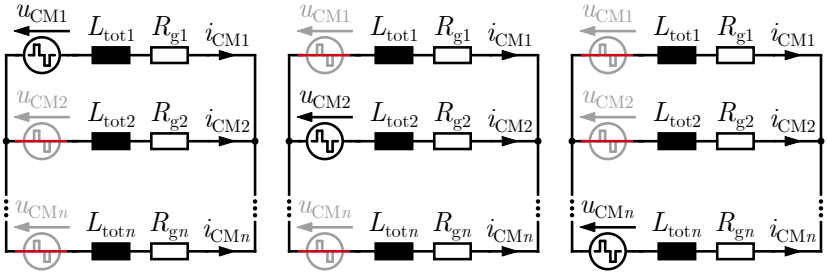


Figure 3.5: CM model for circulating currents with n inverters.

Several methods are available for calculating the individual CM currents. As before, the superposition principle can be used to understand the influence of multiple converters on the CM currents. First, only the CMV source u_{CM1} is considered, and the other sources are shorted, as shown in Figure 3.6 (a). In this case, the first string current i_{CM1} is equal to the negative sum of all the other string currents. Since the passive elements of all systems are assumed to be equal, the current i_{CM1} splits up evenly. The same occurs when investigating the influence of the other sources individually, as shown in Figures 3.6 (b) and (c). Finally, the superposition principle is applied and the calculated currents in each string are summed. Thus, the CM currents in each string add up to zero when all CMVs are equal.

However, each source with a different CMV produces a non-vanishing current component that splits up between all the other strings. For simplicity, only the CMV source u_{CM1} is considered to produce a different pattern to analyze the current that arises in this scenario. According to the superposition principle, shorting all other sources leads to a reduction in the impedance of the current return path. For a larger number of inverters, the impedance becomes negligible; thus, only L_{tot1} and R_{g1} remain as passive components. This results in a system similar to the one in Figure 3.3, but without u_{CM2}. Therefore, under the assumption $u_{\mathrm{CM2}} = 0$, Equation 3.9 can be used. Compared to Section 3.2, the inductance and resistance are halved, but compared to the worst-case scenario in which $u_{\mathrm{CM1}} = -u_{\mathrm{CM2}}$, the voltage across the passive elements is also halved. Thus, the CM current i_{CM1} in the first string is comparable to the worst case scenario with two inverters. Investigating the influence of the other sources on the CM currents according to the superposition principle cancels out the other currents in each path. In this scenario, the only CM current that arises is the one produced by u_{CM1}, which entirely flows in its own string and splits evenly



(a) Superposition 1 (b) Superposition 2 (c) Superposition n

Figure 3.6: Superposition principle of CM model with n inverters.

across the other strings. If more CMVs are unequal, additional non-vanishing currents emerge, which can partially cancel each other out.

If the CM capacitances are not neglected, an additional current path emerges. As before in Section 3.2, it is assumed to be a single lumped capacitor. When increasing the number of converters in such a system, multiple factors influence the CM currents. In general, the CM current through the capacitor increases with each additional converter, because the number of sources producing CM currents increases, while the impedance in the superposition steps simultaneously decreases. Overall, the current in each string increases slightly, and the capacitive CM current splits up equally among all strings. Additionally, the addition of more AFEs shifts the resonance point to Equation 3.13, assuming all CM filter inductances are equal.

$$f_0 = \frac{1}{2\pi} \cdot \sqrt{\frac{n-1}{L_{\mathrm{CM}} \cdot C_{\mathrm{CM}}}} \tag{3.13}$$

Therefore, adding new AFEs to the system may require additional steps to reduce CM currents, which could necessitate redesigning CM filters.

3.4 Model-Based Design of Common-Mode Choke

As shown above, many factors influence the CM currents that can flow in a DC underlay grid with AC-side grounding. The models demonstrate that the CM

filter is a critical component that influences these currents. The following section presents a model-based design guideline for CM filters in this system.

3.4.1 Structure and Components of Common-Mode Filters

CM filters consist of two main components: an inductive CM choke and CM capacitors [67–74]. The choke suppresses CM currents, and the capacitors provide a low-impedance return path to either the reference potential, usually ground, or inside the converter system. However, connecting the CM capacitors to ground can lead to high leakage currents, and connecting them to the DC side of the converter can create a new low-impedance CM path inside the converter system that can saturate CM chokes. Therefore, the size of the capacitors should be chosen carefully for both options and kept small. Additionally, the capacitors form a resonant circuit with the CM inductances; therefore, the resulting pole should be kept away from existing excited frequencies, such as multiples of the switching frequency. Other filter topologies, such as CLC or LCL, are also possible but are not considered here [74].

The performance of the filter regarding CM current suppression is primarily influenced by the CM choke. Therefore, this section focuses on designing the CM choke. A three-phase inverter's CM choke consists of three windings around a single core [72]. This concept is similar to that of two windings for DC or

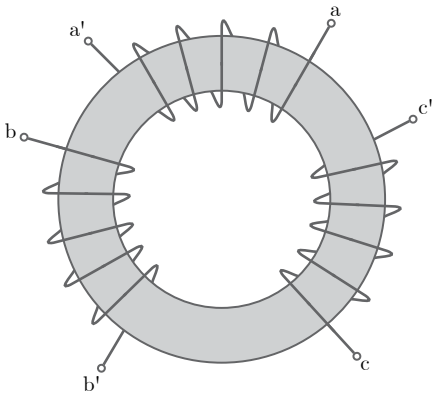


Figure 3.7: Conceptual drawing of a three-phase CM choke with a toroidal core.

single-phase AC systems and four windings for three-phase systems that use the neutral line. Toroidal cores are typically used because they are inexpensive, have low leakage flux, and have low thermal resistance [72]. Figure 3.7 shows a conceptual drawing of a three-phase CM choke with a toroidal core.

3.4.2 Design Guideline for Common-Mode Chokes in DC Systems with AC-Side Grounding

The goal of this design guideline is to estimate the necessary CM inductance L_{CM} to limit the CM currents to a maximum allowed value $i_{\mathrm{CM,max}}$, depending on the system specifications. Several parameters and equations must be considered to achieve this. Figure 3.7 shows that a CM choke consists of two elements: a magnetic core and copper windings wound around it. The inductance of the choke can be estimated using Equation 3.14.

$$L \approx \frac{\mu_0 \cdot \mu_\mathrm{r} \cdot N_\mathrm{w}^2 \cdot A_\mathrm{eff}}{l_\mathrm{eff}} \tag{3.14}$$

Here, μ_r is the relative permeability of the core material; N_w is the number of windings; A_eff is the effective core cross-sectional area; and l_eff is the effective length of the magnetic path through the core. These parameters are all specific to the core and are usually provided in the datasheet, except N_w. If the datasheet provides the inductance factor A_L, then Equation 3.14 can be simplified to Equation 3.15.

$$L = A_\mathrm{L} \cdot N_\mathrm{w}^2 \tag{3.15}$$

However, precisely calculating L_{CM} is not trivial because A_L and μ_r are often frequency dependent and have a tolerance of up to ± 30 % [75]. Both equations provide the ideal value of the inductance of one phase winding. To calculate the CM inductance of the entire choke, Equation 3.16 uses the coupling coefficient k_{CM} [72].

$$L_{\mathrm{CM}} = L \cdot \frac{1 + 2 \cdot k_{\mathrm{CM}}}{3} \tag{3.16}$$

In an ideal CM choke, k_{CM} is equal to 1. In real chokes, k_{CM} is close to 1 but slightly less than it. The difference between L and L_{CM} gives the leakage inductance L_σ of the CM choke, which influences the DM currents. L_σ can be calculated using Equation 3.17.

$$L_\sigma = L \cdot (1 - k_{\mathrm{CM}}) \tag{3.17}$$

If a current i is flowing through the windings, a magnetic flux Φ_{core} arises in the core, which can be calculated using Equation 3.18.

$$\Phi_{\text{core}} = \frac{L \cdot i}{N_{\text{w}}} = \frac{\mu_0 \cdot \mu_{\text{r}} \cdot N_{\text{w}} \cdot A_{\text{eff}} \cdot i}{l_{\text{eff}}} \tag{3.18}$$

If the magnetic flux in a specific area of the core becomes too high, the material saturates, meaning μ_{r} tends to 1. This leads to a reduction of L, which usually leads to a further increase of the current. The magnetic flux density B, or magnetic flux per area, can be calculated using Equation 3.19.

$$B = \frac{\Phi_{\text{core}}}{A_{\text{eff}}} = \frac{\mu_0 \cdot \mu_{\text{r}} \cdot N_{\text{w}} \cdot i}{l_{\text{eff}}} \tag{3.19}$$

Different core materials can have different saturation flux densities B_{sat}, which indicate where saturation begins. For instance, ferrite cores have a B_{sat} of approximately 400 mT, whereas nanocrystalline cores typically begin to saturate at around 1.2 T. However, incorporating an air gap into the core effectively increases these values while reducing μ_{r}. An important consideration for the saturation of CM chokes is that the DM currents can saturate the core through the leakage flux B_σ in the leakage inductance L_σ [72]. The leakage flux density can be calculated using Equation 3.20 [72].

$$B_\sigma = \frac{L_\sigma \cdot \hat{i}_{\text{DM}}}{N_{\text{w}} \cdot A_{\text{eff}}} \tag{3.20}$$

Only the leakage flux through air of each individual phase is considered. This flux does not intersect with the other phases, and it is assumed to be symmetrical. Therefore, the flux density of both the CM and DM components must be considered in the design. This yields the combined saturation flux density limit B_{sat} shown in Equation 3.21.

$$\begin{aligned} B_{\text{sat}} &> \frac{L_\sigma \cdot \hat{i}_{\text{DM}} + L_{\text{CM}} \cdot \hat{i}_{\text{CM}}}{N_{\text{w}} \cdot A_{\text{eff}}} \\ &= \frac{L}{N_{\text{w}} \cdot A_{\text{eff}}} \cdot \left(\hat{i}_{\text{DM}} \cdot (1 - k_{\text{CM}}) + \hat{i}_{\text{CM}} \cdot \left(\frac{1 + 2 \cdot k_{\text{CM}}}{3} \right) \right) \end{aligned} \tag{3.21}$$

The maximum DM current is equal to the peak current at nominal power. A limit must be set for the maximum CM current $i_{\text{CM,max}}$. Section 2.1 defined a limit of 300 mA for leakage currents. Since this is an RMS value, the peak CM current is $\sqrt{3}$ times larger, assuming a triangular current waveform, which yields a peak of 519.6 mA. Equation 3.21 shows that, with a coupling coefficient of $k_{\text{CM}} = 0.99$, an RMS DM current of 36.5 A leads to the same flux density as

the maximum CM current. Therefore, a high coupling coefficient is desirable to avoid saturation from DM currents.

Under the assumption that $L_{\mathrm{tot1}} = L_{\mathrm{tot2}} = L_{\mathrm{CM}}$, rearranging Equation 3.12 yields Equation 3.22.

$$L_{\mathrm{CM}} = \frac{U_{\mathrm{DC}}}{24 \cdot f_{\mathrm{sw}} \cdot \hat{i}_{\mathrm{CM}}} \tag{3.22}$$

Assuming $k_{\mathrm{CM}} = 1$, inserting 3.22 into 3.21 yields Equation 3.23.

$$B = \frac{U_{\mathrm{DC}}}{24 \cdot f_{\mathrm{sw}} \cdot N_{\mathrm{w}} \cdot A_{\mathrm{eff}}} \tag{3.23}$$

The dimensions of the core must also be taken into account. Depending on the inner circumference, only a limited number of turns can be realized. This can be calculated using the inner radius of the core r_{i} minus the outer radius of the winding $r_{\mathrm{w,o}}$. The maximum number of turns can be calculated using Equation 3.24, considering a fill factor k_{fill} to leave space between the windings.

$$N_{\mathrm{w,max}} = k_{\mathrm{fill}} \cdot \frac{\pi \cdot (r_{\mathrm{i}} - r_{\mathrm{w,o}})}{3 \cdot r_{\mathrm{w,o}}} \tag{3.24}$$

Only a single layer of wire is considered here to reduce the resulting stray inductance, which prevents the core from saturating due to DM currents.

Finally, the CM choke design can be carried out using the derived equations. The following steps must be followed to do this:

1. Calculate the minimum necessary CM inductance L_{CM} using Equation 3.22.

2. Calculate the number of turns N_{w} needed to reach L_{CM} using Equation 3.14 or 3.15.

3. Determine whether N_{w} is less than or equal to $N_{\mathrm{w,max}}$, which can be calculated using Equation 3.24. If not, add one core and return to Step 2.

4. Using Equation 3.23, calculate whether the saturation flux density B_{sat} of the material is exceeded. If so, add one core and return to Step 2.

For all calculations, a worst-case scenario must be assumed. Essentially, the tolerance of the core material of typically about ±30 % and the maximum possible DC voltage in a droop-controlled DC grid must be considered. Additionally, a small margin should be included for the stray inductance, especially if high DM currents are expected.

3.4.3 Construction of Common-Mode Choke for Experimental Analyses

Selecting a suitable core is essential for constructing a CM choke because the core's dimensions, permeability, and saturation flux density influence the final design. Two core materials can generally be considered for a CM choke: ferrite and nanocrystalline. Ferrites have medium permeability of around 500 to 10,000, but low saturation flux density, only reaching 400 mT. Nanocrystalline material, on the other hand, has a high permeability of 10,000 to 100,000 and a high saturation flux density of 1.2 T. Amorphous material has comparable parameters to nanocrystalline material, but it has a lower saturation flux density and is therefore not considered. Considering the base parameters of the two materials, it is evident that a higher number of turns or more core material is necessary with ferrites compared to a nanocrystalline core. Therefore, a nanocrystalline core was selected for the CM choke used in the experimental analyses.

According to the design guideline, the minimum necessary CM inductance must first be calculated using Equation 3.22. For this work, a CM current limit of 600 mA is used instead of 300 mA to allow for higher currents, given that no overheating is possible in the defined ground path of the test setup. Using a maximum DC voltage of 750 V and a switching frequency of 8 kHz yields a minimum CM inductance of 3.76 mH. Next, a core must be selected. The L2102-V080 core from VACUUMSCHMELZE is made of nanocrystalline VITROPERM 500 F material, has a nominal inductance factor A_L of 19.1 µH, an effective core cross-sectional area A_eff of 2.47 cm^2, an inner radius r_i of 35 mm, and a saturation flux density B_sat of 1.24 T [75]. Using Equation 3.15 yields a minimum number of turns N_w of 14. In the third step, the maximum number of turns is calculated using Equation 3.24. For this step, the cable used for the windings must be selected. It must be flexible and have a high current-carrying capability and sufficient voltage insulation. Based on these requirements, NSGAFOEU cable with a cross-sectional area of 10 mm^2 is selected, which has a nominal current rating of 98 A and an outer radius $r_\mathrm{w,o}$ of 4.35 mm [76]. With this value, Equation 3.24 yields a maximum number of windings of seven. Therefore, the second step must be redone with added cores. Rearranging Equation 3.24 and adding the parameter N_c for the number of cores yields Equation 3.25.

$$N_\mathrm{c} = \frac{L_\mathrm{CM}}{A_\mathrm{L} \cdot N_\mathrm{w}^2} \tag{3.25}$$

Inserting the values yields the necessary number of cores, which is four. Finally, calculating the maximum flux density in the core using Equation 3.23 yields 0.56 T, which is less than 50 % of B_sat. Therefore, no additional cores are neces-

sary to lower the flux density. The final CM choke, which has seven windings and four cores, should have a CM inductance of 3.74 mH, which is 0.5 % lower than the required value. Considering the ±30 % tolerance for A_L, a measurement of L_CM is necessary to determine the final inductance value of the CM choke. If the inductance value is too low, an additional core must be added to meet the requirement.

Two CM chokes were built according to the design. Using an LCR meter, the CM and DM inductances can be measured and compared to the design values. The CM inductance is measured between the terminals of one phase winding, and the DM inductance is measured by connecting the terminals of two windings and dividing the result by two. Using this method, the first CM choke was found to have a CM inductance of 4.49 mH and a DM inductance of 11.45 µH. Using Equation 3.17 yields a coupling coefficient k_CM of 0.9975, indicating that saturation of the core by DM currents is not expected. The second CM choke was measured to have a slightly lower CM inductance of 4.19 mH and a DM inductance of 8.14 µH. Calculating the coupling coefficient results in a similar value of 0.998. Overall, both CM chokes meet the previously calculated requirements.

3.5 Measuring Common-Mode Voltages

In principle, measuring the three inverter terminal voltages and using Equation 2.1 to calculate the CMV is a viable approach. However, this method requires three voltage measurements, which is disadvantageous because it necessitates three probes and three oscilloscope inputs. A simpler solution is to measure the CMV with a single voltage probe. To do so, an artificial star point is created by connecting capacitors and resistors between the three AC phases and a common connection. Measuring the voltage between this artificial star point and either the NP of the converter or the star point of the transformer yields the CMV. Figure 3.8 shows the measurement of the CMV against the NP.

An active or passive differential voltage probe can then be used to measure the CMV. However, these voltage probes have a non-ideal input impedance, typically expressed as a parallel capacitance and resistance. Together, they form a voltage divider with the capacitances and resistances of the artificial star point, as shown in Figure 3.9. The transfer function of this circuit is shown in Equation 3.26.

$$G(s) = \frac{u_\mathrm{out}}{u_\mathrm{CM}} = \frac{R_2 + s \cdot R_1 \cdot R_2 \cdot C_1}{R_1 + R_2 + s \cdot R_1 \cdot R_2 \cdot (C_1 + C_2)} \tag{3.26}$$

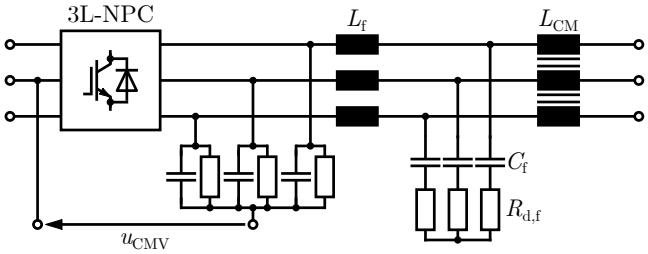


Figure 3.8: CMV measurement against the NP using an artificial star point.

Analyzing the frequency behavior at the boundaries is helpful. As s approaches 0, the function simplifies to Equation 3.27.

$$\lim_{s\to 0} G(s) = \frac{R_2}{R_1 + R_2} \tag{3.27}$$

As s approaches infinity, the function simplifies to Equation 3.28.

$$\lim_{s\to \infty} G(s) = \frac{C_1}{C_1 + C_2} \tag{3.28}$$

Equations 3.27 and 3.28 show that the resistive behavior dominates at low frequencies, while the capacitive behavior is relevant at high frequencies. Therefore, equating both equations is necessary to achieve an optimal frequency response of the system across the entire frequency range. This results in the condition for a frequency-compensated voltage divider, as shown in Equation 3.29.

$$R_1 \cdot C_1 = R_2 \cdot C_2 \tag{3.29}$$

This means that the time constants τ_1 and τ_2 of the two RC circuits must match. To calculate R_1 and C_1, the parallel connection of the resistors and capacitors must be calculated corresponding to their CM impedance. Figure 3.10 shows the response of the voltage divider to a block voltage input, comparable to the

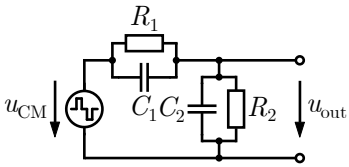
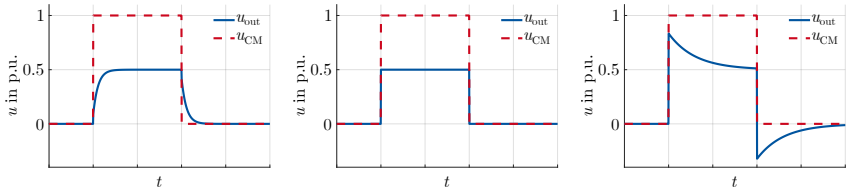


Figure 3.9: Voltage divider for measuring the CMV.



(a) $\tau_1 < \tau_2$ (b) $\tau_1 = \tau_2$ (c) $\tau_1 > \tau_2$

Figure 3.10: Voltage response to a square wave input for different time constants of the frequency-compensated voltage divider.

voltage waveform of a CMV signal. As can be seen, the circuit shows undercompensated behavior if $\tau_1 < \tau_2$, while the output voltage is overcompensated if $\tau_1 > \tau_2$. Neither is desirable because they do not perfectly divide the input voltage during transients.

For the CMV measurements in this thesis, a frequency-compensated voltage divider was constructed, consisting of a three-phase artificial star point and a corresponding voltage divider. Figure 3.11 shows the general setup of the CMV measurement circuit. This setup has advantages over direct measurement at the artificial star point, as shown in Figure 3.8, because the impedance of the frequency-compensated voltage divider can be matched independently of the voltage probe. First, the resistance and capacitance values of the artificial star point R_1 and C_1 are determined to design the voltage divider. For R_1, a sufficiently large resistance value is necessary so that the resistor does not reach its thermal limits. The maximum voltage between two phases of U_{DC} is split equally between two resistors R_1. Considering this, a resistance of 495 kΩ is chosen for R_1. The value for C_1 is determined by the voltage class of available surface-mounted device (SMD) ceramic capacitors. Since the capacitance decreases close to the nominal voltage, a high margin should be considered. At the same time, the capacitance value should not be too small; otherwise, the frequency compensation would not work. Considering these factors, a capacitance of 33.3 pF is chosen for C_1. Next, the division ratio of C_2, R_2, C_3, and R_3 must be calculated. Assuming a CMV source is connected between the circuit's inputs and output, the CM capacitance of the artificial star point must be considered in the division ratio calculation. If R_1 is significantly greater than $R_2 + R_3$, then the the output voltage amplitude u_{out} can be set independently of the artificial star point. Therefore, R_2 is chosen as 22 kΩ, and R_3 is chosen as 3.4 kΩ. The capacitance values C_2 and C_3 can finally be calculated using Equation 3.29, yielding values of 750 pF and 4.85 nF, respectively.

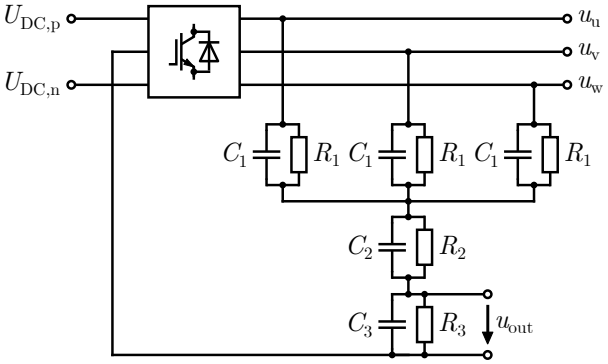
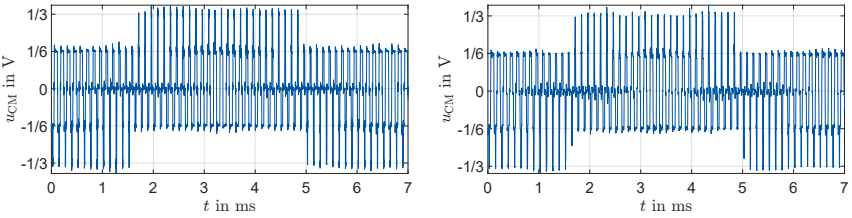


Figure 3.11: Voltage divider for CMV measurement with an artificial star point.

These values yield a division ratio of 1:56 and a maximum output voltage of about ±4.5 V. This voltage range is suitable for the use in ±5 V analog circuits and can be used as an input for many oscilloscopes. However, using this voltage as a direct input for an oscilloscope would elevate its input on a potential. Therefore, a differential probe is used to measure u_{out} during the experimental validations. This does not impact the frequency compensation or division ratio as the input impedance of the differential probe is much higher than the impedance of R_3 and C_3.

Two CMV probes were built to simultaneously measure the CMV of two inverters. Figure 3.12 shows the measured CMV of the two inverters. There seems



(a) PCB 1 (b) PCB 2

Figure 3.12: CMV measurement with two different printed circuit boards (PCBs).

to be an overshoot with slight oscillations present, as can be seen in the figure. However, it is later shown that these are generated by parasitic elements in the circuit, meaning the frequency compensation works as expected, and the CMV is represented correctly.

3.6 Summary

This chapter presents a single-phase model for analyzing the circulating current between two converters. Two phases are omitted to simplify the model. The resulting differential equations describing the current demonstrate its dependency on the converters' switching state, the DC link voltage, the grounding resistance, and the filter inductances.

Next, the three-phase system is analyzed in its entirety. A CM model is derived from the single-phase system's current equation by combining the switching states and DC link voltage into the CMV. If CM capacitances in the DC grid are neglected, the CM current depends mostly on the difference of the two CMVs. When a CM capacitance is considered on the DC side, however, the sum of the two CMVs determines the capacitive CM current. Additionally, a new resonance point emerges. The system behavior depends on whether the resonance point is below or above the converters' switching frequency. For large CM capacitances, the resonance point is below the switching frequency, resulting in capacitive CM current dominance. Conversely, for small CM capacitances, the resonance point is above the switching frequency and may be excited by the converters. In this case, the CM currents can be significantly reduced by switching the converters simultaneously. However, the line-to-ground capacitances of the DC grid move the resonance point below the switching frequency in a real system. Therefore, it is more likely that the resonance point will be below the switching frequency, allowing the capacitive CM currents to dominate in a real application.

Including more than two converters complicates the system but generally results in comparable behavior to that of a system with two converters. Each additional converter adds capacitive CM current components when considering CM capacitances in the DC grid. If half the converters switch in opposition, the capacitive CM current can be reduced; however, circulating CM currents arise between the converters. Depending on the system design, one CM current component dominates and should therefore be reduced by aligning the switching actions accordingly.

In general, the CM inductance is considered a primary element that limits CM currents. A high CM inductance can be achieved via a CM choke. Using the previously developed models, equations are derived to design a CM choke that limits the CM current to a specific value. According to the design guide, two prototypes are built, and the inductance calculation is validated with LCR meter measurements. Later, the CM chokes are used in the experimental analyses in Chapter 5 to determine whether they limit the current as expected.

Finally, a method for measuring the CMV of a converter with a single voltage probe is presented, because the CMV is identified as the exciting source for CM currents. A virtual star point is used in conjunction with a frequency-compensated voltage divider to measure the CMV. Two prototypes are built, and their measured CMV is analyzed. Although the measurements appear to show overshoots, which could suggest incorrect frequency compensation, it is later demonstrated that these are frequencies from specific resonance points. Therefore, the CMV measurement method is validated.

Three primary factors for reducing CM currents can be identified overall: the converter's CMV, alignment of the converter's switching actions with those of other converters, and CM inductance. This chapter has already analyzed the latter by presenting a CM choke design guide. Furthermore, a converter's CMV is significantly affected by the modulator, which selects switching states based on the voltage command from the converter control. Therefore, Chapter 4 analyzes modulation strategies for three-level inverters that reduce CMV. Additionally, Chapter 5 presents a simple, low-cost method for synchronizing the switching actions of locally distributed converters in a DC underlay grid. In summary, this work analyzes all the reduction techniques identified in this chapter.

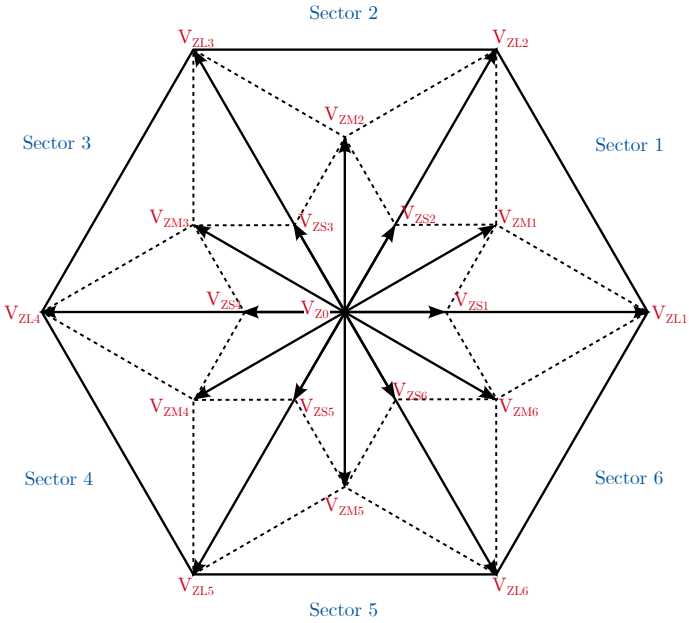
4 Optimized Modulation Strategies for Three-Level Inverters

This chapter contains an analysis of existing modulation strategies for three-level inverters, as well as the development of optimized modulation strategies. First, VSVPWM for three-level inverters is introduced. It is then used as an example for the generalized PWM model of NP clamped converters and active NP control. Next, a novel hybrid-discontinuous modulation strategy is developed using the PWM model. This new modulator should reduce the CMV in specific operating regions without compromising the operating range, comparable to SPWM. Section 4.3 proposes and explains different CB methods for reducing the CMV of three-level inverters. Lastly, the presented modulation strategies are implemented on a 3L-NPC demonstration setup and are compared to each other in terms of output current quality, DC link ripple, CMV, and efficiency.

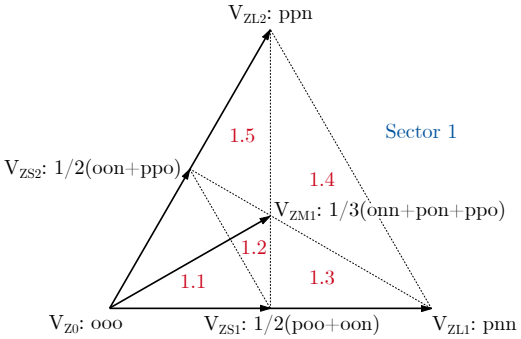
4.1 Virtual Space Vector Pulse Width Modulation

The general idea behind VSVPWM is to achieve a fully balanced DC link voltage without the low-order harmonics present in conventional modulators, such as SPWM or SVPWM. Additionally, the DC link balance is independent of the modulation index and power factor [77]. The concept of virtual vectors was initially introduced for direct torque control of motors using a 3L-NPC [78]. However, the definition and selection of virtual vectors for VSVPWM was introduced later [77].

As already shown in Table 2.4, small and medium vectors introduce an NP current that charges or discharges the DC link capacitors. To maintain a balanced DC link during a switching cycle, virtual vectors are introduced as a linear combination of two or three vectors, canceling out their NP current. Thus, unlike basic vectors in the SVD, a virtual vector does not describe an individual switching state, but rather a set of switching states. Figure 4.1 (a) shows the adapted SVD with virtual vectors instead of basic vectors. There are fewer virtual vectors than basic vectors, and their positions differ slightly, except for the large



(a) Complete diagram



(b) Sector 1

Figure 4.1: Virtual space vector diagram.

vectors. Figure 4.1 (b) shows the virtual vectors and their composition from the basic vectors in sector 1. The virtual vectors are selected according to the following rules:

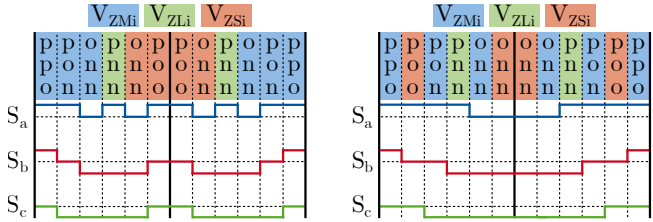
- The large virtual vectors (V_{ZLi}) and the zero vector (V_{Z0}) are identical to their basic vector counterparts because they do not introduce any NP current.

- Virtual small vectors (V_{ZSi}) are composed of two small basic vectors. These two vectors are activated for the same duration and must produce an opposing NP current. For instance, the vector *poo* yields an NP current of $-i_a$, while *oon* leads to an NP current of $+i_a$.

- Virtual medium vectors (V_{ZMi}) are obtained from two small basic vectors and one medium basic vector. Again, the three vectors are activated for an equal duration. However, the sum of the three NP currents must equal zero. For instance, *onn* produces an NP current of i_a, *pon* produces i_b, and *ppo* produces i_c, which sums to zero because $i_a + i_b + i_c = 0$.

Accordingly, the virtual vectors in the remaining sectors can be determined using the same rules. The modulation index and power factor do not influence the NP balance because the synthesis rules ensure that the NP current is always zero during a switching period.

Similar to SVPWM, the synthesis of a reference vector involves selecting the three nearest virtual vectors. One difference in this process is identifying the three nearest vectors, as the subsectors are slightly different and an additional subsector is available per sector. Figure 4.2 shows an exemplary vector sequence of VSVPWM in subsector 1.4. If the switching states remained in the same sequence generated by the sequential selection of virtual vectors, an increased number of switching actions would occur, as shown in Figure 4.2 (a). Therefore, the switching states are sorted in a way to minimize the number of switching actions in a switching period, as shown in Figure 4.2 (b). Furthermore, sorting the switching sequence prevents the need for simultaneous switching of multiple phases. However, Figure 4.2 (b) shows that the middle phase has to switch from *p* to *o* to *n*, which negatively affects the current output quality and increases the number of switching events in a switching period by two. This, in turn, can increase switching losses. These are the two main drawbacks of VSVPWM, in addition to its comparatively complex implementation. Nevertheless, complexity can be reduced by using a CB implementation, which has been developed [79]. However, this was not implemented in this thesis because further modifications to dwell times are carried out, as explained later.



(a) Unsorted (b) Sorted

Figure 4.2: Unsorted and sorted vector sequence of VSVPWM in subsector 1.4.

4.1.1 Calculation of Duty Cycles

In conventional SVPWM and VSVPWM, the duty cycle calculation involves comparing the real and imaginary parts of the vectors with the reference vector and solving the resulting system of equations. However, this approach is sector- and vector-specific, so it does not provide a general solution. Therefore, the general PWM model of NP clamped converters is adopted [79–82]. To simplify the calculations, times and voltages are normalized using the switching period T_{sw} and the DC link voltage U_{DC}. First, according to Equation 4.1, the voltages are classified as maximum, middle, or minimum to take advantage of the sixfold symmetry of the SVD.

$$\begin{aligned} u_{\mathrm{max}} &= \max\left(u_{\mathrm{a}},u_{\mathrm{b}},u_{\mathrm{c}}\right) \\ u_{\mathrm{mid}} &= \mathrm{mid}\left(u_{\mathrm{a}},u_{\mathrm{b}},u_{\mathrm{c}}\right) \\ u_{\mathrm{min}} &= \min\left(u_{\mathrm{a}},u_{\mathrm{b}},u_{\mathrm{c}}\right) \end{aligned} \tag{4.1}$$

Here, the *max*, *mid*, and *min* functions are used. Accordingly, the phase currents are classified as i_{max}, i_{mid}, and i_{min}, not according to their amplitude, but according to their respective phase voltage classification. Using this classification, the line-to-line voltages can be expressed as shown in Equation 4.2.

$$\begin{aligned} u_{\mathrm{max}} - u_{\mathrm{mid}} &= 2 \cdot t_{\mathrm{max,p}} + t_{\mathrm{max,o}} - 2 \cdot t_{\mathrm{mid,p}} - t_{\mathrm{mid,o}} \\ u_{\mathrm{mid}} - u_{\mathrm{min}} &= 2 \cdot t_{\mathrm{mid,p}} + t_{\mathrm{mid,o}} - 2 \cdot t_{\mathrm{min,p}} - t_{\mathrm{min,o}} \end{aligned} \tag{4.2}$$

Here, $t_{\mathrm{k,x}}$, kϵ{max,mid,min} and xϵ{p,o,n}, refers to the clamping time of phase k to the DC bus x. Furthermore, Equation 4.3 must be satisfied.

$$t_{\mathrm{k,p}} + t_{\mathrm{k,o}} + t_{\mathrm{k,n}} = 1 \tag{4.3}$$

The general PWM model is finally achieved by combining Equations 4.1, 4.2, and 4.3, as shown by Equation 4.4 in matrix form.

$$\begin{pmatrix} 2 & 1 & 0 & -2 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2 & 1 & 0 & -2 & -1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & i_{\max} & 0 & 0 & i_{\mathrm{mid}} & 0 & 0 & i_{\min} & 0 \end{pmatrix} \cdot \begin{pmatrix} t_{\max,\mathrm{p}} \\ t_{\max,\mathrm{o}} \\ t_{\max,\mathrm{n}} \\ t_{\mathrm{mid,p}} \\ t_{\mathrm{mid,o}} \\ t_{\mathrm{mid,n}} \\ t_{\min,\mathrm{p}} \\ t_{\min,\mathrm{o}} \\ t_{\min,\mathrm{n}} \end{pmatrix} = \begin{pmatrix} u_{\max} - u_{\mathrm{mid}} \\ u_{\mathrm{mid}} - u_{\min} \\ 1 \\ 1 \\ 1 \\ i_{\mathrm{np}} \end{pmatrix} \tag{4.4}$$

This system of equations consists of six equations and nine unknowns, so it is not unique. Therefore, additional conditions must be introduced to find a unique solution. These conditions depend on the modulation strategy. For VSVPWM, the following conditions are considered:

- The NP current i_{np} is zero.
- The maximum phase switches between the states p and o: $t_{\max,\mathrm{n}} = 0$.
- The middle phase switches between the states p, o, and n.
- The minimum phase switches between the states o and n: $t_{\min,\mathrm{p}} = 0$.

Given these conditions, Equation 4.4 simplifies to Equation 4.5.

$$\begin{pmatrix} 2 & 1 & -2 & -1 & 0 & 0 & 0 \\ 0 & 0 & 2 & 1 & 0 & -1 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & i_{\max} & 0 & i_{\mathrm{mid}} & 0 & i_{\min} & 0 \end{pmatrix} \cdot \begin{pmatrix} t_{\max,\mathrm{p}} \\ t_{\max,\mathrm{o}} \\ t_{\mathrm{mid,p}} \\ t_{\mathrm{mid,o}} \\ t_{\mathrm{mid,n}} \\ t_{\min,\mathrm{o}} \\ t_{\min,\mathrm{n}} \end{pmatrix} = \begin{pmatrix} u_{\max} - u_{\mathrm{mid}} \\ u_{\mathrm{mid}} - u_{\min} \\ 1 \\ 1 \\ 1 \\ 0 \end{pmatrix} \tag{4.5}$$

Even after simplifying, the system has more unknowns than equations. Therefore, the solution to the last equation of the system, $i_{\max} \cdot t_{\max,\mathrm{o}} + i_{\mathrm{mid}} \cdot t_{\mathrm{mid,o}} + i_{\min} \cdot t_{\min,\mathrm{o}} = 0$, is assumed to be $t_{\max,\mathrm{o}} = t_{\mathrm{mid,o}} = t_{\min,\mathrm{o}}$. Applying this additional restrictive condition yields a unique system of equations for calculating

the duty cycles of VSVPWM, as shown in Equation 4.6.

$$\begin{array}{lll} t_{\mathrm{max,p}} = \frac{u_{\mathrm{max}}-u_{\mathrm{min}}}{2} & t_{\mathrm{max,o}} = 1 - \frac{(u_{\mathrm{max}}-u_{\mathrm{min}})}{2} & t_{\mathrm{max,n}} = 0 \\ t_{\mathrm{mid,p}} = \frac{u_{\mathrm{mid}}-u_{\mathrm{min}}}{2} & t_{\mathrm{mid,o}} = 1 - \frac{(u_{\mathrm{max}}-u_{\mathrm{min}})}{2} & t_{\mathrm{mid,n}} = \frac{u_{\mathrm{max}}-u_{\mathrm{mid}}}{2} \\ t_{\mathrm{min,p}} = 0 & t_{\mathrm{min,o}} = 1 - \frac{(u_{\mathrm{max}}-u_{\mathrm{min}})}{2} & t_{\mathrm{min,n}} = \frac{u_{\mathrm{max}}-u_{\mathrm{min}}}{2} \end{array} \tag{4.6}$$

Calculating the duty cycles this way reduces the computing time compared to the conventional approach. Furthermore, the model analytically links the duty cycles and NP current, promoting an easier understanding of NP balancing. Additionally, the generalized PWM model can be used to derive new modulation strategies under appropriate restrictive conditions.

A CB implementation of VSVPWM can be found using the derived equations, reducing the computing time even further. With two carriers and two modulation waves per phase, Equation 4.7 can be used to calculate the duty cycles for the necessary double modulation waves. [79]

$$\begin{array}{ll} u_{\mathrm{max},1} = t_{\mathrm{max,p}} = \frac{u_{\mathrm{max}}-u_{\mathrm{min}}}{2} & u_{\mathrm{max},2} = 1 \\ u_{\mathrm{mid},1} = 1 - t_{\mathrm{mid,n}} = 1 - \frac{u_{\mathrm{max}}-u_{\mathrm{mid}}}{2} & u_{\mathrm{mid},2} = t_{\mathrm{mid,p}} = \frac{u_{\mathrm{mid}}-u_{\mathrm{min}}}{2} \\ u_{\mathrm{min},1} = 0 & u_{\mathrm{min},2} = t_{\mathrm{min},0} = 1 - \frac{u_{\mathrm{max}}-u_{\mathrm{min}}}{2} \end{array} \tag{4.7}$$

With double modulation waves, the first and third switches use $u_{\mathrm{max},1}$, $u_{\mathrm{mid},1}$, and $u_{\mathrm{min},1}$, while the second and fourth switches use $u_{\mathrm{max},2}$, $u_{\mathrm{mid},2}$, and $u_{\mathrm{min},2}$. This approach ensures that all carriers and modulation waves are between 0 and 1, which is favorable for microcontroller implementation. Additionally, this approach enables switching a phase from p to o to n and back to p within one switching period, which is necessary for the middle phase in VSVPWM.

Another simple implementation comparable to the CB approach can be found by comparing the equations with the existing strategies discontinuous PWM MIN (DPWMMIN) and discontinuous PWM MAX (DPWMMAX) [83, 84]. Both were initially developed for two-level inverters. DPWMMIN clamps the duty cycle to 0 for a 120° interval, and DPWMMAX clamps it to 1 when modulation waves between 0 and 1 are assumed. Using DPWMMIN for $u_{\mathrm{max},1}$, $u_{\mathrm{mid},1}$, and $u_{\mathrm{min},1}$, and DPWMMAX for $u_{\mathrm{max},2}$, $u_{\mathrm{mid},2}$, and $u_{\mathrm{min},2}$, yields the CB implementation of VSVPWM with the double modulation wave approach. The zero-sequence necessary for DPWMMIN and DPWMMAX, which is added to all three phases, is shown in Equation 4.8.

$$\begin{aligned} u_{0,\mathrm{DPWMMIN}} &= -\left(1 + \min\left(u_{\mathrm{a}},u_{\mathrm{b}},u_{\mathrm{c}}\right)\right) = -1 - u_{\mathrm{min}} \\ u_{0,\mathrm{DPWMMAX}} &= 1 - \max\left(u_{\mathrm{a}},u_{\mathrm{b}},u_{\mathrm{c}}\right) = 1 - u_{\mathrm{max}} \end{aligned} \tag{4.8}$$

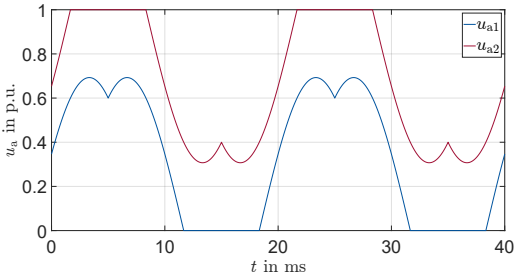


Figure 4.3: Double modulation waves of VSVPWM.

To achieve carrier waves between 0 and 1, the resulting modulation waves must be increased by one and divided by two. Figure 4.3 shows the ideal double modulation waves of VSVPWM for one phase and a modulation index of 0.8. A comparable waveform to regular SVPWM is obtained where $u_{\max}$ switches between p and o, and $u_{\min}$ between o and n, since one of the double modulation waves is clamped to 0 or 1. However, the middle phase has both double modulation waves between 0 and 1, so it switches between p, o, and n.

4.1.2 Active Neutral-Point Control

Although VSVPWM was designed to achieve a balanced DC link at all operating points, the non-ideal switching behavior, different DC link capacitor halves, dead time, and external factors can cause imbalance [42, 85]. Therefore, adding an active NP control to the existing modulation strategy can be beneficial. Otherwise, the SVD becomes distorted, resulting in poor output current quality and potentially destroying the DC link capacitors or IGBTs if the difference is too large.

The NP balance degree α is introduced for the implementation of the active NP control and can be calculated using Equation 4.9.

$$\alpha = \frac{U_{\mathrm{DC,p}} - U_{\mathrm{DC,n}}}{U_{\mathrm{DC,p}} + U_{\mathrm{DC,n}}} \tag{4.9}$$

When $\alpha > 0$, the positive DC voltage is higher, and when $\alpha < 0$, the negative DC voltage is higher. If the NP is perfectly balanced, then α equals zero. To ensure a balanced DC link, the dwell times of the basic vectors must be adjusted

according to Equation 4.10 [86].

$$\begin{aligned} V_{ZS1} &= \frac{k_1}{2} \cdot V_{poo} + \frac{1-k_1}{2} \cdot V_{onn} \\ V_{ZS2} &= \frac{k_2}{2} \cdot V_{oon} + \frac{1-k_2}{2} \cdot V_{ppo} \\ V_{ZM1} &= \frac{k_3}{3} \cdot V_{ppo} + \frac{k_3}{3} \cdot V_{onn} + \frac{k_3}{3} \cdot V_{pon} \end{aligned} \tag{4.10}$$

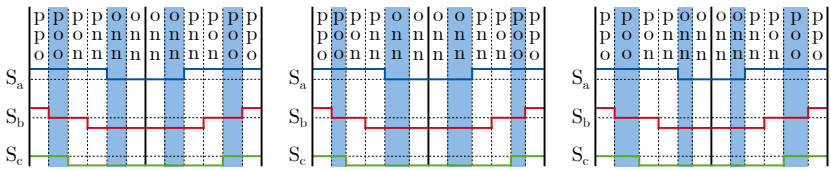
The dwell time adjustment is shown here as an example for the small and medium virtual vectors in sector 1. In principle, large vectors are not modified. The necessary average compensation current can be calculated using Equation 4.11, assuming equal DC link capacitances [86].

$$i_{cmp} = i_{np} = \frac{C_{DC}}{2 \cdot T_{sw}} \cdot U_{DC} \cdot \alpha \tag{4.11}$$

Extending Equation 4.10 with the NP current of the corresponding basic vectors yields the NP current of the virtual vectors. Combining this with Equation 4.11 provides a solution for k_1, k_2, and k_3, as shown in Equation 4.12 [86].

$$\begin{aligned} k_1 &= \frac{1}{2} - \frac{C_{DC}}{2 \cdot t_{VZS1} \cdot i_a} \cdot U_{DC} \cdot \alpha \\ k_2 &= \frac{1}{2} - \frac{C_{DC}}{2 \cdot t_{VZS2} \cdot i_c} \cdot U_{DC} \cdot \alpha \\ k_3 &= 1 - \frac{C_{DC}}{2 \cdot t_{VZM1} \cdot i_b} \cdot U_{DC} \cdot \alpha \end{aligned} \tag{4.12}$$

Here, t_{VZS1}, t_{VZS2}, and t_{VZM1} represent the dwell times of the respective virtual vectors. If multiple virtual vectors are available for NP compensation, the one that can induce the highest compensation current within a switching period must be selected [86]. Figure 4.4 illustrates the effect of active NP control on the dwell times. Figure 4.4 (a) assumes a perfectly balanced DC link. When



(a) $\alpha = 0$ (b) $\alpha > 0$ (c) $\alpha < 0$

Figure 4.4: Vector sequence with adjusted dwell times from active NP control.

there is an imbalance, the dwell times of the switching states *poo* and *onn* are adjusted, as depicted in Figures 4.4 (b) and (c) for $\alpha > 0$ and $\alpha < 0$, respectively.

4.2 Hybrid-Discontinuous Sinusoidal Pulse Width Modulation

Although Chapter 3 has shown that CMV has a significant impact on CM currents, the modulation strategies introduced so far did not consider CMV. Furthermore, the space vector-based modulation strategies, SVPWM and VSVPWM, are expected to produce high CMV because the zero-sequence injection leads to low-order harmonics in the CMV spectrum. Therefore, a novel modulation strategy is developed to reduce the CMV output of an inverter.

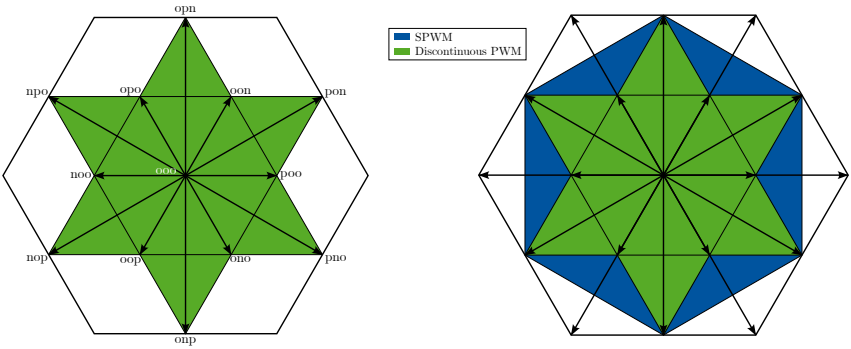
A new modulation strategy is found using the previously introduced general PWM model of NP clamped converters. First, the restrictive conditions must be defined to find a unique solution to Equation 4.4. One simple method of limiting the CMV to $\pm 1/6$ is to clamp the middle phase to the *o* state. This can be determined by analyzing the switching states in the SVD in Figure 2.10. In conclusion, the restrictive conditions are:

- The maximum phase switches between *p* and *o*.
- The minimum phase switches between *o* and *n*.
- The middle phase is clamped to *o*.

The maximum phase switching between *p* and *o*, and the minimum phase switching between *o* and *n*, ensures a good output current quality and reduces switching losses, as is the case with SPWM, SVPWM, and VSVPWM. The conditions show that $t_{\mathrm{mid,p}} = t_{\mathrm{mid,n}} = 0$ and $t_{\mathrm{mid,o}} = 1$, which simplifies Equation 4.4 to Equation 4.13.

$$\begin{pmatrix} 2 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & i_{\max} & i_{\min} & 0 \end{pmatrix} \cdot \begin{pmatrix} t_{\mathrm{max,p}} \\ t_{\mathrm{max,o}} \\ t_{\mathrm{min,o}} \\ t_{\mathrm{min,n}} \end{pmatrix} = \begin{pmatrix} u_{\max} - u_{\mathrm{mid}} \\ u_{\mathrm{mid}} - u_{\min} \\ 1 \\ 1 \\ i_{\mathrm{np}} \end{pmatrix} \tag{4.13}$$

This system of equations is solvable because the number of unknowns is equal to or less than the number of equations. Therefore, no additional restrictive condi-



(a) Discontinuous PWM (b) HDSPWM

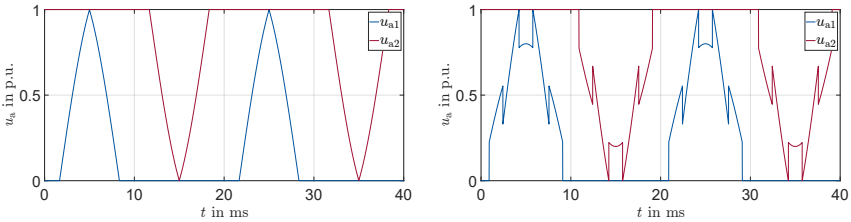
Figure 4.5: SVD of HDSPWM.

tions are necessary. Rearranging Equation 4.13 yields the duty cycle calculations shown in Equation 4.14.

$$\begin{array}{lll} t_{\mathrm{max,p}} = \frac{u_{\mathrm{max}} - u_{\mathrm{mid}}}{2} & t_{\mathrm{max,o}} = 1 - \frac{(u_{\mathrm{max}} - u_{\mathrm{mid}})}{2} & t_{\mathrm{max,n}} = 0 \\ t_{\mathrm{mid,p}} = 0 & t_{\mathrm{mid,o}} = 1 & t_{\mathrm{mid,n}} = 0 \\ t_{\mathrm{min,p}} = 0 & t_{\mathrm{min,o}} = 1 - \frac{(u_{\mathrm{mid}} - u_{\mathrm{min}})}{2} & t_{\mathrm{min,n}} = \frac{u_{\mathrm{mid}} - u_{\mathrm{min}}}{2} \end{array} \tag{4.14}$$

However, these discontinuous PWM conditions restrict the choice of basic vectors, thus limiting the operating area, as seen in Figure 4.5 (a). To extend the operating area to a sufficient range for the given application, the discontinuous PWM is combined with regular SPWM. The discontinuous modulation is used up to the applicable modulation index of 0.66; otherwise, SPWM is used in the remaining area, as shown in Figure 4.5 (b). The restrictive conditions for SPWM are similar, but instead of clamping the middle phase, they switch between p and o for positive middle phase voltages and between o and n for negative middle phase voltages. Since this modulation strategy uses both a discontinuous PWM pattern and SPWM, it is called HDSPWM. An automatic detection of the applicable modulation is possible in the implementation by calculating the current subsector of the reference vector, similar to SVPWM and VSVPWM.

Figure 4.6 shows the resulting double modulation waves for HDSPWM. As expected, the shape of the modulation waves depends on the modulation index. For a modulation index of less than 0.67, corresponding to the length of the small vectors, the modulation waves appear nearly triangular, with clear discontinuous behavior, as shown in Figure 4.6 (a). For higher modulation indices, the



(a) $m_i = 0.666$ (b) $m_i = 0.8$

Figure 4.6: Double modulation waves of HDSPWM.

transition from discontinuous modulation to SPWM is evident in the signal's jumps, as illustrated in Figure 4.6 (b) for a modulation index m_i of 0.8. Clamping the middle phase in certain areas reduces switching actions compared to SPWM, SVPWM, and VSVPWM. However, it is unclear whether the converter efficiency can be increased, as the conduction losses can also differ between the modulators.

As was previously introduced for VSVPWM, an active NP control is implemented for HDSPWM. The concept of adjusting the dwell times of specific vectors based on the DC link imbalance is similar. The compensation time t_{cmp} can be calculated using Equation 4.15.

$$t_{cmp} = m_i \cdot \alpha \cdot k_{cmp} \tag{4.15}$$

Here, the NP balance degree α, introduced in Equation 4.9, is used. Additionally, t_{cmp} depends on the modulation index m_i and a compensation factor k_{cmp}, which can be used to adjust the speed of the compensation control. During the duty cycle calculation, the compensation time is added to all values that are neither 0 nor 1 in order to control the DC link balance. For the active NP control in this thesis, k_{cmp} is set to 1.

In some applications, a higher DC link utilization than SPWM allows is beneficial. SPWM has a linear modulation range of 1 whereas SVPWM increases the linearity to 1.15, as can be seen by drawing a circle with edges on the hexagon spanned by the outermost vectors in the SVD, as shown in Figure 4.7. Additionally, the linear modulation range of SVPWM is limited by the length of the medium vectors, whereas the range of SPWM is limited by three-quarters of the length of the large vectors. The same applies to VSVPWM, which exhibits the same linearity as SVPWM. Since SPWM is used to increase the linearity

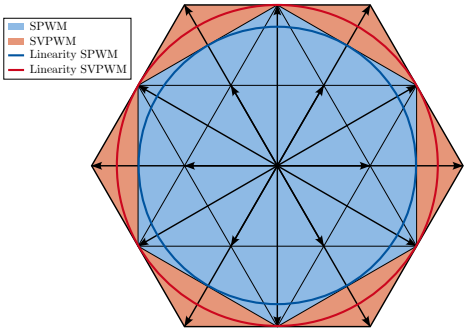


Figure 4.7: Linear modulation range of SPWM and SVPWM.

of HDSPWM, it has the same limit of $m_\mathrm{i} = 1$. HDSPWM can also be combined with SVPWM to increase the linear modulation range, resulting in hybrid-discontinuous space vector pulse width modulation (HDSVPWM). However, it is not necessary for the given application, so HDSVPWM was not implemented.

4.3 Carrier-Based Reduced Common-Mode Voltage Modulation

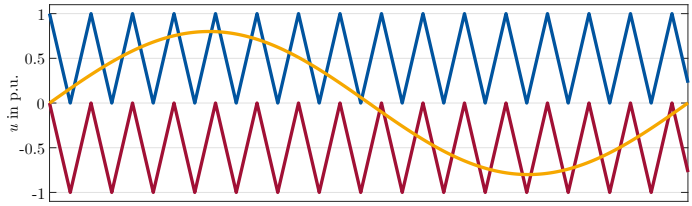
Other measures are necessary to reduce the CMV because HDSPWM only limits it to $\pm 1/6$ at specific operating points. Several methods modify SVPWM and VSVPWM so that they only use basic vectors with low CMV [86–91]. These methods utilize low CMV switching states through modified space vector selection, albeit in slightly different ways. However, they all present challenges that complicate implementation or degrade converter performance. Some methods switch a phase directly from p to n or vice versa, while others rely on the simultaneous switching of multiple phases [87, 89, 91]. This leads to strict timing constraints and worsens the quality of the output current. Another challenge is an increase in switching actions per switching period, even compared to VSVPWM, which increases switching losses and semiconductor stress [86, 88, 91]. One strategy does not rely on simultaneous switching, state changes from p to n, or increased switching actions [90]. Further implementations of reduced CMV modulation use a three-dimensional virtual space vector approach, which increases the modulator's complexity and is usually only applied to four-wire systems with an additional converter leg [92, 93]. Discontinuous PWM meth-

ods that clamp one of the phases to the NP, comparable to HDSPWM, have also been introduced to reduce CMV [94, 95]. However, they are quite complex to implement because they constantly switch between different discontinuous PWM modes to maintain a balanced NP and reduce CMV, which also depends on the power factor.

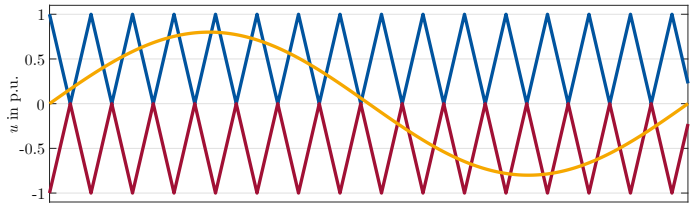
Methods that rely on modified carriers can overcome many of these challenges. They ensure smooth transitions between switching states, limit the number of switching actions per switching cycle, and require minimal computational effort. They can also be combined with different modulation strategies, such as SPWM or CB implementations of SVPWM and VSVPWM. The following section introduces and analyzes two CB methods to reduce the CMV of three-level inverters.

4.3.1 Phase Opposition Disposition

In addition to PD carriers that have already been introduced, it is possible to shift the phase of the bottom carriers by 180° compared to the top carriers, which results in POD [54, 96–98]. Figure 4.8 (a) shows the PD carriers, and



(a) PD



(b) POD

Figure 4.8: Carrier signals with PD and POD.

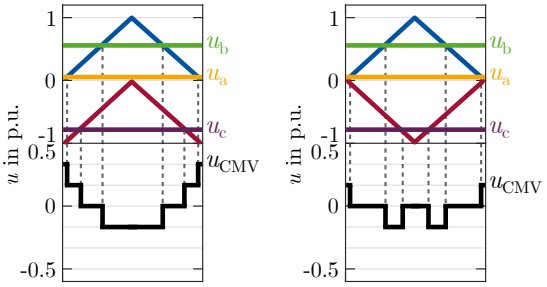


Figure 4.9: Exemplary CMV with PD and POD PWM.

Figure 4.8 (b) shows the POD carriers. Directly comparing the DM output performance shows that PD produces fewer distortions than POD [99]. However, POD's CM output is less than PD's because POD limits the CMV to $\pm 1/6$. Although this method had been known for some time, the reduction of CMV was analyzed and utilized later [99].

To demonstrate the CMV reduction of POD, all three phases must be considered. Generally, the crossing of a modulation wave with a carrier on the rising edge decreases CMV by $1/6$, whereas crossing on a falling edge increases CMV by $1/6$. This is because the phase switches to a higher or lower potential at each carrier crossing, as shown in Figure 4.9. In PD PWM, both carriers are on the rising or falling edge simultaneously, and each phase has one carrier crossing per half switching period. This results in three positive and three negative CMV steps per switching period, as illustrated in Figure 4.9 (a). Therefore, the CMV varies between $-1/6$ and $1/3$ for a positive middle phase voltage u_{mid} and between $-1/3$ and $1/6$ for a negative u_{mid}. However, in POD PWM, one carrier is always on the rising edge, while the other carrier of the phase is on the falling edge. Depending on the polarity of u_{mid}, this results in two positive CMV steps and one negative step in the first half of the switching period and in reverse in the second half, or vice versa for an opposite polarity of u_{mid}. Ultimately, this limits the CMV to $\pm 1/6$, as shown in Figure 4.9 (b). [99]

Here, POD was only shown in combination with SPWM. However, the same CMV reduction can be achieved using SVPWM, VSVPWM, or HDSPWM modulation waves.

4.3.2 Middle Phase Opposition Disposition

A similar CMV limitation to $\pm 1/6$ can be achieved using other carrier disposition methods. If the two carriers of one of the three phases are opposed, a CMV reduction similar to the POD method can be achieved. This approach leads to one carrier with opposing rising and falling edges, resulting in two positive steps and one negative step, or two negative steps and one positive step, depending on the voltage polarity of the opposed phase. However, the timings would be different from those of POD PWM, resulting in a different CMV profile. Furthermore, since one phase switches differently, the DM output of this phase is worse compared to the other phases.

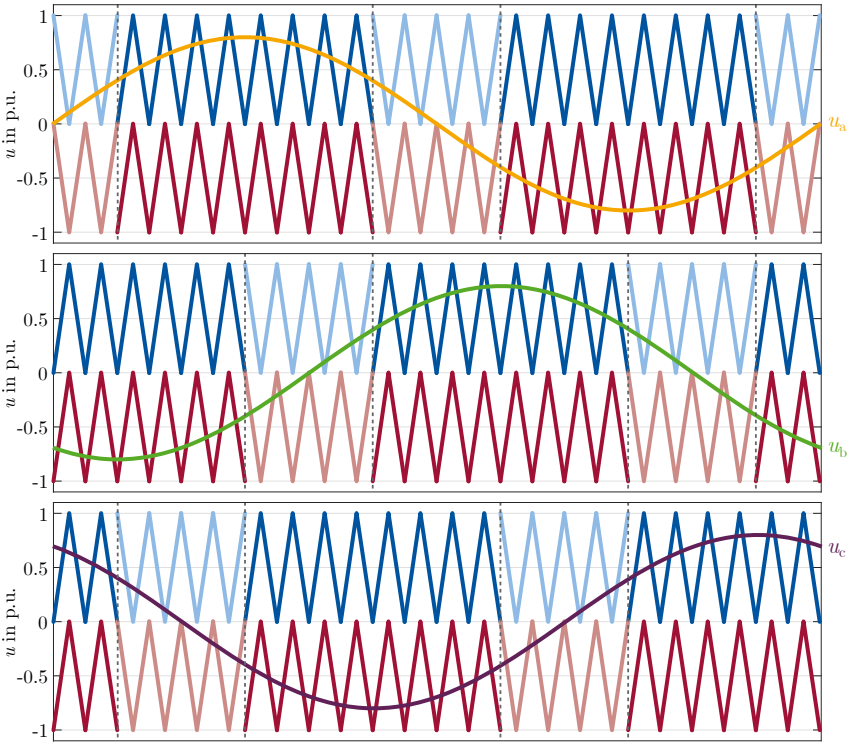


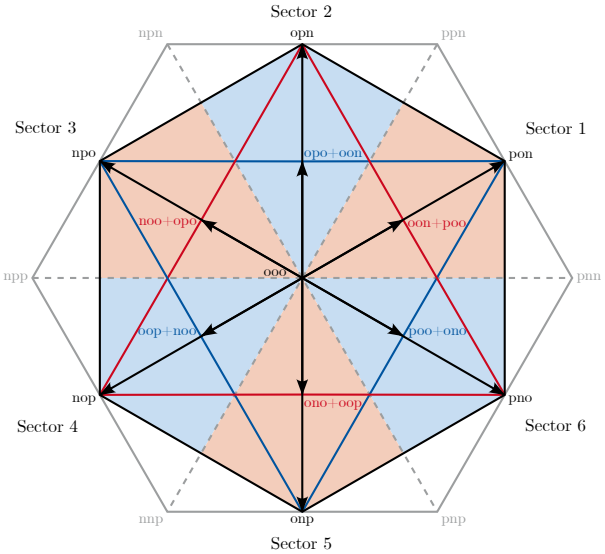
Figure 4.10: Carrier signals of all three phases with MPOD.

Therefore, it is proposed that the opposing carriers are changed so that each phase is opposed for an equal duration. In principle, the opposition can be linked to the phase voltage position being maximum, middle, or minimum. However, for an opposition in maximum or minimum phase voltage, the additional stress would not be distributed equally between the switching devices, resulting in unsymmetrical output currents. Thus, the middle phase is opposed, resulting in the novel MPOD modulation depicted in Figure 4.10. As can be seen, this leads to six changes of the opposed phase per fundamental cycle, as indicated by the light colors.

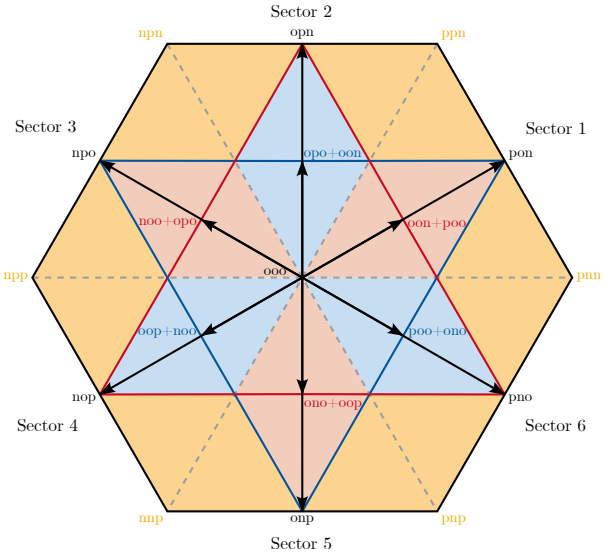
The idea of opposing only the carriers of the middle phase was briefly mentioned in literature as displaced-pattern modulation [100]. However, neither this paper nor the referenced paper investigates MPOD or displaced-pattern modulation in detail [100, 101].

A more detailed understanding of the switching sequences using MPOD can be achieved through analysis of the SVDs. Figure 4.11 (a) shows the SVD of MPOD combined with SPWM. Similar to VSVPWM, small vectors are combined to form new virtual vectors, which avoids small vectors with a CMV of $\pm 1/3\ U_{\mathrm{DC}}$. In each sector, either two medium vectors or one medium vector and the zero vector, along with the corresponding small vector, are activated. Which medium vectors are used depends on the current location of the reference vector in the SVD. For example, if the reference vector is located in the outer part of the right half in sector 1, *pon* and *pno* are used. However, if the reference vector is located in the left half, *pon* and *opn* are used. The red line to the medium vectors in the adjacent sectors indicates which medium vector is used. When the reference vector is in the inner part and the zero vector is used, the medium vector in the adjacent sector is always activated instead of the one in the corresponding sector. Large vectors are generally not used with MPOD and SPWM, even though they would also limit the CMV to $\pm 1/6\ U_{\mathrm{DC}}$.

Combining MPOD with SVPWM yields a slightly different SVD because it utilizes the large vectors, as shown in Figure 4.11 (b). As can be seen in the orange sections, the large vectors are used for higher modulation indices. In this case, two medium vectors, one large vector, and one of the two small basic vectors are used. The closest medium vectors and large vector are used; however, the small vector that is farther away from the reference vector is used. For instance, in the orange area on the right side of sector 1, the vectors *pnn*, *pon*, *pno*, and *oon* are used; *oon* is farther away from the subsector than *poo*. Conversely, in the orange area on the left side of sector 1, the vectors *ppn*, *pon*, *opn*, and *poo* are used, even though *oon* is closer. In general, the same vector sequences as with SPWM are activated in the blue and red areas.



(a) SPWM



(b) SVPWM

Figure 4.11: SVD of MPOD with SPWM and SVPWM.

Overall, the analysis suggests that the THD increases compared to PD, because vectors that are not the closest to the reference vector are used, as shown for both SPWM and SVPWM. Additionally, losses are expected to increase for the same reason, which could reduce efficiency.

To implement MPOD, the middle phase must be determined from the three phase voltages. One simple method is to use the phase angle θ, which can be calculated using Equation 4.16 in the α-β frame.

$$\theta = \operatorname{atan}\left(\frac{u_\beta}{u_\alpha}\right) \tag{4.16}$$

Using θ, the current location in the SVD is determined, which in turn determines the middle phase. However, it is not possible to apply a phase shift to the carrier of the first PWM unit with some microcontrollers, as this unit is used to synchronize all PWM units [102]. In this case, the first phase can be set to regular PD PWM. If the phase to which the first PWM unit is connected to is the middle phase, shifting the other two phases instead leads to the same result as shifting only the phase with the first PWM unit.

With MPOD, a CB implementation of the reduced CMV VSVPWM in [90] can be found. Shifting the middle phase of VSVPWM essentially yields the same vector combinations described in the paper where the CMV is limited to $\pm 1/6$. Thus, using the previously mentioned method of applying DPWMMIN and DPWMMAX for a CB implementation of VSVPWM in combination with MPOD yields a simple CB implementation of reduced CMV VSVPWM.

4.4 Evaluation of Modulation Strategies

Four modulation wave strategies, SPWM, SVPWM, VSVPWM and HDSPWM, and three carrier configurations, PD, POD and MPOD, have been introduced. Combining these yields 12 different modulation strategies that can be compared. SPWM and SVPWM are implemented as CB strategies, whereas VSVPWM and HDSPWM use the space vector approach with dwell time calculation. However, the general PWM model calculates the necessary duty cycles from the dwell times, allowing them to be tested with all carrier configurations. The modulators are implemented on a TI LaunchXL F28379D with double modulation waves [103].

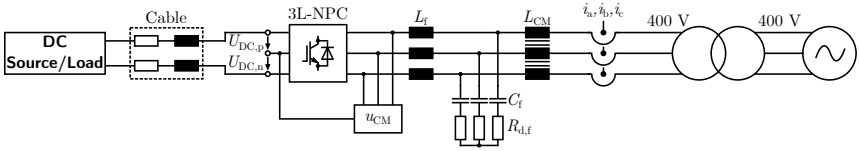


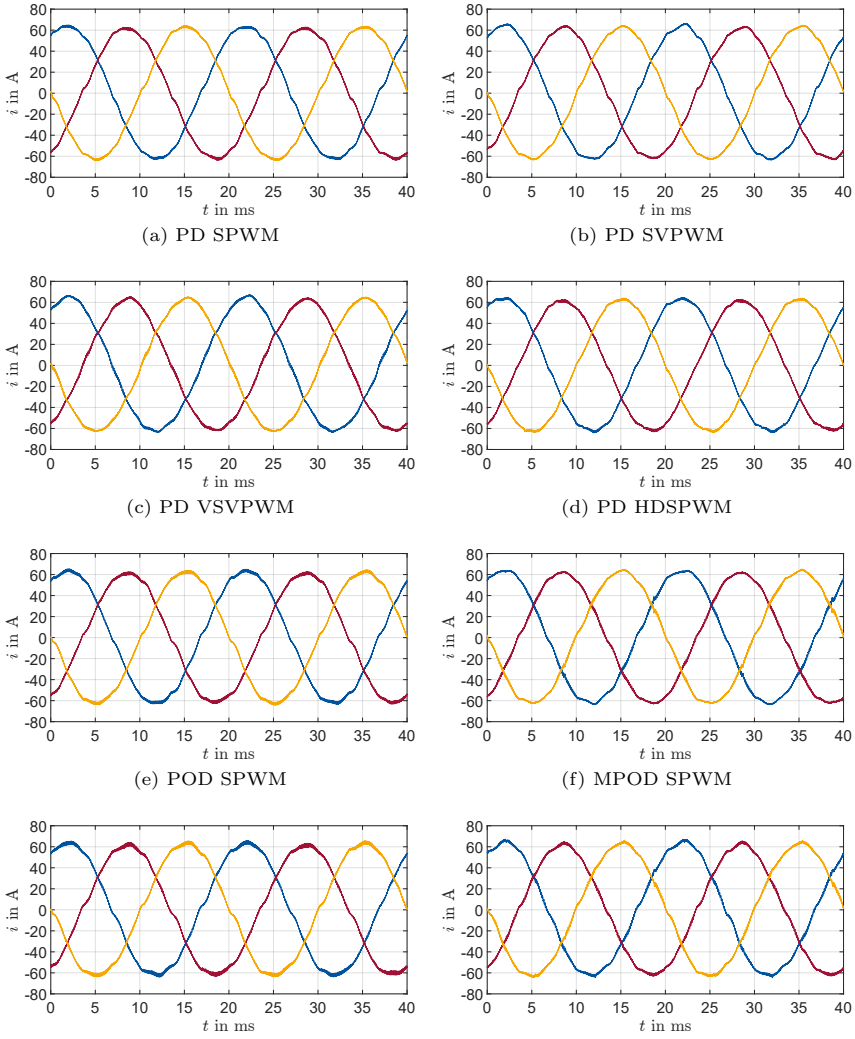
Figure 4.12: Measurement setup for the evaluation of different modulation strategies.

Figure 4.12 shows the measurement setup for evaluating the modulators. Three identical Hall-based current probes are used to measure the AC phase currents. The DC link voltages are measured using differential probes, and the CMV is measured with the PCB introduced in Section 3.5, in combination with a differential probe. A bidirectional source/load with a maximum power of 30 kW is used for DC side loading, and the AC grid side of the isolation transformer is connected to the public LV AC distribution grid.

4.4.1 Output Currents

First, the quality of the output currents produced by the 3L-NPC with different modulation strategies is compared at a power of 30 kW. Figure 4.13 shows selected measurements in rectifying operation. As can be seen, all modulators produce a good sine wave, with only minor differences between them. Additionally, the complete measurements for other combinations, as well as for inverting operation, are shown in Appendix A.2. These measurements are used to calculate the THD for all combinations, which are listed in Table 4.1. For these calculations, a period of 100 ms was used instead of the 40 ms shown in the measurement plots. Additionally, the THD was calculated for all three phases, and the average of the three values is presented.

As seen in Table 4.1, PD produces less THD than the reduced CMV modulation waves in all cases. As previously discussed, this is expected when analyzing the SVD with MPOD because it uses switching states that are farther away from the reference vector. The novel MPOD performs slightly worse than POD for SPWM and HDSPWM. Conversely, MPOD performs better than or similar to POD for SVPWM and VSVPWM. Furthermore, the THD is better in rectifier mode than inverter mode, mostly due to the difference in DC voltages produced by droop control, which exceeds 60 V between the two operating points. HDSPWM generally has the best current output quality, with a THD of only 2.25 % for PD,



(a) PD SPWM (b) PD SVPWM

(c) PD VSVPWM (d) PD HDSPWM

(e) POD SPWM (f) MPOD SPWM

(g) POD SVPWM (h) MPOD SVPWM

Figure 4.13: Output currents with different modulators and a 30 kW load.

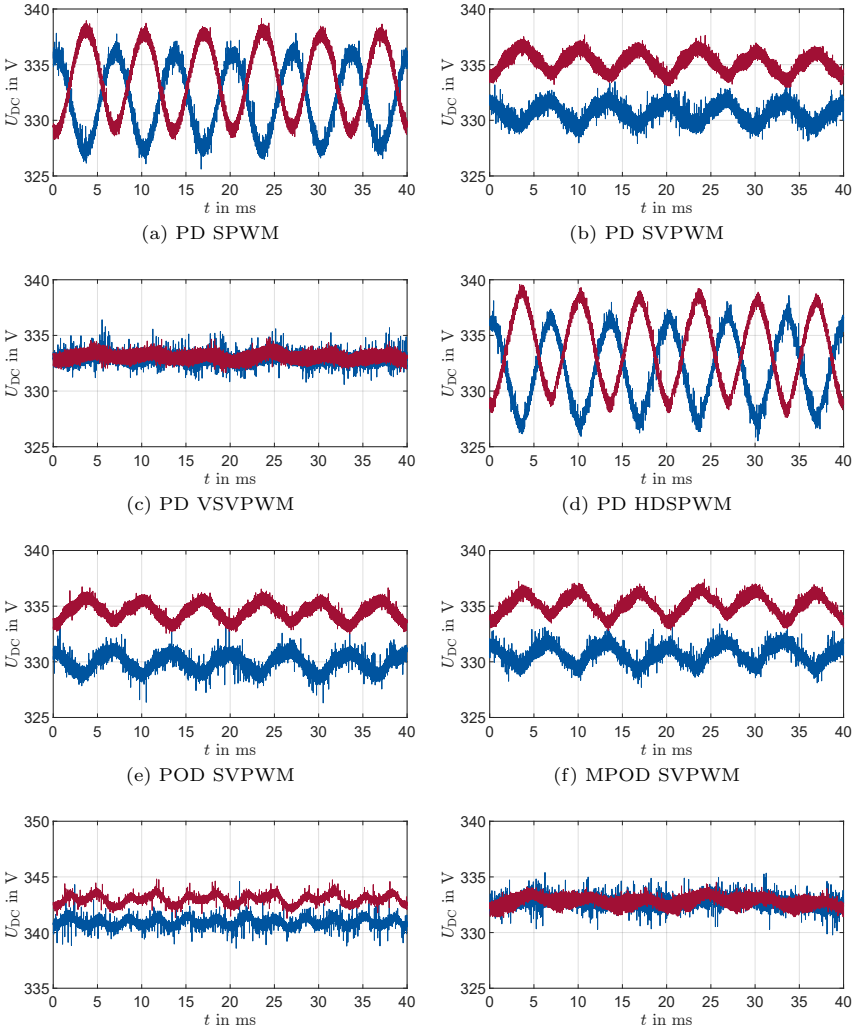
Table 4.1: THD of all modulators in inverting and rectifying operation

		SPWM	SVPWM	VSVPWM	HDSPWM
Inverter	PD	2.90 %	3.19 %	4.02 %	2.67 %
	POD	3.17 %	4.14 %	39.39 %	3.18 %
	MPOD	3.27 %	3.61 %	5.12 %	3.30 %
Rectifier	PD	2.61 %	2.55 %	2.86 %	2.25 %
	POD	3.09 %	3.51 %	21.25 %	2.58 %
	MPOD	3.25 %	3.53 %	4.00 %	2.96 %

while VSVPWM performs the worst. Combining VSVPWM with POD results in very poor current output behavior, with an unacceptably high THD of up to 39.39 % at 13 kW. Thus, the measurements are not performed at a higher power to avoid damaging any components. Overall, the THD is mostly much less than 5 %, which is for example required by the IEEE 1547 and IEC 61727 standards, even though the nominal power of 50 kW was not reached [104, 105].

4.4.2 DC Link Voltage Balancing

The following examines the DC link voltage behavior of the different modulation strategies. Selected measurements are shown in Figure 4.14, and the rest can be found in Appendix A.2. As can be seen, SPWM and HDSPWM produce similar patterns for the DC link halves, both exhibiting a significant 150 Hz component of nearly 10 V peak-to-peak. The 150 Hz ripple is reduced to less than 5 V peak-to-peak with SVPWM, and it completely vanishes with VSVPWM, as expected. Additionally, the 150 Hz component is load-dependent; it is larger for higher loads and smaller for lower loads. This is not visible in the measurements shown here. Furthermore, all modulators exhibit a slight DC offset except for VSVPWM, which uses active NP control to eliminate it. HDSPWM also has an NP controller but shows a similar offset to SPWM and SVPWM, which could be reduced by adjusting the NP control parameters. However, the DC offset is slightly smaller with HDSPWM than with SPWM and SVPWM, suggesting that the implemented active NP control is working, but parameter tuning is necessary. In general, the DC link balancing exhibits similar behavior during inverter operation, albeit with a slightly increased DC offset.



(a) PD SPWM (b) PD SVPWM

(c) PD VSVPWM (d) PD HDSPWM

(e) POD SVPWM (f) MPOD SVPWM

(g) POD VSVPWM (h) MPOD VSVPWM

Figure 4.14: DC link voltages with different modulators and a 30 kW load.

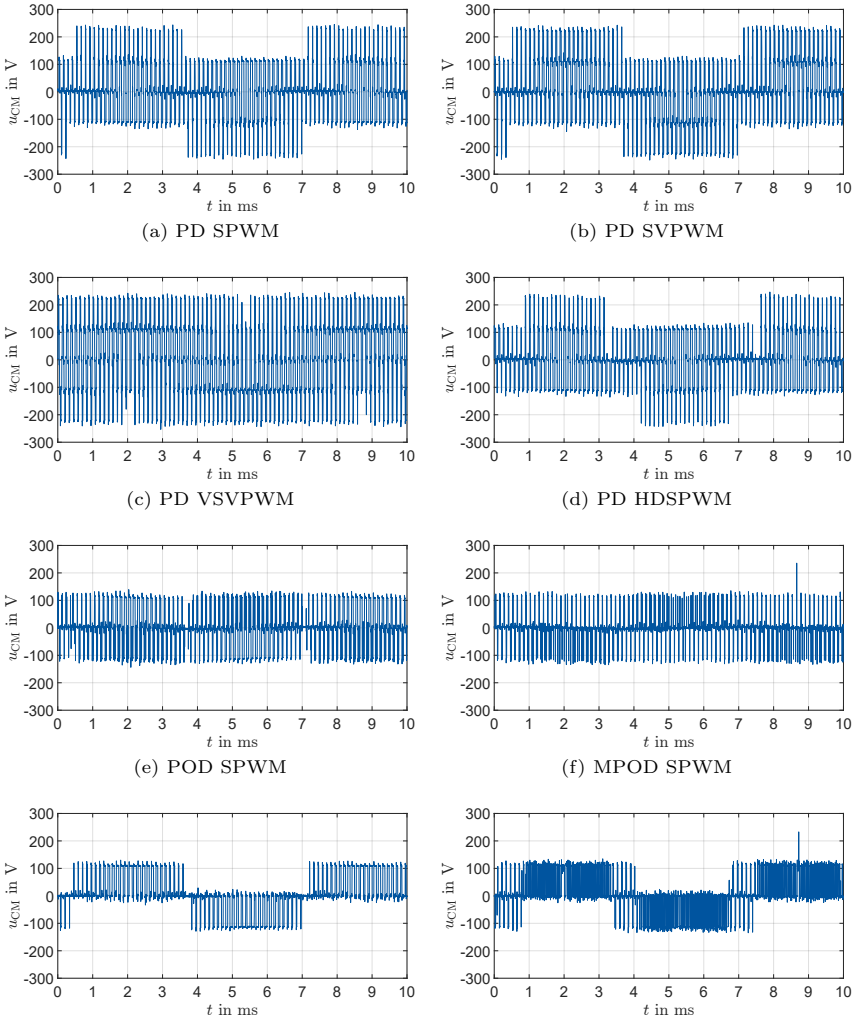
No major differences in the NP balancing are visible when comparing PD with the two reduced CMV carriers. Only POD VSVPWM exhibits slightly different behavior, as it was already an outlier in the output current comparison. The poor current output behavior is presumably responsible for the change in VSVPWM's DC link balancing behavior, as this additional ripple is not visible in no-load measurements. However, the DC offset is present even in no-load measurements, but only when using POD VSVPWM, which could indicate a different problem with this combination. Therefore, using POD with VSVPWM is not recommended; MPOD should instead be used for reduced CMV. Nevertheless, the combination of VSVPWM and POD was still considered for further CM current measurements in Chapter 5.

4.4.3 Common-Mode Voltage

Now, the CMV of different modulators is analyzed. This analysis is relevant because the CMV produced by the converter significantly influences the CM currents. Figure 4.15 shows a selection of CMV patterns produced by different modulators. The remaining measurements can be found in Appendix A.2. Focusing first on the modulators using PD in Figures 4.15 (a) to (d), it is evident that SPWM, SVPWM, and HDSPWM switch between four CMV levels in one switching period, whereas VSVPWM switches between all five. Furthermore, HDSPWM shows areas where it switches between only three levels, which limits the CMV to $\pm 1/6$. Additionally, no major differences are visible between rectifier and inverter modes except when using HDSPWM. In this case, the areas with reduced CMV shrink as the DC voltage increases. This can be explained by the simultaneous increase in AC terminal voltage, caused by the voltage drop across

Table 4.2: RMS value of CMV for all modulators in inverting and rectifying operation

		SPWM	SVPWM	VSVPWM	HDSPWM
Inverter	PD	110.5 V	132.1 V	171.8 V	108.4 V
	POD	83.1 V	70.9 V	65.2 V	84.6 V
	MPOD	58.5 V	76.9 V	84.2 V	59.3 V
Rectifier	PD	98.5 V	117.8 V	150.3 V	94.5 V
	POD	76.8 V	67.0 V	66.3 V	78.3 V
	MPOD	43.2 V	70.0 V	81.2 V	46.2 V



(a) PD SPWM (b) PD SVPWM

(c) PD VSVPWM (d) PD HDSPWM

(e) POD SPWM (f) MPOD SPWM

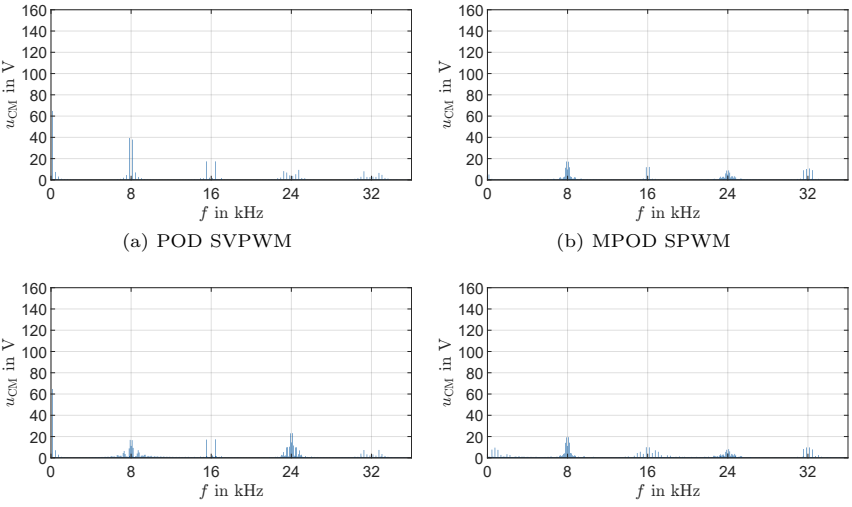
(g) POD SVPWM (h) MPOD SVPWM

Figure 4.15: CMV with different modulators.

the passive components on the AC side, as well as by the power flow direction, both of which increase the necessary modulation index. Thus, the time in the discontinuous PWM mode is reduced.

When analyzing the reduced CMV modulation with POD and MPOD, the limitation of CMV to $\pm 1/6$ becomes apparent. Specifically, combining SVPWM and VSVPWM yields a significantly different CMV waveform, as both switch between only two levels for each sixth of the switching period.

Next, the RMS values of the CMVs with all modulators are calculated and presented in Table 4.2. A period of 100 ms is again considered for calculating these values. It is evident that the modulators using PD have the highest CMV. In some cases, the RMS value of VSVPWM exceeds the other modulation strategies by more than 50 %. Conversely, HDSPWM has the lowest CMV when using PD, reducing the RMS value by 4.1 % compared to SPWM in rectifier mode. Furthermore, POD significantly reduces the RMS values for SVPWM and VSVPWM, which are both lower than SPWM and HDSPWM when combined with POD. However, combining POD and VSVPWM yields poor output current behavior and should be avoided. Additionally, the measurements with



(a) POD SVPWM (b) MPOD SPWM

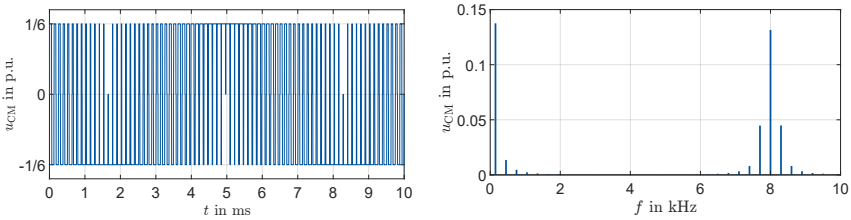
(c) MPOD SVPWM (d) MPOD HDSPWM

Figure 4.16: CMV spectrum with different modulators up to 36 kHz.

POD and VSVPWM were performed at a lower load, leading to a different DC voltage and less comparable results. Overall, combining MPOD with SPWM and HDSPWM yields the lowest CMVs, with reductions of up to 56 % compared to PD. MPOD also significantly reduces the RMS values of SVPWM and VSVPWM, but POD yields lower RMS values for these two modulators.

Nevertheless, the frequency spectrum of the CMV is also important, not only the RMS value. Figure 4.16 shows the frequency spectra of selected CMV measurements which were obtained by applying a fast Fourier transform (FFT) to the signals. The remaining frequency spectra can be found in Appendix A.2. As can be seen, all modulation strategies exhibit significant amplitudes at the switching frequency f_{sw} of 8 kHz and its multiples. Furthermore, SVPWM shows a significant 150 Hz component with PD, POD, and MPOD. This can be seen in Figures 4.16 (a) and (c) for POD and MPOD, respectively. The same applies to VSVPWM, which can be explained by the zero-sequence injection present in both modulators, which has a frequency that is three times the fundamental frequency. HDSPWM shows low-frequency components and increased sideband components compared to the other modulation strategies. This is caused by switching between two modulation strategies during operation.

Analyzing only the discrete PWM mode of HDSPWM, which is active for only a short duration at the investigated operating points, reveals a different CMV waveform than SPWM. Figure 4.17 shows the simulated CMV of HDSPWM with PD and a modulation index of 0.666, which is the maximum for the discrete PWM mode. As expected, the CMV stays between $\pm 1/6$ here. However, significant 150 Hz components and their uneven multiples are present, as can be seen in Figure 4.17 (b). The low-frequency components of the discrete PWM are higher than those of SVPWM and VSVPWM. However, these frequency



(a) Time domain (b) Frequency domain

Figure 4.17: Simulated CMV in time and frequency domain with HDSPWM and $m_{\mathrm{i}} = 0.666$.

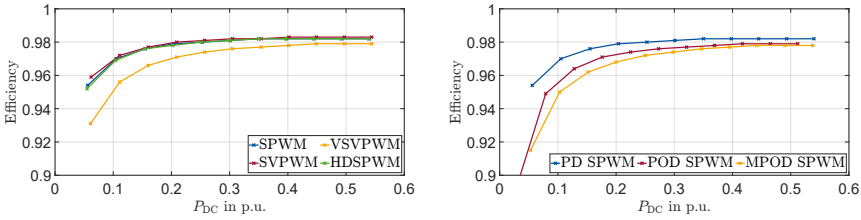
components are only partially transferred to the hybrid PWM CMV waveform because the discrete mode is only active for a short time. Nevertheless, these frequency components, as well as the switching between the two PWM modes, are responsible for the increased low-frequency and sideband components compared to SPWM.

Furthermore, Figure 4.16 shows that POD significantly reduces the amplitude at f_{sw}, but increases the sideband components. Specifically, the reduction is very significant for SVPWM and VSVPWM. MPOD further reduces the switching frequency component for all modulators, but also increases the sideband components. However, the sideband components are more widespread, with much lower amplitudes, compared to POD. Additionally, the amplitude at $3 \cdot f_{\mathrm{sw}}$ increases with MPOD for SVPWM and VSVPWM, but not with SPWM or HDSPWM. Higher frequencies above 40 kHz only exhibit significant amplitudes at multiples of the switching frequency, with decreasing amplitude; thus, they are not shown here.

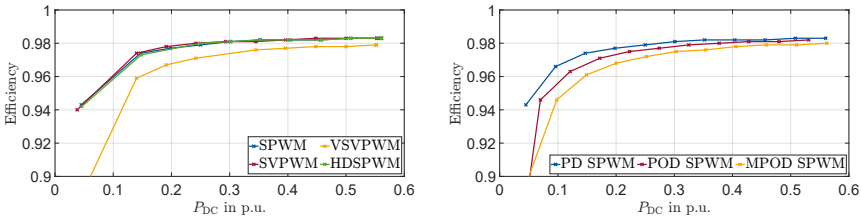
4.4.4 Efficiency

Finally, the efficiency of the converter system using different modulation strategies is compared. Voltage droop control was turned off; therefore, all measurements were performed at 700 V, and current control was used to set various power levels for generating power-dependent efficiency curves. The efficiency was determined using a Matuschek LK601 multi-channel power analyzer in conjunction with Danisense DS600ID current transducers [106, 107]. The efficiency is plotted against the DC side power P_{DC} for both rectifier and inverter operation. The AC side currents and voltages are measured between the transformer and the CM filters, including the CM and DM filter losses.

Figures 4.18 (a) and (b) show the efficiency of SPWM, SVPWM, VSVPWM, and HDSPWM with PD for rectifying and inverting operations, respectively. All modulators show similar efficiency, reaching a maximum of 98.2 %, except for VSVPWM, which is lower due to the additional switching actions of the middle phase. The difference between VSVPWM and the other modulation strategies is therefore larger, especially at partial loads, where switching losses dominate and additional switching actions cause higher losses. Increasing the load reduces the proportion of switching losses, so the maximum efficiency is only about 0.2 % lower. Furthermore, slight differences are visible between the rectifier and inverter operations.



(a) Rectifier



(b) Inverter

Figure 4.18: Efficiency measurements with different modulators.

Next, the efficiency of the different carrier configurations, PD, POD, and MPOD, are shown on the right side of Figure 4.18. PD has the highest efficiency over the entire operating range. Additionally, POD is slightly more efficient than MPOD. This validates the previous considerations obtained from analyzing the SVD with MPOD. Those considerations suggested that increased switching losses would result from using switching states that are farther away from the reference vector. Again, the differences between the modulators decrease at higher loads. However, neither POD nor MPOD reach 98 % efficiency in rectifying operation.

Combining POD and MPOD with SVPWM and HDSPWM yields similar results to SPWM because their efficiencies are very similar with PD. However, the efficiency would be slightly lower with VSVPWM, especially at low loads. As the load increases beyond 30 kW, the curves are expected to remain at a similar level as at loads above 50 % because most measurements already show constant efficiency at this point.

4.5 Summary

This chapter first introduces the existing VSVPWM, which balances the DC link voltages regardless of the modulation index or power factor. Although it was developed more recently than SPWM and SVPWM, a significant amount of research has already been conducted on the modulator. The generalized PWM model for three-level inverters is presented with VSVPWM as an example. This model enables the calculation of duty cycles from dwell times and allows for the use of carriers in combination with a space vector algorithm. Additionally, the model is used to derive an active NP controller for VSVPWM that removes DC offsets resulting from non-ideal converter behavior.

Furthermore, the generalized PWM model is used to derive the novel hybrid modulation strategy, HDSPWM. HDSPWM reduces CMV by clamping the middle phase to the NP, resulting in discontinuous PWM. However, this restricts the linear modulation region. Thus, the discontinuous PWM is combined with SPWM to expand the linear modulation range.

To further reduce CMV, various carrier configurations are analyzed that enable CB CMV reduction. POD is known to limit CMV to $\pm 1/6 \cdot U_{\mathrm{DC}}$ by opposing the bottom carrier. Additionally, MPOD, a novel carrier configuration that opposes both carriers of the middle phase while the maximum and minimum phases essentially use PD carriers, is introduced.

Various modulation strategies are compared against each other in experimental analyses using a 3L-NPC. SPWM, SVPWM, VSVPWM, and HDSPWM are combined with PD, POD, and MPOD. First, the output current behavior is investigated. HDSPWM exhibits slightly less THD than SPWM, while VSVPWM exhibits the poorest output current behavior. Additionally, PD produces the best output currents and MPOD produces currents that are slightly worse than POD. Combining VSVPWM and POD results in poor behavior; therefore, only partial load measurements were conducted.

As expected, the comparison of DC link voltage behavior shows a perfectly balanced DC link with VSVPWM. The other modulators, SPWM, SVPWM, and HDSPWM, exhibit similar behavior, with a slight DC offset and a 150 Hz component in the DC link halves. However, the carrier configuration had no influence on the DC link voltage behavior. A comparison of efficiency shows that HDSPWM is as efficient as SPWM and SVPWM, while VSVPWM is slightly less efficient, especially at partial loads. Additionally, PD is the most efficient

carrier configuration. MPOD is slightly less efficient than POD, but only at partial loads.

Finally, a comparison of the CMVs of the modulation strategies reveals significant differences among them. Although HDSPWM has a slightly lower CMV than SPWM with PD, that is no longer the case with POD and MPOD. Additionally, the RMS value of the CMV with HDSPWM is only 4.1 % lower than with SPWM; a greater reduction would be expected. At the given operating point, however, the modulation index is too high, resulting in discontinuous PWM activation for only a short duration. MPOD significantly reduces the CMV when combined with all modulators, though POD slightly more effectively reduces the RMS value with SVPWM and VSVPWM. Nevertheless, the frequency spectra differ significantly. MPOD reduces the frequency components at the switching frequency and its multiples, spreading them into sidebands. SVPWM, VSVPWM, and the discontinuous mode of HDSPWM all exhibit significant low-frequency components, with the discontinuous PWM ranging up to a few kilohertz. Therefore, the impact of the modulation strategies on the CM currents depends on system impedance characteristics and must be evaluated experimentally, as discussed in Chapter 5.

In summary, the novel modulation strategies reduce the CMV. MPOD, in particular, exhibits very low CMV when used with all modulators. Conversely, HDSPWM reduces the CMV less than expected due to the operating point; however, it demonstrates favorable output current behavior. This could be due to either the active NP control or the vector calculation improving the output current behavior.

5 Experimental Analysis of Common-Mode Currents

This chapter describes the analysis of CM currents in an LV DC underlay grid with AC-side grounding using experiments that isolate different influencing factors. First, the circulating CM currents between two converters are investigated and a novel method of using a GNSS module to synchronize the switching of multiple converters is introduced. Next, a capacitive CM load is added to the DC side, and only one converter is used. Different modulation strategies and their CM current behavior are compared. Concluding the section, the previous experiments are combined by using two converters and a capacitive CM load to realistically represent a DC underlay grid with AC-side grounding. Simulations are then used to extend the measurement findings and identify additional factors influencing the CM currents. Section 5.4 describes EMI measurements analyzing the influence of different modulators on the interference voltage produced by the converter and its relationship to the CMV and CM currents. Lastly, the EMI measurements with one converter are compared to those with two converters.

5.1 Synchronization of Locally Distributed Converters

As previously discussed, synchronizing the switching of the converters is expected to reduce the CM currents and make them more predictable. However, this requires some form of communication between the converters. That is not an issue if the converters are placed close to each other, such as in the same building. For a DC underlay grid, however, the converters are distributed locally and can be several kilometers apart. This would require laying additional cables to establish a communication interface for synchronizing the PWM units, which would incur additional costs. Therefore, a different, low-cost synchronization method that does not require additional infrastructure, can be easily implemented, and can be retrofitted to existing systems is proposed.

5.1.1 Synchronization with Global Navigation Satellite System

GNSS provides a position signal and a time signal. The time signal can be used to synchronize distributed measurement units, for example [108]. It also provides the current date and time, received once per second with nanosecond accuracy [109]. Additionally, the GNSS receiver generates a pulse per second (PPS) from the time signal, which can be used to synchronize multiple converters [26]. If a distributed measurement unit is already installed nearby, the existing GNSS receiver can be used to synchronize the converters.

This work uses a u-blox MAX-M10S mounted on a SparkFun breakout board, as shown in Figure 5.1 [110, 111]. It is a cost-effective solution that provides the necessary PPS signal and has the required interfaces. The board is connected directly to the converter control board and shares the same power supply as the microcontroller. In addition to the 3 m antenna cable, a 10 m extension cable is used to place the GNSS antenna outside the test hall so that it can connect to the satellites. This is theoretically only necessary for the initial connection. Afterwards, the module stays connected, even inside a building, and can connect to the satellites during startup as long as the backup battery has power. If different cables or antennas are used, the delay between the two GNSS receivers can be measured or estimated and stored in their firmware. This allows the receivers to compensate for the delay and provide a more accurate time reference. However, since the same cables are used here, no additional compensation time is configured.

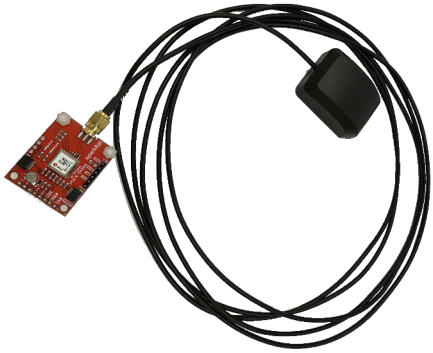
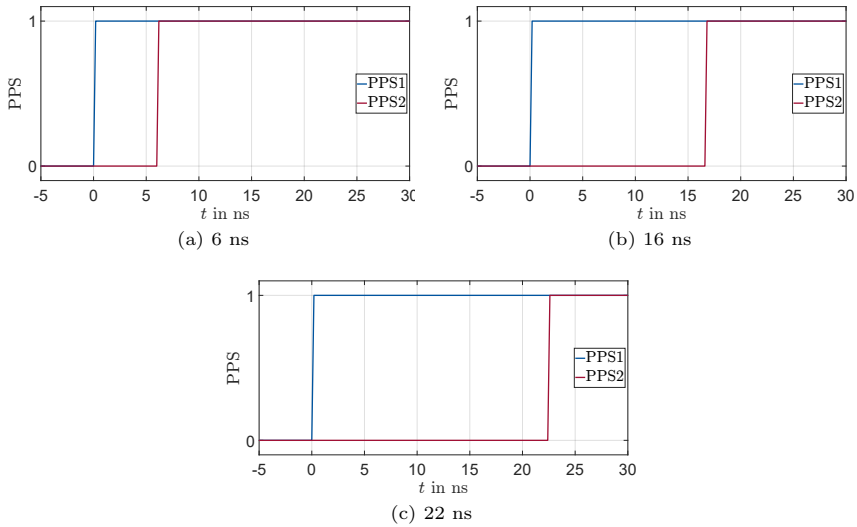


Figure 5.1: GNSS receiver board with u-blox MAX-M10S and antenna with 3 m cable.



(a) 6 ns

(b) 16 ns

(c) 22 ns

Figure 5.2: Different PPS signal delay times of two GNSS receivers.

Furthermore, the PPS signal, which is received once per second, can be configured at a frequency other than 1 Hz. The frequency of the PPS output signal of the u-blox MAX-M10S can be set to any value between 0.25 Hz and 10 MHz. This may be necessary for MPOD, as the microcontroller used for the converter control only updates the phase value used to shift the middle phase carrier when an external synchronization pulse is received. Thus, the PPS frequency must be configured to match f_{sw}, which is 8 kHz for the converters used here. If the clocks of the GNSS receiver and the microcontroller do not match exactly, the reset of the PWM unit, which is initiated by the PPS signal, might not occur precisely at a carrier minimum or maximum. Therefore, depending on the offset, a small deviation in the turn-on or turn-off times of the calculated values can occur. This can also lead to slight distortions once per second when using a 1 Hz PPS signal to synchronize the PWM units, which is possible with PD or POD because no phase shift change is necessary during operation. Overall, the timing of the switching signals is close enough when the synchronization happens at 1 Hz to avoid major offsets.

According to its datasheet, the u-blox MAX-M10S has a PPS accuracy of 30 ns RMS and 60 ns for 99 % of the time [110]. The location of the receivers does

not matter, whether they are close to each other or multiple kilometers apart, because they receive their signal from the same satellites. Even if they were connected to different satellites, the signal would still be well-synchronized [112]. Figure 5.2 shows the PPS signal measurements of the two GNSS receivers used in this thesis. Figure 5.2 (a) and (c) show a minimum difference of 6 ns and a maximum difference of 22 ns, respectively. Here, the PPS frequency was set to 8 kHz. When the PPS frequency is set to the default value of 1 Hz, the measured delay times increase to values between 20 ns and 45 ns. In both cases, however, the PPS signal of the first receiver always leads. Therefore, by configuring a cable delay of 14 ns, the difference between the two PPS signals can be reduced to ±8 ns.

5.1.2 Synchronization of Two Converters

The synchronization of two converters is now investigated on the test bench according to the measurement setup shown in Figure 5.3. Both CMVs and the circulating CM current i_{CM} between the converters are measured. The converters are operated with SPWM and PD and without a load because the CMV, and thus the CM currents, are not significantly load dependent. The CM chokes designed, built, and measured in Section 3.4 are used.

Figure 5.4 shows the measured CMVs and CM currents of both converters. For the unsynchronized measurement, the GNSS receiver antenna was removed from one of the converters. Figure 5.4 (a) shows that the CMVs are not aligned in

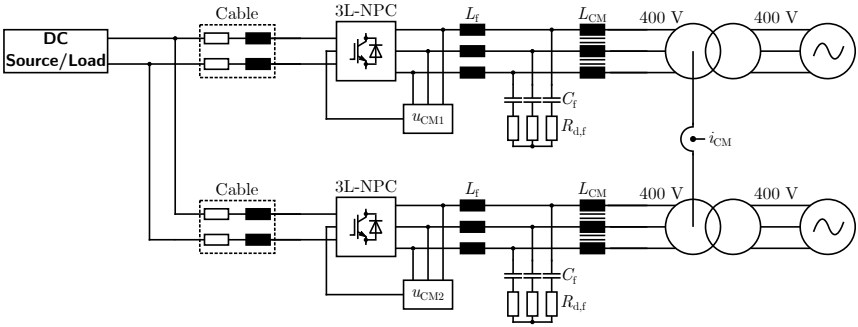
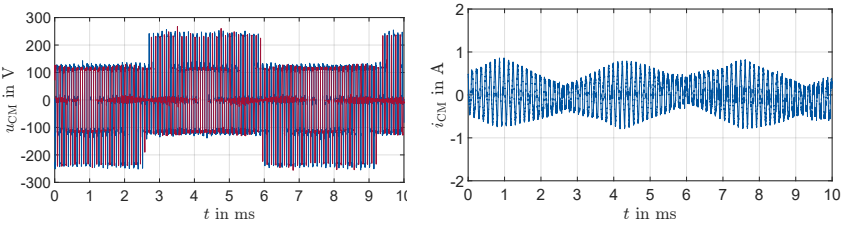
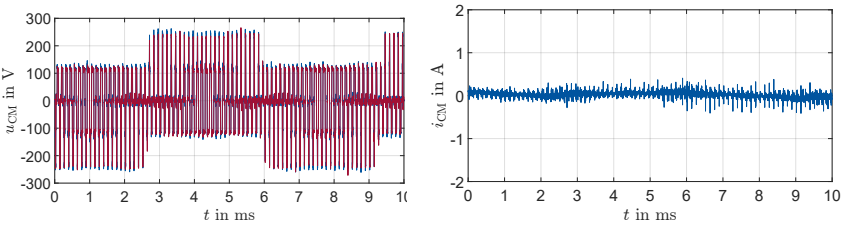


Figure 5.3: Measurement setup with two converters and GNSS synchronization.



(a) Not synchronized

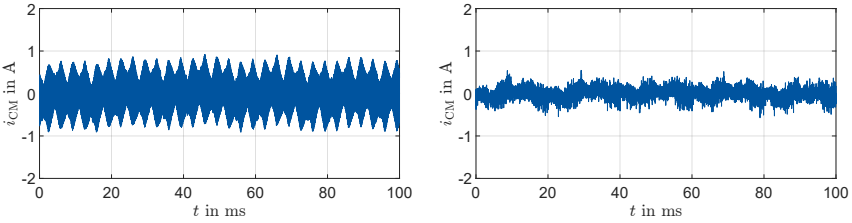


(b) Synchronized

Figure 5.4: CMV and CM currents with and without GNSS synchronization.

time and that a significant CM current of nearly 800 mA peak flows, with a primary frequency of 8 kHz. The amplitude increases and decreases at one-sixth of the AC-side fundamental frequency, according to the amplitude of the difference between the two CMV patterns. Synchronizing the two converters using the PPS signals of the GNSS receivers greatly reduces the current, as seen in Figure 5.4 (b). Only some high-frequency components remain, and the 8 kHz component is mostly removed. Figure 5.5 shows the CM currents over a longer time period of 100 ms. The RMS value of the unsynchronized CM current of 395 mA can be reduced by 82.3 % to a value of 70 mA.

Some minor low-frequency components are still visible, caused by slight differences in the voltage measurements of the two converters. This effect is apparent when the voltage measurement of one converter is intentionally altered. In the measurement shown in Figure 5.6, the DC voltage measurement is offset slightly with a low DC value. This leads to a low-frequency current at three times the grid frequency; in this case, 150 Hz. Although both converters are synchronized using the PPS signal, the RMS value is increased to 203 mA. This increase can be explained by a slight difference in the converters' CMVs because a low DM current flows from one converter to the other due to the perceived voltage difference between the two converters. Consequently, a 150 Hz component emerges



(a) Not synchronized (b) Synchronized

Figure 5.5: CM currents with and without synchronization measured over a longer time period of 100 ms.

alongside the switching frequency and its integer multiples in the difference of the two CMVs, resulting in a CM current. A greater difference between the two measurements results in a higher DM current and, consequently, an increased CM current. This behavior decreases under load due to the droop control, which reduces the voltage difference between the converters as the currents increase. Therefore, the no-load case examined here is the worst case for low-frequency CM currents.

Not all measurements without synchronized converters exhibit the high CM currents shown in Figure 5.4 (a). At certain times, the current is nearly as low as in the synchronized case, as shown in Figure 5.7. In this case, the RMS value is only 81 mA, which is 79.5 % lower than during periods with high CM currents. These periods occur when one microcontroller is synchronized with the real-time clock of the GNSS signal, while the other microcontroller runs freely based on its own clock from the quartz oscillator clock, which is not a real-time clock. Thus,

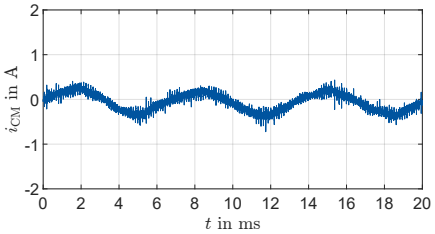
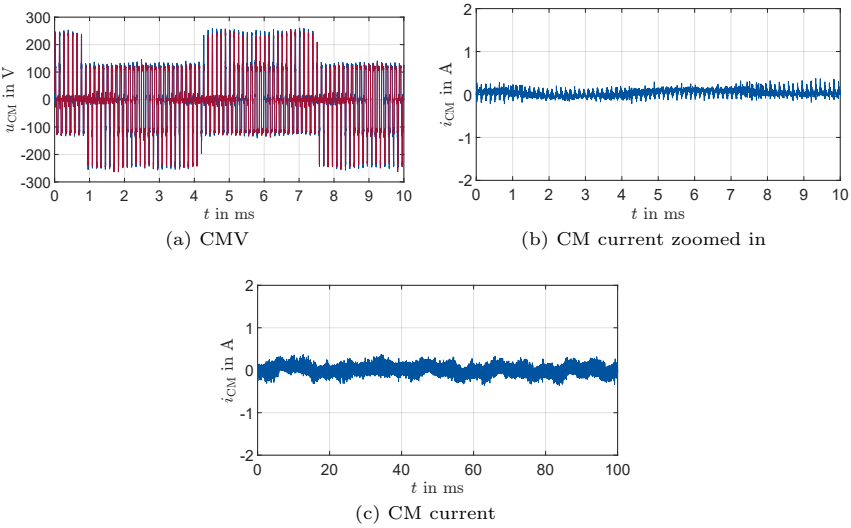


Figure 5.6: CM current with low frequency component from unequal DC voltage measurements.



(a) CMV

(b) CM current zoomed in

(c) CM current

Figure 5.7: CMV and CM currents with coincidentally aligned switching signals.

coincidentally, the switching signals align at certain points in time. However, the difference between the switching signals is still around 4.5 µs, as opposed to 62.5 µs at the maximum CM current. This difference is small enough that it does not cause significant CM currents, which can be estimated using Equation 5.1.

$$\hat{i}_{\mathrm{CM,pp}} = \frac{\Delta u_{\mathrm{CM}} \cdot \Delta t}{L_{\mathrm{CM1}} + L_{\mathrm{CM2}}} \tag{5.1}$$

Multiplying the maximum voltage difference Δu_{CM} of $1/3 \cdot U_{\mathrm{DC}}$ between the two CMVs by the time difference Δt of 4.5 µs and dividing by the sum of the CM inductances yields a peak-to-peak CM current $\hat{i}_{\mathrm{CM,pp}}$ of 117 mA. Assuming a triangular current waveform, this results in a peak value of 58.5 mA, yielding an RMS value of 34 mA. However, since the measured RMS value is higher, the remaining current components can be attributed to specific resonances triggered by switching and the imperfect adjustment of the DC voltage measurements of the two converters.

5.2 Capacitive Common-Mode Currents

After evaluating the circulating CM currents between two converters, the focus turns to investigating capacitive CM currents. To emulate capacitive CM loading, CM capacitors are added close to the DC load from both DC lines to the reference potential, which is the transformer star point. The CM capacitors model line-to-ground capacitance and the capacitance of PV panels to ground, as well as the capacitance of connected converter's EMI filters, as a single lumped capacitance [66, 113]. A value of 300 nF with a series resistance of 100 mΩ was chosen because it yields a resonance frequency of around 3 kHz for the CM capacitor C_{CM} and the CM choke L_{CM}, which is less than the switching frequency. An increased CM capacitance is assumed to lead to similar results, as the CM currents are limited by L_{CM} and no longer influenced by C_{CM}. First, only one converter is considered; later, a second converter is added to examine the impact of multiple converters on the CM currents.

5.2.1 One Converter with Common-Mode Load

First, the CM currents flowing through the CM capacitance induced by one converter are measured and analyzed according to the setup presented in Figure 5.8. The EMC voltage probe is connected to the positive DC line close to the converter while the measurements are being taken. The results of the EMI measurements are presented later in Section 5.4. Different modulators introduced in Chapter 4 are used and compared against each other. Figure 5.9 shows the CM currents of SPWM, SVPWM, VSVPWM, and HDSPWM with PD. SPWM and SVPWM currents exhibit a similar pattern of six increases and decreases per fundamental period. HDSPWM shows a comparable pattern, but with a slightly different waveform mixed in where the discontinuous PWM is active. Conversely, VSVPWM has a consistently high CM current.

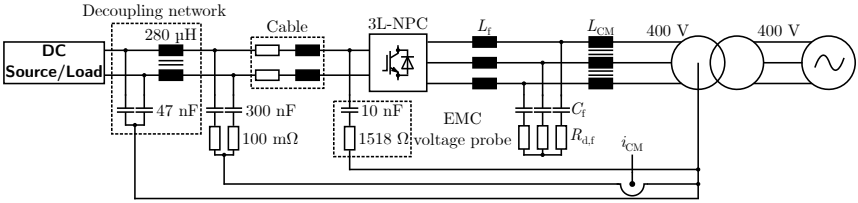
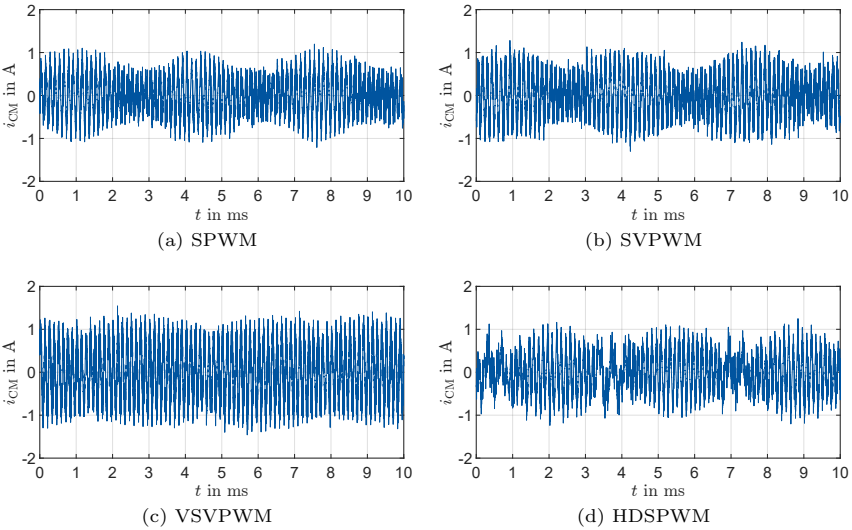


Figure 5.8: Measurement setup with one converter and capacitive CM load.



(a) SPWM (b) SVPWM

(c) VSVPWM (d) HDSPWM

Figure 5.9: Capacitive CM currents with different modulators with one converter and PD.

These findings are also evident when comparing the RMS values of the CM currents, as shown in Table 5.1. Although HDSPWM has a 4.1 % lower CMV RMS value according to Table 4.2, SPWM has the lowest RMS value of 398 mA. This demonstrates that the RMS value of the CMV and the individual frequency components are both relevant when estimating the CM currents generated by a specific modulator. VSVPWM has an RMS CM current that is 57.8 % higher than SPWM, which aligns with its 52.6 % higher RMS CMV value. Overall, the CM choke is designed for a limit of 600 mA, assuming modulators with three CMV steps. For these modulators, the RMS value stays below 600 mA under the given conditions; only VSVPWM exceeds the limit. Since even SVPWM has a margin of over 30 % above the limit, the CM choke design guide is confirmed

Table 5.1: RMS value of capacitive CM currents for all modulators with one converter and PD

SPWM	**SVPWM**	**VSVPWM**	**HDSPWM**
398 mA	459 mA	628 mA	455 mA

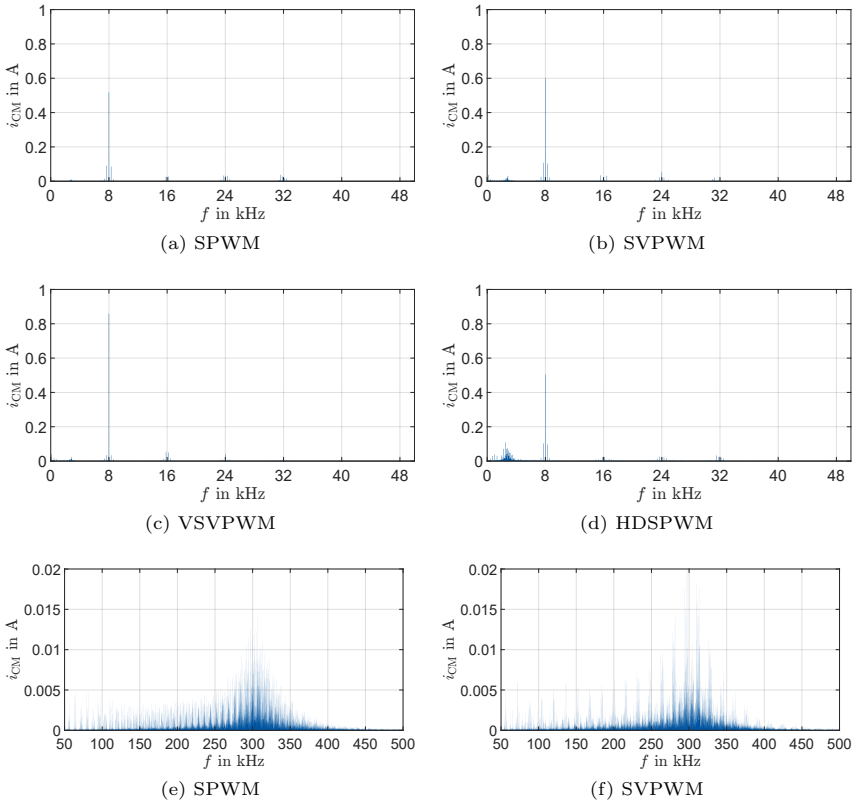


Figure 5.10: Spectrum of CM currents with different modulators with one converter and PD.

to be valid, as the inductance value is approximately 10 % higher than the calculated minimum, and the DC voltage can be increased by 7.5 % with the droop characteristic.

To explain why HDSPWM shows a higher CM current than SPWM, the frequency spectrum obtained with an FFT is analyzed, which is shown in Figure 5.10. Generally, a peak is present at the switching frequency of 8 kHz and its multiples with all modulation strategies. A comparison of the SPWM spectrum in Figure 5.10 (a) and the HDSPWM spectrum in Figure 5.10 (d) reveals similar

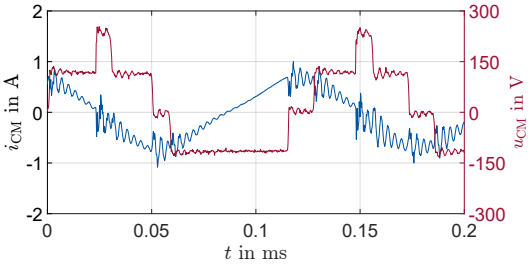
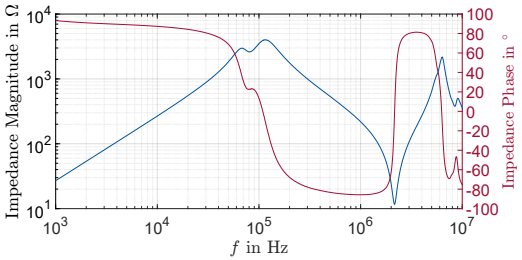


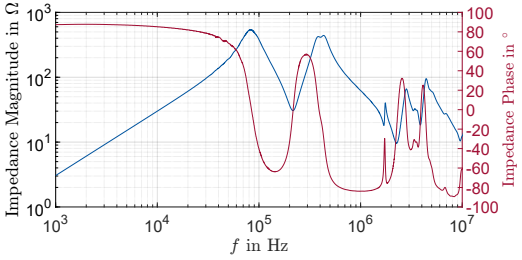
Figure 5.11: CM current and CMV at switching frequency scale.

components above 8 kHz. However, the HDSPWM spectrum contains several additional components below 4 kHz. Notably, there are frequency components at the resonance frequency of the CM capacitors and the CM choke inductance, around 3 kHz. These components are excited by the increased low-frequency components of the discontinuous PWM spectrum, as revealed in Section 4.4. This ultimately leads to an increased RMS value of HDSPWM, as the other frequency components are comparable to those of SPWM. The SVPWM and VSVPWM spectra also show slightly increased low-frequency components, but do not excite the CM resonance frequency as much as HDSPWM. Their higher RMS value, however, is explained by an increased 8 kHz component, which is particularly high with VSVPWM.

In general, above 50 kHz the spectral components decrease with increasing frequency, as can be seen in Figures 5.10 (e) and (f). However, an area with increased spectral components can be observed slightly below 300 kHz. This frequency is also clearly visible in the CM current waveform shown in Figure 5.11. Additionally, Figure 5.11 shows that the CMV exhibits the same oscillations. Each switching action causes an oscillation close to 300 kHz, along with a superimposed oscillation at around 2 MHz. These oscillations cannot be explained by the simplified models used until now. Therefore, the CM choke model must be extended to include a parasitic capacitance in parallel with the CM inductance [72, 114, 115]. An impedance measurement of the CM choke is performed using the OMICRON Lab vector network analyzer Bode 100 [116]. Figure 5.12 (a) shows the impedance magnitude and phase as a function of frequency, obtained by shorting the three input terminals and the three output terminals. As can be seen, up to 100 kHz, the CM choke inductance dominates the impedance, while between 150 kHz and 2 MHz, a capacitive impedance characteristic is visible. Selecting values from these two sections with phases of about 90° and -90° can be used to calculate the inductance and parallel capacitance



(a) CM Choke

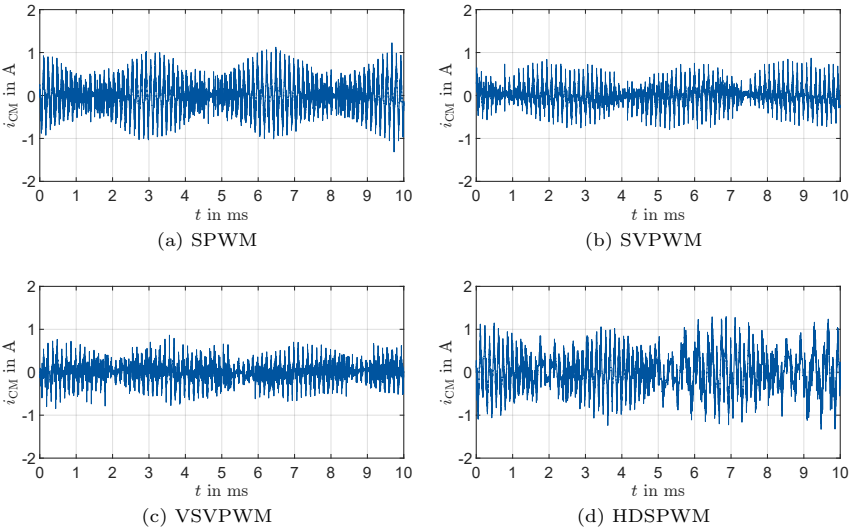


(b) DM Inductor

Figure 5.12: Impedance magnitude and phase of CM choke and DM inductor, measured with a vector network analyzer.

of the CM choke, respectively. At a frequency of 3.195 kHz, a phase of 90° is measured, along with an impedance of 85.45 Ω, yielding a CM inductance value of 4.26 mH, only 1.7 % higher than the measurement taken with the LCR meter in Chapter 3. Conversely, at a frequency of 997.15 kHz, an impedance amplitude of 219.588 Ω is measured at a phase of -85.718°, the lowest impedance phase. Using these values, a capacitance of 727 pF is calculated. However, the first self-resonance cannot explain the oscillations at 300 kHz and 2 MHz visible in Figure 5.11, as the calculated frequency is 90.5 kHz. Furthermore, self-resonance is visible in the impedance magnitude, which shows only a minor decrease at around 90 kHz. Nevertheless, a second self-resonance point of the CM choke is visible at 2.1 MHz, formed by a series connection of a stray inductance to the stray capacitance. At this point, the impedance magnitude drops significantly to 11 Ω, explaining the high-frequency oscillations at around 2 MHz.

To explain the resonance slightly below 300 kHz, the impedance of the DM inductor is measured as shown in Figure 5.12 (b). Similar to the procedure for



(a) SPWM (b) SVPWM

(c) VSVPWM (d) HDSPWM

Figure 5.13: Capacitive CM currents with different modulators with one converter and POD.

the CM choke, the inductance of the DM filter, which was previously measured at 480 µH with an LCR meter, is determined. At a frequency of 1.953 kHz, the impedance magnitude is measured to be 5.927 Ω, with a phase of 87.785°. This yields a DM inductance of 483 µH, resulting in a CM inductance of 161 µH. This value is very close to that measured with the LCR meter. Combined with the parasitic inductance, which is multiplied by three in a CM circuit, the resonance frequency is 269 kHz. Thus, the resonance point created by the DM inductance and the CM choke's stray capacitance is responsible for the oscillations slightly below 300 kHz.

Now, the CM currents using POD are investigated and are shown in Figure 5.13. As can be seen, the CM currents are slightly reduced with SPWM and HDSPWM, and significantly reduced with SVPWM and VSVPWM, compared to PD. This is also evident when comparing the RMS values shown in Table 5.2. The RMS values are reduced by 22.6 % and 16.9 % for SPWM and HDSPWM, respectively. However, the reduction is 57.1 % for SVPWM and 74.8 % for VSVPWM. Note that combining POD with VSVPWM results in poor output current behavior, so the significant reduction cannot be utilized under load.

Table 5.2: RMS value of capacitive CM currents for all modulators with one converter and POD

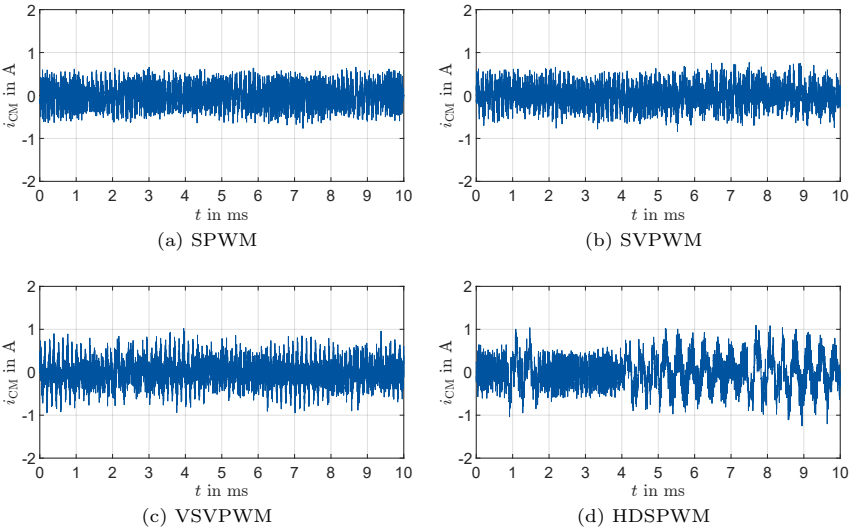
SPWM	SVPWM	VSVPWM	HDSPWM
308 mA	197 mA	158 mA	378 mA

When changing PD to POD, similar percentages of reduction in RMS values of CM currents and CMV are reached for SPWM and HDSPWM, according to Table 4.2. However, SVPWM and VSVPWM show a much greater decrease in CM currents than the CMV reduction. The CMV spectrum, shown in Appendix A.2, has a high 150 Hz component for SVPWM and VSVPWM, which is absent from the CM current spectrum shown in Appendix A.3. This is due to the high impedance of the CM capacitance in the low-frequency spectrum, which reduces the 150 Hz current component. Furthermore, POD significantly reduces the 8 kHz component at the switching frequency in both the CM current and CMV spectra. Since SPWM and HDSPWM do not exhibit significant low-frequency components, the reduction of CM currents is attributed to the reduction of CMV, resulting in a similar percentage change. The frequency spectra above 50 kHz show no significant differences between POD and PD.

Next, the CM currents with MPOD, which are shown in Figure 5.14, are investigated. Compared to PD, all modulators show a significant reduction in CM currents. Even when comparing to POD, the CM currents of SPWM and HDSPWM are visibly reduced, while the waveforms of SVPWM and VSVPWM exhibit slightly different behavior. Table 5.3 shows the RMS values of the CM currents. When compared to the values with PD and POD, it is apparent that MPOD yields the lowest CM currents, except when combined with VSVPWM, when POD results in the lowest values. A reduction of more than 55 % is achieved for SPWM, SVPWM, and VSVPWM when compared to PD. HDSPWM showed the lowest reduction of 36.9 %. For SPWM, the percentage change of the CMV is comparable to that of the CM currents, while for SVPWM and VSVPWM, a higher reduction is observed, and for HDSPWM, a lower reduction of the CM currents is observed. Overall, the RMS currents with SPWM, SVPWM, and

Table 5.3: RMS value of capacitive CM currents for all modulators with one converter and MPOD

SPWM	SVPWM	VSVPWM	HDSPWM
178 mA	175 mA	186 mA	287 mA



(a) SPWM (b) SVPWM

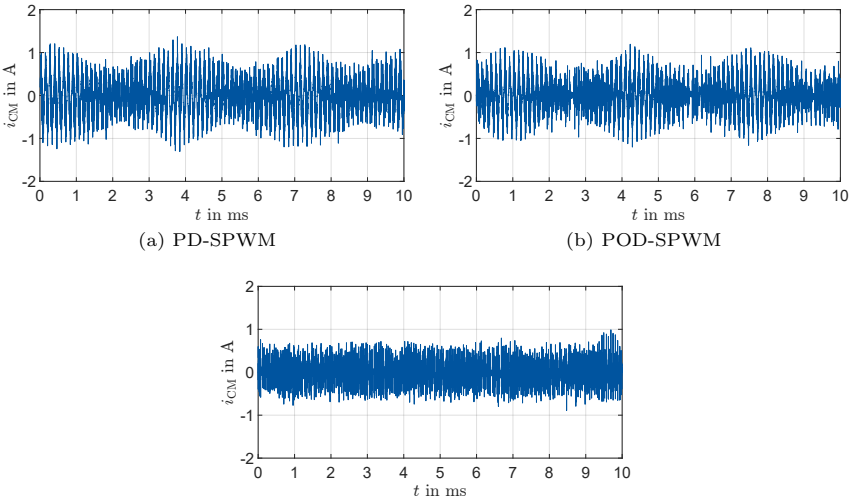
(c) VSVPWM (d) HDSPWM

Figure 5.14: Capacitive CM currents with different modulators with one converter and MPOD.

VSVPWM are very comparable, with values around 180 mA. Therefore, using MPOD could greatly reduce the CM choke inductance value compared to PD, a factor that could be included in the CM choke design guide.

As can be seen in Appendix A.3, comparing the frequency spectra of the CM currents with MPOD to those with PD and POD shows a significant reduction of the 8 kHz component with all modulators. However, an increase of sideband components is evident, similar to what was observed in the CMV spectra. This results in a slightly broader frequency band compared to the pronounced peaks of the PD and POD spectra. Once again, no major differences between PD, POD, and MPOD are identifiable above 50 kHz.

Finally, the possibility of a change in the CM currents under load is investigated. To this end, a 15 kW load is applied, and PD, POD, and MPOD are combined with SPWM. Figure 5.15 shows the resulting CM currents. There are no significant differences when comparing them to Figures 5.9 (a), 5.13 (a), and 5.14 (a). Furthermore, the RMS currents, which are shown in Table 5.4, are within a ± 2 % range compared to the no-load case. Lastly, the frequency



(a) PD-SPWM

(b) POD-SPWM

(c) MPOD-SPWM

Figure 5.15: CM currents with different modulators with one converter and 15 kW load.

Table 5.4: RMS value of CM currents with SPWM and 15 kW load

	PD	**POD**	**MPOD**
SPWM	401 mA	307 mA	175 mA

spectra in Appendix A.3 also show no significant differences. Therefore, the measurements reveal no load dependence of the CM currents.

5.2.2 Increased Common-Mode Resonance Frequency

Previous measurements were carried out with a switching frequency above the resonant point of the capacitive CM load and the CM choke inductance. Unlike the setup shown in Figure 5.8, the 300 nF CM capacitors that were connected between the DC poles and the transformer star point are now removed. This increases the calculated resonance frequency slightly above the switching frequency f_{sw} where an excitation is likely.

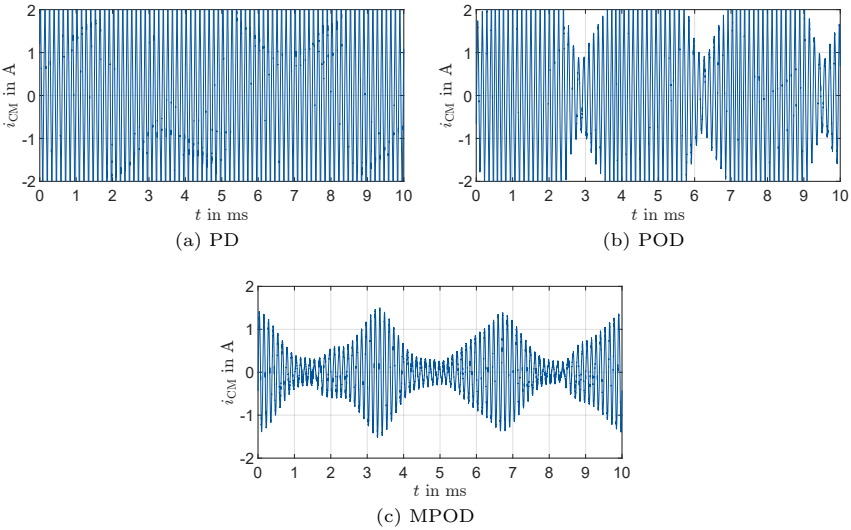


Figure 5.16: CM current with sub-resonant switching frequency and SPWM with different carrier configurations.

Figure 5.16 shows the measured CM currents with SPWM in combination with PD, POD, and MPOD. As can be seen, the CM choke saturates with PD and POD, leading to high CM currents. Stable operation is only possible with MPOD; however, the currents are still significantly higher than in previous measurements. Even with MPOD, the RMS value is 579 mA, which is more than three times higher than with a larger CM capacitance and MPOD SPWM.

In principle, a switching frequency below the resonance frequency is preferable because the capacitive CM currents are low due to the small capacitance, and synchronizing converters reduces the circulating CM currents between them. Consequently, the CM currents should be very low. However, in reality, exciting a resonance frequency can easily increase the CM currents, which can lead to saturation of the CM chokes and drastically increase the CM currents. Furthermore, the parasitic cable capacitances quickly add up to a value that renders a sub-resonant switching frequency infeasible for larger DC systems, such as a DC underlay grid.

5.2.3 Two Converters with Common-Mode Load

Finally, a second converter is added to the system, combining the measurement setups from Sections 5.1 and 5.2.1, as shown in Figure 5.17. The DC connection uses cables of similar length, leading to a system that is mostly symmetrical, except for the transformers, which are from different manufacturers and have slightly different specifications. Additionally, the CM chokes differ by 5 % in their CM inductance. Fuses are added to the two paths connecting the transformer star points to protect the system from high CM currents in the event that one or both CM chokes saturate.

Both converters are synchronized with a GNSS signal, as introduced in Section 5.1, and the PPS signal frequency is set to 8 kHz. Overall, the system now represents a DC underlay grid with two terminals at different distribution grid transformers. This section measures and analyzes the CM current i_{CM} flowing through the CM capacitance. Ideally, this current would split equally between the two converters connected to the DC system, a condition that can be assumed here due to the symmetry of the current paths and the synchronized switching. Different modulators are used and compared against each other and against previous measurements with only one converter.

As shown in Figure 5.18, only PD with SPWM was able to prevent the CM chokes from saturating. Combining PD and SVPWM results in constant saturation, which caused one of the fuses to blow at $t = 8.5$ ms, as seen in Figure 5.18 (b).

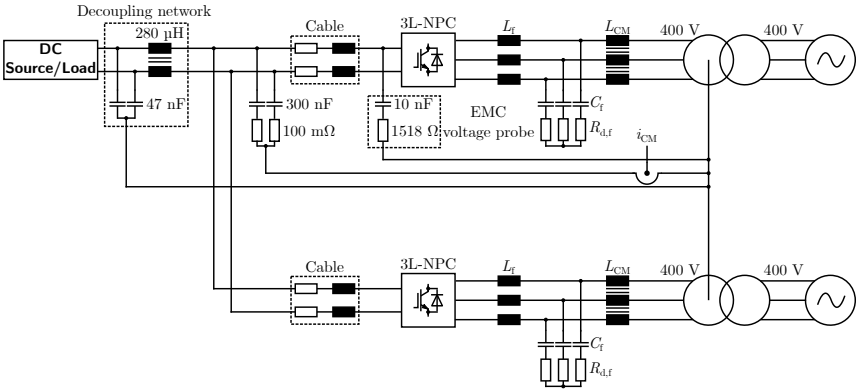
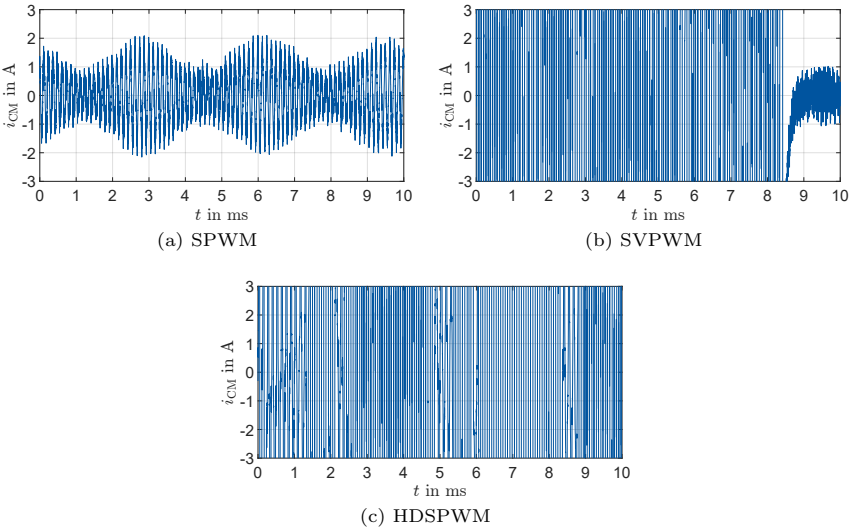


Figure 5.17: Measurement setup with two converters and capacitive CM load.



(a) SPWM

(b) SVPWM

(c) HDSPWM

Figure 5.18: Capacitive CM currents with different modulators with two converters and PD.

HDSPWM, on the other hand, has periods when the CM chokes saturate and periods when the system is stable, as shown in Figure 5.18 (c). The combination of PD and VSVPWM was not tested because even higher CM currents than with SVPWM are expected, where the fuse blew quickly. Overall, the CM currents are more than doubled compared to a single inverter, though the CM model suggests doubling with a switching frequency above the resonance frequency. However, this only applies to much larger CM capacitances, around ten times the resonance capacitance. In this system, the resonance capacitance would be at around 90 nF; thus, the CM capacitance used is not much larger. Therefore, at 8 kHz, its impedance is in a range where the parallel connection with one of the CM chokes reduces the CM impedance compared to the CM capacitance alone in the current path, as was the case with one inverter. Applying the superposition principle to both sources leads to more than double the CM currents. This is also apparent when comparing the RMS values of PD SPWM with one and two converters. An RMS value of 398 mA was measured with one converter, while a value of 878 mA is calculated with two converters, yielding a factor of 2.21. In the cases of SVPWM and in certain regions of HDSPWM, this impedance reduction increases the currents, saturating at least one of the CM chokes.

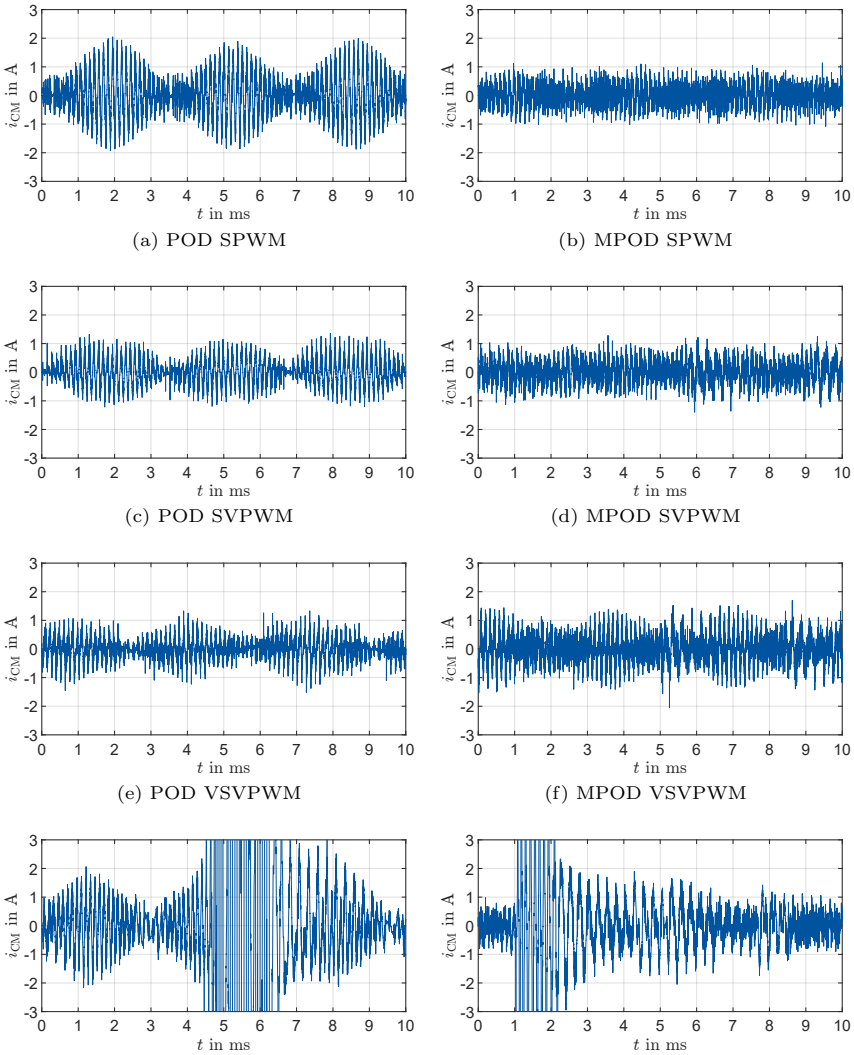
Table 5.5: RMS value of capacitive CM currents for all modulators with two converters

	SPWM	**SVPWM**	**VSVPWM**	**HDSPWM**
PD	878 mA	-	-	-
POD	661 mA	404 mA	290 mA	-
MPOD	312 mA	351 mA	418 mA	-

Continuing with the reduced CMV modulators, HDSPWM is the only one that leads to the saturation of at least one of the CM chokes, while SPWM, SVPWM, and VSVPWM result in stable operation without saturation, as shown in Figure 5.19. Here, POD reduces i_{CM}, especially with SVPWM and VSVPWM. Although a reduction is visible for SPWM and HDSPWM, it is more pronounced with the other two modulators, as was the case with a single converter in the previous section. Again, MPOD produces a significantly different current pattern than PD and POD. The reduction is particularly high in combination with SPWM, as seen in Figure 5.19 (b). Additionally, periods of CM choke saturation are less frequent and shorter with HDSPWM and POD, and even rarer with MPOD.

To make an initial comparison between the different modulators and the case with one inverter, the RMS values of the CM currents are calculated and shown in Table 5.5. Only combinations that did not lead to saturation are considered here. First, the values with two inverters are compared to each other. For SPWM, POD reduces the RMS value by 25 % to 661 mA, compared to PD. With SVPWM, the value can be reduced by an additional 39 % to 404 mA, and with VSVPWM, it can be reduced even further, to 290 mA. However, as previously already mentioned, the combination of POD and VSVPWM is not recommended due to high THD and unusual DC link balancing behavior. Using MPOD with SPWM reduces the RMS value by 64 % compared to PD, reaching a value of 312 mA, the second-lowest value after POD with VSVPWM. Furthermore, MPOD is beneficial with SVPWM, as a 12 % reduction was measured compared to POD. Conversely, MPOD led to a 44 % increase compared to POD for VSVPWM; however, with the expected behavior of VSVPWM and a low THD. Overall, combining any modulator with MPOD yields the lowest RMS values of the CM currents.

Comparing the RMS values of the different modulation strategies with the results of a single converter given in Tables 5.1, 5.2, and 5.3 shows that the general trends are similar, with only minor differences. As mentioned, the ratio of



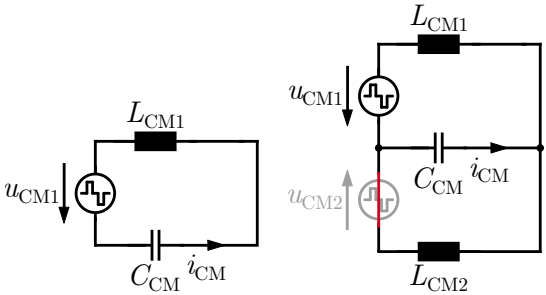
(a) POD SPWM (b) MPOD SPWM

(c) POD SVPWM (d) MPOD SVPWM

(e) POD VSVPWM (f) MPOD VSVPWM

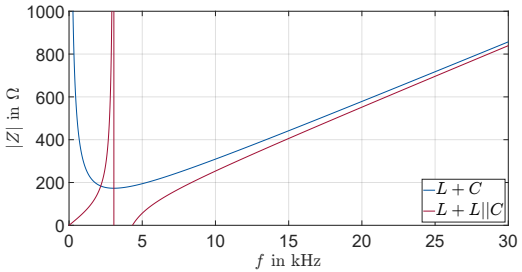
(g) POD HDSPWM (h) MPOD HDSPWM

Figure 5.19: Capacitive CM currents with different modulators and two converters.



(a) Equivalent circuit with one converter

(b) Equivalent circuit with two converters and superposition principle



(c) Impedance curves

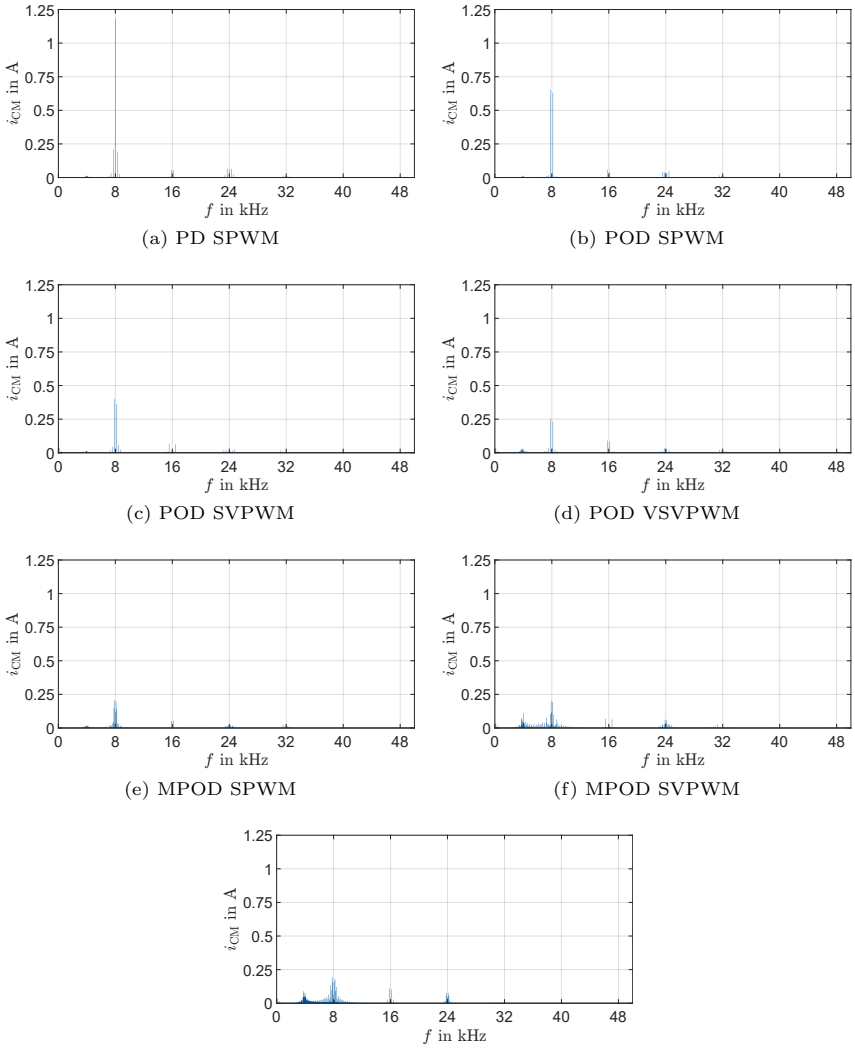
Figure 5.20: Equivalent impedance with one and two converters.

the two PD SPWM measurements is 2.21, slightly above the expected value of 2. This is also true for SPWM and SVPWM with POD and VSVPWM with MPOD. However, a factor below 2 is reached with POD and VSVPWM, as well as with MPOD and SPWM. The only case in which the factor is exactly 2 is between the measurements with MPOD and SVPWM.

A more detailed impedance curve of the two systems is necessary to explain how their behavior changes with the addition of a second converter. With only one inverter and a CM capacitor, an LC series circuit is formed and excited by the CMV, as shown in Figure 5.20 (a). However, with two inverters, one inductance is in series with an LC parallel circuit, as introduced in Section 3.2. Figure 5.20 (b) shows the corresponding equivalent circuit, in which the second source is shorted when the superposition principle is applied. When investigat-

ing the influence of the second source, the first CMV source is shorted, resulting in a similar circuit. If the CM inductances are equal, the resonance poles of both superimposed circuits are the same. Otherwise, two resonance poles arise. Figure 5.20 (c) shows the impedance curves for both cases, neglecting any resistances in the system that would dampen resonance peaks. The values $L_{\mathrm{CM1}} = L_{\mathrm{CM2}} = 4.5$ mH and $C_{\mathrm{CM}} = 600$ nF are assumed, resembling the values of the filters used in the measurements. The impedance curves differ, especially in the low-frequency region and at the resonance point, leading to specific frequencies being dampened more than others. The impedance curve is similar for higher frequencies above the switching frequency with the given values. It should be noted, however, that a superposition exists in the case of two inverters, which is why low-frequency currents that mainly flow through the inductance parallel to the capacitance cancel each other out during simultaneous switching, as shown in Section 3.2. Nevertheless, since the modulators differ slightly in the CMV frequency spectrum up to the switching frequency, the resulting CM currents differ depending on the applied impedance curve. Furthermore, the discontinuous PWM mode of HDSPWM shows significantly higher frequency components than the other modulators, as seen in Figure 4.17. This excites the resonance frequency more, eventually leading to saturation of the CM chokes. Additionally, increasing the CM capacitance shifts the resonance peak to lower frequencies. This eventually leads to a significant increase in the low-frequency components of SVPWM and VSVPWM, which are not reduced by POD and MPOD, as shown in Section 4.4. Unlike the inductive path, they do not cancel each other out when the superposition is applied as they flow through the CM capacitance. Therefore, MPOD SPWM appears to be the best modulation strategy regarding CM currents in all grid configurations because it has the lowest components in the low-frequency range and overall low frequency component levels.

Figure 5.21 shows the frequency spectra of the measured CM currents, where the overall low frequency components of SPWM and MPOD are evident. As was apparent in the time domain, POD reduces the 8 kHz component more for SVPWM and VSVPWM than for SPWM. Further reduction is possible with MPOD, but this increases the sidebands and components around the resonance frequency. Although SPWM combined with MPOD has higher components around the resonance frequency than SPWM combined with PD or POD, these components are still lower than those of MPOD combined with SVPWM or VSVPWM. Overall, the spectra are comparable to those gathered with one converter, but they have increased individual frequency components and slightly higher resonance components below the switching frequency.



(a) PD SPWM

(b) POD SPWM

(c) POD SVPWM

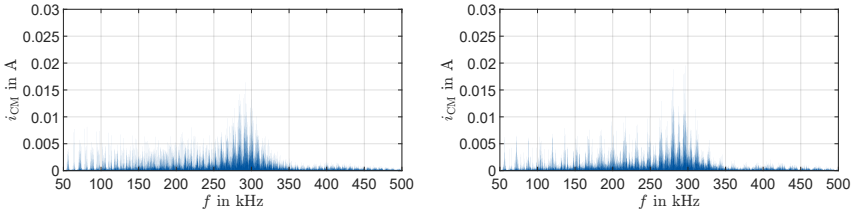
(d) POD VSVPWM

(e) MPOD SPWM

(f) MPOD SVPWM

(g) MPOD VSVPWM

Figure 5.21: Frequency spectrum of CM currents with different modulators with two converters.

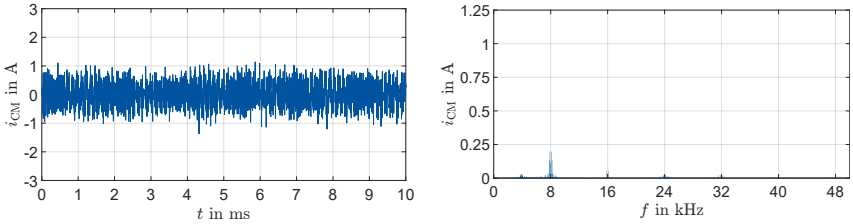


(a) SPWM (b) SVPWM

Figure 5.22: Frequency spectrum of CM currents above 50 kHz with two converters and MPOD.

The same applies to the frequency spectra above 50 kHz, shown in Figure 5.22. Here, the spectral components are even more comparable to those measured with one converter, with only slight differences around the resonance frequency of the CM chokes' parallel capacitance and the DM filter inductance. The remaining frequency spectra, which are not shown here, can be found in Appendix A.3.

Finally, a 15 kW load is added to the system. Figure 5.23 (a) shows the measured CM currents with MPOD SPWM, revealing no significant difference compared to the no-load case. Furthermore, the RMS value of 311 mA is essentially the same, as it is only 1 mA higher. A comparison of the frequency components in Figure 5.23 (b) and Figure 5.21 (e) also reveals no significant differences. Therefore, the CM currents measured here are independent of the load.



(a) Time domain (b) Frequency domain

Figure 5.23: CM current with MPOD-SPWM with two converters and 15 kW load.

5.3 Additional Simulative Considerations

Up to this point, an almost ideal system has been assumed: one that is nearly symmetrical and uses the same converters and control. This system is also essentially connected to the same AC grid. This is beneficial for experimental validation because it reduces the risk of damage. Additionally, some limitations cannot be removed in the laboratory setup. However, these ideal circumstances might not be present in a real system. Therefore, simulations are carried out to extend the measurements and test additional cases.

As can be seen from the CM model derived in Chapter 3, the sum or difference of the converters' CMVs are responsible for the CM currents. Several parameters can influence the CMV of a converter. The following parameters are identified as possible influencing factors with a significant impact:

- AC grid phase, amplitude and harmonics: Deviations in the AC grid phase can result from different vector groups of distribution grid transformers. In theory, any multiple of 30 degrees is possible. However, due to the tripled fundamental frequency of the CMV, a 120° phase difference does not affect the CM currents. Furthermore, the amplitude can vary due to different loading, for example. Lastly, different harmonic distortions from other converters connected to the grid section can influence the control or propagate into the DC system.

- Different modulators: Previous sections have shown that modulation strategies significantly impact the CMV and, consequently, the CM currents. However, only the same modulator was used for both converters. Therefore, the influence of combining different modulators still needs to be investigated.

- Multiple converters: Using more than two converters increases the complexity of the system, as discussed in Chapter 3. Theoretical considerations must be validated through simulations.

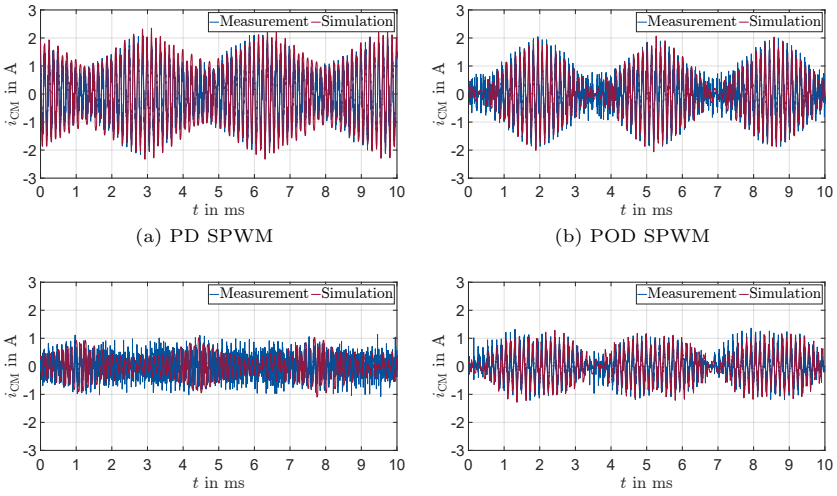
- Switching frequency: The switching frequency is one of the primary frequency components of the CMV, regardless of the modulation scheme.

- CM filter inductance: With vastly different CM filter inductances, the system becomes less symmetric, and specific current components may no longer cancel each other out.

- Control parameters: Two converters may not have the same control parameters, and they may have different control strategies. These differences could affect exact timing in the CMV profile or the behavior of the DC link voltage, which could impact the CMV.

There are other influencing factors, but this section only covers the ones mentioned above.

A simulation model resembling the measurement setup is built in the piecewise linear simulation software PLECS. The AC grids are modeled as ideal voltage sources, and the IGBTs and diodes are treated as ideal switches. The CM chokes are modeled as coupled inductors, and the transformers, DM filter inductance, and DC cables are modeled as LR series elements. All parameters are determined using an LCR meter to achieve the most realistic representation possible. However, parallel capacitances, saturation, and other nonideal components of the CM and DM chokes and the transformers are neglected, leading to slightly different behavior in the high-frequency range. Nevertheless, the simulation investigations focus on the lower frequency range up to 50 kHz, where no signif-



(a) PD SPWM (b) POD SPWM

(c) MPOD SPWM (d) POD SVPWM

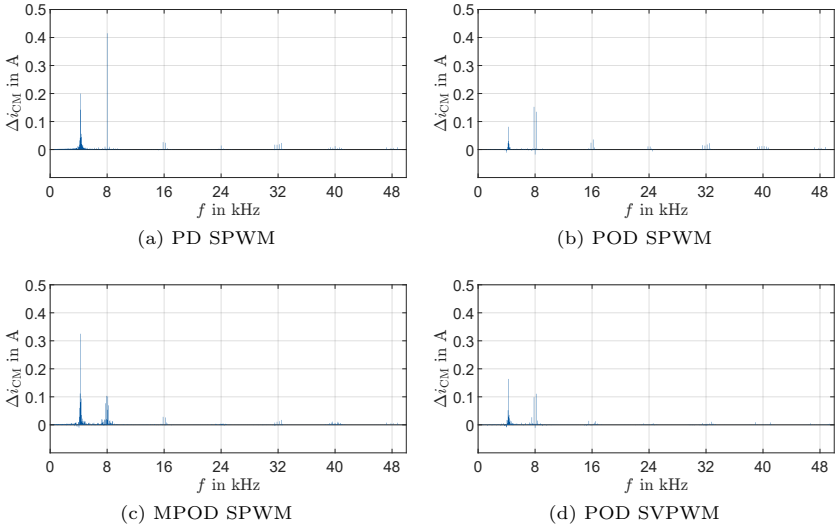
Figure 5.24: Comparison of measured and simulated CM currents with different modulators.

icant influence of parasitic components is expected. The same converter control used in the measurement setup is implemented, but differences remain regarding timing, noise, and modulator implementation compared to a microcontroller. Overall, these simplifications and the slightly different controller behavior can lead to small deviations between measurements and simulations. Nevertheless, investigating the general influence of the previously mentioned parameters can help to draw conclusions about the expected behavior in a real setup.

First, the simulation is validated by comparing it to test bench measurements. For simplicity, the simulations focus on four modulator combinations: PD SPWM, POD SPWM, MPOD SPWM, and POD SVPWM. Figure 5.24 shows the measured and simulated CM currents with different modulators. The overall waveforms are comparable, especially with PD and POD. However, some high-frequency components caused by parasitic elements neglected in the simulation model are missing, making the currents more triangular. A comparison of the RMS values reveals higher values in the simulations, as can be seen in Table 5.6. Although high-frequency components are missing, some effects that limit the CM currents are also neglected. For example, the frequency dependency of resistors. Overall, the values increase by 21 % to 36 % in the simulation, but the order of the highest to lowest RMS values remains the same. Figure 5.25 shows the difference between the individual frequency components of the measured and simulated CM currents. The simulated CM current must first be interpolated because a variable time solver was used for the simulation, whereas a fixed sample time is necessary for the FFT. As was previously evident, the simulation overestimates the CM currents, especially at the resonance and switching frequencies. However, POD SPWM and POD SVPWM have smaller differences between measurements and simulations than PD SPWM and MPOD SPWM. Nevertheless, the frequency components occur at similar points. In summary, the simulation model is suitable for comparative analyses of factors that influence CM currents in a DC underlay grid with AC-side grounding.

Table 5.6: RMS values of measured and simulated CM currents with selected modulators

	Measurement	**Simulation**
PD SPWM	878 mA	1176 mA
POD SPWM	661 mA	802 mA
MPOD SPWM	312 mA	425 mA
POD SVPWM	404 mA	516 mA

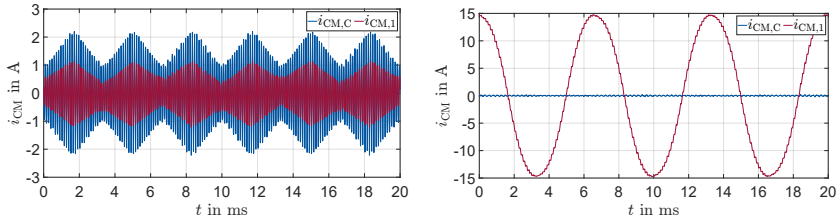


(a) PD SPWM (b) POD SPWM

(c) MPOD SPWM (d) POD SVPWM

Figure 5.25: Difference of measured and simulated CM current spectra.

Now, the influence of various parameters of the supplying AC distribution grids is investigated. Figure 5.26 shows the simulated CM currents with a 60° phase difference between the two supplying AC grids. When both converters use PD SPWM, there is no significant difference in the capacitive current $i_{\mathrm{CM,C}}$ or the current at the star point of the distribution transformer, where the first converter is connected, compared to when both grids are in phase. However, when the modulation strategy of both converters is changed to POD SVPWM, a significant low-frequency current appears in $i_{\mathrm{CM},1}$, while $i_{\mathrm{CM,C}}$ decreases. This can both be explained by analyzing the CMV profiles of the two modulators, which can be found in Figure 4.15. With PD SPWM, a 60° phase shift of the signal results in a similar sum of the two CMVs, whereas the difference increases. Because the sum is much higher than the difference, and because of the increased impedance of the inductive path at the excited frequencies, the capacitive CM currents dominate. However, with POD SVPWM, the phase shift creates nearly perfect opposition between the two CMVs. Thus, the capacitive CM current is significantly reduced, and the frequency components add up when the two signals are subtracted. This results in a significant 150 Hz component in the inductive path, which has a much lower impedance than the capacitance at this frequency. Therefore, it is evident in the circulating current between the

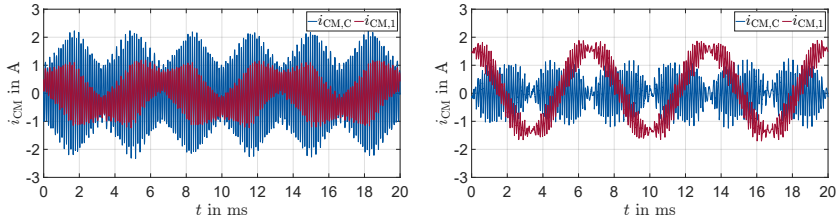


(a) PD SPWM (b) POD SVPWM

Figure 5.26: Simulated CM currents with a phase difference between the supplying AC grids.

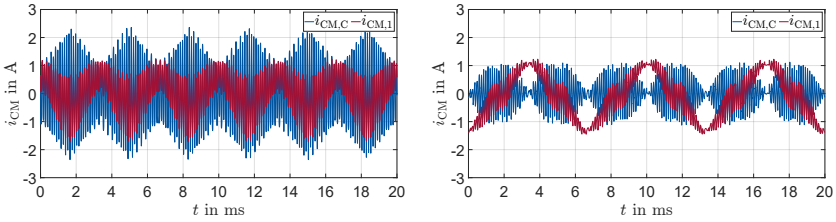
two converters. In general, modulation strategies with significant low-frequency components should be avoided when there is a phase difference between the supplying AC grids. Similar but less pronounced behavior is exhibited by other phase differences because 60° is the worst case.

Next, an amplitude difference between the two AC grid voltages is examined. One of the two grid voltages is set to +10 %, and the other is set to -10 %, which is the maximum expected amplitude difference in the LV AC grid. Figure 5.27 shows the simulated CM currents with both modulators set to PD SPWM or POD SVPWM. In this case, both modulation strategies result in similar capacitive CM currents $i_{CM,C}$ compared to those with the same voltage amplitude. However, the converter CM currents $i_{CM,1}$ show an increased low-frequency component and decreased high-frequency components. Once again, POD SVPWM leads to a higher 150 Hz component, whereas with PD SPWM, the increased



(a) PD SPWM (b) POD SVPWM

Figure 5.27: Simulated CM currents with an amplitude difference between the supplying AC grids.



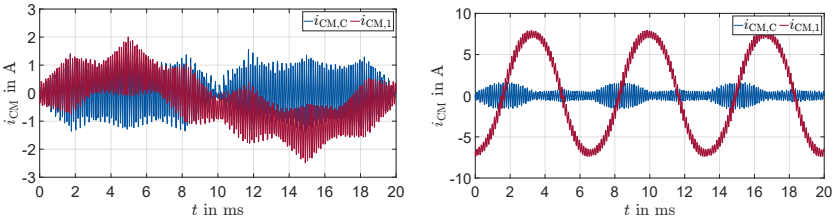
(a) PD SPWM (b) POD SVPWM

Figure 5.28: Simulated CM currents with harmonics in the supplying AC grids.

150 Hz component is only perceived as higher because of the reduced switching frequency component.

Finally, the influence of harmonics added to one of the two AC grid voltages is investigated. In the simulation, the harmonics are added with a fixed amplitude of 10 V to all three phases, each with the corresponding phase shift. Only the addition of a sixth harmonic has a visible influence on the CM currents for PD SPWM and MPOD SPWM, as shown in Figure 5.28 (a) as an example with PD SPWM. In this figure, $i_{CM,1}$ differs, while $i_{CM,C}$ remains unchanged. Both are comparable to the CM currents with a voltage amplitude difference, as shown in Figure 5.27 (a). With POD SVPWM, a fifth and seventh harmonic are added, and the corresponding CM currents are shown in Figure 5.28 (b). The waveforms are again comparable to those shown in Figure 5.27 (b). The sixth harmonic also leads to a similar waveform with POD SVPWM, as seen in Figure 5.28 (b). Other tested harmonics did not significantly affect the CM currents. Furthermore, adding harmonics to both AC grids results in no change to the CM currents.

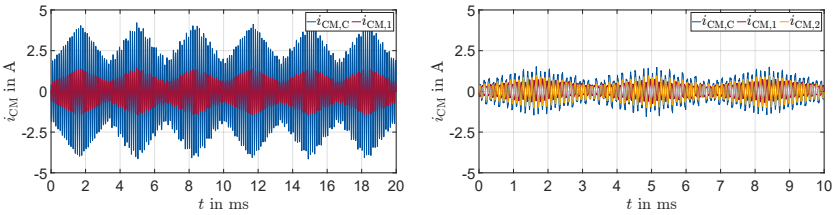
Different modulation strategies are subsequently used for the two converters. First, PD SPWM and MPOD SPWM are used for the first and second converter, respectively. This reduces the capacitive CM current $i_{CM,C}$ compared to using PD SPWM for both converters, while the CM current in the individual converter path $i_{CM,1}$ shows an increased 50 Hz component, as seen in Figure 5.29 (a). Conversely, combining PD SPWM and POD SVPWM adds a significant 150 Hz component to $i_{CM,1}$, while combining POD SVPWM and POD VSVPWM shows no low-frequency component. Therefore, combining different modulators is only feasible if their low-frequency spectra are comparable; otherwise, differences in the low-frequency spectra are present in the circulating CM current.



(a) PD and MPOD SPWM (b) PD SPWM and POD SVPWM

Figure 5.29: Simulated CM currents with different modulators applied to the two converters.

Finally, a third converter is added to the simulation model to examine the theoretical concepts discussed in Section 3.3. The third converter has the same parameters as the second converter. In particular, the CM filter and transformer stray inductance are adopted because they differ from the first converter's values. Two scenarios are examined: In the first scenario, all converters switch simultaneously using PD SPWM as the modulator. In the second scenario, the first converter switches with an opposed carrier, meaning a carrier phase shift of 0.5 for all carriers of the controller. Figure 5.30 (a) shows the simulated CM currents of the first scenario. As predicted by the model, the capacitive CM current increases by about 50 %, while the individual CM current remains mostly the same. Figure 5.30 (b) shows the second scenario, in which the capacitive CM current is significantly reduced and comparable to that measured with a single converter shown in Figure 5.9. This demonstrates that applying the same carrier phase shift to half of the converters while opposing the others can limit the capacitive CM current to that measured with a single converter. However, each



(a) Simultaneous switching (b) Opposed carriers

Figure 5.30: Simulated CM currents with three converters.

AFE installed in the DC underlay grid must have a specific carrier phase shift that must be coordinated prior to connecting a new AFE. With an even number of converters, $i_{\mathrm{CM,C}}$ can be significantly reduced, though it never completely vanishes in the simulation.

Simulating a change in switching frequency and CM filter inductance reveals no significant impact on the CM currents besides a difference due to changed impedances. Therefore, increasing the switching frequency or the CM filter inductance of one of the two converters reduces the CM currents. Additionally, changing both the current and voltage control bandwidths of one of the two converters had no effect on the CM currents.

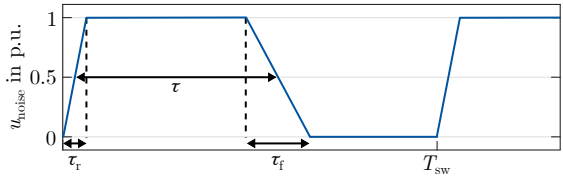
Notably, saturation of the CM chokes was not simulated but must be considered in a real setup. The CM chokes used in the experimental analysis saturate at a current of about 2 A. Therefore, a drastic increase in CM current is expected if currents of such amplitude are present in the converter path.

5.4 Electromagnetic Interference Voltages

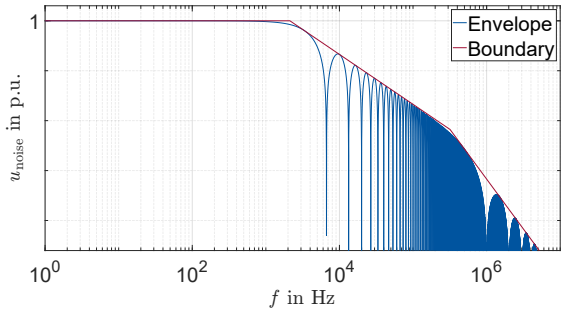
This section investigates the EMI produced by the converter in a DC underlay grid with AC-side grounding. A connection to the measured CM currents is established by analyzing the EMI voltage with different modulation strategies.

5.4.1 Introduction to Electromagnetic Interference Voltages

First, the generation of EMI voltage is examined through an analysis of the spectral components of idealized switching processes. The voltage during switching events is approximated by a periodic trapezoidal pulse train, as shown in Figure 5.31 (a) [117, 118]. In this approximation, τ_{r} and τ_{f} represent the rise and fall times of an IGBT or other power electronic switches, respectively, and τ is the width of the trapezoidal pulse, corresponding to the duty cycle when set in relation to the switching period T_{sw}. To obtain the frequency spectrum of this periodic trapezoidal pulse train, the signal undergoes a Fourier transformation. For simplicity, it is assumed that the rise and fall times are equal. Collecting the expansion coefficients for the one-sided spectrum and replacing the discrete



(a) Time domain



(b) Frequency domain

Figure 5.31: Periodic trapezoidal pulse train in time and frequency domain.

steps with a continuous envelope yields Equation 5.2 [117, 118].

$$|u_{\text{noise}}(f)| = 2A\frac{\tau}{T_{\text{sw}}} \cdot \left|\frac{\sin(\pi\tau f)}{\pi\tau f}\right| \cdot \left|\frac{\sin(\pi\tau_{\text{r}} f)}{\pi\tau_{\text{r}} f}\right| \tag{5.2}$$

Here, A is the amplitude of the signal, which relates to the DC link voltage in a real system. Figure 5.31 (b) shows this envelope with $T_{\text{sw}} = 125$ µs, $\tau = 75$ µs, and $\tau_{\text{r}} = \tau_{\text{f}} = 1$ µs. The pulse width τ corresponds to a constant duty cycle of 0.6, and the rise and fall times are relatively high for a low-voltage IGBT, allowing their influence to be seen more clearly. Furthermore, the maximum boundary is depicted, showing that the amplitude does not decrease up to a frequency of $\frac{1}{\pi \cdot \tau}$. After that, the maximum boundary decreases at a rate of -20 dB/dec up to a frequency of $\frac{1}{\pi \cdot \tau_{\text{r}}}$, at which point it begins to decrease at a rate of -40 dB/dec. This demonstrates that lower switching frequencies reduce noise because the -20 dB/dec decay begins earlier. Additionally, longer rise and fall times, meaning less steep switching slopes, are beneficial because the -40 dB/dec decay begins earlier. However, the exact spectrum of a three-phase inverter differs slightly because the duty cycle is not constant, and there are three simultaneous pulse trains with nonlinear switching slopes, overshoots

during switching, and a varying DC link voltage. Nevertheless, peaks in the spectrum are expected specifically at the switching frequency and its multiples [118]. Furthermore, ringing, which can be introduced by specific resonances triggered by the inverter, accentuates or enhances the spectral components around the ringing frequency [117].

5.4.2 Measurement Settings and Setup

A decoupling network for DC sources is built and connected according to DIN EN 61000-4-6, as shown in Figure 5.8 [37]. According to the standard, a CM choke with an inductance of 280 µH at 150 kHz and a specific minimum reactance is required. To achieve these requirements, two different toroidal cores are used; one for the lower frequency requirement and one for the high-frequency reactance, as specified in the standard [37]. The low-frequency toroidal core uses N30 ferrite material manufactured by TDK/EPCOS [119]. It has an A_L of 5.5 µH and a nominal μ_r of 4,200. Four windings around three cores should reach an inductance value of 264 µH, which was measured at 278 µH using an LCR meter at 150 kHz. Additionally, three Würth 74270191 cores made of 4W620 material with a μ_r of 620 are used for the high-frequency choke [120]. One core has an impedance of 97 Ω at 25 MHz; thus, three cores should fulfill the requirement of an impedance of 260 Ω at 24 MHz. Laboratory cables from ZES Zimmer with 4 mm plugs are used for the windings of the decoupling network. Overall, the 280 µH inductance requirement is met by combining both parts. Furthermore, multiple parallel film capacitors with a high voltage rating are used for the 47 nF decoupling capacitance. Two 22 nF and two 2.2 nF capacitors are connected in parallel to reach the desired capacitance value, which was tested with an LCR meter. The parallel connection of multiple capacitors ensures lower stray inductance and resistance in the decoupling capacitance network.

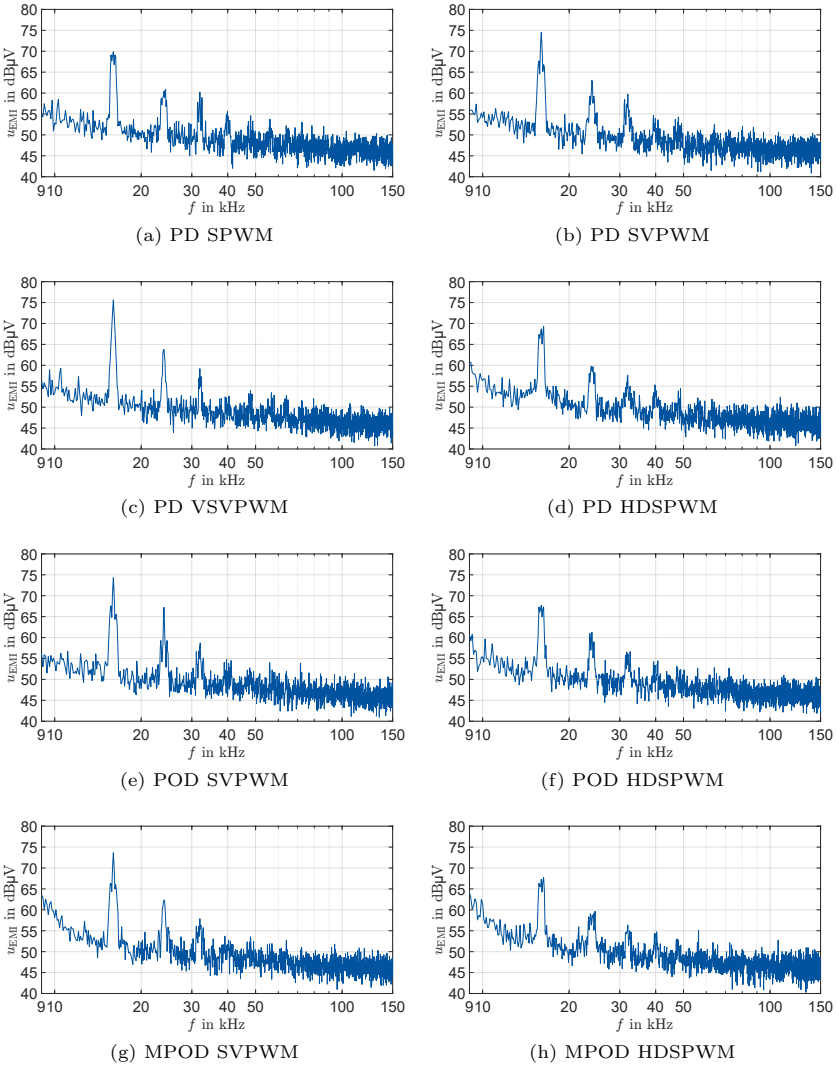
To measure EMI voltages, a 1500 Ω EMC voltage probe according to DIN EN IEC 55016-1-2 is used [34]. In this setup, a Schwarzbeck TK 9420 is installed with a frequency range of 9 kHz to 30 MHz [121]. The TK 9420 consists of a 10 nF series capacitor, which blocks low-frequency components, and two 1470 Ω and 1210 Ω series resistors. The 50 Ω input resistance of an EMI test receiver is connected in parallel to the second resistor, yielding an equivalent resistance of 1518 Ω for all components. In general, around 30 dB must be added to the measured signal to obtain the EMI voltage at the probe tip [121]. An ESL3 EMI test receiver from Rohde & Schwarz is used to capture the EMI voltages [122]. It has the necessary preprocessing units, filters, and detectors to perform measurements according to the standards [118]. A Schwarzbeck VTSD9561-D pulse

limiter is installed between the EMC voltage probe's output and the EMI test receiver's input to protect the receiver's inputs against possible overvoltages [123]. Additionally, the pulse limiter introduces 20 dB of damping to the measured signal, which must be added back in. To power the EMI test receiver, a single-phase isolation transformer is used, with the ground pin connected to the star point of the three-phase transformer. This ensures correct return paths, as the star point is the reference point in all measurements. Otherwise, the Bayonet Neill-Concelman (BNC) connector of the EMC voltage probe would connect the reference point to ground through the ground pin of the EMI test receiver. This is not desirable in this setup, as it could create additional current paths and influencing factors. Unlike the setups proposed in the standards, this setup does not use ground planes, which could alter the measured values compared to compliance measurements. However, ground planes are unnecessary for comparative measurements regarding the influence of different modulation strategies and the addition of a second converter.

Conducted EMI voltage measurements are performed using the test receiver settings introduced in Table 2.2 and the peak detector. The values from the calibration documents were used for the attenuation of the EMC voltage probe and the pulse limiter across the entire frequency range. Three consecutive measurement series are performed across the entire frequency spectrum, from 9 kHz to 30 MHz, for each configuration. Only the peak values at each frequency are stored. This reduces noise and measurement uncertainties compared to a single measurement.

5.4.3 Measurement Results

EMI voltage measurements are performed using the settings previously introduced, starting with one converter, according to the setup presented in Figure 5.8. Figure 5.32 shows the measured EMI voltages within the frequency band from 9 kHz to 150 kHz. First, the measurements with PD are analyzed and displayed in Figure 5.32 (a) through (d). The switching frequency f_{sw} is not visible in the measured frequency spectrum; however, distinct peaks are visible at its multiples with decreasing amplitude for all modulators. SVPWM and VSVPWM, in particular, show dominant peaks that are up to 5 dBµV higher than those of SPWM and HDSPWM. HDSPWM has the lowest peaks, with a more widespread spectrum around the multiples of f_{sw}. This is also evident in the higher values between 9 kHz and 10 kHz, which are sidebands around the switching frequency. As expected, no resonant or switching behavior peaks are visible in any measurement in this frequency band because they usually occur



(a) PD SPWM

(b) PD SVPWM

(c) PD VSVPWM

(d) PD HDSPWM

(e) POD SVPWM

(f) POD HDSPWM

(g) MPOD SVPWM

(h) MPOD HDSPWM

Figure 5.32: EMI spectrum between 9 kHz and 150 kHz with different modulators.

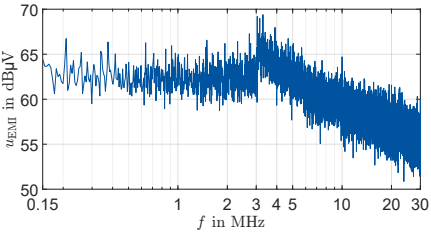
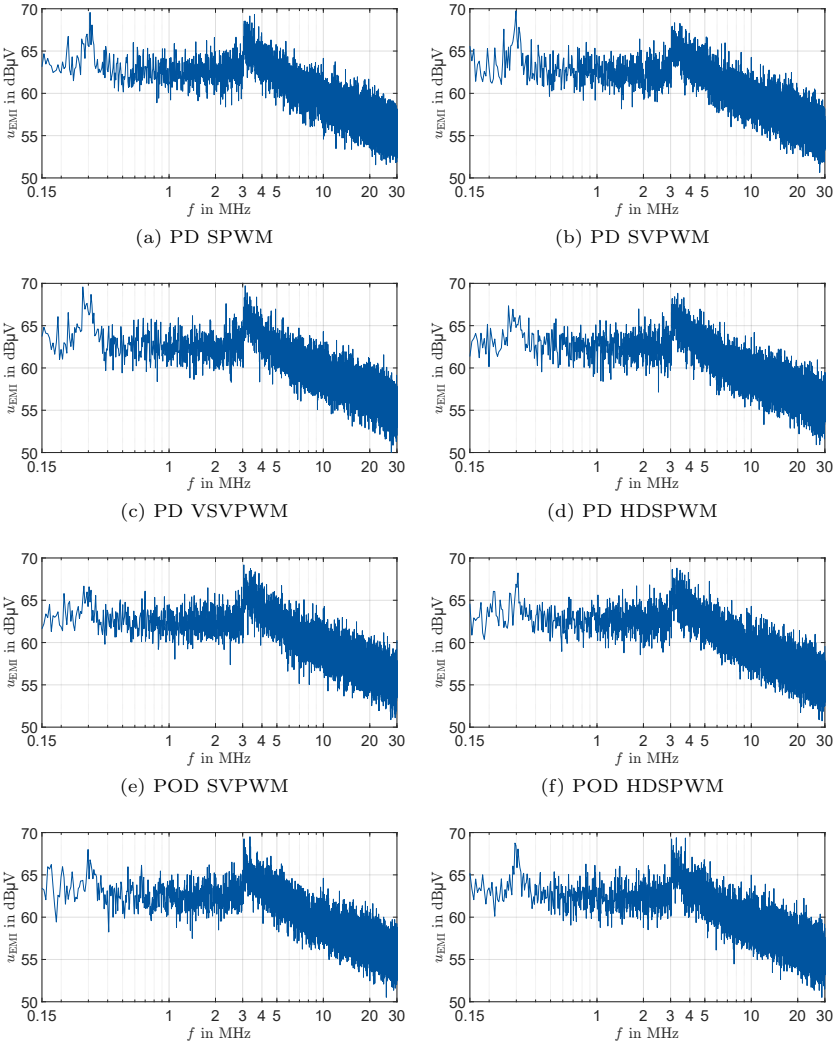


Figure 5.33: EMI spectrum with converter turned off between 150 kHz and 30 MHz.

at higher frequencies. The POD spectrum does not change significantly, as seen in Figure 5.32 (e) and (f). Only slightly lower peaks are visible for HDSPWM. This is even more pronounced with MPOD, as the peaks are slightly reduced for almost all modulators, especially HDSPWM, as shown in Figures 5.32 (g) and (h). However, the spectra are more widespread, as shown by the increased values at frequencies below 16 kHz and around the multiples of f_{sw}. There are no significant differences when adding a 15 kW load to the system with the decoupled DC source. The corresponding measured spectra for SPWM with PD, POD, and MPOD can be found in Appendix A.4. The remaining POD and MPOD measurements that are not shown here can also be found in Appendix A.4.

The frequency band from 150 kHz to 30 MHz is now being investigated. To this end, a measurement was first carried out with the converter turned off, as shown in Figure 5.33. A high amount of noise is evident, especially for frequencies above 3 MHz, where a peak in the EMI voltage is followed by damping. This suggests that frequencies in this range cannot be properly measured with the given setup. This may also explain why VDE SPEC 90037 only recommends it for the frequency band from 9 kHz to 150 kHz [24]. Overall, the measured values are higher than those of the first frequency band because the EMI test receiver settings differ between the measurements. Nevertheless, the EMI voltages measured with different modulators are shown in Figure 5.34. While the higher frequencies show no significant differences between the modulators, a distinct peak appears around 300 kHz. This peak is caused by the resonance frequency of the CM choke parallel capacitance and the DM filter inductance, as discussed earlier in the analysis of CM currents in Section 5.2.1. Since this resonance is visible not only in the CM currents, but also in the CMV, it appears as a peak in the EMI spectrum. The peak is the lowest with PD and HDSPWM. However, POD significantly reduces the peak with SVPWM, see Figure 5.34 (e), and VSVPWM, shown in Appendix A.4. Conversely, POD and MPOD seem



(a) PD SPWM

(b) PD SVPWM

(c) PD VSVPWM

(d) PD HDSPWM

(e) POD SVPWM

(f) POD HDSPWM

(g) MPOD SVPWM

(h) MPOD HDSPWM

Figure 5.34: EMI spectrum with different modulators between 150 kHz and 30 MHz.

to intensify the peak for HDSPWM, though no significant differences are visible for SPWM. MPOD reduces the peak value for SVPWM but increases it for VSVPWM, though their behavior was comparable in most other cases.

Analyzing the spectra at around 2 MHz shows no signs of the second resonance, where the impedance magnitude of the CM choke is minimal. However, it is unclear whether this is due to the high noise and likely low sensitivity of the measurement setup at higher frequencies or whether the amplitude is too low, as the oscillations were barely visible in the CMV and CM current measurements. Furthermore, adding a 15 kW load, shown in Appendix A.4, only slightly reduces the peak at around 300 kHz and otherwise has no significant influence on the measured EMI spectrum between 150 kHz and 30 MHz. The remaining POD and MPOD measurements, which are not shown here, can also be found in Appendix A.4.

The same measurements are performed with two converters, according to the setup presented in Figure 5.17. The measurements show a very comparable behavior to those with one converter, as seen in Appendix A.4. Therefore, increased EMI voltages are not expected when multiple converters supply a DC underlay grid with AC-side grounding. However, measuring at a different point in the DC underlay grid may produce different results due to the increased influence of multiple converters. The measured EMI spectrum would change especially if the second converter had different parameters, such as a higher or lower switching frequency, or significantly different passive components.

In summary, the EMI measurements are connected to the previous CM current and CMV measurements. First, the peaks in the frequency spectra correspond to each other. On the other hand, the influence of using different carrier configurations is less pronounced in the EMI voltage spectrum than in the CM current and CMV measurements. EMI voltage amplitudes were more influenced by modulation wave adaptions of different modulators than by carrier configurations PD, POD, or MPOD. Overall, the modulation strategy and system parameters, such as filter inductances and parasitic values, significantly impact both CM currents and EMI voltages.

5.5 Summary

This chapter presents experimental analyses of CM currents in LV DC underlay grids with AC-side grounding. First, it discusses the synchronization of locally

distributed converters using GNSS. A low-cost solution using a u-blox MAX-M10S is investigated, showing delay times between two receivers ranging from 6 ns to 22 ns. It is demonstrated that a much higher delay of several microseconds would be tolerable in the given setup without significantly increasing CM currents. Measuring the circulating CM currents between two synchronized and unsynchronized converters shows a reduction of up to 82.3 %. Additionally, the study demonstrates that unequal DC voltage measurements are responsible for low-frequency harmonics in the CM currents. The results indicate that the circulating CM currents between two converters can be minimized through synchronized switching. Therefore, these CM current components can be assumed negligible in the following measurements.

Next, the capacitive CM currents are investigated by adding CM capacitors close to the DC load. Specific high-frequency current components at approximately 300 kHz and 2 MHz are identified in the measurements. These result from the resonance of the CM choke's parallel capacitance with the DM filter inductance and an impedance minimum of the CM choke. Additionally, MPOD significantly reduces CM currents with all modulators. POD significantly reduces the CM currents with SVPWM and VSVPWM as well. However, HDSPWM does not result in the expected reduction due to significant frequency components of the discontinuous PWM at the resonance frequency of the CM inductance and capacitance. Similar results are obtained with two converters, where MPOD again reduces the CM currents the most. The differences in the CMV frequency spectra are significant when the system changes, such as with different impedance curves of systems with one and two converters.

Furthermore, reducing the CM capacitance creates a resonance point slightly above the switching frequency, excited by all modulation strategies. Only MPOD with SPWM is able to not saturate the CM choke, resulting in stable operation with increased CM currents compared to the measurements with higher CM capacitance. In general, although the CM currents can be significantly reduced by switching simultaneously, the resonance point should remain below the switching frequency, which is almost always the case in a real system.

Overall, the measurements validate the CM model and the CM choke design guide. The limit of 600 mA was complied with using the three-step CMV modulators SPWM, SVPWM, and HDSPWM in combination with PD. Although the measured CM currents with two converters are higher, the capacitive CM current is expected to split evenly between them, staying below the limit. Additionally, MPOD with SPWM results in the lowest CM currents apart from POD VSVPWM, which exhibited poor current quality and erratic behavior. Overall, these results align with the CMV measurements from Section 3.5. In summary,

CM currents can be significantly reduced by synchronized switching and modulator choice, making the AC-side grounded DC grid viable even without large CM filters.

Next, a simulation model is developed to expand upon the measured results, as the measurement setup is limited in parameter variation. First, the measured and simulated CM currents are compared with different modulators to validate the simulation model. While the simulated currents are slightly lower, their general behavior is similar.

The simulations show significant current increases for different parameter variations when SVPWM or VSVPWM are used. For instance, a substantial low-frequency CM current flows between the converters when the AC distribution grid phases are shifted by 60°. Additionally, combining SPWM with SVPWM or VSVPWM adds a significant 150 Hz component.

The simulation of three converters confirms the analytical considerations from Section 3.3. As expected, the capacitive CM currents can be significantly reduced by opposing carriers of specific converters.

In summary, the simulations show that the system is very complex and that many factors influence the CM currents. However, a DC underlay grid with AC-side grounding is feasible with proper system design. Using a modulator with low frequency components across the entire frequency spectrum, such as MPOD SPWM, is beneficial for preventing the occurrence of low-frequency harmonics or the excitation of resonance frequencies. Additionally, extending the DC underlay grid with more converters is possible without exceeding certain CM current limits if opposed carriers are used for half of the converters. In principle, any modulation strategy or parameter variation that is not feasible in this analysis can be used, provided that the CM choke is designed accordingly.

Lastly, the origin of EMI in converter systems is briefly introduced and the contributing parameters are identified: switching frequency, duty cycle, and rise and fall times. EMI measurements are performed using an EMI voltage probe and an EMI test receiver according to relevant standards. The measurement results show the expected peaks at multiples of the switching frequency, which is just outside the measured spectrum itself. Notable differences appear when adapting the modulation wave, but not when changing the carrier configuration. Specifically, SPWM and HDSPWM exhibit lower peaks between 9 kHz and 150 kHz. Above 150 kHz, however, the measurement setup is not suitable because it shows a lot of noise. Only the peaks at approximately 300 kHz are visible, and they exhibit slightly different behavior with different modulators. Adding a second

converter does not significantly affect the measured EMI voltages at the investigated measurement point.

In general, this measurement setup is applicable for the frequency range of 9 kHz to 150 kHz, and it can identify differences between modulation strategies. However, a different measurement setup would be necessary for higher frequencies. Unlike CM currents, there are no significant differences between PD, POD, and MPOD visible, probably because they influence the switching sequence rather than the duty cycle. The duty cycle was one of the initially identified factors influencing EMI voltage. Overall, the measured EMI voltages are well below the limits established in Section 2.1. However, the measurement setup differs slightly from the standards. Additionally, the CM choke is designed to suppress CM currents and has a large CM inductance, which reduces EMI voltages as well. Therefore, EMI should not be an issue in AC-side grounded DC grids.

6 Conclusions and Outlook

This thesis investigates CM currents in DC underlay grids with AC-side grounding. A CM model is derived and used to determine ways to reduce CM currents. The CM choke, the primary component of a CM filter, is designed using the model to limit the CM currents to specified values. Next, two additional methods are identified: synchronizing the switching of converters and using reduced CMV modulators. Experiments on a test bench resembling a two-terminal DC underlay grid with AC-side grounding are conducted to investigate and validate novel concepts to achieve both. Finally, EMI is examined, because previous studies identified it as a possible challenge for AC-side grounded DC grids. Overall, the experiments show that a DC underlay grid with AC-side grounding is a viable solution, if the system is properly designed.

Modeling Common-Mode Currents and Common-Mode Choke Design

A simplified CM model is derived for two converters using their switching states. Two primary CM currents are identified: a circulating CM current between the two converters through the DC grid, and a capacitive CM current through the CM capacitances in the DC grid. The circulating CM current is excited by the difference in the CMVs of both converters. Conversely, the capacitive CM current is determined by the sum of the CMVs of both converters. The model shows that the timing of the switching signals and the converters' CMV primarily influence the CM currents. This is especially important for more than two converters because small deviations can lead to CM currents in all converter paths.

For all CM currents and systems, CM chokes increase the time constants and reduce high-frequency components. Therefore, equations are derived using the CM model to limit CM currents to a specific RMS value, which leads to a design guideline. Two CM chokes are built according to the design guideline, which validates the inductance calculation. These chokes are then used in an

experimental analysis, which validates their ability to limit CM currents to the specified value.

Converter Synchronization Using the Global Navigation Satellite System

To time the switching actions so that the converters either switch simultaneously or in opposition, it is necessary to synchronize locally distributed converters. GNSS time signals are already used for distributed measurement units to create a common time base. It is investigated here whether the accuracy of GNSS is sufficient for synchronizing multiple converters, given that the short time constants require strict and accurate timing. An initial analysis reveals a delay of a few nanoseconds between two low-cost GNSS receivers. During experimental validations with two converters, one measurement is performed with synchronization and one without, reducing the RMS values of CM currents by up to 82.3 %. Additionally, it is shown that synchronization accurate to a few microseconds would suffice. In conclusion, GNSS is a viable, low-cost method for synchronizing locally distributed converters with high accuracy. This method could be used in other converter applications where the given accuracy is sufficient.

Reduced Common-Mode Voltage Modulation of Three-Level Inverters

Reducing a converter's CMV is of interest in several applications. In DC underlay grids with AC-side grounding, the sum or difference of converters' CMVs is responsible for the CM currents. Thus, two methods are proposed for reducing the CMV of a three-phase three-level inverter.

The first method modifies the modulation wave so that the middle phase is always clamped to the NP, which limits the CMV to $\pm 1/6 \cdot U_{\mathrm{DC}}$. However, this significantly restricts the converter's linear modulation range, reducing it from 1.0 for SPWM to 0.67. Therefore, the discontinuous PWM is combined with SPWM to increase the linear modulation range back to 1, creating the hybrid modulation scheme HDSPWM. Comparing the CMV of the new modulation scheme to SPWM decreases the CMV RMS value by 4.1 % at the given operating point. Clearly, a different operating point with a lower modulation index would reduce the CMV further. However, this is not feasible for the given application.

Additionally, HDSPWM results in higher CM currents than expected because specific resonance points are excited by the discontinuous PWM. Regardless of carrier configuration, operation without CM choke saturation was not possible with two converters using HDSPWM.

The second method uses a carrier configuration that is different from that of PD and POD. It is known that POD limits the CMV to $\pm 1/6 \cdot U_{\mathrm{DC}}$ by opposing the bottom carrier of each phase. However, the novel MPOD opposes both carriers of the middle phase, thereby limiting the CMV to $\pm 1/6 \cdot U_{\mathrm{DC}}$. Comparing the CMV with MPOD to that with POD yields a significant reduction of more than 40 % for SPWM and HDSPWM and similar values for SVPWM and VSVPWM. However, combining POD with VSVPWM resulted in poor output current behavior when evaluating modulation strategies and is therefore not recommended. Additionally, MPOD produced the lowest CM currents with all modulators. Compared to PD, an RMS value reduction of over 55 % is achieved, which mostly aligns with the CMV reduction.

Electromagnetic Interference Voltage in DC Underlay Grids with AC-Side Grounding

VDE SPEC 90037 identifies EMI as one of the challenges of DC grids with AC-side grounding. An EMI voltage probe that meets various standards is used to measure conducted EMI voltages using different modulation strategies with one or two converters. Significant differences are visible between SPWM, SVPWM, VSVPWM, and HDSPWM in the frequency band from 9 kHz to 150 kHz. Conversely, the different carrier configurations did not exhibit significant differences, unlike for the CM current measurements. Overall, SPWM and HDSPWM exhibit the lowest peaks at multiples of the switching frequency; however, all modulators are below the standards' limit values. Yet, significant noise in the test setup limits the usefulness of the measurements for frequencies above 2 MHz. In the frequency band from 150 kHz to 2 MHz, only one meaningful peak is visible at around 300 kHz. There, the resonance point formed by the CM choke parasitic capacitance and the DM filter inductance is located.

Outlook

This section provides an overview of additional investigations that can be conducted in the future.

The CM current modeling can be improved in several ways to more accurately resemble the real system. First, the lumped capacitance can be replaced with distributed capacitors. One option is to use a more detailed cable model that includes cable capacitances or use distributed DC loads with EMI filter capacitors. More parasitic elements, such as the parallel capacitance of the CM and DM inductors, can be included to model additional resonance points. However, each addition increases the model's complexity and may not be necessary for understanding specific phenomena.

CM filters consist of one or more CM chokes combined with capacitors, and sometimes, resistors. This work's CM choke design guideline only focuses on one of these components. To achieve a holistic filter design, the additional components should be included. This could reduce the necessary CM inductance for a specific filtering effect. Additionally, active filters, which include active elements that enhance the filter impedance at specific frequencies, can reduce filter size [124–128]. Active filters could be particularly helpful in the given application, as they can increase the impedance at the switching frequency and its multiples, thereby reducing high-frequency CM current components. However, active filters could introduce additional frequencies that could excite resonance points or add EMI voltage, so they should be thoroughly designed.

The experimental analyses performed here are limited to one system. Although simulations extend these analyses, additional experiments could validate the system. In particular, it would be beneficial to conduct tests using converters at real distribution grid transformers to form a DC underlay grid in order to investigate a larger, more realistic system. In this case, real loads and RESs could be connected to the DC grid instead of a laboratory source, resulting in additional CM current paths.

For the given application, the novel modulator HDSPWM and carrier configuration MPOD were proposed and investigated. However, reducing CMV and CM currents is beneficial in other applications, such as PV systems and drives. In these applications, the converters operate at different operating points, which could lead to different results. The modulation index has a particularly pronounced impact with HDSPWM. Additionally, HDSVPWM can be implemented to increase the modulation index, which is beneficial for drive applications. Fur-

thermore, the presented modulators can be compared to other modulation strategies.

Finally, improvements can be made to the EMI measurement setup. While the given setup could highlight differences between various modulators, the applicable frequency range was limited by noise. Additionally, some aspects of the standards were not implemented, such as ground planes at predefined distances. With these improvements, the EMI measurements can be repeated in accordance with the standards. Furthermore, measuring at different points in the DC underlay grid could reveal a more significant impact of the carrier configuration or a second converter in the system.

A Appendix

A.1 Differential Equation for Common-Mode Currents

Figure A.1 shows the circuit which is used to derive the equation for calculating the CM current in the single-phase model. L_{tot} and u_{tot} are used, which can be calculated according to Equations 3.1 and 3.2, respectively.

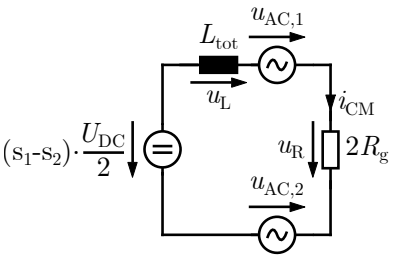


Figure A.1: Equivalent circuit for calculating the CM current.

Kirchhoff's loop rule is applied to the circuit:

$$\begin{aligned} & (s_1 - s_2) \cdot \tfrac{U_{\mathrm{DC}}}{2} + u_{\mathrm{AC,2}} - u_{\mathrm{AC,1}} = u_{\mathrm{tot}} = u_{\mathrm{L}}(t) + u_{\mathrm{R}}(t) \\ \Leftrightarrow \quad & u_{\mathrm{R}}(t) = u_{\mathrm{tot}} - u_{\mathrm{L}}(t) \\ \Leftrightarrow \quad & i_{\mathrm{CM}}(t) \cdot 2R_{\mathrm{g}} = u_{\mathrm{tot}} - L_{\mathrm{tot}} \cdot \tfrac{\mathrm{d}i_{\mathrm{CM}}(t)}{\mathrm{d}t} \\ \Leftrightarrow \quad & i_{\mathrm{CM}}(t) + \tfrac{L_{\mathrm{tot}}}{2R_{\mathrm{g}}} \cdot \tfrac{\mathrm{d}i_{\mathrm{CM}}(t)}{\mathrm{d}t} = \tfrac{u_{\mathrm{tot}}}{2R_{\mathrm{g}}}. \end{aligned} \tag{A.1}$$

Use initial and final value method for solving differential equations of an arbitrary function f depending on x:

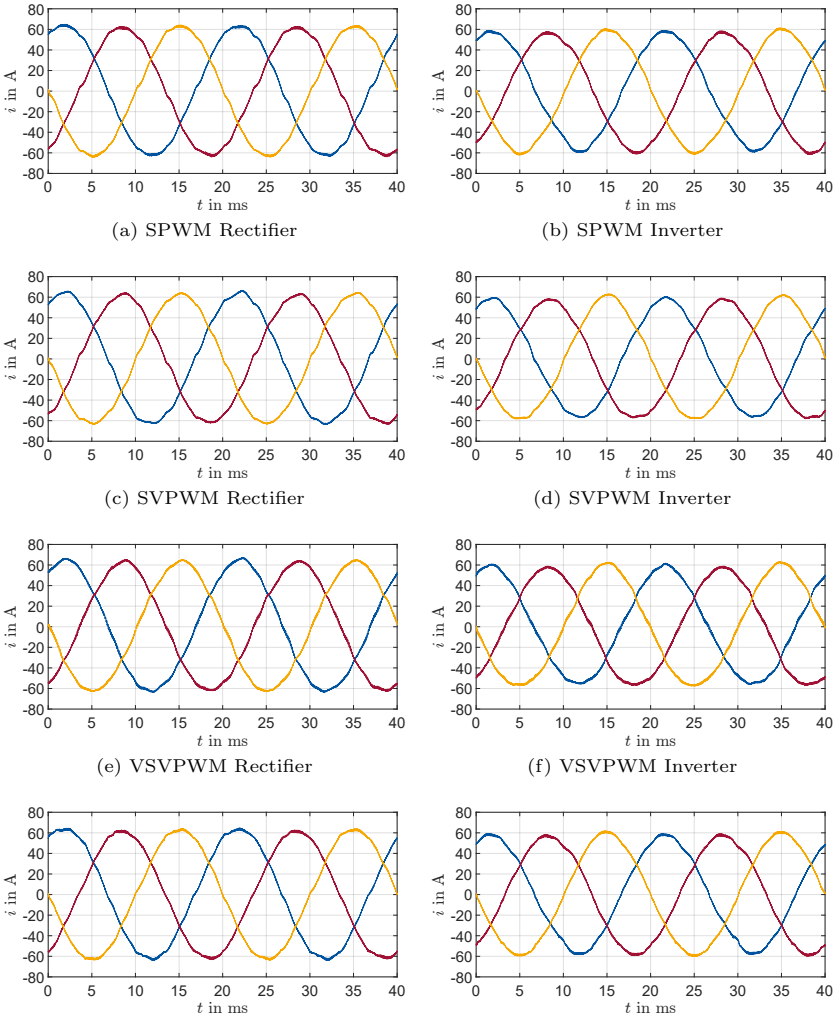
$$f(x) = (f(0) - f(\infty)) \cdot \mathrm{e}^{-\frac{t}{\tau}} + f(\infty). \tag{A.2}$$

Applied to the given differential equation yields:

$$i_{\mathrm{CM}}(t) = \left(i_{\mathrm{CM}}(0) - \frac{u_{\mathrm{tot}}}{2R_{\mathrm{g}}} \right) \cdot \mathrm{e}^{-\frac{2R_{\mathrm{g}}}{L_{\mathrm{tot}}} \cdot t} + \frac{u_{\mathrm{tot}}}{2R_{\mathrm{g}}}. \tag{A.3}$$

A.2 Modulator Evaluation Measurements

This section provides the remaining measurements and frequency spectra not shown in Section 4.4.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

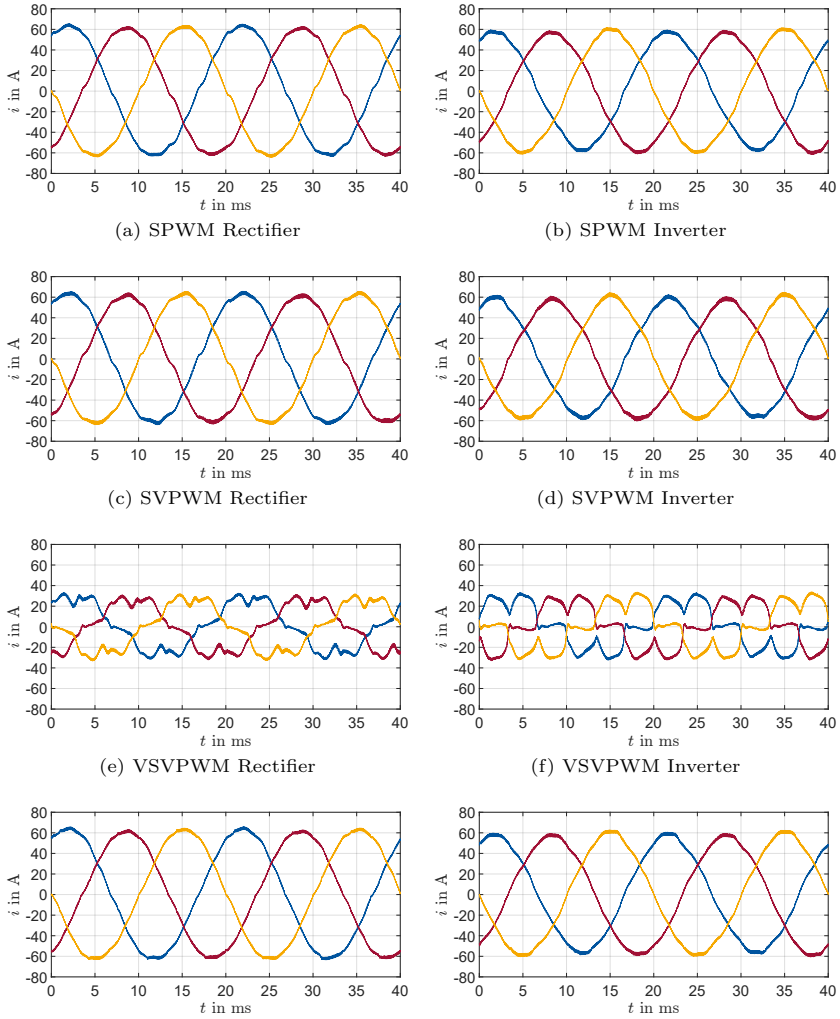
(e) VSVPWM Rectifier

(f) VSVPWM Inverter

(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.2: Output currents with different modulators and PD.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

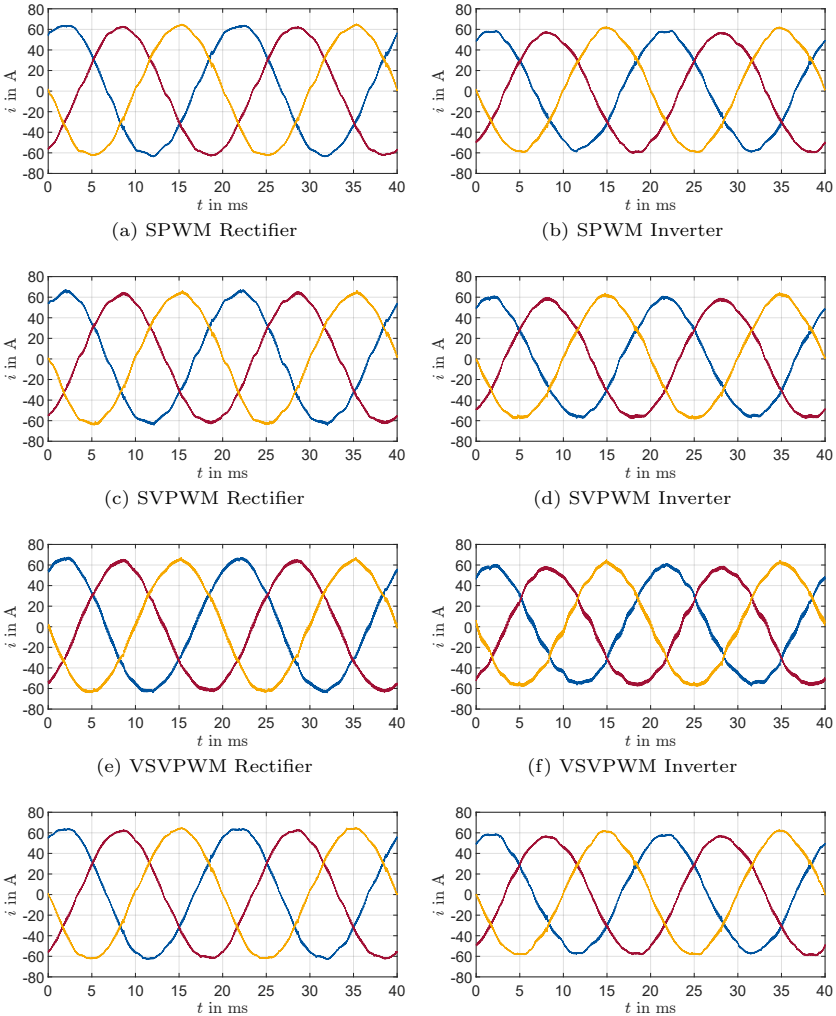
(e) VSVPWM Rectifier

(f) VSVPWM Inverter

(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.3: Output currents with different modulators and POD.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

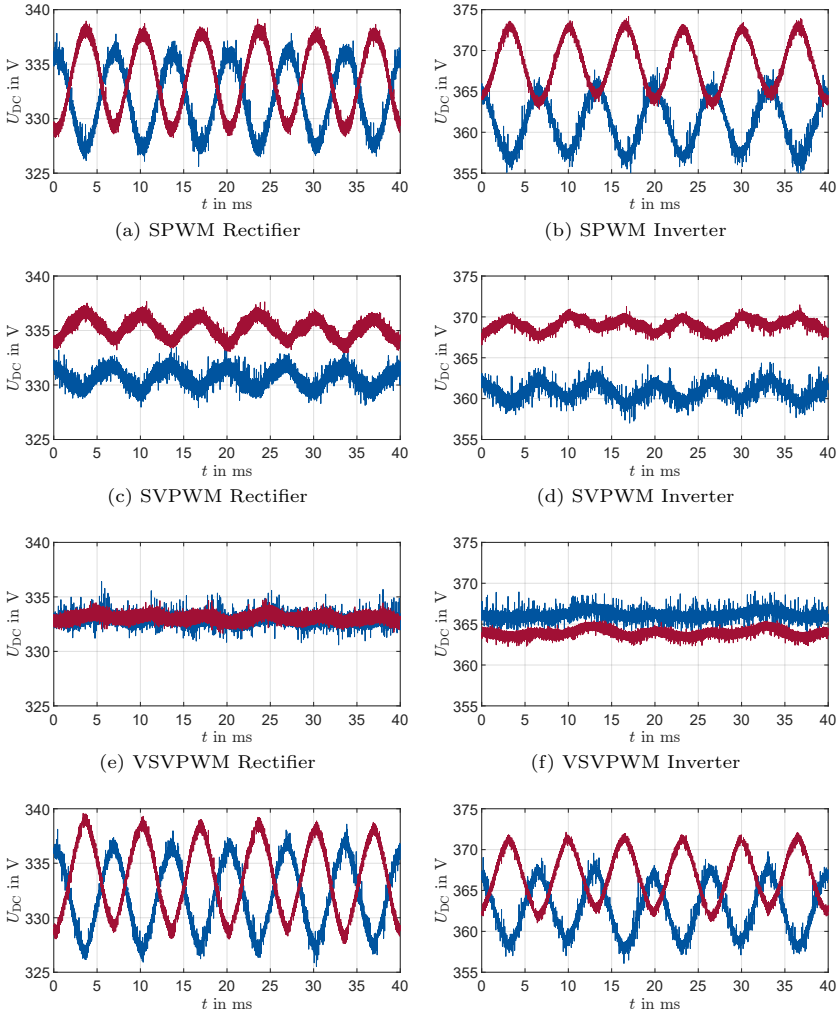
(e) VSVPWM Rectifier

(f) VSVPWM Inverter

(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.4: Output currents with different modulators and MPOD.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

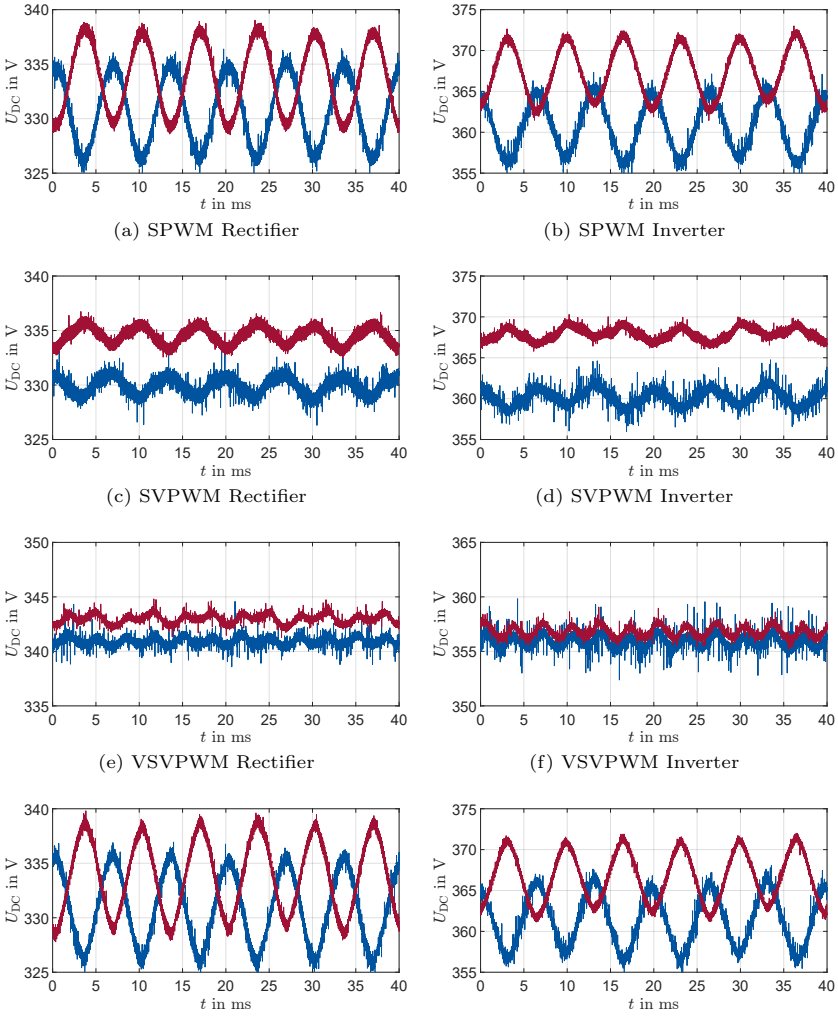
(e) VSVPWM Rectifier

(f) VSVPWM Inverter

(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.5: DC link voltages with different modulators and PD.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

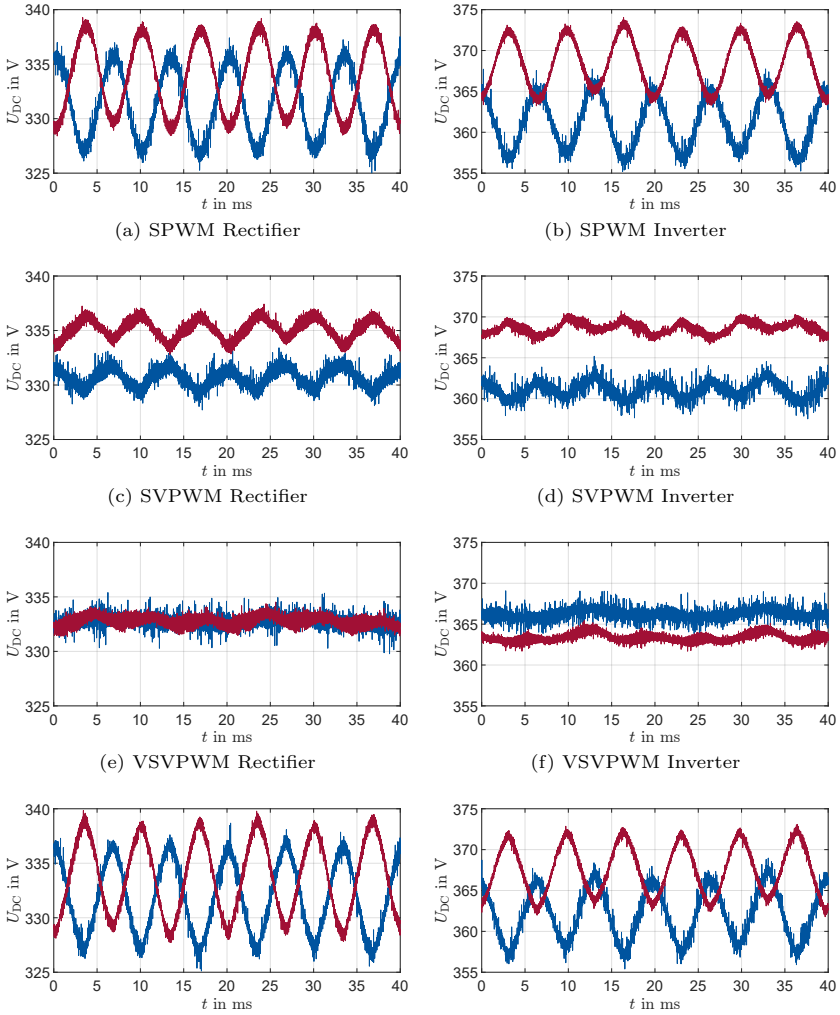
(e) VSVPWM Rectifier

(f) VSVPWM Inverter

(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.6: DC link voltages with different modulators and POD.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

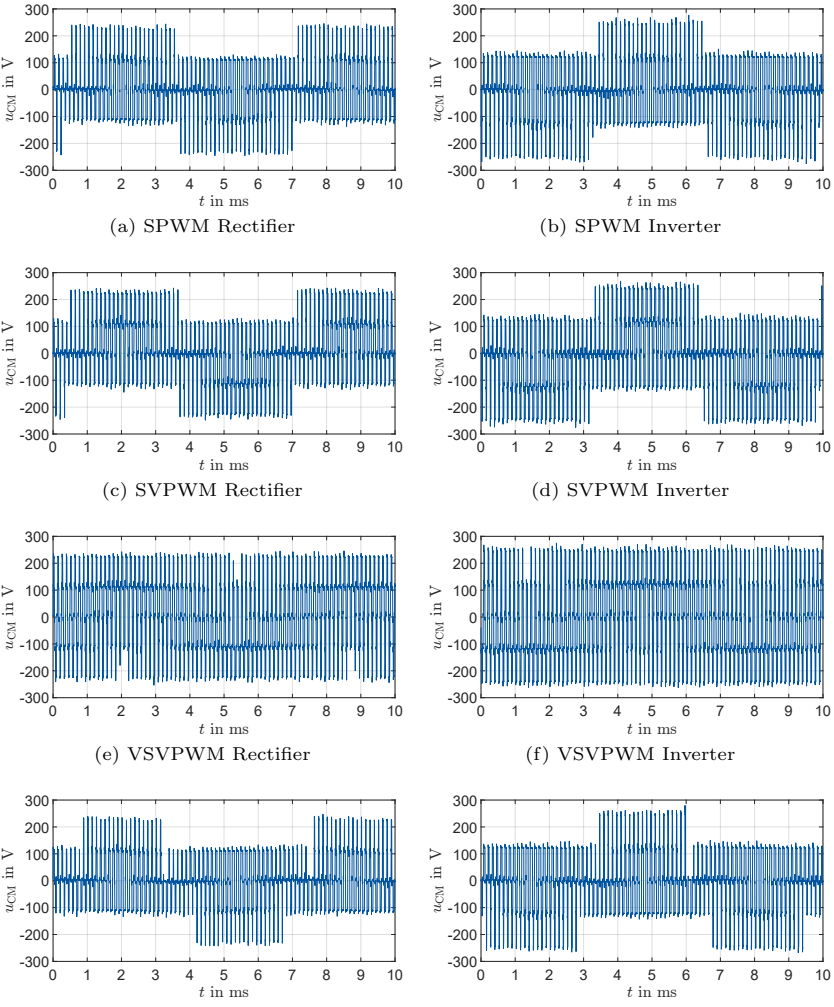
(e) VSVPWM Rectifier

(f) VSVPWM Inverter

(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.7: DC link voltages with different modulators and MPOD.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

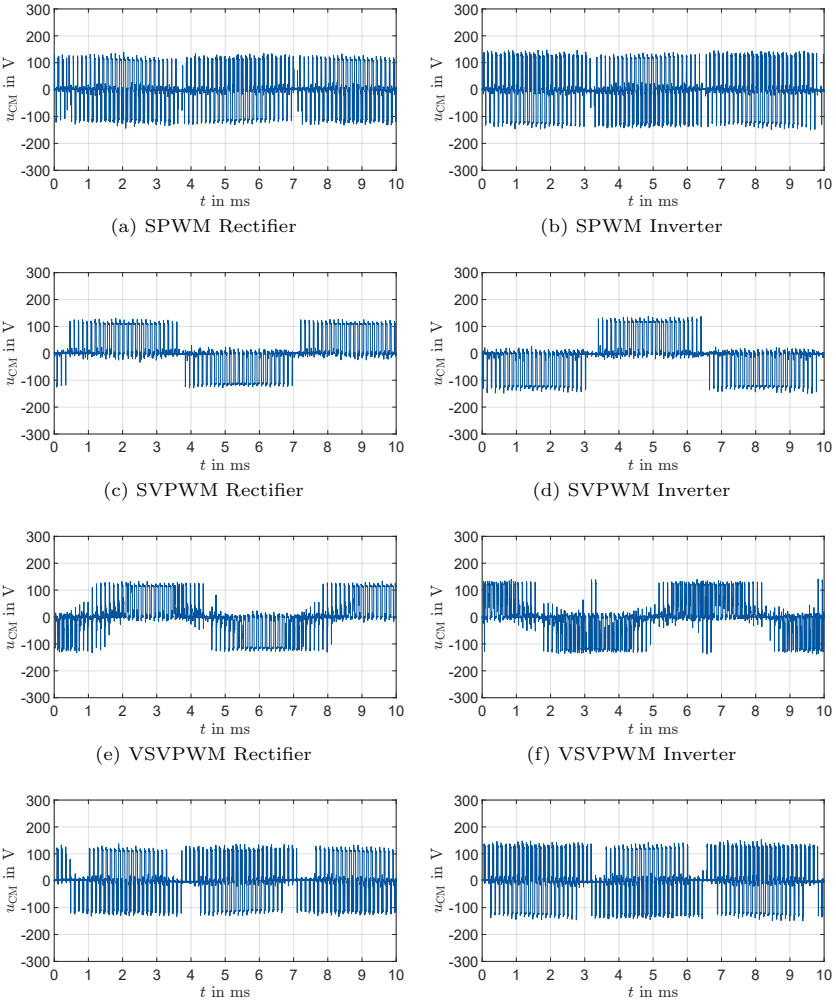
(e) VSVPWM Rectifier

(f) VSVPWM Inverter

(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.8: CMV with different modulators and PD.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

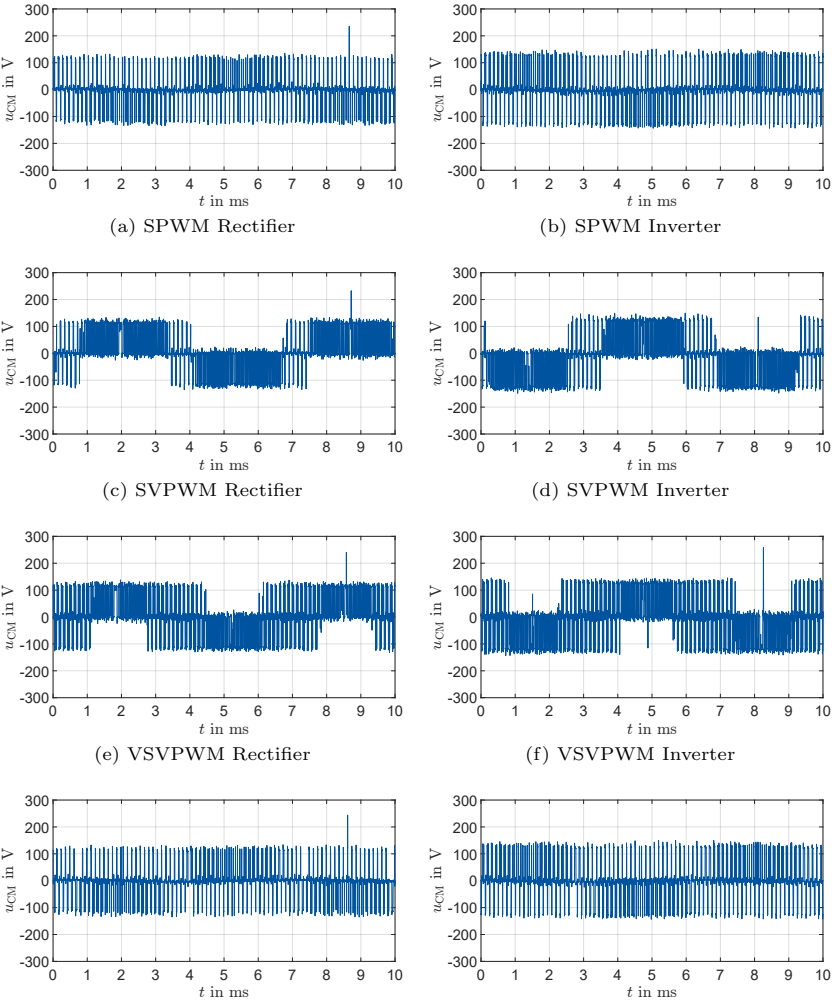
(e) VSVPWM Rectifier

(f) VSVPWM Inverter

(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.9: CMV with different modulators and POD.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

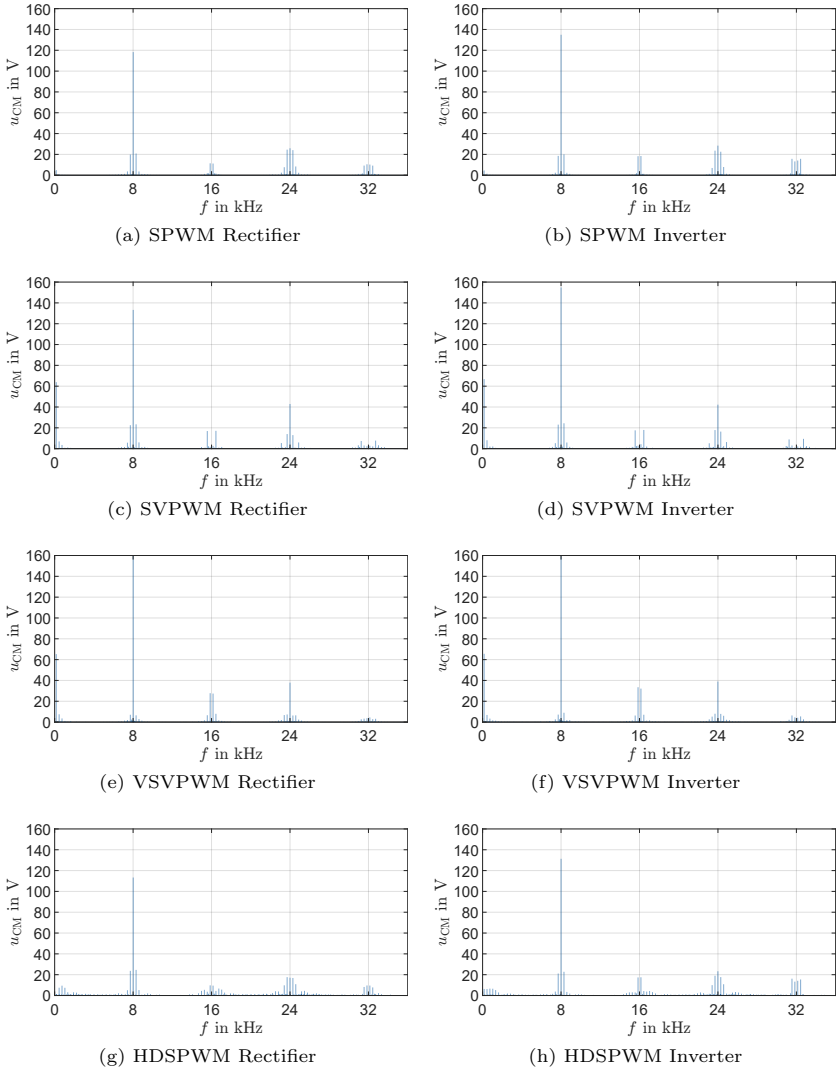
(e) VSVPWM Rectifier

(f) VSVPWM Inverter

(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.10: CMV with different modulators and MPOD.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

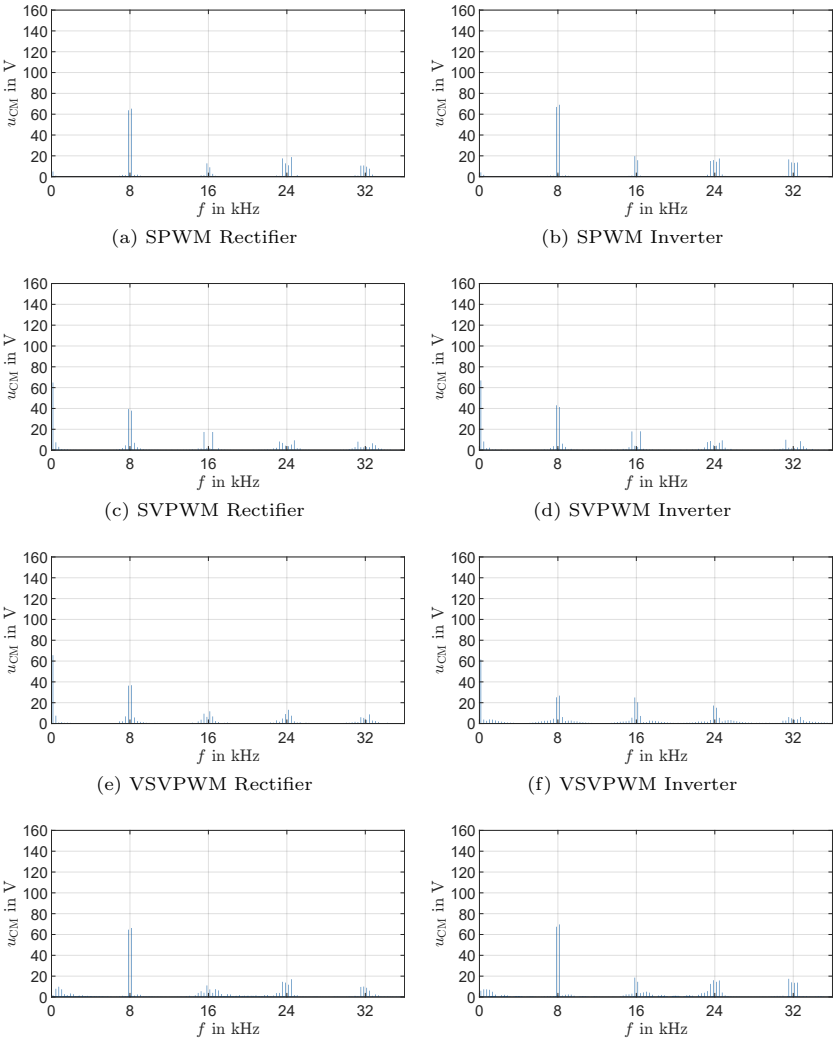
(e) VSVPWM Rectifier

(f) VSVPWM Inverter

(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.11: Frequency spectrum of CMV with different modulators and PD.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

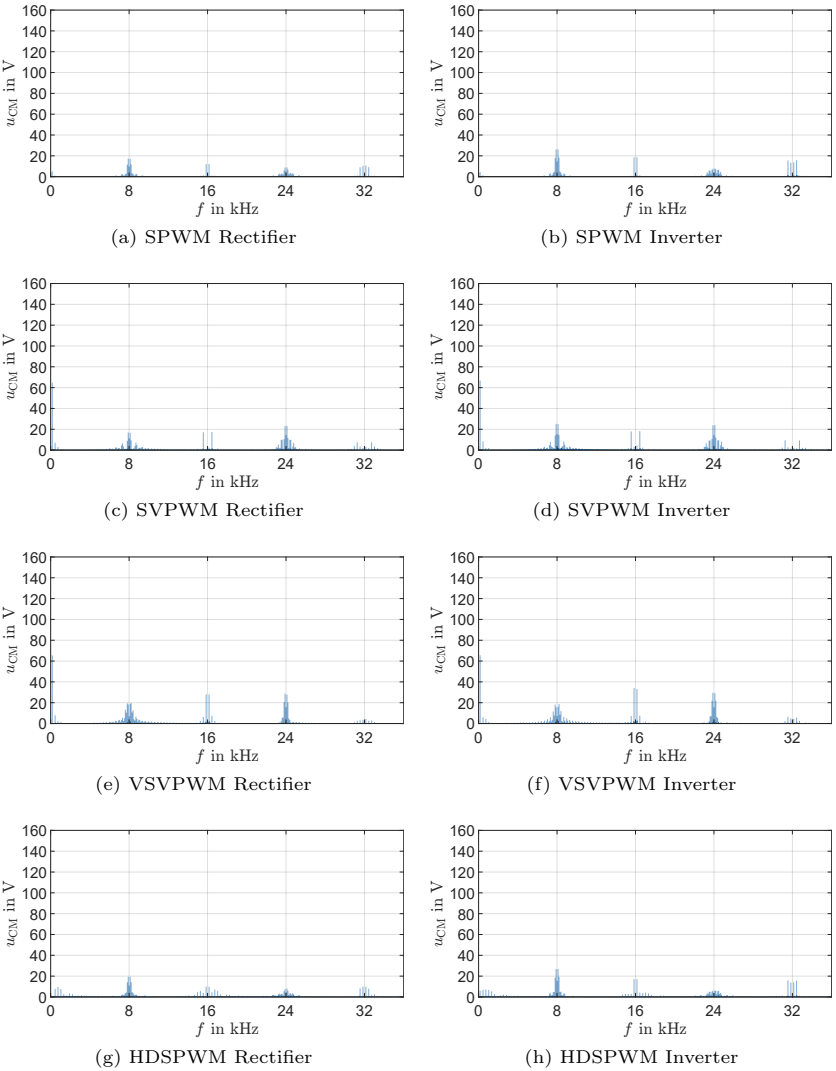
(e) VSVPWM Rectifier

(f) VSVPWM Inverter

(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.12: Frequency spectrum of CMV with different modulators and POD.



(a) SPWM Rectifier

(b) SPWM Inverter

(c) SVPWM Rectifier

(d) SVPWM Inverter

(e) VSVPWM Rectifier

(f) VSVPWM Inverter

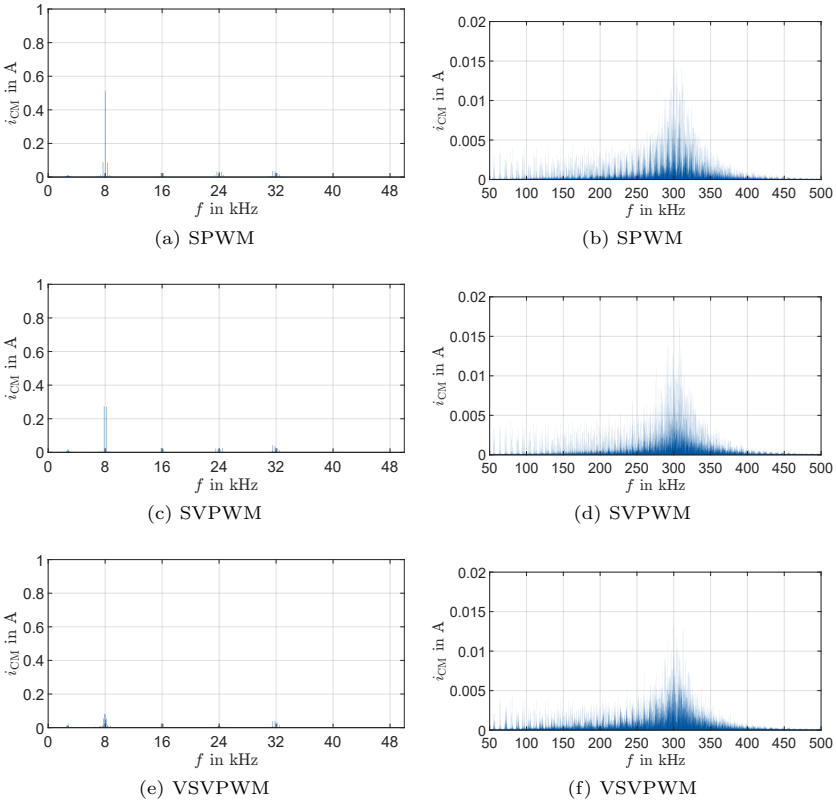
(g) HDSPWM Rectifier

(h) HDSPWM Inverter

Figure A.13: Frequency spectrum of CMV with different modulators and MPOD.

A.3 Frequency Spectra of Common-Mode Current Measurements

This section provides the remaining frequency spectra of the measured CM currents not shown in Section 5.2.



(a) SPWM (b) SPWM

(c) SVPWM (d) SVPWM

(e) VSVPWM (f) VSVPWM

Figure A.14: Frequency spectrum of CM currents with different modulators with one converter and 15 kW load.

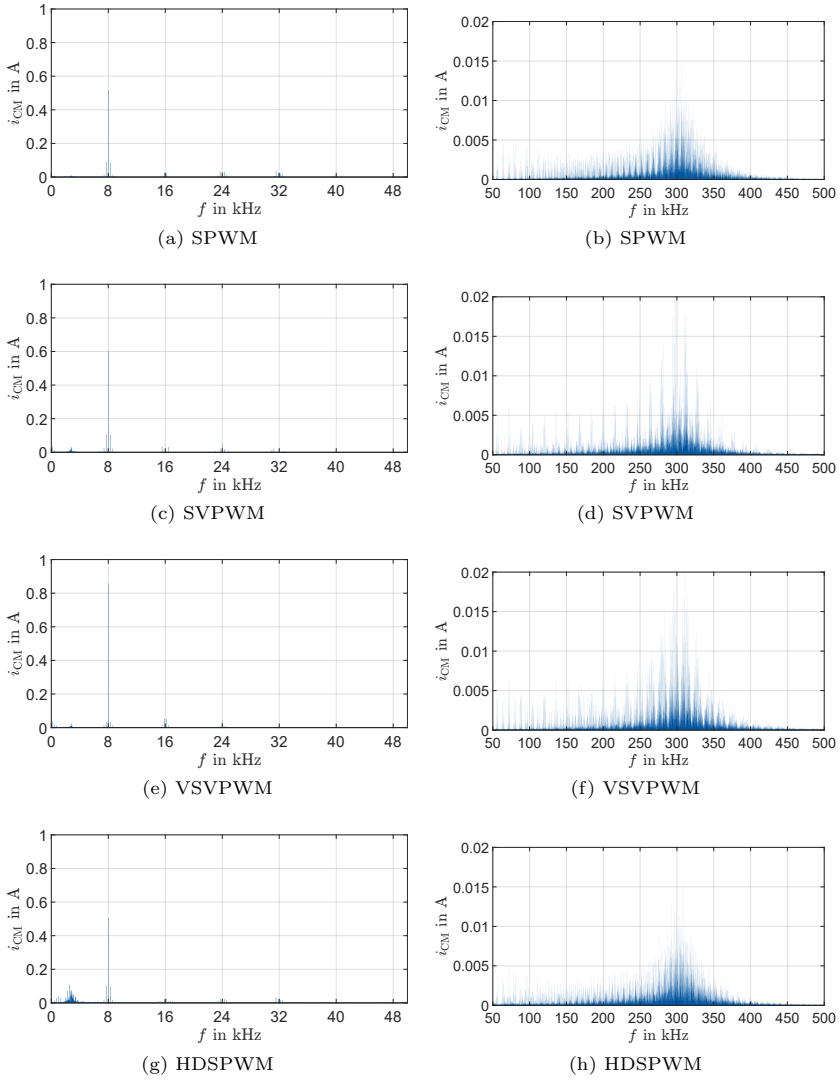
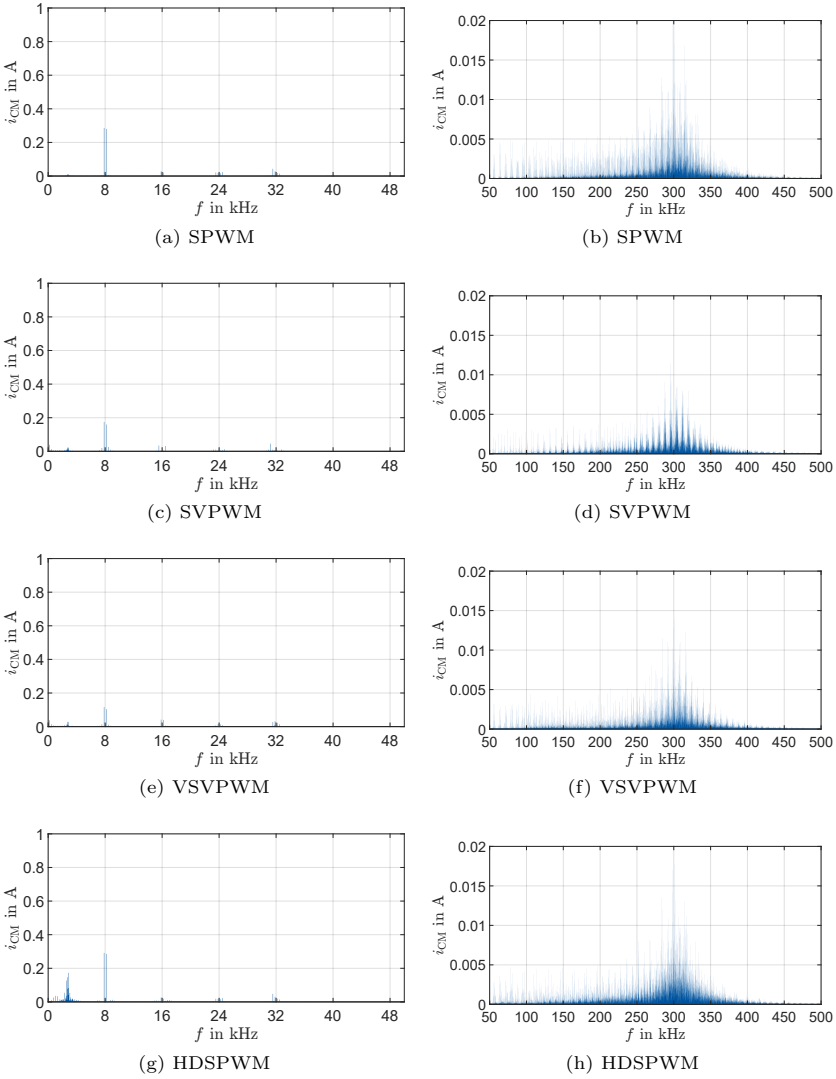


Figure A.15: Frequency spectrum of CM currents with different modulators with one converter and PD.



(a) SPWM (b) SPWM

(c) SVPWM (d) SVPWM

(e) VSVPWM (f) VSVPWM

(g) HDSPWM (h) HDSPWM

Figure A.16: Frequency spectrum of CM currents with different modulators with one converter and POD.

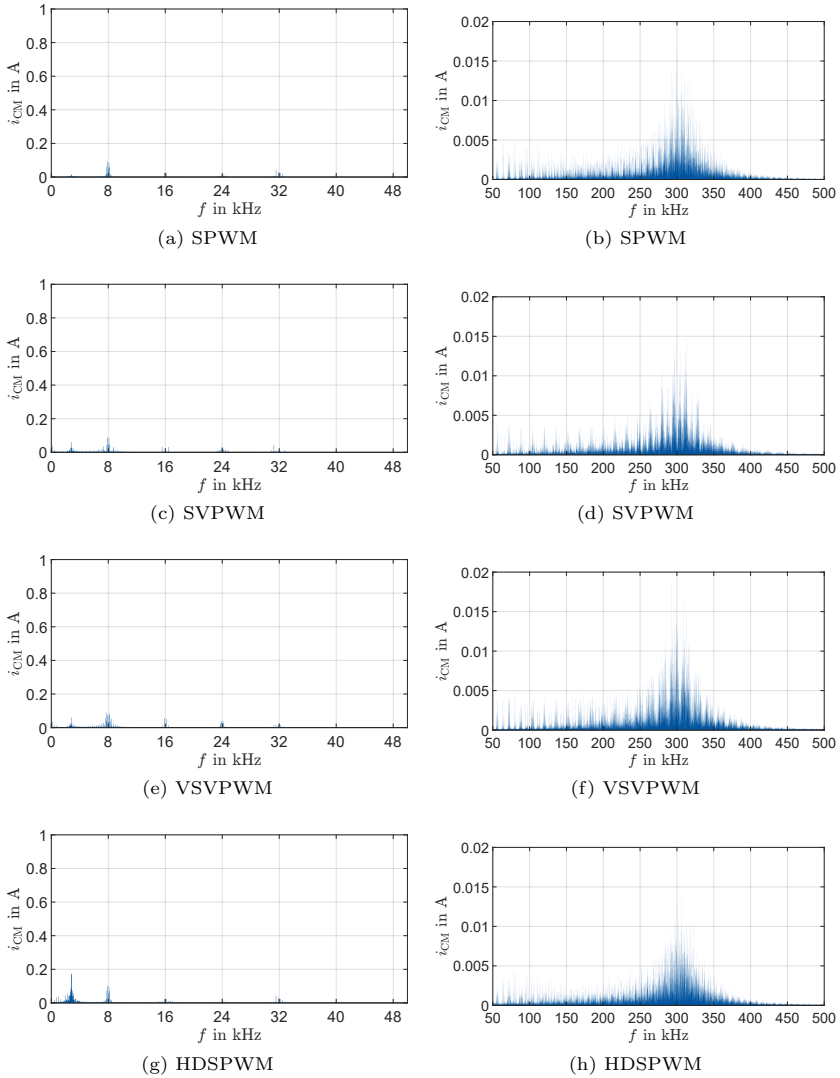
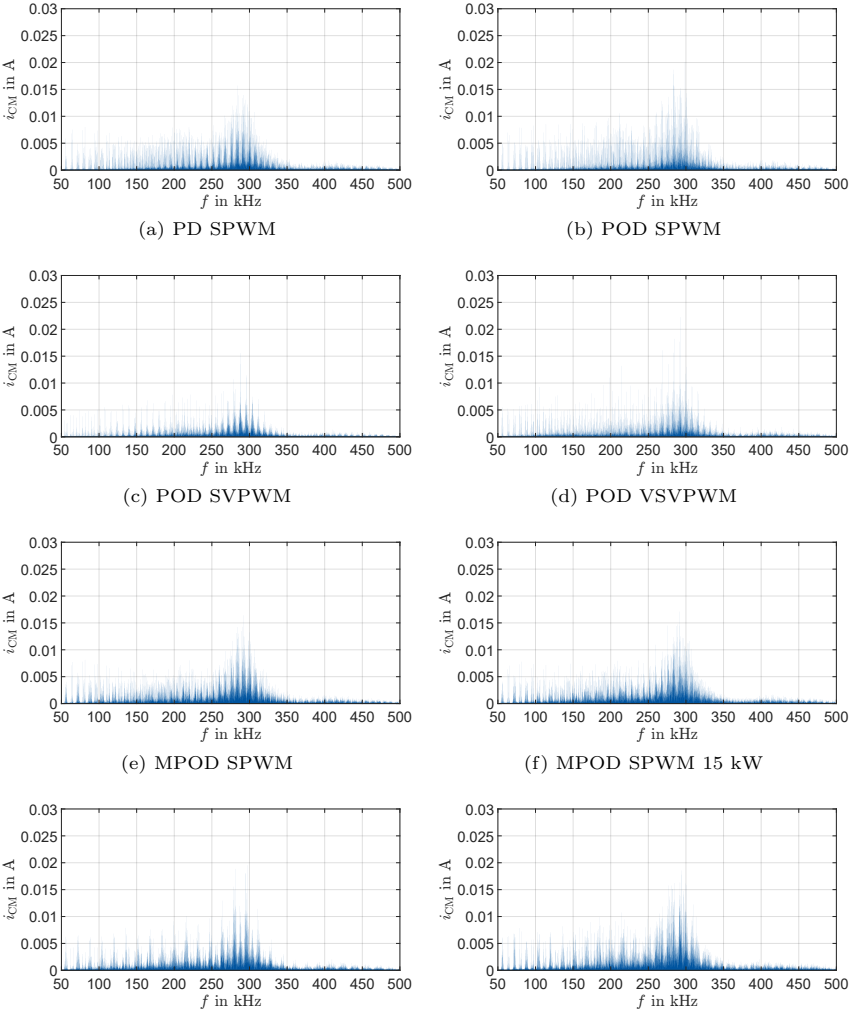


Figure A.17: Frequency spectrum of CM currents with different modulators with one converter and MPOD.



(a) PD SPWM

(b) POD SPWM

(c) POD SVPWM

(d) POD VSVPWM

(e) MPOD SPWM

(f) MPOD SPWM 15 kW

(g) MPOD SVPWM

(h) MPOD VSVPWM

Figure A.18: Frequency spectrum of CM currents above 50 kHz with two converters and different modulators without saturation of CM chokes.

A.4 Electromagnetic Interference Voltage Measurements

This section provides the remaining EMI voltage measurements not shown in Section 5.4.

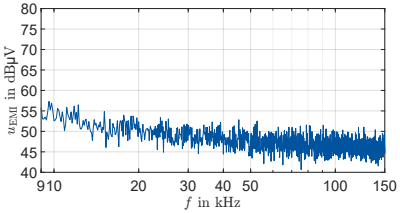
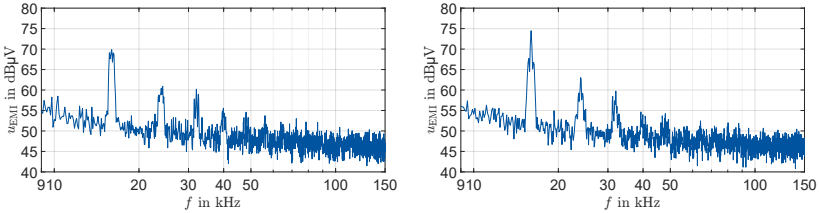


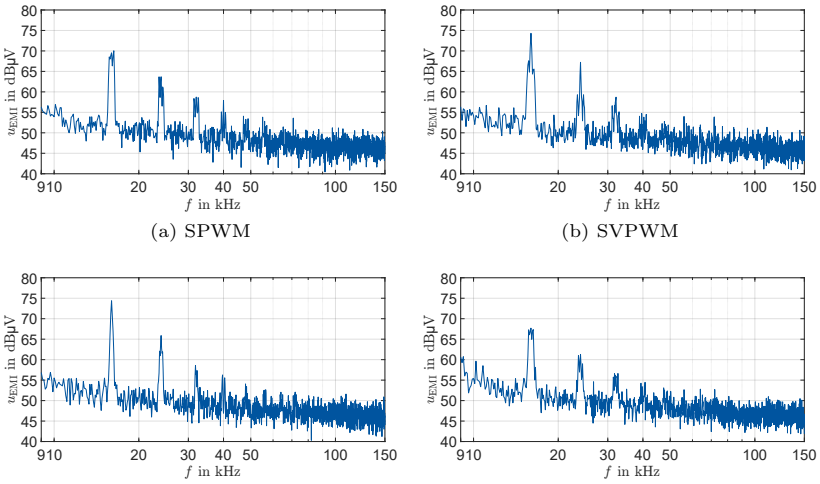
Figure A.19: EMI spectrum with converter turned off (9 kHz to 150 kHz).



(a) SPWM (b) SVPWM

(c) VSVPWM (d) HDSPWM

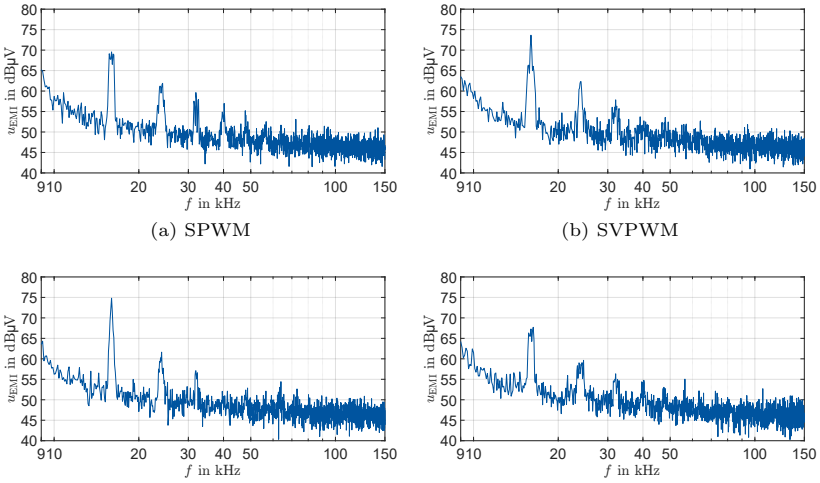
Figure A.20: EMI spectrum with PD (9 kHz to 150 kHz).



(a) SPWM (b) SVPWM

(c) VSVPWM (d) HDSPWM

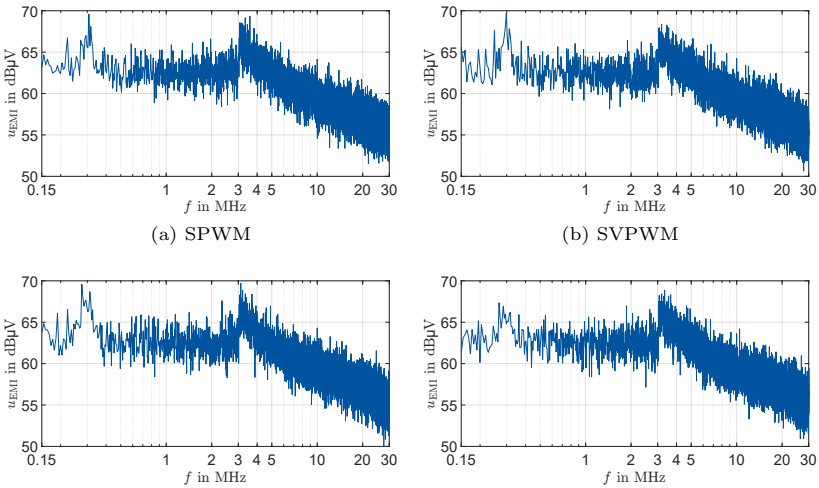
Figure A.21: EMI spectrum with POD (9 kHz to 150 kHz).



(a) SPWM (b) SVPWM

(c) VSVPWM (d) HDSPWM

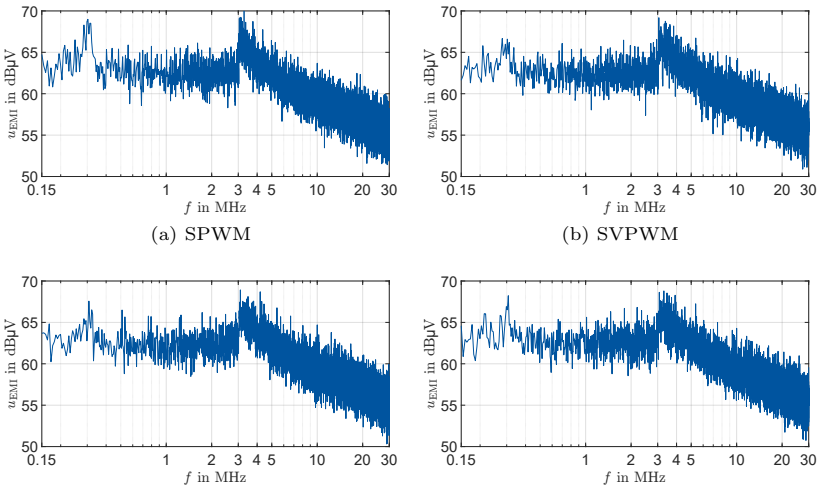
Figure A.22: EMI spectrum with MPOD (9 kHz to 150 kHz).



(a) SPWM (b) SVPWM

(c) VSVPWM (d) HDSPWM

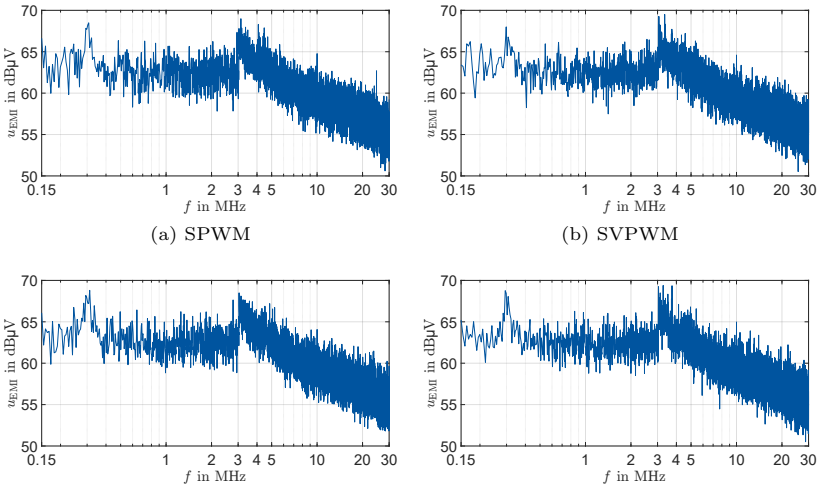
Figure A.23: EMI spectrum with PD (150 kHz to 30 MHz).



(a) SPWM (b) SVPWM

(c) VSVPWM (d) HDSPWM

Figure A.24: EMI spectrum with POD (150 kHz to 30 MHz).



(a) SPWM (b) SVPWM

(c) VSVPWM (d) HDSPWM

Figure A.25: EMI spectrum with MPOD (150 kHz to 30 MHz).

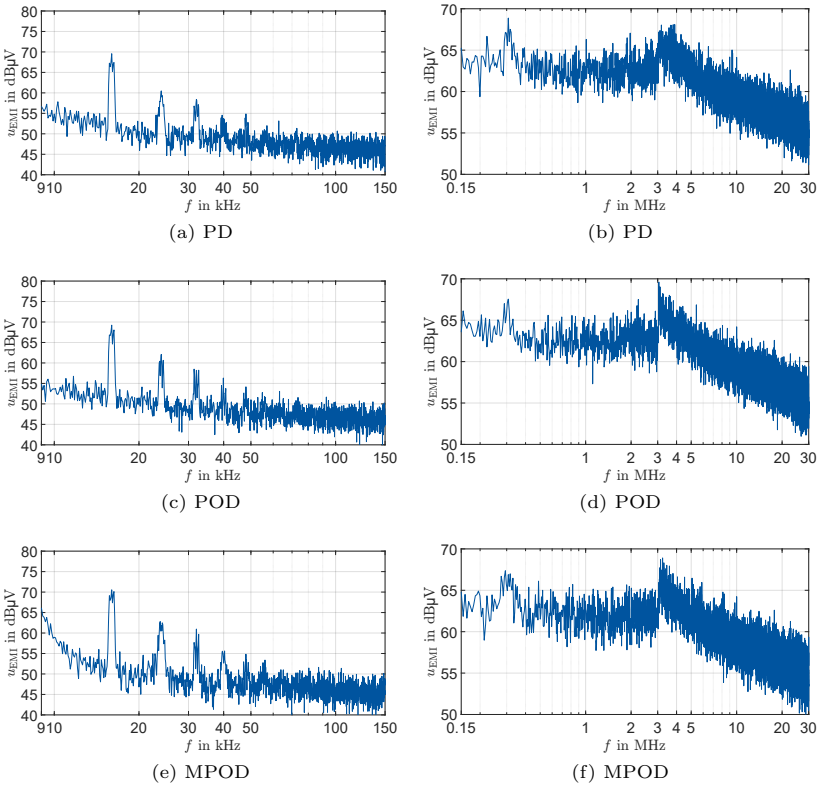
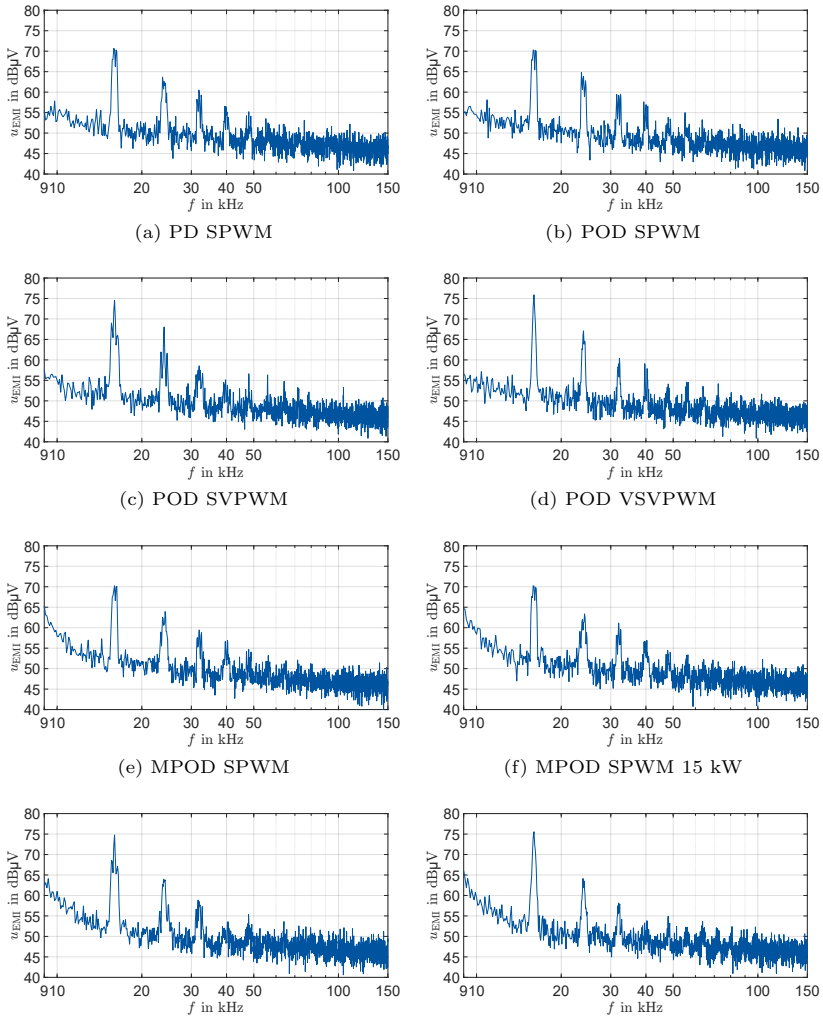


Figure A.26: EMI spectrum with SPWM and 15 kW load using PD, POD, and MPOD.



(a) PD SPWM

(b) POD SPWM

(c) POD SVPWM

(d) POD VSVPWM

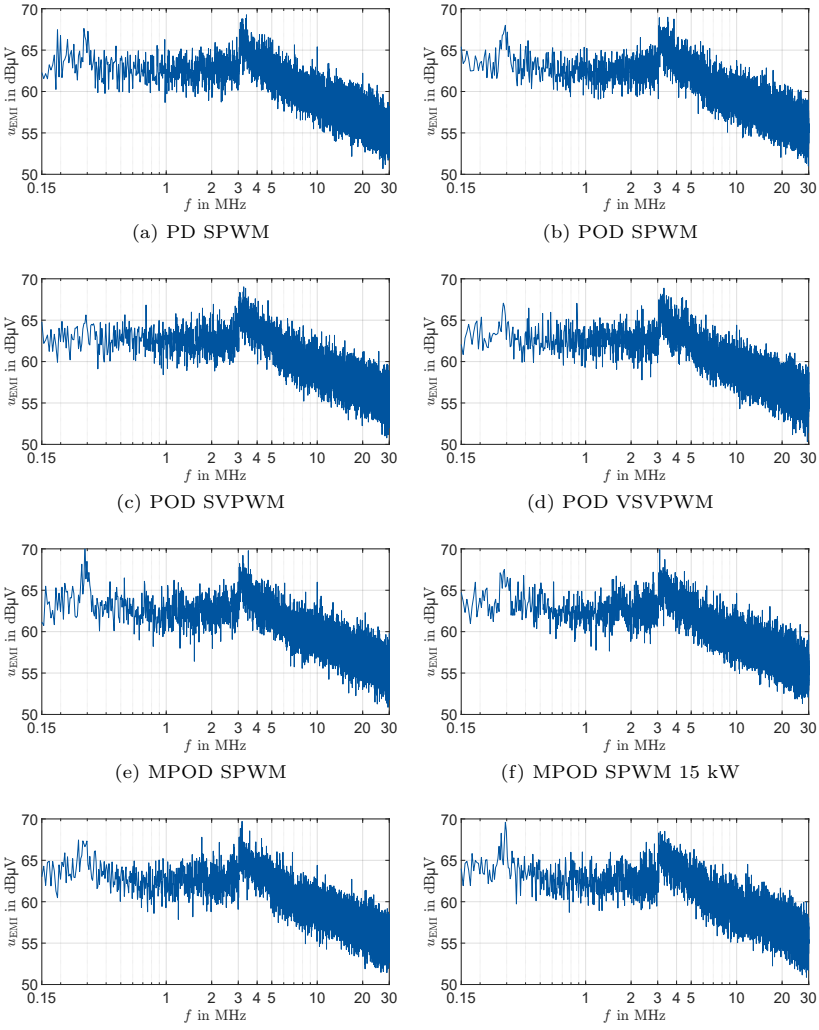
(e) MPOD SPWM

(f) MPOD SPWM 15 kW

(g) MPOD SVPWM

(h) MPOD VSVPWM

Figure A.27: EMI spectrum with different modulators and two converters (9 kHz to 150 kHz).



(a) PD SPWM

(b) POD SPWM

(c) POD SVPWM

(d) POD VSVPWM

(e) MPOD SPWM

(f) MPOD SPWM 15 kW

(g) MPOD SVPWM

(h) MPOD VSVPWM

Figure A.28: EMI spectrum with different modulators and two converters (150 kHz to 30 MHz).

B Acronyms

3L-NPC	three-level neutral point clamped
AFE	active front end
BESS	battery energy storage system
BNC	Bayonet Neill-Concelman
CB	carrier-based
CM	common-mode
CMV	common-mode voltage
CO_2	carbon dioxide
DM	differential-mode
DPWMMAX	discontinuous PWM MAX
DPWMMIN	discontinuous PWM MIN
EMC	electromagnetic compatibility
EMI	electromagnetic interference
FFT	fast Fourier transform
GNSS	global navigation satellite system
GWP	global warming potential
HDSPWM	hybrid-discontinuous sinusoidal pulse width modulation
HDSVPWM	hybrid-discontinuous space vector pulse width modulation
IGBT	insulated-gate bipolar transistor
LCA	life cycle assessment
LISN	line impedance stabilization network
LV	low-voltage

MOSFET	metal-oxide semiconductor field-effect transistor
MPOD	middle phase opposition disposition
MV	medium-voltage
NP	neutral point
ODCA	Open DC Alliance
PCB	printed circuit board
PD	phase disposition
PLL	phase-locked loop
POD	phase opposition disposition
PPS	pulse per second
PV	photovoltaic
PWM	pulse width modulation
RBW	resolution bandwidth
RES	renewable energy source
RMS	root mean square
SMD	surface-mounted device
SPWM	sine-triangle pulse width modulation
SRF	synchronous reference frame
SST	solid-state transformer
SVD	space vector diagram
SVPWM	space vector pulse width modulation
THD	total harmonic distortion
VDE	Verband der Elektrotechnik Elektronik Informationstechnik e.V.
VSVPWM	virtual space vector pulse width modulation

C Symbols

A_L	inductance factor
A_eff	effective core cross-sectional area
A	amplitude of a signal
B_sat	saturation flux density
B_σ	stray flux density
B	magnetic flux density
C_CM	common-mode capacitance
C_DC	DC link capacitance
C_f	filter capacitance
C	capacitance
D_x	diode x
I_DC	DC current
I_d	direct axis current component in dq reference frame
L_CM	common-mode filter inductance
L_f	filter inductance
L_σ	leakage inductance
L_totx	total inductance in path x
L	inductance
N_c	number of cores
$N_\mathrm{w,max}$	maximum number of windings
N_w	number of windings
R_d	droop resistance
$R_\mathrm{f,d}$	damping resistor
R_g	grounding resistance
R	resistance
S_x	power electronics switch x
T_sw	switching period
U_DC	DC link voltage
U_α	α axis voltage component in $\alpha\beta$ reference frame
U_β	β axis voltage component in $\alpha\beta$ reference frame
$U_\mathrm{DC,x}$	DC potential (x=p: positive, x=0: neutral, x=n: negative)

U_d	direct axis voltage component in dq reference frame
U_ref	reference voltage
V_Z0	virtual zero vector
V_ZL	large virtual vector
V_ZM	medium virtual vector
V_ZS	small virtual vector
Δi_max	maximum current ripple
Δt	time difference
Δu_CM	common-mode voltage difference
f_sw	switching frequency
f_g	AC grid frequency
f_res, f_0	resonance frequency
f	frequency
$i_\mathrm{CM,C}$	capacitive common-mode current
$i_\mathrm{CM,max}$	common-mode current limit
i_CM	common-mode current
i_C	circulating current
i_DM	differential-mode current
$\hat{i}_\mathrm{CM,pp}$	peak-to-peak common-mode current
$\hat{i}_\mathrm{CM}$	peak common-mode current
$\hat{i}_\mathrm{DM}$	peak differential-mode current
i_max	maximum phase current
i_mid	middle phase current
i_min	minimum phase current
i_np	neutral point current
i_x	current in phase x
i	current
k_cmp	compensation factor
k_CM	coupling coefficient
k_fill	fill factor
l_eff	effective length of magnetic path
m_i	modulation index
n	number of infeed converters
r_i	inner radius
$r_\mathrm{w,o}$	outer radius of a winding
s_x	switching state x
t_cmp	compensation time
$t_\mathrm{k,x}$	clamping time of phase k to bus x
t	time
u_0	zero-sequence voltage

u_{AC}	AC voltage
u_{CM}	common-mode voltage
u_{EMI}	electromagnetic interference voltage
u_{max}	maximum phase voltage
u_{mid}	middle phase voltage
u_{min}	minimum phase voltage
u_{noise}	noise voltage
u_{out}	output voltage
u_{tot}	total voltage
u_{x}	AC voltage of phase x
u	voltage
Φ	magnetic flux
α	balance degree
μ_0	permeability in vacuum
μ_r	relative permeability
τ_1, τ_2	RC time constant
τ_{f}	fall time
τ_{r}	rise time
τ	width of a pulse
θ	grid voltage angle
ζ	damping factor

List of Figures

1.1 Exemplary grid structure showing a classical grid with consumers on the right side and a grid with many prosumers on the left side. 1
1.2 Exemplary DC underlay grid with two infeed converters connected to different LV AC grid sections. 3
1.3 GWP percentage of various components of a three-level AFE. . . 5

2.1 Possible grounding schemes in VDE SPEC 90037. 13
2.2 Exemplary droop curves in a DC grid according to VDE SPEC 90037. 14
2.3 Quasipeak limit values for interference voltage between 10 Hz and 30 MHz [24]. 17
2.4 DC source decoupling network according to DIN EN 61000-4-6 [37]. 18
2.5 Rectifier topologies considered as AFEs. 20
2.6 Exemplary CMV of two-level and three-level inverters. 22
2.7 Overview of the demonstration setup for experimental analysis. . 25
2.8 Block diagram of the converter controller. 27
2.9 PD PWM carrier and modulation signal with the three-level output voltage. 28
2.10 SVD of a three-level inverter. 29
2.11 CB SVPWM generation with min-max injection. 30
2.12 Possible current paths of three-level inverters [65]. 34

3.1 Current paths in simplified single-phase circuit with different switching combinations. 36
3.2 Simplified three-phase circuit for the analysis of circulating currents. 39
3.3 CM model for circulating currents [26]. 40
3.4 CM model including capacitive CM currents. 41
3.5 CM model for circulating currents with n inverters. 43
3.6 Superposition principle of CM model with n inverters. 44
3.7 Conceptual drawing of a three-phase CM choke with a toroidal core. 45
3.8 CMV measurement against the NP using an artificial star point. 51
3.9 Voltage divider for measuring the CMV. 51

3.10 Voltage response to a square wave input for different time constants of the frequency-compensated voltage divider. 52
3.11 Voltage divider for CMV measurement with an artificial star point. 53
3.12 CMV measurement with two different PCBs. 53

4.1 Virtual space vector diagram. 58
4.2 Unsorted and sorted vector sequence of VSVPWM in subsector 1.4. 60
4.3 Double modulation waves of VSVPWM. 63
4.4 Vector sequence with adjusted dwell times from active NP control. 64
4.5 SVD of HDSPWM. 66
4.6 Double modulation waves of HDSPWM. 67
4.7 Linear modulation range of SPWM and SVPWM. 68
4.8 Carrier signals with PD and POD. 69
4.9 Exemplary CMV with PD and POD PWM. 70
4.10 Carrier signals of all three phases with MPOD. 71
4.11 SVD of MPOD with SPWM and SVPWM. 73
4.12 Measurement setup for the evaluation of different modulation strategies. 75
4.13 Output currents with different modulators and a 30 kW load. . . 76
4.14 DC link voltages with different modulators and a 30 kW load. . . 78
4.15 CMV with different modulators. 80
4.16 CMV spectrum with different modulators up to 36 kHz. 81
4.17 Simulated CMV in time and frequency domain with HDSPWM and $m_\mathrm{i} = 0.666$. 82
4.18 Efficiency measurements with different modulators. 84

5.1 GNSS receiver board with u-blox MAX-M10S and antenna with 3 m cable. 88
5.2 Different PPS signal delay times of two GNSS receivers. 89
5.3 Measurement setup with two converters and GNSS synchronization. 90
5.4 CMV and CM currents with and without GNSS synchronization. 91
5.5 CM currents with and without synchronization measured over a longer time period of 100 ms. 92
5.6 CM current with low frequency component from unequal DC voltage measurements. 92
5.7 CMV and CM currents with coincidentally aligned switching signals. 93
5.8 Measurement setup with one converter and capacitive CM load. . 94
5.9 Capacitive CM currents with different modulators with one converter and PD. 95
5.10 Spectrum of CM currents with different modulators with one converter and PD. 96
5.11 CM current and CMV at switching frequency scale. 97

5.12 Impedance magnitude and phase of CM choke and DM inductor, measured with a vector network analyzer. 98
5.13 Capacitive CM currents with different modulators with one converter and POD. 99
5.14 Capacitive CM currents with different modulators with one converter and MPOD. 101
5.15 CM currents with different modulators with one converter and 15 kW load. 102
5.16 CM current with sub-resonant switching frequency and SPWM with different carrier configurations. 103
5.17 Measurement setup with two converters and capacitive CM load. 104
5.18 Capacitive CM currents with different modulators with two converters and PD. 105
5.19 Capacitive CM currents with different modulators and two converters. 107
5.20 Equivalent impedance with one and two converters. 108
5.21 Frequency spectrum of CM currents with different modulators with two converters. 110
5.22 Frequency spectrum of CM currents above 50 kHz with two converters and MPOD. 111
5.23 CM current with MPOD-SPWM with two converters and 15 kW load. 111
5.24 Comparison of measured and simulated CM currents with different modulators. 113
5.25 Difference of measured and simulated CM current spectra. 115
5.26 Simulated CM currents with a phase difference between the supplying AC grids. 116
5.27 Simulated CM currents with an amplitude difference between the supplying AC grids. 116
5.28 Simulated CM currents with harmonics in the supplying AC grids. 117
5.29 Simulated CM currents with different modulators applied to the two converters. 118
5.30 Simulated CM currents with three converters. 118
5.31 Periodic trapezoidal pulse train in time and frequency domain. . 120
5.32 EMI spectrum between 9 kHz and 150 kHz with different modulators. 123
5.33 EMI spectrum with converter turned off between 150 kHz and 30 MHz. 124
5.34 EMI spectrum with different modulators between 150 kHz and 30 MHz. 125

A.1 Equivalent circuit for calculating the CM current. 137

A.2 Output currents with different modulators and PD. 139
A.3 Output currents with different modulators and POD. 140
A.4 Output currents with different modulators and MPOD. 141
A.5 DC link voltages with different modulators and PD. 142
A.6 DC link voltages with different modulators and POD. 143
A.7 DC link voltages with different modulators and MPOD. 144
A.8 CMV with different modulators and PD. 145
A.9 CMV with different modulators and POD. 146
A.10 CMV with different modulators and MPOD. 147
A.11 Frequency spectrum of CMV with different modulators and PD. 148
A.12 Frequency spectrum of CMV with different modulators and POD. 149
A.13 Frequency spectrum of CMV with different modulators and MPOD. 150
A.14 Frequency spectrum of CM currents with different modulators with one converter and 15 kW load. 151
A.15 Frequency spectrum of CM currents with different modulators with one converter and PD. 152
A.16 Frequency spectrum of CM currents with different modulators with one converter and POD. 153
A.17 Frequency spectrum of CM currents with different modulators with one converter and MPOD. 154
A.18 Frequency spectrum of CM currents above 50 kHz with two converters and different modulators without saturation of CM chokes. 155
A.19 EMI spectrum with converter turned off (9 kHz to 150 kHz). . . 156
A.20 EMI spectrum with PD (9 kHz to 150 kHz). 156
A.21 EMI spectrum with POD (9 kHz to 150 kHz). 157
A.22 EMI spectrum with MPOD (9 kHz to 150 kHz). 157
A.23 EMI spectrum with PD (150 kHz to 30 MHz). 158
A.24 EMI spectrum with POD (150 kHz to 30 MHz). 158
A.25 EMI spectrum with MPOD (150 kHz to 30 MHz). 159
A.26 EMI spectrum with SPWM and 15 kW load using PD, POD, and MPOD. 160
A.27 EMI spectrum with different modulators and two converters (9 kHz to 150 kHz). 161
A.28 EMI spectrum with different modulators and two converters (150 kHz to 30 MHz). 162

List of Tables

2.1 Operating states depending on system voltage and duration [24] 14
2.2 EMI measurement settings with peak detector 18
2.3 Normalized CMV levels for all switching states of the two-level and 3L-NPC inverter 21
2.4 NP current of the 27 switching states 32
2.5 Allowed switching states of a three-level half-bridge 33

4.1 THD of all modulators in inverting and rectifying operation . . . 77
4.2 RMS value of CMV for all modulators in inverting and rectifying operation 79

5.1 RMS value of capacitive CM currents for all modulators with one converter and PD 95
5.2 RMS value of capacitive CM currents for all modulators with one converter and POD 100
5.3 RMS value of capacitive CM currents for all modulators with one converter and MPOD 100
5.4 RMS value of CM currents with SPWM and 15 kW load 102
5.5 RMS value of capacitive CM currents for all modulators with two converters 106
5.6 RMS values of measured and simulated CM currents with selected modulators 114

Bibliography

[1] A. J. Schwab, *Elektroenergiesysteme, Smarte Stromversorgung im Zeitalter der Energiewende*, 7. Aufl. 2022. Berlin, Heidelberg: Springer Berlin Heidelberg, 2022, 1873 pp.

[2] R. W. De Doncker, "Power electronic technologies for flexible dc distribution grids," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 736–743.

[3] E. Akhavan-Rezai, M. F. Shaaban, E. F. El-Saadany, and A. Zidan, "Uncoordinated charging impacts of electric vehicles on electric distribution grids: Normal and fast charging comparison," in *2012 IEEE Power and Energy Society General Meeting*, 2012, pp. 1–7.

[4] H. Vennegeerts, J. Tran, F. Rudolph, and P. Pfeifer, *Metastudie forschungsüberblick netzintegration elektromobilität*, 2018.

[5] B. J. Mortimer, *Horizontal network coupling for charging infrastructure based on three-phase solid-state transformers* (E.ON Energy Research Center 135), First Edition. Aachen: E.ON Energy Research Center, RWTH Aachen University, 2024.

[6] R. De Doncker, "Dc underlay grids for charging stations: Evs and grids partners for charging in the urban environment?" In *ECPE workshop on charging infrastructure*, 2021.

[7] B. Mortimer et al., *Fast-charging technologies, topologies andstandards 2.0*.

[8] M. Müllender, J. Saat, L. Empen, and A. Ulbig, "Planning principles for hybrid ac/dc underlay grids on medium-voltage level," in *27th International Conference on Electricity Distribution (CIRED 2023)*, vol. 2023, 2023, pp. 1035–1039.

[9] F. Herzog, B. Mortimer, and R. W. De Doncker, "Power hardware-in-the-loop test bench for dc grid and battery emulation," in *2024 IEEE 15th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2024, pp. 1–6.

[10] M. Kabus et al., "Environmental impacts of charging concepts for battery electric vehicles: A comparison of on-board and off-board charging systems based on a life cycle assessment," *Energies*, vol. 13, no. 24, 2020.

[11] C. Kockel, B. Mortimer, R. De Doncker, and A. Praktiknjo, "Umweltauswirkungen von gleichstrombasierten ladeinfrastruktursystemen," in *17. Symposium Energieinnovation Graz, Austria*, 2022.

[12] C. Kockel, L. Nolting, R. Goldbeck, C. Wulf, R. W. De Doncker, and A. Praktiknjo, "A scalable life cycle assessment of alternating and direct current microgrids in office buildings," *Applied Energy*, vol. 305, p. 117 878, 2022.

[13] F. Herzog et al., "Technical, ecological and economic analysis of dc underlay grids for the grid integration of charging infrastructure," in *DC=IN 2025; Industrial and Sustainable Direct Current Grids*, 2026, pp. 57–66.

[14] M. Elsobki, P. Daun, L. Rietfort, F. Herzog, R. De Doncker, and A. Praktiknjo, "Ecological impact of dc grid and charging infrastructure: Comparative life-cycle assessment of dc-and ac-based systems in the use case of a parking garage," 2025.

[15] F. Herzog et al., *Ideal - innovative dc-technologie zur nachhaltigen integration moderner ladeinfrastruktur für die elektromobilität*, de, 2025.

[16] K. Heuck, *Elektrische Energieversorgung, Erzeugung, Übertragung und Verteilung elektrischer Energie für Studium und Praxis* (Springer eBook Collection), 9., aktualisierte u. korr. Aufl. 2013, K.-D. Dettmann and D. Schulz, Eds. Wiesbaden: Springer Vieweg, 2013, 78354075 pp.

[17] P. V. Tichelen et al., "Study for european commission dg entr unit b1: Final report, lot 2: Distribution and power transformers, tasks 1-7," VITO and Bio Intelligence Service, Tech. Rep., 2011.

[18] BLOCK Transformatoren-Elektronik GmbH. "Isolating transformer, three-phase: Tt3-a250-4040-0," Accessed: Dec. 5, 2025. [Online]. Available: `https://web.archive.org/web/20240916133456/https://www.block.eu/en_EN/productversion/tt3-a250-4040-0`

[19] A. Joshi and S. Nath, "Efficiency comparison of solid-state transformer and low-frequency power transformer," in *2020 3rd International Conference on Energy, Power and Environment: Towards Clean Energy Technologies*, 2021, pp. 1–6.

[20] D. Dong, M. Agamy, J. Z. Bebic, Q. Chen, and G. Mandrusiak, "A modular sic high-frequency solid-state transformer for medium-voltage applications: Design, implementation, and testing," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 768–778, 2019.

[21] ecoinvent. "Ecoinvent," Accessed: Dec. 13, 2025. [Online]. Available: `https://web.archive.org/web/20251211134913/https://ecoinvent.org/`

[22] GreenDelta GmbH. "Openlca," Accessed: Jan. 2, 2026. [Online]. Available: `https://web.archive.org/web/20260102182901/https://www.openlca.org/`

[23] M. A. J. Huijbregts et al., "Recipe2016: A harmonised life cycle impact assessment method at midpoint and endpoint level," *The International Journal of Life Cycle Assessment*, vol. 22, no. 2, pp. 138–147, 2016.

[24] System Description DC-INDUSTRIE, *VDE SPEC 90037 V1.0*, 2024.

[25] H. J. Abts, *Verteil-Transformatoren* (Praxis). Heidelberg: Hüthig, 2006, 196 pp.

[26] F. Herzog, B. Mortimer, and R. W. De Doncker, "Circulating currents in coupled multi-terminal hybrid ac-dc grids," in *PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2024, pp. 3131–3136.

[27] H. Borcherding, J. Austermann, T. Kuhlmann, B. Weis, and A. Leonide, "Concepts for a dc network in industrial production," in *2017 IEEE Second International Conference on DC Microgrids (ICDCM)*, 2017, pp. 227–234.

[28] M. Schreck, *Schlussbericht der bayerischen motoren werke aktiengesellschaft über das förderprojekt dc-industrie 2 - gleichstrom für die fabrik der zukunft : Laufzeit: 01.09.2019-31.03.2023*, de, 2023.

[29] J. Austermann et al., *Systemkonzept dc-industrie2 : Bewilligungszeitraum: 01. okt. 2019-31. märz 2023*, de, 2023.

[30] A. Sauer, Ed., *Die Gleichstromfabrik, Energieeffizient. Robust. Zukunftsweisend* (Hanser eLibrary). München: Hanser, 2020, 1218 pp.

[31] Current/OS. "Technical rules," Accessed: Jan. 10, 2026. [Online]. Available: `https://web.archive.org/web/20260110104205/https://currentos.org/technical-rules/`

[32] Power electronics systems and equipment - Operation conditions and characteristics of active infeed converter (AIC) applications including design recommendations for their emission values below 150 kHz, *DIN IEC TS 62578*, 2015.

[33] Radio-frequency disturbance characteristics – Limits and methods of measurement, *DIN EN 55011*, 2022.

[34] Specification for radio disturbance and immunity measuring apparatus and methods Part 1-2: Radio disturbance and immunity measuring apparatus – Coupling devices for conducted disturbance measurements, *DIN EN 55016-1-2*, 2019.

[35] Specification for radio disturbance and immunity measuring apparatus and methods Part 1-1: Radio disturbance and immunity measuring apparatus – Measuring apparatus, *DIN EN IEC 55016-1-1*, 2019.

[36] Specification for radio disturbance and immunity measuring apparatus and methods Part 2-1: Methods of measurement of disturbances and immunity – Conducted disturbance measurements, *DIN EN 55016-2-1*, 2019.

[37] Electromagnetic compatibility (EMC)Part 4-6: Testing and measurement techniques – Immunity to conducted disturbances, induced by radio-frequency fields, *DIN EN 61000-4-6*, 2014.

[38] Protection against corrosion by stray current from direct current systems, *DIN EN 50162*, 2005.

[39] Residual current operated circuit-breakers without integral overcurrent protection for household and similar uses (RCCBs), *DIN EN 61008-1*, 2018.

[40] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, 1981.

[41] C. Wang and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level npc converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2262–2271, 2010.

[42] J. Shen, S. Schroder, B. Duro, and R. Roesner, "A neutral-point balancing controller for a three-level inverter with full power-factor range and low distortion," *IEEE Transactions on Industry Applications*, vol. 49, no. 1, pp. 138–148, 2013.

[43] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *IEEE Transactions on Industry Applications*, vol. 41, no. 3, pp. 855–865, 2005.

[44] M. Stecca, T. B. Soeiro, L. R. Elizondo, P. Bauer, and P. Palensky, "Comparison of two and three-level dc-ac converters for a 100 kw battery energy storage system," in *2020 IEEE 29th International Symposium on Industrial Electronics (ISIE)*, 2020, pp. 677–682.

[45] I. Rabl. "Technical explanation 3l miniskiip evaluation inverter," Accessed: Oct. 20, 2025. [Online]. Available: `https://web.archive.org/web/20251020114616/https://assets.danfoss.com/documents/latest/463018/AJ500951785951en-000201.pdf`

[46] A. A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-filter design for a multimegawatt medium-voltage voltage-source inverter," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1205–1217, 2011.

[47] R. Teodorescu, M. Liserre, and P. Rodríguez, *Grid converters for photovoltaic and wind power systems*. Chichester, West Sussex: Wiley, 2011, 1398 pp.

[48] Z. Yang, *On the Stability of Three-Phase Grid-Tied Photovoltaic Inverter Systems* (E.ON Energy Research Center 90), First Edition. Aachen: E.ON Energy Research Center, RWTH Aachen University, 2021.

[49] A. P. N. Tahim, D. J. Pagano, E. Lenz, and V. Stramosk, "Modeling and stability analysis of islanded dc microgrids under droop control," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4597–4607, 2015.

[50] Y. Ito, Y. Zhongqing, and H. Akagi, "Dc microgrid based distribution power generation system," in *The 4th International Power Electronics and Motion Control Conference, 2004. IPEMC 2004.*, vol. 3, 2004, 1740–1745 Vol.3.

[51] S. Augustine, M. K. Mishra, and N. Lakshminarasamma, "Adaptive droop control strategy for load sharing and circulating current minimization in low-voltage standalone dc microgrid," *IEEE Transactions on Sustainable Energy*, vol. 6, no. 1, pp. 132–141, 2015.

[52] X. Tian, Y. Wang, F. Wang, Z. Guo, and Y. Dong, "An improved droop control strategy for accurate current sharing and dc-bus voltage compensation in dc microgrid," in *The 16th IET International Conference on AC and DC Power Transmission (ACDC 2020)*, vol. 2020, 2020, pp. 1466–1473.

[53] V. Jayakumar, B. Chokkalingam, and J. L. Munda, "A comprehensive review on space vector modulation techniques for neutral point clamped multi-level inverters," *IEEE Access*, vol. 9, pp. 112 104–112 144, 2021.

[54] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters, Principles and practice* (IEEE series on power engineering). Hoboken, NJ: John Wiley, 2003, 724 pp.

[55] T. Bruckner and D. Holmes, "Optimal pulse-width modulation for three-level inverters," *IEEE Transactions on Power Electronics*, vol. 20, no. 1, pp. 82–89, 2005.

[56] H. van der Broeck, H.-C. Skudelny, and G. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Transactions on Industry Applications*, vol. 24, no. 1, pp. 142–150, Jan. 1988.

[57] F. Wang, "Sine-triangle versus space-vector modulation for three-level pwm voltage-source inverters," *IEEE Transactions on Industry Applications*, vol. 38, no. 2, pp. 500–506, 2002.

[58] W. Yao, H. Hu, and Z. Lu, "Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 45–51, 2008.

[59] Y. He, Y. Liu, C. Lei, and J. Liu, "Equivalent space vector output of diode clamped multilevel inverters through modulation wave decomposition under carrier-based pwm strategy," *IEEE Access*, vol. 8, pp. 104 918–104 932, 2020.

[60] A. Lewicki, D. Kondratenko, and C. I. Odeh, "Hybridized pwm strategy for three- and multiphase three-level npc inverters," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 8, pp. 8279–8290, 2024.

[61] D. Woldegiorgis and H. A. Mantooth, "A modified neutral-point voltage control strategy for three-level inverters based on decomposition of space vector diagram," *CES Transactions on Electrical Machines and Systems*, vol. 6, no. 2, pp. 124–134, 2022.

[62] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 6, pp. 1582–1588, 2005.

[63] I. Rabl. "Technical explanation 3l miniskiip evaluation inverter," Accessed: Oct. 26, 2025. [Online]. Available: `https://web.archive.org/web/20251026180427/https://assets.danfoss.com/documents/latest/468748/AB501636827467en-000301.pdf`

[64] D. Zhou and D. Rouaud, "Dead-time effect and compensations of three-level neutral point clamp inverters for high-performance drive applications," *IEEE Transactions on Power Electronics*, vol. 14, no. 4, pp. 782–788, 1999.

[65] Y. Kan, S.-W. Hyun, S.-J. Hong, and C.-Y. Won, "Zero dead-time pwm implementation method for reducing total harmonic distortion in 3-level npc inverter," in *2015 18th International Conference on Electrical Machines and Systems (ICEMS)*, 2015, pp. 1069–1073.

[66] W. Chen, X. Yang, W. Zhang, and X. Song, "Leakage current calculation for pv inverter system based on a parasitic capacitor model," *IEEE Transactions on Power Electronics*, pp. 1–1, 2016.

[67] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source pwm inverters," in *Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting*, 1993, 965–970 vol.2.

[68] H. Akagi, H. Hasegawa, and T. Doumoto, "Design and performance of a passive emi filter for use with a voltage-source pwm inverter having sinusoidal output voltage and zero common-mode voltage," *IEEE Transactions on Power Electronics*, vol. 19, no. 4, pp. 1069–1076, 2004.

[69] H. Akagi and S. Tamura, "A passive emi filter for eliminating both bearing current and ground leakage current from an inverter-driven motor," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1459–1469, 2006.

[70] H. Akagi and T. Shimizu, "Attenuation of conducted emi emissions from an inverter-driven motor," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 282–290, 2008.

[71] J. Biela, A. Wirthmueller, R. Waespe, M. L. Heldwein, K. Raggl, and J. W. Kolar, "Passive and active hybrid integrated emi filters," *IEEE Transactions on Power Electronics*, vol. 24, no. 5, pp. 1340–1349, 2009.

[72] M. L. Heldwein, L. Dalessandro, and J. W. Kolar, "The three-phase common-mode inductor: Modeling and design issues," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 8, pp. 3264–3274, 2011.

[73] M. H. Hedayati, A. B. Acharya, and V. John, "Common-mode filter design for pwm rectifier-based motor drives," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5364–5371, 2013.

[74] F. Wang, Z. Zhang, and R. Chen, *Design of three-phase AC power electronics converters*. Hoboken, NJ: Wiley, 2024, 1670 pp.

[75] VACUUMSCHMELZE GmbH & Co. KG. "Specification for soft magnetic cores s-no.: T60006-l2102-v080-01-," Accessed: Oct. 26, 2025. [Online]. Available: `https://web.archive.org/web/20251026160117/https://vacuumschmelze.de/03_Documents/Datasheets%20-%20Drawings/Cores/L2102-V080.pdf`

[76] Klaus Faber AG. "NSGAFOEU 1X10 1,8/3 kV SW," Accessed: Oct. 26, 2025. [Online]. Available: `https://web.archive.org/web/20251026160619/https://shop.faberkabel.de/Flexible-Leitungen/Gummileitungen/Sonder-Gummiaderleitung-NSGAFOeU/050172.html`

[77] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest three virtual space vector pwm - a modulation for the comprehensive neutral-point balancing in the three-level npc inverter," *IEEE Power Electronics Letters*, vol. 2, no. 1, pp. 11–15, 2004.

[78] Z. Tan, Y. Li, and M. Li, "A direct torque control of induction motor based on three-level npc inverter," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, vol. 3, 2001, 1435–1439 vol. 3.

[79] J. Wang, Y. Gao, and W. Jiang, "A carrier-based implementation of virtual space vector modulation for neutral-point-clamped three-level inverter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 12, pp. 9580–9586, 2017.

[80] W.-d. Jiang, S.-w. Du, L.-c. Chang, Y. Zhang, and Q. Zhao, "Hybrid pwm strategy of svpwm and vsvpwm for npc three-level voltage-source inverter," *IEEE Transactions on Power Electronics*, vol. 25, no. 10, pp. 2607–2619, 2010.

[81] J. Wang, W. Zhang, M. Ma, Q. Zhang, and W. Jiang, "Discontinuous pwm strategy for neutral point clamped three-level inverter to achieve multiple control objectives," *IEEE Access*, vol. 7, pp. 158 533–158 544, 2019.

[82] W. Jiang, H. Jiang, S. Liu, S. Ji, and J. Wang, "A carrier-based discontinuous pwm strategy for t-type three-level converter with reduced common mode voltage, switching loss, and neutral point voltage control," *IEEE Transactions on Power Electronics*, vol. 37, no. 2, pp. 1761–1771, 2022.

[83] K. Taniguchi, Y. Ogino, and H. Irie, "Pwm technique for power mosfet inverter," *IEEE Transactions on Power Electronics*, vol. 3, no. 3, pp. 328–334, 1988.

[84] A. Hava, R. Kerkman, and T. Lipo, "Simple analytical and graphical methods for carrier-based pwm-vsi drives," *IEEE Transactions on Power Electronics*, vol. 14, no. 1, pp. 49–61, 1999.

[85] D. Liu, J. Wang, S. Liu, and W. Jiang, "Novel modulation strategy to achieve neutral-point voltage balance, common-mode voltage, and switching loss reduction for neutral-point clamped three-level inverters," *Chinese Journal of Electrical Engineering*, vol. 10, no. 4, pp. 106–118, 2024.

[86] S. Xia, X. Wu, J. Zheng, X. Li, and K. Wang, "A virtual space vector pwm with active neutral point voltage control and common mode voltage suppression for three-level npc converters," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 12, pp. 11 761–11 771, 2021.

[87] W. Jiang et al., "A novel virtual space vector modulation with reduced common-mode voltage and eliminated neutral point voltage oscillation for neutral point clamped three-level inverter," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 2, pp. 884–894, 2020.

[88] F. Guo, T. Yang, S. Bozhko, and P. Wheeler, "A novel virtual space vector modulation scheme for three-level npc power converter with neutral-point voltage balancing and common-mode voltage reduction for electric starter/generator system in more-electric-aircraft," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 1852–1858.

[89] M. Haei, A. Khoshooei, and A. Khoshsaadat, "Unconditional control of npc inverter by a modified virtual space vector modulation," in *2022 13th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC)*, 2022, pp. 275–280.

[90] Z. Huang, J. Wang, S. Zhang, R. Zhu, F. Guo, and Y. Xia, "Enhanced active voltage regulation capability for three-level npc converters with the space vector modulation method," *Journal of Electrical Engineering and Technology*, vol. 20, pp. 1451–1461, 2024.

[91] M. Selvaperumal, D. Kirubakaran, and C. Bharatiraja, "A hybrid space vector modulation for the near-zero common-mode voltage and common-mode current mitigation in diode-clamped multilevel-inverter-fed induction motor drive," *International Transactions on Electrical Energy Systems*, vol. 30, no. 10, e12535, 2020. eprint: `https://onlinelibrary.wiley.com/doi/pdf/10.1002/2050-7038.12535`.

[92] R. Zhang, V. Prasad, D. Boroyevich, and F. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," *IEEE Transactions on Power Electronics*, vol. 17, no. 3, pp. 314–326, 2002.

[93] X. Guo, S. Du, N. Diao, C. Hua, and F. Blaabjerg, "Three-dimensional space vector modulation for four-leg current-source inverters," *IEEE Transactions on Power Electronics*, vol. 38, no. 10, pp. 13 122–13 132, 2023.

[94] J. Wang et al., "A novel discontinuous modulation strategy with reduced common-mode voltage and removed dc offset on neutral-point voltage for neutral-point-clamped three-level converter," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7637–7649, 2019.

[95] J. Wang, S. Ji, S. Liu, H. Jiang, and W. Jiang, "A discontinuous pwm strategy to control neutral point voltage for vienna rectifier with improved pwm sequence," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 3, pp. 3230–3241, 2022.

[96] A. Radan, A. H. Shahirinia, and M. Falahi, "Evaluation of carrier-based pwm methods for multi-level inverters," in *2007 IEEE International Symposium on Industrial Electronics*, 2007, pp. 389–394.

[97] I. Salagae and H. du T Mouton, "Natural balancing of neutral-point-clamped converters under pod pulsewidth modulation," in *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03.*, vol. 1, 2003, 47–52 vol.1.

[98] M. Renge and H. Suryawanshi, "Multilevel inverter to reduce common mode voltage in ac motor drives using spwm technique," *Journal of Power Electronics*, vol. 11, 2011.

[99] T. Nguyen, D. Phan Quoc, N. D. Dao, and H.-H. Lee, "Carrier phase-shift pwm to reduce common-mode voltage for three-level t-type npc inverters," *Journal of Power Electronics*, vol. 14, pp. 1197–1207, 2014.

[100] Y. Y. Shen, S.-C. Peng, S.-W. Lin, P. T. Cheng, and C.-C. Chu, "Dc-link current ripple mitigation of three-phase npc converters using mixed phase-disposition modulation schemes," in *2022 IEEE Industry Applications Society Annual Meeting (IAS)*, 2022, pp. 1–8.

[101] M.-J. Tsai, Y.-Y. Shen, M.-J. Chao, and P.-T. Cheng, "An edge-aligned modulation technique to suppress leakage current in the back-to-back neutral-point clamped converter," *IEEE Transactions on Industry Applications*, vol. 57, no. 3, pp. 3179–3187, 2021.

[102] Texas Instruments. "Tms320f2837xd dual-core real-time microcontrollers," Accessed: Nov. 27, 2025. [Online]. Available: https://web.archive.org/web/20240331183442/https://www.ti.com/lit/ds/sprs880p/sprs880p.pdf

[103] Texas Instruments. "User's guide launchxl-f28379d overview," Accessed: Nov. 27, 2025. [Online]. Available: https://web.archive.org/web/20250715234500/https://www.ti.com/lit/ug/sprui77c/sprui77c.pdf

[104] "Ieee standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces," *IEEE Std 1547-2018 (Revision of IEEE Std 1547-2003)*, pp. 1–138, 2018.

[105] Photovoltaic (PV) systems - Characteristics of the utility interface, *Iec 61727*, 2004.

[106] Matuschek Messtechnik GmbH. "Power analyzer lk601," Accessed: Nov. 13, 2025. [Online]. Available: https://web.archive.org/web/20251113083307/https://www.matuschek.de/power-analyzer/power-analyzer-lk601.htm

[107] Danisense A/S. "Danisense ds600id," Accessed: Nov. 13, 2025. [Online]. Available: https://web.archive.org/web/20251113090602/https://danisense.com/archive/DS600ID-3.pdf

[108] A. Monti, C. Muscas, and F. Ponci, *Phasor measurement units and wide area monitoring systems, From the sensors to the system*. London, UK: Elsevier, 2016, 1 p.

[109] Global Positioning System Joint Program Office. "Gps user equipment (phase iii) interface control document for the precise time and time interval (ptti) interface," Accessed: Nov. 24, 2025. [Online]. Available: https://web.archive.org/web/20250711021301/https://navcen.uscg.gov/sites/default/files/pdf/gps/ICD-GPS-060B.pdf

[110] u-blox Holding AG. "U-blox max-m10s," Accessed: Nov. 14, 2025. [Online]. Available: https://web.archive.org/web/20251114081037/https://content.u-blox.com/sites/default/files/MAX-M10S_DataSheet_UBX-20035208.pdf

[111] SparkFun Electronics. "Sparkfun gnss receiver breakout - max-m10s (qwiic)," Accessed: Nov. 14, 2025. [Online]. Available: https://web.archive.org/web/20251114081521/https://www.sparkfun.com/sparkfun-gnss-receiver-breakout-max-m10s-qwiic.html

[112] u-blox Holding AG. "Max-m10s standard precision gnss module professional grade integration manual," Accessed: Nov. 24, 2025. [Online]. Available: https://web.archive.org/web/20251010165834/https://content.u-blox.com/sites/default/files/MAX-M10S_IntegrationManual_UBX-20053088.pdf

[113] N. El Halabi, M. García-Gracia, M. Comech, and E. Oyarbide, "Distributed generation network design considering ground capacitive couplings," *Renewable Energy*, vol. 45, pp. 119–127, 2012.

[114] D. Han, C. Morris, W. Lee, and B. Sarlioglu, "Determination of cm choke parameters for sic mosfet motor drive based on simple measurements and frequency domain modeling," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 2861–2867.

[115] D. Han, C. T. Morris, W. Lee, and B. Sarlioglu, "Three-phase common mode inductor design and size minimization," in *2016 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2016, pp. 1–8.

[116] OMICRON Lab. "Technical data sheet bode 100 revision 2," Accessed: Nov. 24, 2025. [Online]. Available: https://web.archive.org/web/20251124070400/https://www.omicron-lab.com/fileadmin/assets/Bode_100/Documents/Technical_Data_Bode100R2.pdf

[117] C. R. Paul, *Introduction to electromagnetic compatibility* (Wiley series in microwave and optical engineering), Second edition. Hoboken, N.J: Wiley-Interscience, 2006.

[118] X. Ruan, L. Xie, Q. Ji, and X. Yuan, *Conducted Electromagnetic Interference in Power Converters: Modeling, Prediction and Reduction* (CPSS Power Electronics Series), 1st ed. 2024. Singapore: Imprint: Springer, 2024, 1213198192 pp.

[119] EPCOS AG. "Ferrites and accessories series/type: B64290a0084, b64290l0084," Accessed: Nov. 19, 2025. [Online]. Available: https://web.archive.org/web/20211128153246/https://www.tdk-electronics.tdk.com/inf/80/db/fer/r_102_65_8_15_0.pdf

[120] Würth Elektronik. "We-tof emi suppression toroidal ferrite 74270191," Accessed: Nov. 19, 2025. [Online]. Available: https://web.archive.org/web/20250808234607/https://www.we-online.com/components/products/datasheet/74270191.pdf

[121] Schwarzbeck Mess-Elektronik. "Tk 9420 voltage probe 9 khz - 30 mhz," Accessed: Nov. 19, 2025. [Online]. Available: https://web.archive.org/web/20250808142932/https://schwarzbeck.de/Datenblatt/k9420.pdf

[122] Rohde & Schwarz. "R&s esl emi test receiver specifications," Accessed: Nov. 19, 2025. [Online]. Available: https://web.archive.org/web/20251119155533/https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_common_library/dl_brochures_and_datasheets/pdf_1/ESL_dat-sw_en_5214-0430-22_v0300.pdf

[123] Schwarzbeck Mess-Elektronik. "Pulse limiter with fuse lamp vtsd 9561-d," Accessed: Nov. 19, 2025. [Online]. Available: https://web.archive.org/web/20240624024516/http://schwarzbeck.de/Datenblatt/k9561d.pdf

[124] S. Ogasawara, H. Ayano, and H. Akagi, "An active circuit for cancellation of common-mode voltage generated by a pwm inverter," *IEEE Transactions on Power Electronics*, vol. 13, no. 5, pp. 835–841, 1998.

[125] P. Ide, F. Schafmeister, and N. Froehleke, "Active common-mode voltage cancellation for three-phase pwm rectifier/inverter systems based on a new topology," in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, vol. 1, 2001, 201–207 vol.1.

[126] Y.-C. Son and S.-K. Sul, "A new active common-mode emi filter for pwm inverter," *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1309–1314, 2003.

[127] M. C. Di Piazza, G. Tine, and G. Vitale, "An improved active common-mode voltage compensation device for induction motor drives," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 4, pp. 1823–1834, 2008.

[128] G. Buticchi, D. Barater, E. Lorenzani, and A. Salati, "Active common-mode filter for photovoltaic transformerless inverters," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 5702–5707.

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To counteract climate change, it is necessary to reduce the emission of greenhouse gases, such as carbon dioxide. The electrification of heating and transportation systems, as well as the installation of renewable energy sources (RESs), plays a central role in achieving this goal. However, this puts a strain on the low-voltage and medium-voltage distribution grids, because RESs, heat pumps, and charging infrastructure are primarily connected to them. DC underlay grids that support the existing AC grids are beneficial for integrating RESs and charging infrastructure. They are more efficient, require fewer components, and enable vertical grid coupling. DC grids with AC-side grounding do not require galvanic isolation and offer certain advantages. However, they present two challenges, particularly when multiple infeed converters are used: increased common-mode (CM) currents and electromagnetic interference.

This work thoroughly analyzes these challenges and presents methods to mitigate their effects. First, a CM model is derived to determine potential reduction measures. The CM choke, the common-mode voltage (CMV) of the infeed converters and their switching alignment are identified as the primary influencing factors. These factors are addressed through a model-based CM choke design guide, optimized modulation strategies that reduce CMV for three-level inverters, and synchronization of locally distributed converters via the global navigation satellite system. Experiments on a demonstration setup resembling a DC underlay grid with AC-side grounding analyze all concepts.

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