Skalierbarer Qubit-Shuttle über Si/SiGe Quantenbus und T-junction

Leistungscharakterisierung von Heterostrukturen und Untersuchung Elektrostatischer Potentialstörungen Durch Elektronen-shuttle

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vorgelegt von

Ran Xue, M. Sc.

aus

Tianjin, China

Berichter: Prof. Hendrik Bluhm, PhD
Prof. Dr. Joachim Knoch

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Composition of the doctoral committee:

Vorsitzer:		
Univ.-Prof. Dr. rar. nat.	Michal Czakon	RWTH Aachen University
Berichter:		
Univ.-Prof. Dr. rar. nat.	Hendrik Bluhm	RWTH Aachen University
Univ.-Prof. Dr. rar. nat.	Joachim Knoch	RWTH Aachen University
Weitere Prüfer:		
apl. Prof. Dr. rar. nat.	Thomas Schäpers	Forschungszentrum Jülich

Betreuer:
Dr. rar. nat. Lars R. Schreiber, RWTH Aachen University.



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To my families and everyone who supported
and accompanied me throughout my PhD journey

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Ran Xue, M.Sc.

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ABSTRACT

The quest for the universal fault-tolerant quantum computing demands innovative solutions. The quantum error correction (QEC) emerges as a key point to demonstrate the fault-tolerate quantum computer regardless implementation platforms while requiring millions of coupled qubits. A scalable approach to interconnect these qubits becomes critical. Spin qubits in gate defined quantum dots (QDs) in semiconductors, in particular Si/SiGe heterostructures, are good representatives owing to their miniaturized footprints and the compatibility with mature CMOS manufacturing technologies in semiconductors industries. Leveraging these advancements, one promising approach to scalably interconnect millions of qubits becomes linking sparsely distributed qubits those are coherently transferable.

In this dissertation, an efficient and scalable mechanism for interconnecting qubits carriers i.e. electrons termed the conveyor-mode shuttling is explained and demonstrated experimentally. The conveyor mode shuttle of electrons is implemented by shuttling electrons confined in a sinus conveyor-belt like potential consisting of an array of gate defined QDs in Si/SiGe heterostructures. Only four sinus input signals with a sequential $\pi/2$ phase shift generate the conveyor potential periodically. A device implementation termed the QuBus device is proposed and manufactured which spans over 10 μm long distance targeting the displacement between qubits in a scalable spin qubits architecture (i.e. the SpinBus architecture). A combination of high energy e-beam lithography (EBL) with 100 keV beam energy and metal lift-off process produces prototypes QuBus devices with a gate pitch of 70 nm benchmarking the 10 nm node in semiconductor industries. In this device, the gate electrodes for shuttling electrons are connected in four gate-sets, hence a shuttle distance independent control complexity.

In this work, a conveyer-mode shuttling of electrons over 19.2 μm (bidirectionally in the QuBus) shows a high fidelity of (99.7 ± 0.3) % and the high-fidelity shuttling of arbitrarily chosen patterns of zero and single-electrons (up to 34 electrons) revealing the scalability of the conveyor-mode shuttling in Si/SiGe QuBus and its capabilities to operate as a register hosting multiple electrons. However, the scalability also relies on the homogeneity of the potential landscape mainly limited by the hosting materials such as the charged disorders in oxides-semiconductor interface, those in Si/SiGe heterostructures and alloys disorders in Si/SiGe leading to valley splittings. Above challenges are addressed accordingly in this dissertation.

Firstly, the shuttle tomography method is developed to experimentally address the potential disorders along the QuBus device. By benchmarking the potential imperfections and local shuttle fidelity of the QuBus, shuttle tomography presents an alternative characterization method to sense the potential profile of a long-range coupler i.e. the QuBus device. Secondly, the defect disorders in the Si/SiGe closing to the confined electrons are studied from theoretical perspectives. The focus is mainly about their strong Coulomb interactions towards shuttled electrons. Here the time resolved excitations of

orbital states for shuttled electrons are examined in order to find the correlation between the defect density and the excitation probability which eventually contributes to the shuttle infidelity. In terms of valley splitting, a new prototype of QuBus is explored by introducing a backgate which enhances the valley splitting by tunable perpendicular electric field.

Finally, the path towards a scalable architecture demands extending the linear QuBus to a T-junction serving three way intersections for qubits in a two-dimensional qubits network. The device design and electrostatic simulations suggest the strategy to assist electron turning around the junction while remains in the QD in conveyor potential. In the presence of charged defects, a strong confinement is required whereas adjusting the screening gate locally is of more favorable to decrease shuttle amplitude due to the thermal budget concerns.

This dissertation establishes conveyor-mode shuttling as a viable pathway toward a scalable architecture for quantum chips. The demonstrated high-fidelity electron transport across micrometer-scale distances in Si/SiGe devices addresses key scalability requirements for fault-tolerant quantum computing. Systematic studies of material induced disorders through shuttle tomography and theoretical modeling reveal that local electrostatic potential variations and valley landscape affect the shuttle fidelity, identifying disorder and valley-splitting agnostic shuttling as key routes for performance optimization, while backgate-enhanced valley splitting offers an outlook for the future works. The T-junction extension marks the next essential step toward scalable two-dimensional qubit networks. These advancements position conveyor-mode shuttling as a promising candidate for realizing the million-qubit interconnects required for practical quantum error correction. The methodologies and device architectures presented here provide a framework for scaling semiconductor-based quantum processors while leveraging existing semiconductor manufacturing infrastructure.

ZUSAMMENFASSUNG

Die Suche nach universellen fehlertoleranten Quantencomputer erfordert innovative Lösungen. Quantenfehlerkorrektur (QEC) erweist sich als ein Kernstück, um den fehlertoleranten Quantencomputer unabhängig von Implementierungsplattformen zu realisieren, allerdings Millionen gekoppelter Qubits benötigend sind. Ein skalierbarer Ansatz zur Verbindung dieser Qubits wird kritisch. Spin-Qubits in elektrostatisch-definierten Quantenpunkten (QDs) in Halbleitern, insbesondere Si/SiGe-Heterostrukturen, sind vielversprechende Kandidaten wegen ihrer miniaturisierten Strukturen und Kompatibilität mit gegründeten CMOS-Fertigungstechnologie in der Halbleiterindustrie. Diese Fortschritten ermöglichen die kohärente Transferieren den verteiltern Qubits in einer skalierbare Vernetzung.

In dieser Dissertation wird ein effizienter und skalierbarer Mechanismus zur Verbindung von Qubit-Trägern (Elektronen) - nämlich die Conveyor-mode shuttling - erklärt und demonstriert. Dabei werden Elektronen in einem sinus-Förderbandpotential (Conveyor-potential) bewegt, das aus einer Reihe von elektrostatisch-definierter QDs in Si/SiGe besteht. Nur vier Sinus-signale mit sequentieller $\pi/2$-Phasenverschiebung erzeugen das Conveyor-potential periodisch. Eine Geräteimplementierung, genannt Quantenbus (QuBus), wird vorgeschlagen und hergestellt, die sich über 10 μm erstreckt, mit Ziel der Verschiebung zwischen Qubits in einer skalierbaren Spinqubit-Architektur (SpinBus). Eine Kombination aus E-Beam-Lithographie mit hohen Energie von 100 keV und Metall-Lift-off-Prozess wurden QuBus-Prototypen mit einem Gatter-Pitch von 70 nm (vergleichbar mit dem 10-nm-Knoten in der Halbleiterindustrie) gefertigt. In dieser Probe sind die Gatter zum Shutteln der Elektronen in vier Gatter-Gruppen verbunden, zwar eine Steuerungskomplexität unabhängig von der Shuttledistanz erlaubt.

Es wird das Conveyor-mode shuttling von Einzelnelectronen über 19,2 μm (bidirektional in der QuBus Probe) mit einer hohen Fidelität von $(99,7 \pm 0,3)$ % demonstriert, ebenso wie der Transport frei wählbarer Elektronenfiguren (bis zu 34 Elektronen), was die Skalierbarkeit des Conveyor-mode shuttling in Si/SiGe QuBus belegt sowie seine Fähigkeit, als Register für mehrere Elektronen zu zeigen. Die Skalierbarkeit hängt jedoch auch von der Homogenität der Potentialprofil ab, welche hauptsächlich durch die Trägermaterialien limitiert wird, wie z.B. Ladungsstörungen an Oxid-Halbleiter-Grenzflächen, Defekte in Si/SiGe-Heterostrukturen und Legierungsunordnung die zu Valley-splittings führen in Si/SiGe. Diese Herausforderungen werden in dieser Dissertation präsentiert.

Erstens wird die Shuttle-Tomographie Methode entwickelt, um experimentell die Potentialunordnungen entlang des QuBus-Geräts zu untersuchen. Durch das Benchmarking der Potentialimperfektionen und der lokalen Shuttle-fidelity entlang des QuBus bietet die Shuttle-Tomographie eine alternative Charakterisierungsmethode, um das Potentialprofil eines langreichweitigen Kopplers, also des QuBus-Geräts, zu erfassen. Zweitens werden die Defektunordnungen in Si/SiGe in der nähe von den eingeschlossenen Elektronen theoretisch untersucht. Ihr starken Coulomb-interaction mit den Elektronen

während des Transports wird hauptsächlich disskutiert. Die zeitlaufgelöste Anregungen von Orbitalzuständen werden untersucht, um die Korrelation zwischen Defektdichte und Anregungswahrscheinlichkeit zu finden, die schließlich zur Shuttle-infidelity beitragen kann. Im Rahmen von Valley-splitting wird ein neuer QuBus-prototyp präsentiert, bei dem ein Backgate eingeführt wird, das durch ein einstellbares lotrecht elektrisch Feld das Valley-splitting verstärkt.

Schließlich für skalierbare 2D-Qubit-Netzwerke wird eine T-junction benötigt, die als Drei-Wege-Knotenpunkt für Qubits dient um der linearen QuBus zu erweitert. Die Gerätekonstruktionen und Elektrostatische Simulationen zeigen einen Strategie auf, wie Elektronen in QDs durch die Kreuzung gelenkt werden können, während sie im eigenen QD bleiben. Wenn es Ladungsstörungen gibt in der nähe des T-junction, ist eine starke Konfinierung notwendig, wobei jedoch das lokale Anpassen des Screeningsgatter günstiger ist, um die Shuttle-Amplitude zu reduzieren, wegen thermischen Budgetprobleme.

Zusammenfassend etabliert diese Arbeit Conveyor-mode shuttling als vielversprechenden Ansatz für skalierbare Quantenchips. Der demonstrierte hoch-fidelity Elektronentransport über mikrometergroße Distanzen in Si/SiGe Proben erfüllt wesentliche Skalierbarkeitsanforderungen für fehlertolerante Quantumcomputer. Systematische Studien zur Potentialunordnungen in den Trägermaterialien durch Shuttle-Tomographie und theoretisches Modellieren zeigen, dass lokale Variationen des elektrostatischen Potentials und der Valley-landscape die Shuttle-fidelity beeinflussen, wodurch störungs- und Valley-Splitting-bewusste Shuttle als haupt Ansatz zur Leistungsoptimierung identifiziert wird. Und das Backgate-verstärkte Valley-splitting gibt einen Ausblick auf zukünftige Arbeiten. Das T-junction markiert den nächsten wichtigen Schritt um die skalierbare 2D-Qubit-Netzwerke zu implementieren. Die Ergebnisse positionieren das Conveyor-Modus-Shuttling als einen vielversprechenden Kandidaten zur Realisierung von Millionen-Qubit-Verbindungen, die für praktische QEC notwendig sind. Die vorgestellten Methoden und Gerätearchitekturen liefern einen Rahmen zur Skalierung von Quantenprozessoren auf Halbleiterbasis unter Nutzung bestehender Halbleiterfertigungsinfrastruktur.

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ACRONYM DEFINITION

Table 1: **Abbreviation list**

Abbreviation	Meaning
QuBus	Quantum Bus
QD	Quantum dot
QEC	Quantum error correction
TLF	Two-level fluctuator
2DEG	2 dimensional electron gas
LZT	Landau-Zener Transition
CB	Conduction band
CV	Conveyor-mode (shuttling)
BB	Bucket-brigade mode (shuttling)
VS	Valley splitting
1DEC	1 dimensional electron channel
EBL	E-beam lithography
RIE	Reactive-ion etching
CVD	Chemical Vapor Deposition
MBE	Molecular-beam Epitaxy
APT	Atom probe tomography
RTP	Rapid thermal processing
BEOL	Back-end-of Line
FEOL	Front-end-of Line

Table 2: **Parameter and variable list**

Symbol	Meaning
d_{ch}	The channel width of optimized QuBus and T-junctions.
W_{G}	The width of clavier gates
W_{P}	The gate-pitch of clavier gates
T_{Ox}	The thickness of oxides for gate-electrodes isolation
d_{2DEG}	The depth of 2DEG measured from the top surface of Si-cap layer.

1

INTRODUCTION

La brevità della vita.

As idealized two-level quantum systems, qubits preserve the quantum information coherently while quantum gates operate on qubits for computational tasks. However, noisy reservoirs always couple to such fragile systems resulting in decoherence and eventually leading to errors, known as quantum errors. It is believed that the operation of a fault-tolerate quantum processor demands millions of coupled high-fidelity qubits incorporating with proper quantum error correction (QEC) algorithms. Not only the scalability of the platform hosting qubits, but also the interconnections among qubits are of crucial importance for such an implementation. This dissertation will focus on one of the most critical tasks: the scalable long-range interconnections of qubits by conveyor mode shuttling of electrons demonstrated by gate defined quantum dots in Si/SiGe heterostructure. This implementation underscores a promising approach for a scalable architecture (the SpinBus architecture) based on conveyor mode shuttling concept, and it leads to a pathway towards a scalable quantum processor. In the following chapters, the materials challenges, device fabrication and characterization are covered, incorporating the experimental evidences as well as theoretical studies.

1

1.1. A PLAYGROUND OF QUANTUM COMPUTING

THE playground of quantum computing becomes diverse and blooming in the noisy intermediate-scale quantum (NISQ) era. Semiconductor-based quantum processors remain compelling despite recent advances by competing platforms. Superconducting systems achieved quantum supremacy in 2019 [1, 2], and trapped neutral atom arrays recently demonstrated groundbreaking results [3]. The key advantage of semiconductor platforms lies in their scalability potential. Their miniaturized qubit footprints enable integration of millions of qubits without exponentially increasing the processor's physical dimensions.

The physical dimension per qubit in semiconductors can be miniaturized down to $100 \times 100\,\mathrm{nm}^2$ in the case of the Loss-DiVincenzo single spin qubits [4], whereas $5 \times 5\,\mathrm{m}^2$ [5] and $100 \times 100\,\mathrm{m}^2$[1] [6] area are expected for confining billions of qubits in superconducting and ion-trapped platforms, respectively. For the same amount of qubits, QDs in semiconductors are the most scalable system that can be in principle manufactured. Such an optimism originates from its compatibility with developed modern fabrication techniques of classical electronics that allows an integration of transistors with an effective density with hundreds of million trillions transistors per square millimeter such as the N3 technology node of TSMC [7].

Beyond its miniaturized footprints, the characteristics of spin qubits in semiconductors platforms are remarkable as well in particular those confined by the gate defined QDs in Si/SiGe heterostructures. Given the long coherence time of electron spin qubits in Si-based platforms comparing to those in GaAs, those account for the weak spin-orbital coupling and the low hyperfine interaction between electron spins and the nuclear spin reservoirs, Si-based materials have the possibilities to be further isotopically purified (i.e. ^{28}Si enriched) so that the coupling to the nuclear spins in the hosting materials can be further suppressed. In all, semiconductor based quantum processors in particular the Si/SiGe heterostructures are the most promising host of qubits for constructing the fault-tolerate quantum processor.

1.2. QUANTUM DOTS IN SEMICONDUCTORS

MEANS of implementing qubits within semiconductors have been explored and developed over decades [8–14]. Fundamentally, strong confinement restricts electrons to spatial dimensions comparable to their de Broglie's wavelength, $\lambda_{\mathrm{dB}} = h/p$, which is set by the elecron momentum and thus its kinetic energy and effective mass in the hosting material. This confinement makes discrete quantum states available for encoding qubit states. A quantum dot (QD) is such an artificially made system for confining electrons within a potential well, owing to its sub-micrometer diameters that is comparable to the scale of electron wavefunctions. To be not confusing with the widely used irradiative QD, which rewards the Nobel Prize in Chemistry in 2023, the acronym QD in this thesis only refers to the gate defined QD in semiconductors that hosts electrons as for quantum computing.

QDs in semiconductors especially in Si/SiGe heterostructure confine electrons in all spatial dimensions in a planar structure. This confinement is incorporated by firstly

[1] Owing to the demands of 23×23 ultra-high vaccum chambers

stacking a thin layer of Si with a typical thickness of 10 nm in between $Si_{0.7}Ge_{0.3}$ alloys, forming a strained Si quantum well layer in such a Si/SiGe heterostructure, then depositing metallic gate electrodes on the top of this heterostructure. The former layer stack restricts motions of electrons in a two-dimensional plane namely the two-dimensional electron gas (2DEG) by means of the band energy offsets between Si and SiGe (see details of band structures in Ch. 2 Sec. 2.2.1). The latter induces gate-defined QDs on the 2DEG plane that further confine electrons laterally. By varying the gate voltages, the occupancy of QDs and the motions of electron in QDs can be well controlled (see discussion of quantization conditions of QD in Si/SiGe and its motions in Ch. 2).

1.3. THE DEVIL'S IN THE DETAILS

DESPITE of all aforementioned advantages of QDs in semiconductors for quantum computing, the devil's in the details holding off the neck of the development and the research community. On the upscale of quantum processors, addressing and controlling an individual qubit efficiently is one of the bottleneck regardless of the hardware platforms. In particular, wiring control lines for spin qubits in semiconductors are more challenging due to its inherent compact that a monolithic array of millions of qubits needs interconnections of sub-millions layers, which is known as the fan-out problem. [15]

Numbers of architectures have been proposed to achieve the demanded addressability with efficient control by utilizing for instance a cross-bar architecture [16], a dense qubit array [15], a sparse qubit array [17] and a conveyor-mode shuttling based SpinBus architecture [18]. One of the corner stones of almost all aforementioned architectures is the long-range coupling of qubits. Though some of the architectures inherently solves this problem by increasing the complexity of control electronics [19] or hybridizing photonics mode of superconducting microwave resonators with spin qubits [20]. Coupling qubits over long-range without complicating the architecture remains challenging.

The conveyor-mode shuttling concept is one of the most promising approaches to realize an approximately uniform transport of single electrons over long distance in the scale of 10 μm foreseeable with spin coherence. High-fidelity short-range conveyor-mode charge shuttling [21] and spin shuttling [22] have been demonstrated on two prototypes of QuBus devices. Additionally, the 19.2 μm long-range charge shuttling exceeding a shuttle fidelity of $99.7 \pm 0.3\,\%$ has been achieved [23], aiming at the long-range coupler of qubits in SpinBus architecture. However, the imperfections for instance the charged defects and valley splittings in Si/SiGe heterostructures emerge the bottleneck of conveyor-mode shuttling in a scalable architecture i.e. the SpinBus architecture.

Crucially, QuBus devices sharing the same physics principle as all semiconductors based quantum processors those suffering from the noise. The noise sources involving charge noise and spin noise [24] can be introduced both passively by the hosting materials and actively via the qubit control. They will eventually lead to the decoherence of qubits which is the dominant issue of quantum computing. In the context of shuttling electrons, charge defects are the main obstacles on the pathway of shuttled electrons. Details of the materials limitations are covered by Ch. 2, Sec. 2.2.2.

Homogeneity of qubits over large scale is another figure of merit for benchmarking the performance of a quantum processor. The valley-splitting of electrons is an inher-

ent property of Si-based materials that may holds off the performance of spin qubits as well. It is sensitive to the atomistic details at the Si/SiGe interface where electrons are strongly confined. A randomly fluctuating valley splitting is thus another main decoherence source of spin qubits especially when an electron is shuttled over long distance. This fluctuating valley splitting E_{vs} can range from 20 μeV to 300 μeV [25–28], and sometimes even 0 μeV [29]. Methods to prevent it by enhancing E_{vs} are carried out within Ch. 2, Sec. 2.2.2 from the perspective of its origins and in Ch. 3, Sec. 3.3.2 from the perspective of the device design and fabrication processes.

1.4. THESIS OUTLINE

IN this dissertation, the corner stones of the SpinBus including QuBus and T-junction for shuttling electrons are investigated and reported in the respects of their manufacturing and performance benchmarking. The former one includes mainly the fabrication techniques within the availability of an academic clean-room utilizing metal liftoff technique incorporating with e-beam lithography (EBL), the latter presents the functionalities of the shuttle device and observed bottlenecks. Consequently proper solutions are proposed and demonstrated provided corresponding theory studies in order to answer the questions about **3S** those are the scalability, simplicity and susceptibility:

- Why can a proper coupling mechanism provide the **scalability** of spin qubits?

  The quantum bus (QuBus) spanning over 10 μm is one of the most promising candidates among many of proposed mechanisms for coupling multiple qubits. It provides the possibility and the high fidelity of shuttling electrons in conveyor-mode in a Si/SiGe heterostructure independent of the shuttle distance. The working principle of conveyor-mode shuttle of single electrons is explained in **chapter** 2. In addition, such a long-range coupler for shuttling electrons bi-directionally over 19.2 μm distance releases the space among qubits enabling the integration of classical control electronics. Incorporating a three-way interconnection i.e. the T-junction, it makes the shuttling of qubits in a 2D sparse qubits networks possible with only tiling up a unit cell which in turn establishes a scalable architecture namely the SpinBus for the future quantum processor implementation. In the **chapter** 3, the manufacturing processes of them are reviewed combining with optimizations of the most critical processes yielding high performance devices.

- How to control millions of qubits while maintaining the **simplicity**?

  As being reviewed in **chapter** 2, the conveyor-mode shuttle of electron has a simplicity that is independent of shuttle distance as well as the number of shuttled electrons. The experimental demonstrations of bi-directionally shuttling a single electron over 19 μm distance and shuttling of arbitrarily chosen patterns represented by upto 34 electrons, are presented in **chapter** 4. The latter, the demonstrated micron-scale connectivity function enables multiple electrons being transported simultaneously with the same control simplicity as for a single electron. Moreover, the conveyor-mode shuttling based SpinBus architecture scalably tiles up the unit cell consisting linear QuBuses and T-junctions. It provides a perspective to interconnect millions of qubits on quantum processors.

- How much do we understand about the **susceptibility** of spin qubits against the environment?

  In the presence of unwanted electrostatic imperfections, the performance of long-range coupling for single- and multiple electrons are preserved and able to sense the fluctuations of the realistic electrostatic potential by means of the conveyor-mode shuttle tomography method. Corresponding experimental evidences and discussions are presented in the **chapter** 5.

Beyond the linear QuBus devices, the T-junction interconnecting two perpendicular QuBuses as a three-way intersection enables a scalable architecture based on conveyor mode shuttling. The prototypes of T-junction have been manufactured by similar recipe as for the QuBus and its working principle are studied from simulation perspectives. In the **chapter** 6, the working principle and challenges of operating a T-junction are presented incorporating with an exploration of pulsing optimizations providing an outlook of the operating conveyor-mode shuttle for T-junction devices.

Finally, conclusions in **chapter** 7 summarize the significance and development of the conveyor-mode shuttle of electrons followed by a broad outlook of the development of this research field in the near future.

2

LARGE SCALE SPIN QUBIT SHUTTLE

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Johannes Bernoulli

This chapter reviews the concept of shuttling spin qubits as a strategy to overcome connectivity and scalability challenges in semiconductor quantum computing. Motivated by the demands of quantum error correction, qubit shuttling for interconnecting distant qubits is an essential implementation in scalable fault-tolerant quantum architectures. This chapter firstly focus on the electrons shuttling in conveyor-mode due to its simplicity and scalability. Its device implementation relies on the QuBus in Si/SiGe heterostructures whose advantages over other materials like GaAs and SiMOS are reviewed meanwhile addressing the critical material limitations of SiGe, such as the valley splitting the charged defects. The origin of valley splittings in Si is briefly reviewed and two types of charged defects are discussed. First, those populated in oxides are examined presenting their influence on the orbital states for shuttled electrons in conveyor potential. Then, defects in bulk materials in the vicinity of the shuttle trajectories are studied thoroughly by estimating the critical defect density in SiGe in the case that probabilities of shuttled electrons being excited still satisfying the demands of QEC. With the review of the material imperfections in SiGe, this chapter will provide an overview for the most critical obstacles of electron shuttling in conveyor-mode in SiGe QuBus.

SCALABILITY of qubits is a critical challenge in quantum computing, especially when addressing the demands of quantum error correction (QEC). Quantum systems are inherently fragile and prone to various sources of error, such as control inaccuracies, and the influence of its coupling to environmental noise. These errors can quickly pile up over quantum computations, necessitating active error correction faster than its accumulation to maintain coherent operations within a computational task. Implementing robust QEC requires massive scalability and high qubit connectivity [30, 31], as error correction schemes like the surface code demand millions of physical qubits to redundantly encode and protect logical qubits against errors [5]. Achieving this scale requires the efficient coherent linking of large quantum registers while maintaining low error rates [15].

Spin qubits in semiconductor quantum dots, particularly in group IV systems such as Si/SiGe heterostructures, offer promising advantages such as long coherence times [32] and compatibility with existing CMOS technology [33, 34]. However, achieving the scalability required for effective QEC operations presents significant challenges. For instance, the need of nearest-neighbor exchange interactions for two-qubit gates operations limits connectivities among qubits, making it difficult to scale up to the millions of qubits necessary for fault-tolerant computation. Without a method to enable controlled interactions between distant qubits, the wiring complexity, cross-talk issue and the accumulation of errors becomes unavoidable and critical [15, 16, 35], underscoring the need of innovative solutions such as the spin-qubit shuttling to couple distant qubits coherently with high fidelities and ultimately maintain the high performance of quantum computing incorporating QEC.

Shuttling qubits addresses aforementioned constraints by enabling the physical relocation of spin qubits over long distance. This capability allows distant qubits to interact without needs of complex coupling networks such as converting spin qubits to flying qubits [36–38] or cavity-mediated interactions [20, 39, 40], but directly moving the qubits physically within a predefined architecture such as the cross-bar architecture [16], the SpinBus architecture [18] and the Spiderweb architecture [17], etc. Consequently, shuttling spin qubits offers a scalable solution to interconnect qubits among large quantum registers such as the sparse qubits array that ensures robust qubit operation against cross-talk [15, 17]. Two primary methods for shuttling spin qubits, those are the shuttling in bucket brigade (BB) mode and the conveyor (CV) mode, have been widely investigated in theory [41–43] and experimentally demonstrated [21–23, 44–46]. The BB mode involves sequential tunnelings of qubits between adjacent quantum dots (QDs) i.e. adiabatic Landau-Zener transitions (LZT), requiring precise control of detuning between adjacent tunnel-coupled QDs, which can increase the operational complexity for scalable architectures [43]. In contrast, the conveyor-mode shuttle does not require an array of tunnel-coupled QDs, while uses a propagating sinusoidal potential in the one-dimensional channel (1DEC) to shuttle electrons smoothly (no tunnelings involved) with minimal control complexity i.e. the number of input signals is independent of the shuttle distance. This method ensures higher fidelity and coherence by avoiding adiabatically modulating detuning between tunnel-coupled QDs as in the BB-mode, making it the preferred approach for scalable quantum architectures.

In this chapter, the concept of conveyor-mode shuttling and the mechanism of operation is briefly reviewed in Sec. 2.1, highlighting its advantages regarding its control

simplicity along with the flexibility of its operational mechanisms. Then, the device implementation of conveyor-mode shuttle using a quantum bus (QuBus) in Si/SiGe heterostructures is discussed in Sec. 2.2, focusing on the hosting material properties (see Sec. 2.2.1) and a discussion of critical material limitations in SiGe (see Sec. 2.2.2), such as charged defects and the valley splitting. Corresponding strategies to mitigate these challenges by operating QuBus in conveyor-mode to support large-scale, high-fidelity qubits shuttling are introduced briefly from theoretical perspectives. Details of experimental demonstrations can be found in Ch. 4 and in Ch. 5.

2.1. THE CONVEYOR-MODE SHUTTLE

THE conveyor-mode shuttle is a method for spin qubit shuttling where a propagating potential transports the spin qubit confined in a moving QD. The propagating potential composing an array of QDs is formed by applying a number of phase shifted sinusoidal signals to the gate electrodes. In this approach, electrons are transported adiabatically and coherently over distance along with the propagating potential instead of tunneling among QDs as in BB-mode shuttle.

The intrinsic periodicity of CV potential allows for efficient qubit transport over long distances with minimal control operations. According to the phase shift between input signals, a number of gate electrodes can be connected to the same input signal (i.e. the same electric potential) such that the number of input signals is independent of the shuttle distance ensuring the control simplicity which is essential for solving the fan-out problem in scalable architectures. In the case of conveyor-mode QuBus, every four gate electrodes can be connected together, if input sinusoidal signals are shifted by $\pi/2$ as shown in Fig. 2.1 **a**. In this implementation, the input signals $V_{\mathrm{S_i}}(t)$ applied to the gates $S_i (i = 1,2,3,4)$ read,

$$V_{\mathrm{S_i}}(t) = A_S \cos\left(2\pi f t - \frac{\pi(i+1)}{2}\right) + B_s + \Delta B_s \frac{1+(-1)^i}{2} \tag{2.1}$$

where A_S denotes the confinement strength of the conveyor potential created in the 1DEC. B_S and ΔB_S are DC offsets for accumulating charges in the conduction band in the 1DEC, accommodating different distances of the gate sets from the 1DEC.

If three gate sets are used instead, it provides the least number of input signal, however leads to a rough potential as a result. On the other hand, using more than four gate sets would smooth the propagating potential towards a sinus function at all shuttle times, while with a cost of more complex gate design and gate connectivity. In addition, more input signals provide the flexibility to modulate the barrier shape in a QD array by implementing the conveyor potential with two-tone of input signals [46]. For example, a second sine wave with a halved frequency modulates the shape of barriers between adjacent QDs due to the destructive interference between two tones of input signals (see Fig. 2.1 **b**). Each gate set consists of eight gates whose applied voltages $V_{\mathrm{S_i}}(t) (i = 1,2,\ldots,7,8)$ read:

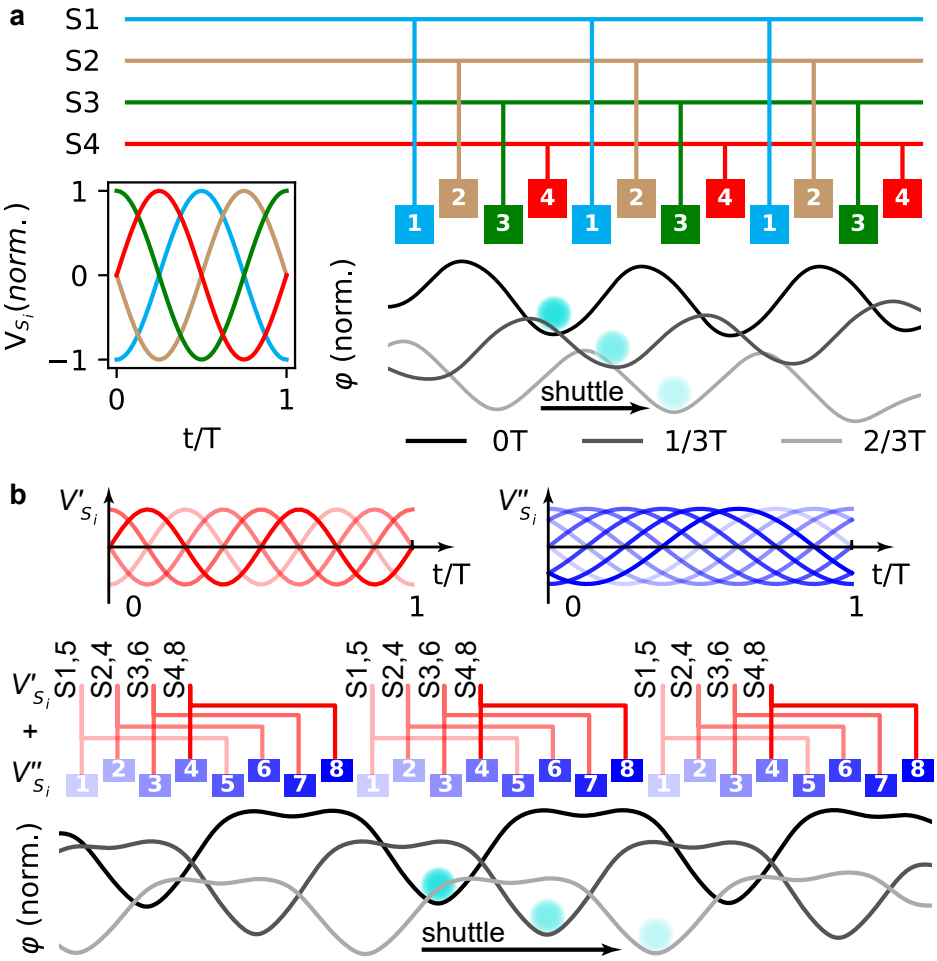

Figure 2.1: **Conveyor-mode shuttle concepts: a**, Schematics of the single-tone conveyor-mode shuttle with its control pulses and the electrostatic potential. The input signals $V_{S_i}(t)$ are applied to the gates $S_i (i = 1,2,3,4)$ with proper circuits connections. Colors of clavier gates in the circuit match with pulses shown on the left. The normalized conveyor-mode potential φ are simulated and plotted below with offset for better visibility. Grey scales here correspond to $t/T = 0, 1/3, 2/3$, where T represents the time for one shuttle period. **b**, Schematics of the two-tone conveyor mode shuttle with decomposed control pulses and the resulting conveyor potential. The input signals V'_i (red) are applied to the gate pairs $S_{i,i+4} (i = 1,2,3,4)$, and V''_i (blue) are applied to all clavier gates $S_i (i = 1,2,\ldots,7,8)$ as being colored in the equivalent circuit in the middle. The conveyor potential superposed by V'_i and V''_i are plotted at bottom using the same grey scales as in **a** for $t/T = 0, 1/3, 2/3$. The light blue ball in both potential plots in **a, b** represents the position of a shuttled electron at given time t. The shuttle direction is labeled by the arrow.

$$V_{\mathrm{S_i}}(t) = V_i' + V_i'' + B_s + \Delta B_s \frac{1+(-1)^i}{2} \tag{2.2}$$

$$V_i' = A_S' \cos\left(2\pi f t - \frac{\pi((i \mod 4)+1)}{2}\right) \tag{2.3}$$

$$V_i'' = A_S'' \cos\left(\pi f t - \frac{\pi((i \mod 8)+1)}{4} + \varphi_0\right) \tag{2.4}$$

where V_i', V_i'' correspond to the conventional sinus input signal and the one with halved frequency tone, respectively. φ_0 represents the relative phase shift between two tones of input signals determining the initial position of the potential minima in a gate set. A_S', A_S'' share the same concept as A_S in Eq. 2.1, while not directly represent the confinement strength in the 1DEC which is in fact given by their combination instead as being expressed in Eq. 2.2.

Fig. 2.1 **b** illustrates such a phenomena where gates S_i and S_{i+4} $(i = 1,2,3,4)$ share the same input signal (V_i') in pair meanwhile the sinus pulses with halved frequency (V_i'') are applied to $\mathrm{S}_{1,2,\ldots,7,8}$ with $\pi/4$ phase shift. In this approach, the tunnel coupling between neighboring QDs is strongly suppressed making the shuttling process more robust against the disordered potential, although doubling the number of input signals comparing to the one-tone conveyor. Nevertheless, the number of input signals is still a constant preserving the independence of shuttle distance. Moreover, composing six gates in a set could make two tones of conveyer potential as well. However, introducing a prime number into the periodicity leads to the difficulty that two paired gate electrodes on different layers i.e. different capacitive coupling to the QDs exhibit the same applied voltage. Different from the argument in the case of monotone conveyor potential consisting three gates, two tones potential encounters with potential symmetry resulting from alternating layer of gates with the same phase. For this reason, the smoothness of conveyor potential is modulated by the layer difference thus forming asymmetric QDs, although six gate sets with 60° makes one complete period of shuttle potential.

In summary, the conveyor-mode shuttle presents a scalable and robust approach for spin qubit shuttling and its particularly advantageous for long-range qubit transport in large-scale quantum computing architectures. Its ability to maintain coherent and adiabatic transport with the tunnel-free mechanism makes it a promising solution for high-fidelity qubit shuttling over long distances. The flexibility in gate signal design including the single-tone and the enhanced two-tone configurations offer the operational stability without drastically increasing the complexity. Regardless the shuttle distance of spin qubits, the control complexity of input signals remains constant resolving the fan-out problem for millions of qubits interconnections. These features position the conveyor-mode shuttle as a foundational technology for commuting qubits among sparsely distributed qubit arrays in scalable quantum processors.

2.2. ELECTRONS SHUTTLE IN SIGE

BEYOND the conveyor-mode shuttle concept that naturally ensures a high shuttle fidelity of spin qubits [21–23, 43], the Si/SiGe heterostructure plays an important role

as a promising hosting material [47, 48] due to its low spin-orbit coupling [49–51], eliminated hyperfine interactions [52, 53] and compatibility with advanced CMOS fabrication techniques [33, 34, 54]. This section starts with an overview of all aforementioned material properties followed by a discussion of its limitations including the charge defects and valley splittings that are impactful for the qubits performance particularly in qubit shuttling experiments. The Si/SiGe QuBus device, specifically designed for the conveyor-mode shuttle of electron spin qubits, will be introduced afterwards. This will be detailed by studies on the QDs in the conveyor potential, which are essential for understanding its working principles and constraints. Eventually, the conveyor-mode shuttling of electrons using QuBus presents capabilities to address the material challenges by mapping the disordered potential and valley splitting, which makes the QuBus in Si/SiGe not only a long-range qubit coupler, but also a useful tool to characterize and benchmark the performance of hosting materials. In this section, the working principles of the methods are discussed from theoretical perspectives, while the experimental demonstrations are presented in Ch. 4 and Ch. 5.

2.2.1. SI/SIGE HETEROSTRUCTURE

The Si/SiGe heterostructure are typically engineered by combining silicon (Si) and germanium (Ge) at the atomic level through advanced growth techniques such as Chemical Vapor Deposition (CVD) and Molecular Beam Epitaxy (MBE). The resulting layer stack consists of a thin Si quantum well (QW) that is sandwiched between two layers of $Si_{0.7}Ge_{0.3}$ alloy named SiGe barrier and SiGe buffer. Due to the band offsets between Si and $Si_{0.7}Ge_{0.3}$, a confinement along the growth direction z (see the conduction band edge in Fig. 2.2 **a**) allows for the population of electrons at the Si/SiGe interface between the SiGe barrier and Si QW layer referred to as two-dimensional electron gas (2DEG). This configuration hosts high-mobility electrons which can be further laterally confined by gate-defined QDs eventually allowing for qubit operations.

The performance of spin qubits in Si/SiGe heterostructures directly links to the transport properties and characteristics of the hosting materials. Though many of initial quantum computing experiments have been demonstrated on group III-V heterostructures such as GaAs/AlGaAs, migrations to group IV heterostructures like Si/SiGe are appealing as their nuclear-spin-free nature eliminates the unavoidable hyperfine-induced decoherence in group III-V materials. Comparing to the abundant isotopes with nuclear spins in GaAs, even natural Si consisting of spin-zero isotope (^{28}Si) at 92.23 % significantly eliminates the hyperfine interactions that limit the qubit coherence in normal GaAs/AlGaAs systems. The coherence time of spin qubits in Si/SiGe can be further enhanced by isotopic purification to reduce the concentration of ^{29}Si [56–58] as low as (50 ± 20) ppm [55].

Despite apparent advantages of Si/SiGe compared to group III-V materials, Si/SiGe systems exhibit intermediate electron mobilities on the order of 10^5 cm$^2 \cdot$s/V [59, 60]. While GaAs/AlGaAs heterostructures typically demonstrate mobilities two orders of magnitude higher, this is primarily attributed to the much lower effective electron mass in GaAs. In addition, GaAs/AlGaAs systems are not strained, in contrast to the strained Si QW in Si/SiGe heterostructures, which can introduce scatterings at interfaces. More specifically, the transversal effective mass of electrons in Si (that is $m_t^* = 0.19 m_e$ where

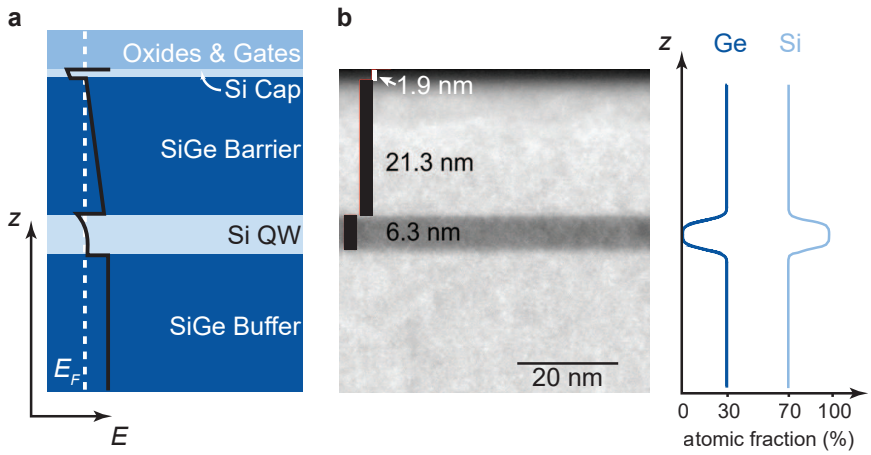

Figure 2.2: **Si/SiGe heterostructure. a** Schematics of a Si/SiGe heterostructure showing the layer stack and the band structure along the growth direction z. The solid black line represents the conduction band edge, while the dashed white line denotes the Fermi energy E_F. The 2DEG forms at the upper Si/SiGe interface leading to the band bending. **b** A scanning transmission electron microscopy (STEM) measurement of LSRL Si/SiGe heterostructure operated at Leibniz IHP (Frankfurt an der Oder), where the thicknesses of Si-cap, SiGe barrier and Si-quantum well layers are inspected. **c** The atomic fraction of Si and Ge species along the growth direction are presented in percentages. The shown results are reproduced according to an atom probe tomography (APT) measurement in Ref. [55]. In this plot, the ingredients of Si and Ge atoms above SiGe barrier layer are not shown.

m_e is the free electron mass) is significantly larger than that in GaAs ($m_e^* = 0.067 m_e$). This larger effective mass in Si results in more localized electron wavefunctions with shorter de Broglie wavelength, which permits greater energy level spacing in similarly sized QDs. However, achieving the same orbital splittings in GaAs would require reducing the dot size (and hence the gate pitch) that challenges the fabrication processes. In Si-based systems, the need for dense gate layouts imposes advanced and mature fabrication processes, and the the CMOS compatibility of Si/SiGe platforms enables high-precision and scalable gate patterning.

Additionally, materials such as ZnSe/ZnMgSe offer a promising alternative: they are valley-free and can be isotopically engineered to be nuclear spin-free. However, despite their favorable electronic properties, these II-VI materials face practical limitations, such as challenges in forming low-resistance ohmic contacts, which currently hinder their viability for scalable quantum dot implementations. [61]

2.2.2. MATERIAL LIMITATIONS

There are intrinsic material imperfections in SiGe heterostructures at atomistic level remaining challenging and should be addressed. Charged defects in semiconductor devices can act either as fluctuating sources of charge noise or as static scattering sites contributing to the potential disorder. The former with fluctuating occupancy lead to time-dependent electric fields that contribute to dephasing and decoherence of spin qubits hosted in semiconductors [62–65]. Whereas the latter creates spatial variations

(spanning from atomic level to sub-micrometers) in the electrostatic potential that deforms QDs and affects device tuning and electron shuttling. Reported investigations reveal that these imperfections are generally originated from remote charged impurities at the interface between the semiconductor substrate and oxides [66, 67], unintentional dopants [68], strain induced QDs [69] and surface roughness where 2DEG is confined [70]. Moreover, the valley splitting is a natural feature of strained Si QW in the Si/SiGe heterostructure that can significantly impact spin coherence. In particular, the magnitude of valley splitting in Si/SiGe heterostructures ranges from 20 to 300 μeV [25–28] depending on the atomistic details of the interface between Si-QW and SiGe barrier layer. In our QuBus devices, nearly zero valley splitting has been measured [29]. Without precise controls over the valley degree of freedom, the spin coherence in a large-scale quantum processor becomes inhomogeneous due to the valley-spin interactions. Therefore, increase valley splitting becomes a natural option. Efforts to enhance valley splitting through epitaxial engineering have also been explored by optimizing the growth stack of SiGe heterostructures such as introducing a Ge-spike in Si QW [71], the wiggle-well implementation [72] and introducing shear strains [73, 74]. These developments highlight the need for further research into atomistic and structural details of SiGe heterostructures.

Atomistic sources of spin decoherence in SiGe are hardly addressable statistically due to limited devices yields and tuning overheads. Industrial approach could brute force it leveraging advanced patterning techniques and the cyro-prober reported by Intel [34]. In fact, both charged defects i.e. the disordered electric potential and valley splittings are addressable by the shuttling electrons in the conveyor-mode. Recent researches [23, 29] reveal that the conveyor-mode shuttling is a useful tool for characterizing the atomistic material properties of SiGe systems and applicable for large-scale quantum processors leveraging the scalability of the conveyor-mode shuttle concept. In the following context, the focus will be on charged defects and the valley splitting in Si/SiGe systems from a theoretical perspective.

CHARGED DEFECTS

Charged defects in semiconductor quantum devices, particularly in SiGe heterostructures, significantly impact the performance and scalability of spin qubits. The characteristics of charged defects in SiGe heterostructures are complex and are commonly addressed as charge noise associated with two-level fluctuators (TLF) [75]. Depending on the dynamics of these defects, they can contribute to either an inhomogeneous disordered electrostatic potential or act as a localized fluctuating electric field. Consequently, the confined electron in a QD experiences lateral displacement due to Coulomb interactions. In term of spins, despite the negligible spin-orbital coupling in Si preserving the electron spin from direct coupling to the electric noise, the lateral displacement of QD in fact changes the renormalization in the electron g-factor. In the presence of a magnetic field gradient that is used for qubit operations, the charge noise can be a source of spin dephasing depending on its magnitude and the gradient of magnetic fields [57].

Origins of charge defects are diverse and they need to be carefully addressed. In most semiconductor devices, charged defects are often located at the interface between semiconductors and oxides due to imperfections during the oxidation process [66, 76–78]. In Si/SiGe heterostructures, this interface refers to the surface between Si cap layer and the

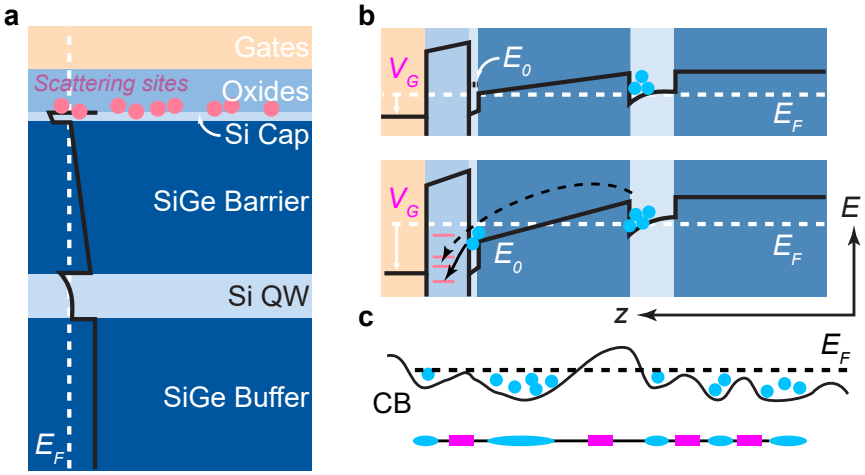

Figure 2.3: **Charged defects in Si/SiGe heterostructures. a** Schematics of charged defects appearing as scattering sites (pink balls) in Si/SiGe heterostructures mostly located at the interface between oxides and the Si cap layer. **b** Band structures of Si/SiGe heterostructures with different gate configurations (i.e. gate voltages V_G). With the V_G approaching the threshold voltage for accumulating charge carriers in Si QW, the eigenstate with energy E_0 (black dotted bar in Si cap) remain unoccupied. When a more positive voltage is applied, energy levels in Si cap layer are lower than the Fermi energy E_F. Defects states deep in the bandgap (pink bars in oxides) can be occupied by electrons in Si QW and most likely in Si cap layer via tunnelings (dashed arrows). **c** A pictorial sketch of the electron percolation in one dimension representing localized states of electrons i.e. "puddles" (blue ellipse) are resistively coupled (pink boxes) in the presence of the disordered potential which prevents the formation of a metallic conducting channel. In the sketch, E_F refers to the fermi-level and the CB is the short for the conduction band bottom.

first dielectric layer. For quantum devices in Si/SiGe, these defects typically manifest as remote scattering sites [66, 79] that are occupiable (see Fig. 2.3 **a**), which in general can be modeled by ensembles of TLFs following the $1/f$ spectrum referring to the charge noise [80–82]. Given that the 2DEG at the upper Si/SiGe are separated from these origins of charged noise by a layer of SiGe, it is already advantageous over quantum devices in Si-MOS systems where 2DEG at the Si-Oxides interface encountered with charged defects severely. However, these charged defects contribute to the electrostatic potentials, though most of them are frozen out at cryogenic temperatures.

These charged defects practically manifest the gate hysteresis in turn-on voltages and slow charge drifts that degrade device stability and amplify charge noise [83]. One of the intuitive picture is the occupation of defect states at the semiconductors-oxides interface. In presence of a positive gate voltage (V_G) for accumulating electrons, the conduction band (CB) is slanted due to the induced electric field along z-axis as shown in Fig. 2.3 **b**. As the V_G is swept closing to the threshold voltage for accumulating 2DEG in Si QW, defect states at the Si cap-oxides layer, normally referred as interface traps are more likely occupied by electrons. These trapped charges shift the electrostatic potential landscape near the quantum well, leading to a shift in the turn-on threshold voltage and the gate hysteresis. Given these states locating deeply in the bandgap, they are unlikely to be excited by thermal fluctuations at low temperatures unless warming up to room temperature. This effect therefore constrains the tuning range of gate voltages to avoid gate hysteresis while rising the tuning overheads.

The occupation of these defect states also significantly affect the 2D transport properties of quantum devices operating at few electrons level. The electrical transport properties including the mobility and the percolation density are commonly used to benchmark the disorders in the host material. However, the mobility peaks at high carrier density exceeding the operational regime for gate defined quantum dots. And the percolation density, which refers to the minimum required density to establish metallic conduction by overcoming charge trapping in the disordered potential, is more relevant [84]. In particular, the defects here result in "puddles" of electrons (see Fig. 2.3 **c**) that rises critical and non-trivial scenario to operate quantum devices in SiGe at single electron level i.e. one needs to maintain sufficient electron density in the 2DEG while avoiding excessive gate voltages V_G that may charge the defects.

Studies also shown that these defect states introduce slow, low-frequency relaxation dynamics [83]. Attempts to optimize the hosting materials have been reported benchmarking eliminated charge noise. For example, a minimum charge noise at 1 Hz is measured to be $(0.29 \pm 0.02)\,\mu\text{eV}/\sqrt{\text{Hz}}$ in Si/SiGe systems by employing thin Si QW (5 nm) and using amorphous Si-rich termination instead of the epitaxial Si cap [85]. Efforts on optimizing the layer stack underscores the importance of reducing defect states and charge noise especially for large-scale quantum devices and its component for instance the long-range coupler. However, those are far beyond the interests of this dissertation. Within this dissertation, I will stay with the conventional Si capped Si/SiGe heterostructures for the shuttling experiments where charge defects are unavoidable while with limited amounts. For the constrains of shuttling experiments due to charged defects, theoretical studies of interactions between limited amounts of charged defects and shuttled electrons will be discussed based on the device design i.e. SiGe QuBus in the Sec. 2.2.3.

VALLEY SPLITTING

Besides limitations in heterostructure, the bulk Si has its own limitation resulting from its crystalline structure. The conduction band of Si has multiple minima in the momentum space named valleys, typically located along the cubic axes of the Brillouin zone. The conduction band in bulk Si is six-fold degenerated. In Si/SiGe heterostructures, the valley degeneracy is lifted by the in-plane tensile strain in Si QW due to the lattice mismatch between Si and SiGe layers. This leads to a splitting between the four-folded Δ and twofold Γ levels with an energy difference of 200 meV [86]. With the band offset between Si QW and SiGe and the electric field along z-axis, the twofold Γ valleys are further broken into two nearly degenerated levels with significantly small energy difference in the order of tens to hundreds of μeV (see Fig. 2.4 **a** for details). The energy difference between these valleys, specifically the energy difference between the lowest two z-valleys is termed valley splitting E_{vs} as valleys in x, y-axes are not bounding states in terms of Si/SiGe heterostructures, and thus out of our interests. As shown in Fig. 2.4 **b**, the four-folded valley states are higher than the potential well defined by the energy discontinuity at the $Si/Si_{0.7}Ge_{0.3}$ interface that is typically 170 meV. Within the Si QW, only the z-valleys remain that is relevant to the interest of our studies.

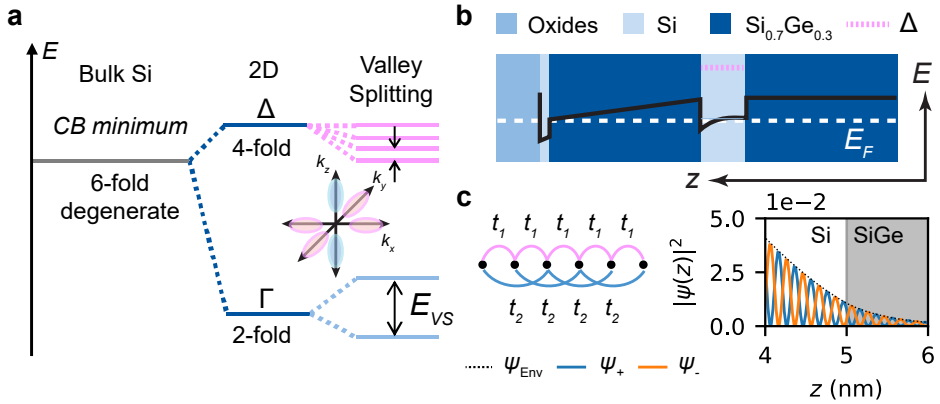

Figure 2.4: **Valley splitting in Si/SiGe heterostructures.** **a** Valley degeneracy of Si in strained Si/SiGe heterostructures. The sixfold energy levels of bulk-Si are splitted by the tensile strain in Si QW into the fourfold Δ band (pink) and twofold Γ bands (blue). **b** The conduction band edge in Si/SiGe heterostructures. The Δ band (pink dashed line) are not confined by the potential well in Si and only twofold valleys (blue) along the growth direction z remain within the Si QW layer. **c** Solving valley states using tight-binding model which includes only the nearest neighbor hops ($t_1 = 683$ meV) and the next nearest neighbor hops ($t_2 = 612$ meV). The electron wavefunctions (ψ_+ and ψ_-) involve a slowly varying envelope function (dotted line) and fast oscillations (blue and orange solid lines) associating to the valley states. The phase difference between two fast oscillations is sensitive to the atomistic details at the Si/SiGe interface.

This phenomena can be qualitatively solved by an empirical tight-binding model. Using a two-band approach without the presence of the disorders i.e. by assuming a perfectly sharp Si/SiGe interface, one could model the valley splitting in a simple one-dimensional tight-binding model involving nearest-neighbor and second-neighbor couplings (see Fig. 2.4 **c**). In this simplest 1D model, the wavefunction $|\psi\rangle$ is written as $|\psi\rangle = \sum_n C_n|n\rangle$ in a position basis where $|n\rangle$ denotes the nth atom, and the Hamiltonian

acting on $|\psi\rangle$ reads,

$$H|\psi\rangle = \sum_n C_n \left(t_1|n+1\rangle + t_1|n-1\rangle + t_2|n+2\rangle + t_2|n-2\rangle\right) \tag{2.5}$$

where $t_1 = 683\,\text{meV}$ and $t_2 = 612\,\text{meV}$ are the set parameters for nearest-neighbor and second-neighbor couplings, respectively, so that the minimum of the lower band is located at $q_0 = 0.82(2\pi/a)$ where a is the lattice constant in Si, and the corresponding curvature at this band minimum yields the longitudinal effective mass in Si ($m_l^* = 0.92 m_e$ [53]). Considering a periodic boundary condition ($\psi(j) = \psi(j+2N+1)$ and $C_{n+j} = C_j$), the eigenvalue $E_q = \varepsilon + 2t_2\cos(2aq) + 2t_1\cos(aq)$. In terms of Si/SiGe heterostructures, this chain of atoms can be interpreted as a cell array with two atoms in a cell, and thus yield two bands with energies $E_q^{(1)} = 2t_1\cos(qa/2) + 2t_2\cos(2\pi - qa)$ and $E_q^{(2)} = 2t_1\cos(\pi - qa/2) + 2t_2\cos(2\pi - qa)$, respectively. With a symmetric potential well and a sharp Si/SiGe interface, the eigenvectors with different symmetries read,

$$\psi_{sym} = -2A\sin\left(\frac{q_+ja + q_-ja}{2}\right)\sin\left(\frac{q_+ja - q_-ja}{2}\right) \tag{2.6}$$

$$\psi_{asym} = 2A\sin\left(\frac{q_+ja + q_-ja}{2}\right)\cos\left(\frac{q_+ja - q_-ja}{2}\right) \tag{2.7}$$

The wavefunction of electrons with different symmetries can be decomposed into an identical slowly varying envelope function and a fast oscillating term corresponding to the term with $(q_+ - q_-)$ and the term with $(q_+ + q_-)$, respectively as both q_+ and q_- are close to q_0 hence $(q_+ - q_-) \ll (q_+ + q_-)$. A pictorial illustration in Fig. 2.4 **c** shows the principle of the valley degeneracy due to the phase difference between fast oscillations while the envelope function remains identical. This ideal model depicts an surreal scenario that the QW interface is perfectly smooth. However, the atomic-scale variations near the well boundary make the phase of fast oscillations aligning to the interface differently. The corresponding energies difference between two-lowest valley states are calculated within perturbation theory in powers of $1/S$, where S is the number of atoms in the quantum well [87]. The result shows that the energy difference E_{vs} oscillates with the well width. This sensitive dependence of valley splitting on atomic-scale physics reveals the importance of including realistic atomistic fluctuations into the model, which is not simply solvable by employing higher order models involving multiple bands in terms of tight-binding model.

At the Si/SiGe interface, the atomic-physics such as alloy disorders and a monolayer of atomistic step are of greater interest. The former is originated from the fact that Si and Ge atoms are randomly distributed in lattice sites with a statistical concentration of 30 %Ge in SiGe layers. It results in a Rice distribution of valley splitting with a lower bound down to 0 μeV [28, 88]. The latter i.e. the atomistic step rises from the growth and some unavoidable structural imperfections such as misfit dislocations or the surface roughness. The atomistic step can be as small as a monolayer of Si or Ge atoms, however, it significantly affects the valley splitting. By including more sophisticated atomic-scale details into the model, simulated E_{vs} show greater agreement with the experimental measurements (see Fig. 2.5 **a**).

In terms of spin qubits in Si/SiGe, the atomistic dependencies of valley splittings are significantly impactful. Due to the spin-valley hotspot in Si/SiGe heterostructures as shown in Fig. 2.5 **b**, valley degeneracy provides a potential dephasing source of spins. The spin-valley hotspot seats at the energy where E_{vs} equals to the Zeemann splitting. At this point, the maximal valley-spin mixing in the excited state of a spin qubit leads to a very fast spin relaxation via electron-phonon interaction [89], and thus a leakage channel of the spin state. Moreover, due to the sensitivity of E_{vs} on the atomistic details at the Si/SiGe interface, the spin-valley hotspot exists in a large spectra making it unpredictable in a large-scale quantum processor. In particular, when the spin qubit is shuttled in such a system, the E_{vs} becomes more critical as the electron spin is shuttled across a disordered landscape, and thus the spin coherence encounters with the statistical fluctuations of valley splitting severely. Although, the conveyor-mode shuttle of electrons in Si/SiGe systems provides a useful tool to characterize the E_{vs} based on the device design i.e. SiGe QuBus [29], enhancing the E_{vs} globally is desirable to reliably avoid spin dephasing due to the spin-valley hotspots.

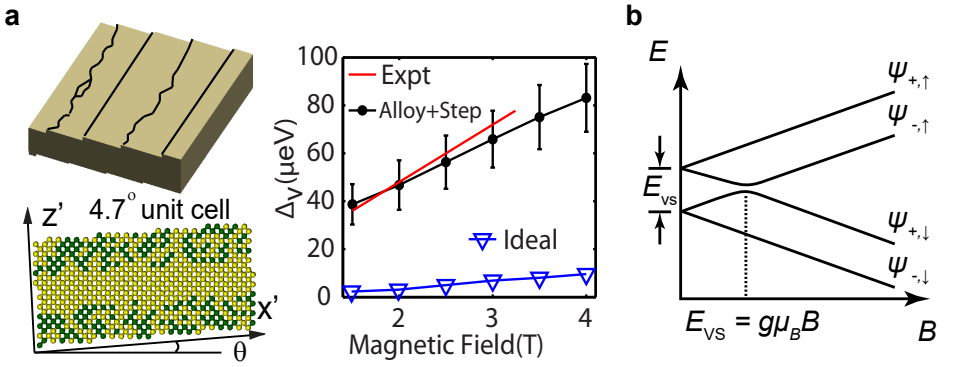

Figure 2.5: **Atomistic dependencies of valley splittings and the spin-valley mixing.** **a** The simulated and experimentally measured E_{vs} in Si/SiGe heterostructures. Based on a complex tight-binding model that includes the slanted Si/SiGe interface (top left panel) and the alloy disorders of Si and Ge atoms (bottom left panel), the simulated E_{vs} (black dots in the right panel) show the agreement with measured E_{vs} (red line). The sketch with 4.7° is used for visualization while 2° is used for simulation representing the miscut. This figure is adapted from [53]. Notably, the ideal case here does not refer to an ideally high E_{vs} but an idealized model corresponding to a free-standing flat and slanted Si QW slab without taking the SiGe buffer layer and alloy disorders into account and hence one order of magnitude lower compared to experimental results. **b** The energy spectrum of spin-valley hotspot. In the presence of a magnetic, an anti-crossing between the spin and valley states at $B = E_{VS}/g\mu_B$ is observed and termed as spin-valley hotspot. Here, + and − in subscripts denote the valley states, while ↑ and ↓ denote the spin states.

The E_{vs} can be influenced by factors such as strain, electric fields, and confinement in low-dimensional materials. Enhancing or tuning the E_{vs} by introducing a Ge-spike in Si QW [71] and the wiggle-well implementation [72] have been demonstrated experimentally (both substrates fabrication and the E_{vs} measurements). In addition, introducing shear strains [73, 74] is also proposed. All these implementations benefit from special resonance conditions of the fast oscillating terms in valley states in the presence

of strain and disorders. However, from the first principle of the valley physics in Si, the corresponding eigenenergy strongly depends on the external electric field that intrinsically exists in the system. With an enhanced electric field along the growth direction, the E_{vs} could be increased. The hindering physics mechanism is rather simple. Given a large electric field along the z-axis, the envelope function of electrons wavefunction in Si QW layer are compressed towards the upper interface between Si QW and the SiGe barrier. With larger overlap with the upper interface, the E_{vs} becomes inevitably larger [90]. The corresponding device implementation will be introduced in Ch. 3 Sec. 3.3.2 where the enhancement of the E_{vs} is achieved by introducing a metallic backgate on the backside of the Si/SiGe heterostructure based on the detailed studies in Ref. [91].

2.2.3. SI/SIGE QUBUS IN CONVEYOR-MODE

By discussing known material limitations, we now move to the device implementation of electron shuttling. Vast of architectures incorporating qubits shuttling concepts are proposed [16–18, 35]. QuBus in SiGe is one of the device implementations for shuttling electron and spin particularly in conveyor-mode over long distances. It serves as an elementary cell in a large-scale quantum processor (the SpinBus architecture) where qubits are positioned sparsely and qubits are only shuttled for demanding operations such as initialization, readout, logical two-qubit gates or qubit swap.

Unlike the implementations of spin shuttling mediated by cavity-qubits [20, 39, 40], the SiGe QuBus shuttles electrons and spin qubits directly [21–23] in conveyor-mode. Leveraging the advantages of SiGe and the adiabaticity of conveyor-mode shuttle concept, the Si/SiGe QuBus relocates electrons and spins in a QD array directly using propagating sinus potential. It consists of an undoped SiGe/Si/SiGe quantum well on top of which three layers of electrically isolated metallic gates are fabricated by electron-beam lithography (EBL) and metal lift-off techniques (see the Ch. 3 for details on the device fabrication). Fig. 2.6 **a** illustrates the core part of the Si/SiGe QuBus. For simplicity, only one side of the QuBus device is shown here as the remaining parts of a QuBus includes only a symmetric SET and repeated gate structure. For shuttling electrons in conveyor mode, three layers of gates are required as decomposed in Fig. 2.6 **b**. This device enables a bi-directional pathway to shuttle qubits 10 μm apart from each other that can be seen as a unit cell of spin qubit array in a quantum processor.

The functional elements of a QuBus device consist of a one-dimensional quantum channel for the interconnections of qubits and two single-electron transistors (SETs) serving for both charge sensing and charge reservoirs. Two 10 μm long grounded split-gate namely the screening gates on the first layer define a nominally depleted one dimensional electron channel (1DEC) in the quantum well. More than 100 clavier gates, equally distributed among the second and third layer above the 1DEC (see Fig. 2.6 **b**) enable the approximately uniform movement of single electrons along the x-direction even in the presence of electrostatic disorder [43]. Notably, every fourth clavier gate is electrically connected to one of four gate sets S_i (i = 1...4). The connection scheme of four gate sets can be easily implemented as our clavier gates are distributed among two electrically isolated layers. At a fixed distance between 1DEC and gate layers, using more than four gate sets would smooth the propagating potential towards a sinus function at all shuttle times and enables the manipulation of barrier profile between QDs as dis-

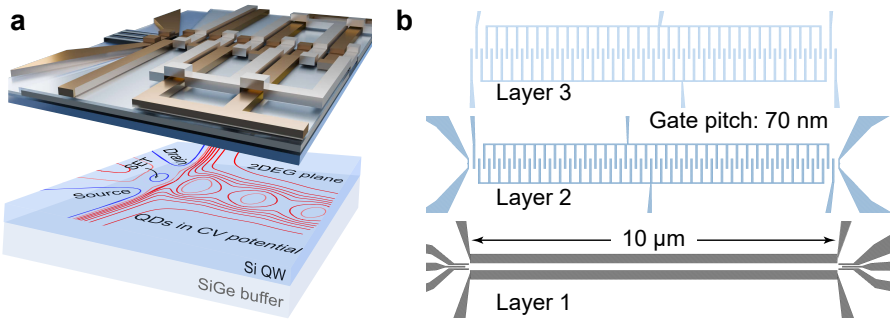

Figure 2.6: **Fine gate structures of the QuBus device: a** The fine gate structure of a QuBus device zooming in to the left SET and the first few periods for the showcase. The 3D structure on top renders geometries above the 2DEG plane, those from top to bottom are clavier gates on layer 3 (silver), SET topgates and clavier gates on layer 2 (golden), screening gates and SET finger gates on layer 1 (grey) and SiGe barrier layer (blue). All layers are insulated by Al_2O_3 (jelly). Corresponding electrostatic potential of the SET and the conveyor-mode shuttling potential are shown as contour plots below. Si QW and SiGe buffer layers are illustrated by blue and grey cubes. Layer stacks beneath SiGe buffer such as a graded SiGe buffer layer and Si substrate are of more interests for wafer growth instead of topics of this dissertation, and thus not shown for simplicity. **b** A complete layout of fine gates for the 10μm QuBus device with a gate pitch of 70 nm. Gate stacks are colored with lighter blue from bottom to top.

cussed in Sec. 2.1 and being demonstrated in Ref. [46]. However, the cost of gate design complexity are significant and the connection scheme strongly bounds to the gate design as well. In this design, only the monotone conveyor-mode shuttle with four gate sets is applicable.

Within the frame and interests of this dissertation, the capability of QuBus devices is discovered to be far beyond simply shuttling electrons. Besides that, the conveyor-mode shuttle becomes a powerful tool to characterize the material properties of Si/SiGe heterostructures such as the potential imperfections (see Ch. 5 for experimental demonstrations) and the valley splittings [29]. In the sections below, we will firstly review how does the QuBus address the material limitations in Si/SiGe systems in particular the charged defects and its impact on shuttled electrons.

2.3. SHUTTLED ELECTRONS IN QUBUS

A shuttled electron in the QD is essentially a single-electron confined in a potential well. In the case of conveyor potential in Si/SiGe, the confinement potential of a QD can be modeled as a two-dimensional potential well since the confinement in z-direction comes from the band structure of Si/SiGe heterostructures as discussed in Sec. 2.2.1. This section will start with a brief review of the simplified model that is the single-electron in a 2D harmonic potential focusing on the characteristics of the conveyer potential and the shuttled electrons in a QD (see Sec. 2.3.1). Charged defects are then included into the model, where a time-independent Schrödinger equation is solved for ensembles of charged defects revealing the impacts of them on shuttled electrons (see Sec. 2.3.2). However, the electrostatic solution appears to be limited to represent the realistic dynamics of the electrons in a shuttling process. Solving a time-

dependent Schrödinger equation is necessary while the model needs to be simplified. In the Sec. 2.3.3, the time-evolution of the shuttled electrons in a conveyor potential will be discussed in the presence of charged defects using the perturbation theory. In this model, only a single charged defect in the bulk material is considered to interact with the shuttled electrons resulting in a qualitatively solvable model and predicting the critical parameters of a defect free channel for the conveyor-mode shuttle.

2.3.1. ELECTROSTATIC POTENTIALS OF QUBUS

We now turn to the detailed studies of the conveyor potential. In a word, the conveyor potential within the QuBus channel consists of a QD array. Assuming a homogeneous QD array for simplicity, each QD in this array shares a two-dimensional parabolic shape that reads,

$$V(x,y) = \frac{1}{2} m_t^* \omega^2 (x^2 + y^2) + V_0 \tag{2.8}$$

where ω is the angular frequency of the confinement potential, V_0 is the depth of the potential well, and m_t^* is the transversal effective mass of electrons in Si. Considering the dimensions of a QD on the order of hundreds of nanometers, the confinement strength lies typically on the order of $\mathcal{O}(10)$ meV (generally lower than that).

In terms of a stationary solution to this model, the time-independent Schrödinger equation $H|\psi(x,y)\rangle = E|\psi(x,y)\rangle$ can be solved analytically, when the Hamiltonian conventionally takes the expression,

$$H = -\frac{\hbar^2}{2m_t^*}\nabla^2 + V(x,y) \tag{2.9}$$

yielding the energy levels of the confined electron in a QD are $E_{n_x,n_y} = \hbar\omega(n_x + n_y + 1)$ where n_x and n_y are the quantum numbers in x and y directions, respectively. As a result, the wavefunctions of the confined electron $\psi_{n_x,n_y}(x,y) = \psi_{n_x}(x)\psi_{n_y}(y)$ where each component takes the form of Hermite polynomials,

$$\psi_j(x) = \left(\frac{m_t^*\omega}{\pi\hbar}\right)^{1/4} H_j\left(\sqrt{\frac{m_t^*\omega}{\hbar}}x\right) e^{-\frac{m_t^*\omega}{2\hbar}x^2} \quad (j = n_x, n_y) \tag{2.10}$$

The ground state shows non-degeneracy as both n_x and n_y are set to zero and the first excited states has the degeneracy of two as either n_x or n_y can take one meanwhile the other takes zero. However, it holds true only when the QD is circular i.e. follows the cylindrical symmetry. In the case of a conveyor potential, the QDs are not always perfectly circular due to many deviations from an ideal device such as the gate layout, the screening effects of the SETs and the charged defects induced potential disorders. The energy levels will inevitably split apart and the level spacing between eigenenergies becomes non-uniform. For this reason, the numerical solution of the confinement potential is required to approach a more realistic model.

Electrostatic potentials of the QuBus device are numerically simulated using COMSOL Multiphysics® [92] based on the gate layout, for instance the 10 μm QuBus as rendered in Fig. 2.7 **a**. The software solves Poisson equation using finite element methods, providing a numerical solution of the electrostatic potential at the 2DEG plane (see

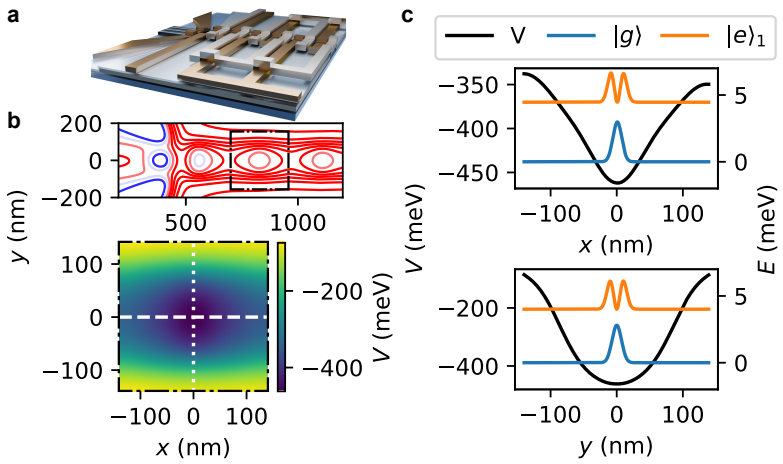

Figure 2.7: **The symmetries of conveyor potential:** **a** 3D model for COMSOL simulation. **b** The simulated electrostatic potential (top) where the first QD for shuttling is selected and highlighted by the dash-dotted box. Zooming-in the simulated potential of the QD_1 (bottom). Two line cuts are taken along the symmetric axis through the centroid (local potential minima) of the selected QD. **c** Calculated eigenenergies and eigenstates along two orthogonal axis in the presence of minor anisotropic shape of potential line-cuts (black). The probability density of two lowest states are shown representing the ground orbital state $|g\rangle$ and the first excited orbital state $|e\rangle_1$ corresponding to the blue and orange lines, respectively. The intensity is amplified by 50-times for visibility without any physical meanings hence not aligning to any axis in the plot. Instead, the secondary y-axis on the right gives the orbital splitting (E_{orb}) with respect to the $|g\rangle$.

Fig. 2.7 **b**). Due to the large dimension of the QuBus device, solving the complete device is computationally expensive and including too much redundancies out of interests region. Thanks to the periodicity and symmetry of the device design, only an SET and the first few periods of clavier gates are included into the model sufficiently describing the principles. As shown in the simulated electrostatic potential of the conveyor-mode shuttle (the top panel of Fig. 2.7 **b**), the shape of potential well appears to be non-uniform (i.e. an ellipse-shape instead of a perfect circle in the contour plot). We now select the first ellipse-shaped QD for the further calculations not only due to its better symmetry, but also due to the fact that the QD next to SET is used for loading and readout instead of shuttling. The tunnel-coupling between SET and the SET design are based on simulations from Ref [93] and will be not discussed in this work in details. A zooming-in view of the selected QD for this work is shown in the bottom panel of Fig. 2.7 **b**.

By slicing the potential along both x and y axis (see Fig. 2.7 **c**), it is obvious that the curvature of QD in two orthogonal directions are different, and thus the energy levels of the first excited state of the confined electron in a QD are splitting due to the anisotropic dot shape. For the studies on corresponding eigenenergies, instead of studying actual eigenenergies, the energy spacing termed orbital splitting (E_{orb}) is adapted here referring to the energy spacing with respect to the ground state. For the minor anisotropic shape, the calculated E_{orb} along two axis differs in the scale of sub-meV (see Tab. 2.1). Therefore, the precise calculations of the E_{orb} in the conveyor potential needs to take all dimensions into account, and the simplified one-dimensional solutions are only indicative instead

Table 2.1: **Calculated orbital splitting (E_{orb}) along axis:** The minor anisotropic geometries along two symmetric axes result in different eigenenergies. Only the lowest four eigenenergies are listed for the showcase. The subscript j of the quantum number n_j takes x and y for individual column, respectively. In this example, relatively large voltages are applied to the clavier gates $A_S = 280$ mV. The following parameters: $W_P = 70$ nm, $T_{Ox} = 10$ nm, $d_{ch} = 200$ nm and $d_{2DEG} = 35$ nm are used for modeling the device.

n_j	$E_{\mathrm{orb}\,x}$ (meV)	$E_{\mathrm{orb}\,y}$ (meV)
1	4.46	4.01
2	8.85	8.15
3	13.16	12.36

of qualitative.

Moreover, the shape of a QD depends on the applied gate voltage and its geometries evolves during shuttling. The former is typically referred to as an artificially tunable parameter termed the shuttle amplitude A_S. The latter can be characterized by tracing the centroid of a QD and the tops of its adjacent barriers. As an example, two scenario are considered corresponding to the shuttled QDs propagating along with the conveyor potential and the static QD providing electrostatic confinements for electrons. The propagating QD helps us to understand the dynamics of QDs in a shuttle process and the static QD in the conveyor potential focus on the confinement strength for electrons depending on the shuttle amplitude A_S. The gate voltages of all electrodes for the simulation are chosen so that the simulated electrostatic potential φ at the 2DEG layer is sufficiently close to the realistic potential in the experiments in Ch. 4 and Ch. 5 for consistency reasons.

QDs ON HOLD

Firstly, we examine the characteristics of QDs in the conveyor potential in the static case to start off. It is in principle a snapshot of a propagating conveyor potential. This simulation helps to understand the confinements of conveyor potential without the present of disordered potential revealing the intrinsic characteristics of electrostatic potentials along the QuBus. With different applied gate voltages (see Fig. 2.8 **a**), the conveyor potential preserves its periodicity, while drastically drops in the barrier height between adjacent QDs. To better interpret the simulated results, subtractions of local minima (i.e. centroids of QDs) and local maxima (i.e. tops of barriers between adjacent QDs) are helpful (see Fig. 2.8 **b**). Regardless of A_S, QDs for confining shuttled electrons are sparsely separated by $\lambda = 280$ nm as intended (see detailed discussions of the dot centroids subtractions in Appx. A, Sec.A.1).

However, with a close look at the results shown in Fig. 2.8, the shape of barriers between QDs varies at different A_S. Particularly, additional unwanted QDs appear within the barrier regions at lower A_S resulting in the splittings of detected barriers (see Fig. 2.8 **b** when $A_S < 50$ mV). In this simulation, the separation of barriers between QDs is the intrinsic characteristic of the conveyor potential attributed to the difference capacitive coupling of clavier gates on different layers. It is not related to any disordered potential.

In addition, the conveyor potential on the left of the QuBus (see Fig. 2.8) appear to be tilted. Detailed estimations of the energy minima between adjacent QDs (see Appx. A, Sec.A.1) can provide the detuning along the QuBus channel. Comparing to a detun-

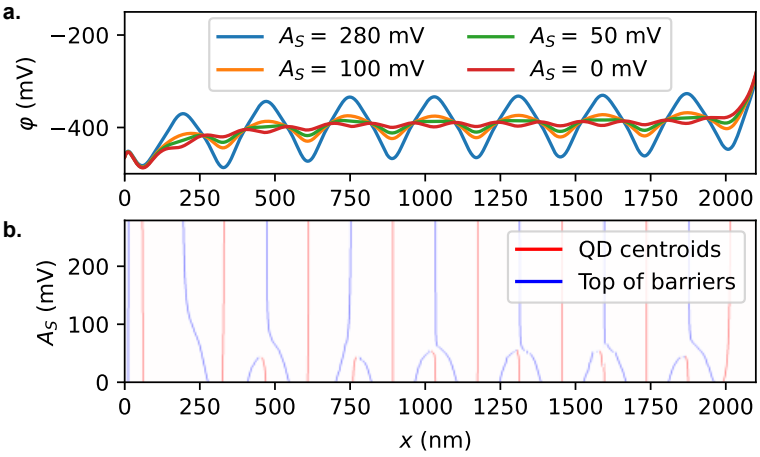

Figure 2.8: **QDs in a conveyor potential**: **a**, the conveyor potential with different A_S applied. The results are simulated by COMSOL Multiphysics® [92] using the same gate layout as shown in the Fig. 2.7 but extending the clavier gates for few more periods. Eight QDs confined by the conveyor potential are shown. Four typical A_S are picked for visualization and sorted in a descending order. **b**, the centroids of each QD (red solid lines) and the tops of its adjacent barriers (blue solid lines) as a function of A_S. Due to the additional stationary points are found in the barriers while reducing the A_S, the splitting of barriers (discrete blue lines) and an insertion of new dots (short vertical lines in red) are expected at lower A_S.

ing between QD_4 and QD_5 of ≈ 1 meV. The detuning between left most two QDs i.e. $QD_{1,2}$ is one order magnitude higher (≈ 15 meV), although an experimentally maximal $A_S = 280$ mV is applied. This behavior is unavoidable due to the screening effect of the charge reservoirs. The conveyor potential along the x-direction is inevitably slanted in particular for the first few QDs. Interestingly, on the other hand, a reduction of the A_S should reveal the inherent background potential of a conveyor potential. Consequently, this finding leads to the shuttle tomography method to map the potential disorders in the conveyor potential. The corresponding experimental demonstrations are reported in Ch. 4 and Ch. 5.

SHUTTLED QDS

In principle, the conveyor potential should propagate smoothly, however, the movement of QDs in a propagating conveyor potential is not necessarily smooth so does the dot size. Despite of the periodicity of conveyor potential preserving the homogeneity of QDs in the conveyor potential (see snapshot of the potential within in one period in Fig. 2.9 **a**), an obvious nonlinearity of the QD centroids in 1λ (see Fig. 2.9) occurs to all QDs revealing the fact that the shuttled electrons in each QD experience inhomogeneous accelerations within one period during a shuttling process. Similarly, the size of QDs varies during shuttle as well. It can be seen as a breathing QD during shuttle meaning that the confinement provided by the conveyor potential intrinsically varies over time. This variation is affected by both the clavier gates width (W_G) and the depth of Si QW (d_{2DEG}). Detailed simulations and discussion of this topic has been reported in Ref. [43]. In a nutshell, the confinements of electrons in conveyor depend on the capacitive couplings

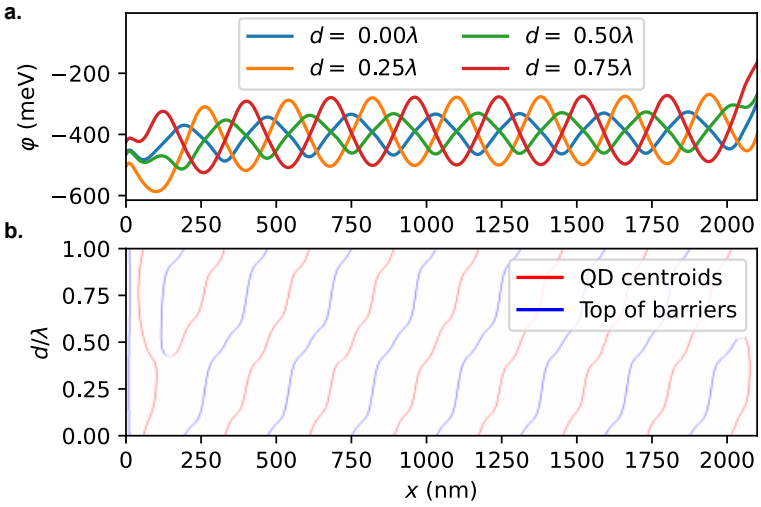

Figure 2.9: **Shuttled QDs in a conveyor potential**: **a**, the moving conveyor potential with different shuttle distance d. A snapshot of the propagating conveyor potential φ along the channel (x-direction) is taken for every quarter of 1λ. The confinement is provided by the experimental maximal $A_S = 280$ mV. **b**, the trajectories of centroids of each QD (red solid lines) and the tops of its adjacent barriers (blue solid lines) for 1λ.

between gates and QDs. It needs to be parameterized in both the distance to the 2DEG and the physical dimension of gate electrodes or equivalently the dimension of one shuttle period (λ). In the case of this simulation, $W_G = 70$ nm corresponds to an optimized capacitive coupling, whereas the energy difference between two orbital excitations signifies. Thus a deterministically breathing within one λ is observed as expected, even though the disordered potential is not yet introduced.

2.3.2. SHUTTLED ELECTRONS AND CHARGED DEFECTS

The ideal electrostatic potential φ_i in a SiGe QuBus device is always perturbed by the disordered potential φ_d, and thus the realistic electrostatic potential can be expressed by the superposition of both terms i.e. $\varphi = \varphi_i + \varphi_d$. The existence of φ_d leads to a more complex electrostatic potential challenging both the charge shuttle fidelity and the spin coherence. To further study the interplay between charged defects and shuttled electrons in the conveyor potential, let's firstly focus on the randomly distributed charged defects at the interface between silicon and oxides, which are the dominant origins of the φ_d acting as remote scattering sites for shuttling process. Here, φ refers to the energy of the center of bandgap in the silicon quantum well where the 2DEG forms.

Now the potential disorders are involved into the simulation as shown in Fig. 2.10 **a**, in which the ideal conveyor potential φ_i is overlaid with defect ensembles marked by red spots. Given a defect density of $5 \times 10^{10}\,\mathrm{cm}^{-2}$ [94], the number of defects within the frame remains significant. In fact, not all defects are equally impactful for the potential. Since the defects plane are close to the screening gates (i.e. only 10 nm beneath due to the thickness of oxides), defects underneath the screening gates areas have minor con-

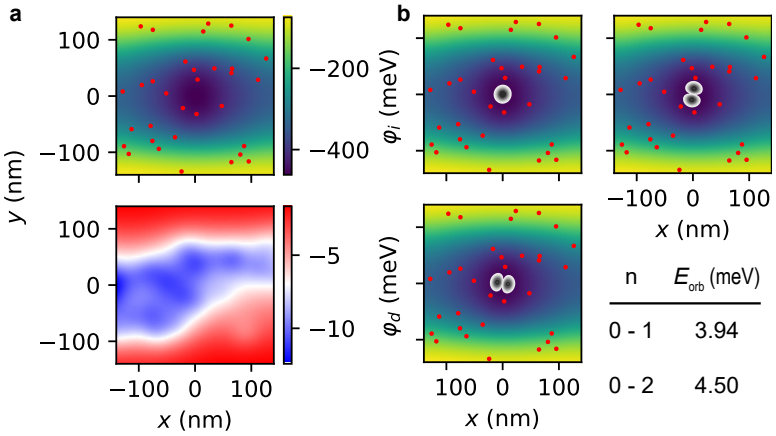

Figure 2.10: **The realistic potential with charged defects: a** The first QD in the simulated ideal conveyor potential φ_i with $A_S = 280\,\text{mV}$ (upper panel). A defect density of $5 \times 10^{10}\,\text{cm}^{-2}$ [94] is assumed and an ensemble of charged defects are randomly placed at the oxide-semiconductor interface. 2DEG is set to be $d_{2\text{DEG}} = 35\,\text{nm}$ from this interface and the $T_{\text{Ox}} = 10\,\text{nm}$ for this simulation. Red spots in the plot indicate their projections on the 2DEG plane. Corresponding induced disordered potential φ_d are shown in the lower panel. **b**. The numerically calculated eigenenergies and eigenvectors of confined electrons in presence of charged disorders. Only the three lowest states are shown here for demonstrations. Calculated orbital splittings are listed at the bottom.

tributions to the potential disorders as they are compensated by the screening effects. However, the potential where the shuttled electron passing through appear to be rough as depicted in the false-color plot of φ_d (see the lower panel of Fig. 2.10 **a**). Despite of a magnitude difference between the ideal conveyor potential φ_i and the disordered potential φ_d in this example, the orbital splitting of shuttled electrons are significantly affected by the disordered potential. Calculated E_{orb} in Fig. 2.10 **b** deviate by hundreds of μeV with respect to the ideal cases listed previously in Tab. 2.1 just by introducing the disordered potential φ_d. Notably, this simulation is based on a relatively large shuttle confinement $A_S = 280\,\text{mV}$ so that the φ_d is an order of magnitude lower than the φ_i. However, lower A_S is favorable for electron shuttling considering the thermal budget of the dilution unit and the unwanted cross-talk.

As being shown in the previous Sec. 2.3.1, a reduced shuttle confinement leads to distortions of shuttled QDs. Fig. 2.11 illustrates this scenario that the electron is shuttled by a much weaker confinement ($A_S = 100\,\text{mV}$) and is shuttled 100 nm to the right from the initial position that was shown in Fig. 2.10. Under these conditions, ensembles of charged defects form a narrow channel at the upper half of the shuttle channel (i.e. $0 < y < 100\,\text{nm}$ in the lower panel of the Fig. 2.11 **a**). Again, the screening effect of the gate electrodes are clearly shown since defects in the range of $|y| > 100$ do not contribute to the φ_d. Only the rest defects within the channel region affect the shuttled electron. When the electron passing through this narrow tunnel perturbed by charged defects, the wavefunctions of electron are trapped obviously by the defect potential located in the upper half of the channel. Consequently, the orbital splitting drops tremendously as

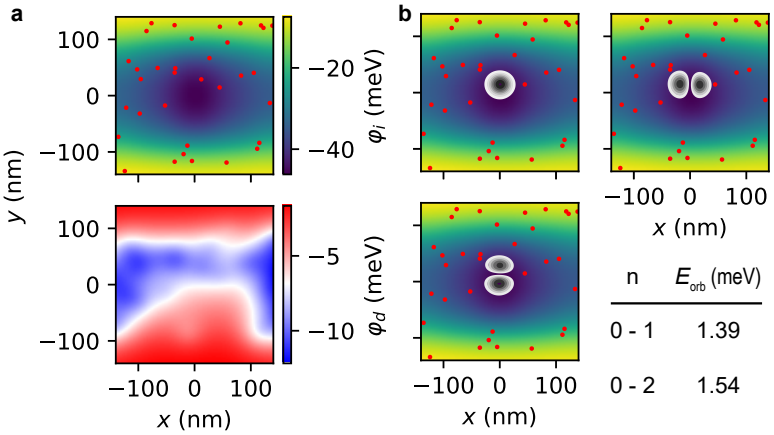

Figure 2.11: **The shuttled electron with weaker confinements: a** Taking the same QD as shown in the Fig. 2.10 while significantly smaller shuttle confinement that is comparable to the disordered potential φ_d after a shuttle distance of 100 nm. **b**. The numerically calculated eigenenergies and eigenvectors of confined electrons in presence of charged disorders. Again, only the three lowest states are shown here for demonstrations. Calculated orbital splittings are listed at the bottom.

shown in the list.

Preserving a high orbital splitting is favorable to tolerate different defect ensembles. In Ref. [43] an $E_{\text{orb}} \geq 1$ meV is proposed as a criteria that is suitable for the optimized geometries ($W_G = 70$ nm and $d_{2DEG} = 45$ nm) at $A_S = 100$ mV. They are similar to the parameters using in this simulation. Although the simulated E_{orb} remain above this threshold value, it does not guarantee the scenario that the shuttled electron remaining in the QD. Experimental evidences of loss of electrons will be presented in Ch. 4 and in Ch. 5.

2.3.3. TIME-DEPENDENT PERTURBATION THEORY

Ensembles of charged defects in the oxides at their interface to the hosting semiconductors have been simulated thoroughly. Given the fact that the orbital excitation due to charged disorders matters only when the shuttle velocity v approaching the orbital excitation rate ($\sim 10^5$ m/s i.e. three orders of magnitudes higher than the targeted v), the orbital excitations due to the charged disorders should not harm the spin coherence of shuttled electrons [43]. However, limited amounts of defects in the bulk Si/SiGe heterostructures could potentially have significant influence on the coherence given their strongly localized Coulomb potentials interacting with the shuttled electrons in a short distance. And the study of this scenario remains uncovered. For this reason, the time-dependent perturbation theory is applied to the system consisting a shuttled electron and a single point charged defect in the vicinity of the shuttle trajectory. With this approach, the defect induced excitations of electrons orbital states is examined by monitoring the time-evolutions of the electron wavefunctions in the presence of defects. Notably, the relaxations are not included in this study as well as the phase errors accumulated during such excitation remains untouched. By studying the probability of defect

induced excitations for shuttled electrons, it aims only at correlates the purity of hosting material to the excitation free probabilities where the purity can be quantified by a defect free channel within in the hosting material so that an electron can be shuttled through without undesired excitations.

Technically, the probability of finding this defect free channel within QuBus devices is probed by calculating the excitation probabilities when the point charged defect is placed closing to the shuttle trajectories. Owing to the periodicity along the shuttle direction and the mirror symmetry with respect to the center of the QuBus channel, it is sufficient to consider a single point charged defect within a cross-section perpendicular to the shuttle direction. Considering the excitations probabilities correlating to shuttle failures as an approximation here, and given that relaxations are not involved in this simplified model hence only one excitation is regarded. The probability of such a channel to be defect free for shuttling an electron should follow the Poisson distribution yielding the defect free probability $P_{\text{defect-free}}$ as,

$$P_{\text{defect-free}} = \exp(-\rho_{\text{defect}} \cdot l \cdot A) \tag{2.11}$$

where ρ_{defect} is the defect density in the bulk material, l represents the desired shuttle distance that is 10 μm, and A is the cross-sectional area of the Poisson channel in the yOz plane. As a result, the required defect free probability can be estimated with a given defect density ρ_{defect} and the demanding shuttle fidelity (for instance 99.9% regarding the threshold error rate for QEC). Detailed simulations and analysis are presented in Ref. [95] and a summary of the methodologies and the key findings are reviewed in the following.

The main goal of this simulation is to investigate the time evolution of electron wavefunctions during shuttling processes in the presence of a single charge defect closing enough to the shuttle trajectory. The time-dependent solutions to this system are calculated based on the solutions of time-independent Poisson Schrödinger problems those were discussed previously in Sec. 2.3.1 to 2.3.2. Firstly, the Poisson equation is solved to obtain the electrostatic potential in the QuBus device including the conveyor potential and the defect induced potential. Secondly, eigenenergies and the wavefunctions of the time independent Schrödinger equation are solved for shuttled electrons in a QD at each sampled time. This step provides stationary results at each time step whereas the time-evolution among each time steps requires the time dependent Schrödinger solver where the adiabatic theorem comes into play. The validation of applying adiabatic theorem demands that the system remains in its instantaneous eigenstate especially the instantaneous ground state and the external perturbation is applied slowly enough. First of all, the relaxation of orbital states is relatively fast with a time scale of ~ 100 ps [96] for the targeting $E_{\text{orb}} \sim 1-2$ meV, given the strong orbit-phonon coupling and significant density of phonon states. Moreover, in the context of the shuttle processes, the optimized shuttle speed 10 nm/ns in earlier theory study [43] is comparably slow enough to satisfy the adiabatic theorem as the targeting E_{orb} corresponds to a frequency in the order of $\sim \mathcal{O}(10^{15})$ Hz. Therefore, the time-dependent Schrödinger equation can be solved by the perturbation theory without taking relaxations into account and treat the defect induced potential as a slowly evolving perturbation with respect to the ideal conveyor potential. The time evolution of the electron wavefunctions can then be calculated by separating the phase term explicitly as, [95]

$$|\psi(t)\rangle = \sum_n \tilde{c}_n(t)|\psi_n(t)\rangle = \sum_n \tilde{c}_n(t)e^{-i\varphi_n(t)}|n(t)\rangle \tag{2.12}$$

where $\tilde{c}_n(t)$ denotes the pre-factors for different instantaneous states $|\psi_n(t)\rangle$ which is decomposed into the time dependent phase evolution $\varphi_n(t) = \frac{1}{\hbar}\int_0^t E_n(t)\,dt$, and the stationary eigenstates $|n(t)\rangle$ calculated by the Poisson-Schrödinger solver at each sampled time. The time-dependent Schrödinger equation to be solved becomes,

$$i\hbar\frac{\partial}{\partial t}|\psi(t)\rangle = H(t)|\psi(t)\rangle \tag{2.13}$$

where the Hamiltonian $H(t) = H_0 + V(t)$ that consists of the Hamiltonian H_0 due to confinements of the conveyor potential and the time-dependent perturbation $V(t)$ representing the defect moving towards the electrons in a QD, if the H_0 is assumed to be time-independent. As a result, the time evolution of the electron wavefunctions is determined by the pre-factors $\tilde{c}_n(t)$ which reads,

$$\frac{\partial}{\partial t}\tilde{c}_m(t) = -\frac{i}{\hbar}\sum_{n\neq m}\frac{\langle m|\frac{\partial V(t)}{\partial t}|n\rangle}{|E_m - E_n|}\cdot\tilde{c}_n(t)e^{-i(\varphi_n(t)-\varphi_m(t))} \tag{2.14}$$

In fact, this gives rise to the probability of a shuttled electron being excited to different instantaneous excited states at time t due to the presence of the defect. To examine this probability, one can calculate the excitation probability for instance from the ground state to the k-th excited state P_{k} ($k = 1,2,\ldots$) as,

$$P_{\mathrm{k}}(t) = |\tilde{c}_k(t)|^2 = 2\cdot\left|\frac{M_k}{E_k(t) - E_0(t)}\right|^2\cdot(1-\cos(E_k(t) - E_0(t))\,t/\hbar) \tag{2.15}$$

where the term $M_k = \langle m|\dot{V}(t)|0\rangle$ corresponds to the Matrix elements in M_{mn} resulting from Eq. 2.14 with $n = 0$ denoting the initial ground orbital state. This equation is valid for the case where the electron is initially in the orbital ground state when the defect is far away from the electron, therefore, the maximum value of $P_{\mathrm{k}}(t)$ estimates the chance of the electron being excited to the k-th excited state due to an approaching point charged defect that would lead to the failure of the shuttle process, though relaxations back to the orbital ground state are not considered yet. Notably that all stationary eigenenergies and eigenstates are solved with a resolution of 16 ns so that the the uncertainty $\Delta t\cdot\Delta E \ll \hbar$ does not break down, and the time evolutions are interpolated with a cubit spline method yielding a resolution of 50 ps (instantaneous energy jitters $\Delta E_{mn} \sim 40\,\mu$eV) in these simulations.

Using aforementioned method, the point charge defect is place in the yOz-plane that is perpendicular to the shuttle direction so that the cross-section of shuttling channel can be evenly sampled. Fig. 2.12 **a, b** present the excitation probabilities when a point charged defect is placed at different positions within the yOz-plane. The sweep along the z-direction set the origin at the 2DEG plane thus having a range of ±30 nm, particularly $z \in [0,30]$ sufficiently map the defect in the SiGe barrier layer that is assumed to be more impactful for the shuttled electron than the defects in oxides. A good symmetry with respect to the 2DEG plane appears as expected due to the same symmetry in the

layer stack. As the point defect closing to the 2DEG plane, its severe impacts on the electron wavefunctions lead to an abnormal data point at $z = 0$ nm as a double dot forms in this condition and the eigenstates are changed thus the adiabatic theorem breaks down. Except for this singularity, P_{01} remains larger than 10 % and 1 % when the defect is placed within the range of ±5 nm and ±11 nm in the z-direction, respectively. Similarly, the sweep along the y-direction shows the radius of 4 nm and 8 nm for the P_{01} to be larger than 10 % and 1 % respectively.

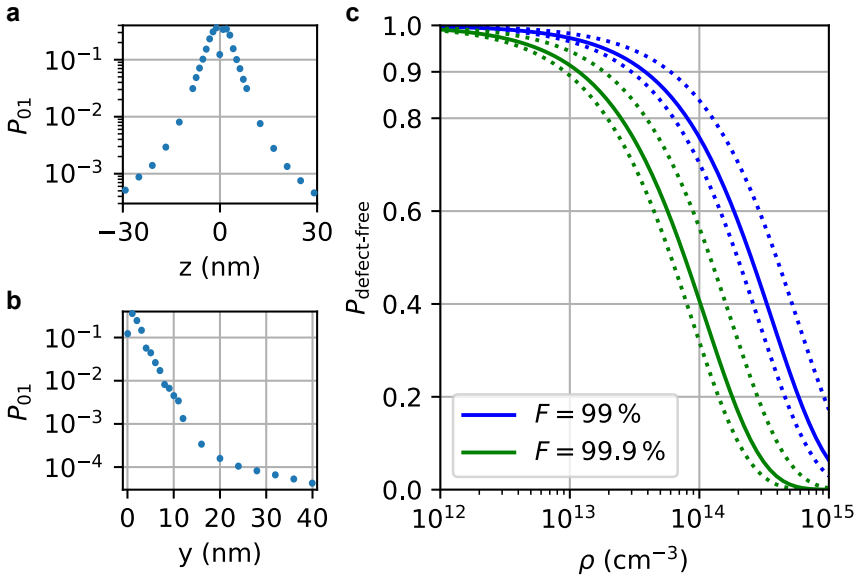

Figure 2.12: **The defect free channel in the presence of a point charged defect:** The orbital excitation probabilities P_{01} in the presence of a point charged defect being placed along **a** the z-direction with respect to the 2DEG plane and **b** the y-direction with respect to the center of the QuBus channel. **c** The defect free probability $P_{\text{defect-free}}$ as a function of the defect density ρ_{defect} in the bulk material at a targeting shuttle fidelity $F = 99\%$ and 99.9% depicted in blue and green, respectively. Three different cross-sectional geometries, those are the rhombic, ellipse and rectangle, have been assumed representing the underestimated (dotted lines above solid lines), intermediate (solid lines) and overestimated (dotted lines beneath solid lines) cross-sectional area A. All shown results are adapted from the bachelor thesis of Nils Ciroth [95].

To correlate these values with observable experimental results, one could assume the most critical case where an undesired excitation leads to a shuttle failure. Therefore the targeting shuttle fidelities of qubits F could correlate to the excitation probabilities as $F = 1 - P_{0\to1}$ which indeed is overestimating the influence of the defects as a pessimistic model without taking the relaxation mechanisms into account. But it provides a upper bound of the failure rates contributed by defects closing to the shuttle trajectories. Given the demanded threshold error rate of QEC, $F = 99.9\,\%$ for shuttling is chosen as well as 99 % according to the state-of-the-art of the electron shuttle experiments corresponding to the $P_{01} = 10^{-2}$ and 10^{-3}. With chosen criteria, the geometrical limitations of finding a defect free channel in the hosting material are bounded by $z = \pm 11$ and ± 22 nm that can be read out from the plots in Fig. 2.12 **a**. And the radius along y-direction are

8 and 13 nm according to the results in Fig. 2.12 **b**. Thanks to the good symmetry along both axes with respect to the center of the QuBus, one can estimate the shape of this cross-sectional area to be a rectangle, ellipse and rhombic bounded by the chose criteria, giving rise to overestimated, intermediate and underestimated cross-sectional area A of the defect free channel to be estimated (see Fig. 2.12 **c**). The shown plot only illustrates the correlation between $P_{\text{defect-free}}$ and ρ closing to the cur-off values. Two extrema in turn suggest a pure enough hosting material for $\rho \leq 10^{12}\,\text{cm}^{-3}$ and low quality one for $\rho \geq 10^{15}\,\text{cm}^{-3}$, which is obvious as the density on the order of $10^{15}\,\text{cm}^{-3}$ corresponds to a doping denstiy in Si. Therefore, in the undoped region of QuBus devices, the region of interests should lay within these two extrema. As a result, if we assume a realistic defect density in Si [94] that it has a defect density not larger than $\approx 5 \times 10^{13}\,\text{cm}^{-3}$, we could find the correlation between the upper bound of the shuttle infidelity and the chance that the shuttled electron does not encounter with any orbital excitations. That means, for instance, when the shuttle fidelity $F = 99.9\,\%$, there is a chance of $P_{\text{defect-free}} \leq 50\%$ that the shuttled electron remains at its orbital ground state and not being excited at all.

This constrained model only gives an overview of the defects influenced shuttling device providing the correlation between the probability of finding a defect free channel (precisely speaking the orbital excitation free probability) for shuttling and the defect density within the bulk hosting material. However, a more complete picture could relief the criteria suggested by this model. For example, the orbital relaxation of electrons is not included in this model yet. The extended work can be found in Nils' master thesis [97]. Moreover, shifting the channel laterally along the y-direction by modulating the applied voltages on screening gates could assistant the shuttled electron "stirring" around a localized charged defect, while the characterization i.e. the pre-knowledge of a specific device is needed. In fact, this strategy is estimated and discussed in Ref. [95] based on the approximation that a lateral shifting of $\approx \pm 50$ nm would not significantly distort the conveyor potential. Further experiments are also demonstrated in Ch. 4 and Ch. 5 hence not detailed here.

3

DEVICE FABRICATION

For one change always leaves a dovetail into which another will fit.

Niccolo Machiavelli

The design of QuBus prototype varies for different purposes of experiments. A sustainable device yield, that is immune to the design variations, improves the efficiency of fabrication processes and fundamentally facilitates further investigations. However, it is always challenging to maintain the device yield under various demanded design changes including material modifications, gate-layout variations and unavoidable process-window fluctuations. On the other hand, they lead to an overhead of tuning and optimizing fabrication processes, whose complexity scales up faster than the device itself. In particular, even higher homogeneity and reproducibility of the fabrication processes are demanded in the case of scaling up the QuBus device such as a T-junction and ultimately the SpinBus architecture. This chapter firstly reviews the integration of the conventional academic approach for QuBus fabrication that is known as the lift-off process. With an overview of its limitations and challenges, corresponding optimizations of critical processes are discussed in details afterwards aiming at manufacturing scalable quantum devices without significant complexity and optimization overhead. Last but not least, additional process developments to overcome the material limitations are briefly introduced in the end to give an outlook for a feasible and viable development routine.

AIMING at shuttling spin-qubits in conveyor-mode with high fidelities, the gate-layout of QuBus has been thoroughly simulated and optimized [43, 93, 98]. Mechanisms including charged disorders, valley splittings, phonon-assistant spin relaxation, etc were investigated suggesting optimal critical parameters such as the gate width of an individual gate-electrode in the clavier gate-sets (W_G) and the oxides thickness (T_{Ox}). However, the model for aforementioned simulations is always idealized by simplifying the charged defects distribution. That means only is the charged defects at the interface between semiconductor and oxides considered and the SiGe heterostructure is treated as a purified system. In reality, manufacturing realistic devices undergoes multiple steps during which process induced imperfections such as pattern misalignment, charged defects are unavoidable, and thus space for adjustments during processing still remains. Moreover, the QuBus devices being fabricated in an academic standard clean-room employs the metal lift-off process incorporating the electron-beam lithography (EBL). Despite of its capabilities of manufacturing different prototypes exceeding 100 gate electrodes per device with the critical dimension (W_G=35 nm) that is comparable to the industrial throughput and even more critical in the aspect of feature size [14, 33, 34, 54, 82], however, any minor changes to the critical processing parameters and their fluctuations during processing eventually lead to unexpected behaviors of final devices as the process window of the metal lift-off process is rather small. Therefore, the standardization and stabilization of an integrated process flow are demanded, after which narrowing down to the optimizations of critical parameters and structures may ultimately produce high-performing QuBus devices with high-yield for shuttling experiments.

The device yield in fact is not an injective function meaning that it is not solvable by only addressing a single variable but multiple factors. A series of criteria should be considered to validate the functionality of the device from which the device yield is evaluated. First of all, the correctly and precisely patterned structures guarantee the expected implementation of design. Second, the robust wiring and connectivity ensure the reliability of the electric characteristics of devices. Finally, the stability of the electric characteristics is of vital importance to justify the sustainability of device for a long-lived quantum experiments.

This chapter focuses on the first two criteria those are the patterned structures and the connectivity to establish the functionalities of QuBus devices as a base line. Firstly, a brief overview of the standardized process represents the state-of-the-art of QuBus fabrication (see Sec. 3.1.1), after which critical processes step to maintain the device yield are listed in Sec. 3.1.2. Details of process optimizations aiming at eliminating the erroneously patterned structures and establishing the connectivity of gate-electrodes are discussed in Sec. 3.2.1 and Sec. 3.2.2, respectively. They are both related to the profile control on-chip and the etching process plays the crucial role here. Therefore, the process optimizations are mainly focusing on the etching methods. In addition, the performance of QuBus devices is improved as well by optimizing the oxides thickness and gate material (see Sec. 3.3.1). Corresponding electric characterizations and the performance benchmarking are discussed and detailed in Ch. 4 and Ch. 5

The third criteria that is the stability of the electric characteristics is only partially involved in this dissertation, although it is an important figure of merit benchmarking the device yield. In fact, the dominant factor affecting the stability relies on the quality

of the oxides quality and the SiGe heterostructure such as the electron mobility, percolation density those need to be optimized during the growth of wafer. The former is involved in fine tuning of the oxides deposition process and the latter, that is the quality of heterostructures, should be characterized in a wafer scale. Instead, this work focuses on the front-end of line (FEOL) to produce the QuBus devices on a well-performed SiGe heterostructure with flexibly changed designs and reliable oxides quality. Corresponding detailed studies and investigations about the massive characterizations of the electric stability of QuBus relevant devices can be found in Ref. [99, 100] and that for qubit devices in general are reported elsewhere [34, 101, 102].

3.1. STATE-OF-THE-ART

QUANTUM devices, for instance the tunnel fall devices from Intel, are widely produced in the industrial pilot lines with a magnificent large throughput due to their capabilities to process 300 mm wafers by advanced manufacturing techniques beyond the institutional cleanroom. The EUV patterning technique is used to pattern the quantum dot gates of tunnel fall devices with a high throughput enabling their investigations of gate pitches from 50 to 100 nm [34], though they are not critical feature dimensions for the EUV lithography. Meanwhile, other processes on 300 mm wafers still incorporate EBL [14, 100, 103] and it is difficult to conclude whether the advanced patterning technique is necessary for the quantum device. Fortunately, leveraging the cutting-edge semiconductor fabrication techniques does not only advance in the device throughput but also the homogeneity as the device-to-device variations have been thoroughly addressed in the case of the homogeneity of billions of classical transistors. Moreover, the quality of gate dielectric get much benefits from the developments of classical electronics as well. Evidences have been seen from a low charge noise quantum dot devices with industrial CMOS manufacturing [82] where a uniform quantum dot operation at the Si/SiO_2 interface at mK temperature is reported providing the reproducibility of scalable high-fidelity qubits. However, the design flexibility is a main challenge for a mature industrial pilot line and that is the playground for the academic fabrication to explore innovative device functionalities with flexibly adjusted designs in a shorter turnaround time for instance the QuBus devices for long-range shuttling of spin-qubits.

3.1.1. PROCESS INTEGRATION OF STANDARDIZED PROCESSES

Processes of QuBus devices had been initiated and developed by Inga Seidler during her research in the group [104], and are stabilized within the frame of this work. To produce functional prototypes of QuBus devices, the material compatibility, gate layouts and the electric characteristics are prioritized to integrate the standardized process. First of all, the material compatibility guaranties the level of contamination during the fabrication processes in order to avoid unwanted leakage path or impurities. In this work, all materials are CMOS compatible within the cleanroom of HNF [105], which include the dopants (phosphorus: P), metallic gates (titanium: Ti, platinum: Pt and palladium: Pd), oxides(aluminum oxides: Al_2O_3) as well as the Si/SiGe heterostructure containing only Si and Ge. Secondly, the gate layout provides the designated electrostatic potential to confine electrons for shuttle experiments. The feature size of gates have to be preserved

for the device integrity and the nature of gate-stack topology has to be preserved for the ease of wiring them out. Particularly, four clavier gates in a QuBus have to be placed on two different layers and fan-out to opposite directions. Finally, the electric characteristics determine the functionalities of a device including the conductivity of the ohmic contacts as well as the isolation among gate electrodes by means of the oxides. All aforementioned criteria have to be preserved during the fabrication of QuBus devices.

Manufacturing QuBus devices has been accomplished in an institutional standard cleanroom for academic researches: the Helmholtz Nano Facility (HNF) which is classified as an ISO 1-3 cleanroom for semiconductor manufacturing [105]. Inclusion of the pattern definition, pattern transfer and the layer deposition techniques, up to 100 mm wafers are generally supplied, those are sufficiently large volume manufacturing (HVM) for the academical scale of investigations. In particular, the fabrication processes of QuBus devices rely on the EBL for defining the most critical gate features (W_G=35 or 60 nm) and the E-beam evaporator for the metallization of gate-electrodes with the demanded thin films thickness ranging from 12 nm to 150 nm. In addition, the ALD oxides are crucially important to provide robust gate isolation. Nontrivial masks including the markers, implantation region, mesa and Ohmic contacts are patterned by optical lithography (OL) using the mask aligner (MA4) whose mercury vapor lamp ensures the patterning of features about 1 μm in the hard contact mode. Finer structures written by EBL uses the Raith EBPG 5200 owing a beam energy upto 100 keV that enables the gate patterning with a resolution down to 10 nm and in principle an overlay of 0.5 ± 2.5 nm. The Leybold Univex 400 evaporates the target metals for gate electrodes including Ti, Pt and Pd those are used for QuBus devices. The gate dielectrics i.e. Al_2O_3 are deposited by the Oxford ALD.

Leveraging all advances of tools in HNF, the process flow for the fabrication of QuBus devices is integrated as follows to maximize the throughput and to simplify the processing complexity. Fig. 3.1 depicts the integrated process flow for the 10 μm QuBus as an example. The complete process flow is categorized into three levels: wafer-, chip- and device-level, sorted by descending physical dimensions. Wafers from different suppliers are firstly diced into $10 \times 10\,\mathrm{mm}^2$ chips. On each chip, 4×4 cells containing different prototypes of QuBus, are organized in a 4×4 chess-board with $2 \times 2\,\mathrm{mm}^2$ size for each cell. This 4×4 configuration resulting in 1 mm margin on all edges that is intended to make use of the uniform thickness of spin-coated photoresist in the center of a chip, which is a critical requirement for the patterning precision during lithography. The final products will be 16 devices being diced out of a chip, and thus one cell in a chip is equivalent to a device. An estimation of the device throughput can be made by simple calculations, for example, maximally 48 chips × 16 devices/chip = 768 QuBus devices can be fabricated on an 100 mm wafer. However, one cell within a chip is practically dedicated to a test structure, typically field-effect transistors (FETs) with only one layer of structure. It is essentially a top-gate bridging over a pair of ohmic contacts with the same working principle as a classical FET. Leveraging its simplicity, it is practically useful for verifying the ion-implantation and the annealing process by measuring the electrical transport properties of FETs. In addition, multiple chips from one wafer or different wafers may be processed together undergoing an identical process flow, thus the number of nominally identically fabricated devices does not bound to the number of devices per chip. To

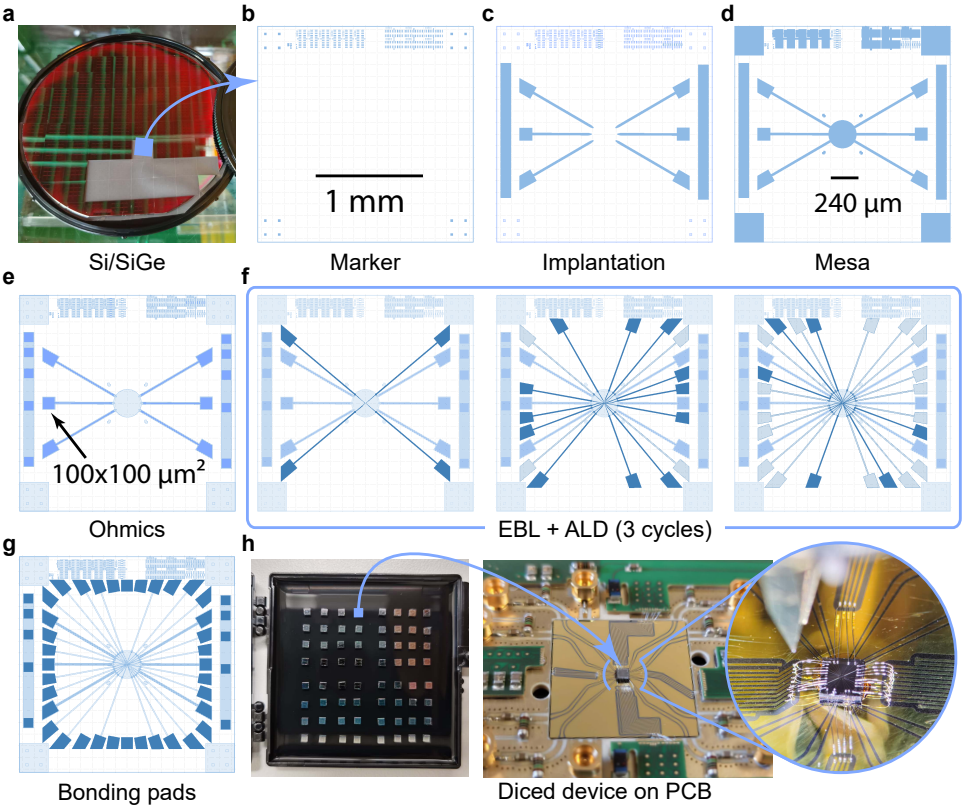

Figure 3.1: **The process integration for** 10 μm **QuBus devices: a** A diced 4-inch wafer (QT477) as an example. 48 chips with dimensions of $10 \times 10\,\mathrm{mm}^2$ can be diced out of it for further processes. **b** Markers for both optical lithography (OL) and e-beam lithography (EBL) on the top center and on four corners, respectively. **c** The exposing areas for ion-implantation. The negative tone photoresist for masking is removed by acetone before the rapid thermal process (RTP) for dopants activation that is operated consecutively and is not shown here. **d** The positive tone photoresist masking areas for mesa etching. The Si-QW under the shaded region remains and uncovered areas are etched into the SiGe heterostructure with a depth of ~ 100 nm. **e** The layout of Ohmic contacts (shaded in flash purple). Three fan-out arms on top of each side of the etched mesa (hatched in light blue) represent the Ohmic contacts for the QuBus device. Square pads on top of two bars on both sides correspond to the transmission line structures for characterizing the contact resistance and sheet resistance on a chip using the transfer length method (TLM). **f** Three-cycles of ALD and EBL for gate isolation and gate-electrodes patterning. Gate-electrodes are metalized by e-beam evaporation and the following lift-off process removes unwanted metal pieces. Three layers of gates are illustrated here interleaving ALD steps and metal lift-off processes. Note that ALD is performed before EBL in each cycle so that Ohmics are isolated and the third layer of gates are not capsulated by oxides. **g** The mask of bonding-pads to enforce the fan-out contacts of gate electrodes including Ohmic contacts and gate electrodes written by EBL on three different layers. Oxides in the shaded areas are wet-etched by 1 % HF to expose metal contacts for reinforcement. 150 nm Platinum (Pt) are evaporated on top of corresponding contacts. **h** Final devices are diced from processed chips and are packaged in a Gel-pack to prevent electrostatic damage (ESD). In this example, $4 \times 16 = 64$ devices are diced out of 4 chips. One QuBus device is then glued on top of an interposer and electrically connected via wire-bonding. Eventually, the device and the interposer are mounted on a PCB for electric characterizations and shuttling experiments. A zoomed in view of a bonded device is shown on the right most.

be clear, the term 'batch' is used here referring to all chips being fabricated at the same time. In Fig. 3.1, all process steps are presented at the device level except for the entry point Fig. 3.1 **a** that shows a 4-inch wafer being diced into $10 \times 10\,\mathrm{mm}^2$ chips. In the rest of this section, each step of the process flow is reviewed and explained in details.

MARKERS

The first structure to be patterned are markers (see Fig. 3.1 **b**) including optical markers and E-beam markers for optical lithography and EBL, respectively. Optical markers employ the concept of Vernier scale in both x- and y-direction for micro-scale alignments. Incorporating with the mask aligner providing an overlay $< 0.5\,\mu$m for patterns with the minimum feature size (MFS) $> 1\,\mu$m, reliable alignments are attainable for patterning all microscopic structures including the markers, implantation area, mesa, ohmic contacts and bonding pads.

E-beam markers, those are squares with the dimension of $20 \times 20\,\mu\mathrm{m}^2$ for each, are etched into the Si/SiGe substrates sufficiently deep for $1\,\mu$m [104] to be identified by the E-beam scanner. Fig. 3.2 **a** sketches the distribution of markers and their working principle in an iteration of EBL. Four clusters of markers are distributed at corners of a cell centering the functional part of a device and each cluster contains four square markers. During EBL writing, the position of them is identified by a perpendicular electron beam that incidents from the top of the device. Thereafter the emission of secondary electrons and backscattered electrons in the field of view contribute to the imaging process of markers. Markers are then identified on corners one after another by means of edge detection program that detects all four edges of a marker and estimates the center of the identified marker. Patterns will be written in place according to the estimated positions of a group of markers and their relative distances to the pattern [106]. The SEM image of an identified marker is shown in Fig. 3.2 **c**. Note that the number of markers should not be less than the iterations of EBL, because the identification of a marker consumes the overlaid photoresist (PR). The following metal evaporation process will cover this area by metal. More specifically, an exposure of markers under electron beam changes the solubility of photoresist on top of marker areas and consequently leaves markers uncovered after developments, and thus it makes these markers useless for the next iteration of EBL (see the metal flakes on the edge of an exposed marker in Fig. 3.2 **c**). Since the gate layout of QuBus devices demands up to four layers of patterns, a set of four square markers is positioned on each corner in a cell i.e. a die.

To etch these markers, a proper etching method has to be decided. In general, either isotropic etching or anisotropic etching is chosen depending on the aspect ratio of the structure. Despite of an uncritical aspect ratio (1:20) in this case, etching the marker areas in all directions homogeneously by an isotropic etching process is not a gainful method as the undercut at the mark edges have influence on the marker identifications [106], and thus eventually affects the pattern alignments. Contrarily to the isotropic etching, the reactive-ion etching (RIE) provides controllable profile in favour of anisotropic etching in the desired direction with the benefit of pattern alignments. Here the sulfur hexafluride (SF_6) is the main etchant consuming the Si/SiGe heterostructure chemically along the growth direction so that etching the markers with a sharp sidewall and a depth of $1\,\mu$m becomes possible (see detailed discussions about RIE processes in Sec. 3.2).

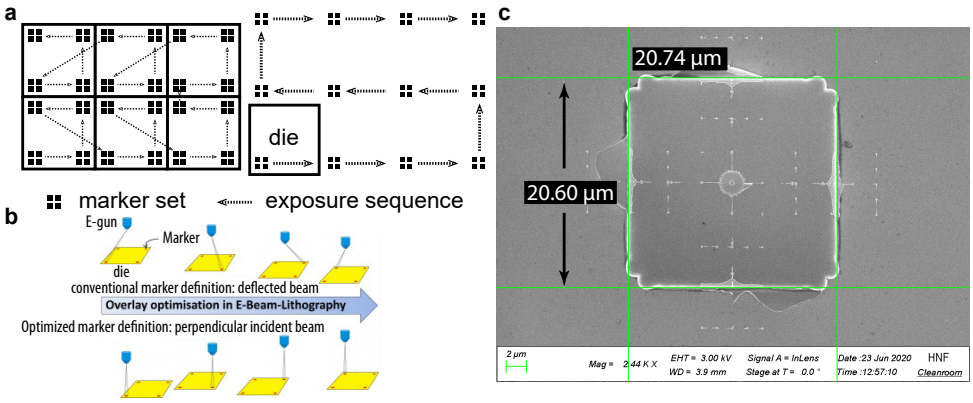

Figure 3.2: **Markers for E-beam alignments: a,b** are reworked and adapted from Ref. [106] where the EBL writing of QuBus devices relies on. **a** Schematics of the markers position in each device (i.e. die) and their exposure sequence in a EBL step. As an example, the left one shows a 2×3 die matrix with marker sets labelled accordingly. The exposure sequence within a die is indicated by dashed arrow. To the right of it, an abstracted writing sequence of dies on a chip is illustrated with only the first set of marker shown for each die. **b** The optimized marker recognition by adjusting the incidents angle of high energy electron beam. An optimized perpendicular incidents angle enables an overlay displacement of $\Delta x = (1.6 \pm 1.6)$ nm and $\Delta y = (0.1 \pm 1.4)$ nm with respect to conventional approach that leads to $\Delta x = (13 \pm 5)$ nm and $\Delta y = (12 \pm 6)$ nm overlay accuracy according to the Ref. [106]. **c** The SEM image of an exposed marker where a physical dimension of $20.60 \times 20.70\ \mu m^2$ are measured according to the image. The measurement error is limited by the pixel size 45.69 nm for this specific example.

For the QuBus device, the overlay between critical layers, those contain clavier gates, should not exceed the oxides thickness (T_{Ox}) that isolates clavier gates so that adjacent claver gates are not overlapping and the capacitive coupling between gate electrodes and the 2DEG is not affected by the gate electrodes underneath. For the QuBus device being characterized in this work $T_{Ox} = 10$ nm is targeted, and thus an accuracy of 10 nm is sufficient. Within the frame of this work, only is the pattern alignment along the x-direction most critical that is along the 1DEC of a QuBus. An overlay of (9.1 ± 0.8) nm has been eventually achieved after process stabilization and optimization which is detailed in the Sec. 3.2.1. In terms of T-junction devices, a similar alignment accuracy is required and achieved in both x and y-dictions to be detailed in the Ch. 6.

ION-IMPLANTATION AND ANNEALING

The ion-implantation is a fundamental process to selectively modify the conductivity of semiconductor substrates by accelerating dopants into them for instance the Si/SiGe heterostructure. In the case of QuBus devices, the electrons are the charge carriers under investigations, hence an n-type dopant (phosphorus: P) has been chosen for this process and a doping concentration of $5 \times 10^5\ cm^{-2}$ is aimed for. A complete ion-implantation process includes three main steps those are masking, doping, annealing and the PR removal. First of all, the implantation areas is masked by the PR that is patterned by OL, after which the doping regions are exposed under the high-energy ion beam. Secondly, phosphorus ions are accelerated to the sample with the energy of 20 keV. Meanwhile, the wafer is tilted by 7° with respect to the injecting ion-beam to avoid channeling effects of

implanted ions which may result in the distribution of dopants deeper than desired inside the Si/SiGe substrates [107]. Lastly, a post annealing step is required to activate the implanted dopants by restoring the crystalline within the implanted areas, because the ion-implantation leads to the doping area amorphous by damaging the crystalline which introduces a high density of defects and vacancies that eventually results in unwanted conductivities. To restore the crystalline by facilitating the diffusion of dopants as well as atoms in the Si/SiGe heterostructure, an annealing process at high temperature (700 °C) is operated within a short time 15 ~ 30 s [55, 108].

The annealing temperature and the duration time are critical parameters due to the limited thermal budget of strained Si QW in the Si/SiGe heterostructure. Key considerations are the followings. First, preserving the strained Si QW from relaxations at high temperatures demands precautions for designing thermal processes. Second, the diffusion of Ge atoms at the Si/SiGe interface, where the 2DEG is formed, should be suppressed to preserve the sharpness of Si/SiGe interface [109]. Moreover, the atomic fluctuations at the Si/SiGe interface affects the spread of valley splitting which is a crucial parameter for SiGe quantum devices [28]. These constraints limit processing temperatures, despite evidence that the growth of Si/SiGe virtual substrates in [750, 950] °C provides high qualities i.e. low densities of field and piled-up threading dislocations during the CVD growth [110, 111]. Consequently, the rapid thermal process (RTP) emerges as the preferred method, featuring a rapid heating rate of 5 K/s to the targeted temeprature, and then holding at 700 °C for minimum 15 seconds to let dopants diffuse within this short time. This combination delivers adequate electric characteristics for quantum devices based on Si/SiGe heterostructures [109]. Alternatively, the laser annealing process for Si/SiGe heterostructures developed by my best desk mate and colleague Malte Neul enables localized activation of implantatnion areas through laser-induced heating (details in the Ch. 5 of his dissertation Ref. [112]). However, its relatively longer processing time compared to RTP places it beyond the scope of this dissertation.

MESA

An etched mesa, that refers to a plateau containing only the undoped functional region of a QuBus and doping areas, defines the boundaries of 2DEG in a device. The mesa is nominally 100 nm high with the 2DEG being confined at the upper Si/SiGe interface that locates ~ 35 nm deep from the top of mesa. Such a feature sufficiently defines the active region of QuBus and eliminates the unwanted leakage paths from gate-electrodes to the substrate presumably during wire bonding by compressing gates to the substrates. The RIE is used to produce the profile of mesa and such a process can be operated on either a wafer level or a chip level as the RIE chamber is compatible with a 4-inch wafer. Though it is the largest feature size to be processed through the complete process flow of QuBus, however, etching an mesa introduces additional surface topography that may violate the device yields. For instance, its side-wall. A sharp cliff at the edge of mesa makes the gate fan-out difficult, given the fact that the thin film of metallic gates ranging from 12 nm to 150 nm has to homogeneously cover a cliff with a height of 100 nm, and thus metallic gate electrodes are subject to a high risk of discontinuity. An example of broken gates at the sharp edge of a mesa will be discussed in Sec. 3.1.2 and a further optimization of this process to smooth the slope of mesa has to be investigated and the details are discussed in Sec. 3.2.2.

OHMIC CONTACTS

Ohmic contacts for the 2DEG layer are demanded to characterize QuBus electrically at either ambient conditions or cryogenically. In other words, the metallic contacts should provide reliable connections to the 2DEG to measure for instance the transport of electrons. Moreover, the heating effects at low temperature should be eliminated as well due to the limited thermal budget in a dilution unit, thus good Ohmic contacts to the doped areas should experience low contact resistance and sheet resistance. However, the chips undergo multiple processing steps after annealing including one step of OL and RIE for mesa etching as well as another OL for patterning Ohmic contacts, thereby native oxides growth on the Si-cap layer underneath the desired Ohmic contacts lead to unexpected high resistance as well as unavoidable dielectric behaviors such as hysteresis. It is important to remove these native oxides entirely before metalizing the Ohmic contacts. A trivial solution is to dip the chips into hydrogen fluoride (HF) which is diluted to 1 % for the standardized recipe. By dipping the chips into HF for 1 min, oxides are sufficiently removed. But it is an upper limit of dipping time. The actual consequence is complex as a longer dipping time affects the adhesion of pattern PR. Pealing off PR flakes changes the well defined patterns of Ohmics for metallization. Therefore, 1 min is set to be a safe limit here. Additionally, cares should be taken that the transfer time from HF solution to the e-beam evaporator should be as soon as possible because the hydrogen absorption taking place immediately (in seconds) after drying the Si surface [113]. The Si surface terminated by hydrogen atoms varies the adhesion of metal on the exposed Si-cap layer. Given the fact that the e-beam evaporator for metallization and the wet bench for HF dip are physically separated without vacuum protection. Transferring processed sample at ambient condition is unavoidable. Loading the samples directly after the HF dip is the current solution. The Ohmic contacts are finally prepared and metalized by e-beam evaporation of Ti:Pt (5:150) nm sequentially, where Ti acts as the adhesion-promoting layer interfacing Si surface and the Pt gate metal.

EBL AND METAL LIFT-OFF

OL patterns features not finer than 1 μm, however, $<$ 100 nm gate pitch is required to define a QD in Si/SiGe heterostructure. Except for the deep ultra violate (DUV) and the extreme-ultra violate (EUV) lithography in industrial pilot lines, EBL is the most feasible option to write desired gate features for the QuBus with flexibilities of changing the design within a short turnaround time, although the writing time exponentially increases upon scaling up the devices. In this section, only the standardized EBL process is reviewed. The outlook of the fabrication techniques for modified QuBus, T-junction and scalable quantum devices such as the SpinBus architecture are beyond the scope of a section for process standardization.

Within the standardized processes, three layers of gate electrodes are written by the e-beam scanner with different sets of tuned parameters. The critical parameters of the electron beam for patterning include the beam energy, the beam dose and the pattern shrinkage factor. The e-beam scanner for this work has a beam energy of 100keV. An spatial resolution down to 10 nm is feasible and sufficient for patterning QuBus prototypes. The key parameters for tuning are the beam dose and the shrinkage factor defining the process window for each individual pattern. Therefore, the dose test of each layer of patterns are made within a parameter space consisting of the beam dose and the shrinkage

factor. After a thorough dose test, the process window of QuBus prototypes is found and established by using the following parameters for each layers of pattern.

The metal lift-off process is a straightforward and essential technique being widely used to manufacture microelectronic devices in an academic standard cleanroom. It mainly contains two steps to stack one layer of metallic gate-electrodes on the top of devices. Firstly, the desired gate layout is written by EBL on the device that is covered by PR. Due to the change of solubility of PR in the exposed area, a development process solves all PR on top of the gate areas so that a metal evaporation process covers the chips globally. Secondly, the liftoff is then accomplished by dipping the chips into solvent that solve all PR meanwhile peeling off metals from unwanted areas. As a result, only metals on the gate regions left.

There are two critical points to be aware of during processing. One is the flank of PR after developments, which determines the success in peeling of unwanted metal flakes. The other is the metal adhesion, that plays a part in the existence of gate-electrodes, because the material properties of the surface where gate adhere to varies. It is very often to have an amorphous Al_2O_3 surface because the metallization of gate-electrodes always interleaves a step of oxides deposition for the gate isolation. Sometimes metallic gates need to contact to a Si surface as well in order to form a Schottky contact. Therefore, metals should be carefully chosen. In this process flow, 5 nm Ti is always evaporated as the adhesion layer for the gate contact metal Pt. As a noble metal with high conductivity, Pt not only prevents the Ti from oxidation, but also offers lower contact resistance as a result. In the case of a Schottky contact to Si, Pd is chosen thanks to its high electron affinity and good adhesion to Si so that it could evaporated directly to a Si surface by one step of metal evaporation.

When stacking gates on a 2D surface, the height variations i.e. the topography of deposition surface has impacts on the gate manufacturing yields as well. Contrarily to the planner process in an industrial fabrication where each surface is flatten before depositing new material [14, 34, 100], the lift-off process does not involve any polishing process or etching steps to shape the surface. That leads to a significant fluctuations on the surface of devices after stacking multiple layers of structures. To overcome this surface topography, the thickness of gate-electrodes increases gradually to assure the continuity and the integrity of materials in the presence of local topography changes. As a result, from bottom to top a three-layer QuBus device needs the metal thickness of (5 nm Ti and 15, 22, 27 nm Pt). Alternatively, a micro-magnet can be patterned on top of the gated chip by an additional cycle.

ATOMIC LAYER DEPOSITION (ALD)

Oxides play a critical role in manufacturing semiconductor devices by serving as gate insulators. To attain a high quality oxides with precisely controlled thickness, the atomic layer deposition (ALD) technique is commonly used to deposit a thin film of oxides with precise and atomic-level control over the film thickness. First of all, the ALD technique allows a conformal coating of features with high aspect ratio due to its self-limiting process, which particularly benefits the gate isolation for the lift-off process that is subject to local topography for higher layers of oxides. Second, from the materials perspectives, Si/SiGe QuBus devices are subject to low thermal budget during processing

to prevent the degradation of the Si/SiGe interface sharing the same concerns as RTP processes. The atomic layer deposited thermal Al_2O_3 is such an option that enables the oxides deposition at rather lower temperature comparing to others growth techniques. In the case of depositing Al_2O_3 thin films, for example, the chemical vapor deposition (CVD) method often operates at temperatures between 400 ~ 700°C those do harm to the Si/SiGe heterostructures. Though a plasma enhanced CVD process may reduce to temperatures even lower than ALD, it compromises the oxides quality, a much lower temperature (300 °C) for ALD Al_2O_3 solves the problem in-place. Moreover, high-k materials are demanded for enhancing the capacitive-coupling between gate electrodes and quantum well layer, thus the gate lever arms. However, they suffer from high density of defects such as HfO_2 [114, 115]. The Al_2O_3, fortunately has a relatively higher dielectric constant (~ 7.6) [116] than SiO_2 (3.6 ± 0.2) [94]. As a result, the ALD thermal process is chosen to deposit a conformal, atomic-level controlled thin films of Al_2O_3 for gate isolation at a sufficiently low temperature (300 °C) for QuBus devices.

In general, the ALD process uses alternating pulses of metal precursor and reactant for depositing oxides on top of the substrates. For the thermal Al_2O_3 in QuBus, the ALD process operates on the chip level. We use the trimethylaluminum (TMA) as the metal precursor to cover the surface of chips. Thereafter, the reactant, highly purified water, is purged subsequently to form a monolayer of Al_2O_3. By repeating such a process for $\approx$ 100 cycles, a 10 nm thick Al_2O_3 is deposited on top of the QuBus device conformably with the chamber temperature at 300°C. Due to a few non-uniform monolayers at the beginning of cycles, 120 cycles are experimentally used to produce the targeted thickness. The growth mechanism is sketched in Fig. 3.6 for demonstration, but not detailed for now as the chemically induced impurities are of more importance and to be discussed thoroughly in Sec. 3.1.2.

ALD thermal Al_2O_3 should provide gate isolation electrically for QuBus devices. The gate leakage is suppressed to pA level with respect to the signal current at nA, providing the high performance of gate insulation. A breakdown voltage of $\approx$ 5 V has been measured for 10 nm thermal ALD Al_2O_3, however, it is a number derived from the MOS cap measurement of micron thick Al_2O_3 where the metallic contacts are also one magnitudes larger that those in a QuBus device. Therefore, cares have to be taken during tuning up a device to maintain the gate voltage difference in small vicinity especially close to the top-gate for accumulation of SETs. Moreover, the frequency responses of MOS caps with ALD Al_2O_3 are recorded where a positive shift of the capacitance voltage characteristics as increments of frequency suggesting the existence of interface traps with negative polarity those are driven by the oscillating probe signal. A defect concentration in the order of $10^{12}\,cm^{-2}$ is evaluated from such an experiment. However, this experiment is conducted at room-temperature. The characteristics at cryogenic temperatures where QuBus devices operate may vary considering the freezing-out defects i.e. defects become inactive as in room temperature. Nevertheless, all aforementioned precautions make the ALD Al_2O_3 critical and worthwhile for further investigations (see Sec. 3.1.2 for details).

BONDING PADS

Bonding pads interfaces the FEOL of QuBus devices and corresponding Back-end of line (BEOL) for device packaging and handling. Since the fan-out gates are all patterned by

EBL and metalized in the same cycle, ultra thin metallic layer with same thickness as fine structures (20, 27, 34 nm) are expected. The wedge of bonding tool can easily damage the thin film and leads to uncertain metal-metal contacts as ultrasound is applied to assistant the inter-diffusion of metals between wires and pads. Therefore, it is necessary to reinforce the bonding pads during processing to enhance its mechanical stability and the electric integrity after wire-bonding. For QuBus devices, the bonding pads are defined and exposed by one step of OL using the mask shown in Fig. 3.1 **g**. Chips are then dipped into 1 % HF for 30 s with the same concerns as for the Ohmic contacts. An etch rate of 1 nm/s is measured and thus 30 s is sufficiently long to expose the contacts of gates on the first layer meanwhile eliminates the risk of peeling off PR. It is more constrained than the dipping time for Ohmic contacts because the surface topography at this step is more complex such that the diffusion of HF molecules becomes more aggressive. Limiting the process time to the least demanded time is feasible to preserve the unreliable adhesion between PR and chip surface.

DEVICE HANDLING

At the end of FEOL, the devices are exported from cleanroom to the lab for electrical characterizations. The device handling during transfer needs extra cautions to avoid non-reversible damages such as the electrostatic damage (ESD). Packaging devices in Gel-boxes prevents ESD by equally grounded all diced devices via the conductive gel inside the box such that no static charges could accumulate on devices. Thereafter, diced device to be electrically characterized is glued on an interposer which interfaces the wirings between micron-scaled bonding pads on the device and the macro-scale pads on a printed circuit board (PCB) as shown in Fig. 3.1 **h**. During the device handling including gluing and wire bonding, all gates and the experimentalist are electrically connected by a connector maintaining all gate electrodes at the same electric potential until the device is mounted in the dilution unit which is connected to the lab ground.

3.1.2. CRITICAL PROCESSES FOR QUBUS MANUFACTURING

Each step in the standardized process flow contributes to the yield of QuBus devices, and, fortunately, not all processing steps are equally critical so that only the most impactful steps get the focus. The often observed degradations of QuBus devices are concluded by measurements with unexpected electrostatic characteristics such as not accumulated 2DEG, high leakage currents, incomplete pinch-off, etc. All these failures represent the imperfect electric integrities of either metallic gate electrodes or dielectrics including both Si/SiGe heterostructure and oxides. While the electronics and wiring in an experiment should also be considered, thoroughly inspecting devices during manufacturing remains a crucial upstream step to ensure fully functional QuBus devices. However, electric characteristics, those sufficiently reveal the functionality of QuBus, are not always accessible at each step during fabrication. Integrating regular optical inspections in the process flow becomes the most powerful measure to efficiently sense the failures during each processing step especially when it undergoes the fine tuning of parameters. Depending on the demanded spatial resolution, either the optical microscopy or the scanning electron microscopy (SEM) inspection is commonly used after development (ADI) and after etching (AEI) those sufficiently monitor the inappropriate features

being patterned and transferred, respectively.

As introduced in the standardized process flow, at least three layers of gate electrodes stack on top of each other on an undoped Si/SiGe heterostructure. All gate electrodes of QuBus devices are patterned by EBL and then metalized via electron-beam evaporation, followed by a metal lift-off process interleaving sequentially the gate isolation by atomic-layer deposited Al_2O_3. Numbers of fabrication failures, that may lead to inappropriate electric characteristics of QuBus devices, are mainly induced by several critical steps such as (i) the overlay i.e. the inter-layer misalignment of the E-beam written patterns, (ii) the anisotropic topography i.e. the smoothness of device, and (iii) the charge impurities. In this section, these fundamental fabrication imperfections are firstly reviewed. They are eventually solved by either optimizing relevant etching processes (see optimized marker etching in Sec. 3.2.1 and the anisotropic topography control for mesa etching 3.2.2) or by exploiting new materials to reduce the charge impurities by eliminating the amount of oxides (see Sec. 3.3.1).

INTER-LAYER MISSALIGNMENT

The misalignment of E-beam written patterns is one of the fabrication failures. Misplaced patterns especially the metallic gate electrodes will eventually lead to inappropriate distribution of electric field in the device. For example, if an inter-layer misalignment in the x-direction happens to the top-gate of SET. One of the two SETs in this device will be hardly pinched off by lower laying barrier gates, despite the other SET can be pinched off on purpose. Additionally, the electric fields of the claviers gates on the top layer will be screened by the metallic gates at lower layer. In particular, it is more impactful for QuBus device who has periodic gate patterns. An inter-layer misalignment does not only affect a single clavier gate, but also a series of clavier gates will be displaced consequently, thus leading to unexpected device functionalities such as forming periodical bumps in the electrostatic potential instead of an expected smooth conveyor-potential belt.

Though such a failure mode can be easily detected and inspected by an SEM inspection after metallization of each layer of electrodes, it is not the golden solution for two reasons. First, it does not prohibit the misalignment of patterns in advance, but passively observes such a non-reversible error taking place. Upon the metallization of a layer of gates, the removal of a thin-film nobel metal is practically nontrivial. While ADI before metallization warns the wrongly patterned features, exposing the E-beam written PR under SEM sacrifices the profile of the shaped PR, and thus degrading the final profile of the gate electrodes which results in an unwanted failure mode as well. Second, exposing the device under SEM presumably inducing higher electric noise due to the injection of high energy electrons into the inspected device. It then becomes an invasive measure of misalignment in a device by sacrificing its electric performance. And it degrades the devices yield as well by destructively inspecting well patterned devices. As a result, the key point to avoid the pattern misalignment is rather to optimize the quality of the markers in advance.

Fig. 3.3 explains the principle of such an issue. In Fig. 3.3 **a**, a non-optimized etched marker is used for QuBus patterning. Due to a non-optimized RIE process, the sidewalls in this cross-section clearly indicates the inhomogeneity of such a marker as its left sidewall is visibly straight comparing to the one on the right-hand side. As being discussed

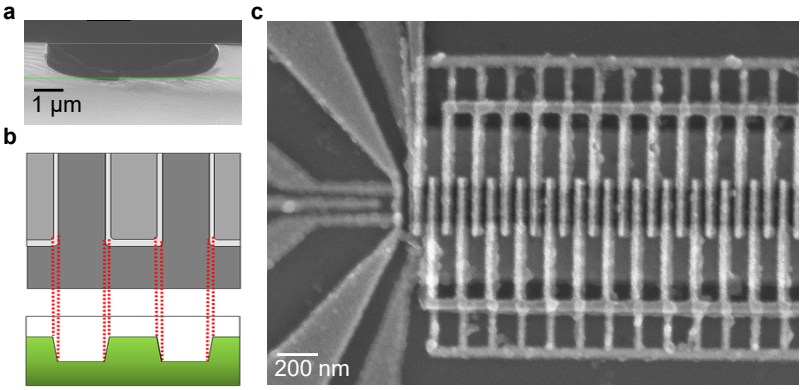

Figure 3.3: **Inter-layer misalignment due to undercutting markers: a** AEI of marker cross-section by SEM operated with a tilt angle of 90° with respect to the incident electron beam. The green line indicates the measured depth of etched marker (1.184 μm$\pm$14.46 nm) whereas the targeted depth is 1 μm. **b** A schematic of undercutting structure's appearance in an SEM arial image. The side wall disturbs the algorithm of EBL tool to identify the center of marker leading to misalignment of patterns to be written. **c** The misalignment of patterns on a QuBus device. The clavier gates on the second and the third layer are almost overlap due to significant misalignment (~ 35 nm).

previously in Sec. 3.1.1, the EBL tool identifies the markers by capturing an SEM arial image with a perpendicularly incident angle. A schematic is shown in 3.3 **b** which illustrates how the undercutting sidewall being transferred into the SEM arial image. The inhomogeneity of sidewalls in this case eventually leads to an error of the estimated center position of the recognized marker, which is later used as reference coordinates for pattern writing. An deviation of tens nanometers already fails one layer of pattern and a QuBus device as shown in Fig. 3.3 **c**. The clavier gates on the second layer are patterned 35 nm to the left of its designated position and in turn they are located exactly beneath the clavier gates on the third layer. Such an unexpected overlap due to misalignment makes the specific device useless since any voltages applied to the third layer will be screened by the metal gates directly underneath. Though it is an extreme case study, solving such a problem is demanded for the device yield and it is possible by carefully shaping the profile i.e. sidewalls of etched markers with an optimized etching process (see detailed discussions in Sec. 3.2.1).

ANISOTROPIC TOPOGRAPHY

Anisotropic topography is an inherent issue of metal lift-off processes since no polishing steps are applied to the processed chips to maintain a planner surface throughout the FEOL. Purely stacking an additional layer of structures on top of substrates leads to severe topography variation as the number of layers increasing. Such topography variation impacts the gate pattern integrity and potentially results in broken gate electrodes that is another crucial failure mode of fabrication. In particular, for the gate electrodes of QuBus, the physical dimension of such topography variation matters as the feature size of a gate electrode in a QuBus device spans from nano-scale to micron-scale and the weak points those may lead to a broken gate appear at both nano-scale and micro-

scale due to different sources of tomography variations and thus should be addressed and solved individually.

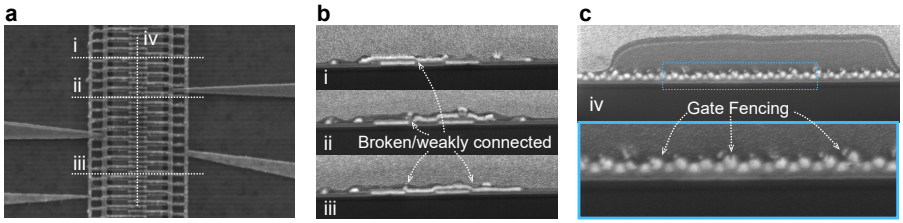

Figure 3.4: **FIB inspections of anisotropic topography on a well-aligned QuBus device: a** An SEM image of the 10μm QuBus device (W_G=35 nm) under FIB inspection. Dashed lines indicate the relative positions where FIB inspections are applied. **b** The cross-sections of clavier gates when they climb over the channel of QuBus. Their corresponding positions and directions are highlighted in **a**. Weakly connected points suffering from magnificent tomography variations, those have high risks leading to broken gates, are indicated by the dashed arrows. From top to bottom, (i) represents a cross-section of clavier gate on the third layer with a metal thickness of 34 nm. (ii, iii) correspond to gates on the second layer with a metal thickness of 27 nm. **c** The cross-section of clavier gates along the QuBus channel as sketched by dashed line (iv) in **a**. In the lower panel, the center part is zoomed in to visualize the gate fencing effects that the gates on the third layer encountered with.

The weakly connected gates at the QuBus channel region is illustrated in Fig. 3.4 corresponding to one type of nano-scale failure. As shown in the Fig. 3.4 **b**, the clavier gates with a thickness of 34 nm and 27 nm have difficulties of covering the channel regions. In the line-cut (i), the arrow indicates a weak point where the inspected clavier gate tends to break. Underneath its left part, a screening gate on the first layer with a thickness of 20 nm is covered by 20 nm Al_2O_3, whereas its right part needs to fill up the QuBus channel that is only covered by 20 nm Al_2O_3 and is appearing as a trend between two screening gates. As a result, the clavier gate on the third layer encounters with a levitation difference of 20 nm corresponding to the height of screening gates. Although 34 nm thickness should sufficiently overcome such topography change, the example shown here indicates that the connection remains fragile. In addition, such a weak point appears only on one side of the trench which reflects the fact that the gate connectivity is sensitive to the incident angle of evaporated metal as well. Similar effects are visible to the gates on the second layer as well. Mover problematic issue can be seen in (ii) where the clavier gates fail to climb over the screening gate on the left-hand side.

Another nano-scale failure mode is the gate-fencing, which refers to the fact that the edges of metallic gate roll upwards forming a fence around the designated region. Such an effect becomes severe when the gate is formed on top of an uneven surface i.e. the topography variations that is discussed here. As depicted in Fig. 3.4 **c**, the cross-section of the clavier gates on the third layer shows obvious fencing effects that either inappropriate metal flakes attaching to the top of clavier gates or the metallic gates squeezing into the gap between gates on the lower layer providing a "heart" shaped cross-section as can be seen in the middle of the zoomed-in view. The former could lead to the difficulties of lifting off unwanted metal as the fencing metal flakes covering the PR flanks which should be exposed to the solvent, and, such unwanted metal leftovers will short to other gates and eventually affect the electric functionalities of the device. The latter, on the

other hand, does not lead to cross-linking to other gates, but rather affect the capacitive coupling of this gate to the 2DEG by its unexpected shape variation due to fencing.

Fortunately, the nano-scale topography variations has a non-critical aspect ratio. It means that the gate stack with increasing thickness solves the gate overlay directly and guaranties the electric connectivity of each gate. Notably that, one should compromise the upper limit according to the PR thickness of CSAR that is ≈ 100 nm. It is intuitive since the thicker metal filling up the trench, the more PR flanks are covered, and thus higher risk of unsuccess lift-off. Consequently, one third of the PR thickness has been empirically chosen as the upper limit of gate electrodes for metal lift-off according to the previously developed recipes by Inga Seidler. In this work, I attempt to reduce unnecessary metal thickness meanwhile maintain the maximum thickness around 30 nm. As a result, the optimized thickness per layer is given as follows: from layer one to three (12, 22, 29)nm Pt are evaporated on top of 3 nm Ti adhesion layer ended up with thickness of (15, 25, 31) nm from bottom to top of a three-layer QuBus device (see details in Appendix).

The micro-scale topography, on the other hand, is more critical, for instance the edge of a mesa. A thin-film of gates with 15 ~ 30 nm thickness should climb over a cliff with a height of 100 nm that is challenging for e-beam evaporated metal. Fig. 3.5 captures a non-optimized mesa produced by standardized process. When a thin-film metal gate covers this area, broken structures are commonly observed at the mesa edge which leads to a not electrically connected metallic gate. Making the mesa smooth rather than a steep cliff (≈ 90°) is a natural solution to that. An extreme case of smoothed mesa would be a plane that is equivalent to a no-mesa design out of the scope of this dissertation. Therefore, the midian value 135° is taken for the initial attempt to smooth the mesa. To reshape the mesa profile, one should look deep into the etching process sharing the same idea as for the marker profile control. Corresponding optimized process can be found in Sec. 3.2.2.

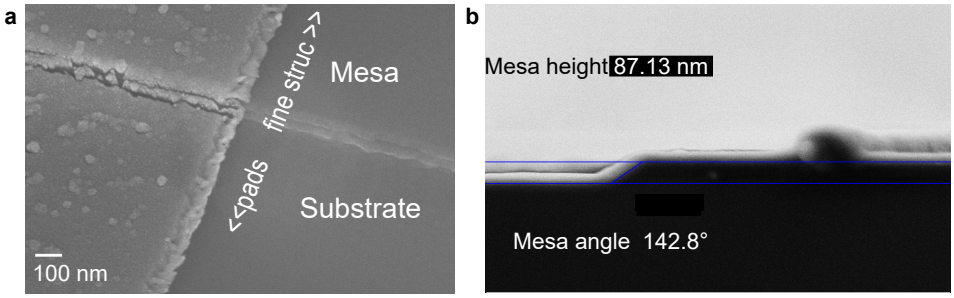

Figure 3.5: **Broken gates fan-out at mesa edge vs the full metal coverage of mesa: a** SEM inspections of broken fan-out gates in the micro-scale (i.e. at the edge of mesa). Two different devices experience the same issue and one of it is shown here. Relative positions of mesa and substrates are labelled accordingly. In addition, overlaid labels indicates the fan-out direction of each metallic gates (from fine structures written by EBL to the micro-scale bonding pads). **b** an example of the full coverage of mesa edge using the optimized etching recipe to be discussed in Sec. 3.2.2. Here an cross-section inspection is applied to a cleaved device. The mesa height of 87.13 nm and an angle of 142.8 ° are measured and labeled accordingly. The blue lines indicating the top surface of mesa. It is covered by 10 nm Al_2O_3 and 20 nm metallic gates corresponding to the brighter part above the blue lines.

CHARGED IMPURITIES

Charged impurities, the atomistic sources of electric noise, widely exist in any semiconductor devices. Despite of all aforementioned critical processes are optimized providing a high yield of QuBus devices, atomistic electric noise are not addressable during fabrications until the devices are electrically characterized. Fortunately, the resources leading to such impurities could be eliminated as much as possible as an upstream treatment.

The charged impurities at the semiconductor-oxides interface has been attributed as the main source by measuring the capacitive voltage characteristics of MOS caps. [94] It suggests that the charged impurities are mostly negatively charged and can be driven by the applied oscillating voltages, given the fact that the C-V characteristics drifts towards the positive voltages as increasing driving frequencies. In the QuBus devices, the only semiconductor-oxides interface located between the first layer oxides and the Si-cap. Therefore, the first layer of ALD Al_2O_3 plays the crucial role in terms of charged impurities.

Fig. 3.6 **a** sketches the working principle of thermal ALD Al_2O_3 which helps us to understand the reason of forming charged defects at the interface. As introduced briefly in Sec. 3.1.1, the TMA acts as the precursor which is pulsed into the reaction chamber and being absorbed by the substrates. The absorption is accomplished by the ligand exchange of TMA with the hydroxyl groups on yielding methane (CH_4) as by-product. Such a chemical interaction is considered to be self-limiting as a cover of monolayer Al-O-Al$(CH_3)_2$ on top of the substrate stops absorptions of excess TMA. Thereafter, a nitrogen purge evacuate CH_4 as well as excess TMA. At the third step, the highly purified deionized water vapors are pulsed into the chamber as reactant producing Al-OH on the surface of substrates and CH_4 as by-products. Similarly, excess water vapors and CH_4 are evacuated by purging nitrogen gas. As a result, the surface of substrates ends up with a monolayer of hydroxyl groups again hence reproducing the initial condition of a cycle.

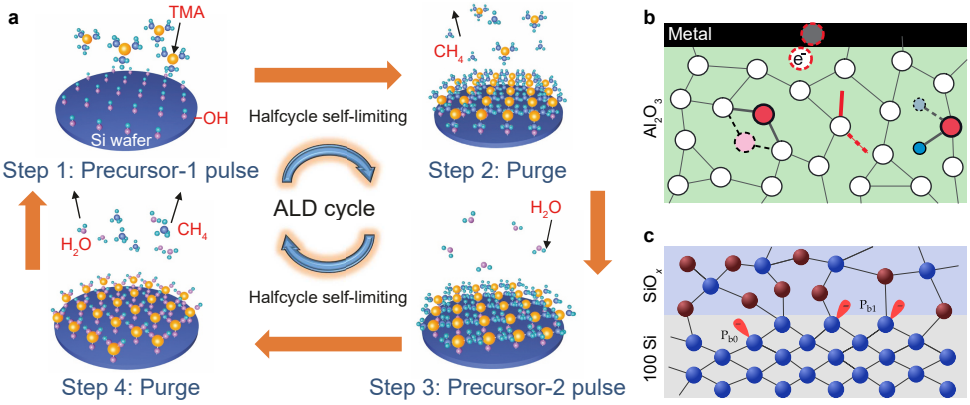

Figure 3.6: **Charged impurities in oxides:** **a** Schematics of the working principle of thermal ALD Al_2O_3 adapted from Ref. [117] **b** The schematic adapted from Ref. [118] depicts impurities within the amorphous Al_2O_3 dielectric and its interface to metallic gate-electrodes. Tunneling atoms, dangling bonds and trapped charges are considered. **c** The reworked schematic of the amorphous dangling bond at Si-SiO_x interface according to Ref. [94]. P_{b0} and P_{b1} represent a single dangling bond of a Si atom backbonded to three Si atoms ($Si^\circ \equiv Si_3$) or two Si atoms and an oxide atom ($Si^\circ \equiv Si_2O$), respectively.

Different types of charged defects at atomistic level are proposed and studied by either simulations [118] or experimentally [94] focusing on the defects in an amorphous layer of oxides. Oxygen or aluminum interstitial and vacancies are common charged defects within Al_2O_3. This could occur to missing bonds of both Al and O atoms in any cycle of ALD. They can be understood as trapped charges and tunneling atoms those contribute to the defect states in Al_2O_3 as depicted in Fig. 3.6 **b**. In principle, all these defects can be charged as long as free charge carriers such as electrons or holes are provided. Metallic gates insulated by such oxides therefore provides additional source of electrons being trapped by defect states. Moreover, the formation of SiO_x is unavoidable when depositing Al_2O_3 thermally on top of silicon. [119] Therefore, not only the defects in the Al_2O_3, but dangling bonds of a silicon atoms also plays a role at the interface between Si and SiO_x forming two types of defects depending on the other side of the dangling bond (see Fig. 3.6 **c**). To this end, defects are nominally unavoidable at the atomistic level, however, one could eliminate its concentration by conservatively using the least amount of oxides.

According to the essential concept of screening gates that aims at defining a channel for shuttling electrons, rarely are the positive voltages applied during device characterizations. As the first attempt to reduce the Al_2O_3 thickness underneath the screening gates, an extreme case is studied by forming a Schottky barrier between screening gate and Si-cap (see discussions in Sec. 3.3.1). Admittedly, this option in turn limited the upper bound of applied voltages for screening gates as too positive screening voltages may break the Schottky barriers. However, the experiments in this work did not hit such limitations. Whether this is a hard limit to the laterally shifting channel within the QuBus remains debatable and requires future works on carefully characterize the barrier height.

3.2. PROCESS OPTIMIZATION

CRITICAL processes are further optimized to achieve well-performed QuBus devices with high yields during my first two-year PhD career incorporate significant inputs and assistance from Dr. Jhih-Sian Tu especially on optimizing the etching recipes. In this section, optimizations of etching processes in the standardized process flow are discussed in order to solve the pattern misalignments and the anisotropic topography issues. Both of them depend on the profile engineering by means of RIE for specific patterns that are markers and the mesa edges, respectively.

RIE operates by introducing reactive gases into a chamber where they are ionized by a radio frequency (RF) electric field, creating a plasma. This plasma generates chemically active species and ions, which is then accelerated toward the material surface by additionally applied DC bias. Such a process combines both physical and chemical etching effects. The accelerated ions with given kinetic energy bombard the surface of substrate physically, whereas reactive radicals chemically interact with the material on the surface, forming volatile by-products. These two mechanisms consume the substrate surface at atomistic level with controllable rates enabling anisotropic etching profiles for micro- and nano-fabrication.

However the physical and chemical etching are competitive in an RIE process leading to either isotropic favorable or anisotropic dominated etching. For the optimizations of an RIE process, the balance between physical and chemical etching is thus the key fac-

tor that should be controlled by fine tuning parameters such as the chamber pressure, chamber temperature, applied DC bias and etchant gas flow rates. For instance, a low-pressure in the chamber represents a low concentration of ionized reactants which on the other hand favors the directional physical etching. Because ion collisions with other gas particles are minimized at such a low pressure and the acceleration due to the applied DC bias dominants. Typically, it contributes to the formation of a more anisotropic profile as the ions are accelerated perpendicular to the substrate surface. Conversely, increasing the pressure enhances the density of ionized etchant, which can boost the chemical etching process at the substrate surface and eventually lead to a more isotropic profile. Similarly, the reaction temperature affects and mostly enhances the reaction rate on the substrate surface where chemical reactions normally take place during RIE. Moreover, varying the flow rate of etchants varies the etch rate and profile as well, as an increased flow of etchant gases enhances chemical etching, while reduced flow rates results in a more physically dominant etching. All aforementioned facts compatibly contribute to the ultimate profile of etched structures.

When etching SiGe layers, in particular for the Si/SiGe QuBus devices, the primary etchant is the SF_6 releasing fluorine radicals that react with Si and Ge atoms, forming volatile fluorides. Such a pure chemical reaction is not self-limiting, and thus O_2 gas is admitted into the chamber to control the etch rate by forming a thin oxide layer on the substrate surface to avoid over etching by SF_6. However, additional O_2 gases molecules enhances the particles collisions thus limiting the physical etching process at the same time. Therefore, carefully adjusted concentration of O_2 in a etchant mixture is demanded incorporating other lever arms such as the temperature and DC bias to achieve the designated etched profiles. For both marker etching and the mesa structures, highly anisotropic profile are required. In the case of marker etching, a sharp sidewall with non-critical aspect ratio is demanded, while smooth edges are expected for the mesa structures. As a result, the anisotropic etching contribution needs to be enhanced by admitting O_2 in general. And the fine tuning of the profile for different structures should be considered differently. In the following subsections, the etching processes of markers and mesa structures will be discussed separately.

3.2.1. OPTIMIZATION OF MARKER ETCHING PROCESS

As previously introduced in Sec. 3.1.1 and Sec. 3.1.2, a well-aligned QuBus device demands high quality of etched markers ensuring the contrast of arial image of the detected marker for the aligning patterns during exposure. A depth of 1 μm is directly adapted from previously developed recipes from Inga Seidler's master thesis [104] which shows sufficient a good contrast of an arial image under e-beam alignments, however the chemical etching component of an RIE step in the standardized process flow yields significant misalignments from time to time due to its uncontrolled undercutting sidewalls. Such severe misalignments eventually degrades the device yield as a result indicating vulnerable condition to be stabilized. In this section the process optimization will focus on shaping a straight sidewall meanwhile remaining the depth of etching markers within the scale of 1 μm.

To produce an 1 μm deep marker with an opening area of $20 \times 20\,\mu m^2$, a mixture of SF_6 and O_2 is used such that the SF_6 consumes the Si/SiGe substrate meanwhile being

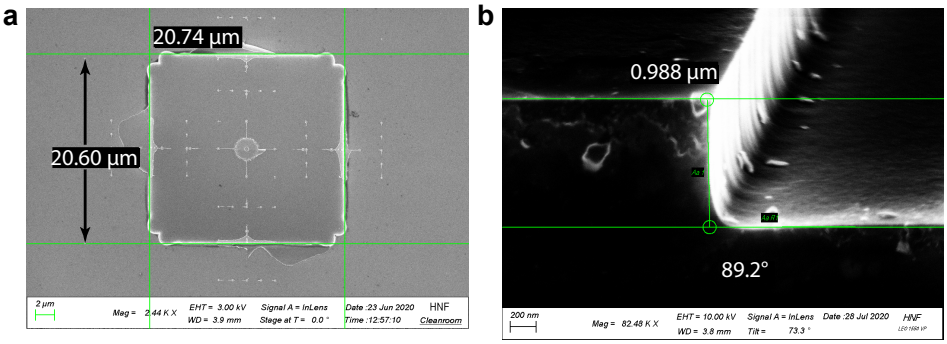

Figure 3.7: **AEI of optimized marker side wall. a** an SEM ariel image of the marker etched by the cryogenic process. The designated dimension is identical to the standardized process that is $20 \times 20 \mu m^2$. **b** A side-wall inspection of a cleaved sample. An etched trench with a depth of 1 μm is measured.

passivated by the O_2. Due to a relatively low aspect ratio that is 20 : 1 for such an isotropic etching, the chemical etching needs to be significantly suppressed. It is achieved by maintaining a low temperature at the substrate surface to limit the increasing temperature due to this chemical reaction. We term markers etched by this approach "the cryo-etched markers".

Fig. 3.7 monitors the ariel image of a cryo-etched marker and the side wall of an identical one being cleaved for better visibility. In this example, a marker with dimensions of $20.64 \times 20.74\ \mu m^2$ is identified, and a clean and straight sidewall with 90.2 ° is measured. The corresponding process operates at −120 ° with the SF_6 and O_2 flow rate of 50 sccm and 10 sccm, respectively. an RF power of 100 W is applied. To better maintain the low temperature condition, the whole etching recipe is splitted into three sub-processes such that after each 1 min etching, the chip is cooled down by waiting for 3 min. As a results, the marker regions are slowly consumed under preserved temperature yielding a smooth and straight sidewall.

3.2.2. OPTIMIZATION OF MESA ETCHING PROCESS

To shape smooth mesa edges, the anisotropic etching component is enhanced by admitting O_2 into the RIE reaction chamber suppressing the chemical consumption of the Si/SiGe substrate. However, the sidewalls of the etched structure differs from the cryo-etched markers. In stead of a straight sidewall, extremely flat and smooth edges are expected. In contrast to purely maintaining a low temperature to suppress the chemical etching component as for the cryo-etched markers, the dynamics of patterns transfer by RIE need to be optimized. Here, a different technique termed "the photoresist reflow and erosion" is used to control the sidewalls of mesa edges assisted by photo-lithography. With a reflow and erosion technique, the sidewall of etching mask, i.e. the photoresist, is firstly smoothed before RIE step by post development heating that reflows the PR resulting in a positive flank on the mesa edges. Consecutively, the RIE process consumes the Si/SiGe substrates meanwhile eroding the PR leading to the retraction of etching masks dynamically. Incorporating the structured PR sidewalls and the enhanced phys-

ical etching component during RIE, smoothed mesa edges, particularly the sidewalls of photoresist, is transferred to the Si/SiGe substrate directly without sophisticatedly tuning of etching parameters, but only the O_2 composition in RIE etchant remains.

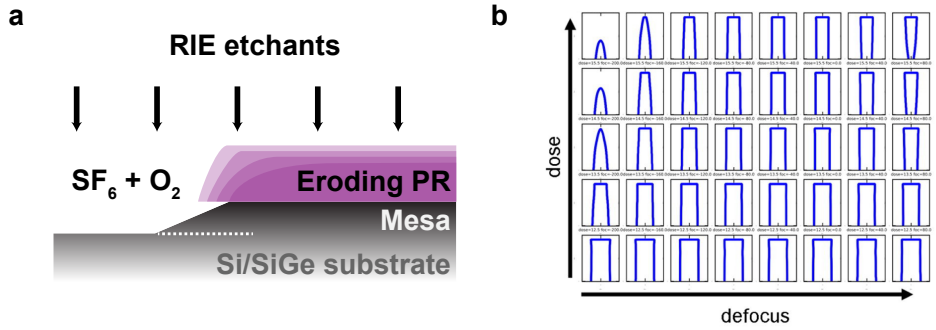

Figure 3.8: **The working principle of "photoresist reflow and erosion". a** A schematic of the photoresist erosion. **b** The simulated profile of PR after photo-lithography presented in the focus-exposure matrices (FEM). This figure is adapted from Ref. [120]

PR with positive flanks is a prerequisite for the PR reflow and erosion technique. As shown in the Fig. 3.8 **a**, the RIE etchants consume PR and the processed substrates simultaneously. With a positive flank at the edge of etching mask, the exposed area of substrate is gradually enlarged leading to a smoothed slope for the etched profile. To produce PR with designated positive flank, we make use of the working window of photo-lithography defined by the dose and defocus parameters for patterning. The dose and defocus are two orthogonal degrees of freedom to benchmark the performance of PR after one step of lithography (i.e. after development). In Fig. 3.8 **b**, the profile of a positive tone PR after development is simulated in its process window represented by dimensions of dose and defocus. With an increment of dose, the top of PR is over exposed due to exceeding photon incidents, and thus a positive flank is produced. On the other hand, the variation in defocus affects the sharpness of the arial image to be patterned. In this example, the center of the defocus produce almost straight flank throughout doses, whereas a negative defocus effectively projecting the arial image to the bottom of PR and results in the blurry at the top of PR. It effectively overexpose the top of PR such that favors a positive flanks. Similarly, the positive defocus underexpose the top of PR for large doses, and thus prone to collapsing PR where the footprint of PR becomes smaller than its top (see the top-right of FEM). Leveraging the tunable dimensions, we pattern the etching mask for mesa with 280 mJ/cm^2 and defocus -10 producing a positive flank on the edge of mesa. To avoid interference along the PR profile that eventually transfer to the substrates as scallop structures, we reflow the PR by heating the patterned sample up to 90 °C for exploring and testing a proper recipe for patterning an optimized smoothed mesa structure.

The process optimization of the RIE step starts from the parameters in the standardized process (see the initial configurations in Tab. 3.1). With a prepared positive and smooth PR profile, the key factor being optimized for RIE to achieve smooth mesa edges is the composition of SF_6 and O_2 in the etchant mixture. As the absolute flow rate of SF_6

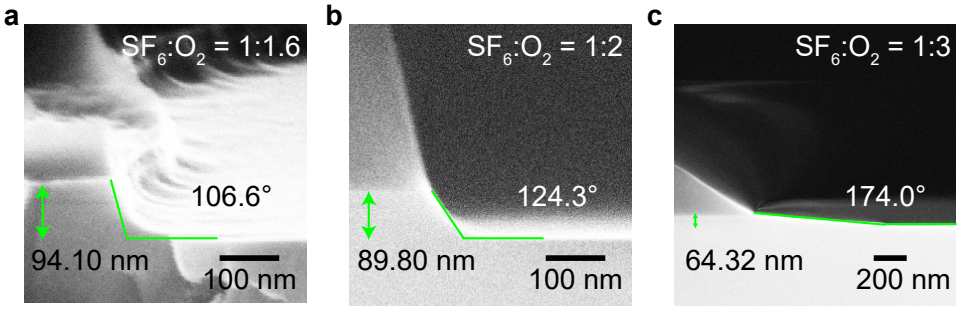

Figure 3.9: **AEI of mesa edges** The cross-section of mesa edge measured after etching with **a** etchant composition (SF_6:O_2 = 1 : 1.6), **b** etchant composition (SF_6:O_2 = 1 : 2), and **c** etchant composition (SF_6:O_2 = 1 : 3).

remains unchanged to maintain a relatively constant etching rate, we express the tuning of mixture composition by the ration between two components where the initial point becomes $SF_6 : O_2 = 1 : 1.6$, and the increasing composition of O_2 is studied for the ratio of 1 : 2 and 1 : 3. AEI of all these configurations are operated to have an overview of the profile variation as the increment of O_2 component (see AEI in Fig. 3.9).

Table 3.1: **The initial and optimized configurations of mesa etching process.** RIE parameters for mesa etching in standardized processes (i.e. the initial configuration of optimization) and the optimized etching parameters for smoothed mesa etching process.

Parameter	Initial	Optimized
Time	1'30"	3'30"
SF_6	25 (sccm)	25 (sccm)
O_2	40 (sccm)	75 (sccm)
RF power	50 (W)	50 (W)
Bias	35 (V)	35 (V)

By using the slope of etched mesa as the figure of merit, we notice that the ratio larger than 1 : 2 sufficiently produce a smoothed mesa slope that is in general larger than 120° without severe undercut and thus assisting the covering of mesa edge by metallic gates. In the Fig. 3.9 **c**, the reflow temperature is 90°C yielding an almost flat mesa edge with a measured angle of 174° within the time-frame of this dissertation. However, due to the change of PR in the clean room, the post-development baking for PR reflow has to be adjusted to be 120 °C for 5 min. This new recipe has been applied to the eight-dot device measured in Ref. [22] and all batches after that. As a result, the PR erosion and reflow provides a reproducible method to produce a smoothed mesa edge with a slope smaller than 10° by leveraging the flank control using photo-lithography and the fine tuning the etchant composition during RIE and consequently ensures the gate integrity and the connectivity.

3.3. NEW PROCESSES

So far only are the geometric optimizations concerned, whereas the atomistic imperfections in QuBus devices remain untouched. New processes covered by this section aim at addressing atomistic details such as the charged impurities in the oxides or substrates and the valley splittings naturally existing in a Si/SiGe device, from the device design perspective.

Sec. 3.3.1 tackles the problem of charged impurities dominantly locating at the interface between oxides and Si/SiGe substrates. These charged impurities are potentially induced by the ALD process for gate isolation that is necessary but can be further optimized by either fine tuning the process parameters of ALD or straightforwardly by eliminating the usage of avoidable amount of oxides. We stay with the latter solution within the frame of this dissertation.

Thereafter, a new generation device is proposed and briefly discussed to enhance the valley splitting by introducing a back-gate (see Sec. 3.3.2). This concept simply enhances the perpendicular electric field seen by the confined electrons in 2DEG yielding a tunable and enlarged valley splitting. The thorough work on this prototype is mainly achieved by Lucas Marcogliese for his master thesis mentored by me and Lars R. Schreiber. Instead of diving into details of numerical simulations, process integrations and the device testing, those can be found in his thesis [91], a brief introduction to the concept and corresponding technical difficulties are firstly reviewed. And this section is enclosed with an overview of the preliminary product and its future improvements as an outlook.

3.3.1. PALLADIUM GATE-ELECTRODES

Charged impurities in the device generate disordered potentials affecting the homogeneity of the potential landscape for shuttling electrons adiabatically in conveyor mode. These impurities could be either the electrostatic inhomogeneity seen by electrons in 2DEG as remote scattering sites [66, 79] or dynamically occupiable sites such as two-level fluctuators [80–82] those are inducing charge noises. Many approaches eliminating the charged impurities during fabrication processes have been suggested such as removing lossy dielectrics wherever possible; carefully optimizing fabrication recipes to avoid defects formation at interfaces; fabricating electrodes from crystalline materials, etc. [118]

The simplest and the most straightforward solution is to eliminate the charged impurities by using minimum amount of defects-rich oxides for manufacturing QuBus devices. In fact, not all oxides in the standardized process flow are necessary and the thickness of oxides may far beyond demands. These unwanted oxides are introduced by the ALD after metalizing Ohmics according to the standardized process flow. The original idea was to ensure an isolated substrate from gate electrodes, in particular the screening gates, using high quality oxides. In principle, a Schottky barrier can achieve the same goal by forming a direct metal-semiconductor contact. For QuBus, this Schottky contact is formed between the metallic screening gates and the Si-cap layer. With the carefully chosen metal and a good adhesion to Si, such a Schottky contact sufficiently prevents the leakage from gate to the substrate meanwhile provides the confinement along y-direction when voltages preserving the Schottky barrier height are applied. Moreover,

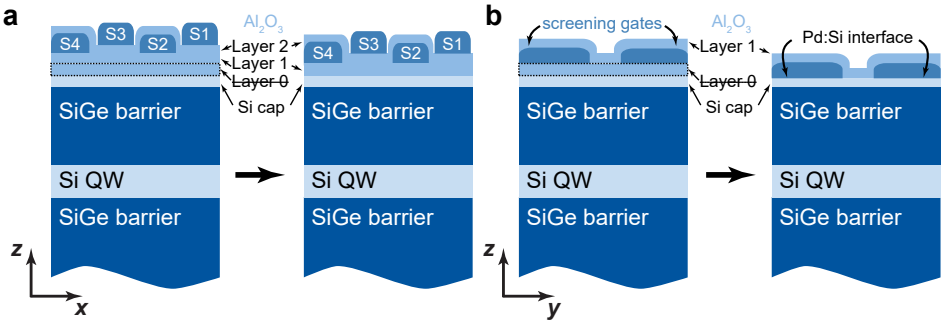

Figure 3.10: **Layer stacks of Pd QuBus comparing to the conventional QuBus: a** The xOz cross-section of conventional QuBus device (left) and the Pd QuBus (right). The first layer Al_2O_3 (Layer 0) is highlighted by the dashed line and not processed for the Pd QuBus. **b** The yOz cross-section of conventional QuBus device (left) and the Pd QuBus (right). Except for the screening gates, clavier gates are not shown here for simplicity. Intended Pd:Si interface for the Schottky contacts are labelled accordingly.

dropping off the first layer of oxides brings metallic screening gates closer to the substrate hence screening charged impurities underneath more efficiently. Last but not least, the capacitive-coupling of QDs to the shuttle gate-sets are enhanced simultaneously due to less oxides in between. Therefore, the optimization task becomes forming a Schottky-barrier with a proper gate material for the screening layer.

To form a Schottky-barrier with Si, alternative CMOS compatible and available metals in HNF are Pt and Pd. Estimating the Schottky barrier height for either one of them with Si is trivial, however inaccurate. Ideally, the Schottky-barrier height can be estimated according to the material work functions, as the band alignment of different materials provides the eventual band bending of the conduction band given by $E_C = -e(\varphi - \varphi_{ref}) - \chi$, where χ corresponds to the electron affinity of the material, and the φ_{ref} is a constant reference potential that is artificially chosen e.g. for silicon, the work function is a good choice i.e. $e\varphi_{ref} = E_w^{Si}$. However, cares must be taken that such a condition corresponds to the Anderson's rule for band alignment in heterostructures, where all materials are assumed to be largely separated from the vacuum level so that the vacuum level is continuous and flat. The real interface effects such as the electrical polarization, defect states and lattice mismatches at the interfaces are ignored in such an idealized model. In fact, contacting metal on top of Si pins the Fermi level in Si in its band gap depending on the density of surface states. This Fermi level pinning leads to an eventual Schottky-barrier height that may not directly correlate to the metal work function.

Interestingly, Pt cannot be directly deposited on top of Si due to its bad adhesion and only Pd remains possible. Despite of reported Schottky-barrier height of (0.72 ± 0.02) eV for the Schottky contact between Pd and Si [121], and applications on doped Si/SiGe quantum devices [122, 123], the most accurate estimation of this barrier height is to measure it electrically. Particularly at the Si-cap layer for QuBus fabrications, where the native oxides SiO_x strongly depends on the processing time and leading to a non-predictable Fermi-level pinning. In addition, the leakage paths to the 2DEG [124, 125] created by dislocations due to strain in the substrates [126] potentially contributes to

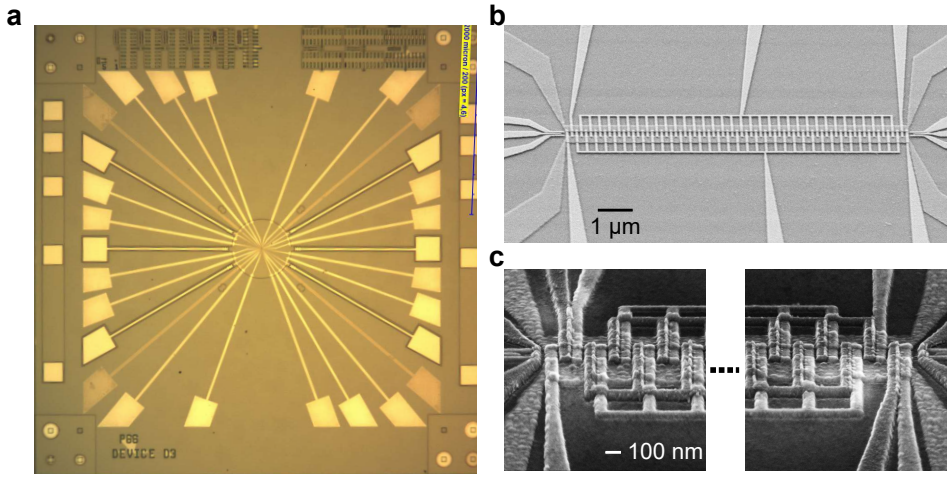

Figure 3.11: **Optical and SEM inspections of a processed Pd QuBus: a**. An optical microscope image of Pd QuBus where the Pd gates (darker) are optically distinguishable from others brighter metallic gate made of Ti:Pt. **b**. An SEM inspection of the Pd QuBus after metallization of the second layer of gates. The device is intentionally tilted by 45° to check the adhesion of Pd on Si by SEM during the device fabrication. **c** SEM inspections for the details of QuBus terminals at the end of the device fabrication.

nontrivial Schottky contact that cannot be expressed simply by a single value of barrier height. While attempts to improve the accuracy of Anderson's rule and calculations of Schottky-barrier between Pd:Si exist, yet imposing computation overheads that are far beyond the research interests of this work. Therefore, the method to validate the material choice for this process optimization becomes firstly ensuring the metal adhesion during fabrication and then electrically characterizing the device.

The new process to fabricate QuBus with Pd screening layer deviates slightly from the standardized process flow. Steps until metalizing the Ohmic contacts remain unchanged. Only will be the first ALD step replaced by a wet etching step (i.e. dipping the sample into 1% HF). This step essentially removes native oxides at the surface of Si-cap and within the exposed area where screening gate will be deposited ensuring a clean interface between the gate metal (Pd) and the substrate surface (Si). Following the similar process to the Ohmics metallization, cleaned chips will be loaded into the e-beam evaporator directly and the transfer lock will be vacuumed immediately to eliminate the oxidation of exposed area at the device surface. Consequently, 12 nm Pd is evaporated on top of the sample and the following lift-off step removes unwanted metal pieces to form designated screening gates. Thereafter, the standardized process flow continues with ALD process to isolate the screening layer.

During metallization of Pd screening gates, no adhesion layer is used as for other gates where a thin film of Ti is always deposited prior to Pt. To ensure the metal adhesion, thorough inspections are operated during processing. An optical inspection sufficiently evident the gate adhesion as shown in Fig. 3.11 **a** where the screening gates made of Pd show distinguishable darker color under microscope comparing to other metal gates made of Ti:Pt stack. This inspection ensures the integrity of Pd screening gates

visibly in micro-scale as no peel-off metal pieces occurring to Pd gates. Corresponding nano-scaled structures are inspected by SEM as shown in Fig. 3.11 **b, c** where the device is monitored after the second and the last loop of EBL patterning.

This new prototype QuBus device has been manufactured and characterized showing designated functionalities. Experimental results of the device using Pd screening gate is shown and discussed in Ch. 4 where the single-electron shuttling in conveyor-mode has been achieved with high charge shuttling fidelity of (99.7 ± 0.3) % across the full device and back (a total distance of 19 μm). Additionally, by positioning and detecting up to 34 electrons, a register of 34 QDs is initialized and demonstrated with arbitrarily chosen patterns of zero and single-electrons. These demonstrations draw the capability of employing Pd screening gate for high fidelity charge shuttle experiments. Furthermore, the disordered potential of this device is mapped by shuttle tomography in the conveyor-mode (see Ch. 5) benchmarking the performance of the shuttle device with the adapted material optimization and provides the first insights of the potential homogeneity in a long-range coupler for spin qubits. During the experiments, the Pd screening gate provides required confinement until the applied voltage exceeding 300 mV resulting in a breakdown of the Schottky-barrier. This upper limit shifts the QD perpendicular to the shuttle direction by ~ 30 nm providing sufficiently large space to circumvent the shuttled electron from atomistic defects such as localized potential disorders and valley splittings [29]. As a result, integrating Pd screening layer into QuBus prototypes appears to be a promising approach to eliminate the charged impurities and to potentially enhance the performance of QuBus devices.

3.3.2. BACK-GATE ETCHING

The valley splitting E_{VS}, corresponding to the energy difference between two low-lying energies of strained Si in Si/SiGe heterostructure, poses a main obstacle to use Si/SiGe heterostructure as host material of spin-qubits for a scalable quantum processor. Not only due to the spin-valley coupling resulting in the spin relaxation hotspot [26], also this intrinsically existing property varies randomly across the chip with a large span of experimentally observed energies (from 6 μeV to 270 μeV) [26, 27, 29, 127, 128] strongly relying on the atomistic details of the interface of Si-QW. Systematically enhancing E_{VS} becomes emerging interests for theorists, material growth and device design. Despite of appealing innovations on heterostructure engineering such as introducing a Ge-spike into Si QW layer [71] and the modulated Ge composition in Si QW forming a "wiggle-well" [72], theory studies reveal that E_{VS} can be tuned electrically by presenting its dependence on perpendicular electric field E_z. Based on the theory study, E_{VS} linearly depends on the out-of-plane E_z when $E_z > 2$ MV/m as the envelope function of ground state in a 10 nm Si QW shows negligible overlap with the lower Si/SiGe interface. [90] Further simulations employing both the tight-binding model and the effective mass method in Ref. [91] suggest that an $E_z > 3$ MV/m approximately enhances two-fold E_{VS}. Therefore, the corresponding FEOL approach from the device design perspective is accomplished by introducing a back gate to enhance the electric field E_z perpendicular to the 2DEG not less than 3 MV/m.

In particular, the QuBus devices in Si/SiGe demand only the local enhancement of E_{VS}. On one hand, the Si/SiGe heterostructure is grown on top of a Si substrate with

a thickness > 500 μm. If the back-gate is globally metalized on the backside of the Si substrate, the device needs to survive from a back-gate voltage of 1.5 kV to achieve the targeted E_z > 3 MV/m, which is not realistic. On the other hand, only is the channel region of a QuBus device demands enhanced valley splittings as a low E_{VS} during shuttle leads to the spin relaxation due to spin-valley coupling. As a result, the back-gate for QuBus needs to be efficiently implemented by etching through the Si substrate to place the back-gate closing to the 2DEG and it has to be aligned with the QuBus channel on the opposite side of the chip.

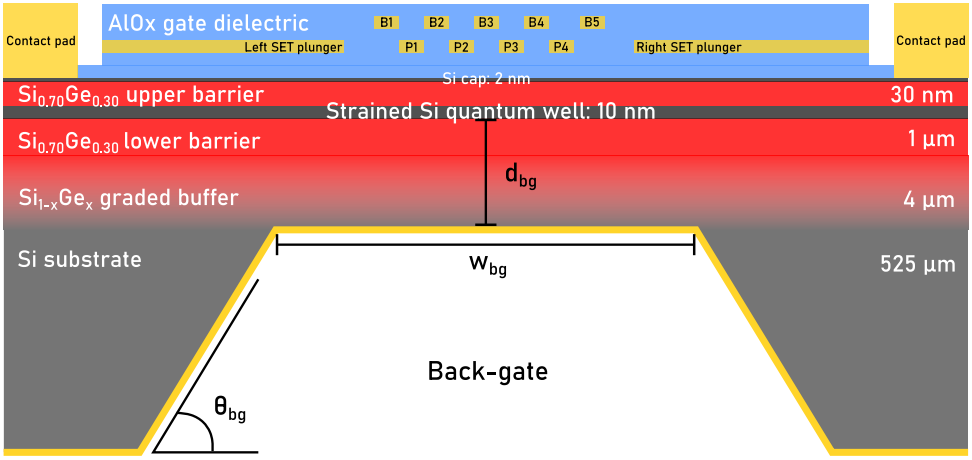

Figure 3.12: **Schematic of back-gated QuBus** The cross-section of a back-gated QuBus on Si/SiGe heterostructure taken along the center of a QuBus channel. This figure is adapted directly from Lucas Marcogliese's master thesis in Ref. [91]. In this example, a Si/SiGe heterostructure consists of (from bottom to top) 525 μm Si substrate, 4 μm graded SiGe buffer, 1 μm SiGe lower barrier, 10 nm SiGe upper barrier; and 2 nm Si cap layer. The back gate fills up an etched area with dimensions of $w_{bg} \times w_{bg}$ through the Si substrate and an flank angle of θ_{bg}. The functional part to enhance the electric field E_z is d_{bg} away from the 2DEG and is aligned with the QuBus on top of the Si cap layer.

Fig. 3.12 presents the initial guess of the back-gated QuBus. The metallic back gate is placed closing to the 2DEG by filling up the etched area aligned to the QuBus channel. The lower bound of the distance between back-gate and 2DEG (d_{bg}) is set to the thickness of the graded buffer layer plus the thickness of the lower SiGe barrier, in this case 5 μm for the wafer grown by Lawrence semiconductor, which is mainly processed and characterized for this dissertation. This design allows an local enhancement of the E_z taking the following criteria into account. First, the strained Si QW in the Si/SiGe heterostructure should not experience relaxation due to etched back-gate. Second, the leakage current of back-gate should not induce exceeding heat dissipation at demanded E_z. Third, the newly implemented back-gate should not affect the functionalities of QuBus devices. Last, the introduced back-gate should not limit the readout bandwidth of SETs. These criteria result in the final geometric constraints of: $d_{\mathrm{bg}} \in [5, 15]$ μm assuming one could apply maximally −50 V back-gate voltage; $w_{\mathrm{bg}} \in [50, 175]$ μm, given that the readout bandwidth is not less than 6 MHz to fulfill the need of Pauli-spin blockade readout; and $\theta_{\mathrm{bg}} < 90°$ for the ease of metallization as the readout bandwidth is nominally inde-

pendent of the flank angle (see detailed simulations and analysis in Ref. [91]).

Different from the etching processes discussed previously in Sec. 3.2.1 for the cryo-markers and in Sec. 3.2.2 for the smoothed mesa, deep etching with high aspect ratio is needed for back-gates. Both wet etching and dry etching are applicable, whereas owing specific challenges. On one hand, the former requires a longer process time by dipping masked Si-substrate into 25 % TMAH at 80 °C over few hours meanwhile the front size of the processed chip is sealed by a special sample holder. This approach yields inefficiency as the processed chip cannot by parallelized and each process takes few days. On the other hand, the latter deep dry etching is more time efficient, however meets more constraints and more process parameters to tune with. For this high aspect ratio etching task, the Bosch process is generally used in industrial fab-line to produce features such as through-silicon vias (TSV). It essentially separate the deep etching process into cycles. Each cycle includes three step: (i) the isotropic etching of the masked Si by SF_6, (ii) fluorocarbon polymer (C_4F_8) deposition for sidewall passivation, and (iii) Anisotropic etching of polymer on the bottom of trench to expose Si for the next cycle. Such an approach intrinsically induce a scallop-like periodic pattern on the sidewall and polymers covering the sidewall is difficult to thoroughly clean. Moreover, the flank is nearly straight leading to difficulties for metallization. For these concerns, the tapered Bosch process is employed and developed for the back-gated QuBus. The tapered one is inspired by iterating isotropic etching and anisotropic Bosch etching cycles to preserve hard mask while yielding positive sidewall angle via intentional undercut. Similarly, the tapered Bosch process can be decomposed into cycles. Each cycle includes: (i) a number of Bosch cycles explained before. (ii) using inductively-coupled SF_6/O_2 plasma mixture for polymer removal from sidewalls. (iii) isotropic etching of Si by SF_6/O_2 mixture to smooth and tapper the sidewalls.

The back-gated QuBus fabricated by the tapered Bosch process is inspected under SEM as shown in Fig. 3.13 **a,b** corresponding to an etched and metalized back-gate with targeted $w_{bg} = 80\ \mu$m and $d_{bg} = 500\ \mu$m. The metallization step for this example employs the e-beam evaporated Al, which can be replaced by the Ti:Pt as for the standardized process or sputtered TiN. The device validation is accomplished by operating a transmission Fourier transform infrared spectroscopy (FTIR) measurement with an incident IR light of $\lambda = 2.53\ \mu$m. Leveraging the transmittance of IR through Si, any discontinuity of the Al coverage on top of the etched back-gate can be visualized (see Fig. 3.13 **c,d**). As an example, an intended broken metalized gate is shown in Fig. 3.13 **d** as a reference. As a result, the complete coverage of etched area for the back-gate evidently shows the capability of tapered Bosch process for manufacturing back-gated QuBus devices.

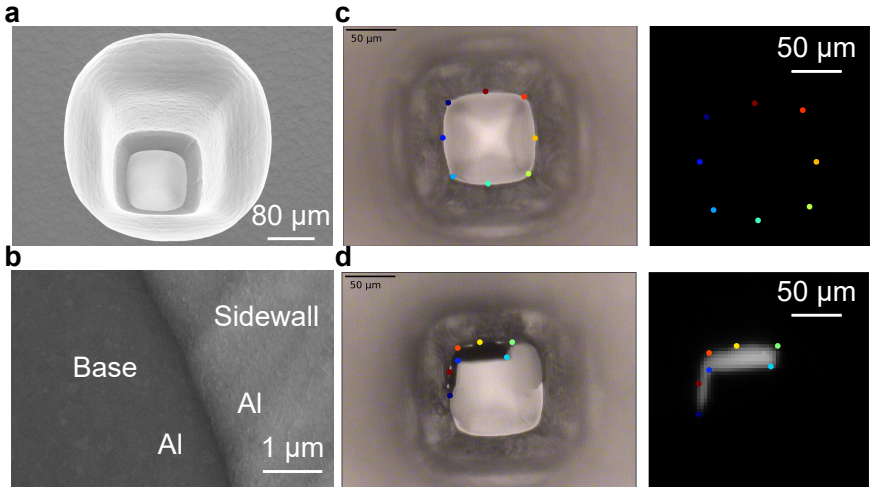

Figure 3.13: **SEM inspection and the transmission FTIR measurement of back-gated QuBus: a** An SEM image of back-gate etched by tapered Bosch process. **b** Zoomed-in view at the bottom of edged hole. Darker and brighter region correspond to the base and the sidewall covered by Al as labelled. **c** Transmission FTIR of a conformal metal coverage of edged hole. The darkness of figure in the right panel stands for the relative transmittance of incident light with a wavelength of 2.53 μm. Coloured dots indicate the corresponding positions on the measured device. **d** Transmission FTIR measurement of an intentionally broken back-gate sample. All figures are adapted from Ref. [91].

4

LONG-RANGE SHUTTLING OF ELECTRONS BY QUBUS

Si/SiGe QuBus for single electron information-processing devices with memory and micron-scale connectivity function

Ran Xue[1], Max Beer[1], Inga Seidler[1], Simon Humpohl[1,2], Jhih-Sian Tu[3], Stefan Trellenkamp[3], Tom Struck[1,2], Hendrik Bluhm[1,2] and Lars R. Schreiber[1,2]

1. JARA-FIT Institute for Quantum Information, Forschungszentrum Jülich GmbH and RWTH Aachen University, Aachen, Germany
2. ARQUE Systems GmbH, 52074 Aachen, Germany
3. Helmholtz Nano Facility (HNF), Forschungszentrum Jülich, Jülich, Germany

The connectivity within single carrier information-processing devices requires transport and storage of single charge quanta. Single electrons have been adiabatically transported while confined to a moving quantum dot in short, all-electrical Si/SiGe shuttle device, called quantum bus (QuBus). Here we show a QuBus spanning a length of 10 μm *and operated by only six simply-tunable voltage pulses. We introduce a characterization method, called shuttle-tomography, to benchmark the potential imperfections and local shuttle-fidelity of the QuBus. The fidelity of the single-electron shuttle across the full device and back (a total distance of 19* μm*) is* (99.7 ± 0.3) %*. Using the QuBus, we position and detect up to 34 electrons and initialize a register of 34 quantum dots with arbitrarily chosen patterns of zero and single-electrons. The simple operation signals, compatibility with industry fabrication and low spin-environment-interaction in* ^{28}*Si/SiGe, promises long-range spin-conserving transport of spin qubits for quantum connectivity in quantum computing architectures.*

AUTHOR'S CONTRIBUTION

THIS chapter is mainly based on the published peer-reviewed journal article "Si/SiGe QuBus for single electron information-processing devices with memory and micron-scale connectivity function" in *Nature Communications* **15**, 2296 (2024). The main context experiences minor changes with respect to the adapted figures in order to match the consistency of this dissertation. In this chapter, the experiment setup and the characteristics of the measured device at 4 K are explained in details in addition to the original published manuscript. Moreover, expanding the read-out method and the sensitivity of the SET gives more insights of the device performance as well as the limitation of this experiments. Contrarily to the original manuscript, some detailed discussions of the measured charged defect in this experiment is only introduced briefly and to be revised incorporating further characterizations in the Ch. 5.

Many hands make light work. The experiment was mainly conducted by R.X. with help from M.B., L.R.S., R.X. and M.B. analyzed the data with L.R.S. S.H. provided measurement software. T.S prepared the passive voltage adder. M.B. adapted the developed process by R.X., J., S.T. and I.S for the device fabrication and fabricated the device. S.T. operated e-beam lithography. L.R.S. designed the device and supervised the experiment. L.R.S. and H.B. provided guidance to all authors. R.X., M.B. and L.R.S. wrote the manuscript, which was commented by all other authors.

4.1. RESEARCH BACKGROUND

CONTROLLING local charge densities in a semiconductor by metallic gate-electrodes sets the foundation of modern nanoelectronics. Miniaturization of gate-electrodes reveals quantum mechanical effects and entertains the development of nanoelectronics devices operating with single charge quanta. Discrete charge states of quantum dots (QDs) are stored to process digital information [129] and the spin of individual electrons is used to encode quantum bits for quantum computing in semiconductors [130, 131]. The exchange of charge quanta between functional blocks such as charge-photon interfaces [132–134], quantum registers [135], spin manipulation zones [136], single charge detectors [137] and current standard devices [138] would lead to quantum devices with new functionalities.

For conventional electronics, wires transport currents or voltages over extended distances. In quantum technology, wires cannot transport individual charges, as disorder limits their localization length hardly exceeding 100 nm. In micron-sized quantum structures, the charging energy becomes impractically small for utilizing charge states with definite electron number. A proposed device named quantum bus (QuBus) [43] solves this fundamental difficulty and might provide the key for the required [5, 139] scale-up of quantum computing architectures [15–18].

Single electron [140, 141] and spin-conserving electron [142] shuttling has previously been demonstrated employing surface acoustic waves in piezoelectric semiconductors. Shuttling in non-polar materials such as silicon, which is highly attractive for quantum computing with electron-spins [58, 143–145], becomes more involved, as the electron transport requires a series of top gates. However, this additional complexity comes with the benefit of electron acceleration and velocity control [44, 45, 146–148]. In particular,

the conveyor-mode shuttling approach in Si/SiGe combines this advantage with predictable spin coherence during shuttling and the requirement for just four input signals independent from the length of the shuttle device [43]. High-fidelity short-range conveyor-mode charge [21] and spin [22] shuttling has been demonstrated.

4.2. LONG-RANGE SHUTTLE OF SINGLE-ELECTRONS

IN this work, we all-electrically position and detect up to 34 electrons in Si/SiGe by a 10 μm long QuBus working in a single-electron conveyor-mode. Firstly, a workflow of characterizing QuBus device according to the protocol developed by Niels Focke [98] is employed and being operated by Max Beer [149] as a part of his master project to select a well-performed device (see details of the measured device in Sec. 4.2.1). Here the potentially functional devices are pre-screened at 4 K to find out a fully functional QuBus by verifying its electrical characteristics and functionalities. The functionalities under investigations includes the formation of both SETs, the induced current through 1DEC and the pinch-off of such an induced current by all clavier gates individually. Corresponding experimental results are presented in Sec. 4.2.2. Secondly, the selected best performed QuBus is transferred into a millikelvin cryostat (see the details of experimental setup in Sec. 4.2.3) where the charge sensing of the QDs at both ends of 1DEC and the formation of shuttle QDs within 1DEC is experimentally operated and characterized (see measurement results in Sec. 4.2.3 and 4.2.4). Ultimately, the conveyor-mode shuttling of up to 34 electrons is demonstrated with a 10 μm QuBus device. Despite its unprecedented length and more than 100 electrostatic gates, the QuBus can be controlled by only six input terminals with low voltage pulse complexity (see pulsing schemes in Sec. 4.2.4).

Shuttling electrons by means of QuBus is not only an ultimate goal of designing such devices, but also a useful method to thoroughly understand the material properties of a quantum device based on semiconductors particularly the Si/SiGe heterostructures. In this research, we introduce a characterization method we call shuttle tomography to benchmark the local shuttle fidelity of the QuBus using a single electron as a probe. Experimental results are detailed in the Sec. 4.3. By composing elementary pulses, we can control and detect any single electron pattern filling a series of 34 QDs (see Sec. 4.4). The conveyor-mode shuttle approach opens up new possibilities for probing local potential disorder in a quantum well, detecting single electrons with high lateral resolution across a length of 10 μm and boosting multi-electron control for scalable spin qubit quantum computation.

4.2.1. 10 μm LONG QUBUS

The QuBus device under investigations is fabricated on a Si/SiGe heterostructure. The undoped quantum well heterostructure is grown by chemical vapour deposition on a 200 mm silicon wafer and consists of a 7 nm tensile-strained silicon layer sandwiched between two relaxed layers of $Si_{0.70}Ge_{0.30}$. The upper barrier layer of $Si_{0.70}Ge_{0.30}$ has a nominal thickness of 30 nm and is capped by 2 nm of Si. Ohmic contacts to the quantum well are created by the selective phosphorus ion-implantation followed by a rapid thermal anneal at 700 °C for 30 s. The contacts are then metalized using optical lithography and metal lift-off. Three metallic gate layers including fan-out are fabricated via elec-

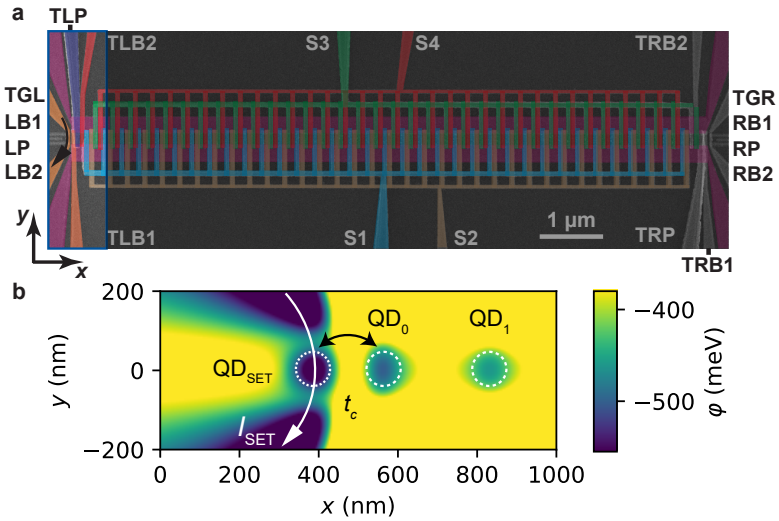

Figure 4.1: **QuBus device for shuttling electrons and the simulated electrostatic potential of its left terminal. a**, False-colored scanning electron micrograph of a top-view on a device nominally identical to the measured device. The gate labelled TGL overlaps with two barrier gates LB1 and LB2 and accumulates the electron reservoirs for the left SET. The gate labeled TLB2 is electrically connected to terminal S_4. **b**, The simulated electrostatic potential (φ) of the left terminal of the QuBus corresponding to the highlighted region in **a**. The dashed circles illustrate the relative positions of SET sensor dot (QD_{SET}), the first individually controlled QD by gates TLB1, TLP and TLB2 (QD_0) and the first shuttle QD in the conveyor potential belt defined by clavier gate sets $S_{1,...,4}$ (QD_1). The QD_0 is either tunnel-coupled to the QD_{SET} for loading and unloading electrons or capacitively coupled to the QD_{SET} to sense the occupancy of QD_0 without unloading the electron depending on the gate voltage applied to gate TLB1. The measured current path I_{SET} is indicated by the white arrow. The Thomas-Fermi approximation is applied to the SET region for the electrostatic simulations using COMSOL [92].

tron beam lithography and evaporation followed by metal lift-off. Details of fabrication processes and the optimizations are discussed previously in Ch. 3. A scanning electron micrograph of a device nominally identical to the device measured in this work can be seen in Fig. 4.1 **a**. The first gate layer is deposited directly onto the silicon capping layer, the native oxide layer of which was removed immediately before metal evaporation via HF etching. For this lowest layer 15 nm of palladium is used in order to fabricate a Schottky contact to the Si-cap. According to the electrostatic simulations [43], this results in a lower potential disorder in the quantum well. The later two gate layers are fabricated on 7 nm of atomic layer deposited Al_2O_3 and consist of 5 nm of titanium and 22/29 nm of platinum for the second and third layer, respectively.

The first fine gate layer defines both the SET plunger and barrier gates as well as the channel-confining split-gate. The split-gate constrains the 1DEC to a width below 200 nm. The second and third metal gate layers define the SET top gates as well as the clavier gates, which form the individual QDs in the 1DEC. These clavier gates have a width of 60 nm with a pitch of 70 nm. More than 100 clavier gates, equally distributed among the second and third layer above the 1DEC enable the approximately uniform movement of single electrons (conveyor-mode shuttling, the dynamics of which is visu-

alized by the video of the simulated electrostatics in the Supplement of published online version.) along the x-direction (Fig. 4.1 **a**) even in the presence of electrostatic disorder [43]. Notably, every fourth clavier gate is electrically connected to one of four gate sets S_i ($i = 1...4$). The connection scheme of four gate sets can be easily implemented as our clavier gates are distributed among two electrically isolated layers. The designed distance between SET and QD_0 and thus the tunnel-coupling is based on Ref. [93].

On demand, a single electron can be loaded into the 1DEC from the left SET formed by the gates TGL, LB1, LP and LB2. The right one as a twin SET is formed by the gates TGR, RB1, RP and RB2 (see the gate layouts and corresponding names in Fig. 4.1a). Both SETs act as electron reservoirs and charge sensors simultaneously setting the foundation of an electron shuttling experiment. Therefore, a QuBus device with fully functional SETs needs to be selected. Additionally, as being explained in the Sec. 2.2.3, the working principle of the QuBus requires an all-electrically controllable 1DEC, in which a series QDs can be laterally controlled by clavier gates. It thus demands a fully conducted 1DEC and the current path can be pinched off by each clavier gates individually.

Moreover, the formation of QD is one of the most fundamental requirements that confines electrons for shuttling in conveyor-mode. Within the 1DEC, the plunger gate TLP of the leftmost quantum dot QD_0 controls the loading of exactly one electron from the SET to QD_0 which is tunnel coupled to the SET as depicted in Fig. 4.1b. Furthermore, to shuttle the single electron in a moving QD, the shuttle QDs are formed by applying sinusoidal voltages to clavier gate sets as being explained in the Sec. 2.2.3. The possibility of forming QDs becomes an essential electric characteristic of a fully functional QuBus for single-electron shuttling experiments.

Notably that, basic functionalities of the SETs and the 1DEC can be simply verified at 4 K before more complicated wiring and measurement techniques are conducted to the device at a millikelvin cryostat. However, 4 K is a relatively too high temperature to form QD in Si/SiGe that is limited by physics. Therefore, the pre-characterization at 4 K covers all verifications till the formation of QDs. Such a process efficiently accelerates the turnaround time of finding a well performed QuBus for single-electron shuttling experiments. The formation of QDs is only operated on pre-selected devices with presumably high performance at millikelvin cryostat as a part of the device tuning.

4.2.2. DEVICE PRE-SCREENING AT 4 K

Three working packages are involved in a pre-screening measurement at 4 K in order to efficiently validate the functionalities of both two SETs and the electrical controllability of the 1DEC. Firstly, the formation of SETs is accomplished by accumulating 2DEG under the top gates of SETs i.e. the TGL(R) gates and consequently pinching off the current individually by each barriers i.e. L(R)B1 and L(R)B2. Secondly, the current through 1DEC is induced by ramping up all clavier gates covering the channel region and then such a current path is pinched off by each clavier gates individually providing their existence and completeness. Thirdly, a barrier-barrier two dimensional scan of each SETs is operated providing the working point of corresponding SET within the gate space that is constructed by barrier gates of each SETs.

An I-V characterization essentially reveals the functionality of an SET. For SETs based on an undoped Si/SiGe heterostructure, those are operated in the accumulation mode,

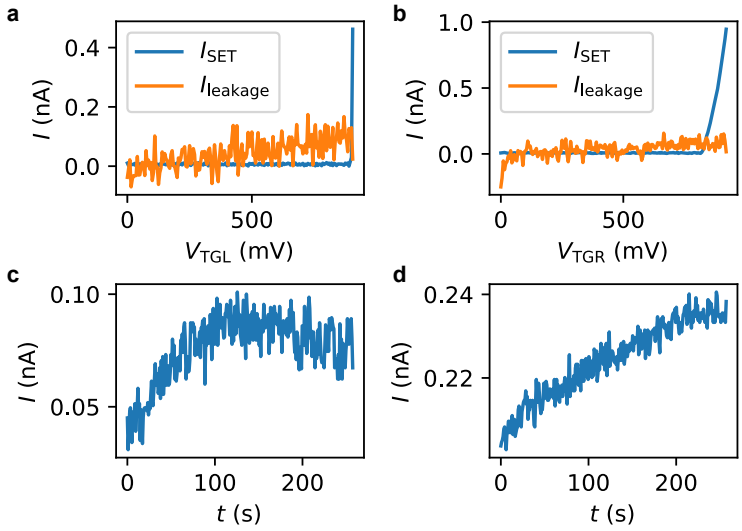

Figure 4.2: **Verification of SETs by I-V characteristics and their time stabilities at** 4 **K. a**, the accumulation I-V characteristic of the left SET by ramping up the top gate (TGL) voltage (blue). The leakage currents from TGL to grounds are inspected and plotted in orange. **b**, similar I-V characteristic of the right SET with the measured accumulation current (blue) and the leakage current (orange) from TGR to grounds. **c**, The time stability measurement of the left SET current over 250 s. **d**, The time stability of the right SET over the same time span as the left one. Results are adapted from Ref. [149] and rearranged here to fit the content.

their conductive channels need to be accumulated by ramping up the top gate voltage exceeding corresponding threshold voltage analogy to the field effect transistors (FETs). Particularly, the conventional design of the SET in a QuBus device, where the top gates overlaps with two barrier gates, demands extra cares during accumulation due to the screening effects from the metallic gates underneath top gates. In this experiment, the top gate (TGL(R)) and barrier gates (L(R)B1,2) are ramped simultaneously with the same ramp rate such that the conducting channel opens up easily. In addition, the top gate should be well isolated from the substrate and the device ground so that the integrity of the accumulated current I_{SET} remains and it is not interfered by leakage currents from the top gate to the grounds or wherever unwanted. Fig. 4.2 a,b illustrate the accumulation I-V curves of SETs on the left- and right-hand side of the QuBus, respectively. Analogy to that of an FET in classical electronics, an exponentially increasing current is expected and observed upon the top gate voltages exceeding a threshold voltage so that electrons as free charge carriers are accumulated under the region of the top gate and flow from source to drain driven by an applied bias voltage. For each SET, the measured current I_{SET} represents the current flow from the source to drain under the biasing voltage V_{SD} (solid blue lines in Fig. 4.2 a,b). The top gate leakage (solid orange lines in Fig. 4.2 a,b) is measured simultaneously as ramping up the top gate voltages ($V_{TGL(R)}$). A negligible leakage current (one magnitude lower than the I_{SET}) is measured for each SETs reflecting a sufficiently high quality of the oxides surrounding the top gates for the measured device.

Not only the capabilities of accumulating a conductive channel under the top gates, but also the sustainability of induced current guaranties the functionalities of an SET. Once the current path is accumulated, a stable current level over time is demanded to reduce the retuning overhead during the shuttling experiment which may run for a few months. Fig. 4.2 c,d inspect the time stabilities of SETs in this QuBus device at 4 K. A slightly and gradually increasing current level is observed on both SETs within the measurement time frame (250 s). It is obvious that the stability of SETs are not as robust as expected, however, the setup limitations play a role for a 4 K measurement. First of all, the temperature of the device is significantly higher than sub-100 mK where a long term experiment is operated. And the electric noise isolation of the 4 K setup is not treated as seriously as the cryostat. After all, the device reaches different thermal equilibrium states after each cool-down with different charge configurations and thus the induced currents saturates over time to different current levels. Therefore, the absolute current level at 4 K does not give a full picture of the SET performance and the slowly charging up behaviors as shown in Fig. 4.2 c,d are in fact acceptable as long as no distinguishable and discrete jumps of current levels being detected.

Eventually, the functionalities verification for both SETs are finalized by the two dimensional pinch off scan in the gate space as depicted in Fig. 4.3 a,b where a conducting island on the top-right corner for both SETs is measured. It indicates the existence of induced current underneath the corresponding top gate that can be pinched off by ramping down the barrier gates. On the left bottom corner of a conducting island in a 2D pinch off scan, the sensor dot is formed and Coulomb oscillations are expected as finger prints of an existing QD. However, due to the thermal broadening at 4 K, the Coulomb oscillations are not easily detectable. Also such a measurement needs to be repeated after transferring the device to a cryostat, which is a sensitive and nontrivial task to tune the device for shuttling experiments. Therefore, only the 2D scans with a rough voltage resolution (50 mV) are acquired at 4 K to verify the basic functionalities of SETs efficiently and to be repeated for the device tuning at sub-100 mK temperature in a cryostat.

In addition to SETs, the induced current through the 1DEC is equally essential and can be simply verified during a pre-characterization at 4 K as well. By ramping up all clavier gates covering the 1DEC region, the 1DEC is accumulated and the current flowing through the 1DEC becomes detectable by applying bias voltage between two reservoirs at both ends of the QuBus i.e. source or drains of both SETs. In this measurement, a bias voltage of 100 μeV is applied on only one SET, whereas the other experiences no bias voltage. Notably that, due to non-zero bias output of the Stanford Research Lock-in Amplifier (SR830) being used in this experiment, a minimum 0.4 μeV biasing voltage is unavoidably applied to the non-biased SET.

Fig. 4.3 c presents the induced current through 1DEC that is pinched off by each clavier gate individually. All I-V curves show a similar cutoff voltage within a span of 0.2 V. In particular, the clavier gates S2 and S4 located at the second layer show a similar pinch off voltage due to their nominally same features. Moreover, each of them contains 34 gate electrodes providing the highest capacitive coupling to the 1DEC thus the highest pinch off voltage among all clavier gates. Similarities of S1 and S3 gates are observed as well given the nominally identical I-V curves. Additional oxides beneath them comparing to S2 and S4 reduces their capacitive coupling to the 1DEC, and thus a lower pinch off

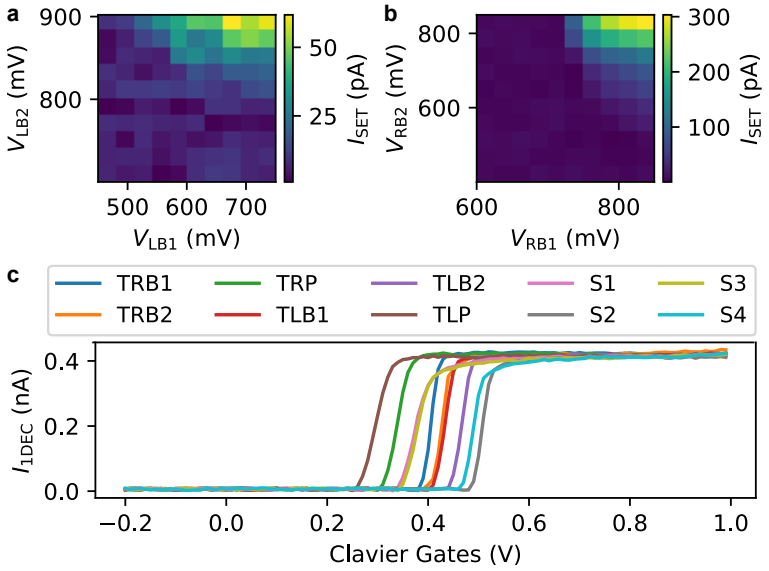

Figure 4.3: **Operational window of the SETs and 1DEC a**, A two-dimensional conductance measurement of the left SET in the gate space by sweeping voltages applied to two barrier gates (LB1, LB2). **b**, A two-dimensional conductance measurement of the right SET in the gate space by sweeping voltages applied two barrier gates (RB1 and RB2) similar to the scan for SET left in **a**. **c**, Pinching off the current in 1DEC along the QuBus by ramping down each clavier gates individually. Notably that the scan direction is from the higher voltages to the lower end. All line scans are acquired consequently and the name of corresponding clavier gate is labeled in the legend on top of the plot. After each scan, the current is always reset to the initial point by resetting the swept clavier gate voltage to its starting point. Results are adapted from Ref. [149] and rearranged here to fit the content.

voltage is measured. Different from the S-gates with multiple gate electrodes, the T-gates at each terminals of a QuBus contain only one gate electrode providing lowest capacitive coupling to the 1DEC. Furthermore, their relatively closer position towards SETs lead to a larger influence from the screening effects of reservoirs. Spreading pinch off voltages are expected and detected in this experiments where TL(R)P gates show lower values as they are on the third layer, and TL(R)B1, 2 show a similar and higher pinch off voltage near 0.4 V between those of S-gates. Such observations indicate the homogeneous electric characteristic among all clavier gates and eventually signal a potentially well-performed and valuable QuBus for the electron shuttling experiments.

4.2.3. DEVICE TUNING AT CRYOGENIC TEMPERATURE

EXPERIMENTAL SETUP

A pre-selected QuBus device with potentially full functionalities is transferred to a dilution unit operating at sub-100 mK. Experiments are conducted in an Oxford Triton 200 dilution refrigerator (named "Selene" for internal reference) operating at ~ 60 mK (see schematics of the cryostat in Fig. 4.4). In total, 96 DC lines and 14 RF coaxial cables are available in the system. However, only the electric connection to the mixing chamber

(MC) plate (i.e. one DC loom with 24 lines see the orange dashed band in Fig. 4.4) fully functional and is connected to the device under investigation. To compromise, a base band experiment for shuttling electrons in conveyor-mode is conducted here meaning that both electrically pulsed gate voltages and the charge read-out rely on DC looms with limited bandwidth (1 kHz and 3 kHz, respectively).

In Fig. 4.4 the wiring scheme attaches to the schematics of experimental setup. Voltage pulses are generated by a Zurich Instruments HDAWG8 and superposed with DC voltages from a home-built DAC by a passive voltage adder at room-temperature. Different resistance (10 and 150 Ω for the DC port and the pulsing input, respectively) resulting in a factorized pulsing output composing both channels so that pulsing gates in range of millivolts requires an output in the magnitude of volts that makes use of a full output range of AWGs. All signal lines (outputs of the voltage adder) are then filtered by Pi-filters with a cut-off frequency of 1 kHz in the break-out box. No low-temperature filtering is used. For the read-out, the SET current is converted by the low-noise transimpedance amplifier SP983c from Basel Precision Instruments. A secondary low-pass filter with a cut-off frequency of 3 kHz is integrated inside the amplifier and is used in this experiment. The converted voltages passes a Gain-one amplifier which does not amplify voltages but serves as ground decoupler to avoid ground loops. Finally, the SET signals are digitized by an AlazarTech ATS9440 waveform digitizer. The composition of pulse sequences employs the open-source Python package qupulse [150].

DEVICE TUNING AT ~ 60 MK

Similar to the procedure as being done for 4 K characterizations, the device is cooled down to sub-100 mK with all gates being grounded to avoid unwanted charging effects. Once the system cooled down to the operational temperature, the device is connected to the control electronics at room temperature for further experiments. The complete tuning routine upon shuttling electrons contains (i) the SET accumulation and characterization; (ii) the charge sensing of the terminal QD (i.e. the QD at the end of 1DEC controlled by T-gates); (iii) forming a shuttle QD next to the terminal QD.

Firstly, both SETs are accumulated by ramping up the sensor top gates TGL(R) and barrier gates L(R)B1, 2 underneath. Thanks to the better isolation to electric noise than the 4 K setup and its significantly lower temperature suppressing the thermal broadening, both SETs show the Coulomb oscillations of sensor dots (see Fig. 4.5 **a,b**) in 2D pinch off measurements.

Different voltage symmetries are observed by comparing two pinch off results. The Coulomb oscillations of the left SET distinguishably appear in the gate space of LB1 and LB2 where both barriers gates are swept in a similar voltage range (360 ± 50 mV and 350 ± 50 mV for LB1 and LB2 respectively) as shown in Fig. 4.5 **a**. However, asymmetric scan window (see Fig. 4.5 **b**) has to be applied to the right SET (380 ± 50 mV and 230 ± 50 mV) to detect the Coulomb oscillations. It indicates clearly that the sensor dot of left SET forms at the designated position between two barrier gates and it is controlled equally by either barrier gates, whereas the barrier gate RB1 for the right SET experiences screening effects comparing to its twin barrier gate RB2 that operates at a lower voltage range (i.e. 150 mV less than RB1). It signals that the left SET will potentially behave ideally but the right one may not perform as expected.

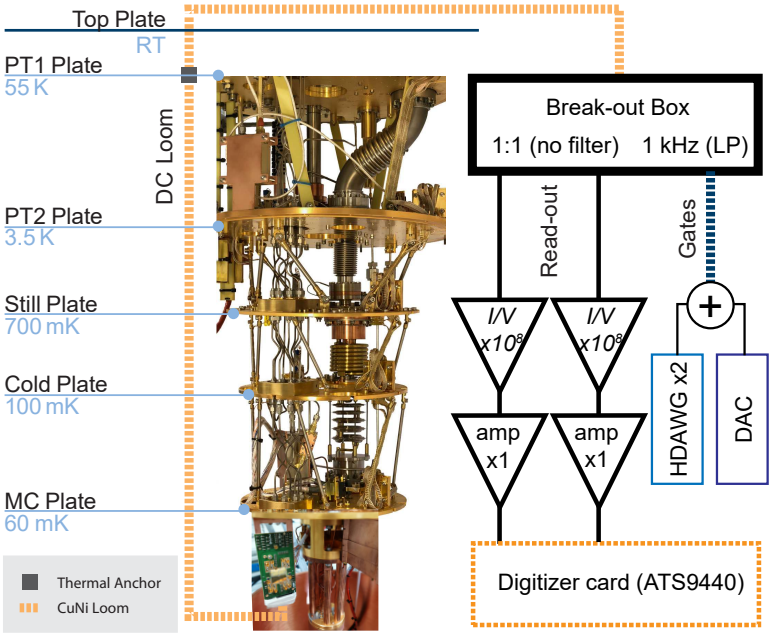

Figure 4.4: **Experimental setup and wiring schematics** The pulsed tube dilution unit ("Selene") for cooling down the QuBus device down to 60 mK. The device is thermal anchored to the mixing chamber plate by a copper "L-piece" sample hold. DC looms connect all gate electrodes and ohmic contacts of the QuBus without low temperature filters. Only within in the break-out box at room temperature are the gate voltages filtered by a low-pass (LP) Pi-filter with a cut-off frequency of 1 kHz. Voltage pulses are generated by a Zurich Instruments HDAWG8 and superposed with DC voltages from a home-built DAC by a passive voltage adder at room-temperature. The SET currents are not filtered in the break-out box but converted to voltages by the low-noise transimpedance amplifier SP983c from Basel Precision Instruments with a gain factor of 10^8 V/A. Amplifiers with a gain factor 1 (i.e. no amplification applied) are used to decouple the ground between setup and the PC where the waveform digitizer card AlazarTech ATS9440 is mounted.

Besides the symmetry of the applied voltages to both barrier gates, the level spacing between Coulomb oscillations matters and indicates the performance of SETs as well, because the level spacing between Coulomb oscillations corresponds to the charging energy of a sensor dot and in turn reflects the physical dimension of a sensor dot. From the bottom left to the top right of Fig. 4.5 **a**, the left SET shows nominally equally spacing oscillations with increasing conductance as higher voltages are applied to both barrier gates. It is an expected behavior of a quantum dot defined by a parabolic potential well with a fixed charging energy, indicating a potentially fully functional SET without charged defects nearby. Contrarily, the oscillations of right SET are modulated and obscured by conductance variations (i.e. the dense and periodical pattern on the right-hand side of the 2D pinch off plot in Fig. 4.5 **b**) with higher frequency than that of the sensor dot. Such an observation is attributed to imperfect reservoirs near the right sensor dot and strongly tunnel-coupled to the designated sensor dot. Given the fact that the unwanted pattern has a higher oscillating frequency than the sensor dot in the gate space, it is straightforward to conclude such a scenario that the physical dimension of

unwanted potential well is much larger than the sensor dot. As a result, amounts of quantized states are available for electrons to tunnel into within the small vicinity of the targeted sensor dot. Consequently, the measurable current path becomes more complex than an ideal SET that is source - sensor dot - drain and it eventually leads to a useless SET for charge sensing.

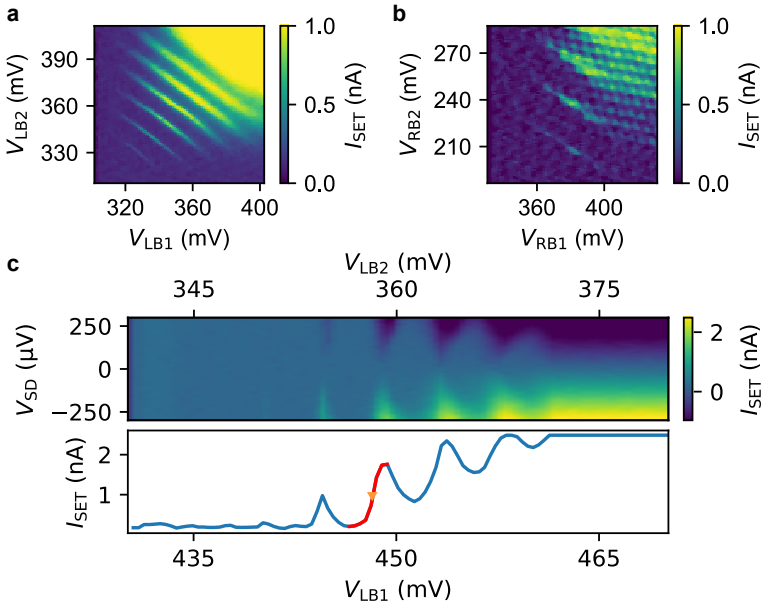

Figure 4.5: **Tuning up SETs at sub-100 mK and the Coulomb diamond measurement of left SET a**, The 2D pinch off measurement of the left SET in gate space. **b**, The 2D pinch off measurement of the right SET in gate space. **c**, The Coulomb diamond measurement of left SET in gate space constructed by both LB1, 2 (upper panel). Corresponding sweep ranges of each barrier gates are labeled on the top of upper panel and on the bottom of the lower panel. A line-cut at $V_{SD} = -300\,\mu$eV is taken and plotted in the lower panel, in which the selected Coulomb peak for charge sensing of proceeding experiments is highlighted in red with the operational point marked by the orange triangle at the steepest slope of this Coulomb peak.

In this experiment, only the left SET is used to load an electron into QD_0 and senses its the charge occupancy for read-out, while the right SET and the rightmost clavier gates are not used here and voltages are chosen to have an open 1DEC towards an energetically lower lying electron reservoir.

The read-out method of this experiments relies on the base-band single-shot read-out that the charge occupancy of the terminal QD next to the SET (e.g. the QD_0 next to the left SET) is sensed by the discrete current levels of the SET. The current-charge conversion is the corner stone of such a technique. One needs to know how to convert the read-out current level to the charge occupancy of QD_0 correctly. Also the sensitivity of detecting a single-electron tunneling by such an SET needs to be characterized, and to this end Coulomb diamonds of left SET are measured after 2D pinch off (see Fig. 4.5 **c**). Two barriers of left SET (LB1 and LB2) are swept from left to right with corresponding voltage ranges as labelled in the x-axis of the lower panel and that of upper panel, re-

spectively. A scan of the bias voltage (V_{SD}) ranging from $-300 \rightarrow 300\,\mu$eV is labelled as the y-axis of the upper panel.

Distinguishable Coulomb blockades are observed within the measurement window as expected indicating the formation of a defect free sensor dot that is ideal for charge sensing. The working point of the SET is empirically determined by choosing a Coulomb peak whose steepest slope aligns with respect to the current level 1 nA (see the lower panel of Fig. 4.5 **c**). Here the red line highlights the chosen slope of a Coulomb peak whose waist aligns to 1 nA and is marked by the orange triangle. It is an empirical number to tolerate the electric background noise at sub-100 pA that is only used to tune up the QuBus device into an intermediate stage for electron shuttling experiments. The sensitivity of SET for the single-shot read-out depends rather on the capacitive coupling between the SET and QD_0 which is inspected and analyzed more accurately after the formation of terminal QD, because the tuning of the shuttle QDs would eventually drift the working point of the SET due to the cross-coupling between clavier gates and the sensor dot.

DETAILED STUDIES OF RIGHT SET

The right single-electron transistor (SET) exhibited a charging energy of 3.6 meV, as determined from Coulomb diamond measurements (see Fig. 4.6 **a**). This characteristic is significantly modulated by quantized states with charging energies (< 1 meV). We attribute them to imperfections in the reservoirs (i.e. the source and the drain of the right SET). Further discussion is based on the assumption that the lattice imperfections in the Si/SiGe HS could potentially be the origin of this disordered potential. To investigate this hypothesis, we employed two complementary structural characterization techniques: the Scattering X-ray Diffraction Microscopy (SXDM) provided by Cedric from ESRF and the Electron Channeling Contrast Imaging (ECCI) operated by Chen-Hsun from IKZ.

SXDM provides nanoscale strain mapping with high sensitivity to lattice deformations. This technique reveals strain patterns consisting of for instance the misfit dislocations and gate electrodes induced strains. In particular, the nanoprobe beamline ID01/ESRF [151, 152] being used for this experiment provides about 60 nm lateral resolution [153], that has the same scale of clavier gate width W_G. It should capture in principle the local lattice deformations on the gate level by measuring the spatially dependent strain tensor. The other technique, the ECCI was then applied as a high-resolution, rapid characterization method for crystalline defects in the scanning electron microscope (SEM). This technique's sensitivity to lattice deformation enables direct visualization of misfit dislocations with sub-micron resolutions [154], despite potential contrast reduction from surface oxides. In addition, its non-destructive nature and large-area inspection capability make it particularly valuable for this study to only confirm the presence of misfit dislocations. The combined SXDM-ECCI approach offers more insights into the materials beyond the electrostatic characteristics.

Fig. 4.6 **b** presents the preliminary results of a combination of these two experiments. Here only the strain component ε_{zz} is presented as an example representing the subtracted data from the strain tensor. It corresponds to the out-of plane strain. A clear fluctuation of ε_{zz} (in the order of 3×10^{-4}) along the y-axis propagates underneath the SET area. The ECCI measurement under the diffraction condition of $[\bar{4}00]$ confirms this

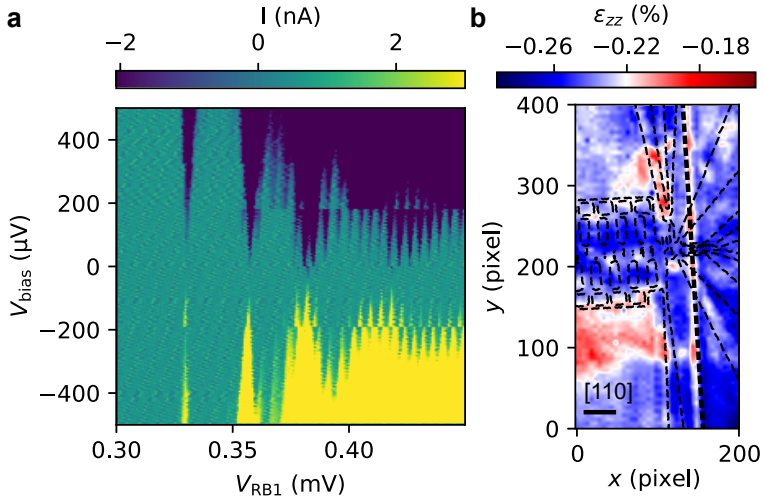

Figure 4.6: **Further studies on the right SET: a**, the Coulomb diamond measurement of right SET in gate space constructed by RB1. **b**, the Scanning X-Ray Diffraction Microscopy (SXDM) measurement data (false-colored plot) and the Electron Channeling Contrast Imaging (ECCI) measurement data (dahsed lines) in the area of right SET. Here the strain component ε_{zz} are selected from the SXDM dataset for illustration. The original ECCI data is an SEM image, and here only the contours of gate electrodes and the detected misfit-dislocation are shown and overlaid on top of the SXDM data.

deformation and identifies the misfit dislocation illustrated by the bolded dashed line in Fig. 4.6 **b**. According to the gate layouts depicted by the thin dashed lines in Fig. 4.6 **b**, this misfit dislocation propagates through both the source and drain of the right SET. This observation fits our assumption that a disordered potential originated from lattice deformations affect both reservoirs leading to the modulation of sensor dot charging energies as shown in the Coulomb diamond measurement.

These experimental results indeed evidently confirm the existence of the misfit dislocation. However, its correlation to the modulated charging energies requires more qualitative evaluations. The further study is still under investigation by the time of writing up. The focus is now on the numerically modeling of strain-induced potential in the QuBus device operated by Costanza in IHP. Further developments and studies are expected.

4.2.4. FINE TUNING QUBUS IN GATE SPACE

CHARGE CONFIGURATION AT QUBUS TERMINALS

After tuning up SETs, fine tuning the QDs in 1DEC starts with forming the terminal QD by adjusting gate voltages applied to T-gates. On the left-hand side of the 1DEC, the terminal QD is indexed as QD_0 which is alternatively tunnel- or capacitive-coupled to the sensor dot of the left SET depending on the gate voltage applied to TLB1. Such a QD serves as the entry point of the 1DEC through which an electron can be loaded into or unloaded from 1DEC. Its functionalities demand a well controlled chemical potential aligning to that of the sensor dot. Here the chemical potential of QD_0 is electrically controlled by the gate voltages applied to TLP that plunges the quantized levels in QD_0 with

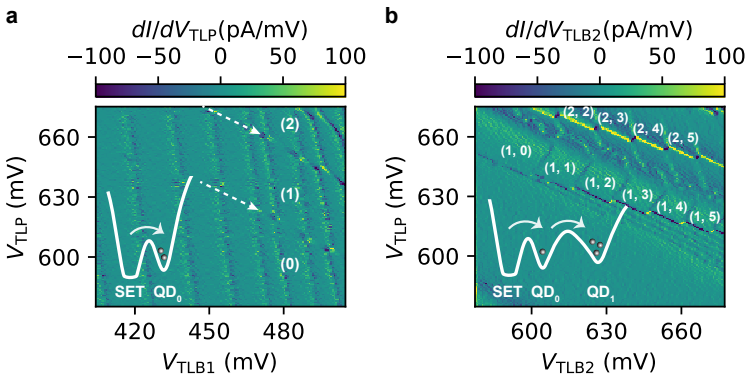

Figure 4.7: **Charge scans of terminal dots in QuBus a**, A single dot charge scan in gate space (TLB1 and TLP) for QD_0 at the left end of QuBus. Dashed arrows parallel to the charge transition lines of QD_0 indicate the corresponding gate voltage configurations in order to add one more electron from the left SET to the QD_0. The charge occupancy of the QD_0 is labelled accordingly providing the number of electrons in it. The inset on the bottom left sketches the simulated electrostatic potential φ of SET and QD_0 in which solid balls illustrate the confined electrons. **b**, A charge scan in the gate space (TLB2 and TLP) for the double dot system consisting of QD_0 and QD_1. Charge occupancies of both QDs are labeled by (n_0, n_1) where n_0 and n_1 represent the number of electrons in QD_0 and QD_1, respectively. A simulated electrostatic potential landscape of SET, QD_0 and QD_1 is shown as an inset on the bottom left where the tunnelings of electrons from SET to QD_1 via QD_0 are illustrated by arrows. Similarly, solid balls represent the electrons without specific physical meanings here.

respect to the chemical potential of sensor dot so that loading an electron from SET to QD_0 or unloading reversely can be all-electrically controlled (see the simulated electrostatic potential in the inset of Fig. 4.7 **a**).

The QuBus works in a few electrons regime, particularly it shuttles single-electron by conveyor potential all-electrically. Taking charge scans is common to map the charge configurations (i.e. the filling number of QD_0) to the applied gate voltages. Here the charge scan of QD_0 is measured in the gate space of TLP and TLB1. Gate voltages applied to TLP step from 575 mV to 675 mV with an increment of 0.67 mV during which the voltage applied to TLB1 scans from 405 mV to 505 mV with the same voltage resolution. Within this measurement window, charge transition lines of QD_0 are expected to appear on the top right of the scan. To visualize them, a differential calculation along the y-axis (i.e. V_{TLP}) is applied to the measured data therefore the color bar corresponds to dI/dV_{TLP}. As shown in Fig. 4.7 **a**, no charge transition lines are observed until V_{TLP} exceeding 600 mV, which corresponds to the gate voltage to load the first electron into QD_0. Charge transitions appear as a group of parallel lines in a charge scan, in which the addition of the second electron in the QD_0 needs a V_{TLP} higher than 630 mV. Both transition lines are indicated by the dashed arrows and the charge filling numbers of the QD_0 are labelled in gates space accordingly.

The charge transition lines in this measurement are not parallel to either axes meaning that both TLP and TLB1 are capacitively coupled to QD_0. Moreover, the lines become invisible when V_{TLB1} is lower than ~ 450 mV as TLB1 gate controls the tunnel barrier between SET and QD_0. The lower V_{TLB1} is applied, the more opaque the barrier will be. As a result, an expected group of charge transition lines with a negative slope are observed

in the charge scan that stands for a demand of higher V_{TLP} to add one electron into QD_0 with a decreasing V_{TLB1}. And eventually the TLB1 shuts down the electrons tunneling between SET and QD_0 when the V_{TLB1} is lower than 450 mV. Such a measurement evidently maps the filling number of QD_0 in gates space (TLP and TLB1) and indicates the corresponding voltage ranges of both gates allowing a QD_0 working in a few electrons regime. Notably that, the TLB1 gate locates on the second layer and seats closer to the SET than TLP, therefore oscillating Coulomb peaks of SET are visible in the background and they are almost perpendicular to the x-axis (i.e. V_{TLB1}) suggesting a stronger coupling to the gate TLB1 comparing to TLP. Further fine tuning to compensate such effects is applicable but unnecessary and it is beyond the purpose of this experiments hence not discussed here.

In addition to QD_0, launching the electron shuttling demands the properly tuned conveyor potential consisting of a series of shuttle QDs (34 QDs in a 10 μm QuBus). That means aligning the chemical potential of a series QDs deeper inside the QuBus to the QD_0 by tuning the gate voltages V_{S_i} where $i = 1,2,3,4$. All 34 QDs are electrically controlled by only four clavier gates (S1, S2, S3 and S4). Tuning up the QD_1 replicates itself and naturally forms the rest QDs in QuBus thanks to the gates periodicity. A charge scan of the double quantum (DQD) system including only QD_0 and QD_1 is thus sufficient to tune all gate voltages approaching their working point to form a smooth conveyor potential. Fig. 4.7 **b** illustrates the charge scan of such a DQD system with a single lead tunnel-coupled to the left end of QD_0. A typical honey comb pattern appear on the top right of the charge scan, providing a DQD system working at a few electrons regime. In this measurement, the voltage applied to TLP steps from 575 mV to 675 mV with a 0.67 mV resolution during which the voltage applied to TLB2 scans within the same voltage range and with the same voltage resolution as TLP. The differential calculation of the charge scan is taken along the x-axis (i.e. V_{TLB2}) yielding a plot of dI/dV_{TLB2}.

In a charge scan of a conventional DQD system those tunnel-coupled to two leads on both sides, leads transitions to two QDs appear with similar visibilities. However, the DQD system here has only one lead transition tunnel-coupled to one of the QDs (i.e. QD_0), and thus the charge transitions are not straightforward to interpret, especially the charge transitions of the last electron in the QD_0 in this experiment. At the lower end of the honey comb patterns, the dark blue lines represent the lead transition from SET to the QD_0 that is equivalent to the lower charge transition line in Fig. 4.7 **a** (i..e (0) → (1)). It means that until the V_{TLP} reaching the yellow lines on the top right corner in gate space, only has one electron being loaded into the QD_0. The increment of V_{TLB2} within this voltage range allows adding electrons into QD_1 via QD_0, thus inter-dot transitions with positive slope in the charge scan are measured instead of a negative slope as in the charge scan of the QD_0. Corresponding charge occupancies of both QD_0 and QD_1 are labelled accordingly for the ease of understanding such a scenario.

Care should be taken for the gate voltages applied to S-gates and T-gates as the QD_0 and the QD_1 have different physical dimensions. The former one is defined by three T-gates being two barriers and one plunger gate, whereas the latter one the QD_1 is defined by four clavier S-gates (S1, S2, S3 and S4). The joint point between them is the gate TLB2, which in this experiment is electrically connected to the S4 gate so that an electron can be smoothly transferred from QD_0 to QD_1 for shuttling single-electrons in conveyor-

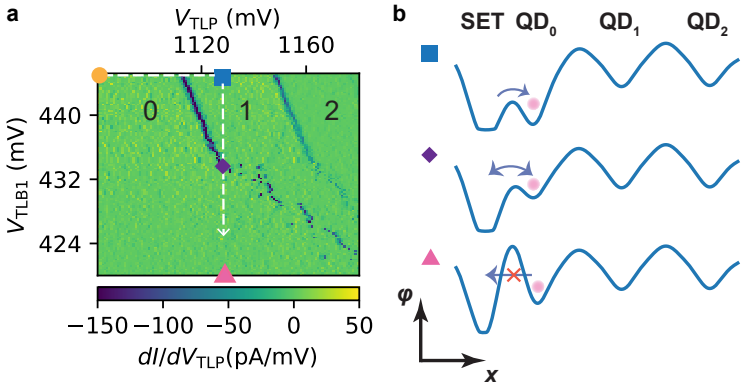

Figure 4.8: **Charge stability diagram of fine-tuned conveyor potential: a** The charge stability diagram for controlling the QD_0 filling (numbers) by individually controlled gate electrodes TLP and TLB1. Symbols indicate positions in gates space consist with (**b**). **b** The line-cut of the simulated electrostatic potential φ of the SET, QD_0 and first few shuttle QDs taken along x-direction are sketched for three positions those are marked by blue square, purple diamond and pink triangle in gates space.

mode. That means the TLP and TLB2 gates share the same phase as S3 and S4, respectively. A smooth transfer from QD_0 to QD_1 can be then interpreted as the convergence of voltage difference between TLP and S3 or similarly the convergence of gate voltages of TLB2 and S4. As listed in Tab. 4.1, the fine tuning of the conveyor potential ends up when the gate TLB2 and S4 share the same voltage (520 mV). The exceptional voltage applied to TLP gate resulting from an overcharging coincident during tuning thus experiencing additional offset (140 mV) with respect to S3.

Ultimately, a charge stability diagram of QD_0 is taken with the gate voltage configurations in Tab. 4.1. Only using the TLP and TLB1 gates sufficiently controls the filling number of QD_0 as overlaid labels in Fig. 4.8 **a**. The dashed line here indicates the possible routine to load an electron from SET to QD_0. It starts from the top left position of this charge scan which corresponds to the DC configurations listed in Tab. 4.1 and terminates at the far bottom of the charge stability diagram, which is marked by the pink triangle. At this position the barrier between SET and QD_0 is built due to a significantly low V_{TLB1} that is far beyond the measurement frame (i.e. $V_{TLB1} \leq 400$ mV). In stead of acquiring a charge scan spanning large gate space, voltages are pulsed programmatically in gates space to loading a single-electron practically.

PULSING SCHEMES IN GATE SPACE

The voltage pulses in gate space to load single-electron for shuttling are indicated in Fig. 4.8 **a** from the yellow dot to the blue square. This is followed by raising the tunnel barrier by gate TLB1 (pink triangle in Fig. 4.8 **a,b**). We label the corresponding pulse segment as P_1. Contrarily, if the voltage V_{TLP} applied to gate TLP remains low during the entire segment, no electron is loaded which we label as P_0 (see Fig. 4.9 **a** for the time sequence for both pulse segments). Reversely, we can also use the SET current I to detect either zero or one electron in QD_0 by the pulse segment D_L (Fig. 4.9 **b**). The detection pulse includes the unloading of the electron (see Fig. 4.11 in sub-section 4.3.2 for details

Table 4.1: **DC voltages configuration of all gate electrodes.** The voltages applied to gate electrodes correspond to the initial configuration (the yellow dot symbol in Fig. 4.8 **a**) in gates space for loading an electron from SET to QD_0.

SET left		SET right	
Gate	Voltage (V)	Gate	Voltage (V)
TGL	1.3	TGR	1.07
LB1	0.36	RB1	0.30
LP	0.30	RP	0
LB2	0.34	RB2	0.30
BiasL	-250 (μeV)	BiasR	0

1DEC left		1DEC middle		1DEC right	
Gate	Voltage (mV)	Gate	Voltage (mV)	Gate	Voltage (mV)
TLB1	445	S1	380	TRP	450
TLP	1080	S2	520	TRB2	450
TLB2	520	S3	940	TRB1	350
ScrTL	0	S4	520	ScrBR	0

on the charge detection).

To shuttle the single electron in a moving QD, simple sinusoidal voltage pulses $V_{S_i}(t)$ are applied to the gate sets S_i forming shuttle QDs (i.e. QD_n where $n = 1,2,3,\ldots,34$ within the 1DEC form left to right):

$$V_{S_i}(t) = A_S \cos\left(2\pi f t - \frac{\pi(i+1)}{2}\right) + B_s + \Delta B_s \frac{1+(-1)^(i-1)}{2}, \tag{4.1}$$

where the pulse amplitude A_S sets the confinement strength of the propagating sinusoidal potential created in the 1DEC. B_S and ΔB_S are constant offsets for accumulating charges in the conduction band in the 1DEC, accommodating different distances of the gate sets from the 1DEC. Both B_S and ΔB_S are independent of the shuttle process and the electron position and thus remain constant for all pulse sequences. This is significantly easing the operation of the conveyor-mode shuttle device. The shuttle velocity is given by $f\lambda = 14\,\mu\text{m}\cdot\text{s}^{-1}$, where the frequency of the shuttle pulse is $f = 50$ Hz and $\lambda = 280$ nm is the lateral period of the potential in the 1DEC. Fig. 4.1 **b** exemplifies the profile of a shuttle QD by the QD_1 in the conveyor potential.

To transport all electrons in the 1DEC by a distance of λ in the positive (negative) x-direction, the pulse segment λ_{+1} (λ_{-1}) is employed (Fig. 4.9 **c,d**). Note that all voltages applied to gates of the device return to their initial values at the end of each $\lambda_{\pm 1}$ pulse segment. This implies that the correction of the SET's operating point for capacitive cross-coupling to the clavier gate sets S_i is constant and thus simple. The right SET and the rightmost clavier gates are not used here and voltages are chosen to have an open 1DEC towards an energetically lower lying electron reservoir Thus, the pulse sequences we developed could be applied to shuttle devices with just one SET detector. Specifically, the shuttle tomography presented below could be used to identify the position of a faulty break in a shuttle device. In total only six voltage pulses V_{S_i}, V_{TLP} and V_{TLB1} given by the

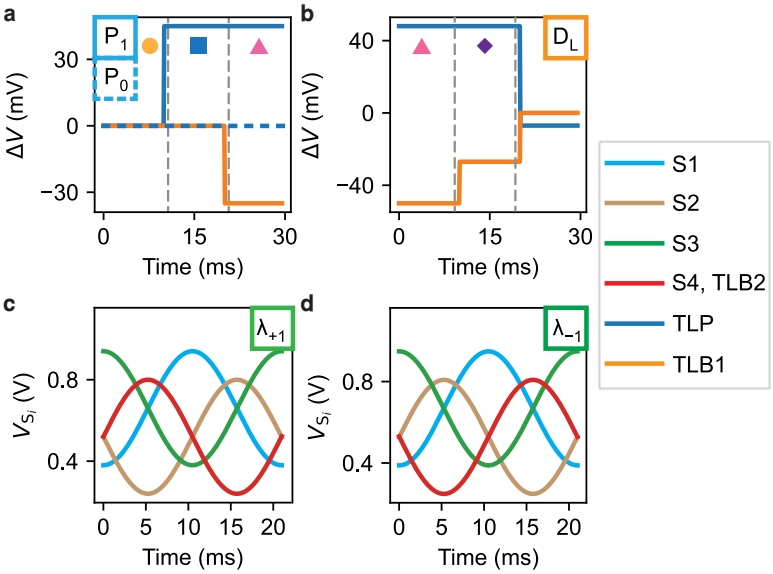

Figure 4.9: **Pulsing QuBus in gates space by elementary pulse segments: a** Voltage pulses ΔV for loading one (solid line) and zero electrons (dashed line) labelled P_1 and P_0, respectively. **b**, Voltage pulse ΔV of the segment labelled D_L for detecting an electron in QD_0 by the left SET. After detection the electron is unloaded to the SET. **c, d** Pulse segments λ_{+1} and λ_{-1} for shuttling an electron by a distance λ in positive (panel c) and negative (panel d) x-direction using all terminals S_i (see legend). All unchanged voltages during pulse segments are not plotted here and all panels share the same legend illustrated on the bottom right. ΔV are voltage pulses with respect to the zero-point marked by the yellow dot in Fig. 4.8 **a**.

elementary pulse segments P_0, P_1, λ_{+1}, λ_{-1} and D_L control the whole 10 μm long shuttle device, inside of which a total of 35 QDs (QD_i with $i = 0...34$) are formed along the 1DEC.

4.3. SINGLE-CHARGE SHUTTLE TOMOGRAPHY

In order to discuss the composition and interplay of pulse segments during the operation of the QuBus, we choose the pulse sequence called shuttle tomography as a first example. The sequence is designed to measure the local shuttle fidelity F_λ, i.e. the shuttle success rate of λ_{+1} for a specific position of the probe electron. Thus, we might identify local weak spots in the QuBus, although charge detection by the SET is limited to QD_0. The strategy is to shuttle a single electron from the left end of 1DEC further into the 1DEC by some short distance and then back to the detector. We repeat this experiment in order to record the shuttle fidelity and sequentially increase the shuttle distance until the electron is shuttled the full distance of 19 μm forth and back. The obtained data serves as a benchmark of the local shuttle fidelity in the QuBus. In this section, the pulse sequence of shuttle tomography is firstly introduced in Sec. 4.3.1 followed by details of single-shot charge-readout method (see Sec. 4.3.2) from which the local shuttle fidelity in the QuBus is determined and evaluated. Corresponding analysis are presented and discussed in Sec. 4.3.3 with carefully treated error estimation (see Sec. 4.3.4 for details).

4.3.1. PULSE SEQUENCE

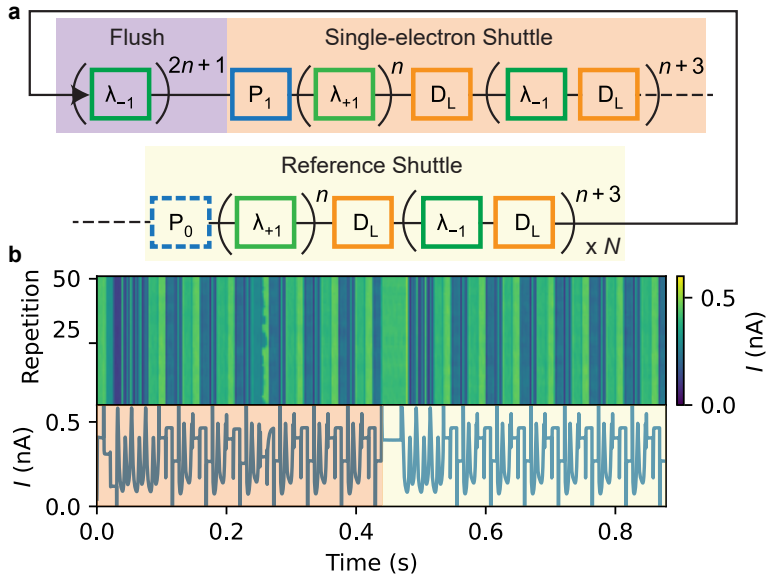

Figure 4.10: **Pulse sequence of shuttle tomography and the recorded full SET current traces.** **a**, The pulse sequence of a shuttling tomography experiment consists of a flush pulse, a single-electron shuttle sequence and a reference shuttle pulse without an electron being loaded. The pulse is repeated N-times. **b** An example of 50 randomly selected repetitions out of 10000 are shown as a false-color plot. The SET current during the single electron shuttle and the reference shuttle with $n = 3$ are shown. The statistical mean of all 10000 current traces is plotted below the false-color plot.

The corresponding pulse sequence for shuttle tomography is displayed in Fig. 4.10 **a**. First, the depleted 1DEC is flushed by applying λ_{-1} $(2n+1)$-times with $A_S = 280$ mV and $B_S = 520$ mV to ensure an empty channel. Then, it is loaded with a single electron (P_1) which is shuttled into the 1DEC for a distance of $n \cdot \lambda$ (by repeating λ_{+1} n-times). Afterwards the electron filling of the first $n+4$ QDs is measured by consecutively detecting (D_L) $(n+4)$-times (see Fig. 4.10a) and shuttling one period back towards the SET (λ_{-1}). First shuttle tests on this device revealed that measuring 4 additional QDs is sufficient to detect an erroneously shuttled electron. Finally, we apply a reference pulse by repeating the full pulse, but replace the P_1 segment by P_0. This shuttle pulse is repeated N-times.

Exemplified SET current traces are shown in Fig. 4.10 **b** corresponding to the single-electron shuttle tomography with $n = 3, N = 10000$. 50 traces out of 10000 are randomly selected and plotted in the upper panel. The lower panel depicts the statistical mean of all 10000 current traces. The single-electron shuttle sequence and the reference shuttle sequence are shaded accordingly by the same colors as in Fig. 4.10 **a**. In fact, SET current traces are recorded over the complete sequence in which the flush pulse has almost double the time span of either the single-electron shuttle or the reference shuttle but contains no meaningful information hence not plotted here.

In the beginning of the single-electron shuttle, three steps from 0.4 nA to 0.15 nA via an intermediate level ~ 0.3 nA represent the loading of an electron from SET to QD_0

by pulse segment P_1 with distinguishable current drops in the SET. At the last current stage, the TLB1 builds up a barrier. Without intentionally compensating such an effect the SET drifts to the Coulomb blockage region where low current level is measured as expected. Thereafter, three period oscillations reveal the significantly capacitive cross-coupling between SET current and clavier gates, in particular the shuttle pulse segments $\lambda_{\pm 1}$. In this example, the loaded electron is shuttled for 3λ and then a detection of QD_0 by D_L ensures whether the electron follows the conveyor potential or not. The typical signal of this pulse segment shown as three stages in the current traces as well. Almost all of those current levels have the same profile unless the one after the third λ_{-1} since the shuttled electron comes back to the QD_0 and being sensed by the SET current. Instead of starting from a high current level, the D_L after the third λ_{-1} shows a low current level (293.36 pA) at the beginning that is close to the intermediate current level within a loading pulse P_1 thus representing the presence of an electron in the QD_0. Additionally, the electron tunnels out of QD_0 afterwards leaving a current jump of SET stochastically across repetitions (see the upper panel of Fig. 4.10 **b**), and resulting in an exponentially increasing current in the statistical mean of all current traces (see the lower panel of Fig. 4.10 **b**).

For the rest of this example i.e. the reference shuttle, no current jumps due to tunneling of electrons are observed. It is essentially a measurement of the capacitive cross-coupling of SET to the pulsing sequence that can be seen as a measurement of the background noise per trace and can be subtracted from the single-electron shuttle. Eventually, it contributes to the development of the read-out method and defines the sensitivity of the SET.

4.3.2. SINGLE-SHOT CHARGE-READOUT

To deterministically identify the charge filling number of the QD_0, both current traces of the single-electron shuttle part and the reference shuttle part of the pulse sequence of shuttle tomography are used. Two representative current traces are shown in Fig. 4.11 **a** illustrating the recorded SET current trace during a pulse segment D_L when the QD_0 is either empty or occupied by one electron. Three current stages are assigned to hold, intermediate and empty suggesting the status of QD_0. Each of them lasts for 10 ms and is labeled by the same symbols in Fig. 4.8 **a**. We also refer each stage as a measurement window. The existence of an electron is evaluated from the averaged current difference between two measurement windows (hold and empty in this case) instead of the detection of an instantaneous jump of the current level due to the tunneling of electrons in the intermediate stage. If QD_0 is filled by one and zero electrons, we typically observe the orange and blue traces, respectively. Comparing two current traces, the averaged current level of each trace within the hold stage differs by 66.71 pA and a single current blip with an increment of ≈ 75 pA appears in the intermediate stage when an electron is read out.

Both observations evidently indicate the presence of an electron in the QD_0. There are two methods to detect either of them. One is the conventional single-shot read-out method that detects the single current blip in the intermediate stage, the other is evaluating and comparing the averaged current level within the hold stage that we eventually used for the data analysis. In contrast to the conventional single-shot read-out which

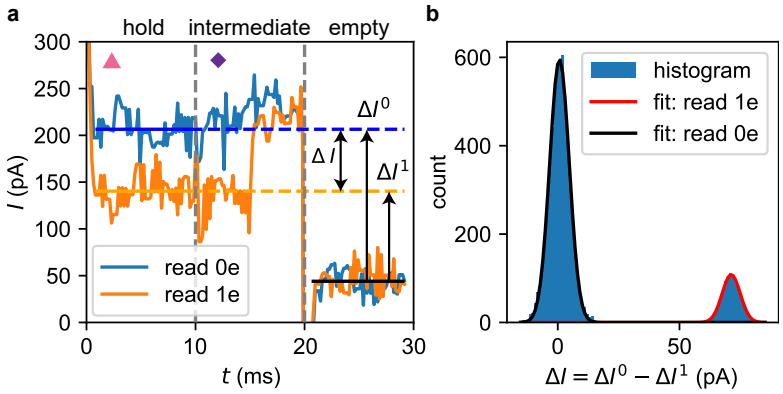

Figure 4.11: **Single-shot charge-readout. a**, Two representative SET current traces I recorded during the detection pulse segment D_L. It consists of three stages namely hold, intermediate and empty. The hold and intermediate stages are labeled by the same symbols in Fig. 4.8 **a**. The orange and blue traces correspond to the measurement of read an electron or no electron presented, respectively. The solid horizontal lines within the hold stage and the empty stage indicate the averaged current levels from which ΔI^0 (arrow) and ΔI^1 (arrow) are calculated. The dashed lines are extended only for guide-to-the-eye. **b**, Histogram of current differences ΔI (as defined in panel a). The statistics plotting here is a result of shuttling a single electron for $n\lambda$ where $n = 3$ and $N = 1000$.The x-axis is centered with respect to the averaged current level of detecting an empty QD_0 that is labeled as ΔI^0 in **a**. The two Gaussian fits are assigned to detecting an empty QD_0 (black) and filled QD_0 (red), respectively.

is sensitive to the current noise, the charge-readout method we used here immunes to the charge noise particularly for the base-band charge-readout during this experiment. By analyzing the current trace in the intermediate stage during which the tunnel barrier is opened to allow electrons tunneling out, the current noise is evaluated to be ≈ 80 pA (3σ) obscuring the current jump with ≈ 75 pA. However, the evaluated mean values of each trace in the hold stage are distinguishably separated by 66.71 pA despite of a comparable 3σ current noise (≈ 68 pA). Moreover, the slow noise such as drifts of the SET current, that may occur after a number of current traces, has impacts on the sensitivity of the charge-readout method as well. Subtracting such a variation among measurement traces can be simply done by evaluating the averaged current level of the empty stage and comparing the level difference between hold and empty stages. As a result, we evaluate the averaged current levels in the hold stage and empty stage for each current trace within a D_L pulse segment (see the solid horizontal lines within the hold stage and the empty stage in Fig. 4.11 **a**), from which ΔI^0 and ΔI^1 are evaluated and ultimately the $\Delta I = \Delta I^0 - \Delta I^1$ is calculated.

An exemplified charge-readout is demonstrated by shuttling single electrons for a distance of $3 \cdot \lambda$ and is repeated $N = 1000$ times for statistics. The corresponding results are presented in a histogram plot (see Fig. 4.11 **b**). The current level difference ΔI of all detection pulse segments D_L bin into two separated Gaussian-like distributions. The higher one centered around 0 pA corresponds to the detection of an empty QD_0 and the other one beyond 50 pA represents the detection of an occupied QD_0. Two Gaussian fits are applied to the histogram and are colored by black and red for detecting none electron and one electron, respectively.

According to the pulse sequence, D_L is applied $N \times (n+4) = 7000$ times, in which only one electron is shuttled per trace, and thus 1000 electrons being detected in total. Such counts are represented by the integral of two distributions those should show a ratio of 1 : 6 for this experiment. In particular, the statistical results here experience the same noise source in the measurement frame, a similar width of the distribution is expected. As a result, the maxima of each distribution show the ratio of 1 : 6 as can be seen in Fig. 4.11 **b** providing the integrity i.e. the charge conservation of this readout method. In addition, two distributions are separated sparsely by 70.50 pA with 3σ standard deviation of 15.7 and 17.0 pA for each ensuring the precise identification of none or one electron in the QD_0. Given the overlap between the two Gaussian fits is relevant to the detection error that is evaluated to 2.29×10^{-20}, subtracting ΔI by comparing the current level of hold and empty stages within each D_L pulse segment provides a sufficient sensitivity to distinguish the presence of a single-electron in the QD_0. Remarkably, this method does not require fine tuning for each D_L pulse segment as the operating point of the SET is chosen only once while $V_{S_i}(t = 0)$ are applied to all four clavier gates. After any λ shuttle step, the operation point of the SET is recovered due to the periodicity of the shuttle pulse. Calibrating the D_L appears to be a reliable and replicable method.

4.3.3. SHUTTLE FIDELITY

The local shuttle fidelity benchmarking of a QuBus relies on the shuttle tomography using the single-shot charge-readout method. As an instructive subset of such a measurement over $N = 40$ pulse repetitions with $n = 7$ and $A_S = 245$ mV, we observe the filling of each of the first eleven QDs as shown in Fig. 4.12 **a**. During the majority of shuttle pulses the electron remains within QD_7, into which it was shuttled. This result indicates a well operating QuBus. Sometimes the electron is detected in QD_8 and QD_9, thus the shuttle process failed during these repetitions. Via the reference pulse segment, we check whether electrons leak into the 1DEC. Since we never observe any electrons during the reference pulse across thousands of repetitions for all n, we conclude that there is no such leakage and the SET charge-detector does not faultily detect electrons in an empty QD.

The full observation of shuttle tomography with $A_S = 280$ mV, $N = 1000$ and $n = 1...36$ shows that the single electron is nearly always detected in the expected QD_n, into which it has been loaded (Fig. 4.12 **b**). In order to thoroughly discuss the charge conservation of shuttle tomography method, the electron counts of all QDs are labelled accordingly in Fig. 4.13 for all subsets of the shuttle tomography measurement. In principle, all shuttled electrons should be detected, if the 1DEC has no leak. However, it is obvious that not all $n = 1 \ldots 34$ has a total count of electron numbers summing up to $N = 1000$ despite of the maximum shuttle amplitude $A_S = 280$ mV. In fact, a few electrons are not detected. Rather than a leakage in the 1DEC, such observations are attributed to the load and measure errors. Though each subset of the measurement are repeated 1000-times in the first place. The total count of electrons is mostly lower than 1000 for three reasons. (I) In very few cases, the AWG output gave the wrong pulse output (maybe due to miscommunication with the computer). These few traces are not included in the counting. It is filtered by the averaged current I_{SET} within the reference shuttle as a failed AWG output (i.e. no pulsing at all) results in none cross-capacitive coupling to the SET. Setting a threshold

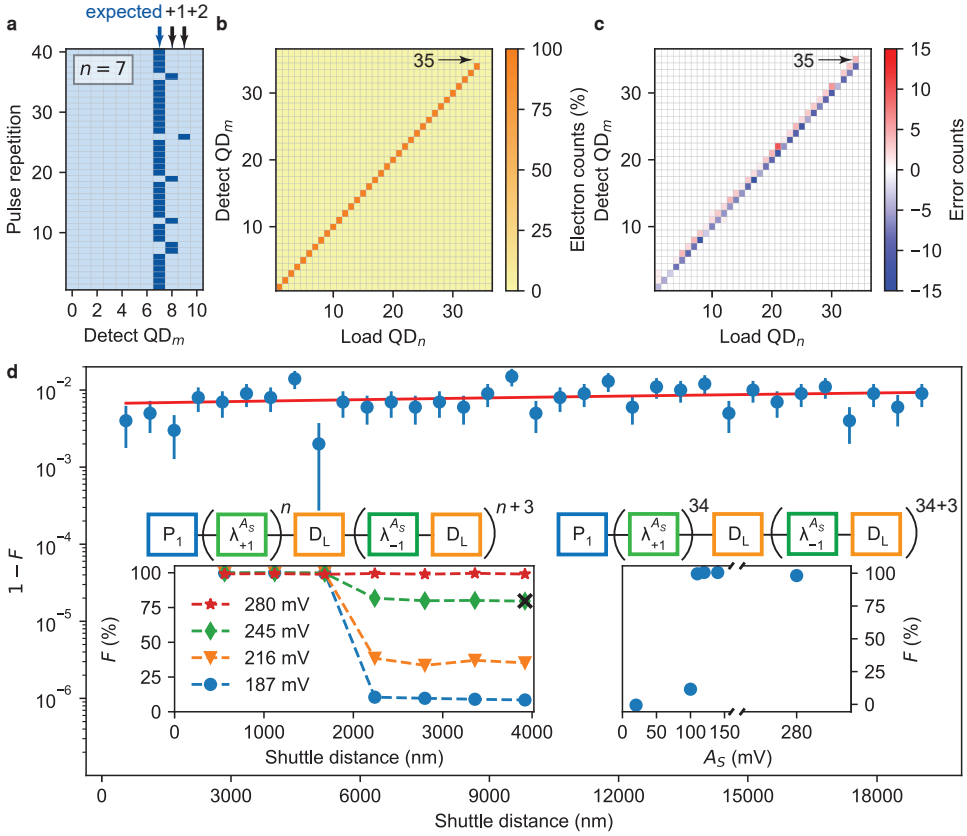

Figure 4.12: **Single-charge shuttle tomography.** **a**, Digitized electron-detection map recorded during the single-electron shuttle pulse for A_S = 245 mV and n = 7. By single-shot charge-detection (D_L) of the QD_0 to QD_{10}, we either find zero (light blue) or one (dark blue) electron for each of the 40 pulse cycles. The expected occurrence of an electron is indicated by the blue arrow and faulty locations by black arrows. The F for this specific data set is marked by a cross in the left inset of panel e. **b**, Relative error counts i.e. fraction of electrons detected in QD_m, if one electron is loaded in QD_n for A_S = 280 mV and N = 1000. For each column, we count all single-electron detection event from an electron-detection map as shown in panel b. **c**, Same as in panel c, but the error counts are plotted, i.e. the difference between expected and detected electron counts. The statistics shown in panel c and d are based on the same data set. False electron detection of QD_{35} is marked by an arrow. **d**, The shuttle infidelity $1 - F$ (blue dots with 1σ error bar) determined from the full shuttle-tomography sequence for A_S = 280 mV and N = 1000. Number of applied $\lambda_{\pm1}$-pulse segments is converted into total single-electron shuttle distance forwards and backwards. Red-line is fit to the data (see text). Left insert: Shuttle fidelity F as a function of the total shuttle distance (forth and back) for various A_S and N = 1000 (lines are guide-to-the-eyes). Right insert: Shuttle fidelity F as a function of A_S for maximum shuttle distance n = 34. Note that A_S=280 mV is only used for the fourth λ_{+1} and for the 31st λ_{-1} shuttle pulses. The modified single electron shuttle pulses are sketched above the corresponding inserts. The applied flush and reference pulses are not shown for simplicity.

of 10 pA that is one magnitude smaller than the working cases eventually filters out all these AWG failures. For the data in Fig. 4.13, one trace is omitted for $n = 1, 9, 25, 33$ and being subtracted from the total count N. It is an obvious reason to miss an electron and not related to the shuttle device. (II) Detection and loading errors occur (see detailed discussion about the error estimation in Sec. 4.3.4). (III) It is surely impossible to fully rule out that an electron gets stuck in the shuttle maybe due to a defect or tunnels out of the 1DEC. But comparing to the total repetition of 1000, it is such a rarely occurring that can be conclude as a leakage during shuttle.

Additionally, no electrons are observed for $n = 35, 36$. This is expected as the right end of the 1DEC is open and the 1DEC only contains QD_0 to QD_{34}. Hence, the electron is pushed out of the 1DEC through its right end for $n = 35, 36$ as their positions exceeding the physical dimension of the 1DEC in this QuBus device. The last sub-plot for $n = 35$ in Fig. 4.13 depicts such a scenario that a single-electron is constantly pushed out of the channel and never shuttled back to the left-end of the QuBus over all 1000 repetitions. There is no single electrons being detected in any QDs as well ensuring that the leakage to the right SET does not exist and thus not influence the benchmarking of the charge shuttle fidelities in this experiment.

Mathematically introducing the electron count C_m^l assists us to express the number of electrons detected in QD_m by summing detected electrons over all N pulse repetitions where l is the expected filling of QD $_m$, which is 1 only for $n = m$ and 0 otherwise. Thus, the error count of each QD relative to its expectation is given by $\Delta C_m^l = C_m^l - l \cdot N$. The single-electron error count (Fig. 4.12c) reveals that in very few repetitions the electron was detected in a QD_m with $m > n$ and almost never for $m < n$. In approximately 1 % of the repetitions the electrons seem to disappear ($\sum_{m,l} C_m^l < N$) that facilitates the observations of a generally lower total electron counts than expected as shown in Fig. 4.13.

Remarkably, some electrons are detected in QD_{35} when loaded in QD_{34}, although QD_{35} does not exist. Hence, delayed electrons got stuck during a λ_{-1} pulse segment, instead of hopping over one QD during a λ_{+1} pulse segment. This indicates a directionality of the shuttle error. In other words, if we shuttle an electron to QD_n and detect an electron in e.g. QD_{n+1} (Fig. 4.12c), the electron has never reached QD_{n+1}. We apparently detect it there, because a shuttle error (a delay) occurred at λ_{-1}, if shuttling back to the SET.

We define one shuttle pulse as successful, if three conditions are simultaneously fulfilled: (I) An electron is detected in the n-th QD, into which an electron has been loaded. (II) No electron is detected in all other QDs, which are detected during the sequence. (III) No electron is detected during the reference shuttle sequence in any QD. We count the number of successful shuttle pulses with the same n and divide by the total number N of pulse repetitions to get the charge shuttle-fidelity $F(n)$.

With $A_S = 280$ mV and $N = 1000$ for each of the $n = 1...34$ covering a shuttle distance of $2n \cdot 280$ nm, we observe an average shuttle infidelity of $1 - F = (0.785 \pm 0.051)$ % (Fig. 4.12d). This infidelity, however, also includes errors from loading and detection pulse segments. Remarkably, $F(n)$ is almost independent of the shuttle distance. Therefore, we split the observed infidelity into two error sources: First, the shuttle error ε_λ occurring during each $\lambda_{\pm 1}$-pulse, which is a shuttle dependent error that accumulates over the increment of shuttle periods. Second, an electron loading and detection (LD) error

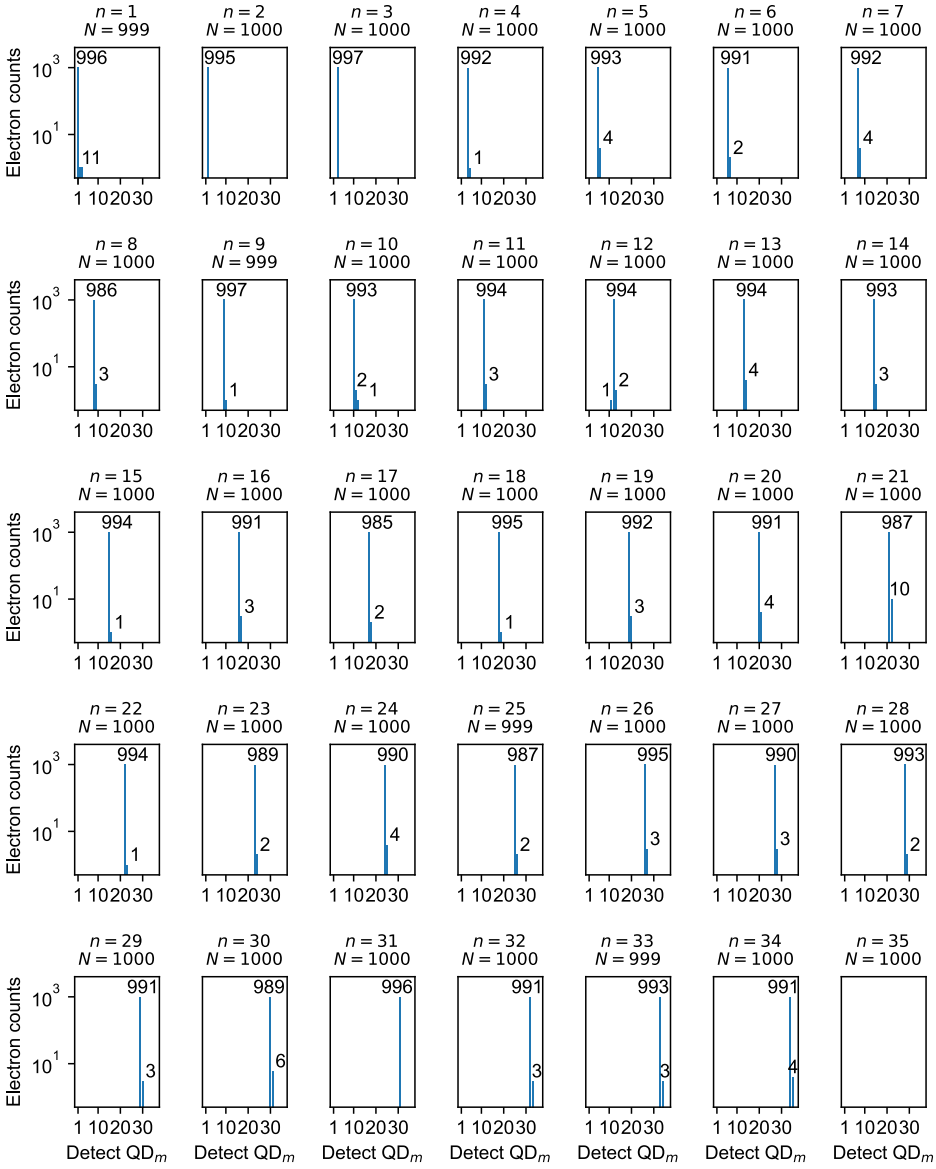

Figure 4.13: **Electron counts for single charge shuttle-tomography.** Each panel is the electron count for N shuttle-pulse repetitions for $A_S = 280\,\text{meV}$ as a function of the QD number m, in which the electrons are detected. For each panel a different n is used in the pulse sequence. Numbers label the height of bars larger than zero. For $n = 35$ the shuttle distance exceeds the physical dimension of QuBus.

ε_{LD}, which is independent of shuttling and attributed to errors occurring during the P_1 (no electron initialized by error) and D_L (no electron detected by error) pulse segments. By linearly fit $\ln(F) = A \cdot n + B$ where $A = 2\ln(F_\lambda) = 2\ln(1-\varepsilon_\lambda), B = \ln(F_{LD}) = \ln(1-\varepsilon_{LD})$, the average shuttle fidelity per period is estimated to be $F_\lambda = (99.996 \pm 0.003)\,\%$ at $A_S = 280$ mV. Further electrostatic simulations facilitate such a high fidelity given the fact that the orbital splitting between the ground and the first orbital excited state exceeds 4 meV (see Fig. 4.14). In general, stronger confinement relative to local electrostatic disorder reduced the shuttle error. Comparing to the targeted $E_{orb} \geq 1$ meV, which sufficiently competes with the spin relaxation due to disordered potential and spin-orbital coupling, that ensures a coherent shuttle fidelity of 99.9 %, the estimated averaged charge shuttle fidelity per period $F_\lambda = (99.996 \pm 0.003)\,\%$ stays inline with the theoretical study in Ref. [43].

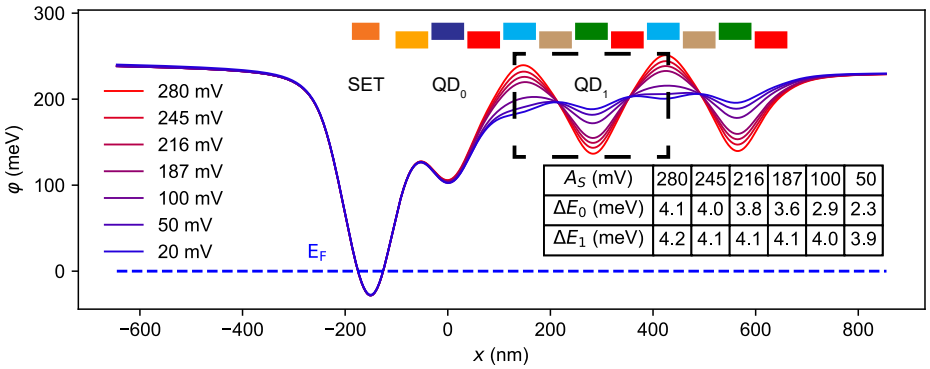

Figure 4.14: **Simulated electrostatic potential of 1DEC.** Line-cut of the finite-element numerically simulated electrostatic energy $\varphi(x)$ along the center of QuBus 1DEC for various A_S in the area of the left SET and $QD_{0...2}$. The finite-element model includes the realistic gate-electrode pattern and material layer stack, but no charge defects. Thomas-Fermi approximation is used to simulate the SET in order to take screening of electron reservoirs into account. The Schrödinger-Poisson equation is solved for QD_1 in the region marked by the black dashed rectangle. Three lowest orbitals s, p_x and p_y are used to calculate the lowest orbital splittings ΔE_0 and ΔE_1. The dashed horizontal line represents the Fermi energy E_F for electrons confined by the Si/SiGe heterostructure at operating temperature. Cross sections of SET top-gate and clavier gates are shown on top of the simulated potential using the same color scheme as in Fig. 1a in the main text.

As a result, the LD error is estimated to be $\varepsilon_{LD} = (0.7 \pm 0.1)\,\%$, thus the LD-corrected shuttle fidelity across the full channel and back is $\hat{F}(34) = (99.7 \pm 0.3)\,\%$ (total distance 19 μm, see Sec. 4.3.4 for details on the estimations of errors). Presumably, larger A_S could increase the shuttle fidelity as long as heating effects remain negligible.

Finally, we provoke shuttling errors by reducing A_S and thus the confinement of the QDs in the shuttle potential. Note that the amplitude of the flush pulse is always constant at $A_S = 280$ mV. We observe that as we decrease A_S, the shuttle fidelity drops between the third and the fourth shuttle period and then remains constant (left insert in Fig. 4.12 **d**). Thus, we attribute the decrease in F to a local weak spot in the QuBus potential, likely due to static potential disorder. To confirm this hypothesis, we modify the shuttling tomography pulse sequence by tuning A_S as a function of shuttle distance. Therefore,

temporarily enhanced confinement is realized by keeping $A_S = 280$ mV during the fourth λ_{+1} and the $(n-3)$-rd λ_{-1} pulse segment, thus at the position of the weak spot only. This demonstrates a tunable method to shuttle electrons over the QuBus with high F at much lower A_S applied during all other pulse segments $\lambda_{\pm1}$ (right inset of Fig. 4.12 **d**). The observed cut-off amplitude at 100 mV matches well with simulations of semiconductor-oxide interface charge-defect induced potential disorder in the 1DEC [43]. The origin of the weak spot in the QuBus requires further investigation. Note that for the measurement of $F(n)$, we cannot fully exclude two errors appearing during shuttling which compensate each other. However, the observation that faulty shuttling behavior occurs locally in the QuBus, makes it probable that two such spots should be separately observed by the n-dependence of the shuttling tomography.

4.3.4. ERROR ESTIMATION

Here we discuss and estimate the error probability for manipulating the charge state during each elementary pulse segment ε_i with $i = \mathrm{P_0}, \mathrm{P_1}, \lambda_{+1}, \lambda_{-1}, \mathrm{D_L}$. First, we assume for simplicity that the average error for shuttling one electron by a distance of λ is $\varepsilon_\lambda \approx \varepsilon_{\lambda_{+1}} \approx \varepsilon_{\lambda_{-1}}$ despite the experimentally observed small directionality. Since we never observe any electrons during the reference pulse across thousands of shuttle tomography repetitions for all n, we conclude that $\varepsilon_{\mathrm{P_0}} \approx 0$ and that the detector does not faultily detect electrons in an empty QD. We combine the error from loading one electron $\varepsilon_{\mathrm{P_1}}$ and missing an electron during detection $\varepsilon_{\mathrm{D_L}}$ to be the loading and detection error $\varepsilon_{\mathrm{LD}}$ with $(1-\varepsilon_{\mathrm{LD}}) = (1-\varepsilon_{\mathrm{P_1}})(1-\varepsilon_{\mathrm{D_L}})$. The experimentally observed shuttle fidelity $F(n)$ during a shuttle tomography pulse sequence of shuttle distance $2n\lambda$ is composed of several elementary pulse segments:

$$F(n) = (1-\varepsilon_{\mathrm{LD}}) \cdot (1-\varepsilon_\lambda)^{2n}. \tag{4.2}$$

By linearly fitting $\ln(F(n))$, we find $\varepsilon_{\mathrm{LD}} = (0.7 \pm 0.1)\,\%$ and the average shuttle fidelity per period $F_\lambda = 1-\varepsilon_\lambda = (99.996 \pm 0.003)\,\%$. Thus, the expected LD-corrected shuttle fidelity $\hat{F}(n) = (1-\varepsilon_\lambda)^{2n}$ for a total shuttle distance of $\approx 19\,\mu$m is $\hat{F}(34) = (1-\varepsilon_\lambda)^{68} = (99.7 \pm 0.3)\,\%$. This corresponds to the fidelity of shuttling a single electron across the full QuBus and back. Note that we distinguish ε_λ from $\varepsilon_{\mathrm{LD}}$ by increasing the number of λ pulses.

4.4. MULTI-ELECTRON SHUTTLE

For the shuttle tomography, only exactly one electron was loaded into the QuBus at a time. The QuBus can also be operated with many electrons using the aforementioned elementary pulse segments. Each electron can be placed in any of the QDs between $\mathrm{QD_1}$ and $\mathrm{QD_{34}}$ in a controlled manner. Thus, we can create a pattern of electron fillings in a 34 QD register. The pulse sequence for loading and detecting an arbitrary electron pattern in the QuBus (Fig. 4.15 **a**) is similar to the sequence employed during shuttle tomography. The repetition of λ_{+1} segments is replaced by a series of single λ_{+1} interleaved with $\mathrm{P_0}$ and $\mathrm{P_1}$ pulse segments. The latter determine the pattern filling the QDs. The key expectation is that any $\lambda_{\pm1}$ segment should move all electrons simultaneously by shifting the sinusoidal potential in the 1DEC.

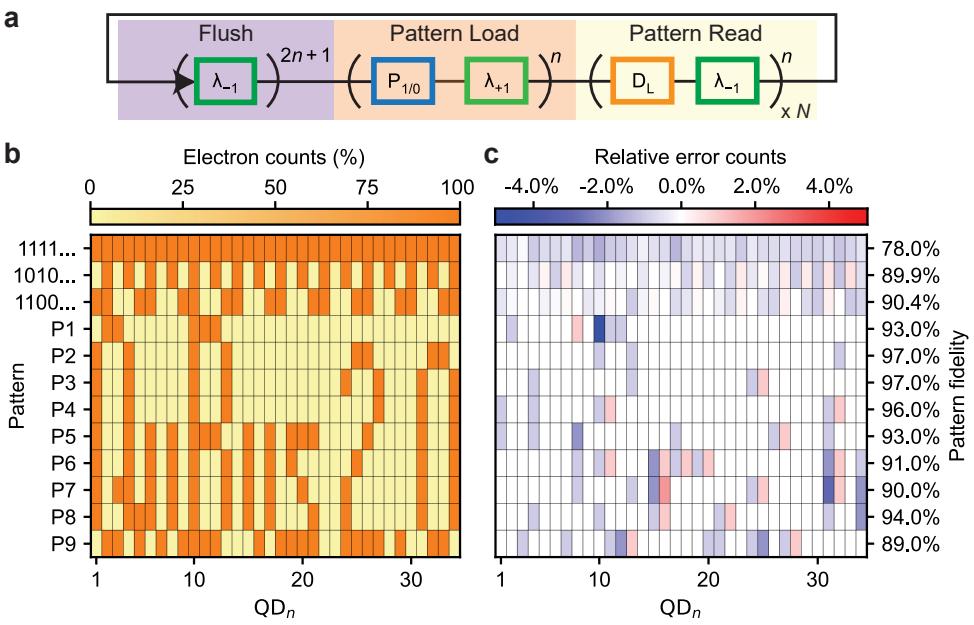

Figure 4.15: **Multi-electron operation.** **a**, Pulse sequence composed of elementary pulse elements. **b**, Detected number of electrons in QD_n normalized by the total number of pulse repetitions N for an arbitrary target filling pattern (rows with labels on the left). For P_i the target pattern is non-periodic but can be identified from the data due to the low shuttle error and is therefore not explicitly given. **c**, The relative error counts of each QD for shuttled patterns. The pattern fidelity, as defined in the text, is shown on the right for each individual row.

Using $A_S = 280$ mV, we load one electron in each of the 34 QDs (1111...), every second QD (1010...) or a more complex periodic pattern (1100...). We repeat the pattern loading and detecting for $N = 1000$ times to gather statistics on the electron count in each QD (Fig. 4.15 **b**). We observe that the fraction of counted electrons in all QDs is very close to the expected filling pattern. Next, nine non-periodic patterns P1-P9, representing the lines of a binary image comprising 34×9 bits, are successfully loaded and detected as observed from the statistics of $N = 100$ pulse repetitions.

The dominant bluish color in the error-count map for all patterns (Fig. 4.15 **c**) reveals that the main error is the apparent loss of electrons. We assign this notion to the dominance of the loading and detection error $\varepsilon_{\mathrm{LD}}$. It also explains why the pattern fidelity, which we define analogue to the shuttle-fidelity as the rate of successfully and exclusively placing and detecting electrons in all intended QDs, is lowest for the pattern with the highest electron count (111...). Blue/red dipoles in the error-count map indicate a shuttle error. As for shuttle tomography, we mainly observe individual electrons being misplaced by one QD to the right, provided this adjacent QD is nominally empty. This observation underlines the directional character of the shuttle error, which we already noted for the shuttle tomography.

4.5. DISCUSSION

Our all-electrical Si/SiGe electron-shuttle device is successfully operated in conveyor mode. Only six input terminals control the more than 100 clavier gates of the 10 µm long device. Independent of its length, only four sinusoidal signals are required to operate the shuttle as well as two signals for loading and detecting electrons by a single-electron transistor. We introduce a method called shuttle tomography, which uses a single electron to probe the local shuttle fidelity and thus local imperfections in the confinement of the moving QD. We estimate the fidelity for shuttling one electron across the full length and back, thus a total distance of 19 μm, to be $\hat{F} = (99.7 \pm 0.3)$ %. Employing other pulse sequences composed of the five elementary pulses for our QuBus, we programmatically distribute and detect up to 34 electrons across the 34 QDs formed in the shuttle device. Any QD filling pattern can be initialized and we encode a digital image, the pixels of which are represented by single electrons.

The QDs can be interpreted as a 34 bit stack with a maximum of 34 electrons or as the initialization procedure of a series of 34 QDs towards a quantum register for spin qubits. Preparing such patterns of electrons in a one-dimensional channel with low electrostatic disorder opens up possibilities to study the interplay of tunnel coupling and Coulomb interaction for a specific charge configuration. For example, as the amplitude of the periodic shuttle potential set by A_S is lowered and tunnel coupling between neighbouring QDs increased, electrons become ordered by their Coulomb interaction. The reordered position of electrons might be observed by ramping up the periodic potential and readout the filling of each QD. Furthermore, our conveyor-mode QuBus device paves the way to scalable quantum computation, since it is expected that the electron-spin evolution is deterministic during conveyor-mode shuttling at a velocity of approximately $8\,\mathrm{m\cdot s^{-1}}$ and spin-coherent shuttle fidelities of 99.9 % are predicted [43]. Besides the coherent spin-shuttling demonstrated for shorter distance [22], our current work gives perspectives for shuttle fidelity of the QuBus across $\approx 10\,\mu$m required for a sparse and scalable quantum computation architecture [17, 18]. Notably our QuBus is technologically compatible to industrial fabrication and Si/SiGe has been proven to be an ideal host-crystal for spin qubits. Spin-qubit connectivity across a distance of several micrometers could be a game changer for spin quantum computation.

DATA AVAILABILITY

The data generated in this study have been deposited in the Zenodo database (https://doi.org/10.5281/zenodo.8375442).

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has been done at HNF - Helmholtz Nano Facility, Research Center Juelich GmbH [105].

COMPETING INTERESTS

Conveyor-mode shuttling is covered by a patent family (EP 4031486, US 2022/0293846 A1, CN114424346 A) by inventors L.R.S, H.B., I.S., Künne. The patent application, co-owned by RWTH Aachen University and the Forschungszentrum Jülich, is currently pending. L.R.S. and H.B. are founders and shareholders of ARQUE Systems GmbH. The other authors declare no competing interest.

5

PERFORMANCE BENCHMARKING OF SIGE QUBUS

Ran Xue[1], Max Beer[1], Hendrik Bluhm[1,2] and Lars R. Schreiber[1,2]

1. JARA-FIT Institute for Quantum Information, Forschungszentrum Jülich GmbH and RWTH Aachen University, Aachen, Germany
2. ARQUE Systems GmbH, 52074 Aachen, Germany
3. Helmholtz Nano Facility (HNF), Forschungszentrum Jülich, Jülich, Germany

Scaling up quantum computing requires robust and efficient mechanisms for transferring quantum information over long distances. A promising approach is the high-fidelity shuttling of single electrons as carriers of spin qubits across QD arrays. Demonstrations such as dense qubit arrays with shared gate-electrodes and the quantum bus (QuBus) aim at shuttling electrons confined in gate-defined QDs with high fidelity and low control complexity, but require a highly homogeneous transport network. Potential disorders in such networks can disrupt electron transport and qubit coherence significantly. In this work, we present shuttle tomography method for reconstructing the disordered potential profile along the QuBus. It probes position- and confinement-dependent electron rearrangements in two complementary operating modes. We analyze rearranged electrons under varying confinement strengths and positions along the channel and cross-validate the physical dimensions and positions of local potential imperfections along the QuBus channel with a spatial resolution of 35 *nm. Specifically, according to the sensed potential profile, we identify localized traps and humps at specific QDs such as traps at* QD_9, QD_{17} *and* QD_{21} *with dimensions comparable with dot size* $\lambda = 280$ *nm. These results demonstrate a reliable technique for benchmarking electron transport channels and provide crucial insights for implementing scalable and reliable spin-qubit transport in a scalable quantum processor.*

AUTHOR'S CONTRIBUTION

THIS chapter is written in parallel to a journal article in preparation. The main context remains consistent with an early manuscript and it will experience major changes in the future. The concept and the main outcomes of the reported experiment should remain unchanged. In this chapter, a close look at the disordered potential in the QuBus device is thoroughly studied incorporating both electrostatic simulations and the cryogenic experiments.

It is a continuous further experiment based on the shuttle tomography experiments in Ch. 4 incorporating with additional thorough analysis. The author contribution here only evaluates the efforts on data analysis and results interpretation. The experiment was mainly conducted and operated by R.X. with help from M.B.; R.X. analyzed the data with discussions with M.B. and L.R.S.; M.B provided the software interface for the measurement software that part of the reported results rely on. The software for pulsing devices and the contributions to device fabrication are the same as previously acknowledged in Ch. 4. R.X. and L.R.S designed the measurement protocol and L.R.S supervised the experiment. L.R.S and H.B. provided guidance to all authors. R.X. and L.R.S wrote the manuscript with inputs from all other authors.

5

5.1. RESEARCH BACKGROUND

TO address the challenge of coupling the large number of physical qubits required for quantum error correction implementations, arranging and transferring qubits in arrays has emerged as a naturally scalable solution. However, this poses a general challenge for all hardware platforms. [155] While solutions such as a dense qubit array with crossbar architecture [15, 16] and a sparse qubit array [17, 156] with coherent links are particularly proposed for spin qubits based on electron or hole spins in gate-defined quantum dots, qubits in these implementations still susceptible to the decoherence channels not mutually excluding the disordered potential [68], valley splittings [26], g-factor variations [109] and nuclear hyperfine interactions [157]. In particular, unlike others decoherence mechanisms those have typically atomic scales, disordered potential exhibits a vast range of physical dimensions, spanning from the atomic level to sub-micrometer scale, and is widely exists in semiconductor based quantum devices. It dominantly affects the homogeneity of the quantum devices especially impactful for their scalability. The well-studied causes of these disorders reveal that they are generally originated from remote charged impurities at the interface between the substrate and oxides [66], unintentional dopants [68], strain induced quantum dots [69] and surface roughness [70].

Conventional methods for probing disordered potential, such as measurements of electron mobility and density derived from Hall measurements and Shubnikov-de Haas oscillations, are inherently limited in resolution. They primarily reveal substrate properties at the micro-scale and fail to capture atomistic-level disorders [109]. Similarly, cryogenic wafer probing has facilitated large-scale characterization of electrical uniformity for quantum devices, such as threshold voltages, across industrially manufactured 300 mm wafers. However, this process requires the individually addressing over 10,000 gates [34], making it resource-intensive. In contrast, our QuBus device demonstrates the

capability to sense potential disorders across a wide range of physical dimensions with remarkable simplicity. The QuBus shuttles electrons as qubit carriers using a propagating conveyor-like periodical potential, demanding only four input signals to cover the shuttle distances from the sub-micron scale to 10 μm. This fully electrical and straightforward approach enables efficient electron shuttling while simultaneously probing on-chip potential homogeneity. Experiments evidently show its viability to detect localized potential imperfections [23] and to map the valley splitting in QuBus prototypes [29] employing the method we term the shuttle tomography. Particularly, the measurement of disordered potential has been successfully demonstrated on a 10 μm long QuBus containing 34 QDs. This system also has the potential to investigate the linear Wiegner crystal.

In this chapter, we attempt to sense the disordered potential in the same 10 μm long QuBus by shuttling electrons in conveyor-mode using two complementary methods: "roll-in and out" with single electrons and "drop and catch" with a periodic configuration of multiple electrons. The former one has been previously introduced and investigated, which identifies a localized potential imperfection at 1 μm in the QuBus channel by shuttling a single electron in and out as a probe (see Ch. 4 Sec. 2.3). The latter, the drop and catch method, operates differently. A periodic charge configuration is initialized by filling every second QD in conveyor-mode. By deliberately reducing the confinement potential, electrons are subjected to electrostatic disorders that rearrange their positions. The rearranged electron configurations are then recorded, revealing displacements caused by disordered potential. Interestingly, the localized potential imperfection detected by the roll-in and out method is not observed in the drop and catch measurement. However, the indirectly sensed disordered potential deducing from the drop and catch measurements replicates the fluctuations of local shuttle fidelity observed in roll-in and out experiment. Such a correlation suggests that these two methods complement each other and sense the disordered potentials in different range of physical dimensions. Leveraging the periodicity and the simplicity of full-electrical control, the conveyor mode electron shuttling incorporating two complementary shuttle tomography methods enables scalable and parallelized probing of disordered potential over a 10 μm long QuBus.

5.2. METHODS

In the context of this chapter, the conveyor potential used in Ch. 4 Eq. 4.1is rewritten as,

$$V_{S_i}(t) = a_S \cos\left(2\pi f t - \frac{\pi(i+1)}{2}\right) + B_s + \Delta B_s \frac{1+(-1)^i}{2}, \tag{5.1}$$

where a_S represents the strength of the driving confinement during shuttle. The position of the shuttled electron is given by $x = \lambda f t$. Others remain identical to the Eq. 4.1 that f denotes the shuttle frequency and $\lambda = 280$ nm is the lateral period of the potential in the 1DEC determined by the gate width. A constant DC bias B_S accumulates electrons in the conduction band, while an offset ΔB_S is additionally applied to the gate sets $S_{1,3}$ account for their larger distances from the 1DEC compared to $S_{2,4}$. Both B_S and ΔB_S are time independent and thus remain constant during shuttling. The QD_0, which does

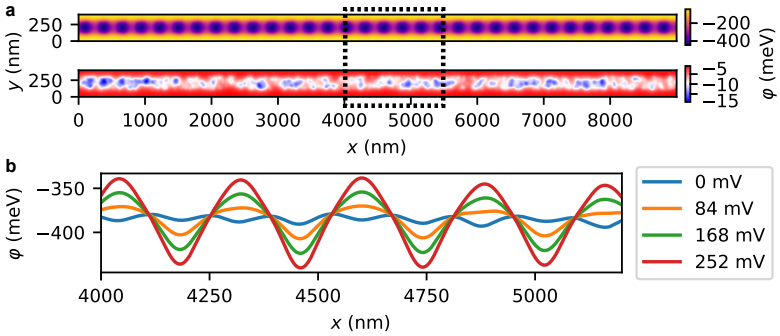

Figure 5.1: **The conveyor potential and the disordered potential: a** The simulated conveyor potential with $A_S = 280\,\text{mV}$ (upper panel) and the disordered potential due to the charged defects (lower panel). A defect density of $5 \times 10^{10}\,\text{cm}^{-2}$ is assumed and placed at the oxide-semiconductor interface. **b**. Given the presence of charged defects, the line-cut of electrostatic potential is taken through the center of QuBus spanning $1.2\,\mu\text{m}$ for chosen a_S. The disordered potential here is originated from identical defects ensembles as shown in **a** and the relative position within QuBus is illustrated by the dashed box in **a**.

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not propagate along with the conveyor potential, is individually controlled by gate electrodes TLB1, TLP and TLB2 same as in Ch. 4. This static QD interfaces the QD array with the single-electron transistor (SET) to the left. The SET, defined by gates TGL,LB1, LP and LB2, serves as both a charge sensor to detect the charge occupancy of QD_0 and a charge reservoir for loading and unloading electrons. The upper panel of Fig. 5.1(b) illustrates the simulated ideal conveyor potential φ_i generated by the experimentally applied maximum driving amplitude $a_S = A_S = 280\,\text{mV}$ [23].

5.2.1. THE REALISTIC DISORDERED POTENTIAL

As discussed in Ch. 2, the ideal electrostatic potential φ_i is always perturbed by the disordered potential φ_d that both contribute to the realistic potential φ given by $\varphi = \varphi_i + \varphi_d$. The existence of φ_d leads to a more complex electrostatic potential challenging both the charge shuttle fidelity and the spin coherence. To further exemplify this, we focus on the randomly distributed charged defects at the interface between silicon and oxides, which are the dominant origins of the φ_d [66]. The lower panel of Fig. 5.1(b) depicts a simulated ensemble of such remote defects with a surface density of $5 \times 10^{10}\,\text{cm}^{-2}$. Despite of a magnitude difference between the ideal conveyor potential φ_i and the disordered potential φ_d, the detuning between two neighboring QDs that is modulated by φ_d draws our attention due to its capability of resulting in the displacement of shuttled electrons. Maximizing the driving confinements a_S straightforwardly solves the issue, however, lower a_S is favorable for electron shuttling considering the thermal budget of the dilution unit and the unwanted cross-talk. Fig. 5.1(c) visualize this scenario across a range of a_S. Line cuts of potential φ along the x-direction for the four central QDs in the 1DEC are shown with chosen a_S. Here, φ refers to the energy of the center of bandgap in the silicon quantum well where the two-dimensional electron gas (2DEG) forms. As driving amplitudes a_S decrease, detuning effects intensify.

5.2.2. TWO METHODS FOR THE SHUTTLE TOMOGRAPHY

To experimentally access such detuning, we employ two methods: the "roll-in and out" and the "drop and catch" methods. Both methods are implemented by applying programmably assembled pulse sequences sharing the same base of pulse segments termed elementary pulse segments. The following notations are used to express these elementary pulse segments with corresponding functionalities. P_1 loads an electron from SET to QD_0, similarly, P_0 initiates an empty QD_0. D_L detects the charge occupancy of QD_0 by reading the current level of SET (I_{SET}) to its left. $\lambda_n^{a_S}$ shuttles electrons for a distance of $n\lambda$ with the driving amplitude a_S. In general, n can be an integer with positive or negative sign representing the positively (along x-direction) or reversely propagating conveyor potential, respectively. Since the conveyor potential repetitively evolves with a period of λ, we denote the shuttle pulse by $(\lambda_{\pm1}^{a_S})^n$ where n indicates the repetition counts of the elementary shuttle pulse $\lambda_{\pm1}^{a_S}$. Furthermore, a fractional shuttle pulse is possible as well, corresponding to a phase shift of the potential within one period. Therefore, $\lambda_{\pm1}^{a_S}$ can be further deduced as $(\lambda_{\pm1/j}^{a_S})^q$ where $q, j \in \mathbb{Z} : q \in [0, j]$.

5.3. EXPERIMENTAL RESULTS

The roll-in and out method probes the local shuttle fidelity along the 1DEC i.e. the success rate of shuttling an electron for any incremental λ within the 1DEC. This provides the insight into the homogeneity of the electrostatic potential. The procedure begins with loading an electron from the SET, shuttling it further into the 1DEC for a certain distance, and then shuttle it back to the SET. Ideally, the forward and backward shuttle distances are equal, and the charge number is conserved throughout the process. If the shuttled electron is not detected as expected, or a different number of electrons is measured, the discrepancy indicates a faulty break at that shuttle distance in the QuBus. For each shuttle distance x, the process is repeated N times to gather statistics. By sequentially increasing x in increments of λ, the electron is eventually shuttled across the entire QuBus channel. This incremental scanning reveals a full map of realistic potential disorders along the 1DEC.

The pulse implementation for this experiment requires only four elementary pulse segments: P_1, D_L and $\lambda_{\pm1}^{a_S}$. An example of the roll-in and out pulse sequence is shown in Fig. 5.2(a). In this sequence, an electron is loaded into the QuBus by P_1 and then shuttled forward for a distance of $n\lambda$ ($n = 1, 2, \ldots, 7$) using a chosen driving amplitude a_S by repeating the pulse segment $\lambda_{+1}^{a_S}$ n-times. It effectively rolls the electron into QD_n in the QD array. Subsequently, the readout of QD_0 using D_L is repeated $(n+4)$-times, interleaving with $\lambda_{-1}^{a_S}$ pulses to roll out electrons from the QDs one by one. During each D_L readout segment, the electron is unloaded from QD_0 to the SET, ensuring that each D_L outcome is independent. Notably, four additional D_L repetitions are necessary: the first one confirms whether the shuttled electron follows the conveyor potential, and the subsequent three extend the measurement window, enabling detection of delayed electrons in the shuttle sequence. Consequently, the occupancy of each QD_m where $m = 0, 1, \ldots, n+3$ is recorded, providing information on the displacement of the shuttled electron and the preservation of electron number. The complete pulse sequence is then repeated N-times for statistics, which is set to 1000 in this example.

Fig. 5.2(b) present the outcomes of roll-in and out method for $a_S = 280$, 245, 216, and

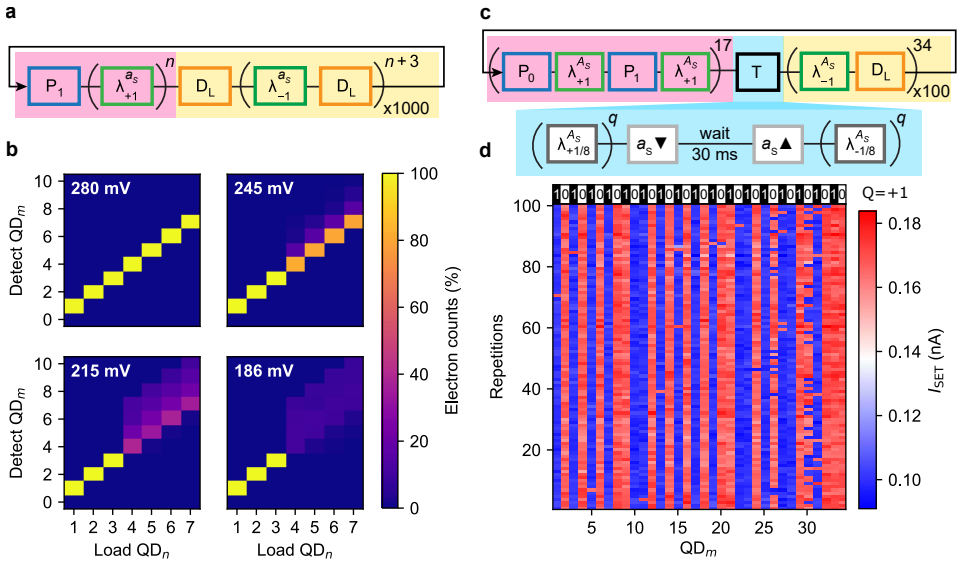

Figure 5.2: **Measurement outcomes of "roll-in and out" and "drop-and-catch"method: (a)** The pulse sequence for the roll-in and out method by assembling four elementary pulse segments: P_1, D_L and $\lambda_{\pm 1}^{a_S}$ accordingly. Pulse segments for initialization and readout are highlighted by pink and yellow, respectively. Superscripts in this representation stand for the repetition counts of pulse segments in corresponding parentheses. The entire pulse sequence is repeated for 1000-times. **(b)** The measurement outcomes of the roll-in and out method for the first seven λ with varying $a_S = 280$, 245, 216, and 187 mV (labelled for each panel accordingly). Here, the electron counts in percentage is normalized to the total repetition number $N = 1000$. **(c)** The pulse sequence for the drop and catch method. Electrons are shuttled during elementary pulse segment denoted by λ with the constant driving amplitude $A_S = 280$ mV that is the experimentally applied maximum amplitude. The sign and value in subscripts represent the shuttle direction and distance, respectively. The pulse segment T represents the drop and catch operation and is detailed in the second row. The conveyor potential stops propagating during the segments $A_S \rightarrow \alpha$ and $\alpha \rightarrow A_S$, whereas only are the driving amplitudes tuned between A_S and a chosen value α. **(d)** An example of single-shot readout with $\alpha = 28$ mV and phase shift $q = 0$. The alternating colored bar on top of the false-color plot illustrates the expected occupancy of each QD_m with corresponding charge occupancy labelled. For the false-color plot, a lower (blue) or a higher (red) I_{SET} corresponds to the detection of an occupied QD or an empty QD, respectively.

187 mV, as previously discussed in Ref. [23]. Except for the case with $a_S = A_S = 280$ mV that is the experimentally applied maximum amplitude, the results show a decrease in electron counts for $QD_{m\geq 4}$ as a_S is reduced. In contrast, the electron counts of $QD_{m<4}$ remain close to 100 %. It clearly indicates that the displacement of the electron from its expected position QD_n to others QDs ($QD_{m>n}$) becomes distinctively likely as the shuttled electron encounters with the potential imperfection at QD_4. And such displacement becomes more severe with further reductions in the driving confinement amplitude a_S, meaning that the shuttled electron cannot travel beyond this weak link without sufficient driving confinements.

This experiment detects a weak link at QD_4 using the roll-in and out method highlighting a potential weak spot in a long-range coupler for spin qubits. In fact, such a weak spot can be experimentally mitigated by temporarily applying sufficiently large confinement such as $A_S = 280$ mV to assist the electron circumventing the weak link. Further experimental results demonstrated that by applying the maximum confinement A_S only when the electron passing by QD_4, the driving amplitudes can be reduced to 100 mV elsewhere meanwhile maintaining a high shuttle fidelity [23]. It in turn concludes that the detected weak link corresponds to a local effect with a limited footprint not larger than the dimension of QD_4.

Although the "roll-in and out" method shows its simplicity and capability to sense a weak link i.e. the localized disordered imperfection in the 1DEC, the "drop and catch" method offers an even simpler and more parallelized alternative. Instead of probing the 1DEC incrementally with a single electron by varying the shuttle distance, the "drop and catch" method simultaneously senses potential disorders of all QDs in the QuBus by filling the QD array with a series of electrons. Initially, every second QD within the array is populated with an electron, creating a half-filled configuration. The driving confinement a_S is then adiabatically reduced, allowing the electrons to rearrange due to the influence of disordered potential. After a sufficiently long waiting time, the rearranged electrons are recaptured by the conveyor potential and shuttled out with the experimentally maximum driving confinement. As with the "roll-in and out" method, each QD is emptied after the readout and the displacements of all electrons are recorded. As a result, the directions of electron displacement eventually imply the gradient of disordered potential in the 1DEC.

The elementary pulses segments are now assembled in consequence as follows (see the pulse sequence in Fig. 5.2(c)). First, the QuBus is initialized in a half-filled state, denoted by Q, where every other QD is populated with an electron. This initialization is practically achieved by alternately loading electrons into every other QD ($P_{0/1}$), interleaved with a shuttle pulse λ_{+1} using the maximum $A_S = 280$ mV, until every second QD is populated after 17 cycles. Depending on the order of the $P_{0/1}$ in the pulse sequence, either the odd-indexed QDs are filled with electrons or the even-indexed QDs are occupied. We label these two configurations as the half-filled state $Q = +1$ for filling odd-indexed QDs and $Q = -1$ for filling even-indexed QDs. Next, a phase shift pulse T is applied, which contains three steps: (i) the initialized QD-array is shifted by a fraction of λ with the maximum amplitude (A_S). This is implemented by repeating the fractional shuttle pulse $\lambda^{A_S}_{+1/8}$ for q-times, where $q = 0,\ldots,8$. The phase shift is then followed by a reduction of A_S to a chosen value α exposing electrons to the potential disorders; (ii)

a 30 ms waiting time allows the electrons to rearrange according to the local disordered potential; (iii) the electrons are recaptured by ramping α back to its maximum value A_S, and the shift in step (i) is reversed to maintain symmetry in the electrostatic potential for readout. The occupancy of each QD is measured repeatedly as in the "roll-in and out" method, but due to the longer pulse sequence resulting in gigantic datasets, it is repeated only 100 times to balance ease of analysis with statistical requirements.

When multiple electrons are involved in the "drop and catch" method, the electron counting becomes more complex to distinguish errors in each QD. The electron count in percentage as in the "roll-in and out" method is no longer sufficient for this case. Instead, we use the term C_m^l to denote the number of electrons detected in QD_m over all N repetitions, where l is the expected filling of QD_m according to the initialized charge configuration hence m dependent. The error count, $\Delta C_m^l = C_m^l - N \cdot l_m$, measures deviations from the expected electron occupancy for each QD, from which one could subtract the local impacts of disordered potential on shuttled electrons. For instance, in a single-shot readout with a half-filled QuBus ($Q = +1$), electrons in QD_9 and QD_{21} preferably tunnel into neighboring QDs (i.e. QD_{10} and QD_{22}) over 100 repetitions (see Fig. 5.2(d)). This behavior suggests a local tunneling event that is influenced by the disordered potential, rather than stochastic tunneling due to random electric noise. Notably, this example is taken with $\alpha = 28\,\mathrm{mV}$ (a weak confinement) and $q = 0$, meaning no phase shift pulse applied for the ease of understanding for now.

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5.3.1. SENSITIVITY TOWARDS DIFFERENT SCALE OF DISORDERS

We completed the drop and catch method by systematically varying the confinement α and the phase shift $(\lambda_{1/8})^q$. The rearrangement of electrons is provoked by lowering α down to a regime comparable to the disordered potential. Fig. 5.3 illustrates the error counts ΔC_m^l as a function of α and the phase shift quanta q along the QuBus channel. Since q is not literally express in the plot, we modify the notation of error counts as $\Delta C_{m,q}^l$ to remark its dependencies. In the plot, vertical dashed lines highlight the range of each QD and aligning the indices of QDs to the physical dimension along x-direction.

First, the tunnel direction of electrons at each QD_m is determined by comparing the measured electron rearrangement patterns with the initial filling configuration. Electron loss and gain are color-coded as blue and red, respectively (inset sketch of Fig. 5.3(a)). This differentiation reflects the local monotonicity of the disordered potential in the vicinity of each QD. For instance, along the last row of Fig. 5.3(a) (i.e. $\alpha = 0\,\mathrm{mV}$), alternating blue and red bins reveal fluctuations in the disordered potential. At QD_4, for example, a trap in the potential leads to electron gain by attracting electrons from neighboring QDs. Conversely, a local potential hump between QD_8 and QD_9 results in electron loss, given the fact that the electrons are subsequently captured by the conveyor potential to the right of their original positions.

Besides the tunnel direction, the bins with the same color cluster together with variations in width and height. The width of a cluster maps the spatial extent of a disordered potential with a uniform slope. For instance, the wider red bins at $\mathrm{QD}_{21,25,28}$ correspond to larger traps, where electrons preferably tunnel into. In contrast, narrower clusters at $\mathrm{QD}_{4,17}$ indicate smaller traps. The height of clusters i.e. the non-zero $\Delta C_{m,q}^l$, is not continuous along the confinement axis, but terminates at specific values instead, termed

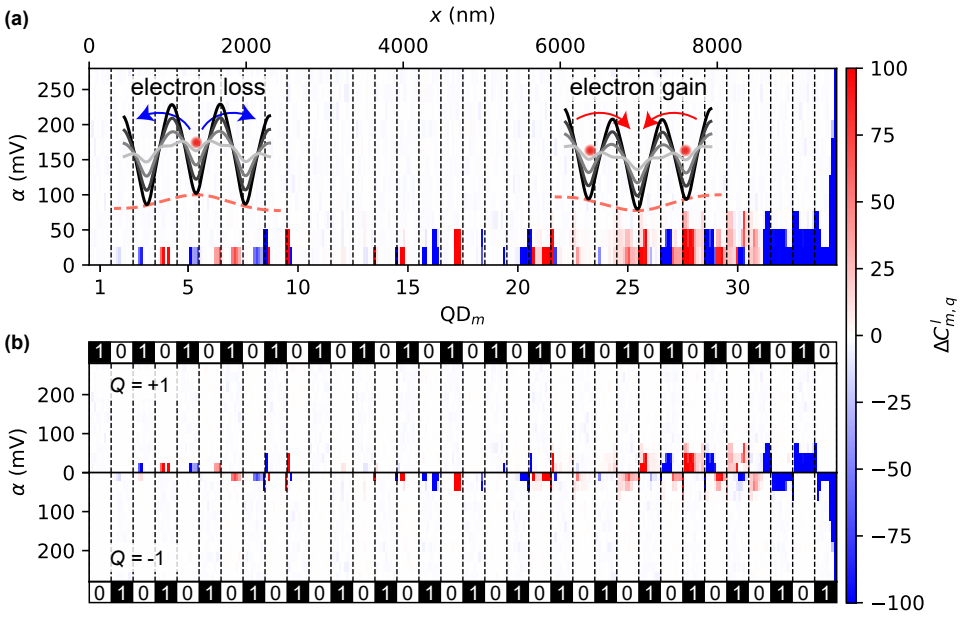

Figure 5.3: **A full map of half-filled QuBus: (a)** Measured error counts of the half-filled QuBus configuration. The vertical dashed lines separate individual QDs. Each QD is further sampled by the repetition count q of the phase shift pulse, and thus the width of each bin along the x-axis maps $\lambda/8 = 35\,\text{nm}$ in real space. The sign of $\Delta C^l_{m,q}$ depicts the loss (negative) and gain (positive) of an electron at QD$_m$ shifted by $q\lambda/8\,\text{nm}$ those are color-coded in blue and red, respectively. Note that sketches here are not to the scale of axes. **(b)** Sorting the error counts by the filling configuration Q yields the error map of the entire QuBus constructed by two complementary configurations: $Q = +1$ (up) and $Q = -1$ (down).

the critical confinement. This value represents the minimum confinement needed at this position to avoid the loss or gain of electrons, effectively preserving the initialized charge configurations. Furthermore, the intensity of the bin colors provides an indicator of tunneling likelihood, revealing the strength of the local disordered potential. Regions with more intense colors reflect stronger local potential gradients that increase the probability of electron tunneling.

In addition, the height of clustered error counts i.e. the non-zero $\Delta C^l_{m,q}$, is not continuous along the confinement axis α, but terminates at specific values, termed the critical confinement. That means the QD starts to loss or to gain an electron at the critical confinement. For confinements lower than this value, the sign of $\Delta C^l_{m,q}$ remains the same. Considering the statistics over N repetitions, this behavior represents a stable disordered potential distribution along the QuBus.

One may argue that some zero error counts could be results of combined electron loss and gain. However, it is unlikely to encounter with an interference between the electron loss and gain as each phase shift q corresponds to an independent measurement. For the sanity check, we decompose the $\Delta C^l_{m,q}$ into complementary contributions according to the two half-filled states Q of the QuBus (see Fig. 5.3b). A notable example is the QD_{27}, where both electron loss and gain are observed at different phase shifts q. With a resolution of $\lambda/8 = 35\,\text{nm}$, electrons shuttled upon the left side of QD_{27} tend to tunnel into $QD_{26,28}$, indicating a positive slope in the disordered potential along the x-direction. In contrast, electrons shuttled to the right side of QD_{27} remain within QD_{27} and if an empty QD_{27} is initialized (i.e. $Q = -1$), it gains electrons from $QD_{26,28}$ at these positions. A similar behavior is observed at QD_{29} suggesting that the variation in the disordered potential in this area occurs over a spatial scale shorter than the dot size λ. Consequently, the drop and catch method is capable to sense the disordered potentials extending different physical dimensions.

Finally, the behavior at the right end of the QuBus requires separate consideration. Significant electron loss occurs at the open end of the 1DEC, as the tunnel barrier between the QuBus and right SET is not tuned to compensate for the potential slope and the varying confinements a_S. Therefore, the $QD_{31,\ldots,34}$ for $Q = \pm 1$ both experience severe detuning at lower a_S in the existence of the SET. When $a_S > 50\,\text{mV}$ and an electron is loaded into the right-most QD_{34}, the electron is gradually pushed out of the channel by $(\lambda_{+1/8})^q$ as q increases, leading to eventual loss (see the right-most segment in the case of $Q = -1$ in Fig. 5.3 **b**). In the case of the filling configuration $Q = +1$, the QD_{34} remains empty in any combinations of (q, α) as being initialized. That implies that this QD does not gain electrons from the right SET. It implies that the electrostatic potential of the last QD remains higher than that of the SET. This feature preserves the total number of shuttled electrons, which is crucial for estimating the disordered potential fluctuations across the device.

5.3.2. CORRELATION BETWEEN TWO SHUTTLE METHODS

Are the measured error counts only influenced by the disordered potential? Does the conveyor potential plays a role in this experiment inducing deterministic errors? Considering the periodic gate layout of the QuBus, the confinements of QDs in the conveyor potential vary periodically termed the breathing effect. It could be another impactful

factor of the measured $\Delta C^l_m(q,\alpha)$.

Firstly, we show the evolution of QDs in the $q-\alpha$ parameter space to examine the breathing effect of QDs in conveyor potential. We simulated the orbital splitting (E_{orb}) of a QD at the center of the QuBus in the absence of potential disorders to quantify the breathing effect. The time-independent Schrödinger equation was solved in one-dimension (along the x-direction). As shown in the upper panel of Fig. 5.4(a), E_{orb} evolves periodically within one-λ which appears to be a direct consequence of the conveyor potential's periodicity. This breathing effect of a QD, represents a periodic modulation of the confinement strength via the fluctuating capacitive coupling as previously investigated in Ref. [43]. Importantly in this simulation, the E_{orb} drops significantly down to 0 at certain values of (q,α). However, these extreme cases here are mainly results of insufficient confinement due to significantly low α those we make use of providing a baseline for understanding the sensitivity of the measured $\Delta C^l_{m,q}$ to local potential disorders. Conversely, these extreme cases vanish in the presence of disorders (see the lower panel of Fig. 5.4(a)). On the other hand, when the realistic potential is mainly affected by the disordered potential, the breathing effect vanish and should not shade the analysis of measured results.

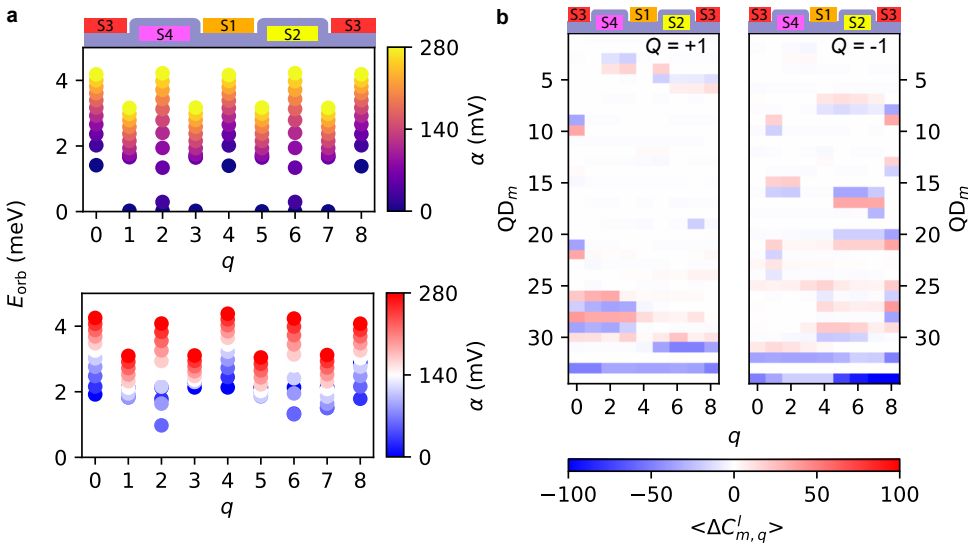

Figure 5.4: **Errors in sectors: (a)** Breathing effect of a QD within one-λ presented by its orbital splitting (E_{orb}) without and with disordered potential φ_d for the upper and lower panels, respectively. Each circle represents the simulated orbital splitting at a given phase q and is colored for different α according to the colorbar. Each column is aligned to the center of corresponding gate-electrodes or the oxides in between, respectively. **(b)** Binning the error counts $\Delta C^l_m(q,\alpha)$ for each QD_m according to the phase shift q by weighted averaging error counts $\Delta C^l_m(q,\alpha)$ along α. Two complementary filling configurations are inspected separately.

To analyze the measured $\Delta C^l_{m,q}$, we categorize the error counts by the half-filled states Q of the QuBus as labeled in the left and right panel in Fig. 5.4(b) accordingly. Here, we introduce the weighted averaged error counts $\langle \Delta C^l_{m,q} \rangle$ to reduce the dimen-

sionality of the parameter space, which reads,

$$\langle \Delta C^{l}_{m,q} \rangle = \frac{\sum_{\alpha=0}^{A_S} (A_S - \alpha) \cdot \Delta C^{l}_{m}(q,\alpha)}{\sum_{\alpha=0}^{A_S} (A_S - \alpha)} \tag{5.2}$$

where the weighing factor $(A_S - \alpha)$ ensures that errors occurring at the maximum confinement A_S get the least weight, while errors at lower α (where the potential disorders dominate) are naturally amplified. This approach simplifies the analysis by allowing us to focus solely on the q-axis.

Interestingly, $\langle \Delta C^{l}_{m,q} \rangle$ does not exhibit any obvious periodic subsequence as a function of q (see Fig. 5.4(b)). If the breathing effect of the conveyor potential dominated electron tunneling, one would expect error suppression at periodic values of $q = 0, 4, 8$. In fact, abrupt error counts appear at $q = 0$ and $q = 8$ for both $Q = \pm 1$ driven by the local disordered potential under QD_9 and QD_{21} as discussed in Sec. 5.3.1. These results suggest that $\langle \Delta C^{l}_{m,q} \rangle$ offers an insight of disordered potential features with negligible intrinsic effects due to the conveyor periodicity.

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5.3.3. VALIDATION OF DISORDERED POTENTIALS

We further compare the sensed fluctuation of $\langle \Delta C^{l}_{m,q} \rangle$ with the result of the roll-in and out method and the SXDM measurements to confirm the sensed disordered potential. Our assumption is that the potential profile of the QuBus along the shuttle direction is indirectly sensed by summing the cumulative $\langle \Delta C^{l}_{m,q} \rangle$ from the left to right along the QuBus channel. The resulting assumed potential profile is shown as the orange ribbon in Fig. 5.5. To correct for systematic errors arising from detection and loading inaccuracies, we subtract the accumulated load and detection error $\varepsilon_{\mathrm{LD}}$ that has been previously determined using the Eq. 4.2. This correction allows us to isolate the contribution of local disordered potentials. Such as the potential traps in QD_9, QD_{17}, and QD_{21}. Additionally, transitions between positive and negative slopes of the potential profile occur at QD_{27} and QD_{29}.

Validation of these findings exploits the roll-in and out results with the maximum confinement A_S as illustrated by the blue dots in Fig. 5.5(b). The single charge shuttle infidelity $1 - F$ was measured and reported in the Ref. [23] providing a globally high success rate of shuttle a single-electron over the full QuBus channel in a round trip spanning over $19\,\mu$m ($F = 99.7 \pm 0.3\%$). While conveyor-mode shuttling with the maximum A_S is generally immune to disordered potential, minor fluctuations in $1 - F$ are still perturbed by the local potential imperfections. A linear fit to the measured $1 - F$ indicates the averaged error rates that is nominally independent of the shuttle distance, meaning that the cumulative errors are eliminated in this measurement, and thus no needs to correct the cumulative error as for the drop and catch method. To better visualize the fluctuations caused by disordered potentials, we also plot the residues of the linear fit in Fig. 5.5(c).

Comparing the sensed potential profile from both methods, fluctuations of potential are observed at similar positions in the QuBus channel. We highlight the these potential fluctuations by shaded purple blocks in Fig. 5.5. For example, at QD_9, a narrow clustered bins is detected in the drop and catch measurement and we also noticed a hump in potential between QD_8 and QD_9. This observation agrees with a drop of the $1 - F$

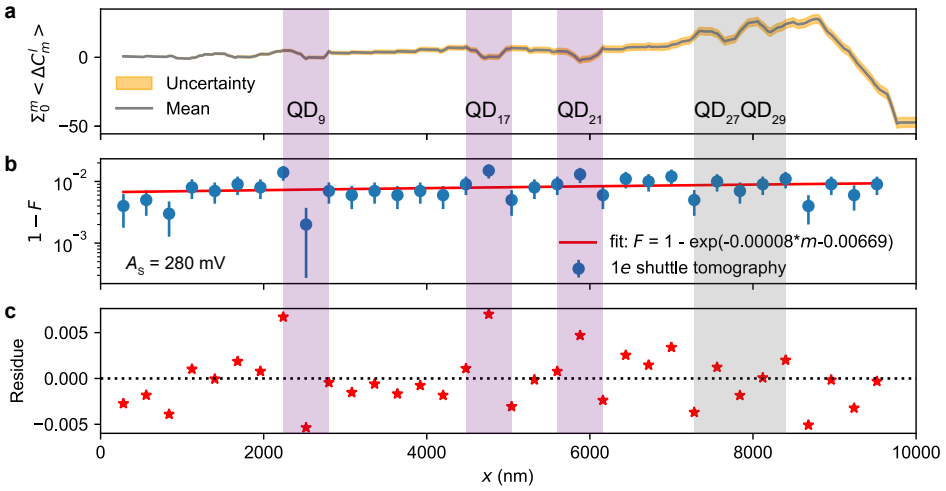

Figure 5.5: **Correlation between the electron rearrangements and single-electron shuttle fidelities:** **a** The estimated potential landscape along the QuBus channel interpreted by the $\sum_0^m \langle \Delta C_{m,q}^l \rangle$ for the half-filled QuBus charge configuration. The rigid band in orange represents the uncertainty of estimations with the expected value depicted by the solid line. **b** The infidelity of roll-in and out method. A linear fit in the logarithmic scale here subtracts a shuttle distance dependent error $\varepsilon_\lambda = (0.004 \pm 0.003)\%$ and an independent error $\varepsilon_{\mathrm{LD}} = (0.7 \pm 0.1)\%$, which is used to correct the systematic error in **a**. **c** The residue of the linear fit in **b**.

at QD_9 as well as an abrupt jump of the residue. We interpret such an behavior as the shallow trap cannot trap the shuttled electron with high probabilities, despite of a physical dimension comparable to one-λ, and thus resulting in a higher F in single-electron shuttle tomography (i.e. the roll-in and out method). In contrast, at QD_{17} and QD_{21}, the potential profile suggest deeper traps with physical dimensions comparable to twice the QD size ($2 \times \lambda = 560$ nm) causing higher infidelity $1 - F$ along with abrupt changes in the linear fit residues.

In addition to localized traps with varying depth and dimensions, regions containing combined humps and traps such as QD_{27} and QD_{29} are identified. These features are uniquely sensed by the drop-and-catch method, as the roll-in and out method is insensitive to compensated tunneling events caused by nearby potential humps and traps. Consequently, fluctuations in $1 - F$ of the roll-in and out method are not observed at QD_{27} and QD_{29}, even though the drop-and-catch measurements clearly identify variations in the potential profile. These observations underscore the complementary nature of the two shuttle tomography methods, with drop-and-catch providing finer sensitivity to complex disordered potential.

It is observable that the residues within the dot regions of QD_9 shows a different sign comparing to QD_{17} and QD_{21}. It indicates that the correlation between the electron error counts and the sensed potential disorder is vaguely defined. We intended to further investigate the origin of fluctuations in the electron error counts, and thus the SXDM measurements are analyzed in details here. All strain tensor components can be found in the Appendix A.4. In this section, I will show preliminary results of correlation be-

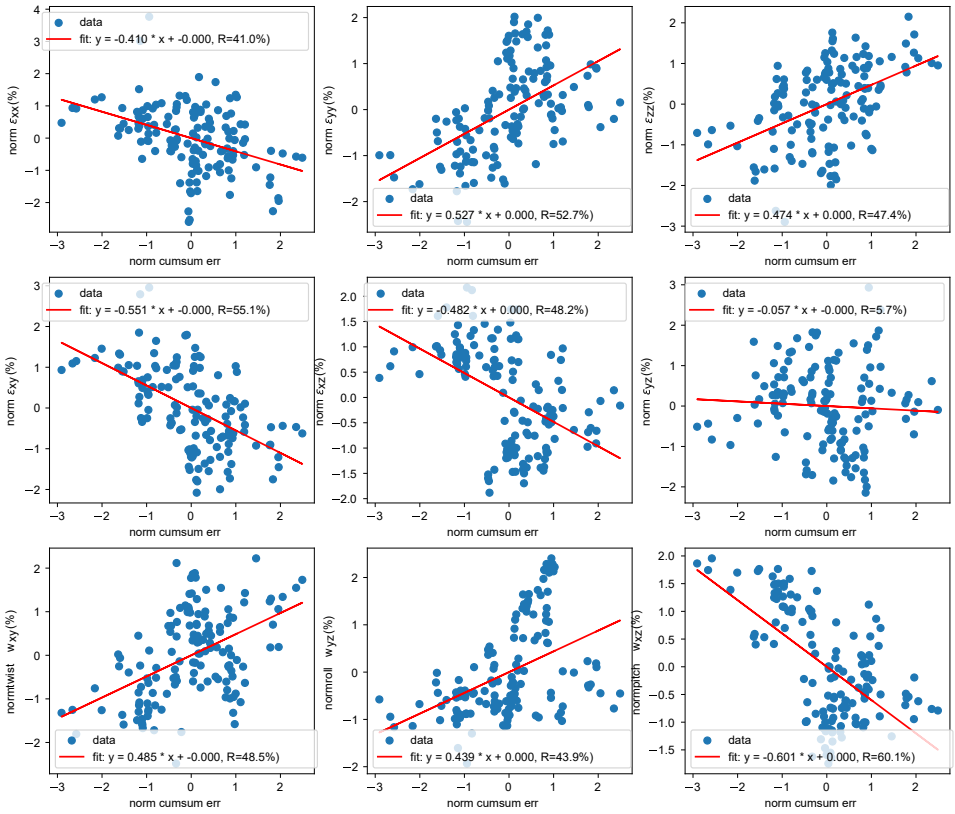

Figure 5.6: **Correlation between the electron rearrangements and each strain tensor components:** The normalized $\sum_0^m \langle \Delta C_{m,q}^l \rangle$ for the half-filled QuBus charge configuration correlates to each components of the strain tensor components subtracted from the SXDM measurement results.

tween the electron error counts based on the drop and catch shuttle experiments and the strain maps measured by SXDM.

The analysis consists of two parts. First of all, the correlations between the electron error counts ($\sum_0^m \langle \Delta C_{m,q}^l \rangle$) and each strain tensor components (within the channel region) are analyzed by linear fit as shown in the Fig. 5.6. Here only the strain map in the QuBus channel is trimmed and averaged along the axis perpendicular to the shuttle direction. Note that to correlate two parameters with different units, both datasets are normalized with respect to their own mean and the standard deviations such that both datasets are centered at their mean value and normalized to its own distribution. In addition to that, the linear regression method is also applied to fit the normalized electron error counts by considering linear combinations of all components of the strain tensor.

Table 5.1: **Linear fit residues for each components of the strain tensor**

Param.	ε_{xx}	ε_{yy}	ε_{zz}	ε_{xy}	ε_{xz}	ε_{yz}	w_{xy}	w_{yz}	w_{xz}
R	0.410	0.527	0.474	-0.551	-0.482	0.057	0.485	0.439	-0.601

The residues of each linear fit and corresponding coefficients are summarized in Tab. 5.1 for better interpretation. The components ε_{xx}, ε_{yy} and ε_{zz} have similar correlation to the sensed potential disorders. In principle, the strain-induced modulation of the conduction band edge should be primarily governed by them (i.e. the in-plane strain components ε_{xx}, ε_{yy} and the out-of-plane component ε_{zz}) [153]. However, the linear fit in this study dose not show their significant correlations to the strain-induced potential disorder with respect to other off-diagonal elements such as ε_{xy} and ε_{xz}. But the analysis shows that these two off-diagnal components have inversed (i.e. a negative sign in the fit) correlation to the fit potential. In particular, clavier gates are visible in the ε_{xy} component, which might be indicative to the localized fluctuations in the disordered potential. Moreover, the ε_{yz} does not show observable correlation to the potential given the fact that $R = 0.057$ closing to zero.

In addition to the strain components, the deduced terms w_{xy}, w_{yz} and w_{xz} representing the local lattice rotation [158] are also analyzed here. From the component w_{yz} and w_{xz}, the curvature of lattice are observed suggesting a bending in the lattice (along the z-axis) at the middle of the QuBus channel. This bending lattice is not obvious in the sensed disordered potential by drop and catch shuttling, however, the strongest correlation between w_{xz} and the normalized electron error counts ($R = -0.601$) confirms its existence and its impact on the localized shuttle errors. Interestingly, it has also an inverse correlation to the error counts.

Apart from the analysis of the correlation between electron error counts and each strain tensor components, we also conduct a linear regression analysis to understand the contribution of each strain component to the shuttle error and potentially the disordered potential. Fig. 5.7 **a** presents the normalized cumulative summation of the electron error counts ($\sum_0^m \langle \Delta C_{m,q}^l \rangle$) and the corresponding fit by the linear regression using all strain components as well as rotational elements. Here the bend in the middle of QuBus is clearly visible as sensed by the w_{xz} element. Moreover, the traps at QD_{17} and QD_{21} are also successfully fitted corresponding to the traps closing to $d = 4500$ nm and

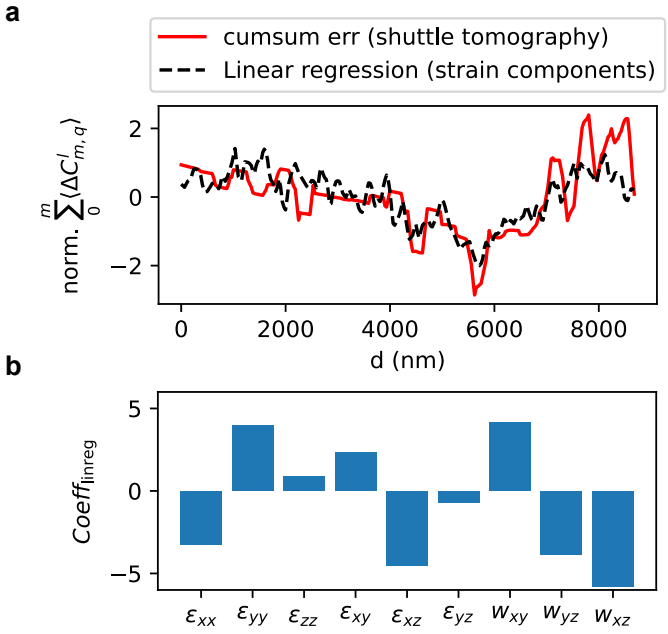

Figure 5.7: **Linear regression of the electron rearrangements based on all strain tensor components: a** using linear regression to fit the normalized $\sum_0^m \langle \Delta C^l_{m,q} \rangle$. All components of the strain tensor components subtracted from the SXDM measurement results are used here including three rotational elements w_{xy}, w_{yz} and w_{xz}. **b** The pre-factor of each component in the strain tensor subtracted from the linear regression result.

$d = 5500\,\text{nm}$ respectively. The trap at QD_9 is not successfully fitted by the linear regression at the expected position. However, a trap to the left of it ($d = 2000\,\text{nm}$) closing to QD_8 is evaluated by the linear model, which in fact fits the observation of single-electron shuttle tomography shown in the Fig. 5.5 **c** where the abrupt jump of the residue appears one λ earlier than QD_9.

The observed correlations among three measurements (roll-in and out, drop and catch shuttling and SXDM) at specific positions along the QuBus channel indicatively point out the localized potential disorders, while lacking of an lever arm to translate detected shuttle error to the energy scale describing the local fluctuations of electrostatic potentials. The concrete correlation still requires the study on strain-induced potential disorder in QuBus that is currently conducting by Costanza from IKZ.

5.4. CONCLUSION

We have presented a comprehensive analysis of disordered potentials along a QuBus channel using the "drop and catch" method, supported by simulations and comparative measurements in the "roll-in and out" method. The "roll-in and out" method shuttles only one electron, whereas the "drop and catch" method paralyzes the shuttle tomography method by shuttling multiple electrons in QuBus. The same elementary pulse segments are assembled accordingly for both methods, providing a scalable method to sense the uniformity of the electrostatic potential in the QuBus. The sensed potential profile from "drop-and-catch" measurements reveals localized traps and humps, with traps at QD_9, QD_{17} and QD_{21}. These features were validated by independent "roll-in and out" measurements, showing agreements in the physical dimensions and positions of disordered potentials. On one hand, the "drop-and-catch" method provides unique sensitivity to complex potential profiles, such as combined humps and traps in QD_{27} and QD_{29}, which are not fully resolved by the "roll-in and out" method. On the other hand, the weak link at QD_4 detected by the "roll-in and out" method is confirmed by the "drop and catch" measurement to some extent, providing a identified trap with dimension less than λ, however, less observable as other traps, which in turn reflects the complementary nature of the two shuttle tomography methods.

In addition the SXDM measurement maps the strain components in the region of QuBus device. The correlation analysis incorporating the linear regression analysis links the electron error counts of drop and catch method to the potential profile. Among all strain components, ε_{xy} appears to be the most relevant term to correlate localized shuttle errors sensed by the drop and catch mode. However, its significance is not so distinguishable comparing to other elements such as ε_{xx}, ε_{yy}, ε_{zz} and ε_{xz} that the linear regression can not reveal its significant correlation to the electron error counts. Nevertheless, the element ε_{yz} appears to be least relevant to the localized shuttle errors. And the deduced rotational element w_{xz} is capable to represent the potential bending in the center of the QuBus due to the lattice rotation.

As a result, these findings demonstrate the robustness of shuttle tomography as a high-resolution tool for characterizing potential landscapes in spin-qubit devices, particularly offering the insight of the realistic disordered potential for long-range coupler of spin qubits. Additionally, compared to the pulsing schemes of the conventional "roll-in and out" method, the phase shift pulses in the "drop and catch" method inherit simplic-

ity and further enable the conveyor-mode shuttling by a fraction of λ thereby enhancing the spatial resolution of the shuttle tomography method without additional control complexity. By establishing these methods, we provide a pathway for benchmarking the charge transport in scalable quantum computing architectures. Further studies on the strain induced potential in QuBus devices and its correlation to the localized shuttle error could be helpful to develop a new method to characterize long-range coupler in the SpinBus architecture.

6

TOWARDS A SCALABLE ARCHITECTURE

No, but I am told it works even if you don't believe in it.

Niels Bohr (probably apocryphal)

In the pursuit of scalable quantum processors, the integration of extended QuBus i.e. the T-junctions into SpinBus architecture presents a promising approach to enhance the connectivity of qubits in a two-dimensional array. More specifically, the T-junction provides an interface between perpendicular shuttle lanes enabling both linear and corner shuttling modes. The former in principle replicates the operation of QuBus devices, and the latter navigates electrons through the three-way intersection with ideally the same control complexity as a linear QuBus. Efforts on simulations presented in this chapter reveal that the individual controls are required for either shuttle modes to maintain the adiabaticity of conveyor-mode shuttle. The critical point appears for the corner shuttling where the symmetry of confinement breaks at the junction area. This issue can be mitigated by operating the T-junction in the parking mode incorporating a sigmoid-shaped pulsing voltage applied to the individually controlled gates in the junction area especially the confinement gate T-CG that separates two shuttle lanes. However, strong confinements provided by the shuttle amplitude $A_S \geq 160\ mV$ are demanded to avoid potential tunnelings at the junction area in the presence of charged defects. Further improvement requires optimizations on the gate layout particularly the screening gate as well as the potential homogeneity of the hosting material for ultimately implementing a scalable quantum processor based on the SpinBus architecture.

The QuBus device in Si/SiGe has been shown its capabilities of shuttling electron linearly and bi-directionally over a 19 μm distance in conveyor mode. The number of control signals remains constant and independent of shuttle distance. However, the interconnection of a two dimensional qubit array for a scalable architecture lacks of the core part that is the T-junction which interfaces two perpendicular QuBus devices. The T-junction device has been investigated from the theoretical perspectives in the past few years [159–161] with yet limited public reports [18]. This chapter covers all my working efforts related to T-junction including the device design and the control pulse optimizations.

Following the brief overview of the T-junction device as a core part of the SpinBus architecture (Sec. 6.1), the main focus of this chapter will be on the discussions of the working principle of T-junction. In Sec. 6.2, two ways of operating a T-junction are reviewed those are the linear shuttle and the corner shuttling. The former is identical to a linear QuBus which is essentially the base line to justify the functionality of a T-junction. The latter is the unique operational mode for T-junction to shuttle electrons between two perpendicular lanes by turning electrons around the corner. Specific issues that break the tunnel free principle of conveyor mode shuttling are observed when the electron turning around the corner within the junction area. The reason behind lies on the symmetry change of confinements leading to drops of orbital splittings (E_{orb}) and indicating a high possibility of tunnelings. The critical points and attempts to avoid tunneling between shuttle lanes are presented for instance the parking-mode of corner shuttling. In a more realistic study, the charged disorders are involved to examine the weakness of T-junction shuttling (see Sec. 6.3). Demands of further investigations will be listed in Sec. 6.4 as an outlook.

6.1. T-JUNCTIONS IN THE SPINBUS ARCHITECTURE

WITHIN the frame of scalable architecture for spin qubits operations, dense qubit array faces challenges in connectivity and control crosstalk often being referred as the fan-out problem [15]. Implementing spare qubits arrays emerges an appealing solution [14, 17]. The conveyor-mode shuttling by SiGe QuBus discussed previously has presented the capability of commuting spin qubits over long distance paving the way towards a network of qubit arrays. Inheriting advantageous of QuBus, the SpinBus architecture should have the possibility to circumvent the foreseeable fan-out issues and connecting sparse qubits array by shuttling electrons in conveyor mode at a frequency in the order of $\mathcal{O} \sim 10$ MHz meanwhile maintaining the spin coherence through the motional narrowing effects [18, 22].

The SpinBus architecture consists of multiple functional blocks such as the linear shuttle lanes i.e. QuBus, the T-junction, the initialization and readout zone and the manipulation zone (see Fig. 6.1) in a tileable unit cell. Among aforementioned building blocks, the T-junction is one of the corner stones of the SpinBus architecture enabling the 2D connectivity of spare qubit arrays. A T-junction connects two perpendicular shuttle lanes without, in principle, introducing additional gates, while in fact extending the clavier gate. In addition, the T-junction plays an important role in a unit cell of the SpinBus architecture by connecting different operation zones such as the initialization, manipulation and readout zone as a three-way intersection those are necessary for qubits

operations.

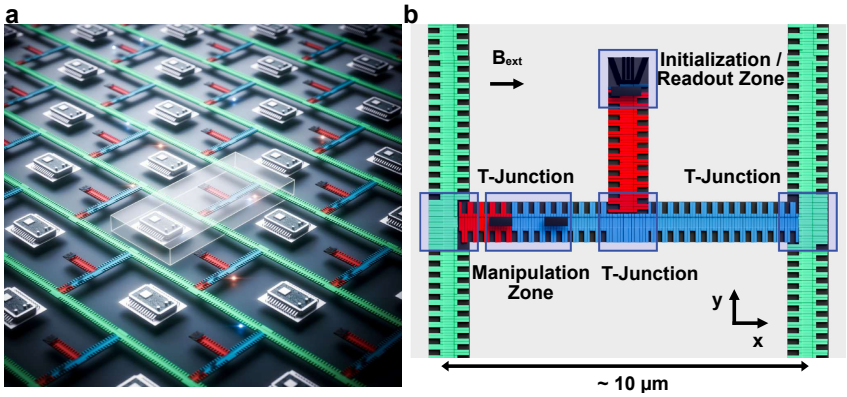

Figure 6.1: **Schematics of SpinBus architectures and its unit cell: a** The SpinBus architecture for scalable quantum processors by tiling a unit cell (highlighted by the transparent block). QuBus (green shuttle lanes) and T-junctions (cross-sections between differently colored shuttle lanes) are interconnecting sparsely positioned qubit arrays interleaving space for cryo-electronics (micro-chip symbols). The SiGe heterostructure is not shown here, instead the sparkling spots in red and blue symbolically illustrate spin qubits. **b** A unit cell of the SpinBus architecture including different functional blocks such as initialization and readout zone and manipulation zone interfaced by T-junctions. 10 μm corresponds to the scale of QuBus being demonstrated previously. Both sketches are directly adapted from published journal paper Ref. [18].

A T-junction device is fabricated in the CMOS compatible processing line identical to the QuBus devices. It follows mostly similar processing recipe of QuBus except for the steps those are sensitive to the modification of gate layouts such as the EBL step. Fine gate patterns being processed by the EBL are shown in Fig. 6.2.

6.2. SHUTTLE TRAJECTORIES AND CONTROL PULSE OPTIMIZATIONS

TWO trajectories of shuttling should work in a T-junction device those are: one the linear shuttling and the other the corner shuttling. This section will examine the linear shuttling pulse conveying electrons from the right to the left branch of a T-junction device, and then a detailed discussion about the working principles of corner shuttling is followed. Either shuttle trajectory has its own challenges to be addressed. For the linear shuttling, the study of its robustness will be explored in the parameter space of voltage pulses because of the relatively trivial dynamics in a shuttling process. In contrast, a stable corner shuttling requires more lever arms including the modification of the pulse profiles and changes in gate structures.

6.2.1. LINEAR SHUTTLING

Linear shuttling in T-junction is the most essential working mode and the base line of an operational T-junction, because it is in principle identical to a QuBus device that has been thoroughly investigated and optimized [43, 98]. In this study, the focus will include only the left and the right branch of a T-junction device (see Fig. 6.3 **a**). Omit-

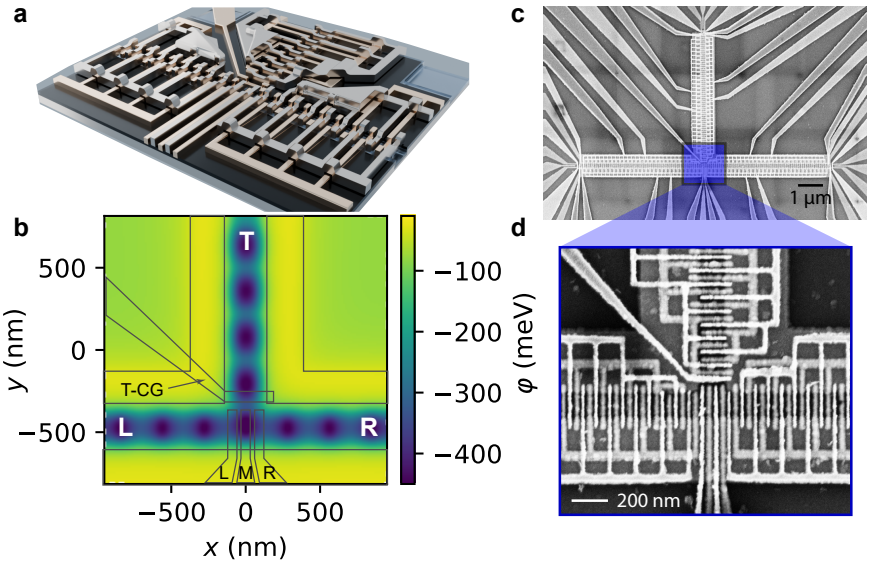

Figure 6.2: **T-junction devices: a**, 3D visualization of the T-junction device focusing on the junction area and the gate layouts. Three branches (**T, L, R**) are connected by a three-way junction. Each individual branch shares similar gate layout as QuBus consisting four clavier gates. T-branch is separated by an individually controlled gate (T-CG). The junction area consists five individually controlled gate being the up-to-date design. **b**, simulated electrostatic potential of the T-junction device with a gate pitch $W_P = 70$ nm representing the stat-of-the-art of T-junction optimizations. The outer two individually connected gates in the junction area are electrically connected to the clavier gates of **L** and **R** branch respectively, and thus not explicitly shown here. Only are three centric individual gates L, M and R are overlaid above the simulated electrostatic potential. **c** the SEM image of a fabricated T-junction device for the proof-of-principle. A gate pitch $W_P = 35$ nm was chosen underscoring the capability and resolution limitations of EBL. **d** A zoom-in view of the junction area highlighted in **c**.

ting all clavier gates in the T-branch except for the confinement gate (T-CG), the rests of a T-junction operate identically as a linear QuBus. The only difference is that three clavier gates cover the junction area breaking the periodicity of conveyor pulses along the linear channel. It is unavoidable unless the gate pitch matches a quarter of channel width which violates the optimized capacitive couplings. In this T-junction model, the channel width $d_{\mathrm{ch}} = 200\,\mathrm{nm}$ and the clavier gate pitch $W_{\mathrm{P}} = 70\,\mathrm{nm}$ are inherited from an optimized QuBus [43, 98]. To firstly adapt optimized geometries, clavier gates in the right branch needs a shift in phase. For the ease of understanding, gate phases are denoted with respect to the left branch. As shown in Fig. 6.3 **b**, the gate layout above simulated potentials is marked by $1,2,3,4$ representing the indices of clavier gates in the left branch. Three gates in the junction area (L, M and R) are individually controlled and synchronized to the phase of CL_2, CL_3 and CL_4, respectively.

Analogy to the conveyor shuttling in QuBus, pulse voltages applied to clavier gates in this T-junction device read,

$$\begin{cases} V_{\mathrm{CJ}_i}(t) = r \cdot g(i) \left[A_S \cos\left(2\pi f t - \dfrac{\pi(i+1)}{2}\right) + B_s \right] + \Delta B_s \cdot g(i+1) \\ g(w) = \dfrac{1+(-1)^w}{2} \end{cases} \tag{6.1}$$

where $V_{\mathrm{CJ_i}}$ denote the voltages applied to the i-th clavier gate in the branch J, thus $i = 1,2,3,4$ and J = L, R, T. In contrast to the QuBus pulses, the parameter r, representing the voltage ratio between gates on two different layers, is explicitly introduced for optimization purposes, and thus a helper function $g(w)$ is used to mask parameters according to the gate indices. $g(w) = 0$ when w are odd, and $g(w) = 1$ when w are even numbers. In this example, the clavier gates with odd indices are on the third layer. As a result, ΔB_S only applies to the gates CJ_i ($i = 1,3$), and the pre-factor r will reduce the voltages for gates on the lower layer with a ratio not larger than 1. Consequently, the shuttle amplitude A_S describes the amplitude of sinus pluses for gates on the third layer, thus the global upper limit of sinus pulses for clavier gates.

With given voltages, the time evolution of the potential can be presented by tracking the local minima of a chosen QD. Assuming an electron is confined by this QD, the shuttled electron follows the trajectory as being indicated by the dashed arrow in Fig. 6.3 **b**. It starts from the right branch and approaches the junction (i.e. $x = 0\,\mathrm{nm}$ beneath the clavier gate M) after one shuttle period T. After that, the QD moves towards the L-branch. The abrupt jump in Fig. 6.3 **b** does not stand for a physical trajectory of shuttled QD, but due to the periodicity of the potential instead. The whole process involves two shuttle periods. By setting the moment when the QD aligning to gate M as an origin, the influence of the free parameters r and ΔB_S on the confinement can be examined in the time span of $t/T \in [-1,1]$.

Providing the obvious breathing effect of the potential φ along the shuttle trajectory in Fig. 6.3 **b**, qualitative studies of confinement variations are necessary. An intuitive approach would be evaluating the potential variation as being shown in Ref. [160], however, the evolution of the orbital splitting E_{orb} are of more interests during shuttling processes. As previously derived in Ch. 2 Sec. 2.3.1, the curvature closing to the local minima of the shuttle QD is another metric strongly correlating to the E_{orb}. Therefore, the curvature c of the chosen QD is evaluated in the parameter space of r and ΔB_S as depicted

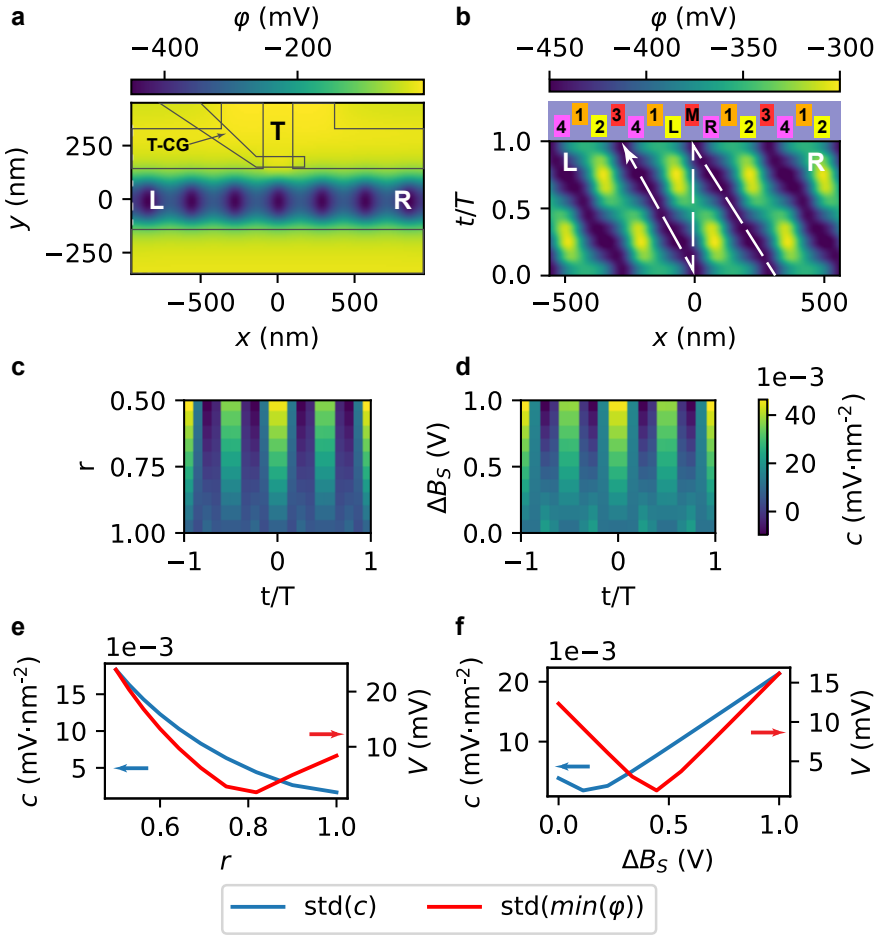

Figure 6.3: **Linear shuttling in T-junction: a**, The simulated electrostatic potential for linear shuttling along the left and right branch of T-junction device. Overlaid blocks illustrate the projection of screening gates and that of the confinement gate (T-CG) to separate the **T**-branch from linear part of the T-junction. **b**, T-junction in linear shuttling modes. The time evolution of φ is represented by only the line-cut along the linear channel for simplicity. The dashed arrow denotes the shuttling direction aligning with the gates shown on top. **c**, The voltage ratio (r) dependence of QD's curvature (c) for a shuttled QD along the trajectory shown in **b**. **d**, The relative voltage offset between two layers of gate electrons (ΔB_S) affects the QD's curvature (c) for a shuttled QD along the trajectory shown in **b**. **e**, the standard deviation of c (blue) and that of the local minima of φ (red) as a function of r. **f** the standard deviation of c (blue) and that of the local minima of φ (red) as a function of ΔB_S.

in Fig. 6.3 **c, d**, respectively. In these results, the significant periodicity along the t-axis comes from the gate layout as being expected. By varying the parameters r and ΔB_S, the periodic breathing of c tends to smearing out at specific values.

To be more precise and comprehensive, the standard deviation of $c(t)$ within the studied time span $t/T \in [-1,1]$ is evaluated for each swept parameters (see Fig. 6.3 **e, f**), and the standard deviation of the potential minima $min(\varphi)$ in the chosen QD is plotted as well for reference. Although the $std(min(\varphi))$ show a minima in both parameter scans which appear to be a good figure of merit for tuning, the curvature c does not agree with the tendency. In the scan of ratio r, the standard deviation of curvature c drops monotonically as r approaching 1 suggesting no needs of the pre-factor between layers to maintain less varying E_{orb}. On the other hand, the relative voltage offset ΔB_S is more favorable to compensate the lever arm difference for gate electrodes on two layers. Its influence is significant as the deviation of c reaches minima quickly when $\Delta B_S \approx 100\,\text{mV}$, indicating a rather narrow margin for a coarse tuning, yet a smaller range $100 \pm 100\,\text{mV}$ benefiting the fine tuning with a higher voltage resolution. Moreover, the breathing effect of c becomes monotonically severe for $\Delta B_S > 250\,\text{mV}$ leading to a completely detuned conveyor potential that should be avoided in the actual operation. Remarkably, these parameters sweeps are one dimensional by setting the other parameter constant closing to the local minima of $std(c)$. It is indeed necessary to make a fine 2D scan in the parameter space to explore a global minima for pulse optimizations. However, the results are sufficiently indicative due to a monotonic dependence of r. Last but not least, a minor change in c eventually the E_{orb} is observed in simulations. The reason for that is the symmetry change at the junction area. It is not too severe in this show case due to a compensation voltage is applied to the T-CG gate such than the confinement symmetric at the junction remains mostly constant. The observation of potential variation in the vicinity of the T-junction are detailed in the Appendix A.3 by simulated results and analysis. In conclusion, maintaining a linear conveyor belt across the junction area is capable by setting parameters r, ΔB_S as well as the voltage $V_{\text{T-CG}}$. Although the lateral confinement along the y-axis at the junction area is provided by the T-CG gate instead of the screening gates with stronger lever arm, it is possible to be compensated by voltage configurations in particular $V_{\text{T-CG}}$. But it is not exclusively rule out the necessity of segmenting the bottom screening gate in the linear lane as suggested in Ref. [18], because the voltage compensation here tackles solely the linear shuttling so far.

6.2.2. CORNER SHUTTLING

Shuttling electron around the corner of the T-junction emerges the necessity and the critical role of T-junctions in a 2D qubits network. The base line of shuttling electrons through this three way intersection demands a conveyor mode shuttling between two perpendicular shuttle lanes that is in another word a tunneling free corner shuttling process. To have a first insight on the dynamics during corner shuttling, electrostatic potentials are simulated incorporating the evaluation of E_{orb} for the shuttled electron in a QD. Due to the mirror symmetry of T-junction, turning an electron from right or from left to the top branch are identical. The following studies take the corner shuttling from the right branch (**R**) to the top branch (**T**) as an example.

The electrostatic potential for corner shuttling is depicted in Fig. 6.4 **a** which is noth-

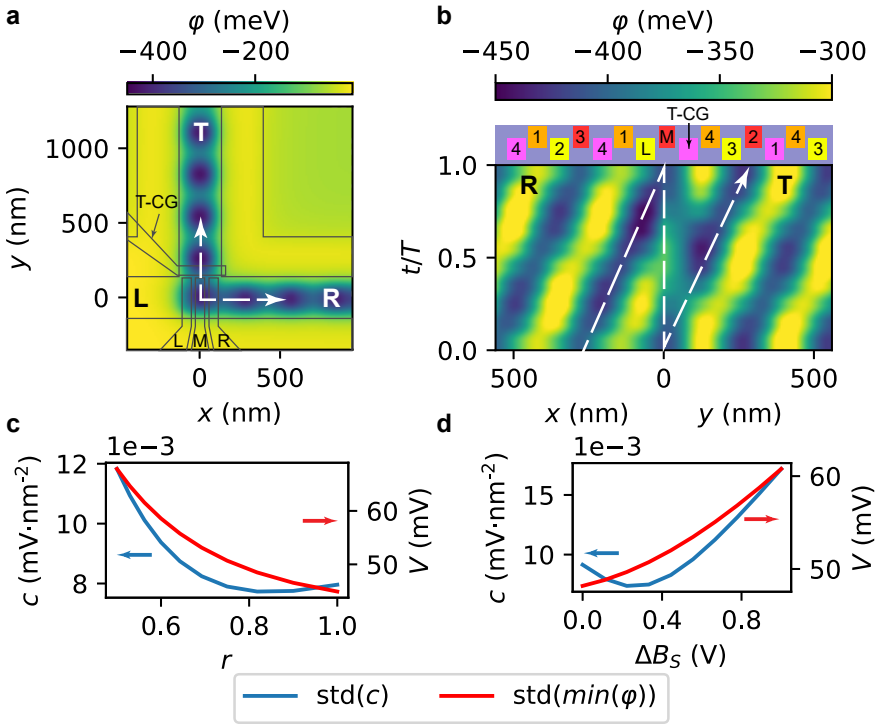

Figure 6.4: **Corner shuttling in T-junction: a**, The simulated electrostatic potential for corner shuttling between the right (**R**) and top branch (**T**) of a T-junction device. Overlaid blocks illustrate the projection of screening gates for confining the linear shuttle lane, the confinement gate (T-CG) and three individually controlled finger gate (L, M, R). The corner shuttling is a bi-directional process as depicted by the dashed arrow. **b**, T-junction in corner shuttling modes. The time evolution of φ is represented by tracing the local minima along the shuttle trajectory shown in **a**. The dashed arrow here denotes the shuttling direction **R** → **T** as an example. $\varphi(t)$ is aligned to the gate layout shown above. Notably that the right half of this layout locates on the **T** branch perpendicular to the **R** branch, thus not a linear sequence in real devices. **c**, the standard deviation of c (blue) and that of the local minima of φ (red) as a function of r. **d** the standard deviation of c (blue) and that of the local minima of φ (red) as a function of ΔB_S.

ing difference than the linear shuttle but enabling the **T**-branch meanwhile turning off the **L**-branch. This can be implemented by mapping the voltages for clavier gate sets on the **L**-branch to their counterparts in the **T**-branch one-to-one and grounding all clavier gates in the **L**-branch by setting $V_{\mathrm{CL}_i} = 0$. In addition, synchronizing individually controlled gates in the junction area (L, M, R) to (V_{CT_4}, V_{CT_3}, V_{CT_2}) accordingly as being calculated by Eq. 6.1 settles the potential in the junction area with correct phase to interface conveyor potentials in two perpendicular shuttle lanes (**R** and **T**). The dynamics of φ in one period is subtracted by following the local minima of the shuttled QD over time as shown in Fig. 6.4 **b**. Notably that the left- and right-half of this plot correspond to different shuttle lanes thus two perpendicular axes are joint at the origin.

Analogously, the variation of dot curvature c and the fluctuation of φ have impact on the E_{orb} of shuttled electron as in the linear shuttling. Due to the symmetry break of confinements in two perpendicular directions, their influence on E_{orb} requires more careful calculations to prevent unintended double dots configurations, which may lead to the tunnel events violating the adiabatic and tunnel-free shuttle process aimed by conveyor-mode shuttling. This is in turn representing a smooth transition of the local minima of φ across the corner. In another word, the wavefunction of shuttled electron should remain within the same QD instead of appearing in an adjacent QD for instance the QD in the **T** branch. If it happens, the simulated E_{orb} will typically show a sudden jump along the t-axis indicating an uncaptured tunneling due to the use of a stationary Schrödinger solver.

Since the purpose of this simulation is not to study the time-evolution of the wavefunction, but to explore a reasonable voltage range to implement a tunnel-free corner shuttle, the pre-factor r and the relative gate voltage offset ΔB_S in Eq. 6.1 are swept to coarsely target a set of parameters (see Fig. 6.4 **c, d**). Interestingly, the standard deviation of c shows minima for both parameter sweeps underscoring the hot-spot to find a smooth transition across the corner. The sweep of r reaches the minimum closing to 0.82 and the sweep of ΔB_S reaches the minimum at ≈ 200 mV when setting $r = 0.82$. This behavior suggests the need of tuning both layer factor and the DC offset to avoid uneven variations in the dot curvature and eventually the E_{orb}.

Setting applied voltages to this local minimum does not entirely ensure the adiabaticity of corner shuttling, meaning that the DQD configuration could occur during the corner shuttling. In terms of the conveyor-mode shuttling, the tunneling-free mechanism should be preserved as well. More qualitative and thorough study rely on the evaluations of orbital splittings E_{orb}. Previous optimizations on the capacitive couplings suggested a gate pitch of 70 nm [43] which is adapted in T-junction. For this configuration, $E_{\mathrm{orb}} \geq 1$ meV is targeted to maintain the adiabaticity of conveyor mode shuttling in the present of potential disorders. Unfortunately, unintended low $E_{\mathrm{orb}} < 1$ meV are witnessed even before introducing potential disorders (see Fig. 6.5 when $t/T \approx 0.7$). This observation implies the intrinsic deformation of dot geometries in the T-junction leading to the change of electron wavefunctions as can be seen in the inset of Fig. 6.5, although the fluctuations of E_{orb} have been optimized by adapting parameters $r = 0.82$ and $\Delta B_S = 200$ mV as being discussed above. Therefore, it should be attributed to the formation of unintended DQD configuration in the junction area being one of the critical points of T-junction corner shuttle.

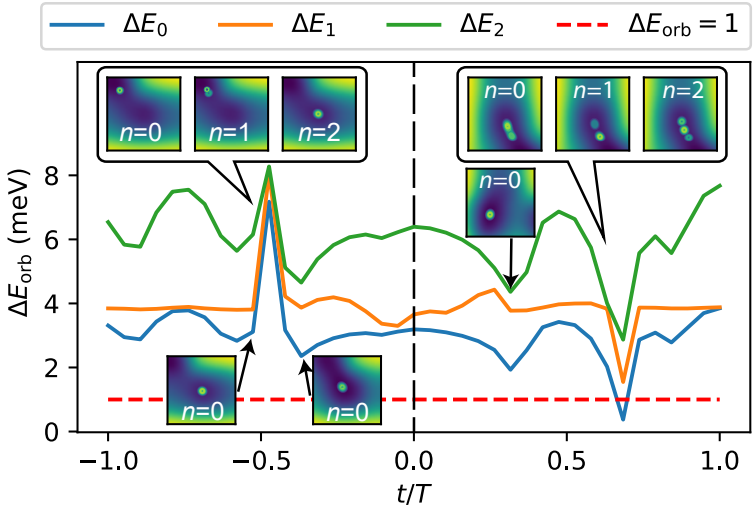

Figure 6.5: **Critical points in corner shuttling:** The evaluated E_{orb} for the lowest three eigenstates when the shuttled electron passing through the junction area. The center of the junction is marked by the vertical dashed line (black) at $t/T = 0$. A negative t/T stands for the shuttling process in the **R**-branch and the positive t/T the **T**-branch. The red dashed line represents the critical E_{orb}= 1 meV. The simulated φ and wavefunctions $|n\rangle$ are presented selectively only when an abnormal E_{orb} taking place. Bounding boxes for solving the Schrödinger equations were set sufficiently large (i.e. covering both QDs adjacent to the junction area) to avoid digital error through all time steps. The upper left bubble includes three lowest $|n\rangle$ at the spike closing to $t/T \approx -0.5$ and two snapshots before and after this spike on the bottom left illustrate the ideal $|n\rangle$ of the shuttled electron (ground states). The other bubble on the top right presents the wavefunctions at the dip around $t/T \approx 0.7$. In addition, a shallower dip at $t/T \approx 0.25$ gives rise to an exceptional case that the electron is pushed towards the grounded **L**-branch before entirely being injected into the **T**-branch.

The typical and critical points of corner shuttle are highlighted in Fig. 6.5 appearing as abrupt jumps of E_{orb}. Two significant jumps at $t/T \approx -0.5$ and 0.7 correspond to the configurations that the shuttled electron is approaching and leaving from the junction area at $t/T = 0$, respectively. When the electron remains within the **R**-branch ($t/T < 0$), the wavefunction of shuttled electron $|n\rangle$ should have the appearance of an s-orbital state being the initialized ground state. However, its energy may not be the lowest one when the unintended double dot forms as depicted in the top left insets. At the moment when $t/T \approx -0.5$, the QD in the **T**-branch experiences a minor detune with respect to the **R**-branch such that both s, p-orbits in that QD have lower energies than the s-orbits in the shuttle QD within the **R**-branch. As can be seen in the electron wavefunctions, the $n = 0, 1$ represent the s, p-orbits in the QD within the **T**-branch however the s-orbit in the QD within the **R**-branch experiences a higher eigenenergy. In fact, these three eigenstates are mostly degenerated. This is an obvious indicator of a tunneling event that breaks the conveyor mode shuttling. Similarly, the strong deformation of φ appears repeatedly when the electron is leaving from the junction, for instance $t/T \approx 0.7$.

Moreover, another shallower dip appears at $t/T \approx 0.25$ when the electron is yet conveyed out of the junction. As the conveyor potential in the **R**-branch evolves continuously, the shuttled electron is inevitably pushed towards the **L**-branch which is turned-off in this example. In another word, this dip would be enlarged if the conveyor potential in the **L**-branch is enabled. Considering the extreme case that the phase is onsite with respect to the **R**-branch, this onsite conveyor potential will bring the electron to the **L**-branch as a linear shuttling process instead of letting electron turning into the **T**-branch.

The observed jumps of E_{orb} are mainly affected by the voltage detuning between different branches, which could be compensated by tunning the voltage offsets B_S on different branches. However, it is not a favorable solution for operating T-junctions. The reason is that the tuning of B_S should apply to all clavier gates on each individual branch. In an operational T-junction, B_S is supposed to be supplied by DC voltage sources either at room temperature or a cryogenic one and is shared by the linear lanes. Tuning B_S would interfere the tuned configurations in other shuttle lanes. Moreover, it is possible to have another qubit idling in an individual branch when a qubit is turning around the corner. This scenario can be expected in the T-junctions interconnecting manipulation zone and readout/initialization zone. Therefore, constraining the voltage adjustments locally in the junction area is necessary not only due to the simplicity for optimizations but also benefiting the use cases of T-junction in practice.

6.2.3. PULSE OPTIMIZATIONS

Four individually controlled gates (L, M, R and T-CG) are designated for optimizing the shuttle trajectories in particular the corner shuttling locally with minor interference to connected shuttled lanes. The so far observed DQD configurations are mainly resulting from controlling barriers between two lanes by continuously evolving conveyor potential. That means a dissolution of demanded barriers at the corner. Adjusting the continuity of the sinus pulse in time would circumvent this issue. Notably, breaking the continuity here stands for the iteratively operating conveyor potentials on two perpendicular shuttle lanes instead of a sudden switch of voltages on any gates. For example, the **T**-branch or at least the T-CG gate idles or remains depleting before the shuttled

electron entering the junction ($t/T < 0$). And the **R**-branch remains idling or depletes the electron when the electron is conveyed by the potential in the **T**-branch ($t/T \geq 0$). Consequently, one branch remains static forming a parking slot at the junction for the electron, and the other conveys an electron into or out of this parking lot, hence being termed the *parking mode*.

The plain parking mode, that only are the conveyor potentials alternatively switched over between two perpendicular lanes, is exemplified in Fig. 6.6 **a** from the perspective of E_{orb} evolution (see Appendix Fig. A.6 for the applied voltages). It is apparent that the existing drops in the dynamically evolving corner shuttle remain unoptimized, while a minor change happens to the significant drop of E_{orb} at $t/T \approx 0.7$. As can be seen in the insets, the wavefunction of the ground state is successfully carried by the conveyor potential in the **T**-branch yet entirely isolated from the linear lane by proper barriers. That indicates the needs of tuning T-CG gate to form barrier so that the shuttled electron does not tunnel backwards to the **R**-branch again. Similarly, the significant drop of E_{orb} at $t/T \approx -0.5$ remains challenging for the same reason that the barrier between two perpendicular channels is vaguely formed, and thus the shuttled electron has a high probability to tunnel through. In addition, the dip at $t/T \approx 0.25$ becomes severe and the electron risking tunneling. The reason is that the middle gates (L, M, R) are still operating in conveyor mode thus the parking lot evolves continuously. Consequently, the optimization of corner shuttle in parking mode demands carefully design and tuning of individually controlled gates in the junction area.

Technically, the parking mode relies on docking and undocking the shuttled electrons into and out of the junction that can be accomplished by the following alternatives.

- by gates (L, M, R incorporating T-CG)
- by the lower screening gate (Scr)
- by a segment of bottom screening gate (adjustments in gate layouts)

From the pulsing voltage perspectives, all approaches could employ the same pulse profile to fine adjust the detuning between the static QD and the propagating conveyor potential. Due to the need of breaking continuity of sinus pulses meanwhile avoiding abrupt jumps in pulsing, a sigmoid pulse shape is the most natural and straightforward choice which gradually links two different values. Considering the periodicity, the pulse needs to be a closed loop thus a general expression of pulse within the targeted ramp time and idling time can be explicitly written by,

$$V_{\mathrm{J}}(t) = \delta A_{\mathrm{J}} \cdot \left(1 - \frac{1}{1 + e^{-\alpha \cdot |t-\beta| + \gamma}}\right) + B_{\mathrm{J}} + \delta B_{\mathrm{J}}; \qquad \mathrm{J} = (\mathrm{L, M, R, T\text{-}CG, Scr}) \tag{6.2}$$

where δA_{J} stands for the absolute pulsing amplitude for the individual gate J. δB_{J} is the DC offset for fine tuning gate J in addition to its original DC offset B_{J} in the conveyor potential. More importantly, parameters α, β and γ describe the shape of pulse. α dominantly controls the steepness of the rising pulse, β for the time when the rising pulse reaches the setting value, and the γ is used to flattening the target voltage i.e. the halting time at the setting value. The larger γ, the smoother transition between ramping up and down. However, having multiple parameters in exponents leads to drastic changes in the

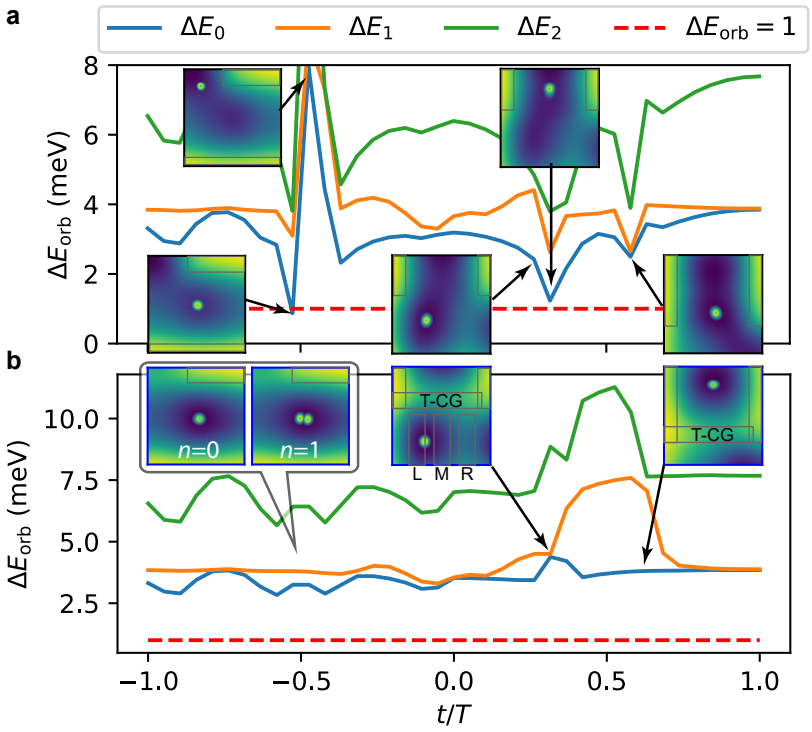

Figure 6.6: **Evolutions of E_{orb} in the parking mode: a**, the E_{orb} in the plain parking mode without pulsing any individually controlled gates in the junction area. Similarly, four lowest eigenenergies are calculated yielding three E_{orb}. Insets present all inspected ground state ($n = 0$) at critical points pinned by corresponding arrows. **b**, the optimized E_{orb} with gradually rising $V_{\text{T-CG}}$ meanwhile idling gates L, R. Middle gate M is ramped inversely with respect to the T-CG gate. Without specifically labelled, only ground states ($n = 0$) are shown for clearance. Both plots share the same legend above **a** and the critical E_{orb}= 1 meV are marked in both simulations. Corresponding pulsing voltages for the plain parking mode and the optimized parking mode, are shown in Appendix Fig. A.6 and Fig. A.7 in the Appendix Sec. A.4, respectively.

final pulse shape despite of a minor variation in any parameter, yet a rather constrained parameter space to search for an optimal pulse shape. Assuming a ramp is completed when it reaches 99% and 99.9% of the setting value. $\alpha \in [20, 30]$ results in the rising time of approximately $[0.5, 0.3]\,T$ for 99% completeness and approximately $[0.7, 0.5]\,T$ for 99.9%, respectively. In terms of γ, the completeness of [99%, 99.9%] corresponds to a range $\gamma \in [5, 7]$.

Leveraging the narrow margin for tuning and given observations in Fig. 6.6 **a**, an optimized pulsing scheme involves the L, R and T-CG gates is applied (see Appendix Fig. A.7 for the detailed pulses). This pulsing scheme aims at eliminating the significant jumps of E_{orb} at $t/T \approx -0.5, 0.25$ and 0.7 due to the continuously evolving conveyor potential in the junction area when docking and undocking the electron. In consequence, the requirements become the followings. First, a proper barrier should be formed before docking the electron ($t/T \approx -0.5$) and after undocking electrons ($t/T \approx 0.7$) between two perpendicular lanes. Second, the electron should not be squeezed against the blocking branch ($t/T \approx 0.25$). That means shutting off the **T**-branch by the T-CG gate before docking the electron as being done in the linear shuttling, and then the voltage of L, R stays on-hold after $t/T = 0$ to maintain a quasi-static QD in the junction. At the same time (i.e. $t/T \geq 0$), the middle gate (M) and T-CG gate ramps in opposite phases to hand over docked electrons from M to T-CG and eventually the **T**-branch.

Applying the aforementioned strategy, the E_{orb} over time for a corner shuttling in the parking mode becomes mostly flat above 2.5 meV (see Fig. 6.6 **b**). First of all, the most dramatic spikes in E_{orb} at $t/T \approx -0.5$ is flattened significantly, providing the critical and essential role of T-CG in maintaining confinements along the linear shuttle lane as being evidenced in Appendix Sec. A.3. Second, the enlarged drop of E_{orb} at $t/T \approx 0.25$ in the case of plain parking mode vanishes due to the proper confinement provided by T-CG gate (see the middle inset in Fig. 6.6 **b**). Notably, the electron is still squeezed towards the **L**-branch given the fact that the wavefunction of the ground state lies between L and M gate. This effect is mainly a result of the asymmetric potential in the linear shuttle lane in which the **L**-branch is closed by setting all clavier gates to zero and the conveyor potential in the **R**-branch remains positive. This will lead to a detuning of the QD at the junction whose curvature is smaller on the left hand side and vice versa. On the other hand, the potential steepness under gate L is larger than that under gate R. As a result, the local minima of this QD appears off-centered and lies closing to L gate, especially when the M gate in ramped down to push the electron into the **T**-branch in this case. This issue is in fact tunable demanding carefully tuning of the waveform applied to M gate and the T-CG gate for $t/T \geq 0$. It is accomplished by fine adjusting the parameters $\delta A_{\mathrm{J}}, \alpha, \beta$ and γ in Eq. 6.2. The detailed study has been shown in Ref. [160] instead of being repeated here. Last but not least, the eigenenergies for $t/T \geq 0.7$ particularly the ΔE_0 between lowest two eigenstates is significantly flattened. As being depicted in the top right inset of Fig. 6.6 **b**, the ground state conservatively carried by the conveyor potential in the **T**-branch without risking a backwards tunneling owing to a properly formed barrier by the T-CG gate.

While the tuning strategy works properly to maintain a large ($E_{\mathrm{orb}} \geq 1$ meV) and the voided fluctuations for corner shuttling in the parking mode, it does not stand for a golden rule to preserve the adiabaticity through the junction. The screening gate plays

an important role as well. An alternative is pulsing the lower screening gate of the linear shuttle lane to push docked electrons into **T**-branch with the waveform of Eq. 6.2. Another way towards an optimal control in the junction area is to split this screening gate into segment such that the junction area has a designated segment of screening gate to fine tune the local potential. Both methods are detailed in Ref. [160] and will not be repeated in this section.

6.3. PRESENT OF CHARGED DEFECTS

CHARGED defects inducing potential disorders and are impactful for the conveyor mode shuttling of electrons as being discussed in previous chapters. It matters for T-junction devices for the same reason, and may be more impactful at the junction area where the confinement exchanging directions. An optimal control over this region in the presence of charged defects is of more practical interests. A good examiner of the tuning strategy being proposed above would be introducing the charged disorder ensembles into the model and evaluate the E_{orb} when the T-junction operates in the parking mode. In this section, the charged defects locating at the oxides-semiconductor interface will be again considered as the dominant source of potential disorders as for QuBus devices. For a good statistics, 100 ensembles of defects with a density of $5 \times 10^{-10}\,\text{cm}^{-2}$ are involved.

By applying the pulsing strategy discussed in Sec. 6.2.2, the T-junction is modeled under varying shuttle amplitudes A_S for the parking mode (see Fig. 6.7 **a**). To justify the robustness against defects i.e. avoiding the degenerated orbital states those $E_{\text{orb}} < 10\,\mu\text{eV}$, a higher orbital splitting $E_{\text{orb}} = 1\,\text{meV}$ is employed as a threshold value to filter out ensembles those may result in degenerated eigenstates. With a sufficiently strong confinement ($A_S = 280\,\text{mV}$), the E_{orb} remains higher than 2 meV, whereas occasional ensembles start pulling down the E_{orb} already with $A_S = 200\,\text{mV}$. Although the overall $E_{\text{orb}} > 1\,\text{meV}$ is still valid, this behavior implies a weakness of the parking mode, which is in fact the intrinsic geometrical issue of T-junction that the strongest confinement changing its directions when switching the shuttle lane. More sever drops appear at $t/T \approx 0.25$ for $A_S = 120\,\text{mV}$ as being expected. This reveals the fact that the pulsing strategy is suboptimal at $t/T \approx 0.25$ when introducing potential disorder. It is expected as mentioned above that the QD in the junction area remains asymmetric due to an all-grounded **L**-branch. Additional potential disorder therefore leads to severe detuning and finer optimizations are still required to adjust the phase between T-CG and gates (L,M,R). Consequently, it is not unexpected to see both failures of linear shuttling and corner shuttling when $A_S = 40\,\text{mV}$ which is much lower than required confinements for conveyor potential. Nevertheless, the parking mode shows its strong robustness against defects while halting the electron in the junction properly. In addition, the optimizations of T-CG voltages provide a clear stability in the presence of defects, particularly when the $A_S = 120\,\text{mV}$ falls approximately the similar voltage range for operating linear QuBus (i.e. $A_S = 100\,\text{mV}$).

These results are indicative to estimate the lower bound of the charge shuttle fidelity F (i.e. the shuttle success rate) by employing $E_{\text{orb}} < 1\,\text{meV}$ as a pessimistic criteria for shuttle failures. This could be technically accomplished by counting the occurrence of $E_{\text{orb}} < 1\,\text{meV}$ for each attempt of shuttling under different ensembles and different A_S.

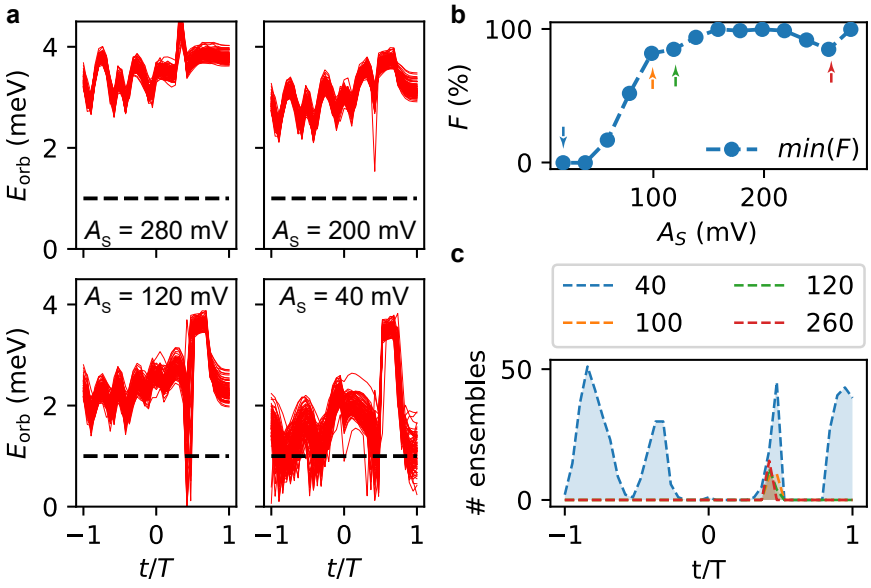

Figure 6.7: **Simulated E_{orb} for T-junction in parking mode with defects:** **a** In the presence of 100 defects ensembles, the variation of E_{orb} during the parking mode operation is examined under different shuttle amplitude $A_S = 280, 200, 140, 40$ as being labelled accordingly. Only the lowest E_{orb} is considered for clarity. The critical $E_{orb} = 1$ meV is marked by dashed line. **b** The estimated shuttle success rate F as a function of A_S by counting occurrence of $E_{orb} < 1$ meV under different A_S configurations. The minimum estimated F is shown here providing the lower bound of possible shuttle success rate i.e. F in this simulation. **c** Number of ensembles when $E_{orb}(t) < 1$ meV at different time within a complete corner shuttling process. A_S are selected from pinpointed datasets in **b**.

The statistics originate from in total 100 ensembles of defects distributions. For each ensemble distribution, any occurance of $E_{\mathrm{orb}} < 1$ meV in the simulated trace counts for a shuttle failure providing the lower bound of F (i.e. $\min(F)$). Given the dependence of confinements, the shuttle success rate depending on the applied amplitude A_S could be estimated as shown in Fig. 6.7 **b**. In this analysis, a critical confinement closing to 100 mV as for the linear QuBus sets the cut-off of $\min(F)$. With even lower shuttle amplitudes, the estimated $\min(F)$ reaching 0 % suggesting a poor possibility to maintain the orbital splitting of shuttled electron above 1 meV for all simulated defects ensembles those induce potential disorders in the device. A minor dip is observed at $A_S = 240$ and 260 mV revealing that some ensemble distributions lead to more asymmetric potentials during undocking the electron from the junction area, and the electron risks tunneling from the junction to the **T**-branch ahead of the movement of conveyer potential minima.

The heatmap of weak points in a corner shuttle is presented by Fig. 6.7 **c** for chosen characteristic confinements. It is obvious that the insufficient confinement $A_S = 40$ mV equally breaks the linear shuttling ($t/T < 0$) and the corner shuttling ($t/T > 0$). For the others larger than 100 V, neither the linear shuttling nor the parking of electron encounter with defects induced potential disorders due to the zero counting of failed ensembles in the vicinity of $t/T = 0$. Only when the electron leaving from the junction (i.e. $t/T \approx 0.25$), approximately 10 % ensembles risk tunnelings into the **T**-branch. To eliminate this failures, pulsing screening gate voltages offers a straightforward way. Detailed simulations have been shown in the Ref. [160].

6.4. OUTLOOK

WITHIN the frame of implementing scalable quantum processors by the SpinBus architecture, T-junction along with QuBus present their significant importance owing to their control simplicity and scalability to interconnect a two-dimensional sparse qubit array. The scalability and control simplicity are concluded according to the assumptions that shuttle lanes except for readout zones and manipulation zones could share the same set of control voltages. However, the simulations suggest that the weakness of T-junction i.e. during corner shuttling, a separate control of the screening gate is necessary to avoid the tunnelings at weak points including docking ($t/T \approx -0.5$) and undocking ($t/T \approx 0.25, 0.7$) the electrons into and out of junction area.

Although circumventing the weak points by high shuttle amplitude $A_S \geq 160$ mV is possible, few ensembles lead to tunnelings of electrons even at higher amplitudes as shown in Fig. 6.7. This effect mainly occurs at $t/T \approx 0.25$ when the electron is parked in the junction area and experiencing an asymmetric potential along the linear channel for instance an all-grounded **L**-branch in this study. It demands further investigations. Moreover, the lower shuttle amplitude is of more favorable considering the thermal budget that is not yet taken into account in this case study. Therefore, fine tuning the junction area by individually controlled gates particularly the screening gates becomes necessary in the future. Whereas slightly increase the control complexity should be expected. Furthermore, pulsing the screening gates globally affects other electrons halting in the linear shuttle lane. In consequence, the best solution would be splitting up the screening gate in the linear shuttle lane by leaving a small segment designated for the local control of the junction area. Taking all above issues into account, a remarkable wiring

complexity has been estimated to be $(15N+4)$ AC signals and $(3N+4)$ DC voltages for a SpinBus architecture with N unit cells [18], and to be demonstrated experimentally.

Last but not least, the intrinsic issue of Si/SiGe heterostructure i.e. the randomly distributed valley splitting is still missing in this model. Given the shuttle tomography for mapping valley splitting has been demonstrated for QuBus devices [29], an analogous protocol could be adapted for pre-screening T-junction as well. Leveraging more controls over the screening gates, locally circumventing electrons away from the detected low valley splitting regions becomes a potential alternative to shuttle spin qubit in the SpinBus architecture while maintaining its coherence. The experimental evidences are needed, and by the time of writing up this dissertation, a charge shuttling across the corner with 99.4 % fidelity at a shuttle frequency of $f = 100$ kHz has been observed according to the recent experiments ran by my colleague Max Beer. This result corresponds to the shuttling path including entirely both **T, L**-branches. A spin shuttling across the corner is to be accomplished and to be optimistically expected with reasonable fidelities.

7

CONCLUSION

The conveyor-mode shuttling presented in this dissertation represents the key ingredient of the scalable architecture (i.e. the SpinBus architecture) for large scale quantum processors. The device implementation including the linear QuBus devices and the T-junction devices are all produced on Si/SiGe heterostructures and thus CMOS compatible. The foundation of this work relies on reproducible and sustainable fabrication processes, which are standardized and optimized in this dissertation. Targeting a 60 nm gate width and 70 nm gate pitch (10 nm Al_2O_3 for isolation) benchmarking the 10 nm in semiconductors industries, the combination of high energy EBL (100 keV) and metal lift-off process yields multiple functional prototypes of QuBuses for charge shuttling, valley splitting mapping and bias-cooling experiments. Notably that, the fabrication processes presents its own scalability as a scaled-up T-junction shares a similar processing recipe as the linear QuBus revealing the scalable essence of conveyor-mode shuttling concept from the manufacturing perspective.

In practice, the conveyor-mode shuttling offers a replicable and full-electrically controllable method to transfer electrons in a scaled qubit network coherently without complicating the control complexity meaning that the number of required input signals for pulsing gate electrodes remains constant independent of the shuttle direction and shuttle distance. The demonstration of the long-range shuttling of electrons in a 10 μm long QuBus device is a testament to the capabilities of conveyor-mode shuttling and its scalability. The presented experiment provides the capabilities of shuttling electrons over 19.2 μm with high fidelities of (99.7 ± 0.3) % evidently. Only six input signals are required for such a long distance. Besides the shuttle distance, up to 34 electrons with arbitrarily chosen patterns of zero and single-electrons are initialized and detected as a register by this QuBus device using the same number of input signals, promising the scalability of conveyor-mode shuttling for transferring multiple qubits in large scale quantum computing architectures. However, challenges related to material limitations are witnessed as well where a locally enhanced confinement is required to circumventing specific weak spot in the long-range coupler. Notably, all aforementioned experiments are conducted for the purpose of prototyping the conveyor-mode shuttling and its scalability, and thus

shuttling in the slow motion with a velocity of 14 μm·s^{-1}, that is not at the target speed for spin shuttling (i.e. 10 m/s). Leveraging the tunability and controllability of the programmable pulsing schemes, the advanced characterization technique i.e. the shuttle tomography method is developed and demonstrated tackling the local potential disorders in a long-range coupler operating in conveyor-mode.

The shuttle tomography method is employed and developed to sense the electrostatic potential disorders and the randomly distributed valley splittings those are most critical and intrinsic material limitations in Si/SiGe based quantum devices. In this dissertation, the shuttle tomography method is mainly used to sense the electrostatic potential disorders. Two complementary methods are further developed based on the shuttle tomography namely the *roll in and out* method and the *drop and catch* method. Using the same 10 μm long QuBus device consisting of an array of 34 QDs, localized traps and humps in the conveyor potential at specific positions (QD_9, QD_{17} and QD_{21}) are detected with dimensions comparable to the dot size (λ = 280 nm) and being resolved with a spatial resolution of 35 nm. These findings are further correlated to the SXDM measurement, providing a chance to correlate the localized potential disorders to the strain components. These findings remarkably imply the necessity of characterizing the potential homogeneity of long-range couplers in advance as these potential disorders could significantly disrupt the electron transport and potentially the qubit coherence. It is worthy as scaling up quantum processors face severe inhomogeneity issues in potential landscapes. Owing to the scalability of the shuttle tomography method, it provides a reliable and efficient technique for benchmarking electron transport channel before fine tuning scalable quantum processors for qubit operations.

Despite of shuttle tomography being a scalable manner to characterize the potential profile along the channel, the actual physics resulting in the potential disorders needs further investigations. The vast majority of the origin lies in the charged defects in the hosting material including defects at the oxides-semiconductors interface and those in the Si/SiGe particularly closing to the Si QW where 2DEG are formed. Both types of defects are covered in this dissertation from either practical or theoretical perspectives. The former ones mainly induce potential disorders and act as remote scattering sites due to the decay of Coulomb interactions. Optimizations of this type of defects are involved in the fabrication processes by using the least amounts of oxides which eliminates the defects and enhances the screening effect of the gate electrodes. In terms of the defects in the vicinity of Si QW, a theoretical model is studied by solving time-depended Schrödinger equation for the orbital states of electrons in conveyor potential. Using the transition probabilities from the ground state to the first excited state as a criteria to justify the shuttle fidelity crucially, the correlation between finding a defect free channel and the defect density is estimated for a 10 μm long QuBus. Notably, the relaxation due to valley-phonon coupling are not involved in this model, thus it is a rather harsh estimation for targeted fidelities. However, the further studies (unpublished results for now) suggest not significant difference although further experimental evidences are still needed.

In the scaled up device (T-junctions), the charged defects play a critical role as well especially when an electron is shuttled through the intrinsic weak point in a T-junction. By reviewing the working principle of the T-junction device, it is observed that exchang-

ing of confinements at the junction area need to be treated carefully. According to the simulations, the corner shuttling needs to be operated in the *parking mode* incorporating pulsing individually controlled gates in the junction area with a waveform of sigmoid function. Using $E_{\mathrm{orb}} \geq 1$ meV as criteria to maintain the confinement of conveyor potential in the presence of defects induced potential disorders, the parking mode meets the requirement with shuttle amplitudes $A_S \geq 100$ mV suggesting an optimal strategy to navigate electrons into the junction area. However, the weak point appears when the electron leaving from the junction and entering the **T**-branch due to the directional change of confinements. While shuttle amplitudes $A_S \geq 160$ mV maintain the condition $E_{\mathrm{orb}} \geq 1$ meV, further optimizations such as splitting screening gate at the junction area could relief the needs of large confinement that is much favorable considering the thermal budget.

Last but not least, not only is the charged defect an obstacle on the pathway to the scalable architecture, but also the randomly distributed valley splitting plays a critical role. The alloy disorders in Si/SiGe heterostructures is believed to be the dominant resources and occasional low valley splittings or even zero valley splittings become impactful for shuttled spin qubits. Although pulsing screening gates laterally changes the shuttle trajectory and it could circumvent specific weak spots along a shuttle lane, efforts on pre-characterizations and local control are needed. Another solution to tackle this issue is to globally enhance valley splitting from the device manufacturing. Thanks to the electrically tunable nature of the valley splitting in Si/SiGe heterostructures, a new prototype of QuBus device is firstly explored by introducing a global backgate. By enhancing the perpendicular electric field, a systematic increase of the valley splitting can be expected.

Overall, the conveyor-mode shuttling offers a significantly improvement towards the scalable quantum processors in semiconductors, particularly in achieving reliable qubit transport over long distance without scaling up the control complexity. As the research progressing, the application and integration of shuttle tomography method will be expected to instrumentally improve the performance of operational SpinBus architectures. Based on standardized fabrication processes, minor structural modifications to the elementary devices could be straightforwardly applied without tuning overheads on the exploration of processing parameters. It is ultimately foreseeable that an operational unit cell of the SpinBus architecture will contribute to the research community in the near future.

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A

APPENDIX

A.1. QDs IN CONVEYOR POTENTIAL

Most QDs remain unchanged and static while reducing the confinement as illustrated in Fig. A.1 where $QD_{3,6}$ show an absolute no movement and $QD_{4,5}$ drifts by only 1 nm due to the digital error. $QD_{0,1,2}$ are almost robust against the confinement variation as their drift are negligible comparing to the wavefunction of a confined electron. The most significant drift of QD_7 is an exception due to edge effects and is not involved in the further discussion as well.

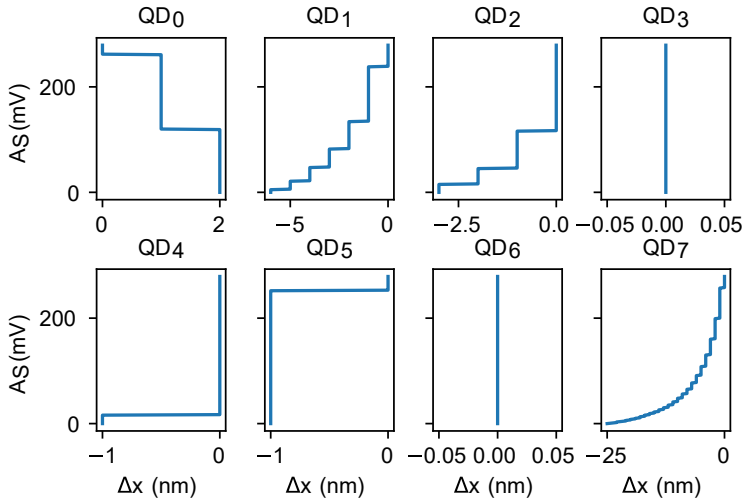

Figure A.1: **Traces of centroids of each QD**: The movement of the centroid of each QD while reducing the A_S are traced with respect to their initial position i.e. the centroid of each QD confined by the maximum A_S. Eight QDs are indexed from zero corresponding to the QDs in Fig. 2.8a.

A

The slanted electrostatic potential along the 1DEC provides detuning changes for the QDs. Regardless of the confinement potential, one magnitude higher detuning is observed between $QD_{1,2}$ (see Fig. A.2) compared to QDs further away from the SET.

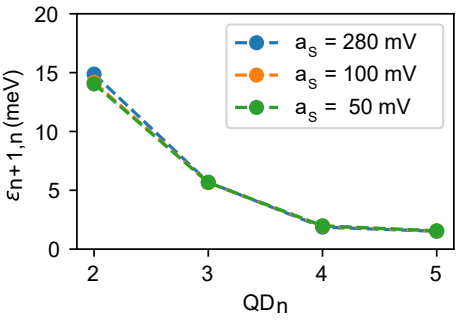

Figure A.2: **Estimated detuning between adjacent QDs**: Detuning between adjacent QDs in the present of SET to the left of the QuBus. Three shuttle amplitudes $a_S = 280, 100, 50$ mV are chosen corresponding the results shown in Ch. 2 Fig.2.8.

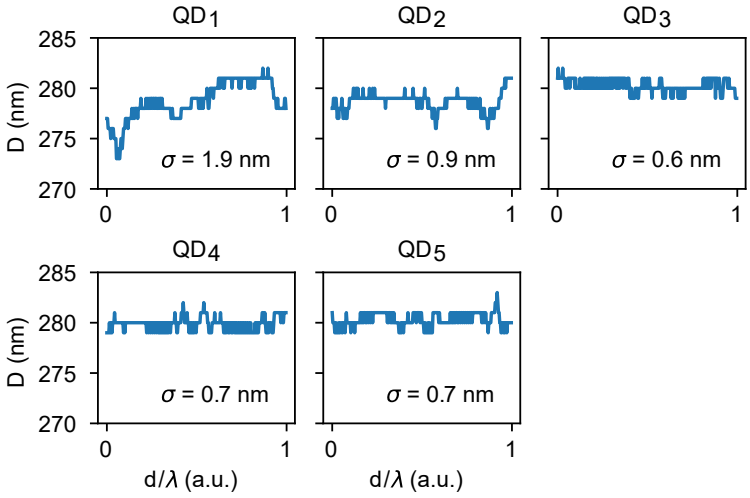

Figure A.3: **Variations of dot size in** 1λ: estimations of D for each QD. The variation of D in 1λ is given by its standard deviation σ.

Fig. A.3 shows that the variation of dot size D smears out as QD being shuttled away from the SET on the left. After 1λ, the non-zero σ dominantly results from the meshing resolution (1 nm) in this simulation, and thus not revealing the physical jittering effect.

A.2. STRAIN MAPS OF THE QUBUS DEVICE

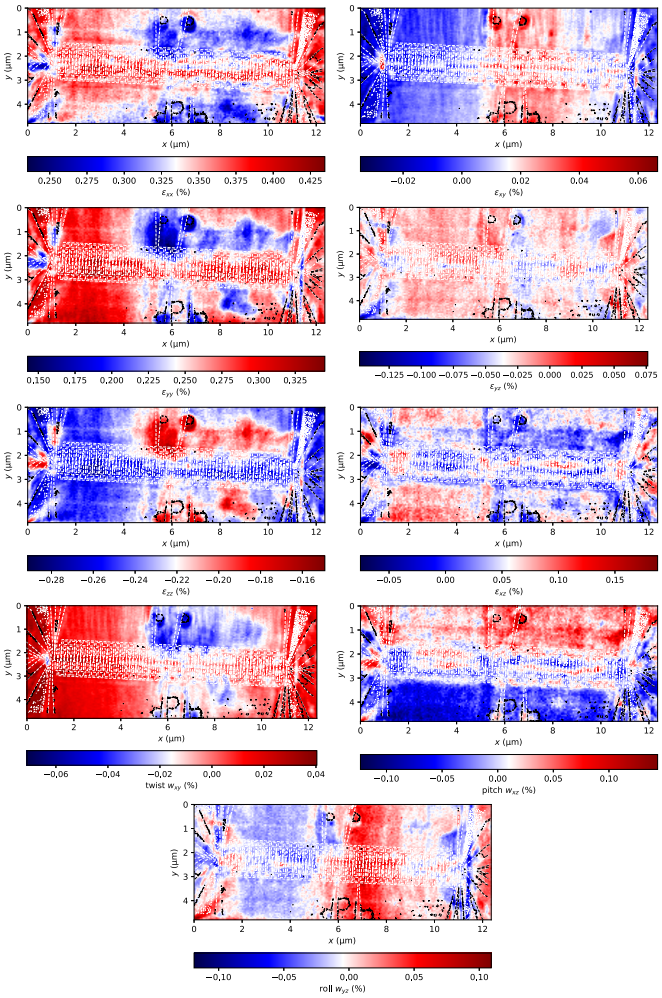

Figure A.4: **The strain map of the measured QuBus device in Ch. 4 and Ch. 5**: All components of the strain tensor measured by the SXDM measurement are overlaid with SEM image of the QuBus device (contours of gate-electrodes) where the while dashed lines are identified edges of gates and the black dashed lines outlining contrast variation on the surface of the device mainly on the oxides layer.

A

A.3. T-CG GATE IN LINEAR SHUTTLE

The critical issue for linear shuttling in T-junction resulting from a symmetry break of confinements at the junction area. Options including voltage compensations and gate layout optimizations offer capabilities to circumvent this issue. Here, the discussion covers the voltage compensation by T-CG gate due to its simplicity and the least violation to the device geometries. The simulation aims at a minimal deviation of E_{orb} when the shuttled QD passes through the junction area along the linear shuttle lane. The curvature of the shuttled QD appears to be the merit correlating to the E_{orb}. Therefore, the optimal voltage configuration of T-CG gate lies in the range where the deviation of c reaches a mimimum value.

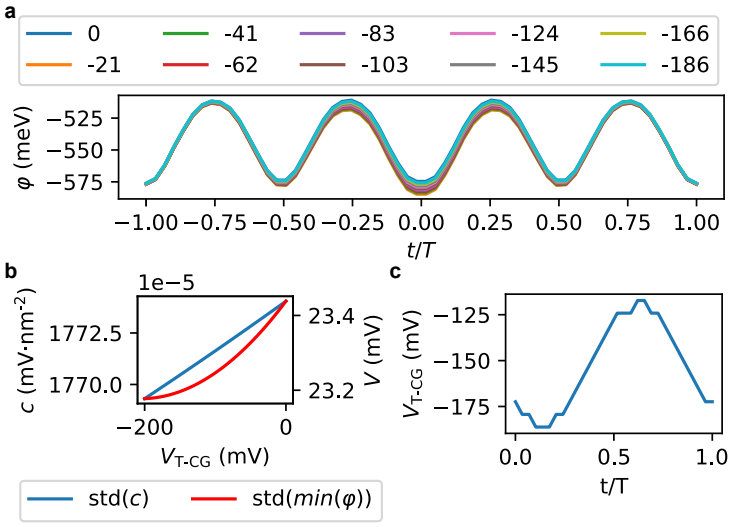

Figure A.5: **T-CG gate in linear shuttle**: **a**, simulated electrostatic potentials φ for linear shuttling an electron across the junction area with varying voltages applied to the T-CG gate. Corresponding $V_{\text{T-CG}}$ are listed in the legend with a unit of mV. **b**, standard deviations of fitted curvature c (blue) and that of local minima in tracked QD $min(\varphi)$ (red). **c**, The demanded $V_{\text{T-CG}}$ to maintain least variation of $min(\varphi)$.

Employing the same model as shown in Ch. 6, the time evolution of φ shows obvious decrease in the vicinity of the junction (see Fig. A.5 **a**). The more negative $V_{\text{T-CG}}$ is applied, the less drop at $t/T = 0$ as a negative $V_{\text{T-CG}}$ enhances the confinement in the direction perpendicular to the shuttle direction, thus consequently maintain the confinement in the junction area despite of lacking of the screening gate. Both $std(c)$ and $std(min(\varphi))$ monotonically within the range of swept $V_{\text{T-CG}}$ whereas c drops linearly and $min(\varphi)$ non-linearly (see Fig. A.5 **b**). Without a larger sweep range, a minimal deviation of either metrics are not visible. However, the time evolution of $min(\varphi)$ give rise to a suggestive way to optimize the voltage pulse for T-CG gate when operation T-junction in the linear shuttling mode. As shown in Fig. A.5 **c**, a sinus profile appears in the demanded $V_{\text{T-CG}}$ for maintaining a minimal deviation of $min(\varphi)$ within one period. Its sinus profile reveals essentially the cross couplings of conveyor potential indicating a way to compensate by means of T-CG gate voltages solely.

In summary, this simulation only focus on the evolution of potential in the vicinity of junction area when a T-junction device is operating in the linear shuttle mode. Instead of complicating the model for the sake of searching a global optimization strategy, this results preliminarily suggests an approach to live tune the device by pulsing T-CG solely so that the symmetry break of confinements does not affect the shuttling processes along the linear shuttle lane. Splitting a segment of the bottom screening gate in this region is another option that enables an individual control on the φ benefiting the voltage margin (i.e. a smaller compensation voltage range due to its larger lever arm towards 2DEG), and the corner shuttle as well, whereas increases the wiring complexity and the design complexity.

A.4. T-CG GATE IN CORNER SHUTTLE

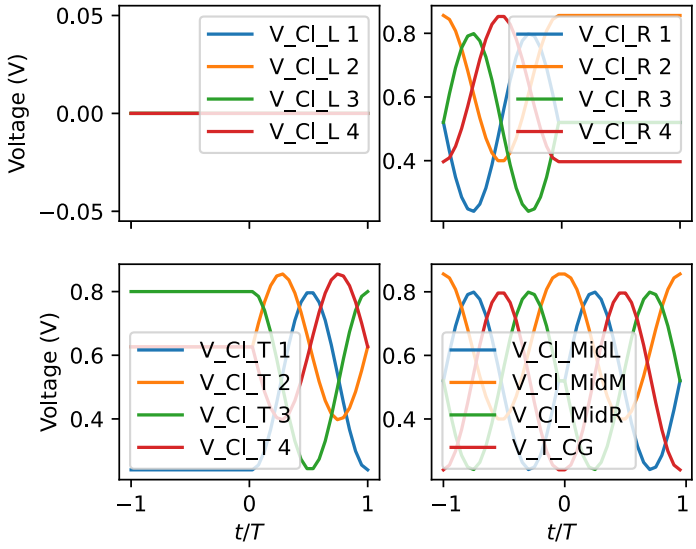

Figure A.6: **Pulsing voltages for a plain parking mode in corner shuttle**: Pulsing voltages of all gate electrodes in T-junction to demonstrate the plain parking mode for corner shuttling.

As being explained in the Ch. 6, the plain parking mode is identical to two concatenated linear shuttling pulses and being applied to the two perpendicular branches. When one conveyer potential is propagating, the other branch is idled. In this example, the electron is shuttled from the R-branch and being loaded in the T-junction area. Gates in the junction area (L, M, R and T-CG) are electrically connected to the clavier gates (R3, R2, R1 and R4) for $t/T \leq 0$, respectively. Consecutively, they have the same phases as claiver gates (T2, T3, T4 and T1) when $t/T \geq 0$.

The parking mode with optimized pulse shape are shown in Fig. A.7. The gate electrodes in the junction area inherit the same phases as for the plain parking mode. Only are the pulsing voltages of the T-CG gate and L, R gates subject modifications. In this case, the L, R gates are idled for undocking the electron from the junction area. During

A

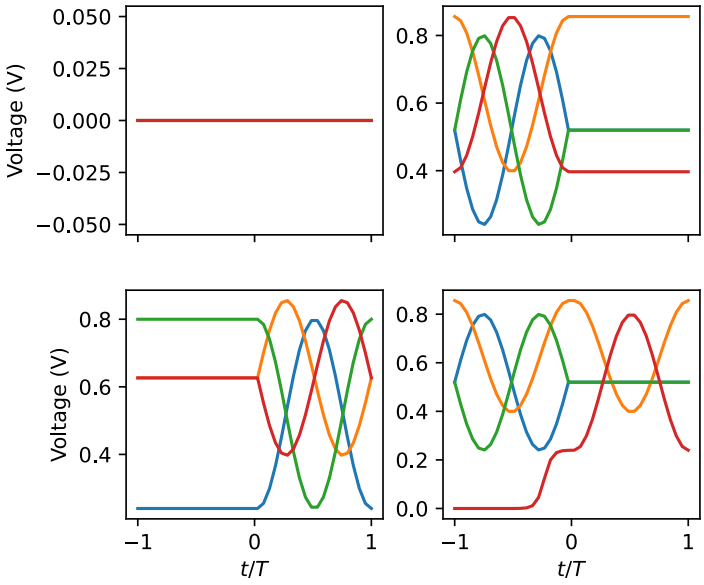

Figure A.7: **Pulsing T-CG and idling L, R for optimized parking mode**: Pulsing voltages of all gate electrodes in T-junction particularly the L, R and T-CG gate to optimize the plain parking mode for corner shuttling. The legend is same as in Fig. A.6 above thus not shown for better visibility.

the docking of electrons into the junction area, a sigmoid shaped puling voltage is applied to the T-CG gate that gradually adjust the detuning between the QD formed within the junction area and the propagating QD in the conveyor potential. Then voltage of T-CG is further raised to undock the electron from the junction to the T-branch as being depicted by the red curve in the bottom right penal in Fig. A.7.

A.5. PROCESS FLOW OF QUBUS DEVICES

In this section, the process flow of QuBus devices is attached. During the process development and establishment, spin coating instruments were changed thus modified lithography processes are listed afterwards with highlighted modifications.

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (Sample Cut)

	Process	Date	Chemicals	Target Parameters	Commentary	Operator
0.	Starting Material			70nm Gate pitch QuBus - 9-gate-device - 10µm QuBus	3x 10x10 mm^2 Si/SiGe 2x Lawrence 1x QT477 Delft implanted at PGI-9 (marker etched with old recipe)	Ran Xue
1.	Cleaning (Solvent):		ACE IPA	> 10 min (> 5min for each)	ultrasonic bath at WB 2.1 power level 9, N2 blow dry.	

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (Marker dry etch)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
0. Starting Material			70nm Gate pitch QuBus - 9-gate-device - 10µm QuBus	3x 10x10 mm² Si/SiGe 2x Lawrence B	Ran Xue
1. Cleaning (Solvent):		ACE IPA	> 10 min (> 5min for each)	ultrasonic bath at WB 2.1 power level 9, N2 blow dry.	
2. Spin coating (Coating)				All at WB 2.2	
2.1. Dehydrationbake			130 °C, >3 mins	Cool down on spin coater By N2 blow for 10 s	
2.2. Spin on		AZ 5214E	Program: 3000 rpm 1min		
2.3. Softbake			95 °C, 120 s	With Natalie's recipe for softbake	
3. Exposure				All at mask aligner 4 + mask cleaner	
3.1. Exposure: N2 blow clean, expose		MA4	30 mJ/cm²	Recipe Bruger_AZ5214_1.4µm_neg (~1.5s, 30 mJ/cm^2) Image Reversal Bake (Si Coating Bench) Bake <120 °C for 2 min 40 s Recipe Bruger_AZ5214E_flood	
4. Development (Development):				All at WB 2.3	
4.1. Development		AZ326 MIF DI	1min	> 2 min in resining tanks, N2 blow dry	
5. RIE etching		SF6 O2	1min30sec	In RIE4, with recipe ' RIE-4, Ch1-JST-SiGe-LowT EBL marker '.	
6. Stripping		ACE IPA	> 10 min (> 5min for each)	ultrasonic bath at WB 2.1 power level 9, N2 blow dry.	
7. Analysis			Mesa height ~1 µm	Dektak 150	

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (Ohmic Ion-Implantation & RTP)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
0. Starting Material			70nm Gate pitch QuBus - 9-gate-device - 10µm QuBus	3x 10x10 mm² Si/SiGe Etched cryo-E-beam markers on top 1x Lawrence B to be implanted at PGI-9 1x Lawrence B to be implanted at Rossendorf Etched standard markers on top 1x QT477 Delft implanted at PGI-9	Ran Xue
1. Cleaning (Solvent):		ACE IPA	> 10 min (> 5min for each)	ultrasonic bath at WB 2.1 power level 9, N2 blow dry.	
2. Spin coating (Coating)				All at WB 2.2	
2.1. Dehydrationbake			130 °C, >3 mins	Cool down on spin coater By N2 blow for 10 s	
2.2. Spin on		AZ 5214E	Program: 3000 rpm 1min		
2.3. Softbake			95 °C, 120 s	With Natalie's recipe for softbake	
3. Exposure				All at mask aligner 4 + mask cleaner	
3.1. Exposure: N2 blow clean, expose		MA4	30 mJ/cm²	Recipe Bruger_AZ5214_1.4µm_neg (~1.5s, 30 mJ/cm^2) Image Reversal Bake (Si Coating Bench)	
4. Development (Development):				All at WB 2.3	
4.1. Development		AZ326 MIF DI	1min	> 2 min in resining tanks, N2 blow dry	
5. Ion implantation		P	20keV 5e 15 [cm^-2]	1x Lawrence B implanted at PGI-9 (Dan Buca) 1x Lawrence B implanted at Rossendorf	
6. Stipping		AR300-76 IPA	overnight	AR300-76(overnight due to hardening of resist), IPA	
7. Annealing in RTP		RTP	5 K/s, 700°C, 15s and 30s	Doubled time for comparisons	

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (Mesa dry etch)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
2. Starting Material	15.10.2020		70nm Gate pitch QuBus - 9-gate-device - 10µm QuBus	3x 10x10 mm^2 Si/SiGe Etched E-beam markers on top and ion implantation is done. 1x Lawrence B implanted at PGI-9 1x QT477 Delft implanted at PGI-9 1x Lawrence B implanted at Rossendorf RTP (IHP-Aachen) condition 700 oC and 750 oC 15s	Ran Xue
3. Cleaning (Solvent):		ACE IPA	> 10 min (> 5min for each)	ultrasonic bath at WB 2.1 power level 9, N2 blow dry.	
4. Spin coating (Coating)				All at WB 2.2	
4.1. Dehydrationbake			130 °C, >3 mins	Cool down on spin coater By N2 blow for 10 s	
4.2. Spin on		AZ 5214E:EBR=2:1 , 2 drops	Program: 3000 rpm		
4.3. Softbake			95 °C, 120 s	With Natalie's recipe for softbake	
5. Exposure				All at mask aligner 4 + mask cleaner	
5.1. Exposure: N2 blow clean, expose		MA2	45 mJ/cm^2	2" Chuck; vaccum contact, Channel #1 With Natalie's recipe for positive_0.7um process.	
6. Development (Development):				All at WB 2.3	
6.1. Development		AZ326 MIF DI	1min	> 2 min in resining tanks, N2 blow dry	
7. RIE etching		SF6 O2	1min30sec	In RIE4, with recipe 'Ch1-IS-Si SF6 O2'.	
8. Stripping		ACE IPA	> 10 min (> 5min for each)	ultrasonic bath at WB 2.1 power level 9, N2 blow dry.	
9. Analysis			Mesa height ~80 nm	Dektak 150 Lawrence chips: 100 nm QT477 Delft: 75 nm	

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (Ohmic metallization)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
0. Starting Material	15.10.2020				Ran Xue
1. Cleaning (Solvent):		ACE IPA	> 10 min (> 5min for each)	ultrasonic bath at WB 2.1, N2 blow dry.	
2. Spin coating (Coating)				All at WB 2.2	
2.1. Dehydrationbake			130 °C, >3 mins	Cool down on spin coater By N2 blow for 10 s	
2.2. Spin on		AZ 5214E:EBR=2:1 , 2 drops	Program: 3000 rpm		
2.3. Softbake			95 °C, 120 s	With Natalie's recipe for softbake	
3. Exposure				All at mask aligner 4 + mask cleaner	
3.1. MA4			30 mJ/cm²	2" Chuck; vaccum contact, Channel #1 With Natalie's recipe for negative_0.7um process.	
4. Reversal bake			115°C 120 s	With Natalie's recipe for image reverse	
5. Flood exposure (MA4)			220 mJ/cm"	With Natalie's recipe for flood exposure 40s.	
6. Development (Development):				All at WB 4	
6.1. Development		AZ326 MIF DI	1min	> 2 min in resining tanks, N2 blow dry	
6.2. Drying			Hot-plate @ 130°C > 10 min	Only do that when rushing HF dip at the same day as development.	
7. HF dip		HF	1% for 1min	WB4 and load in Univex 400 loadlock as soon as samples leaving water bath.	
8. Evaporation		Ti/Pt	5 nm 0.1 nm/s; 150 nm 0.4 nm/s	Univex 400	
9. Lift-off		ACE IPA	Acetone lift-off overnight	WB9.1	
10. Analysis				Optical inspection, no token ohmic contacts on Lawrence chips. Delft ones have bad ohmic adhesion same as Batch 7 from Jhih Sian.	

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (L1- ALD Al2O3)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
0. Starting Material	16.10.2020				Ran Xue
1. Cleaning (Solvent):		ACE IPA	> 5 min for each	at WB 9.1 after lift-off overnight, N2 blow dry.	
2. ALD				Nanoclaster ALD	
2.1. Deposition		Al2O3	10 nm		
3. Analysis				No	

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (First fine gates and coarse contacts)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
0. Starting Material					Ran Xue
1. Cleaning (Solvent):		none		Not necessary as samples are unloaded from ALD right before spin coating. (In case not: ACE + IPA >5min in each at WB2.1)	
2. Spin coating (Coating)				All at WB 2.2	
2.1. Dehydrationbake			150 °C, >3 mins	Cool down on spin coater By N2 blow for 10 s	
2.2. Spin on		CSAR dilute 1:1, 1~2 drops	Program: 2500 rpm with lid		
2.3. Softbake			150 °C, 60 s		
3. E-beam exposure	16.10.2020			QPC_2device_v4_SiGe_L1a	
3.1. E-beam writing					
4. Development (Development):				All at WB 2.1	
4.1. Development		AR600-55 IPA DI	60 s for each	N2 blow dry	
5. Evaporation		Ti/Pt	5/15 nm		
6. Lift-off	22.10.2020	AR-600-71 IPA DI IPA		ultrasonic bath at WB 9 power level 1, Stay in AR600-71 >4hr, N2 blow dry.	
7. Analysis					

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (L2-ALD Al2O3)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
0. Starting Material	22.10.2020			L1 complete.	Ran Xue
1. Cleaning (Solvent):		none		Not necessary as samples are loaded into ALD loadlock right after lift-off.	
2. ALD				Nanoclaster ALD	
2.1. Deposition		Al2O3	10 nm		
3. Analysis				No	

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (Second fine gates and coarse contacts)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
0. Starting Material	22.10.2020			L1 complete. Second Al2O3 deposited	Ran Xue
1. Cleaning (Solvent):		none		Not necessary as samples are unloaded from ALD right before spin coating. (In case not: ACE + IPA >5min in each at WB2.1)	
2. Spin coating (Coating)				All at WB 2.2	
2.1. Dehydrationbake			150 °C, >3 mins	Cool down on spin coater By N2 blow for 10 s	
2.2. Spin on		CSAR:AR600-2= 1:1, 2 drops	Program: 2500 rpm		
2.3. Softbake			150 °C, 60 s		
3. E-beam exposure				Design: QPC_2device_V4_SiGe_L2b	
3.1. E-beam writing					
4. Development (Development):				All at WB 2.1	
4.1. Development		AR600-55 IPA DI	60 s	N2 blow dry	
5. Metalization		Ti/Pt	5/22 nm		
6. Lift-off	29.10.2020	AR-600-71 IPA DI IPA		ultrasonic bath at WB 9 power level 1, Stay in AR600-71>4 hr, N2 blow dry.	
7. Analysis					

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (L3 ALD Al2O3)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
0. Starting Material	29.10.2020			L1 &L2 complete.	Ran Xue
1. Cleaning (Solvent):		none		Not necessary as samples are loaded into ALD loadlock right after lift-off.	
2. ALD				Nanoclaster ALD	
2.1. Deposition		Al2O3	10 nm		
3. Analysis				no	

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (Third fine gates and coarse contacts)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
0. Starting Material	29.10.2020			L1 &L2 complete. Third Al2O3 deposited.	Ran Xue
1. Cleaning (Solvent):		none		Not necessary as samples are unloaded from ALD right before spin coating. (In case not: ACE + IPA >5min in each at WB2.1)	
2. Spin coating (Coating)				All at WB 2.2	
2.1. Dehydrationbake			150 °C, >3 mins	Cool down on spin coater By N2 blow for 10 s	
2.2. Spin on		CSAR:AR600-2= 1:1, 2 drops	Program: 2500 rpm		
2.3. Softbake			150 °C, 60 s		
3. E-beam exposure	29.10.2020			Design: QPC_2Device_V4_SiGe_L3c	
3.1. E-beam writing					
4. Development (Development):				All at WB 2	
4.1. Development		AR600-55 IPA DI	60 s for each	N2 blow dry	
5. Metalization		Ti/Pt	5/29 nm		
6. Lift-off		AR-600-71 IPA DI IPA		ultrasonic bath at WB 9 power level 2, Stay in AR600-71>4 hr, N2 blow dry.	

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (Bonding pads for Batch 3.2)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
0. Starting Material	29.10.2020			L1 &L2 complete. L3 Al2O3 and fine gates deposited	Ran Xue
1. Cleaning (Solvent):		ACE IPA	>5 min for each	at WB 2.1, N2 blow dry.	
2. Spin coating (Coating)				All at WB 2.2	
2.1. Dehydrationbake			130 °C, >3 mins	Cool down on spin coater By N2 blow for 10 s	
2.2. Spin on		AZ 5214E:EBR= 2:1, 2 drops	Program: 2500 rpm		
2.3. Softbake			95 °C, 120 s	With Natalie's recipe for softbake	
3. MLA		MLA	300 mJ defoc +4		
3.1. Development		MIF 326 DI	1 min	In DI water bath > 1min	
3.2. HF dip	30.10.2020	HF 1%	30 second	Sample stay in box overnight	
4. Evaporation		Ti/Pt	5 nm 0.1 nm/s; 150 nm 0.4 nm/s	Univex 400	
5. Lift-off		ACE IPA	30 mins in Acetone (1 min ultrasonic bath with power level 1)	WB9.1	
6. Analysis					

Version: 15 10 2020 **Process responsible: Ran Xue**

Sample ID: QuBus Batch 3.2 **Sample size:** 10x10 mm
User/Group: QuTech **Institute:** RWTH/HNF

Workflow (Device cut for Batch 3.2)

Process	Date	Chemicals	Target Parameters	Commentary	Operator
0. Starting Material				L1, L2 and L3 complete.	Ran Xue
1. Cleaning (Solvent):		ACE IPA	> 5 min for each	at WB 2.1, N2 blow dry.	
2. Spin coating (Coating)				All at WB 2.2	
2.1. Dehydrationbake			130 °C, >3 mins	Cool down on spin coater By N2 blow for 10 s	
2.2. Spin on		AZ 5214E, 4 drops	Program: 4000 rpm 500 rpm/s		
2.3. Softbake			95 °C, 120 s	With Natalie's recipe for softbake	
3. Device cut				Saw & Dicing DISCO 1	
4. Cleaning (Solvent):		ACE IPA	> 5 min for each	at WB 2.1, N2 blow dry and place in Gel Pack.	
5. Delivery				Bring back to Aachen	

CSAR E-beam Coating and Development

Coating

1. Cleaning:
    1. Acetone (US if no fine gates / low power) minimum 3 min
    2. IPA (US if no fine gates / low power) minimum 3 min
    3. N_2 blow dry
2. Spin coating (Si Coating Bench)
    1. Dehydration:
        i. 150 °C for >3 min (removes residual water)
    2. Coat:
        i. Cool/clean sample with nitrogen gun
        ~~ii. AR 600.62 4000 rpm closed lid~~
        NEW SPIN COATER:
        Diluted CSAR62: AR600 = 1:1
        2500 rpm, 1min => 90 nm
        iii. Bake:
        iv. 150 °C for 1 min

Cleaning Coater with DMSO TechnicSTrip 350 and then IPA

Development (@WB2.1 or 9.1/9.2) - Special Gloves (one for HF) due to developer (Toxic & green gloves dissolvable)

Do it with 3 beakers! Better not use inner basket to hold contamination from beaker to beaker.

1. 60s AR 600-55 (MIBK)
2. 30 s IPA
3. 30 s H20 (large beaker to reduce residue IPA content percentage)
4. N2 blow dry

Lift-off (WB9.1)

5. CSAR Remover Ar600-71 (> 30 minutes to remove)
6. Dip in Acetone (removes Remover residue)
7. IPA (few minutes)
8. N2 blow dry

User: Ran Xue

Optical Lithography 0.7 µm negative process

Coating

1. Cleaning:
    1. Acetone (US if no fine gates / low power) minimum 3 min
    2. IPA (US if no fine gates / low power) minimum 3 min
    3. N_2 blow dry
2. Spin coating (Si Coating Bench)
    1. Dehydration:
        i. 120 °C for >3 min (removes residual water)
    2. Coat:
        i. Cool/clean sample with nitrogen gun
        ~~ii. AZ5214 E 3000 rpm closed lid~~
        NEW SPIN-COATER
            1. Diluted AZ5214E:EBR = 3:1
            2. 3500 rpm, 1min => 0.778 um.
    3. Bake:~
        i. <100 °C for 2 min (Bruger_softbake)

Exposure

1. Mask Cleaning:
    1. Both sides of mask (SiGe Qubus… RWTH /Seidler 2016)
2. Mask Aligner 4:
    1. Recipe Bruger_AZ5214_0.7µm_neg (~1.5s, 30 mJ/cm^2)
    2. Clean sample with N2 before exposure
3. Image Reversal Bake (Si Coating Bench)
    1. Bake <120 °C for 2 min (bruger_imagel)
4. Flood Exposure
    1. 40 s Recipe Bruger_AZ5214E_flood

Development

1. Sample In basket
2. AZ326 MIF for 60 s
3. > 1 min in “Vorspülung”
4. > 1 min in “Qualitätsspülung”
5. N2 blow dry

User: Ran Xue

Optical Lithography 1.4 µm negative process

Coating

1. Cleaning:
    1. Acetone (US if no fine gates / low power) minimum 3 min
    2. IPA (US if no fine gates / low power) minimum 3 min
    3. N_2 blow dry
2. Spin coating (Si Coating Bench)
    1. Dehydration:
        i. 120 °C for >3 min (removes residual water)
    2. Coat:
        i. Cool/clean sample with nitrogen gun
        ~~ii. AZ5214 E 5000 rpm~~
        NEW SPIN-COATER
            1. AZ5214E (not diluted!) 3000 rpm 1min
    3. Bake:~
        i. <100 °C for 2 min

Exposure

1. Mask Cleaning:
    1. Both sides of mask
2. Mask Aligner 4:
    1. Recipe Bruger_AZ5214_1.4µm_neg (~1.5s, 30 mJ/cm^2)
    2. Clean sample with N2 before exposure
3. Image Reversal Bake (Si Coating Bench)
    1. Bake <120 °C for 2 min
4. Flood Exposure
    1. 40 s Recipe Bruger_AZ5214E_flood

Development

1. Sample In basket
2. AZ326 MIF for 70 s
3. > 1 min in “Vorspülung”
4. > 1 min in “Qualitätsspülung”
5. N2 blow dry

User: Ran Xue

B

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- T. Struck, M. Volmer, L. Visser, T. Offermann, **R. Xue**, J.S Tu, S. Trellenkamp, L. Cywinski, H. Bluhm, L. R. Schreiber Spin-EPR-pair separation by conveyor-mode single electron shuttling in Si/SiGe. *Nat Commun.* **15**, 1325 (2024).
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- M. Volmer, T. Struck, A. Sala, B. Chen, M. Oberländer, T. Offermann, **R. Xue**, L. Visser, J.-S. Tu, S. Trellenkamp, Ł. Cywiński, H. Bluhm, L. R. Schreiber. Mapping of valley splitting by conveyor-mode spin-coherent electron shuttling *npj Quantum Inf* **10** (2024).
- J. Ferrero, T. Koch, S. Vogel, D. Schroller, V. Adam, **R. Xue**, I. Seidler, L. R. Schreiber, H. Bluhm and W. Wernsdorfer. Noise reduction by bias cooling in gated Si/Si_xGe_{1-x} quantum dots *Appl. Phys. Lett.* **124**, 204002 (2024).
- I. Seidler, T. Struck, **R. Xue**, N. Focke, S. Trellenkamp, H. Bluhm, and L. R. Schreiber. Conveyor-mode single-electron shuttling in SiSiGe for a scalable quantum computing architecture. *npj Quantum Inf* **8**, 100 (2022).