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Regrown quasi-vertical GaN-based p^+-n Diode with CF_4-plasma and *in-situ* TMGa pretreatments

Qi Shu[1,*], Aleksandar Ivanov[1], Yao Ma[1], Arno Kirchbrücher[1], Arne Debald[2], Michael Heuken[1,2], Holger Kalisch[1] and Andrei Vescan[1]

[1] RWTH Aachen University Compound Semiconductor Technology, Sommerfeldstraße 18, 52074 Aachen, Germany
[2] AIXTRON SE, Dornkaulstraße 2, 52134 Herzogenrath, Germany
[*] Author to whom any correspondence should be addressed.

E-mail: shu@cst.rwth-aachen.de

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Abstract

This work reports on CF_4-plasma and *in-situ* TMGa treatments for the fabrication of etched-and-regrown quasi-vertical GaN p^+-n diodes. The regrown p^+-n diodes can suffer from high reverse leakage currents and premature breakdown directly related to electrically active states in the p–n junction region. The CF_4-plasma treatment prior to p-GaN regrowth effectively reduces leakage currents and improves breakdown voltage. However, CF_4-plasma treatment alone parasitically increases device resistance and limits the on-current. An additional *in-situ* TMGa preflow treatment prior to p-GaN regrowth is applied, restoring the forward characteristic. Using the combined CF_4-plasma and *in-situ* TMGa treatments prior to p-GaN regrowth, unetched planar-regrown p–n diodes with 2 μm n^--GaN drift layer achieve a breakdown voltage of −360 V, corresponding to a critical electric field of 1.9 MV cm^{-1}, close to that of continuously grown reference diodes (2.2 MV cm^{-1}). For etched-and-regrown p^+-n diodes with a 4 μm n^--GaN drift layer, the median breakdown voltage is improved to approximately −450 V, compared with approximately −150 V for the untreated reference.

1. Introduction

GaN-based vertical electronic devices hold great promise for high-power applications owing to a wide bandgap of 3.4 eV and a critical electric field of approximately 3.3 MV cm^{-1} [1, 2]. In many devices with (quasi-)vertical architecture, such as Junction-Barrier-Schottky (JBS) diodes and vertical Junction Field-Effect Transistors (vJFETs) (figure 1), a reverse biased lateral p^+-n junction is required in the off-state. Due to asymmetric doping, its depletion region mainly extends into the lightly doped n^-GaN drift regions, as illustrated in gray in figures 1(b) and (e). A widely adopted approach to realize such lateral p^+-n junctions in vertical GaN devices is etch-and-regrowth [3–6]. Schematically illustrated in figure 2, this technique starts with an as-grown n^-GaN template. A defined area on the n^-GaN surface is recessed to a specific depth (i.e. the vertical length of the p–n junction), followed by a p^+-GaN regrowth process to fill the etched region and form the p–n junction (lateral and vertical) with the adjacent n^-GaN.

However, p–n junctions with regrown p-GaN are usually of inferior quality compared to continuously grown ones. During recessing, reactive-ion etching (RIE) using BCl_3 or Cl_2 [7, 8] predominantly generates nitrogen vacancies in the n^-GaN surface [9]. Etch mask processing and removal as well as the exposure of the sample to ambient air prior to p-GaN regrowth inevitably leave residues and contamination on the surface. Such impurities are incorporated at the regrowth interface, further contributing to the electrically active defect density in the high-field region of the device. Fu *et al* reported substantial Si, O, and C concentrations at the regrowth interface of p–n diodes, as confirmed by secondary ion mass spectrometry (SIMS) [7]. Both impurity incorporation and etch-induced damage facilitate trap-assisted tunneling (TAT) currents through the p–n junction which are relevant especially under reverse bias. This is severely limiting the blocking properties of the diode [7, 8]. Extensive research has been devoted to

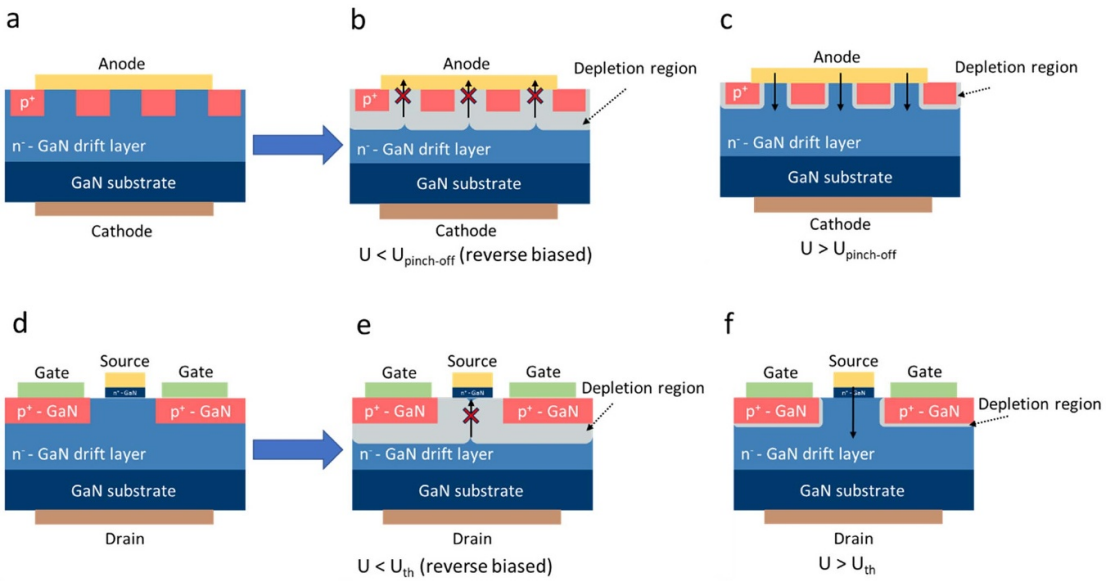

Figure 1. Schematics and operation mode of vertical JBS diode and vJFET. (a) and (d), layer structures, (b) and e: off-state with expanded depletion regions in gray, (c) and (f), on-state with minimal depletion regions. Depletion of p^+-GaN can be neglected due to asymmetric doping.

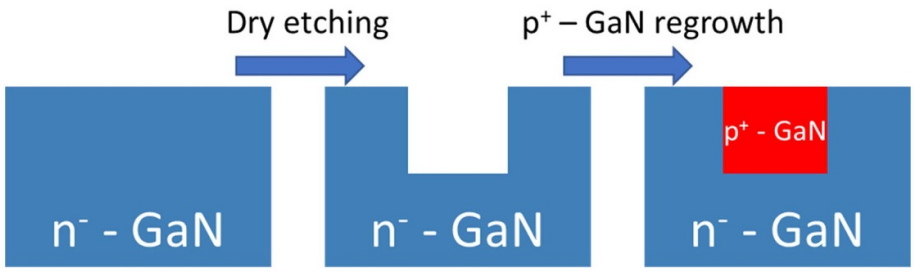

Figure 2. Etch-and-regrowth to realize a lateral p–n junction (including a vertical one).

mitigating these issues through various surface conditioning techniques, including plasma treatments using N_2/NH_3 or CF_4 [10–12], thermal annealing [13],and wet-chemical treatments using hot TMAH or AZ400K solutions [3, 4, 14].

A CF_4-plasma has been reported to be effective in the removal of impurities on the n^-GaN surface before the p-GaN regrowth [3, 15, 16]. In our previous study, we have employed Schottky diodes on CF_4-plasma-treated n-GaN as test vehicles to confirm the reduction of metal-semiconductor interface states resulting from proceeding etching processes and sample handling and processing [12]. However, CF_4-plasma treatment is known to leave nonvolatile fluorinated residues on the GaN surface. These are subsequently buried during regrowth, leading to an increased F concentration at the p–n junction interface [17]. Organic species such as triethylaluminum (TMAl) or dimethylaluminum chloride (DMAC) have been demonstrated to effectively remove fluorine-containing residues through ligand-exchange reactions between methyl groups and F atoms at elevated temperatures in some reported studies [18–21]. However, these metal-organic compounds themselves can introduce new species to the GaN surface, such as Al and Cl. In this work, a trimethylgallium (TMGa) exposure prior to the p^+-GaN regrowth in the metal-organic vapor phase epitaxy (MOCVD) reactor is proposed. At 400 °C, TMGa provides pyrolyzed methyl groups similar to TMAl and DMAC, but does not add additional chemical species to the process. As this *in-situ* treatment can be applied directly before the start of p^+-GaN deposition in the MOCVD chamber, adsorbed Ga atoms can be considered as benign and further oxidation or contamination can be excluded.

In this work, quasi-vertical trench-structured p–n diodes were fabricated using the etch-and-regrowth technique, as shown in figure 3. These devices are now used as test vehicles to investigate the quality of

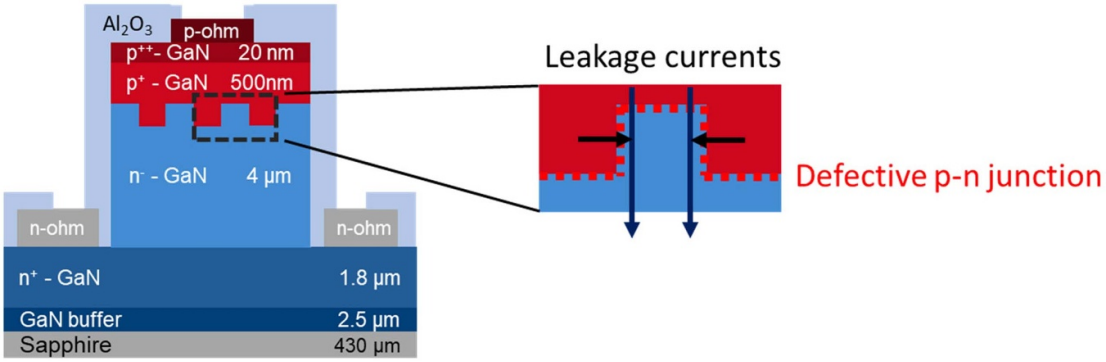

Figure 3. Schematic view of the quasi-vertical trench-structured p–n diode and the leakage current paths facilitated by etch-induced damage and incorporated impurities introduced during the growth interruption.

Table 1. Overview of all wafers with information of the etching and pre-regrowth treatment.

Nr.	p–n junction	Drift layer thickness (μm)	n$^-$GaN etching	CF_4-plasma	*In-situ* TMGa
R1	Continuously-grown	2			
R2	Regrown	2			
P1	Regrown	2		✓	
P2	Regrown	2		✓	✓
T1	Regrown	4	✓		
T2	Regrown	4	✓	✓	✓

regrown p–n junctions. Defective p–n junctions would result in high reverse leakage currents and premature breakdown. By analyzing the performance of the etched-and-regrown p–n diodes with and without CF_4-plasma treatment, as well as the specific difference of the diode characteristics after treatment with TMGa, the effectiveness of the combined CF_4-plasma and *in-situ* TMGa treatments in suppressing leakage paths associated with growth interruption and etching can be assessed. This knowledge can be directly applied to the fabrication of other vertical electronic devices which require enhanced high-voltage performance or current-guiding features such as JBS, JFET or current aperture vertical electron transistors (CAVET).

2. Experiments and devices

For device fabrication and characterization, six p^+-n diode wafers with different growth and processing schemes were fabricated. To distinguish and study the impact of a growth interruption with atmospheric exposure, etch steps and treatments, one continuously grown reference wafer R1 and one reference wafer R2 featuring just a growth interruption (with atmospheric exposure but no etching or pre-regrowth treatment step) were fabricated. P1 and P2 are planar regrown diode structures with CF_4-plasma treatment alone (P1) and an additional *in-situ* TMGa exposure step (P2), respectively. (A TMGa-only pre-treatment was not investigated in this work.) A recess by trench etching was only applied to T1 and T2 with T1 being untreated before regrowth and T2 experiencing the full conditioning program. Because CF_4-plasma treatment alone strongly limited the diode on-current, as discussed later in the Results and Discussion section, a CF_4-only treatment was not further investigated for the etched structures.

To give an overview, all samples are listed in table 1. Sample and processing details will be introduced in the following. R1, the reference for all regrowth experiments, is a continuously grown p–n diode wafer using a standard growth process on sapphire substrate with a 0.2° offcut toward the m-plane, using an AIXTRON CCS multi-wafer MOCVD system with conventional precursors TMGa and NH_3 in H_2 carrier gas. After unloading from the MOCVD reactor, the wafers were stored under cleanroom ambient conditions. Wafer R1 nominally features the same layer stack and approximately identical doping concentrations as all remaining wafers to be discussed below.

For the growth processes with interruption, several template wafers with a layer stack consisting of a 1.8 μm heavily doped n^+-GaN current-spreading layer ($N_D > 1 \times 10^{18}$ cm^{-3}) and on top an either 2 μm or 4 μm thick lightly doped n$^-$GaN drift layer were employed (previously fabricated in the CCS MOCVD reactor and stored under ambient atmosphere). The apparent net doping concentration of

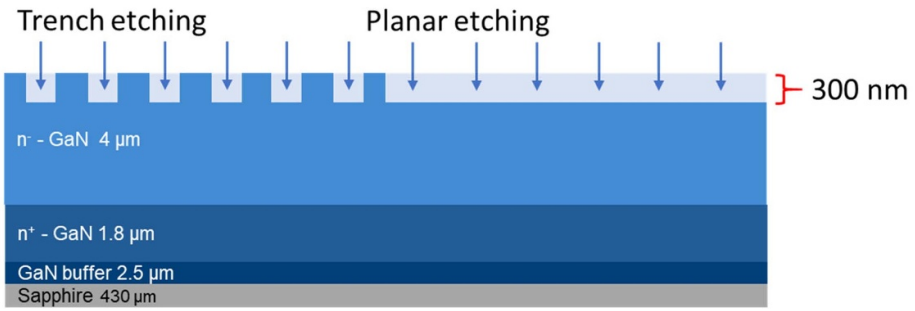

Figure 4. Schematic view of recess etching of wafers T1 and T2.

the lightly doped n^-GaN drift layer determined from capacitance–voltage (C–V) measurements on each wafer ranged from 5×10^{15} to 9×10^{15} cm^{-3},as discussed further below in the manuscript.

For comparison, another reference wafer (R2) was fabricated. In contrast to the continuously grown reference sample R1 (CCS reactor), wafer R2 is based on the same CCS-grown template as P1 and P2 (see below) and was regrown with the p^+-GaN/p^{++}-GaN stack under the same conditions of wafer P1 and P2 in an AIXTRON 200/4 RF-S reactor. However, wafer R2 experienced no treatment before regrowth.

For samples P1 and P2 (without prior recess-etching), the surface of two template wafers with 2 μm drift layers was directly treated by CF_4-plasma using a gas mixture of $CF_4/O_2 = 45/5$ sccm at 1 Pa with RF/ICP powers of 25/0 W. In this process, the plasma was generated by the capacitively coupled RF source with a self-bias voltage of −65 V, while the inductively coupled plasma (ICP) source remained off. This power setting targeted to remove accumulated surface contamination by applying a very soft ion bombardment and removed approximately 25 nm of GaN over a 2 h treatment, as confirmed by a calibration sample. Following the CF_4-plasma step, the wafers were immediately transferred to the glovebox of the AIXTRON 200/4 system to minimize recontamination. Wafer P1 was first held at 400 °C for 10 min in N_2 (the same condition as for the following *in-situ* TMGa treatment on P2). Then, 500 nm of p^+-GaN ($N_A > 1 \times 10^{19}$ cm^{-3}) and an additional ∼20 nm p^{++}-GaN cap layer ($N_A > 1 \times 10^{20}$ cm^{-3}) were regrown using magnesocene (Cp_2Mg) as precursor. Both layers were deposited under the conditions of 890 °C and 200 hPa and H_2 as carrier gas. This low-temperature process was chosen to suppress Mg diffusion into the n^-GaN beneath [22]. The precursor flows were set to be $TMGa/Cp_2Mg/NH_3 = 0.04$ mmol· min^{-1}/0.24 μmol· min^{-1}/45 mmol· min^{-1} for p^+-GaN and 0.04 mmol· min^{-1}/0.65 μmol· min^{-1}/45 mmol· min^{-1} for p^{++}-GaN, respectively.

On wafer P2, an additional TMGa preflow of 100 sccm in N_2 was introduced during the holding time at 400 °C reactor temperature, aiming to remove fluorinated residues from the preceding CF_4-plasma treatment. TMGa is known to decompose at around 400 °C with < 5% pyrolyzed methyl groups [23]. Without unloading, the reactor was subsequently set to GaN growth conditions, and the same p^+-GaN/p^{++}-GaN stack as for wafer P1 was deposited.

For the investigation of damage induced by BCl_3-based recess etching, two wafers T1 and T2 with a 4 μm n^--GaN drift layer were selected. Prior to regrowth, the wafer surface was patterned by photolithography in the form of ∼300 nm deep long trenches with 5 μm width and 5 μm distance. Etching was performed in an ICP-RIE tool using BCl_3/Ar (10/10 sccm) under ICP/RF powers of 60/50 W at 1 Pa for 10 min. In addition to the trench-patterned regions, some areas on the wafers were not covered with photoresist, allowing to study the impact of planar etching of the wafer surface. Up to this point, both trench wells and (blanket recessed) planar region were identically produced on both wafers T1 and T2 as illustrated in figure 4. After etching, wafer T1 was directly transferred into the 200/4 MOCVD system. The same p-GaN layer stack as for samples P1, P2 and R2 was regrown directly on the etch-damaged surface. For wafer T2, combined CF_4-plasma and *in-situ* TMGa treatments as described above were applied before regrowth. Details of surface etching and pre-regrowth treatments for wafers T1 and T2 are also listed in table 1.

X-ray diffraction (XRD) rocking-curve measurements were performed on wafers P1, P2, R1, R2. The full width at half maximum (FWHM) values of the GaN (002) and (102) peaks and the edge/screw dislocation densities calculated according to an equation given by Moram [24] are given in table 2. The different treatments did not lead to an obvious change of the dislocation density after the regrowth.

Table 2. FWHM values and correspondingly estimated dislocation densities obtained from the rocking curve measurements on XRD.

	Before regrowth	P1	P2	R1	R2
FWHM (002) (arcsec)	267	280	268	273	267
FWHM (102) (arcsec)	553	487	663	550	596
Edge dislocation density (cm^{-2})	1.3×10^9	8.6×10^8	2.0×10^9	1.2×10^9	1.5×10^9
Screw dislocation density (cm^{-2})	1.4×10^8	1.6×10^8	1.4×10^8	1.5×10^8	1.4×10^8

Diode fabrication commenced with mesa isolation. A SiO_2/Ti/Ni (300/10/200 nm) etch mask was deposited and patterned into a circular form with a diameter of 200 μm. The top Ni layer features a solid etch resistance during mesa etching. The Ti layer serves as an adhesion layer for Ni on SiO_2. The underlying SiO_2 layer facilitates etch-mask removal in BOE. To expose the bottom n^+-GaN layers on all wafers, mesa etching was performed in an ICP-RIE system using $Cl_2/BCl_3/Ar$ (21/8/5 sccm) under ICP/RF powers of 200/300 W. Wafers P1, P2, R1 and R2 (2 μm drift layer thickness) were etched for 330 s, yielding an etch-depth of 2.7 μm. In analogy, wafers T1 and T2 (4 μm drift layer thickness) were etched for a prolonged time of 570 s with an etch depth of 4.8 μm. Ohmic contacts were deposited by e-beam evaporation: Ti/Al/Ni/Au (20/100/40/50 nm) for n-type contacts and Ni/Au (20/20 nm) for p-type contacts. The n-ohmic contacts were annealed at 600 °C for 5 min in N_2, while the p-ohmic contacts were annealed at 535 °C in air for 10 min (inevitably also affecting the n-ohmic contacts). Specific contact resistances of 4.7×10^{-6} $\Omega{\cdot}cm^{-2}$ (n-ohmic) and 1.9×10^{-5} $\Omega{\cdot}cm^{-2}$ (p-ohmic) were measured using the circular transfer length method (CTLM). Finally, a 50 nm Al_2O_3 passivation layer was added by atomic layer deposition (ALD). The Al_2O_3 coating over the contacts was removed by photolithographic patterning followed by ICP-RIE etching with BCl_3/Ar (12/4 sccm) at ICP/RF powers of 200/100 W and 0.3 Pa for 90 s. The side and top views of the diodes are schematically shown in figures 5(a)–(e), and representative optical microscopy images are given in figures 5(f) and (g).

The fabricated diodes were characterized using *C–V* measurements and current–voltage (*J–V*) measurements. The *C–V* measurements were performed over a voltage range from −2 to 2 V with a step size of 0.1 V at an AC frequency of 1 MHz. *J–V* characteristics were measured separately under forward and reverse bias conditions. Under forward bias, the voltage was swept from 0 to 8 V with a step size of 0.02 V until the compliance current of 0.1 A was reached. Under reverse bias, the voltage was first swept from 0 to −100 V with a step size of −1 V. Breakdown measurements were conducted from 0 V with a step size of 1 V until destructive breakdown occurred. The compliance current was set to 0.01 A. The measurement was performed at room temperature under ambient air condition.

3. Results and discussion

This chapter is structured as follows. First, planar diodes fabricated on P1, P2, R1, and R2 are discussed to analyze the impact of atmospheric exposure before regrowth on the performance of regrown p–n diodes, as well as the effectiveness of the various treatments introduced in the previous chapter. Then, etch-damage mitigation achieved by these treatments is examined using diodes fabricated on T1 and T2 with etched n^-GaN surfaces. (For simplicity, diodes on the respective wafers will be also referred to as P1, P2, R1, R2, T1, and T2.)

3.1. Planar p–n diodes P1, P2, R1 and R2 with various pre-regrowth treatments

The planar diodes were firstly characterized by *C–V* measurements. The resulting $1/C^2$ curves are presented in figure 6(a). Except for R2, which experienced atmospheric exposure, but no treatment before p-GaN regrowth, all diodes exhibit a linear $1/C^2$ characteristic. Their built-in voltages were extracted using linear extrapolation to the *x*-axis, yielding values of 3 ± 0.1 V, in good agreement with the theoretical value of around 3.0 V for GaN p–n junctions [25]. However, the non-linear behavior of R2 in the $1/C^2$ curve does not allow for an extraction of the built-in voltage. Under the assumption of a one-sided abrupt junction ($N_A > 1 \times 10^{19}$ cm^{-3} vs $N_D < 1 \times 10^{16}$ cm^{-3}), an apparent net charge concentration in the n^-GaN layers was extracted from the *C–V* measurements, as plotted in figure 6(b). It should be noted that the extracted doping concentration values of regrown diodes are influenced by the non-abrupt junction, including effects from interfacial states, traps and fixed charges. For R2, the non-linear $1/C^3$ behavior leads to an apparently high near-interface charge concentration exceeding 2×10^{18} cm^{-3}. This value indicates the presence of a high density of donor-like states at the p–n interface. Despite the absence of direct chemical evidence, this behavior implies electrically active impurities or defect states

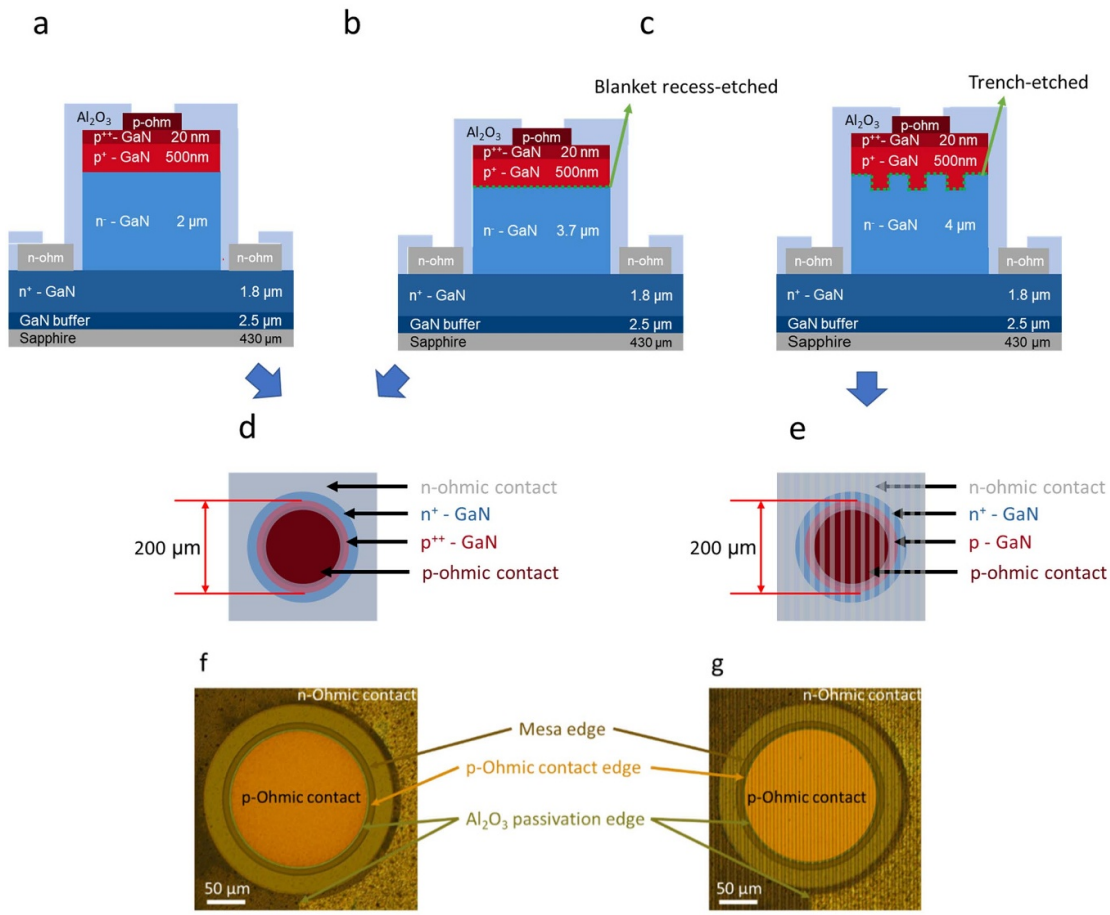

Figure 5. Schematics of the various types of diodes. (a): Side-view of the diodes on P1, P2, R1 and R2. (b): Diodes with blanket recessed n$^-$GaN surface on T1 and T2. (c): Diodes with n$^-$GaN etched in trench-form on T1 and T2. (d): Top view of the planar diodes shown in images a and b. (e): Top view of the trench-etched diodes in image c. Optical microscopic images of (f): planar diodes and (g): trench-etched diodes.

introduced during atmospheric exposure. Furthermore, it should be noted that the calculated depth of the depletion region in n$^-$GaN of R2 in figure 6(b) is incorrect. For sample R2, N_A and N_D (close to the regrowth interface) are of the same order of magnitude, and the assumption of a depletion zone present only in the n-region does not hold. After CF_4-plasma treatment, non-linear $1/C^2$ curves and the high density of states near the p–n junction were no longer observed. This is indicative of the depletion region only extending into the n-drift region. Wafers P1 and P2 showed homogeneous doping levels around 5–9 $\times$ 10^{15} cm^{-3} (very close to that of wafer R1).

J–V measurements were performed for the p–n diodes on wafers P1, P2, R1 and R2 (forward direction shown in figure 7(a)). At low forward voltages ($V < 2.5$ V), all regrown diodes (P1, P2, and R2) exhibited higher current densities J_P than the continuously grown reference diode R1, with the trend (extracted at 2 V) $J_{R2} > J_{P1} > J_{P2} > J_{R1}$. These elevated sub-threshold leakage currents indicate parasitic conduction, likely associated with TAT or a hopping-type transport mediated by defects or impurities at the regrowth interface [25]. The maximum leakage current is found for R2, shown in orange in figure 7(a), and correlates well with the suspected largest impurity density at the regrown GaN interface (as it was previously detected in the *C–V* measurement discussed above). The reduced leakage currents of the diodes P1 and P2, shown in green and black in figure 7(a), respectively, demonstrate an effective reduction of this parasitic contribution.

In the large forward voltage range ($V > 2.5$ V), the steeper increase in current density was likely caused by a more dominant thermionic emission (TE) conduction. The turn-on voltages, representing the start of dominant TE current flow, were extracted using linear extrapolations of *J–V* curves in linear scale, as presented in figures 7(b) and (c). For the diodes P2, R1 and R2, the turn-on voltages were extracted to be 3.0 $\pm$ 0.2 V, very close to their built-in voltages derived from *C–V* measurements. However, the turn-on voltage for the diodes P1, which were treated only by CF_4-plasma, was extracted to be 4.5 V, higher than its built-in voltage obtained from the *C–V* characterization. This value is even

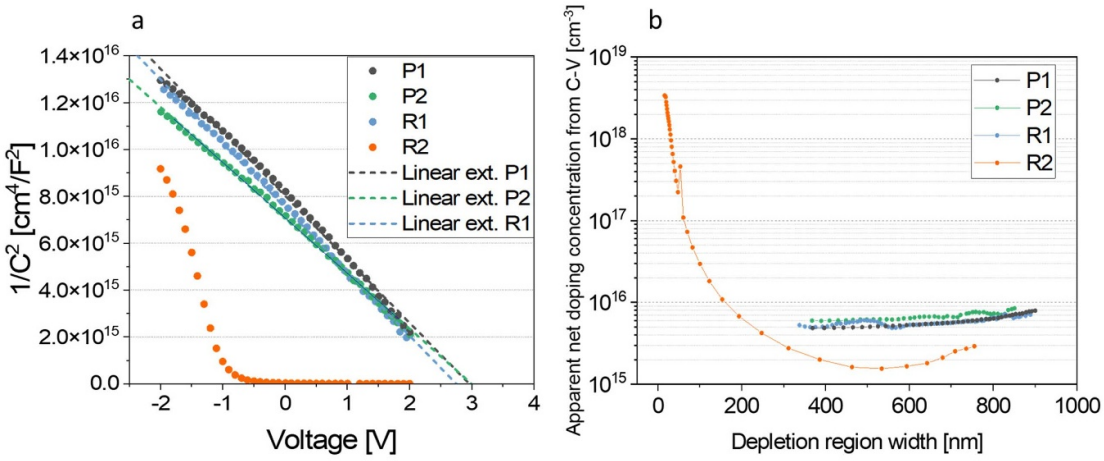

Figure 6. (a) $1/C^2$ vs bias voltage plots of the diodes P1, P2, R1 and R2. The dashed lines represent the linear fit of the $1/C^2$ curves with extrapolation to the x axis yielding the built-in voltage. (b), The apparent net doping concentrations as a function of the (apparent) depletion region widths of the diodes P1, P2, R1 and R2 extracted from the C–V plots.

significantly exceeding the limits set by the bandgap of GaN of 3.4 eV^{-1}. Furthermore, the current density in the on-state of the diodes P1 was clearly lower than those of P2, R1 and R2. The on-resistance of the diodes was calculated from the *J–V* curves and box-plotted with 10 diodes on each wafer, shown in figure 7(d). The diodes P1 exhibited a median on-resistance of 566 $m\Omega{\cdot}cm^{-2}$,much higher than those of the continuously-grown reference R1 and the untreated regrown reference R2 of 4.43 $m\Omega{\cdot}cm^{-2}$ and 4.16 $m\Omega{\cdot}cm^{-2}$,respectively, as well as higher than those of typical GaN p–n diodes reported in the literature [3, 4, 13, 26–29]. In sum, the deviating *J–V* performance of the diodes P1 is probably caused by a thin insulating compound between the n- and p-sides of the p–n junction. As explained above, this barrier may be related to a highly fluorinated interfacial layer (e.g. GaF_x [17]), formed during the long CF_4-plasma treatment. Evidently, the *in-situ* TMGa treatment of the diodes P2 reduced the on-resistance by about two orders of magnitude to 4.86 $m\Omega{\cdot}cm^{-2}$ and restored the on-current close to that of the reference R1. Although the chemical composition of the interface was not directly investigated, the recovery of the forward characteristics after the TMGa preflow is consistent with an assumed reduction of a CF_4-induced interfacial barrier, possibly related to fluorinated residues.

The ideality factor was calculated using the equation $n = q\ (\ln\ (10) \times m \times k \times T)$ from the TE model $I = I_0\ (e^{\ q\ (V-Ir)/nkT-1}$[30], where I_0 is the reverse saturation current, q is the elementary charge, r is the series resistance, k is the Boltzmann constant, T is the temperature, and m is the slope of the exponential region in the *J–V* curve calculated by the derivative $d\ (\log\ (I))/d\ (V)$. A box plot with the ideality factors from 10 diodes on each wafer is shown in figure 7(e). The continuously-grown reference diode R1 presented a median ideality factor of 2.10, the best among all. An ideality factor approaching 2 is widely attributed to Shockley-Read-Hall recombination and often observed in vertical GaN p–n diodes with thick n^-GaN drift layer [31, 32]. Without any treatments, the diodes on the regrown wafer R2 feature a higher median ideality factor of 2.79, under the assumption that a considerable higher fraction of the current was contributed by impurity-related leakage, largely deviating from the ideal TE characteristics. After CF_4-plasma treatment, the ideality factor of the diodes on P1 remained high, with a median value of 2.91. The high ideality factor was related to limited TE current flow due to the suspected fluorinated barrier layer, as discussed above. After further treatment with *in-situ* TMGa, the median ideality factor of the diodes P2 was clearly improved to 2.37, closer to that of the continuously-grown p–n diodes R1. The restored ideality factor aligned well with results of the improved on-current.

The *J–V* characteristics in the reverse-bias region, measured down to −100 V, are presented in figure 8(a). Without any pre-regrowth treatment, the leakage current of the diodes R2 increased steeply to 2×10^{-3} A cm^{-2} at −8 V and reached 6×10^{-2} A cm^{-2}at −100 V, much higher than that on the continuously-grown diodes R1 (with a leakage current of $\sim 1 \times 10^{-5}$ A cm^{-2} at −100 V). This elevated reverse leakage indicates a pronounced contribution from electrically active defects or impurities introduced during the growth interruption. With the low-power CF_4-plasma treatments, the leakage current was consistently reduced to 1×10^{-3} A cm^{-2} for P1 and 3×10^{-3} A cm^{-2} for P2 at −100 V, consistent with a reduction of impurity- or defect-related leakage contributions after the CF_4-plasma treatment.

As the reverse bias increased, most diodes on R2 exhibited destructive breakdown between -200 and −230 V with a median value of −213 V (see box plot in figure 8(b) with the absolute values of the

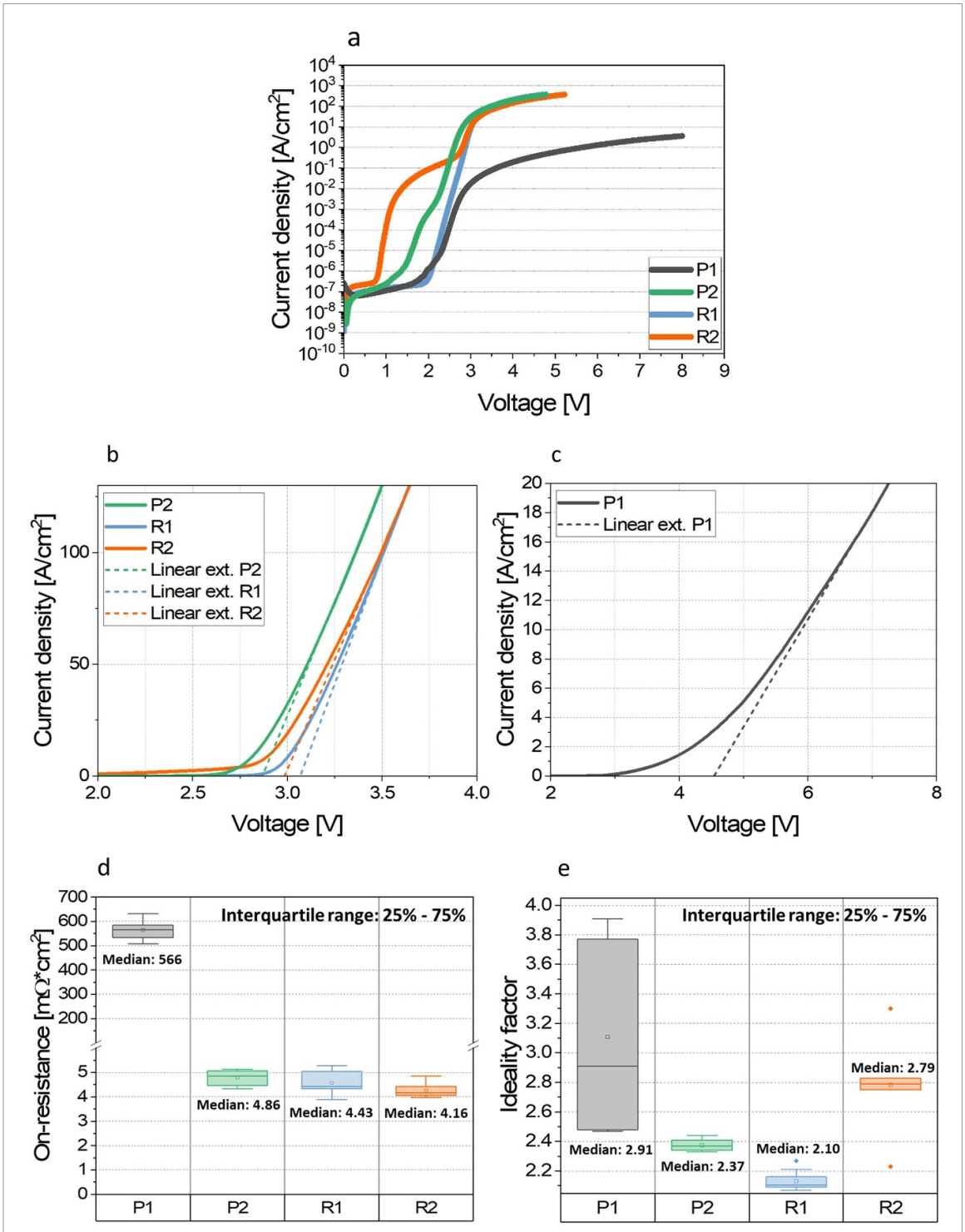

Figure 7. (a): Semi-log J–V plot of the diodes P1, P2, R1 and R2. (b), Solid lines are the linear J–V plots of the diodes P2, R1 and R2, dashed lines are the linear fits of the J–V curves, (c), Solid line is the linear J–V plot of the diodes P1, dashed line is the linear fit of the J–V curve, (d), Box plot of the on-resistances of the diodes P1, P2, R1 and R2, each containing 10 diodes for each wafer, (e) Box plot of the ideality factor of the diodes on P1, P2, R1 and R2, containing 10 diodes for each wafer.

breakdown voltage on the *Y* axis). As illustrated in the SEM images in figure 8(c), breakdown appears to have occurred through the diode bulk. In contrast, the diodes with continuously-grown p-GaN on R1 feature a doubled breakdown voltage of −410 V in median. It corresponds to a critical electric field of 2.2 MV cm^{-1}, calculated using the punch-through equation [33], which assumes complete depletion of the drift region:

$$E_C = \frac{-V_{BR}}{t_{drift}} + \frac{qN_D}{2\varepsilon_r\varepsilon_0} t_{drift} \quad (1)$$

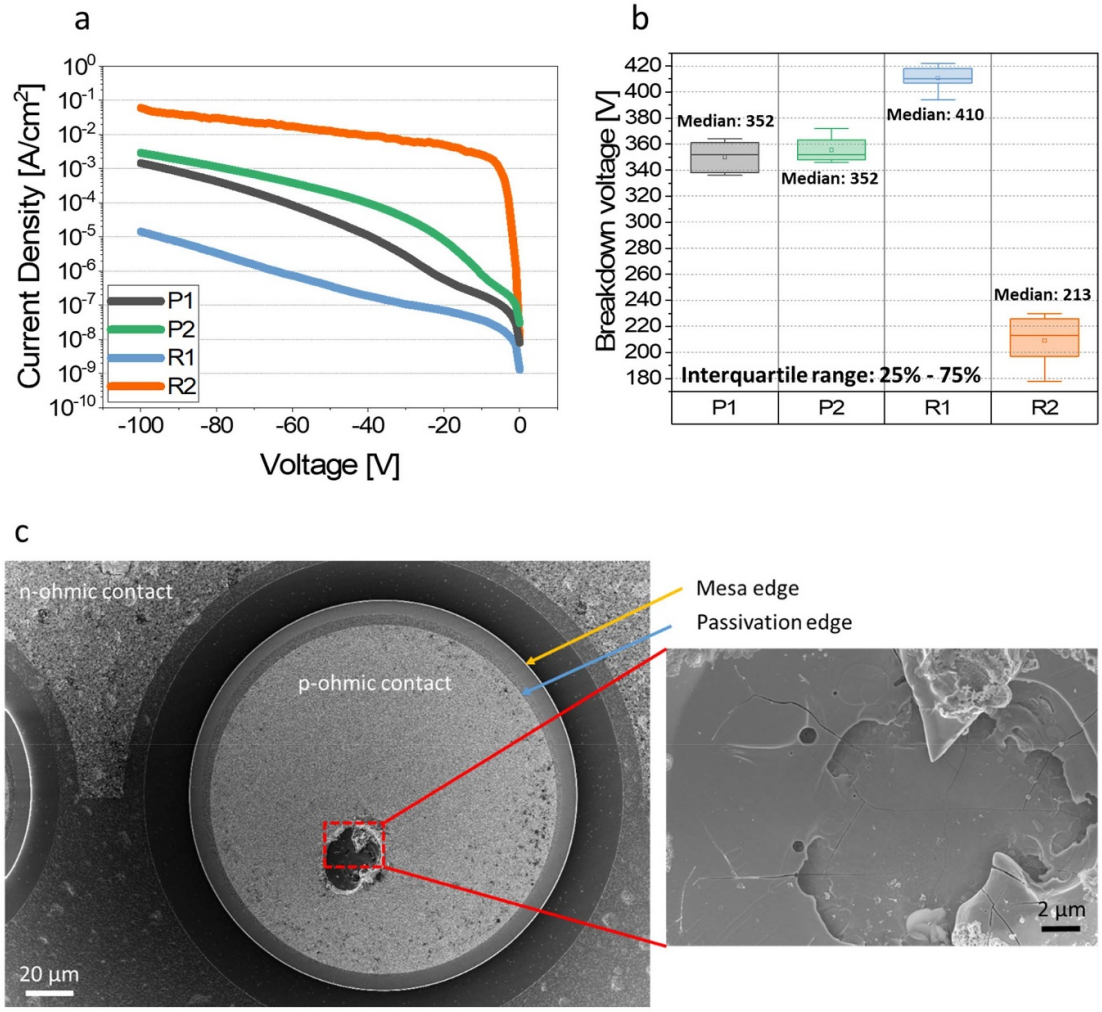

Figure 8. (a): Reverse J–V characteristics of the diodes P1, P2, R1 and R2 measured from 0 to −100 V, (b), box plot of the breakdown voltage of the diodes P1, P2, R1 and R2, containing 10 diodes for each wafer, (c): SEM images of the destructive breakdown through the diode bulk.

where $\varepsilon_r = 10.6$ [34] is the relative permittivity of GaN, ε_0 is the vacuum permittivity, $t_{drift} = 2$ μm, and N_D is the net doping concentration (5×10^{15} cm^{-3} for wafer P1, taken from figure 6(b) at $V = 0$). For the R2 diodes, the breakdown behavior is likely limited by electrically active contamination or defect states at the regrown p–n junction. With the CF_4-plasma treatment applied, the median breakdown voltages for the diodes on P1 and P2 were largely improved to −352 V, corresponding to a critical electric field of 1.9 MV cm^{-1}. The positive effect of the pre-regrowth treatment is indicated by the breakdown field values of the regrown p–n diodes approaching those of the continuously-grown ones. Both achieved critical fields are competitive among GaN p–n diodes grown on foreign substrates such as sapphire and Si. [16, 26–28, 35, 36].

3.2. Etched-and-regrown p–n diodes

The etched-and-regrown p^+-n diodes T1 and T2 were first characterized using C–V measurements. The $1/C^2$ curves and the extracted apparent charge profiles are shown in figure 9. The extracted apparent concentration on wafer T1 was very high near the p^+-n junction region, approximately 7×10^{16} cm^{-3} and 2×10^{17} cm^{-3} for the planar (unmasked areas) etched diodes ('pla') and the trench-etched ones ('trench'), respectively. The high apparent near-interface concentrations in these diodes are likely associated with etch-induced damage. For wafer T2, the apparent near-interface concentration derived from the C–V measurements was reduced compared with T1. In analogy with P2, this result suggests that the combined CF_4-plasma and TMGa treatment reduced the electrically active interface states caused by the BCl_3-based ICP-RIE, although direct chemical evidence is not available in this work. For blanket recessed diodes ('pla'), the $1/C^2$ characteristics became linear with no elevated apparent concentration near the p–n junction, plotted in blue color in figure 9(b). The trench-etched diodes ('trench') on

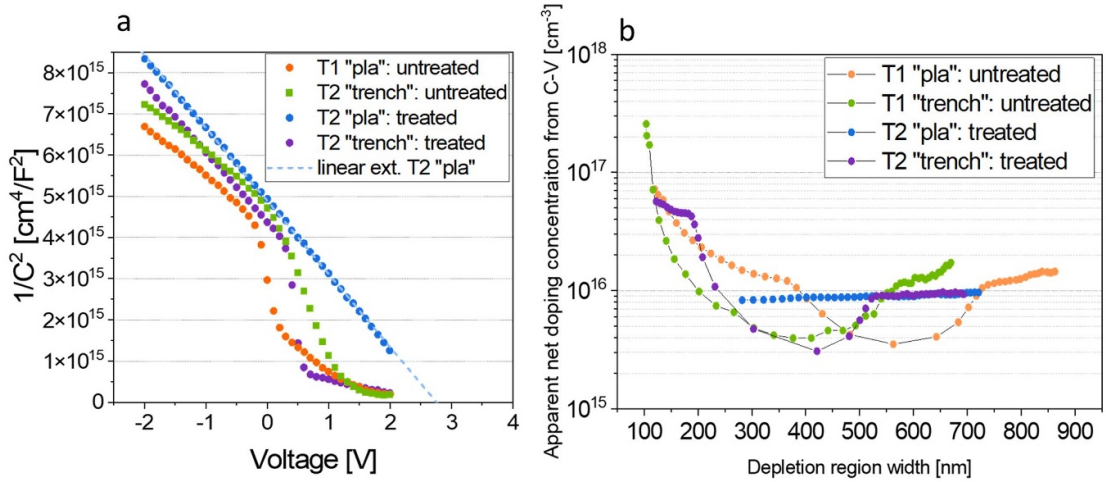

Figure 9. (a) $1/C^2$ plot from C–V measurement. (b): Apparent net doping concentration as a function of (apparent) depletion-region width derived from C–V measurements.

T2 still exhibited a high apparent near-interface charge concentration near the p–n junction (around 6×10^{16} cm^{-3}), but it was reduced by one order of magnitude compared to the trench-etched diodes 'trench' on T1. Compared with the purely planar *c*-plane-etched surfaces on blanket recessed diodes 'pla', trench etching exposed nonpolar a-/m-plane facets. Due to their different atomic surface configurations and dangling-bond-related defect formation, non-polar sidewalls are more susceptible to plasma-induced structural damage and the generation of a high density of interface states [37]. In our previous study with trench-etched Schottky diodes, these residual defects on non-polar planes have proven difficult to be fully removed by post-etch treatments [12]. These defects at the regrowth interface are expected to dominate the leakage of regrown trenched p–n diodes.

J–V measurements were performed on diodes with blanket recessed and trench-etched diode on both T1 and T2. For all devices, current density was normalized to the circular p-contact area, not to the actual regrown p–n junction area. The additional contribution of the trench sidewalls is estimated to be only 5.7% and is not accounted for here. However, the trench-device current density should still be regarded as a nominal current density. The curves are plotted in figures 10(a) and (b). On the untreated sample T1, a parasitic conduction path at voltages below the diode turn-on is most likely associated with the etch-damaged p–n junction interface, as the current density increased to 2×10^{-1} A cm^{-2} for the 'trench' diode, but only to 3×10^{-2} A cm^{-2} for the 'pla' diode, respectively. For reverse voltages, it reached 1×10^{-1} A cm^{-2} for the 'trench' diode and $2 \times 10^{\circ}$ A cm^{-2} for the 'pla' diode at −100 V, respectively. The higher leakage current in the 'trench' diodes compared with the 'pla' types might again be an indication of different etch-induced damage on the different GaN crystal planes, in analogy with the results from *C–V* measurements. Generally, the trench structure alters the electric field distribution, especially enhances the electric field at the trench corners [38], which could contribute to the higher reverse leakage current. After CF_4-plasma and *in-situ* TMGa treatments, the leakage currents for both the 'trench' and 'pla' diodes on T2 were reduced. Under forward bias, the parasitic leakage currents at 2 V were decreased to 5×10^{-4} A cm^{-2} for 'pla' diodes and 5×10^{-3} A cm^{-2} for 'trench' diodes, respectively. The reverse leakage current was suppressed below 1×10^{-2} A cm^{-2} for both 'pla' and 'trench' diodes, close to the leakage current of the unetched and planar regrown diodes P2. It should be noted that the P2 diodes have a thinner drift layer. Therefore, the absolute current densities of P2 and T2 cannot be compared quantitatively without considering the different drift-layer thicknesses, junction geometries, and electric-field distributions. In addition, the ideality factor was improved by the treatments. For the 'pla' diode, the ideality factor decreased from 2.8 to 2.4, while a more substantial improvement from approximately 18.8 to 3.2 was achieved for the 'trench' diode.

At high reverse voltages, the breakdown voltages were significantly improved. Without treatment, the 'pla' and 'trench' diodes experienced destructive breakdown at approximately −180 V and −120 V, respectively. The lower absolute breakdown voltage of the trench-etched diode is related to the etch damage on the sidewalls and the trench-corner electric field enhancement, as mentioned above. After CF_4-plasma and *in-situ* TMGa treatments, both types of diodes exhibited an improved breakdown voltage with the median values below −460 V, as shown in the box plot in figure 10(c) with the absolute

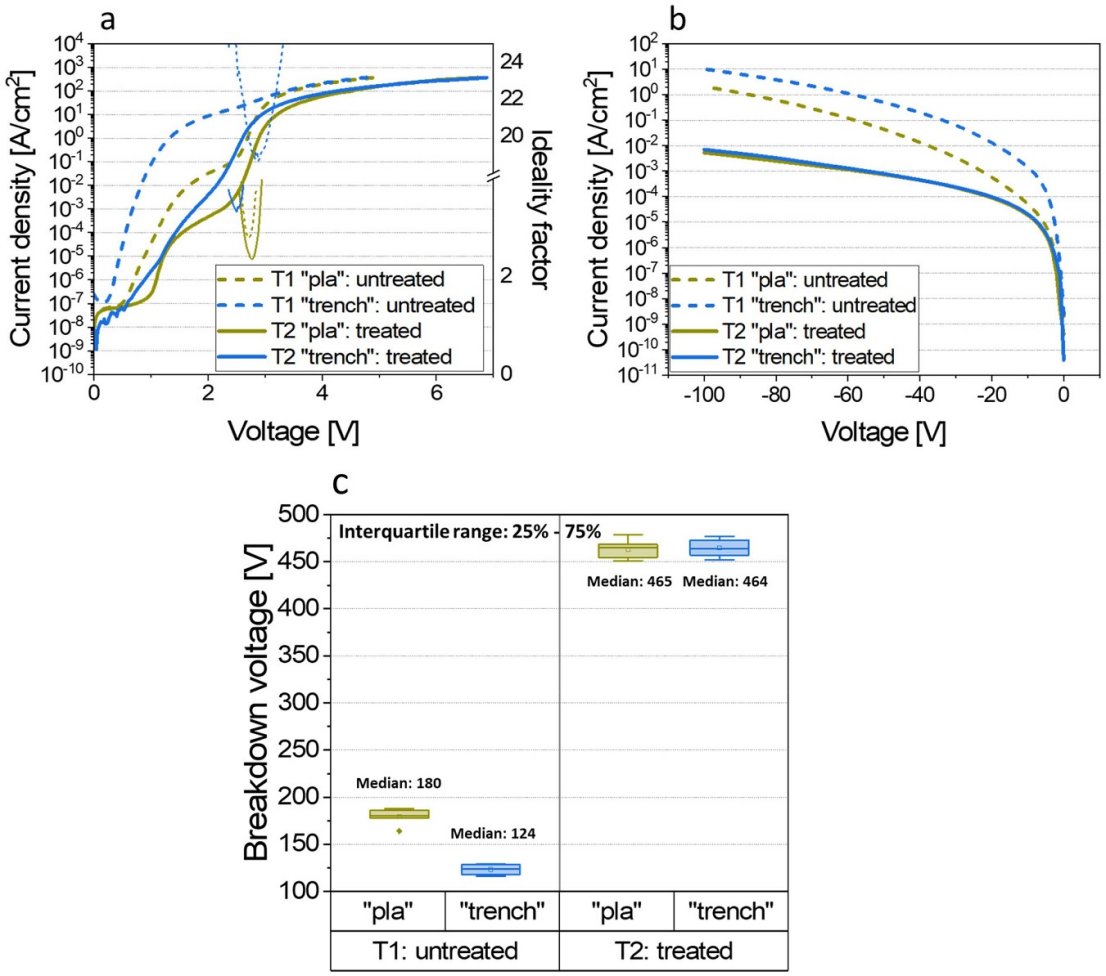

Figure 10. (a) Forward J–V characteristics with ideality factor plot. (b), Reverse J–V characteristics to −100 V. (c), Box plot of the breakdown voltage containing the data of 10 diodes for each type.

values of the breakdown voltages on the *Y* axis. The improved breakdown voltage is likely associated with the reduced leakage current related to etch damage and a possibly smaller field-enhancement due to smoothened trench corners. Previous studies have shown that CF_4-plasma can slowly etch GaN and modify the near-surface region while maintaining a smooth morphology [39]. Thus, minor surface-profile modification at exposed trench edges/corners cannot be excluded, although no pronounced corner rounding was observed in our samples. A modified trench corner could reduce the peak electric field and thereby contribute to the improved breakdown voltage [40]. As mentioned above, the electric field distribution is inhomogeneous in the trench structures, calculating of the maximum breakdown field based on the equation (1) is incorrect and hence not performed for these structures.

4. Conclusion

This work evaluates regrown p^+-GaN quasi-vertical GaN p^+-n diodes. The results indicate that impurity incorporation and etch-induced damage at regrowth interfaces can be major contributors to leakage currents and premature breakdown. CF_4-plasma treatment effectively reduces reverse leakage current but limits the on-current and increases the on-resistance. This can probably be attributed to the formation of a CF_4-induced interfacial barrier, possibly by fluorinated residues. A subsequent *in-situ* TMGa treatment restores forward conduction, suggesting a reduction of this CF_4-induced interfacial barrier. For etched-and-regrown structures, the combined treatment suppresses electrical degradation related to etch damage and enables improved high-voltage blocking behavior. In sum, CF_4-plasma treatment followed

by *in-situ* TMGa pretreatment is shown to be a practical and MOCVD-compatible interface-conditioning approach for high-performance regrown GaN p–n junctions.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Conflict of interest

The authors declare no conflict of interest.

Author contributions

Qi Shu 0009-0006-1463-0427
Conceptualization (lead), Data curation (lead), Formal analysis (lead), Investigation (lead), Methodology (lead), Resources (lead), Software (lead), Supervision (equal), Validation (lead), Visualization (lead), Writing – original draft (lead), Writing – review & editing (lead)

Aleksandar Ivanov
Data curation (equal), Formal analysis (equal), Investigation (equal), Methodology (equal), Resources (equal), Software (equal), Validation (equal), Visualization (equal), Writing – review & editing (supporting)

Yao Ma 0009-0005-2702-5472
Data curation (equal), Formal analysis (equal), Investigation (equal), Methodology (equal), Resources (equal), Software (equal), Validation (equal), Visualization (equal), Writing – review & editing (supporting)

Arno Kirchbrücher 0009-0003-0613-7016
Investigation (supporting), Methodology (supporting), Resources (supporting), Software (supporting), Supervision (supporting), Writing – review & editing (supporting)

Arne Debald 0000-0002-5631-2586
Data curation (supporting), Formal analysis (supporting), Investigation (supporting), Resources (equal), Visualization (supporting)

Michael Heuken 0000-0001-9739-9692
Funding acquisition (equal), Project administration (equal), Resources (equal), Supervision (equal)

Holger Kalisch
Conceptualization (equal), Funding acquisition (equal), Project administration (equal), Resources (equal), Supervision (equal), Writing – review & editing (equal)

Andrei Vescan 0000-0001-9465-2621
Conceptualization (equal), Funding acquisition (lead), Project administration (lead), Resources (lead), Supervision (lead), Writing – review & editing (equal)

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