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Reliability challenges for resistive random-access memory-based parallel logic computing

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Conventional computing architectures are reaching their scalability limits, while their energy demands increase rapidly. A bottleneck is the separation of memory and processing units, which requires a continuous data transfer. This memory wall increases the power consumption and limits the processing speed at the same time. Computing-in-Memory (CIM) has emerged as an alternative computing paradigm, where the data is processed directly within the memory array, thereby reducing data transfer costs. Emerging non-volatile devices such as magnetic-tunnel junctions (MTJ), phase-change memory (PCM), or resistive random-access memory (RRAM) are promising candidates for CIM. As re-programmable and highly scalable devices, they combine both computing and memory functionalities. While the feasibility of RRAM-based CIM has been proven, both in simulation and in experimental demonstrations, the operational reliability is still an ongoing issue. In this work, we demonstrate the parallel and cascading execution of logic functions in an RRAM-based CIM array. The experimental results are complemented by an in-depth simulation study to investigate the logic accuracy and optimization strategies. These results provide new insights into the reliability and logic correctness of resistive CIM and outline a potential path towards scalable and energy-efficient computing architectures.

The demand for computational power is rising steadily, driven by the advancements in data-intensive applications such as artificial intelligence and machine learning[1]. Conventional von-Neumann computing architectures rely on the physical separation of memory and processing units[2,3]. This requires a continuous data transfer between both parts during the operation, which leads to significant energy consumption and bandwidth limitations. Therefore, overcoming this von-Neumann bottleneck by combining memory and processing unit has become a central research topic[4,5]. Computing-in-memory (CIM) has emerged as a promising candidate in this regard. In CIM architectures, the memory unit is designed in a way that it performs a specific computational task directly without transferring the data to the processing unit[6]. While CIM can be implemented in CMOS-based SRAM structures, "beyond-CMOS" memory technologies are particularly interesting for CIM[7]. Examples for these emerging memories are magnetic-tunnel-junctions (MTJ), phase-change memory (PCM), or resistive random access memory (RRAM)[8–10].

RRAM devices or resistive switching devices consist of a thin insulating metal-oxide layer sandwiched between two metallic electrodes[11]. During an initial electroforming process, the stoichiometric arrangement of mobile ionic donors, e.g., oxygen vacancies, within the oxide is locally modified. This process leads to the formation of a conductive filament that connects the electrodes[12]. After electroforming, the RRAM resistance is predominantly determined by the concentration of mobile donors in the gap region between the filament tip and the electrode interface. Applying suitable voltages across the electrodes modulates this concentration (Fig. 1a). An increased concentration narrows the gap and reduces the device resistance, whereas a reduced concentration widens the gap and results in a higher resistance state[13]. The electrical resistance is an inherent analog quantity, yet for logic computing, digital values are preferred. Therefore, the continuous resistance range of RRAM devices is typically sampled into digital states. In the simplest binary mode, two resistance levels are defined: a low-resistance-state (LRS), assigned to logic "1", and a high-resistance-state (HRS), assigned to logic "1". In practical implementations, RRAM devices are rarely used in isolation. Instead, they are integrated in a one-transistor one-resistor (1T-1R) configuration in series with an n-MOSFET (Fig. 1b). The n-type transistor acts as an access element or selector within RRAM arrays, suppressing potential sneak-path currents[14]. Due to the improved operational reliability, the co-integration as a 1T-1R configuration has

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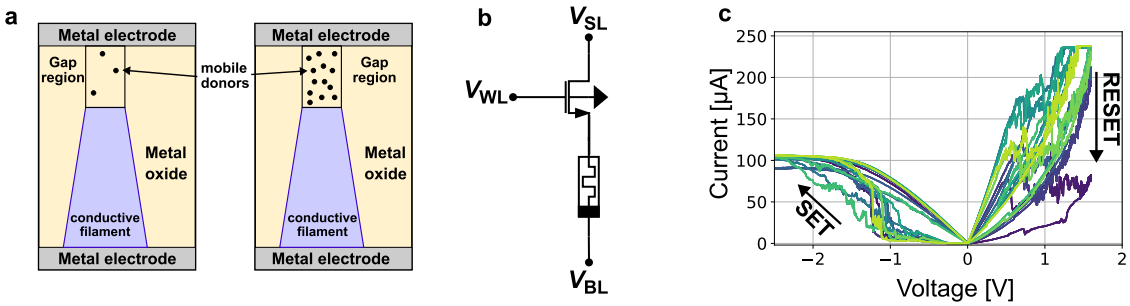


Fig. 1 | Schematic illustration of the RRAM device and its functionality. a The filamentary switching mechanism in an RRAM. The device consists of a metal-insulator-metal material stack. The filament and the gap region are formed during an initial electroforming step. A high donor concentration in the gap reduces the device resistance (low-resistive state, LRS), whereas a decreased concentration results in a higher resistance (high-resistive state, HRS). **b** Circuit diagram of a one-transistor one-resistor (1T-1R) RRAM cell for CIM. One electrode of the RRAM is connected in series with the drain of an n-MOSFET device. The voltage nodes are indicated as Word-Line (V_{WL}) at the transistor gate, Source-Line (V_{SL}) at the transistor source, and Bit-Line (V_{BL}) at the opposite RRAM electrode. **c** Exemplary current–voltage (I–V) characteristic from 1T-1R devices on the 130 nm test-chip. The data set consists of a single RESET-SET cycle measured for 10 different 1T-1R devices.

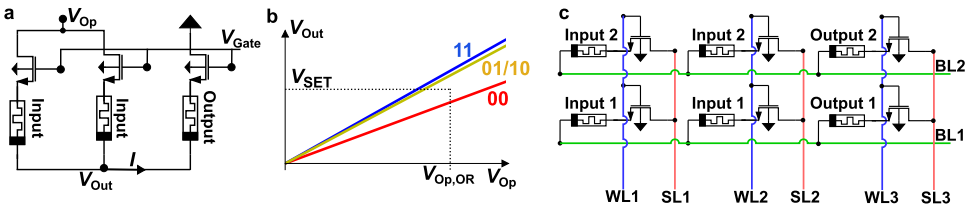


Fig. 2 | Operation principle of VCL. a The primitive circuit for a two-input, one-output VCL operation. During the operation, the access transistors are opened by applying a sufficiently high gate voltage, V_{Gate}. The operation voltage V_{Op} is applied at the inputs, while the output device is grounded. **b** The potential at the shared floating line, V_{Out}, will adjust depending on V_{Op} and the input states according to the principles of a resistive voltage divider. For a logic OR, the output device is initialized in the HRS as logic "1", while the inputs can be either in LRS ("1") or HRS ("1"). If V_{Out} exceeds the switching threshold, V_{SET}, the output device should perform a *SET* switching. In the example, this is expected for the input combinations "1"/"1" (orange) and "1" (blue), while for "1" (red) the output should remain in its state. **c** Executing parallel VCL operations in an array. The gate voltage, V_{Gate}, is applied at the Word-Lines (WL1–WL3), and the operation voltages, V_{Op} for inputs and GND for the output, are applied at the Source-Lines (SL1–SL3). The Bit-Lines (BL1 and BL2) act as shared lines and are left floating.

become the de facto standard in both academic research[10] and industrial development[15]. However, in this arrangement, a body effect in the nMOS transistor has to be considered if operated with bipolar RRAM.

In this paper, we utilize a 1T-1R resistive memory chip from the Memory Advanced Demonstrator 200 (MAD-200) process, with on-chip transistors and analog components in a standard CMOS process, the HCMOS9A 130 nm from STMicroelectronics, and back-end-of-line RRAM, based on a TiN/HfO_2/Ti material stack with 10 nm layers of HfO_2 and Ti each[16]. Figure 1c shows 10 exemplary current-voltage (I–V) measurements for single 1T-1R RRAM devices on the test chip. The devices exhibit bipolar switching as transitions from HRS to LRS (*SET*) and from LRS to HRS (*RESET*) are triggered by voltages of opposite polarity. Further information on the test-chip can be found in Supplementary Note S2.

The advantages of 1T-1R RRAM for CIM are high scalability, with demonstrated integrations down to a 14 nm CMOS node[17], an enhanced endurance of up to 1e8 switching cycles[18], and an intrinsic non-volatility. Utilizing these properties, RRAM-based arrays have been successfully used for a variety of computing tasks such as image processing or encryption[10,19,20].

In this work, we focus on the concept of stateful logic CIM[21,22]. Stateful schemes exploit non-volatile RRAM resistance states to represent logic inputs and outputs[23]. The underlying operation principle is called voltage-controlled logic (VCL). In VCL, a resistive voltage divider is formed between one or more input devices and a designated output device[24,25]. The concept is shown exemplarily for a two-input operation in Fig. 2a. During the VCL operation, two inputs and the output device are activated by applying a sufficiently high gate voltage, V_{Gate}, at the corresponding access transistor. Then, simultaneous voltage pulses of the operation voltage, V_{Op}, are applied at the inputs, while the output device is grounded. The line shared between the inputs and the output is left floating and will adopt a potential, V_{Out}, which is determined by the resistive voltage divider. If the amplitude of V_{Out} exceeds the switching threshold of the output device, it undergoes a conditional switching event; otherwise, it remains unchanged (shown in Fig. 2b for a logic OR). In this way, fundamental Boolean operations such as NOR, AND, OR, XOR, or NOT[23] can be implemented directly within the memory array. While we demonstrate VCL operations in filamentary RRAM arrays, the same principle has also been demonstrated with other emerging non-volatile memories, including magnetic tunnel junctions (MTJ)[8,25], spin-transfer torque (STT) RAM[22], and PCM[26]. Exploiting an array structure instead of a single VCL offers the benefit of parallel computing[27]. As the operation voltages are applied along shared lines, identical operations can be executed simultaneously across multiple array parts (as illustrated in Fig. 2c). This substantially improves operation throughput[28].

Despite their advantages, filamentary RRAM devices suffer from their intrinsic state variability, which leads to state fluctuations[29]. This variability poses significant challenges for reliable logic operations. Variations in the resistive states of both, inputs and outputs cause the output potential, V_{Out}, to fluctuate, resulting in a broader distribution rather than a fixed value. Consequently, identical logic operations performed on different devices may yield different outputs. So-called "Write-Verify" schemes can partially mitigate this effect by narrowing the resistive state variations and their impact on logic operations[30]. However, the stochastic nature of filamentary RRAM introduces another fundamental variability in the switching threshold voltage. Since the resistive switching is driven by the ionic arrangement of mobile donors as a stochastic process, two RRAM devices will generally not

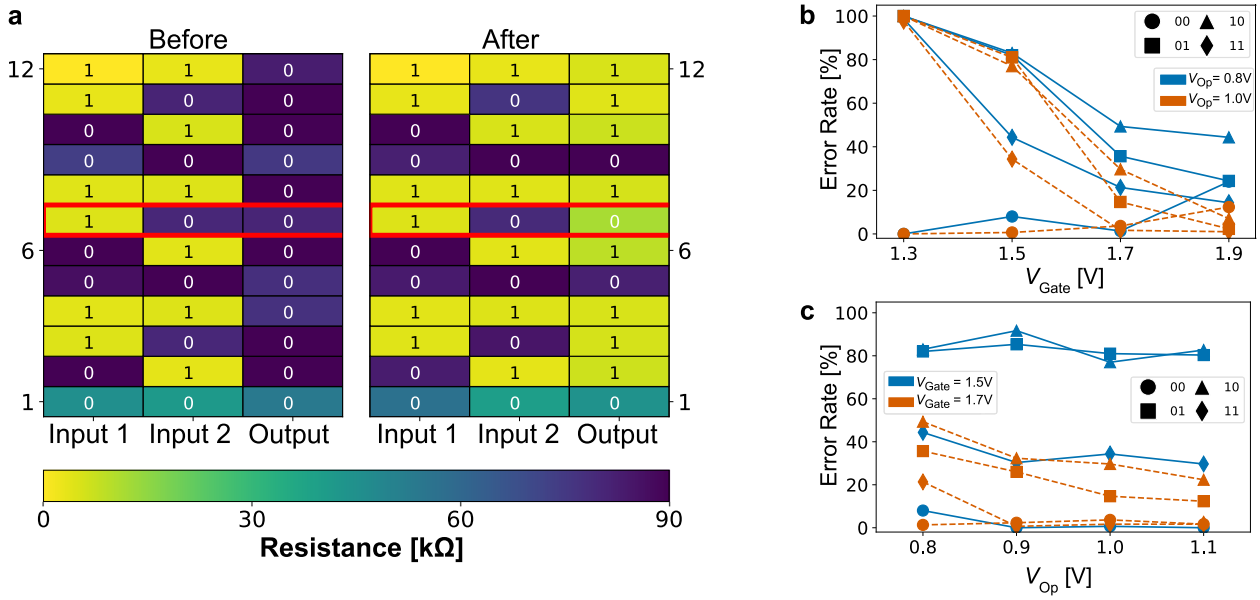


Fig. 3 | Experimental results for parallel VCL-OR operations. a Proof-of-concept for a parallel two-input logic OR operation with 12 gates. The measured resistances of inputs and outputs before (left) and after (right) the operation are displayed color-coded. The red box in row 7 highlights a false non-switching operation. The output of OR("1") is expected to be "1". Although the output device decreases its resistance (lighter color), the change is not sufficient to be distinguished correctly based on the threshold of 9.6 kΩ. The parallel operation is repeated 100 times each for different values of **b** V_{Gate} and **c** V_{Gate}, with re-initializing the outputs and inputs after each operation cycle. From the post-operation resistances, the voltage-dependent error rates are calculated as $\frac{\#\text{correct operations}}{\#\text{total operations}}$. The total number of operations is $n = 300$, as each input combination occurs three times.

exhibit an identical switching behavior under the same voltage pulse, even if their resistance states have been programmed to the same value[31]. This variability is visible already in the exemplary I–V measurement data displayed in Fig. 1c. Even though all programming pulses were identical, the resulting switching curves are similar in their general shape, yet non-identical.

In this work, we demonstrate the parallel execution of 12 VCL-OR gates in 1T-1R RRAM arrays, proving their potential for large-scale resistive CIM logic. Building on this, we systematically investigate the critical parameters that impact VCL operations, their reliability, and logic correctness. Although our experiments focus on logic OR gates, we extend the underlying concepts to variability-aware circuit simulations to explore other logic primitives. Our results provide an experimental benchmark for resistive CIM logic and reveal pathways towards more robust computing architectures. Together, these findings highlight both the promise and the limitations of resistive logic and lay the groundwork for future, energy-efficient CIM systems.

Results

Device programming

The chip and its RRAM devices were first characterized using single-device programming. After verifying the measurement setup, individual 1T-1R devices were tested under various programming pulse conditions. From these experiments, suitable operation parameters (width and amplitude) for a reliable single-device programming were extracted. Further to map the continuous resistance to binary logic states, a threshold value was defined as $R_{\text{threshold}} = 9.6\,\text{k}\Omega$. This value minimized the error probability for single devices (more details in Supplementary Note S2). Measured devices with a resistance below this threshold, $R < R_{\text{threshold}}$, are counted as LRS (logic "1"). In case the resistance exceeds the threshold, $R \geq R_{\text{threshold}}$, a device is classified as HRS (logic "1").

Parallel logic OR

As a first proof-of-concept, we demonstrate $N = 12$ parallel VCL-OR operations on a total of 36 1T-1R devices, 24 inputs, and 12 outputs. The inputs are uniformly programmed to cover all binary two-input combinations (3 × "1", "1", "1" and "1", graphically displayed in Supplementary Note S3). The programming of the initial states is performed and verified for all inputs individually to ensure their correctness.

During the operation, V_{Op} and V_{Gate} are applied simultaneously to the input and output devices via the Word-Lines (WL) and Source-Lines (SLs), while the 12 Bit-Lines are left floating. To determine the result of the conditional VCL switching, the electrical resistances of all devices are measured immediately before and after the operation. According to the logic OR, the output devices for "1" inputs should remain in HRS, while for all other combinations the output should switch from HRS to LRS, corresponding to a change of logic "1" to "1".

Figure 3a presents the color-coded changes in the electrical resistances for an exemplary VCL operation. In 11 of 12 rows, the output device shows the expected state after the operation. However, in row 7 with an input of "1" (highlighted as a red box in Fig. 3a), a false non-switching event is observed. Although the output resistance decreases, it does not exceed the threshold required for a full *SET* transition and is therefore still recorded as a logic "1" output. In order to quantify the occurrence of such false logic evaluations, the same operation cycle is repeated 100 times each for different pairs of V_{Op} and V_{Gate}, according to the measurement flow presented in Supplementary Note S3. From all measurements, the voltage-dependent cumulative error rates are extracted and displayed in Fig. 3b and Fig. 3c. The data reveal a critical dependence on the gate voltage V_{Gate} (Fig. 3b) as increasing V_{Gate} significantly decreases the probability of logic errors for input combinations "1", "1", and "1". In contrast, variations in the operation voltage, V_{Op} (Fig. 3c), barely have any impact. Only at elevated gate voltages can an increase of V_{Op} further reduce the logic error rate. Further, a distinct asymmetry in the error rate is observed between the logic inputs "1"/"1" and "1". In principle, all three cases should exhibit similar behavior. However, the error rates for "1"/"1" are consistently higher than those for "1" across all applied voltages. Our best recorded case, $V_{Op} = 1.0$ V and $V_{Gate} = 1.9$ V, had an operation success rate (inverse of error rate) of 87.6% ("1"), 97.6% ("1"), 93% ("1"), and 99% ("1").

These observations imply that for a successful VCL, another parameter besides the operating voltage has to be taken into account. If the switching operation were purely voltage-driven, V_{Op} should show a more dominant

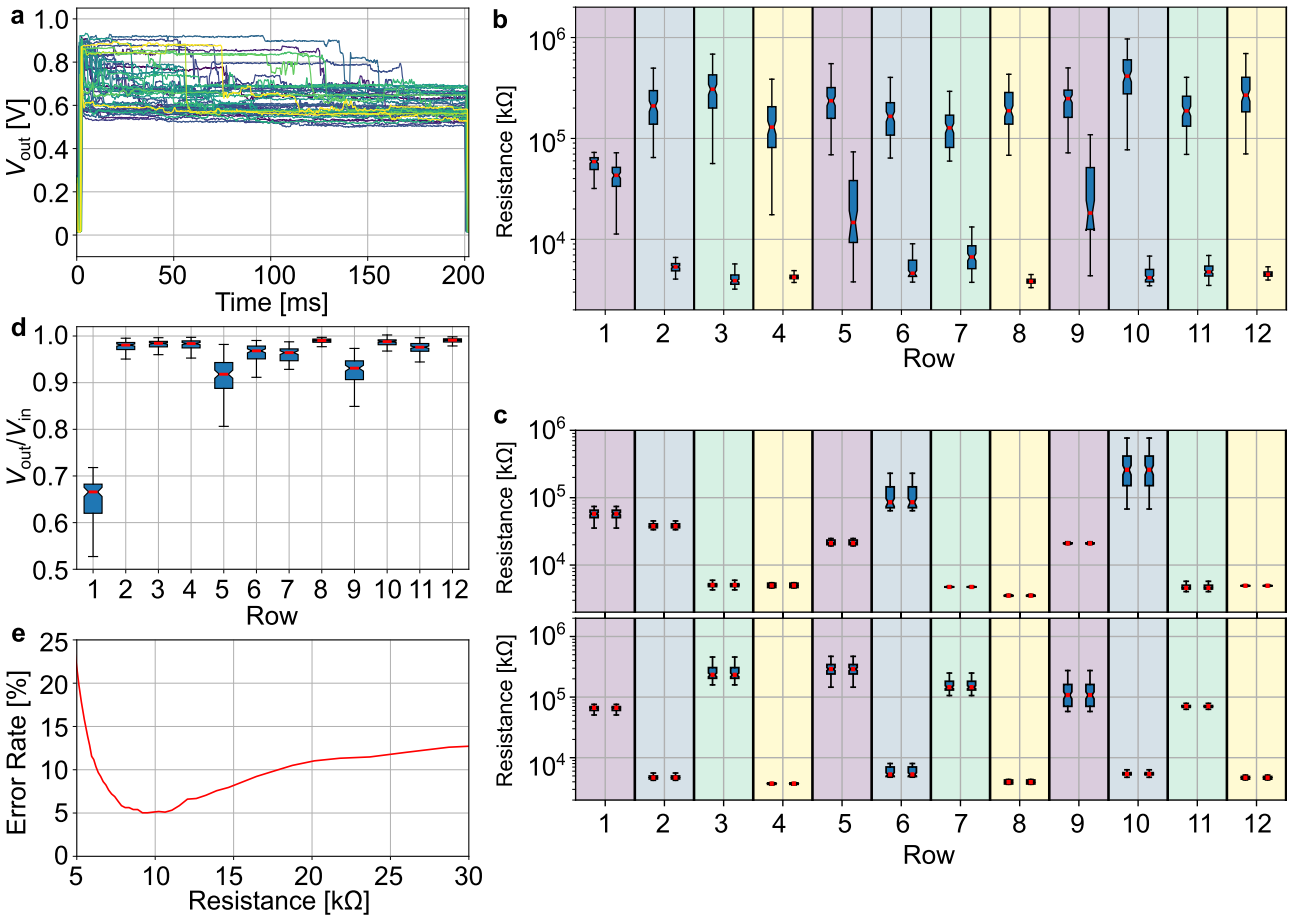


Fig. 4 | Operational behavior of the VCL voltage divider. a Bit-Line potential during the parallel VCL operation for an "1"-input. **b**, **c** Boxplots of the output (**b**) and input (**c**) resistances before (left) and after (right) the VCL operation in 12 parallel rows. Each boxplot contains the data of 100 operations from the voltage set V_{Op} = 1.0 V and V_{Gate} = 1.9 V. **d** Calculated resistive voltage divider ratio based on the initial resistances from (**b**, **c**). **e** Cumulated error rate in dependence of the threshold resistance, $R_{threshold}$, as a binary distinction between HRS and LRS.

impact. However, the resistive SET switching in filamentary RRAM is coupled to ionic processes that require local Joule heating[32]. Generating sufficient thermal energy depends not only on the applied voltage, but also on the current flowing through a device. In the 1T-1R VCL structure (Fig. 2a), the current is limited by the channel resistance of the access transistors, which is controlled by V_{Gate}. Increasing V_{Gate} leads to elevated currents, which go hand in hand with an extended local heating and an improved switching. The origin of the observed asymmetry might also be linked to the aforementioned current limitation. In addition to the transistor channel resistance, the current flowing through the output device is further constrained by the parallel resistance of the two inputs. In the "1" case, both inputs are in the LRS, resulting in a comparatively low parallel input resistance and thus higher current. In contrast, in the "1"/"1" cases, the HRS input suppresses the current required for successful switching.

Even without the current limitation, resistive switching remains an inherently stochastic process that is susceptible to significant variability. This stochastic nature is also reflected in the switching dynamics. Figure 4a shows the recorded voltage across a Bit-Line during a VCL-operation with an "1" input. When the output device switches to the LRS, the resistive voltage divider arrangement shifts, and the Bit-Line voltage decreases rapidly. For the recorded "1" input, all Bit-Lines show such a voltage drop as expected. However, the time until this happens varies substantially. In our analysis, we define the switching time as the duration until the Bit-Line voltage has decreased to 75% of its maximum value. The resulting distribution quartiles are [0.73, 12.9, 172.9] ms. Approximately 25% of the output devices switch almost instantaneously. However, in 25% of the outputs, only limited heat is generated, which results in a delayed SET and switching times longer than 172 ms. This SET variation has been observed in the literature before and originates from the local Joule heating in the device that triggers a so-called "thermal runaway"[33]. Ensuring a sufficient current flow and extended pulse lengths, therefore, enhances the heat generation and the overall SET switching process. However, pulse lengths up to 200 ms drastically reduce the computational throughput and may also trigger unintended output switching for "1" inputs.

The concept of VCL relies on analog resistances, in our case provided by RRAM devices. To gain deeper insights into the performance of VCL and the underlying error mechanisms, the corresponding resistance distributions must be analyzed in detail. Figure 4b shows the output resistances before and after the operation as boxplots for the best operating condition, V_{Op} = 1.0 V and V_{Gate} = 1.9 V. Although the output devices 2-4, 6-8, and 10-12 are expected to undergo similar switching, the cycle-to-cycle (C2C) and device-to-device (D2D) variability is pronounced. In particular, output devices 6 and 7 exhibit multiple outliers towards higher resistances. In contrast to this, the output devices 1, 5, and 9 are expected to retain their initial resistance states. However, significant shifts toward lower resistances are observed, most prominently for devices 5 and 9. These deviations may arise from multiple sources, such as fabrication-, forming-, or cycling-related variability[34,35]. Conceptually, the same mitigation strategies used for single-device programming, e.g., write-verify algorithms and improved voltage control, also apply here and can improve switching performance[36,37]. However, compared to single device operation, the switching potential in VCL, V_{Out}, is not directly imposed by the driving circuitry. Instead, it arises

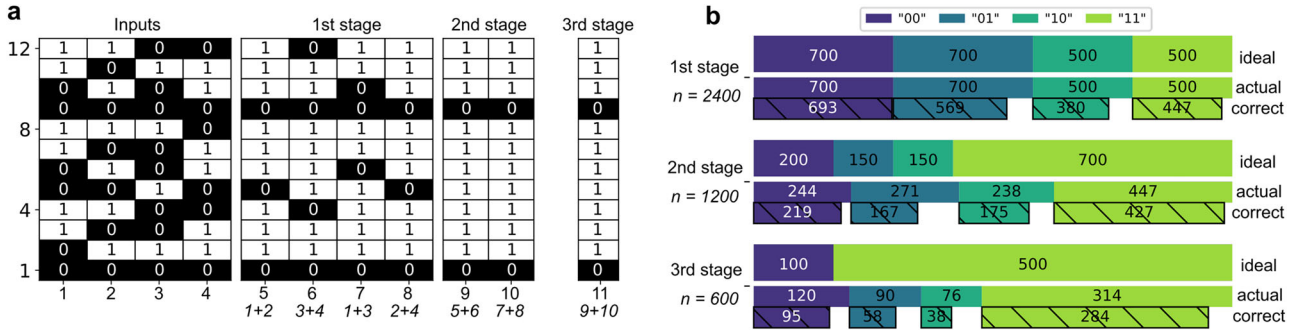


Fig. 5 | Cascading parallel logic operations. a Ideal operation flow of the 3-stage cascading logic. The Inputs (columns 1–4) are programmed and verified. Afterward, the evaluations of stages 1–3 are performed as parallel logic OR. **b** Total distribution of logic OR operations in 50 three-stage cascaded evaluations. The numbers on the left state the total number of operations performed per stage. In each stage, the colored bars represent the distribution of theoretical operations based on ideal inputs ("ideal"), the actually conducted operations ("actual"), and of these, the operations with a correct output ("correct", as shaded bars).

from the resistance ratio between the input and output devices and the applied input potential, V_{In}, which makes it harder to control the switching precisely. To examine this ratio, the input resistances before and after the operation are shown in Fig. 4c. Based on these values and the output resistances, we calculated the initial voltage-divider ratios (see Supplementary Note S3 for details), which are displayed in Fig. 4d. Analytically, the ratio should lie between 2/3 for a "1" input and 1 for a "1" input. As the ratio approaches 1, the output potential V_{Out} increases, and a successful output switching becomes more likely. Yet, also the Bit-Lines 5 and 9, which should not switch, show ratios that are comparatively high. This explains the observed downward shift of their output resistances. Conversely, Bit-Lines 6 and 7 exhibit lower ratios than the other Bit-Lines with similar input configurations, resulting in weaker switching and the observed tails toward higher resistances. A more precise adjustment of the input and output resistance leads to a greater separation of the voltage-divider ratios for non-switching and switching input combinations. This can enhance the correctness of the VCL operation.

The output resistances in Fig. 4e exhibit large variations in their analog states, which are covered by the binary classification. Ideally, the resistance distributions of LRS (logic "1") and HRS (logic "1") outputs would not overlap. In practice, the goal is to minimize this overlap in order to reduce the rate of false classifications. This can be achieved by improving the switching conditions, as discussed above. Another way to improve the correct classification is by adjusting the threshold value, $R_{threshold}$. Originally, we set this value to 9.6 kΩ based on the single device classification. In Fig.4e, we have calculated the corresponding error rate, i.e., the total number of wrong classifications divided by the total number of operations, based on a varied threshold. It is seen that the error rate decreases towards the minimum of 5.5% around 10.0 kΩ and rises again for higher values. Balancing the threshold is an important step towards an optimized VCL operation. However, this step has to be performed for each specific crossbar implementation as it depends on the physical 1T-1R behavior.

Cascading logic operations

A promising implementation of parallel logic CIM is cascading operations. As the operation outputs are represented in the same form as the logic inputs, i.e., the non-volatile state of an RRAM device, the output of an operation can directly serve as the input of a subsequent operation without any intermediate conversion. This can be exploited to implement more complex computations, in which the intermediate results are generated and used directly in the memory array. While cascading operations enhance energy efficiency as the data is never transported to the processing unit, any errors introduced in one stage might propagate as corrupted input through the following steps. Ultimately, compromised final-stage outputs can lead to logic errors.

We investigate the feasibility of cascading logic in a three-stage computing concept. Although the number of cascaded operations is relatively small, this study provides a proof-of-concept for RRAM-based stateful parallel logic. The insights gained from this demonstration can be transferred to larger designs and serve as a foundation for developing scalable and reliable RRAM-based CIM architectures.

Prior to the operation, four input columns comprising a total of 48 RRAM were programmed and verified to ensure error-free initial conditions. Using these inputs, we carried out 7 consecutive parallel OR operations arranged in three cascading stages (see Fig. 5a). In the first stage, four OR operations were performed directly on the inputs. It has to be noted that these operations are done sequentially, i.e., one after another, in the same manner as explained in the previous section. For executing the different operations, the voltages are applied as described in Supplementary Note 3, yet on different crossbar columns. The resulting outputs then served without any correction as inputs for two second-stage operations. Both outputs of the second stage were then combined in a final third-stage OR. The complete cascading scheme is repeated 50 times with a total number of $7 \times 12 \times 50 = 4200$ operations, according to the operation flow in Supplementary Note S3. Afterwards, the operation accuracy is evaluated by extracting the measured outputs and comparing them with the theoretically expected results under ideal conditions.

A critical aspect in cascading concepts is that the distribution of input states may diverge from stage to stage. This shift arises from errors in the intermediate outputs, which serve as the following inputs. This effect is visualized in Fig. 5b. In the first stage, with error-free inputs, the measured and expected distributions still match. However, in the second stage, the deviations are already evident; for example, 253 fewer "1" operations were recorded than expected. These missing operations are a direct consequence of false non-switching events in the first stage, leading to a reduced number of logic "1" outputs. This behavior persisted in the third stage, and the distributions further diverged. Surprisingly, not all such re-distributions automatically result in logic errors. If an expected "1" shifts to "1" or "1", the OR operation can still produce the correct output. Only if both inputs are corrupted, or another false non-switching event occurs, does the evaluation produce a logic error. This resilience is observable in the third stage, where in total the evaluations of 58 "1" and 38 "1" yield the correct result despite one corrupted input.

The overall accuracy of the cascaded logic operations is summarized in Table 1. The input patterns "1" and "1" demonstrate a comparably high reliability, while the mixed inputs "1"/"1" suffer from error rates around 25%. This behavior is consistent with the trends seen in the voltage-dependent measurements in Fig. 3b, c.

Simulation of logic gates

Our experimental study is limited by the capability of the measurement system, which allows a single analog voltage output per operation. With this, only VCL-based OR operations can be investigated (see Supplementary Note S3). However, OR is not Boolean complete and must be combined with

other functions to realize more complex computing architectures. A widely spread method for RRAM-based logic is to implement OR together with the negated material implication, NIMP[38]. Based on the primitive NIMP gate, a logic NOT and XOR can be realized, which, in combination with OR, offer a Boolean complete set of logic functions[39,40] (more details on the NIMP implementation can be found in Supplementary Note S4). To assess whether the experimentally observed voltage dependence in Fig. 3b, c is consistent with the underlying RRAM dynamics, we performed variability-aware circuit simulations. As an example of a Boolean-complete logic, we selected the VCL gates NOT, XOR, and OR. The Monte–Carlo simulations incorporate variability effects of both, transistors and RRAM devices, to analyze the performance and accuracy of logic gates beyond the experimental setup (the simulation setup is presented in Supplementary Note S4).

The simulated voltage-dependent error rates of OR, NOT, and XOR are shown in Fig. 6. In general, elevated voltages reduce the error rates for the input cases "1"/"1" and "1". At higher voltages, the RRAM switching becomes more likely, which prevents false non-switching events. This trend is consistent with our experimental findings. However, in contrast to the measurements shown in Fig. 3c, the simulations indicate that the operation voltage, V_{Op}, is the dominant factor, while V_{Gate} has only a marginal impact on the accuracy. In contrast to the experiments, the simulations isolate the effect of V_{Op} as the simulated ideal voltage sources do not introduce a current limitation. Therefore, the resistive switching probability is directly connected to the applied voltage[41]. While some studies report a similar observation and identify the operation voltage as the main parameter for improving the single-gate accuracy[42,43], others find only a weak influence[44]. These mixed results suggest that these operational parameters cannot be independently investigated. Instead, the combined effect of both voltages is crucial. While V_{Gate} lowers the channel resistance of the access transistor and reduces the current limitation, V_{Op} increases the current through the 1T-1R structure. When optimized together, they enable a more reliable logic performance.

Discussion

In this work, we investigated the feasibility, opportunities, and challenges of parallel logic CIM based on resistive 1T-1R arrays. In particular, we focused on the reliability challenges arising from the variability and stochasticity, and how these effects impact the correctness and stability of VCL operations. The parallel evaluation of 12 logic OR gates was demonstrated as a proof-of-concept, expanding previous examples of 4 parallel XOR gates[45] or 8 parallel NAND gates[46]. Our experimental results showed that the operational voltages, namely the access transistor gate voltage, are a critical parameter for reliable switching and, therefore, for the accuracy of stateful switching-based voltage-controlled-logic operations. Furthermore, we observe a current-limitation effect by the asymmetric input configurations "1"/"1" and "1". This limitation arises from the inherent asymmetry of the VCL-OR scheme. Increasing the HRS/LRS ratio may help to enlarge the voltage-divider ratio and separate the switching and non-switching conditions. It is seen that the VCL operation also exhibits several challenges that differ fundamentally from single-device programming. Due to the voltage-divider-based switching, the output potential is more difficult to control precisely, as it depends not only on the applied voltage but also on the resistance configuration of three 1T-1R devices. Further, the voltage divider arrangement is not static during the operation. The resistances of the output device and potentially also the input devices change dynamically, which complicates the prediction of the switching behavior. All these factors make optimization of VCL performance challenging, particularly given its intrinsically antagonistic nature. The VCL operating conditions must simultaneously prevent false switching events and avoid false non-switching events. However, these two objectives are fundamentally antagonistic: any measure that increases the likelihood of successful switching also elevates the risk of unintended switching, and vice versa. Consequently, the VCL reliability constitutes an optimization problem in which the goal is to minimize the overall error rate to an acceptable level.

It should be emphasized that the devices used in this study were not optimized. Since the device properties are largely determined by the fabrication process, our primary focus was on exploring the impact of the voltage parameters on the logic accuracy. The RRAM electroforming[47] and the single-device programming techniques[35,36] offer substantial opportunities for improvement in future work, enabling a more precise adjustment of the voltage divider conditions. In addition, specific VCL measures such as an adaptive classification threshold, may further reduce the overall logic error rate and improve the binary reliability. Another important aspect to consider is the body effect in the nMOS select transistors. As depicted in the VCL circuit (Fig. 2a), the transistor body terminals are not shorted to the source terminals. This configuration is required by the bipolar nature of the 1T-1R devices, which must support a bidirectional operation for both, SET and RESET polarity. This is in contrast to conventional digital CMOS architectures, in which the source and drain terminals are permanently assigned. Consequently, for one of the switching directions, either SET or RESET, a non-zero source-body voltage unavoidably develops, leading to a body effect and a shift in the threshold voltage. This phenomenon has been extensively studied in the RRAM-based CIM literature, and several mitigation strategies have been proposed. One approach is to orient the 1T-1R cell such that the body effect occurs in RESET polarity, which reduces the impact on the device performance[48]. Further optimizations on circuit-level are the use of low-voltage threshold MOSFETs with a relatively large W/L

Table 1 | Total error rates for the logic OR operations across all cascaded stages

Inputs	Operations			
	No switching	Switching		
	00	01	10	11
Total correct	94.6%	74.8%	72.8%	91.8%

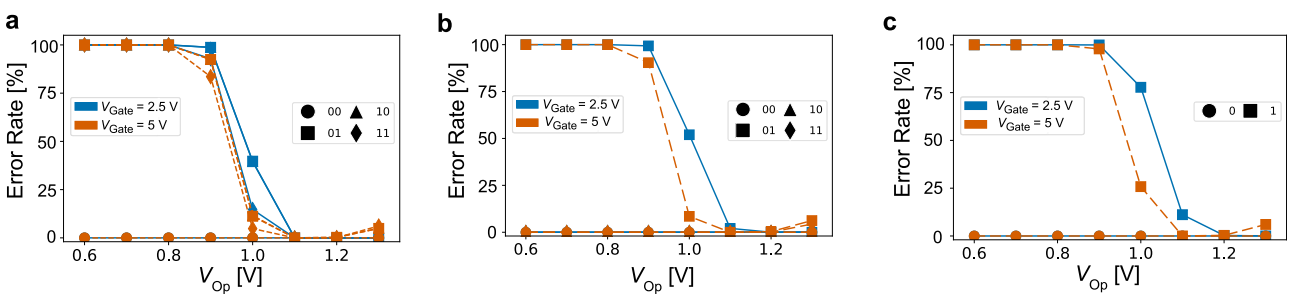


Fig. 6 | Simulated VCL accuracies. The logic gates **a** OR, **b** XOR, and **c** NOT are simulated for all possible input combinations (more details on the simulation setup are presented in Supplementary Note S4). For each input and set of V_{Op} and V_{Gate}, a total of n = 1000 Monte–Carlo parameter points are simulated. The error rate is calculated as $\frac{\#\,\text{correctoperations}}{\#\,\text{totaloperations}}$ where an operation is counted as correct if the post-operation resistance is more than (inputs "1" and "1") or less than (all other inputs) 9.6 kΩ.

ratio and increasing the applied gate voltage[44,49]. This ensures the operation of the transistor in the saturation regime with low channel resistance in both polarities.

The suitability of resistive arrays for cascading logic was explored in a three-stage operation. This is important as non-volatile CIM is proposed for large-scale data processing and computing architectures, such as neural networks or database applications. While errors can propagate through successive stages, the exploited OR gate demonstrated an intrinsic resilience, as certain corrupted inputs still yielded correct outputs. Nevertheless, this resilience might worsen when executing other logic functions. Especially since OR is not logically complete, at least one other logic function, e.g., NOT, has to be implemented as well. These observations underline the need to investigate error accumulation and propagation across multiple stages and a broader set of logic gates in the future.

Our variability-aware Monte–Carlo simulations confirmed the strong impact of the operational voltages on the logic accuracy. In contrast to the experiments, the improvements were primarily due to the applied operation voltage rather than the access transistor gate voltage. Yet, these divergent observations point to the same underlying mechanism: a current limitation. The crucial factor for switching a filamentary RRAM device is not solely the applied voltage, but the resulting current through the device[32]. While the gate voltage reduces the channel resistance of the access transistor, the operating voltage drives the current through the 1T-1R structure. Together, both parameters determine the current level and the associated Joule heating, which is required to prevent or induce a resistive switching event[50]. While this sets restrictions for the switching-based VCL, it also opens the perspective for utilizing thermal effects in future computing concepts[51].

In summary, our measurements demonstrated 2-Input OR accuracies between 72.8% and 94.6% in cascading operations and up to 87.6%–99% for optimized voltages. These numbers match previous experimental studies reporting 99.4% for a 2-Input NAND in MTJ arrays[8], 87.4%–100% for a2-Input NOR in STT-RAM[52], or 80% for a 2-Input NAND in RRAM[53].

RRAM devices show a promising performance compared to other emerging non-volatile memory technologies, particularly in terms of scalability and integration in 1T-1R arrays. While the concept of exploiting RRAM arrays for logic CIM is not novel, this work provided the first large-scale experimental demonstration of feasibility and accuracy investigation for parallel and cascaded operations, which are essential for implementing complex and energy-efficient computing tasks. For example, CIM-based logic has been successfully combined with memory and arithmetic operations to enable generalized matrix multiplication (GeMM) and processing[54,55]. However, significant challenges remain on the path to full-scale CIM architectures. These limitations apply not only to RRAM-based approaches but to all non-volatile memory technologies (MTJ, PCM, STT-RAM) to some extent. Yet, we tried to provide valuable insights for optimizing logic CIM on the way to reliable RRAM computing hardware.

Methods

VCL

A VCL function is defined by the initial state of the output devices and the applied voltage polarity. In our case, the outputs are initialized in the HRS and biased in *SET* polarity, which implements a logic OR gate. Although other operations such as NOR or NAND are theoretically possible, previous RRAM experiments demonstrated reliability issues, leaving OR as the most feasible option[39]. More details on the principle of VCL and the VCL-OR are given in Supplementary Note S3. In this work, we aim to investigate parallel VCL-OR operations. The attribute parallel indicates that the logic gates are not executed sequentially, i.e., one after another, but within a single operation cycle and through the same applied voltage pulses. This is possible due to the matrix-like structure of 1T-1R RRAM arrays in which multiple devices share common voltage lines. In our crossbar array, the WL connects the transistor gates of one column. Parallel to this, a SL is connected at the transistor sources. Orthogonal to SL and WL, a Bit-Line (BL) is shared row-wise by the opposite RRAM electrode. The crossbar layout is visualized in Fig. 2c and in Supplementary Note S3.

Electrical characterization

The electrical measurements were performed in a 1T-1R RRAM crossbar array based on the Memory Advanced Demonstrator 200 mm (MAD-200) process. The chip was fabricated in two steps. First, the transistors and all analog components were fabricated in a standard 130 nm CMOS process. Afterwards, the filamentary TiN/HfO_2/Ti-based RRAM devices were integrated by CEA-LETI in the back-end-of-line[35]. The chip was mounted on a custom Printed Circuit Board (PCB), which interfaced with a Labjack T7 data acquisition system for digital control, a DC laboratory power supply to provide V_{DD}, and an aixACCT Systems µ C module for delivering analog voltage signals and performing the current sensing. The chip and the measurement system are explained in detail in Supplementary Note S1.

Data availability

The datasets generated and/or analyzed during the current study are available online on the Juelich Data platform under DOI: 10.26165/JUELICH-DATA/XKYQVK.

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Author contributions

L.B. conducted the experiments and simulations and was the main contributor to writing the manuscript. T.Z. designed and developed the demonstration hardware and software for the experiments. N.K. provided theoretical details of RRAM devices and variability effects, co-wrote and revised the manuscript. R.W. coordinated the entire project and supervised the work. S.M. provided theoretical details of the logic functions and supervised the work. All authors reviewed and discussed the results and contributed to the completion of the manuscript.

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Competing interests

The authors declare no competing interests.

Additional information

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