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Damage-free van der Waals metal/NbO_x–$NbSe_2$ integration for reliable and flexible memristor in neuromorphic computing

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Abstract

Ultrathin native oxides formed on two-dimensional (2D) metallic transition metal dichalcogenides (MTMDs), such as $NbSe_2$, have recently emerged as promising active switching layers for memristive devices. However, these oxides are highly susceptible to surface damage during conventional top-electrode deposition processes, which leads to interfacial disorder and degraded switching reliability. Here, we demonstrate a highly reliable and flexible NbO_x–$NbSe_2$ memristor utilizing a damage-free van der Waals (vdW) metal transfer technique. By gently laminating a prefabricated gold (Au) electrode onto the NbO_x–$NbSe_2$, a pristine and chemically undisturbed metal/oxide interface is achieved. While metallization-induced barrier damage causes a large OFF-state direct tunneling (DT) current in the evaporated-metal memristor (Ev-MEM), preserving the pristine oxide interface in the transferred-metal memristor (T-MEM) effectively suppresses this OFF-state DT current. Consequently, the T-MEM exhibits an ON/OFF ratio of 10^5—a 1,000 times improvement over the Ev-MEM (10^2)—along with a stable retention time of $> 10^4$ s and an endurance exceeding 10^3 cycles. Furthermore, the T-MEM exhibits exceptional synaptic linearity ($\beta = 0.6$) and a full dynamic range (0–1), in contrast to the Ev-MEM, which suffers from poor linearity ($\beta = 3.1$) and a limited dynamic range (0.2–1). As a result, a hardware-aware convolutional neural network (CNN) simulation shows a near-ideal MNIST image recognition accuracy of 98.1% for the T-MEM based system, significantly outperforming the Ev-MEM counterpart (75.8%). In addition, capitalizing on the inherent flexibility of the 2D $NbSe_2$ and the vdW interface, devices fabricated on a polymer substrate demonstrate remarkable mechanical robustness, maintaining stable switching characteristics over 200 bending cycles at a 30° angle. Our findings establish that damage-free vdW metal integration is a crucial prerequisite for developing reliable, highly accurate, and flexible neuromorphic hardware.

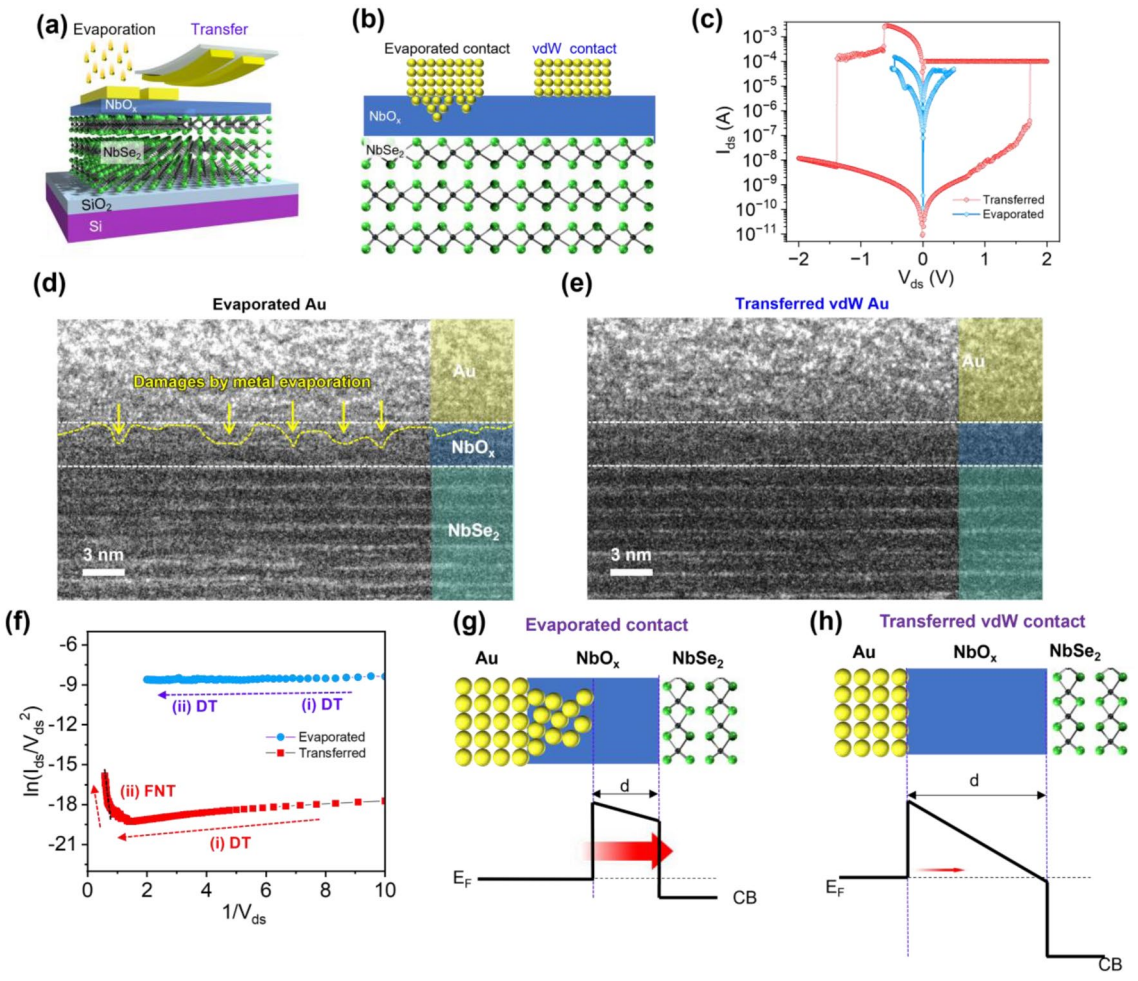
Keywords Niobium diselenide ($NbSe_2$), Transferred contact memristor (T-MEM), Evaporated contact memristor (Ev-MEM), Direct tunneling (DT), Fowler Nordheim tunneling (FNT)

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Graphical abstract



1 Introduction

As artificial intelligence (AI) and data-centric computing tasks become increasingly complex, the inherent energy inefficiency and latency of conventional von Neumann architectures have emerged as critical bottlenecks [1–4]. In response, brain-inspired neuromorphic computing has been extensively investigated as a promising paradigm to process vast amounts of unstructured data with unprecedented energy efficiency [3–5]. To realize such hardware-based artificial neural networks (ANNs), memristors have garnered significant attention as ideal artificial synapses due to their non-volatile analog resistance modulation, high integration density, and low power consumption [6–8]. For neuromorphic hardware to achieve high pattern recognition accuracy comparable to software-based algorithms, the artificial synapses must exhibit highly linear and symmetric weight updates, a large dynamic range (high ON/OFF ratio), and excellent operational reliability.

Recently, two-dimensional (2D) transition metal dichalcogenides (TMDs) materials and their van der Waals (vdW) heterostructures have provided a breakthrough platform for next-generation flexible neuromorphic electronics [9–12]. A variety of TMD-based memristors have been investigated for in-memory computing, including floating-gate memristors (FGMEMs) [13–16], resistive memristors (RMEMs) [17, 18], phase-change memristors (PCMEMs) [19, 20], magnetic memristors (MMEMs) [21, 22], and ferroelectric field-effect transistors (FeFETs) [23, 24]. Among them, RMEMs using metallic niobium diselenide ($NbSe_2$) offer unique advantages. By precisely controlling the thermal oxidation of $NbSe_2$, a native NbO_x insulating layer can be formed on its surface, spontaneously creating an atomically flat, vertical NbO_x–$NbSe_2$ heterostructure [25, 26]. In this architecture, the metallic $NbSe_2$ acts as a seamless bottom electrode, while the NbO_x layer serves as a highly reliable active switching medium. Despite these structural advantages, realizing

high-performance memristors based on ultra-thin 2D native oxides faces a severe technological hurdle regarding top electrode integration [25–28].

In conventional NbO_x–$NbSe_2$ memristors, top metal electrodes are deposited using high-vacuum thermal evaporation. However, during this process, high-kinetic-energy metal atoms physically bombard the delicate surface of the ultra-thin oxide barrier. This high-energy metallization inevitably causes structural damage, atomic penetration, and the formation of defect-induced leakage pathways [29, 30]. In ultra-thin NbO_x layers, such interface degradation shifts the charge transport mechanism toward uncontrollable direct tunneling (DT). Consequently, the device suffers from a degraded ON/OFF ratio, high OFF-state leakage current, and excessively abrupt switching behaviors. In the context of neuromorphic computing, this severely degrades the dynamic range and the linearity of synaptic weight updates, which ultimately causes catastrophic failures in neural network training and classification accuracy.

Recently, the vdW integration of three-dimensional (3D) metals and 2D materials has emerged as a compelling strategy to form an ideal interface [11, 29, 31]. By physically laminating pre-fabricated, atomically flat 3D metal electrodes onto dangling-bond-free 2D materials without direct chemical bonding, an ultra-clean interface devoid of physical or chemical damage is achieved. This ideal interface makes it possible to approach the Schottky–Mott limit in vdW metal–semiconductor junctions [32] and the intrinsic exciton physics limit in 2D semiconductor diodes [33]. In this work, we demonstrate a highly reliable and flexible NbO_x–$NbSe_2$ memristor utilizing a damage-free vdW metal transfer technique. By gently laminating a prefabricated gold (Au) electrode onto the NbO_x surface, we successfully constructed a chemically undisturbed, pristine metal/oxide interface. Comprehensive transport mechanism analyses reveal that preserving the physical integrity of the oxide barrier effectively suppresses the DT leakage, enabling a controlled Fowler–Nordheim tunneling (FNT) mechanism. As a result, the transferred-metal memristor (T-MEM) exhibits an outstanding ON/OFF ratio of over 10^5, stable endurance ($>10^3$ cycles), and robust retention ($>10^4$ s). More importantly, the damage-free interface grants exceptional synaptic linearity ($\beta = 0.6$) and a full dynamic range, allowing a hardware-aware convolutional neural network (CNN) simulation to achieve a near-ideal MNIST image recognition accuracy of 98.1%. Furthermore, capitalizing on the inherent flexibility of the 2D $NbSe_2$ and the vdW interface, the fabricated memristor on a polymer substrate demonstrates remarkable mechanical robustness, maintaining stable switching characteristics over 200 bending cycles at a 30° angle. Our findings establish that damage-free vdW metal integration is a crucial prerequisite for developing reliable, highly accurate, and flexible neuromorphic hardware.

2 Results

Figure 1 illustrates the synthesis process, material characterization, and device fabrication of the NbO_x–$NbSe_2$ heterostructure-based memristor. As depicted in Fig. 1a, the 2D $NbSe_2$ flakes were synthesized using a chemical vapor deposition (CVD) system. The growth was achieved by selenizing an amorphous niobium oxide (ANO)-coated SiO_2 substrate using a solid selenium (Se) precursor transported by a carrier gas [25]. Fig. 1b shows the atomic schematic of the synthesized metallic $NbSe_2$ crystal structure. By precisely controlling the Se heating temperature from 300 to 380 °C, the thickness of the CVD-grown $NbSe_2$ flakes could be systematically tuned from approximately 2 nm to 12 nm, as confirmed by the optical microscope images and the corresponding thickness plot (Fig. 1c, Fig. S2). To study the impact of the surface oxide on memristive behavior, 6–10 layers $NbSe_2$ flakes were utilized because thinner flakes (2–4 layers) degrade rapidly after surface oxidation, making them unsuitable for multi-step device fabrication (Fig. S3).

The crystalline quality and chemical composition of the as-grown $NbSe_2$ were verified using Raman and X-ray photoelectron spectroscopy (XPS). The Raman spectrum (Fig. 1d) exhibits distinct peak at 230 cm^{-1} and 246 cm^{-1}, corresponding to the characteristic out-of-plane (A_{1g}) and in-plane (E^1_{2g}) vibrational modes of $NbSe_2$. [34, 35] For comparison, Raman spectra of the as-grown $NbSe_2$ flake before and after oxidation are provided in Fig. S4. Increasing the oxidation time decreases the overall Raman intensity due to the weakening of Nb–Se bonds and partial film amorphization. Notably, oxidation causes the E^1_{2g} peak (246 cm^{-1}) to surpass the A_{1g} peak (230 cm^{-1}) in intensity. This inversion deviates from the typical signature of pristine $NbSe_2$, confirming partial oxidation of the flake [35]. Fig. 1e and f shows Nb 3d and Se 3d core level spectra. Deconvoluted peaks at 203.49 eV and 206.42 eV can be identified as Nb^{4+} $3d_{5/2}$ and Nb^{4+} $3d_{3/2}$ of $NbSe_2$, confirming + 4 oxidation state of Nb and complete selenization. Similarly, peaks at 54.7 eV and 55.6 eV can be assigned to Se $3d_{5/2}$ and Se $3d_{3/2}$, indicating -2 oxidation state of Se [34]. These results are in good agreement with previous reports, indicating the high quality of $NbSe_2$ flakes grown using the CVD method.

To fabricate the memristive device, the pristine metallic $NbSe_2$ was subjected to a controlled thermal oxidation process (O_2 annealing) for 30 min, as illustrated in Fig. 1g. This process partially oxidizes the top layers of the $NbSe_2$, spontaneously forming a vertical NbO_x–$NbSe_2$ heterostructure. This structural transformation drastically alters the electrical characteristics of the device. As shown in

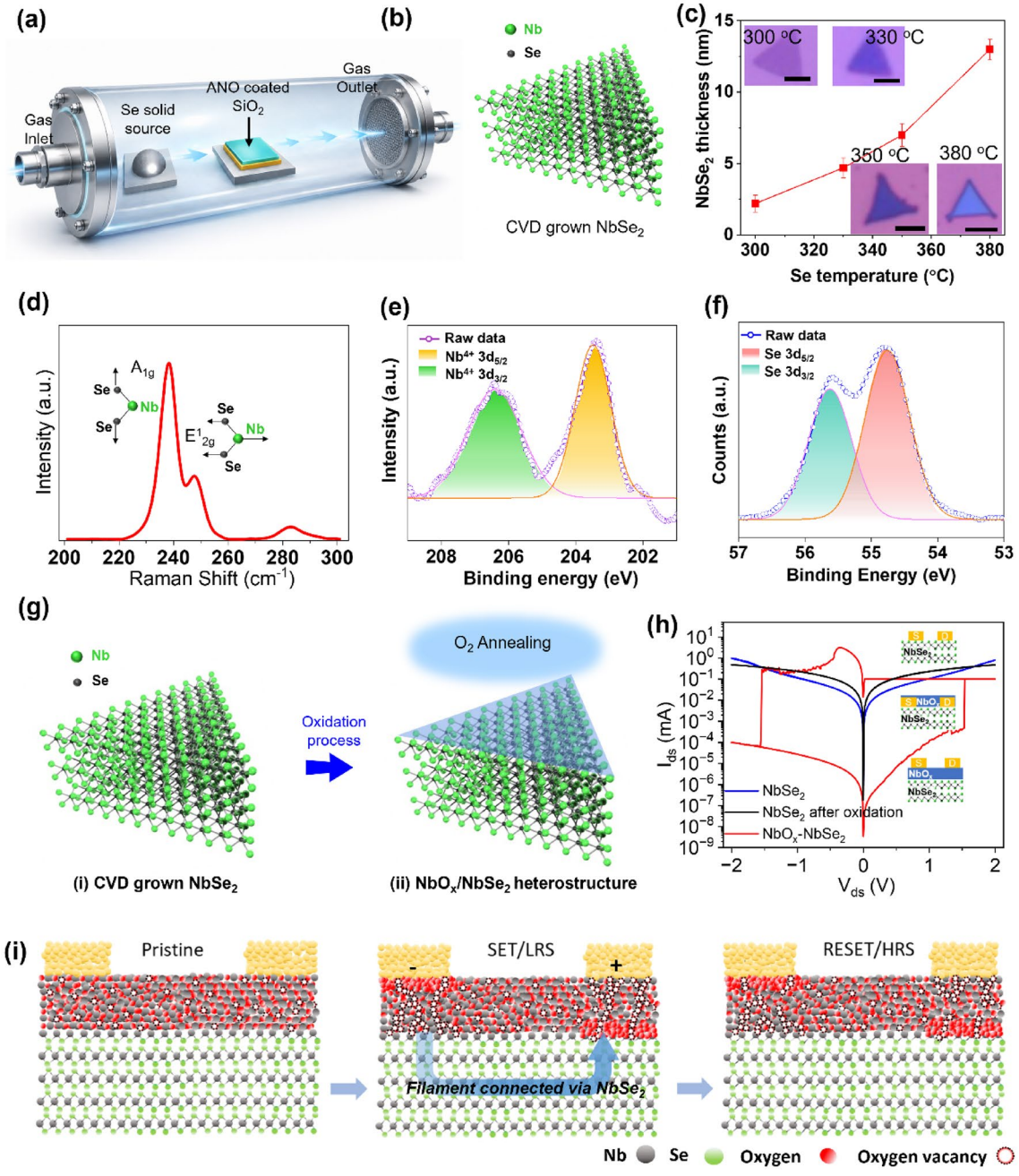


Fig. 1 Synthesis, material characterization, and resistive switching mechanism of the NbO_x-$NbSe_2$ heterostructure. **a** Schematic illustration of the chemical vapor deposition (CVD) system used to synthesize 2D $NbSe_2$ flakes by selenizing an amorphous niobium oxide (ANO)-coated SiO_2 substrate. **b** Atomic structure schematic of the CVD-grown metallic $NbSe_2$. **c** $NbSe_2$ flake thickness as a function of the solid selenium (Se) precursor heating temperature. The insets show optical microscope images of the flakes grown at corresponding temperatures. Scale bar is equal to 5 µm. **d** Raman spectrum of the as-grown $NbSe_2$, displaying the characteristic out-of-plane (A_{1g}) and in-plane (E^1_{2g}) vibrational modes at ~ 230 cm^{-1} and ~ 246 cm^{-1}, respectively. **e, f** X-ray photoelectron spectroscopy (XPS) core-level spectra of the as-grown $NbSe_2$ for (e) Nb 3d and (f) Se 3d, confirming its chemical composition and oxidation states. **g** Schematic illustration of the structural transformation from (i) pristine CVD-grown $NbSe_2$ to (ii) a vertical NbO_x-$NbSe_2$ heterostructure via a controlled thermal oxidation (O_2 annealing) process. **h** Typical current–voltage ($I_{ds} - V_{ds}$) characteristics comparing the highly conductive metallic behavior of pristine $NbSe_2$ (blue line), oxidized $NbSe_2$ (black line) and the bipolar memristive switching behavior of the oxidized NbO_x-$NbSe_2$ device (red line). The insets depict the cross-sectional schematics of the respective devices. **i** Schematic illustration of the proposed filamentary switching mechanism. It highlights the dynamic formation (SET/LRS) and rupture (RESET/HRS) of oxygen vacancy-driven nanoscale conductive filaments within the insulating NbO_x layer, utilizing the underlying metallic $NbSe_2$ as a seamless bottom electrode

the current–voltage ($I_{ds} - V_{ds}$) curves (Fig. 1h), the pristine $NbSe_2$ exhibits a highly conductive metallic behavior (blue line), which is preserved even after its oxidation (black line). In contrast, the oxidized NbO_x–$NbSe_2$ device initially exhibits a high-resistance state (HRS) due to the insulating NbO_x layer, followed by a sharp SET transition to a low-resistance state (LRS) at a threshold voltage of ~ 1.5 V (red line), which clearly indicates the emergence of resistive switching properties.

The underlying mechanism for this memristive behavior is governed by the dynamic formation and rupture of nanoscale conductive filaments, as detailed in the structural schematic, Fig. 1i. In the pristine state, the oxidized NbO_x layer acts as a highly resistive switching barrier (HRS). Upon the application of an electric field (SET process), field-induced ion migration drives oxygen vacancies to self-assemble into dendritic conductive paths. Notably, rather than bridging the top electrodes through the lateral oxide gap, these filaments propagate vertically to interface with the underlying, unoxidized highly conductive $NbSe_2$ layer. In this configuration, the highly conductive metallic $NbSe_2$ serves seamlessly as an atomically flat bottom electrode that completes the circuit ("Filament connected via $NbSe_2$ switching the device to LRS"). During the RESET process, reversal of the voltage polarity induces vacancy redistribution, assisted by localized Joule heating, which ruptures the filamentary pathway near the electrode/NbO_x interface. As a result, the conductive path is disrupted, and the device returns to the non-volatile HRS. To further validate this filamentary conduction model, the corresponding $I_{ds} - V_{ds}$ characteristics have been fitted on a double-logarithmic scale, as presented in Fig. S5.

To explain the critical role of the metal-oxide interface in determining the resistive switching performance, we comparatively investigated two different top electrode integration methods: conventional thermal evaporation (Ev-MEM), and vdW metal transfer (T-MEM). Figure 2a and b schematically illustrate the fabrication processes and the resulting structural differences between the two architectures. During conventional thermal evaporation, the high-kinetic energy of the incoming Au atoms physically bombards the delicate surface of the device. As depicted in the magnified schematic (Fig. 2c), this high-energy metallization inevitably causes structural damage and atomic penetration into the ultra-thin NbO_x switching layer. In contrast, the vdW transferred electrode formed by gently stacking a prefabricated Au thin film onto the NbO_x surface by polydimethylsiloxane (PDMS) stamping method (details are provided in the Experimental Section and Figs. S6, S7). This process yields a chemically undisturbed, pristine interface that is bound solely by weak vdW forces.

The structural discrepancies between the two approaches were visually confirmed through cross-sectional high-resolution transmission electron microscopy (HR-TEM). For the device with the evaporated Au electrode (Fig. 2d), significant metallization-induced damage is clearly observed at the interface. The Au atoms penetrate the top region of the NbO_x layer, resulting in a remarkably uneven and degraded boundary (indicated by yellow arrows and dashed lines). This localized thinning and structural disruption of the NbO_x layer create unintended leakage pathways. In contrast, the HR-TEM image of the device with the transferred vdW Au electrode (Fig. 2e) reveals a highly uniform and damage-free interface between the Au electrode and the NbO_x layer, while perfectly preserving the layered crystalline structure of the underlying $NbSe_2$. Consequently, the physical integrity of the top interface directly governs the electrical characteristics and reliability of the memristors. Figure 2f compares the typical current–voltage ($I_{ds} - V_{ds}$) characteristics of both devices. The Ev-MEM (blue curve) exhibits a substantially elevated OFF-state current (10^{-7} A), leading to a severely degraded ON/OFF ratio of 10^2. This severe leakage is attributed to the high tunneling current through the thin NbO_x layer caused by the penetrating Au clusters. Conversely, the T-MEM (red curve) demonstrates exceptional switching characteristics, featuring a suppressed OFF-state current (10^{-9} A) and a high ON/OFF ratio of over 10^5 facilitated by the pristine insulating barrier.

The superiority of the damage-free vdW interface is further manifested in the long-term operational stability. During the pulse-induced endurance test (Fig. 2g), T-MEM maintains highly stable and distinguishable SET and RESET states for over 10^3 cycles without noticeable degradation. However, the Ev-MEM exhibits rapid deterioration, with its memory window severely degraded after a few hundred cycles. Furthermore, the retention characteristics (Fig. 2h) demonstrate that the T-MEM can stably retain high ON/OFF ratio of over 10^5 for more than 10^4 s, despite minor fluctuations. In contrast, Ev-MEM exhibits low and fluctuated ON/OFF ratio between 10 to 10^2, indicating a failure to hold the data stably. These results compellingly demonstrate that employing a vdW metal transfer technique to construct a damage-free interface is a crucial prerequisite for achieving reliable, high-performance NbO_x–$NbSe_2$ memristors. Device-to-device variability was further evaluated by comparing the switching characteristics of multiple devices, as shown in Figs. S8 and S9. The results confirm the reproducibility of the device operation and provide statistical support for the observed memristive behavior. In addition, $NbSe_2$ thickness dependence is evaluated using T-MEM devices with different flake thicknesses (Fig. S10). For ultrathin flakes (< 5 layers), the thermal

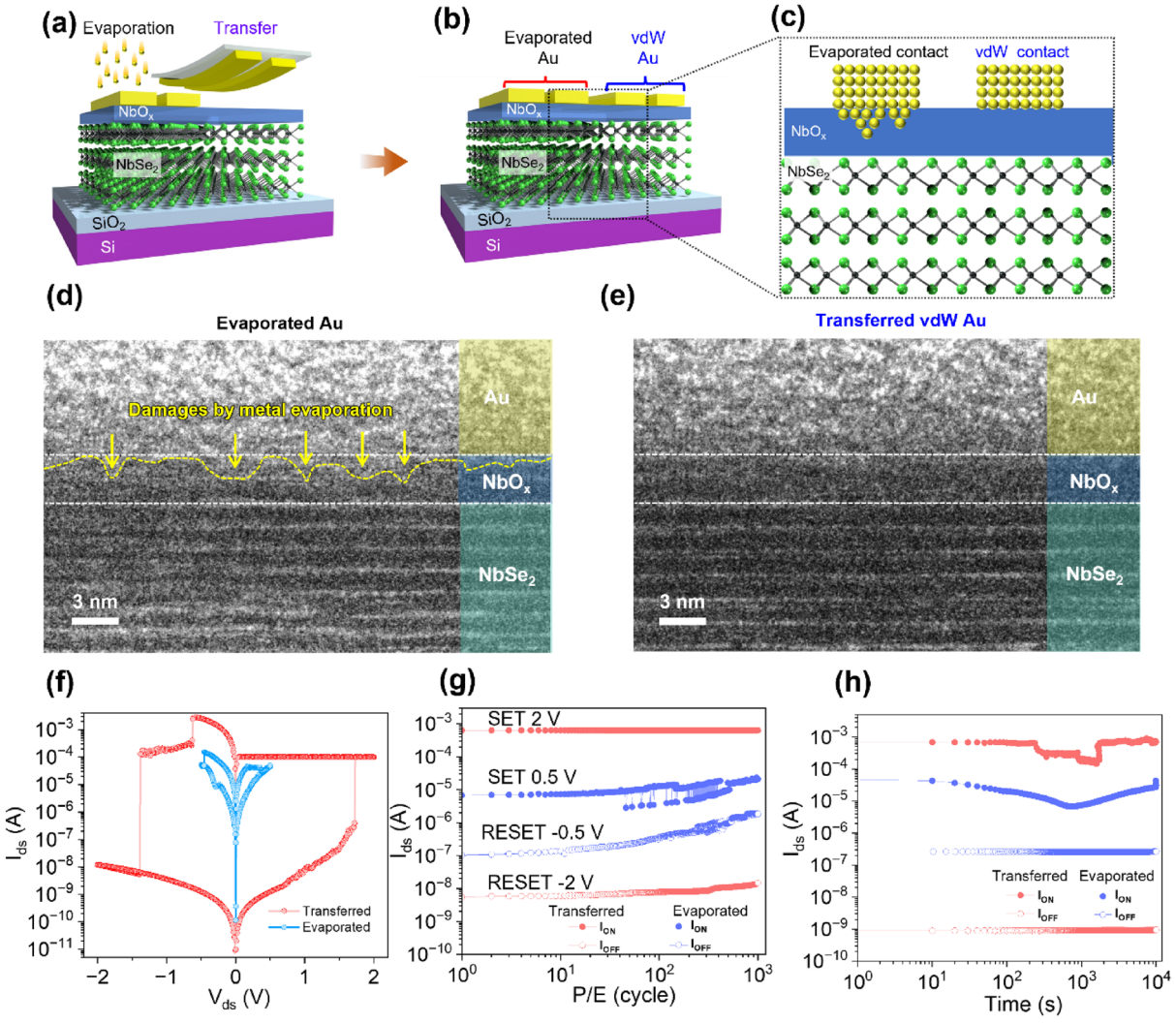


Fig. 2 Structural and electrical comparison of NbO_x-$NbSe_2$ memristors with evaporated versus vdW-transferred top electrodes. **a, b** Schematics illustrating the fabrication processes (**a**) and the resulting device architectures (**b**) for top metal electrodes integrated by conventional thermal evaporation (left) and vdW metal transfer (right). **c** Magnified atomic schematic comparing the metallization-induced damage and atomic penetration caused by evaporated contacts, with the chemically undisturbed, pristine interface achieved via vdW metal transfer. **d, e** Cross-sectional high-resolution transmission electron microscopy (HR-TEM) images of the metal/oxide interface for (**d**) the evaporated Au electrode device (Ev-MEM) and (**e**) the transferred vdW Au electrode device (T-MEM). The yellow arrows and dashed line in (**d**) indicate localized structural degradation and Au penetration into the ultrathin NbO_x layer, whereas (**e**) shows a highly uniform, damage-free interface. **f** Typical current–voltage ($I_{ds} - V_{ds}$) characteristics comparing the Ev-MEM (blue) and T-MEM (red). The T-MEM exhibits a significantly suppressed OFF-state leakage current and a superior ON/OFF ratio of 10^5. **g** Pulse-induced endurance characteristics over program/erase (P/E) cycles, demonstrating rapid degradation in the Ev-MEM and high stability in the T-MEM. **h** Long-term retention characteristics of the ON and OFF states for both devices, monitored for over 10^4 s

oxidation process consumed almost the entire flake, leaving no residual metallic underlayer to serve as the bottom electrode, giving minimal hysteresis. Therefore, such thin flakes are unsuitable for stable NbO_x–$NbSe_2$ memristor operation. Conversely, in the optimal thickness range (>6 layers), the oxidation process consumes only the topmost layers to form a pristine oxide barrier while leaving a highly conductive, atomically flat 2D metallic bottom electrode intact. Thus, varying the $NbSe_2$ thickness primarily determines whether a residual metallic electrode remains post-oxidation, rather than directly decoupling the top-interface effect.

To systematically evaluate the physical insight of interface effect on the electrical properties, we investigated the charge transport mechanisms of the memristors in their HRS prior to the SET transition. Figure 3 is used to describe the interfacial charge-injection process at the Au/NbO_x interface in the HRS before SET using the $\ln\left(I_{ds}/V_{ds}^2\right)$ versus $1/V_{ds}$ curve to identify DT and FNT behavior. After charge injection, carrier transport within

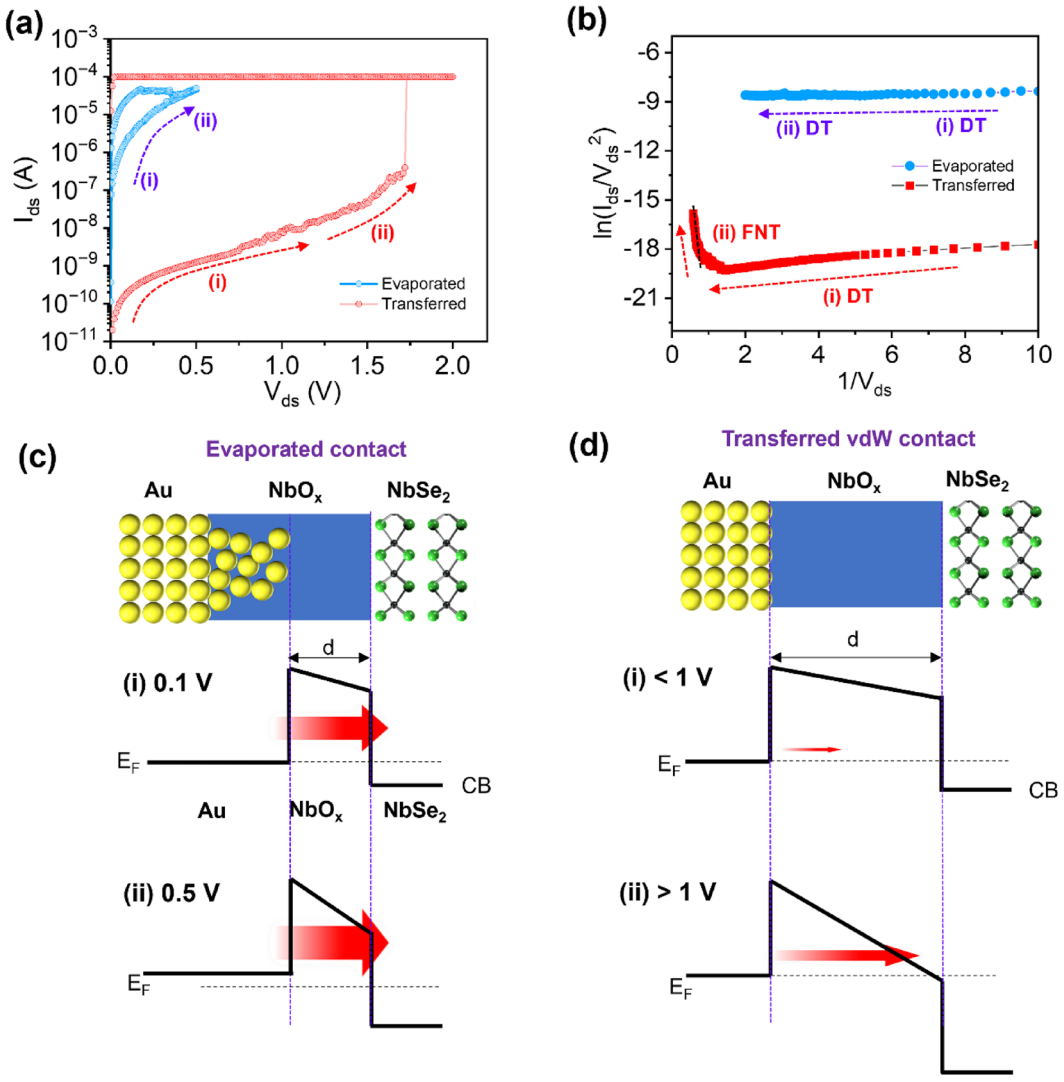


Fig. 3 Charge transport mechanisms and energy band diagrams of the metal/NbO_x interfaces. **a** Current–voltage ($I_{ds} - V_{ds}$) characteristics for the evaporated (Ev-MEM, blue) and transferred (T-MEM, red) devices in their HRS prior to the SET transition. **b** Corresponding tunneling analysis plots used to identify the dominant conduction mechanisms. Ev-MEM exhibits a flat profile across the entire sweep range, indicating dominant direct tunneling (DT). In contrast, T-MEM demonstrates a distinct transition from a low-electric-field DT regime (i) to a high-electric-field Fowler–Nordheim tunneling (FNT) regime (ii). **c, d** Structural schematics and corresponding energy band diagrams illustrating the charge transport mechanisms for (**c**) Ev-MEM and (**d**) T-MEM. In Ev-MEM (**c**), physical penetration of Au atoms reduces the effective barrier thickness, d, leading to severe and uncontrollable DT leakage even at low applied biases of 0.1 V (i) and 0.5 V (ii). In T-MEM (d), the full intrinsic barrier thickness is preserved, effectively suppressing leakage via a minimal background DT at low bias (< 1 V) (i). At higher bias (> 1 V) (ii), significant band bending enables field-driven FNT, facilitating a controlled and abrupt SET transition

the NbO_x bulk is governed by trap-controlled space-charge-limited conduction (SCLC), as shown in Fig. S5 using the $\log(I_{ds}) - \log(V_{ds})$ relationship during the positive and negative voltage sweep [36]. These processes operate in sequence: DT and FNT administers the initial carrier injection at the Au/NbO_x interfacial barrier, and trap-controlled SCLC subsequently guides the carrier transport within NbO_x that drives the filamentary SET transition. Figure 3 focuses on this interfacial injection mechanism to explain the difference in the off-currents between the transferred contact (T-MEM) and the evaporated contact (Ev-MEM).

Figure 3a displays the low-voltage regime of the $I_{ds} - V_{ds}$ curves for both Ev-MEM and T-MEM. Ev-MEM exhibits a severely high tunneling current (10^{-7}–10^{-5} A) at the narrow voltage sweep ranges (0–0.5 V), while T-MEM strictly suppresses the tunneling current (10^{-11}–10^{-7} A) at the wide voltage sweep ranges (0–1.7 V) until a threshold voltage is reached, whereupon a sharp SET transition occurs.

To identify the dominant conduction mechanisms governing these distinct behaviors, the $I_{ds} - V_{ds}$ data were replotted as $\ln\left(I_{ds}/V_{ds}^2\right)$ versus $1/V_{ds}$ (Fig. 3b).

Depending on the applied electric field and the effective barrier shape, the current density typically transitions between DT and FNT, which can be mathematically expressed by Eqs. (1) and (2), respectively [37].

$$I_{DT}(V) = \frac{A_{eff}\sqrt{m\varphi_B}q^2V_{ds}}{h^2 d} exp\left[\frac{-4\pi d\sqrt{m^*\varphi_B}}{h}\right] \quad (1)$$

$$I_{FNT}(V) = \frac{A_{eff}q^3 m V_{ds}^2}{8\pi h\varphi_B d^2 m^*} exp\left[\frac{-8\pi d\sqrt{2m^*}\varphi_B^{3/2}}{3hqV_{ds}}\right] \quad (2)$$

where A_{eff}, φ_B, q, m, m^*, d, and h are the effective contact area, barrier height, electron charge, free electron mass, effective electron mass, barrier width (NbO_x thickness), and Planck's constant, respectively. In this plot, a voltage-independent horizontal line signifies DT, whereas a negatively sloped linear region is the classic signature of FNT. For the Ev-MEM, the plot remains entirely flat across the measured voltage range, indicating that DT is the sole conduction mechanism. Conversely, the T-MEM (red curve) exhibits two distinct regimes: a flat DT region at low electric fields (high $1/V_{ds}$), followed by a steep transition to FNT at higher electric fields (low $1/V_{ds}$).

These vastly different transport behaviors can be thoroughly explained by the energy band diagrams at the metal/NbO_x interfaces (Fig. 3c and d). For Ev-MEM (Fig. 3c), the physical penetration of Au atoms structurally damages and effectively reduces the thickness (d) of the NbO_x insulating barrier. Because the barrier is severely thinned, electrons can easily traverse the narrowed trapezoidal barrier via DT even at minimal applied biases (e.g., 0.1 V to 0.5 V). This unimpeded tunneling pathway accounts for the high OFF-state leakage current and the premature, uncontrollable switching observed in the evaporated devices.

In contrast, the T-MEM (Fig. 3d) preserves the physical and chemical integrity of the NbO_x layer, maintaining its full original thickness (d). At a low bias (< 1 V, Fig. 3d–i), the thick and pristine barrier effectively blocks electron transport, restricting the conduction to a negligible background DT current and yielding a highly insulating OFF-state. As the applied voltage increases to the threshold level (> 1 V, Fig. 3d–ii), the strong localized electric field causes significant energy band bending in the NbO_x layer. This band bending reshapes the rectangular barrier into a sharp triangular potential barrier, sufficiently narrowing the tunneling width at the tip to allow electrons to tunnel through via the FNT mechanism. This field-induced FNT process enables the precise and abrupt injection of charges required to initiate the filament formation, resulting in a controlled and sharp SET transition. Consequently, these band-alignment analyses decisively corroborate that preserving the intrinsic barrier thickness via vdW metal transfer is fundamentally essential for realizing reliable, field-driven memristive switching.

It is to be noted that the overall charge transport is a series combination of charge injection at the metal/NbO_x interface and subsequent conduction through the bulk layer. While FNT governs the charge injection across the interface, SCLC dictates the bulk conduction and the switching process as injected charges fill the oxygen vacancy traps. At low electric fields in the High Resistance State (HRS) (V_{ds} < 1 V), the current is primarily limited by the potential barrier at the metal/NbO_x interface. As the applied voltage increases, the barrier becomes triangular, leading to a transition from DT to FNT (Fig. 3). As the applied voltage increases further towards the threshold voltage (V_{ds} > 1 V), a massive number of electrons are injected into the bulk NbO_x via FNT. At this stage, the transport bottleneck shifts from the interface to the bulk of the NbO_x layer (Fig. S5). The bulk contains abundant oxygen vacancies acting as deep trap states. The injected carriers gradually fill these traps, causing the transport to be governed by trap-controlled SCLC. When all traps are entirely filled, an abrupt current jump occurs (Trap-Filled Limit, TFL), triggering the SET process.

The physical origin of this difference is further quantified by estimating the NbO_x barrier thickness and Schottky barrier height (SBH). From the cross-sectional TEM images in Fig. 2, the effective barrier thicknesses of T-MEM and Ev-MEM were estimated to be approximately 3 nm and 1.3 nm, respectively. The SBH of T-MEM and Ev-MEM in the HRS are calculated to 0.665 eV and 0.438 eV, respectively. The SBH is commonly estimated from the $I_{ds} - V_{ds}$ characteristics by determining the saturation current through extrapolating the logarithmic $I_{ds} - V_{ds}$ curve to $V_d = 0$ [38–40]. The corresponding extraction plots and details are provided in Fig. S11 and Table T1 in the Supplementary Information.

To evaluate the feasibility of the NbO_x–$NbSe_2$ memristors for analog neuromorphic computing, we investigated their long-term potentiation (LTP) characteristics. Figure 4a compares the normalized synaptic weight updates of the evaporated and transferred devices in response to a sequence of 1000 potentiation pulses, applied at 0.5 V/10 ms for Ev-MEM and 2 V/10 ms for T-MEM. The current at each conductance level is normalized and fitted using the synaptic conduction (G) equation: $\Delta G = \alpha e^{-\beta\frac{G-G_{min}}{G_{max}-G_{min}}}$, where the α and β indicate the value of conductance change and non-linearity factor (NLF), respectively. The ideal artificial synapse requires a linear and gradual conductance change ($\beta = 0$) to ensure accurate weight updates during network training. T-MEM demonstrates a highly linear and progressive

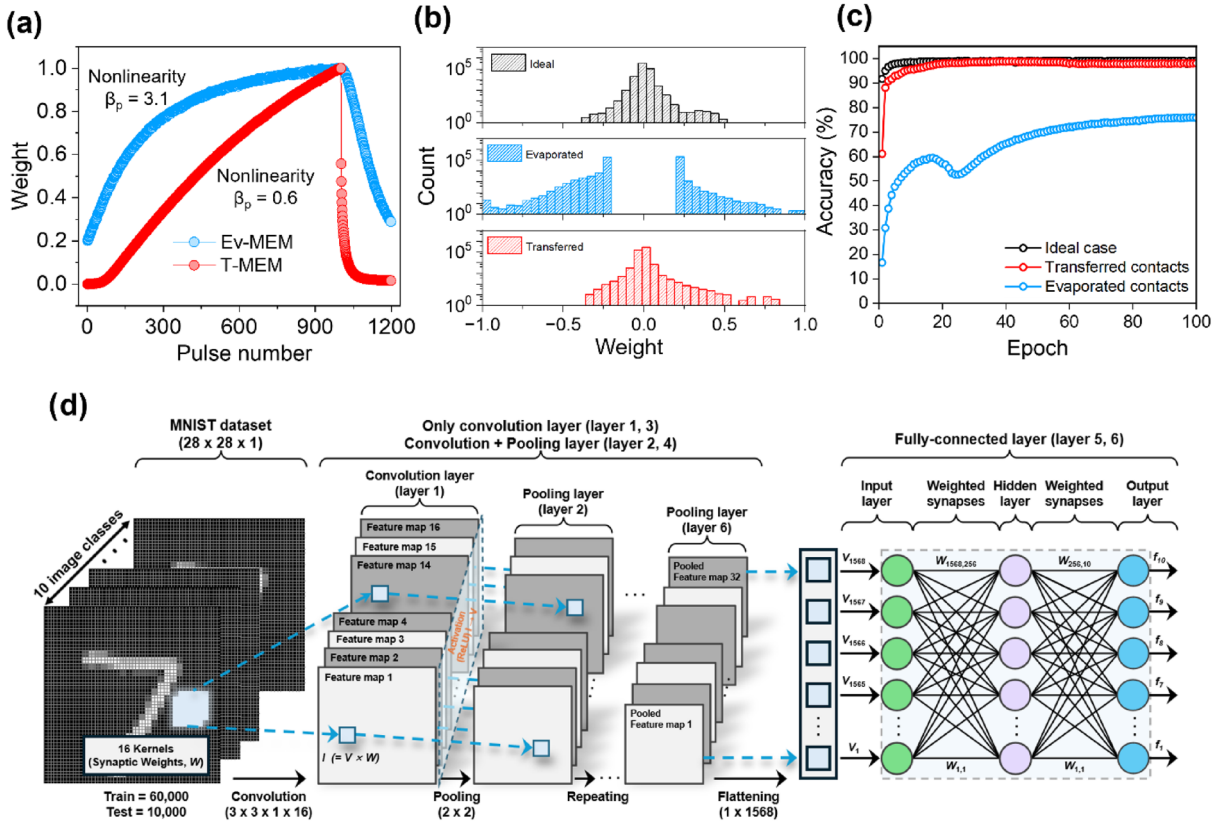


Fig. 4 Synaptic weight update characteristics and neuromorphic computing simulations for MNIST image recognition. **a** Long-term potentiation (LTP) characteristics showing the normalized synaptic weight updates as a function of the applied pulse number. T-MEM (red) exhibits highly linear weight modulation for potentiation (NLF, $\beta_p = 0.6$) and utilizes a full dynamic range (0–1). In contrast, Ev-MEM (blue) shows strong nonlinearity (NLF = 3.1) and a restricted dynamic range (0.2–1) due to its high OFF-state current. **b** Statistical distributions of the trained synaptic weights after network learning for the ideal software-based model, Ev-MEM model, and T-MEM model. The restricted dynamic range of the evaporated device prevents population of the near-zero weight region (creating a gap between approximately − 0.2 and 0.2), whereas the transferred device successfully replicates the continuous, symmetric distribution of the ideal model. **c** Simulated MNIST image-recognition accuracy over 100 training epochs. By virtue of its linear weight updates and full dynamic range, T-MEM achieves a near-ideal recognition accuracy of 98.1%, significantly outperforming Ev-MEM (75.8%). **d** Schematic architecture of the convolutional neural network (CNN) used for the neuromorphic simulation. The network consists of sequential convolution and pooling layers for spatial feature extraction, followed by a flattening layer and fully connected layers for the final digit classification

weight modulation with an excellent nonlinearity factor of $\beta_p = 0.6$, outperforming Ev-MEM ($\beta_p = 3.1$) and thereby ensuring accurate weight updates during network training. In addition. T-MEM and Ev-MEM exhibit NLF, $\beta_d = 1.7$ and 5 for depression curve, respectively. Furthermore, T-MEM utilizes the full dynamic range (normalized weight range of 0–1), owing to its high ON/OFF ratio (10^5). Conversely, Ev-MEM shows a limited dynamic range (weight range of 0.2–1). This limitation arises from the high off-state current, which prevents the device from representing low-weight states (values near 0).

The impact of these device characteristics on system performance was simulated using the CNN simulation for the classification of the MNIST handwritten digit dataset (Fig. 4c and d). The network consists of sequential convolution and pooling layers to extract spatial feature maps, followed by a flattening layer and fully connected layers for final digit classification. The experimentally extracted device parameters, including the nonlinearity factors (β) and dynamic range, were directly incorporated into the synaptic weight update algorithms of this simulation. The profound impact of dynamic range on network training is clearly visualized in the statistical distribution of the trained synaptic weights (Fig. 4b). For optimal learning, a network requires a continuous and symmetric weight distribution centered around zero, as seen in the 'Ideal' software-based model (black histogram). The simulation using the transferred device parameters (red histogram) successfully replicates this ideal continuous distribution, proving that its wide dynamic range (0–1) is sufficient for fine-tuning intermediate weights. Conversely, the Ev-MEM (blue histogram) completely fails to populate the near-zero weight region (from -0.2 to 0.2), which is a direct consequence of its restricted dynamic range in the OFF state. Consequently, the T-MEM

based system achieves a high image recognition accuracy (98.1%), almost identical to the ideal case (99.1%). In contrast, the Ev-MEM based system suffers from significant performance degradation (75.8%), demonstrating that the high ON/OFF ratio and linear update capability enabled by transferred electrode are essential for reliable neuromorphic computing. Table T2 presents a comprehensive benchmarking of the proposed damage-free vdW integrated NbO_x-$NbSe_2$ memristor against previously reported Nb- and TMD-based memristive devices. As summarized in the table, conventional devices lacking a damage-free interface-including the evaporated counterpart (Ev-MEM) developed in this work, frequently suffer from severe OFF-state leakage and restricted ratios due to metallization-induced barrier degradation. In stark contrast, by utilizing a transferred vdW top contact, our device fully preserves the structural integrity of the ultra-thin NbO_x barrier. This effectively suppresses background DT, yielding a highly insulating OFF-state and a superior ratio of 10 [5]. Furthermore, while prior literature (Table T1) indicates a persistent trade-off between reliable memory retention, mechanical flexibility, and synaptic precision, the T-MEM simultaneously excels across all these metrics. It combines robust non-volatile data retention ($>10^4$ s) with verified mechanical flexibility; a combination rarely achieved in existing platforms. Ultimately, the high ON/OFF ratio and linear synaptic weight updates enabled by the pristine interface directly translate to an outstanding hardware-aware MNIST recognition accuracy of 98.1%, demonstrating a significant leap in performance over both its evaporated baseline (75.8%) and other state-of-the-art memristors. To further support the analog synaptic functionality, repeated LTP/LTD cycling, multilevel conductance modulation, and retention of intermediate states were evaluated. The device exhibits reversible potentiation/depression behavior and gradual conductance tuning from LRS to HRS under negative depression pulses. The programmed intermediate states remain distinguishable over time, confirming their suitability for analog synaptic weight representation. The detailed results are provided in Fig. S12.

Leveraging the physically intact vdW interface and the inherently pliable nature of the 2D $NbSe_2$ crystal, we further evaluated the feasibility of our memristors for flexible and wearable neuromorphic applications. The NbO_x–$NbSe_2$ memristor arrays utilizing the vdW transferred top electrodes were successfully fabricated on a transparent and flexible polymer substrate polyethylene terephthalate (PET). Figure 5a displays an optical photograph of the highly flexible device array bent between fingers, with the inset showing a magnified optical micrograph of a single functioning memristor cell. Unlike conventional evaporated electrodes, which physically penetrate the oxide and create rigid, brittle defect sites that easily crack under stress, the vdW transferred electrodes smoothly conform to the substrate's deformation without compromising the ultra-thin NbO_x switching barrier. Figure S13 contains optical photograph and micrograph images of CVD-grown $NbSe_2$ flakes after transfer onto PET substrate.

To quantitatively assess the mechanical tolerance of the device, we measured its electrical characteristics under varying degrees of mechanical strain. Figure 5b presents the current–voltage ($I_{ds} - V_{ds}$) switching curves measured at different static bending angles ranging from 0° (flat) to 30°. Remarkably, the bipolar resistive switching behavior remains highly uniform across all bending states. Neither the operating voltage nor the resistance states show any severe degradation, proving that the structural integrity of the NbO_x tunneling barrier and the conductive filament formation process are perfectly preserved under static bending stress. Furthermore, we rigorously investigated the dynamic mechanical fatigue resistance of the flexible memristor by subjecting it to repeated bending cycles at a severe angle of 30°. As illustrated in Fig. 5c, both the SET and RESET threshold voltages exhibit outstanding stability, tightly fluctuating around ~ 0.2 V and ~ -0.3 V, respectively, without any noticeable voltage drift over 200 continuous bending cycles. Similarly, Fig. 5d demonstrates the reliable ON and OFF current during the cyclic fatigue test. Although a minor initial relaxation is observed in the ON-current, both the ON and OFF- currents stabilize, reliably maintaining a distinct ON/OFF ratio.

In addition, bending-stability measurements were performed to evaluate the mechanical robustness of the native $NbSe_2$ flake (Fig. S14). The nearly overlapping $I_{ds} - V_{ds}$ curves measured under different bending angles indicate that the flake maintains stable electrical behavior under mechanical deformation, confirming the flexibility and mechanical stability of the residual $NbSe_2$ bottom electrode.

3 Conclusion

In conclusion, we have successfully realized a highly reliable and mechanically robust artificial synapse based on a vertical NbO_x–$NbSe_2$ heterostructure by employing a damage-free vdW metal transfer technique. Our comparative investigation reveals that preserving the structural and chemical integrity of the ultra-thin native oxide is fundamentally critical for controlling the charge transport mechanism. While conventional high-energy metallization inflicts interfacial damage that triggers uncontrollable DT and severe leakage, the gently laminated vdW electrode maintains a pristine barrier. This structural preservation effectively suppresses the background leakage and enables a precise, field-driven FNT mechanism, leading to highly controlled memristive

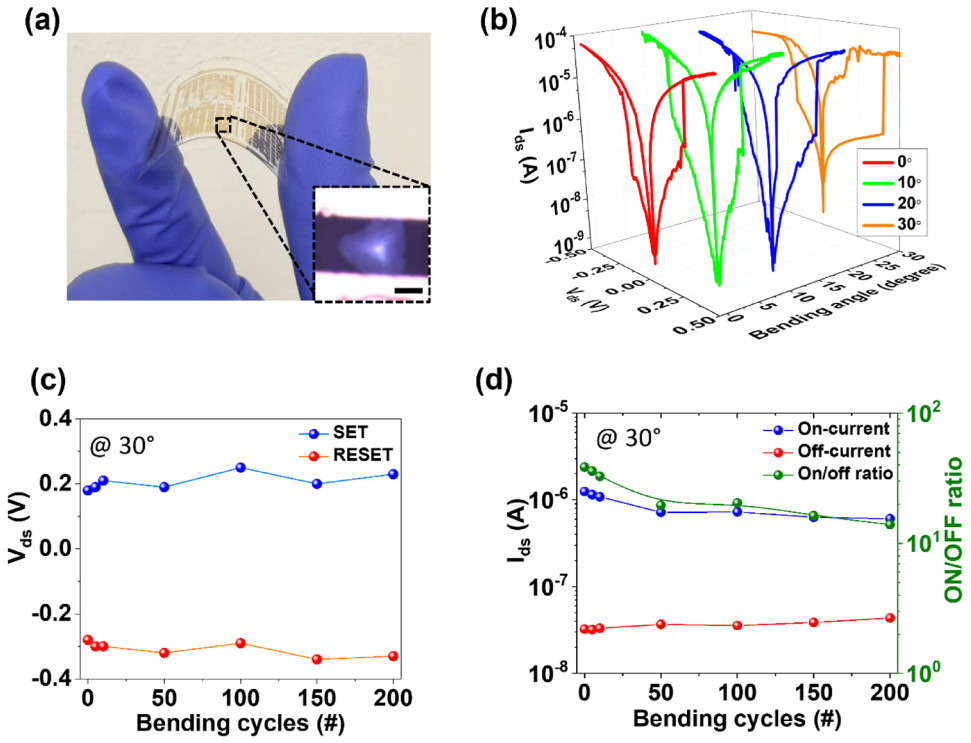


Fig. 5 Mechanical flexibility and robustness of the vdW-transferred NbO_x-$NbSe_2$ memristors on a polymer substrate. **a** Optical photograph of the highly flexible memristor device array fabricated on a transparent polymer (PET) substrate, shown bent between fingers. The inset shows a magnified optical micrograph of a single functioning memristor cell. Scale bar shown in the microscopic image is 5 μm. **b** Current–voltage ($I_{ds} - V_{ds}$) resistive switching curves measured at different static bending angles ranging from 0° (flat) to 30°, demonstrating highly uniform electrical performance and the preservation of the NbO_x tunneling barrier under static strain. **c** Dynamic mechanical fatigue characteristics, showing stable SET and RESET threshold voltages without noticeable change over 200 continuous bending cycles at a bending angle of 30°. **d** Evolution of the ON-current, OFF-current, and the corresponding ON/OFF ratio during the 200 cyclic bending tests at 30°, confirming reliable memory operation and the mechanical durability of the damage-free vdW interface

switching. Consequently, the vdW-integrated devices exhibit exceptional operational stability, an expanded dynamic range, and highly linear synaptic weight modulation. These optimized synaptic characteristics directly translate into near-ideal learning and pattern recognition capabilities in hardware-aware neuromorphic network simulations. Furthermore, capitalizing on the seamless vdW interface and the inherent pliability of 2D materials, the fabricated memristors demonstrate outstanding mechanical durability, maintaining stable switching behaviors under continuous bending stress without performance degradation. Ultimately, our findings establish that ensuring a damage-free metal/oxide interface through vdW integration is a pivotal strategy for advancing highly accurate, reliable, and flexible next-generation neuromorphic hardware.

4 Experimental section

4.1 Synthesis of $NbSe_2$ flake via CVD method

Initially, ammonium niobium oxalate (ANO, Sigma-Aldrich) was employed as the niobium (Nb) precursor. A stock solution of Nb was prepared by dissolving a predetermined amount of ANO powder in deionized (DI) water (0.3 g/10 ml). Sodium hydroxide (NaOH) served as a promoter, and a medium solution of iodixanol (Opti Prep density gradient medium, Sigma Aldrich) was added to enhance adhesion between the solution and the growth substrate during the liquid source coating process. These components were combined in precise proportions and uniformly mixed at 300 rpm to attain a homogeneous solution phase. Subsequently, the mixed solution was deposited onto SiO_2/Si substrate via spin-coating at 3500 rpm for 1 min. The coated substrate underwent annealing at 500 °C for 30 min in ambient air to convert ANO into Nb_2O_5 and to remove carbon residues from OptiPrep. The coated substrate was then positioned on a ceramic plate and placed at the center of the quartz tube within a CVD chamber. Solid Selenium (Se) was positioned at the entrance region, 17 cm away from the center of the quartz tube. The temperature was maintained at 380 °C at the Se source location, while the growth reaction occurred at 800 °C for 20 min under a flow of 300 sccm N_2 and 20 sccm H_2 gas, serving as a carrier gas throughout the growth process (Fig S1, Supporting Information). Finally, the chamber was rapidly cooled

by opening the furnace upon completion of the synthesis process.

4.2 Electrode transfer

Before fabrication of transferred metal-contact devices, the CVD-grown $NbSe_2$ flakes are transferred on a clean SiO_2 substrate using the standard hydrofluoric acid (HF) assisted wet layer transfer. Subsequently, $NbSe_2$ is annealed in thermal CVD in the presence of oxygen for 30 min, which leads to formation of NbO_x–$NbSe_2$ heterostructure. Subsequently, a series of metal (Au) electrodes is pre-fabricated on a silicon substrate using photolithography and conventional metal deposition technique, electron beam evaporation. A PDMS stamp was physically laminated onto the substrate to mechanically pick up and transfer the pre-patterned electrodes. The released metal electrodes were then aligned under an optical microscope and laminated onto the CVD-grown $NbSe_2$ flakes using a dry-transfer system, forming non-damaging vdW metal contacts with an atomically sharp and clean metal–semiconductor interface. Finally, the PDMS stamp covering the contact pads is mechanically released from the substrate, leaving the metal pads exposed for probing and electrical measurements.

4.3 Material characterization

An optical microscope (Axio Imager 2, Carl Zeiss) was used to capture the optical microscopic images of the CVD-grown $NbSe_2$ films and their fabricated devices. The structure and morphology of the films was analyzed through an atomic force microscope (AFM; NX 10, Park System). Cross–sectional TEM samples were prepared on a copper grid using a focused ion beam (He-lios 5 UX, ThermoFisher Scientific) system and images were acquired using transmission electron microscope (TEM; JEOL, JEM ARM 200F). Elemental analysis was conducted via X-ray photoelectron spectroscope (ESCALAB 250, Thermo Fisher) and Raman scattering measurements were conducted using a Nanobase spectrometer integrated with an Olympus optical microscope, utilizing a 532 nm laser for excitation. Electrical and photocurrent characteristics were measured using a semiconductor device analyzer (B1500A, Keysight) at room temperature.

4.4 CNN simulations

The integrated benchmarking platform DNN + NeuroSim, developed to evaluate compute-in-memory (CIM) accelerators for deep neural network applications, was employed for system-level performance assessment. The implemented CNN architecture consists of a feature extraction module and a classification module, as illustrated in Fig. 4d. The MNIST dataset, consisting of 60,000 training and 10,000 testing grayscale images of handwritten digits with a size of $28 \times 28 \times 1$, was used for the simulation. The CNN consisted of two convolutional layers, two pooling layers, and two fully connected layers. In the first convolutional layer, 16 kernels of size $3 \times 3 \times 1$ were used to generate feature maps, followed by 2×2 pooling. The same convolution–pooling process was repeated to extract higher-level features. For hardware-aware simulation, image pixels were represented as input voltage signals, while kernel weights were mapped to synaptic conductance values. Experimentally measured device parameters, including conductance dynamic range, nonlinearity, number of conductance states, and minimum/maximum conductance, were incorporated into the model. During feed-forward propagation, output currents were calculated using Ohm's law, $I = V \times W$, followed by ReLU activation and max-pooling. After the final pooling layer, the feature maps were flattened into a 1×1568 vector and passed through two fully connected synaptic layers to classify digits from 0 to 9. During back-propagation, synaptic weights were iteratively updated based on the output error. After training, inference was performed using 10,000 test images, and the recognition accuracy of devices with transferred and thermally evaporated metal contacts was compared.

Supplementary Information

The online version contains supplementary material available at https://doi.org/10.1186/s40580-026-00569-7.

Supplementary Material 1.

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Author contributions

W.J.Y., P.A., and T.L.P. conceived the research, designed the experiments and wrote the manuscript. P.A. contributed to material synthesis, device fabrication, morphological and electrical characterizations. M.C.N., and D.X.D. performed the oxidation process, and assisted with the metal transfer process. V.T.V. contributed to CVD growth of $NbSe_2$ and materials characterization. T.T.H.V. assisted in device fabrication and characterization. H.W.Y. performed simulations. H.L., J.L., and M.C.L, assisted with manuscript editing and analysis of the experimental results. All authors read and approved the final manuscript.

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Data availability
The datasets used and/or analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Competing interests
The authors declare that they have no competing interests.

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References

1. Z. Wang, H. Wu, G.W. Burr, C.S. Hwang, K.L. Wang, Q. Xia, J.J. Yang, Resistive switching materials for information processing. Nat. Rev. Mater. **5**(3), 173–195 (2020). https://doi.org/10.1038/s41578-019-0159-3
2. A. Sebastian, M. Le Gallo, R. Khaddam-Aljameh, E. Eleftheriou, Memory devices and applications for in-memory computing. Nat. Nanotechnol. **15**(7), 529–544 (2020). https://doi.org/10.1038/s41565-020-0655-z
3. F. Aguirre, A. Sebastian, M. Le Gallo, W. Song, T. Wang, J.J. Yang, W. Lu, M.F. Chang, D. Ielmini, Y. Yang, A. Mehonic, A. Kenyon, M.A. Villena, J.B. Roldán, Y. Wu, H.H. Hsu, N. Raghavan, J. Suñé, E. Miranda, A. Eltawil, G. Setti, K. Smagulova, K.N. Salama, O. Krestinskaya, X. Yan, K.W. Ang, S. Jain, S. Li, O. Alharbi, S. Pazos, M. Lanza, Hardware implementation of memristor-based artificial neural networks. Nat. Commun. **15**(1), 1974- (2024). https://doi.org/10.1038/s41467-024-45670-9
4. A. Mehonic, A.J. Kenyon, Brain-inspired computing needs a master plan. Nature **604**(7905), 255–260 (2022). https://doi.org/10.1038/s41586-021-04362-w
5. B. von Neumann, Nat. Nanotechnol. **15**(7), 507–507 (2020). https://doi.org/10.1038/s41565-020-0738-x
6. X. Duan, Z. Cao, K. Gao, W. Yan, S. Sun, G. Zhou, Z. Wu, F. Ren, B. Sun, Memristor-based neuromorphic chips. Adv. Mater. **36**(14), 2310704 (2024). https://doi.org/10.1002/ADMA.202310704
7. S.O. Park, H. Jeong, J. Park, J. Bae, S. Choi, Experimental demonstration of highly reliable dynamic memristor for artificial neuron and neuromorphic computing. Nat. Commun. **13**(1), 2888- (2022). https://doi.org/10.1038/s41467-022-30539-6
8. W. Chen, L. Song, S. Wang, Z. Zhang, G. Wang, G. Hu, S. Gao, Essential characteristics of memristors for neuromorphic computing. Adv. Electron. Mater. **9**(2), 2200833 (2023). https://doi.org/10.1002/AELM.202200833
9. S. Ji, J. Kim, J. Hong, J. Choi, S. Yun, A.K. Katiyar, F. Niklaus, J.H. Ahn, 2D material-based memristor arrays for flexible and thermally stable neuromorphic applications. Small (2025). https://doi.org/10.1002/SMLL.202507845
10. X.Q. Ma, G. Ding, W. Niu, Z. Jia, S.T. Han, C.C. Kuo, Y. Zhou, Flexible neuromorphic devices based on two-dimensional transition metal dichalcogenides. IEEE J. Flex. Electron. **3**(1), 10–28 (2024). https://doi.org/10.1109/JFLEX.2023.3298593
11. B. Wang, H. Luo, X. Wang, E. Wang, Y. Sun, Y.C. Tsai, H. Zhu, P. Liu, K. Jiang, K. Liu, Bifunctional NbS_2-based asymmetric heterostructure for lateral and vertical electronic devices. ACS Nano **14**(1), 175–184 (2019). https://doi.org/10.1021/ACSNANO.9B06627
12. A. Daus, S. Vaziri, V. Chen, Ç. Köroğlu, R.W. Grady, C.S. Bailey, H.R. Lee, K. Schauble, K. Brenner, E. Pop, High-performance flexible nanoscale transistors based on transition metal dichalcogenides. Nat. Electron. **4**(7), 495–501 (2021). https://doi.org/10.1038/s41928-021-00598-6
13. Y. Cai, J. Yang, Y. Hou, F. Wang, L. Yin, S. Li, Y. Wang, T. Yan, S. Yan, X. Zhan, J. He, Z. Wang, 8-bit states in 2D floating-gate memories using gate-injection mode for large-scale convolutional neural networks. Nat. Commun. **16**(1), 2649- (2025). https://doi.org/10.1038/s41467-025-58005-z
14. Q.A. Vu, Y.S. Shin, Y.R. Kim, V.L. Nguyen, W.T. Kang, H. Kim, D.H. Luong, I.M. Lee, K. Lee, D.S. Ko, J. Heo, S. Park, Y.H. Lee, W.J. Yu, Two-terminal floating-gate memory with van der waals heterostructures for ultrahigh on/off ratio. Nat. Commun. **7**(1), 12725- (2016). https://doi.org/10.1038/ncomms12725
15. Q.A. Vu, H. Kim, V.L. Nguyen, U.Y. Won, S. Adhikari, K. Kim, Y.H. Lee, W.J. Yu, A high-on/off-ratio floating-gate memristor array on a flexible substrate via CVD-grown large-area 2D layer stacking. Adv. Mater. **29**(44), 1703363 (2017). https://doi.org/10.1002/ADMA.201703363
16. U.Y. Won, Q. An Vu, S.B. Park, M.H. Park, V. Dam Do, H.J. Park, H. Yang, Y.H. Lee, W.J. Yu, Multi-neuron connection using multi-terminal floating–gate memristor for unsupervised learning. Nat. Commun. **14**(1), 3070- (2023). https://doi.org/10.1038/s41467-023-38667-3
17. P. Aggarwal, H. Sheoran, P. Bisht, O.K. Prasad, C.H. Chung, E.Y. Chang, B.R. Mehta, R. Singh, Synthesis of a large area ReS2 thin film by CVD for in-depth investigation of resistive switching: effects of metal electrodes, channel width and noise behaviour. Nanoscale **15**(34), 14109–14121 (2023). https://doi.org/10.1039/D3NR02566G
18. K.J. Ahn, D.K. Yun, M.H. Park, H.W. Yun, M.C. Nguyen, V.T. Vu, H. Li, P. Aggarwal, W.J. Yu, Synthesis of amorphous-crystalline mixture boron nitride for balanced resistive switching operation. Small (2025). https://doi.org/10.1002/SMLL.202503877
19. E. Hwang, D. Kim, N. Kim, H. Hong, C.Y. Heo, W. Cho, H.Y. Yoo, K. Watanabe, T. Taniguchi, H. Yang, Ferroelectric-induced phase change device with polymorphic Mo1-XWxTe_2 for neuromorphic computing. Small (2025). https://doi.org/10.1002/SMLL.202505378
20. W.K. Kim, G.Y. Cho, T.T.H. Vu, J.S. Son, Y.H. Shin, H.W. Yun, M.S. Kim, Y.S. Shin, H. Yang, W.J. Yu, Robust metal and semiconductor phase transition memristor using Ag-intercalated transition metal dichalcogenide. Adv. Mater. **38**(5), e16115 (2025). https://doi.org/10.1002/ADMA.202516115
21. W.K. Kim, Y.H. Shin, N. Kim, J.H. Lee, H. Cho, J.H. Lee, M.C. Nguyen, W.J. Yu, Room-temperature ferromagnetism in semimetallic Co-intercalated $MoTe_2$. Appl. Surf. Sci. **672**, 160706 (2024). https://doi.org/10.1016/J.APSUSC.2024.160706
22. W.K. Kim, N. Kim, M.H. Park, Y.H. Shin, G.Y. Cho, G. Kim, W.J. Yu, High electrical conductance in magnetic emission junction of Fe_3GeTe_2/ZnO/Ni heterostructure via selective spin emission through ZnO ohmic barrier. Adv. Mater. **37**(3), 2409822 (2025). https://doi.org/10.1002/ADMA.202409822
23. S. Park, D. Lee, J. Kang, H. Choi, J.H. Park, Laterally gated ferroelectric field effect transistor (LG-FeFET) using α-In_2Se_3 for stacked in-memory computing array. Nat. Commun. **14**(1), 6778 (2023). https://doi.org/10.1038/S41467-023-41991-3;TECHMETA
24. I.-J. Kim, J.-S. Lee, I.-J. Kim, J.-S. Lee, Ferroelectric transistors for memory and neuromorphic device applications. Adv. Mater. **35**(22), 2206864 (2023). https://doi.org/10.1002/ADMA.202206864
25. J.E. Kim, V.T. Vu, T.T.H. Vu, T.L. Phan, Y.R. Kim, W.T. Kang, K. Kim, Y.H. Lee, W.J. Yu, A non-volatile memory based on NbOx/$NbSe_2$ van der Waals heterostructures. Appl. Sci. **10**(21), 7598 (2020). https://doi.org/10.3390/APP10217598
26. C. Xiong, F. Tang, M. Xu, J. Shen, Y. Li, K.H. Xue, M. Xu, X. Miao, Natively oxidized 2D $NbSe_2$ enables ultralow-power electrical switching. J. Mater. Chem. C **13**(12), 6095–6103 (2025). https://doi.org/10.1039/D4TC04697H
27. U. Byun, H. Na, S. Kim, Universal neuromorphic element: NbOx memristor with co-existing volatile, non-volatile, and threshold switching. Adv. Funct. Mater. **36**(15), e19431 (2025). https://doi.org/10.1002/ADFM.202519431
28. D. Ju, S. Kim, Versatile NbOx-based volatile memristor for artificial intelligent applications. Adv. Funct. Mater. **34**(49), 2409436 (2024). https://doi.org/10.1002/ADFM.202409436
29. J.H. Lee, S.G. Choi, J.W. Lee, Van der Waals metal contacts for electronic and optoelectronic devices. ACS Appl. Electron. Mater. **5**(4), 1903–1925 (2023). https://doi.org/10.1021/ACSAELM.2C01789
30. W. Zheng, B. Yuan, M.A. Villena, K. Zhu, S. Pazos, Y. Shen, Y. Yuan, Y. Ping, C. Liu, X. Zhang, X. Zhang, M. Lanza, The origin and mitigation of defects induced by

metal evaporation in 2D materials. Mater. Sci. Eng. R. Rep. **160**, 100831 (2024). https://doi.org/10.1016/J.MSER.2024.100831
31. X. Zhang, C. Huang, Z. Li, J. Fu, J. Tian, Z. Ouyang, Y. Yang, X. Shao, Y. Han, Z. Qiao, H. Zeng, Reliable wafer-scale integration of two-dimensional materials and metal electrodes with van der waals contacts. Nat. Commun. **15**(1), 4619 (2024). https://doi.org/10.1038/s41467-024-49058-7
32. Y. Liu, J. Guo, E. Zhu, L. Liao, S.J. Lee, M. Ding, I. Shakir, V. Gambin, Y. Huang, X. Duan, Approaching the Schottky–Mott limit in van der Waals metal-semiconductor junctions. Nature **557**(7707), 696–700 (2018). https://doi.org/10.1038/s41586-018-0129-8
33. P. Chen, T.L. Atallah, Z. Lin, P. Wang, S.J. Lee, J. Xu, Z. Huang, X. Duan, Y. Ping, Y. Huang, J.R. Caram, X. Duan, Approaching the intrinsic exciton physics limit in two-dimensional semiconductor diodes. Nature **599**(7885), 404–410 (2021). https://doi.org/10.1038/s41586-021-03949-7
34. B. Wang, B. Ma, K. Wang, H. Zhang, Z. Zhang, T. Song, S. Wang, M. Chen, S. Li, Q. Wang, H.L. Zhang, Fractal growth of 2D $NbSe_2$ for broadband nonlinear optical limiting. Adv. Funct. Mater. **34**(29), 2401490 (2024). https://doi.org/10.1002/ADFM.202401490
35. D.F. Carrasco, S. García-Dalí, S. Villar-Rodil, J.M. Munuera, E. Raymundo-Piñero, J.I. Paredes, $NbSe_2$ nanosheets/nanorolls obtained via fast and direct aqueous electrochemical exfoliation for high-capacity lithium storage. ACS Appl. Energy Mater. **6**(13), 7180–7193 (2023). https://doi.org/10.1021/ACSAEM.3C00893
36. P. Aggarwal, P. Bisht, S. Jana, A. Mishra, S.K. Ray, E.Y. Chang, B.R. Mehta, R. Singh, Effect of gamma irradiation on the structure, morphology, and memristive properties of CVD grown ReS_2 thin film. Adv. Mater. Technol. (2024). https://doi.org/10.1002/ADMT.202400400
37. P. Tiwari, J. Biswas, C. Joishi, S. Lodha, Nb_2O_5 high-k dielectric enabled electric field engineering of β -Ga_2O_3metal-insulator-semiconductor (MIS) diode. J. Appl. Phys. **130**(24), 245701 (2021). https://doi.org/10.1063/5.0075627/1065690
38. B. Gaggio, A. Jan, M. Muller, B. Salonikidou, B. Bakhit, M. Hellenbrand, G. Di Martino, B. Yildiz, J.L. MacManus-Driscoll, Sodium-controlled interfacial resistive switching in thin film niobium oxide for neuromorphic applications. Chem. Mater. **36**(11), 5764–5774 (2024). https://doi.org/10.1021/ACS.CHEMMATER.4C00965
39. Schroder, D. *Semiconductor Material and Device Characterization*; 2015.
40. Y.R. Kim, T.L. Phan, Y.S. Shin, W.T. Kang, U.Y. Won, I. Lee, J.E. Kim, K. Kim, Y.H. Lee, W.J. Yu, Unveiling the hot carrier distribution in vertical graphene/h-BN/Au van der waals heterostructures for high-performance photodetector. ACS Appl. Mater. Interfaces **12**(9), 10772–10780 (2020). https://doi.org/10.1021/ACSAMI.9B19904

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