Ultra-Fast Characterization of Memristors for Neuromorphic Applications

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Abstract

Over several decades, the continuous scaling of semiconductor devices has led to significant performance improvements in information technology. As device scaling approaches its physical limits and the importance of data-intensive applications continues to grow, conventional computing architectures are increasingly reaching their performance limits. This is particularly true for the von Neumann architecture, in which memory and processing units are physically separated. This separation induces continuous data transfer between the processing and memory units, resulting in increased energy consumption and additional latency [1, 2]. These limitations have significantly increased interest in alternative memory technologies and neuromorphic computing systems [3].

Among these alternative memory technologies, memristive devices, particularly resistive random-access memory (RRAM) based on the valence change mechanism (VCM) in transition metal oxides such as TaO_x have emerged as promising candidates. These devices offer high scalability, low energy consumption, fast writing speed, and the ability to support gradual analog conductance modulation [4–7]. In addition to oxide-based RRAM devices, phase change memory (PCM) represents another technologically relevant alternative that also enables fast switching and analog functionality [8, 9]. For synaptic applications, gradual and linear conductance changes are required to emulate biological learning processes. Despite the advantages of VCM and PCM materials, the switching dynamics of these devices at sub-nanosecond (ns) timescales remain insufficiently understood, and their potential for synaptic applications in this regime remains unexplored.

This dissertation addresses the ultra-fast electrical characterization of memristive devices, focusing on switching dynamics at sub-ns timescales. For this purpose, dedicated high-frequency measurement setups are developed to generate ultra-short voltage pulses and capture the transient response of the devices. An initially realized radio-frequency (RF) measurement setup allowed the investigation of TaO_x-based VCM devices, but showed limitations at high resistance levels. Subsequently, the RF setup is upgraded to overcome this limitation and to extend the investigation to PCM devices.

The investigation of TaO_x devices is conducted under two distinct operating conditions. First, the switching behavior is studied using ultra-short SET pulses, with long inter-pulse delays of one second to ensure complete thermal relaxation between consecutive pulses. Under these conditions, repeated sub-100 picosecond (ps) pulses induce a transition from

abrupt to gradual and linear switching behavior. Both pulse width and pulse amplitude significantly influence this transition. Using 50 ps pulses at 1.77 V, more than 100 consecutive pulses remain within the linear regime ($R^2 = 99.5\%$). Although variability is inherent to filamentary devices, the role of the initial low conductive state (LCS) is analyzed. Previous studies have shown that lower initial LCS values are typically associated with more abrupt switching [7, 10]. In contrast, operating in the ultra-short pulse regime mitigates this effect, enabling linear conductance modulation even when starting from a low initial LCS.

In a second phase of the VCM investigation, the inter-pulse delay is reduced to the sub-ns range to study the influence of thermal relaxation on the switching dynamics. When a short pulse train is applied with sub-ns delays, residual heat from previous pulses accumulates and modifies the conductance evolution. Although theoretical studies predicted such thermal accumulation effects, experimentally verifying them at these timescales is challenging. At sub-ns inter-pulse delays, conventional DC readout between pulses is not feasible due to insufficient time. Furthermore, determining the device conductance from the transient electrical response is difficult because capacitive charging and discharging dominate the measured signal, obscuring the true resistive response. To address this limitation, dedicated analysis techniques were developed to extract the device conductance from the transient RF response for pulse widths and delays down to 50 ps. Using these evaluation methods, it was observed that reducing the delay below approximately 250 ps leads to steeper conductance transitions. This behavior is attributed to thermal accumulation. These findings demonstrate that temperature acts as a second internal state variable, giving rise to second-order memristive behavior and enabling short-term synaptic plasticity such as paired-pulse facilitation and post-tetanic potentiation.

After characterizing VCM devices, the investigation extends to PCM using the upgraded RF setup, where the SET and RESET switching kinetics of SnTe-doped In_3SbTe_2 (SIST) are studied at sub-ns timescales. The SET process is systematically characterized over a wide range of pulse amplitudes and durations, allowing differentiation between nucleation-dominated and growth-dominated crystallization regimes. At lower voltages, stochastic behavior characteristic of nucleation processes is observed, whereas higher voltages result in more reproducible, growth-dominated switching. This experimental distinction addresses a long-standing challenge in PCM research. In addition, RESET switching into the high-resistance amorphous state is demonstrated for pulse widths below 100 ps with $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio of over one thousand. These switching times fall below the previously reported RESET time record of approximately 200 ps [8], providing new insights into melt-quench dynamics at these timescales.

The results of this study offer a comprehensive understanding of ultra-fast switching dynamics across different memristive material systems and highlight their potential for sub-ns neuromorphic functionality.

Kurzfassung

Über mehrere Jahrzehnte hinweg hat die kontinuierliche Skalierung von Halbleiterbauelementen zu erheblichen Leistungssteigerungen in der Informationstechnik geführt. Mit der Annäherung an physikalische Skalierungsgrenzen sowie dem rasanten Wachstum datenintensiver Anwendungen stoßen konventionelle Rechenarchitekturen zunehmend an ihre Grenzen. Dies gilt insbesondere für die von Neumann-Architektur, bei der Speicher- und Recheneinheiten physisch voneinander getrennt sind. Diese Trennung induziert einen kontinuierlichen Datentransfer zwischen Rechen- und Speichereinheit und somit einen erhöhten Energieverbrauch sowie zusätzliche Latenzen [1, 2]. Diese Limitation hat das Interesse an alternativen Speichertechnologien und neuromorphen Rechenkonzepten deutlich verstärkt [3].

Unter den alternativen Speichertechnologien haben sich *memristive* Bauelemente, insbesondere *Resistive Random-Access Memory* (RRAM) basierend auf dem Valenzwechselmechanismus (VCM) in Übergangsmetalloxiden wie TaO_x, als vielversprechende Kandidaten herausgestellt. Diese Bauelemente zeichnen sich durch hohe Skalierbarkeit, geringen Energieverbrauch, schnelle Schreibgeschwindigkeiten sowie die Möglichkeit einer graduellen analogen Leitwertmodulation aus [4–7]. Neben oxidbasierten RRAM-Systemen stellt auch *phase-change-memory* (PCM) eine technologisch relevante Alternative dar, die ebenfalls schnelle Schaltprozesse und analoge Funktionalität ermöglicht [8, 9]. Für synaptische Anwendungen in neuromorphen Systemen sind insbesondere graduelle und möglichst lineare Änderungen des elektrischen Leitwerts erforderlich, um biologische Lernprozesse nachbilden zu können. Trotz dieser vielversprechenden Eigenschaften sind die Schaltmechanismen beider Bauelementtypen im Subnanosekundenbereich bislang nur unzureichend verstanden.

Die Ergebnisse dieser Arbeit tragen zu einem vertieften Verständnis ultraschneller Schaltdynamiken in verschiedenen memristiven Materialsystemen bei und zeigen deren Potenzial für neuromorphe Anwendungen im Subnanosekundenbereich. Hierzu werden hochfrequente Messaufbauten entwickelt, die das Erzeugen ultrakurzer Spannungspulse sowie die zeitaufgelöste Erfassung der transienten Bauelementantwort ermöglichen. Ein zuvor entwickelter Radiofrequenz-(RF)-Messaufbau erlaubt die Untersuchung von TaO_x-basierten VCM-Bauelementen, zeigt jedoch Einschränkungen bei hohen Widerstandswerten. Durch Erweiterung des Messaufbaus können auch PCM-Bauelemente untersucht werden.

Die Untersuchung der TaO_x-Bauelemente wird unter zwei unterschiedlichen Betriebsbedingungen durchgeführt. Zunächst wird das Schaltverhalten mithilfe ultra-kurzer *SET*-Pulse untersucht, wobei lange Interpulsabstände von einer Sekunde verwendet werden, um eine vollständige thermische Relaxation zwischen aufeinanderfolgenden Pulsen sicherzustellen. Unter diesen Bedingungen führen wiederholte Pulse mit einer Dauer von unter 100 ps zu einem Übergang von abruptem zu graduellem und linearem Schaltverhalten. Sowohl die Pulsbreite als auch die Pulsamplitude beeinflussen diesen Übergang deutlich. Bei Verwendung von 50 ps-Pulsen bei 1,77 V bleiben mehr als 100 aufeinanderfolgende Pulse im linearen Bereich ($R^2 = 99{,}5\,\%$). Jedoch wird dabei die inhärente Variabilität der filamentären Bauelemente deutlich. Darüber hinaus wird die Rolle des anfänglichen niedrigleitenden Zustands (LCS) analysiert. Frühere Studien haben gezeigt, dass niedrigere anfängliche LCS-Werte typischerweise zu einem abrupten Schaltverhalten führen [7, 10]. Im Gegensatz dazu reduziert der Betrieb im ultra-kurzen Pulsregime diesen Effekt und ermöglicht eine lineare Modulation der Leitfähigkeit selbst bei einem niedrigen anfänglichen LCS.

In einer zweiten Phase der VCM-Untersuchung wird der Interpulsabstand in den Sub-Nanosekundenbereich reduziert, um den Einfluss der thermischen Relaxation auf die Schaltdynamik zu untersuchen. Wird eine kurze Pulsfolge mit Sub-Nanosekunden-Abständen angelegt, akkumuliert die Restwärme vorheriger Pulse, wodurch die Dynamik des Schaltvorgangs moduliert wird. Obwohl theoretische Studien solche thermischen Akkumulationseffekte bereits vorhergesagt haben, ist deren experimentelle Bestätigung auf diesen Zeitskalen schwierig. Bei Interpulsabständen im Sub-Nanosekundenbereich ist ein konventionelles DC-Auslesen zwischen den Pulsen aufgrund der unzureichenden Zeit nicht möglich. Außerdem ist die Bestimmung der Leitfähigkeit des Bauelements aus der transienten elektrischen Antwort schwierig, da kapazitive Lade- und Entladevorgänge das gemessene Signal dominieren und die tatsächliche resistive Antwort überdecken. Um diese Einschränkung zu überwinden, werden spezielle Auswertungsmethoden entwickelt, mit denen die Leitfähigkeit des Bauelements aus der transienten HF-Antwort für Pulsbreiten und Interpulsabstände bis hinunter zu 50 ps extrahiert werden kann. Mithilfe dieser Methoden wird beobachtet, dass eine Verringerung des Interpulsabstands unter etwa 250 ps zu steileren Leitfähigkeitsübergängen führt. Dieses Verhalten wird auf thermische Akkumulation zurückgeführt. Diese Ergebnisse zeigen, dass die Temperatur als zweite interne Zustandsvariable wirkt, was zu einem Memristorverhalten zweiter Ordnung führt und kurzzeitige synaptische Plastizität wie *paired-pulse facilitation* und *post-tetanic potentiation* ermöglicht.

Anschließend wird das verbesserte RF-Messsystem verwendet, um das Schaltverhalten von PCM-Bauelementen im Sub-Nanosekundenbereich zu untersuchen. Die *SET*- und *RESET*-Schaltkinetik von SnTe-dotiertem In_3SbTe_2 (SIST) wird über einen weiten Bereich von Pulsamplituden und Pulsdauern untersucht, wodurch eine Unterscheidung zwischen

nukleationsdominierten und wachstumsdominierten Kristallisationsregimen ermöglicht wird. Bei niedrigeren Spannungen wird ein stochastisches Verhalten beobachtet, das charakteristisch für Nukleationsprozesse ist, während höhere Spannungen zu einem reproduzierbareren, wachstumsdominierten Schaltverhalten führen. Diese experimentelle Unterscheidung adressiert eine langjährige Herausforderung in der PCM-Forschung. Darüber hinaus wird *RESET*-Schalten in den hochohmigen amorphen Zustand für Pulsbreiten unter 100 ps mit einem $R_{\mathrm{off}}/R_{\mathrm{on}}$-Verhältnis von über eintausend demonstriert. Diese Schaltzeiten liegen unter dem zuvor berichteten *RESET*-Zeitrekord von etwa 200 ps [8] und liefern neue Einblicke in die *Melt-Quench*-Dynamik auf diesen Zeitskalen.

Die Ergebnisse dieser Studie liefern ein umfassendes Verständnis der ultraschnellen Schaltdynamik in verschiedenen memristiven Materialsystemen und verdeutlichen deren Potenzial für neuromorphe Funktionalität im Sub-Nanosekundenbereich.

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Contents

1 Introduction **1**

2 Fundamentals **6**

2.1 Memory Types 6
2.2 Phase Change Memory (PCM) 8
2.3 Redox-based Resistive Random Access Memory 12
2.3.1 Valence Change Mechanism (VCM) 13
2.4 High Frequency Domain 16
2.4.1 Transmission-Line Theory 17
2.4.2 Experimental Approach 19
2.4.3 Scattering Parameters 21
2.4.4 Fourier Transformation of a Square Pulse 23
2.5 Multilevel and Gradual Conductance Modulation in Filamentary VCM . . 23
2.6 Fundamental Aspects of Thermal Effects in VCM Devices 25
2.6.1 Fundamental Concepts of PPF and PTP 28
2.7 Coefficient of Determination 30

3 Experimental Details **33**

3.1 Experimental Setup 33
3.1.1 RF Setup 1 36
3.1.2 RF Setup 2 37
3.2 Sample Design and Fabrication 39
3.2.1 Sample Design 39
3.2.2 Device Fabrication 40
3.3 Characterization 41
3.3.1 Electroforming and *I-V* Characteristics 41
3.3.2 Scattering Parameters Measurements 43
3.4 Further Device Optimization 48
3.5 Conclusion 49

4 VCM Switching with Short Pulses and Long Delays 51
4.1 Experimental Methodology . . . 52
4.1.1 SET Pulse Measurements . . . 52
4.1.2 Data Analysis . . . 54
4.2 Results & Discussion . . . 56
4.2.1 Number of Pulses in Linear Regime . . . 56
4.2.2 Pulse Width and Voltage Dependencies . . . 58
4.2.3 Variability . . . 63
4.2.4 Impact of Initial Low Conductive State (LCS) . . . 67
4.3 Conclusion . . . 70

5 VCM Switching with Short Pulses and Short Delays 73
5.1 Experimental . . . 74
5.1.1 Measurement Protocol . . . 74
5.2 Evaluation Methods . . . 77
5.2.1 Reference Method . . . 77
5.2.2 Integration Method . . . 80
5.2.3 Discussion . . . 82
5.3 Studying Thermal Effects in VCM Devices . . . 86
5.4 Short-Term Synaptic Plasticity in VCM Devices . . . 90
5.5 Conclusion . . . 94

6 Electrical Characterization of PCM Devices 98
6.1 Experimental Methods . . . 99
6.1.1 Measurement Procedures . . . 99
6.2 SET Switching Kinetics . . . 102
6.2.1 Analysis of Crystallization Mechanisms . . . 106
6.2.2 Reproducibility of SET Switching Behavior . . . 109
6.3 RESET Switching Kinetics . . . 111
6.4 Conclusion . . . 114

7 Conclusion and Outlook 117
7.1 Conclusion . . . 117
7.2 Outlook . . . 119
7.2.1 Future Directions for VCM Devices . . . 119
7.2.2 Future Directions for PCM Devices . . . 121

List of Acronyms and Symbols 123

List of Publications 126

Supervised Theses **127**

Bibliography **129**

Appendix **144**

1. Introduction

The digital world is expanding at an extraordinary rate. Every moment, billions of sensors in phones, cars, homes, and wearable devices capture images, sounds, temperatures, movements, and biological signals. Much of this data is imperfect, fragmented, noisy, and context-dependent. Yet, it must be interpreted in real time. The challenge is not just storing this information but also processing continuous data streams rapidly while maintaining energy efficiency. Despite remarkable advances in transistor scaling and computational power, the fundamental computing architecture has remained largely unchanged. The processor and memory still reside in physically separate locations, requiring continuous data transfer between them. This constant data movement has become a primary limitation on system performance and energy efficiency [1, 2].

This separation is central to the von Neumann architecture and has become one of the most persistent obstacles in information technology [1, 2]. Data must be continuously transferred between distinct memory and processing units, and this movement increasingly dominates both latency and energy consumption, a limitation widely referred to as the von Neumann bottleneck. As data volumes continue to grow, conventional hardware improvements alone are insufficient. Researchers are therefore exploring alternative computing paradigms, ranging from quantum computing and hyperdimensional computing to biologically inspired approaches. Neuromorphic computing has gained significant attention as a brain-inspired paradigm that processes information in a massively parallel and energy-efficient manner. Unlike conventional systems, biological neural networks do not separate memory and computation into distinct units. Instead, storage and signal processing are co-integrated within the same physical substrate. However, when neuro-inspired algorithms are implemented on conventional CMOS (complementary metal-oxide-semiconductor) platforms, they remain constrained by the same architectural bottleneck they aim to overcome. This limitation has intensified the search for device technologies capable of physically integrating memory and computation at the hardware level, enabling architectures that operate fundamentally differently from the von Neumann model rather than simply optimizing within its constraints.

Current memory technologies face additional constraints beyond this architectural bottleneck. Dynamic random-access memory (DRAM) provides fast access times on the order of 10 nanoseconds (ns) but requires constant power to retain information, resulting in high

energy consumption and volatility constraints [3]. Non-volatile memories such as Flash provide long-term data retention but suffer from slower write speeds, high programming voltages exceeding 10 V, and limited endurance [11]. The large performance difference between fast but volatile memories and slower non-volatile memories is commonly referred to as the memory gap [3]. This gap has motivated research into novel memory technologies capable of combining high speed, non-volatility, scalability, and energy efficiency.

To overcome these limitations, Redox-based resistive random access memory (ReRAM) has emerged as a promising candidate for next-generation computing systems [4, 5]. These devices store information through electrically induced resistive switching within simple metal-insulator-metal (MIM) structures, enabling non-volatile operation. Their structural simplicity and compatibility with established CMOS fabrication processes make ReRAM attractive for integration into existing technology platforms. ReRAM devices can also exhibit multi-level switching and gradual, linear conductance modulation beyond binary storage, making them attractive for neuromorphic and computing-in-memory (CIM) applications [7, 10, 12, 13]. Among the various ReRAM switching mechanisms, the valence change mechanism (VCM) has received significant attention due to its reliable switching characteristics and material versatility [14–16]. In VCM devices, resistive switching is governed by the migration of oxygen vacancies and metal cation interstitials, along with associated redox processes within a transition metal oxide, such as TaO_x, HfO_x, and ZrO_x [14, 15]. Experimental studies have demonstrated switching times in the sub-100 picoseconds (ps) regime, indicating ultra-fast switching capabilities [6, 17].

Neuromorphic computing systems require devices that can emulate synaptic behavior. A key requirement for synaptic functionality is achieving gradual and linear conductance changes during repeated programming operations [18, 19]. However, the SET transition in filamentary VCM devices is typically abrupt, which makes it difficult to achieve the gradual potentiation required for synaptic weight updates. This abrupt behavior is commonly attributed to positive electrothermal feedback, where an increase in current during the SET process leads to local Joule heating, accelerating filament growth, and resulting in sudden changes in conductance [16, 20]. Previous studies have shown that the switching dynamics can be influenced by the temporal characteristics of the applied pulses. Operating on timescales comparable to or shorter than the thermal time constant of the conductive filament can suppress positive feedback and enable more gradual switching [7, 10]. However, these studies were limited to pulse widths down to 100 ns and reported only a few linear conductance states. This leaves open the question of whether operating at much shorter timescales could fundamentally alter the switching dynamics.

To investigate this possibility, the switching behavior of VCM devices was characterized under ultra-short pulse conditions. A radio frequency (RF) measurement setup was used to apply SET pulses while measuring the device conductance after each pulse using a direct current (DC) read voltage. The devices were integrated into coplanar waveg-

uide (CPW) structures to ensure proper signal delivery at high frequencies. A key aspect of the experiment was applying ultra-short SET pulses using an RF setup. To ensure that the device response to each pulse was not affected by residual heating from the preceding pulse, long delays were introduced between consecutive pulses. These delays were chosen to exceed the thermal time constant of the filament, thereby preventing thermal accumulation. Under these conditions, each pulse interacted with a fully thermally relaxed device state, enabling independent study of the effects of the applied pulse parameters on the SET behavior. The resulting conductance evolution was analyzed to identify the linear switching region and determine how the number of achievable linear conductance states depends on pulse parameters, the initial low conductive state (LCS), and cycle-to-cycle (C2C) variability.

The gradual, linear conductance modulation achieved with long inter-pulse delays represents a form of long-term potentiation (LTP), where the device retains a modified conductance state after each applied pulse. This behavior occurs when the device fully relaxes thermally between consecutive pulses, ensuring that each switching event is primarily determined by the applied pulse parameters rather than by residual heating effects. This motivates the investigation of how potentiation changes when the inter-pulse delay in a pulse train is reduced to the sub-ns range. As the inter-pulse interval approaches the thermal relaxation time of the conductive filament, the device no longer returns to thermal equilibrium between consecutive pulses. Residual heating from one pulse then influences the conductance change induced by the next pulse, making the device response dependent not only on the applied pulse parameters but also on the temporal spacing between pulses. Thermal effects, which were previously suppressed, now shape the switching dynamics.

Such timing-dependent behavior is conceptually related to short-term synaptic plasticity in biological systems, where the synaptic response depends on recent activity. In biological synapses, calcium ion dynamics act as an internal state variable that retains temporal information between stimuli [21–23]. In oxide-based memristive devices, temperature can play a comparable role. Previous studies have reported thermal accumulation effects at microsecond to nanosecond delays, typically employing multi-pulse schemes to emulate a spike rather than treating each electrical pulse as a discrete spike event [24]. A simulation study has predicted that thermal accumulation effects could occur even at sub-ns delays [25]. However, experimental verification at these timescales has been lacking.

Experimentally validating these predicted thermal accumulation effects with sub-ns delays between consecutive pulses is challenging. At such short timescales, there is insufficient time to perform conventional DC read operations between consecutive pulses. In addition, evaluating conductance changes from the transient electrical response is difficult because capacitive charging and discharging of the device dominate the measured signal and obscure the true resistive response.

To address this limitation, dedicated analysis techniques were developed that enable

the reliable extraction of device conductance from the transient electrical response for pulse widths and inter-pulse delays as short as 50 ps. Using these methods together with a high-frequency measurement setup equipped with an ultra-fast pulse pattern generator (PPG30), the interaction of closely spaced pulses within the device was characterized. This enabled the investigation of thermal accumulation effects at sub-ns inter-pulse delays, allowing the switching behavior to be studied as a function of the inter-pulse delay. When the delay between pulses is sufficiently reduced, residual heating from the preceding pulse enhances the conductance change induced by the subsequent pulse. Under these conditions, temperature acts as a second state variable, leading to timing-dependent conductance modulation and short-term plasticity (STP).

To extend ultra-fast characterization capabilities to other memory technologies, the RF setup used for the VCM studies had to be improved. The original setup, while effective for VCM devices, exhibited limitations when characterizing devices with resistance values in the megaohm range, such as phase change memory (PCM) in its amorphous state, where leakage currents in the measurement setup become significant and distort the measured device response. An enhanced RF measurement setup (RF Setup 2) was therefore developed within the scope of the present study to address this limitation and allow flexible control of pulse parameters, enabling ultra-fast characterization of memory technologies beyond VCM. In this upgraded setup, the bias tee was replaced with RF switches to avoid leakage currents and enable fully automated measurements. Additionally, an arbitrary waveform generator (AWG) was integrated to allow flexible control of pulse parameters.

Using the enhanced RF setup, initial measurements were performed on PCM devices based on SnTe-doped In_3SbTe_2 (SIST). These devices operate through reversible structural transitions between amorphous and crystalline phases induced by electrical pulses. The SET crystallization process, in particular, is governed by thermally activated mechanisms, such as nucleation and crystal growth [26, 27]. Distinguishing between nucleation- and growth-dominated crystallization during electrical operation has remained experimentally challenging [28]. Experiments were conducted to investigate the nucleation-dominated and growth-dominated crystallization regimes in SIST using RF Setup 2 under ultra-fast pulse conditions. Furthermore, RESET kinetics were examined in the sub-250 ps regime.

The thesis is organized as follows. Chapter 2 provides the physical background of the investigated memory technologies and the theoretical foundations for high-frequency electrical measurements. Chapter 3 describes the experimental infrastructure, including the two RF measurement setups and device fabrication procedures. Chapters 4 and 5 present the experimental studies on ultra-fast switching in VCM devices under long and short inter-pulse delay conditions, respectively. These chapters focus on gradual, linear conductance modulation and timing-dependent plasticity. Chapter 6 extends the ultra-fast characterization approach to PCM devices. Finally, Chapter 7 summarizes the main findings and discusses future research directions.

2. Fundamentals

2.1. Memory Types

Most modern computers operate on the von Neumann architecture, where the central processing unit (CPU) and memory are physically separated [1, 2]. During computation, the CPU temporarily stores and retrieves data from the main memory, which is typically implemented as DRAM. In DRAM, data are stored in capacitors that can be charged or discharged to represent logical ‘1’ or ‘0’. Writing times as short as 10 ns have been demonstrated [3, 5], making DRAM one of the fastest available memory technologies. However, once the applied voltage is removed, the capacitors gradually discharge, and the stored information is lost. To maintain data integrity, the stored bits must be periodically refreshed every 64 ms [3, 29]. This volatility categorizes DRAM as volatile memory.

For long-term data storage, computers utilize non-volatile memory, which retains information even when power is off. Prominent examples include the hard disk drive (HDD) and solid-state drive (SSD). In HDDs, information is stored in magnetic domains on a rotating disk. Data access is mechanical, as a movable arm positions the read/write head over the appropriate track. Because disk rotation speeds reach only a few thousand

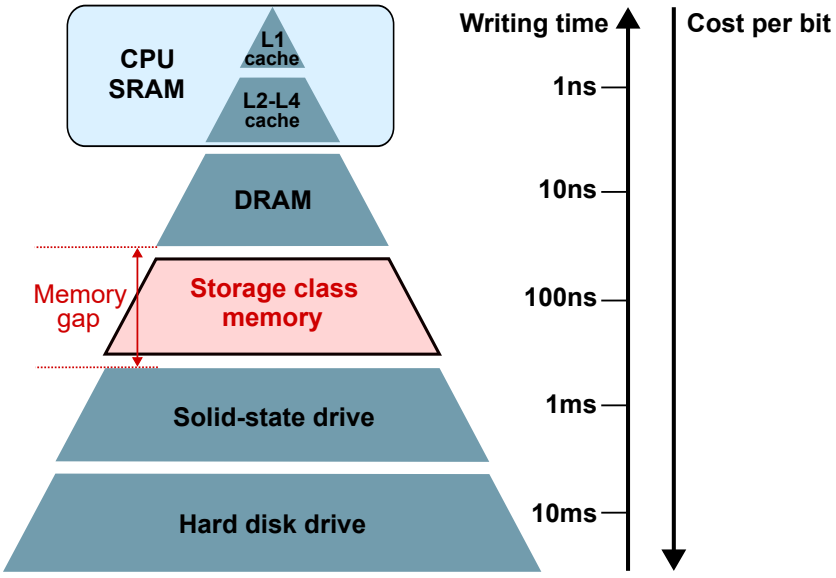


Figure 2.1: Illustration of the memory gap. Adapted from [30].

revolutions per minute, typical read and write times exceed 1 ms [5]. Additionally, the mechanical motion of the spindle and actuator arm consumes significant power, making HDDs among the most energy-intensive memory types.

In contrast, SSDs utilize Flash memory, in which data are stored as electrical charge within a metal oxide semiconductor (MOS) structure. This mechanism is analogous to that of a MOSFET (metal oxide semiconductor field effect transistor), where the stored charge in the floating gate modulates the channel conductivity. The presence of trapped electrons corresponds to a logical '1', and their absence to a logical '0'. Flash memories exhibit long data retention exceeding ten years and write times down to 50 ns, but they require high programming voltages ($\geq$ 10 V) and exhibit limited endurance [3]. The energy consumed per programming cycle is the second highest among state-of-the-art memories [3].

The difference in write speed between Flash and DRAM spans approximately three orders of magnitude [11], as illustrated in Figure 2.1. This latency gap between the fastest non-volatile and the most efficient volatile memory defines the *memory gap*. Moreover, volatile memories are more costly due to their larger feature sizes and smaller information density [5]. The ideal solution would be a technology that combines the speed of DRAM with the non-volatility and density of Flash. Memory technologies envisioned to bridge this gap are known as storage-class memories (SCMs) [31].

Several emerging non-volatile memories have been investigated to fulfill this role. Among the most prominent are Ferroelectric RAM (FeRAM), Spin-Transfer Torque RAM (STTRAM), and Resistive Random Access Memory (RRAM).

Ferroelectric RAM (FeRAM) operates by modulating the polarization of a ferroelectric layer, typically $Pb(Zr,Ti)O_3$ [32]. Electrical polarization states can be switched by applying an electric field across the gate, corresponding to logical "0" and "1". FeRAM combines low leakage currents with extremely low switching power [31], endurance up to 4×10^{10} cycles [33], and fast write times down to 20 ns [34]. The technology has been demonstrated at feature sizes down to 22 nm [35], and with HfO_2- and ZrO_2-based films as thin as 5 nm [36].

Spin-Transfer Torque RAM (STTRAM) stores information based on the magnetization orientation of two ferromagnetic layers separated by a thin tunnel barrier (e.g., MgO) [37]. The device resistance depends on the relative magnetization alignment: parallel (P) configuration results in a low resistive state (LRS), while antiparallel (AP) configuration yields a high resistive state (HRS). Switching between these states is achieved by injecting spin-polarized currents that exert torque on the free magnetic layer. STTRAM offers non-volatility, high endurance, and low switching energy, but its scalability remains limited by the magnetic stack thickness and the need for precise current control [38–40].

Resistive RAM (RRAM) is a memristive device that stores information by changing its electrical resistance [41]. Unlike conventional memory technologies such as static random access memory (SRAM), DRAM, and Flash, RRAM encodes data directly in the resistance

state of the device. Typically, two resistance states are defined: LRS or high-conductive state (HCS), and HRS or low-conductive state (LCS), which are commonly assigned to the ON state and OFF state, respectively [14]. The choice of terminology depends on the specific application and whether resistance- or conductance-based representations are preferred.

Based on their electrical switching characteristics, RRAM devices are generally classified into bipolar and unipolar switching types [41]. In bipolar switching, the resistance change depends on the polarity of the applied voltage. The SET operation occurs under one voltage polarity, while the RESET operation requires the opposite polarity. As a result, switching between the two resistance states cannot be achieved by changing the voltage amplitude alone; a reversal of polarity is necessary. This polarity-dependent behavior originates from an intrinsic asymmetry of the device, which can be introduced by using different electrode materials or by an electroforming process carried out at a specific voltage polarity [14].

In contrast, unipolar RRAM devices exhibit switching behavior that is independent of the voltage polarity. In this case, both SET and RESET transitions can be induced using voltages of either polarity, and the distinction between the two operations is governed by other pulse parameters, such as the applied voltage amplitude, pulse duration, or the temporal characteristics of the electrical stimulus, including rise and fall times [42].

The resistive switching phenomenon can arise from various physical mechanisms [43]. These mechanisms are generally categorized based on their switching polarity (bipolar or unipolar) and underlying physics, including electrostatic effects, redox-based processes, and phase-change transitions. This work primarily investigates redox-based RRAM, with a focus on VCM devices. Additionally, PCM was explored in the final phase of the study as an alternative class of non-volatile memory with distinct switching mechanisms. The PCM experiments served to demonstrate the capabilities of the newly developed RF setup 2 (Section 3.1.2), which was designed to capture ultra-fast switching dynamics at sub-ns timescales. Understanding the fundamental processes governing switching at these ultra-fast timescales remains an open challenge, even for commercially mature PCM technologies. The operational principles and switching mechanisms of both ReRAM (especially VCM) and PCM are discussed in detail in the following sections.

2.2. Phase Change Memory (PCM)

Phase change materials derive their name from their inherent ability to undergo reversible phase transformations [26]. These materials can rapidly switch their microscopic structure between a crystalline and an amorphous configuration. The transition between these two states is driven by electrical pulses, as illustrated in Figure 2.2. When a short but intense pulse is applied, the RESET process forces the PCM into its amorphous phase through rapid

melt-quenching. This process melts the crystalline material and subsequently quenches it at high cooling rates, freezing the disordered structure of the liquid phase into the solid phase to produce an amorphous state [27]. This amorphous phase typically exhibits a high electrical resistance, corresponding to the logical "0" or the HRS. In contrast, the crystalline phase, which represents the logical "1" or LRS, can be achieved through two distinct methods.

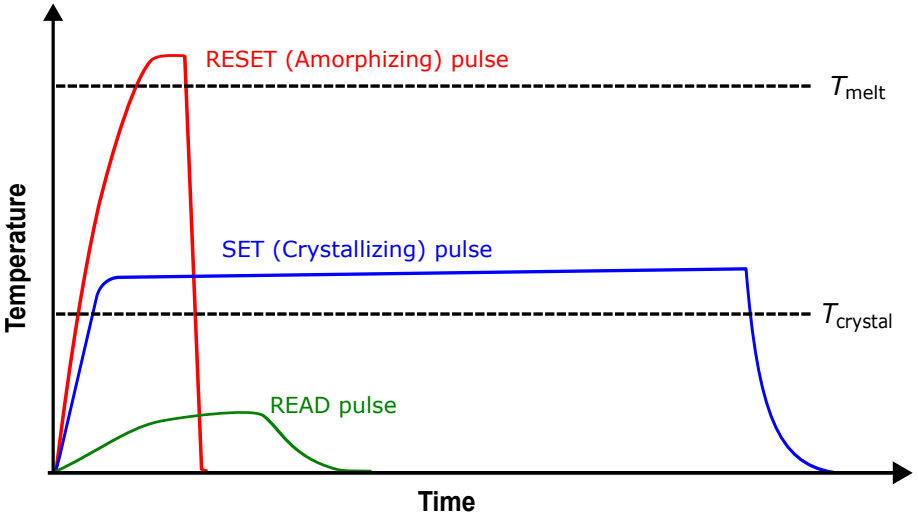


Figure 2.2: Pulse characteristics for READ, SET, and RESET operations in a PCM cell. The READ pulse remains below the crystallization temperature $T_{crystal}$ and preserves the existing phase. The SET pulse exceeds $T_{crystal}$ but remains below the melting temperature T_{melt} for a sufficient duration to enable crystallization. In contrast, the RESET pulse briefly exceeds T_{melt}, melting the material, which is then rapidly quenched into the amorphous state. Adapted from [27].

The first SET method involves crystallization directly from the amorphous phase by heating the material to its crystallization temperature, commonly referred to as solid phase crystallization (SPC) [44]. The second method, known as melt and slow cooling (MSC), induces crystallization by melting the material and then cooling it slowly. These two crystallization methods have distinct functions, with SPC providing faster switching speed and lower energy consumption. On the other hand, MSC offers improved control of final resistance levels, making it particularly useful for multilevel memory operation [44].

The mechanisms underlying crystallization and amorphization involve fundamental changes in atomic arrangement and material disorder. Figure 2.3 illustrates the different stages of amorphous, liquid, and crystalline phases, along with the disorder present in each state and the transitions between them. Heating a crystalline PCM above its melting temperature (T_{melt}) transforms it into a liquid, significantly increasing atomic disorder. Rapid cooling of this molten state leads to undercooling, enabling the material to solidify into an amorphous phase with substantially greater disorder than in its crystalline form. Conversely, reheating the amorphous phase to a temperature below T_{melt} provides sufficient energy for atoms to realign and reorganize into a crystalline lattice [45].

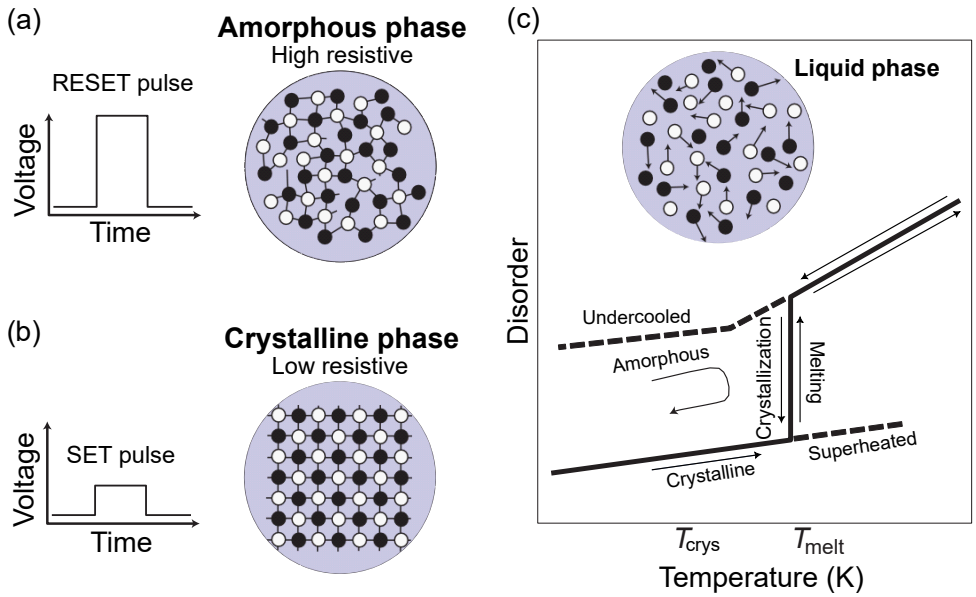


Figure 2.3: Illustration of the phase-change process in PCM, showing transitions among amorphous, liquid, and crystalline states. (a) A short, high-intensity pulse causes melting followed by rapid quenching, trapping atoms in a highly disordered amorphous state with high resistivity. (b) In contrast, a longer, low-intensity pulse allows atomic rearrangement below the melting temperature T_{melt}, promoting crystallization and resulting in a low-resistivity phase. (c) The structural disorder linked to each state is also illustrated, highlighting its dependence on temperature and thermal history. Adapted from [45].

Electrically inducing these phase transitions presents a key challenge. If only the high resistance of the PCM in its HRS were considered, a very large voltage would be needed to generate enough Joule heating for crystallization. However, one of the earliest phenomena observed in PCM is a sudden drop in resistance when the applied voltage reaches a critical threshold. This specific voltage, termed the threshold voltage, is associated with threshold switching, a process that transitions the material from the amorphous-off state to the amorphous-on state [46]. The behavior is illustrated in Figure 2.4.

In the crystalline phase, the PCM behaves as a simple resistor, with the slope of its $I(V)$ curve determined by both the resistance of the low-resistive chalcogenide layer and the external circuit resistance necessary for device operation. In contrast, the amorphous phase exhibits three distinct regions in its I-V response as the applied voltage increases. The initial sub-threshold region, also called the amorphous-off state, exhibits ohmic behavior with minimal conductivity. As the voltage approaches the threshold voltage (V_{th}), the conductivity increases sharply, leading to a super-exponential I-V relationship that defines the amorphous-on state, during which no structural transformation yet occurs. This state corresponds to the negative differential resistance (NDR) region of the curve, typically manifested as a voltage snapback in current-controlled operation or a sudden current rise in voltage-driven conditions. If the applied bias is removed at this point, the PCM naturally reverts to its amorphous-off state. At still higher voltages, the exponential increase

in current resulting from threshold switching produces significant Joule heating in the chalcogenide layer, which can eventually trigger the non-volatile phase transition to the crystalline state if the applied bias is maintained for a sufficient duration [47, 48].

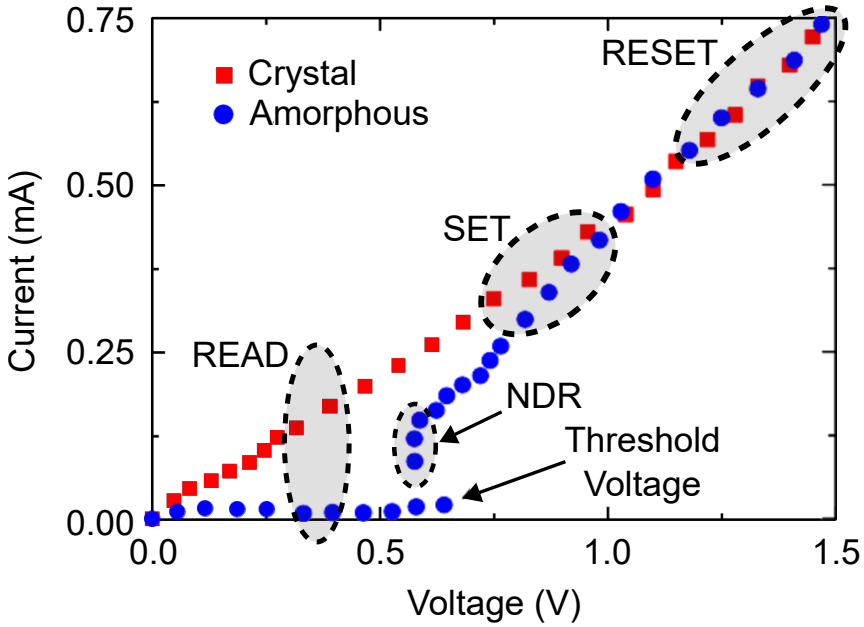


Figure 2.4: *I-V* characteristics of a PCM device in both the amorphous and crystalline states. The curve highlights the Ovonic threshold voltage V_{th}, marking the onset of threshold switching in the amorphous phase. The operating regions for the SET, RESET, and READ conditions are indicated, illustrating the distinct electrical behavior associated with each memory operation. Adapted from [47].

As in most materials, crystallization in PCMs occurs in two consecutive stages. The first stage is nucleation, during which small, stable crystalline clusters form spontaneously within the disordered amorphous matrix. The second stage is growth, where these crystalline regions expand and eventually transform the entire amorphous volume into a fully ordered crystalline phase [48, 49]. The relative rate of these two processes defines the overall crystallization kinetics and, therefore, directly influences the SET speed, power efficiency, and reliability of PCM devices [48]. Because nucleation is random in both space and time, it introduces stochastic variations in switching delay, especially in nanoscale devices where the number of potential nucleation sites is limited. Once nucleation occurs, crystal growth typically proceeds much faster and in a more deterministic manner [48, 49].

A long-standing challenge in studying PCM switching dynamics has been the inability to distinguish clearly between nucleation-dominated and growth-dominated crystallization during electrical operation, because conventional electrical measurements typically provide only the final resistance state after switching. This obscures the intermediate microscopic processes and prevents direct observation of how nuclei form and evolve under electrical excitation. This limitation has hindered a quantitative understanding of the stochastic nature of nucleation and its contribution to switching variability [28], which is important

for improving switching speed, reducing C2C variability, and enabling reliable device scaling. Addressing this requires high-speed transient electrical measurement setups capable of resolving ultra-fast switching processes. In this work, such a setup was realized and applied to the investigation of PCM switching behavior in the following chapter 6.

2.3. Redox-based Resistive Random Access Memory

Among the various emerging non-volatile memories discussed above, ReRAM has received particular attention due to its simple structure, scalability, and potential for fast and energy-efficient operation [4–6, 17]. In ReRAM, information is stored in HRS and LRS, both of which can be programmed by applying electrical stimulation. The resistance switching arises from electrochemical processes and the migration of charged ions within the device [14, 41]. ReRAM technologies are generally classified into three distinct types: electrochemical metallization memory (ECM), thermochemical memory (TCM), and VCM. These variants are based on a common MIM structure in which the insulator functions as an ionic conductor. All three ReRAM types usually require an initial electroforming step that involves applying a relatively high voltage amplitude to the device. This process generates an electronically conducting filament within the insulating material. To prevent device damage during the electroforming stage, current overshoot can be restricted through several approaches, including external current compliance mechanisms, series resistors, or integrated transistor-based current limiters.

In ECM devices, one electrode is electrochemically active, such as silver (Ag) or copper (Cu), while the opposing electrode is electrochemically inert, for example, platinum (Pt) [50, 51]. ECM devices typically operate in bipolar switching mode, meaning that the SET and RESET operations require voltage applications of opposite polarity. During the SET process, a positive voltage applied to the active electrode (AE) causes anodic dissolution of metal atoms and the formation of positively charged metal cations. Driven by the applied electric field, these cations migrate through the insulating layer toward the inert electrode, where they are electrochemically reduced and deposited as metallic atoms. This leads to the nucleation and subsequent growth of a conductive metallic filament extending toward the AE. Once the filament bridges the electrode gap, the device switches to the LRS. During the RESET process, the voltage polarity is reversed, destabilizing the metallic filament. This leads to electrochemical oxidation and dissolution of the filament, typically initiating at its narrowest region, thereby rupturing the conductive path and restoring the HRS. Joule heating may assist the RESET process by facilitating filament dissolution [41].

TCM devices typically consist of two symmetrical electrodes (e.g., Pt) combined with an ion-conducting insulator (such as Nickel Oxide (NiO_x) [52]. These devices operate in a unipolar switching mode. Unlike the unipolar switching mode seen in PCM devices, the SET operation in TCM requires higher voltage amplitudes than the RESET. During

the SET, the induced current elevates the device temperature, which increases electrical conductivity and leads to thermal runaway. This significant temperature increase within the conductive pathway accelerates redox reactions, causing oxygen anions to thermo-diffuse into the surrounding area of the conductive path. The remaining oxygen vacancies within the path function as n-type donors, permanently lowering the device resistance to the LRS. Successful unipolar SET operations require relatively high currents; consequently, high current compliance around 1 mA is typically implemented [53]. The RESET operation is achieved by applying a voltage lower than that used for the SET and without current compliance, which attracts the oxygen vacancies toward the negatively charged electrode. This process causes a rupture in the conductive path, reverting the device to the HRS.

2.3.1. Valence Change Mechanism (VCM)

Among the various ReRAM mechanisms, VCM is particularly notable for its reliable switching characteristics and material compatibility. As this work primarily focuses on VCM devices, their underlying physical principles are discussed in more detail in the following section.

VCM devices are typically designed as MIM structures. In this configuration, the insulating layer (I) is a thin film, usually less than 10 nm thick. It is commonly made of a binary transition metal oxide such as HfO_x, ZrO_x, TiO_x, or TaO_x [14, 15]. Ternary oxides, for example $SrTiO_x$, are also used [41]. The two metallic electrodes (M) consist of one AE and one ohmic electrode (OE). The AE generally uses a metal with a high work function, such as Pt, Ir, or TiN, which forms a Schottky barrier at the metal-oxide interface. The OE typically has a lower work function and a stronger oxygen affinity, forming an ohmic contact with the oxide [41].

The basic operation of VCM-type ReRAM relies on the partial reduction of the cation sublattice within the oxide, accompanied by partial oxidation of the OE. When oxygen ions are removed from the oxide lattice, empty lattice sites known as oxygen vacancies are formed. According to the Kröger-Vink notation [54], an oxygen vacancy is denoted as $V_O^{\cdot\cdot}$, indicating a missing oxygen atom that is doubly positively charged relative to the stoichiometric oxide. Electrically, the oxygen vacancy remains neutral because the local charge is promptly neutralized by mobile electrons. These electrons enable each oxygen vacancy $V_O^{\cdot\cdot}$ to function as a donor dopant, thereby reducing the resistance of the switching oxide. In addition to oxygen vacancies, metal cation interstitials may also contribute to the resistive switching process [55]. Such interstitial metal ions introduce positively charged point defects within the oxide lattice and act in a donor-like manner, similar to oxygen vacancies, thereby enhancing the electronic conductivity and participating in the formation and modulation of conductive paths within the oxide.

Electroforming

Before resistive switching can occur, the initially highly resistive pristine VCM cell must undergo an electroforming process [41]. This step involves applying a relatively high negative voltage to the AE, generating oxygen vacancies at the interface between the oxide and the OE. Following the Kröger-Vink notation [54], the reaction can be expressed as:

$$\mathrm{O}_{\mathrm{O}}^{X} \rightarrow V_{\mathrm{O}}^{\cdot\cdot} + 2e' + \tfrac{1}{2}\mathrm{O}_2 \tag{2.1}$$

where O_{O}^{X} represents an oxygen ion at a lattice site [56]. The released oxygen ($\frac{1}{2}O_2$) may either escape as gas [57] or react with the OE. The generated $V_{\mathrm{O}}^{\cdot\cdot}$ vacancies decrease the oxide resistance and increase the current flow [58]. This decrease in resistance occurs because oxygen vacancies act as donor defects, increasing the number of free electrons in the oxide and thereby improving its electrical conductivity. Under an applied electric field, oxygen vacancies accumulate in localized regions, creating highly conductive paths that serve as precursors for filament formation during electroforming. As the current rises, Joule heating raises the local temperature, further accelerating vacancy generation. Without adequate current limitation, this feedback can lead to thermal runaway and irreversible damage [56]. In earlier studies, dielectric breakdown was considered a major reliability issue in MOSFETs due to its effect on the gate dielectric [59]. In VCM devices, however, a controlled dielectric breakdown results in an n-type conductive filament that reduces the oxide resistance [56]. In addition to filamentary switching, which is the focus of this work, some studies report an interface-type switching mechanism in which vacancies are distributed across the entire device area rather than confined in a filament [41].

Electroforming can be initiated either by a triangular voltage (or current) sweep or by applying a rectangular pulse. In both cases, a threshold must be reached. When a triangular sweep is used, the forming voltage depends on the sweep rate. In pulsed operation, the probability of electroforming increases with both pulse duration and amplitude. The forming kinetics are influenced by internal factors such as grain size and oxide microstructure, as well as external parameters like temperature and ambient atmosphere [56]. Higher ambient temperatures generally accelerate the forming process [56, 60]. The oxygen partial pressure also affects oxide resistance [56, 61], and atmospheric humidity has been shown to influence forming behavior strongly [57].

The material of the OE has a direct effect on forming. Guo *et al.* calculated the defect formation energy (DFE) needed to create an oxygen vacancy at the interface between the OE and the oxide [62]. This was determined by subtracting the oxide free energy gained from oxidizing the OE metal from the formation energy of one oxygen vacancy in the bulk oxide [62]. Their findings indicate that the DFE increases with the oxygen chemical potential of the metal, which means higher forming voltages are required for such materials [62]. This theoretical prediction was experimentally verified by Wiefels *et al.*,

who demonstrated a clear correlation between increased DFE, higher forming voltages, and enhanced device endurance for different OE materials in oxide-based resistive switching memories [63].

Resistive Switching

The general switching behavior of a formed VCM cell is illustrated in Figure 2.5, using a $Pt/ZrO_x/Zr$ device as an example. The active Pt electrode is on the left, and the ohmic Zr electrode is on the right, adjacent to the switching ZrO_x layer.

After electroforming, the device is in the LRS or ON state, as shown in Figure 2.5(C). The oxide layer is bridged by an n-type conductive filament formed by oxygen vacancies. This filament consists of a plug region near the OE and a disc region near the AE. The Schottky barrier height at the AE/oxide interface depends on the oxygen vacancy concentration in the disc region. A high vacancy concentration in the LRS results in a reduced barrier height and consequently lower resistance [41].

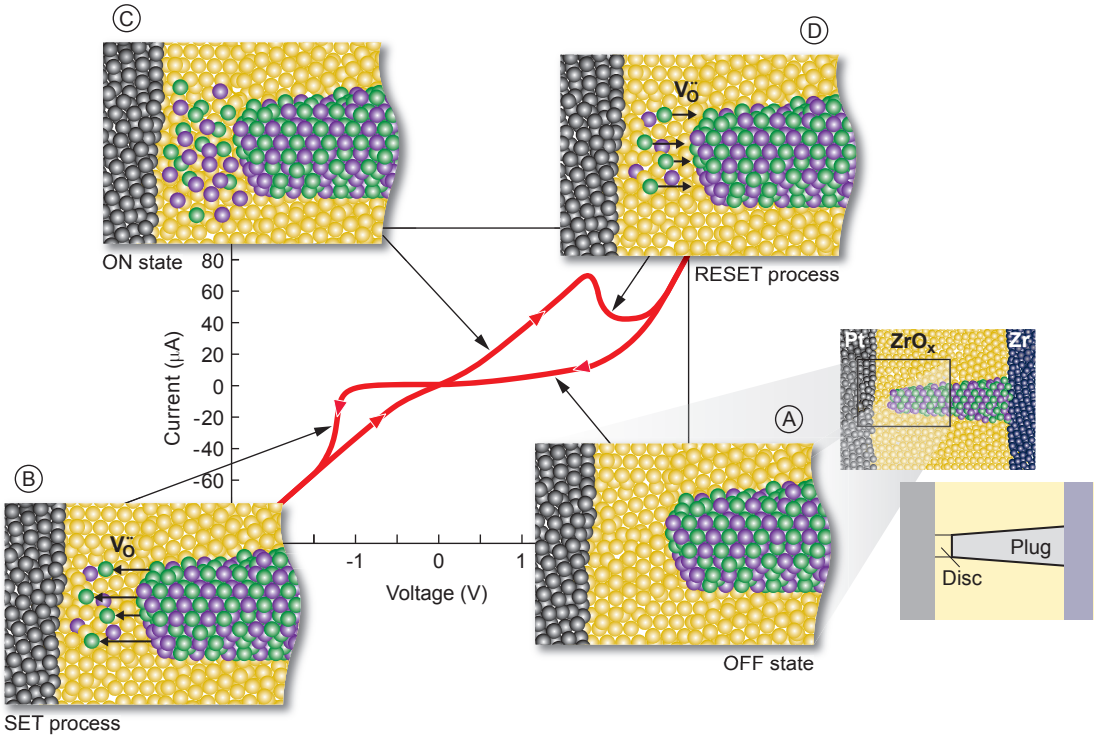


Figure 2.5: Illustration of the (counter eight-wise) VCM switching mechanism in a $Pt/ZrO_x/Zr$ cell. The conductive filament is composed of a plug and disc region (see inset on the right). (A) In the HRS or OFF state, oxygen vacancies are depleted in the disc, leading to a high Schottky barrier and increased resistance. (B) Applying a negative voltage to the AE shifts oxygen vacancies from the plug to the disc, initiating the SET process. (C) This results in the LRS or ON state, where a higher vacancy concentration lowers the Schottky barrier. (D) A positive voltage at the AE moves the vacancies back into the plug, RESETs the cell. Reproduced from [41], © 2012 Wiley-VCH Verlag.

When a positive voltage is applied to the AE, oxygen vacancies drift from the disc into the plug, partially re-oxidizing the disc region. This RESET process (D) increases the barrier height and switches the device to the HRS or OFF state, as shown in Figure 2.5(A). The HRS resistance remains lower than the pristine state before forming [41]. Applying a negative voltage to the AE moves vacancies from the plug back into the disc, restoring the LRS in the SET process (B) [41]. This switching mechanism represents the counter eight-wise (c8w) mode, where the *I-V* curve follows the reverse direction of drawing the number eight [41]. Although both c8w and eight-wise (8w) or anomalous switching modes [64] have been observed in different VCM systems [65–68], this work focuses on the commonly observed c8w mode. While the model depicted in Figure 2.5 explains many experimental characteristics [69], the conduction mechanism in VCM-type ReRAM remains a topic of discussion.

In this thesis, TaO_x based VCM devices were investigated due to their fast and stable resistive switching characteristics. These devices exhibit extremely short SET times, reported to be as low as 20 ps [6, 17]. However, the RESET operation is intrinsically limited by the coexistence of a unipolar switching mode, where instead of a full RESET, a unipolar SET event can occur at higher voltages. This effect can be mitigated by inserting an ultrathin Al_2O_3 interfacial layer between the oxide and the electrode, which suppresses oxygen exchange and improves RESET stability [70].

2.4. High Frequency Domain

High-speed writing processes require fast signals, typically associated with high frequencies, commonly referred to as radio frequencies (RF). These high frequencies correspond to short electrical wavelengths, which can pose challenges when the wavelength becomes shorter than the length of the transmission line under consideration [71]. In such situations, the voltage distribution varies along the transmission line and must be analyzed using transmission-line theory, which is introduced in the subsequent section below. The concepts of phase velocity and skin depth are also examined, as they are relevant to the objectives of the present research. The significance of transmission-line theory for experiments involving VCM devices operating within the RF range is further discussed, concluding with the definition of scattering parameters. The content presented in this section is based on *Microwave Engineering* by Pozar [71].

Maxwell's equations play a crucial role in analyzing electromagnetic phenomena within the RF regime. These equations provide the foundation for understanding the propagation of electromagnetic waves through various media, allowing RF signals to be described as waveforms. Furthermore, Maxwell's equations enable the calculation of necessary quantities such as phase velocity and skin depth. The phase velocity, denoted v_p, represents the speed at which an electric field propagates through a given medium and is expressed

as:

$$v_p = \frac{c}{\sqrt{\varepsilon_r \mu_r}} \tag{2.1}$$

where c denotes the speed of light in a vacuum, ε_r is the relative permittivity, and μ_r is the relative magnetic permeability of the medium. In the case of a cable where a non-magnetic expanded polytetrafluoroethylene (ePTFE) dielectric surrounds the inner conductor, the relative permeability is typically approximated as $\mu_r \approx 1$. For a dielectric with a relative permittivity of $\varepsilon_r = 1.7$ [72], the phase velocity (v_p), as determined by Equation 2.1, is approximately 2.30×10^8 m/s, which corresponds to around 75% of the speed of light.

The skin depth, δ_s, is defined as the distance within a conductor at which the amplitude of a signal undergoes attenuation by a factor of e^{-1} and is represented as:

$$\delta_s = \sqrt{\frac{2}{\omega \mu \sigma}} \tag{2.2}$$

In this equation, ω is the angular frequency, $\mu = \mu_r \mu_0$ is the magnetic permeability of the conductor, with μ_0 representing the permeability of free space, and σ is the electrical conductivity of the conductor.

In this thesis, the conductors of VCM devices are made of Pt, which is non-magnetic ($\mu_r = 1$) and possesses a high electrical conductivity of $\sigma = 9.52 \times 10^6$ S/m at 20°C [73]. Based on Equation 2.2, this yields a skin depth of $\delta_s = 816$ nm at a frequency of 40 GHz. Since the thickness of the Pt electrodes (30 nm) is much smaller than the calculated skin depth at 40 GHz ($\delta_s = 816$ nm), the electromagnetic field penetrates the entire electrode thickness. Therefore, attenuation of high-frequency signals is not governed by the classical skin effect.

2.4.1. Transmission-Line Theory

A transmission line can be modeled as a series of infinitesimally small segments of length Δz, each containing distributed electrical elements. Specifically, each segment is characterized by a series resistance per unit length R, a series inductance per unit length L, a shunt conductance per unit length G, and a shunt capacitance per unit length C. These elements are illustrated in Figure 2.6. The signal traveling along the line is described by its voltage $v(z,t)$ and current $i(z,t)$, both of which vary with position z along the transmission line and with time t. By applying Kirchhoff's voltage and current laws to the circuit model, two fundamental equations describing the voltage and current propagation can be derived:

$$v(z,t) - R\Delta z i(z,t) - L\Delta z, \frac{\partial i(z,t)}{\partial t} - v(z+\Delta z,t) = 0 \tag{2.3}$$

$$i(z,t) - G\Delta z v(z+\Delta z,t) - C\Delta z, \frac{\partial v(z+\Delta z,t)}{\partial t} - i(z+\Delta z,t) = 0 \tag{2.4}$$

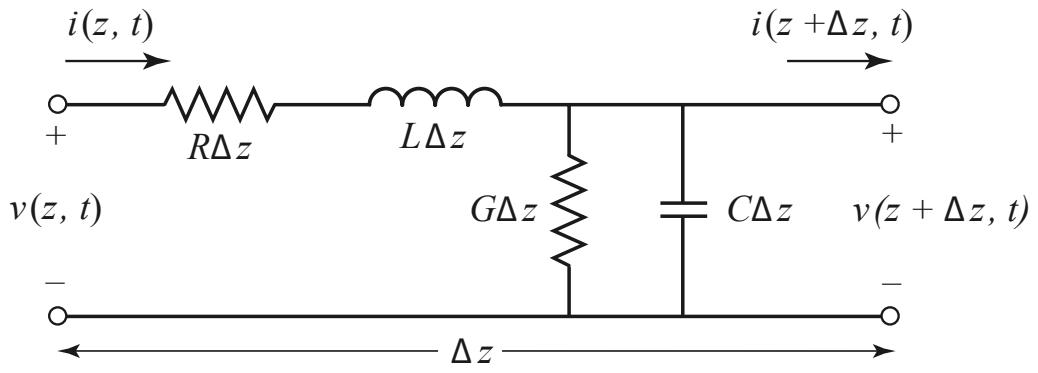


Figure 2.6: Infinitesimal segment Δz of a transmission line. The parameters are defined in the main text. Adapted from [71].

By dividing these equations by Δz and taking the limit as $\Delta z \to 0$, the telegrapher's equations are obtained:

$$\frac{\partial v(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t} \tag{2.5}$$

$$\frac{\partial i(z,t)}{\partial z} = -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t} \tag{2.6}$$

These equations are explicitly solved in *Microwave Engineering* by Pozar [71] by assuming sinusoidal waveforms for $v(z,t)$ and $i(z,t)$, characterized by an angular frequency ω and amplitudes V and I, respectively. For the scope of this thesis, only relevant steady-state solutions are considered. One key outcome of solving the telegrapher's equations is the expression for the characteristic impedance Z_0 of the transmission line:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.7}$$

If the transmission line is terminated by a load impedance Z_L, the voltage reflection coefficient Γ is given by:

$$\Gamma = \frac{v^-(t)}{v^+(t)} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.8}$$

Here, $v^+(t)$ represents the incoming voltage and $v^-(t)$ the reflected voltage. This solution highlights the importance of proper impedance matching of $Z_0 = 50\ \Omega$ at every connection in the experimental setup, since improper impedance matching would result in reflections of the incoming signal.

These two equations are of significant importance, as they enable estimation of the voltage effectively applied to the device under test (DUT), which, in the context of this thesis, is mainly a VCM device. The voltage at the device, $V_{\mathrm{DUT}}(t)$, is determined by the sum of the incoming and reflected voltage components. By substituting Equation 2.8 for

$v^-(t)$, it becomes evident that $V_{\mathrm{DUT}}(t)$ depends strongly on both Z_L and Z_0:

$$V_{\mathrm{DUT}}(t) = v^+(t) + v^-(t) = 2v^+(t)\frac{Z_L}{Z_L + Z_0} \tag{2.9}$$

This relationship will be used in the following sections to determine the actual voltage applied to the DUT during measurements.

2.4.2. Experimental Approach

Most studies investigating the kinetics of VCM devices utilize pulse generators and cables with a characteristic impedance of $Z_0 = 50\ \Omega$. However, VCM devices typically exhibit significantly higher resistance values, even in the LRS, where $Z_L > 1\ \mathrm{k}\Omega$. In such cases, where $Z_L \gg Z_0$, Equation 2.8 simplifies to a reflection coefficient $\Gamma = 1$, indicating that the entire signal is reflected at the device. As a result, according to Equation 2.9, the voltage at the DUT becomes twice the incoming voltage $V_{\mathrm{DUT}}(t) = 2v^+(t)$.

Once the pulse reaches the DUT, the reflected signal travels back toward the pulse generator. The time required for the pulse to propagate from the pulse generator to the DUT is defined as the setup time t_{setup}:

$$t_{setup} = \frac{l_{cable}}{v_p} \tag{2.10}$$

where l_{cable} is the length of the cable, and v_p is the phase velocity in the transmission line. If the width of the input pulse is at least twice t_{setup}, the incoming and reflected signals will superimpose at all points along the cable, resulting in a doubling of the voltage.

Assuming a cable length of $l_{cable} = 1$ m and a relative permittivity of $\varepsilon_r = 1.7$ [72], the calculated value for t_{setup} using Equation 2.1 and Equation 2.10 to be approximately 4.35 ns. Kinetic measurements of VCM devices can typically be categorized into two distinct regimes: a slow regime, concerning measurements with time scales greater than 10 ns ($2t_{\mathrm{setup}} \approx 10$ ns), and a fast regime, where the kinetics occur at time scales below 10 ns. Since the present study focuses primarily on the fast regime, only the experimental approach relevant to this work and applied in this regime is described in the following. Further experimental methodologies and detailed discussions can be found in von Witzleben [70].

In the slow regime, voltages and currents can often be interpreted using simple DC principles [16, 67, 74, 75]. However, in the fast regime, DC rules are no longer applicable, and instead, the equations presented in Section 2.4.1 must be employed. All pulse generators, oscilloscopes, and passive components, such as cables and connectors, have characteristic impedances of 50 Ω, which ensures proper impedance matching across the system. In this study, the experimental approach corresponds to the configuration shown in Figure 2.7, where the DUT is directly connected to the pulse generator. However, due to the high resistance of the DUT relative to $Z_0 = 50\ \Omega$, nearly the entire incoming signal V_P

is reflected. As a result, the voltage at the DUT effectively doubles, leading to $V_{\mathrm{DUT}} = 2V_P$. As also observed in previous studies employing the same method, the reported voltage corresponds to twice the set pulse amplitude of the generator [70, 76–79].

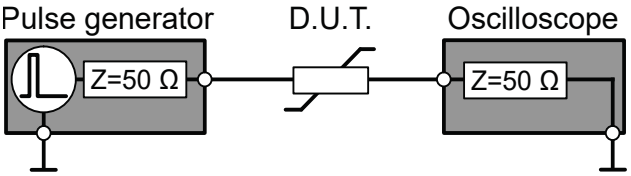


Figure 2.7: Experimental setup used in the fast regime, where the DUT is directly connected to the pulse generator. Adapted from [70].

The capacitances and inductances inherent in cables influence the pulses generated by the pulse generator, causing the actual signal applied to the device to differ from the original emitted signal. Additionally, signal reflections occur at every connection point, leading to partial signal loss before reaching the device. Therefore, each component in the RF circuit must be carefully selected to minimize these effects.

For example, even a standard 2.92 mm adapter can introduce a signal loss of approximately -0.5 dB at 40 GHz [80], corresponding to around 5.6% loss. Similarly, typical coaxial cables exhibit attenuation between 2 dB/m and 3 dB/m at the same frequency [81], which translates to a signal loss between 20.6%/m and 29.6%/m. To minimize these losses, it is recommended to use the fewest possible interconnects and to keep cable lengths short. Consequently, all RF components utilized throughout this thesis have been specifically optimized for operation at 40 GHz.

Coplanar Waveguides (CPWs)

CPW structures were integrated into the device layout to minimize impedance mismatch between the sample contact pads and the measurement probes [6, 76, 78]. As illustrated in Figure 2.8, CPWs consist of three parallel metallic stripes: an inner conductor (S) that carries the signal, and two outer conductors (G) connected to ground. CPWs offer several advantages, notably their compatibility with standard CMOS fabrication processes [82] and their wide operational bandwidth, which extends from DC to beyond 100 GHz [83].

The characteristic impedance Z_0 of a CPW is determined by the relative permittivity ε_r of the substrate and the physical geometry of the waveguide, specifically, the width w of the inner conductor, the spacing s between the inner and outer conductors, and the substrate thickness h [84].

In an ideal case, if the CPW conductors were entirely suspended in air, solving the Laplace equation would yield transverse electromagnetic (TEM) wave propagation, where electric and magnetic field components along the direction of the conductors are zero [71, 85]. However, the presence of a substrate alters this behavior. Due to the difference in relative permittivity between the air above and the substrate below the conductors, the

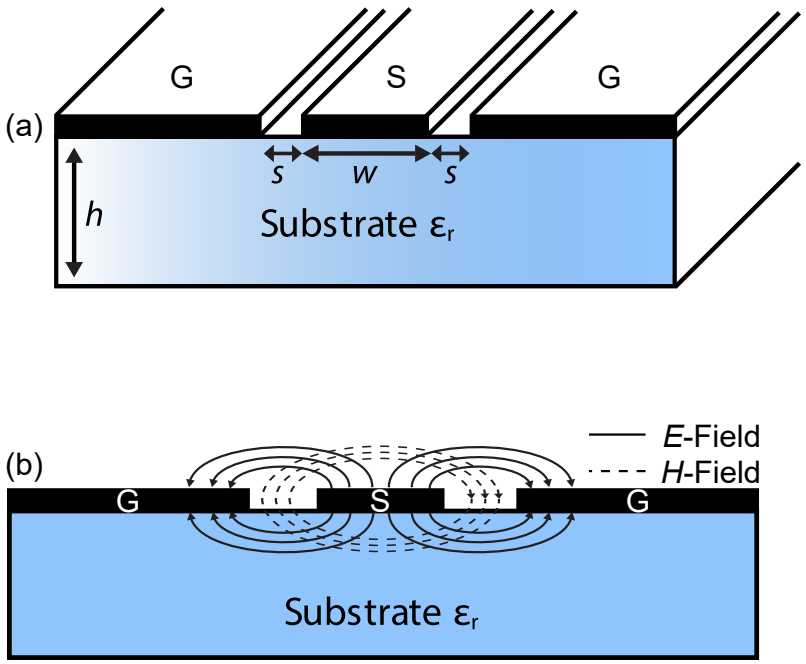


Figure 2.8: (a) Ground-Signal-Ground (GSG) CPW structure. (b) Electric field (solid line) and magnetic field (dashed line) distribution in CPW.

electromagnetic fields are distributed unevenly. Consequently, the CPW supports quasi-TEM modes, which are illustrated in Figure 2.8 and discussed in detail in *Microwave Engineering* by Pozar [71].

2.4.3. Scattering Parameters

Scattering parameters, or *S*-parameters, are widely used to characterize the transmission and reflection behavior of electrical signals in high-frequency networks [71]. The parameter S_{ij} describes the relationship between the incoming signal $v_i^+(t)$ at port i and the outgoing signal $v_j^-(t)$ at port j. When $i = j$, S_{ii} represents the reflection at port i, whereas for $i \neq j$, S_{ij} indicates transmission from port j to port i [71]. These parameters are frequency-dependent, with $S_{ij}(f) > 1$ indicating gain in the signal's components at a given frequency f and $S_{ij}(f) < 1$ signifies attenuation.

The scattering parameters $S_{ij}(f)$, along with the input signals $V_i^+(f)$ and the output signals $V_i^-(f)$, are defined in the frequency domain and are inherently complex-valued. These input and output quantities are obtained by applying the Fourier transform to the time-domain representations of the signals. Specifically, $V_i^+(f)$ results from the Fourier transformation of the incoming signal $v_i^+(t)$, while $V_i^-(f)$ corresponds to the Fourier transformation of the reflected or transmitted signal $v_i^-(t)$. The Fourier transformation of the time-domain signals is given as:

$$V_i^+(f) = F(v_i^+(t)), \quad V_i^-(f) = F(v_i^-(t))$$

For an n-port network, the relationship between incoming and outgoing signals is described by the scattering matrix:

$$\begin{pmatrix} V_1^- \\ \vdots \\ V_n^- \end{pmatrix} = \begin{pmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & \ddots & \vdots \\ S_{n1} & \cdots & S_{nn} \end{pmatrix} \cdot \begin{pmatrix} V_1^+ \\ \vdots \\ V_n^+ \end{pmatrix}. \tag{2.11}$$

In the specific context of this work, focusing on a two port network such as a ReRAM device with two contacts, the scattering matrix simplifies considerably to:

$$\begin{pmatrix} V_1^- \\ V_2^- \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \cdot \begin{pmatrix} V_1^+ \\ V_2^+ \end{pmatrix}. \tag{2.12}$$

During kinetic measurements, the electrical pulses are typically applied to only one contact of the DUT. Consequently, the second component of the incoming signal, V_2^+, can be neglected (i.e., $V_2^+ = 0$). This simplification means that only two components of the scattering matrix from Equation 2.12 become relevant for our analysis: the forward reflection coefficient (S_{11}) and the forward transmission coefficient (S_{21}). These are defined as:

$$S_{11} = \left.\frac{V_1^-}{V_1^+}\right|_{V_2^+=0} \tag{2.13}$$

$$S_{21} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0} \tag{2.14}$$

Once S_{11} and S_{21} are known, the reflected and transmitted components of the incoming signal, $v_1^-(t)$ and $v_2^-(t)$, can be reconstructed. This is done by applying the inverse Fourier transform to the corresponding frequency-domain signals, $V_1^-(f)$ and $V_2^-(f)$:

$$v_1^-(t) = F^{-1}(V_1^-(f)) \tag{2.15}$$

$$v_2^-(t) = F^{-1}(V_2^-(f)) \tag{2.16}$$

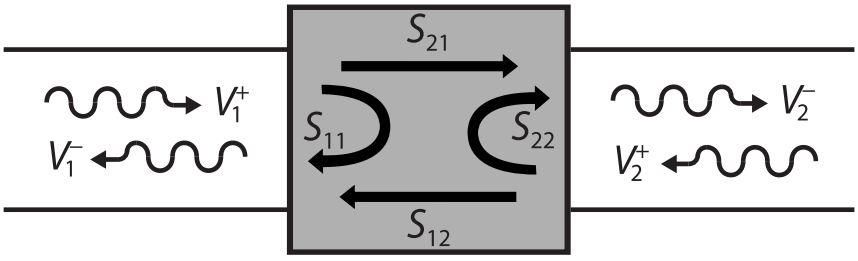


Figure 2.9: Illustration of S-parameters in a two-port network.

This method is employed in Section 3.3.2 to compute the time-dependent voltage at the DUT, $V_{\mathrm{DUT}}(t)$, which is obtained by summing the incoming wave $v_1^+(t)$ and the reflected wave $v_1^-(t)$, as described in Equation 2.9. Further experimental procedures for extracting the scattering parameters are also described in the same section.

2.4.4. Fourier Transformation of a Square Pulse

Square pulses are frequently used when investigating the switching behavior of VCM devices. To accurately assess the effective voltage response at the device, it is necessary to analyze the frequency content of these pulses. This is done using the Fourier transform, as previously discussed in Section 2.4.3. The following derivation, based on the reference [86], outlines the analytical transformation of a square pulse into the frequency domain.

An ideal square pulse $x(t)$ of width T is defined as:

$$x(t) = \begin{cases} 1 & \text{for } |t| \leq T/2 \\ 0 & \text{for } |t| > T/2 \end{cases} \tag{2.17}$$

Applying the Fourier transform to $x(t)$ yields:

$$\begin{aligned} F(x(t))(f) &= \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} x(t) e^{-ift}\, dt \\ &= \frac{1}{\sqrt{2\pi}} \int_{-T/2}^{T/2} e^{-ift}\, dt \\ &= \frac{1}{\sqrt{2\pi}} \left[\frac{e^{-ift}}{-if} \right]_{-T/2}^{T/2} \\ &= \frac{1}{\sqrt{2\pi}} \cdot \frac{1}{-if} \left(e^{-ifT/2} - e^{ifT/2} \right) \\ &= \sqrt{\frac{2}{\pi}} \cdot \frac{\sin\left(\frac{fT}{2}\right)}{f} \end{aligned} \tag{2.18}$$

The result is a sinc-shaped function in the frequency domain. A visual representation of this transformation for a 10 ns square pulse can be found in von Witzleben [70].

2.5. Multilevel and Gradual Conductance Modulation in Filamentary VCM

Since filamentary VCM devices can, in principle, adjust their conductance over a wide range, they have long been considered strong candidates for multilevel memory applications. Achieving a large number of stable intermediate states would enable each device

to store multiple bits of information, thereby greatly increasing memory density without requiring additional area.

Early studies have shown that VCM cells are theoretically capable of supporting many distinct conductance levels. Sheng *et al.* [12] demonstrated more than 256 resistance states (8 bits) in a single device when the full conductance window was utilized. Even under low-power operation, they were able to achieve eight- and four-state programming corresponding to 3-bit and 2-bit storage [12]. Similarly, Stathopoulos *et al.* [13] reached approximately 92 distinguishable levels by modifying the interfacial oxide stack. More recently, Rao *et al.* [87] demonstrated up to 2,048 distinguishable conductance states in HfO_2-based memristors integrated with CMOS circuitry by reducing conductance noise through repeated verification and denoising steps. While this result demonstrates the analog programmability of VCM devices, achieving thousands of stable states requires active noise suppression and feedback-based control rather than relying on intrinsic switching behavior, which poses challenges for fast and scalable array-level operation.

Despite these demonstrations, most practical implementations report only a few reliably programmable states, typically between two and eight, due to variability, overlap between intermediate levels, and strong fluctuations in the filament evolution process [77, 88–97]. Review studies confirm that although filamentary structures may support a large number of internal microstates, only a small subset can be used as reproducible multilevel states under standard operating conditions [42, 98]. These works established the potential for multilevel operation but also revealed the intrinsic difficulty of stabilizing closely spaced intermediate resistances.

As research progressed, the focus gradually shifted from merely demonstrating the number of accessible intermediate states in a device to understanding how to achieve gradual and linear conductance evolution. Studies conducted on a broad range of material systems, such as HfO_2 [7, 18, 99–106], Ta_2O_5 [107–111], $SrTiO_3$ [112], Al_2O_3 [113–115], and TiO_2 [116, 117], have shown that gradual conductance modulation is indeed possible. However, such behavior is typically confined to narrow operational windows and is frequently accompanied by significant variability or non-linear response characteristics [118–120]. The key challenge originates from the intrinsic nature of the SET transition in filamentary VCM devices. These devices often switch abruptly due to strong electro-thermal feedback, where increased current leads to local Joule heating, which accelerates vacancy migration and rapidly reinforces filament growth. This positive feedback loop, extensively analyzed in kinetic studies [16, 20], makes it inherently difficult to achieve small, predictable conductance increments required for neuromorphic applications.

More recent work has therefore focused on controlling the dynamics of the switching process. Early indications of gradual switching were reported by Stathopoulos *et al.* [13], who showed that dividing the operation into several short pulses enabled small, stepwise resistance changes, suggesting that limiting the energy delivered per pulse can slow

filament growth and support controlled conductance modulation. Hardtdegen *et al.* [10] later demonstrated that the initial LCS plays a key role in this behavior, as the thermal and structural conditions of the filament at the beginning of switching largely determine whether the SET transition becomes gradual or abrupt. Building on these insights, Cüppers *et al.* [7] showed that using pulse widths shorter than the device's intrinsic transition time helps suppress electro-thermal runaway, enabling more linear conductance evolution over several applied short pulses. Collectively, these studies highlight the importance of the filament's thermal time constant. Since thermal feedback requires a finite delay before it becomes significant, applying pulses that are shorter than this delay suppresses abrupt switching and helps the device remain in a gradual switching mode [7]. However, because earlier work was limited to pulses in the nanosecond range, the achievable linear regime remained narrow, with only about ten states accessible before abrupt switching dominated again [7]. This limitation raises the question of whether much shorter pulses could further suppress thermal feedback and enable more gradual and linear potentiation. These open questions form the basis of the investigations presented in Chapter 4, where gradual and linear potentiation is examined using ultra-short pulses to explore switching behavior in a regime where thermal feedback is expected to be significantly reduced.

2.6. Fundamental Aspects of Thermal Effects in VCM Devices

In recent years, memristors have emerged as promising candidates for emulating synaptic functions within biologically inspired neuromorphic systems [121]. In such systems, presynaptic spikes (action potentials) are transmitted through the synapse (memristor), and postsynaptic responses are generated, whose amplitudes are determined by the synaptic weight, that is, the conductance of the memristor. This synaptic weight can be modified by spikes coming from pre- and postsynaptic neurons, and the updated weight can be retained over long periods, thereby enabling learning and memory in the system.

Several studies have demonstrated key synaptic learning rules, most notably spike timing dependent plasticity (STDP), using memristors [19, 122, 123]. However, in these studies, memristors were effectively treated as programmable resistors rather than dynamic physical systems. To implement a given synaptic learning rule, the spike waveforms had to be carefully designed so that the overlap of pre- and postsynaptic spikes produced a suitable effective programming pulse width or amplitude, thereby encoding information about the relative timing of the two spikes [19, 122, 123]. In a spike-based, asynchronous system, such overlap was necessary because there was no other internal mechanism to represent relative spike timing and use it to modulate the memristor response under different stimulation conditions [24]. This limitation arises because, in these devices, conductance

modulation, determined by an internal state variable such as the conduction channel size w, was directly controlled only by the input voltage V and the state variable itself, expressed as:

$$\frac{dw}{dt} = f(w, V, t) \tag{2.19}$$

Consequently, achieving the desired conductance change required careful engineering of both pulse width and pulse height [19, 122, 123]. Such devices are mathematically classified as first-order memristors [124].

In biological synapses, plasticity is driven by simple, generally non-overlapping spikes. It is mainly controlled by synaptic activity (for example, spike frequency and relative timing) rather than by the precise shape or amplitude of the spikes [125–128]. A crucial point is that the spikes themselves do not directly change the synaptic weight. Instead, it is modulated by secondary internal state variables, most importantly the postsynaptic calcium ion (Ca^{2+}) concentration. During a spike, the Ca^{2+} concentration increases and then gradually decays over time. This temporal evolution acts as an internal timing mechanism, because at the moment a spike occurs, the Ca^{2+} level is determined by the combined effect of the current spike and the residual Ca^{2+} remaining from earlier spikes. Because Ca^{2+} decays between spikes, the relative timing of spikes is automatically encoded in the current Ca^{2+} value. Models based on Ca^{2+} dynamics have successfully explained a wide range of synaptic plasticity phenomena, including long-term plasticity and STDP [126, 127]. In contrast, first-order memristors lack Ca^{2+}-like internal dynamics because a single state variable governs their conductance, typically the size of a volatile conduction channel [129, 130]. As a result, they require engineered pulse shapes for each learning rule [131, 132] and yield only phenomenological, non-biorealistic implementations [124].

A more comprehensive approach considers memristors as dynamic devices governed by internal processes, as emphasized in the theoretical framework [121], rather than a simple programmable memory device, analogous to calcium signalling in biology. From this viewpoint, second-order memristors [124] can be formulated, in which the primary conductance state variable w is further regulated by an additional internal variable T. The presence of this secondary state variable introduces more complex temporal dynamics and enables the device to reproduce biorealistic synaptic behaviors. Mathematically, the model can be expressed as [124]:

$$\frac{dw}{dt} = f(w, T, V, t) \tag{2.20}$$

As expressed in Equation 2.20, w denotes the first-order weight state variable, and T represents a second-order state variable. When T exhibits Ca^{2+}-like dynamics, the device can reproduce biorealistic synaptic functions. This internal timing mechanism enables activity-dependent modulation of the conductance without the need for overlapping input pulses or specially engineered spike shapes, thereby enabling memristive devices to

implement synaptic plasticity in a way that closely reflects biological processes [124].

A physical realization of such second-order behavior can be found in ReRAM devices, such as TaO_x. In addition to the conductance state, these devices possess a transient internal state variable, namely the local temperature T. When an electrical stimulus is applied, Joule heating causes T to increase, and after the stimulus is removed, T gradually relaxes back towards its initial value due to thermal dissipation [133–135]. Since the temperature influences the effective switching behavior of the device, the evolution of the conductance is indirectly controlled by this internal thermal state, analogous to the way synaptic plasticity in biological neurons is regulated by the intracellular Ca^{2+} concentration [126–128].

The presence of this internal thermal state becomes especially evident when examining the thermal response of ReRAM cells under pulsed operation. Previous studies have shown that this thermal behavior provides clear evidence of second-order dynamics [24, 25]. Because these devices have a finite thermal capacitance, they remain thermally active for a short period after a pulse, allowing the effective temperature to be adjusted simply by varying the delay between pulses in a pulse train [24, 25, 136], as illustrated schematically in Figure 2.10. The figure shows that short-delay pulses cause thermal accumulation in the RRAM device, leading to a higher temperature and an additional rise of ΔT after the second pulse, whereas long-delay pulses do not produce this increase. Kim *et al.* [24] demonstrated this behavior using a two-pulse protocol that separated heat generation from resistive switching. In their work, a long, low-voltage heating pulse and a short programming pulse did not produce switching when applied individually. However, when the delay between the two pulses was reduced to a sub-microsecond timescale (e.g., 100 ns), residual heat from the first pulse lowered the activation barrier for the second, resulting in a timing-dependent change in conductance. These observations provide strong evidence for second-order behavior and show that internal temperature dynamics can act as an intrinsic timing mechanism, linking the physical operation of ReRAM devices to synaptic-like plasticity [24].

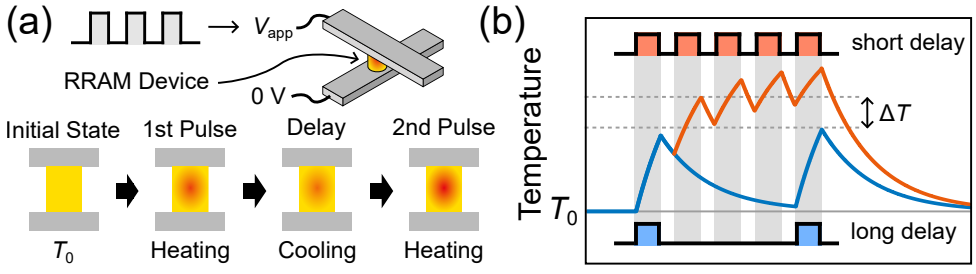


Figure 2.10: (a) Schematic illustration of thermal accumulation in an RRAM device when voltage pulses are applied with a short delay. (b) Comparison of the temperature evolution for pulse trains with short and long delays, showing that only the short-delay case exhibits an additional temperature increase ΔT after the second pulse. Reproduced from Schön *et al.* [137], © 2025 The Authors, licensed under CC BY 4.0.

Schön *et al.* [25] extended this concept by studying thermal effects in TaO_x-based

VCM devices using electrothermal simulations coupled to a compact switching model. Their work showed that, due to the transient thermal response of the device, residual heat from preceding voltage pulses can influence the switching behavior of subsequent pulses when the temporal spacing between them is sufficiently short, as illustrated schematically in Figure 2.10. Therefore, the effective switching kinetics depend on the delay between consecutive voltage pulses. Under these conditions, closely spaced pulses lead to thermal accumulation, resulting in an elevated device temperature. This temperature increase reduces the activation barrier for ion migration, thereby accelerating conductance changes. For sufficiently long pulse delays, the thermal accumulation effect is no longer observed, and the switching dynamics are no longer affected by pulse spacing. These observations suggest that temperature can serve as a secondary internal state variable in VCM devices, providing a physical basis for frequency-dependent potentiation and STP. Following the simulation study by Schön *et al.* [25], Chapter 5 investigates these thermal dynamics experimentally using delay-dependent switching measurements with ultra-short voltage pulses.

2.6.1. Fundamental Concepts of PPF and PTP

The previous section established that device temperature functions as a second state variable in oxide-based memristors. Since the device temperature does not return immediately to its equilibrium value after a pulse is applied, the response to a subsequent pulse depends on the spacing between stimuli. This transient modulation of conductance, arising from the internal temperature dynamics, resembles the short-term synaptic behavior observed in biological systems, where the strength of the synaptic response is influenced by recent activity rather than by individual spikes alone [24, 25, 136]. To place this behavior in a biological context and enable quantitative comparison, two forms of STP are introduced: paired-pulse facilitation (PPF) and post-tetanic potentiation (PTP). PPF refers to the enhancement of the second postsynaptic response relative to the first, whereas PTP describes a longer-lasting increase in synaptic strength following a train of stimuli. Both phenomena describe how the synaptic response varies with the interval between successive spikes. PPF and PTP are widely used metrics to benchmark STP in memristive synapses, as they provide a compact and quantitative description of rate-dependent conductance modulation across different material systems and device architectures.

Biological Mechanisms underlying PPF and PTP

The postsynaptic response of many biological synapses depends strongly on the timing between presynaptic spikes. In the granule-Purkinje cell synapse, two closely spaced presynaptic spikes produce an enhanced second response, demonstrating PPF, as shown by the green curve in Figure 2.11 [21]. Similar behavior is observed at the frog neuromuscular

junction, where a pair of stimuli (N = 2, yellow curve) again produces PPF, while a train of ten closely spaced stimuli (N = 10, blue curve) leads to the stronger cumulative enhancement associated with PTP [22, 23]. With increasing inter-stimulus interval, the magnitudes of both PPF and PTP decrease, consistent with the characteristic timing dependence of STP (see Figure 2.11).

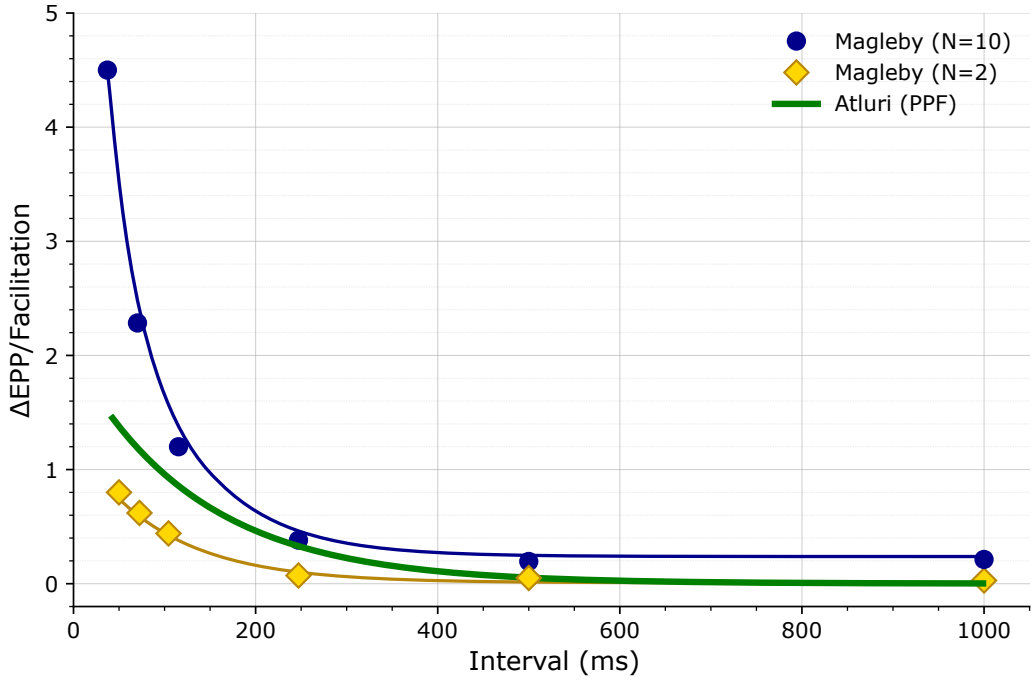


Figure 2.11: Effects on stimulation rates observed in biological systems, showing PPF data (green and yellow curves) and PTP data (blue curve). Adapted from [129].

These rate-dependent responses originate from the dynamics of calcium ions in the presynaptic terminal. A presynaptic spike opens voltage-gated calcium channels, allowing calcium to enter and trigger neurotransmitter release. After the spike, the calcium concentration decays gradually as it is removed through pumps and exchangers [21–23]. If a second spike arrives before the calcium level has returned to baseline, the residual calcium adds to the new influx, producing an enhanced postsynaptic response and giving rise to PPF. Under repeated stimulation, calcium accumulates across multiple spikes, resulting in the prolonged enhancement characteristic of PTP [21–23]. In oxide-based memristors operating as second-order devices, analogous interactions arise from thermal accumulation effects, where residual device heating from preceding pulses modulates the response to subsequent stimuli, giving rise to pronounced rate-dependent behavior [24]. This alignment with biological STP mechanisms further supports the suitability of memristors for emulating memory transitions in neuromorphic systems. A similar investigation of STP, including both PPF and PTP, is carried out on the TaO_x-based device, with the behavior evaluated at sub-ns timescales and discussed in detail in Section 5.4.

Quantitative Definitions of PPF and PTP

Rate-dependent conductance modulation in memristive devices can be characterized using the metrics PPF and PTP [129, 138]. PPF quantifies the relative increase in current during the second pulse of a two-pulse sequence and is defined as:

$$\mathrm{PPF} = \frac{I_2 - I_1}{I_1},$$

where I_1 and I_2 denote the currents measured during the first and second pulses, respectively.

PTP describes the cumulative conductance enhancement that develops during a sequence of repeated pulses and is given by:

$$\mathrm{PTP} = \frac{I_n - I_1}{I_1},$$

where I_n is the current measured during the n^{th} (typically final) pulse of the pulse train.

These definitions capture how the device response depends on both the inter-pulse interval and the number of applied pulses. By systematically varying these parameters, the characteristic timescales and underlying mechanisms of STP in VCM devices can be quantitatively determined [129, 138, 139].

2.7. Coefficient of Determination

The Coefficient of Determination, often denoted as R^2, is a crucial statistical metric employed to evaluate the explanatory power of a regression model. It quantifies the proportion of the total variance in the dependent variable that is predictable from the independent variable(s) within the model [140]. In this thesis, the measure is applied in Chapter 4 to quantify the linearity of the switching region in the conductance evolution analysis.

The value of R^2 lies within the interval $[0, 1]$. An R^2 of 0 indicates that the model fails to explain any of the variability in the dependent variable, whereas a value of 1 signifies a perfect fit, with the model capturing the entire variability [140].

The coefficient of determination is computed using the following formula:

$$R^2 = 1 - \frac{\mathrm{SSR}}{\mathrm{SST}} = 1 - \frac{\sum_{i=1}^{n}(Y_i - \hat{Y}_i)^2}{\sum_{i=1}^{n}(Y_i - \bar{Y})^2} \tag{2.21}$$

In this expression, SSR represents the sum of squared residuals, which accounts for the unexplained variation in the model. SST stands for the total sum of squares, capturing the total variability in the observed data. The term Y_i refers to the actual observed value of the dependent variable for the i-th observation, while $\hat{Y}_i$ denotes the predicted value from the

regression model. The symbol $\bar{Y}$ represents the mean of the observed dependent variable values. This formulation allows R^2 to serve as a concise summary of how effectively the regression model accounts for the variability in the data. This definition and computation of the coefficient of determination are subsequently applied in Section 4.1.2 to quantify the linearity of the switching region in the conductance analysis.

3. Experimental Details

3.1. Experimental Setup

In this section, two RF measurement setups used for the electrical characterization of VCM devices are presented. Each setup serves a distinct purpose and reflects the evolution of the measurement environment over time. RF setup 1, initially built by von Witzleben [70], and RF setup 2, developed and upgraded during this thesis, were both utilized. The primary experiments were conducted using RF setup 1, while RF setup 2 was later introduced to improve automation and measurement efficiency. Detailed descriptions of both setups are provided in the following sections.

Figure 3.1 shows the RF measurement setup, including all components used in both RF setup 1 and RF setup 2. Each label corresponds to a key component within the setup, with further explanations provided later in the text. The photograph displays 11 main labeled components, which are listed below:

1. Cascade Microtech EPS150RF probe station
2. RF switch box
3. Sympuls pulse pattern generator (PPG30)
4. Sympuls pulse generator (PG5)
5. AMOtronics arbitrary waveform generator (AWG)
6. Tektronix DPO73304D oscilloscope [141]
7. Keithely 2634B
8. Device under test (DUT)
9. HP 8722ES VNA [142]
10. Computer controls the components for measurements
11. Computer's operating components

Most of the components shown in Figure 3.1 have been described in detail in [70]. For context, the Tektronix DPO73304D oscilloscope (pink 6 in Figure 3.1) has a bandwidth of $F_{Osc} = 33\,\text{GHz}$ and a sampling rate of $f_S = 100\,\text{GS/s}$ [141]. Its rise time (T_{Osc}, 10% to 90%) can be calculated as $T_{Osc} = 0.339/F_{Osc}$, and this is about 10.3 ps [143]. The Sympuls PG5 pulse generator (green 4 in Figure 3.1) provides a fixed output voltage of 2.5 V[1] and

[1] An alternative unit of the same model provides 5 V output with a pulse width range of 50 ps to 250 ps.

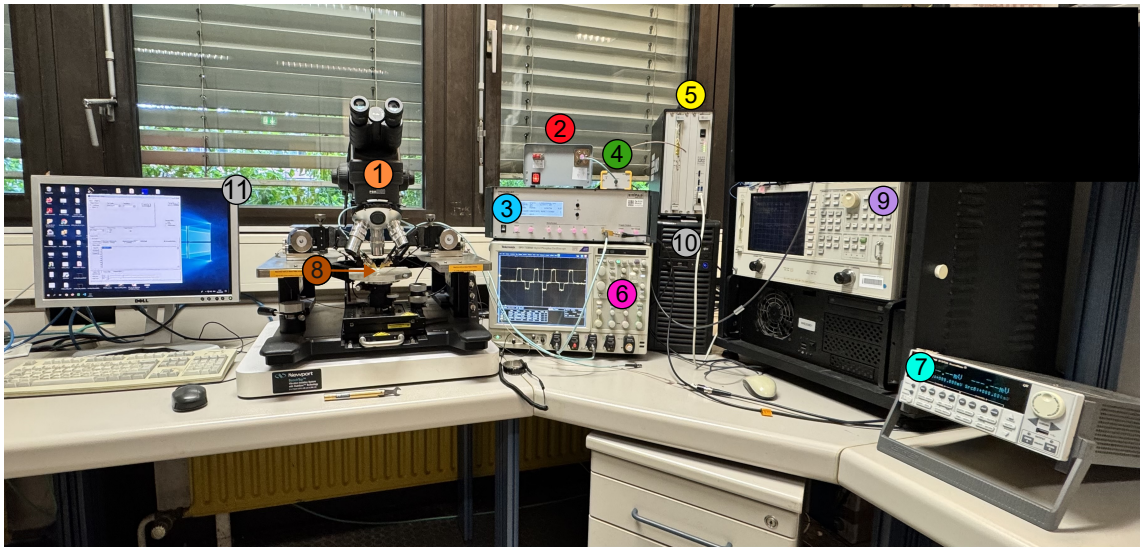


Figure 3.1: Photograph of the experimental RF measurement setup. The labeled components used in RF setup 1 and RF setup 2, as described in the main text.

able to generate pulse widths ranging from 50 ps to 100 ns. The amplitude can be adjusted using external attenuators ranging from 1 dB to 20 dB. In addition, the Keithley 2634B (cyan 7 in Figure 3.1) is a source measure unit (SMU) used in the RF setups.

All other passive components in the setup, including cables, attenuators, probes, and adapters, have a bandwidth of 40 GHz. The HP 8722ES vector network analyzer (VNA) (purple 9 in Figure 3.1) is used to measure the scattering parameters across a frequency range from 50 MHz to 40 GHz (see Section 3.3.2) [142]. All these components are connected to a computer (grey 10 and 11 in Figure 3.1) via GPIB and USB, and are controlled using the `py-ivtools`[2] software. The RF switch box, PPG30, and the AWG were also integrated into this software framework as part of this thesis.

Probe Station

The sample is connected to a Cascade Microtech EPS150RF probe station, indicated as orange 1 in Figure 3.1. To reduce disturbances caused by vibrations in the laboratory environment, the probe station is mounted on a Newport VIP600 vibration isolation platform. The RF signals are transmitted to the device, labeled as brown 8 in Figure 3.1, using Cascade Microtech Z40-X-GSG-100 RF probes with a bandwidth of up to 40 GHz [144]. These probes differ from those used in the original setup developed by von Witzleben [70], where Z40-X-GSG-150 probes were used. The change was necessary to accommodate the updated device structure employed in this work. The RF probes are positioned using two Cascade Microtech RPP210-S/100TPI probe positioners, allowing precise alignment. Visual inspection and alignment during measurements are performed using a Motic PSM 1000 microscope equipped with lenses offering magnifications of 5×, 10×, and 20×.

[2] Source code available at `https://git.rwth-aachen.de/hennen/py-ivtools/-/tree/Witzleben`

RF Switch Box

An RF switch box (indicated as red 2 in Figure 3.1) was integrated into the measurement setup to enable automated signal routing and minimize leakage currents. This box contains two coaxial switches from Ducommun: one SP3T (single-pole, triple-throw) switch from the 3K Series and one SPDT (single-pole, double-throw) switch from the 2K Series. Both switches feature 2.92-mm female connectors and support a frequency range from DC to 40 GHz, with a required operating voltage of 5 V DC. The SP3T switch provides three input paths and one output, while the SPDT switch offers two input paths and one output. These switches are controlled via a custom relay circuit that was programmed and integrated within the switch box assembly.

Pulse Pattern Generator (PPG30)

The PPG30 (indicated as blue 3 in Figure 3.1) integrated into the measurement setup is manufactured by Sympuls GmbH. This device has two independently programmable channels, as well as an additional bipolar output for generating both positive and negative pulses. It allows flexible adjustment of key parameters, including amplitude, pulse width, and repetition rate. The device operates over a frequency range from 200 Mbit/s to 30 Gbit/s and can generate pulse widths as short as 33 ps. The positive output amplitude ranges from 1 to 2 V_{pp}, while the negative output amplitude ranges from 0.6 to 1.2 V_{pp}. Additionally, the rise and fall times of the pulses are about 20 ps.

The PPG30 can produce pulse sequences with a pattern length of $128 \times m$ digits (where $m = 1, 2, \ldots, 2^{22}$), allowing for a maximum sequence length of 536,870,912 digits. Since each digit corresponds to a ternary value (positive, negative, or zero), the actual bit encoding uses a 2-bit scheme per digit for pattern storage. The PPG30 represents an upgraded version of the earlier Sympuls PG5, offering expanded functionality.

Arbitrary Waveform Generator (AWG)

An AWG from AMOtronics, indicated as yellow 5 in Figure 3.1, was integrated into the measurement setup. It features a four-channel digital-to-analog converter with a sampling rate of 1 GS/s and 16-bit resolution. Each channel provides an analog output accompanied by a digital synchronization signal to ensure precise timing. The output voltage is selectable between ± 3.3 V, ± 5 V, and ± 10 V, enabling a wide range of signal amplitudes. The AWG allows for flexible adjustment of pulse width, rise and fall times, and amplitude, enabling the generation of customized waveform shapes suitable for various device tests. Figure 3.2 illustrates a typical rectangular output pulse generated by the AWG, highlighting the key parameters amplitude A, rise time t_{rise}, duration t_{duration}, and fall time t_{fall}. This flexibility is particularly advantageous for evaluating advanced device architectures, such as PCM, ECM, and 1-transistor-1-memristor (1T1R) devices.

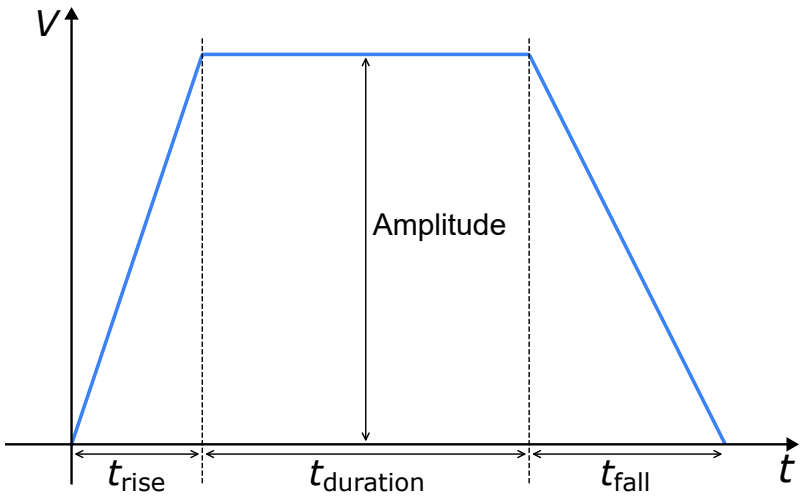


Figure 3.2: Rectangular pulse from the AWG with amplitude A, rise time t_{rise}, duration t_{duration}, and fall time t_{fall}.

3.1.1. RF Setup 1

The setup in Figure 3.3, referred to as RF setup 1, was originally developed by von Witzleben [70], as mentioned earlier. It includes key components such as the SMU, the pulse generators (PG5 or PPG30), the bias tee, the oscilloscope, and the attenuators (ranging from 1 dB to 20 dB). The attenuators [145] are crucial for adjusting the fixed voltage output from the PG5. The pulse voltage after attenuation, V_{P}, is defined as:

$$V_{\text{P}} = V_{\text{PG}} \cdot 10^{-\frac{A\,[\text{dB}]}{20}}, \tag{3.1}$$

where A is the attenuation in dB and V_{PG} is the output voltage of the PG5 with a fixed voltage of 2.5 V (alternative PG5 with a fixed voltage of 5 V). Due to reflection at the

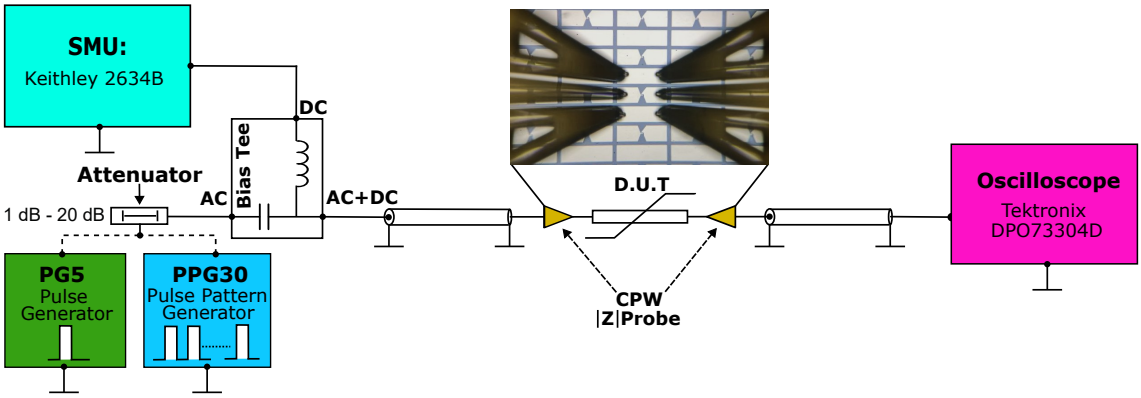


Figure 3.3: Schematic of RF setup 1, illustrating key components including the SMU, the pulse generators (PG5 or PPG30), the bias tee, the attenuators, and the oscilloscope. The color coding matches the components shown in the image of the experimental setup in Figure 3.1.

DUT, the pulse voltage effectively doubles, resulting in an effective pulse voltage, $V_{P,eff}$, which is also listed in Table 3.1. The bias tee is a key component of the setup, enabling the simultaneous application of alternating current (AC) and DC signals and providing automated, precise control over testing conditions. In some experiments, the PG5 pulse generator was used; in others, the PPG30 was introduced as an upgrade within the scope of this thesis.

Table 3.1: List of attenuators connected to the PG5 with a fixed output voltage of 2.5 V, showing the resulting pulse voltages V_P after attenuation and the corresponding effective voltages $V_{P,eff}$ at the DUT

Attenuation [dB]	V_P [V]	$V_{P,eff}$ [V]
0	2.50	5.00
1	2.23	4.46
2	1.99	5.01
3	1.78	3.54
4	1.58	3.16
5	1.41	2.81
6	1.25	2.51
7	1.12	2.23
8	0.99	1.99
9	0.89	1.77
10	0.80	1.58

3.1.2. RF Setup 2

The setup in Figure 3.4 illustrates RF setup 2, which was built within the scope of this thesis as an upgraded version of RF Setup 1. The primary difference is the use of an RF switch instead of a bias tee, as the RF switch helps automate measurements and avoids the leakage currents that can occur with a bias tee, especially at high resistances. Additionally, this setup incorporates an AWG, allowing for easy adjustment of the rise and fall times of the pulses, providing greater flexibility and precision in testing. Overall, this advanced setup extends the measurement capabilities to new types of devices, such as PCM and ECM devices, which often operate in a highly resistive state in the megaohm range.

It should be noted that throughout this thesis, SET pulses applied to VCM devices using either RF setup were always applied to the top electrode (TE)/OE of the device. This configuration was necessary due to the voltage output characteristics of both pulse generators. The PG5 provides only a positive fixed output voltage of 2.5 V (or 5.0 V in alternative units), while the PPG30 offers a low negative voltage range of 0.6 V to 1.2 V

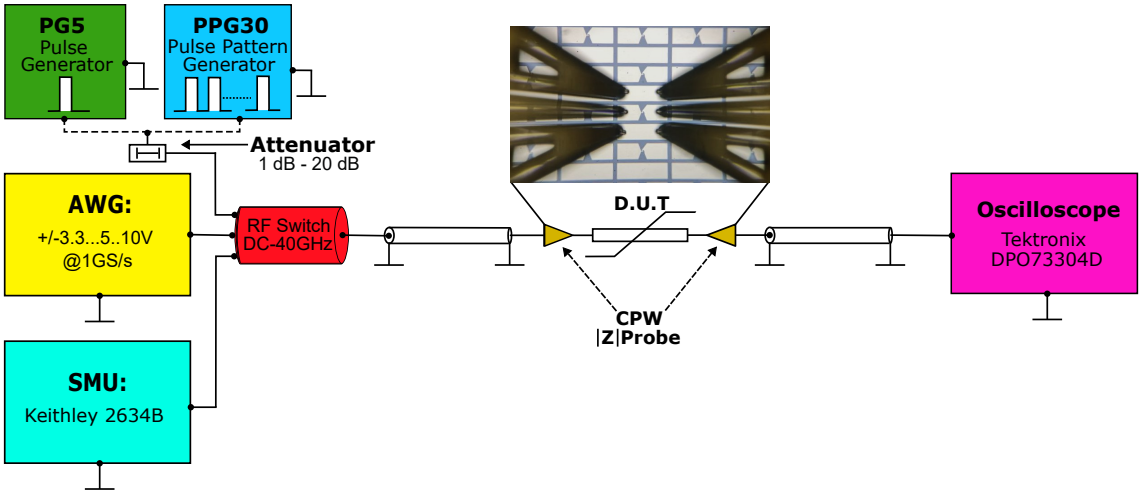


Figure 3.4: Schematic of RF setup 2, illustrating the key components including the SMU, AWG, pulse generators (PG5 or PPG30), RF switch, the attenuators, and the oscilloscope. The color coding matches the components shown in the image of the experimental setup in Figure 3.1.

compared to its positive range of 1.0 V to 2.0 V. Therefore, positive pulse voltages were applied to the OE to perform SET operations. Accordingly, the polarity of the SET and RESET *I-V* sweeps applied by the SMU during RF measurements was reversed, with positive voltages used for SET and negative voltages used for RESET.

However, for the electroforming step and the initial 100 *I-V* sweeps, where the RF setups were not required, voltages were applied directly to the bottom electrode (BE)/AE using only the SMU. In this case, negative voltages were used for electroforming and SET operations, while positive voltages were applied for the RESET.

3.2. Sample Design and Fabrication

This section introduces a new sample design developed for high-frequency measurements, motivated by limitations of previously reported device implementations. In earlier designs, such as those presented by Moritz von Witzleben [70], the device layouts enabled high-frequency characterization but required complex fabrication procedures and exhibited limited compatibility with standard probing schemes, particularly with multi-probe wedge probe cards. To address these limitations, the new sample design focuses on simplified fabrication and improved compatibility with both the RF measurement setup and the 4-probe wedge probe card. Additionally, the CPW structure implemented in these devices is described in detail.

3.2.1. Sample Design

As the focus of this thesis primarily lies on measurement techniques, the fabrication processes are briefly described in this section. The photolithographic mask design was initially developed by Moritz von Witzleben and later modified by Pascal Stasner and the author. The final layout comprises three distinct device geometries: crossbar-shaped, standard-shaped, and U-shaped configurations. Among these, the crossbar and standard devices are structurally similar, differing only in their electrode overlap area, as illustrated in Figure 3.5(a) and 3.5(b). In contrast, the U-shaped device differs primarily in the configuration of its outer conductor (OC), which adopts a U-shape (as shown in Figure 3.5(c)).

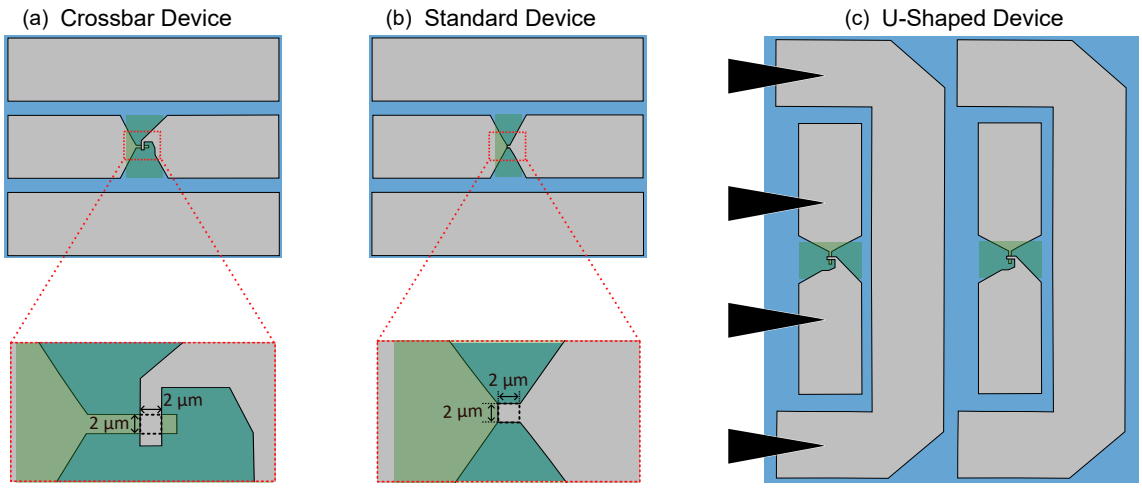


Figure 3.5: Design of three device geometries on a single mask: (a) crossbar-shaped device, (b) standard-shaped device, and (c) U-shaped device. All devices feature a $2 \times 2\,\mu m^2$ electrode overlap, with differences arising only from the mask layout, while the fabrication process remains identical. The U-shaped device was designed specifically to accommodate measurements using the 4-probe wedge probe card. Insets show zoomed-in views of the electrode overlap region for the crossbar and standard devices (the U-shaped device exhibits the same overlap geometry as the crossbar device).

The inner conductor (IC), however, retains a structure analogous to that of the crossbar device. The U-shaped device was specifically designed to ensure compatibility with the 4-probe wedge probe card.

To optimize high-frequency performance and reduce parasitic capacitance, the overall CPW structure length was decreased in comparison to earlier designs [70]. For the crossbar and standard shapes, the length was reduced to 230 µm, down from 590 µm, as shown in Figure 3.6(a). The length for the U-shaped layout, on the other hand, was reduced to 560 µm. Moreover, the spacing between the IC and OCs was decreased from 60 µm to 20 µm, and the conductor width was narrowed from 100 µm to 80 µm, as illustrated in Figure 3.6(a).

3.2.2. Device Fabrication

The fabrication of the devices was carried out on a fused silica substrate, which had been coated with a 10 nm titanium oxide (TiO_x) adhesion layer. The film deposition process was conducted using RF magnetron sputtering, by methods reported in previous studies [147, 148]. The BE comprises a 30 nm Pt layer, which functions as the AE for the resistive switching device. In addition to the BE, a 5 nm TaO_x layer was sputter-deposited to act as the active switching material. The TE consists of a 20 nm Ta layer that establishes an ohmic contact and is in-situ passivated with a 30 nm Pt layer to prevent oxidation. The OC of the CPW structure is fabricated using the same material stack as the TE. The IC is 80 µm wide and spaced 20 µm from the OC. As the tapered structure approaches the ReRAM cell, it narrows down to an overlap area of $2 \times 2\,\mu m^2$ at the point where the top and bottom electrodes intersect. Although the mask design includes devices with

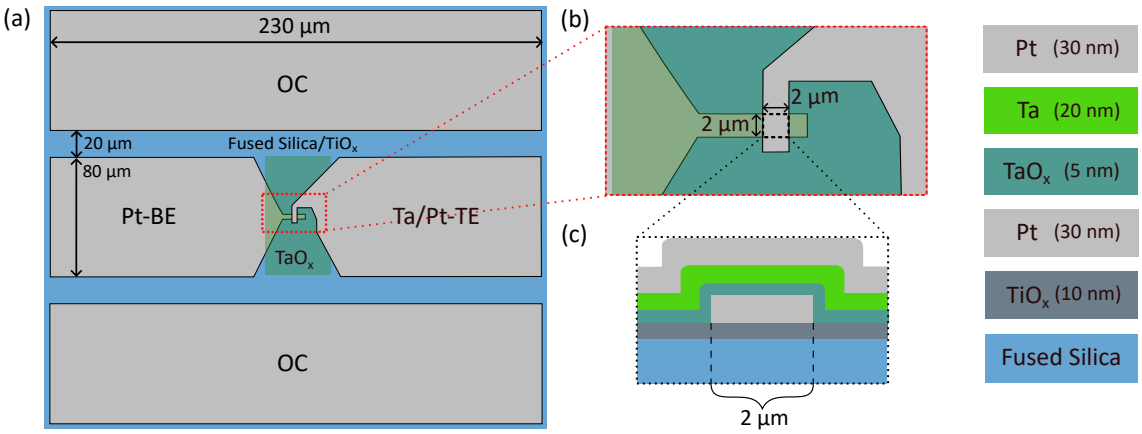


Figure 3.6: (a) Top view of the TaO_x CPW structure, including the outer conductor (OC). (b) Zoom-in on the TaO_x crossbar layout, highlighting the $2 \times 2\,\mu m^2$ electrode overlap. (c) Cross-sectional illustration of the TaO_x device layer showing the VCM stack. The device is fabricated on an insulating fused silica substrate, which minimizes parasitic capacitance, and is coated with a full-surface TiO_x adhesion layer. Adapted from Munir *et al.* [146] under CC BY 4.0.

various electrode overlap areas ($3 \times 3\,\mu m^2$, $5 \times 5\,\mu m^2$, and $10 \times 10\,\mu m^2$), this work focuses primarily on devices with a $2 \times 2\,\mu m^2$ overlap. All patterning steps were carried out using optical lithography in combination with a lift-off process.

3.3. Characterization

A comprehensive understanding of how devices behave under various electrical conditions is essential for evaluating their performance and reliability. This section describes the methodologies used to characterize the fabricated TaO_x-based VCM devices, focusing on their forming behavior, *I-V* characteristics, and high-frequency response. The electroforming process is described first, along with the criteria used to ensure stable and repeatable switching behavior. During forming, a 10 kΩ series resistor was used to limit the forming current. To minimize parasitic capacitance between the current-limiting resistor and the DUT, the resistor was placed as close as possible to the DUT in the electrical signal path. The high-frequency properties of the devices were then investigated using scattering parameter (S-parameter) measurements and a vector network analyzer (VNA). These measurements enabled the precise reconstruction of the voltage waveform at the DUT, allowing the accurate extraction of key parameters such as rise time and electrical charging time.

3.3.1. Electroforming and *I-V* Characteristics

Initially, the TaO_x devices were electroformed and 100 *I-V* sweeps (SET and RESET sweeps) were conducted to ensure sufficient device endurance and achieve a stable (more), reproducible behavior. The forming and *I-V* sweep settings are detailed in Table 3.2.

The devices were formed using a measurement configuration that included a 10 kΩ series resistance placed close to the probe needle, as illustrated in Figure 3.7. This configuration was chosen to minimize parasitic capacitance between the current-limiting resistor and the DUT, thereby significantly reducing current overshoot during the forming process. Earlier electroforming experiments employed a 100 kΩ external series resistance inserted between two coaxial cables, each approximately 0.6 m in length, connecting the SMU to the DUT. This setup introduced significant parasitic capacitance, resulting in substantial current overshoot, particularly evident during the first RESET operation

Table 3.2: Device operations under different voltage sweep conditions

Operation	**Voltage**	**Sweep rate**	**Current Compliance (CC)**
Forming	-3.5 V to -4.0 V	0.5 V/s	10 µA
SET	-1.0 V to -1.4 V	0.5 V/s	300 µA
RESET	1.4 V to 1.8 V	0.5 V/s	-

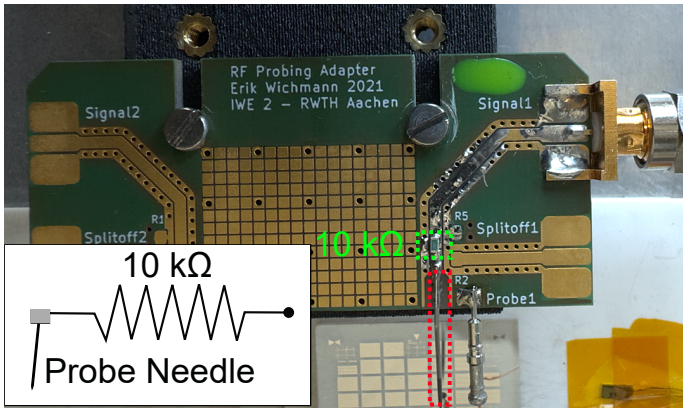


Figure 3.7: A 10 kΩ series resistance (highlighted in green) placed on a printed circuit board (PCB) close to the probe needle (highlighted in red). This placement reduces the electrical path length between the current-limiting resistor and the device under test, thereby minimizing parasitic capacitance during electroforming.

following electroforming. The observed behavior can be understood within established filamentary switching models for bipolar ReRAM devices [149]. During electroforming, a thick and highly conductive filament is created, such that the RESET current required to thermally destabilize and rupture the filament is of the same order of magnitude as the forming or SET current. Under these conditions, transient currents arising from the discharge of parasitic capacitances can substantially increase the instantaneous RESET

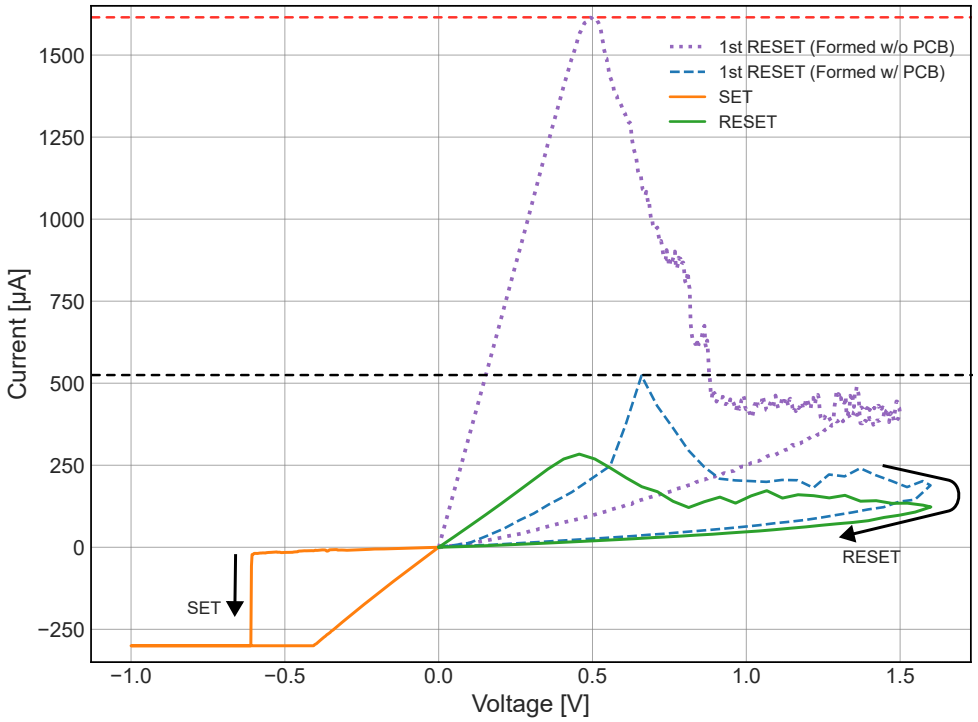


Figure 3.8: *I-V* characteristics of TaO_x devices. The purple dotted curve shows the first RESET after forming without using a PCB, while the blue dashed curve shows the first RESET on a device that was formed with a PCB. The orange and green curves represent typical SET and RESET operations. The settings of the sweeps are listed in the Table 3.2.

current, leading to pronounced overshoot effects. In subsequent switching cycles, the conductive path is re-established under controlled SET current compliance, resulting in thinner filaments and reduced RESET currents. As shown in Figure 3.8, the purple dotted RESET curve indicates a maximum current overshoot of approximately 1.6 mA for devices formed with the external series resistance inserted between the coaxial cables rather than placed close to the probe needle.

In contrast, placing the series resistance close to the DUT (as shown in Figure 3.7) significantly reduced the parasitic capacitance, resulting in a substantially lower overshoot current. The blue dashed RESET curve in Figure 3.8 illustrates this improvement, showing a reduced maximum overshoot current of approximately 600 µA. These results demonstrate that minimizing the electrical path length between the current-limiting resistor and the DUT enables more controlled and stable electroforming behavior.

The *I-V* sweep of the TaO_x device is presented in Figure 3.8, with the SET and RESET transitions highlighted in orange and green, respectively. The *I-V* characteristics exhibit typical VCM behavior, featuring a nonlinear HRS and a linear LRS. The HRS values range from approximately 8 kΩ to 30 kΩ, while the LRS ranges from around 500 Ω to 3.5 kΩ.

3.3.2. Scattering Parameters Measurements

Scattering parameter (S-parameter) measurements are a crucial technique for characterizing the high-frequency behavior of DUTs. These measurements are conducted using a VNA, which applies signals across a range of frequencies to the DUT and subsequently measures the reflected and transmitted signals. Further details on VNA functionality can be found in [142]. For this thesis, S-parameters were specifically utilized to determine the electrical charging times of the investigated TaO_x devices.

The VNA employed for these measurements was an HP 8722ES, operating within a frequency range of 50 MHz to 40 GHz, as indicated by the purple marker "9" in Figure 3.1. Prior to device characterization, the VNA must be calibrated to ensure accurate S-parameter measurements. In this work, the Short-Open-Load-Through (SOLT) calibration method was employed. A detailed description of this procedure can be found in earlier work by von Witzleben [70].

Throughout all S-parameter measurements, the signal power was consistently set to -10 dBm. This power level corresponds to an input power of 0.1 mW, or a voltage amplitude of approximately 70 mV at a characteristic impedance of 50 Ω. As elaborated in Section 2.4.1, the voltage at the DUT effectively doubles $V_{DUT} = 2V_p$ due to impedance matching conditions. Given that the typical switching voltages for VCM devices are greater than 0.5 V, the devices were intentionally prevented from switching during the VNA measurements. To further ensure this and avoid potential leakage currents, all VCM devices were driven into their HRS before conducting the frequency-domain measurements.

The primary objective of performing these scattering measurements on the newly designed devices (referred to as "redesigned device") was to compare their high-frequency response with previously characterized reference devices (specifically, the Ta3 devices), detailed in von Witzleben's study [70]. While the older Ta3 devices, also with a $2 \times 2\,\mu m^2$ size, were known for their challenging fabrication process, the updated device structure, developed by von Witzleben, aimed to simplify fabrication while maintaining comparable electrical charging times.

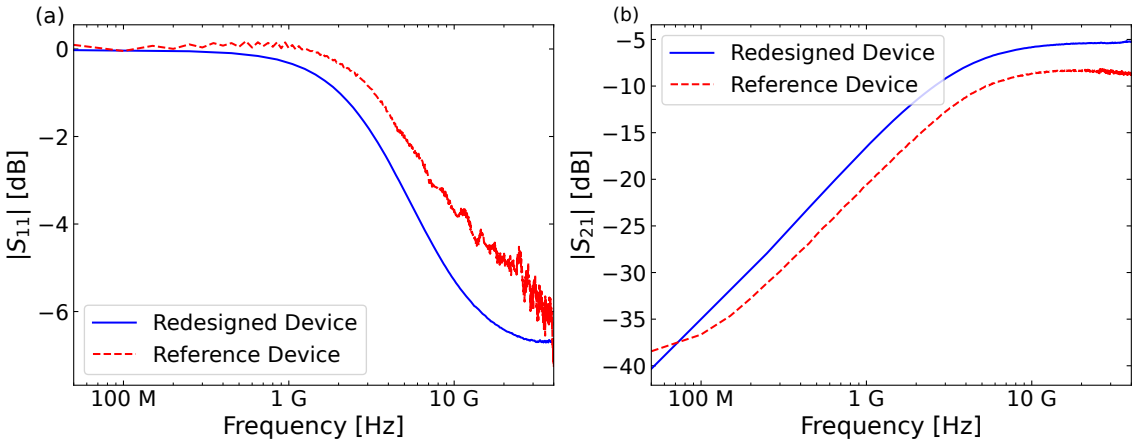


Figure 3.9: Magnitude of (a) forward reflection (S11) and (b) forward transmission (S21) for both the redesigned and reference device [70] structures. Measurements were performed using the HP 8722ES VNA. Partially adapted from [70].

Figure 3.9 presents the scattering parameters for both the new structure device and the reference device. The forward reflection (S_{11}) and forward transmission (S_{21}) characteristics of the new device are notably smoother and cleaner compared to those of the older device. Quantitatively, at 40 GHz, the S_{11} for the new device was measured at -6.67 dB, which is comparatively better than the -7.10 dB observed for the old device. In this context, a higher S_{11} value is desirable, as it indicates more signal reflection within the DUT. Conversely, the S_{21} for the new device was -5.26 dB, which is slightly higher than the -8.65 dB of the old device. A lower S_{21} value is generally preferred, as it signifies less signal transmission through the DUT. Despite these minor differences, these preliminary measurements confirmed that the high-frequency characteristics of the new device structure are indeed comparable to those of the reference device. More details on S-parameter measurements can be found in von Witzleben [70].

Effective Voltage at DUT

The voltage at the DUT, $V_{\mathrm{DUT}}(t)$, is the superposition of the incoming voltage pulse $v_1^+(t)$ and the reflected pulse $v_1^-(t)$ at port 1, minus the transmitted pulse $v_2^-(t)$ to the other electrode of the VCM device at port 2. This reduces the effective voltage drop over the device and needs to be considered. The method used for reconstructing $V_{\mathrm{DUT}}(t)$ is based on

the approach described in detail in [70]. The overall voltage at the device is consequently given by:

$$V_{\mathrm{DUT}}(t) = v_1^+(t) + v_1^-(t) - v_2^-(t) \tag{3.2}$$

The incoming voltage pulse $v_1^+(t)$ is measured using an oscilloscope. The reflected signal $v_1^-(t)$ and the transmitted signal $v_2^-(t)$ are calculated using the frequency-domain scattering parameters of the device.

To obtain the reflected signal, the discrete Fourier transform of $v_1^+(t)$ is first computed:

$$V_1^+(f) = F(v_1^+(t)) \tag{3.3}$$

This frequency-domain representation is then multiplied by the forward reflection parameter $S_{11}(f)$:

$$V_1^-(f) = V_1^+(f) \cdot S_{11}(f) \tag{3.4}$$

Applying the inverse Fourier transform yields the reflected signal in the time domain:

$$v_1^-(t) = F^{-1}(V_1^-(f)) = F^{-1}(V_1^+(f) \cdot S_{11}(f)) \tag{3.5}$$

The transmitted signal $v_2^-(t)$ is calculated in the same way, using the forward transmission parameter $S_{21}(f)$:

$$V_2^-(f) = V_1^+(f) \cdot S_{21}(f) \tag{3.6}$$

$$v_2^-(t) = F^{-1}(V_2^-(f)) = F^{-1}(V_1^+(f) \cdot S_{21}(f)) \tag{3.7}$$

The voltage at the device, $V_{\mathrm{DUT}}(t)$, is finally calculated using Equation 3.2 and is shown as the red curve in Figure 3.10. The amplitude is almost twice as high as the incoming signal $v_1^+(t)$, which makes sense because most of the signal is reflected. However, $V_{\mathrm{DUT}}(t)$ takes some time to reach its peak. This delay represents the device charging time, as discussed in the following section.

Electrical Charging Time

The forward reflection (S_{11}) and forward transmission (S_{21}) parameters (which were previously derived as shown in Figure 3.9) are essential for determining the electrical charging times of the devices. Several metrics exist for quantifying electrical charging time, including the time constant τ_{RC}, the rise time t_{80} (20% to 80%), and the rise time t_{90} (10% to 90%). Among these, t_{90} was selected as the most appropriate measure for this

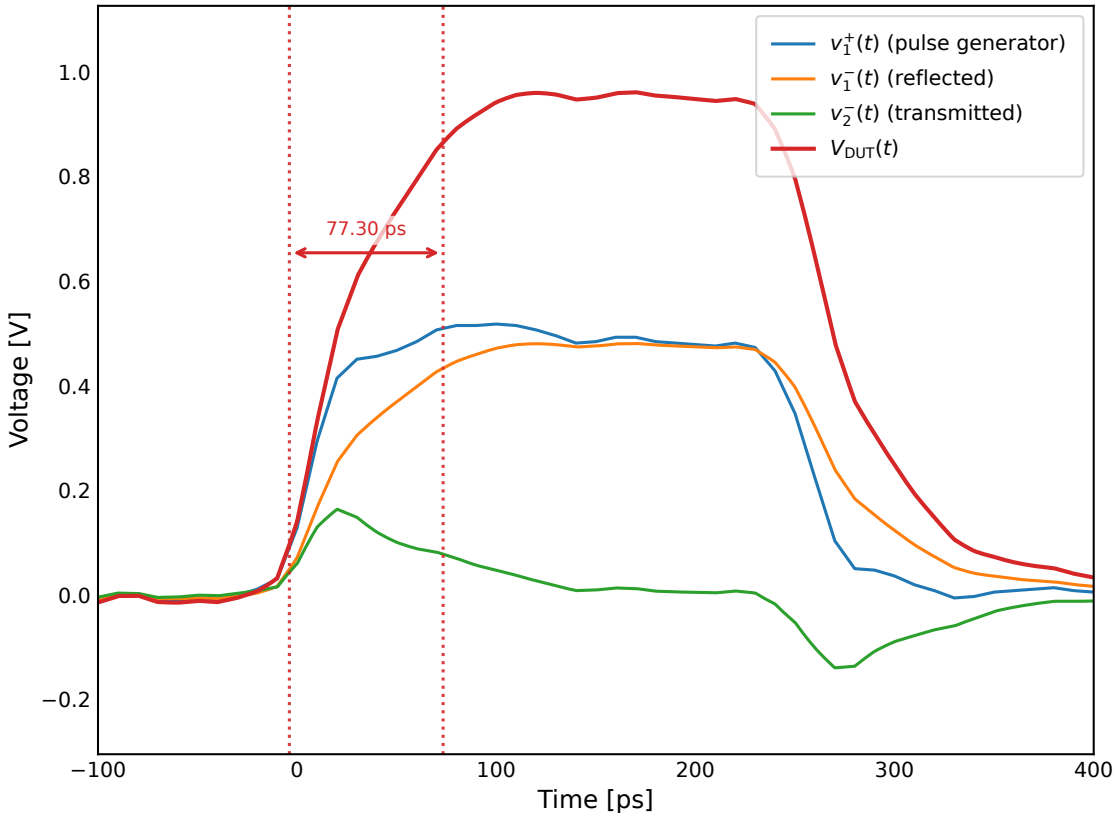


Figure 3.10: The voltage at the device, $V_{\mathrm{DUT}}(t)$, derived using Equation 3.2 for the redesigned device. The red vertical dotted lines indicate the rise time (10%–90%) of the device. The plot also shows the incoming pulse $v_1^+(t)$, the reflected signal $v_1^-(t)$, and the transmitted signal $v_2^-(t)$.

study. The t_{90} metric is defined as the time required for the voltage to rise from 10% to 90% of its maximum value. The t_{90} rise time measure has been consistently used in [70] for characterizing similar devices. This particular metric is favored because other measures, such as τ_{RC} and t_{80} are shorter and therefore yield significantly shorter electrical charging time, whereas t_{90} provides a more comprehensive representation of the actual charging behavior. The differences are explained in more detail by von Witzleben [70]. Therefore, to ensure comparability between the redesigned device and the reference devices, t_{90} rise time is also adopted as the primary measure in this study.

After determining $V_{\mathrm{DUT}}(t)$ using Equation 3.2 (as previously illustrated in Figure 3.10), the charging behavior of both the reference device and the redesigned device was compared by plotting their respective $V_{\mathrm{DUT}}(t)$ curves. To accurately measure the rise time, the devices needed to achieve a full charge during the pulse application. To minimize the influence of the pulse generator's own rise time on the device's rise time, a 250 ps pulse with an amplitude of 0.5 V was employed. This amplitude was selected as it represented the highest voltage at which the devices would not switch. This pulse, generated by the PG5 pulse generator, was applied as $v_1^+(t)$ to devices with rise times faster than 250 ps.

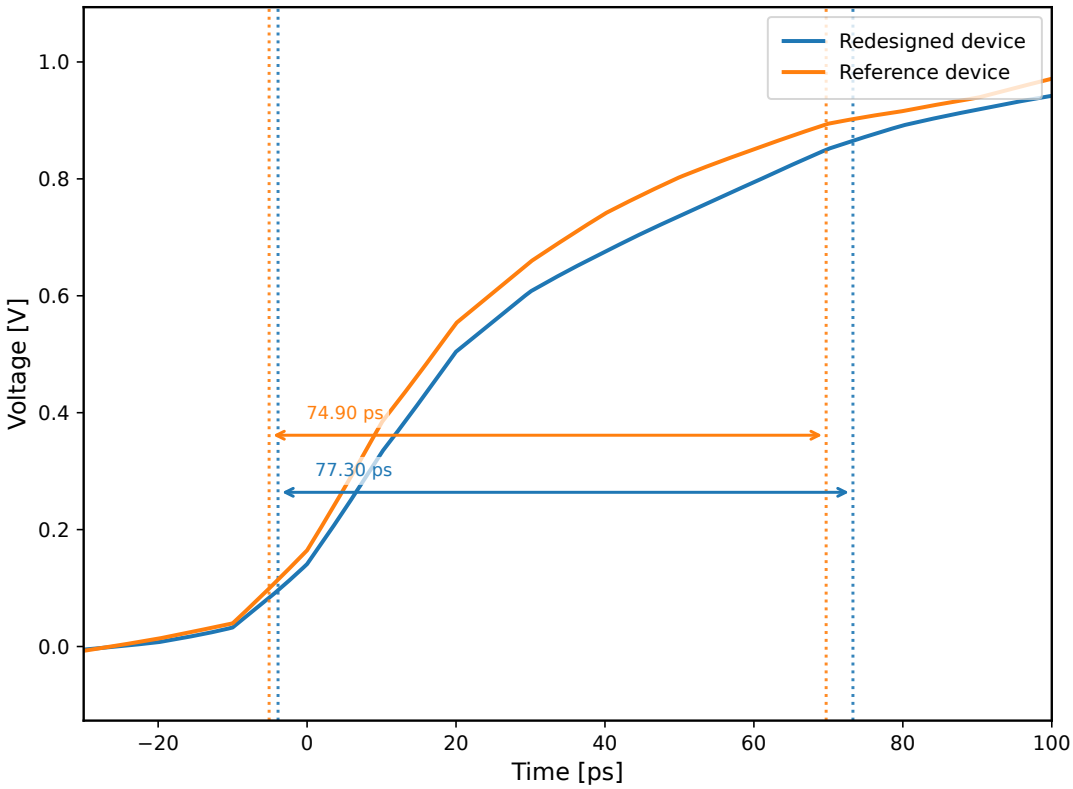


Figure 3.11: A zoomed-in view of the initial voltage response, $V_{\mathrm{DUT}}(t)$, for the reference and redesigned device, derived from Equation 3.2. The vertical dotted line indicates the rise time (10% - 90%), for both devices.

The resulting $V_{\mathrm{DUT}}(t)$ curves and corresponding rise times for both devices are presented in Figure 3.11. The reference device exhibited a rise time of 74.9 ps, whereas the redesigned device had a rise time of 77.3 ps. However, this comparison is not fully accurate because the rise time of the input pulse has not yet been taken into account. The actual rise time of the device, T_{rise}, can be determined using:

$$T_{\mathrm{rise}} = \sqrt{T_{\mathrm{calc}}^2 - T_{\mathrm{PG}}^2} \tag{3.8}$$

where T_{calc} is the calculated rise time of the device (as shown in Figure 3.11), and T_{PG} is the rise time of the PG5 pulse generator, which amounts to 34.5 ps. Using Equation 3.8, the rise time amounts to 66.5 ps for the reference device and 69.2 ps for the redesigned device. These results show that the rise times of both devices are comparable. However, the redesigned device has the advantage of easier fabrication compared to the reference device. Furthermore, it is important to distinguish between the intrinsic switching speed of the device and the electrical charging time required to charge the device. The electrical charging time determines how rapidly the voltage is applied across the device. However, these devices are capable of switching within the electrical charging time, with reported switching times as short as 20 ps [6, 17]. This demonstrates that the switching process can occur during the charging phase. Improving the device rise time can therefore further

enhance the accessible switching speed.

3.4. Further Device Optimization

An initial investigation into the electrical behavior and S-parameter characteristics of the redesigned TaO_x devices reveals that their charging times are comparable to those of the reference devices characterized by von Witzleben [70]. This conclusion is based on a preliminary evaluation of a limited number of devices per geometry. This indicates promising potential for neuromorphic computing applications, where fast and efficient switching at sub-ns timescales is desirable.

One key advantage of the redesigned devices is their easy fabrication, which helps address some of the challenges seen in reference devices. However, further improvements are still needed to reach their full potential. Future work should systematically characterize the capacitive contributions from both the VCM stack and the CPW structure through detailed S-parameter and rise time measurements, following the methodology described by von Witzleben [70].

Several optimization strategies that were previously explored [70] remain highly relevant to the development of these redesigned devices:

- **Electrode thickness:** Thicker electrodes are known to increase the CPW bandwidth [76]. Existing devices use Pt conductors with a thickness of just 30 nm, far below the skin depth of Pt at 40 GHz, which is approximately 816 nm as calculated in Section 2.4. While attempts to use thicker electrodes in [70] resulted in short circuits at device edges, alternative fabrication strategies such as chemical-mechanical polishing may help realize a planar electrode configuration that mitigates edge effects.

- **Lateral architectures:** Reducing the influence of the VCM stack by implementing lateral device designs could decrease overall capacitance and improve charging behavior [70]. While lateral VCM configurations are challenging to implement, similar approaches are more common in PCM technologies [150]. Nevertheless, the trade-off between residual angular capacitance and usable CPW bandwidth must be carefully considered.

In addition to structural optimization, material engineering of the switching layer can significantly improve device scalability. While sputter-deposited TaO_x was employed for the devices in this study, recent findings by Stasner *et al.* [151] indicate that thermally oxidized TaO_x offers improved performance characteristics. This approach facilitates bottom-up growth, resulting in better interface quality and enabling finer control over stoichiometry via tunable oxidation time and temperature. Notably, devices utilizing

thermally oxidized TaO_x exhibit lower leakage currents, more stable pristine resistances, and reduced forming voltages, which are essential factors for scalable and energy-efficient ReRAM integration.

Moreover, the consistency provided by thermal oxidation across different fabrication systems enhances reproducibility, making this method more suitable for backend of line (BEOL) compatibility and nano-scaled ReRAM technologies. These characteristics suggest that thermally oxidized TaO_x could be a promising option for future memristive device development, particularly for neuromorphic and high-frequency applications.

3.5. Conclusion

This chapter described the experimental setup and characterization methods used to investigate high-frequency switching in TaO_x-based VCM devices. Two RF measurement setups were described: RF setup 1, originally developed by von Witzleben, and RF setup 2, an enhanced configuration developed during this work. The primary improvements in RF setup 2 include the integration of an RF switch box to enable automated signal routing and minimize leakage currents, and the incorporation of an AWG providing flexible control over pulse parameters. These enhancements extend the measurement capabilities beyond VCM devices to other resistive switching technologies, such as PCM and ECM devices, which often operate in highly resistive states.

The redesigned devices were developed with the primary aim of enabling easier fabrication while maintaining compatibility with both RF probing and standard 4-probe wedge probe card measurements. Three geometries were implemented on the mask, including crossbar, standard, and U-shaped configurations. The U-shaped geometry was specifically designed for compatibility with 4-probe wedge probe cards. Compared to previous designs, the CPW structure was significantly shortened, and the spacing between conductors was reduced.

Furthermore, the electrical characterization of the redesigned devices was investigated using electroforming, *I-V* characteristics, and scattering parameter measurements. Placing a series resistance close to the DUT during forming reduced current overshoot and resulted in more stable switching behavior. The high-frequency response was evaluated using S-parameter measurements with a VNA, which allowed the effective voltage at the DUT to be reconstructed and the electrical charging time to be determined. Based on the S-parameter analysis, the redesigned devices exhibited high-frequency characteristics comparable to those of the reference devices, while offering the advantage of a simpler fabrication process.

4. VCM Switching with Short Pulses and Long Delays

Filamentary VCM devices are promising candidates for neuromorphic applications due to their ability to modulate conductance over a wide range [42, 98]. For synaptic applications, however, the key requirement is not simply accessing multiple conductance states, but achieving gradual and linear conductance changes during repeated SET operations [119, 120]. The SET transition in filamentary VCM devices is typically abrupt, which makes it difficult to achieve gradual and linear potentiation. This abrupt behavior is commonly attributed to positive electro-thermal feedback, where the increase in current during SET leads to local Joule heating that accelerates filament growth and results in sudden conductance changes [16, 20].

Previous studies have shown that the switching dynamics can be influenced by the temporal characteristics of the applied pulses. Hardtdegen *et al.* [10] and Cüppers *et al.* [7] demonstrated that gradual SET behavior depends on the initial LCS and can be achieved when positive feedback between current increase and Joule heating is suppressed by using SET pulses shorter than the transition time. These works suggest that operating on timescales comparable to or shorter than the thermal time constant of the conductive filament can be used to achieve more gradual and linear switching behavior.

However, these studies were limited to relatively long pulse regimes, with pulse widths down to 100 ns, and typically reported only a limited number of pulses in the linear region. It therefore remains unclear how the switching behavior evolves when operating at much shorter timescales, where electro-thermal feedback is expected to be further reduced. This raises the question of whether linear potentiation in filamentary VCM devices can be achieved by operating with very short SET pulses, shorter than the thermal time constant of the conductive filament.

To address this question, an RF-based measurement setup (RF Setup 1, as described in Section 3.1.1) is used to apply trains of short SET pulses to Pt/TaO_x/Ta/Pt filamentary VCM devices. The use of an RF setup enables reliable generation and delivery of pulses in the sub-ns regime. The pulse width and pulse amplitude are systematically varied, and the conductance is measured after each pulse using a DC read voltage. This approach allows the conductance evolution to be analyzed pulse by pulse and enables the determination of

operating conditions under which gradual and linear potentiation may occur. The results presented in this chapter are based on Munir *et al.* [146].

4.1. Experimental Methodology

The experimental setup used in this study corresponds to RF Setup 1, as described and shown in Figure 3.3 (Section 3.1.1). This configuration was selected because it incorporates a bias tee, which enables the simultaneous application of short pulses from the pulse generator and a DC signal from the SMU. For these measurements, the PG5 pulse generator was used instead of the PPG30, as the PPG30 was not yet fully integrated into the measurement setup at the time of the experiments.

The DUTs were TaO_x-based devices, illustrated in Figure 3.5 (Section 3.2). Most of the measurements were performed on crossbar-shaped devices. However, additional tests were also carried out on U-shaped and standard-shaped layouts to ensure broader applicability of the results. No significant differences in switching behavior were observed between the different geometries.

As described in Section 3.3.1, all devices were initially electroformed, followed by 100 *I-V* sweep cycles to improve endurance and ensure stable, reproducible behavior. The detailed forming and SET/RESET sweep conditions are summarized in Table 3.2. Both the electroforming and subsequent cycling were performed using a Keithley 2634B SMU, with voltages applied to the BE of the TaO_x devices.

4.1.1. SET Pulse Measurements

After electroforming and performing 100 *I-V* sweeps to stabilize the device behavior, SET pulse measurements were performed using a repeated measurement cycle. Each measurement cycle starts with a sequence of 10 SET/RESET *I-V* sweeps (shown as red triangles in Figure 4.1), which ends with a RESET operation and transitions the device into the LCS, thereby providing a well-defined initial condition.

After the initial 10 *I-V* sweeps in each cycle, a constant DC read voltage of 0.2 V was applied using the SMU with an integration time of nplc = 1. This read voltage was used to monitor the device conductance in parallel with the short pulses and remained active throughout the measurement, as shown by the green region in Figure 4.1.

While the read voltage was applied, a sequence of 200 short pulses was applied to the DUT using the PG5, as indicated by the orange rectangles in Figure 4.1. These pulses were evenly spaced, with a 1-second delay between consecutive pulses. This delay is much longer than the thermal time constant reported for TaO_x-based resistive switching devices and therefore avoids thermal accumulation between pulses. As shown by Schön *et al.*, thermal accumulation occurs only when the pulse spacing is comparable to the thermal

time constant, whereas for much longer delays, the device temperature relaxes back to the ambient level before the next pulse is applied [25].

To obtain statistically meaningful results, the SET pulse measurement cycle is repeated 200 to 300 times for each fixed pair of pulse width and pulse amplitude. Across different measurements, the pulse width and amplitude are systematically varied, spanning pulse widths from 50 ps to 100 ps and pulse amplitudes from 1.41 V to 2.23 V.

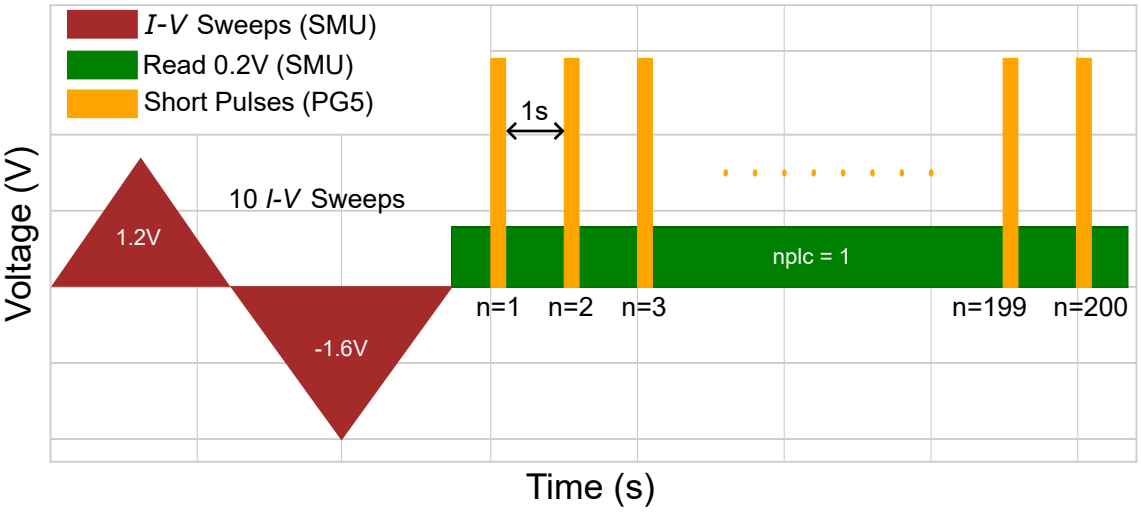


Figure 4.1: Schematic of the measurement cycle used for SET pulse experiments. At the beginning of each cycle, 10 SET/RESET *I-V* sweeps (indicated as red triangles) are performed, ending with a RESET operation that brings the device into the LCS. After that, a constant 0.2 V DC read voltage (indicated in green) is applied continuously throughout the cycle. Within this window, 200 short pulses (shown as orange rectangles) are applied by the pulse generator (PG5), with a 1-second delay between consecutive pulses, which is sufficient to allow the device temperature to relax to the ambient level and thereby avoid thermal accumulation. Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

It is important to note that the SET pulse measurements were conducted by applying pulses to the TE of the device. This configuration was selected because the PG5 outputs a fixed maximum voltage of 2.5 V, which is externally adjusted to the desired level using attenuators, as shown in Figure 3.3. As a result, the read voltage and *I-V* sweep signals had to be applied with reversed polarity during the pulse measurements to maintain consistency in device biasing; specifically, positive voltages were applied to the TE during SET operations, while negative voltages were applied during RESET operations. All SET pulse measurement cycles were performed after the initial electroforming step and the subsequent 100 *I-V* sweeps that were used to stabilize device behavior. Unless otherwise stated, all pulse amplitudes applied on the device in this chapter refer to the effective voltage $V_{\mathrm{P,eff}}$, as defined in Table 3.1.

4.1.2. Data Analysis

After conducting the SET pulse measurements, the device conductance (G_n) was evaluated following each application of n pulses, as illustrated in Figure 4.2. The timing of each pulse (marked by vertical orange lines) was used to define the intervals over which the conductance (G_n) was calculated. For example, the conductance G_1 is determined within the time window between the first and second pulse, which is highlighted in blue in Figure 4.2. Within each interval, the mean and sample standard deviation of the conductance values are computed to obtain both the conductance and its associated uncertainty, as shown in Figure 4.2. The analysis begins with $n = 0$, representing the initial LCS.

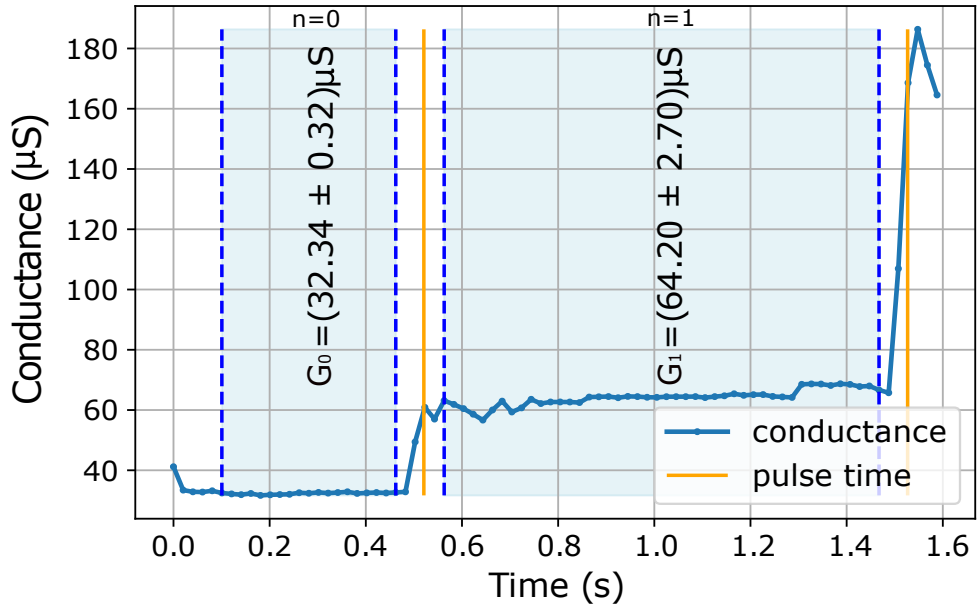


Figure 4.2: Illustration of the calculation of conductance after n pulses. The time intervals for calculating the conductance (G_n) and its uncertainty are highlighted in blue. The horizontal dashed blue line marks the left and right boundaries of these intervals. Using the recorded pulse times (horizontal orange lines) to set the boundaries, the mean and standard deviation of conductance are computed within these limits. Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

To further analyze the switching behavior, the extracted mean conductance values are plotted as a function of the number of applied pulses, as shown in Figure 4.3. This visualization reveals three distinct regions: the delay region, where conductance remains unchanged; the switching region, characterized by a typically linear increase in conductance; and the saturation region, where the conductance begins to level off. To identify and separate these regions, a piecewise fitting function is applied, which is defined as follows:

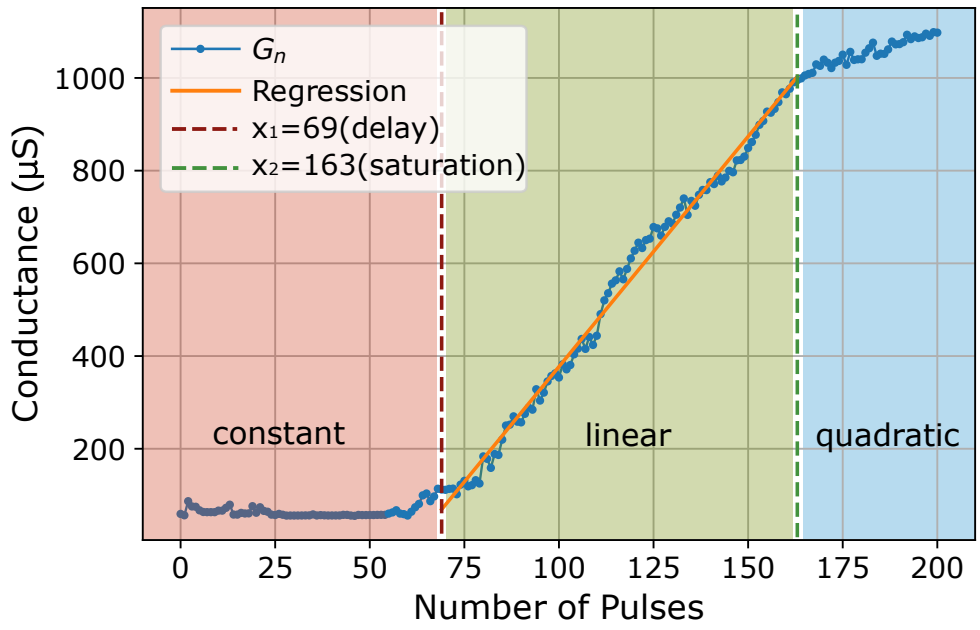


Figure 4.3: Extracted conductance G_n over up to 200 applied SET pulses with a pulse width of 50 ps and a pulse voltage of 1.77 V. The blue line with dots represents the measured conductance G_n, while the orange line depicts the regression fit. This plot is used to identify and characterize the delay, switching, and saturation regions, which are modeled by constant (red), linear (green), and quadratic (blue) functions, respectively. The points x_1 and x_2 indicate the boundaries between these regions. Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

$$\text{fit}(x) = \begin{cases} a & \text{if } x < x_1, \\ \left(\frac{b-a}{x_2-x_1}\right)x + a - \left(\frac{b-a}{x_2-x_1}\right)x_1 & \text{if } x_1 \leq x < x_2, \\ dx^2 + cx + b - cx_2 - dx_2^2 & \text{if } x \geq x_2 \end{cases}$$

In Figure 4.3, the red region represents the constant delay phase, the green region corresponds to the linear switching phase, and the blue region models the quadratic saturation behavior. The parameters a through d are fitting coefficients, while x_1 and x_2 denote the breakpoints separating the different regions. The significance of each parameter within the fitting model is outlined as follows:

- a: conductance of the delay region
- x_1: end of the delay region
- b: conductance at the end of the switching region
- x_2: beginning of the saturation region
- c: linear coefficient in the saturation region
- d: quadratic coefficient in the saturation region

Once the regions are identified, the analysis focuses on the switching region. Although the conductance change generally follows a linear trend, it exhibits some stochastic variation. To assess the linearity more precisely, a cutoff pulse n_{cutoff} (corresponding to x_2) is selected, and linear regression is performed on the conductance values $\{G_n | n_{\text{delay}} \leq n \leq n_{\text{cutoff}}\}$. The predicted conductance values from the regression are denoted by $\hat{G}_n$, and the linearity is quantified using the coefficient of determination R^2, yielding a value R_n^2 for each pulse n. This linear regression approach and the computation of R^2 directly follow the methodology described in Section 2.7.

To define the linear regime, a threshold condition is applied. In this work, a criterion of $R^2 \geq 0.95$ is used. The number of pulses within the linear regime is then given by:

$$n_{\text{linear}} = \max\{n \mid R_n^2 \geq 0.95\} \tag{4.1}$$

4.2. Results & Discussion

This section presents the key findings from experimental investigations, focusing on the complex switching characteristics of TaO_x devices under sub-100 ps pulse application. The analysis first quantifies the number of pulses that facilitate a linear conductance change within the optimal regime. Subsequently, the pronounced dependencies of linearity on both pulse width and pulse amplitude are explored, demonstrating how these parameters can be precisely tuned to achieve desired switching behaviors. Furthermore, the inherent variability observed in the experimental data is thoroughly addressed, explaining its origins and implications for device reproducibility. Finally, the critical impact of the initial LCS on the device switching dynamics is examined, contrasting the findings with established literature to provide a comprehensive understanding of the observed phenomena.

4.2.1. Number of Pulses in Linear Regime

The experiments were conducted on several TaO_x devices to investigate how pulse parameters affect linearity. Here, linearity is characterized as the maximum number of pulses that induce conductance state transitions while maintaining a linear regression fit with an $R^2 \geq 95\,\%$. Notably, higher R^2 values correspond to better linearity. The optimal linearity was achieved using a pulse width of 50 ps and a voltage of 1.77 V, yielding 104 pulses in the linear regime with an $R^2 = 99.5\,\%$, as illustrated in Figure 4.4(a). However, if a marginally lower R^2 (98%) is acceptable, a linear transition spanning 175 pulses can be achieved with a pulse width of 60 ps and a voltage of 1.98 V, as depicted in Figure 4.4(b). This indicates that relaxing the R^2 requirement enables a larger number of pulses in the linear transition, whereas stricter R^2 criteria significantly limit the pulse count within the linear regime. Regardless of the R^2 threshold chosen, the number of pulses achieved in the linear regime

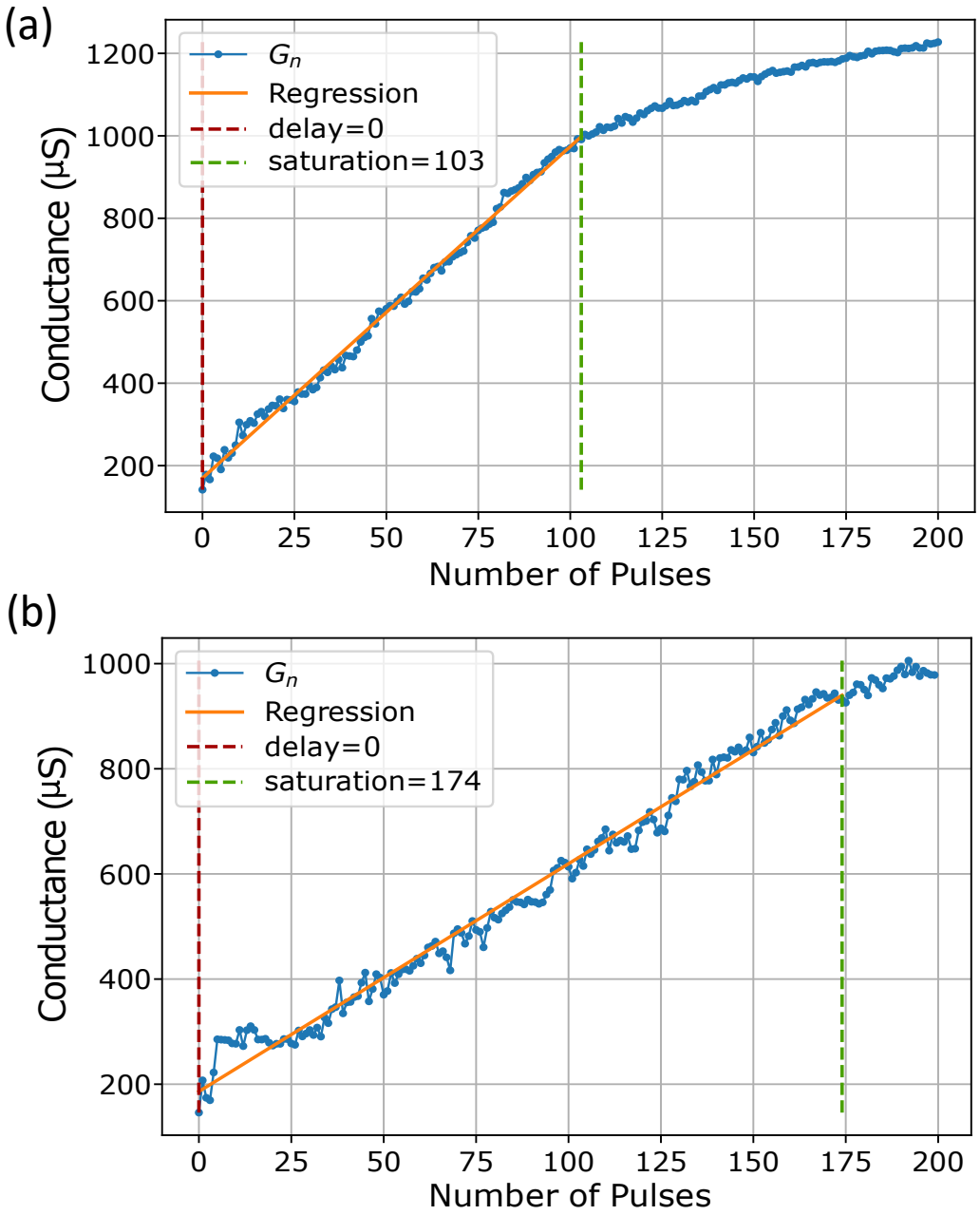


Figure 4.4: Gradual and linear switching characteristics observed in a TaO_x device. (a) Linear conductance modulation obtained with a 50 ps pulses at an applied voltage of 1.77 V. A total of 104 pulses were observed within the linear regime, with an R^2 value of 99.5 %. The conductance change commenced without initial delay. (b) Gradual conductance modulation with 60 ps pulses at 1.58 V. In this case, 175 pulses were sustained in the linear region with an R^2 value of 98 %. Although the overall switching remains highly linear, the R^2 value is slightly lower than in (a). Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

represents a significant increase compared to previous studies. Cüppers *et al.* [7] reported linear conductance evolution over approximately ten pulses when operating with SET pulses in the 100 ns regime. In contrast, using sub-100 ps pulses, which are shorter than the thermal time constant, allows a substantially larger number of pulses to be achieved within the linear regime. Additional raw data examples, including cases with pulse widths of 70 ps and 100 ps, are provided in Appendix A.

4.2.2. Pulse Width and Voltage Dependencies

This subsection systematically analyzes how pulse width and pulse amplitude influence the observed linear transition in the number of pulses. Heatmaps are employed for clear visualization of these dependencies, as presented in Figure 4.5(a) and Figure 4.5(b). The median number of pulses in the linear region is displayed in Figure 4.5(a), providing a robust measure of typical device performance under specific pulse conditions. The maximum number of pulses achieved in the linear regime for various R^2 values is illustrated in Figure 4.5(b), highlighting the full potential and range of linearity.

As shown in Figure 4.5(a), a distinct pulse width dependency is observed across the entire range of applied voltages. The column corresponding to 1.77 V provides the most illustrative example of this trend. At the shortest pulse width investigated (50 ps), the median number of pulses within the linear region reaches a maximum of 50, the highest value observed across all tested pulse widths. This higher median for shorter pulse widths can be attributed to the effective mitigation of Joule heating and its associated positive electro-thermal feedback. When the applied pulses are shorter than the thermal time constant of the conductive filament, the rapid current increase does not lead to an instantaneous temperature rise that would otherwise drive abrupt and uncontrollable filament overgrowth. As the pulse width increases, the median number of pulses decreases consistently, indicating that longer pulses are less effective in promoting a stable and linear transition of conductance states. This reflects the increased influence of thermal effects at longer timescales, leading to more abrupt switching.

Concurrently, pronounced dependencies on pulse voltage are also observed, with the device linearity changing significantly with varying amplitudes. The row corresponding to a pulse width of 60 ps serves as a useful reference to demonstrate how linearity is influenced by pulse amplitude. At a voltage of 1.41 V within this pulse width, the median number of pulses is relatively high. However, as the pulse amplitude increases, this median value decreases noticeably. An additional case with a 50 ps pulse width is considered to investigate these pulse voltage dependencies. Here, optimal performance is achieved at a benchmark voltage of 1.77 V, where the median number of pulses is the highest. At voltages below 1.77 V, fewer pulses are observed within the linear regime, primarily because these lower voltages are often insufficient to reliably switch the device, leading to significant non-

switching events and consequently lower median values. Conversely, at voltages exceeding 1.77 V, the device exhibits rapid switching, which drastically reduces the number of pulses sustained within the linear region and often results in highly abrupt transitions. This phenomenon arises from the excessive driving force that promotes accelerated filament formation and overgrowth. Therefore, for any given pulse width, both voltages below

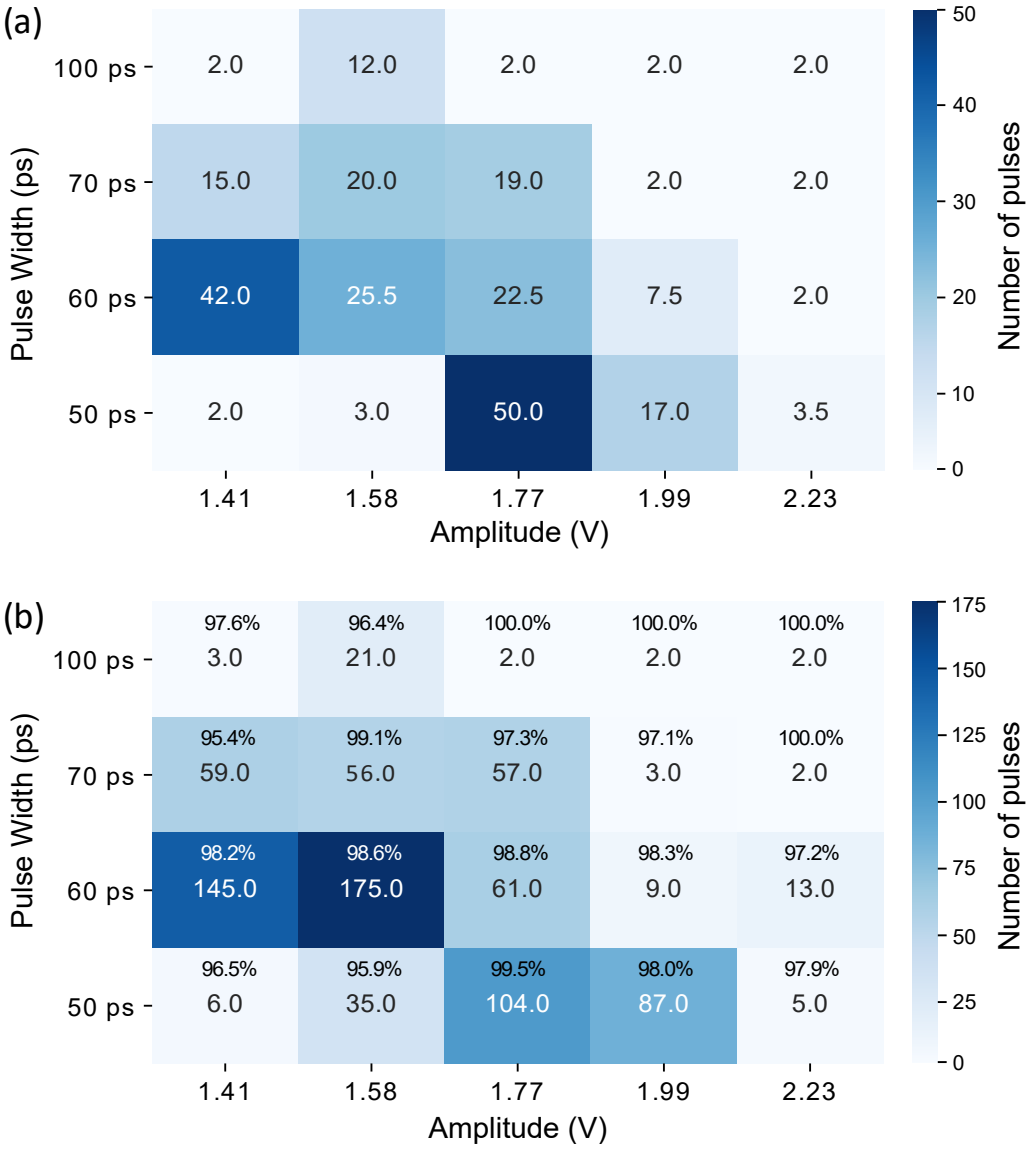


Figure 4.5: (a) Heatmap illustrating the median number of pulses sustained in the linear switching regime of the TaO_x device for $R^2 \geq 95\,\%$. The vertical axis corresponds to pulse width, the horizontal axis to applied voltage, and the color scale represents the number of pulses. The highest median number of pulses in the linear regime is observed at 1.77 V with a pulse width of 50 ps. (b) The plot shows the maximum number of pulses in the linear regime achieved for $R^2 \geq 95\,\%$. When a stricter linearity requirement is considered (higher R^2 value), the maximum number of pulses is reduced but remains above 100. For slightly lower R^2 values, a larger number of pulses can be sustained in the linear regime, as observed for 60 ps pulses at 1.58 V compared to 50 ps pulses at 1.77 V. Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

and above the optimal benchmark voltage (where the median value is maximal) result in reduced linearity. This indicates that achieving optimal linearity requires a careful balance of both pulse width and pulse amplitude. Despite these identified optimal conditions, the observed linearity consistently exhibits considerable variability, a critical aspect that is explored in Section 4.2.3.

Cycle-to-Cycle (C2C) Average Conductance

To further study the C2C variation observed in these potentiation schemes, this section focuses on the best-case and worst-case examples shown in Figure 4.6 and Figure 4.7, corresponding to pulse widths of 50 ps and 100 ps, respectively. Specifically, Figure 4.6(a) shows the conductance evolution during the first 20 pulses for 50 ps pulse width at different applied voltages. At a pulse amplitude of 1.77 V (highlighted by green boxes), a large number of pulses within the linear regime were observed, with up to 104 pulses recorded in a single measurement cycle. This desired gradual behavior is visible in the plot, demonstrating that the mean conductance increases gradually and linearly over these first 20 pulses, without an abrupt increase in conductance within this time interval. Conversely, at lower voltages (represented by blue and orange boxes), small conductance changes are observed. In these cases, the applied voltage is not sufficient, at this pulse width, to drive a noticeable transition from the LCS to the HCS.

In contrast, when subjected to higher voltages (depicted by red and purple boxes), the device conductance increases abruptly within the very first few pulses, quickly reaching the HCS, indicating a rapid switching capability inherent at these elevated voltage conditions.

Transitioning to longer pulse widths, Figure 4.6(b) presents the box plots for a 100 ps pulse width. Here, it is evident that the mean conductance increases abruptly, reaching the HCS across all applied voltages after a mere 2 to 4 pulses. This swift and rapid transition inherently leads to a significantly reduced number of pulses in the linear regime when compared to the performance observed at shorter pulse widths, such as 50 ps.

Further extending this analysis, Figure 4.7 illustrates the average conductance over an entire cycle of 200 pulses. In this visualization, line plots are used instead of box plots to provide a clearer and more continuous representation of the conductance evolution over time. This particular format facilitates a more insightful interpretation of the device behavior throughout the complete pulse sequence. Along with the mean conductance trend, the shaded regions around each curve represent the full range of conductance values observed across multiple measurement cycles, thereby providing insight into the C2C variability during repetitive pulsing.

As previously observed in the analysis presented in Figure 4.6, Figure 4.7 further demonstrates that the mean conductance at 50 ps and 1.77 V (represented by the green line plot) increases gradually and linearly over the entire 200-pulse sequence. In contrast, for a pulse width of 100 ps, the conductance swiftly reaches saturation, stabilizing at the

HCS within a limited number of pulses. These findings support the earlier conclusions, indicating that shorter pulse widths effectively enable a greater number of pulses to sustain within the linear regime. As discussed previously, this desirable behavior is likely attributed to the fundamental mechanism by which shorter pulses effectively limit Joule heating and the resultant positive electro-thermal feedback, both of which are known to drive abrupt switching phenomena in VCM devices.

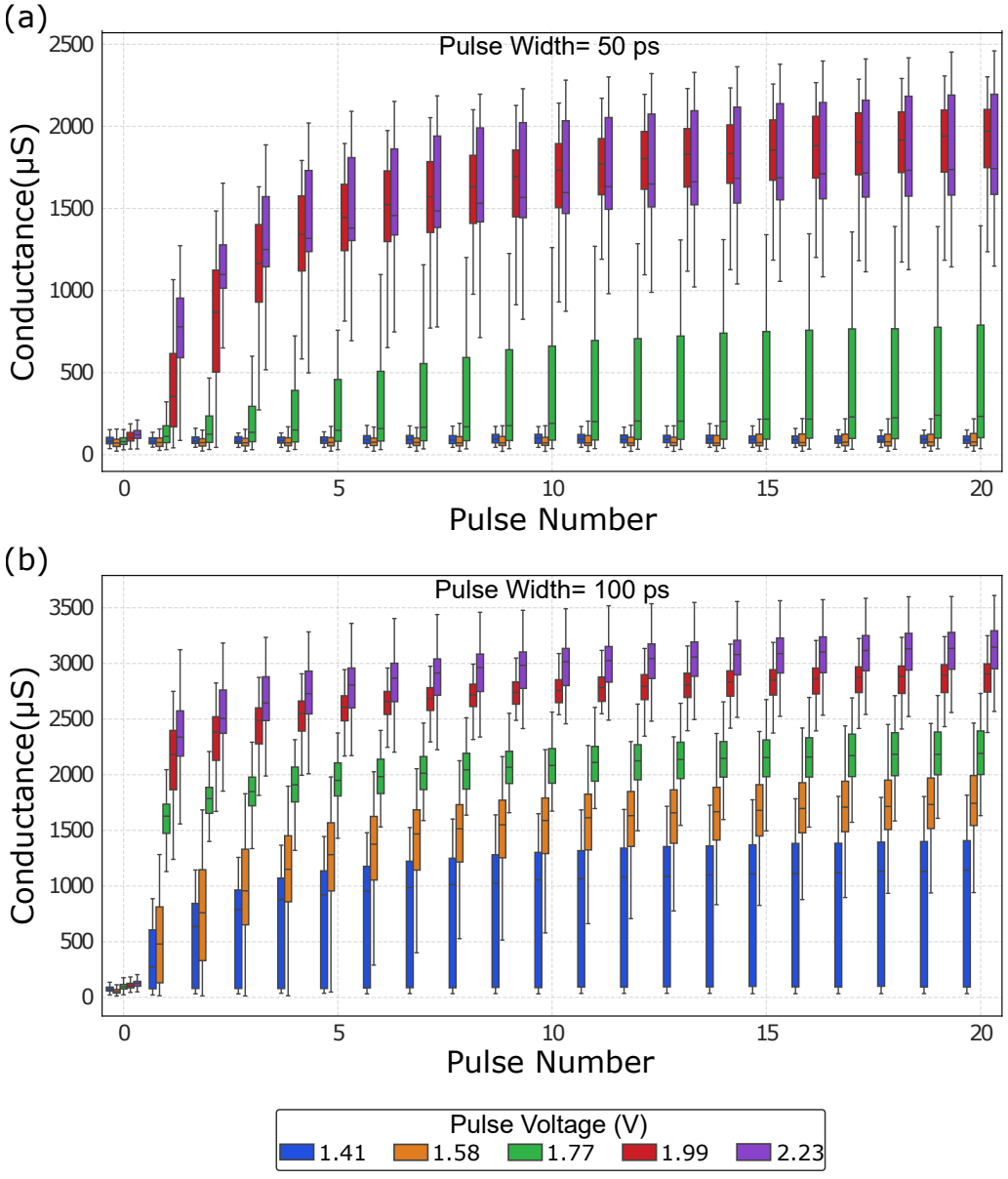


Figure 4.6: Box plots showing the evolution of device conductance during the first 20 SET pulses for two different pulse widths. (a) For 50 ps pulses at 1.77 V (green boxes), the mean conductance increases gradually and remains relatively low across the initial 20 pulses. (b) For 100 ps pulses, the mean conductance rises sharply within the first 2 to 4 pulses for all tested voltages, indicating that the devices rapidly transition to the HCS. Each box represents the distribution of conductance values obtained from multiple measurement cycles. Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

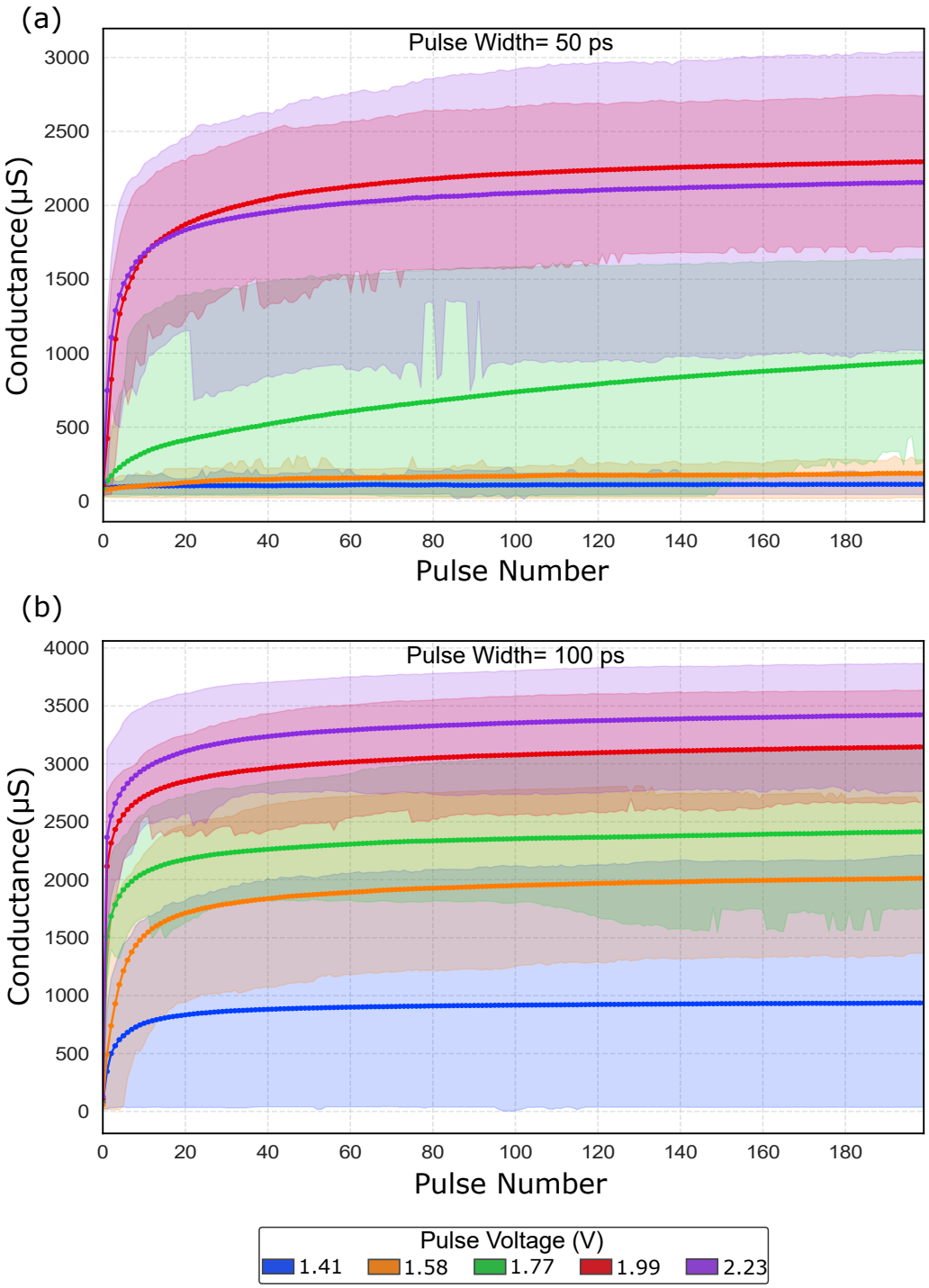


Figure 4.7: Average conductance evolution over a sequence of 200 pulses for pulse widths of (a) 50 ps and (b) 100 ps. Solid lines represent the mean conductance trends, with different colors corresponding to the applied pulse voltages for direct comparison. Shaded regions around each line indicate C2C variability, spanning the minimum to maximum values measured across multiple cycles. Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

The data presented in both the box plots in Figure 4.6 and the line plots in Figure 4.7 were generated using the complete set of measured data, including cycles in which no switching events occurred. No R^2-based filtering was applied to this dataset, ensuring that the plots provide a full and unbiased statistical representation of the average conductance observed across all measurement cycles. Additional plots for the 60 ps and 70 ps pulse widths are provided in the Appendix B for reference.

4.2.3. Variability

This study demonstrates that a gradual and linear conductance transition extending over 104 pulses can be achieved when using short pulses. However, despite this capability, the results also reveal that the inherent variability of the devices places a significant limitation on reproducibility. This limitation is illustrated in the box plots shown in Figure 4.8. These box plots, generated from the heatmaps (Figure 4.5), effectively illustrate the distribution of the experimental outcomes.

In Figure 4.8(a), the influence of pulse width on linearity and its associated variability is highlighted. For this case, a fixed pulse amplitude of 1.77 V was chosen to focus specifically on the effect of pulse width. The results show that, even at this optimal amplitude, the number of pulses sustained within the linear regime exhibits a considerable spread. This is evident from the wide interquartile ranges and extended whiskers in the box plots. These findings indicate that although shorter pulse widths are effective in achieving linearity, they are nevertheless accompanied by notable C2C inconsistencies. Furthermore, the occasional presence of outliers highlights deviations from the expected device behavior.

Similarly, Figure 4.8(b) demonstrates the influence of pulse voltage on linearity and the associated variability. For this analysis, a fixed pulse width of 60 ps was chosen to highlight the amplitude dependence. A significant degree of variability is observed across different pulse amplitudes. Specifically, lower amplitudes tend to show a broader spread in the data, indicating greater inconsistency in device response, even when these conditions are close to optimal. These findings collectively highlight the substantial challenges in consistently maintaining linearity and underscore the critical need for precise control over both the pulse width and pulse amplitude.

To gain a more in-depth understanding of this variability, the distribution of slope versus amplitude was also analyzed for various pulse conditions, as presented in Figure 4.9. In this context, the spread of these slope values serves as a direct indicator of variability: narrower distributions signify a stable and linear switching behavior, whereas wider distributions point to greater variability. Specifically, at a pulse amplitude of 1.77 V and a pulse width of 50 ps, narrower slope distributions are observed, as shown in Figure 4.9(a). This indicates a higher number of pulses achieved in the linear regime and, crucially, more consistent switching characteristics under these specific conditions. In contrast, other pulse voltages

resulted in the broader spread of slope values, directly reflecting increased variability in the device response. Similar trends were observed for the 60 ps pulse width, as depicted in Figure 4.9(b). At lower voltages (e.g., 1.43 V), the slope distribution is relatively narrow, suggesting better linearity. However, as the voltage increases, the spread of the slope values widens considerably, indicating a corresponding decrease in linearity due to the heightened

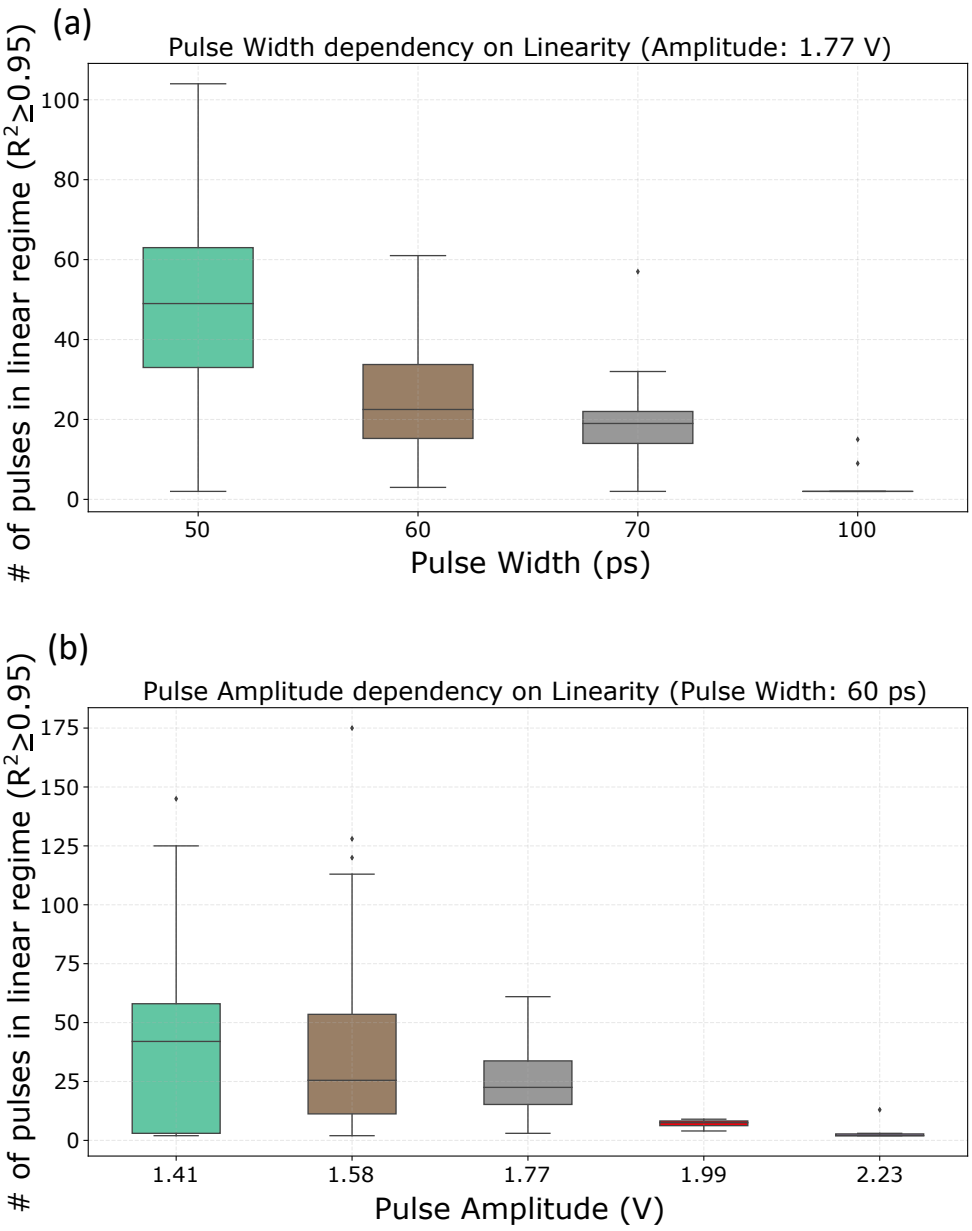


Figure 4.8: (a) Box plot illustrating the relationship between pulse width and the number of pulses sustained in the linear region at a fixed voltage of 1.77 V. The shortest pulse width of 50 ps yields the largest number of pulses, while the median gradually decreases as the pulse width increases. (b) Box plot showing the effect of pulse amplitude on the number of pulses in the linear region at a pulse width of 60 ps. Higher voltages lead to a reduction in the median number of pulses. The wide spread of the quartiles highlights substantial C2C variability, with each distribution constructed from approximately 300 measurements. Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

variability. The observed variability is primarily driven by C2C variability arising from the stochastic switching behavior of VCM devices [88, 118, 119].

Although preliminary measurements were also carried out on other devices showing similar gradual and linear behavior (as discussed in a later section), the detailed analysis focuses on a single device. This approach was chosen to ensure a statistically robust dataset. The current experimental setup had practical limitations, making it unfeasible to perform equally detailed studies on many devices due to the extensive measurement time required

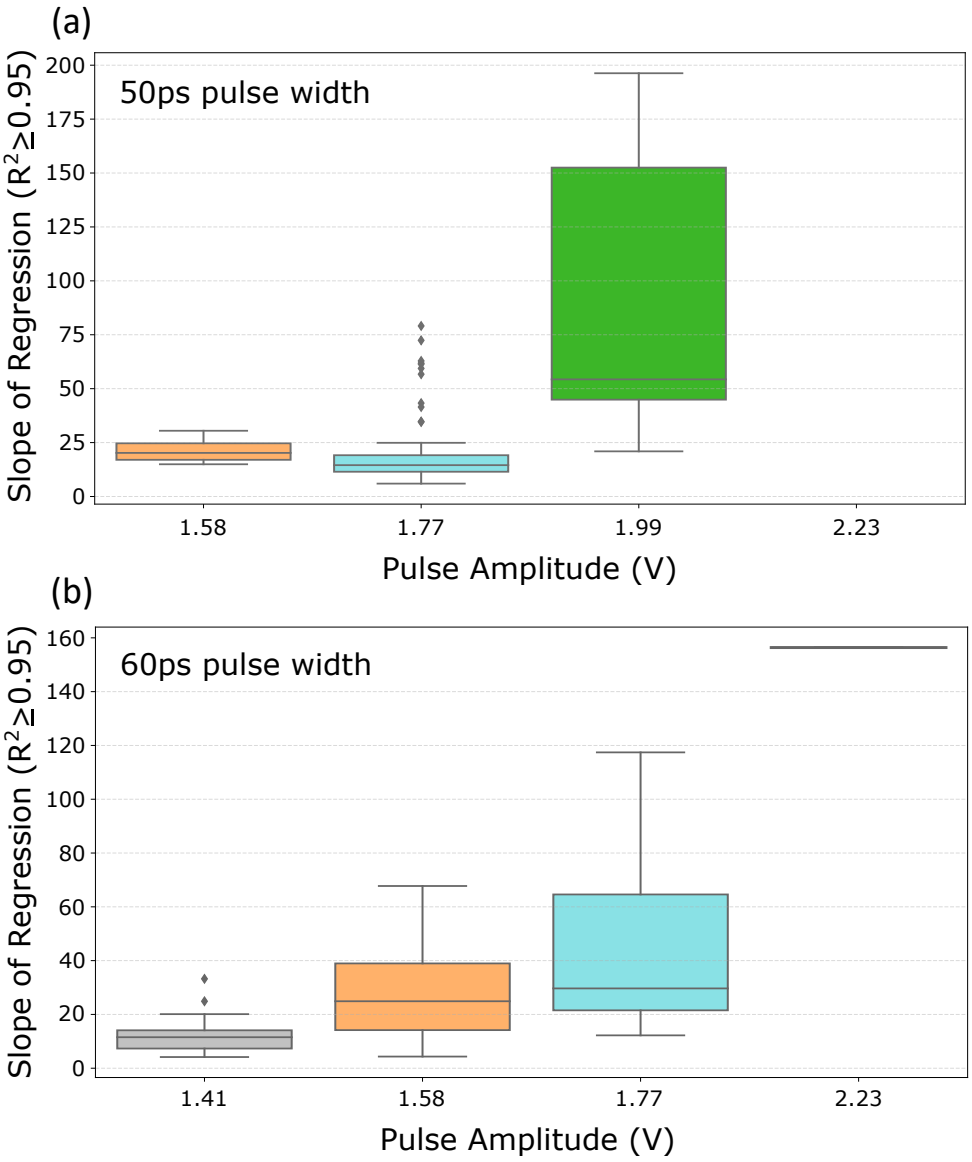


Figure 4.9: (a) Distribution of slope values for a pulse width of 50 ps, considering at least 10 pulses in the linear regime. The optimal linear transition is observed at 1.77 V, where the box plot is narrow, indicating minimal variability. At voltages above and below this value, the slopes become more dispersed, reflecting greater variability. (b) Distribution of slope values for a pulse width of 60 ps. The optimal linear transition occurs at 1.41 V, again evidenced by a narrow box plot with low variability. As the voltage increases, the spread of slopes widens, pointing to increased variability. Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

and device endurance constraints. Furthermore, analyzing less extensive data from multiple devices could have led to unrepresentative or distorted statistical distributions. Therefore, by focusing on one device, this study was able to gather extensive C2C statistics across various biases and timing conditions, providing strong evidence for the observed gradual and linear switching behavior.

Finally, it is important to mention that, in addition to these intrinsic variability factors, specific failure mechanisms were also encountered during the experiments. These instances involved the device unexpectedly switching to the RESET direction instead of the intended SET direction. Raw data illustrating these switching mechanisms can be found in Appendix C. While these anomalous measurements were mostly filtered out from the dataset to preserve the integrity and accuracy of the subsequent analysis, some specific analyses did include this data (in Section 4.2.3).

Device-to-Device (D2D) Switching Behavior

Although the detailed C2C analysis focused on one device, several additional devices were measured to confirm that the gradual and linear switching behavior is consistent across devices and not unique to the single device studied. Figure 4.10 presents the results obtained from four additional TaO_x devices, specifically identified as RF33_026_R3_C3, RF33_026_R3_C4, RF33_026_R3_C5, and RF33_026_R3_C6. For clarity, the device naming convention follows a structured format: RF33 designates the sample name, 026 denotes the specific block number within that sample, and the characters R and C indicate the row and column positions of each device within its respective block.

A critical observation from these supplementary measurements is that all four of these additional devices consistently exhibited gradual and linear conductance behavior, mirroring the trends observed in the primary device. Each of these devices demonstrated the ability to maintain between 35 to 50 pulses within the linear region, and their respective linear fits consistently yielded a coefficient of determination (R^2) greater than 95%. This consistency across multiple devices, including the device extensively studied in Figure 4.4 (RF33_056_R3_C2), demonstrates that gradual and linear switching is a reproducible and intrinsic feature of the TaO_x device structure.

As mentioned earlier, the primary in-depth analysis focused on a single device due to practical experimental limitations, which allowed comprehensive C2C statistics to be collected across different biases and timing conditions. This approach provided a clear proof of concept for the observed gradual and linear switching. The consistent results from the additional devices shown in Figure 4.10 further confirm that gradual and linear potentiation can be achieved at short timescales across multiple devices, supporting the general applicability of these findings.

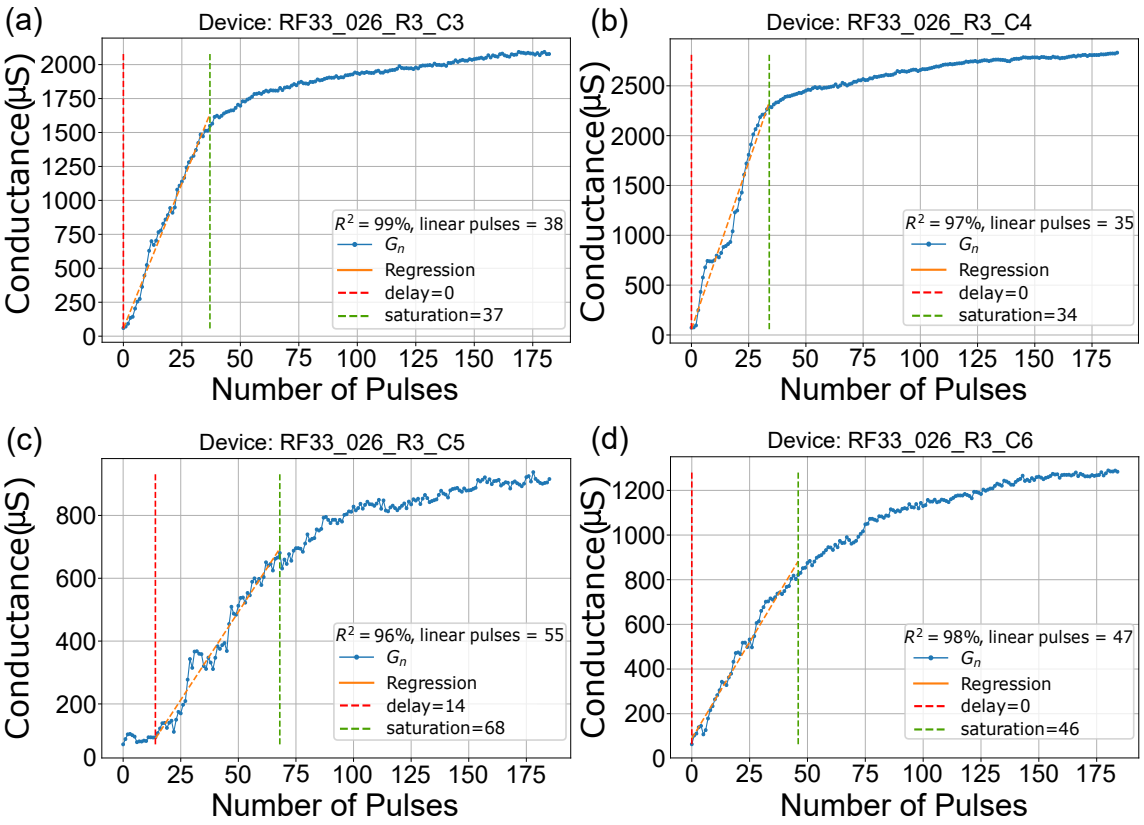


Figure 4.10: Gradual and linear switching behavior recorded in several TaO_x devices using a pulse width of 50 ps. The applied voltages are: (a) 2.23 V, (b) 2.5 V, (c) 1.77 V, and (d) 1.99 V. In all cases, the conductance evolution follows similar trends, with linear fits yielding R^2 values greater than 95 %. This observation aligns with the trends shown for the representative device in Figure 4.4. Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

4.2.4. Impact of Initial Low Conductive State (LCS)

Beyond device variability and failure mechanisms, the influence of the initial LCS on switching behavior was investigated. To gain deeper insight into this dependency, device behavior was characterized across both ultra-fast and slow timescales, with particular attention to how the initial LCS impacts the switching characteristics.

The initial LCS distribution for SET pulse measurements conducted at fast timescales is presented in Figure 4.11(a). This distribution indicates that the majority of measurements fall within the range of 25 µS to 150 µS. Importantly, this distribution encompasses all collected measurements, including those affected by variability and instances of device failure.

Building upon these observations, Figure 4.11(b) illustrates the success rate of achieving gradual and linear switching under various initial LCS conditions, specifically with short pulse measurements at a 50 ps pulse width. For this analysis, “success” is rigorously defined as the device exhibiting switching with a minimum of 10 pulses in the linear region and attaining a coefficient of determination (R^2) of 95%. This figure (Figure 4.11) provides

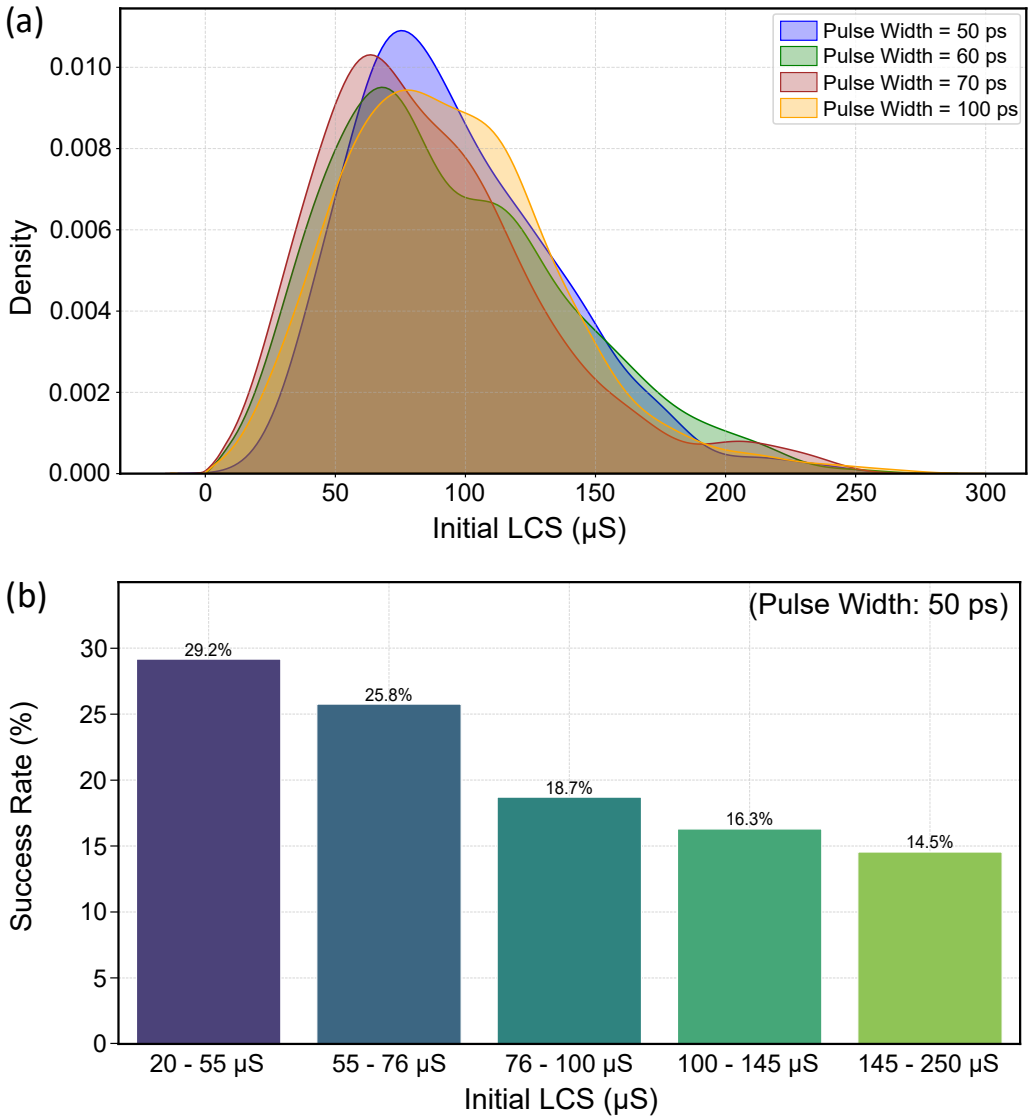


Figure 4.11: (a) Distribution of the initial LCS, showing the total number of SET pulse measurements that fall within the LCS range for different pulse widths. (b) Bar plot presenting the success rate of achieving linear switching for a pulse width of 50 ps, defined as sustaining at least 10 pulses in the linear regime with $R^2 \geq 95\,\%$. The data indicate that linear transitions are more reliably obtained when the initial LCS is lower, as this provides a broader window of linear states before saturation occurs. Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

a direct comparison with established prior research. Previous studies [7, 10, 152] indicated that a higher initial LCS typically facilitates a more gradual and linear transition, while a lower initial LCS often leads to abrupt switching characteristics. However, the data presented in Figure 4.11(b) reveals a contrasting behavior when short pulses are employed. The results demonstrate that even with a low initial LCS, the device switching remains gradual and linear at fast timescales. This is particularly evident within the 20 µS to 55 µS LCS range, where a high success rate for linear potentiation is observed. This suggests that the application of short pulses effectively mitigates the abrupt transitions conventionally associated with a low initial LCS. Moreover, a key advantage of starting from a low initial LCS is the inherently wider conductance window available. This expanded window provides increased capacity for achieving multiple linear states before saturation, thereby enabling short pulses to effectively utilize the entire conductance range for switching. This mechanism facilitates gradual and linear transitions in small, controlled steps, ultimately leading to a higher number of pulses within the linear region.

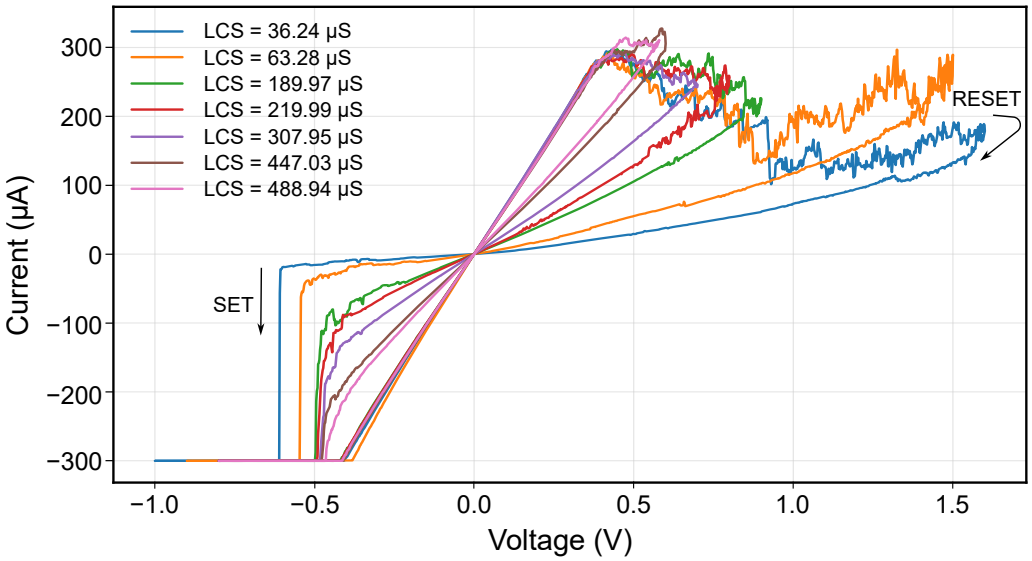


Figure 4.12: The *I*-*V* characteristics of the VCM device reveal that increasing the RESET voltage reduces the LCS, which in turn facilitates a sharp transition to the HCS during the SET process, as demonstrated by the blue *I*-*V* trace. Reproduced from Munir *et al.* [146], © 2025 The Authors, licensed under CC BY 4.0.

Following the short pulse measurements, supplementary DC measurements were performed on the same device to confirm the distinct behavior observed at different timescales, as illustrated in Figure 4.12. This figure displays various *I*-*V* sweeps, each initiated from a different RESET voltage. Consistent with prior observations, when the initial LCS is low (e.g., 36.24 µS), the device exhibits an abrupt switching behavior. Conversely, as the LCS increases, the switching transition progressively shifts from an abrupt to a more linear response. These DC characteristics are in agreement with previous studies [7, 10, 152], which similarly reported that a higher initial LCS promotes a more

linear transition. This direct comparison unequivocally confirms that the influence of the initial LCS on device behavior is indeed dependent on the timescale of the applied electrical stimuli, exhibiting different responses in the fast and slow regimes.

The findings highlight the complex interplay between pulse parameters, device variability, and potential failure mechanisms. Some pulse conditions may help achieve more stable and linear switching, while others could exacerbate C2C variations or even cause unexpected switching behavior. Therefore, a thorough understanding and effective management of these variability factors and failure mechanisms are paramount for the successful development of reliable and predictable resistive switching devices, particularly for their integration into advanced neuromorphic computing applications.

4.3. Conclusion

This chapter has presented a significant advancement in the understanding and control of resistive switching dynamics in Pt/TaO_x/Ta/Pt stack filamentary VCM devices, demonstrating for the first time a proof of concept that gradual and highly linear conductance modulation is achievable on sub-100 ps timescales. In this regime, the Joule heating-induced thermal runaway is suppressed because the applied pulses are shorter than the thermal time constant of the conductive filaments, thereby preventing positive feedback. By carefully engineering the pulse width and voltage, linear transitions in VCM devices were achieved. The results specifically showed that a 50 ps pulse at 1.77 V enables the VCM devices to switch gradually and linearly ($R^2 = 99.5\%$) with 104 pulses in the linear region.

This finding provides a significant point of comparison to prior research, where similar gradual switching in HfO_2-based and HfO_2/TiO_x bilayer ReRAM devices has been reported [7, 10]. While their work demonstrated that gradual switching could be achieved with pulse widths down to 100 ns, and emphasized the importance of suppressing positive feedback from Joule heating for linear potentiation, their investigations were primarily confined to these longer pulse regimes. Crucially, these prior works typically yielded a limited number of pulses (e.g., a maximum of 10) in the linear region. In contrast, operation in the sub-100 ps regime in this study allowed for a significantly higher number of linear pulses (over 100), thereby extending the accessible linear window for synaptic applications.

A notable finding was that short pulses overcome the typical behavior associated with a low initial LCS. While prior research often indicates that a low LCS leads to abrupt transitions [7, 10, 152], this study shows that operating in the sub-100 ps regime allows for gradual and linear transitions even when starting from a low initial LCS. This offers a distinct advantage, as it enables access to a wider range of linear conductance states.

Despite demonstrating gradual and linear switching, the reproducibility of this behavior

faces a significant challenge due to inherent C2C variability. Extensive statistical analysis conducted in this study highlights the spread in experimental outcomes, indicating the stochastic nature of switching at these fast timescales. Nevertheless, the consistent behavior observed across multiple TaO_x devices (D2D) confirms that this gradual and linear potentiation is an intrinsic and reproducible characteristic of the device structure, rather than a singular occurrence.

5. VCM Switching with Short Pulses and Short Delays

In Chapter 4, it was shown that applying ultra-short pulses can overcome abrupt switching and enable linear potentiation in TaO_x-based VCM devices. These experiments, however, were carried out with long delays between pulses on the order of seconds, meaning that possible interactions between closely spaced pulses were not considered. Under these conditions, each pulse acts on a device state that is not influenced by preceding pulses, and the switching dynamics are determined primarily by the applied pulse amplitude and width.

When the delay between consecutive pulses is reduced, this assumption may no longer hold. Experimental studies have demonstrated that thermal accumulation can influence the switching behavior of oxide-based memristive devices when voltage pulses are applied with sufficiently short delays, primarily at microsecond to nanosecond timescales [24]. Complementary theoretical and simulation studies have further suggested that the characteristic thermal relaxation time of VCM devices may be short enough for residual heat to influence subsequent pulses even when the inter-pulse delay is reduced toward the sub-ns regime [25]. This raises the question of how potentiation behaves when the delay between ultra-short pulses is reduced to the sub-ns range.

The presence of such delay-dependent effects is of fundamental interest for understanding switching dynamics in VCM devices. As discussed in Section 2.6.1, device temperature can function as a second internal state variable, analogous to the calcium ion concentration in biological synapses. If thermal accumulation mimics these calcium dynamics, timing-dependent synaptic behaviors, such as PPF and PTP, can be observed in response to voltage pulse trains with short inter-pulse delays.

Investigating switching dynamics at sub-ns delays is experimentally challenging. The ultra-short interval between consecutive pulses does not allow for conventional DC read operations to be performed between pulses. As a result, the device conductance cannot be accessed directly during pulse application, and alternative approaches are required to extract the conductance evolution under these conditions.

To address this challenge, this chapter employs a high-bandwidth RF setup to apply trains of ultra-short SET pulses with systematically varied pulse widths, amplitudes, and

inter-pulse delays. Instead of performing read operations between pulses, the conductance evolution is reconstructed from the transient electrical response measured during pulse application using appropriate evaluation methods [153].

Based on this approach, the chapter investigates delay-dependent switching behavior in TaO_x-based VCM devices and extends the analysis to short-term synaptic plasticity phenomena, specifically PPF and PTP.

The chapter first introduces the experimental methodology and evaluation methods, then investigates delay-dependent switching and synaptic-like behavior in TaO_x-based VCM devices. The evaluation methodology presented in this chapter is based on the work published in Munir *et al.* [153], for which the experimental measurements and analysis were carried out as part of this doctoral research.

5.1. Experimental

The experimental setup employed in this study was the same as that described in Chapter 4 (see Figure 3.3), with the only modification being the replacement of the PG5 pulse generator by the PPG30. The PPG30, developed by Sympuls GmbH, provides greater flexibility in adjusting the electrical pulse parameters, including amplitude, width, repetition rate, and delay. In particular, the delay between pulses can be controlled down to 33 ps, and the generator produces pulses with rise and fall times of approximately 20 ps. A more detailed description of the PPG30 is provided in Section 3.1.

The DUTs were TaO_x-based structures, similar to those used in Chapter 4, with an active device area of $2\times2\,\mu m^2$, and are also described briefly in Section 3.2. Before carrying out the high-speed pulse measurements, all TaO_x devices were prepared in the same way as described in Chapter 4. Each device first underwent the necessary electroforming step, after which 100 *I-V* sweep cycles were performed. The parameters used for the electroforming and the subsequent SET/RESET cycles were the same as those employed for the devices discussed in Chapter 4. This procedure was carried out to improve the endurance of the devices and to ensure that their switching behavior remained stable and reproducible. Both the electroforming and the *I-V* sweeps were performed using a Keithley 2634B SMU, with the voltage applied to the BE of the devices.

5.1.1. Measurement Protocol

After completing the electroforming and 100 *I-V* sweeps, fast pulse measurements were carried out on the DUTs. The overall fast measurement procedure followed a structured cycle consisting of four main steps, as illustrated in Figure 5.1.

- **Pre-read:** Before applying any pulse train, the conductance state of the device was measured at a low read voltage of 0.2 V.

- **Ultra-fast pulse sequence:** A sequence of ultra-fast SET pulses was applied using the PPG30 generator. Each pulse train consisted of 25 pulses. The parameters were systematically varied across measurement cycles:
  - Pulse width: 50 ps to 500 ps
  - Pulse delay: 50 ps to 1 ns
  - Pulse amplitude: +1.0 V to +2.0 V
- **Post-read:** After the pulse train, the device conductance was again measured at 0.2 V, allowing direct comparison with the pre-read state and providing information on the conductance change induced by the applied pulses.
- ***I-V* sweep:** To complete the measurement cycle, a full *I-V* sweep was performed to verify that the device remained fully functional and had successfully returned to its initial LCS (HRS). The SET sweep was performed up to a maximum voltage of $+1.2$ V with a compliance current of 300 μA, while the RESET sweep was performed to a maximum voltage of -1.6 V, both using the same sweep rate of 0.5 V/s.

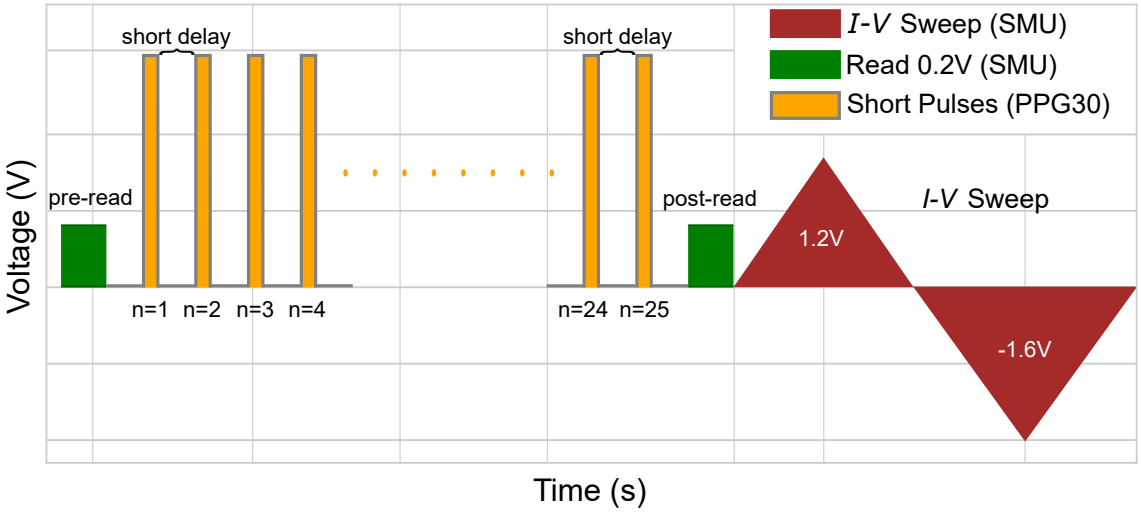


Figure 5.1: Schematic of the measurement cycle used for fast pulse measurements. Each cycle begins with a pre-read, during which the device resistance is measured at a low DC read voltage of 0.2 V. This is followed by the application of a sequence of ultra-fast SET pulses (shown as orange rectangles), generated by the PPG30. Each pulse train consists of 25 pulses, applied with a short delay between consecutive pulses (50 ps - 1 ns). After completion of the pulse sequence, a post-read at 0.2 V is performed to evaluate the conductance change induced by the pulses. Finally, a full *I-V* sweep is carried out using the SMU (shown as red triangles) to verify device functionality and to ensure that the device has returned to its initial LCS (HRS). Unless stated otherwise, all electrical stimuli in this cycle were applied to the top TE.

This sequence of four steps constituted one complete fast pulse measurement (RF measurement) cycle. In these cycles, the electrical pulses were applied to the TE rather than the BE. This configuration was adopted because the PPG30 generator provides a significantly higher positive output amplitude ($+1.0$ to $+2.0$ V) compared to its negative output amplitude (-0.6 to -1.0 V). The limited negative amplitude was insufficient to reliably switch the devices to the HCS (LRS) at such short pulse widths. To maintain consistency with this pulsing scheme, the polarity of the SMU operations during the measurement cycle was reversed accordingly.

It should be noted that throughout this chapter, the applied voltage V_{app} refers exclusively to the effective device voltage, $V_{\text{P,eff}}$. Due to signal reflections at the device interface, the effective voltage at the device is approximately twice the amplitude generated by the PPG30, as detailed in Table 3.1.

During the fast pulse measurements, the transient response of the devices was monitored using a high-bandwidth oscilloscope, as described in Section 3.1. The oscilloscope was connected to the device BE through a 50 Ω input termination. This configuration enabled

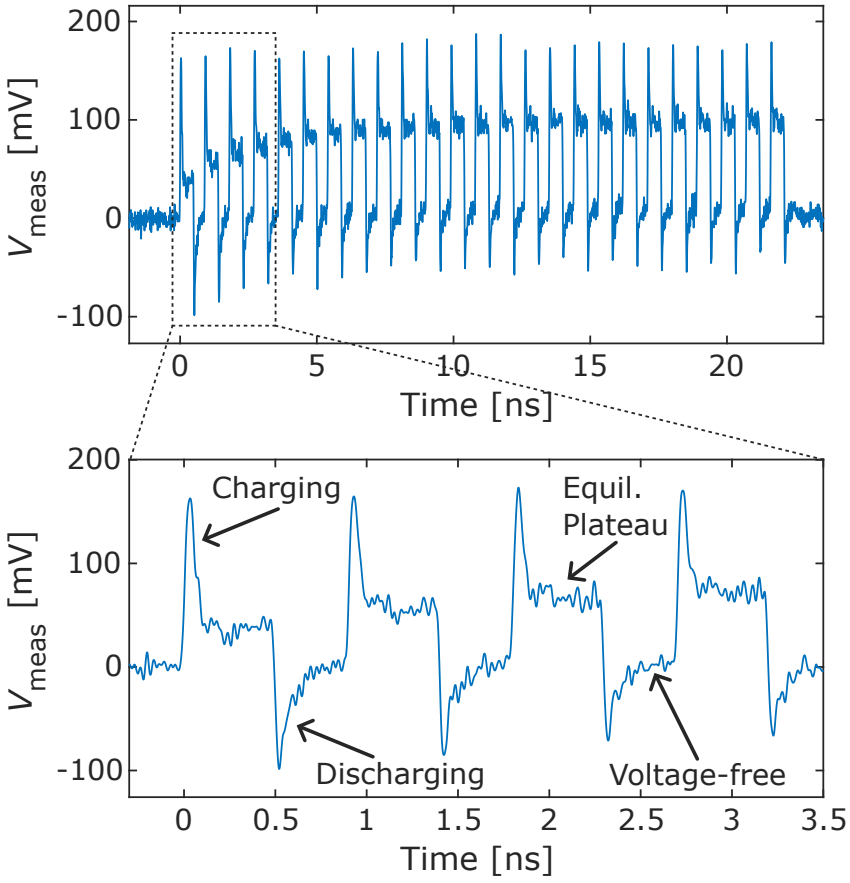


Figure 5.2: Oscilloscope response showing a pulse train with 500 ps pulse width and 400 ps pulse delay at an applied voltage of $V_{\text{app,S}} = 1.2$ V. The voltage peaks observed at the start and end of each pulse result from capacitive charging and discharging effects. Reproduced from Munir *et al.* [153], © 2025 The Authors, licensed under CC BY 4.0.

direct recording of the voltage drop across the device during the application of ultra-fast electrical pulses, which could then be translated into the corresponding current response. A representative oscilloscope trace of a pulse train is shown in Figure 5.2. Careful inspection of such traces reveals that each pulse can be divided into four characteristic regions: an initial charging peak, an equilibrium plateau, a discharging peak, and finally a short voltage-free interval before the arrival of the next pulse.

When the pulse width and the delay between consecutive pulses are relatively long, all four regions can be clearly distinguished. The charging and discharging peaks correspond to the fast capacitive currents that arise from the intrinsic capacitance of the TaO_x devices and the measurement setup. The plateau region reflects the steady-state conduction current through the device during the pulse, while the voltage-free section provides a short interval in which the device is not biased. In this case, the current level observed on the plateau can be taken as a reliable indicator of the device conductance state.

However, as the pulse width and the delay are reduced to very short timescales in the sub-ns regime, the situation changes significantly. The charging and discharging transients begin to dominate the signal, while the plateau and the voltage-free regions shrink considerably or may even vanish completely. Under such conditions, the capacitive contribution overlaps strongly with the actual conduction current, and the measured trace no longer provides a direct indication of the resistive state of the device. This overlap is particularly problematic when attempting to determine the potentiation behavior at these timescales, as the short inter-pulse delays provide insufficient time for DC read operations between consecutive pulses.

Therefore, although the oscilloscope provides valuable raw data of the fast transient response, additional evaluation methods are required to separate the capacitive contribution from the true device current. Only by doing so can the conductance dynamics of the TaO_x devices be accurately characterized at ultra-short timescales. This necessity forms the motivation for the development and application of the *reference method* and the *integration method*, which are discussed in the following sections.

5.2. Evaluation Methods

5.2.1. Reference Method

The reference method is designed to address one of the main difficulties in ultra-fast pulse characterization: the strong capacitive contribution of the measurement setup. When a voltage pulse is applied to the device, the oscilloscope records not only the current flowing through the device but also the capacitive charging and discharging of the setup. This means that the measured current I_{meas} always contains two parts: the actual device current I_{dev} and the capacitive current I_{cap}. For a reliable evaluation of the switching dynamics, it

is therefore necessary to separate the device current from the capacitive contribution.

The basic principle of the reference method is to measure the capacitive current separately under conditions where the device does not switch, and then subtract this reference current from the switching measurement. For this purpose, two types of pulse trains are used: one that induces switching, called a *switching pulse train*, and another that does not change the device state, called a *non-switching pulse train*. The non-switching train is applied in the same way as the SET pulses in terms of timing, number of pulses, and duration, but the pulse amplitude is reduced to a value $V_{\mathrm{app,NS}}$ that is too small to switch the device. In this study, $V_{\mathrm{app,NS}} = 0.8$ V or lower was used. Under these conditions, the measured current corresponds only to the capacitive part and is taken as I_{cap}.

Since I_{cap} is proportional to the applied voltage, the non-switching trace measured at $V_{\mathrm{app,NS}}$ cannot be directly compared to the switching trace recorded at $V_{\mathrm{app,S}}$. Therefore, the reference trace has to be scaled to the switching voltage before subtraction. This relation is given by [6]:

$$I_{\mathrm{cap}}(V_{\mathrm{app,S}}) = I_{\mathrm{cap}}(V_{\mathrm{app,NS}}) \cdot \frac{V_{\mathrm{app,S}}}{V_{\mathrm{app,NS}}} \tag{5.1}$$

An example of this procedure is shown in Figure 5.3(a). After scaling, the non-switching curve closely matches the switching curve. The slight difference that remains between them is due to the change in the device resistance during the SET process. Once I_{cap} is known, the device current I_{dev} can be obtained by subtracting it from the measured current I_{meas}:

$$I_{\mathrm{dev}} = I_{\mathrm{meas}}(V_{\mathrm{app,S}}) - I_{\mathrm{cap}}(V_{\mathrm{app,S}}) \tag{5.2}$$

The resulting device current I_{dev} is shown in Figure 5.3(b). Within each pulse, the current increases while the pulse is applied and then decreases again in the interval before the next pulse. This behavior reflects the expected change of the device state during the pulse sequence. Small fluctuations can also be seen in the signal, which mainly come from measurement noise and the small differences that occur between repeated measurements.

To assign a specific current value to each pulse, a pulse window is introduced. This interval is defined by two limits: the start of capacitive charging at t_1 and the end of capacitive discharging at t_2. The width of the pulse window is therefore $t_2 - t_1$. The positions of these limits must be determined visually from the measured voltage or current response. In practice, t_1 can usually be identified quite clearly, since the onset of charging produces a distinct feature in the trace. In contrast, t_2 is more difficult to locate, because the discharging follows an exponential decay and gradually approaches zero. Nevertheless, small variations in the choice of t_2 have only a minor influence on the calculated integral in Equation 5.3 and Equation 5.4, as the current at the end of the discharging process is already very close to the zero line.

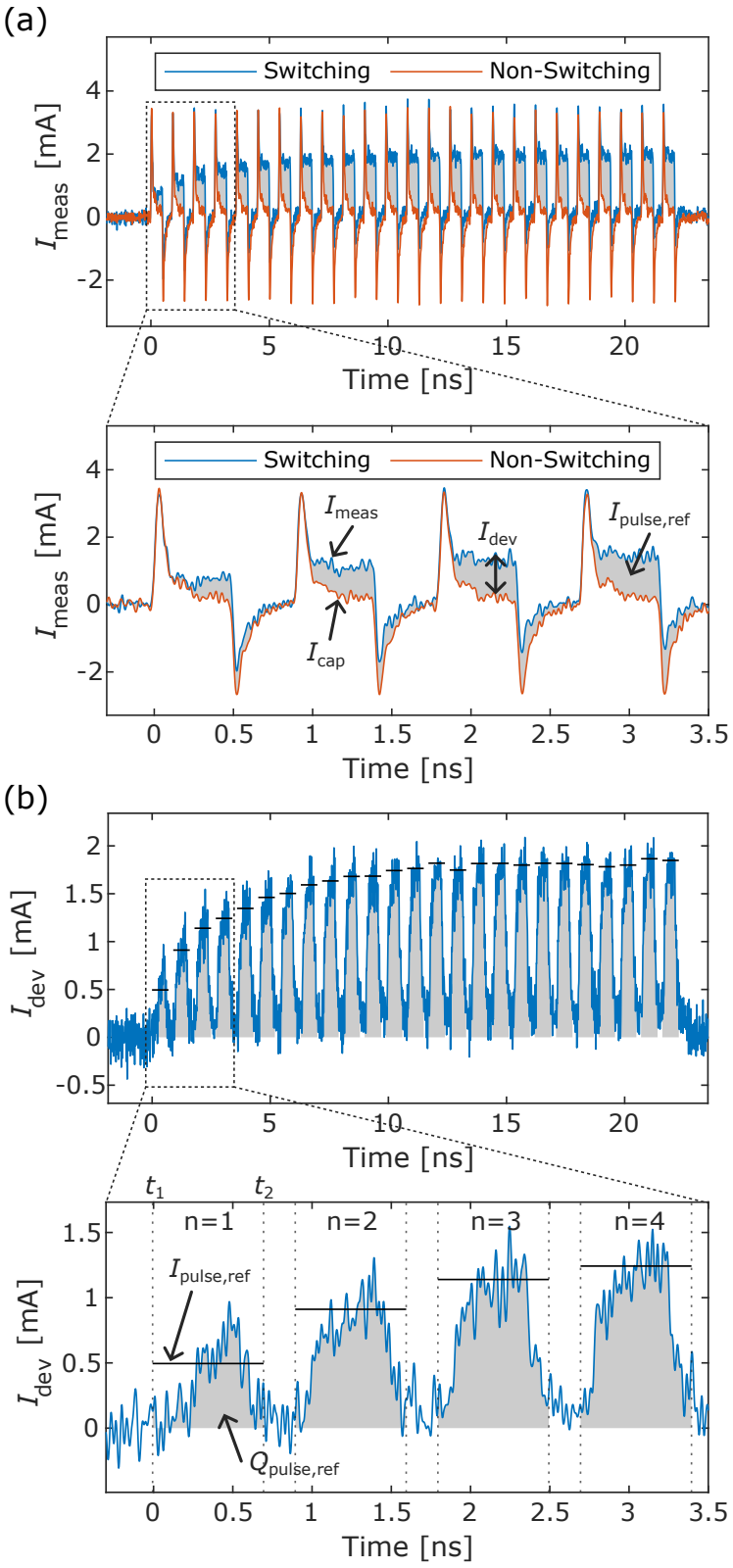


Figure 5.3: In the reference method, both a switching measurement ($V_{app,S} = 1.2$ V) and a non-switching measurement ($V_{app,NS} = 0.8$ V) are required. (a) displays the measured current I_{meas} for a switching pulse train together with the (scaled) non-switching current I_{cap}. Their difference corresponds to the device current I_{dev}, which is presented in (b). The mean value of the current is then used to assign a characteristic current level to each pulse. The vertical dashed lines mark the beginning and end of the pulse window. Reproduced from Munir *et al.* [153], © 2025 The Authors, licensed under CC BY 4.0.

As shown in Figure 5.3(b), the grey-shaded area beneath the curve represents the electrical charge $Q_{\text{pulse,ref}}$ that passes through the device during a single pulse. By assuming that this charge is distributed over the pulse width T_{pw}, an average current value can be calculated. This average current is defined as $I_{\text{pulse,ref}}$, which represents the mean current flowing through the device during the pulse duration. The same calculation is performed for every pulse n in the pulse train, allowing the current values for the entire pulse sequence to be determined. The procedure can be summarized mathematically as:

$$I_{\text{pulse,ref}}(n) = \frac{Q_{\text{pulse,ref}}(n)}{T_{\text{pw}}} = \frac{\int_{t_1(n)}^{t_2(n)} I_{\text{dev}}(t)\,\mathrm{d}t}{T_{\text{pw}}} \tag{5.3}$$

By repeating this procedure for the complete pulse train, the evolution of the device current I_{dev} from one pulse to the next can be determined with reasonable accuracy. This reveals how the device state evolves during the application of fast pulses. The reference method therefore provides a way to separate I_{cap} from I_{meas} and to calculate I_{dev} for each pulse. Although the method requires additional non-switching measurements and careful scaling of the signals, it offers a reliable approach for extracting meaningful results from the oscilloscope traces, which would otherwise be difficult to interpret directly.

5.2.2. Integration Method

In the integration method, the underlying assumption is that the capacitive charging and discharging that occur during the application of a voltage pulse essentially cancel each other out over the entire duration of the pulse. This makes the method fundamentally simpler than the reference method, since no additional non-switching measurement is required to separate the capacitive part from the device response. In other words, the integration method directly uses the measured signal, relying on the fact that the positive and negative capacitive contributions balance each other when integrated across the pulse.

For evaluating the current response, the same pulse window is applied as in the reference method. This means that both the charging phase at the beginning and the discharging phase at the end of the pulse are included in the calculation. The interval of interest is therefore defined between t_1, which marks the onset of charging, and t_2, which corresponds to the completion of discharging. Within this time window, the measured signal is integrated to obtain the total charge.

As shown in Figure 5.4, the shaded grey area under the curve represents the charge $Q_{\text{pulse,int}}$ that passes through the device during a single pulse. To convert this charge into a current value that can be compared across different pulses, the charge is divided by the width of the pulse T_{pw}. This procedure gives the average current associated with each pulse n in the pulse train, expressed mathematically as:

$$I_{\text{pulse,int}}(\mathrm{n}) = \frac{Q_{\text{pulse,int}}(\mathrm{n})}{T_{\text{pw}}} = \frac{\int_{t_1(\mathrm{n})}^{t_2(\mathrm{n})} I_{\text{meas}}(t)\,\mathrm{d}t}{T_{\text{pw}}} \tag{5.4}$$

By applying this calculation repeatedly for all pulses within the train, the evolution of the device current as the number of pulses increases can be followed. This typically results in a gradually increasing current response during the switching process, consistent with the expected resistive change of the device. The integration method, therefore, provides a straightforward approach for analyzing pulse measurements. It avoids the additional reference steps required by the reference method while still providing reliable information on the switching behavior of the device.

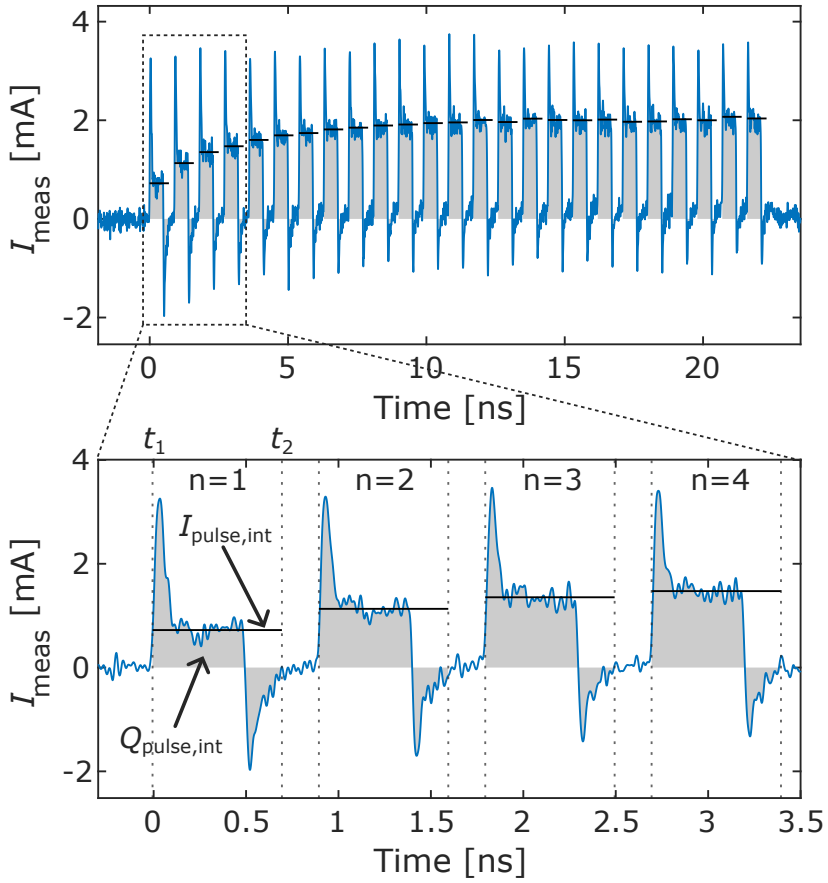


Figure 5.4: The integration method relies on the assumption that capacitive charging and discharging cancel one another. The regions used for the calculation are highlighted in grey. For each pulse, a corresponding current value is determined and represented by the horizontal black lines. The vertical dashed lines mark the beginning and end of the pulse window. A voltage of $V_{\text{app,S}} = 1.2\,\text{V}$ is applied to the device during this measurement. Reproduced from Munir *et al.* [153], © 2025 The Authors, licensed under CC BY 4.0.

5.2.3. Discussion

A direct comparison between the reference method and the integration method is shown in Figure 5.5(a) for an exemplary measurement with a pulse width of 500 ps and a delay of 400 ps. The figure illustrates how both methods capture the gradual switching of the device as it transitions from the pre-read state, corresponding to the LCS (HRS), toward the post-read state, corresponding to the HCS (LRS). In both cases, the evolution of the device state over consecutive pulses is clearly visible. To quantify the consistency between the two methods, the absolute error was calculated, representing the deviation between the current values obtained from pulse pairs of the reference and integration methods. The results demonstrate that this error does not follow any systematic trend and, importantly, is independent of both the pulse number and the conductance state of the device. This indicates that the two evaluation approaches generally track the same switching behavior of the device.

Although both methods provide reliable information, the values extracted using the reference method are systematically lower than those obtained from the integration method. The origin of this difference lies in the fact that during reference measurements (non-switching measurements), a small current continues to pass through the device even when non-switching pulses are applied. This current, denoted as $I_{\mathrm{cap}}(V_{\mathrm{app,NS}})$, cannot be neglected and becomes evident when comparing the two methods directly. The effect is not limited to a single set of parameters but is observed consistently across all measurement conditions. This trend is summarized in Figure 5.5(b), where the mean absolute error (MAE) between the reference method and the integration method is plotted.

The figure clearly shows that the deviation between the two methods is smaller when short pulses are combined with short delays. Under such conditions, less current flows through the device during non-switching measurements due to the shorter time available. In contrast, longer pulse widths provide sufficient time for the device to fully charge and for current to flow through the device for a longer duration. Consequently, more current passes through the device during non-switching measurements with longer pulses, leading to larger deviations between the two methods. This analysis demonstrates that while both methods are valid, the degree of agreement between them depends on the pulse parameters.

For benchmarking the accuracy of both evaluation methods, the conductance state obtained from the last pulse in a train is compared directly to the value recorded during the post-read operation. The deviations resulting from this comparison for different combinations of pulse widths and delays are shown in Figure 5.5(c) and Figure 5.5(d). These deviations do not follow a systematic trend but appear randomly distributed. This randomness reflects the stochastic nature of read noise and short-term instabilities that can occur in the short time interval between the last applied pulse and the subsequent post-read measurement [154]. As a result, both positive and negative deviations are

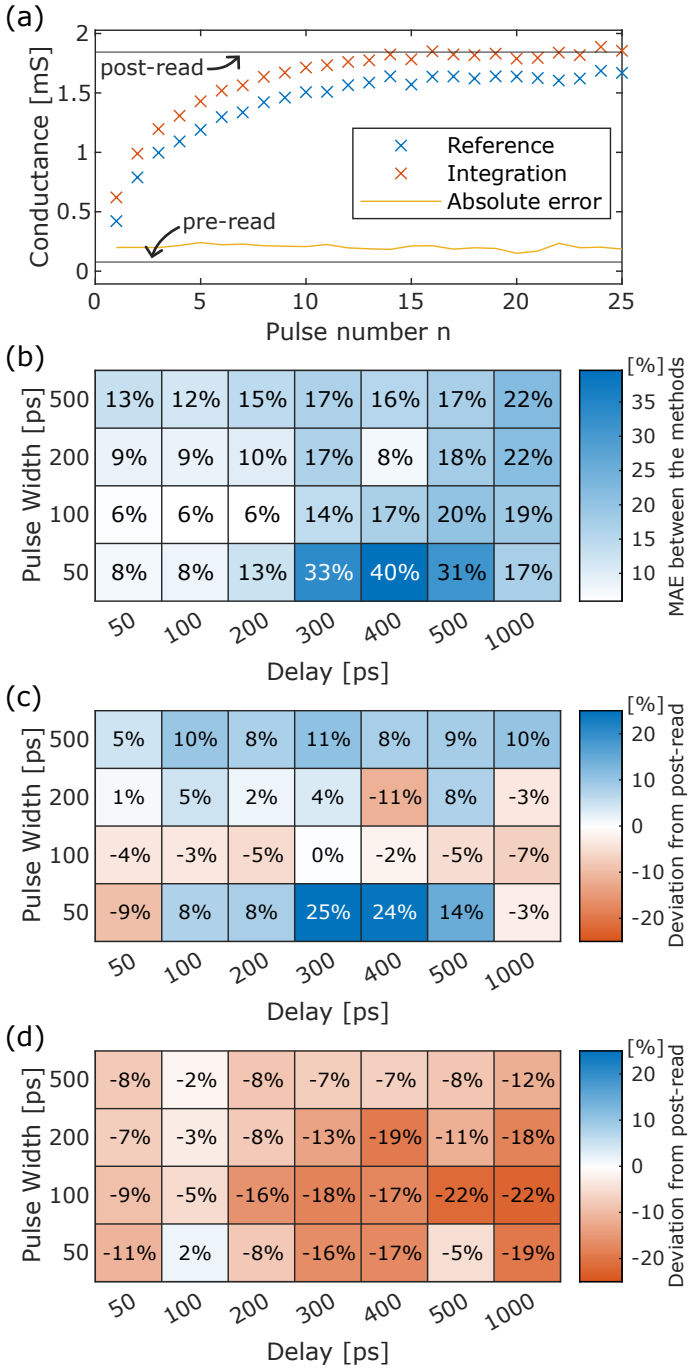


Figure 5.5: (a) Conductance states determined after each pulse using both the reference method and the integration method. The data are shown for a measurement with a pulse width of 500 ps and a delay of 400 ps. Horizontal lines mark the pre-read LCS (HRS) and post-read HCS (LRS) states. The yellow line represents the absolute error between both methods, indicating no systematic trend in deviation across pulse number or conductance state. (b) presents how the MAE between the two methods varies with pulse width and delay parameters. (c) illustrates the deviation of the final pulse conductance state from the post-read value using the integration method, while (d) shows the corresponding deviation for the reference method. Data shown in (b)-(d) represent averaged values obtained from ten individual measurements for each parameter configuration. Reproduced from Munir *et al.* [153], © 2025 The Authors, licensed under CC BY 4.0.

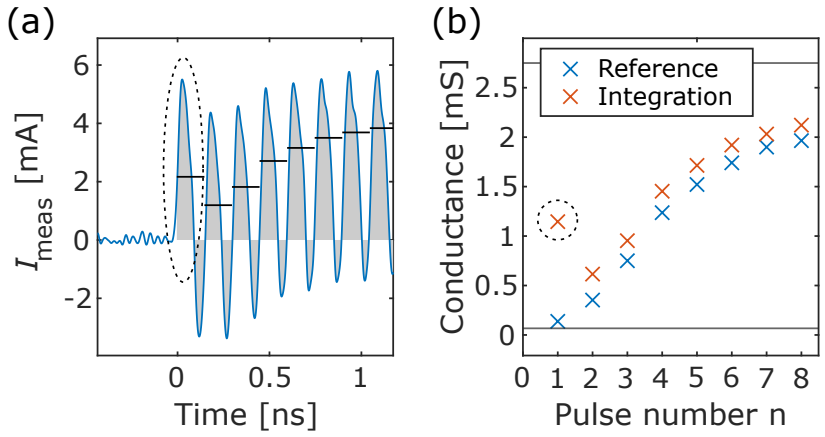


Figure 5.6: (a) presents the measured current from a pulse train with 100 ps pulse width and 50 ps pulse delay at an applied voltage of $V_{app,S} = 2$ V. The capacitive charging peak of the first pulse appears larger because no preceding pulse is present. (b) demonstrates the incorrect determination of the conductance of the first pulse when evaluated with the integration method. Reproduced from Munir *et al.* [153], © 2025 The Authors, licensed under CC BY 4.0.

observed, depending on the specific pulse sequence. When averaged across all conditions, the integration method shows a mean deviation of about 3.8 %. In contrast, the reference method systematically underestimates the conductance state. This underestimation occurs in addition to the deviations already introduced by read noise and stochastic effects. As illustrated in Figure 5.5(d), the average deviation for the reference method amounts to approximately -11.2 %. These results demonstrate that the reference method consistently produces lower current values compared to the integration method because part of the true device current is effectively subtracted during the non-switching reference measurements required by the method.

A particular limitation of the integration method arises from its assumption that capacitive charging and discharging cancel each other completely within the pulse window. If the delay between two pulses is too short, the device may not fully discharge before the next pulse arrives. In this case, the discharging component does not fully occur within the defined pulse window and is therefore not completely subtracted in the integration method. This leads to an overestimation of the charge associated with the first pulse, resulting in a conductance value that is higher than the actual device state. This effect is illustrated in Figure 5.6(a). However, this effect becomes less significant for longer pulse lengths, since the integrated contributions from the charging and discharging sections become progressively smaller relative to the total pulse duration. In addition, increasing the delay between consecutive pulses allows the device to fully discharge before the next pulse arrives, further reducing the influence of incomplete charging and discharging. In contrast, the reference method is not affected by this limitation because it explicitly removes the charging and discharging contributions through an additional non-switching measurement.

As a result, the conductance state remains correctly determined even when short delays between pulses are used (see Figure 5.6(b)).

Both methods, however, require a careful visual determination of the time limits t_1 and t_2 that define the pulse window for each parameter set. In practice, this means that the start of the charging phase and the end of the discharging phase must be identified from the oscilloscope trace. Slight inaccuracies can occur in this step, for example, when the beginning of the charging cannot be pinpointed exactly, or when the tail of the discharging extends smoothly towards the baseline, making the precise end difficult to define. Fortunately, such minor deviations have only a minimal influence on the calculated results. This is because the current values near the start and end of the pulse are already relatively low, and any remaining asymmetry is typically balanced so that the effect cancels out.

When applying the reference method, additional care must be taken regarding the influence of noise. For very short pulses combined with higher applied voltages $V_{\mathrm{app,S}}$, noise in the measured current has a stronger effect on the evaluation. Since the reference measurement is performed at a fixed lower amplitude $V_{\mathrm{app,NS}}$, the current curve including noise must be rescaled according to Equation 5.1. This scaling increases the relative impact of noise in the calculation of the device current I_{dev} in Equation 5.2. Consequently, shorter pulse widths and higher applied voltages lead to an increased influence of noise on the results obtained with the reference method.

Another critical aspect of the reference method is the precise temporal alignment, often referred to as x-alignment. For accurate evaluation, the charging and discharging peaks of the switching and non-switching measurements must lie exactly on top of one another. Even a slight horizontal shift between the two traces can lead to significant changes in the calculated device current, since the current is determined by taking the difference between the signals (see Figure 5.3). This misalignment effect is particularly strong for shorter pulse widths, where the relative influence of timing is greater. By comparison, the integration method is more robust against such timing shifts, since it does not rely on subtracting a separate reference measurement trace.

Finally, as shown in Figure 5.5(a), the curves obtained using the reference and integration methods generally follow the same overall trend. The main difference is that one set of values appears scaled relative to the other. This indicates that the conductance states can be adjusted to match the post-read values by applying a scaling factor derived from the deviations shown in Figure 5.5(c) and Figure 5.5(d). For demonstration purposes, the scaled conductance states are shown in Figure 5.7(a). After applying this correction, the mean absolute deviation between the two methods becomes quite small, as illustrated in Figure 5.7(b). Noticeable deviations remain only in the case of large delays combined with very short pulse widths, where the scaling factor cannot fully account for the differences. Overall, the main drawback of the reference method compared to the integration method

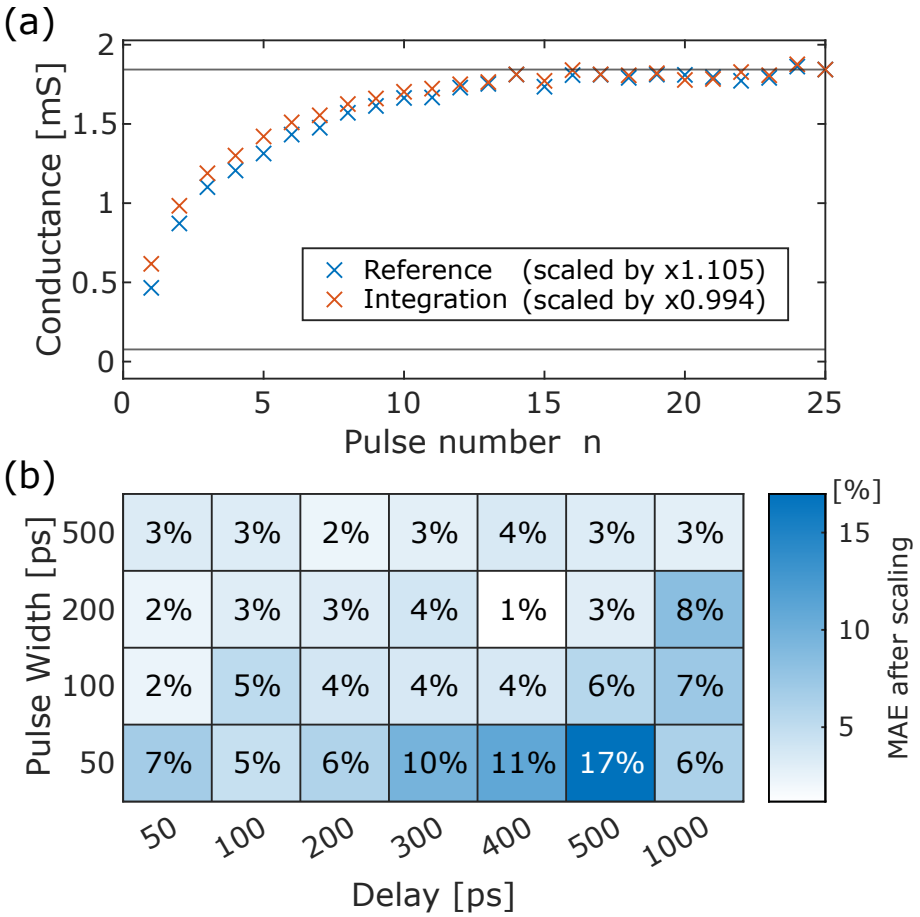


Figure 5.7: (a) Comparison of the reference and integration methods after scaling to the post-read values (cf. Figure 5.5(a)). (b) MAE between the two methods was calculated after applying the scaling correction. The axes and evaluation procedure are identical to those in Figure 5.5(b), but the MAE values are obtained after scaling and are reduced compared to the unscaled case. Reproduced from Munir *et al.* [153], © 2025 The Authors, licensed under CC BY 4.0.

is the additional effort required for reference measurements. Despite this, both methods provide consistent trends and can be reconciled through simple scaling, making their results largely comparable. These evaluation methods form the basis for the subsequent analysis of thermal effects and synaptic-like behavior at sub-ns time scales.

5.3. Studying Thermal Effects in VCM Devices

This section is based on Schön *et al.* [137], for which the experimental measurements were conducted as part of this thesis. Previous experimental studies have demonstrated that thermal accumulation can influence the switching behavior of ReRAM devices when voltage pulses are applied with sufficiently short delays, primarily in the microsecond to nanosecond regime [24, 136]. Electrothermal simulations by Schön *et al.* [25] suggested that such effects should persist at much shorter timescales, extending into the sub-ns

regime, but experimental validation remained limited. The present work experimentally investigates these simulation predictions by studying delay-dependent switching behavior and transient thermal effects in TaO_x-based VCM devices using ultra-short pulses at sub-ns timescales [25].

In the previous sections, evaluation methods for extracting conductance values from such ultra-fast pulse experiments were introduced. Their importance becomes evident at sub-ns timescales, where conventional DC readout between pulses is not feasible due to ultra-short delays between the pulses. In addition, capacitive charging and discharging dominate the measured transient signal, obscuring the device's true resistive response. These methods, therefore, enable the experimental investigation of how short delays between consecutive pulses influence switching behavior in TaO_x-based VCM devices through thermal accumulation effects, which are not observable with conventional read-out approaches.

A representative measurement example is shown in Figure 5.8, which illustrates the evolution of the device conductance as a function of the number of applied pulses. The experiment was performed using a pulse train of 25 consecutive pulses, each with a width of 100 ps and a delay of 50 ps, repeated 500 times to obtain statistically reliable results and account for stochastic variations. The device, initially in the LCS, increases its conductance with successive pulses until it reaches a stable HCS, where the conductance saturates. This demonstrates that SET switching can evolve progressively over multiple sub-ns pulses rather than occurring as a single abrupt event, depending on the applied stress conditions.

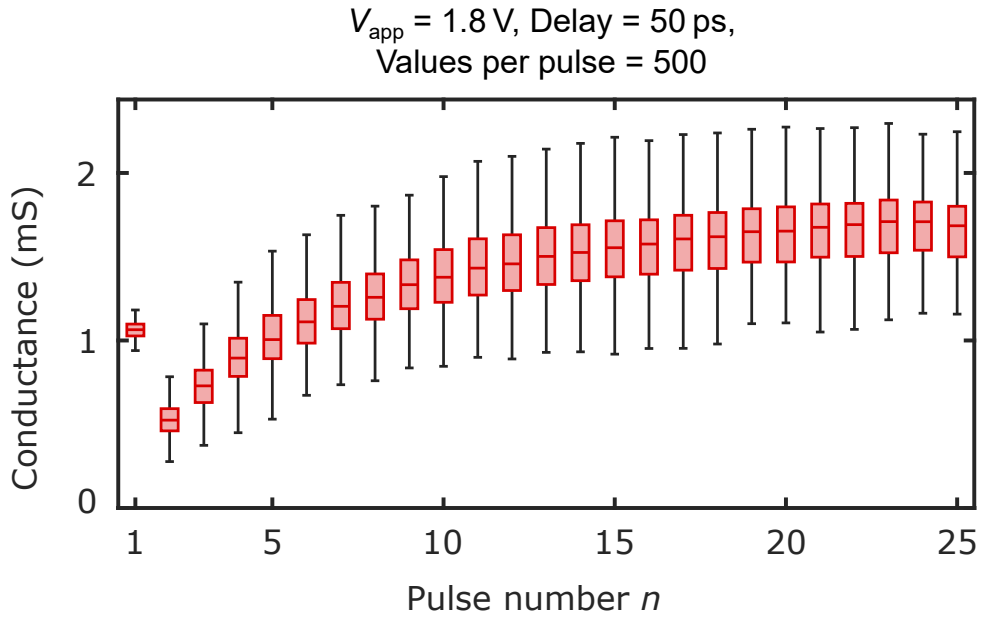


Figure 5.8: An example of a measurement series performed with a pulse width of 100 ps and a pulse delay of 50 ps at an applied voltage of 1.8 V. For each parameter pair, 500 cycles were recorded, which allowed reliable mean values to be determined from the dataset. The conductance evolution was reconstructed using the integration method, enabling the identification of gradual switching dynamics within the applied pulse train.

For this example, the integration method was used to reconstruct the conductance values pulse by pulse, enabling the resolution of gradual conductance changes even at sub-ns timescales, where direct read-out after each pulse would not be feasible.

While Figure 5.8 provided a single measurement example at a fixed delay, Figure 5.9(a)-(f) presents a systematic comparison across different delays and voltages, thereby allowing the thermal accumulation effect to be analyzed in more detail. The figure is divided into three sets of subfigures, each corresponding to one applied voltage: 1.5 V, 1.8 V, and 2.1 V. For each applied voltage, the left subfigures (a, c, e) display the conductance evolution as a function of pulse number for different delays, while the corresponding right subfigures (b, d, f) show the delay-dependent conductance values after selected pulse numbers.

For the lowest applied voltage of 1.5 V, shown in Figure 5.9(a), an apparent delay dependence of the switching behavior can be observed. For short delays (e.g., 50 ps), residual heat from preceding pulses enhances switching, such that the device reaches the HCS within fewer pulses. With increasing delay, the influence of thermal accumulation weakens, the conductance evolution becomes more gradual, and more pulses are required for the device to reach the HCS. At delays of 250 ps and above, the delay dependence is no longer pronounced, and the conductance evolution is mainly determined by the applied pulse amplitude.

A similar delay-dependent behavior is observed at higher pulse amplitudes of 1.8 V and 2.1 V (Figure 5.9(c) and (e)). Short delays again lead to enhanced switching due to thermal accumulation, resulting in a faster increase in conductance, whereas increasing the delay progressively reduces this effect. For delays exceeding approximately 250 ps, thermal accumulation no longer plays a significant role. Compared to 1.5 V, the higher voltages result in a generally faster conductance increase and earlier saturation in the HCS due to the increased electrical stress applied to the device.

The thermal accumulation effect can be more clearly visualized through the delay-dependent analysis presented in Figure 5.9(b), (d), and (f), where the conductance values after selected pulse numbers (5, 10, 15, and 20) are plotted as a function of delay. For delays shorter than about 250 ps, the conductance values obtained after the given pulse numbers (5, 10, 15, and 20) increase noticeably as the delay is reduced, consistent with a faster conductance increase due to thermal accumulation. In contrast, for delays of 250 ps or longer, the device has sufficient time to cool between consecutive pulses and the influence of thermal accumulation is no longer observed. In this case, the conductance evolution for the same pulse numbers no longer depends on the delay, but is mainly determined by the applied pulse amplitude. This characteristic delay of around 250 ps therefore represents the thermal relaxation time of the device and is determined primarily by its intrinsic thermal properties rather than by the external stress conditions.

Therefore, the observed delay-dependent behavior can be attributed to thermal accumulation during pulsed operation, where each voltage pulse generates localized Joule heating

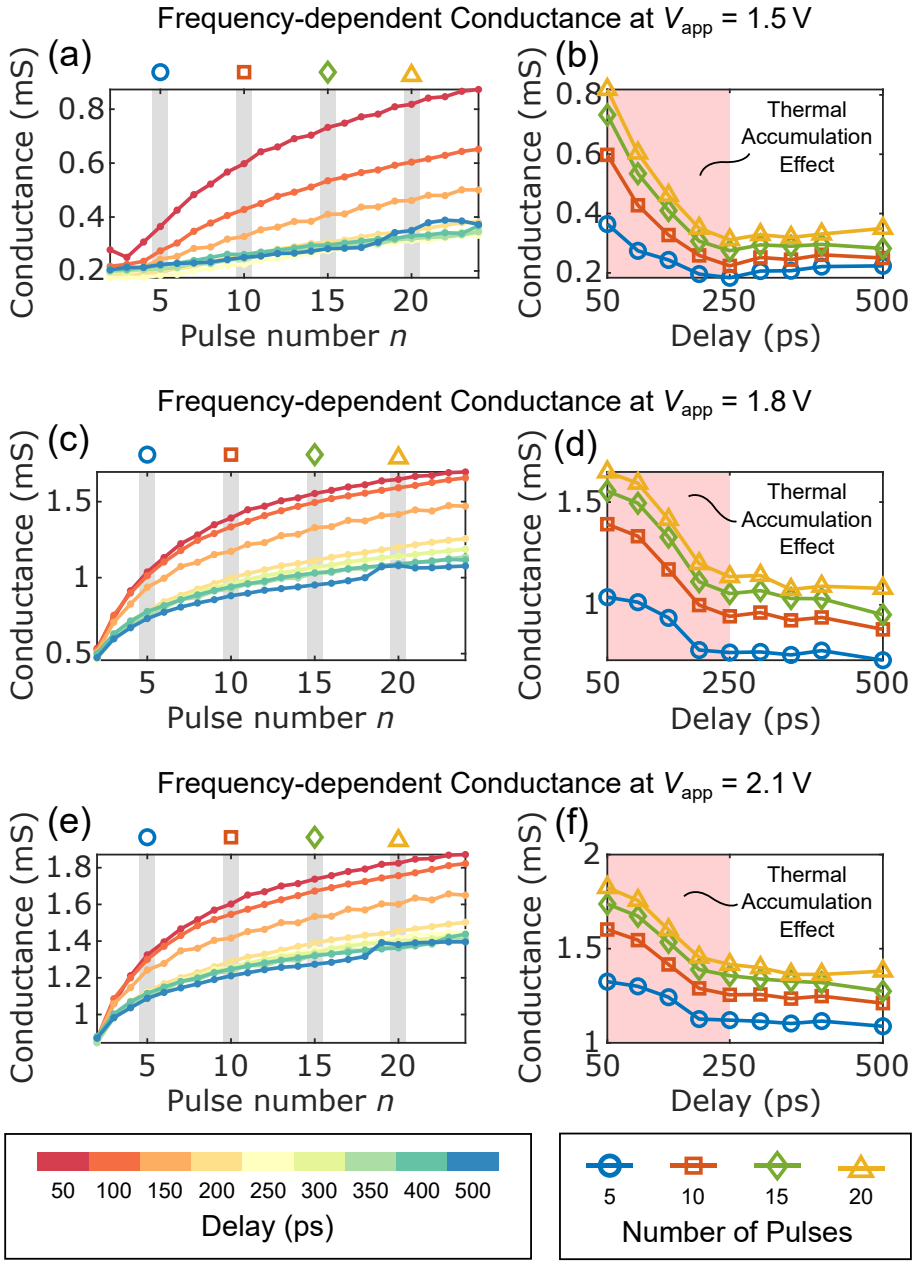


Figure 5.9: (a)-(f) show the delay-dependent conductance during pulse application for the applied voltages 1.5 V, 1.8 V, and 2.1 V. On the left, the mean conductance values from a series of measurements are shown as a function of pulse number for delay times ranging from 50 ps to 500 ps. On the right, the conductance values after four selected pulse numbers (5, 10, 15, and 20) are plotted as a function of the delay time to emphasize the thermal accumulation effect. Reproduced from Schön *et al.* [137], © 2025 The Authors, licensed under CC BY 4.0.

in the conductive filament region that temporarily raises the device temperature. When the delay between consecutive pulses is very short, the heat from the previous pulse does not fully dissipate before the next pulse arrives. As a result, the device remains in a slightly elevated temperature state, which lowers the energy barrier for subsequent ion migration and accelerates the switching process. For longer delays, the device has sufficient time to cool back toward its baseline temperature between pulses. In this case, each pulse starts from comparable thermal conditions, and the influence of residual heating from previous pulses becomes negligible. Consequently, the switching dynamics are primarily determined by the applied electrical stress rather than by thermal accumulation. The transition between these two behaviors occurs at delays of approximately 250 ps, which corresponds to the characteristic thermal relaxation time of the device under the investigated conditions.

Finally, these measurements demonstrate that the pulse amplitude, together with the delay between consecutive pulses, determines the accessible conductance window and affects the linearity of the conductance evolution. For example, the final conductance at 1.5 V is lower than at 1.8 V, which in turn is lower than at 2.1 V, as expected for increasing pulse amplitude. This demonstrates that by carefully adjusting the pulse amplitude together with the delay between consecutive pulses, gradual and controlled conductance changes can be achieved. At the same time, Figure 5.9(a)-(e) highlights why reliable evaluation methods are essential. Without separating the device current from capacitive contributions and noise, the gradual increase in conductance and its dependence on the pulse delay would not be visible on such short timescales.

These results show that temperature acts as a second state variable in TaO_x-based VCM devices, in addition to the applied electric field, since the residual heat from one pulse directly affects the switching dynamics of the next. This thermal contribution enables frequency-dependent potentiation and STP, which are important features for mimicking adaptive synaptic behavior in neuromorphic computing [137].

5.4. Short-Term Synaptic Plasticity in VCM Devices

Having established that pulse delay plays a crucial role in modulating thermal effects and switching dynamics in VCM devices (Section 5.3), this section extends the investigation of the same dataset to biologically inspired synaptic behaviors: PPF and PTP, as defined in Section 2.6.1. While these STP phenomena have been widely demonstrated in memristive systems at millisecond to microsecond timescales [129, 138, 139], their behavior at sub-ns scales has remained unexplored prior to this work. The PPF and PTP metrics are widely used to benchmark STP in memristive synapses, as they provide a compact and quantitative description of rate-dependent conductance modulation. As discussed in Section 2.6.1, in biological synapses, these rate-dependent responses originate from the dynamics of calcium ions in the presynaptic terminal [21–23]. After a spike, the calcium concentration decays

gradually, and if a second spike arrives before the calcium level has returned to baseline, the residual calcium adds to the new influx, producing an enhanced postsynaptic response (PPF). Under repeated stimulation, calcium accumulates across multiple spikes, resulting in the prolonged enhancement characteristic of PTP. In oxide-based memristors operating as second-order devices, analogous interactions arise from thermal accumulation effects [24], where residual device heating from preceding pulses modulates the response to subsequent stimuli. Using the evaluation methods from Section 5.2, this section examines how ultra-fast resistive switching in TaO_x-based VCM devices reproduces these fundamental synaptic functions at sub-ns timescales.

Paired-Pulse Facilitation (PPF)

PPF describes short-term synaptic enhancement that depends on the temporal spacing between stimuli, reflecting the device immediate response to closely spaced pulses through transient thermal dynamics. Figure 5.10 shows PPF values as a function of the pulse delay for applied voltages of 1.5 V, 1.8 V, and 2.1 V, calculated from conductance changes induced by the first two consecutive pulses.

The data show that the PPF decreases with increasing delay. This trend is most pronounced at an applied voltage of 2.1 V, where strong facilitation is observed for short delays and decreases as the delay increases. The observed delay dependence is consistent

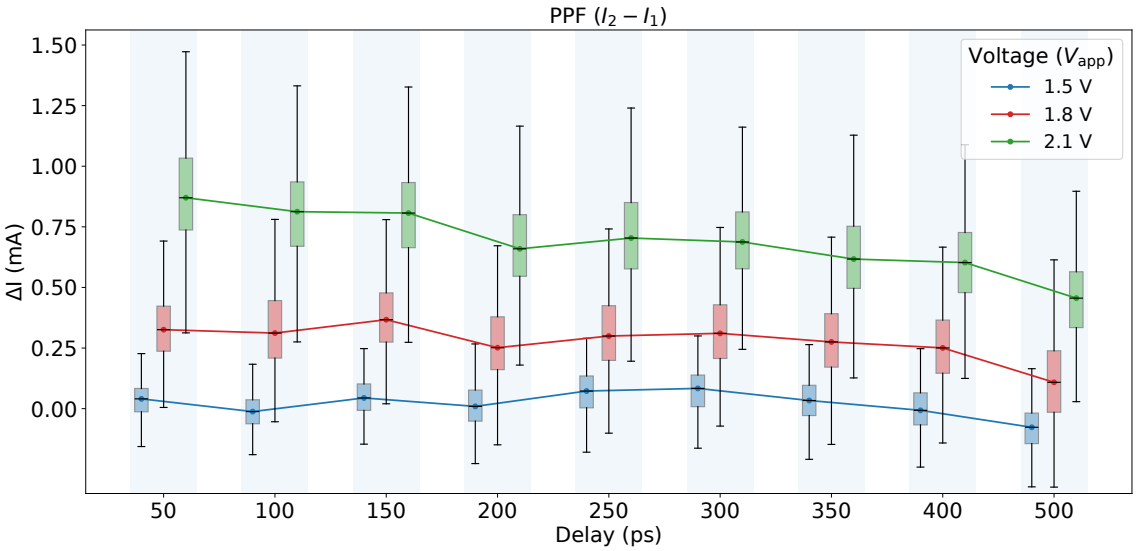


Figure 5.10: Delay dependence of PPF extracted from TaO_x devices for a pulse width of 100 ps at an applied voltage of 1.5 V, 1.8 V, and 2.1 V. The delay between successive pulses was varied from 50 ps to 500 ps. Each box represents the distribution obtained from 500 repeated measurement cycles, with conductance values extracted using the reference method. As can be seen, the PPF values decrease with increasing delay, most prominently at 2.1 V, whereas only a minor change is observed at 1.5 V. A dependence of the PPF values on the applied pulse voltage is observed, with higher voltages yielding higher PPF values. Data taken from [137].

with the fundamental characteristics of PPF discussed in Section 2.6.1 and illustrated in Figure 2.11, where biological PPF is strongest for closely spaced stimuli and decays with increasing inter-stimulus interval. At lower voltages, this decay in PPF weakens significantly. At 1.8 V, only a slight decrease in PPF with increasing delay is observed, while at 1.5 V, the decay of PPF is almost negligible over the investigated delay range. This occurs because lower voltages fail to induce measurable conductance changes within the first few pulses at such short pulse widths. As a result, the PPF decay is barely observable at these lower voltages when evaluated over the first two pulses.

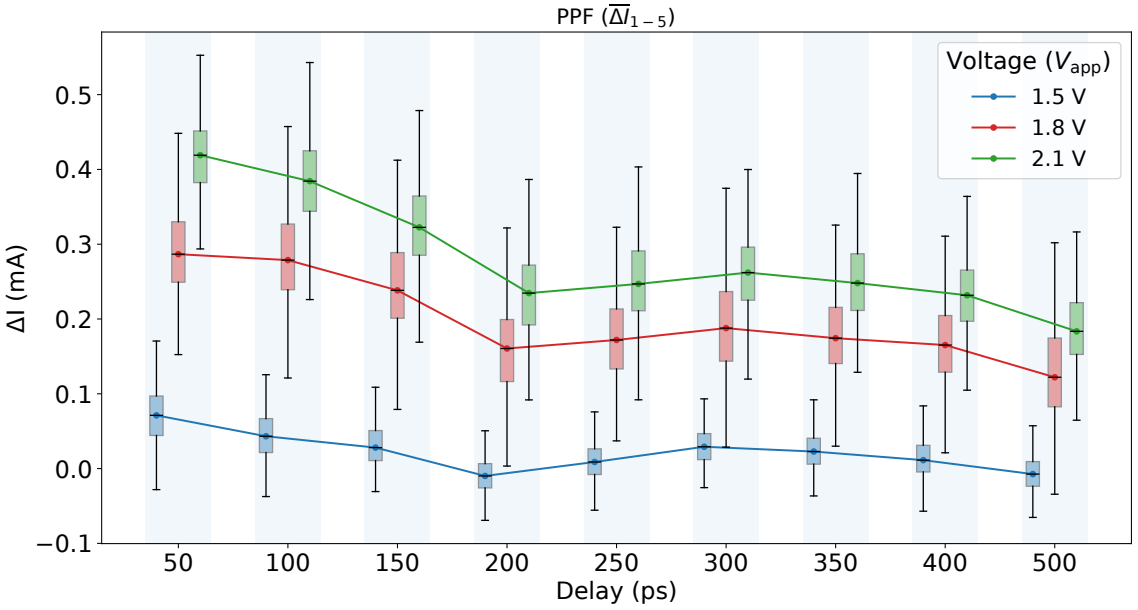


Figure 5.11: PPF as a function of pulse delay for applied voltages of 1.5 V, 1.8 V, and 2.1 V. The PPF is obtained from the incremental current changes (ΔI) over the first five pulses. The decay in PPF with increasing delay is visible at all voltages, with the effect being most pronounced at 2.1 V. Data taken from [137].

To better capture the PPF at lower pulse amplitudes, the analysis was extended to the first five pulses. In this case, the PPF is calculated as the average incremental conductance change between successive pulses, defined as:

$$\mathrm{PPF} = \frac{1}{5}\sum_{i=1}^{5}\Delta I_i, \tag{5.5}$$

where $\Delta I_i = I_{i+1} - I_i$. The results are shown in Figure 5.11. This figure shows that, when PPF is evaluated using the average incremental conductance change (Equation 5.5), a decay with increasing delay becomes visible not only at 2.1 V, but also at 1.8 V and, to a lesser extent, at 1.5 V. This demonstrates that STP occurs even at lower voltages when evaluated over multiple pulses, with PPF values decreasing as the delay increases.

In addition to the delay dependence, PPF exhibits pronounced voltage dependence. For instance, at a delay of 50 ps, the PPF value is lowest at 1.5 V and increases with pulse

amplitude, reaching its highest value at 2.1 V. This amplitude dependence arises from enhanced Joule heating [133] at higher voltages, producing larger transient temperature rises and stronger conductance modulation. This behavior is observable in both PPF evaluations, as shown in Figure 5.10 and Figure 5.11.

Post-Tetanic Potentiation (PTP)

In biological systems, PTP results from prolonged stimulation, producing enhancement through accumulated presynaptic calcium [22, 23]. Similarly, in memristive devices, PTP can arise from thermal accumulation, where closely spaced pulses produce cumulative heating that enhances the device response. Since thermal dynamics in TaO_x-based devices act analogously to calcium dynamics in biological synapses, it is of interest to investigate whether PTP can be observed at sub-ns timescales.

To investigate this, PTP was evaluated from the current increase between the first pulse and the final (25th) pulse of the train. The results are shown in Figure 5.12. The figure shows that PTP values are highest for short delays and decrease as the delay between pulses increases, a behavior present across all three applied voltages (1.5 V, 1.8 V, and 2.1 V). At longer delays, only a minor further decrease in PTP is observed, indicating that the influence of thermal effects is reduced as the device has more time to cool between consecutive pulses. Similar to PPF, PTP is stronger at higher pulse amplitudes due to increased Joule heating at higher voltages, which leads to larger transient temperature rises and stronger conductance modulation.

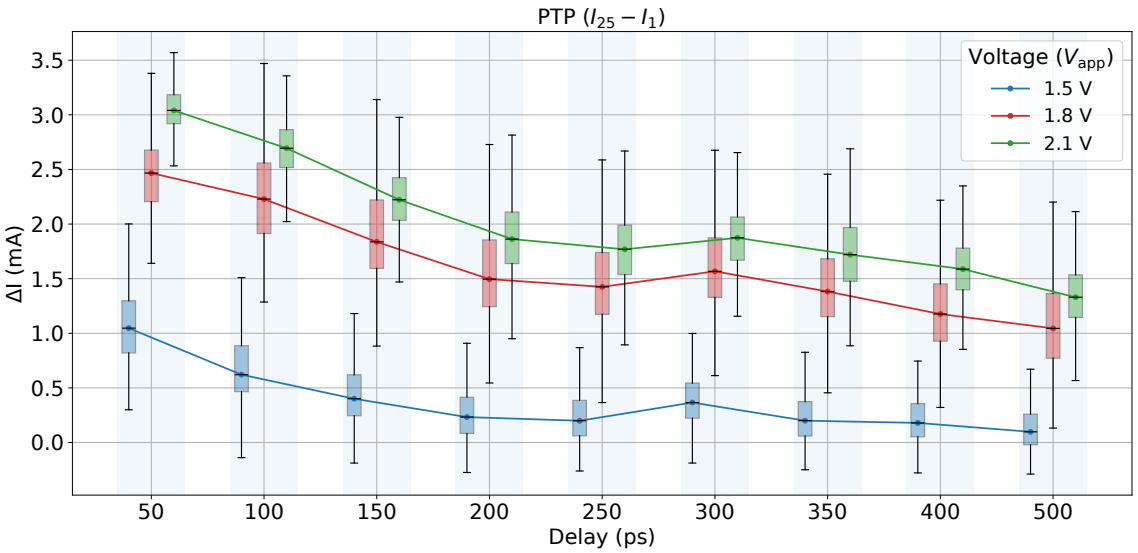


Figure 5.12: PTP as a function of pulse delay for applied voltages of 1.5 V, 1.8 V, and 2.1 V. The PTP values are highest at short delays and decrease as the delay increases, with only a minor further reduction at longer delays. Higher pulse amplitudes result in larger PTP values, reflecting increased electrical stress and thermal effects. Each box represents the distribution obtained from 500 repeated pulse sequences. Data taken from [137].

The demonstrated ability to modulate both PPF and PTP through pulse timing and amplitude at sub-ns timescales highlights the capability of TaO_x-based VCM devices to support high-frequency synaptic functionalities. These results provide experimental evidence that thermal accumulation supports biologically relevant synaptic functions at timescales shorter than previously demonstrated. In this context, the internal temperature dynamics enable activity-dependent plasticity without requiring overlapping pulses or specially engineered spike shapes [124], validating the interpretation of temperature as a Ca^{2+}-like internal state variable and supporting the classification of oxide-based memristors as second-order memristive devices [24, 136].

5.5. Conclusion

In this chapter, the switching behavior of TaO_x-based VCM devices was investigated under short pulses and delays at sub-ns timescales. At these timescales, conventional DC read operations between pulses are not feasible, requiring dedicated evaluation methods to extract conductance evolution from transient electrical responses during pulse application.

To address this limitation, two methods were developed to reconstruct the device conductance from the measured transient responses: the reference method and the integration method [153].

The reference method determines the device conductance during ultra-fast pulse measurements by subtracting the capacitive contributions of the measurement setup from the device current. Since the transient response contains both capacitive and conductive components, an additional non-switching pulse train is applied to capture the capacitive response. By subtracting this contribution from the switching measurement, the remaining response represents the device current, allowing the conductance to be determined for each pulse. This method provides a reliable extraction of conductance states for short pulse delays and pulse widths. However, it requires additional reference measurements and precise temporal alignment between switching and non-switching traces, particularly for very short pulse widths where even small horizontal shifts can significantly affect the extracted device current.

Alternatively, the integration method determines the device conductance by integrating the measured transient response over a defined pulse window, such that capacitive charging and discharging components cancel each other out. This method requires no additional measurements and can be directly applied to the measured transient response. A limitation arises at very short pulse delays, where the device does not fully discharge before the arrival of the next pulse. In this case, residual charge leads to an overestimation of the charge associated with the first pulse. For longer pulse widths and delays, the device is fully discharged within the pulse window, and this method provides a more reliable determination of the conductance state. Although the two methods differ in their imple-

mentation, they yield similar switching trends and conductance values, differing mainly by scaling factors. The choice between the reference method and the integration method should therefore be based on the specific requirements of the experiment, including the applied pulse width and pulse delay. These evaluation methods bridge the gap between the microsecond-to-nanosecond regime studied experimentally [24] and the sub-ns predictions from electrothermal simulations [25]. Without such methods, the conductance evolution during ultra-fast pulse application would remain inaccessible to experimental investigation, as the capacitive charging and discharging dominate the measured signal and obscure the device's true conductive response at these timescales.

Using these evaluation methods, the delay-dependent switching behavior of TaO_x-based VCM devices was studied at sub-ns timescales. The results showed that when the pulse delay was short, the device conductance increased rapidly with pulse number due to thermal accumulation, as the device does not fully cool between closely spaced pulses [137]. This elevated temperature lowers the activation barrier for oxygen vacancy migration and enhances the conductance change induced by subsequent pulses. For longer pulse delays, the device has sufficient time to thermally relax, and the switching behavior becomes largely independent of pulse spacing, being primarily determined by the applied pulse parameters. For the TaO_x devices studied in this work, thermal accumulation was observed for pulse delays shorter than approximately 250 ps, corresponding to the characteristic thermal relaxation time, consistent with electrothermal simulation studies [25]. Above 250 ps, the device conductance was no longer influenced by thermal effects and depended mainly on the applied pulse amplitude. These observations confirm that temperature acts as a second-order state variable in TaO_x-based VCM devices, providing an internal timing mechanism that modulates the switching response based on recent activity [137].

The delay-dependent conductance modulation arising from thermal accumulation further enables TaO_x-based VCM devices to exhibit short-term synaptic plasticity. Since the device temperature does not immediately return to equilibrium after pulse application, the response to subsequent pulses depends on recent activity, resembling the behavior of biological synapses [21, 23]. In this work, STP was evaluated using PPF and PTP. Both synaptic behaviors were observed and found to depend on pulse delay and applied voltage. For PPF, the facilitation decreased with increasing pulse delay, with the strongest effect occurring at higher pulse amplitudes. At lower voltages, the PPF decay was weak when evaluated using only the first two pulses, but became visible when the conductance change was evaluated over the first five pulses, indicating that STP remains present even when the initial conductance change is small. Similarly, PTP values were highest for short pulse delays and decreased with increasing delay, with higher voltages producing stronger potentiation due to enhanced Joule heating.

The demonstrated PPF and PTP extend the experimental validation of STP phenomena [129, 138, 139] from millisecond-to-microsecond timescales down to the sub-ns regime.

Unlike first-order memristor implementations that require overlapping pulses or specially engineered spike shapes [124], the thermal accumulation mechanism provides an internal timing mechanism analogous to calcium ion dynamics in biological synapses [21–23]. These results confirm simulation predictions [25] regarding thermal accumulation at sub-ns timescales, extend earlier experimental work at longer timescales [24], and validate the theoretical framework of second-order memristive devices [124], in which temperature serves as a Ca^{2+}-like internal state variable.

6. Electrical Characterization of PCM Devices

Electrical switching in PCM relies on reversible transitions between amorphous and crystalline phases induced by electrical pulses [26, 27]. While the physical mechanisms underlying SET crystallization and RESET amorphization are well established [27, 45], the temporal evolution of these processes under ultra-fast electrical excitation remains insufficiently understood. In particular, how phase-change dynamics evolve when pulse durations approach the sub-ns regime is still an open experimental question.

Previous studies have shown that PCM switching is governed by thermally activated processes such as nucleation, crystal growth, and melt-quench amorphization [27, 48, 49]. However, most experimental investigations have focused on nanosecond or longer timescales, where only the final resistance state after programming is typically accessible. As a consequence, intermediate switching dynamics that determine variability and reproducibility are often obscured, making it difficult to experimentally distinguish between nucleation-dominated and growth-dominated crystallization during electrical operation [28, 48, 49].

Addressing these limitations requires experimental setups capable of applying well-defined electrical pulses while resolving resistance changes over very short timescales and across a wide resistance range. In particular, reliable access to the high-resistance amorphous state during ultra-fast RESET operation remains challenging due to leakage currents and measurement constraints [47]. Although RESET switching down to 200 ps has been reported in GST-based cells [8], these experimental challenges have limited systematic studies of switching kinetics and access to highly resistive amorphous states in the sub-100 ps regime.

In this context, the present chapter investigates the SET and RESET switching kinetics of PCM devices under controlled electrical excitation conditions. By systematically varying pulse amplitude and duration using a dedicated RF measurement setup, the experiments aim to explore how ultra-fast electrical stimuli influence phase-change dynamics and whether distinct kinetic regimes can be accessed. The following sections describe the experimental methods and present the measurements performed to address these questions.

6.1. Experimental Methods

The experimental investigations in this chapter were conducted using RF Setup 2, developed within the scope of this thesis and described in Section 3.1.2. Unlike RF Setup 1, this setup uses an RF switch instead of a bias tee for signal routing, enabling automated measurements and suppressing leakage currents that can become significant when devices operate in the megaohm resistance range. RF Setup 2 integrates multiple signal sources, including an AWG, a PG5 pulse generator for ultra-short pulses in the sub-ns regime, and an SMU for DC operations (see Section 3.1 for detailed specifications of these components). The RF switch enables automated routing between these sources, while an oscilloscope is used to capture the transmitted pulse responses. The AWG provides precise control over pulse parameters, including amplitude, width, and programmable rise and fall times down to 2 ns, enabling systematic investigation of the influence of pulse shaping on the switching kinetics of PCM devices.

Device Samples

The PCM devices investigated in this work were provided by Yiming Zhou. The device stack consists of a SnTe-doped In_3SbTe_2 chalcogenide film (hereafter denoted as SIST) with doping concentrations of 10% or 40% SnTe, sandwiched between bottom and top TiN electrodes and integrated into a CPW structure to ensure accurate high-speed signal transmission. The thickness of each layer is summarized in Table 6.1. A detailed description of the device design, fabrication process, and material properties is provided in Zhou [30].

Table 6.1: Layer thickness of the PCM device

Material	**TiN**	**SiO_2**	**In_3SbTe_2–SnTe (90:10 / 60:40)**	**TiN**	**Pt**
Thickness [nm]	30	30	50	25	45

6.1.1. Measurement Procedures

Before performing any measurements, each PCM device undergoes an initialization procedure to verify its functionality and to stabilize the switching behavior. This initialization step consists of repeatedly cycling the device between the amorphous and crystalline states by applying 100 RESET and SET pulses using the AWG. The pulse parameters used for device initialization are summarized in Table 6.2. This procedure ensures reproducible switching characteristics. After successful initialization, separate measurement procedures were carried out to investigate the SET and RESET behavior of the PCM devices, as described in the following.

Table 6.2: RESET and SET parameters used for the initialization procedure

Parameter	**RESET pulse**	**SET pulse**
Amplitude	5 V	2.3 V
Rise time t_r	2 ns	100 ns
Pulse duration t_{dur}	10 ns	500 ns
Fall time t_f	2 ns	500 ns

SET Measurement Procedure

The SET behavior of the PCM was investigated by systematically varying the SET pulse amplitude and duration, while the RESET pulse parameters were kept constant throughout the measurements. The electrical parameters used during the SET measurements are summarized in Table 6.3. While the SET pulse amplitude and duration were systematically varied within the specified ranges, the rise and fall times, RESET conditions, and readout parameters were kept constant to ensure reproducible and comparable switching behavior.

Table 6.3: Electrical parameters applied during SET measurements

Parameter	**Applied value(s)**
SET pulse amplitude	0.5 V - 4 V
SET rise/fall time t_r, t_f	2 ns
SET pulse duration t_{dur}	2 ns - 1000 ns
RESET pulse amplitude	5 V
RESET pulse duration	10 ns
RESET rise/fall time	34.5 ps
Read voltage V_{read}	0.2 V
Maximum sweep voltage	5 V
Sweep rate	0.5 V/s

The SET measurement procedure follows the steps shown in Figure 6.1:

(i) **Pre-RESET read**: Determine the device resistance in the LRS using the SMU.

(ii) **RESET**: Apply a RESET pulse using the pulse generator (PG5).

(iii) **Pre-SET read**: Determine the resistance of the device in the HRS using the SMU.

(iv) **SET**: Apply a SET pulse with defined amplitude and duration using the AWG.

(v) **Post-SET read**: Determine the resistance of the device after the SET operation using the SMU.

(vi) **Sweep**: Apply a DC sweep using the SMU to bring the device back to the LRS.

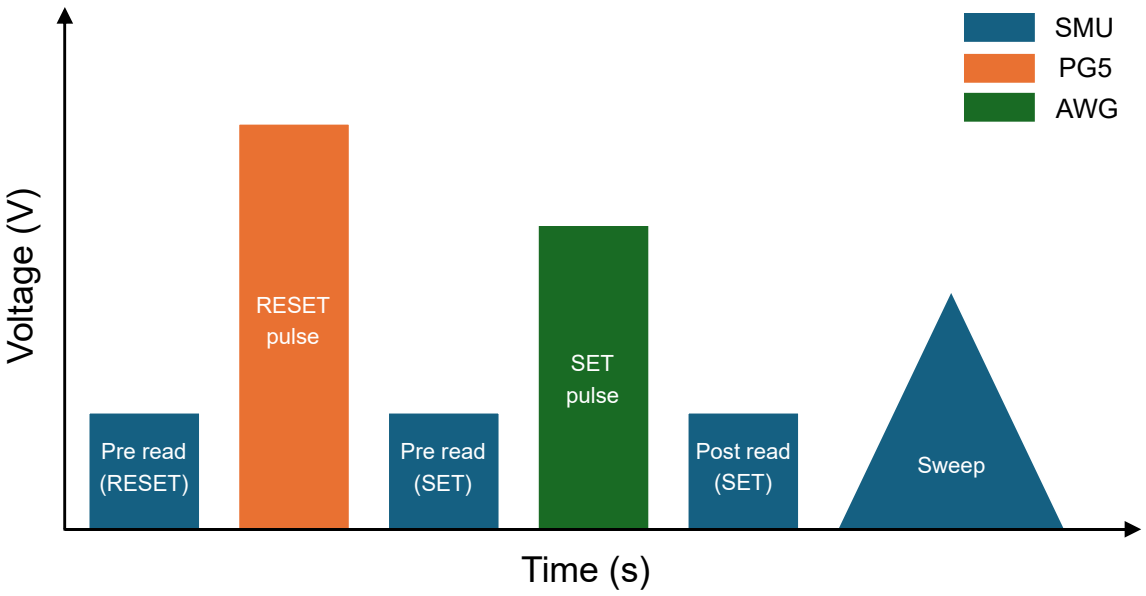


Figure 6.1: Schematic of the SET measurement cycle. The sequence includes pre-RESET read with the SMU, application of a RESET pulse with fixed parameters using the PG5, pre-SET read with the SMU to verify HRS, application of a SET pulse with variable amplitude and duration using the AWG, post-SET read with the SMU, and a final DC sweep with the SMU to fully restore the device to LRS.

RESET Measurement Procedure

During the RESET measurements, the RESET kinetics of the PCM devices were characterized in the sub-250 ps range. At these timescales, pulses generated with a PG5 operating at a fixed output voltage of 2.5 V were insufficient to reliably switch the device into the HRS. Therefore, a PG5 operating at a fixed output voltage of 5 V was used for this characterization. The voltages discussed below refer to the effective voltage at the device. In this configuration, external attenuators were used to adjust the RESET pulse amplitude.

The electrical parameters applied during the RESET measurements are summarized in Table 6.4. During the measurements, the SET and readout conditions are kept constant, while only the RESET pulse parameters are systematically varied. Each RESET measurement cycle consists of the following steps:

(i) **Pre-RESET read**: The resistance of the device in the crystalline LRS is measured using the SMU.

(ii) **RESET pulse**: A RESET pulse with the selected pulse width is applied using the PG5.

(iii) **Post-RESET read**: The resistance after the RESET pulse is measured using the SMU to determine whether the device has switched to HRS.

(iv) **SET pulse**: A SET pulse with fixed parameters is applied using the AWG to return the device to the crystalline LRS before the next cycle.

The complete measurement cycle was repeated multiple times to ensure statistical reliability of the results.

Table 6.4: Electrical parameters applied during RESET measurements

Parameter	**Applied value(s)**
SET pulse amplitude	1.8 V
SET rise / fall time t_r, t_f	2 ns
SET pulse duration t_{dur}	500 ns
RESET pulse amplitude	7 V - 10 V
RESET pulse width	50 ps - 250 ps
Read voltage V_{read}	0.2 V

6.2. SET Switching Kinetics

To investigate the SET switching kinetics, measurements were performed based on the SET measurement procedure described previously in Section 6.1.1. In this measurement sequence, all DC operations and RESET pulse parameters were kept constant according to the values listed in Table 6.3, while only the SET pulse parameters were systematically varied. Figure 6.2 presents a representative example of this measurement sequence.

Each measurement sequence started with the device initialized in the LRS. A RESET pulse was then applied, switching the device into the HRS. Then, a SET pulse with specific parameters was applied, followed by a resistance readout to determine the device state. Finally, a DC sweep was performed to initialize the device to the LRS before the next cycle, as illustrated in Figure 6.2(a–e). In this particular example, the SET voltage was fixed at 1.8 V, while the pulse width was varied from 2 ns to 100 ns across successive cycles.

As observed in Figure 6.2(a), the device starts each cycle from the LRS with a resistance of approximately 1.2 kΩ to 1.5 kΩ. Following the application of the RESET pulse (Figure 6.2(b)), the device switches to the HRS, exhibiting a mean resistance of around 710 kΩ, as indicated by the red inverted triangles in Figure 6.2(c). The subsequent SET pulse (Figure 6.2(d)) application reveals distinct switching behavior depending on the pulse duration. At a SET voltage of 1.8 V, short pulse durations of 2 ns do not induce a transition back to the LRS, as evident from the green triangles in Figure 6.2(c), where the resistance remains in the HRS. This behavior indicates that the applied energy is insufficient to induce crystallization at such short timescales [46, 47]. Similar non-switching behavior is observed for pulse durations up to 20 ns. However, when the pulse duration is increased to 50 ns, the device successfully transitions to the LRS, demonstrating that this pulse duration provides sufficient energy to induce the amorphous-to-crystalline phase transition.

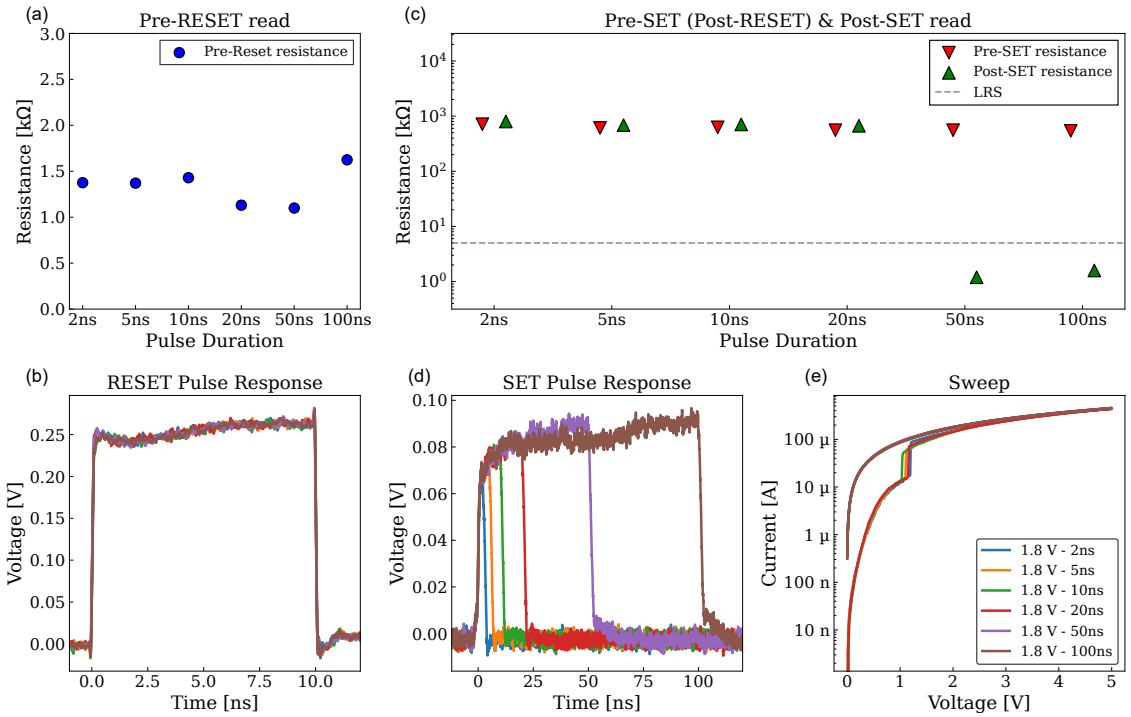


Figure 6.2: Electrical characterization of 10% SIST device at a fixed SET amplitude of 1.8 V and varying pulse durations. Each subfigure corresponds to a measurement step outlined in Figure 6.1. Panels (a)-(d) show the resistance evolution and transient voltage responses during RESET and SET operations, while (e) presents the post-SET DC sweep.

To further investigate the influence of pulse amplitude on SET switching kinetics, an additional measurement series was performed following the same procedure as described above, with the SET pulse amplitude increased to 3.0 V. All other parameters, including the DC operations and RESET pulse conditions, were kept identical, allowing for a direct comparison of the SET kinetics as a function of pulse amplitude and pulse duration.

As illustrated in Figure 6.3(c), the post-SET resistance exhibited a systematic dependence on the applied pulse duration. At 2 ns, the device retained the HRS, with no observable transition to the LRS. Upon increasing the pulse duration to 5 ns and 10 ns, the resistance decreased progressively to intermediate levels of approximately 151 kΩ and 39.8 kΩ, respectively, reflecting partial crystallization within the amorphous region. For pulse durations of 20 ns and longer, complete crystallization was achieved, as evidenced by the device reaching the LRS characteristic of the fully crystalline phase.

These results demonstrated a clear dependence of crystallization on the combined effect of pulse amplitude and pulse duration. At the lower voltage of 1.8 V (Figure 6.2), pulse durations of at least 50 ns were required to induce a transition to the LRS. In contrast, increasing the voltage to 3.0 V enabled the device to reach the LRS at significantly shorter pulse durations of 20 ns. This behavior arose because higher voltages generate stronger Joule heating, allowing the active region to reach the crystallization temperature within a shorter time window [47, 48]. These preliminary measurements motivated a more detailed

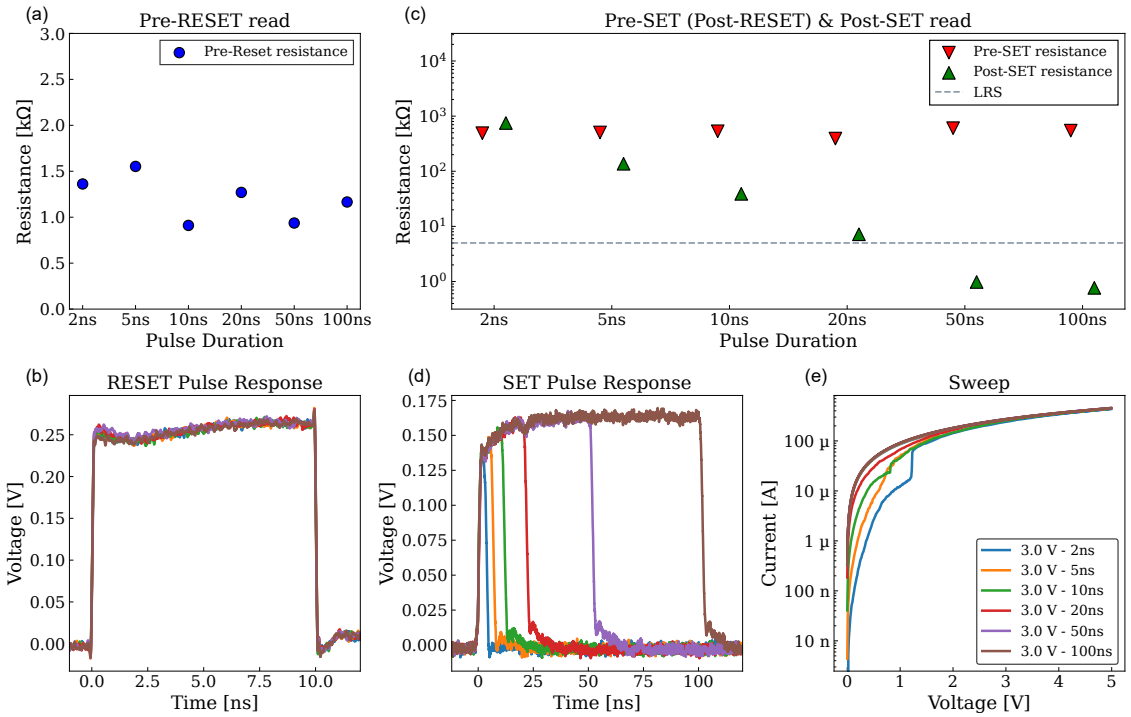
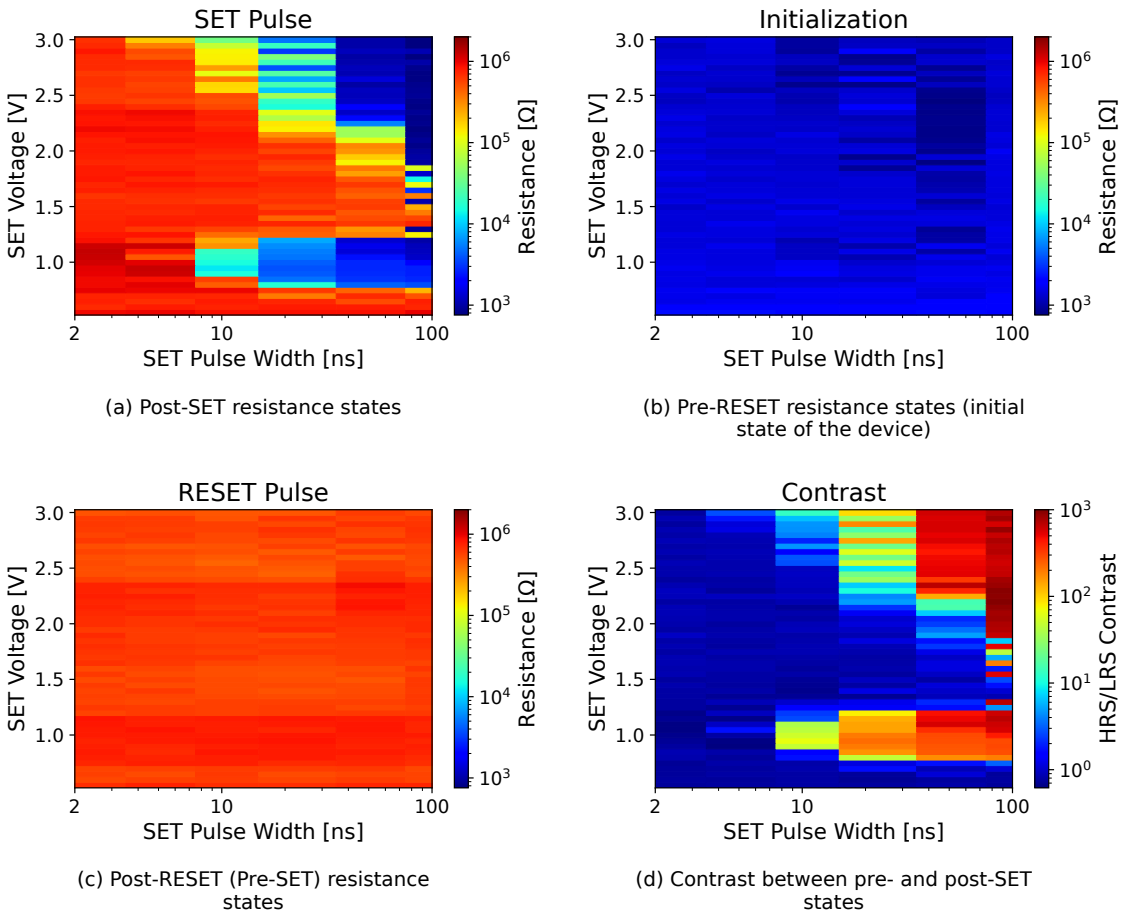


Figure 6.3: Electrical characterization of 10% SIST device at a SET amplitude of 3.0 V for different pulse durations; (e) shows the post-SET *I-V* sweep.

analysis of SET switching kinetics in the following section, with particular focus on distinguishing nucleation-dominated and growth-dominated crystallization regions.

To analyze the SET switching behavior observed in the exemplary measurements, the same SET measurement procedure was applied systematically across a wide range of pulse amplitudes and pulse durations. The SET kinetics of 10% SIST devices are presented in heat maps (Figure 6.4), where the SET pulse duration varies along the horizontal axis, and the SET pulse amplitude varies along the vertical axis. Each data point represents the mean resistance calculated from five measurements conducted with identical parameters to ensure statistical reliability. The post-SET resistance heat map shown in Figure 6.4(a) reveals the parameter combinations under which switching occurs, with the LRS marked in blue and the HRS marked in red. The initialization map in Figure 6.4(b) and the post-RESET map in Figure 6.4(c) confirm that the device starts each measurement cycle from the LRS and is RESET to the HRS prior to each SET pulse. The contrast map shown in Figure 6.4(d) highlights successful switching events through high contrast values, providing a complementary visualization of the SET switching behavior.

As shown in Figure 6.4(a), three distinct regions can be identified in the switching behavior. At low voltages below approximately 0.8 V, the device remains in the HRS regardless of pulse width. This lower boundary at around 0.8 V corresponds to the threshold voltage [46], which represents the minimum voltage required to trigger threshold switching and enable sufficient current flow for crystallization. Above this threshold, a first switching



(a) Post-SET resistance states

(b) Pre-RESET resistance states (initial state of the device)

(c) Post-RESET (Pre-SET) resistance states

(d) Contrast between pre- and post-SET states

Figure 6.4: SET switching kinetics of a 10% SIST device (3-DIE-03-C2, R2C2) visualized as resistance heat maps as a function of SET pulse duration (2 ns to 100 ns) and SET pulse amplitude (up to 3.0 V). (a) show post-SET resistance, (b) pre-RESET resistance, (c) post-RESET resistance, and (d) the resulting resistance contrast.

region appears between approximately 0.8 V and 1.2 V, where the device successfully transitions to the LRS for pulse widths of 20 ns and longer.

Between approximately 1.2 V and 2.0 V, a non-switching region is observed in Figure 6.4(a), in which the device fails to reach the LRS despite voltages exceeding the threshold. In this intermediate regime, the applied voltage is sufficient to induce threshold conduction but does not generate a temperature high enough to sustain deterministic nucleation and subsequent crystal growth. Instead, the moderate Joule heating may promote structural relaxation and resistance drift within the amorphous phase, phenomena widely reported in PCM devices [28, 45], without meeting the kinetic conditions required for stable crystallization. As a result, the device remains trapped in a metastable amorphous state, giving rise to an apparent forbidden operational window for reliable SET switching.

At higher voltages above approximately 2.0 V, a second switching region emerges in Figure 6.4(a), in which successful SET transitions are again achieved. In this regime, the switching behavior exhibits a strong dependence on both the applied voltage and the pulse width. A pronounced reduction in resistance is observed for pulse widths as short

as 5 ns. The transition from switching to non-switching conditions in this high-voltage region occurs gradually as the pulse width is reduced, with intermediate resistance states appearing near the boundary. This gradual transition reflects the continuous nature of the crystallization process and its dependence on the total energy delivered to the device. These observations further suggest that applying voltages above 3 V may enable SET switching at even shorter pulse durations.

The distinct separation between the switching regions observed in the heat maps indicates that the crystallization behavior of the device depends strongly on the applied electrical conditions. Such a pronounced dependence on pulse amplitude and duration suggests that the underlying crystallization pathway changes across the range of applied pulse conditions, rather than being determined by a single uniform mechanism.

6.2.1. Analysis of Crystallization Mechanisms

As discussed in Section 2.2, PCM devices are known to exhibit crystallization kinetics that can be classified into nucleation-dominated and growth-dominated regimes [48, 49], which are characterized by fundamentally different temporal and statistical behavior. This observation raises the question of whether the different switching regions identified in the heatmaps (Figure 6.4) correspond to distinct crystallization pathways accessed under different electrical excitation conditions.

To address this question, detailed transient measurements were performed on 30% SIST devices, enabling C2C analysis of the crystallization dynamics. For each SET pulse width, a sequence of voltage pulses with increasing amplitude was applied, and the device resistance was measured after each pulse. This procedure was repeated over multiple cycles to capture C2C variability. All SET pulse widths were defined using the full width at half maximum (FWHM), while the rise and fall times were kept constant. The analysis presented in this section was carried out by Yiming Zhou.

Figure 6.5 presents representative SET programming curves obtained for different SET pulse widths ranging from 4 ns to 22 ns. For each pulse width, multiple programming cycles are shown to illustrate both stochastic and deterministic aspects of the SET process. The resistance is plotted as a function of the applied SET voltage, allowing direct comparison of switching behavior across different pulse widths and cycles.

The SET programming curves shown in Figure 6.5 can be separated into four distinct regions as a function of applied voltage and pulse width, each corresponding to a different switching behavior.

In the first region (red background), corresponding to low applied voltages, the current flowing through the device remains insufficient to raise the active region to the crystallization temperature. As a result, the device remains in the HRS for all pulse widths, and no SET switching is observed.

In the second region, highlighted in green, where the applied voltage slightly exceeds the threshold switching voltage, abrupt resistance drops occur even for very short pulse widths. This region is characterized by pronounced stochastic behavior, with large C2C variations in the switching response. Such behavior reflects the probabilistic nature of nucleation [48, 49], where the formation of stable crystalline clusters occurs randomly. The probability of successful switching increases with pulse duration, consistent with the cumulative effect of stochastic nucleation over time.

In the third region, highlighted in blue and observed at higher applied voltages, a gradual and more reproducible switching behavior emerges. In this regime, the final resistance exhibits a strong correlation with pulse width, indicating that crystallization proceeds predominantly through crystal growth once nucleation has occurred [48, 49]. The reduced C2C variability observed in this region reflects the increasingly deterministic nature of growth-dominated crystallization.

In the fourth region, highlighted in orange and appearing at voltages above approximately 2.5 V, longer SET pulses with durations of 17 ns and 22 ns lead to an increase in

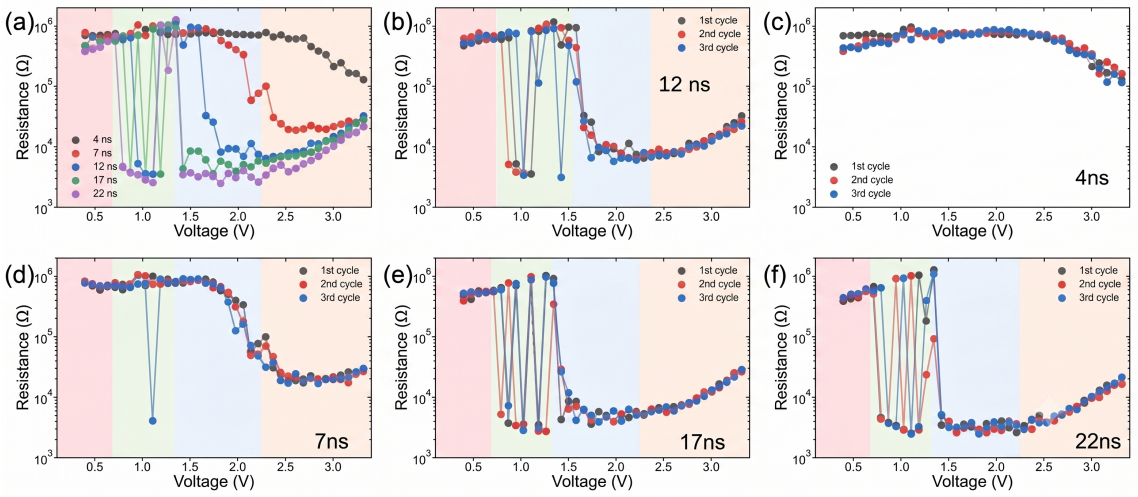


Figure 6.5: SET programming behavior of PCM devices under varying pulse widths. (a) shows resistance-voltage curves for pulse durations of 4 ns, 7 ns, 12 ns, 17 ns, and 22 ns, revealing four distinct switching regimes. The red region represents the low-voltage regime, where the applied voltage is below the threshold required for switching; thus, only a small current flows, and the cell remains in the HRS. The green region corresponds to voltages just above the threshold, where the device exhibits stochastic switching behavior, occasionally transitioning to the LRS even with short pulse widths. This randomness arises from the probabilistic nature of nucleation, where the likelihood of phase transformation increases with time. In the blue region, higher voltages lead to a gradual and more deterministic SET process, with the final resistance strongly dependent on the pulse width. Finally, the orange region corresponds to voltages above approximately 2.5 V, where longer pulses (17 ns and 22 ns) induce partial melting followed by quenching, resulting in increased resistance and RESET-like behavior. (b)-(f) present C2C comparisons for selected pulse widths, confirming the stochastic nature of switching at intermediate voltages and reduced variability at higher voltages. Reproduced from [30].

resistance rather than further reduction. This behavior suggests the occurrence of melting and RESET behavior [27, 44]. Figure 6.5(d-f) shows C2C comparisons of SET programming for pulse widths of 12 ns, 17 ns, and 22 ns. These measurements show that the intermediate-voltage region is characterized by the stochastic nature of nucleation, whereas SET switching at higher voltages is dominated by deterministic crystal growth.

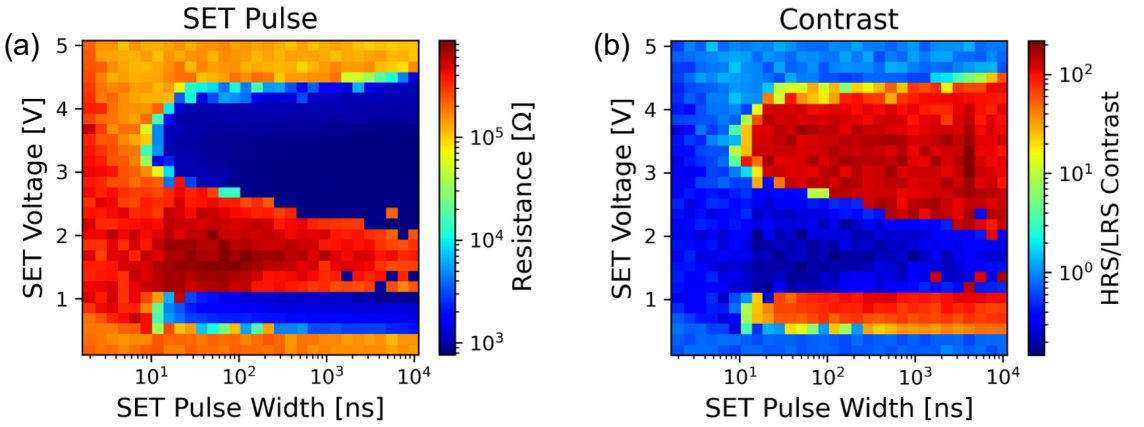


Figure 6.6: Heatmap representation of SET switching in a 10% SIST device. (a) Post-SET resistance versus SET pulse width and voltage. (b) Resistance contrast between the HRS and the post-SET state. Reproduced from [30], where the different measurement setup is described in detail.

Building on the insights gained from the detailed transient analysis of 30% SIST devices, the switching behavior observed in 10% SIST devices can be interpreted in terms of the underlying crystallization processes.

As a proof of concept, measurements on 10% SIST cells performed over a higher SET voltage range, shown in Figure 6.6, reveal a clear separation between a nucleation-growth mode and a pure growth mode of crystallization. The measurements employed electrical pulses with rise and fall times of 2 ns, consistent with RESET pulse conditions, thereby suppressing melt and slow cooling effects [44] and allowing the SET process to be dominated by crystallization dynamics.

The heatmaps in Figure 6.6 show two distinct switching regions after SET pulse application, similar to those observed in Figure 6.4, but measured over a higher SET voltage range. The low-voltage switching region corresponds to the nucleation-growth mode, in which the device can be switched to the LRS for pulse widths around 15 ns. This region is bounded by two characteristic cutoffs. The lower cutoff corresponds to the threshold voltage below which crystallization cannot be initiated due to insufficient current flow. The upper cutoff marks conditions where the device temperature exceeds the range favorable for stable nucleation. At voltages above this cutoff, pronounced resistance drift and aging effects occur, resulting in a non-switching region despite voltages exceeding the threshold.

At higher voltages, a second switching region emerges that corresponds to the pure growth mode of crystallization. In this regime, SET switching exhibits a clear dependence on both the applied voltage and the pulse width. For longer pulse durations, lower voltages are sufficient to induce switching, indicating that the total energy delivered to the device determines the crystallization kinetics. Under these conditions, nucleation occurs rapidly, and the switching behavior is governed primarily by the subsequent deterministic growth of crystalline regions. The gradual transition between switching and non-switching states at the boundaries of this region, accompanied by intermediate resistance values, reflects the continuous nature of the growth process and its dependence on the supplied pulse energy.

These proof-of-concept measurements confirm the interpretation of the switching regions observed in the 10% SIST devices and provide a consistent physical framework for distinguishing the nucleation-growth mode from the pure growth mode in SET operation.

6.2.2. Reproducibility of SET Switching Behavior

To confirm the reproducibility of the switching behavior observed in 10% SIST devices, identical SET measurements were performed on two additional devices from the same fabrication batch using RF Setup 2. The results for these devices are shown in Figure 6.7 and Figure 6.8. For comparison, the switching behavior discussed in Figure 6.4 was also obtained using RF Setup 2, whereas the data presented in Figure 6.6 were acquired using a different measurement setup and are described in detail in Zhou [30]. All devices measured using RF Setup 2 exhibit the same fundamental switching characteristics.

Figure 6.7 shows measurements performed over an extended voltage range up to 4.0 V, where additional switching behavior is observed at higher voltages. Starting from approximately 2.4 V, partial crystallization occurs even for short pulse durations of 2 ns, indicating that the increased voltage provides sufficient Joule heating to initiate crystallization within a very short time window. With further increases in voltage, a gradual reduction in resistance is observed, consistent with the increased energy delivered to the active region and the resulting enhancement of crystal growth.

Similar switching behavior is observed in the second device, as shown in Figure 6.8, which exhibits the same two dominant switching regions and the appearance of intermediate resistance states, particularly for short pulse durations such as 2 ns.

It should be noted that a difference is observed in the achievable HRS/LRS resistance ratio between the measurement setups. The measurements in Figure 6.6 show HRS/LRS ratios of approximately 10^2, while RF Setup 2 measurements (Figure 6.4 and 6.8) achieve ratios around 10^3. This difference results from the PG5 pulse generator's fast rise and fall times ($\sim$34.5 ps), which enable rapid quenching into highly resistive amorphous states, combined with RF Setup 2 capability to reliably measure high resistance values through RF-switch routing that suppresses leakage currents.

The consistent switching patterns observed across all devices confirm the reproducibility of the identified switching regimes and validate the robustness of the underlying crystallization mechanisms. These results demonstrate RF Setup 2 capability to characterize both nucleation-growth and pure growth regimes while accessing the highly resistive states required for comprehensive SET kinetics analysis.

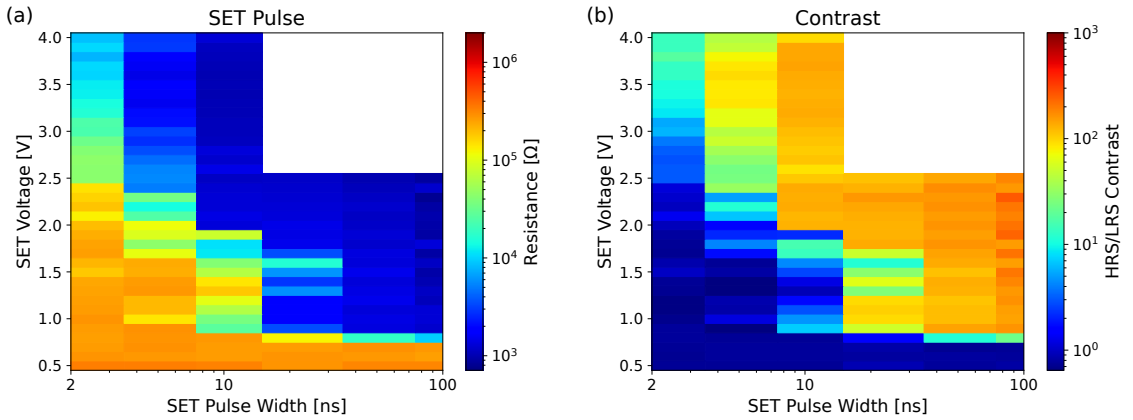


Figure 6.7: SET switching behavior of a 10% SIST device (3-DIE-03-C2, R2C1) over an extended SET voltage range up to 4.0 V and pulse durations from 2 ns to 100 ns.
(a) Post-SET resistance states showing progressive resistance reduction at higher voltages, even for 2 ns pulses. (b) Resistance contrast between pre- and post-SET states.

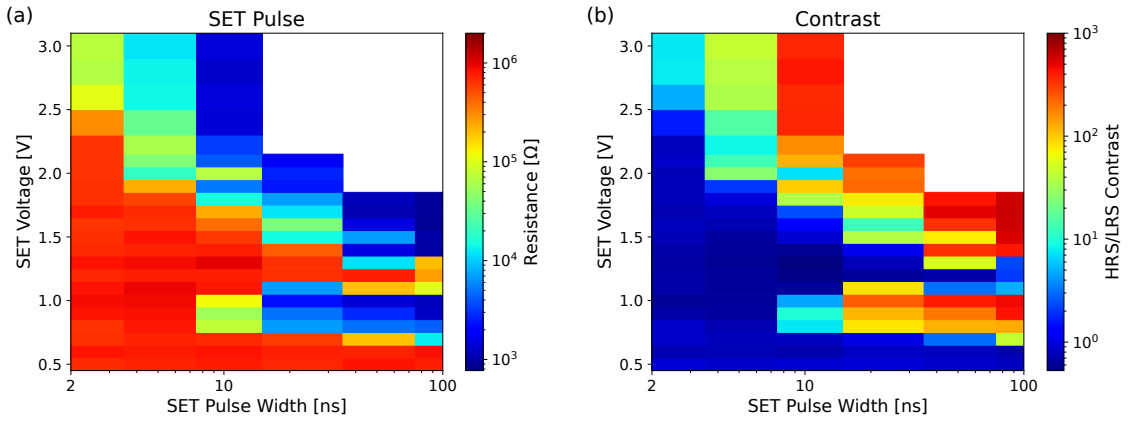


Figure 6.8: SET switching behavior of a 10% SIST device (3-DIE-03-C2, R1C2) measured over SET voltages up to 3.0 V and pulse durations from 2 ns to 100 ns, achieving a high HRS/LRS ratio of approximately 10^3. (a) Post-SET resistance states. (b) Resistance contrast.

6.3. RESET Switching Kinetics

This section presents the analysis of measurements performed to study the kinetics of the RESET process. In contrast to the SET investigations performed on 10% SIST, the RESET measurements were conducted on 40% SnTe-doped In_3SbTe_2 (40% SIST). The SnTe concentration in SIST influences the electrical resistivity and structural properties of the material. Increasing the SnTe fraction leads to higher resistivity and enhanced scattering at grain boundaries and phase interfaces, which results in a more pronounced resistance contrast in the RESET state [30]. For this reason, a higher SnTe content (40% SIST) was selected for the RESET investigations, as it enables clearer observation of the HRS after amorphization. Additionally, during the period in which the measurements were performed, devices with other SIST compositions were not consistently available for RESET experiments.

The measurement procedure is described in Section 6.1.1, where RESET pulses were applied using the PG5 pulse generator, with pulse widths ranging from 50 ps to 250 ps in 5 ps increments. The pulse amplitude was controlled using an external attenuator. Initial RESET measurements were therefore carried out at three different voltages.

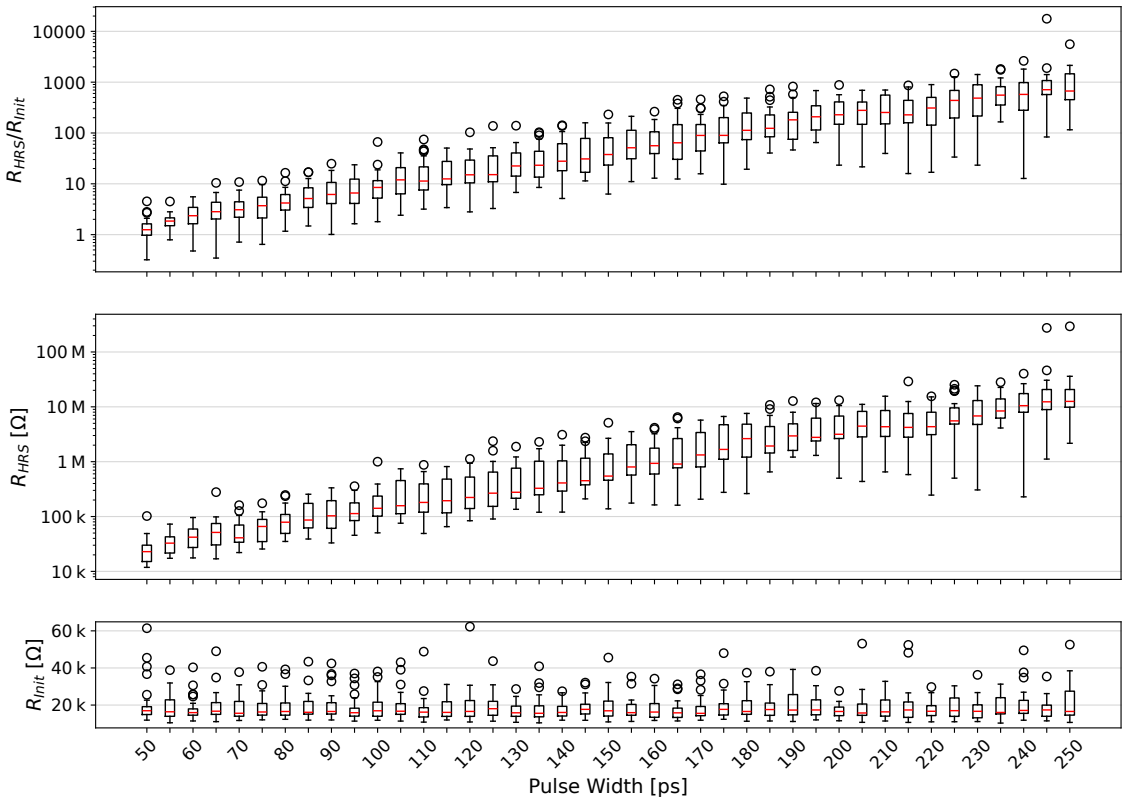


Figure 6.9: RESET switching behavior of a 40% SIST device at 7.08 V for pulse widths from 50 ps to 250 ps. Each box plot represents ten measurements. Top: $R_{\mathrm{HRS}}/R_{\mathrm{init}}$ ratio. Middle: HRS resistance. Bottom: initial LRS resistance.

The effect of the RESET pulse was evaluated by comparing the resistance state before and after pulse application. After each RESET attempt, the device was returned to the LRS using a SET pulse with fixed parameters, as listed in Table 6.4. The results obtained at a RESET voltage of 7.08 V are shown in Figure 6.9 using box plots, where each box represents ten repeated measurements. The first panel shows the HRS/LRS resistance ratio, the second panel presents the post RESET resistance, and the third panel shows the initial LRS resistance R_{init} as a function of pulse width. For short pulse widths of 50 ps, the median value of $R_{\text{HRS}}/R_{\text{init}}$ remains close to unity, indicating that the RESET pulse does not significantly affect the device state. As the pulse width increases, the resistance ratio increases gradually, indicating a stronger RESET effect. At pulse widths of approximately 110 ps, resistance ratios on the order of 10^2 are observed, showing a transition of the device into the HRS in the megaohm regime. With further increase in pulse width, the HRS/LRS ratio continues to rise and reaches values of approximately 10^3 at 250 ps. These results demonstrate that reliable RESET switching into the megaohm resistance regime can be achieved using RF Setup 2 by applying short RESET pulses.

Figure 6.10 extends the RESET kinetics analysis by showing the effect of higher RESET voltages of 8.91 V on the switching behavior. As expected, increasing the RESET voltage to 8.91 V results in faster switching behavior compared with the lower voltage case.

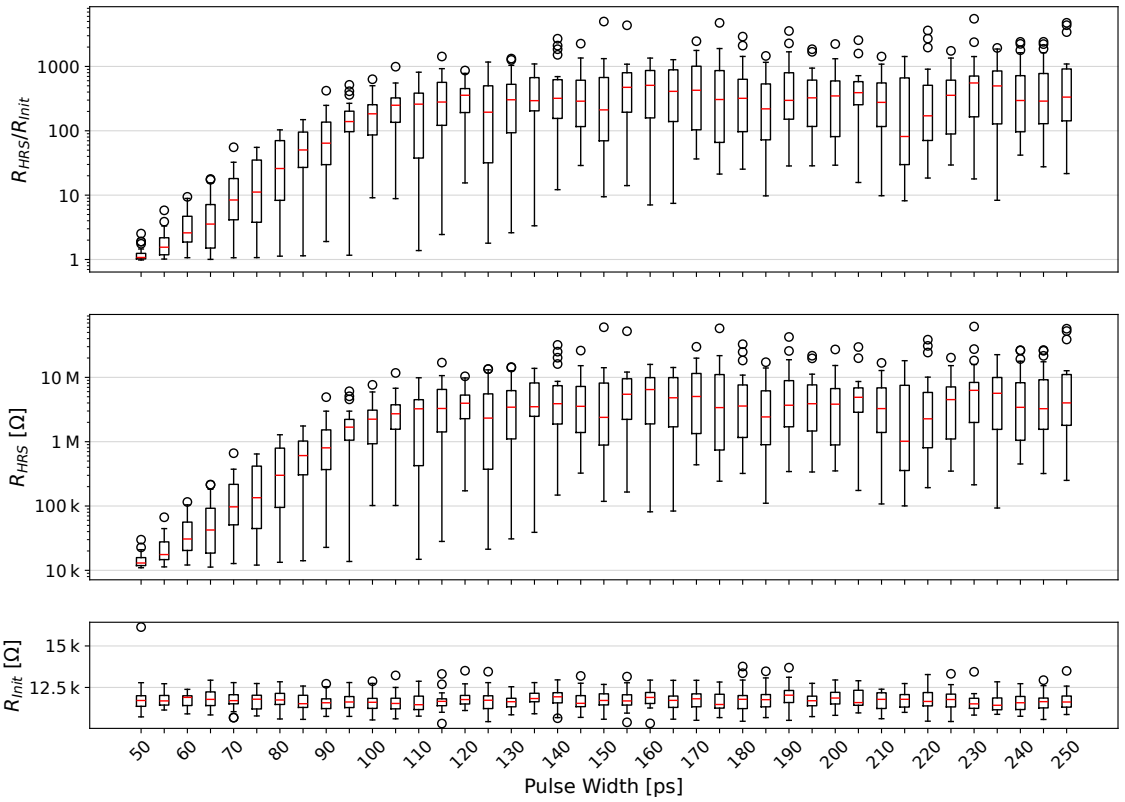


Figure 6.10: RESET switching behavior of a 40% SIST device at 8.91 V, demonstrating faster switching compared to 7.08 V.

As the pulse width increases beyond 70 ps, the resistance ratio continues to rise, reaching values exceeding 1000 at longer pulse durations. The higher voltage amplitude enables more rapid Joule heating and faster melting of the crystalline phase, allowing the melt-quench amorphization process to complete within shorter time windows.

These results demonstrate that the RESET switching speed can be systematically controlled through the pulse amplitude, with higher voltages enabling faster transitions to the HRS at shorter pulse widths. This voltage-amplitude dependence reflects the thermal nature of the RESET process, where increased Joule heating accelerates both the melting and subsequent quenching phases [27, 47].

To directly compare the influence of pulse amplitude on RESET switching kinetics, Figure 6.11 presents the combined results for all three investigated voltages (7.08 V, 7.94 V, and 8.91 V), corresponding to attenuation levels of 3 dB, 2 dB, and 1 dB, respectively, over

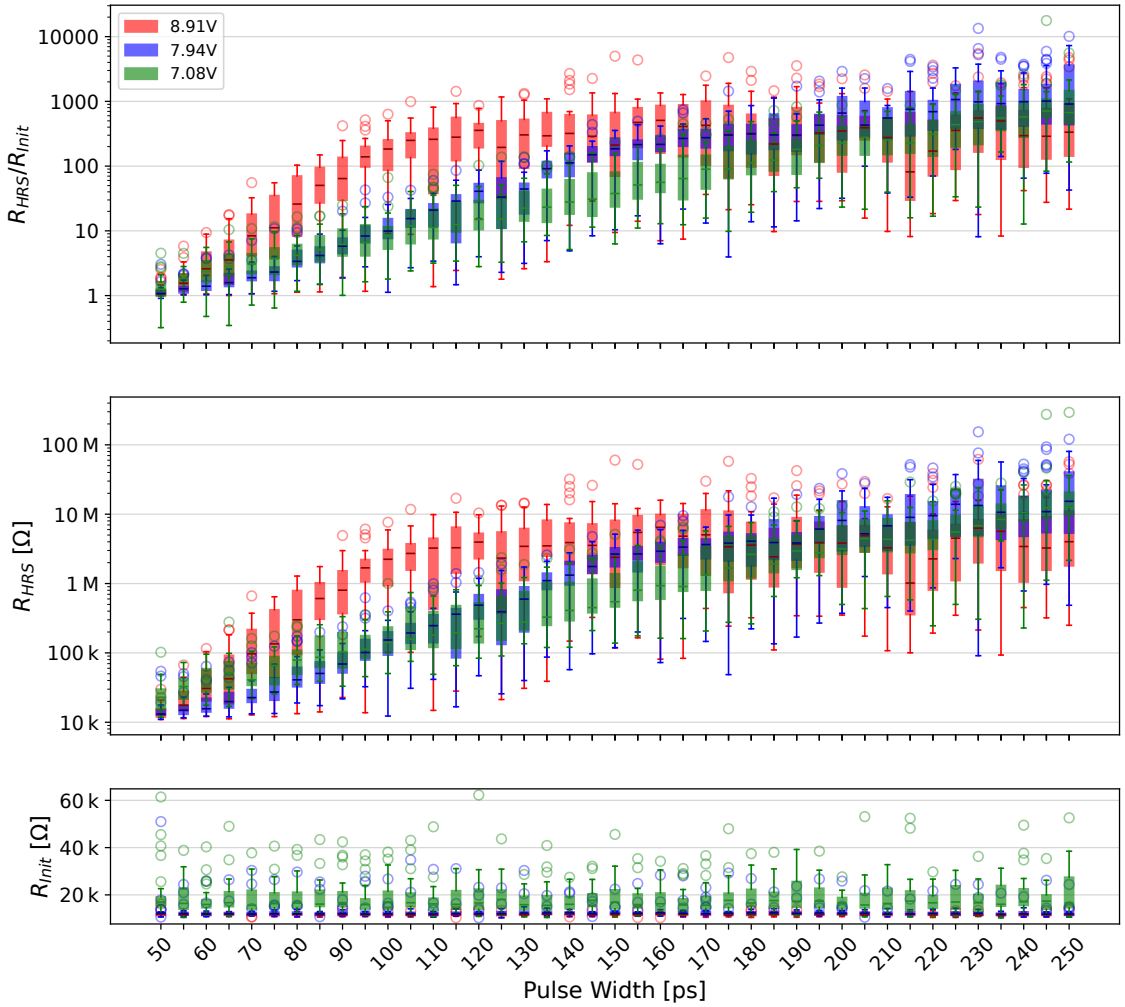


Figure 6.11: Comparison of RESET switching kinetics for three different RESET voltages (7.08 V, 7.94 V, and 8.91 V) as a function of pulse width. The figure shows the evolution of the resistance ratio $R_{\mathrm{HRS}}/R_{\mathrm{init}}$, highlighting the combined influence of pulse amplitude and duration on the RESET behavior. Higher RESET voltages enable faster switching and higher resistance contrast at shorter pulse widths.

the same pulse width range. This allows a direct comparison of the combined effects of voltage and pulse duration on the RESET behavior.

A clear voltage dependence of the switching dynamics is observed. At the lowest RESET voltage of 7.08 V, the ratio $R_{\mathrm{HRS}}/R_{\mathrm{init}}$ increases gradually with increasing pulse width, requiring approximately 100 ps to reach values around 100. In contrast, at 8.91 V, large $R_{\mathrm{HRS}}/R_{\mathrm{init}}$ ratios are already achieved at pulse widths of about 70 ps, and the corresponding HRS values are consistently higher than those observed at lower voltages. This is faster than the 200 ps RESET switching previously reported for GST-based PCM cells [8], demonstrating that SIST devices can achieve higher RESET speeds.

These first systematic measurements demonstrate a clear dependence of RESET switching on pulse amplitude. Higher voltages enable the device to reach HRS at shorter pulse durations, whereas lower voltages require extended pulse widths to achieve comparable switching contrast. This behavior is consistent with the thermal nature of the melt-quench amorphization process [27, 47], where increased Joule heating at elevated voltages accelerates both the melting and subsequent quenching. These findings confirm that both pulse amplitude and duration play essential roles in determining RESET switching kinetics in the sub-100 ps regime, and demonstrate that RF Setup 2 enables reliable characterization of ultra-fast RESET dynamics with access to highly resistive amorphous states.

6.4. Conclusion

This chapter presented the first comprehensive experimental investigation of the SET and RESET switching kinetics of PCM devices using the newly developed RF Setup 2. The setup enabled reliable electrical characterization over a wide temporal range, extending into the sub-ns timescale, while suppressing leakage currents and enabling accurate HRS measurements.

Systematic SET measurements on 10% SIST revealed a strong dependence of crystallization behavior on both pulse amplitude and pulse duration. By varying these pulse parameters and analyzing the resulting resistance states, distinct switching regimes were identified, corresponding to nucleation-dominated and growth-dominated crystallization processes [48]. Heatmap representations provided a compact visualization of these regimes and showed that higher voltages enable faster and more reproducible SET switching through enhanced Joule heating and crystal growth [47, 48]. The separation of stochastic nucleation-dominated behavior from deterministic growth-dominated switching addresses a long-standing challenge in PCM research [28] and provides insights into the origins of switching variability. Measurements across multiple devices confirmed that this behavior is reproducible and device-independent.

RESET measurements on 40% SIST devices in the sub-250 ps regime demonstrated that RESET kinetics depend on both pulse amplitude and width. At lower voltages, RESET

switching occurred gradually and required longer pulse durations, whereas higher voltages enabled rapid transitions into highly resistive amorphous states at sub-100 ps pulse widths, faster than the 200 ps RESET switching previously reported for GST devices [8]. The systematic voltage dependence confirms that RESET switching is dominated by a thermally driven melt-quench amorphization process [27, 47]. The ability to achieve $R_{\mathrm{HRS}}/R_{\mathrm{init}}$ ratios exceeding 10^3 demonstrates the enhanced characterization capabilities of RF Setup 2 compared to conventional measurement approaches. These findings provide a foundation for optimizing pulse programming strategies and motivate further investigations into PCM switching dynamics.

7. Conclusion and Outlook

7.1. Conclusion

This work addressed the ultra-fast electrical characterization of memristive devices for neuromorphic applications, focusing first on TaO_x-based filamentary VCM devices and later on PCM devices. The aim was to access the sub-ns regime and investigate switching dynamics, linear potentiation, thermal effects, and STP under ultra-short pulse operation. To this end, high-frequency RF setups were developed and upgraded to enable reliable characterization at these timescales.

Investigations on TaO_x-based VCM devices were carried out under two main operating conditions. First, switching was studied using sub-100 ps SET pulses separated by long inter-pulse delays of one second, ensuring full thermal relaxation between consecutive pulses. It was shown that pulse widths shorter than the thermal time constant of the conductive filament suppress positive electrothermal feedback, enabling gradual and highly linear conductance modulation. Under optimized conditions of 50 ps pulse width and 1.77 V effective voltage, up to 104 pulses were achieved within the linear regime with an R^2 value of 99.5 %. Compared to previously reported results at nanosecond pulse widths, the accessible linear conductance window was significantly extended.

Furthermore, the dependence on the initial LCS was investigated. Unlike behavior observed at slower timescales, devices starting from a lower initial LCS exhibited improved linear switching behavior in the sub-100 ps regime. This can be attributed to the wider available conductance window before saturation is reached. Although C2C variability remains present due to the stochastic nature of filament formation and dissolution, measurements on multiple devices confirmed reproducible gradual switching behavior, indicating that the observed effects are intrinsic to the TaO_x material system.

In a second step, the inter-pulse delay was reduced to the sub-ns range to study the effects of thermal accumulation. In this regime, residual Joule heating from previous pulses is not fully dissipated before the arrival of the next pulse, and the switching dynamics therefore depend not only on the applied pulse parameters but also on the thermal history of the device. Since conventional DC read operations are not feasible at these timescales, two dedicated evaluation methods were developed to extract the resistive contribution

from the transient RF response. Both methods showed good agreement with post-pulse DC resistance measurements. Systematic variation of the inter-pulse delay demonstrated that the switching dynamics depend on thermal accumulation. For short pulse delays, an elevated device temperature enhances conductance changes, while for delays above approximately 250 ps the switching behavior becomes independent of pulse spacing. This delay corresponds to the thermal relaxation time of the conductive filament under the investigated conditions. The results indicate that temperature acts as an internal state variable and that TaO_x-based VCM devices exhibit second-order memristive behavior under ultra-fast pulse operation.

The delay-dependent conductance evolution was further analyzed in terms of short-term synaptic plasticity. PPF and PTP were demonstrated at sub-ns timescales. Both effects decrease with increasing inter-pulse delay and increase with higher pulse amplitude, consistent with the role of transient temperature dynamics.

In addition to VCM devices, PCM devices were characterized using RF Setup 2, an upgraded version of RF Setup 1 in which the bias tee was replaced by RF switches to suppress leakage currents and enable reliable resistance measurements in the megaohm range. The setup also incorporated an AWG for programmable control of the pulse shape. With this configuration, SET and RESET switching kinetics were investigated at sub-ns timescales. In the SET direction, the switching behavior showed a strong dependence on pulse amplitude and duration. Two distinct switching regimes were identified, separated by a non-switching aging region. The lower-voltage regime exhibited pronounced stochastic behavior consistent with nucleation-dominated crystallization. In contrast, the higher-voltage regime exhibited more reproducible switching, indicating growth-dominated crystallization once stable nuclei are formed. This electrical distinction between the two regimes provides insight into the underlying crystallization mechanisms without requiring structural analysis. RESET measurements in the sub-250 ps regime further demonstrated that amorphization strongly depends on pulse amplitude. Increasing the RESET voltage accelerates the melt-quench process, enabling the HRS to be reached at progressively shorter pulse widths. HRS/LRS ratios exceeding 10^3 were achieved at sub-100 ps pulse widths, demonstrating reliable amorphization in the sub-250 ps regime.

7.2. Outlook

7.2.1. Future Directions for VCM Devices

Improving Linearity and Stability

The findings of this thesis open several directions for future research. Although highly linear potentiation was achieved at sub-100 ps timescales, C2C variability continues to limit reproducibility due to the inherently stochastic formation of conductive filaments. One promising approach to mitigate this is lateral filament confinement through nano-scaling of the switching oxide, as demonstrated in [155]. In their nano-fin device design, the switching oxide volume was laterally confined to 10 nm within a silicon nitride diffusion barrier, suppressing lateral oxygen vacancy diffusion and thereby reducing the number of available filament configurations. As a result, electrical measurements showed a substantial reduction in HRS write variability compared to a micro-sized reference device. Kinetic Monte Carlo simulations linked this improvement to an increased oxygen vacancy concentration within the confined filament and a reduced filament-to-electrode gap. Applying such a lateral oxide confinement approach to the CPW integrated TaO_x devices investigated in this thesis, therefore, represents a viable path toward improving the reproducibility of linear potentiation at sub-100 ps timescales.

Beyond structural confinement, the choice of switching oxide material itself offers another degree of freedom for reducing read variability. It has been shown that VCM devices fall into two conduction types based on the energy gap between oxygen vacancy defect states and the conduction band, with type 1 materials exhibiting significantly lower ionic noise due to their band-conduction-dominated transport [156]. Since TaO_x belongs to type 2, its switching dynamics are inherently accompanied by pronounced ionic noise from oxygen vacancy hopping, directly contributing to C2C variability. Transitioning to a material system with band-conduction-dominated transport could therefore reduce read noise and improve conductance stability, although potential trade-offs in switching dynamics would need to be carefully evaluated.

Integration into a 1T1R configuration represents another important future direction, as the series transistor can provide tighter current control and suppress leakage in array environments. It has been shown that the transistor W/L ratio determines the accessible current range and controls whether the transistor operates in the linear or saturation region during SET. Operation in the saturation region is essential for effective variability suppression [157]. Translating the sub-100 ps pulse regime into a 1T1R configuration would therefore require careful matching of transistor characteristics to the TaO_x switching dynamics. In addition, the influence of transistor parasitics and interconnect capacitances on pulse fidelity at sub-ns timescales must be systematically investigated.

Finally, while this thesis demonstrated gradual and linear conductance increase during SET at sub-100 ps timescales, the complementary depression process in the RESET direction remains to be systematically characterized in this regime. Previous studies have shown that gradual depression can be achieved alongside potentiation by matching the pulse duration to the intrinsic switching transition time and restricting operation to a well-defined conductance window, thereby enabling symmetric LTP/long-term depression (LTD) cycles [7]. Extending this concept to sub-ns timescales would first require a detailed investigation of gradual RESET behavior under sub-100 ps pulse excitation, followed by the integration of potentiation and depression into complete LTP/LTD sequences. Achieving symmetric and controllable gradual switching at these timescales would represent an important step toward artificial synapses operating at sub-ns speeds.

Thermal Dynamics and Short-Term Plasticity

The results presented in this thesis demonstrate that TaO_x devices are capable of emulating key synaptic behaviors such as PPF and PTP at sub-ns timescales. However, the analysis was performed on a limited set of measurements, and extending these to higher pulse amplitudes and longer inter-pulse delays would allow stronger and more pronounced plasticity effects to be observed, thereby providing a more complete understanding of the synaptic behavior of TaO_x devices at these timescales.

Beyond potentiation, the corresponding behavior in the RESET direction remains unexplored. Varying the inter-pulse delay during RESET pulse trains would allow extraction of the thermal time constant of filament dissolution and determination of whether a gradual conductance decrease can be achieved analogously to the SET case. This builds on the concept of device temperature acting as an internal state variable with a characteristic relaxation time, regulating both conductance increase and decrease [24]. Extending these measurements to the RESET direction at sub-ns timescales would provide direct insight into the ultra-fast thermal dynamics governing filament rupture.

Such experiments are also directly relevant to paired-pulse depression (PPD), a form of short-term synaptic plasticity where a second pulse produces a smaller conductance change than the first due to insufficient thermal relaxation at short inter-pulse delays [158]. Investigating whether PPD can be realized in TaO_x at sub-ns timescales, therefore, represents a meaningful extension of the work presented in this thesis.

7.2.2. Future Directions for PCM Devices

Switching Kinetics and Gradual Conductance Modulation

The SET kinetics measurements presented in this thesis provide the first systematic characterization of the switching behavior of the confined PCM device across a wide range of pulse amplitudes and widths, establishing a foundation for further investigations using RF Setup 2. Further investigations at higher pulse amplitudes, combined with shorter pulse widths, would provide additional insight into the SET kinetics. In particular, extending the measurements beyond the 4.0 V range at short pulse widths would clarify whether full crystallization can be achieved under these conditions, resulting in a stable transition to the LRS. The SIST devices investigated in this thesis already show a direct separation between the nucleation-growth regime and the pure growth regime, as illustrated in Figure 6.6. However, the separation between the upper cutoff of the low-voltage region and the lower boundary of the high-voltage region observed in the heatmap remains unexplained. The physical origin of this gap requires further investigation. Heat dissipation during the pulse may contribute to this behavior and therefore represents a relevant aspect for future study.

In contrast to the SET investigation, the RESET measurements presented in this thesis demonstrate that the PCM device can be switched back to the HRS at pulse widths down to approximately 80 ps using RF Setup 2. A more systematic investigation of the RESET kinetics at even shorter pulse widths is therefore required to assess whether reproducible amorphization can be achieved down to 50 ps and whether the device reliably returns to the megaohm resistance range under these conditions. Amorphization in PCM is inherently abrupt due to the melt-quench process, and gradual RESET has only been demonstrated down to 0.4 ns by operating below the thermal time constant of the device [9]. Extending this approach to sub-100 ps timescales using RF Setup 2 would allow evaluation of whether gradual and more linear conductance modulation can be achieved at even shorter pulse durations. Achieving controlled conductance modulation in PCM would provide functionality comparable to the gradual potentiation demonstrated in the TaO_x-based VCM devices investigated in this thesis. Furthermore, the RESET measurements were performed only on the 40% SIST device. Extending the study to additional SIST geometries would allow systematic comparison of the RESET dynamics as a function of device dimensions.

List of Acronyms and Symbols

Acronym	Definition
1T1R	One transistor one memristor
8w	eight-wise
AE	Active electrode
AWG	Arbitrary waveform generator
BE	Bottom electrode
C2C	Cycle-to-cycle
c8w	Counter-eight wise
CC	Current compliance
CIM	Computing-in-memory
CMOS	Complementary metal-oxide-semiconductor
CPU	Central processing unit
CPW	Coplaner waveguide
D2D	Device-to-device
DC	Direct current
DFE	Defect formation energy
DRAM	Dynamic random-access memory
DUT	Device under test
ECM	Electrochemical metallization memory
FeRAM	Ferroelectric random access memory
FWHM	Full width at half maximum
GPIB	General-purpose interface bus
GSG	Ground-signal-ground
HCS	High conductive state
HDD	Hard disk drive
Hf	Hafnium
HfO_2	Hafnium oxide
HRS	High resistive state

Acronym	Definition
IE	Inner conductor
I-V	Current-voltage
IWE 2	Institut für Werkstoffe der Elektronik
LCS	Low conductive state
LTD	Long-term depression
LTP	Long-term potentiation
LRS	Low resistive state
OC	Outer conductor
OE	Ohmic electrode
MAE	Mean absolute error
MIM	Metal-insulator-metal
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
MSC	Melt and slow cooling
ns	Nanoseconds
NDR	Negative differential resistance
PCB	Printed circuit board
PCM	Phase change memory
PGI	Peter Grünberg Institute
PG	Pulse generator
ps	Picosecond
PPD	Paired-pulse depression
PPF	Paired-pulse facilitation
PPG30	Pulse pattern generator
Pt	Platinum
PTP	Post-tetanic potentiation
ReRAM	Redox-based resistive random access memory
RF	Radio frequency
RRAM	Resistive random access memory
SCM	Storage-class memory
SMU	Source measurement unit
SOLT	Short open load trough
SP3T	Single-pole, triple-throw
SPC	Solid phase crystallization
SPDT	Single-pole, double-throw
SRAM	Static random access memory
SSD	Solid state drive

Acronym	Definition
STDP	Spike timing dependent plasticity
STP	Short-term plasticity
STTRAM	Spin-transfer torque random access memory
Ta	Tantalum
TaO_x	Tantalum oxide
TCM	Thermochemical memory
TE	Top electrode
TEM	Transverse electromagnetic
Ti	Titanium
TiO_x	Titanium oxide
USB	Universal serial bus
VCM	Valence change mechanism
VNA	Vector network analyzer

List of Publications

Peer Reviewed Journals

F. Munir, J. Klinkmann, P. Stasner, S. Jia, R. Waser, and S. Wiefels, "Linear Potentiation in Filamentary Valence Change Mechanism With Sub-100 ps Pulses," *IEEE Access*, vol. 13, pp. 120762-120771, 2025, DOI: 10.1109/ACCESS.2025.3586720

D. Schön, **F. Munir**, P. Stasner, S. Wiefels, and S. Menzel, "Exploiting Thermal Accumulation on Sub-ns Timescales for Tuning Potentiation of RRAM," *IEEE Electron Device Letters*, vol. 46, no. 11, pp. 2018-2021, 2025, DOI: 10.1109/LED.2025.3612742

F. Munir, D. Schön, S. Menzel, P. Stasner, R. Waser, and S. Wiefels, "Evaluation Methods for ReRAM Potentiation on Sub-Nanosecond Timescales," *IEEE Transactions on Electron Devices*, vol. 71, no. 11, pp. 6691-6697, 2024, DOI: 10.1109/TED.2024.3461676

Y. Zhou, **F. Munir**, J. Zedler, A. Kiehn, S. Wiefels, and M. Wuttig, "Direct observation of nucleation and growth event in SnTe doped In_3SbTe_2 phase change memory," *In preparation*.

Conference Talks and Posters

F. Munir, D. Schön, S. Menzel, P. Stasner, R. Waser, and S. Wiefels, "Unveiling Conductance States in ReRAM Cells through Analysis of Ultra Fast Pulse Sequences," in *Proc. Int. Conf. Neuromorphic Comput. Eng. (ICNCE)*, Aachen, Germany, Jun. 2024.

F. Munir, D. Schön, S. Menzel, P. Stasner, R. Waser, and S. Wiefels, "Investigating Thermal Accumulation Effects in ReRAM Devices at Sub 100ps Timescales with Variable Delays," in *Proc. 22nd Non-Volatile Memory Technol. Symp. (NVMTS)*, Busan, Korea, Oct. 2024.

Supervised Theses

Bachelor's Theses

J. Klinkmann, "Tuning the SET Kinetics of Resistive Switching Devices Towards Gradual Potentiation on a Sub-100 ps Timescale," RWTH Aachen University, October 2023.

J. J. Zedler, "Electrical Characterization of Phase-Change Memory Devices on a Sub-1 Nanosecond Timescale," RWTH Aachen University, August 2024.

A. Iamashev, "Algorithm-Based Automated Endurance Characterization of VCM Devices on Sub-10 ns Timescales," RWTH Aachen University, December 2025.

Master's Theses

S. Gadit, "Exploring Conductance Dynamics in VCM Devices at Ultrafast Pulses with Variable Delays in the Sub-100 ps Regime for Neuromorphic Computing," TU Darmstadt, November 2024.

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Appendix

A. Additional Examples of Linear Switching Behavior in TaO_x

This appendix presents supplementary examples of gradual and linear conductance modulation observed in TaO_x devices under varying pulse widths. Figures A.1 - A.4 illustrate the linear switching behavior for pulse widths of 50 ps, 60 ps, 70 ps, and 100 ps, respectively. Each case highlights the number of conductance state transitions achieved within the linear regime, along with the corresponding R^2 values used to assess linearity.

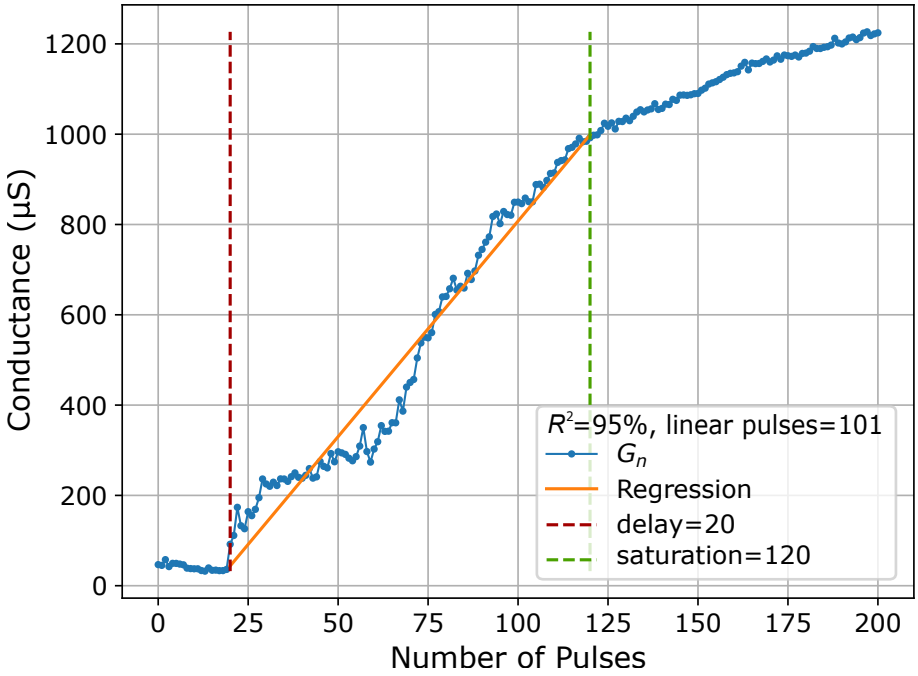


Figure A.1: Gradual and linear switching behavior observed at a pulse width of 50 ps and a voltage of 1.77 V, demonstrating 101 conductance state transitions within the linear region with R^2=95%.

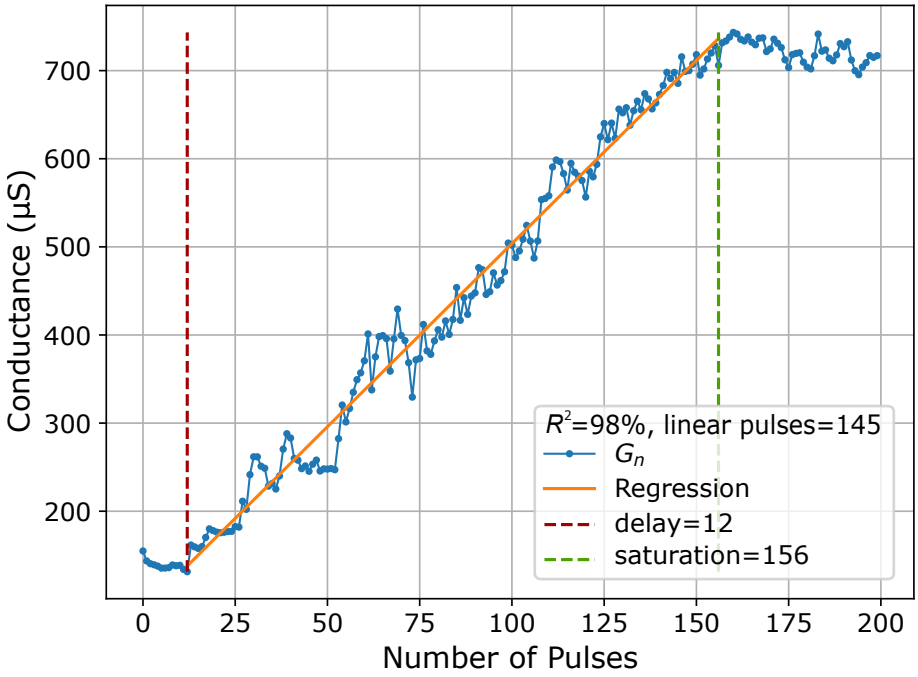


Figure A.2: Linear switching behavior at a pulse width of 60 ps and a voltage of 1.58 V, showing 145 conductance states in the linear regime with R^2=98%.

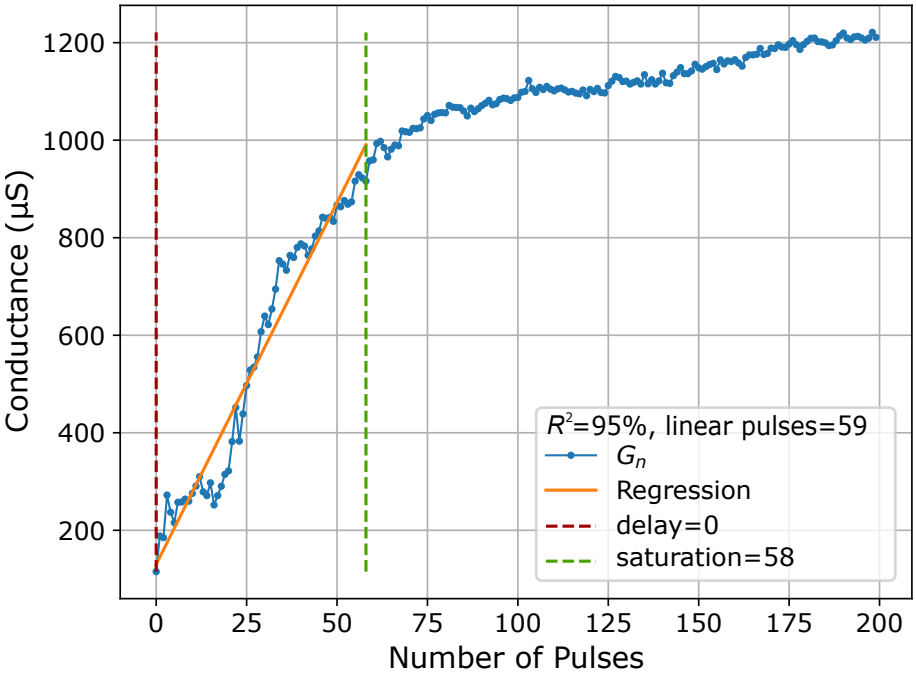


Figure A.3: Example of linear conductance modulation using 70 ps pulse width and 1.58 V, yielding 59 linear states with R^2= 96%.

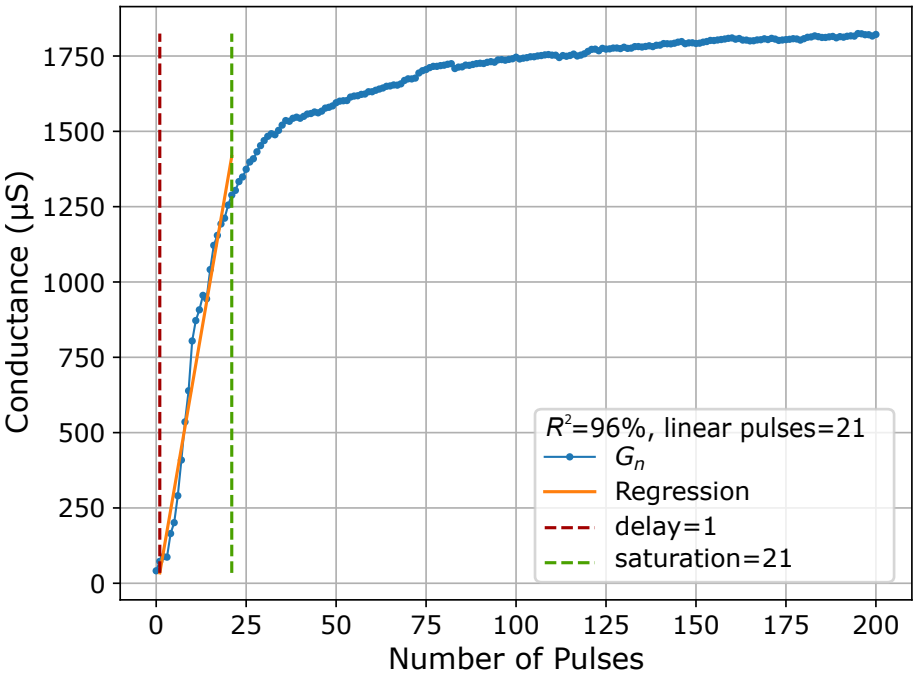


Figure A.4: Limited linear switching observed at 100 ps pulse width and 1.41 V, with 21 conductance transitions and R^2= 95%.

B. Average Conductance Across All Measurement Cycles

The device response at intermediate pulse widths of 60 ps and 70 ps reveals how optimal voltage selection is critical for controlling the duration of the linear switching regime (Figure B.1 and Figure B.2). For the 60 ps pulse width, the 1.77 V amplitude initially shows a gradual and linear increase in mean conductance over the first 20 pulses (Figure B.1(a)). However, for the full 200-pulse sequence (Figure B.2(a)), slightly lower voltages (1.41 V and 1.58 V) show more effectiveness at sustaining this gradual, linear transition across the longer conductance time window. Similarly, at the 70 ps pulse width, the 1.58 V amplitude demonstrates the optimal gradual and linear increase over the initial 20 pulses (Figure B.1(b)). Over the 200-pulse cycle (Figure B.2(b)), the gradual evolution is sustained by both the 1.41 V and 1.58 V amplitudes. Overall, these results demonstrate that a gradual and linear transition is achievable in TaO_x devices by carefully selecting both pulse width and amplitude.

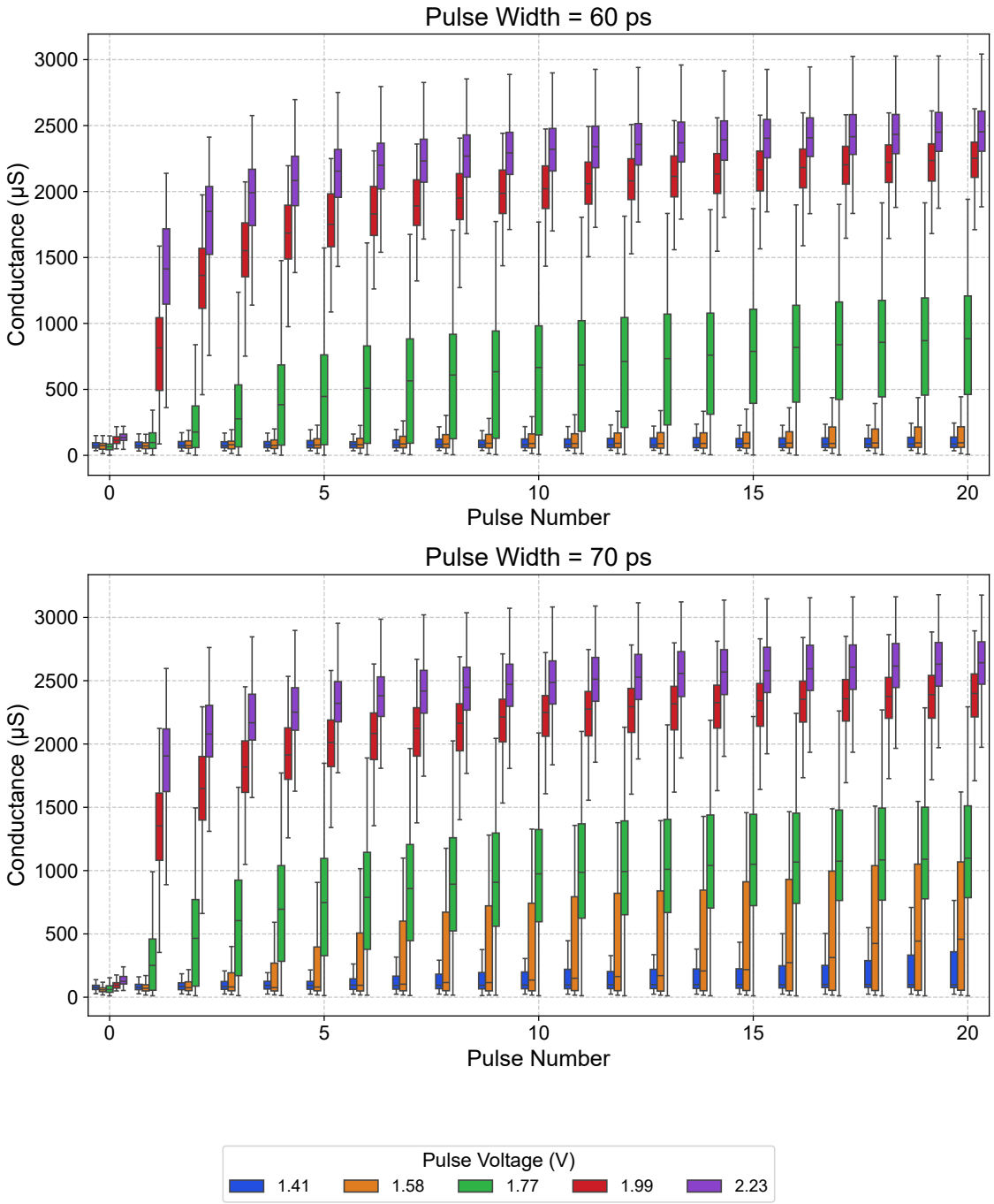


Figure B.1: Box plots showing the conductance evolution during the initial 20 pulses for intermediate pulse widths: (a) 60 ps and (b) 70 ps. Each box illustrates the distribution of measured conductance values across all measurement cycles for a given voltage. The plots confirm that a gradual and linear increase in mean conductance is achieved by tuning the voltage. This demonstrates the feasibility of maintaining the desirable linear switching regime by adjusting the voltage to compensate for the small increase in pulse duration.

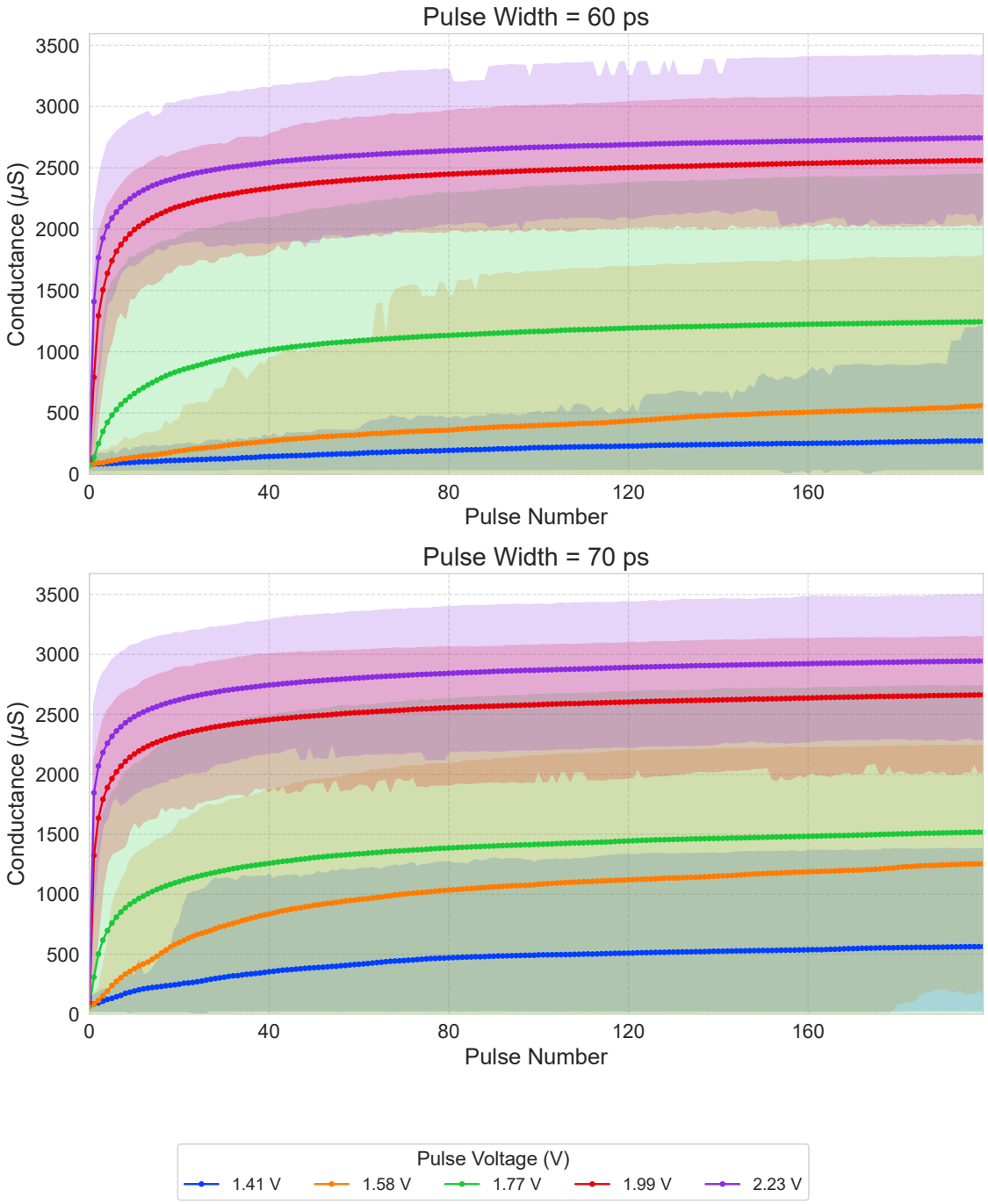


Figure B.2: Average conductance evolution over a full 200-pulse sequence for intermediate pulse widths: (a) 60 ps and (b) 70 ps. The solid lines show the mean conductance trends for various pulse voltages, while the shaded regions surrounding each line represent the C2C variability, indicating the full range of measured conductance values across all measurement cycles.

C. Examples of Non-Switching Events in VCM

In addition to the main results presented in the manuscript, several experimental cycles exhibited non-ideal behavior. To provide a complete picture of the device response, this appendix section includes representative raw data from measurements where switching did not occur, as well as instances of abnormal transitions such as unipolar RESET events. These plots highlight the variability occasionally observed in TaO_x devices under pulsed operation and serve to illustrate the full range of measured outcomes, including unsuccessful switching cycles.

Figures C.1, C.2, C.3, and C.4 show examples of cycles in which unipolar RESET occurs, i.e., the device conductance decreases instead of increasing during SET switching. Figure C.5, C.6 illustrates a typical failed SET switching event, where the conductance remains largely unchanged. Figure C.7 presents the results of poor probe contact, which also leads to non-switching behavior. These plots provide representative examples of non-ideal device responses encountered during experimentation.

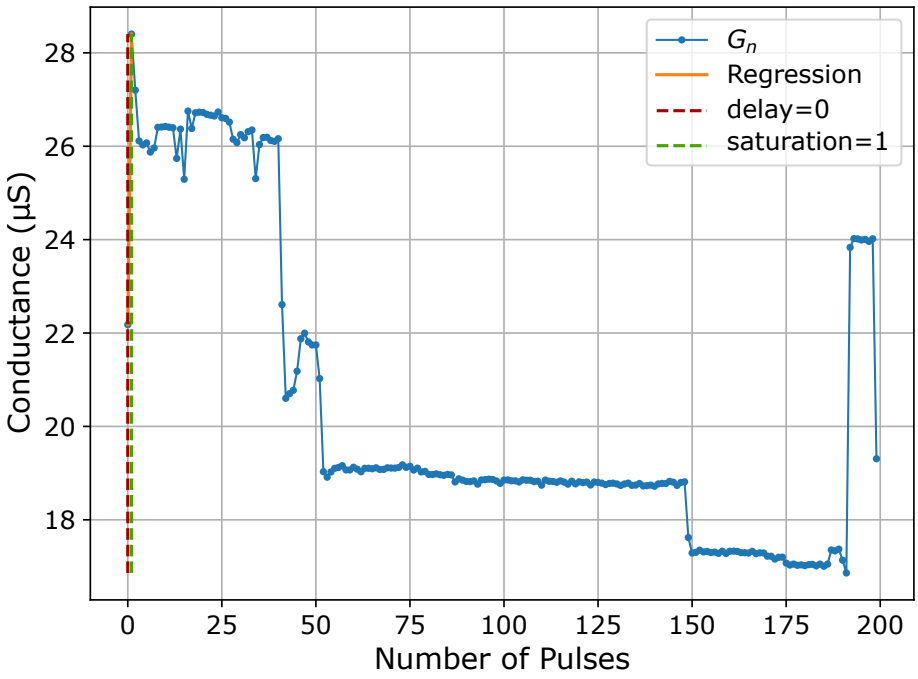


Figure C.1: Example of a cycle showing unipolar RESET, where the device conductance decreases instead of increasing during SET switching. Measurement performed with a pulse width of 50 ps and a pulse amplitude of 1.58 V.

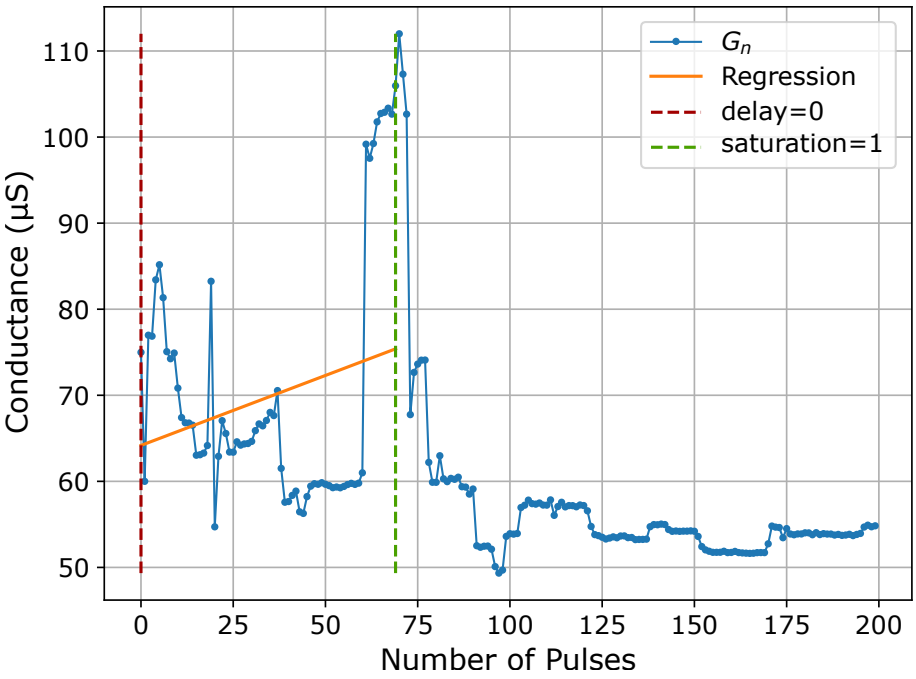


Figure C.2: Another cycle exhibiting unipolar RESET behavior. The device conductance is reduced during the SET process, contrary to the expected increase. Measurement performed with a pulse width of 50 ps and a pulse amplitude of 1.58 V.

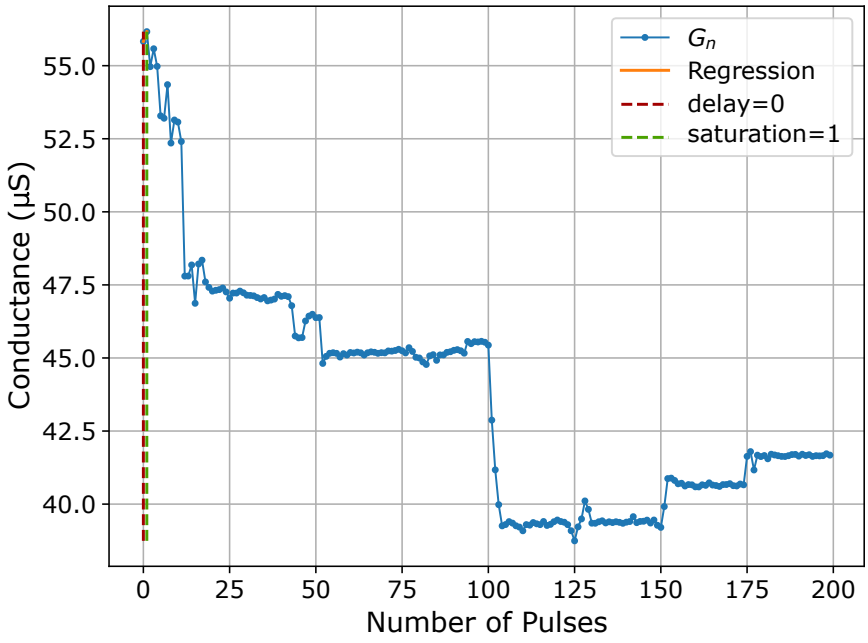


Figure C.3: Cycle illustrating unipolar RESET behavior under the same measurement conditions, with conductance decreasing during SET switching. Pulse width of 50 ps and pulse amplitude of 1.58 V were applied to the device.

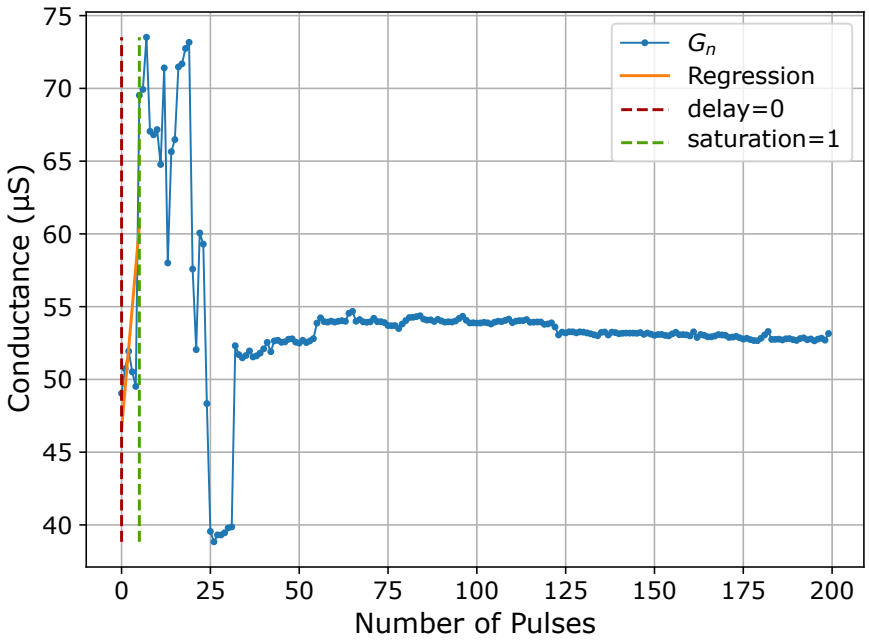


Figure C.4: Further example of unipolar RESET switching. Instead of an increase in conductance, the device shows a decrease during the SET process. Measurement carried out with a pulse width of 50 ps and a pulse amplitude of 1.58 V.

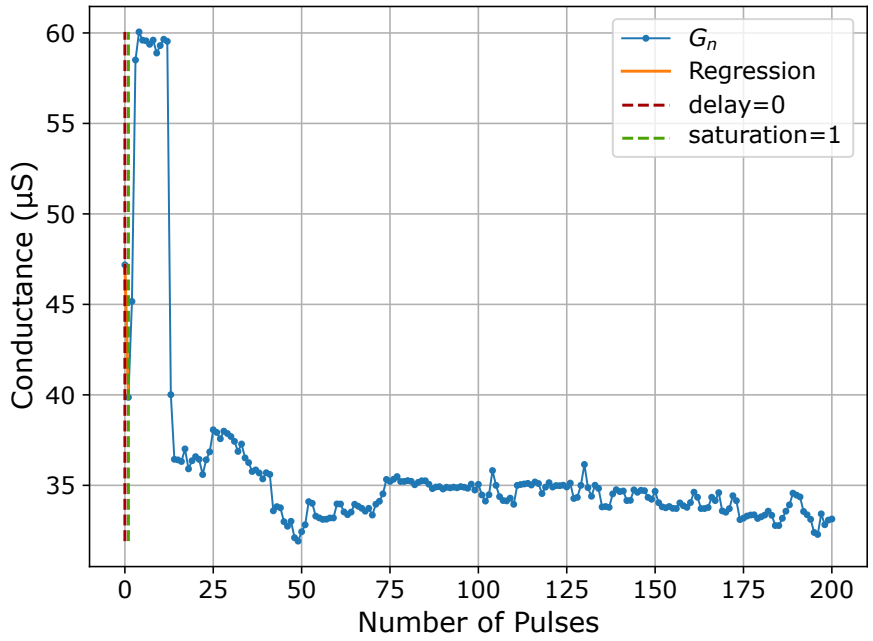


Figure C.5: Typical failed SET switching event with 50 ps pulses at 1.58 V amplitude, demonstrating minimal conductance variation and absence of successful switching behavior.

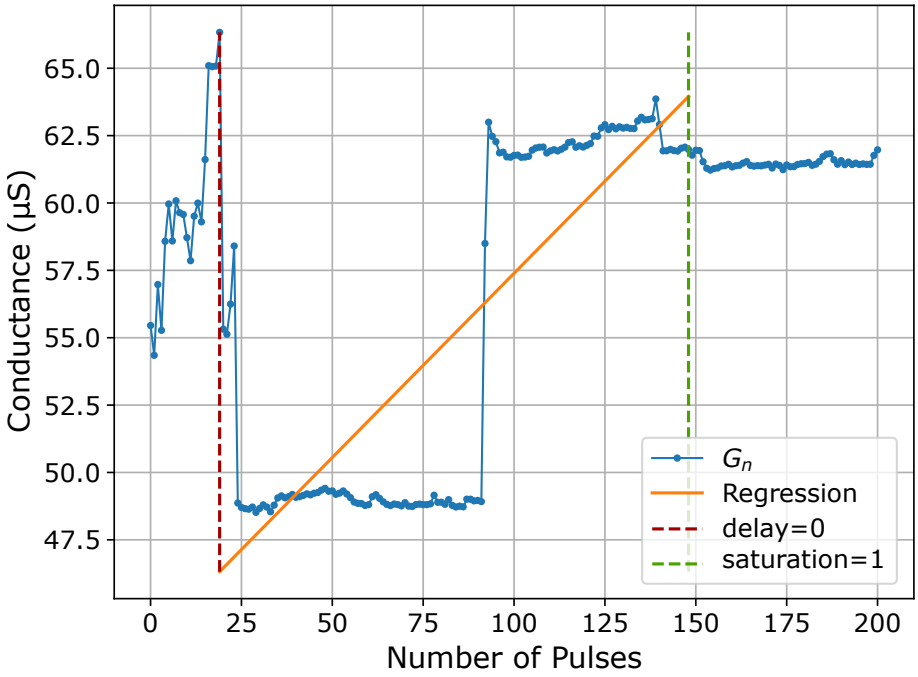


Figure C.6: Representative example of unsuccessful SET switching using 50 ps pulses with 1.58 V amplitude, showing negligible conductance change and switching failure.

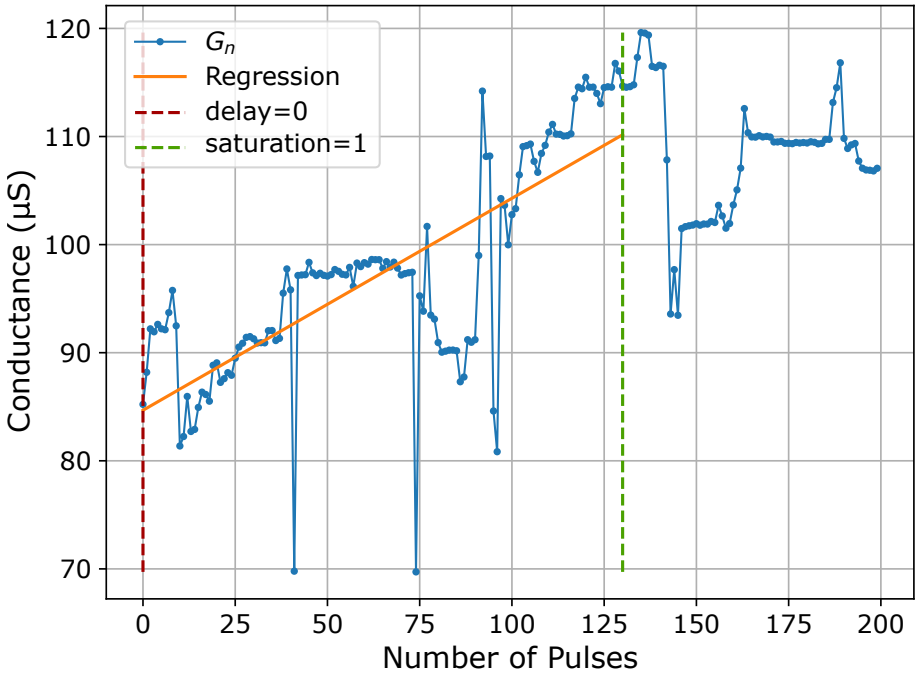


Figure C.7: Results of poor probe contact during measurement with 50 ps pulses at 1.58 V amplitude, leading to non-switching behavior and compromised device response.