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Thickness-Defined Transport Regime Toward Near-Ideal Area-Type Switching

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ABSTRACT

Area-type memristors are attractive for analog in-memory computing, but their use is often limited by parasitic charge storage, causing readout drift, non-pinched hysteresis, and degraded readout fidelity. We show that near-ideal area-type switching emerges within a tunneling-governed transport regime in ultrathin layers that suppresses charging-related readout artifacts. By varying the thickness in TiN/Ta_2O_5/Pt in a range of 3–10 nm, we reveal the transition from filamentary switching to near-short-circuit transport with two gradual-switching modes with different readout stability. The 5–6 nm thickness window suppresses non-pinched hysteresis and short-time drift while preserving analog switching, yielding nearly polarity-symmetric hysteresis and readout, clear area scaling, and continuous near-linear conductance modulation. Our analysis indicates that trap-assisted tunneling dominates the stabilized-state response, whereas ionic redistribution governs pristine-state reconstruction and the stability boundaries. A compact model is derived for the 5 nm device which reproduces the quasi-static I–V behavior and the dynamic resistance evolution based on pulse-width-dependent characteristics. The verified model is provided as Verilog-A code enabling simulation in circuit design tools. Our results demonstrate that ultrathin scaling is a regime-defining design rule for near-ideal area-type operation in oxide memristors, implying a fundamental approach to fabricating robust multi-state memristors for in-memory computing applications.

1 | Introduction

The energy and latency cost of moving data has become a major bottleneck in AI hardware, motivating nonvolatile devices that can store information and perform computation through local conductance modulation [1]. Memristive devices are therefore widely regarded as key enablers for analog in-memory computing. Oxide memristive devices operating through the valence-change mechanism (VCM) can exhibit either filamentary or spatially distributed area-type switching. Filamentary switching is governed by the formation and rupture of localized conductive paths and typically produces abrupt, digital-like

Cuo Wu and Junjie Zhao contributed comparably to this work.

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transitions, whereas the area-type switching relies on more spatially distributed defect modulation, enabling gradual multilevel conductance for analog state encoding [1–4]. However, many area-type memristors suffer from parasitic charge storage and relaxation, here collectively referred to as parasitic charging, which manifests itself as time- and history-dependent readout drift, non-pinched hysteresis, and the so-called battery effect or battery-like offset [5–8]. The associated settling-time penalty and read-offset calibration are incompatible with low-latency, high-frequency operation and ultimately degrade readout fidelity [9–11]. Achieving a near-ideal area-type operating state with stable readout, pinched hysteresis, near-symmetric I–V switching, and continuous analog state encoding remains an unresolved barrier to the practical use of area-type oxide memristors in analog in-memory and analog in-memory computing systems [7, 8].

A central hypothesis of this work is that an ultrathin operating thickness window determines whether near-ideal area-type switching can occur. At nanometer thickness, tunneling increasingly affects charge transport, accelerating charge redistribution and suppressing charge accumulation [12, 13]. A current research gap for ultrathin VCM devices is the systematic understanding of how oxide thickness determines the transport regime, switching behavior, and readout stability, and how these relationships can guide device design [14–16]. We identify two challenges: first, nanometer-scale thickness variations shift the dominant transport and switching mode; and second, defect kinetics in these ultrathin films amplify the effect of small oxygen-vacancy rearrangements on device stability [17, 18]. As a result, many studies still favor thicker dielectrics to reduce variability, underscoring the need for stringent validation on a technologically mature yet mechanistically demanding oxide material.

Among candidate VCM oxides, Ta_2O_5 offers a particularly stringent validation material because it is technologically mature yet intrinsically susceptible to oxygen-vacancy aggregation and localized conduction. However, reported Ta_2O_5 memristors are mostly switching in the filamentary regime [3, 19, 20]. By contrast, only a few studies have reported gradual or apparently non-filamentary switching in ultrathin Ta_2O_5 layers, and a combined demonstration of area scaling, pinched hysteresis, stable low-bias readout, and continuous conductance tuning remains limited [21–24]. These devices generally exhibit pronounced self-rectification, non-zero-crossing hysteresis, or limited retention [21–24]. Demonstrating readout-stable area-type switching in ultrathin single-layer Ta_2O_5 therefore goes beyond optimizing one material stack and suggests that critical ultrathin scaling may also benefit other oxide systems.

Here, using ultrathin TiN/Ta_2O_5/Pt memristors as the device under investigation, we derive the physical boundary conditions under which near-ideal area-type switching might emerge in ultrathin oxide VCM devices. We show that the transition in ultrathin films between filament-type switching and short-circuit-like transport reveals a physically structured regime containing two distinct gradual switching modes with sharply different readout stability and analog programmability. By combining thickness-series comparisons, transport and switching kinetics investigations, as well as area-scaling tests, we delineate the regime boundaries and identify an approximate operating thickness window between 5 and 6 nm in which near-ideal area-type behavior emerges, including polarity-symmetric readout, absence of non-pinched hysteresis and short-time relaxation, area-proportional conductance scaling, and continuous reproducible conductance tuning. We further describe the observed behavior within a two-stage framework in which ionic reconstruction governs initial-state evolution and stability boundaries, whereas injection-controlled trap occupancy controls stabilized-state reversible switching and analog state modulation. Based on this separation, we develop a single-state physics-based compact model for the stabilized 5 nm operating regime that reproduces the quasi-static I–V response and pulse-driven state dynamics enabling EDA circuit simulation. Together, these results identify critical ultrathin scaling as a promising design strategy for readout-stable area-type oxide memristors.

2 | Results

2.1 | Thickness Window for Area-Type Switching

To investigate the effect of oxide thickness on switching behavior, TiN (20 nm)/Ta_2O_5/Pt (50 nm) devices were fabricated with Ta_2O_5 thicknesses ranging from 3 to 10 nm in 1 nm increments, as shown in Figure 1a. The I–V characteristics of the samples with all eight thicknesses are summarized in Figure 1b. The curves in Figure 1 represent one stabilized cycle used for the thickness comparison. For the 5–6 nm devices, the presented curves represent the stabilized response after activation, as discussed further in Figure 2. Here, activation refers to a clear first-cycle-to-stabilized-state transition in the switching response. Such behavior was not observed for the other thickness groups. The 3–4 nm devices showed nearly linear, short-circuit-like transport from the first sweep onward, while the 7–8 nm devices exhibited only a small drift of the non-zero-crossing position without a change in the overall loop shape. We therefore attribute this evolution to charging-related drift rather than activation. The 9–10 nm devices likewise retained their strongly rectifying response during repeated sweeps within the investigated voltage range, unless the voltage approached the forming regime.

In addition to the overall increase in resistance with thickness, the measured curves can be empirically grouped into four distinct thickness-dependent switching regimes. Specifically, the 9–10 nm devices show pronounced rectification without a clear switching window. The 7–8 nm devices exhibit gradual switching together with rectification and an obvious zero offset. The 5–6 nm devices also show gradual switching, but with little or no zero offset or rectification. In contrast, the 3–4 nm devices display nearly short-circuit-like transport without an observable switching window. For clarity, representative I–V curves for 10, 7, 5, and 3 nm are separately shown in Figure 1c–f, illustrating the features observed in these four thickness regimes.

As shown in Figure 1c, the samples having 9–10 nm thick Ta_2O_5 show no pronounced hysteresis within the applied sweep range, and resistance modulation cannot be induced reproducibly without applying a forming pulse. Instead, the devices exhibit strong rectification. Applying a sufficiently large negative bias triggers filament formation and irreversibly converts them into a filamentary-type device. In the present study, none of the devices having 9–10 nm thick switching layers showed area-type

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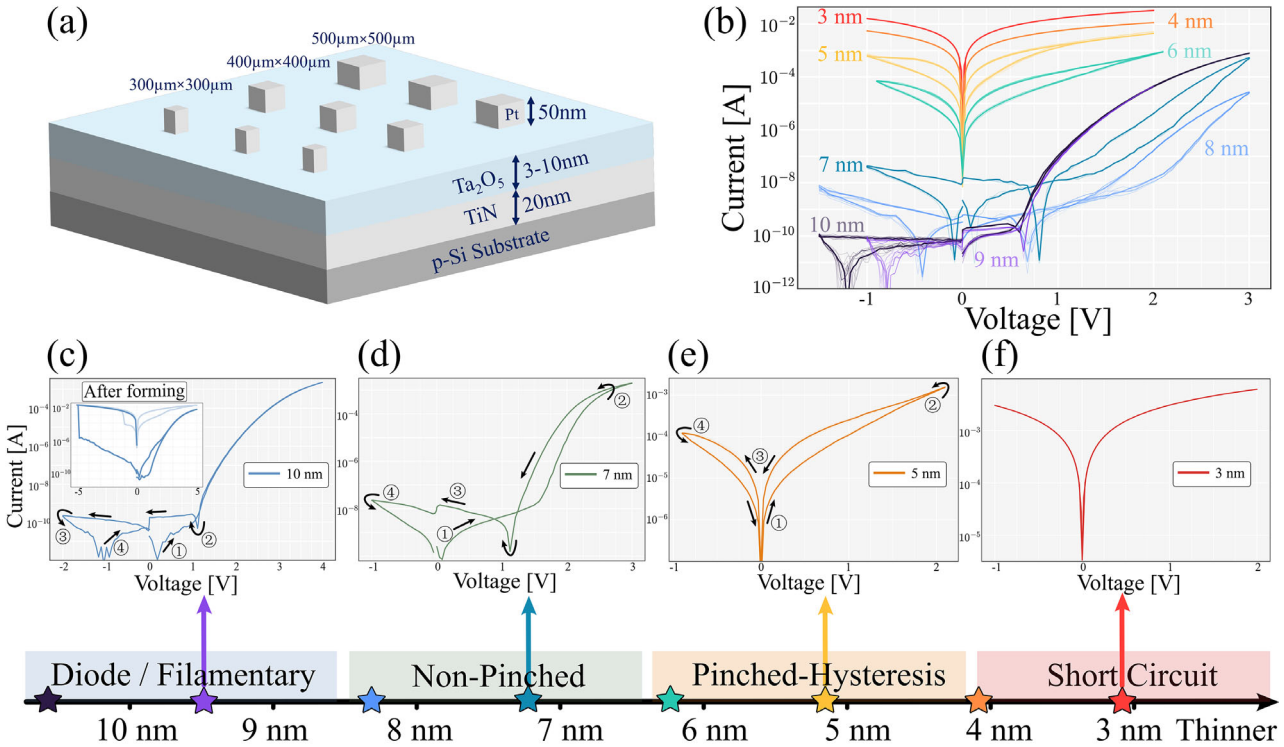


FIGURE 1 | Different switching modes across the ultrathin oxide thickness window. (a) Sketch of the fabricated TiN/Ta_2O_5/Pt devices. (b) Semilogarithmic I–V loops of devices with Ta_2O_5 thicknesses ranging from 3 to 10 nm. For the 5 and 6 nm devices, the curves show the stabilized response after the activation (Figure 2). The median cycle is highlighted, while others are with increased transparency. (c–f) Representative I–V loops for samples having 10 (c), 7 (d), 5 (e), and 3 nm (f) thick Ta_2O_5. The different switching types are labeled below.

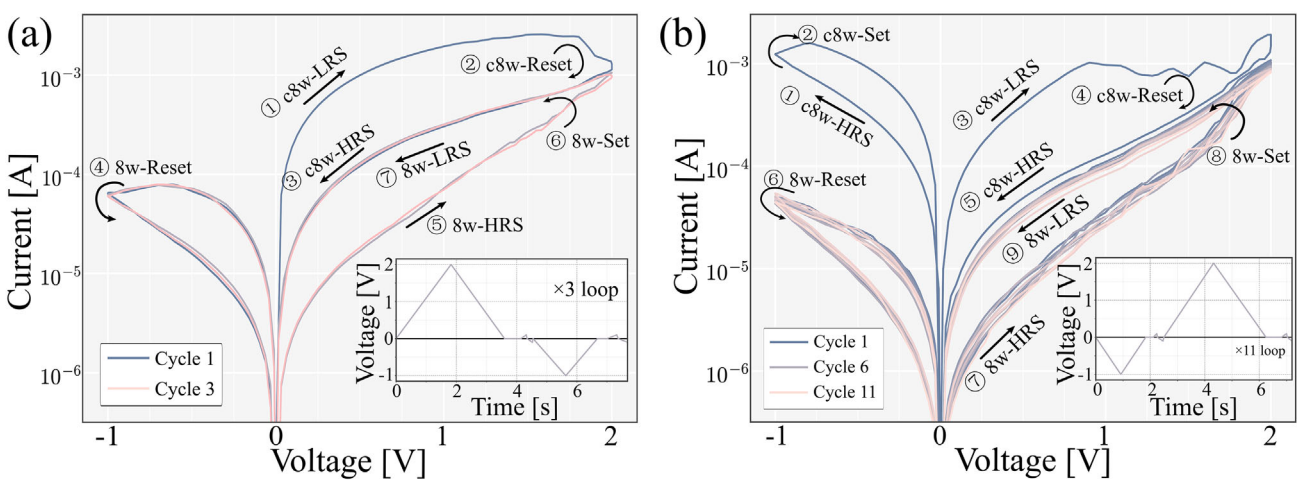


FIGURE 2 | Activation of a 400 × 400 μm^2 device with 5 nm Ta_2O_5. (a,b) I–V evolution under positive-first (a) and negative-first (b) sweep sequences, showing the transition from the pristine high-conductance c8w-like response to the stabilized 8w state. The insets show the applied voltage waveforms and repetition numbers.

switching behavior. Reducing the thickness to 7–8 nm (Figure 1d) leads to a transition in the switching behavior: the devices begin to show area-dependent switching with an eight-wise (8w) pinched hysteresis direction, indicating a shift from diode/filament-type toward a near-area-type transitional transport regime.

However, this regime remains dominated by parasitic charging, as indicated by the stable current minimum shifted from zero to approximately +1 V. Such a zero-offset, together with the accompanying rectifying behavior, suggests a parasitic interfacial charging contribution superimposed on the resistive-switching response. Because this offset can drift as the interfacial charge distribution relaxes, it compromises the reliability of the low-bias readout for samples having Ta_2O_5 thicknesses in the 7–8 nm regime. Slowly relaxing interfacial charges can generate an internal field that displaces the current minimum away from

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0 V so that compensation is reached only when the inert electrode is biased sufficiently positively. Consistent with this picture, the limited number of studies using oxides in this thickness regime reporting similar 8w area-type loops also exhibit pronounced charging artifacts, strong rectification, and transport characteristics more consistent with Poole–Frenkel emission (PF) or Schottky emission (SE) than with tunneling [23]. The offset and self-rectifying characteristics of this 7–8 nm regime resemble previously reported non-filamentary Ta_2O_5 devices, whereas the near-pinched and nearly symmetric response emerging at 5–6 nm was not identified in those studies [21, 22, 24].

By contrast, the devices having 5–6 nm thick Ta_2O_5 in Figure 1e exhibit nearly polarity-symmetric I–V loops, with resolvable pinched hysteresis within the operating window. In addition, the devices retain stable area-scaled switching together with continuous and reproducible conductance tuning. These features indicate that parasitic charging is strongly suppressed in this thickness range. The observed behavior is therefore consistent with substantially faster charge re-equilibration and transport that is tunneling-dominated, or at least tunneling-enhanced, rather than emission-dominated. A notable parallel has previously been reported for a TiN/HfO_2/Pt device with a 5 nm HfO_2 layer, which showed similar switching behavior [25]. This cross-material similarity suggests that a related balance between thickness-dependent electronic transport and oxygen-related defect redistribution may also occur in other ultrathin oxides. In sufficiently thin films, activation may establish a stabilized defect configuration, after which transport within the operating window becomes increasingly tunneling-dominated, while stronger ionic redistribution may re-emerge when the applied bias exceeds this range. Although the present results do not prove a universal mechanism, this cross-material similarity suggests that the interplay between oxide thickness, tunneling transport, and switching behavior may also be relevant in other ultrathin oxide systems. The 5–6 nm regime identified here therefore represents an experimentally accessible operating regime in Ta_2O_5 and motivates further investigation of similar thickness-dependent behavior in other ultrathin oxides.

In the 3–4 nm thickness range, the results shown in Figure 1f indicate pronounced leakage, corresponding to near-short-circuit-like behavior with negligible rectification and the absence of controllable resistance modulation. These observations suggest that transport is likely dominated by direct tunneling (DT) through the reduced effective insulating thickness. We attribute this apparent shorting already at a nominal thickness of 4 nm to the high oxygen reactivity of the TiN electrode, which promotes interfacial reduction and gives rise to a quasi-metallic suboxide-like region [26]. This highly defect-rich layer effectively reduces the insulating thickness of the oxide. Nevertheless, we admit that the large device area versus the identified thickness after ALD deposition is in the range 5 orders of magnitude. In this context it is not only surface roughness but also barely detectable clusters of defects that may additionally increase the probability of shorts. The near-short-circuit-like behavior observed at a nominal thickness of 4 nm may therefore suggest that the reduced oxide region is smaller, possibly on the order of 2–3 nm, while the effective thickness may still modulate dynamically under an applied electric field. Based on ultrathin scaling of HfO_2 [27], we assume that oxide materials have the potential for further miniaturization down to the angstrom scale, provided the electrodes are scaled and designed appropriately.

Among the investigated devices, the 5 nm devices provide the clearest near-area-type switching behavior, with negligible zero offset, highly symmetric I–V characteristics, and more stable low-bias readout. We therefore focus the remainder of this work on the 5 nm devices (measured thickness: 5.24 nm) and further analyze their electrical characteristics and the mechanism causing the resistive switching.

2.2 | Activation and Area-Type Operation of 5 nm Ta_2O_5 Devices

2.2.1 | Activation of the Device

Fresh 5 nm devices initially show a high-conductance counter-eight-wise (c8w)-like loop and evolve into a stable eight-wise (8w) loop after one positive bias sweep. This evolution resembles an initial conditioning process, but the transition occurs gradually during the first positive sweep, without an unusually high forming voltage or an abrupt current jump. We therefore refer to it as activation rather than conventional filamentary forming. Figure 2a,b directly shows this process under two different sweep orders.

As shown in Figure 2a, the first sweep applied in the positive programming direction exhibits an unusually high current, approximately one to two orders of magnitude above the subsequent stabilized operating range. Once the voltage exceeds approximately +1.2 V, the current begins to decrease and gradually converges onto the stable 8w branch near +2.0 V. Reversing the sweep order does not eliminate the initial high-conductance response, as shown in Figure 2b. The preceding negative sweep causes only a modest conductance increase, while the subsequent positive sweep again drives the device toward the same stabilized branch. The initial high-conductance state is therefore a reproducible feature of the pristine device rather than an artifact caused by the sweep order.

Oxygen-ion migration in amorphous Ta_2O_5 has been reported to become appreciable at electric fields of approximately 2.8 MV cm^{-1} [28]. For a 5 nm oxide, +1.2 V corresponds to an average field reaching 2.4 MV cm^{-1}, close to the field range associated with the onset of activation in Figure 2. This agreement suggests that the activation process involves field-driven redistribution of oxygen-related defects. This redistribution is therefore mainly associated with the initial activation and the high-field boundary, whereas the subsequent low-field transport of the stabilized device is analyzed under a largely frozen ionic/defect configuration. The XPS and Au-electrode experiments supporting this interpretation are discussed together with the mechanism in Section 2.4.2.

After activation, the c8w-like response and the pronounced I–V drift do not reappear within the defined operating window. Unless explicitly stated otherwise, all measurements discussed below refer to this stabilized 8w state.

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2.2.2 | Electrical Performance of the Stabilized State

The 5 nm devices exhibit clear and pronounced area-dependent switching. Area-scaling measurements were performed using devices with edge lengths of 300, 400, and 500 μm.

Area-scaling tests were performed over 10 switching cycles under a fixed write window of -0.8 to +3.0 V. For each cycle, the HRS and LRS conductances extracted at -0.1 V were plotted against device area, as summarized in Figure 3a. Additional area-scaling data obtained at reset voltages of -0.6 and -1.0 V are provided in Figure S1. Under all three sweep voltages, the HRS and LRS conductances show a strong linear dependence on device area, with the fitted lines passing close to the origin.

Linear fits of conductance versus device area yielded R^2 values above 0.95, confirms the assumption of a strict area-dependent switching and supports a spatially distributed parallel conduction mode. In double-logarithmic representation, the fitted slopes remain close to unity, again with correlation coefficient R^2 above 0.95. The slight sublinearity likely reflects geometric nonidealities, series resistance, and local thickness variations or defects. The active area is defined by the top electrode while the bottom electrode is much larger. As a result, current spreading towards the bottom contact introduces spreading and an additional series resistance, slightly reducing the apparent scaling exponent. Overall, the switching behavior of the 5 nm devices appears to be intrinsically area dependent.

In addition to the area scaling, the 5 nm devices show highly symmetric low-bias readout. For 400×400 μm^2 cells, read currents at +0.1 V and -0.1 V were measured after programming between -1.0 and +2.0 V, and the corresponding cycle-by-cycle resistance values were extracted, as shown in Figure 3b. The resistances obtained at the two read polarities agree within the observed cycle-to-cycle scatter, indicating near-ideal read symmetry within the low-bias window and the absence of pronounced zero-offset or rectification. This makes the state extraction highly reliable for analog weight evaluation.

Devices from the same fabrication batch further show selective control of the LRS and HRS through the set and reset voltages, respectively. The cycle-to-cycle (C2C) I-V characteristics of 5 nm, 400×400 μm^2 devices were measured by fixing one write polarity while gradually varying the other. After each cycle, resistances were read at +0.1 and -0.1 V, and the average of the two read polarities was used to calculate the on/off ratio. Cycle-to-cycle (C2C) variability was quantified as the standard deviation of read-resistance divided by the mean. In the above given figures, the median I–V trajectory is highlighted without transparency, while the remaining cycles are shown with reduced opacity to emphasize the overall voltage-dependent trend. Figure 3c shows the results obtained by fixing the set voltage at +1.5 V and varying the reset voltage, whereas Figure 3d shows the opposite case, with the reset voltage fixed at -0.9 V and the set voltage gradually increased. In both measurements, the device retained clear analog hysteresis, while the set voltage mainly controlled the LRS and the reset voltage mainly controlled the HRS.

As shown in Figure 3c,d, the resistance states change approximately linearly with programming voltage within the investigated range. In Figure 3c, at fixed set bias, the LRS remains nearly unchanged for different V_{reset}, whereas the HRS increases nearly linearly with increasing reset amplitude, leading to an expanded hysteresis window and larger on/off ratio. Conversely, in Figure 3d, at fixed reset bias, the HRS remains essentially constant for different V_{set}, whereas the LRS gradually decreases with increasing set amplitude, again enlarging the hysteresis window and on/off ratio. These results indicate that, within the studied voltage range, the set bias primarily controls the LRS, whereas the reset bias mainly determines the HRS, enabling continuous and nearly linear analog weight updates.

The reproducibility of the switching behavior within the 5–6 nm thickness range was verified across five independently fabricated ALD batches, all of which showed consistent, nearly symmetric switching loops and the same voltage-dependent resistance trends. Each batch contained about 10 wafer pieces, with more than 20 devices measured per wafer. Although around 10% of the devices were shorted, most likely due to particle contamination before metallization or defect-assisted tunneling paths, the most devices in the stabilized switching regime showed C2C values below 0.03 and highly reproducible analog switching.

This analog programming window is restricted asymmetrically on the negative and positive bias sides. When the reset voltage exceeds -1.2 V, corresponding to a negative field of about 2.4 MV/cm, the device undergoes an irreversible transition from gradual area-type (8w) switching to abrupt, filament-dominated counter-eight-wise (c8w) switching, permanently degrading its analog performance (Figure S2). This indicates that oxygen-vacancy migration becomes dominant at sufficiently high negative field. By contrast, increasing the set voltage does not readily trigger filament formation, but set voltages above +3.0 V lead to pronounced C2C fluctuations, while set voltages above +4.0 V cause severe interfacial degradation and eventual shorting. On the other hand, programming becomes ineffective when either the set or reset voltage is too small. Near-ideal area-type switching therefore exists only within a confined programming window defined by asymmetric failure thresholds. The physical origin of these bias limits is discussed further in Section 2.4.2.

2.3 | Transport and Switching Kinetics of the Stabilized State

2.3.1 | Low-Bias Transport Characteristics

To investigate the transport mechanism in the low-bias read regime of the nearly polarity-symmetric, continuously tunable switching state, we first established a simple timescale constraint from the baseline device impedance. For the 500×500 μm^2 devices, a preliminary instrument check indicated a capacitance on the order of 100 pF. Together with the low-bias resistance of approximately 1–10 kΩ, this gives an estimated RC time constant in the sub-microsecond range, well below the read-pulse duration. This order-of-magnitude estimate suggests that capacitive charging is unlikely to dominate the stabilized low-bias response. The subsequent transport analysis therefore focuses on conduction within the read window [29–31].

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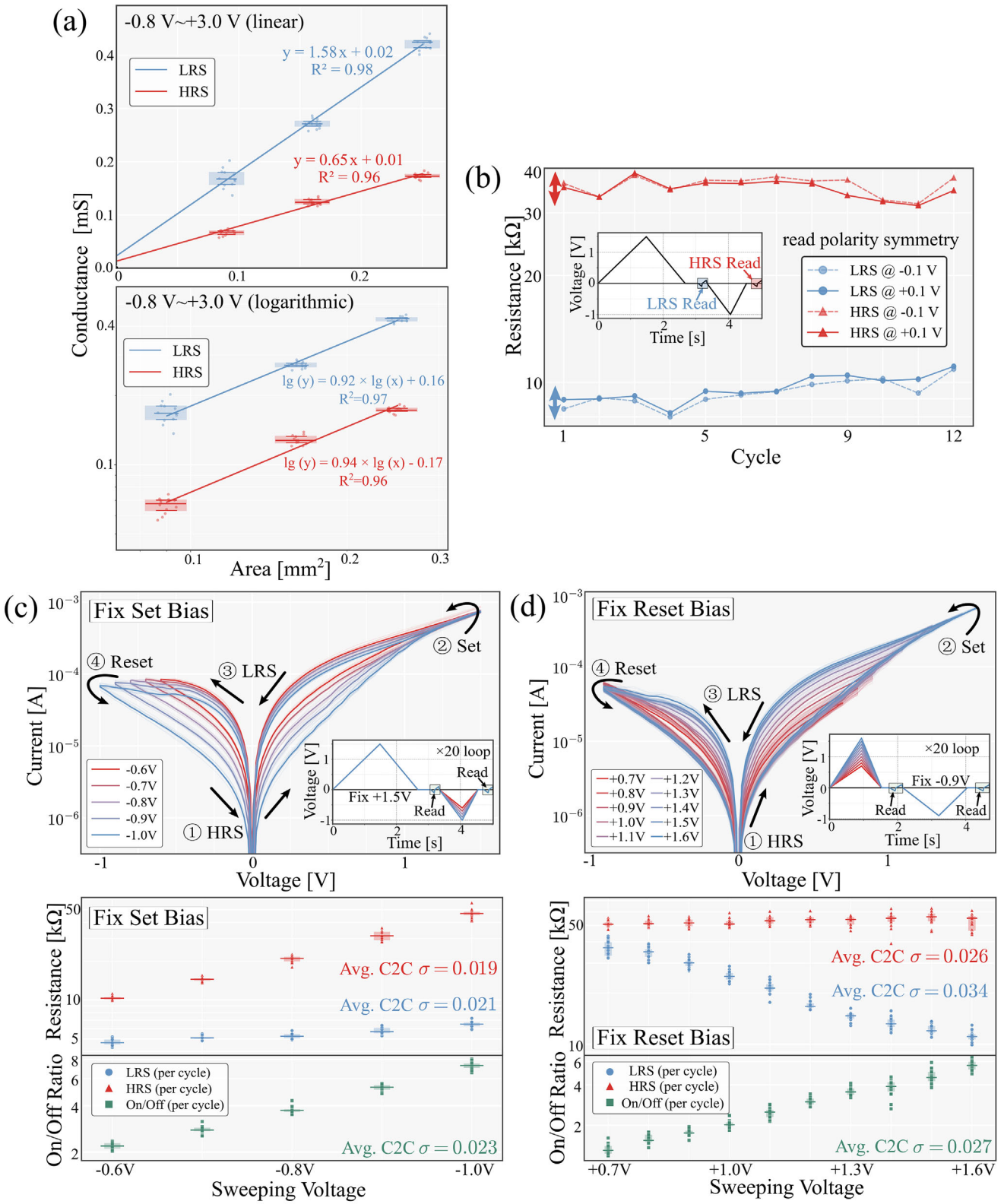


FIGURE 3 | Area scaling and analog tuning of devices having 5 nm of Ta_2O_5. (a) Area-dependent Conductance for the set and reset states obtained after applying voltages from −0.8 V (reset) to +3.0 V (set) plotted on a linear-linear scale (top graph) and logarithmic- logarithmic scale (bottom graph) conductance axis. (b) Cycle-to-cycle HRS and LRS values extracted at +0.1 V and -0.1 V as a function of the number of performed switching cycles at −0.8 V to +3.0 V. (c,d) Switching curves (top graphs) using fixed set bias of +1.5 V (c) and a fixed reset bias of −0.9 V with a varied maximum reset (c) and set (d) bias measured on a 400 × 400 μm² device. The bottom graphs show the memory window as a function of the maximum reset (c) and set (d) voltage extracted from the results of the I–V curves in the top graphs.

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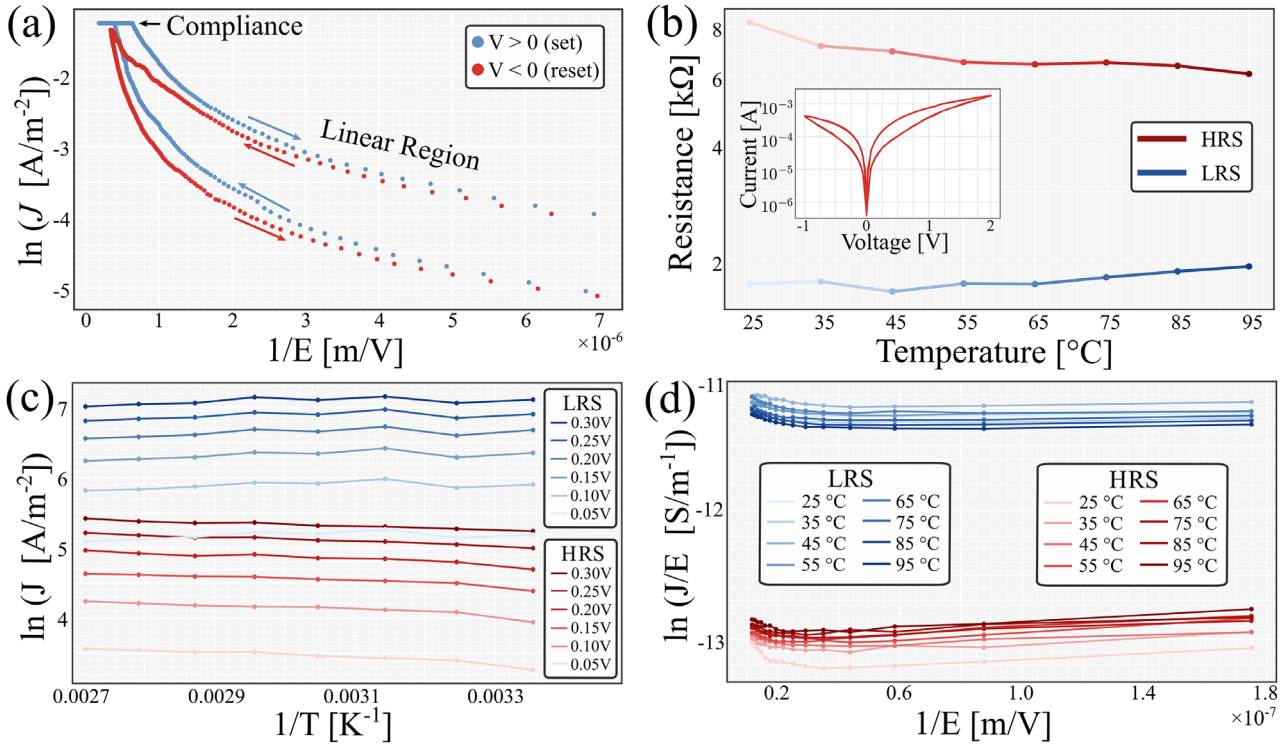


FIGURE 4 | Transport analysis of the device having 5 nm thick Ta_2O_5. (a) $ln(J)$ versus $\frac{1}{E}$ for the set and reset branches. (b) Temperature-dependent resistance. The inset shows a representative I–V sweep. (c) Arrhenius plots of the read current extracted at different read biases. (d) Temperature-dependent $ln\left(\frac{J}{E}\right)$ versus $\frac{1}{E}$ plots.

We then examined the field dependence of the read current by replotting the I–V data as $ln(J)$, $ln\left(\frac{J}{E}\right)$, and $ln\left(\frac{J}{E^2}\right)$ versus 1/E (Figure 4a; Figure S3). In the low-voltage region ($|V| < 0.5$ V), the $ln(J) - \frac{1}{E}$ representation shows the clearest quasi-linear behavior for both the set and reset branches, whereas systematic deviations from linearity become more evident at higher bias. This behavior suggests that the readout regime is governed mainly by an exponential field dependence, consistent with field-assisted tunneling-like transport [29, 32]. To test whether the same behavior could instead be explained by thermally activated emission, HRS and LRS were programmed at -1 and +2 V, respectively, and then read within a narrow low-bias window from -0.2 to +0.3 V (0.1 V each point) in a temperature range from 25°C to 95°C (Figure 4b). Under these conditions, the LRS remains nearly unchanged with temperature, while the HRS conductance shows only a slight increase. The corresponding Arrhenius plots of the read current, shown in Figure 4c, exhibit positive but very small slopes for both states, indicating that thermal activation makes only a limited contribution in this bias range. Together with the weak rectification, the pinched hysteresis, and the stable low-bias readout observed experimentally, these results do not support a conduction mechanism dominated by thermally activated emission such as PF or SE. Although temperature-dependent measurements extending to cryogenic temperatures would provide a more stringent test, the weak temperature dependence observed over the present measurement range is consistent with a tunneling-dominated contribution. Instead, the low-bias read current is more consistently described by electron-dominated trap-assisted tunneling (TAT), while field-driven ionic motion may still contribute during programming [29, 32–35].

Because TAT involves tunneling via localized trap states, its rigorous description generally requires spatial and energetic integration over trap position, trap-energy distribution, trap occupancy, and field-induced barrier deformation. Therefore, unlike PF emission or Fowler-Nordheim tunneling (FNT), TAT does not provide a single universally accepted diagnostic non-integrated form of equation for all trap distributions and device geometries. For a compact and phenomenological description of field-assisted trap-mediated conduction, the current density is commonly expressed in the empirical form [29, 35–38].

$$J_{TAT} \propto E^m \exp\left(-\frac{B}{E}\right)$$

where B and m are fitting constants, and E is the electric field strength estimated from the applied voltage divided by the nominal Ta_2O_5 thickness. A free-exponent compact-model fit to the same device data, presented later in Section 2.5, yields an exponent $m \approx 1$. Therefore, for the present diagnostic replot, we plot the temperature-dependent read-current data as $ln(\frac{J}{E})$ versus $\frac{1}{E}$, as shown in Figure 4d. This transformation is directly applied to the low-bias part of the temperature-dependent I–V data shown in Figure 4c, corresponding to the original read-voltage window from +0.05 to +0.30 V. After transformation, the data remain approximately linear over the measured temperature interval. Together with the weak temperature dependence, this behavior supports a field-modulated TAT contribution to the low-bias read transport in this nearly symmetric, continuously switching device [32–38].

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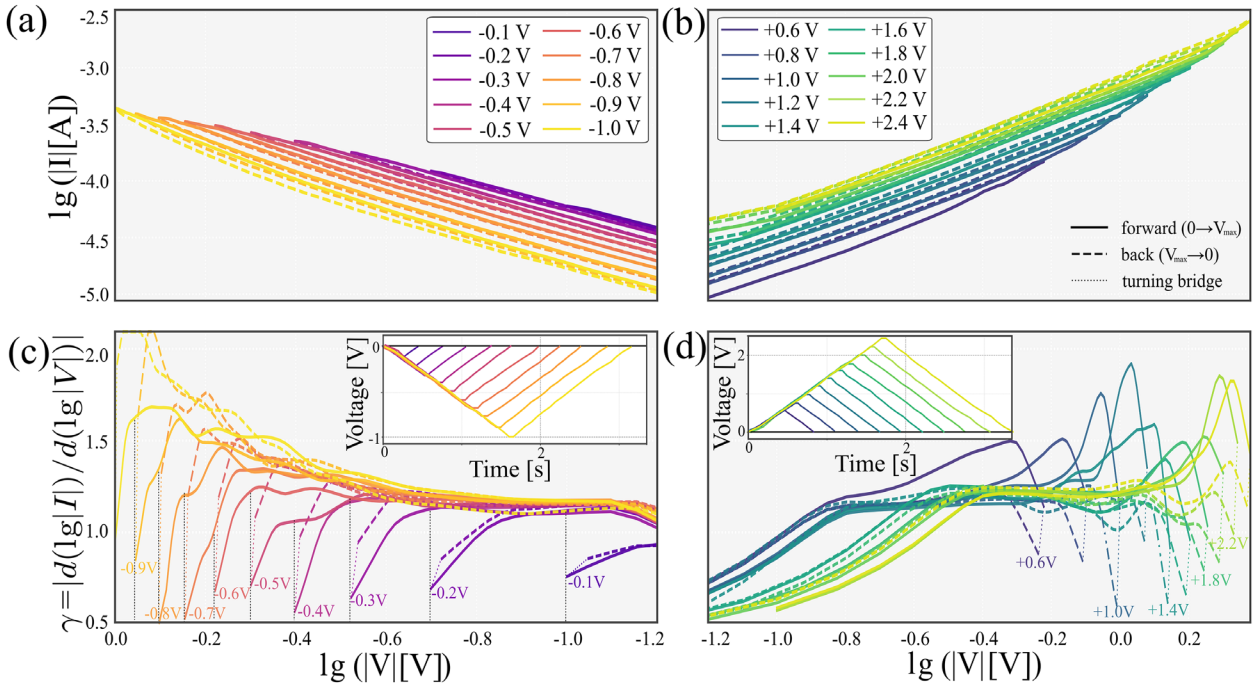


FIGURE 5 | Power-law analysis of the continuous trap-mediated switching process. (a,b) Double-logarithmic I–V characteristics of the reset (a) and set (b) branches under progressively increased voltage limits. Solid and dashed lines denote the forward and backward sweeps, respectively. (c,d) Corresponding extracted exponent γ for the reset (c) and set (d) operations. The insets show the applied voltage sequences.

2.3.2 | Bias-Dependent State Evolution

To resolve how the device state evolves with programming bias, the I–V curves measured under reset voltages from 0 to -1.0 V with a step size of 0.1 V and set voltages from +0.6 to +2.4 V with a step size of 0.2 V were plotted on double-logarithmic axes, as shown in Figure 5a,b. A linear curve in a double-logarithmic plot points towards a power-law exponent and the exponent γ can be deduced from the slope of the curve according to

$$\gamma = \frac{d\log_{10}|I|}{d\log_{10}|V|}$$

γ is extracted in Figure 5c,d, with solid and dashed lines denoting the forward and reverse sweeps, respectively.

At low biases, the applied bias mainly probes the present conductance state and causes only little measurable change in the resistance state. In this voltage range, the trajectories from successive cycles remain nearly parallel, and γ stays close to 1, consistent with near-ohmic readout transport [39, 40]. At the same time, the evolution of the resistance state is clearly not confined to the highest programming voltages. Even under relatively small set or reset biases, γ already departs from unity over part of the sweep window, and these deviations are accompanied by measurable conductance changes. These results show that measurable state evolution begins progressively before the maximum programming voltage is reached.

A second prominent feature is the dependence of the device state on the previously applied maximum voltage. Once the device has been programmed to a given maximum bias, subsequent sweeps that do not exceed that previously applied amplitude produce almost no further change in either γ or the conductance state. Additional switching appears only when the bias is extended beyond the previous maximum or when the polarity is reversed. This behavior indicates that further resistance changes occur mainly when the applied voltage exceeds the previously reached maximum. Taken together, the early deviation of γ from unity, the incremental conductance changes over successive voltage steps, and the maximum-voltage dependence indicate progressive access to a distributed set of switching states. Increasing electric field may activate deeper trap subpopulations or states with higher effective barriers, accounting for the voltage-dependent conductance evolution observed in Figure 3c,d [41]. The complete bias-dependent I-V family is therefore used in Section 2.5 to calibrate the state-dependent terminal-current branch of the compact model.

At higher bias, however, the transport behavior changes. For reset sweeps V_{reset} with voltages up to about −0.4 V and set sweeps with V_{set} voltages above +1.2 V, γ shows a much stronger increase and significantly departs more clearly from unity, indicating that the low-field near-ohmic conduction component alone is no longer sufficient to describe the state-update switching process. Instead, an additional high-field contribution becomes important. In view of the preceding low-bias transport analysis, this contribution is most plausibly associated with field-enhanced tunneling, such as FNT, which gradually emerges alongside low-field TAT and becomes more influential as the electric field is increased [42, 43].

2.3.3 | Pulse-Programming Kinetics

Pulse-programming measurements further reveal strongly asymmetric yet continuously evolving switching kinetics. As shown

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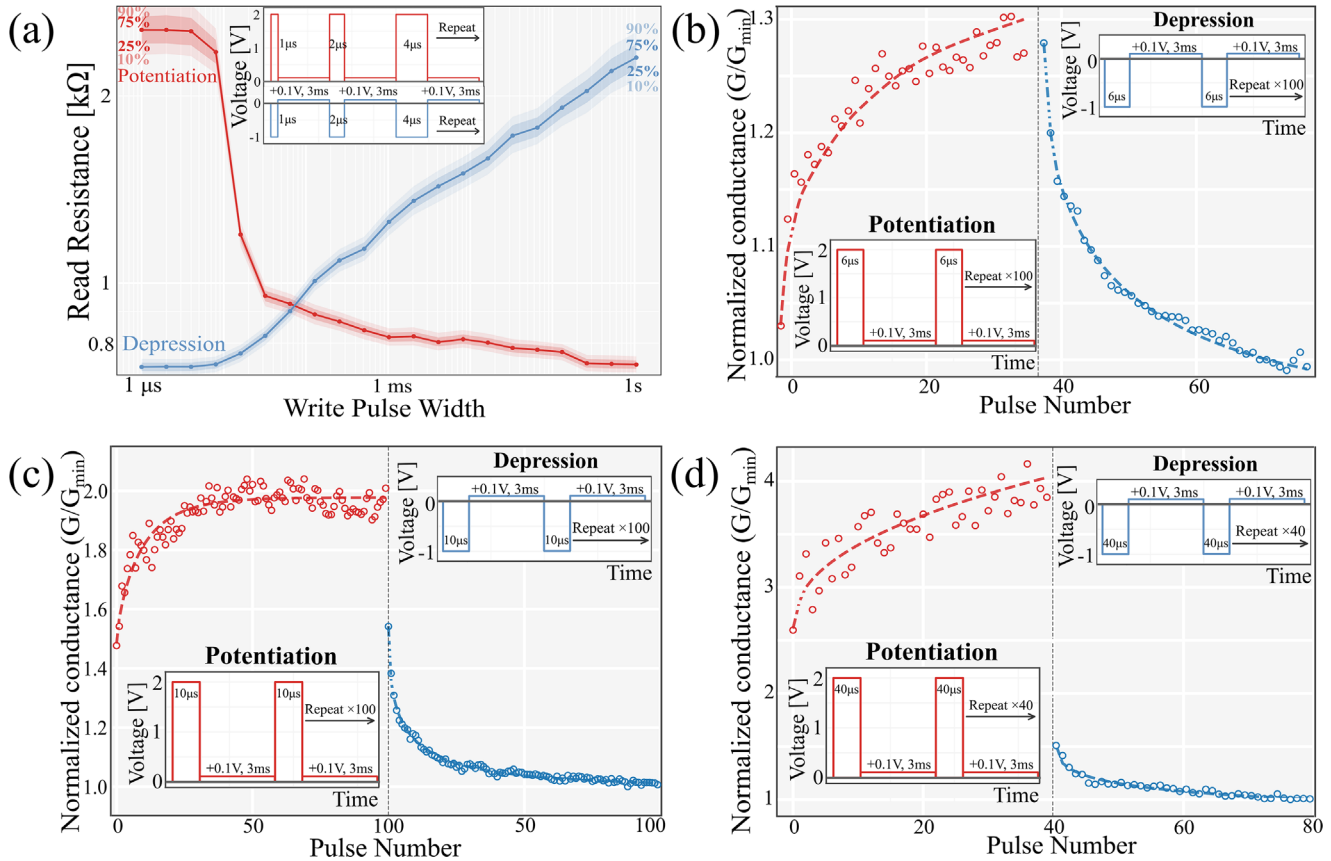


FIGURE 6 | Pulse-width- and pulse-number-dependent cumulative programming characteristics. (a) Read resistance as a function of write-pulse width using a fixed-write-pulse amplitude of +2 V for potentiation and -1 V for depression. (b–d) Normalized conductance as a function of pulse number under cumulative programming with fixed write pulse amplitude of +2 V for potentiation, -1 V for depression and widths of 6 (b), 10 (c), and 40 µs (d), respectively. The insets show the corresponding pulse schemes used in the experiments. Potentiation and depression denote cumulative conductance increase and decrease, respectively.

in Figure 6a, cumulative programming experiments were performed at fixed pulse amplitudes, with potentiation at +2 V and depression at -1 V, while the write-pulse width was increased in exponential steps from 1 µs to 1s. Here, potentiation and depression simply denote cumulative conductance increase and decrease, corresponding to repeated set and reset operations, respectively. After each programming pulse, the device state was read using a +0.1 V read pulse for 3 ms. Under these conditions, potentiation shows a clear delayed onset: little change is observed at the shortest widths, followed by an apparent transition at approximately 8–10 µs, beyond which the resistance decreases rapidly and then continues to decrease more gradually at longer pulse widths. Depression, in contrast, evolves more smoothly over the full-time range, with the resistance increasing nearly linearly as the pulse width increases and no abrupt transition is observed.

A second important feature is that neither potentiation nor depression reaches full saturation even when the write-pulse width is extended to 1 s. Instead, both branches continue to increase/decrease over the entire accessible time window, indicating that the switching process is not governed by a single characteristic timescale. To examine this behavior further, cumulative pulse-programming measurements were performed using pulse widths of 6, 10, and 40 µs at fixed amplitudes of +2 V for set and -1 V for reset, as shown in Figure 6b–d.

All three pulse widths produce clear set/potentiation and reset/depression trajectories, demonstrating that the device state can be effectively tuned both by changing the individual pulse width and by repeated pulsing.

The three fixed pulse widths were selected around and beyond the apparent onset of measurable conductance modulation identified in the pulse-width-dependent measurement. At 6 µs (Figure 6b), the pulse width is slightly below the onset of efficient conductance programming, yet repeated pulses still produce a clear cumulative conductance increase. At 10 µs (Figure 6c), the pulse width lies close to the rapid-onset region, leading to a stronger conductance change per pulse while the conductance still evolves progressively with pulse number. At 40 µs (Figure 6d), the pulse width is already beyond this onset region, but the potentiation branch remains unsaturated and continues to evolve under repeated pulsing. This confirms that the rapid transition around 8–10 µs marks the beginning of efficient programming rather than the completion of the switching process. Overall, the device state can be tuned by the write-pulse width and the accumulated pulse number, while the pulse amplitude was intentionally kept fixed. Although increasing the pulse amplitude, as in incremental-step pulse programming, may accelerate the update, the usable amplitude range is limited by the need to remain within the stable analog switching regime. We therefore focus on pulse-width

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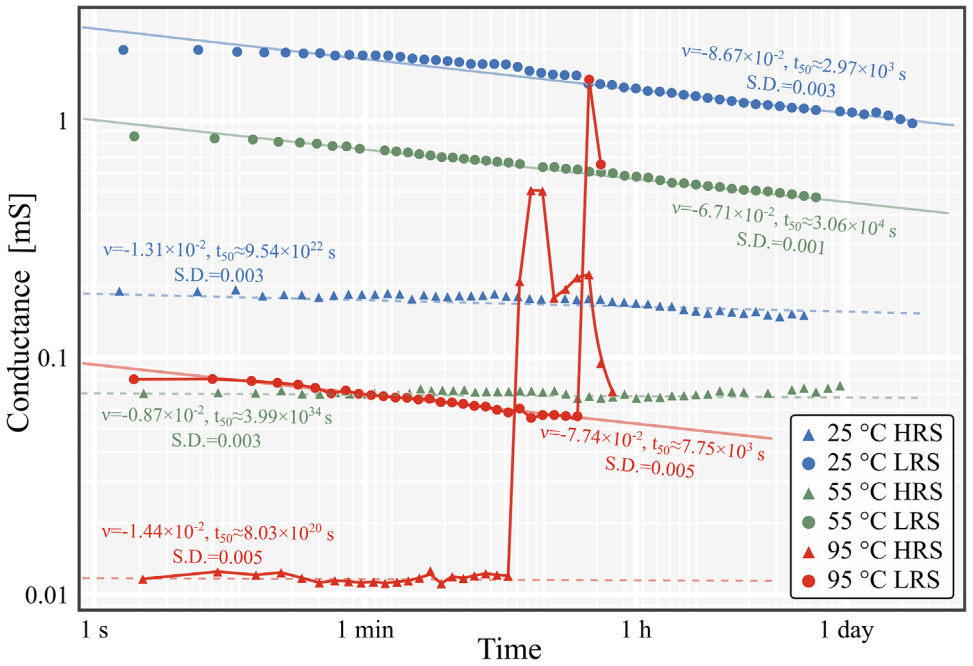


FIGURE 7 | Retention characteristics of the conductance and extraction of the power-law exponent for the 5 nm device.

and pulse-number modulation as a conservative programming approach.

These measurements were performed under ambient illumination. The measurement setup exhibited a capacitive response associated with the connecting wires, which may contribute to the measured transient response. Therefore, the extracted pulse timescale should be regarded as an effective experimental timescale rather than the intrinsic device-switching time [44]. Taken together, the delayed but rapid onset of potentiation, the smoother depression branch, and the absence of full saturation within the measured window indicate distributed switching-kinetics rather than a single discrete switching event. This behavior is consistent with a broad distribution of internal defect-state depths and transition barriers [45–47]. The delayed onset of potentiation and the smoother depression branch may reflect different effective activation barriers, which will be further examined in the compact-model analysis below. These asymmetric pulse-programming kinetics provide the experimental basis for calibrating the state-evolution branch of the compact model in Section 2.5.

2.3.4 | Retention and Dispersive Relaxation

In retention measurements, the 5 nm devices show a pronounced asymmetry in HRS/LRS relaxation, while the high- and low-resistance states remain clearly distinguishable over several days. Specifically, the devices were first programmed into the reset state at -1.0 V and the set state at +2.0 V, and then read for up to several days at 25°C, 55°C, and 95°C. The results are summarized in Figure 7. The most direct observation is that, in double-logarithmic coordinates, the read conductance decreases approximately linearly with time rather than following an exponential decay with a single characteristic time constant. The drift exponent ν was quantified using

$$\nu = \frac{\Delta \log G}{\Delta \log t}.$$

For the 95°C data, only the data acquired before the abrupt resistance change was used for power-law fitting. All datasets show very small fitting errors (standard deviation < 0.05), indicating that the relaxation is well described by a power law. Such power-law relaxation does not correspond to a single barrier or a single time constant but instead points to a continuous distribution of trap energies and/or local barrier heights, where multiple relaxation processes having different time constants are superimposed to produce a characteristic dispersive-relaxation behavior [48]. This defect-state-controlled dispersive picture is also consistent with the low-voltage programmability in Figure 3c,d, the pulse-width-dependent writing behavior in Figure 6a, and the limited retention discussed above. Shallow traps can contribute to conduction already at low bias or under short pulses, but they also relax on relatively short timescales, giving rise to a volatile or partially volatile conductance component. Deeper traps require higher fields or longer pulses to be activated and relax more slowly, thereby contributing to the longer-lived part of the programmed state.

The temperature-dependent retention data further show that temperature mainly shifts the absolute conductance level, while leaving the drift kinetics largely unchanged. For both LRS and HRS, the extracted drift exponents ν remain very similar at 25°C, 55°C, and 95°C. Here, the conductance half-life t_{50} is defined as the time at which the fitted conductance has relaxed halfway from its initial programmed value toward the extrapolated long-time value. For the LRS, this t_{50} remains on the order of hours at all three temperatures, and no clear saturation plateau is observed within the measured retention window. By contrast, the HRS relaxes much more slowly, with extrapolated half-lives far beyond the measured time window; although the drift is

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extremely weak, it is still ongoing. Since the LRS relaxation progressively reduces the separation between the programmed states, the overall memory window should be regarded as partially volatile rather than fully non-volatile. This weak temperature sensitivity is consistent with the low-bias read measurements in Figure 4b,c, but does not by itself exclude thermally assisted trap relaxation; it only indicates that no strong thermally accelerated degradation is resolved within the measured temperature and time range [49, 50].

The much faster relaxation of the LRS compared to the relaxation of the HRS can also be understood naturally within an electron trapping/detrapping picture under tunneling-dominated transport, such as TAT. The LRS corresponds to a higher trap occupancy and stronger parallel conduction pathways and is therefore more sensitive to detrapping and interfacial charge re-equilibration. As these metastable electronic configurations gradually relax, the connectivity of the conduction network is reduced and the conductance decreases accordingly. In contrast, the HRS is closer to an electron-depleted configuration and is therefore intrinsically more stable. Even so, the reset process does not necessarily empty all deep traps completely, so an extremely slow long-term drift may still persist, albeit on timescales far beyond the present experimental window.

It should be noted that the trend in Figure 7, where the conductance decreases with increasing temperature, does not contradict the nearly temperature-independent readout observed in Figure 4b,c. The two measurements probe different processes. In Figure 4, the device state was written first and then read at different temperatures under low bias, so the data mainly reflect the temperature response of the read operation itself. In the retention experiment, by contrast, instrumental constraints required programming and immediate readout at the target temperature, so elevated temperature affects not only the readout but also the initial programmed state. Figure S4, which compiles the sweep data and corresponding Arrhenius analysis from 30 to 80°C, likewise shows that higher programming temperature leads to an overall increase in resistance. The origin of this effect is discussed further in Section 2.4.1. In addition, the 95°C retention data show a qualitatively distinct anomalous behavior, indicating that contributions beyond the purely electronic relaxation picture begin to emerge under these conditions; this point is addressed separately in Section 2.4.3. For completeness, Table S1 compares the present device with representative non-filamentary Ta_2O_5 memristors in terms of conventional device metrics and switching characteristics.

2.4 | Mechanisms of the Pristine and Stabilized States

2.4.1 | Electronic Trap-Mediated Switching in the Stabilized 8w State

Taken together, the preceding transport, switching kinetic, and retention measurement results point towards an electronically dominated switching mechanism. Within this framework, the observed behavior can be described by TAT. Oxygen-vacancy-related defects are considered a plausible origin of the trap states that modulate the resistance through electron capture and release, although the specific microscopic defect configuration cannot be uniquely identified from the present measurements [51, 52]. Transport then involves electrode injection, trap occupation, and subsequent trap-mediated hopping or emission [3, 53]. Because the energy barriers associated with electron traps make electron capture faster than electron release, detrapping is expected to be the rate-limiting step [38, 54, 55], consistent with the asymmetric potentiation/depression kinetics observed in the pulse-programming measurements.

In the asymmetric electrode structure used here, the reactive-contact TiN side makes a nearly ohmic contact to the Ta_2O_5 while the Pt electrode exhibits more Schottky-like injection characteristics [56]. The corresponding HRS/LRS states and set/reset processes are schematically illustrated in Figure 8. When a positive bias is applied to the Pt electrode, electron injection from the ohmic TiN contact and subsequent trapping in the oxide are favored over electron detrapping, leading to a net increase of the number of traps filled with electrons, progressively strengthening trap-assisted transport pathways, and resulting in the LRS (Figure 8, (1) to (2)) [3, 57]. Under the opposite bias, by contrast, electron injection from the Schottky-like side is suppressed, while electron detrapping and extraction toward the ohmic side becomes more favorable resulting in the HRS state (Figure 8, (3) to (4)) [3, 57].

A higher set bias injects more electrons and enhances net trapping, thereby reducing the resistance and driving the device toward the LRS. Conversely, a higher reset bias promotes electron release and extraction, thereby increasing the resistance and driving the device toward the HRS. This mechanism is also consistent with the area-dependence and the observed 8w hysteresis. As a control experiment, the Pt top electrode was replaced with Ni to reduce the asymmetry between the two electrode/oxide interfaces. In this configuration, the switching window is strongly suppressed, as shown in Figure S5. This result supports an important role of electrode-dependent injection and extraction asymmetry in the switching response. Reducing the injection and extraction asymmetry severely suppresses the switching window.

From a state-variable perspective, the stabilized resistance modulation can be represented by changes in effective trap occupancy, giving rise to pinched hysteresis, and continuously tunable resistance states. Here, near-ideal is used in an operational sense to describe these area-type read/write characteristics within the defined bias window; it does not imply that the device satisfies the strict ideal-memristor relation [5, 58, 59]. Within this scope, the device provides a reproducible analog switching response relevant to weight modulation [60, 61].

The electronic trap-occupancy picture is intended to describe the stabilized switching response within the operating window between -1.0 and +2.0 V, where the measurements are consistent with predominantly electronic trapping and detrapping. At larger electric fields, under prolonged set or reset stress, or at elevated temperature, oxygen-vacancy motion and other defect rearrangements can no longer be neglected. This limitation is particularly important in the ultrathin operating regime, where even a small redistribution of defects can appreciably change the effective tunneling distance and thereby perturb the electronic current. The electronic description should therefore be restricted

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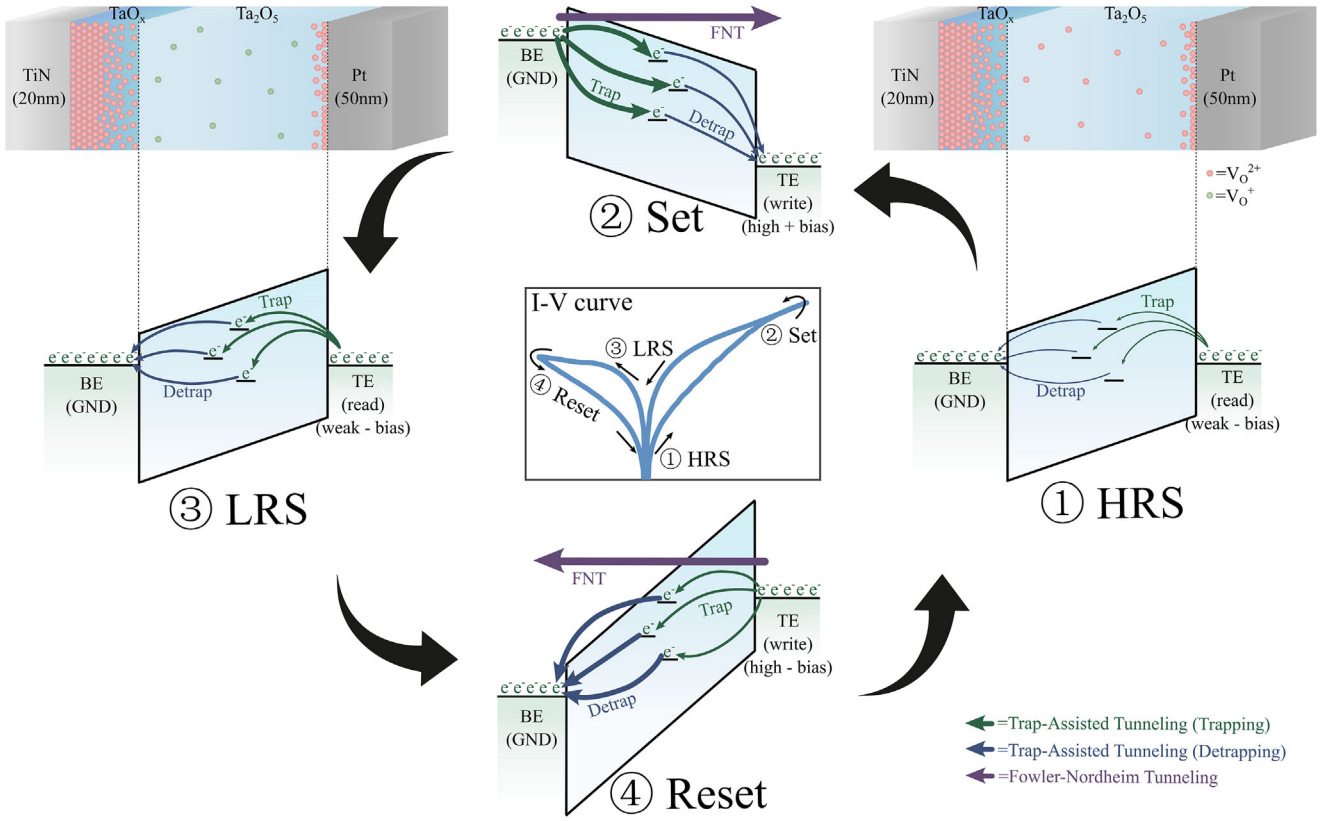


FIGURE 8 | Schematic illustration of the switching mechanism in the device having a 5 nm thick switching layer.

to the defined bias and timescale window. The ionic processes that establish and destabilize this window are considered below.

2.4.2 | Ionic Redistribution Linking the Pristine and Stabilized States

Evidence for an asymmetric defect profile and field-driven oxygen redistribution is provided by the XPS and Au-electrode experiments. Angle-resolved XPS analysis (Figure S6) reveals a depth-dependent distribution of Ta oxidation states already in the pristine film, with a higher fraction of reduced Ta species toward the TiN interface. This result is consistent with a more oxygen-deficient region near the reactive electrode.

To examine whether this defect distribution can be reconfigured electrically, the Pt top electrode was replaced by Au, which has a low oxygen solubility. During a slow positive sweep from 0 to +3.0 V at 1.0 V min^{-1}, bubbles appeared at the initially flat Ta_2O_5/Au interface once the voltage exceeded approximately +2.0 V and subsequently increased in size (Movie S1). This observation is consistent with field-driven oxygen transport and oxygen evolution at the positively biased inert electrode. No macroscopic gas accumulation is observed in the Pt devices, although oxygen-related interfacial redox can still occur and may contribute to the stronger drift observed under high positive bias in Figure S2d.

Taken together, these results suggest that the evolution from the pristine c8w-like response to the stabilized 8w state involves a change in the relative contributions of ionic and electronic processes. The stabilized 8w response is consistent with predominantly electronic trap-mediated modulation, whereas the pristine c8w-like response contains a stronger ionic-redistribution contribution. Both processes may operate during the first sweep, but the larger resistance change produced by defect redistribution initially determines the loop direction. After the defect profile has been reconfigured, the electronically controlled 8w response becomes stable within the defined operating window.

To account for the high pristine conductance, activation into stable 8w switching, and reverse-bias-induced destabilization, the observations are summarized using the ionic-redistribution picture in Figure 9. In ultrathin transition-metal oxides containing a reactive electrode, a reduced and oxygen-deficient region can form near the reactive interface. A TaO_x/TiO_xN_y interfacial region may also form at the TiN side, although its composition and thickness were not measured directly in this work. This region is treated here as an extended defect-rich layer with higher conductivity, rather than as the localized filamentary channel assumed in the disk model of reference [4]. The oxide closer to the inert electrode remains more highly oxidized and less conductive. Its thickness can therefore be regarded as an effective tunneling distance between two electrodes. When this effective oxidized region is thin, direct and high-field tunneling contributions become stronger. As it becomes thicker, these contributions are rapidly suppressed and the relative contribution of trap-mediated tunneling increases [38, 62].

In the pristine state, the higher conductance and c8w-like response suggest that the effective insulating thickness is initially reduced relative to the activated state. A possible explanation

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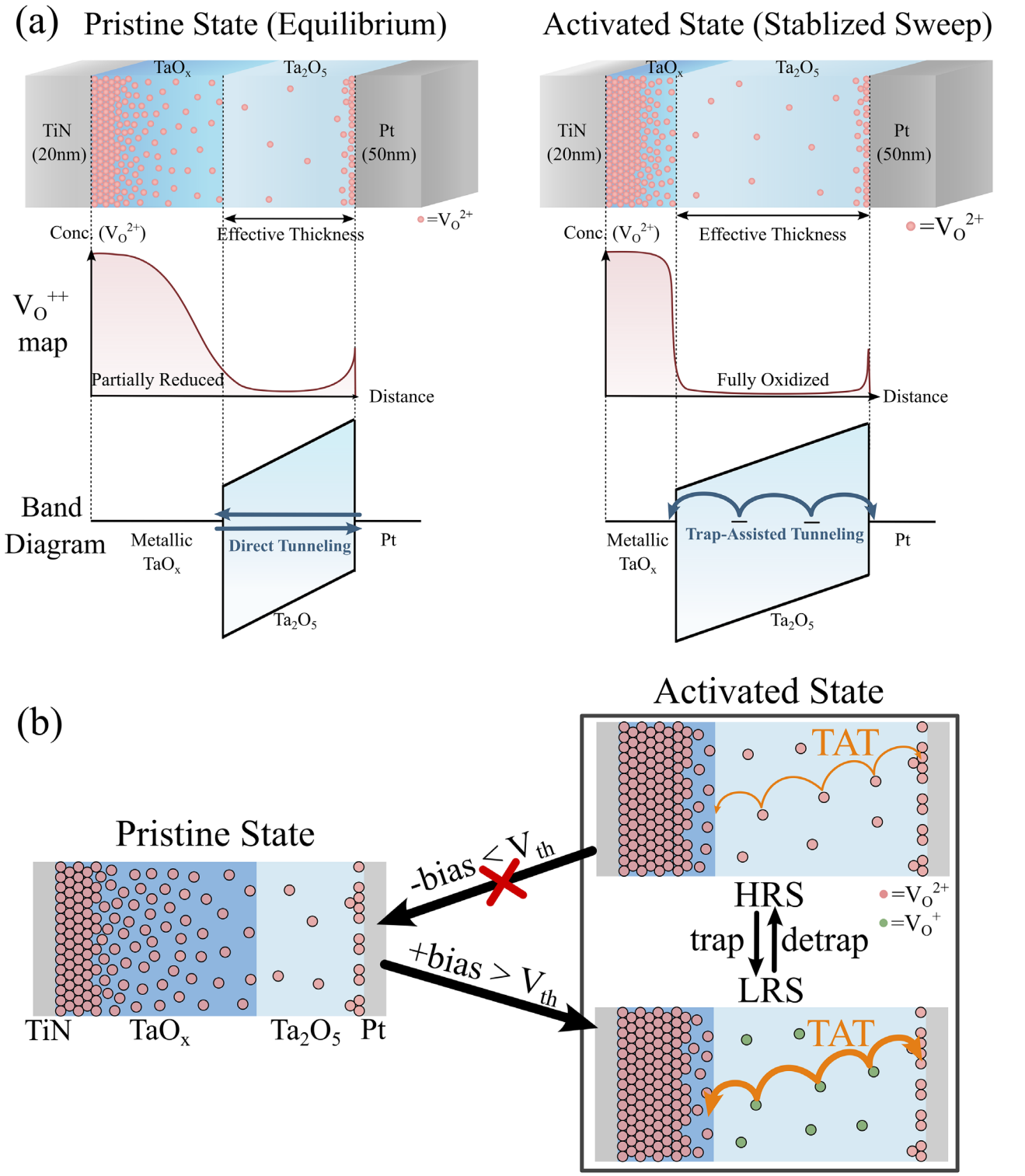


FIGURE 9 | Proposed ionic transport framework for activation and stabilized-state switching. (a) Schematic of the pristine and activated states, showing oxygen-vacancy redistribution and effective insulating thickness evolution. (b) Schematic of activation above the threshold voltage and subsequent electronically controlled switching in the activated state.

is that oxygen ions partially migrate toward the more defect-rich suboxide-like region during ALD and subsequent cooling, forming a quasi-equilibrium defect profile that favors DT/FNT-dominated conduction. When positive bias is applied to the inert-electrode side, oxygen ions are driven from the "metallic" side toward the insulating side, increasing the effective insulating thickness. As a result, the DT/FNT contribution rapidly decreases, TAT becomes dominant again, and the device is activated into its stable operating mode, corresponding to the c8w-to-8w transition illustrated in Figure 2a,b. Conversely, if the opposite-polarity bias exceeds the ionic-migration threshold, oxygen ions are driven back in the opposite direction, destabilizing

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the activated state and returning the device to an ionic-dominated regime, experimentally manifested as c8w behavior, filament-like switching, or increased C2C variability, as shown in Figure S2. This picture directly explains why a restricted opposite-polarity operation strategy is required: the activating bias must exceed the ionic-migration threshold to reconstruct the pristine defect profile and establish the stabilized-state operating mode, whereas the reverse bias must remain below this threshold to prevent the effective insulating thickness from being reduced again. Under this condition, the effective insulating thickness remains essentially unchanged during the positive bias sweep, allowing the device to stay within the near-ideal area-type window, as illustrated in Figure 9b.

Experimentally, stable area-type switching is observed only within a limited programming window (Figure S7). Within this window, the otherwise complex ultrathin-device behavior can be described by the TAT+FNT-based framework summarized in Figure 9b. In this window, the ionic contribution mainly defines the boundary conditions and initial-state reconstruction, whereas the stabilized-state analog switching is governed by electronically controlled transport.

Interestingly, a similar bias-limited area-type switching window has also been observed in our previous 5 nm HfO_2 devices, where exceeding the reset window drives the device into filament-type switching [25]. This similarity suggests that the relationship between operating window and switching regime may merit further investigation in other ultrathin oxide systems, while providing a practical basis for predictive modeling and simulation in the present Ta_2O_5 devices.

2.4.3 | Thermal Boundary of the Near-Ideal Operating Window

The near-ideal operating window is bounded not only by bias but also by thermal stability. This limit becomes evident in the retention data of Figure 7. At 95°C, the device no longer remains in the stabilized-state electronic-storage regime over extended unbiased storage, but instead develops irregular, near-short-circuit-like switching events after tens of minutes, indicating the onset of additional ionic or structural instability. Abrupt conductance changes appear in both HRS and LRS, and repeated measurements rule out an instrumental origin. Notably, these anomalous states are at least partially reversible: applying a positive bias drives the near-shorted device back into an activation-like state, with the I–V curve recovering the pristine-like c8w hysteresis direction before returning to stable switching after reprogramming. This behavior therefore reflects not simple noise, but entry into a regime beyond the stabilized-state electronic model, most plausibly associated with local reactivation induced by thermally assisted defect redistribution.

Similar conductance increases followed by partial recovery during unbiased storage were observed in our previous work [25]. A plausible physical picture is that high-temperature defect diffusion intermittently creates transient tunneling-percolation paths, leading to erratic-bit- or tunneling-stepping-stone-like behavior similar to erratic bits [63] and anomalous stress-induced leakage current or moving bits [64, 65]. Because such phenomena remain rare in memristive systems, a definitive microscopic assignment is not yet possible; the soft-filament or tunneling-stepping-stone picture should therefore be regarded as a qualitative interpretation rather than a uniquely established model. Even so, the effect is clearly characteristic of the ultrathin regime and is largely absent in thicker oxides.

Reducing the lateral device area may also improve thermal stability by lowering the statistical probability of including localized defect-rich regions that initiate abrupt conductance changes. This thermal-stability limit may be mitigated either by moderately increasing the oxide thickness, which significantly delays the abrupt failure at 95°C, or by inserting an ultrathin diffusion-barrier layer, such as a thin Al_2O_3 interlayer, to suppress defect percolation and reduce erratic switching. Ultrathin devices thus offer access to a near-ideal area-type operating window, but at the cost of a narrower thermal-stability margin. Future design must therefore balance writability, analog linearity, and high-temperature robustness.

2.5 | Physics-Based Compact Model of the 5 nm Device in its Stabilized Operation Regime

The preceding analysis establishes a hierarchy of device processes. Ionic redistribution creates the activated state and defines the bias and thermal boundaries of the stabilized operating regime, whereas electronic trapping and detrapping govern the continuous conductance evolution within this regime. The compact model represents this experimentally identified regime through a quantitative digital-twin suitable for device- and circuit-level simulation. Only a few compact models exist for gradual switching memristors such as for NbO_x-based devices [66], possibly because non-ideal charging effects frequently obscure the intrinsic switching dynamics of area-type devices. For the 5 nm near-ideal area-type switching device presented here, we developed an extended memristor model based on the identified physical mechanisms and calibrated it against the measured quasi-static and pulse-switching data.

The compact model is based on a normalized internal state variable x, representing the effective internal configuration underlying the conductance continuum sampled during progressive set and reset operations. Here, $x = 0$ and $x = 1$ correspond to the calibrated HRS and LRS limits, respectively. The state x can be interpreted as a resulting scaling parameter of the internal atomic arrangement related to trap density, electron occupancy, or oxygen-vacancy concentration. The model is calibrated against the quasi-static I–V characteristics and pulse-width-dependent programming data to represent the experimentally defined stabilized operating regime. It cannot describe the pristine c8w-to-8w activation, filament formation outside the safe programming range, long-term zero-bias relaxation, or thermally induced instability.

The compact model can be represented as an extended voltage-controlled memristor given by:

$$I_{model}(V, x) = G(x, V) \cdot V, \quad \frac{\mathrm{d}x}{\mathrm{d}t} = f(x, V).$$

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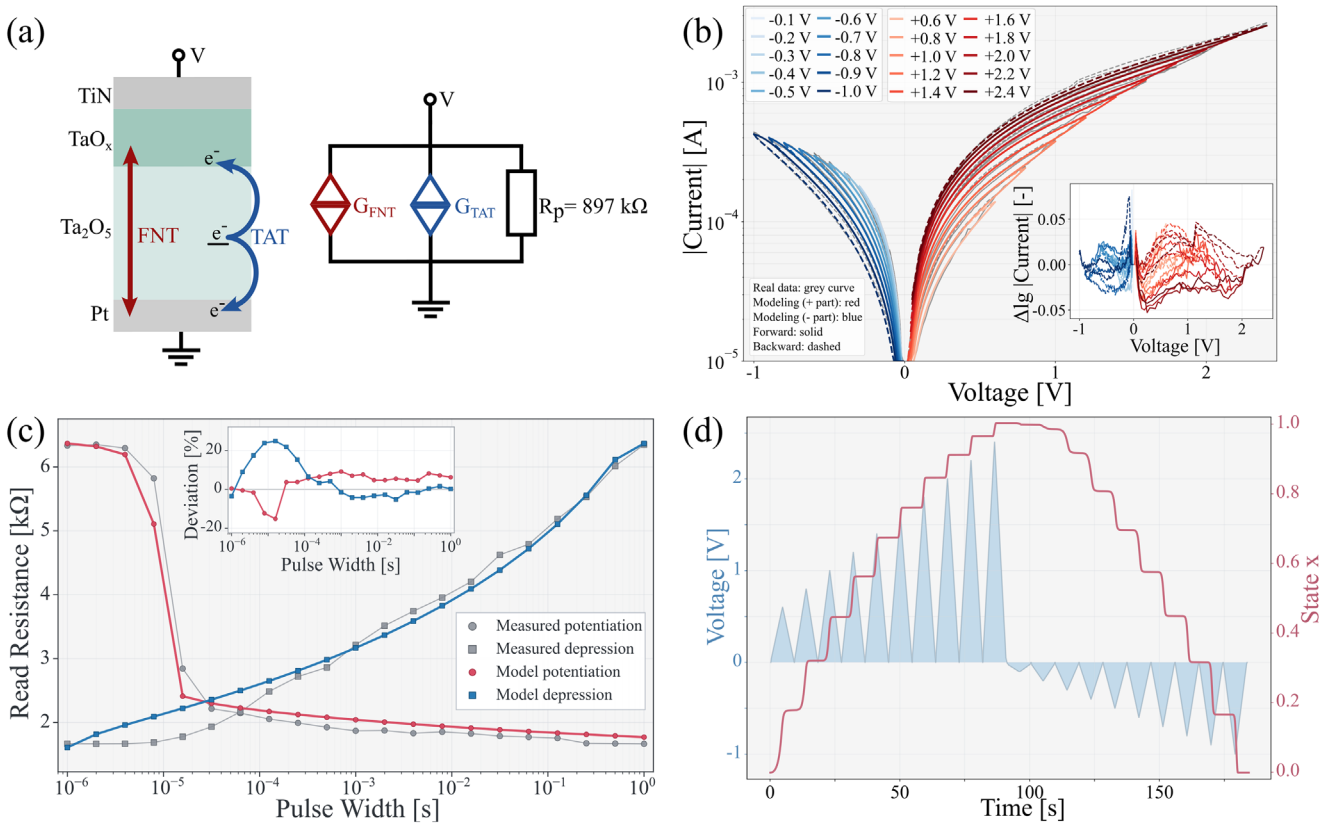


FIGURE 10 | Compact-model representation of the stabilized 5 nm operating regime. (a) State-dependent phenomenological TAT-like and FNT-like transport contributions and the corresponding equivalent-circuit representation. (b) Comparison between the measured and modeled quasi-static I–V family from Figure 5. The inset shows the logarithmic current residual, $\Delta log_{10}|I|$. (c) Comparison between the measured and modeled pulse-width-dependent programming response from Figure 6a. The inset shows a deviation between fitted and real data. (d) Model-inferred internal state trajectory under the experimentally applied voltage sequence. The blue areas show $V(t)$, and the red curve shows the normalized state $x(t)$.

By applying this form of the state-based Ohm's law, I_{model} can be determined for a set (s) and reset (r) voltage polarity as a superposition of TAT and FNT transport mechanisms, given in Figure 10a and represented by:

$$I_{model}\ (V,x) = \begin{cases} \left[J_{\mathrm{TAT},s}\,(x,V) + J_{\mathrm{FNT},s}\,(x,V)\right]\ A_{area} + \frac{V}{R_p} & \text{for } V \geq 0 \\ -\left[J_{\mathrm{TAT},r}\,(x,V) + J_{\mathrm{FNT},r}\,(x,V)\right]\ A_{area} + \frac{V}{R_p} & \text{for } V < 0 \end{cases}, \quad x \in [0,1],$$

where the transport mechanism is defined as

$$J_{\mathrm{TAT},l}\ (x,V) = |V|^{c_{1,l}}\ e^{p_x\left(x,c_{2,1}^{min},c_{2,1}^{max}\right)} e^{-p_x\left(x,c_{3,1}^{min},c_{3,1}^{max}\right)|V|}, \quad l \in \{s,r\}$$

and

$$J_{\mathrm{FNT},l}\,(x,V) = |V|^2 \left(a_{1,l}^{int} + x a_{1,l}^{slp}\right) e^{-\frac{p_x\left(x,a_{2,1}^{min},a_{2,1}^{max}\right)}{|V|}}, \quad l \in \{s,r\}$$

with a state-dependent parameter modulation defined as

$$p_x\,(x,p_{min},p_{max}) = p_{min} + (p_{max} - p_{min})\,x.$$

Here, A_{area} is the device area, V is the applied voltage across the memristor, R_p is the parallel leakage resistance, and $l \in \{s,r\}$ denotes the set and reset branches, respectively. $J_{\mathrm{TAT},l}$ and $J_{\mathrm{FNT},l}$ denote phenomenological trap-assisted-tunnelling-like and Fowler–Nordheim-like current-density contributions, respectively. The parameter $c_{1,l}$ determines the voltage dependence of the TAT-related branch, while $c_{2,1}^{min}$, $c_{2,1}^{max}$, $c_{3,1}^{min}$, and $c_{3,1}^{max}$ define its state-dependent prefactor and state-dependent field modulation factor. For the FNT-like branch, $a_{1,l}^{int}$ and $a_{1,l}^{slp}$ define the intercept and state-dependent slope of the prefactor, whereas $a_{2,1}^{min}$ and $a_{2,1}^{max}$ define the state-dependent field modulation factors. The interpolation function p_x varies each parameter linearly between its calibrated values $x = 0$ and $x = 1$. All parameters are effective fitting parameters rather than uniquely extracted microscopic material constants. The global numerical parameters are summarized in Table S2, while the fitted transport parameters and their bounds used for fitting are provided in Table S3.

The low-field current is described by a phenomenological trap-assisted-tunnelling-like contribution [29, 35–38], while the high-field current is represented by a Fowler–Nordheim-like term [43]. The fitted parameters are consistent with a nearly symmetric low-field trap-mediated contribution and a stronger polarity dependence in the high-field branch.

For the state-evolution equation, we assume the Mott-Gurney law with a field-dependent barrier [67]. The state-evolution equation $\frac{dx}{dt} = f(V,x)$ is defined:

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$$\frac{dx}{dt} = \begin{cases} e^{-\alpha_s(1-x)^{\beta_s}} e^{(|V|-p_x(x,v_s^{min},v_s^{max}))\delta_s x} \sinh\left[\theta_s \left|\gamma_{0s} - \gamma_{1s} x^{\gamma_{2s}}\right| |V|\right] \sigma_n(1-x) & \text{for } V \geq 0 \\ -e^{-\alpha_r x^{\beta_r}} e^{(|V|-p_x(x,v_r^{min},v_r^{max}))\delta_r} \sinh\left[\theta_r \left(\gamma_{0r} - \gamma_{1r}(1-x)^{\gamma_{2r}}\right) |V|\right] \sigma_n(x) & \text{for } V < 0 \end{cases}.$$

Here, α_l and β_l control the state-dependent suppression of the evolution rate near the corresponding resistance-state boundary. The parameters v_l^{min} and v_l^{max} define the state-dependent effective programming voltage through $p_x(x, v_l^{min}, v_l^{max})$, while δ_l controls the sensitivity of the exponential activation term to the voltage overdrive. For the set branch, this activation term is additionally weighted by x. The parameter θ_l scales the voltage dependence of the sinh term, whereas γ_{0l}, γ_{1l}, and γ_{2l} define the state-dependent local field enhancement factor accounting for the polarizability of the material [68]. The second exponential term describes a state-dependent effective activation barrier: as $|V|$ approaches and exceeds $p_x(x, v_l^{min}, v_l^{max})$, the voltage-overdrive term increases and accelerates the state evolution, possibly due to trap filling or emptying. The scaled sigmoid window functions $\sigma_n(1-x)$ and $\sigma_n(x)$ suppress the state evolution near $x = 1$ and $x = 0$, respectively, thereby constraining x to the interval [0,1]. Here, n controls the steepness of the sigmoid window near the state boundaries. The sigmoid window function is defined as:

$$\sigma_n(x) = \frac{1}{1 + ne^{-nx}}$$

The fitted state-evolution parameter values are provided in Table S4. The full model, including the current and state change equation, was fitted jointly to the quasi-static I-V characteristic results shown in Figure 5 and dynamic pulse measurements shown in Figure 6a. The I–V dataset includes the forward and backward sweeps measured under progressively varied set and reset voltage limits and therefore samples a continuum of stabilized resistance states.

The compact model results are visualized in Figure 10. The model parameters were extracted exclusively from the quasi-static I-V sweeps and pulse-width-dependent programming measurements. Fixed-width pulse-train measurements, which were excluded from parameter extraction, were subsequently used to evaluate whether the fitted state-evolution law could describe these independent datasets without parameter readjustment. Figure S8 shows close agreement with the 6, 10, and 40 µs pulse-train data in Figure 6b–d, supporting the state-evolution equation under independent programming conditions.

Figure 10a illustrates the state-dependent phenomenological TAT-like and FNT-like transport contributions and the corresponding equivalent-circuit representation. Figure 10b compares the modeled and measured quasi-static I-V characteristics using the dataset from Figure 5. The grey curves show the experimental data, while the colored curves show the compact-model results. Solid and dashed lines denote the forward and backward voltage sweeps, respectively. The inset shows the logarithmic current residual, defined as

$$\Delta log_{10} |I| = log_{10} |I_{model}| - log_{10} |I_{measured}|$$

Figure 10d shows the corresponding internal state trajectory $x(t)$, calculated numerically under the experimentally applied voltage sequence $V(t)$. Figure 10c shows the pulse-width-dependent resistance evolution obtained from the fitted state equation using the data in Figure 6a. The model captures the delayed onset and subsequent rapid evolution of potentiation, together with the smoother depression branch. The compact model consequently captures the static and dynamic behavior linking the identified physical transport mechanisms with the observed programming kinetics. To establish circuit-simulator compatibility, the same model was implemented in Verilog-A, compiled into the OSDI format using OpenVAF, and executed in NgSPICE. The Verilog-A/OSDI implementation produced the expected quasi-static hysteresis, bidirectional conductance modulation, and bounded state dynamics (Figure S9). The Verilog-A source code is provided as Code S1, enabling direct reuse of the experimentally calibrated device representation in circuit-level simulations.

3 | Conclusion

This work addresses a persistent limitation of area-type memristors: parasitic charge storage can induce readout drift and compromise practical operation, particularly under high-frequency and low-latency conditions. We systematically investigate TiN/Ta_2O_5/Pt devices across a wide thickness regime and identify a narrow thickness window in which stable area-type switching can emerge. Two gradual-switching regimes with distinctly different readout stability are resolved within this transition. Most notably, the 5 nm devices exhibit operationally near-ideal area-type characteristics within the defined operating range, including pinched hysteresis, nearly symmetric low-bias readout, continuous conductance tuning, and area-proportional conductance scaling.

Our results support a hierarchical picture in which stabilized-state switching is governed primarily by electronically controlled trap occupancy, whereas ionic and defect redistribution become important mainly during initial-state reconstruction and at the boundaries of the operating regime. In this framework, low-bias readout is consistent with a dominant trap-mediated tunneling contribution, while an additional FNT-like high-field contribution becomes increasingly important during programming. Ionic redistribution therefore defines the accessible regime and its stability limits, while electronic trap modulation controls the reproducible conductance evolution within that regime.

Finally, a physics-based compact memristor model describes accurately the quasi-static I–V behavior as well as the dynamic pulse-width-dependent resistance evolution of the 5 nm device in its stabilized operating regime. The model was implemented in Verilog-A, which paves the way for an integration of the device in

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circuit simulators. In this way, the thickness study, mechanism analysis, and compact model together provide a continuous description from regime selection to near-ideal multi-state area-type memristive device behavior.

4 | Experimental Section

$TiN/Ta_2O_5/Pt$ memristors were fabricated by ALD at 250°C with Ta_2O_5 thicknesses of 3.04 nm (3 nm device), 4.11 nm (4 nm device), 5.24 nm (5 nm device), 6.36 nm (6 nm device), 7.38 nm (7 nm device), 8.41 nm (8 nm device), 9.46 nm (9 nm device), and 10.43 nm (10 nm device) measured by spectroscopic ellipsometry. For simplicity, the measured thicknesses are referred to by their rounded values of 3–10 nm hereafter. The devices employed a 20 nm TiN bottom electrode on Si, and a 50 nm Pt top electrode defined by a shadow mask. Square devices with edge lengths of 300, 400, and 500 μm were measured, with the device area defined by the top electrode. No post-deposition annealing was applied. Quasistatic I–V measurements were performed using a Keysight B1500A analyzer. The bias was applied to the Pt electrode while the TiN electrode was grounded. Resistance values were obtained from sequential reads +0.1 V and -0.1 V and averaged. For pulse programming, voltage waveforms were generated and acquired using ADP3450 (Digilent), with details of the pulse-generation and current-readout circuitry provided in the SI. The as-deposited TiN/Ta_2O_5 film was also characterized by x-ray photoelectron spectroscopy (XPS) using different incidence angles. Detailed fabrication, XPS fitting constraints, and measurement protocols are provided in the Supporting Information. For plotting/analysis, only isolated points showing a deviation of more than 50% from the local trend defined by the two adjacent data points as noise outliers, were automatically excluded using the same criterion across all datasets.

Author Contributions

Cuo Wu: writing – review and editing, writing – original draft, conceptualization, methodology, software, data curation, investigation, validation, formal analysis, visualization, supervision, project administration. **Junjie Zhao**: investigation. **Richard Schroedter**: writing – review and editing, project administration, validation, visualization, software, funding acquisition. **Jason Vincent**: validation. **Hampus Hoffman**: writing – review and editing. **Leif Riemenschneider**: methodology. **Abdallh Herbawe**: methodology. **Hao Shen**: investigation. **Ronald Tetzlaff**: supervision, writing – review and editing, resources, project administration, funding acquisition. **Stefan Slesazeck**: supervision, project administration. **Gianaurelio Cuniberti**: resources, supervision. **Thomas Mikolajick**: funding acquisition, resources, project administration, supervision, writing – review and editing. **Benjamin Max**: writing – review and editing, supervision, project administration, funding acquisition, resources.

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Use of Generative AI and AI-Assisted Technologies in the Writing Process

During the preparation of this manuscript, the authors used ChatGPT (OpenAI) to assist with language polishing, including grammar, sentence structure, and logical flow. Generative AI was not used to generate or modify experimental data, perform data analysis, or produce scientific results. Generative AI was also used for the schematic illustration in Figure S6a, as disclosed in the corresponding figure caption, and for part of the ToC image. All AI-assisted content was reviewed and revised by the authors. The authors have reviewed the entire manuscript and take full responsibility for all of its content.

Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section.

Supporting File 1: adma75393-sup-0001-SuppMat.docx.

Supporting File 2: adma75393-sup-0002-MovieS1.mp4.

Supporting File 3: adma75393-sup-0003-S1_VerilogA.va.txt.

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