Untersuchung von "high-κ" Materialien als alternative Dielektrika für AlGaN/GaN-basierte Metall-Isolator-Halbleiter Heterostruktur-Feldeffekt-Transistoren (MISHFET)

Investigation of "high-κ" materials as alternative dielectrics for AlGaN/GaN-based metal-insulator-semiconductor heterostructure field effect transistors (MISHFET)

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Zusammenfassung

Gallium Nitrid (GaN) basierte Heterostruktur Feld-Effekt Transistoren (HFET) stellen vielversprechende Bauteile für Leistungsanwendungen bei hohen Frequenzen dar, die insbesondere von den Eigenschaften des GaN profitieren, das eine große Bandlücke aufweist und eine hohe Mobilität und Sättigungsgeschwindigkeit der Ladungsträger besitzt.

In den letzten Jahren wurden Leistungsverbesserungen der Bauteile durch eine Isolierung der Steuerelektrode erreicht (MISHFET). Die vorliegende Arbeit trägt zu einer weiteren Verbesserung von GaN basierten MISHFETs bei, indem die Steuerelektrode mittels Material mit hoher Dielektrizitätszahl ("high-κ") isoliert wird. Hierzu wird auf die neusten Fortschritte mit Gadolinium Scandat ($GdScO_3$) und Hafnium Dioxid (HfO_2) zurückgegriffen - Materialien, die in erster Linie auf ihre Tauglichkeit als SiO_2-Ersatz in der CMOS Technologie untersucht werden.

Um Experimente mit den anvisierten Bauteiltypen durchführen zu können, wurde die GaN Prozessierungstechnologie, die am IBN fest etabliert ist, modifiziert und erweitert. Im Besonderen wurden Techniken zur Deposition von high-κ Material - darunter die Pulsed-Lased Deposition (PLD) und die Electron-Beam Evaporation (EBE) - untersucht und teilweise modifiziert. Ebenfalls wurden Methoden zur elektrischen Charakterisierung der Bauteile optimiert oder neu eingerichtet, beispielsweise wurde die Möglichkeit zur Vermessung von Isolatorströmen neu geschaffen.

Die ersten Experimente zielten auf die Herstellung und Charakterisierung von SiO_2 Bauelementen, die im Verlauf der Arbeit als Referenz für high-κ MISHFETs dienten. Die SiO_2 Bauteile zeigten sich hinsichtlich eines niedrigen Leckstroms, eines hohen Ausgangsstroms und einer verbesserten RF Verstärkungsleistung als den konventionellen Bauteilen überlegen. Darüber hinaus wurden Einblicke in die Rolle von Passivierungseffekten und die Mechanismen des Strom-Transports bei MISHFETs gewonnen.

Parallel dazu wurden erste Versuche unternommen, Isolationsschichten aus $GdScO_3$ und HfO_2 in Transistoren und Dioden einzubringen. Insbesondere konnte die Nachbehandlung deponierter $GdScO_3$ Schichten in Sauerstoffatmosphäre als Schlüsselelement zur Herstellung von elektrisch-dichten $GdScO_3$ Material identifiziert werden. Andererseits ergaben die Untersuchungen, dass HfO_2 als Isolator für GaN basierte MISHFET nur bedingt geeignet ist. Dieses Ergebnis wurde auch durch theoretische Betrachtungen der relativen Lage der Energiebänder eines GaN/HfO_2 Überganges bestätigt.

Die sich anschließenden Experimente fokussierten auf die Verwendung von $GdScO_3$ als Isolator der Steuerelektrode von Transistoren. Erste MISHFETs und MIS Dioden wurden erfolgreich hergestellt. Die elektrische Charakterisierung ergab, dass das $GdScO_3$ Dielektrikum den Leckstrom um bis zu sieben Größenordnungen verringert. S-Parameter Messungen ergaben, dass $GdScO_3$ Bauteile potenziell bei Frequenzen bis 60 GHz betrieben werden können. Und "Load-Pull" Messungen zeigten, dass die Ausgangsleistung bei 7 GHz im Vergleich zu konventionellen Bauteilen mehr als verdoppelt werden kann.

Die demonstrierten Stärken des Gate-isolierenden $GdScO_3$ hinsichtlich der Verringerung des Leckstromes, der Erhöhung der Strom-Steuerwirkung und der Verdopplung der Ausgangsleistungs zeigen, dass der $GdScO_3$ MISHFET sowohl eine Verbesserung gegenüber konventionellen HFETs darstellt, als auch die SiO_2 MISHFET Variante übertrifft.

Summary

Gallium Nitride (GaN) based heterostructure field-effect transistors (HFET) are promising devices for high-power applications at high frequencies, as to be found in communication technology. The devices benefit from the properties GaN has to offer, namely a wide bandgap, a high carrier mobility and a high saturation velocity of carriers.

In recent years, improvements of the device performance were achieved by insulating the gate electrode by means of a dielectric layer (MISHFETs). This study contributes to the further improvement of GaN-based MISHFETs by insulating the gate with high-κ material, taking up latest advances with Gadolinium Scandate and Hafnium Dioxide - materials which are primarily intended to serve as a substitute for SiO_2 in CMOS technology.

To perform experiments with this novel kind of MISHFETs, the processing technology for the fabrication of HFETs, which has been well established at the IBN, was modified and extended. In particular, deposition techniques for the high-κ materials - e.g. pulsed-laser deposition (PLD) and electron-beam evaporation (EBE) - were investigated and partly modified. Also, methods for the electrical characterization of the processed devices were optimized or established, in particular means to investigate currents through insulators were established.

The first experiments conducted aimed at the fabrication and characterization of SiO_2 MISHFETs, which served as a reference for the subsequent studies with high-κ material. The SiO_2 devices proved to be superior to conventional HFETs in terms of a low gate leakage, a high drain current, and improved RF power performance. Furthermore, insights into the role of surface passivation in MISHFETs were gained and the gate current mechanisms were studied.

In parallel, first attempts to incorporate $GdScO_3$ and HfO_2 insulation layers into diodes and transistors were performed. In particular, annealing in O_2 atmosphere was identified to be a key element to gain electrically dense $GdScO_3$ material. One the other hand, HfO_2 was found to be an unsuitable material to serve in GaN-based MISHFETs, which was also confirmed by theoretical considerations regarding the GaN/HfO_2 energy band offsets.

The subsequent experiments focused on $GdScO_3$ to be used as gate insulation. First MISHFETs and MIS diodes were fabricated successfully. Electrical characterization revealed, that the $GdScO_3$ dielectric reduces the gate leakage currents by up to seven orders of magnitude. S-parameter measurements indicated the potential use of $GdScO_3$ devices up to 60 GHz, and Load-Pull measurements showed that the delivered output power at 7 GHz can be more than doubled compared to conventional devices.

In conclusion, $GdScO_3$ was demonstrated to be a promising candidate for MISHFETs for high-power applications at high frequencies. The strengths in terms of gate leakage reduction, channel control increase, and increase of RF power performance not only outperforms conventional HFETs but also SiO_2 MISHFETs. Besides the demonstration of the superior performance of $GdScO_3$ MISHFETs, this study also identifies aspects for further optimization, e.g. leaves the breakdown characteristic room for improvements.

Contents

Part I

Introduction

During the last three decades, researchers and developers have made tremendous progress in exploring Gallium Nitride (GaN) for a vast spectrum of applications. In particular, epitaxially grown heterostructures have been the basis for many devices with highly improved or novel properties, as illustrated in figure I. For instance, in the field of opto-electronics, utilizing GaN has lead to blue and ultra-violet light emitting diodes (LED), closing the gap in the optical spectrum covered so far by commercial LEDs.

Besides opto-electronics, GaN is the material of choice whenever its properties as wide bandgap, high electron mobility and high saturation velocity of carriers can be exploited. Considering heterostructures with an Aluminum Gallium Nitride (AlGaN) film on a GaN layer, many device types have yet been realized such as sensors, diodes and varactors. But certainly, the device that has received the most attention is the heterojunction transistor. Powerful and fast devices have been proven to withstand even harsh ambient conditions.

When talking of heterostructure transistors, the main focus is on the field-effect type (HFET), although bipolar devices were realized as well. Many authors were successful in utilizing HFETs for a broad range of applications, for instance as switch, attenuator, mixer or oscillator; even logic circuits have been realized by means of HFETs. But using the HFET in amplifiers is what attracts the most interest. Low noise and highly linear amplifiers have been fabricated yet. But clearly the most attention is drawn to high power amplifiers which were already realized for a wide range of frequencies and operation modes.

This work will contribute to the improvement of GaN/AlGaN HFETs for high power amplifiers by insulating the gate electrode from the semiconductor by means of a thin dielectric film, thus creating a metal-insulator-semiconductor heterojunction field-effect transistor (MISHFET). Several material options for the insulating layer will be discussed, namely SiO_2, HfO_2, and $GdScO_3$, whereas the latter two belong to the high-κ materials.

In the following, an insight into the status quo of research concerned with GaN/AlGaN HFETs and MISHFETs is given, i.e. motivation, objectives, challenges and approaches will be discussed. Then, the research done at the FZJ/IBN in the previous years will be summarized briefly, since it is the basis for the actual work. The current project will be presented afterwards, i.e. the specific approach of gate insulation will be sketched, its impact on the major difficulties of GaN-based transistors will be explained, and the objectives of this work will be defined. An outline of this work concludes the opening part.

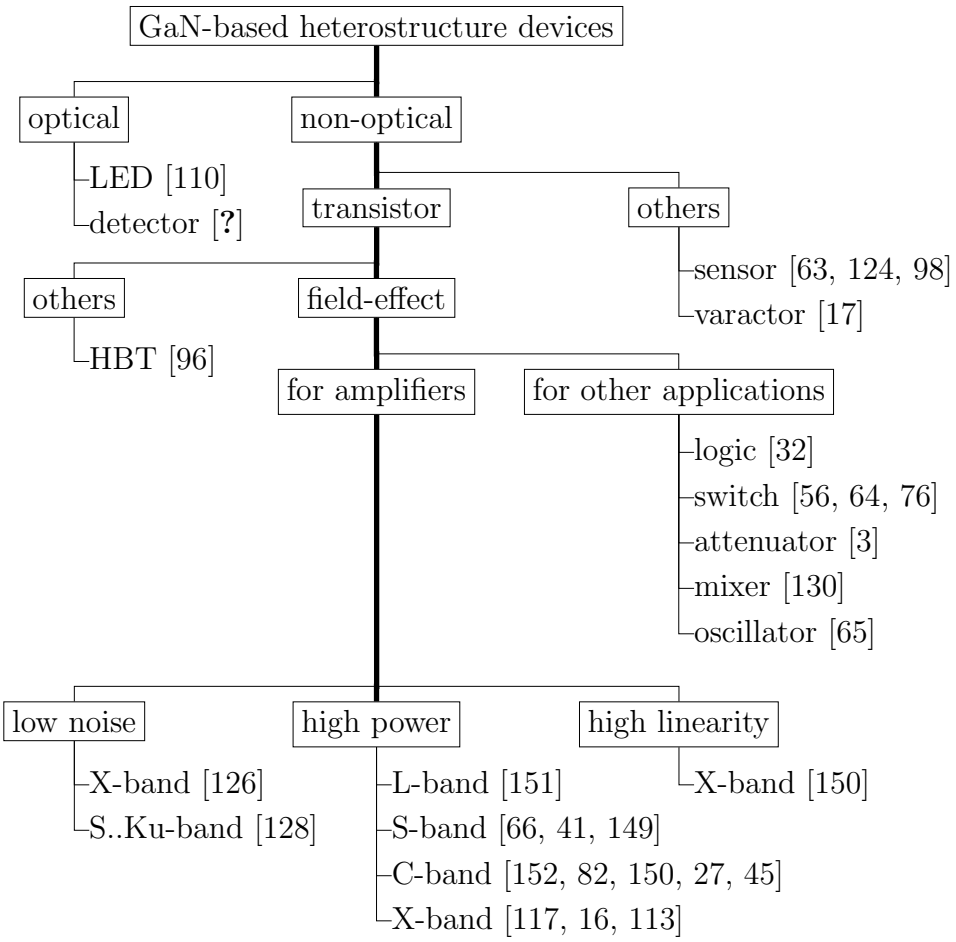


Figure 1: Taxonomy of GaN-based heterostructure devices.

Chapter 1

Research Status Quo

The high-power amplifier is certainly one of the major applications in which GaN-based HFETs can be utilized. The intent of this chapter is to give a status quo of the research related to GaN-based HFETs for high-power amplifiers working at RF frequencies. In a first step, the reasoning will be presented why GaN is considered a suitable material for high-power HFETs. Then, the research goals and requirements of industry and academic institutions will be sketched briefly. A survey of the difficulties that have to be solved to reach the goals and to fulfill the requirements will follow. And finally, approaches to solve the difficulties will be discussed. In other words, this chapter tries to give answers to the questions "why do researchers deal with GaN devices for high-power amplification?", "which goals do they have?", "which problems do they have to solve?", and "how do they solve the problems?".

1.1 Motivation

One way to illuminate the motivation for research on GaN-based transistors is to find answers to the questions "what makes a good transistor for high power applications?" and "what is the enabling GaN property?". According to Mishra [103], these questions can be answered as follows.

An essential need for the desired transistors is a high output power density. Due to the wide bandgap of GaN and the high fields it can withstand, devices of this material can outperform competing technologies by a factor of ten. As a consequence, devices can be designed more compact in size. And the reduction in size not only translates in less production costs, it also increases the impedance which results in less matching effort.

Secondly, high voltage operation is favorable for a good transistor. Again, it is the wide bandgap of GaN which results in high breakdown fields and devices which can withstand several hundred volts. A practical aspect lies in the fact that commercial systems operate at 28 V. Since GaN can be operated at this voltage with ease, the need for voltage conversion can be reduced or even eliminated.

A further need is a high efficiency. Here, the key feature of GaN is again the wide

bandgap which results in a high operating voltage. Thus, power can be saved and less effort is necessary for cooling the device. The latter aspect is of great importance, since cost and weight of the cooling means make up a great fraction of the overall costs and weights.

The ease of thermal management is a further criterion for a good transistors. Although native substrates are not yet available in sufficient quantities, the commonly used SiC substrate offers a fairly good heat conductance. As a consequence, high power devices with reduced cooling needs can be realized in GaN technology.

Mishra points at a further important aspect: the need for some technology leverage. Since GaN is a direct bandgap semiconductor, it is frequently used in opto-electronics. The research activities in this particular field serves as a driving force for the HFET technology and provides knowledge at low cost.

Furthermore, a good transistor operates at high frequencies and with high linearity. The GaN inherent high carrier velocity together with the specific topology of the heterostructure results in devices operating at high frequencies and with a broad bandwidth. This allows an optimum frequency band allocation for fast future applications in telecommunications.

Also, a transistor should be capable of being operated at elevated temperatures. In this context it is again the wide GaN bandgap that enables rugged, reliable, and reduced cooling. Good transistors should have a low noise figure. The high gain and the high velocity that can be realized with GaN enable low noise operation and thus makes high dynamic range receivers feasible.

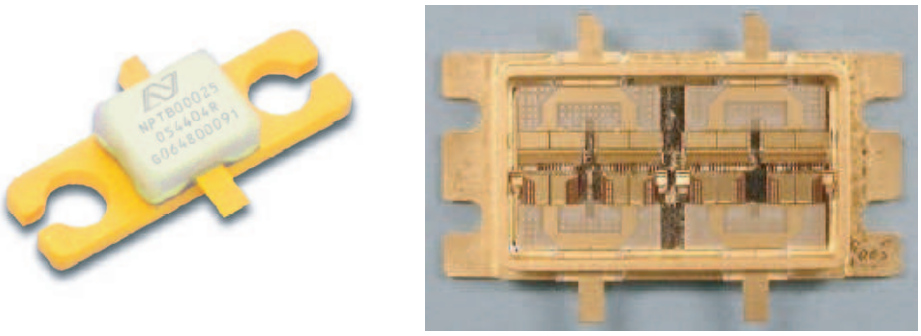
1.2 Objectives, Challenges, and Approaches

Objectives

Some companies already sell GaN-based HFETs. For instance, Nitronex Corporation offers a device delivering an output power of 25 W at an operating voltage of 28 V for a frequency range between 400 MHz and 3 GHz [28] (see figure 1.1(a)). Other companies have started ambitious development projects to deploy products soon. For instance, BAE systems was assigned the development of a 160 W GaN amplifier for military applications by the Defense Advanced Research Projects Agency (DARPA), the project aims at product deployment in 2010 [6].

But although commercialization of GaN-based transistors is gaining momentum, the GaN technology will not be a self-selling item. A look at the rivals in business reveals: Currently, Si laterally diffused MOSFETs are utilized in base stations of mobile communication networks, where frequencies of up to 2.5 GHz are needed. For higher frequencies between 3 GHz and 10 GHz, GaAs HFETs are well established and InP devices are a further option. In addition, SiC-based MESFETs have become competitive for application frequencies up to 10 GHz [125].

Thus, at this stage of development, business companies aim at optimizing GaN-based



(a) (b)

Figure 1.1: GaN-based HFET today. Commercially available Nitronex device delivering 25 W [28] a) and a device study of Eudyna Devices with 800 W [104] b).

devices to meet performance, reliability, production, and cost requirements to compete against the well established and emerging technologies.

Academic Institutions, in contrast to business companies, are not as much concerned with optimization of the devices. To a certain extent, these devices have to meet the same requirements as the devices to be commercialized. Nevertheless, the device itself serves as a facility to test hypotheses from the fields of solid-state physics, material science, etc.

Challenges

The difficulties researchers have to solve are similar for business companies as for academic institutions. But due to the different objectives, the relevance of a problem can be considered differently: A company as Fujitsu currently focuses at the investigation of mass production techniques and reliability issues [9], whereas at the IBN a technology to fabricate some dozens of transistors is fully sufficient. Nevertheless, the major challenges are listed in the following to give an answer to the question "which problems do researchers have to solve?".

The ultimate challenge is to drive the RF power *performance* of a device as high as possible. Of course, the optimization of performance can not be considered without taking into account reliability, cost and other issues. But judging from the numerous publications, the run for highest output power densities and related figures of merit seems to be a major concern. To illustrate this trend, consider the following figures: In 2004, Kikkawa et al. [72] reported an output power of 150 W. Three years later, a 800 W device was presented by researchers of Eudyna Devices [104] (figure 1.1(b)).

Until recently, reliability issues were not as much focused by research as the challenge to increase performance [123]. But now, since commercialization of GaN transistors has begun, business companies are increasingly concerned with the *reliability* of devices [9]. Reliability can be translated with stability of device performance over time and under

application specific conditions. For satellite applications for instance, the device must withstand radiation to be reliable [87]. For other applications, performance must not degrade under bias stress [79] or elevated temperatures.

Closely related to reliability is the topic of *trap-related effects*. Electrons can become trapped in electronic states located within the band gap and can cause corruptive effects. For instance, Khan et al. [70] observed a significant decrease of drain current after a high drain source voltage ($> 20\,\mathrm{V}$) was applied and attributed this effect - also known as current collapse - to the trapping of electrons in the AlGaN layer of the device. Another effect attributed to trapping is the knee voltage walkout [123]. The mitigation of trap-related effects is still a vital issue [105, 100, 118, 125], since they can have severe impact on device performance and reliability.

The high *gate leakage current* can still be considered one of the big challenges. Although many groups have invested much research effort [47, 74, 101] there is still considerable interest in reducing the leakage currents. The reason is that the gate current not only degrades the power performance of a device. It is also related to other major problems. Saito et al.[121] presented results illustrating the dependencies of gate current, breakdown voltage, and surface state density. And Tan et al. [138] proposed that electrons leaking from the gate can propagate along surface states towards the drain. This current mechanism degrades the breakdown characteristics of the device. Thus, the reduction of the gate leakage is still one of the key challenges.

The optimization of the *heat dissipation* is a further challenge in research related to GaN-based HFETs. Although many publications claim high power densities of their GaN/AlGaN devices, these results are usually calculated from measurements of devices with small gate widths. For instance, Chu et al.[26] achieved a $9.1\,\mathrm{W/mm}$ power density for a device with $2 \times 75\,\mu\mathrm{m}$ gate width. But these high power densities can not be attained by large gate width transistors due to the insufficient heat dissipation [31]. As an example, consider a device delivering $150\,\mathrm{W}$ with a $36\,\mathrm{mm}$ gate width device [72], resulting in a power density of only $4.2\,\mathrm{W/mm}$.

Approaches

To encounter the challenges described above, various approaches are pursued. The most important of these approaches are briefly sketched in the following and thus an answer will be given to the question: "how do researchers solve the problems?"

Although GaN-based heterostructures have been grown for quite some time, there is still room for the *improvement of the material* [115], in particular the reduction of dislocation densities. According to Fujitsu, problems such as device failure and unstable output at high drive voltages are caused by non-uniformity and defects in the GaN epitaxial layer [9].

In the field of *optimization of the layer structure* [92, 20, 21] still considerable research effort is invested. For instance, experiments with an AlN interlayer and with varying doping levels [93, 95, 94] aim at improving the 2DEG properties. The use of an additional GaN cap layer is proposed to reduce the gate leakage and all the related difficulties with

electron trapping [70].

In a wider sense, the following approaches can also be interpreted as approaches to optimize the layer structure. Heat-spreading diamond films were deposited to mitigate the problem of insufficient heat dissipation [127], the same problem is tackled by Dietrich et al. [31] by thinning down the substrate layer and by thickening the Au metallization. In depth analysis of particular aspects, as the dependence of barrier height on Al concentration [116, 68], help to further optimize the devices.

Although much effort has been invested to GaN/AlGaN HFET research, there is still room for *improving the processing technology*. For instance, cleaning of the material surfaces [92, 36] to reduce gate leakage and density of traps is an issue, or the modification of gate contacts [80, 106, 107, 111, 153, 36].

Some authors *optimize the device geometry*. The use of T-shaped gates is a means to increase the RF performance by minimizing the effective gate length and by providing a low gate resistance. This approach also impacts the RF power performance as shown by Thompson et al. [141] reaching an output power density of 16 W/mm at $V_{\mathrm{ds}} = 60\,\mathrm{V}$ and $f = 10\,\mathrm{GHz}$. Also, the optimization of the device geometry (e.g. increase of gate pitch and mesa width) is an appropriate means to decrease the thermal impedance of the device [31] and thus serves to improve the insufficient heat dissipation for large gate width devices.

The layout of multi-fingered devices is also a powerful means to increase power performance [76]. The field-plate approach modifies the distribution of the electric field in the device such that higher drain source voltages can be applied without device breakdown. Saito et al. reached a six times higher breakdown voltage of remarkable 600 V [122]. The output power density can be increased as well as shown by Koudymov et al. [75] for lower frequencies (2 GHz) reaching 20 W/mm at a drain source voltage of 55 V, and for higher frequencies (18 GHz) by Kumar et al. [78] who reached 9.1 W/mm at 55 V.

Much effort is spent on the *development of substrates*. The state-of-the-art substrate materials currently used are Silicon Carbide (SiC) and Sapphire (Al_2O_3). Silicon (Si) has proven to be a good candidate for fast transistors [35]. Although Si is not as effective in removing heat as SiC, it has the advantage of being a thoroughly known material. GaN/AlGaN transistors were fabricated by Javorka et al. [60] reaching cutoff frequency of 32 GHz and a maximum frequency of oscillation of 27 GHz for a gate length of 500 nm. Also, good power results could be obtained, Dumar et al. [33] demonstrated a device with an output power density of 7 W/mm at 10 GHz and $V_{\mathrm{ds}} = 40\,\mathrm{V}$.

The use of native substrates as GaN or AlN rather than substrates like SiC, Al_2O_3, and Si is commonly viewed at as a promising approach to increase the material quality and to improve heat dissipation [102]. Despite the fact that native substrates are still available only at high prices, some authors have conducted research with GaN substrates [38, 71, 55, 26], AlN substrates [52], and AlN/SiC templates [62, 129, 81, 108].

Numerous articles in literature contribute to the *passivation* of the semiconductor surface of a device. This approach aims at reducing surface trap related effects and has been performed with various materials, e.g. Si_3N_4 [44, 90, 91, 137], ScO_3 [43, 92, 90, 91, 86, 88, 87], Al_3O_4 [49], and MgO [43, 92, 90, 91, 86, 87].

Last but not least, the approach to *insulate the gate electrode* aims at reducing the gate leakage current. Many different materials were used to fabricate MISHFETs, e.g. SiO_2 [69, 25], Si_3N_4 [1, 112], and multi-layer stacks as $SiO_2/Si_3N_4/SiO_2$ [40] or Si-oxynitrides [13]. Other authors used ScO_3 [97, 99, 89, 42], Al_3O_4 [48, 49, 114, 6], and MgO [73] for MISHFETs and HDiodes. The feasibility to incorporate MISHFETs into integrated circuits was demonstrated by Simin et al. realizing a RF switch based on a MISHFET. [131].

1.3 Research at the IBN

In the previous sections, the status quo of research concerned with GaN-based HFETs was sketched. Research done at the Institute of Bio- and Nanosystems (IBN) is listed explicitly in the following, although part of the work was already cited in the above review. This is due to the fact that this work benefits to a great extent from the experience gathered at the IBN over the last years. It is founded on the processing technology and characterization methods developed and established by my former colleagues.

P. Javorka [59] contributed a technology to fabricate GaN/AlGaN HFETs on Si and Al_2O_3 substrates. The standard technology was expanded by issues as air-bridging and passivation. Also, the concept of Round-HFET for fast and cheap fabrication of HFET prototypes was implemented. The impact of layer structure and device geometry on the behavior of HFETs on Al_2O_3 substrates was investigated. Regarding devices on a Si substrate, the influence of intentional doping on device performance and the role of thermal effects were discussed. SiO_2 and Si_xN_y passivation experiments were performed with HFETs on either of the substrates. Inter alia, novel characterization methods as temperature-dependent DC measurements, pulsed IV characterization and Load-Pull RF power measurements were implemented.

M. Wolter [147] investigated trapping states and related effects, as current collapse and DC/RF dispersion by means of Photo-Ionization Spectroscopy, Backgating Current Deep Level Transient Spectroscopy ($BC-DLTS$), and Pulsed Measurements. Furthermore, traps in the GaN buffer on SiC and Si substrates were examined by means of Admittance-Spectroscopy. Studies were performed with GaN/AlGaN HFETs on sapphire substrates. In particular, SiO_2 and Si_3N_4 passivation to mitigate the trap-related effects was examined.

The studies on GaN/AlGaN HFETs were continued by J. Bernát [17], who focused on optimization of processing technology of HFETs on SiC substrates. In particular, field plate and air bridging technology were successfully applied, and first approaches to realize SiO_2 MISHFET devices were accomplished. With the fabricated devices, experiments concerning the influence of passivation and intentional doping on device performance were performed.

Chapter 2

Research of this Work

2.1 Approach, Challenges, and Objectives

In the previous chapter, the current status of GaN HFET related research in industry and academic institutions was presented, starting with the specific objectives, describing the challenges, and giving an overview of the various approaches to tackle the challenges. In the following, the current work will be sketched. This time starting with the approach chosen - namely the insulation of the gate - then listing the common challenges that can be tackled by means of gate insulation, and finally outlining the objectives of this work.

Approach

The approach followed in this theses is to insulate the gate of a HFET from the semiconductor stack either by oxides as SiO_2 or high-κ material as $GdScO_3$ and HfO_2. This Metal-Insulator-Semiconductor (MIS) approach was chosen mainly because of three reasons: First of all, insulation of the gate seems to be a very *effective* approach. Numerous authors have successfully demonstrated the principal strength of the MIS approach. But on the other hand, the current achievements leave plenty of room for improvements, as will become clear from the discussion to follow.

Secondly, the MIS approach is an *efficient* approach. It aims primarily at the reduction of the gate leakage. Therefore, it tackles one of the key challenges of current research: A reduction of leakage currents helps to meet other challenges. For instance, a lowering of leakage current can mitigate trapping effects, it can increase the device reliability, and it can improve the RF power performance. In addition, due to the technological similarities with surface passivation, the MIS concept also offers the chance to exploit the advantages of coating the semiconductor surface with passivating materials. Thus, the MIS approach possibly integrates the advantages of the passivation approach.

And last but not least, the MIS approach offers an interesting opportunity to merge latest advances in the field of high-κ research at the IBN with the GaN device related knowledge available: The group of J. Schubert at the IBN developed a technology to

deposit high-κ material with excellent insulating and dielectric properties [50, 143]. And although the materials were primarily developed to serve as a gate dielectric in Si-based devices, it appears worthwhile to combine the novel achievements also with GaN devices.

Challenges

As already mentioned, the MIS approach is not only an interesting and effective means, moreover it is very efficient. The manyfold contributions to tackle the major challenges in GaN/AlGaN HFET research can be well explained by looking at an article of Khan et al. [69] which reports on the first SiO_2 MISHFET successfully fabricated in 2000.

The major challenge tackled by the MIS approach is the reduction of the gate leakage current. Khan et al. demonstrate a decrease of the reverse current of six orders of magnitude due to a SiO_2 insulation (although it has to be noted that the reference device showed an unusually high gate current of around 0.1 mA at $V = -10\,\mathrm{V}$).

With respect to the forward gate current, the difference between conventional HFET and MISHFET is even more drastic because in Schottky-contact devices the forward current increases exponentially. What is particularly important about the forward current reduction is the fact, that it provides the possibility to operate the transistor up to $V_{\mathrm{gs}} = 10\,\mathrm{V}$, an operation mode where twofold drain currents can be reached.

But the work of Khan et al. also reveals the difficulties with MISHFETs in general and for an insulator like SiO_2 in particular: The additional insulation layer decreases the channel control capability, because part of the applied voltage that is applied to control the channel properties of the 2DEG drops across the dielectric. Thus, the transconductance reduces and a higher voltage is to be applied to pinch off the device.

For the SiO_2 device of Khan this fact can be expressed by concrete figures: The threshold voltage drops from $-5\,\mathrm{V}$ for the HFET down to $-9\,\mathrm{V}$ for the MISHFET with a 7 nm thick SiO_2 layer. The authors argue that this threshold increase in combination with a improved linearity "should, in principle, lead to a smaller intermodulation distortion, a smaller phase noise, and a larger dynamic range." [69]

This might be the case for specific applications. But in general we assume, that a transistor with a sharp on- to off-state transition and low absolute threshold voltages offers the better channel control. Thus, the increase of threshold voltage is a major concern for MISHFETs and can be accomplished by an increase of the input capacitance. And in this context it is worthwhile to note, that an increase of capacitance per se does not slow down the device. As long as the ratio of input capacitance and parasitic capacitances remains high, the device will remain functional even for high frequencies.

Yet another drawback of MISHFETs is revealed by Khan et al.: The CV characteristic shows a threshold shift of 1 V, depending on the illumination conditions. This indicates difficulties with trapping states, most likely introduced by imperfections of the insulating SiO_2 layer. Also worth noting is an aspect concerning technology: Khan et al. intended to deposit 10 nm SiO_2, but from CV measurements they extract an effective thickness of 7 nm. The authors claim this to be a reasonable agreement, but one could also say that

there is still room for technology optimization.

Apart from the contributions of Khan, two more aspects need to be mentioned. The reduction of gate leakage also impacts other general difficulties in GaN HFET research, for instance the reliability issue. To illustrate this aspect consider a contribution of Fujitsu, the company claims to have realized a GaN-based Si_3N_4 MISHFET operating for 100 years at 200 °C [7]: Besides the use of higher-quality materials, the key factor to realize the long lasting device is the incorporation of a n-type GaN cap layer with an gate-insulating Si_3N_4 layer on top, stating the basic link between gate leakage current and device reliability:

The MIS approach is also efficient in another sense: The insulation of the gate possibly comes along with a passivation of the semiconducting surface. From literature concerning passivation it is known, that passivation can yield higher drain currents and mitigate gate lag or current collapse effects. Thus, by insulating the gate the challenges of performance increase and mitigation of trapping-effects can be met at once due to the passivation property of the dielectric material.

Objective

The main objective of this work is to show, that the MIS approach can be even more effective and efficient if high-κ material is used instead of SiO_2. In particular, a technology to fabricate MISHFETs using $GdScO_3$ and other promising materials is to be developed and the appropriate characterization means need to be provided. To provide a reliable reference for comparison, conventional HFETs and SiO_2 MISHFETs will be fabricated and characterized in parallel.

2.2 Outline

Besides the actual introductory part I, this theses comprises two parts: Part II provides the theoretical basis concerning the heterostructure field-effect transistor (HFET), the gate dielectrics, and the metal-insulator-semiconductor HFET (MISHFET), Part III presents the essential experiments conducted within this work and provides the discussion of the results.

Within the first chapter of part II, namely chapter 3, the formation of a two-dimensional electron gas (2DEG) at the interface of a GaN and a AlGaN layer is sketched, and the use of the 2DEG in the context of a HFET is explained. Then in chapter 4, gate dielectrics are treated in general, covering important properties as resistivity, permittivity, and stability. Chapter 5 provides models to explain and predict the electrical behavior of the HFET and the MISHFET.

The experimental part III starts with chapter 6, which covers two experiments. The first experiment aims at the investigation of the passivation effect of SiO_2 on the performance of SiO_2 MISHFETs. The second experiment examines the scalability of the SiO_2 thickness for MISHFETs and reveals insight into the relationship of passivation effect and

insulator thickness.

Then, attempts to achieve electrically dense $GdScO_3$ material to insulate the gate electrode are presented in chapter 7. The chapter comprises two experiments: An exemplary experiment, which stands for the approach to vary the annealing temperature, and one of the key experiment of this work, dealing with post-deposition annealing in oxygen atmosphere.

Chapter 8 covers experiments performed with $GdScO_3$ heterostructure diodes, based on the results gathered from the experiments in chapter 7. Here, permittivity and insulation properties of $GdScO_3$ are investigated, electronic states are studied using CV measurements, and by means of Impedance Spectroscopy the sheet carrier concentration and mobility within the 2DEG channel of the $GdScO_3$ device are investigated.

After having gained first knowledge concerning the integration of $GdScO_3$ into GaN-based devices, the promising attempt to fabricate and characterize $GdScO_3$ MISHFETs on SiC substrates is described in chapter 9. The following chapter 10 treats an experiment to investigate the possibility to use HfO_2 as a gate dielectric in MISHFETs.

Chapter 11 compares SiO_2 and $GdScO_3$ MISHFETs, and the final chapter of the experimental part summarizes the major conclusions drawn from the experiments and gives an outlook to further work to be done.

To provide an insight into the processing technology developed within this work, chapter A of the appendix presents details concerning important process steps specific to the fabrication of MISHFETs, including the deposition and etching of the gate dielectrics and the modification of the electron-beam lithography process. It also documents the complete process to fabricate MISHFETs, where the MISHFET specific elements are brought together with the standard HFET process established at the IBN.

The documentation of the methods and means to characterize electrically the fabricated devices can be found in chapter B of the appendix. The chapter comprises methods that have already been established for a long time at the IBN, other methods as the measurement of very low insulator currents and the Impedance Spectroscopy have been implemented within the scope of this work. The methods are subdivided into four groups, namely current-voltage, impedance, S-parameter, and Load-Pull measurements.

Part II

Fundamentals

Chapter 3

Heterojunction Field Effect Transistor (HFET)

This chapter gives a brief introduction into transistors made of heterostructure material: At first, the fundamental physics of GaN/AlGaN-based heterojunctions and the formation of the two-dimensional electron gas will be explained. Thereafter, the transformation of the heterojunction material into a heterostructure field-effect transistor will be treated.

3.1 Gallium Nitride based Heterojunction

If a GaN- and an AlGaN layer are brought into intimate contact, a two-dimensional electron gas (2DEG) can form slightly underneath the interface. In the following, the formation process will be explained and the necessary conditions will be listed that need to be fulfilled for a 2DEG to form. Then, the 2DEG will be characterized by means of charge carrier concentration, mobility, and velocity.

Formation Each of the two semiconductors have a bandgap (E_g) of different widths. In general, the energies of the lower conduction band edge of the two materials are not at the same level, neither are the energies of the upper valence band edges. The energy difference is denoted conduction band (ΔE_CBO) and valence band offset (ΔE_VBO). The relative alignment of the energy bands can be calculated in a rough first-order approximation according to Anderson's electron affinity rule [5], being the difference of the electron affinities (χ) of the two semiconductors (for a more detailed discussion on the formation of a band offset see section 4.2):

$$\Delta E_\mathrm{CBO} = \chi^\mathrm{AlGaN} - \chi^\mathrm{GaN} \tag{3.1}$$

$$\Delta E_\mathrm{VBO} = E_\mathrm{g}^\mathrm{AlGaN} - E_\mathrm{g}^\mathrm{GaN} - \Delta E_\mathrm{CBO}. \tag{3.2}$$

According to Freeman, ΔE_CBO between GaN and AlGaN layers can only be determined with great uncertainty, i.e. $0.15\,\mathrm{eV} < \Delta E_\mathrm{CBO} < 0.56\,\mathrm{eV}$ [39]. Nevertheless, Schwierz

et al. report the ΔE_{CBO} for a $GaN/Al_{0.3}Ga_{0.7}N$ heterojunction to be 0.42 eV [125]. Figure 3.1(a) represents the situation of the two semiconductors not being in contact by means of an energy band diagram.

In both semiconductors, electric fields due to spontaneous polarization exist, whereas spontaneous polarization in AlGaN is stronger than in GaN. Due to the smaller lattice constant of AlGaN compared to GaN, the AlGaN layer is under tensile strain. As a consequence, a piezoelectric polarization field in the AlGaN layer needs to be taken into account in addition.

Since a constant electric field is represented by a tilting of the energy bands, the sum of polarization fields on either side of the heterostructure causes the energy bands to tilt; the stronger the polarization effects the steeper the slope is. Assuming that the polarization fields of AlGaN and GaN point into the same direction (i.e. assuming Ga-faced growth), the slopes of the energy bands have the same sign, resulting in energy bands as illustrated in Figure 3.1(b). Note, that the semiconductors are still separated from each other at this point of discussion.

If the two semiconductors are brought into intimate contact, the Fermi energy levels (E_{F}) on either side need to even out to ensure thermodynamic equilibrium. Since E_{F} is pinned at the AlGaN surface on the left end (e.g. $E_{\mathrm{C}}^{\mathrm{AlGaN}} - E_{\mathrm{F}} = 1.6\,\mathrm{eV}$ in the case of $\mathrm{Al_{0.24}Ga_{0.76}N}$ [58]) and $E_{\mathrm{C}}^{\mathrm{GaN}} - E_{\mathrm{F}}$ is determined by the GaN bulk doping on the right end of the heterostructure, one has two boundary conditions that need to be satisfied. Thus, the energy bands bend correspondingly. The bending of the GaN portion of the energy bands is accompanied with the accumulation of free electrons forming the 2DEG. Figure 3.1(c) shows the characteristic energy band structure of an GaN/AlGaN heterostructure.

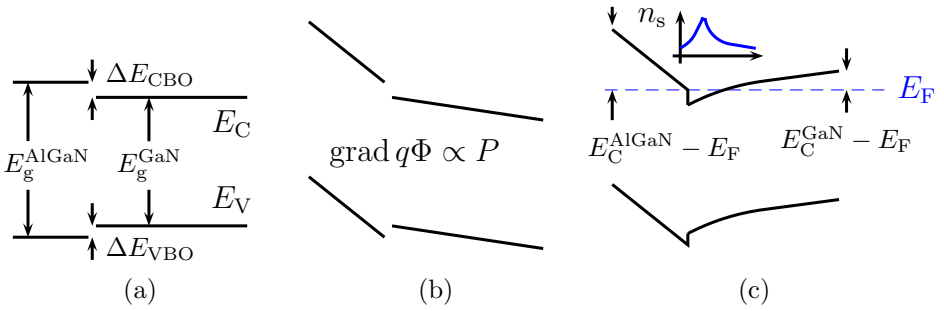


Figure 3.1: Necessary conditions for the formation of the 2DEG at a GaN/AlGaN heterojunction with n-doped GaN layer. Alignment of energy bands (a), spontaneous and piezoelectric polarization fields causing the energy bands to tilt (b), and boundary conditions at both ends of the heterostructure (Fermi level relative to conduction band at AlGaN surface and in GaN bulk) that are satisfied by appropriate band bending and corresponding accumulation of charge carriers, resulting in a certain sheet carrier concentration (n_{s}) (c).

Some authors explain the formation of the 2DEG with slightly different accentuation,

e.g. Freeman [39] and also Schwierz and Ambacher [125] explain the formation of the 2DEG as a process to compensate the resulting positive polarization sheet charge (due to $divP = \sigma_{pol}$) to ensure locale charge neutrality: "The 2DEG forms to screen the bound spontaneous and piezoelectric charge residing at the interface".

It is worthwhile to note, that in a GaN/AlGaN heterostructure the doping of the barrier layer, i.e. the AlGaN layer, is not a necessary condition for the 2DEG to form, other than e.g. in the $GaAs/AlGaAs$ material system. Also, some authors stress the question of where the electrons of the 2DEG "come from", proposing that the electronic states of the conduction band are filled by electrons "coming from" high free carrier concentration of GaN and AlGaN layers, or that they are injected from the metal contacts [4], which provide access to the 2DEG in electrical devices as will discussed in the following sections.

A common way to calculate the exact band bending and charge carrier distribution is to solve the Poisson-Schrödinger equations self-consistently by numeric simulation. Figure 3.2 shows the energy band configuration for different biasing conditions of a numerical simulation performed with WinGreen [54], a software based on realtime Green's functions and providing a quantum mechanical approach for the description of dynamic and kinetic properties of interacting many-particle systems in a thermodynamic non-equilibrium state. With the 2DEG potential becoming increasingly more negative relative to the surface potential, the conduction band well forming at the interface lifts above the Fermi energy level, meaning that fewer conduction band states are occupied, which corresponds with a weaker bending of the band. Further discussions concerning the numerical simulation of the 2DEG formation in GaN/AlGaN structures can be found in [51, 24].

Electrical Properties For the intended use of the 2DEG as conductive channel in diodes and transistors, it is mandatory to have means at hand to characterize the electronic transport. If an electric field (E) parallel to the 2DEG is applied, then the charge carriers of the 2DEG will be accelerated and will reach a certain steady-state velocity (ν) parallel to E, depending on the involved scattering processes. In general, the dependence of ν to E can be written as

$$\nu = \mu(E, n_{\mathrm{s}}, T)E, \tag{3.3}$$

where μ is the mobility of carriers, which itself is strongly dependent on E, the sheet carrier concentration (n_{s}), temperature (T), and scattering mechanisms.

The main scattering mechanisms of relevance at room temperature are summarized by Ambacher at al. [4]: "At room temperature, the maximum electron mobility is limited by polar optical phonon scattering. At low sheet carrier densities, impurity and piezoacoustic scattering diminish the mobility. For higher densities, these scattering processes are screened, which explains the increase in mobility. At very high sheet carrier densities, the average distance of the 2DEG to the AlGaN/ GaN interface becomes smaller. Depending on the interface quality, this can decrease the mobility significantly due to the increase in interface roughness scattering."

Farahmand et al. derived an expression for μ for bulk wurzite phase material [34]. By means of ensemble Monte Carlo simulation they calculated the steady-state electron drift

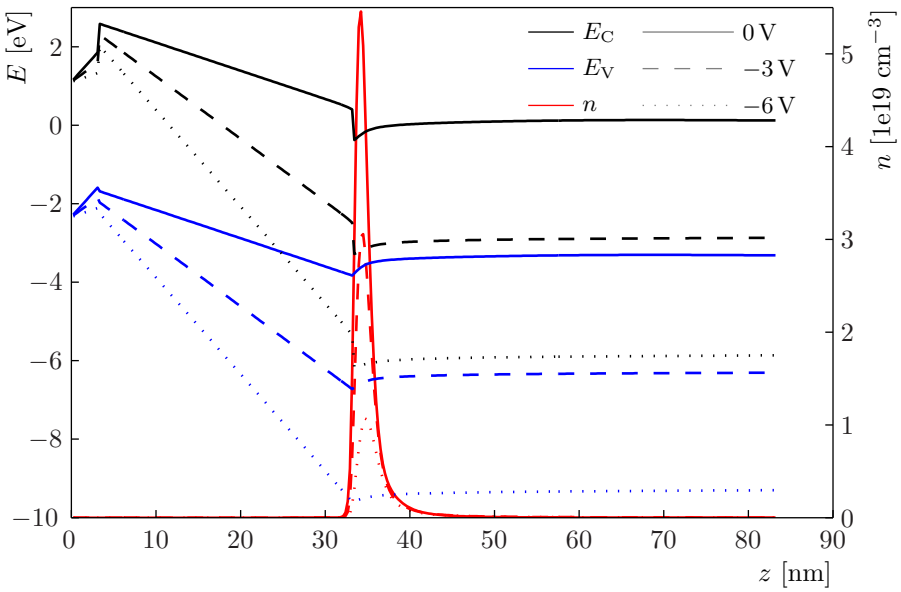


Figure 3.2: Simulated energy bands and charge carrier distribution of a GaN/AlGaN/GaN structure for different biasing conditions. The plot shows the lower conduction band edge (E_C), the upper valence band edge (E_V), and the charge carrier distribution (n). The band structure was simulated by means of WinGreen [54].

velocity for particular electric fields, assuming energy band structures with non-parabolic spherical valleys and incorporating scattering mechanisms as acoustic phonon scattering, non-polar optical phonon scattering, polar optical phonon scattering, ionized impurity scattering, piezoelectric scattering, and alloy scattering. As a result, they formulated an expression for μ to fit the calculated values:

$$\mu = \frac{\mu_0(T,N) + \nu_{sat}\frac{E^{n_1-1}}{E_c^{n_1}}}{1 + a\left(\frac{E}{E_c}\right)^{n_2} + \left(\frac{E}{E_c}\right)^{n_1}}, \tag{3.4}$$

where ν_{sat}, E_c, n_1, n_2, and a are fitting parameters. For GaN, $Al_{0.2}Ga_{0.8}N$, and AlN, ν shows the typical dependence on E as depicted in Figure 3.3(a). For low electric fields, ν increases linearly with E. For higher E it reaches its maximum (ν_{max}), and for even higher electric fields, ν saturates (ν_{sat}) and becomes independent on E. Note, that in this approach only μ_0 depends on temperature and charge carrier concentration.

If expression 3.4 is looked at for low electric fields, then it reduces to $\mu \simeq \mu_0$, and thus ν becomes proportional to E. As mentioned above, the proportionality constant μ_0 depends mainly on T and on n_s. The interrelationship between μ_0 and n_s in a 2DEG is described by Schwierz et al. [125]:

$$\mu_0 = \frac{1}{\frac{1}{a} + \frac{1}{bn_s^c} + \frac{1}{dn_s^f}}, \tag{3.5}$$

where a, b, c, d and f are fitting parameters. Figure 3.3(b) illustrates the above function with parameters found to represent an average fit of experimental data from many

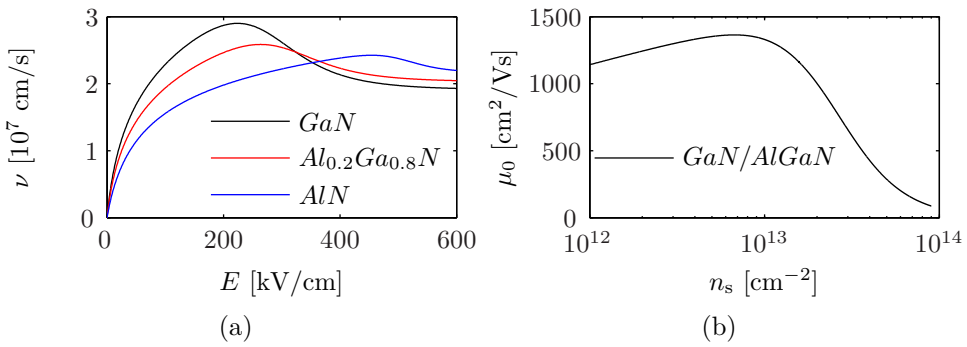


Figure 3.3: Carrier velocity (ν) and low-field mobility (μ_0) in GaN-based devices. The carrier velocity versus electric field (E) plot is based on expression 3.4 using appropriate fitting parameters (a), and μ_0 as a function of sheet carrier concentration (n_s) is plotted according expression 3.5 (b). Room-temperature is assumed.

sources [125].

It is worthwhile noting, that the low-field mobility is not directly dependent on the specific doping level of the HFET device [95]: The only effect an increase (decrease) of doping level has with regards to the low-field mobility is that a lower (higher) gate source bias needs to be applied to reach a certain sheet carrier concentration in the 2DEG.

In summary, the 2DEG can be characterized electrically by means of the sheet charge carrier concentration (n_s), the low-field drift mobility (μ_0), the peak velocity (ν_{max}), and the saturation velocity at high fields (ν_{sat}). But only for μ_0 reliable models exist for the case of two-dimensional transport [125], thus ν_{sat} and ν_{max} can only be used as an estimate. Table 3.1 shows typical mobility and velocity values for important material systems.

Material System	μ [cm^2/Vs]	ν_{max} [10^7cm/s]	ν_{sat} [10^7cm/s]
$GaN/AlGaN$	1400	2.5	2
$GaAs/AlGaAs$	8000	2	0.8
Si (10^{17} cm^{-3} n-doped)	700	1	1

Table 3.1: Low-field drift mobility (μ), peak velocity (ν_{max}), and saturation velocity at high fields (ν_{sat}) for various material systems [125]. Note, that values for ν_{max} and ν_{sat} are for bulk material only.

The knowledge of ν_{sat}, n_s, and μ enables to estimate DC, RF, and power measures of devices utilizing the 2DEG. For instance, the current density (j_{2DEG}) that will be present in the conducting channel in the linear and in the saturation regime can be expressed in terms of ν and n_s as in $j_{2DEG} = qn_s\mu_0 E$ and $j_{2DEG} = qn_s\nu_{sat}$, respectively. Concerning the RF performance of a HFET (e.g. represented by f_T and f_{max}), μ_0 and ν_{max} ought to be high. With regard to power performance, a high n_s mainly matters - besides that

high breakdown fields and a high thermal conductivity of the substrate is of importance for good power performance.

3.2 Heterojunction Field Effect Transistor

The HFET consists essentially of the two dimensional electron gas (2DEG) that forms at the GaN/AlGaN heterojunction (see section 3.1). Two ohmic contacts give access to the channel which are denoted the drain and source electrodes. When a drain-source voltage (V_{ds}) is applied, then the 2DEG acts as a conducting channel which carries the drain current (I_{d}). V_{ds} and I_{d} make up the output of the transistor.

To complete the transistor in principle, a gate electrode is placed on top of the upmost semiconducting layer, located in between the drain and source electrode. By applying a bias between gate and source (V_{gs}), the properties of the 2DEG can be modified and thus I_{d} can be controlled. In general, the current flowing through the Schottky barrier (I_{g}) can not be neglected, and together with V_{gs} it constitutes the input of the device.

The input characteristic of the HFET is determined by a heterostructure diode (HDiode). This bears the chance to study a separate HDiode to gain knowledge concerning the internal HDiode of the HFET. But the so gathered knowledge must only be transferred to the HFET case with care. For instance, to pinch off the HFET, the voltage applied to the input diode needs to be below the threshold voltage (V_{th}). But since the effective bias at the input diode results from the superposition of the applied source drain (V_{ds}) and V_{gs} voltage, it will differ from the applied V_{gs}. Thus, the threshold voltage (V_{th}) identified for a HDiode will differ from the V_{gs} that is needed to pinch off the transistor.

In practice, the transistor will be fabricated in parallel with many other transistors on the same wafer. Thus it is mandatory to insulate the devices from each other electrically. A very efficient way to reach this goal is to take away the AlGaN material in between the regions designated to hold the devices. Without an AlGaN layer, a 2DEG will not form and thus a current can not flow between the devices. Due to their appearance, the remaining AlGaN regions are called mesa. A second practical aspect concerns the accessability of the device for testing purposes. Metal layers are placed in such a way that the gate, source, and drain electrodes can be conveniently contacted with DC and RF probes. For a detailed illustration of the device with all the essential and additional elements see section A.3 of the appendix.

Chapter 4

Gate Dielectrics

This Section will - from a general perspective - cope with issues concerning the gate dielectric itself, namely the permittivity and the resistivity of dielectric films, and the stability of the dielectric/semiconductor interface. Other important issues as the electronic states at the interface and within the dielectric film, the compatibility with yet established processing technologies, thickness and density of the gate dielectrics will be discussed later in part III in the context of the specific dielectric materials investigated in this work.

4.1 Permittivity

Permittivity as a physical quantity describes the interaction between an electric field and a dielectric material: when the material is brought into an electric field ($\underline{E}$), charges are redistributed within its atoms or molecules; the material is said to polarize and a polarization density field ($\underline{P}$) builds up.

The way $\underline{E}$ affects and is affected by the organization of the charges in the dielectric material can be formally expressed by the electric displacement field $\underline{D} = \epsilon_0 \underline{E} + \underline{P}$, with ϵ_0 being the dielectric constant in vacuum. For a linear and isotropic material, $\underline{P}$ relates to $\underline{E}$ by $\underline{P} = \epsilon_0(\epsilon_\mathrm{r} - 1)\underline{E}$, with ϵ_r being the relative dielectric constant - or permittivity. Thus, $\underline{D}$ can be expressed as $\underline{D} = \epsilon_0 \epsilon_\mathrm{r} \underline{E}$. ϵ_r can be a tensor for anisotropic material, and it can be a function of frequency (dielectric dispersion) of the electric field.

It shows, that ϵ_r is the material parameter of choice to characterize the behavior of the material within electric fields. By means of ϵ_r various dielectric absorption mechanisms can be aggregated and elements to be used in lumped circuit models can be defined, such as the capacitance of a plated capacitor $C = \epsilon_0 \epsilon_\mathrm{r} \frac{A}{d^{\mathrm{insul}}}$, where A denotes the area and d^{insul} stands for the thickness of the dielectric.

The main driver of the high-κ research is the International Technology Roadmap for Semiconductors (ITRS) [57], defining the demands for future Si-based transistors. Since the scaling-down of the SiO_2 gate dielectric has reached its technological limits, novel materials that might substitute SiO_2 are desired. That is the reasoning to define high-κ

material as an insulator with a dielectric constant (ϵ_r) larger than that of SiO_2 [84].

The dielectric constant of a high-κ material is higher than in SiO_2 because of ionic polarization: The permittivity of a material results from ionic and electronic polarization (EP). The latter is roughly proportional to the inverse of the band gap. The material with the smallest E_g considered in this work is approximately 60 % of the E_g of SiO_2. If only EP would contribute to ϵ_r of the high-κ material, its permittivity would be only two-third higher compared to SiO_2. Thus, the remaining difference must be due to ionic polarization. Most of the high-κ materials have highly polarizable, often metal-oxygen, bonds which are responsible for the major difference in ϵ_r [37].

The permittivity of a material depends on various parameters, e.g. on the composition as was shown by Reji et al. [140]: the permittivity of ternary rare-earth scandate ($DyScO_3$) is more than twice as high as the permittivities of the binary oxides Dy_2O_3 and ScO_3 (figure 4.1). Due to the structural and electrical similarities of $GdScO_3$ and $DyScO_3$ with respect to the electric properties [50], a similar relationship can be assumed for $GdScO_3$ as well.

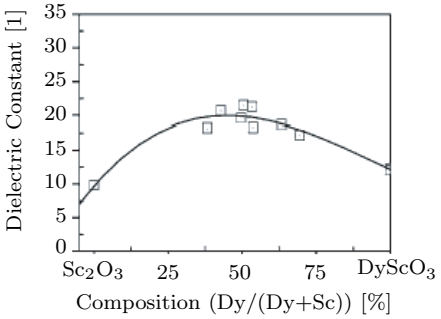


Figure 4.1: Dependence of permittivity of $Dy_xSc_yO_z$ on $Dy/(Dy + Sc)$ composition [140].

The microstructure impacts dielectric properties as well. Polycrystalline films can be problematic when used as gate dielectric: grain size and orientation change throughout a polycrystalline film. This can result in significant variations of the dielectric constant and irreproducible properties. For film thicknesses approaching the grain size this difficulty becomes even more severe [145].

Figure 4.2 plots the permittivity of classical and high-κ materials along the abscissa. Also incorporated into the plot is the bandgap of the materials, which is an indicator for the insulating properties of a gate dielectric which is covered in the following section.

4.2 Insulation

Band Offsets The band gap of a potential gate dielectric is a first indication whether the material is a good insulator. But a far more adopt approach is to look at the relative

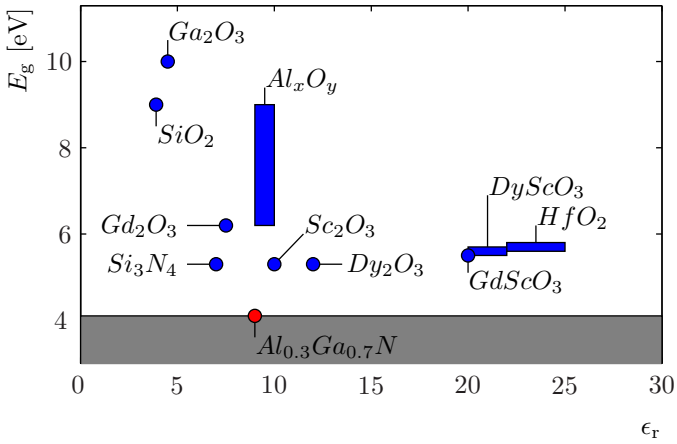


Figure 4.2: Survey of gate dielectrics. A material with a great bandgap (E_g) is likely to be a good insulator. If it combines good insulation with a high permittivity (ϵ_r) it might serve as a gate dielectric for GaN-based devices. The plot illustrates the insulating and dielectric properties of commonly used and novel oxides and nitrides: SiO_2 [49, 119], Si_3N_4 [119], Al_3O_4 [49, 119, 22, 2], Ga_2O_3 [49], HfO_2 [119, 15, 2], ScO_3 [140], Dy_2O_3 [140], Gd_2O_3 [29], $GdScO_3$ [50, 140, 2], $DyScO_3$ [50, 2]. The properties of $Al_{0.3}Ga_{0.7}N$ [49] are also shown, determining a minimum E_g illustrated by the upper edge of the gray square.

alignment of the energy bands of the two adjacent materials, i.e. the valence band (ΔE_{VBO}) and the conduction band offset (ΔE_{CBO}).

The ΔE_{VBO} of a layer stack consisting of material A and B can be defined as the energy difference of the upper valence band edge of the materials A and B. Accordingly, the ΔE_{CBO} is defined as the energy difference between the lower conductance band edge of the materials A and B.

For instance, the lower the ΔE_{CBO} the higher the leakage current which is due to current mechanisms like Schottky emission over the barrier or Poole-Frenkel emission using the electrically active defects in the oxide [84]. As a figure of merit, the ΔE_{VBO} and the ΔE_{CBO} should be higher than 1 eV to reach sufficient insulation properties [133].

There are several ways the energy bands can align relative to each other. Two configurations are of practical relevance for this work: the straddling and the staggered lineups [77] which are depicted in figures 4.3(a) and 4.3(b), respectively. Staggered lineups imply large offsets in either the conduction or the valence band, which can be beneficial for non-optical and unipolar devices [42] as is the case with HFETs.

In the following, the band offsets of the relevant interfaces will be determined in a first-order estimation. Robertson and Falabretti [120] provided a method to calculate the band offsets of various oxide material on GaN based on charge neutrality levels.

$$\Delta E_{CBO} = (\chi_{sem} - \Phi_{CNL,sem}) - (\chi_{ox} - \Phi_{CNL,ox}) + S(\Phi_{CNL,sem} - \Phi_{CNL,ox}), \tag{4.1}$$

$$\text{with } S = \frac{1}{1 + 0.1(\epsilon_r - 1)^2}, \tag{4.2}$$

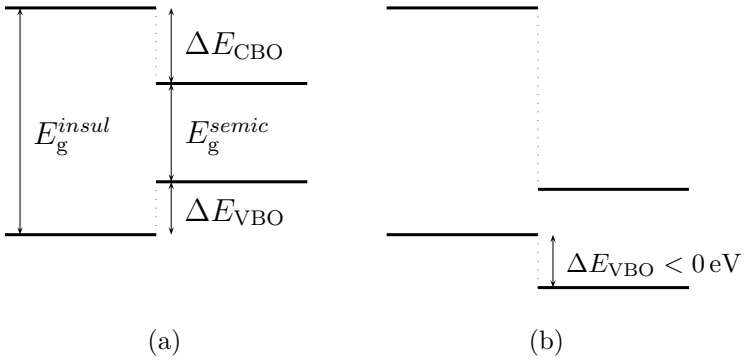


Figure 4.3: Types of energy band linups. The alignment of the energy bands of oxide and semiconductor is crucial to have an insulating effect. The energy bands either align in a straddling (a) or in a staggered (b) lineup [77]. The first type is mandatory for bipolar devices, the latter can be sufficient for unipolar n-type MISHFETs.

$$\Delta E_{\mathrm{VBO}} = E_{\mathrm{g}}^{insul} - E_{\mathrm{g}}^{oxide} - \Delta E_{\mathrm{CBO}}, \tag{4.3}$$

where $\Phi_{CNL,ox/sem}$ denotes the charge neutrality level with respect to the vacuum level, $\chi_{ox/semi}$ stands for the electron affinity. The charge neutrality level of surface and interface states is the position for the Fermi energy level (E_{F}) which renders the semiconductor surface or interface without a net charge. If E_{F} is above the charge neutrality level, the surface is negatively charged. If the Fermi level is below the charge neutrality level, the surface is positively charged.

Figure 4.4(a) and 4.4(b) illustrate respectively the results for various dielectrics on GaN and $Al_{0.3}Ga_{0.7}N$. In the following it is assumed, that due to the n-type conduction of the considered devices only the ΔE_{CBO} is of relevance.

The results confirm the suitability of SiO_2 for insulated-gate GaN applications: $\Delta E_{\mathrm{CBO}} = 2.56\,\mathrm{eV}$, which is far above 1 eV serving as the figure of merit. In this respect, SiO_2 outperforms insulators as Si_3N_4 and Al_3O_4. Hafnium dioxide as one of the gate dielectrics considered in this work shows an inappropriate band alignment. Although it is slightly above the 1 eV limit for GaN interfaces, it is clearly below that figure of merit for AlGaN. Thus, HfO_2 will not be the first choice for GaN-based MIS devices.

The results for $GdScO_3$ are very promising: The ΔE_{VBO} is close to zero or even negative, and since in this work only n-type conduction is assumed, the small valence band offset is not of importance in terms of conduction processes. Moreover, due to the small ΔE_{VBO}, almost the entire difference in band gaps contributes to the ΔE_{CBO}. Thus, the ΔE_{CBO} is far above 1 eV and reaches a value even higher than for SiO_2. It is interesting to note, that the binary oxides Gd_2O_3 and ScO_3 show much lower ΔE_{CBO} values. Only the mixture of both in the form of the ternary $GdScO_3$ makes the big difference - similar to the increase in permittivity discussed in section 4.1.

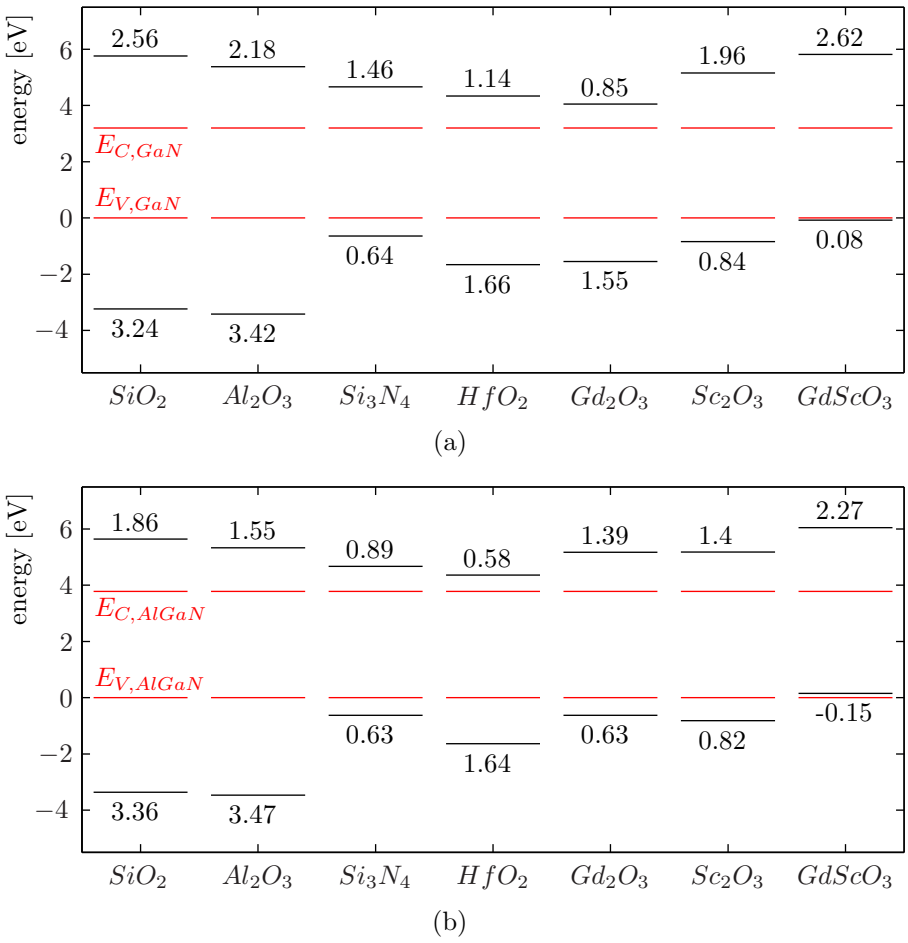


Figure 4.4: Band offsets between various oxides on GaN (a) and $Al_{0.3}Ga_{0.7}N$ (b). The GaN and $Al_{0.3}Ga_{0.7}N$ bandgaps are represented by red lines, the black ones stand for the bandgaps of the oxides. The numbers refer to the conduction (upper row) and valence band offsets (bottom row) in eV, calculated according to the charge neutrality model as in [120].

4.3 Stability

The fabrication of MIS devices implies the formation of semiconductor/insulator and insulator/metal interfaces. These interfaces need to be stable, i.e. reactions inducing the formation of other phases must not occur. The importance of this issue can be well illustrated by an example from research concerned with high-κ gate dielectrics for Si systems. Here, the formation of interlayers, e.g. SiO_2, can have severe impact on the performance of the device. The total capacitance of the device drops drastically, and the prediction of gate currents becomes difficult, since the effective interlayer thickness can not be determined better than 1 nm+-0.25 nm with currently available instruments, which corresponds to an uncertainty of two orders of magnitude in gate current[84].

Stability has a kinetic and a thermodynamic aspect [84]. If thermodynamic equilibrium conditions are assumed, then the thermodynamic stability of an interface can be considered by looking at the Gibbs free energies of the possible phases in a first-order estimate. Locquet at al. [84] demonstrate this procedure for the ZrO_2/Si interface: first they determine the Gibbs free energy of any possible reaction, then they associate each reaction a certain likelihood to occur, and finally they discuss what might happen to the dielectric and insulating properties of the junction if certain phases would be involved.

But even if thermodynamic stability is predicted for a particular interface, interfacial layers may form [145], indicating the need to consider kinetic aspects under non-equilibrium conditions as is the case during deposition. Locquet et al. [84] give some examples on how to approach this issue: for instance, the speed of the formation of certain phases can be derived by estimating the molecular incident rate with accompanying assumptions concerning sticking and oxidation coefficients under certain growth parameters. Or, diffusion related considerations might help to estimate the likelihood of certain phases to form. For instance, the diffusion of gate constituents through the dielectric is enhanced by the presence of grain boundaries for a polycrystalline microstructure.

But within the scope of this work, first-order estimates of the above kind regarding interfaces such as AlGaN/$GdScO_3$ is out of reach. Concerning thermodynamic considerations, too many phases would have to be considered, too limited is the availability of Gibbs free energies. And last but not least, the results would bear a great uncertainty due to general difficulties (validity of bulk-considerations for thin film interfaces, variation of material properties due to strain and material orientation) [84]. And considering the kinetics of deposition processes is of limited use without profound understanding of the thermodynamical issues. Thus, the effort to be invested would not be justified.

Despite the principle difficulties at this point, interface stability needs to be considered in some way, although in the context of GaN/AlGaN devices the problem of interlayers should not play a significant role: Gila et al. [42] showed that dry oxidation of GaN at temperatures below 900 °C results only in a minimal oxidation. Nevertheless, in this work the possibility of interlayers to form will be taken into account when comparing experimentally derived capacitances with values predicted in literature. For instance, if the total capacitance of a $GdScO_3$ HDiode is far less than expected, then a interfacial layer is likely to be involved.

Chapter 5

Metal-Insulator-Semiconductor HFET (MISHFET)

By introducing a dielectric layer, the electrical behavior of the device changes with regard to important aspects such as the gate-source capacitance, the gate current, the drain current, the cut-off frequency, the maximum frequency of oscillation, the gain, and the power added efficiency. This chapter provides models to explain essential differences in device behavior of the MISHFET in comparison to the HFET.

To discuss the impact of the dielectric layer systematically, four aspects of device behavior will be treated in the following, namely the input and the output characteristics under DC conditions, the RF small-signal, and the RF large-signal behavior. For each aspect, well established models will be introduced to explain the behavior of conventional HFET devices. These models will be modified in such a way, that the specific differences in device behavior due to the dielectric layer of a MISHFET become transparent.

5.1 DC Input Characteristic; The Gate-Source Capacitance

The conventional HFET

The gate-source capacitance (C_{gs}) - as one of the key figures to describe the input behavior of a HFET - can be defined as the derivative of the charge (Q) stored in the two-dimensional electron gas (2DEG) with respect to the applied gate-source voltage (V_{gs}):

$$C_{\mathrm{gs}} = \frac{\mathrm{d}Q}{\mathrm{d}V_{\mathrm{gs}}}, \tag{5.1}$$

which can, considering the dependence $Q = q \cdot L_{\mathrm{g}} \cdot W_{\mathrm{g}} \cdot n_{\mathrm{s}}$, also be written in an integral form to express the sheet carrier concentration (n_{s}):

$$n_{\mathrm{s}} = \frac{1}{q \cdot L_{\mathrm{g}} \cdot W_{\mathrm{g}}} \cdot \int C_{\mathrm{gs}}\, \mathrm{d}V_{\mathrm{gs}}, \tag{5.2}$$

where q, L_g, and W_g denote the elementary charge, the gate length, and the gate width, respectively.

Typically, C_{gs} of a GaN/AlGaN device depends on V_{gs} as depicted in figure 5.1(a). From the C_{gs}-level at $V_{gs} = 0\,V$, C_{gs} decreases slightly the more negative V_{gs} becomes. Close to a specific V_{gs}-value denoted as the threshold voltage (V_{th}), C_{gs} reduces significantly by around two orders of magnitude. Integration of C_{gs} according to equation 5.2 yields the dependence of n_s from V_{gs}, as illustrated in figure 5.1(b).

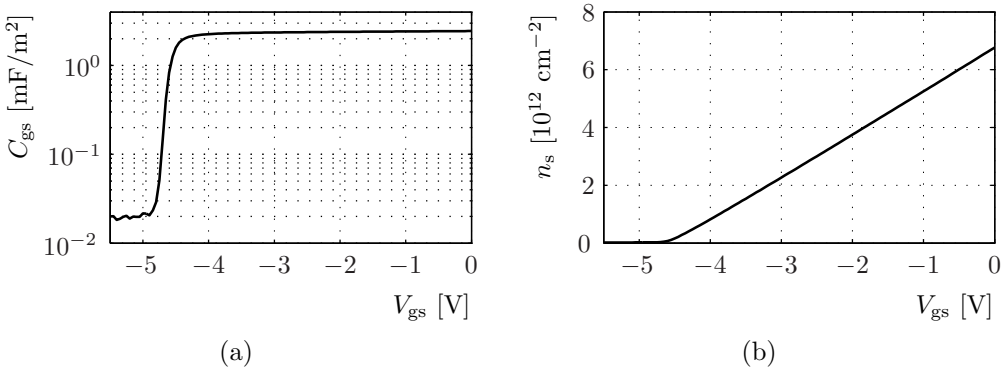


Figure 5.1: Gate-source voltage (V_{gs}) dependence of the gate-source capacitance (C_{gs}) showing the GaN/AlGaN-characteristic C_{gs}-drop at threshold voltage (a), and the corresponding sheet carrier concentration (n_s) scaling almost linearly with V_{gs} (b).

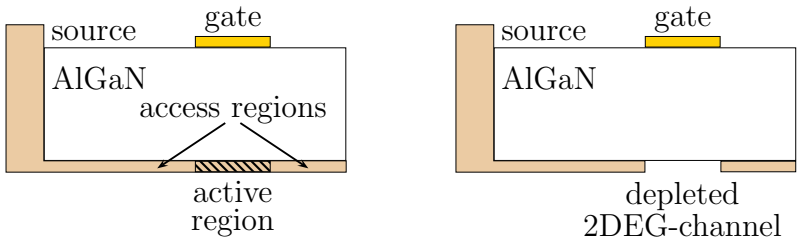
At $V_{gs} = 0\,V$, the C_{gs}-level corresponds to the capacitance of a plated capacitor, with the gate-electrode and the 2DEG underneath the gate - acting as an equipotential plane - being the capacitor-plates. The 2DEG is assumed to have the same electrical potential as the source contact, i.e. all parasitic resistances are neglected. Thus, C_{gs} at $V_{gs} = 0\,V$ can be formally expressed by

$$C_{gs} = \epsilon_0 \cdot L_g \cdot W_g \cdot \frac{\epsilon_r^{semic}}{d^{semic}}, \tag{5.3}$$

where ϵ_0 is the dielectric constant in vacuum, L_g is the gate length, W_g is the gate width, ϵ_r^{semic} is the relative dielectric constant of the semiconducting material, and d^{semic} is the distance between the gate-electrode and the 2DEG. At $V_{gs} = 0\,V$, n_s shows the initial value ($n_{s,0}$) determined by the material and structural parameters of the layer system and to the 2DEG formation mechanism described in section 3.1.

For $V_{th} < V_{gs} \leqslant 0\,V$, C_{gs} varies slightly, which can be explained as follows: The 2DEG is situated underneath the GaN/AlGaN heterointerface and can be attributed a certain thickness. The thickness of the 2DEG varies with the variation of the applied V_{gs}, thus the mean distance between the heterointerface and the 2DEG (d_{ig}) changes. The more negative V_{gs} the greater d_{ig} becomes. For a GaAs/AlGaAs HFET for instance, d_{ig} varies from 8 nm to 20 nm [30]. This corresponds to a plated capacitor whose plates move away from each other. Thus, C_{gs} reduces slightly. Despite the slight variation of C_{gs}, n_s varies almost linearly with V_{gs}. The more negative V_{gs} becomes, the more n_s decreases.

For voltages around V_{th}, the 2DEG underneath the gate-electrode has vanished. As a consequence, the capacitance can not be modeled as a plated capacitor any more, consisting of plates of the size of the gate-electrode as illustrated in figure 5.2(a).



(a) on-state (b) off-state

Figure 5.2: Geometries representing a heterostructure in the on- (a), and the off-state, i.e. with the 2DEG underneath the gate electrode being depleted (b).

Moreover, C_{gs} can be interpreted as the capacitance of a structure consisting of the gate-electrode, the semiconducting material and a source-electrode sided contact formed by the 2DEG of the access region as depicted in figure 5.2(b). For the off-state configuration, less charge can be stored within the system compared to the on-state configuration at identical voltages, i.e. the capacitance of the off-state geometry is significantly reduced compared to the on-state.

Impact of a dielectric layer on the gate-source capacitance

In case of an additional dielectric layer between the gate electrode and the semiconducting material as in MISHFET devices, the total gate-source capacitance ($C_{\text{gs}}^{\text{MISHFET}}$) can be modeled as a series of the capacitance found above for the HFET ($C_{\text{gs}}^{\text{HFET}}$), and a second capacitance which is due to the dielectric layer. In the following, $C_{\text{gs}}^{\text{MISHFET}}$ relative to $C_{\text{gs}}^{\text{HFET}}$ is expressed as a function of the relative dielectric constants for the insulating ($\epsilon_{\text{r}}^{\text{insul}}$) and semiconducting material ($\epsilon_{\text{r}}^{\text{semic}}$), the thickness of the dielectric layer (d^{insul}), and the distance between the 2DEG and the upper side of the semiconducting layer (d^{semic}):

$$C_{\text{gs}}^{\text{MISHFET}} = C_{\text{gs}}^{\text{HFET}} \cdot \left(1 + \frac{\epsilon_{\text{r}}^{\text{semic}}}{\epsilon_{\text{r}}^{\text{insul}}} \cdot \frac{d^{\text{insul}}}{d^{\text{semic}}}\right)^{-1}. \tag{5.4}$$

Due to the additional series capacitance, C_{gs} of the MISHFET will in general be less than that of the HFET. Figure 5.3 illustrates this dilemma for various material and geometrical configurations. The best case for a MISHFET would be to reach C_{gs}-values as close to the $C_{\text{gs}}^{\text{HFET}}$ as possible. To achieve this goal, it is more appropriate to increase the dielectric constant of the insulating material (figure 5.3(a)) rather than to decrease its thickness (figure 5.3(b)).

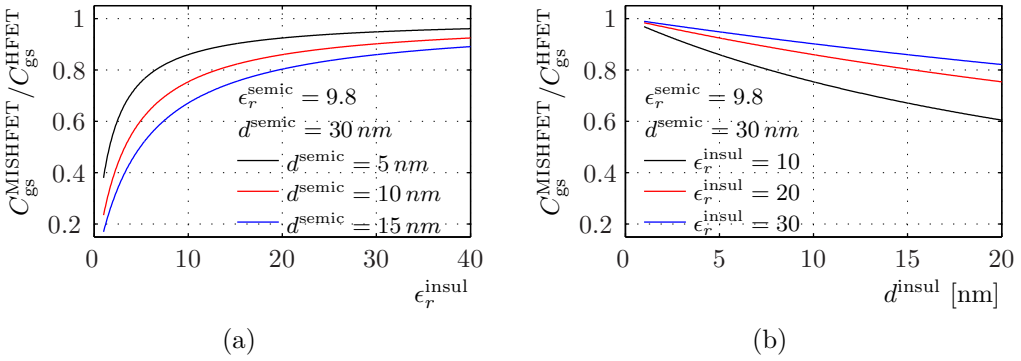


Figure 5.3: The MISHFET- to HFET-capacitance ratio ($C_{gs}^{MISHFET}/C_{gs}^{HFET}$) as a function of the relative dielectric constant of the insulator (ϵ_r^{insul}) (a) and of the insulator thickness (d^{insul}) on top of a 30 nm thick semiconducting layer (b). For low ϵ_r^{insul}, e.g. SiO_2, reducing of d^{insul} has a strong influence on $C_{gs}^{MISHFET}/C_{gs}^{HFET}$, but substitution of the low-κ by a high-κ material outperforms the down-scaling option by far.

Equation 5.4 can also be written in a form to determine the effective insulator thickness (d_{CV}^{insul}) from capacitance voltage measurements, as being frequently used in part III:

$$d_{CV}^{insul} = d^{semic} \cdot \frac{\epsilon_r^{insul}}{\epsilon_r^{semic}} \left(\frac{C_{gs}^{MISHFET}}{C_{gs}^{HFET}} - 1 \right). \tag{5.5}$$

Impact of a dielectric layer on the threshold voltage

To explain the effect of the dielectric layer on the threshold voltage (V_{th}) it may be sufficient to point at the increased gate-to-channel separation as Khan et al. do [69]. Nevertheless, in the following two further alternative explanations will be given. Assume an initial 2DEG sheet carrier concentration for the HFET and the MISHFET of the same amount, i.e. $n_{s,0}^{HFET} = n_{s,0}^{MISHFET}$. Furthermore, assume the gate-source capacitances being constant for $V_{th} < V_{gs} \leqslant 0\,V$. As introduced previously, the gate-source capacitance (C_{gs}) describes the ability to change n_s by changing the gate-source voltage. Due to the fact, that $C_{gs}^{MISHFET} < C_{gs}^{HFET}$, it takes a higher V_{gs} for the MISHFET to deplete the 2DEG compared to the HFET, thus $V_{th}^{HFET} < V_{th}^{MISHFET}$.

An alternative way to explain the higher threshold voltage of the MISHFET is to consider the band diagrams as shown in figure 5.4. The mechanism to control the 2DEG sheet carrier concentration by means of a gate-source voltage is as follows: by applying a negative gate-source voltage, the conduction band is bent in such a way, that the potential well is lifted above the Fermi energy level (figure 5.4(a)). In the MISHFET case, the applied V_{gs} drops partially across the dielectric layer and thus a V_{gs} sufficient to deplete the 2DEG in the HFET case will only partly deplete the 2DEG in the MISHFET case, thus $V_{th}^{HFET} < V_{th}^{MISHFET}$ (figure 5.4(b)).

The partial voltage drop across a series of capacitances can be estimated by the expression

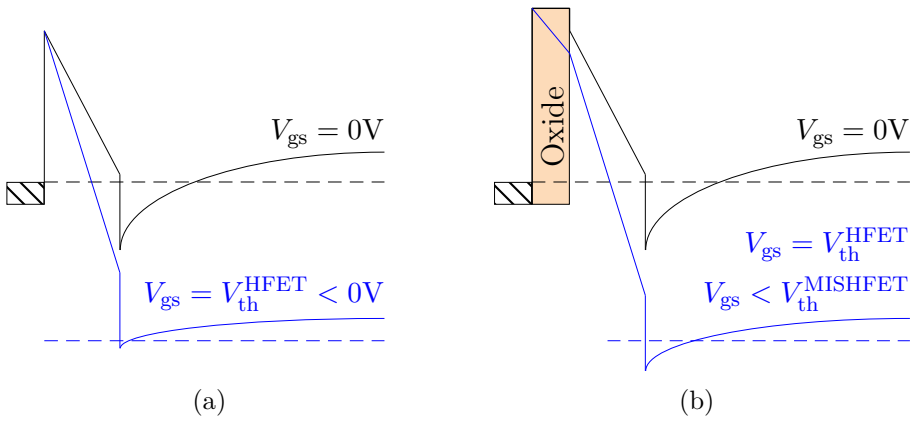


Figure 5.4: Band Diagram to illustrate the differences in threshold voltage (V_{th}) for HFETs (a) and MISHFETs (b). The gate-source voltage (V_{gs}) sufficient to deplete the 2DEG of a HFET, i.e. $V_{gs} = V_{th}^{HFET}$, does not suffice to reach the off-state of a MISHFET, because part of the voltage drops across the insulator and thus does not contribute to the conduction band bending necessary to lift the potential well above the Fermi energy-level to fully deplete the 2DEG, i.e. $V_{gs} = V_{th}^{HFET} > V_{th}^{MISHFET}$.

$V_{semic} = V \cdot \frac{C^{insul}}{C^{insul}+C^{semic}}$. Assuming $C^{semic} = 3\,mF/m^2$ for the semiconducting layer ($\epsilon_r = 9.8$, $d^{AlGaN} = 30\,nm$) and $C^{insul} = 18\,mF/m^2$ for a $GdScO_3$ layer ($\epsilon_r = 20$, $d^{GdScO_3} = 10\,nm$), then 86 % of the applied voltage drops across the semiconducting layer. Assuming a SiO_2 layer instead ($\epsilon_r = 3.9$ and $d^{SiO_2} = 10\,nm$) then only 54 % of the voltage drops across the semiconducting layer. This will - in a very rough first-order approximation - necessitate an almost twofold voltage to be applied to pinch-off of the device.

5.2 DC Input Characteristic; The Gate Current

The conventional HFET

The gate current is an essential aspect to be considered since it influences the RF power performance figures as power gain, saturation output power, linearity, and stability [23]. Furthermore the gate current severely impacts the breakdown characteristic of the devices [138] (figure 5.5(a)), which was also shown numerically [121].

To investigate the impact of a dielectric layer on the gate current it is helpful, to distinguish two major gate current contributions. After the electrons constituting the gate current have passed a Schottky-barrier, they either proceed a) via the semiconducting surface or b) through the semiconductor and via the 2DEG. To finally reach the drain or source contact, the electrons in either case have to surpass an ohmic contact (which is basically a thin Schottky barrier).

With regard to the former mechanism, Miller et al. [101] suggest that Field Emission

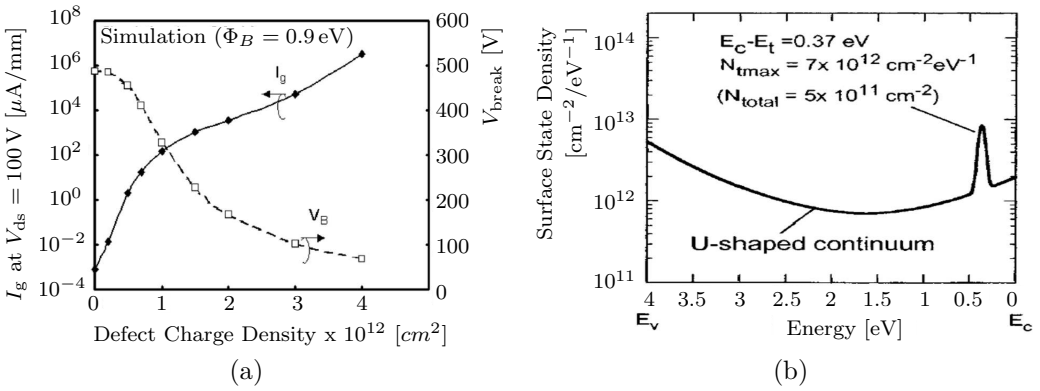


Figure 5.5: Correlation of gate current (I_g) and breakdown voltage (V_{break}) [121] (a) and distribution of surface states [47] (b).

tunneling and dislocation related current mechanisms are responsible for the current via the surface. Tan et al. [138] argue the same way: electrons tunnel through the Schottky barrier and propagate towards the ohmic contacts by hopping from one vacant N-related surface state to the other. In this respect, Hasegawa et al. [47] proposed an appropriate state distribution as depicted in figure 5.5(b).

The gate current contribution via the AlGaN and the 2DEG is primarily determined by the Schottky barrier, which can be concluded by comparing a typically observed gate current of around 1 μA at -5 V through a heterostructure diode (200 μm^2-Schottky contact, 30 nm-thick AlGaN layer) with a hypothetical current of around 200 mA, which would flow through an accordingly sized AlGaN crystal (assuming the conductivity of $Al_{0.3}Ga_{0.7}N$ being two orders of magnitude lower than for GaN [67], which is $\rho_{GaN} = 9\,(\Omega\text{cm})^{-1}$). The typical transport mechanisms through a Schottky barrier are illustrated in figure 5.6.

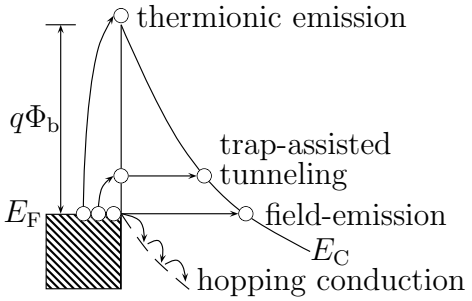


Figure 5.6: Current Mechanisms for a Schottky barrier [101].

The propagation of electrons through the AlGaN or GaN bulk in parallel to the 2DEG plane can be neglected considering the low conductivity of these semiconductors com-

pared to the conductivity of the 2DEG. Figure 5.7(a) illustrates the major gate current contributions for a HFET.

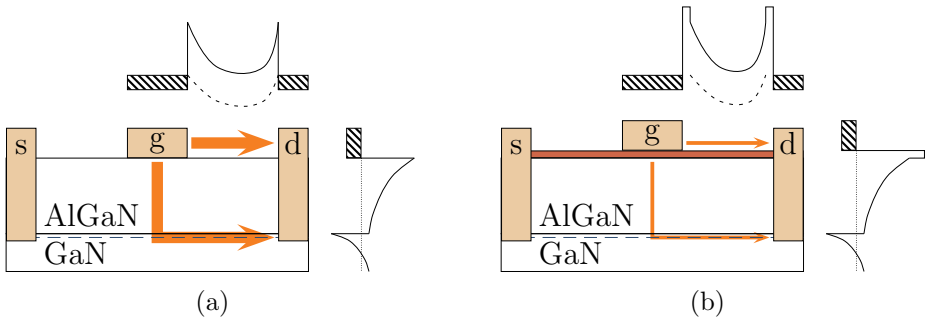


Figure 5.7: Transport mechanisms contributing to the gate current of the HFET (a) and the MISHFET (b). For both device types, electrons propagate from the gate either via the surface or the 2DEG. But for the MISHFET, the propagation along the surface may be hindered by surface passivation and the current along the 2DEG path may be reduced by the substitution of the Schottky Barrier by the more effective MIS contact.

Impact of a dielectric layer on the interface resistivity

For a conventional HFET, the metal/semiconductor interface, i.e. the Schottky contact, is the main gate-current limiting element. One of the main intentions of the MISHFET is to replace the Schottky contact by a Metal-Insulator-Semiconductor (MIS) contact, which is in general a much more effective way to reduce the gate-current.

But although the MIS-contact is in general more effective than the Schottky contact, it nevertheless shows a certain conductivity which is based on various transport mechanisms. In the following, typical MIS-related mechanisms will be listed, some of them having great similarity to Schottky-related processes as Schottky Emission and Field Emission; others do not have a correspondent process in the Schottky-context. The described mechanisms may depend upon each other, but a single one will dominate in certain temperature and voltage ranges [135].

One of the basic transport mechanisms of a MIS-contact is the Schottky Emission, which is very similar to the Thermionic Emission (TE) for Schottky barriers, i.e. carriers gain the energy necessary to overcome the metal/insulator ($V < 0\,\mathrm{V}$) or the insulator/semiconductor barrier ($V > 0\,\mathrm{V}$) from thermal excitation [134]. The higher the band-offsets between insulator and semiconductor, the better the insulation, as was discussed above in section 4.2.

Field Emission (FE) in the context of MIS-devices describes either the ionization of trapped electrons and subsequent tunneling into the conduction band or the direct tunneling of electrons from the metal into the insulator conduction band. The latter variant is identical to the FE-process in the context of Schottky contacts. The FE shows the

strongest dependence on the applied voltage and is essentially independent from temperature.

Since a real MIS structure contains electronic states at the oxide/semiconductor interface and within the insulator itself, state-related conduction mechanisms are likely. Frenkel-Poole Emission is due to field-enhanced thermal excitation of trapped electrons into the conduction band of the insulator. The formal expression is similar to that of the Schottky Emission, only that the factor scaling the electric field in the exponent is twice as large and that the barrier height Φ_B denotes the energetic depth of the trap state relative to the conduction band of the insulator.

Space charge limited current is observed if carriers are injected into the insulator whereas there is not any compensating charge present in the insulator. The space charge limited current scales with the square of the applied voltage. Ohmic conduction denotes the conduction process where electrons proceed from one electronic state of the insulator to another, to be observed at high temperatures and lower biases. Since the carriers obtain their energy from thermic excitation this process is exponentially dependent on the temperature. Ionic conduction is similar to a classical diffusion process.

Impact of a dielectric layer on the surface conductivity

As pointed out before, Field Emission tunneling and dislocation related current mechanisms are held responsible for the current via the surface [101, 138]. A dielectric layer can now impact the current transport in a twofold manner: In the first place, the Field Emission tunneling is hindered by means of an effectively insulating MIS-contact, such that fewer electrons pass the potential barrier and can contribute to the surface current.

Secondly, the surface current is mitigated because surface states are either "buried", so that electrons leaking from the gate can not be trapped, or because Si-atoms - in the case of SiO_2-passivation - replace the donor-like states during the deposition process [142]. In either case, the necessary conditions for a trap "hopping" conduction are not given. Therefore, the incorporation of a dielectric layer may have a reducing impact on the surface-related contribution of I_g.

5.3 DC Output Characteristic

The key figure to describe the DC output characteristic of a HFET is the drain current that can be controlled mainly by the drain-source and the gate-source voltages. It also depends on many other parameters, some of them being influenced by a dielectric layer in case of a MISHFET. The aim of this section is to provide a model to explain the drain current influencing parameters in general and to model the impact of the dielectric layer on the output-current in particular.

The conventional HFET

In the following, a simple and an advanced model to describe and predict the DC output characteristic of a HFET will be derived. Both models are based on the following general expression for the drain current (I_d)

$$I_\mathrm{d} = W_\mathrm{g} \cdot q \cdot n_\mathrm{s} \cdot \nu, \tag{5.6}$$

where W_g is the gate width, n_s is the 2DEG charge carrier concentration, and ν is the 2DEG charge carrier velocity. To derive the dependency of I_d from V_ds and V_gs, certain assumptions need to be made concerning the dependence of n_s and ν on V_ds and V_gs.

Simple Model For a simple model, the assumptions concerning n_s and ν are chosen according to Thayne et al. [139]. The sheet carrier concentration is a function of the gate-source voltage (V_gs) as already introduced in section 5.1 by equation 5.2. Assuming that C_gs remains constant, n_s is a linear function of V_gs for $V_\mathrm{th} \leqslant V_\mathrm{gs} \leqslant 0\,\mathrm{V}$:

$$n_\mathrm{s}(V_\mathrm{gs}) = \frac{C_\mathrm{gs}}{q \cdot L_\mathrm{g} \cdot W_\mathrm{g}} \cdot (V_\mathrm{gs} - V_\mathrm{th}). \tag{5.7}$$

With regard to ν, two cases were distinguished by Thayne et al. In the first case it was assumed, that ν depends linearly on the absolute electric field (E), coupled by the low field mobility of the 2DEG charge carriers (μ_0), i.e. $\nu = \mu_0 \cdot E$. Furthermore, a constant electric field due to V_ds is assumed along the 2DEG channel, i.e. $E = V_\mathrm{ds}/L_\mathrm{g}$ [139]. In the second case it was assumed, that the 2DEG charge carriers have reached the saturation velocity (ν_{sat}), thus $\nu = \nu_{sat}$ [139]. Insertion of the formally expressed assumptions into equation 5.6 yields expressions for the linear (equation 5.8) and the saturation region (equation 5.9) of the DC output characteristic:

$$I_\mathrm{d} = \frac{C_\mathrm{gs}}{L_\mathrm{g}} \cdot (V_\mathrm{gs} - V_\mathrm{th}) \cdot \mu_0 \cdot \frac{V_\mathrm{ds}}{L_\mathrm{g}} \tag{5.8}$$

$$I_\mathrm{d,sat} = \frac{C_\mathrm{gs}}{L_\mathrm{g}} \cdot (V_\mathrm{gs} - V_\mathrm{th}) \cdot \nu_{sat}. \tag{5.9}$$

Differentiating the saturated drain current with respect to the gate-source voltage yields the intrinsic transconductance (g_m):

$$g_\mathrm{m} = \frac{C_\mathrm{gs}}{L_\mathrm{g}} \cdot \nu_{sat}. \tag{5.10}$$

Advanced Model Compared to the simple model, Das [30] based a more advanced model on similar but more demanding assumptions concerning n_s. Here, n_s not only depends on the difference between gate-source and threshold voltage ($V_\mathrm{gs} - V_\mathrm{th}$), but also on the electrical potential due to the drain-source voltage ($V(x)$), which adds to the total

potential underneath the gate-electrode. As above, C_{gs} is assumed to remain constant and n_{s} can be expressed as

$$n_{\mathrm{s}}(x) = \frac{C_{\mathrm{gs}}}{q \cdot L_{\mathrm{g}} \cdot W_{\mathrm{g}}} \cdot (V_{\mathrm{gs}} - V_{\mathrm{th}} - V(x)) \,. \tag{5.11}$$

With respect to the charge carrier velocity (ν), Das chose a non-linear relationship between ν and electrical field (E), utilizing the critical field E_{c} at which the carrier velocity attains half of its saturation velocity given by $\nu_{sat} = \mu_0 \cdot E_{\mathrm{c}}$:

$$\nu = \frac{\mu_0 \cdot E}{1 + \frac{E}{E_{\mathrm{c}}}}, \tag{5.12}$$

Insertion of equations 5.11 and 5.12 into the general equation for I_{d} (equation5.6) and integration of the expression over x results in an expressions for the linear regime (equation 5.13), and analyzing the maximum of I_{d} yields an appropriate expression for the saturation drain current (equation 5.14) (For a detailed derivation of the expressions for I_{d} refer to [30, p. 30]):

$$I_{\mathrm{d}} = \frac{C_{\mathrm{gs}}}{L_{\mathrm{g}}} \left((V_{\mathrm{gs}} - V_{\mathrm{th}}) \cdot \mu_0 \cdot \frac{V_{\mathrm{ds}}}{L_{\mathrm{g}}} - \mu_0 \cdot \frac{V_{\mathrm{ds}}^2}{2L_{\mathrm{g}}} \right) \cdot \left(1 + \frac{V_{\mathrm{ds}}}{V_{\mathrm{c}}} \right)^{-1} \tag{5.13}$$

$$I_{\mathrm{d,sat}} = \frac{C_{\mathrm{gs}}}{L_{\mathrm{g}}} \cdot (V_{\mathrm{gs}} - V_{\mathrm{th}} - V_{\mathrm{ds,sat}}) \cdot \nu_{sat}, \tag{5.14}$$

$$V_{\mathrm{ds,sat}} = \sqrt{V_{\mathrm{c}}^2 + 2V_{\mathrm{c}} \cdot (V_{\mathrm{gs}} - V_{\mathrm{th}})} - V_{\mathrm{c}}, \text{ and} \tag{5.15}$$

$$V_{\mathrm{c}} = L_{\mathrm{g}} \cdot E_{\mathrm{c}}. \tag{5.16}$$

Differentiating the saturated drain current with respect to the gate-source voltage yields the intrinsic transconductance (g_{m}):

$$g_{\mathrm{m}} = \frac{C_{\mathrm{gs}}}{L_{\mathrm{g}}} \cdot \left(1 - \left(1 + 2 \cdot \frac{V_{\mathrm{gs}} - V_{\mathrm{th}}}{V_{\mathrm{c}}} \right)^{-\frac{1}{2}} \right) \cdot \nu_{sat} \tag{5.17}$$

Parasitic resistances The above considerations were based on the assumption that parasitic resistances could be neglected. One way to model the effects of the source (R_{s}) and the drain resistance (R_{d}) is to substitute all occurrences of V_{gs} and V_{ds} in the above expressions by

$$V_{\mathrm{gs}} = V'_{\mathrm{gs}} - I_{\mathrm{d}} R_{\mathrm{s}}, \tag{5.18}$$

$$V_{\mathrm{ds}} = V'_{\mathrm{ds}} - I_{\mathrm{d}} \cdot (R_{\mathrm{s}} + R_{\mathrm{d}}), \tag{5.19}$$

where V'_{gs} and V'_{ds} denote the voltages applied to the gate-source and the drain-source contacts, respectively. Figure 5.8(a) illustrates the results of a matlab-routine solving the system of equations 5.13, 5.18, and 5.19 numerically, utilizing common values for a GaN/AlGaN HFET.

From figure 5.8(a) it is apparent. that the parasitic source resistance (R_s) has major impact on the output of a HFET device. The higher R_s, the lower the saturation drain current ($I_{d,sat}$), the less steep the slope of I_d in the linear regime, and thus the higher the drain source bias at which drain current saturates ($V_{ds,sat}$). The parasitic drain resistance (R_d) also impacts the output of a HFET device. The higher R_d, the less steep the I_d-slope in the linear regime, the higher $V_{ds,sat}$ at which the drain current saturates. In contrast to the influence of R_s, R_d does not affect $I_{d,sat}$. Obviously, the I_d-reducing effect of R_s has a negative impact on g_m as well, as shown in figure 5.8(b).

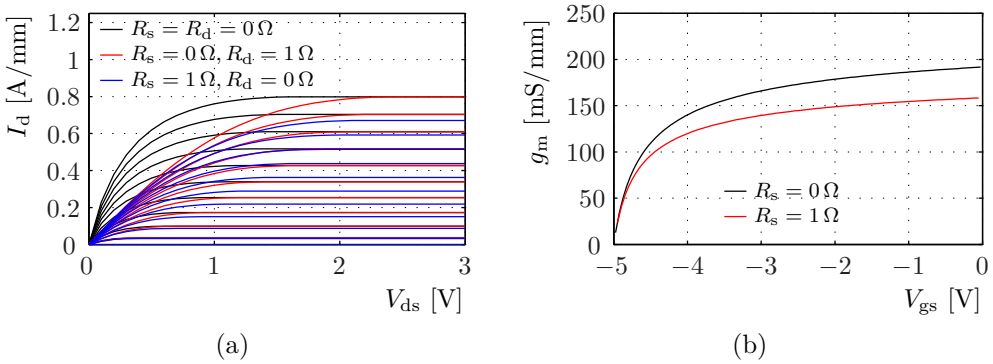


Figure 5.8: Influence of the drain and source resistances (R_d and R_s) on the drain current and the knee voltage (I_d, $V_{ds,sat}$) (a) and the transconductance (g_m) (b). $R_d > 0\,\Omega$ does not impact $I_{d,sat}$ but increases $V_{ds,sat}$, whereas $R_s > 0\,\Omega$ decreases $I_{d,sat}$ and shifts $V_{ds,sat}$. $R_s > 0\,\Omega$ lowers g_m.

Besides the resistive parasitics, C_{gs} and V_{th} will also impact the output characteristic and the transconductance of a HFET, as is shown in figures 5.9(a) and 5.9(b), respectively.

Output characteristics of real devices will deviate from the characteristic shown in figure 5.8(a) as the slope of I_d in the saturation regime is negative, which is due to channel heating effects [18]. Since it is not expected that a dielectric layer will impact this specific aspect, it will not be treated in depth in the following course of discussion.

Impact of a dielectric layer on the drain current

Impact of the dielectric layer on sheet carrier concentration As discussed in section 3.1, the formation of the 2DEG is due to the heterointerface and related physical effects. Thus, a certain sheet carrier concentration (n_s) is given in the 2DEG. Depending on the conditions at the semiconductor surface, n_s is subject of change. The surface condition is mainly determined by electronic states. For instance, Wolter al. [146] found AlGaN surface states with an activation energies of 2.84 eV and 3.25 eV. Ibbetson [53] reported on 1.65 eV surface donors with a density of at least $1.1 \cdot 10^{13}$ cm^{-2}.

In the following, the impact of surface- and interface-states on the behavior of devices based on GaN/AlGaN will be explained briefly. In particular, ionized N_2-vacancy related deep donors play a dominant role in GaN/AlGaN-heterostructures. For instance,

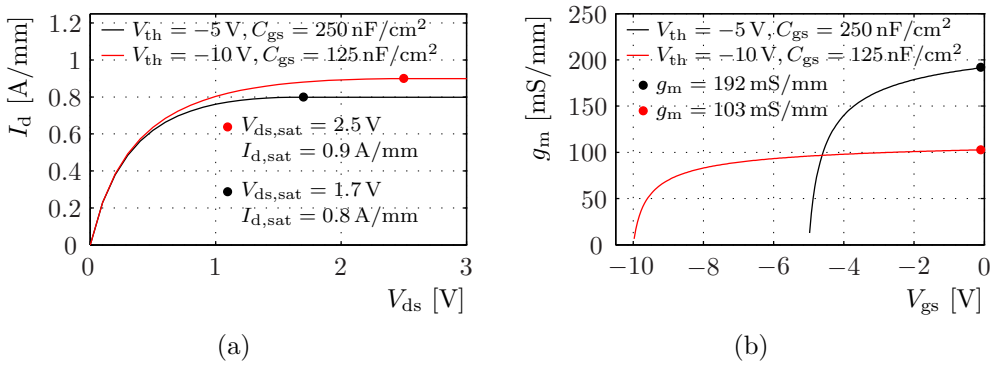


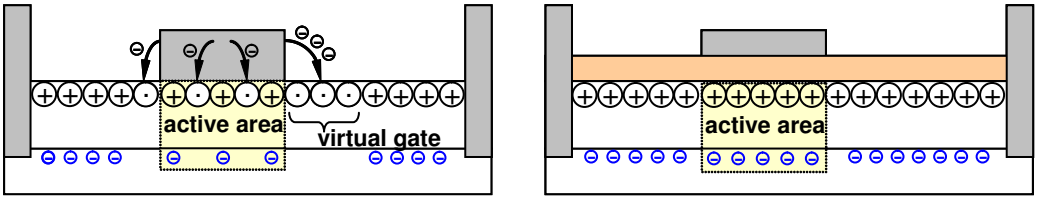
Figure 5.9: Influence of the gate-source capacitance and threshold voltage (C_{gs} and V_{th}) on the drain current and the knee voltage (I_d, $V_{ds,sat}$) (a) and the transconductance (g_m) (b). A reduction of C_{gs} with correspondingly increased V_{th} - as is the case for MISHFETs - increases both $I_{d,sat}$ and $V_{ds,sat}$. A reduction of C_{gs} with correspondingly increased V_{th} leads to a reduced g_m, but g_m does not decrease exactly linearly with C_{gs}, an important fact concerning the RF properties ($f_T \propto g_m/C_{gs}$, see section 5.4).

Hasegawa [47] proposed continuously distributed surface states together with a deep donor surface state located at around $E_C - 0.37\,eV$ associated with nitrogen vacancies (figure 5.5(b)).

Depending on their location, these states have different impact on the device-behavior: if they are located in the AlGaN-layer near the free surface between the electrodes, these states can trap electrons. As a consequence, the positive net charge at the free surface of the GaN/AlGaN-heterostructure is partially compensated, thus the gate depletion region extends to the drain-side and the source-resistance increases due to a decrease of charge carrier concentration in the 2DEG regions between the electrodes. This mechanism has similar effects as a reversely biased gate, thus it is also denoted as virtual gate. The virtual gate mechanism also depends upon the frequency of applied gate-source-voltage and causes the phenomenon of DC/RF-current-dispersion [142].

If the donor-like states are located in the AlGaN-layer below the gate and close to the metal/AlGaN-interface, then electrons can also be trapped and the charge-balance is changed in such a way that the charge carrier concentration in the active region of the 2DEG decreases. Since these interface-states are caused e.g. by ion-bombardment during gate-metallization, coating of the AlGaN-layer before metallization can prevent the formation of traps [47].

Passivation can prevent the formation of a virtual gate, although the exact mechanism is not entirely clear yet. It is suggested that either surface states are “buried”, so that electrons leaking from the gate can not be trapped, or that Si-atoms - in the case of SiO_2-passivation - replace the donor-like states during the passivation process [142]. Also, a suppression of carrier transport along the passivated surface might be taken into account as an explanation. Therefore, the incorporation of a dielectric layer can have a significant impact on n_s, if it can be attributed a surface passivating effect.



(a) (b)

Figure 5.10: Surface state related effects. For a HFET, donor-like states near the surface may trap electrons leaking from the gate. The electrons can propagate along the surface towards the drain forming a surface current, and/or the electrons contribute to the formation of a virtual gate as they reduce the sheet carrier concentration in the 2DEG in the active and the access regions of the device (a). For the MISHFET, the dielectric layer passivates the surface and thus reduces the aforementioned effects (b).

Impact of the dielectric layer on the knee voltage

As seen before, the introduction of a dielectric layer results in an increase of V_{th}. According to equation 5.15, this will affect the drain-source voltage, at which the saturation current will be reached. To get an idea, consider the following comparison: A GaN/AlGaN HFET might have a V_{th} of $-5\,\mathrm{V}$ and a $V_{\mathrm{ds,sat}}$ of $1\,\mathrm{V}$. According to equation 5.15 this results in a V_{c} of around $0,125\,\mathrm{V}$. Using the same V_{c}-value for a MISHFET with $V_{\mathrm{th}} = -10\,\mathrm{V}$, then the same formula yields a 46 % increase in $V_{\mathrm{ds,sat}}$. Thus, the impact of the insulation layer will have a serious impact on the $V_{\mathrm{ds,sat}}$-value, if the V_{th}-increase is significant.

Impact of the dielectric layer on the transconductance

In a simple approach, a decrease in gate-source capacitance due to the introduction of a dielectric layer impacts the transconductance in the same extend: according to equation 5.10, a 50 % decrease in C_{gs} results in a 50 % decrease in g_{m}.

But taking into account the more sophisticated expression 5.17, then it becomes apparent that for HFET and MISHFET the transconductance is corrected by a factor smaller than one, i.e. $g_{\mathrm{m}} < C_{\mathrm{gs}}/L_{\mathrm{g}} \cdot \nu_{sat}$. But due to the fact that $V_{\mathrm{th}}^{\mathrm{MISHFET}}$ is in general greater than $V_{\mathrm{th}}^{\mathrm{HFET}}$, the correction factor is greater for the MISHFET, thus the decrease in g_{m} due to the C_{gs}-decrease is partly compensated by the V_{th}-increase.

Figure 5.9(b) illustrates this effect: Compared to a HFET, a MISHFET with a V_{th} twice as high and half the C_{gs} shows a g_{m} which is only reduced by 46 %. This finding will become important, when the consequences of the dielectric layer will be discussed in the context of RF properties in section 5.4.

5.4 Small Signal Model

The previous sections introduced models aiming at the DC device behavior. In the following, a small-signal model and related measures will be presented to enable the investigation of RF frequency limits of HFETs and MISHFETs. Since the devices under consideration are meant to be used in amplifier applications, the main interest is to have measures that reflect the ability of the device to amplify the applied signals.

The conventional HFET

A commonly used model to investigate the RF device performance is the small signal model which is able to describe and predict the behavior of the device if an alternating voltage with an amplitude not exceeding the order of the thermal voltage (approximately 26 mV at room-temperature) is applied. One way to determine the values of the model elements is to perform S-parameter measurements (see appendix B.3). The measured and derived values of the lumped elements of the equivalent circuit are valid only a) for a distinct working point defined by the biasing conditions, i.e. V_{gs} and V_{ds}, and b) for the specific characteristic of the applied signal, in particular its oscillating frequency (f). Figure 5.11 illustrates the equivalent circuit used hereafter.

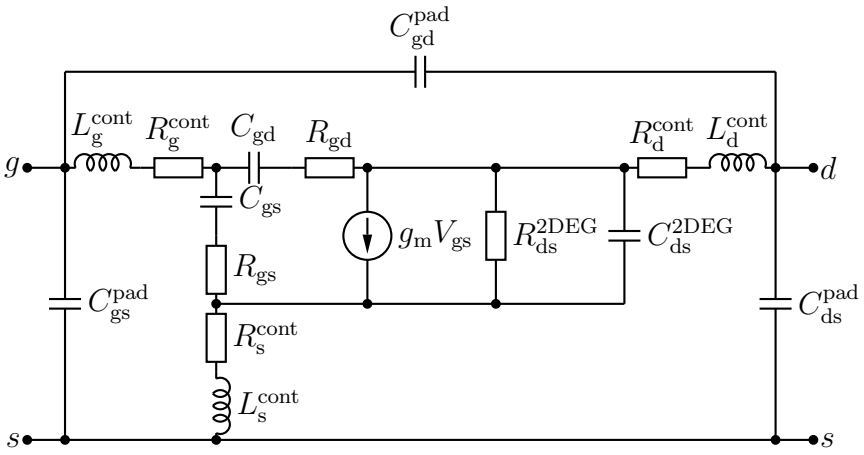


Figure 5.11: Equivalent circuit of the HFET and MISHFET to model the small signal RF behavior. In particular, the model enables the quantitative explanation of figures as cutoff frequency and maximum frequency of oscillation in terms of lumped circuit elements, which can be extracted from S-parameter measurements.

One measure of great importance in the context of this work is the short current gain, i.e. the drain to gate current ratio with the output shorted, since the power delivered by the device is proportional to the square of the output current. By means of the above small-signal model and neglecting all elements but C_{gs} and g_{m}, the following expression

can be derived for the short current gain

$$\frac{I_\mathrm{d}}{I_\mathrm{g}} \approx \frac{g_\mathrm{m}}{\jmath\, 2\pi f \cdot C_\mathrm{gs}}. \tag{5.20}$$

The frequency at which the short current gain becomes unity is defined as the cutoff frequency (f_T) and serves as an indicator for the frequency limit for the device operation as a power amplifier. Derived from the simplified current gain in equation 5.20, f_T is proportional to g_m and inversely proportional to Cgs:

$$f_\mathrm{T} \propto \frac{g_\mathrm{m}}{C_\mathrm{gs}}. \tag{5.21}$$

Taking into account the expressions for g_m derived in section 5.3, f_T can be related to the saturation velocity of charge carriers in the 2DEG (ν_{sat}) the gate length (L_g), the gate-source voltage (V_gs) and the threshold voltage (V_th):

$$ft \propto \frac{\nu_{sat}}{L_\mathrm{g}}, \text{ according equation 5.10, or} \tag{5.22}$$

$$\propto \frac{\nu_{sat}}{L_\mathrm{g}} \cdot \left(1 - \left(1 + 2 \cdot \frac{V_\mathrm{gs} - V_\mathrm{th}}{V_\mathrm{c}}\right)^{-\frac{1}{2}}\right), \text{ according equation 5.17.} \tag{5.23}$$

A more accurate formulation for f_T incorporating the parasitic capacitances and resistances of the small-signal equivalent circuit model is given by

$$f_\mathrm{T} = \frac{g_\mathrm{m}}{(C_\mathrm{gs} + C_\mathrm{gd})} \cdot \frac{1}{\left(1 + \frac{R_\mathrm{d}+R_\mathrm{s}}{R_\mathrm{ds}}\right) + C_\mathrm{gd}\; g_\mathrm{m} \cdot (R_\mathrm{d} + R_\mathrm{s})} \text{ [139].} \tag{5.24}$$

Another important measure utilized in this work is the maximum available gain (MAG), which is defined as the forward power gain under optimum matching conditions at both input and output [139]. The maximum frequency of operation (f_max) is the frequency at which the MAG falls to unity. The formal expressions derived from the small signal model for MAG and f_max are

$$MAG = \frac{\left(\frac{f_\mathrm{T}}{f}\right)^2}{4\frac{R_\mathrm{s}+R_\mathrm{g}+R_\mathrm{gs}}{R_\mathrm{ds}} + 4\pi \cdot f_\mathrm{T} \cdot C_\mathrm{gd}\,(2R_\mathrm{g} + R_\mathrm{gs} + R_\mathrm{s})}, \text{ and} \tag{5.25}$$

$$f_\mathrm{max} = \frac{f_\mathrm{T}}{\sqrt{4\frac{R_\mathrm{s}+R_\mathrm{g}+R_\mathrm{gs}}{R_\mathrm{ds}} + 4\pi \cdot f_\mathrm{T} \cdot C_\mathrm{gd}\,(2R_\mathrm{g} + R_\mathrm{gs} + R_\mathrm{s})}}. \tag{5.26}$$

Impact of a dielectric layer on the cutoff frequency

From equation 5.21 it is known, that f_T is proportional to ν_{sat} and inversely proportional to L_g. Since L_g is of the order of some hundreds of nanometers, it does not (effectively) change by the introduction of a dielectric layer of some tens of nanometers. Therefore,

the only possibility for f_T to change is due to a change in ν_{sat}. But per definition, the saturation velocity can not be changed. It describes the fact, that the carrier velocity has become field-independent because a certain electrical field has been exceeded (see also section 3.1). In this sense, the saturation velocity would have to be treated as a constant and would not be affected by any dielectric-layer-induced impact .

But two arguments open up the way to treat the velocity of carriers not as a constant in the actual context: First of all, the concept of the saturated velocity originates from the investigation of carrier transport problems in bulk material. But According to Schwierz et al. little is known on the high field transport in GaN/AlGaN-2DEGs [125]. Secondly, the electric fields in the 2DEG that result from the bias conditions used in this work should not be classified as high-fields. For instance, a bias of 20 V and a channel of 700 nm-length will result in an approximate electrical field of 300 kV/cm field far away from high-field conditions (compare figure 3.3(a)). In conclusion, the velocity of the 2DEG-carriers that determines f_T is not necessarily a constant. It can be well assumed to be dependent on the electric field and the mobility, which is dependent from 2DEG-properties as the sheet carrier concentration (n_s).

Thus, an impact of the dielectric layer on mobility and the f_T-determining velocity is assumed to be possible. A potential mechanism is that the dielectric layer passivates the surface, changes n_s, therefore influences the carrier mobility, and finally impacts the f_T-determining velocity. But since it is not known whether an increase of n_s enhances carrier mobility (better screening) or reduces mobility (carrier scattering), a possible passivation effect might both increase or decrease f_T.

Another possible impact on the 2DEG charge carrier mobility is due to the screening of the Coulomb interactions of the charged surface and the interface states by electrostatic induction in the gate metallization of the MOSHFET as shown by Marso et al.[19]. They utilized channel-conductivity methods and time-delay evaluations to investigate the influence of a 10 nm-thick SiO_2 layer of a GaN/AlGaN MISHFET which revealed a 50 % mobility and a 45 % RF small-signal performance increase compared to a HFET.

Besides ν_{sat} and L_g, equation 5.23 offers another parameter to explain a possible impact of the dielectric layer on f_T: a change in threshold voltage (V_{th}). For devices with a high V_{th}, as for SiO_2-MISHFETs, the V_{th}-dependent factor correcting the ν_{sat}/L_g-ratio will be closer to unity than for a device with smaller V_{th}. For a SiO_2-MISHFET with $V_{th} = -10\,V$, a higher f_T will be observed than for a conventional HFET with $V_{th} = -5\,V$, although this effect will not make up more than a few percent.

In addition to the V_{th}-related effect, equation 5.24 reveals that a higher gate-drain capacitance (C_{gd}) and increasing source and drain resistances (R_s and R_d, respectively) will decrease f_T. With regard to the capacitive parasitic, the introduction of a dielectric layer increases C_{gd}, since the gate-drain capacitance due to the insulation layer (C_{gd}^{insul}) can be modeled as an additional capacitance in parallel to the gate-drain capacitance of the HFET (C_{gd}^{HFET}), thus $C_{gd}^{HFET} + C_{gd}^{insul} \equiv C_{gd}^{MISHFET} > C_{gd}^{HFET}$. Therefore, capacitive effects will reduce f_T.

Concerning the resistive parasitics, the impact of the dielectric layer towards an increased or decreased f_T is not as obvious. Assuming that the dielectric layer passivates the

surface and thus impacts the carrier concentration (n_s) of the 2DEG-channel in the access areas of the device, then it is not to say whether the mobility of carriers increases (better shielding) or decreases (more scattering). Thus it is undecided at this point of discussion, whether the dielectric layer evokes a change in R_s and R_d beneficial for an increased f_T.

In Summary, there is not a clear indication at this point of discussion, whether a dielectric layer is obstructive or beneficial for an increase of f_T. The f_T-reducing increase of C_{gd} may be reinforced or compensated by passivation-related effects - depending on the specific material and structural parameters of the device.

Impact of the dielectric layer on the maximum frequency of oscillation

From equation 5.26 it is obvious, that f_{max} is mainly determined by f_T, i.e. a MISHFET showing improved f_T-values compared to a HFET will reach higher f_{max}-values as well. This general correspondence is affected to a certain but subordinate degree by parasitic capacitances and resistances.

But with the strong dependence of f_{max} on f_T, the difficulty to establish a definitive prediction whether the MISHFET or the HFET will reveal superior f_{max}-results replicates. The question whether a particular MISHFET possesses better RF-properties than a conventional HFET will only be decided by the experiment. But although a thorough prediction can not be offered due to the many uncertainties, the above discussion provides the knowledge and the f_T- and f_{max}-affecting parameters to explain the results gained from the experiments covered in part III of this thesis.

5.5 Large Signal Model

The HFETs and MISHFETs under consideration will serve as devices in high power, high frequency amplifiers. Typical criteria to characterize a power amplifier are center frequency and frequency bandwidth, transmission gain, output power, power added efficiency, linearity, return loss, and operating temperature [23].

In this section, the influence of the insulation layer of a MISHFET will be modeled with regard to the RF-power performance of the device. In the context of this work, output power, gain, and PAE will be investigated mainly. Linearity, noise, and bandwidth aspects will not be covered since the transistors treated in this work are not meant for optimized low noise, high linearity, or broad band applications.

The conventional HFET

A simple amplifier stage consists of a transistor, the DC power supply circuits, the input-, and the output matching networks. The DC conditions determine the operating point

and the load line and thus serve as a means to adjust the characteristics of the amplifier in terms of output power, linearity, and efficiency.

The various conditions are categorized into classes as illustrated in figure 5.12(a). The classes A, B, AB, and C describe operational conditions where the transistor serves as a controlled current source in an amplifier, high efficiency class E and class F amplifiers use the transistors as a switch [23]. In a class A amplifier, the transistor is biased and driven in a way that the complete swing of the output current is within the saturation region of the transistor, thus the class A amplifier features the highest linearity in comparison to other classes but has the drawback of low efficiency due to high DC power consumption.

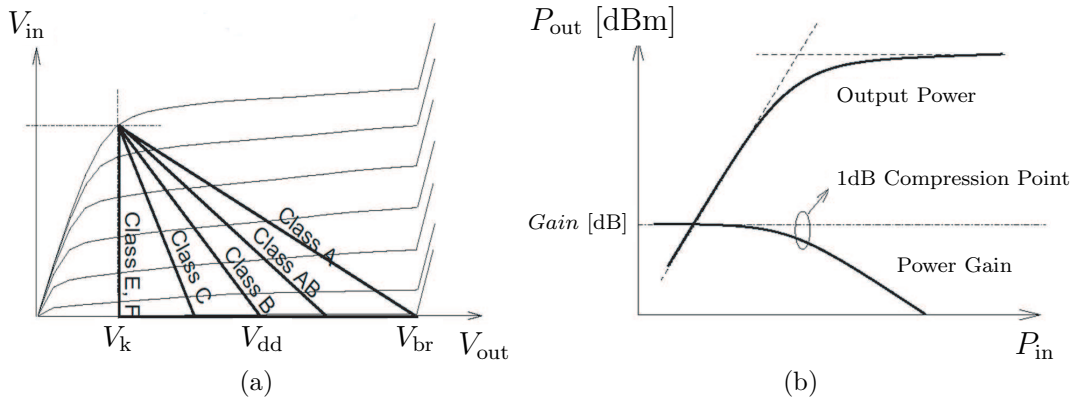


Figure 5.12: Categorization of amplifier operating classes depending on specific load configurations [23] (a), illustration of the definition of the output power (P_{out}) at 1 dB compression [23] (b).

Output Power The output power of each amplifier stage is a function of the RF drain current and the supply voltage. For power amplifiers, the output of the transistor is matched to an optimum load resistance to provide maximum available output power. In the DC characteristic of the transistor, the load can be depicted as a load line.

The output power increases as the input power is raised until it comes to the point of saturation where the power gain begins to drop. A power amplifier is normally driven to the beginning of the saturation, where the gain drops by 1 dB at the so-called 1 dB-compression point and the efficiency is maximum (figure 5.12(b)).

For a class A driven transistor, the RF voltage swing along the load line is limited by the knee voltage ($V_{ds,sat}$) and the breakdown voltage (V_{break}). The drain current through the load is maximum ($I_d = I_{d,sat}$) at the bias point where $V_{ds} = V_{ds,sat}$ (figure 5.12(a)). Thus, the RF output power of a device in class A operation can be estimated by the following expression

$$P_{out}^{RF} = \frac{1}{8} \cdot I_{d,sat} \cdot (V_{break} - V_{ds,sat}). \tag{5.27}$$

Since the drain current (I_d) is inversely proportional to the drain source distance (d_ds), a short distance between the electrodes would be preferable with respect to $I_\mathrm{d,max}$. But on the other hand, a small distance decreases V_break. To overcome this dilemma, the Field-Plate technology can be applied.

Due to trap related effects, e.g. DC/RF dispersion, the RF power performance of the device can be smaller than predicted from the DC measures. This is the reason why large-signal measurements under matched conditions (see section B.4) are indispensable. The phenomenon of DC/RF dispersion is closely related to surface states, as already discussed in section 5.3.

A closely related and commonly used measure is the output power density (p_out), which is simply defined as P_out normalized to the gate width (W_g). It has to be noted, that for devices with large W_g, p_out is usually smaller than for devices with small W_g due to heat dissipation issues.

Linearity Linearity is a strong requirement for power amplifiers [148, 23]. If this requirement is not fulfilled, non-linearities can cause signal errors and perturbations in the time-domain. In the frequency domain, non-linearities cause spectral regrowth and lead to interferences of the adjacent bands, as depicted in figure 5.13(a). As a consequence, power leaks to the harmonics and thus the output power and efficiency are being reduced. Furthermore, safety margins need to be introduced between the frequency bands, which reduces the bandwidth capacity. Last but not least, nonlinearities can generate a DC component which modifies the DC bias point of the active device.

The power of the third order intermodulation products is proportional to the cube of the input power whereas the output power of the fundamentals is linearly proportional to the input power. The intercept point of the extrapolated fundamental and the third order responses is called third order intercept point (IP3), which serves as an indication for the operation becoming nonlinear as the input power increases - which is illustrated in figure 5.13(b).

In a rough first-order approximation, a transconductance (g_m) being constant over the V_gs operating range implies linear amplification under RF conditions [69]. This enables a rough comparison of devices in terms of linearity by means of a simple measure derived from the DC characteristics.

Gain For a power amplifier, the *Gain* is defined as the ratio of input power level ($P_\mathrm{in}^\mathrm{RF}$) to the output power level ($P_\mathrm{out}^\mathrm{RF}$), usually expressed in (pseudo) units of dB:

$$\frac{Gain}{\mathrm{dB}} = 10 \log \left(\frac{P_\mathrm{in}^\mathrm{RF}}{P_\mathrm{out}^\mathrm{RF}} \right). \tag{5.28}$$

To provide the required *Gain*, several amplifying stages are frequently needed. However, the number of stages must be limited since parasitics, loss and noise generated in each stage can affect the overall efficiency of the power amplifier. Thus, a high *Gain* per stage is desirable. In some case, e.g. for the sake of bandwidth or stability, the specified *Gain* of a stage is lower than the maximum obtainable gain [23].

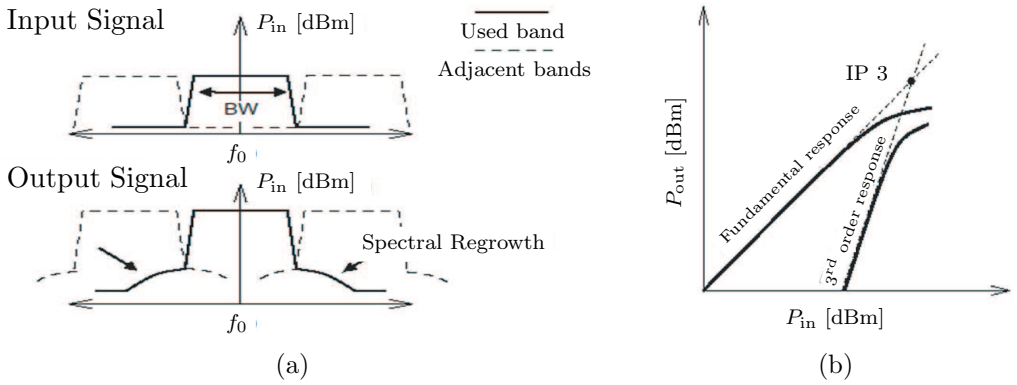


Figure 5.13: Spectral regrowth as a frequency-domain effect due to non-linearities, leading to output power reduction and a decrease of bandwidth capacity due to necessary safety margins [23] (a), illustration of the definition of the third order intercept as a measure for linearity [23] (b).

A trade-off between gain and output power exists regarding the decision on device size. On the one hand, the output power increases with increasing device size due to the increased maximum drain current. On the other hand, the gain decreases with increasing device size due to the following reasons. Firstly, parasitics, gate resistance and source inductance, become larger. Secondly, phase errors are not negligible in large devices, since the geometry of the active area is not insignificantly small compared to the wavelength of the signal propagating through it. Thirdly, in a large device with multiple gate fingers, the thermal impedance is higher than in a device with only one finger due to the mutual heating between adjacent channels.

Power-Added Efficiency In modern communications and radar applications, the RF power amplifier may be the subsystem which consumes the biggest share of DC power, Chalermwisutkul [23] states that in a typical UMTS base station, about 47 % of the power consumption is due to power amplifiers. Thus, the efficiency of DC to RF power conversion is an important issue. This becomes even more evident if mobile or satellite communications are considered where generation and/or storage of electrical energy is a limiting issue. A further advantage of an efficient conversion from DC-power to a high frequency signal is a the minimized heating of the amplifier. Thus, the cooling system of the power amplifier can be designed in a simple, small, and cost-efficient way.

For an amplifying device at low frequencies, high levels of power gain can be observed. Thus, the direct contribution of the RF input signal to the RF output power level can be neglected. In this case, the drain efficiency defined as $\eta = P_{\text{out}}^{\text{RF}}/P^{\text{DC}}$ is a sufficient measure [23], where P^{DC} includes the power associated with all the bias lines of the amplifier. The theoretical drain efficiency of an ideal class A amplifier is 50 %, and the feasible value is between 30 % and 40 % [23].

But under RF conditions, the power gain is relatively low, and $P_{\text{in}}^{\text{RF}}$ contributes to $P_{\text{out}}^{\text{RF}}$

significantly. This can yield $\eta \geq 1$, which shows that η apparently is not a meaningful measure for energy conversion efficiency at high frequencies. Therefore, the power-added efficiency (η_{PAE}) is defined as the ratio of the "added" RF power ($P_{\mathrm{out}}^{\mathrm{RF}} - P_{\mathrm{in}}^{\mathrm{RF}}$) to P^{DC}. Lucyszyn [85] interprets the η_{PAE} as "the efficiency of the network to convert the input DC power into the amount of the output RF power that is left over after the direct contribution from the input RF power has been removed.":

$$\eta_{\mathrm{PAE}} = \frac{P_{\mathrm{out}}^{\mathrm{RF}} - P_{\mathrm{in}}^{\mathrm{RF}}}{P^{\mathrm{DC}}}. \tag{5.29}$$

and can also be expressed in terms of the drain efficiency and the *Gain*:

$$\eta_{\mathrm{PAE}} = \eta \cdot \left(1 - \frac{1}{Gain}\right). \tag{5.30}$$

In general, the efficiency depends on many parameters as frequency, temperature, input drive level, load impedance, bias point, device geometry, and intrinsic device characteristics. And one last aspect to mention in the context of η_{PAE}, amplifier circuits will always have a lower η_{PAE} than transistor devices because matching networks and ensuring stability will always reduce efficiency.

Impact of a dielectric layer on the output power

Chalermwisutkul [23] stated in 2007, that the introduction of a SiO_2-insulation layer will not only reduce the gate leakage current, but the power gain, the saturated output power, linearity and stability are all improved compared to a normal HFET.

The simple expression 5.27 implies, that an increase of $I_{\mathrm{d,max}}$ and V_{break} and a decrease of V_{knee} increases P_{out}. The most important factor to increase I_{d} in the actual context is the increase of sheet carrier concentration (n_{s}), which is given if a dielectric material with passivating effect is chosen for a MISHFET. The knee voltage decreases with lower source and drain resistances, a factor which can be also influenced by a passivating dielectric layer. A third impact a passivating dielectric layer may have is due to a mitigation of the DC/RF-dispersion. Refer to section 5.3 for further details on passivation, knee voltage shift and DC/RF-dispersion.

Impact of a dielectric layer on the gain

In the context of this work, the dependence of the *Gain* on the input resistance is of particular interest. To explain the effect of an increased input resistance on the *Gain* qualitatively, consider the following model: Assuming devices with identical and constant g_{m} for $V_{\mathrm{th}} < V_{\mathrm{gs}} < 0\,\mathrm{V}$ and constant input resistances $R_{\mathrm{input,1}}$ and $R_{\mathrm{input,2}}$. The load line of the devices is determined by external circuitry and is assumed identical and constant as well. Furthermore it is assumed, that the RF power levels $P_{\mathrm{in}}^{\mathrm{RF}}$ and $P_{\mathrm{out}}^{\mathrm{RF}}$ are respectively proportional to the DC figures $(\Delta V_{\mathrm{gs}})^2/R_{\mathrm{input}}$ and $\Delta I_{\mathrm{d}} \cdot \Delta V_{\mathrm{ds}}$ (note, that in this model the fact is neglected, that the input voltage is also determined by the input capacitance).

If a signal with $P_{\mathrm{in},1}^{\mathrm{RF}}$ is applied to the input of a (conventional) device, then the potential difference at the input will vary in a certain range of $\Delta V_{\mathrm{gs},1}$. At the output, a current in the range $\Delta I_{\mathrm{d},1}$ will arise following $I_{\mathrm{d}} = g_{\mathrm{m}} \cdot V_{\mathrm{gs}}$. Since the load line is fixed, $\Delta I_{\mathrm{d},1}$ will correspond with a voltage drop at the output of $\Delta V_{\mathrm{ds},1} = m \cdot \Delta I_{\mathrm{d},1}$, where m is the load resistance. Thus, $P_{\mathrm{out},1}^{\mathrm{RF}}$ is determined.

Now, if $R_{\mathrm{input},2}$ is assumed to be higher than $R_{\mathrm{input},1}$, then the same input power $P_{\mathrm{in},2}^{\mathrm{RF}} = P_{\mathrm{in},1}^{\mathrm{RF}}$ will correspond to a higher $\Delta V_{\mathrm{gs},2}$. This will yield a higher $\Delta I_{\mathrm{d},2}$ under the assumption that g_{m} is constant for both devices (note, that if HFET and MISHFET were to be compared, g_{m} would differ. But in this case the difference would be overcompensated by the difference between $\Delta V_{\mathrm{gs},1}$ and $\Delta V_{\mathrm{gs},2}$ due to the highly different input resistances). Furthermore, since the load line is assumed identical, $\Delta V_{\mathrm{ds},2}$ increases as well. Thus, by increasing R_{input} a higher output power will result for an unchanged $P_{\mathrm{in}}^{\mathrm{RF}}$. In other words, an increase in input resistance - as is the case for MISHFETs - corresponds with a higher *Gain*. Figure 5.14 illustrates the proposed model.

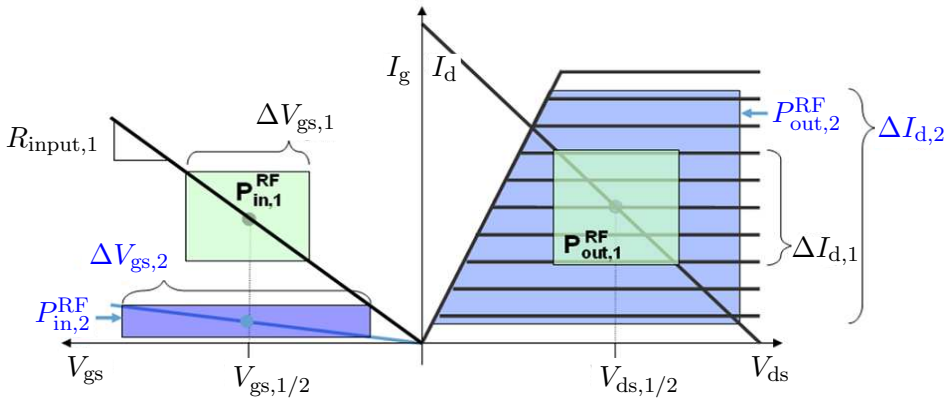


Figure 5.14: Impact of a dielectric layer on the gain.

Impact of a dielectric layer on the power added efficiency

According to equation 5.30, the η_{PAE} increases with increasing η and *Gain*. As has been shown above, the introduction of a dielectric layer has beneficial impact on the *Gain*, and due to the reduction of the input currents, P^{DC} reduces, thus η increases. Therefore it can be concluded that the η_{PAE} is increased for a MISHFET compared to a HFET.

Part III

Experiments, Results, and Discussion

In the previous part of this work, the fundamentals have been introduced that form the theoretical basis to conduct and discuss experiments with GaN/AlGaN-based HFETs incorporating dielectric layers to insulate the gate. This part will cover the experiments themselves that aim at improving the conventional HFETs utilizing novel high-κ materials.

The first experiments performed at the IBN in the field of GaN-based MISHFETs aimed at fabricating and characterizing MISHFETs utilizing a SiO_2 layer as the gate dielectric. This way an appropriate MISHFET-technology was established at the IBN on the one hand, on the other hand results to serve as a benchmark for further experiments with high-κ-based MISHFETs were gathered. The first experiment with SiO_2-MISHFETs - treated in section 6.1 - was designed as a comparative study to investigate the role of passivation for the performance of MISHFETs.

Despite the convincing attributes of SiO_2 as a gate dielectric, a severe disadvantage was the loss of channel control due to the rather thick SiO_2 layer. Therefore, the task was to recover the channel control. One way to achieve this goal was to use a smaller SiO_2 layer thickness, as described in section 6.2.

An alternative way to increase the channel control was to make use of high-κ material. This way, the oxide thickness can be chosen far above the technological limits, and thus insulating properties can be improved on the one hand, on the other hand, capacitance comparable to the capacitance of thin SiO_2 layers can be reached due to the high dielectric constants.

The results of the first attempts to achieve electrically dense $GdScO_3$ material to insulate the gate electrode are presented in chapter 7. The chapter comprises an exemplary experiment, which stands for the approach to vary the annealing temperature, and the key experiment, dealing with post-deposition annealing in oxygen atmosphere.

Chapter 8 covers the first experiment with $GdScO_3$ heterostructure diodes. The insulating and dielectric properties of the diodes are discussed, issues related to electronic states within the oxide film are investigated, and the effect of the insulating layer on the 2DEG properties are examined.

Encouraged by the results achieved with $GdScO_3$ heterostructure diodes, the more complex MISHFETs were fabricated utilizing $GdScO_3$ for the dielectric layer. Chapter 9 treats this major experiment utilizing SiC substrates in detail.

To examine high-k materials other than $GdScO_3$, MISHFETs were also fabricated with HfO_2 as the insulating layer. Chapter 10 summarizes the experiment performed. To conclude the experimental part, a thorough comparison of the results achieved in the experiments is presented in chapter 11 and the major findings are summarized in chapter 12.

Chapter 6

Silicon Dioxide Transistors

6.1 Passivation and Insulation

This chapter treats the first experiments with MISHFETs performed at the IBN utilizing a SiO_2 layer as the gate dielectric. During this experiment, an appropriate MISHFET-technology was established at the IBN on the one hand, on the other hand the results were planned to serve as a benchmark for further experiments with high-κ-based MISHFETs.

The experiment was designed as a comparative study to investigate the role of passivation for the performance of MISHFETs. In recent publications it was shown that MIS structures are suitable to decrease the gate leakage current significantly [69, 14, 25, 1]. Another approach, namely the passivation of free semiconducting surfaces by means of oxide and nitride layers, can be applied to suppress the gate current as well [44, 11]. Both approaches show a vast similarity in technological respect. On the one hand, passivation of HFETs involves covering the free semiconductor surface of the device with a thin insulating layer. For Metal-Insulator-Semiconductor HFETs (MISHFET) on the other hand, a layer of insulating material is not only deposited onto the free semiconducting surface but also underneath the metallic gate electrode.

As pointed out in chapter 5, surface- and interface states have a significant influence on the behavior of GaN/AlGaN-based devices. In this experiment, we aim at comparing both the gate insulation and the passivation approach with respect to DC, RF and power performance. In particular, we try to distinguish the impact of passivation effects on the MISHFET behavior from effects that are due to the insulation of the gate.

Experiment

To investigate the contributions of the passivation of the free and the gated surfaces, conventional and passivated HFETs and MISHFETs were processed. In addition, heterostructure diodes (HDiode), van der Pauw, and TLM patterns were fabricated simultaneously. The material structure of all devices consisted of 3 μm GaN- and 30 nm $Al_{0.28}Ga_{0.72}N$ layers that have been grown on semi-insulating $4H-$SiC substrate by

LP – MOCVD. The processing involved the fabrication of Ti/Al/Ni/Au ohmic and Ni/Au Schottky contacts and is documented in detail in appendix A.3.

The transistors had a gate length (L_g) between 0.3 μm and 2 μm, and the gate width was either 100 μm or 200 μm. A two finger design was chosen. The source drain spacing ranged from 2 μm to 4 μm. The areas of the square diodes were between $0.625 \cdot 10^{-9}$ m^2 and $40 \cdot 10^{-9}$ m^2, the electrode spacing was 5 μm. Van der Pauw patterns had an active area of $(0.3\,\mathrm{mm})^2$.

A SiO_2 layer of nominally 10 nm thickness was deposited by PECVD to fabricate the passivated devices. Refer to appendix A.1 for details of SiO_2 deposition. To prepare the MIS devices, the same oxide thickness and deposition technology was chosen. The deposited SiO_2 was not treated any further. Figure 6.1 illustrates the three fabricated device types.

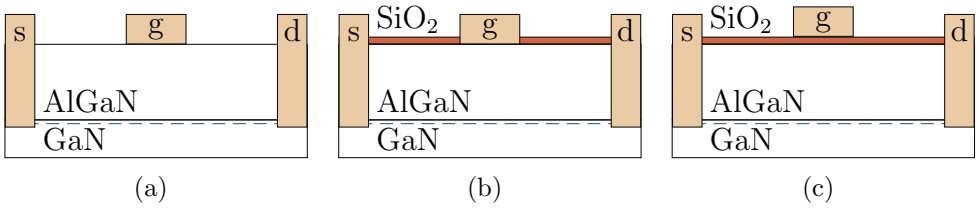


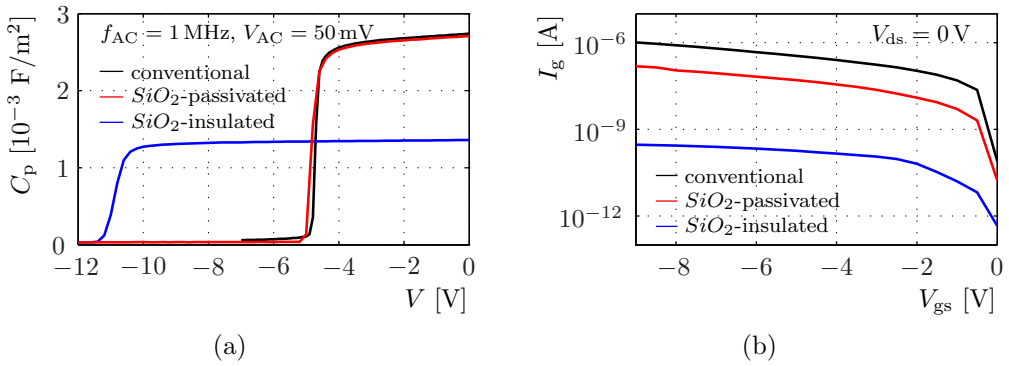
Figure 6.1: Structure of the conventional HFET (a), the SiO_2-passivated HFET (b), and the SiO_2-MISHFET (c).

To characterize the devices, IV, CV, DC, S-parameter, Load-Pull, and Hall measurements were performed, as described in appendix B.

Results and Discussion

Input Characteristic By means of CV measurements according to appendix B.2, the gate source capacitance (C_{gs}) and the threshold voltage (V_{th}) of an unpassivated HDiode was measured to be 2.7 mF/m^2 and -4.8 V, respectively. The C_{gs} value and V_{th} values for the passivated structure differed negligibly. For the MISHDiode, C_{gs} was half the corresponding value of the unpassivated structures and V_{th} was found to be -10.8 V. Figure 6.2(a) illustrates the CV-measurement results for the three device types.

According to the definition given by equation 5.1, the nearly identical C_{gs} values measured for the unpassivated and the passivated HFET can be interpreted such that both device types possess nearly identical abilities to control the properties of the channel - which is not surprising, since the surface passivation does not impact the layer stack underneath the gate. But the fact of nearly identical channel control abilities in combination with the almost identical V_{th} values measured for both device types, means in conclusion that the initial sheet carrier concentration in the active region of the device is identical as well. That is a clear indication that a free surface passivation does not



(a) (b)

Figure 6.2: Input characteristic of SiO_2-passivated, SiO_2-insulated, and conventional devices. The capacitance (C_p) vs. bias (V) plot shows the influence of passivation and insulation on the channel control capability (a), and the gate current (I_g) vs. gate source bias (V_{gs}) reveals the current reducing contributions of passivation and insulation (b). For CV measurements a square diode with $(100\,\mu m)^2$ was utilized. A transistor with 700 nm gate length and 200 μm gate width was used for IV measurements.

impact the properties of the 2DEG underneath the gate - without conflicting the possibility that the 2DEG region underneath the passivated surface itself might be changed due to passivation effects.

The situation for the MISHFET is different. Here, the C_{gs} value is significantly reduced, which is in accordance with the model suggested in section 5.1, assuming that the SiO_2 layer underneath the gate electrode and the AlGaN depletion region form a series of capacitances. From the measured C_{gs} values for the HFET and the MISHFET and knowing the AlGaN-layer thickness, an effective insulator thickness (d_{CV}^{insul}) of 12.8 nm can be calculated for the MISHFET structure. Apparently, the suggested model is suitable even for quantitative considerations, as the deviation of d_{CV}^{insul} from the nominal thickness of 10 nm is acceptably low. In the following, i.e. for the further discussion of the actual experiment and also for all the following experiments of this thesis, the insulator thickness calculated from the CV measurement results will be used for the interpretation of results, referred to as the effective thickness.

Since the reduction of C_{gs} is equivalent with a reduced ability to deplete the 2DEG channel with a given bias, a much higher V_{gs} is needed to pinch-off the MISHFET device, which is well reflected by the more than doubled V_{th} value compared to the HFET case. The fact that the reduction of C_{gs} by 50 % does not exactly correspond a twofold V_{th}-increase can be taken as an indication towards a higher sheet carrier concentration (n_s) in the active region of the device. This explanation is supported by Hall measurements which yielded a 30 % increase for n_s for Hall-patterns with a MIS-structure compared to conventional Hall-patterns. Bringing together the knowledge gained from the results of the passivated HFET and the MISHFET one can conclude, that an increase of n_s due to passivation effects in the active region of the device can only be reached, if the semiconducting surface underneath the gate is coated with a dielectric material -

passivation of the free surfaces is not sufficient in this context.

To characterize the current-related aspect of the input characteristic, the gate current of HFETs and MISHFETs with $L_g = 700\,\text{nm}$ and $W_g = 200\,\mu\text{m}$ were measured according to the methods outlined in appendix B.1. For unpassivated HFETs, a gate leakage current (I_g) in the range of $1\,\mu\text{A}$ was measured. The corresponding value for passivated HFETs was approximately one order of magnitude lower, and for the MISHFET it was around three to four orders of magnitude smaller. Figure 6.2(b) displays the reverse gate current of the three device types.

In section 5.2 it was suggested that both a gate current via the surface and a current via the 2DEG channel contribute to the total gate current. The surface current is due to an electron "hopping" along surface states [138], assuming an electronic state distribution as in [47] (see figure 5.5(b)). The impact of SiO_2 is either due to a "burying" of surface states, such that electrons leaking from the gate can not be trapped, or due to Si-atoms replacing the donor-like states during the passivation process [142]. For the passivated HFET, the reduction of I_g can only be associated with the passivation of the semiconductor surface, since the conditions underneath the gate electrode is unchanged. Thus, SiO_2-passivation of the surface limits the gate current by one order of magnitude.

For the MISHFET, the observed gate leakage reduction is significantly higher than for the passivated HFET. Since the free semiconducting surfaces were coated with SiO_2 the same way as for the passivated device it is reasonable to assume, that one order of magnitude of the total current reduction is also due to the limitation of surface currents. The remaining reduction of two to three orders of magnitude can be associated with the substitution of the Schottky barrier by a more effective MIS structure [69]. Therefore it can be concluded, that the current path through the Schottky barrier, the AlGaN layer, and the 2DEG is the major contributor to the total gate current, and that the MIS-concept offers an effective approach to limit not only this major current contribution but also to reach an additional current-reducing effect by free surface passivation.

Output Characteristic To characterize the output characteristic of the devices, standard DC measurement methods as described in appendix B.1 were utilized. Applying a gate source voltage (V_{gs}) of 1 V, a maximum drain current ($I_{d,max}$) of $0.66\,\text{A/mm}$ was measured for the unpassivated HFET. For the passivated HFET and the MISHFET, the $I_{d,max}$ values were 40 % and 80 % higher, respectively. The output characteristics are illustrated in figure 6.3.

To further analyze the output characteristics, consider the plots in figure 6.4, where the calculated transconductance (g_m) and the conductance (g_d) of the different device types are illustrated. According to the data plotted in figure 6.4(a), the conventional HFET has a maximum transconductance ($g_{m,max}$) of $142\,\text{mS/mm}$ and pinches off at $-4.8\,\text{V}$. The passivated HFET shows a 31 % higher $g_{m,max}$-value, the V_{th}-value is identical to that of the reference device. The MISHFET shows a threshold voltage 2.4 times as high as the reference device, its mean g_m-value in the on-state was 33 % lower than that of the reference.

Following figure 6.4(b), the maximum conductance ($g_{d,max}$) of the unpassivated device

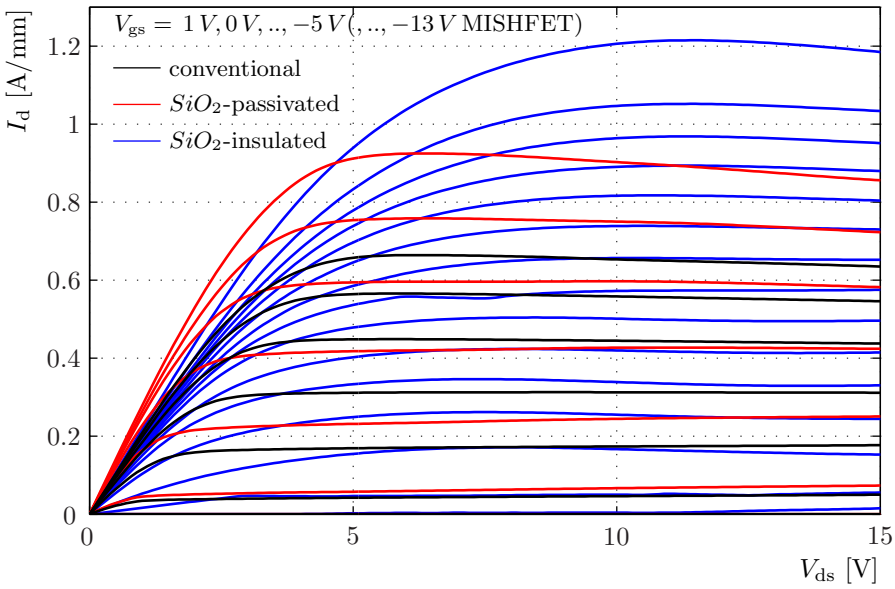


Figure 6.3: Output characteristic of a conventional HFET, a SiO_2-passivated HFET, and a SiO_2 MISHFET. The drain current (I_d) vs. drain source bias (V_{ds}) plot characterizes the DC output of a transistor in dependence on the gate source voltage (V_{gs}) applied to the input. A transistor with 700 nm gate length and 200 μm gate width was used.

was 200 mS/mm and the knee voltage ($V_{ds,sat}$) was 7 V. For the passivated device, $g_{d,max}$ was 35 % higher and $V_{ds,sat}$ identical to that of the reference. For the MISHFET, $V_{ds,sat}$ was 57 % higher, but $g_{d,max}$ was nearly identical compared to the unpassivated HFET.

The measurement results will be interpreted in the following, starting out with the passivated HFET. As was already concluded from the CV measurement results, the passivation of the free semiconductor surface does not directly impact the properties of the 2DEG in the active region of the device. Consequently, the observed increase in $I_{d,max}$ for the passivated HFET has to be induced by other factors than a change of the $n_s \cdot \mu$-factor in the 2DEG underneath the gate. One explanation for the $I_{d,max}$-increase is, that the passivation of the free surfaces has caused the $n_s \cdot \mu$-product to rise and thus the source resistance (R_s) to reduce significantly. According to section 5.3, a reduced R_s would result in an increased I_d current and a higher $g_{d,max}$ (compare figure 5.8(a))- which both is the case. The same argument of a reduced R_s explains the difference between the $g_{m,max}$-values of the passivated and the unpassivated devices: According to section 5.3, a reduced R_s has a $g_{m,max}$-reducing effect (compare figure 5.8(b)).

Drawing the attention to the MISHFET, the explanation of the measured output characteristic is different to that of the passivated HFET. From CV and Hall measurements it was already concluded, that the coating of the semiconductor surface underneath the gate causes the sheet carrier concentration (n_s) of the active region of the device to rise significantly. The n_s increase in the active region due to passivation is likely the main reason for the drastic increase of $I_{d,max}$. To explain the significant shift in $V_{ds,sat}$, it is again referred to section 5.3, where it was shown that a decrease in C_{gs} with

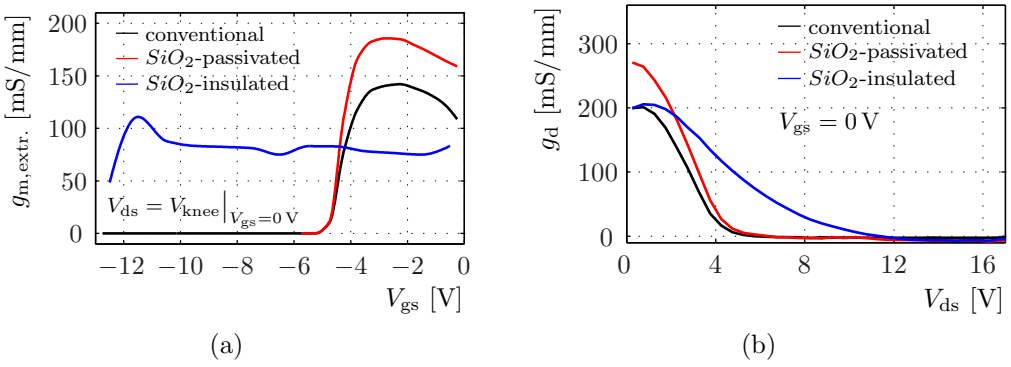


Figure 6.4: Transconductance (g_m) (a) and output conductance (g_d) (b) of a conventional HFET, a SiO_2-passivated HFET, and a MISHFET with SiO_2 insulation.

accompanying increase in V_{th} increases $I_{d,sat}$ slightly and shifts $V_{ds,sat}$ significantly (compare figure 5.9(a)). The difference in $g_{m,max}$ between the conventional HFET and the MISHFET can be explained mainly by the significantly higher I_d-values reached for the MISHFET, the non-linear dependence of g_m from C_{gs} and V_{th} as discussed in section 5.3 should be of minor importance in this case. It remains to be noted, that the R_s/R_d-decreasing passivation effect discussed in the context of the passivated device should also be effective for the MISHFET. But contrary to the expectation, the experiment showed nearly identical $g_{d,max}$-values for the conventional HFET and the MISHFET. It remains to be clarified, whether the R_s/R_d-decreasing effect was compensated by other impacts, or if it was not existing for the MISHFET.

In Summary it can be stated, that the passivation of the semiconductor surface underneath the gate electrode can yield a tremendous positive effect on I_d, although the accompanying increase of V_{th} and the decrease of C_{gs} shifts $V_{ds,sat}$ significantly.

Breakdown Measurements So far, the HFET and MISHFET devices were characterized under moderate operational conditions. For instance, DC measurements were conducted up to $V_{ds} = 20\,V$ at maximum. But due to the wide band gap of Gallium Nitride, GaN-based transistors should be able to be operated at much higher voltages. To give a rough indication whether the SiO_2-insulated devices can compete with conventional devices, breakdown measurements were conducted as described in section B.1.

For the conventional HFET, off-state breakdown voltages (V_{break}^{off}) were measured up to 70 V, for the passivated HFET the best result achieved was around 40 V, and measurements with MISHFETs yielded V_{break}^{off}-values of 25 V at best. Figure 6.5 plots the results gained from breakdown measurements.

The measurement results for the conventional HFETs are in good accordance to results achieved with HFETs fabricated at the IBN in recent years (Al_2O_3 substrates, comparable GaN/AlGaN structure and geometry [59]) and to values predicted by literature, assuming a defect charge density of $4 \cdot 10^{12}$ cm^{-2} [121] (compare figure 5.5(a)). This is

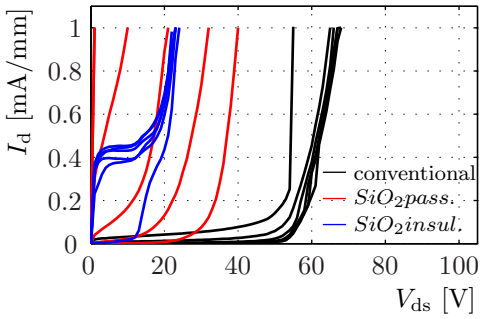
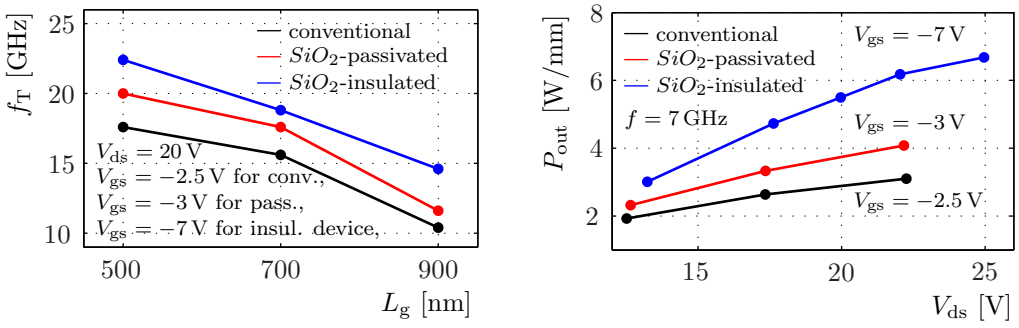


Figure 6.5: Off-state breakdown voltage (V_{break}^{off}) of a conventional HFET, a SiO_2-passivated HFET, and a MISHFET with SiO_2 insulation.

even more true since the HFETs were not optimized for high-voltage operation, e.g. by applying the field plate technology.

The remarkable fact about this measurement series is, that the results for the devices incorporating SiO_2 were so much behind the conventional HFET. The experiences gained from other measurements, e.g. the (surface-) gate current reducing effect of the SiO_2-coating of the surface, legitimated the expectation, that the SiO_2-devices should outperform the conventional HFET by far.

S-Parameter Measurements To study the RF behavior of the transistor devices, S-parameter measurements were performed. Considering a particular L_g of 500 nm, the cutoff frequency (f_T) for unpassivated HFETs was determined to be 17.6 GHz. For passivated HFETs and for MISHFETs, f_T was 14 % and 27 % higher, respectively. For results gained from transistors with various gate lengths and for further details on the operational conditions refer to figure 6.6(a).



(a) cutoff frequency vs. gate length

(b) output power vs drain source bias

Figure 6.6: Small (a) and large signal characteristic (b) of a conventional, a SiO_2-passivated, and a SiO_2-insulated transistor.

From the discussion concerning the impact of a dielectric layer on the RF small signal properties in section 5.4 it is known, that a prediction whether the RF-figures of a

MISHFET are superior to those of a conventional HFET is not feasible. Nevertheless, the model can give an explanation for empirical results by discussing the impact of the dielectric layer on carrier-mobility (μ), threshold voltage (V_{th}), gate-drain capacitance (C_{gd}), and resistive parasitics (as R_{d} and R_{s}).

The fact that both passivated HFET and MISHFET show higher f_{T}-values than the conventional HFET can be explained by lower resistive parasitics due to a passivation of the access regions. This is in accordance to the conclusions made previously in the context of the DC measurements. Apparently, the resistance-reducing effect is stronger than the disadvantageous effect of the C_{gd}-increase, which needs to be assumed for both device types. The fact that the MISHFET shows even better f_{T}-values than the passivated device can be explained by a beneficial effect of the high V_{th}-value on the one hand, on the other hand it might be due to the passivation of the semiconductor underneath the gate which improves the carrier-mobility.

Load-Pull Measurements Large-signal power measurements were performed at a frequency of 7 GHz, and a V_{gs} of -2.5 V and -7 V for HFETs and MISHFETs, respectively. For a drain source voltage (V_{ds}) of 22 V, the output power (P_{out}) of 3.1 W/mm for the unpassivated HFETs increased to 4.1 W/mm for passivated HFETs. A P_{out} value of 6.2 W/mm was measured for MISHFETs as illustrated in figure 6.6(b).

The increase in P_{out} for the passivated HFET can be explained as follows: On the one hand it is caused by the already discussed increase of $I_{\mathrm{d,max}}$ due to passivation. On the other hand, it is likely caused by the mitigation of the virtual gate effect, thus reducing the DC/RF dispersion phenomenon. Again, these explanations can be applied for the MISHFET as well. But in addition, a passivation effect underneath the gate results in a higher n_{s} in the active region of the device, enabling a higher drain current. Thus, P_{out} reaches even higher values than in the case of passivated HFETs.

Summary

This study demonstrated the superiority of MISHFETs compared to unpassivated and passivated HFETs with regard to DC, RF, and power performance. We argue, that the behavior of MISHFETs was not only governed by the gate current reducing effect of the insulated gate but also by passivation effects, that have a beneficial influence on the DC, RF, and power performance. Due to the additional SiO_2 coating of the AlGaN surface underneath the gate electrode, the total passivation effect for MISHFETs was even stronger than the effect of conventionally passivated HFETs.

Considering the performance increase of a SiO_2 MISHFET relative to the HFET, the following can be stated in summary: The gate leakage current was three orders of magnitude lower, the maximum drain current increased by around 80 %, and the output power nearly doubled. Despite the encouraging findings, the MISHFETs suffered from a loss of channel control, i.e. the gate source voltage needed to be more than doubled to pinch of the device. Furthermore, the surface treatment significantly reduced the off-state breakdown voltage.

6.2 Silicon Dioxide Insulator Thickness

The previous section 6.1 presented successfully fabricated SiO_2 MISHFETs and the role of passivation was distinguished from the role the gate insulation plays for the performance of a MISHFET. It turned out that the SiO_2 dielectric was favorable with respect to many device properties. But the major drawback was the significant loss in channel control.

One attempt to overcome this obstacle is to reduce the oxide layer thickness and thus to improve the channel control capabilities, i.e. to increase the absolute threshold voltage to pinch of the device, to increase the capacitance, and to improve the transconductance. In this section, the consequences of reducing the SiO_2 layer of a MISHFET to a few nanometer thickness will be investigated.

Experiment

Since the actual experiment aimed at optimizing the MIS devices that were processed successfully in the previous experiment, the parameters regarding device types, processing, and geometry remained the same as in section 6.1. The material structure was different though, all devices consisted of 20 nm $Al_{0.28}Ga_{0.72}N$ layer and a 3 nm GaN cap layer that have been grown on semi-insulating $4H-$SiC substrate. The processing involved the fabrication of Ti/Al/Ni/Au ohmic and Ni/Au Schottky contacts and is documented in detail in appendix A.3.

The transistors had a gate length (L_g) between 0.3 μm and 2 μm, and the gate width was either 100 μm or 200 μm. A two finger design was chosen. The source drain spacing ranged from 2 μm to 4 μm. The areas of the square diodes were between $0.625 \cdot 10^{-9}$ m^2 and $40 \cdot 10^{-9}$ m^2, the electrode spacing was 5 μm. Van der Pauw patterns had an active area of $(0.3\,\mathrm{mm})^2$.

For the MIS devices, plasma-enhanced chemical-vapor-deposition (PECVD) technology was utilized to deposit SiO_2 layers as was discussed in appendix A.1. The nominal thicknesses of the insulating layers ($d^{\mathrm{insul}}_{\mathrm{PECVD}}$) were 3 nm and 6 nm.

To characterize the devices, the standard characterization routine was performed, including current-voltage (IV), capacitance-voltage (CV), standard output characterization (DC), S-parameter, and Load-Pull measurements as described in section B.

Results and Discussion

Input Characteristic CV measurements were performed with heterostructure diodes. The capacitance (C_p) of the conventional diode was 3.7 mF/m^2. Taking the conventional device as a reference, the C_p values of the MISHDiodes were 20 % and 40 % less for oxide thicknesses of 3 nm and 6 nm, respectively. In terms of threshold voltage (V_{th}), a value of -3.6 V was identified for the conventional device, 14 % and 72 % higher absolute values were found for the 3 nm and 6 nm SiO_2 devices, respectively. The CV paths showed the

typical capacitance drop as depicted in figure 6.7(a).

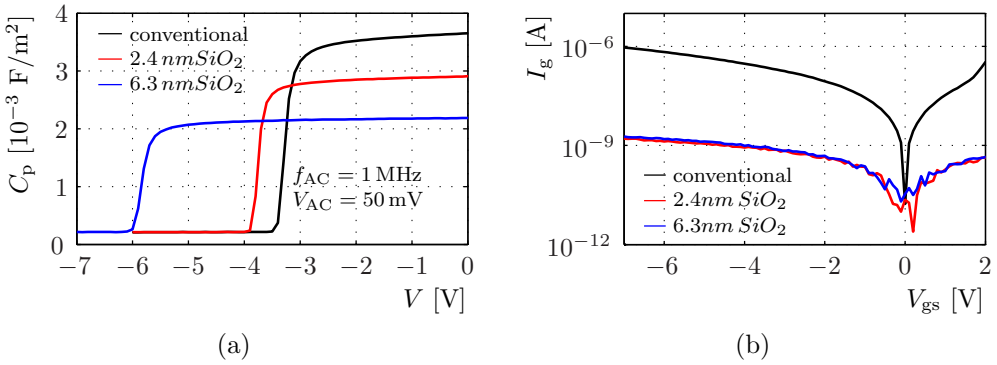


Figure 6.7: Input characteristic of MISHFETs with varying SiO_2 thickness: Gate-source capacitance (C_p) versus applied bias (V) (a) and gate current (I_g) versus gate-source voltage (V_{gs}) (b).

According to equation 5.5 and assuming a dielectric constant of 3.9 for SiO_2, the CV results reveal that the effective thicknesses (d_{CV}^{insul}) of the SiO_2 layers deviate slightly from the nominal values (d_{PECVD}^{insul}), i.e. 2.4 nm instead of 3 nm and 6.3 nm instead of 6 nm, respectively. The results show, that the model suggested in section 5.1 is very well applicable. In the following, the d_{CV}^{insul}-values extracted from CV measurements will be used.

To explain the different V_{th}-values the model presented in section 5.1 can be used: the thicker the oxide film, the higher the voltage that drops across the oxide, and thus the voltage which effectively lifts the potential well above the fermi energy level is reduced accordingly. Therefore, the thicker the insulator film, the higher the voltage that needs to be applied to pinch-off the device.

The sheet carrier concentrations were computed from the CV measurement results according to equation 5.2: For the conventional device, n_s was $1.08 \cdot 10^{13}$ cm^2. For the device with 3 nm thick SiO_2 layer the value was 2 % less, the device with the thicker dielectric layer showed a 10 % higher value. In combination with the results from the previous section, where a n_s increase of 15 % for a 12.8 nm SiO_2 layer was observed, it it can be concluded, that the passivated effect of the SiO_2 grows stronger with the increase of oxide thickness.

To investigate the insulating properties of the oxide layers, the gate currents were measured by means of a low-current measurement setup (see appendix B.1). The maximum reverse gate current (I_{max}^{rev}) of the conventional HFET was 0.94 μA at $V_{gs} = -7$ V. For both MISHFETs, I_{max}^{rev} was around 2.7 orders of magnitude smaller with the same bias being applied as in the conventional case. The maximum forward gate current (I_{max}^{forw}) was 0.33 μA at a V_{gs} of 2 V for the conventional device. For the two MIS devices, the current was 2.9 orders of magnitude lower. Both SiO_2 devices showed a smooth and regular IV path with MIS characteristic as illustrated in figure 6.7(b).

The results imply, that the insulation property of SiO_2 for negative biases as well as for

positive voltages is independent on the layer thickness. But considering the fact that the SiO_2 layers were deposited by non-optimized PECVD-technology, uncertainties remain whether the films were sufficiently homogeneous and the device-to-device variation were sufficiently low. Therefore, the finding should not be overrated. Nevertheless, in combination with the results gained from the previous experiment, where a reverse current reduction of 3.5 orders of magnitude was achieved with a 12.8 nm thick SiO_2-layer, the general conclusion is legitimate that the resistivity of the SiO_2 film increases with its thickness.

Output Characteristic DC measurements were performed to study the impact of the varying SiO_2 layer thickness on the output characteristics of the MISHFETs. For the conventional HFET, the maximum drain current ($I_{d,max}$) obtained at $V_{gs} = 1\,V$ was 0.71 A/mm. The drain current of the 2.4 nm SiO_2 MISHFET had an identical peak value as the reference device. The device with the 6.3 nm SiO_2 layer showed a $I_{d,max}$ which was 8 % higher than the reference value. The output characteristics is presented in figure 6.8.

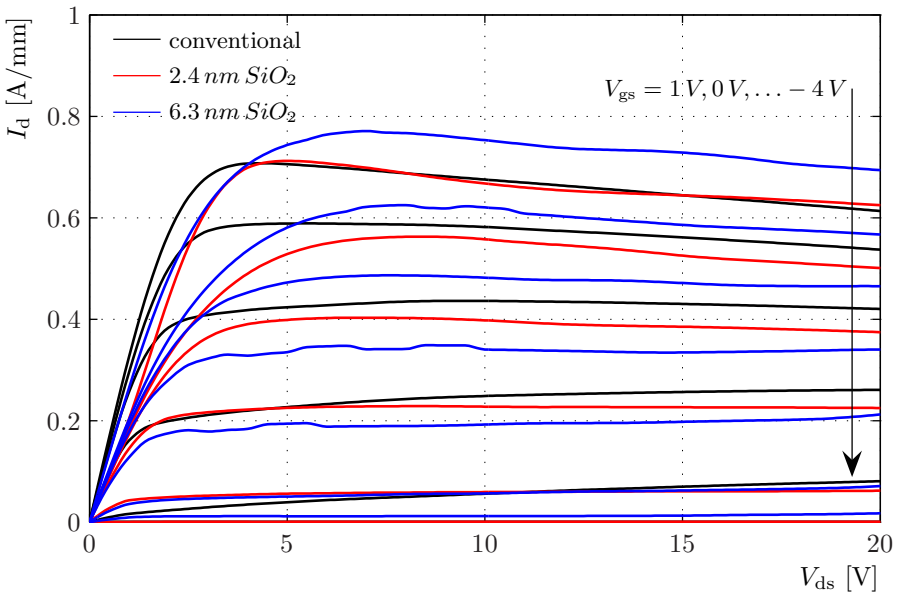


Figure 6.8: Output characteristic of MISHFETs with varying SiO_2 thickness.

From the measured I_d-values the transconductance (g_m) and the output conductance (g_d) were calculated. The maximum g_m ($g_{m,max}$) was 200.9 mS/mm for the HFET. For the MISHFETs, $g_{m,max}$ was 10 % and 24 % lower than the reference value for the 2.4 nm and the 6.3 nm SiO_2-thickness, respectively. For the conventional device, a threshold voltage (V_{th}) of $-4\,V$ was found, the corresponding absolute value of the 2.4 nm device was 7.5 % and that of the thicker layer device V_{th} was 67.5 % higher. In figure 6.9(a) g_m is depicted as a function of V_{gs}.

The maximum output conductance ($g_{d,max}$) of the conventional HFET was 315 mS/mm

and the zero-crossing of g_d , i.e. the knee voltage ($V_{ds,sat}$), was found at 4.5 V. For the MISHFETs, $g_{d,max}$ was evaluated to be smaller than for the HFET: −38.7 % and −32.6 % for the 2.4 nm and for the 6.3 nm device, respectively. The knee voltages were higher than the reference though, $V_{knee} = 5$ V and 7 V were determined for the 2.4 nm and for the 6.3 nm device, respectively. See figure 6.9(b) for the plot of g_d.

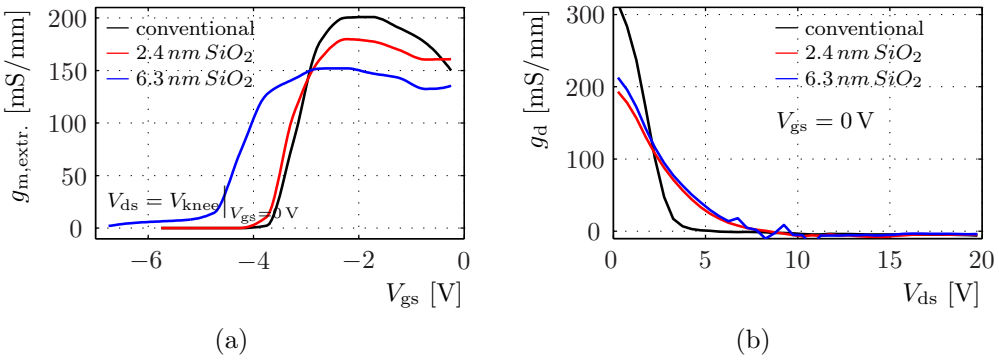


Figure 6.9: Transconductance (g_m) (a) and output conductance (g_d) (b) of SiO_2 MISHFETs with varying insulator thickness.

As was already concluded from CV measurements, the 6.4 nm-thick SiO_2-layer causes an increase in carrier concentration (n_s) of 10 % due to the passivation of the semiconducting surface underneath the gate electrode. This can be seen as the likely cause for the increased $I_{d,max}$-value. On the other hand, the thin SiO_2 layer could not attributed a passivation effects from CV measurements, which corresponds well with the $I_{d,max}$-value nearly identical to the reference value. Obviously, the SiO_2 layer needs to exceed a certain thickness to result in a passivation effect. In the context of the findings from section 6.1 - where a significant I_d increase was achieved with a 12.4 nm SiO_2-layer - the actual results suggest the tendency of increasing drain currents with increasing SiO_2 layer thicknesses.

Drawing the attention towards the output conductance, then it becomes apparent that the $g_{d,max}$-values of both SiO_2 devices were significantly lower than that of the conventional device. This fact can be explained by a higher drain resistance (R_d), but it is not likely to be induced by a increased source resistance (R_s): Assuming identical n_s-values for the conventional and the 2.4 nm-SiO_2 device, then a higher R_s-value would yield - according to figure 5.8(a) - a smaller drain current, which is not the case. The question remains whether the increase of R_d is a result of the SiO_2-coating of the free semiconductor surface. Since a similar effect has not been observed in the previous experiment (section 6.1) and because it does not seem likely, that the free surface passivation solely impacts R_d without affecting R_s, the R_d increase is assumed to be due to processing-imperfections, i.e. a random piece-to-piece variation of the gate-drain distance.

S-Parameter Measurements To characterize the RF small signal characteristics of the devices in question, S-parameter measurements were performed as described in appendix B.3. The cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) were

then calculated for devices with a gate length of 700 nm. The V_{gs}/V_{ds} working points considered for the different device types and the f_T and f_{max} values are listed in table 6.2 (the f_T-results gained from the former experiment is added to the table). Figures 6.10(a) and 6.10(b) illustrate the measured data for f_T and f_{max}, respectively.

device type	SiO_2 thickness	V_{gs}	V_{ds}	f_T	f_{max}
HFET	-	−2 V	20 V	19.5 GHz	36.5 GHz
MISHFET	2.4 nm	−2.5 V	20 V	+18 %	+26 %
MISHFET	6.3 nm	−3 V	20 V	+30 %	+10 %
MISHFET	12.4 nm	−7 V	20 V	+27 %	n.a.

Table 6.1: Working points for the extraction of cut-off frequency (f_T) and frequency of oscillation (f_{max}) of HFET and SiO_2-MISHFETs with $L_g = 700$ nm.

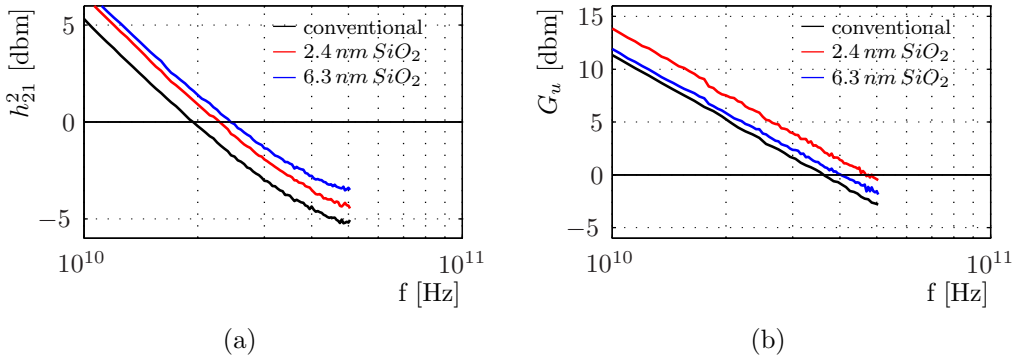


Figure 6.10: Cutoff frequency (f_T) (a) and maximum frequency of oscillation (f_{max}) (b) for conventional HFET and SiO_2 MISHFETs with $L_g = 700$ nm.

As was already observed in the previous experiment, f_T shows improved values for the MISHFETs compared to the conventional device: In section 6.1 is was argued that the improvement is due to a lowering of the resistive parasitics (which over-compensates the disadvantageous effect of an increased C_{gd} due to the additional SiO_2-layer) and due to an increase of the mobility of carriers of the two-dimensional electron gas (2DEG). From the actual measurements a further conclusion can be drawn: Since for the actual devices the resistive parasitics of the SiO_2-devices are higher than for the conventional device (see paragraph "Output Characteristics"), the first reason is not applicable for the actual case. Thus, the main reason for the increased f_T-values should be an improved carrier mobility caused by the passivation of the semiconductor surface of the active region. Furthermore, this effect becomes stronger the thicker the SiO_2-layer is. But this tendency is likely to be limited to certain thickness-intervals, considering the fact that the devices with 6.3 nm and 12.4 nm SiO_2-thickness both yield comparable f_T-improvements.

To explain the superior f_{max} performance of the SiO_2-device with the thin insulation layer, the gate-drain capacitance (C_{gd}) might make the difference. Taking a look at

equation 5.26 it shows, that a decreasing C_{gd}-value increases f_{max}. Since the additional SiO_2-induced capacitance is proportional to the layer thickness, the total C_{gd}-value will be smaller for a thin SiO_2 layer. But although C_{gd} has been identified as a possible reason for the superior f_{max} performance of the 2.4 nm-device, it has to be noted that due to the many f_{max}-influencing parameters the above reasoning needs to be handled with care and must not be overrated.

Load-Pull Measurements To characterize the RF large signal behavior, the output power (P_{out}), gain ($Gain$), and power added efficiency (η_{PAE}) were extracted from Load-Pull measurements. While performing the measurements it showed, that the fabricated devices were still at a premature level - many MISHFETs broke under moderate input power levels and the power sweeps could not be performed such that commonly used figures of merit, e.g. output power at 1 dB compression, could be measured. Nevertheless, for devices with a gate length of 700 nm comparable results were measured and are presented in figure 6.11. The bias conditions were set to $V_{ds} = 20\,V$ and $V_{gs} = -3\,V$, the oscillating frequency was 7.5 GHz. The maximum P_{out} for the conventional HFET was 22.5 dBm. Over the whole P_{in}-range, the P_{out}-values of the SiO_2 MISHFETs were between 2 dB and 2.5 dBm higher. All devices showed similar η_{PAE}-values.

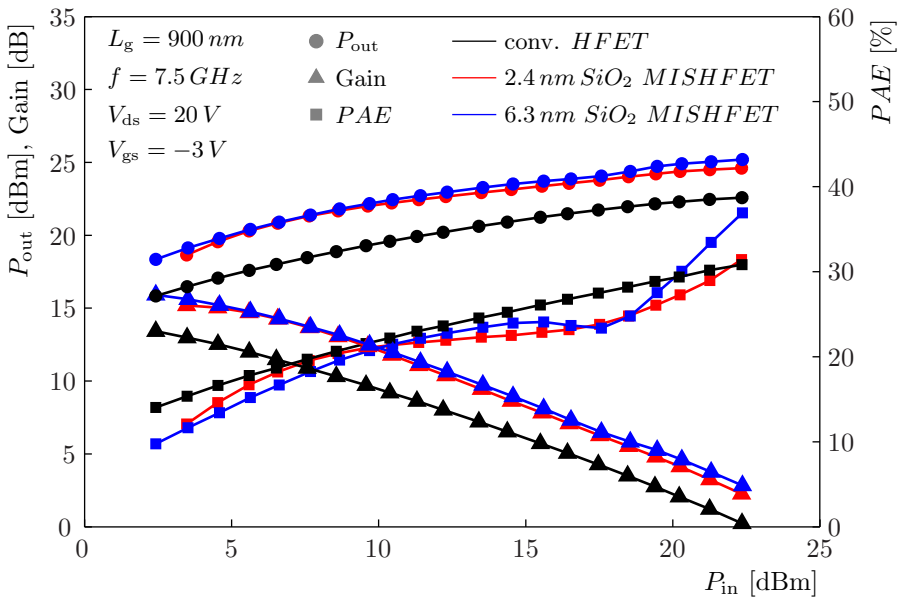


Figure 6.11: RF power performance of MISHFETs with varying SiO_2 thickness relative to a conventional HFET.

Despite the difficulties during measurements, the results give a clear indication that SiO_2-MISHFETs deliver a higher P_{out}-level at a given P_{in} - which is in accordance with results achieved in the previous experiment, where a MISHFET with 12.4 nm thick SiO_2-insulation reached P_{out}-levels twice as good as a conventional HFET. The increase in RF power performance is likely due to the increase in I_d (passivation effects) and the mitigation of the DC/RF-dispersion.

Summary

As expected, scaling down the SiO_2 thickness increased the total capacitance and the absolute V_{th} value, thus the ability to control the 2DEG channel improved. It is interesting to note that a minimum SiO_2 thickness was necessary to yield passivation effects. Below that limit, the SiO_2 gate insulation was even counterproductive regarding the DC performance. The SiO_2 coating of the free surfaces increased the drain and/or source resistances. Nevertheless, the SiO_2 MISHFETs showed superior RF properties compared to the conventional devices. It also showed that the insulation of the gate improved the RF power performance, e.g. P_{out} increased up to 2.7 dB.

6.3 Comparison with Silicon Nitride related Experiments

In the following, the results presented in the previous sections will be compared with experiments with Si_3N_4 devices. The relative dielectric constant (ϵ_r) of Si_3N_4 and SiO_2 is 7 and 3.9, respectively. The band gap (E_g) of Si_3N_4 and SiO_2 is 5.3 eV and 9 eV, respectively. In a rough first order estimate these figures imply that Si_3N_4 offers a better channel control due to a higher gate-source capacitance, but SiO_2 should provide better insulation properties. This section is divided into subsections dealing with passivated and gate-insulated devices.

Passivated Devices

To compare the SiO_2-passivated devices discussed in section 6.1, results from former experiments conducted at the IBN will be utilized because of similar layer structure, device geometry, and fabrication technology: Bérnat et al. fabricated Si_3N_4-passivated GaN/AlGaN heterostructures on SiC substrates with a 150 nm thick passivation layer [19, 18], deposited by PECVD, and Javorka et al. investigated the impact of a 100 nm thick Si_3N_4 passivation layer on the DC and RF performance of GaN/AlGaN HFETs on Si substrates, here the PECVD deposition technology was utilized as well [61, 59].

2DEG Properties For SiO_2-passivated HFETs, as described in detail in section 6.1, a 30 % increase in sheet carrier concentration (n_s) was found for SiO_2-coated Van-der-Pauw patterns relative to conventional patterns. To compare the Hall measurement data of SiO_2-coated devices with those gained from Si_3N_4 devices, the available data concerning n_s, the mobility of sheet carrier (μ), and sheet resistivity (R_s) are listed in table 6.3.

dielectric material	substrate	Δn_s	$\Delta\mu$	ΔR_s	data-source
SiO_2	SiC	+30 %	−12 %	−13 %	section 6.1
Si_3N_4	SiC	+27 %	−14 %	−8 %	[18]
Si_3N_4	SiC	+20 %	−9 %	−9 %	[19]
Si_3N_4	Si	+28 %	−6 %	−17 %	[19, 59]

Table 6.2: Impact of SiO_2- and Si_3N_4-passivation on sheet carrier concentration (n_s), sheet carrier mobility (μ), and sheet resistivity (R_s), extracted from Hall measurement results.

Apparently, the relative differences in n_s, μ, and R_s for SiO_2- and Si_3N_4-coated Van-der-Pauw patterns are of comparable size. Knowing from experience that Hall measurements are commonly accompanied with certain measurement inaccuracies and variation over time, it can be stated that a SiO_2-coating of a free AlGaN surface impacts the 2DEG properties n_s, μ, and R_s nearly the same way.

Threshold Shift As presented in section 6.1, SiO_2-passivation does not cause any shift of the threshold voltage (V_{th}). Deviating from this finding, Bérnat et al. [18] and Javorka et al. [59] reported a 6 % and 12 % shift of the threshold voltage (V_{th}) to more negative values after Si_3N_4-passivation, respectively.

The difference in V_{th} was explained by the authors as a consequence of an increased sheet carrier concentration in the channel underneath the gate electrode. Contrary to this explanation it was concluded in section 6.1, that SiO_2-passivation of the region between Schottky and ohmic contacts does not affect the properties of the 2DEG properties underneath the gate-electrode, since neither the gate-source capacitance nor the threshold voltage has changed.

To the author it seems plausible that the argument used in the context of SiO_2-passivation should be applicable for the Si_3N_4-case as well. In other words, there is not any reason to believe that the Si_3N_4-coating of the free AlGaN surface impacts the pinch-off properties of a HFET with a gate-electrode with a length of some hundreds of nanometers.

To resolve the difficulty consider the definition of threshold voltage, which is the gate-source voltage (V_{gs}) at which the 2DEG channel is pinched-off and the drain current (I_d) practically becomes 0 A. From experimental data, V_{th} can be extracted either from the C_{gs}-V_{gs}-, the g_m-V_{gs}-, or the I_d-V_{gs}-plot. A closer look at the I_d-V_{gs}-plots in [18, 59] reveals, that for the Si_3N_4-passivated and the conventional HFETs the drain current reaches 0 A at nearly the same V_{gs}-value. Thus, the reported V_{th} shifts of 6 % and 12 % appear not to by valid. Therefore, the presented explanation of Si_3N_4 influencing the 2DEG properties underneath the gate is apparently not legitimate.

Gate Current In section 6.1 it was found, that SiO_2-passivation reduces the reverse gate leakage current (I_g) by around one order of magnitude. From former experiments with Si_3N_4 it is known that the gate leakage currents of Si_3N_4-passivated samples either do not differ [59] or differ only slightly [18] from those measured on unpassivated samples.

Thus it can be concluded, that SiO_2 is more appropriate to mitigate the surface current by either "burying" surface states such that electrons leaking from the gate can not be trapped, or due to Si-atoms replacing the donor-like states during the passivation process [142].

DC The experiment described in section 6.1 revealed that the SiO_2-passivated HFET shows a 40 % increase of the maximum drain current ($I_{d,max}$) compared to its conventional counterpart. For Si_3N_4-passivated HFETs, coating of the free surface increases the maximum drain current ($I_{d,max}$) as well. For instance, Si_3N_4-passivated HFETs by Bérnat et al. had a maximum drain current ($I_{d,max}$) of 0.94 A/mm, which was 34 % higher than the conventional HFET [18]. On the other hand, experiments conducted by Javorka et al. yielded a I_d increase by 51 % for Si_3N_4-passivated HFETs with $I_{d,max} = 0.68$ A/mm [61, 59].

Apparently, SiO_2- and Si_3N_4-passivated devices show an I_d increase of some tens of percent. It is interesting to note, that for each experiment the relative change of I_d between conventional and passivated HFET is significantly higher than the relative change of

sheet resistivity, which was extracted from Hall measurements as listed in table 6.3. In this respect, the statement "The improved properties of 2DEG after Si_3N_4 passivation resulted in improved DC HEMT properties" [18] is not wrong, but a more differentiated explanation might improve the understanding of the I_d-increase for both the SiO_2- and the Si_3N_4-case.

The free surface passivation affects the properties of the 2DEG between the gate- and ohmic-contacts. In particular, the source resistance decreases (see table 6.3). It is known from section 5.3, that a decrease of the source resistance not only increases the output transconductance (g_d), but also increases I_d. In this sense, the R_s-decrease of 13 % for the SiO_2-passivated HFET is partially responsible for the 40 % I_d-increase. So is the 17 % R_s-decrease partially responsible for the 51 % I_d-increase of the Si_3N_4-passivated HFET in [61, 59]. It remains to be clarified though, which mechanism is responsible for the remaining I_d-increase in either case.

RF For a SiO_2-passivated HFET with a gate-length (L_g) of 500 nm the cutoff frequency (f_T) was 14 % higher than that of a conventional HFET with $f_T = 17.6$ GHz. As an example for RF-performance figures reported on Si_3N_4-passivated devices consider a 65 % increase from 17 GHz to 28 GHz achieved by Javorka et al. [61].

According to the models presented in section 5.4, an improvement of f_T can be due to an increase in g_m, a decrease in C_{gs} and/or C_{gd} and a decrease in resistive parasitics. For both the SiO_2- and the Si_3N_4-passivated devices C_{gs} will be the same for passivated and conventional devices. The change in C_{gd} due to the 100 nm thick Si_3N_4 layer is too small to have an effect on f_T, so does the 12.4 nm SiO_2-layer. The obvious reason for the f_T-increase of the SiO_2-device is the g_m-improvement of comparable order. For the Si_3N_4-passivated device though, the 20 %-increase in g_m does not seem sufficient as explanation of the 65 %-improvement in f_T. Therefore, the data reported in [61] state that Si_3N_4-passivated devices reach better RF performance than SiO_2-passivated devices, but this finding has to be treated with caution due to the lacking explanation of the f_T-increase in [61] and considering the results reported in [18], where only a marginal increase of f_T was reported for Si_3N_4-passivated devices.

Load Pull For SiO_2-passivated HFETs, an output power density of 4.1 W/mm was found at $V_{ds} = 22$ V and $f = 7$ GHz, corresponding an improvement relative to a conventional HFET of 32 %. For Si_3N_4-passivated devices, comparable results were reported as follows: Bérnat et al. achieved an 88 % increase from 3.81 W/mm to 7.16 W/mm at $V_{ds} = 27$ V and $f = 7$ GHz. According to the author, this improvement is mainly due to the improvement of the DC behavior [18]. Other authors report improvements of comparable order. For instance, Green et al. state that the addition of a Si_3N_4 passivation layer to undoped GaN/AlGaN HFETs increases the saturated power density by up to 100 % to 4 W/mm at 4 GHz [44]. An increase of breakdown voltage by 25 % and the mitigation of DC/RF-dispersion are seen as the main reasons for the increase.

Insulated Devices

In the following, the performance of SiO_2-insulated devices discussed in section 6.1 and 6.2 will be compared to GaN/AlGaN MISHFET using Si_3N_4 as a gate insulator. The results chosen for comparison were reported by Ochiai et al. [112] and by Adivarahan et al. [1]. Ochiai et al. fabricated a GaN/AlGaN MISHFET with a n-doped layer structure on sapphire substrate according to a technology well comparable to the one used throughout this work. The 10 nm thick Si_3N_4-layer was deposited by ECR sputtering. Adivarahan et al. chose an unintentionally doped GaN/AlGaN layer structure on SiC-substrate and deposited a 8 nm thick Si_3N_4-layer by PECVD. Again, the technology applied is comparable to the one used to fabricate the SiO_2-MISHFETs.

Threshold Voltage In section 6.1, a MISHFET with SiO_2-insulation was presented with a threshold voltage (V_{th}) of $-10.8\,\mathrm{V}$, which was 125 % higher than that of a conventional HFET. The shift of V_{th} was due to the additional dielectric layer ($d^{\mathrm{insul}} = 12.8\,\mathrm{nm}$, $\epsilon_{\mathrm{r}} = 3.9$) causing the gate-source capacitance to drop by $-50\,\%$, and a 80 % higher drain current. Ochiai et al. reported on a Si_3N_4-insulated MISHFET with a V_{th} shift of $+150\,\%$ relative to the conventional reference device with $V_{\mathrm{th}} = -2\,\mathrm{V}$ [112]. Here, the V_{th}-shift was due to the additional layer ($d^{\mathrm{insul}} = 10\,\mathrm{nm}$, $\epsilon_{\mathrm{r}} = 7$) and an 20 % increased drain current.

From the available figures it can be concluded, that the SiO_2-MISHFET provides better channel control abilities, since the V_{th}-loss is smaller than for the Si_3N_4-device although the dielectric is thicker, the relative dielectric constant is lower, and the drain current to control is higher.

Gate current For the SiO_2-MISHFETs presented in the previous sections, gate currents (I_{g}) slightly above 100 pA were measured, being 3 to 4 orders of magnitude lower than the gate currents of a conventional HFET. In comparison, the gate leakage currents reported by Ochiai were about three orders of magnitude lower compared to I_{g} of the conventional GaN/AlGaN HFETs [112]. The gate-leakage currents of Si_3N_4-MISHFETs presented by Adivarahan et al. [1] were well below 100 pA at gate bias values from $-10\,\mathrm{V}$ to $+8\,\mathrm{V}$, i.e. the MISHFET gate-leakage current is 5 orders of magnitude lower than that of a conventional HFET.

The comparison of the available empirical data reveals the potential for further I_{g}-reductions of SiO_2-MISHFETs: due to the wider band gap and also the greater conduction band offset of SiO_2, even more effective mitigation of the gate current than for Si_3N_4-MISHFETs should be feasible (see section 4.2).

RF In section 6.2, the cutoff frequency (f_{T}) and maximum frequency of oscillation (f_{max}) of a series of SiO_2-MISHFETs of different insulator thicknesses were presented. The improvements for f_{T} and f_{max} relative to a conventional HFET were up to 30% and 26 %, respectively. Contrary to these findings, Adivarahan et al. reported on Si_3N_4-MISHFETs with only similar RF performance compared to those of regular III-N HFETs.

For instance, for devices with $L_g = 250\,\text{nm}$, an intrinsic cutoff frequency of 63 GHz for both the HFET and the MISHFET was determined [1]. Since further details regarding the Si_3N_4-devices are not available, the reasons for the superior small signal performance of the SiO_2-MISHFETs remains to be clarified.

Load Pull The output power (P_{out}) of the SiO_2-MISHFET presented in section 6.1 was 6.2 W/mm at a drain-source voltage of 22 V at 7 GHz and reached a twofold value compared to the conventional HFET. By Adivarahan et al. a Si_3N_4-device was reported with an output RF power of around 6 W/mm at 40 V drain bias within a frequency range of 2 to 26 GHz. This power performance was 3 dB higher than that from HFET of the same geometry [1].

Although a comparison of the devices in question is difficult due to the different parameter sets used, the available data give a first indication that SiO_2 is at least as suitable for MISHFET as Si_3N_4. Apparently, the gate-insulation by means of either SiO_2 or Si_3N_4 seems equally appropriate to increase the output power performance significantly.

Summary

The passivation of free AlGaN surfaces of heterostructure devices with SiO_2 and Si_3N_4 (both utilizing PECVD-technology), causes comparable changes in n_s and μ such that in either case R_s is reduced by approximately 10 to 20 %. Also, for SiO_2- and Si_3N_4-passivated devices, neither V_{th} nor C_{gs} is changed. Concerning the gate current, SiO_2 has proven to mitigate the surface current by one order of magnitude, whereas Si_3N_4 is not effective as a current-reducing means. For both dielectrics in question the DC output characteristic is improved, I_d rises for instance by 40 to 50 %. Regarding the RF-performance the circumstances are not quite clear: Although a significant f_T-improvement for Si_3N_4-passivated devices was reported, other experiments led to contrary conclusions - stating that the passivation with Si_3N_4 only marginally increases f_T. For SiO_2-passivated devices though, a moderate and plausible improvement of 14 % could be reached. In terms of RF power performance, a final conclusion is difficult due to the varying experimental parameter sets used. But here, a tendency in favor of Si_3N_4 is obvious.

Utilizing SiO_2 as gate-insulation appears to be beneficial in terms of better channel control: even though Si_3N_4 has a higher relative dielectric constant and even though the Si_3N_4-layer was significantly thinner, the gate-source voltage to be applied to pinch-off the SiO_2-device was (relatively) smaller but enabled to shut off a much higher drain current. Regarding the gate current reducing effect, the available data showed Si_3N_4-MISHFETs to be more effective - although band gap and conduction band offsets legitimate the opposite expectation. Nevertheless, the results show that it is reasonable to assume that the gate-currents can be further reduced by optimizing the SiO_2-technology. In terms of RF small signal figures, the comparison showed the superior performance of SiO_2-MISHFETs: Here, a significant increase of up to 30 % and 26 % could be achieved for f_T and f_{max}, respectively, whereas for Si_3N_4 the RF figures of merit remained nearly unchanged. Concerning the RF power performance, one has to cope with the same

difficulty as for the passivated devices: the configurations and parameter sets of the available experiments differed widely and a comparison is hardly possible. But it appears that both dielectric materials open up the possibility to increase the output power by approximately 3 dB at frequencies around 7 GHz and moderate drain-source voltages.

Chapter 7

Post-Deposition Annealing of Gadolinium Scandate

In the previous chapter, encouraging results with SiO_2 MISHFETs have been presented. It was shown that the approach to insulate the gate electrode has the potential to outperform conventional and passivated devices of similar structure and geometry. But it was also revealed that at least for dielectrics with a low dielectric constant, as is the case for SiO_2, the ability to control the 2DEG properties by means of the field effect is weakened significantly. And it was shown that the approach to use less than 10 nm thick SiO_2 layers is not appropriate to circumvent the above difficulty.

The substitution of SiO_2 by high-κ $GdScO_3$ is the method of choice to improve the control of the channel properties on the one hand, and to realize the advantages observable for SiO_2 MISHFETs, namely the improvement of DC, RF, and RF-power performance, on the other hand. But before starting to fabricate $GdScO_3$ MISHFETs, preliminary experiments had to be conducted aiming at the optimization of the specific annealing conditions after $GdScO_3$ deposition.

It is known from literature, that post-deposition annealing of rare-earth oxides can increase the structural density and permittivity of the material, and it can contribute to a reduction of the CV hysteresis [83]. The first attempts to incorporate $GdScO_3$ into GaN/AlGaN devices at the IBN showed, that annealing is not only an issue to further increase certain properties. In fact, neglecting the annealing issue ends up with devices which are hardly improved or even worse compared to conventional devices. Only if the optimum annealing parameters are known, the devices can benefit from the insulating and dielectric properties attributed to $GdScO_3$.

7.1 Variation of Annealing Temperature

From the many experiments conducted, two trials to find the optimal annealing routine will be presented in the following. The first experiment discussed in this section represents attempts to optimize the annealing process by varying the annealing temperature. In the subsequent section 7.2, the influence of utilizing an oxygen (O_2) atmosphere will be investigated. The findings will then be used in the subsequent chapters dealing with the performance of $GdScO_3$ heterojunction diodes (HDiode) and MISHFETs.

Experiment

The HDiodes were fabricated utilizing metal-organic vapor-phase epitaxy (MOVPE) grown GaN/AlGaN material on Al_2O_3 substrate. The AlGaN layer had a nominal thickness of 30 nm. The processing of the HDiodes started with a first optical lithography step defining the ohmic contacts. The ohmic contacts consisted of a Ti/Al/Ni/Au stack annealed at 900 °C for 30 s. The ohmic contacts covered the entire surface except for round openings dedicated to host the Schottky contacts. The Schottky contacts were defined by a second lithography step and were either $9.85 \cdot 10^{-9}$ m^2 or $2.46 \cdot 10^{-9}$ m^2 in size and consisted of a Ni/Au material stack. The spacing between the Ohmic and the Schottky contact was 5 μm.

To fabricate MISHDiodes, a $GdScO_3$ layer was deposited by electron beam evaporation (EBE) prior to the processing of the Schottky contact as described in appendix A.1. Figure 7.1 illustrates the EBE setup and thicknesses ($d_{\mathrm{EBE}}^{\mathrm{insul}}$) and annealing parameters used are listed in table 7.1.

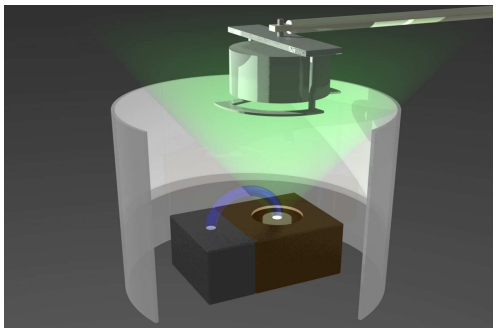


Figure 7.1: Electron-beam evaporation setup (provided by M. Roeckerath).

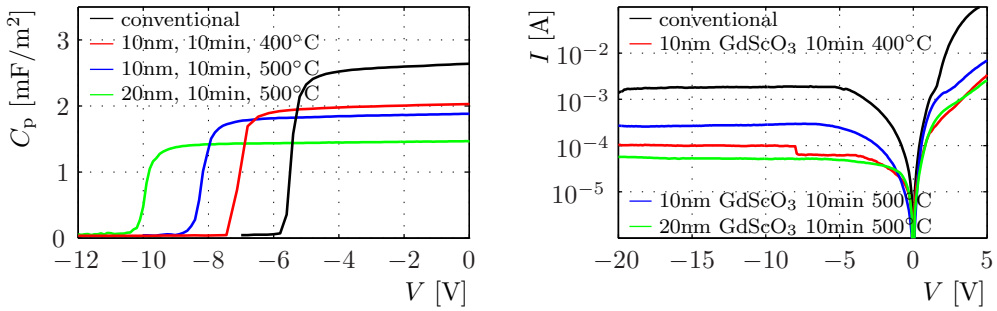
The HDiodes were characterized electrically by capacitance-voltage (CV) and current-voltage (IV) measurements as described in appendices B.1 and B.2.

Sample ID	$GdScO_3$ thickness (d_{EBE}^{insul})	annealing parameters
1068-16 (reference)	0 nm	no annealing
1068-15	10 nm	10 min@400 °C
1068-14	10 nm	10 min@500 °C
1068-13	20 nm	10 min@500 °C

Table 7.1: Parameters of $GdScO_3$ deposition and annealing to fabricate HDiodes on Al_2O_3 substrate.

Results and Discussion

First of all, the diode characteristics were measured by CV measurements. The resulting CV plots are illustrated in figure 7.2(a) and the main quantities are listed in table 7.2. The sheet carrier concentration (n_s) and the effective insulator thickness (d_{CV}^{insul}) were calculated from the given C_p values according to equation 5.2.



(a) capacitance vs. bias. (b) gate current vs. bias.

Figure 7.2: Influence of post-deposition annealing temperature on dielectric properties (a) and insulation (b) of $GdScO_3$ HDiodes. Results show that annealing at varying temperature did not improve the insulating properties significantly. The size of the Schottky contacts was $9.85 \cdot 10^{-9}$ m^2 (a) and $2.46 \cdot 10^{-9}$ m^2 (b).

Apparently, for all MISHDiodes the effective thickness d_{CV}^{insul} of the $GdScO_3$ layer deviates strongly from the nominal value d_{EBE}^{insul}. But what is more important is the fact, that the ratio between the thickness extracted from the C_p values (d_{CV}^{insul}) and the nominal thickness (d_{EBE}^{insul}) is the same for the 10 nm and 20 nm samples which were both annealed at 500 °C, and that $d_{CV}^{insul}/d_{EBE}^{insul}$ is higher for the samples annealed at 500 °C compared to the sample annealed at 400 °C. If it is assumed that the deposition of the $GdScO_3$ films was linear in time and identical for all samples, then the increase of the thickness deviation might be due to a sustained increase of the layer thickness during the annealing process, which becomes larger with increasing temperature.

The CV measurements also reveal, that a passivation effect is hardly noticeable when $GdScO_3$ is deposited on AlGaN: Although a 6 % increase of n_s was calculated for the 10 nm device annealed at 500 °C, this value is far too low to indicate a systematic passivation effect and might be due to the inaccuracies of the measurement system.

Sample ID	C_p	$\lvert V_\mathrm{th}\rvert$	n_s	$d_\mathrm{CV}^\mathrm{insul}$	$d_\mathrm{CV}^\mathrm{insul}/d_\mathrm{EBE}^\mathrm{insul}$
1068-16	$2.6\,\mathrm{mF/m^2}$	$5.8\,\mathrm{V}$	$8.9\cdot10^{12}\ \mathrm{cm^{-2}}$	-	-
1068-15	$-23\,\%$	$+28\,\%$	$+2\,\%$	$20\,\mathrm{nm}$	$200\,\%$
1068-14	$-29\,\%$	$+55\,\%$	$+6\,\%$	$27\,\mathrm{nm}$	$270\,\%$
1068-13	$-45\,\%$	$+90\,\%$	$+2\,\%$	$54\,\mathrm{nm}$	$270\,\%$

Table 7.2: Results of CV measurements of annealed $GdScO_3$ MISHDiodes. The sheet carrier density (n_s) and the effective $GdScO_3$ thickness ($d_\mathrm{CV}^\mathrm{insul}$) extracted from the C_p values are also listed. The % values indicate an increase (+) or decrease (-) relative to the value of the conventional HDiode (1068-16).

Current-voltage (IV) measurements were performed in a second characterization step. For the conventional HDiode, the maximum reverse current ($I_\mathrm{max}^\mathrm{rev}$) was 1.9 mA and the forward current at 3 V was 33 mA. Relative to the conventional device, the currents of the $GdScO_3$ MISHFETs were reduced between 0.8 and 1.6 orders of magnitude for negative voltages and between 1.2 and 1.6 orders of magnitude for positive voltages, as shown in figure 7.2(b). The measurements reveal an exponential increase of the forward current for all the devices.

The low current reductions and the exponential current increase of the MISHDiodes indicate, that the insulation property of all $GdScO_3$ layers prepared with a simple temperature treatment is far underneath expectations. Nevertheless, it is interesting to note, that the 10 nm $GdScO_3$ layer annealed at 400 °C insulates nearly as well as the 20 nm layer of the sample annealed at 500 °C. Apparently, the $GdScO_3$ films are sensitive to the annealing temperature.

In the following, the conclusions drawn from CV and IV measurements will be combined: if a) the $GdScO_3$ layer becomes thicker with increasing annealing temperature, and if b) the 10 nm device annealed at 500 °C shows lower insulation than the 10 nm device annealed at 400 °C, then it can be concluded that the insulation property is mainly governed by the density of the $GdScO_3$ material rather than its thickness. Thus, the higher the annealing temperature, the more the dielectric layer expands, becomes less dense and insulates less effectively.

Summary

In summary, the approach to find optimal annealing conditions by varying the annealing temperature does not improve the insulating properties of the insulating layer significantly. Temperature treatment increases the effective thickness, but decreases the density of the material and thus makes the material less resistive.

7.2 Annealing in Oxygen Atmosphere

The previous section has demonstrated that a simple post-deposition temperature treatment of $GdScO_3$ is not a sufficient means to realize highly effective gate-insulating layers. In the following, the key experiment will be presented that helped to find a way to fabricate $GdScO_3$ layers with competitive insulation on the one hand side and excellent dielectric properties on the other hand.

Experiment

For this experiment, heterojunction diodes (HDiode) were fabricated utilizing metal-organic vapor-phase epitaxy (MOVPE) grown GaN/AlGaN/GaN material on a SiC substrate. The AlGaN layer had a nominal thickness of 20 nm and a GaN cap-layer of 3 nm was deposited on top. The processing of the HDiodes started with a first optical lithography step defining the ohmic contacts. The ohmic contacts consisted of a Ti/Al/Ni/Au stack annealed at 900 °C for 30 s. The ohmic contacts covered the entire surface except for round openings dedicated to the Schottky contacts regions. The Schottky contacts were defined by a second lithography step, were either $9.85 \cdot 10^{-9}$ m^2 or $2.46 \cdot 10^{-9}$ m^2 in size, and consisted of a Ni/Au material stack. The spacing between ohmic and Schottky contact was 5 μm.

For the MISHDiodes, a $GdScO_3$-layer with 10 nm thickness was deposited by means of electron beam evaporation (EBE) as described in appendix A.1 and was annealed under different atmospheric conditions prior to the processing of the Schottky contact. The thickness ($d_{\mathrm{EBE}}^{\mathrm{insul}}$) and the annealing parameters used are listed in table 7.3.

diode/ transistor	$GdScO_3$ thickness ($d_{\mathrm{EBE}}^{\mathrm{insul}}$)	annealing parameters
F10 (reference)	0 nm	no annealing
F12	10 nm	10 min@500 °C, O_2-atmosphere
F13	10 nm	10 min@500 °C

Table 7.3: Parameters of $GdScO_3$ deposition and annealing to fabricate GaN/AlGaN/GaN heterojunction diodes on SiC substrate.

Results and Discussion

Input characteristic Capacitance-voltage (CV) measurements were performed as described in appendix B.2, the results are plotted in figure 7.3(a) and the main data extracted from the plots are listed in table 7.4 - together with basic calculation results concerning the sheet carrier concentration (n_{s}) and the effective $GdScO_3$-thickness ($d_{\mathrm{CV}}^{\mathrm{insul}}$) according to equation 5.2 and 5.5, respectively.

The CV data of the MISHDiode annealed without O_2 atmosphere (F13) shows CV data that do not seem reliable for $V < -4$ V. Apparently the 2DEG can not be controlled

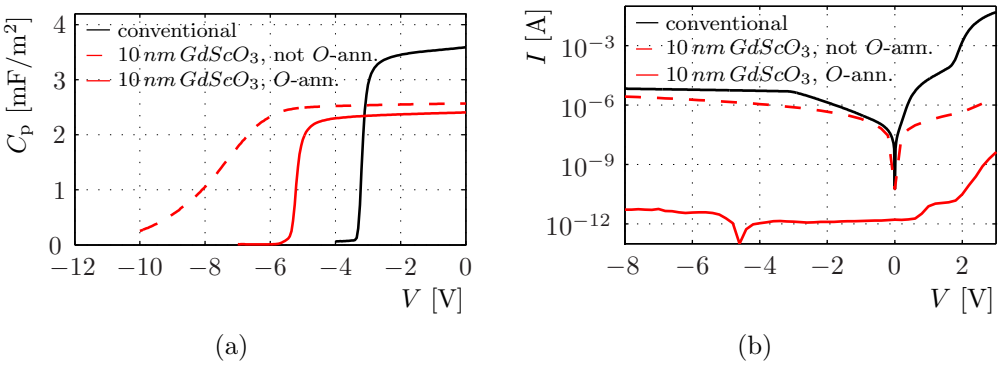


Figure 7.3: Effect of annealing in O_2 atmosphere on dielectric properties a) and insulation b) of $GdScO_3$ films. MISHDiodes were prepared to investigate the influence of $GdScO_3$ post-deposition anneal in O_2 atmosphere. Results show that an O_2 anneal is mandatory to yield $GdScO_3$ layers with excellent insulating properties.

Sample ID	C_p	$\lvert V_{th}\rvert$	n_s	d_{CV}^{insul}
F10	$3.6\,mF/m^2$	3.6 V	$6.9 \cdot 10^{12}\ cm^{-2}$	-
F12	−33 %	+61 %	+10 %	33 nm
F13	−28 %	-	-	27 nm

Table 7.4: Results of CV measurements of O_2-annealed and conventionally annealed $GdScO_3$ MISHDiodes. The sheet carrier density (n_s) and the effective $GdScO_3$ thickness (d_{CV}^{insul}) extracted from the C_p values are also listed. The % values indicate an increase (+) or decrease (-) relative to the value of the conventional HDiode (F10).

effectively. Nevertheless, the CV data at 0 V should be usable for the further discussion. Comparing the CV data of the O_2-annealed sample (F12) with the data of the conventionally annealed sample (F13) it becomes apparent that the C_p-difference to the HFET-value is higher for the O_2-annealed sample. In other words, the $GdScO_3$ layer of the device F12 is (effectively) 6 nm thicker than the dielectric film of device F13. Since for both samples identical annealing temperatures were used, the thickness increase must be due to the annealing in O_2-atmosphere, e.g. by incorporation of oxygen into the crystal structure.

For the sake of completeness, a brief comparison with the CV data of the previous experiment will be made. The actual reference device (F10) had a higher C_p value and reduced V_{th}- and n_s values compared to the reference HDiode (1068-16) of the previously described experiment. The differences are due to the differences in the layer stacks used: The actual device (F10) had a 20 nm AlGaN- and a 3 nm GaN-layer on top, whereas the previously utilized device (1068-16) included a 30 nm AlGaN-layer.

In a second characterization step, current-voltage (IV) measurements were performed, figure 7.3(b) contains the IV plots. For the GaN/AlGaN-based HDiode, which served as the reference device, a typical IV curve was measured with a maximum reverse current of

7 μA and a forward current of 50 mA at 3 V. In comparison, $I_{\max}^{\text{rev}}$ was 6.1 and 0.4 orders of magnitude lower for the O_2 annealed MISHDiode and for the device annealed without O_2 atmosphere, respectively. With respect to the forward current, the comparison yields respectively 7.1 and 4.4 orders of magnitude lower currents for the above mentioned devices.

Apparently, the O_2-annealed $GdScO_3$ layer reveals excellent insulation properties over a broad voltage range. The shift of the current minimum to $V = -4.3$ V can be attributed to charging effects of the measurement system and should be independent of the device properties (the measurements had been made at a time before the measurement system was optimized for low-current measurements). On the other hand, the MISHDiode annealed without O_2-atmosphere shows a similarly insufficient performance as the MIS devices treated in the previous experiment.

As in the previous experiment, the findings gathered so far will be brought together in the following conclusions: a) the insulation property of $GdScO_3$ film increases drastically if it is annealed in O_2 atmosphere; b) the thickness of the $GdScO_3$ film increases if it is annealed in O_2 atmosphere; c) but from the previous experiment it is known that an increase of thickness does not necessarily increase the insulating properties of $GdScO_3$ films. It can be concluded, that annealing the $GdScO_3$ layer in O_2 atmosphere increases the layer thickness, but also increases the layer density, e.g. by incorporation of oxygen into the lattice.

Summary

To fabricate MISHDiodes with a highly insulating $GdScO_3$ dielectric it is mandatory to anneal the $GdScO_3$ layer in O_2 atmosphere. This treatment increases the effective density of the film and increases the effective thickness. Due to the increased thickness a slight drop in capacitance arises, but this minor drawback could be opposed by adjusting the deposition parameters towards thinner films.

Chapter 8

Gadolinium Scandate Diodes

On the way towards the fabrication of Metal-Insulator-Semiconductor Field-Effect Transistors (MISHFETs) with a highly effective Gadolinium Scandate ($GdScO_3$) layer, the optimum deposition and annealing parameters have been determined in the previous chapter. This chapter is dedicated to experiments that aim at realizing Metal-Insulator-Semiconductor Heterostructure Diodes (MISHDiodes) utilizing $GdScO_3$ as the dielectric, making use of the technology-related findings above.

The chapter is split into three sections. The first section reports on the dependence between the insulation property and the thickness of $GdScO_3$ layers, the following section presents experiments aiming at the electronic states at the AlGaN/$GdScO_3$ interface, and the final section applies the impedance spectroscopy method to study the dependence of the $GdScO_3$ coating of the semiconducting surface and the 2DEG properties.

8.1 Insulation versus Thickness

The experiment documented in this section aimed at the relation of insulating property of the $GdScO_3$ layer and its thickness. In particular, conventional HDiodes and $GdScO_3$ MISHDiodes were fabricated to a) prove the reproducibility of the achieved insulator thicknesses, b) to achieve small thicknesses of around 5 nm to compare the insulating properties directly to the results available for SiO_2 devices, and c) to investigate whether there is a dependence between leakage current reduction and insulator thickness.

Experiment

Heterostructure material grown by metal-organic vapor-phase deposition (MOVPE) at the IBN was used. A 1.5 μm GaN layer was grown on Al_2O_3-substrate, followed by a $Al_{0.3}Ga_{0.7}N$ layer of 30 nm thickness. As a key element of the applied MOVPE technology, an inverted inlet was utilized ("Jülich Process" [46]). For further details regarding the control of the GaN buffer resistivity and the growth of the AlGaN layer (Al content and layer thickness) refer to [132].

Square and round diodes were processed according to the standard processing technology as described in depth in appendix A.3. For the round and square HDiodes, the areas of the Schottky electrode were in the range of $0.625 \cdot 10^{-9}$ m^2 to $40 \cdot 10^{-9}$ m^2 and from $0.625 \cdot 10^{-9}$ m^2 to $10 \cdot 10^{-9}$ m^2, respectively. Figure 8.1 illustrates the structure of the HDiode and shows a picture calculated from Scanning Electron Microscopy (SEM) measurements of the device.

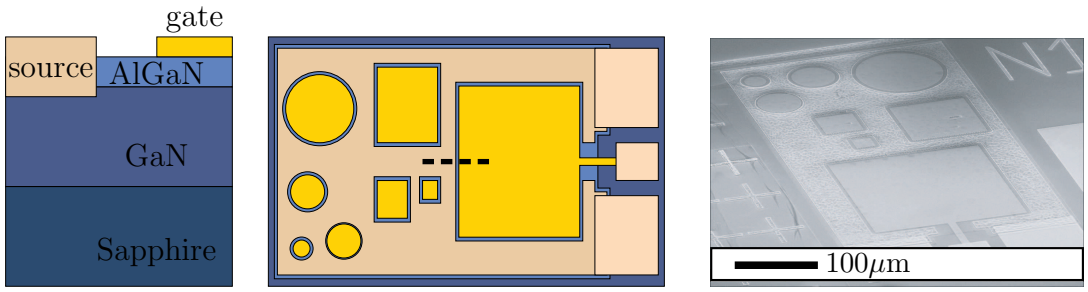


Figure 8.1: Profile (a), top-view (b), and SEM-picture of a heterostructure diode (c).

To insulate the gate electrode, $GdScO_3$ layers with a nominal thickness ($d_{\mathrm{EBE}}^{\mathrm{insul}}$) of 5 nm, 20 nm, and 30 nm were deposited by electron-beam evaporation (EBE) (for details see appendix A.1). After deposition, the layers were annealed at 500 °C for 10 min in an O_2 atmosphere - as was identified to be the optimum annealing procedure in chapter 7.

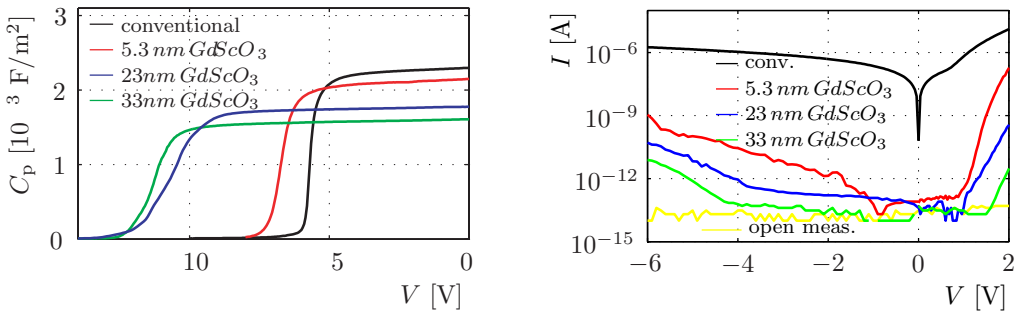
The devices were characterized electrically by means of current-voltage (IV) and capacitance-voltage (CV) measurements, according to the appendices B.1 and B.2, respectively.

Results and Discussion

Input Characteristic In a first characterization step, CV measurements were performed and revealed a gate-source capacitance (C_{p}) for a conventional $(100\,\mu\mathrm{m})^2$ HDiode of 2.3 mF/mm. For the 5 nm, 20 nm, and 30 nm MISHDiodes, the C_{p} value was 6 %, 23 %, and 30 % lower, respectively. Threshold voltage (V_{th}) was −6.7 V for the conventional device, the absolute V_{th} values of the $GdScO_3$ devices were 15 % higher for the 5 nm thickness, and doubled for the 20 nm and 30 nm $GdScO_3$ diodes. The CV curves are depicted in figure 8.2(a).

Taking into account a dielectric constant of 20 for $GdScO_3$, calculations according to equation 5.5 yield effective thicknesses ($d_{\mathrm{CV}}^{\mathrm{insul}}$) of 5.3 nm, 22.7 nm, and 33 nm for the thin, medium, and thick insulation layer, respectively. Apparently, the deposition rates are much closer to the nominal $d_{\mathrm{EBE}}^{\mathrm{insul}}$-values than in the first experiment (compare chapter 7), which is mainly due the improvements achieved for the EBE technology.

IV measurements were performed in a second characterization step. The maximum reverse current ($I_{\mathrm{max}}^{\mathrm{rev}}$) of a $(50\,\mu\mathrm{m})^2$ square diode made of a conventional layer stack was



(a) (b)

Figure 8.2: Input characteristic of a $GdScO_3$ MISHFETs compared to a conventional HFET.

1.8 μA at a bias of -6 V. For the 5.3 nm, 22.7 nm, and 33 nm $GdScO_3$ MISHDiodes the same figure was determined to be 3.2, 4.5, and 5.4 orders of magnitude lower, respectively. The maximum forward current ($I_{\text{max}}^{\text{forw}}$) for the conventional device at 2 V was 12.9 μA, which is 1.9, 4.6, and 6.7 orders of magnitude higher than the corresponding values for the 5.3 nm, 22.7 nm, and 33 nm MIS devices, respectively. The IV plots are illustrated in figure 8.2(b).

The results indicate that the insulation due to the $GdScO_3$ layers increases with the oxide thickness for both the forward and the reverse bias case. In figure 8.3 the $d_{\text{CV}}^{\text{insul}}$ values are correlated with the achieved reductions of the reverse current. At this point of discussion it is not suggested that the resistivity depends exponentially on the $GdScO_3$-layer thickness: Although the data points in the logarithmic-scale plot could be connected by a straight line it must be noticed, that the data-line would intersect the y-axes at positive ΔI_{rev} values. Nevertheless, it can be stated that there clearly is a dependence between thickness and the resistivity of the layer for layers that have gone through an annealing step in O_2-atmosphere.

Summary

The experiments showed, that the insulation of the gate with $GdScO_3$ results in very low gate currents even for oxide layers as thin as 5 nm. Furthermore, the gate leakage reduction is more effective the thicker the $GdScO_3$ becomes. It also showed, that input capacitances for MISHFETs can be reached that are only slightly underneath the capacitance values of conventional devices.

8.2 Electronic States

While performing capacitance-voltage (CV) measurements with MISHDiodes in the experimental context described in section 8.1, the following phenomenon became notice-

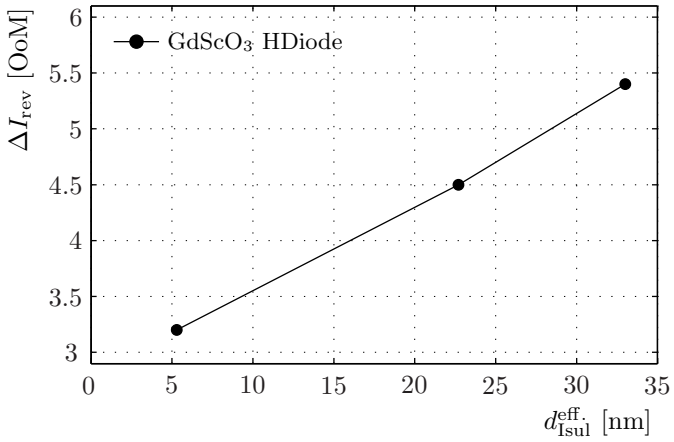


Figure 8.3: Current reduction relative to conventional device versus $GdScO_3$ thickness.

able: the threshold voltage (V_{th}) changes from its initial value to a more positive value if the applied bias range expands into the positive bias regime, i.e. a threshold shift (ΔV_{th}) is observed, defined as the difference of the threshold voltage before and the threshold voltage after application of positive voltage stress. Even at this point it is reasonable to assume, that this effect is due to a charging of traps located in the oxide film and/or at the oxide/semiconductor interface of the device, as discussed for instance in [136].

This finding might bear a disadvantage for MISHFETs, since a charging of traps would have a significant effect on device operation and performance if it is operated with gate source biases (V_{gs}) above 0 V. And operating a MISHFET with positive V_{gs} values has been identified as one major advantage of the MIS concept over the conventional HFET approach, as argued in section 2.1).

On the other hand, the observed ΔV_{th} opens up the chance to study the electronic states within the oxide film and at the oxide/semiconductor interface. Thus, this section will investigate the above effect in detail, starting out with some preliminary considerations on how to ensure stable measurement conditions, followed by an analysis of the dependence of ΔV_{th} on the biasing conditions.

Experiment

To investigate traps and related effects, GaN/AlGaN HDiodes and MISHDiodes on SiC substrates were processed according to the standard processing technology described in appendix A.3. The MISHDiodes were fabricated with 5 nm and 10 nm thick $GdScO_3$ layers underneath the gate. Electron-beam evaporation (EBE) was chosen for deposition, a subsequent annealing at 500 °C was performed for 10 min in O_2-rich atmosphere.

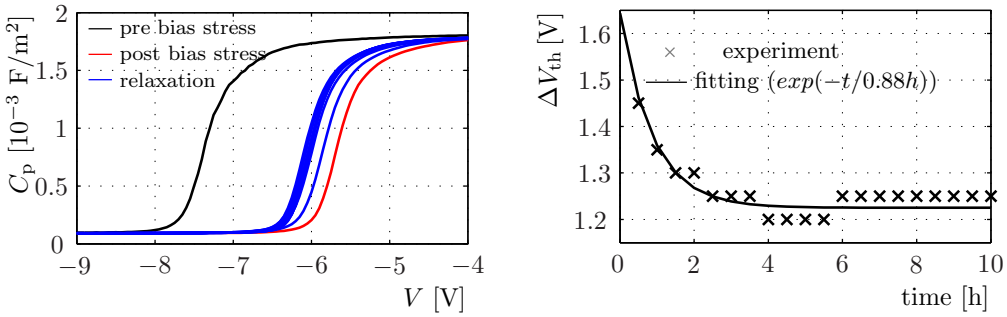
The CV measurement technique was utilized as described in appendix B.2. A ultra violet (UV) lamp was used in addition to manipulate the states of the existing traps by optical excitation. The series of subsequent measurements were controlled by a Matlab script

running on a personal computer which was connected to the measurement system by a GPIB interface.

Results and Discussion

Positive Bias Stress At first, the dependence of ΔV_{th} on time was examined. The devices used for this experiment were measured for the first time many weeks after processing had been finished, i.e. any possible charging effect of the devices due to fabrication should have decayed. Figure 8.4(a) illustrates the results of a measurement series expanding over a 10 h-time period. The initial CV curve is colored in black. For the ease of analysis, V_{th} is defined as the voltage at which $C_{\mathrm{p}} = 1\,\mathrm{mF/m^2}$. With this rule, V_{th} is determined to be $-7.3\,\mathrm{V}$ for the initial CV measurement.

The red curve represents the first measurement after a bias stress of $+3\,\mathrm{V}$ had been applied for 10 s. In this case, $V_{\mathrm{th}} = -5.7\,\mathrm{V}$, thus ΔV_{th} was 1.6 V. The blue curves stand for periodically performed CV measurements with 30 min in between. The blue curves indicate a relaxation process towards the initial CV curve, but the curves converge towards a level corresponding to a V_{th} of $-6\,\mathrm{V}$, which is far off the initial CV curve. To analyze the relaxation process in detail, the experimental data were fitted to an exponential function with a time constant of 0.88 h. Both the experimental data and the fit are plotted in figure 8.4(b).



(a) (b)

Figure 8.4: Threshold voltage shift of a $GdScO_3$ MISHDiode over time after positive bias stress: Capacitance-voltage (CV) curves (black: initial state, red: state after positive bias stress, blue: relaxation states) (a) and fitting of threshold shift (ΔV_{th}) to an exponential function (b).

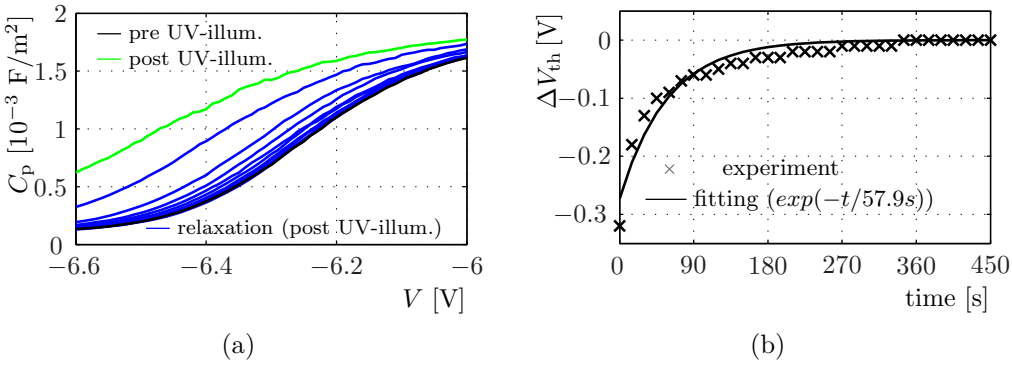
To interpret the results it is assumed that electronic states exist in regions underneath the gate and above the 2DEG. At room-temperature, a certain fraction of the states are occupied with charge carriers. Applying a positive voltage to the device, charge carriers are injected into the region between gate electrode and 2DEG and occupy the vacant electronic states. In other words, the charge carriers get trapped. Compared to the initial state of the device, the region above the 2DEG is less positively charged. As a consequence, the bias to be applied to the gate to reach depletion of the 2DEG needs to

be less negative, thus $\Delta V_{\mathrm{th}} > 0\,\mathrm{V}$.

It was observed that ΔV_{th} did not vanish over time but converged to a value far off from the initial level. This indicates that the trapping of the charge carriers is very stable and permanent. Thus it is necessary to find a means to reset" the device to its initial state.

UV illumination The previously described measurement series has shown, that once a positive bias has been applied to a MISHDiode the resulting ΔV_{th} does not vanish even after a long time period. But for a systematic study of different bias conditions it is mandatory to "reset" the device to its initial state. Thus, ultra violet (UV) illumination was examined as a possible means to bring back the device to its original state.

Figure 8.5(a) shows the CV curves of a measurement series carried out to investigate the influence of UV light on a device which is in its original state: The black curve represents the initial state of the device, with V_{th} evaluated to be $-6.2\,\mathrm{V}$. After the device has been exposed to UV light for 10 s, the measured CV curve - colored in green - shifts to more negative values, resulting in a ΔV_{th} of $-0.3\,\mathrm{V}$. The subsequent measurements yield CV curves, which are blue colored, approaching the initial curve, i.e. ΔV_{th} vanishes after approximately 4 min. Fitting ΔV_{th} to an exponential function yields a time constant of 58 s. Both the experimentally determined threshold shifts and the fitted function are depicted in figure 8.5(b).



(a) (b)

Figure 8.5: Threshold voltage shift of a $GdScO_3$ MISHDiode over time after UV illumination for 10 s: Capacitance-voltage (CV) curves (black: initial state, green: state after UV illumination, blue: relaxation states) (a) and fitting of threshold shift (ΔV_{th}) to an exponential function (b).

Again it is assumed, that the initial condition of the device is characterized by a certain fraction of the existing electronic states being occupied. By UV illumination the trapped charge carriers received energy sufficient to let them escape from the electronic state. The region above the 2DEG is - compared to the initial condition - more positively charged. Thus, the negative bias applied to the device to reach depletion of the 2DEG needs to be increased. After UV illumination has stopped, the electronic states are filled again with negative charge carriers, the device relaxes within a few minutes to its initial condition.

Method to "Reset" Device The finding of the above paragraph was that the combination of UV illumination followed by a 4 min relaxation period does not distort the initial state of a device. In the following, the illumination of the device with UV light is utilized to bring the device back to its initial state - even if a positive bias had been applied before.

An additional measurement series was performed in which a positive bias stress was applied to a MISHDiode, and afterwards the stress-induced change was eliminated by a 30 s UV treatment. Figure 8.6(a) shows the initial CV curve in black color, the three curves in red correspond to measurements performed after distinct bias stress treatments, a green curve stands for the measurement after UV illumination, and the series of blue curves represent the relaxation process towards the initial device state. The ΔV_{th} over time is depicted in figure 8.6(b).

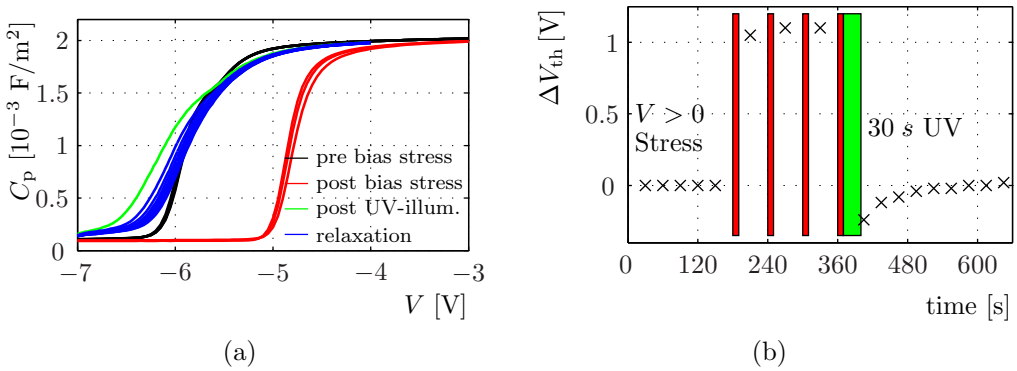


Figure 8.6: UV illumination (30 s) to eliminate threshold voltage shift induced by positive voltage stress, illustrated by a series of capacitance-voltage curves recorded over time (a), and the corresponding threshold voltage shifts (ΔV_{th}) over time (b).

As a result of the previous experiments a method to reach a clearly defined trapping state has been established; and further experiments involving a variation of the bias stress parameters can be performed in the following.

Location and Density of Traps With the previously gathered knowledge, the task is now to find out about the location and density of traps. The following considerations help to understand the experiment to be made. If the ΔV_{th}-relevant traps were located at any other region but the oxide film or the semiconductor/oxide interface, then the V_{th} shift as a consequence of positive bias stress would be observable for conventional devices also.

If the traps can be assumed to be located either in the oxide bulk or the semiconductor/oxide interface, then the exact region can be determined by comparing the threshold shifts of $GdScO_3$ devices with different thicknesses. If the traps were located within the oxide bulk, then the V_{th} shift should be greater for devices with thicker $GdScO_3$ layer, because the total amount of charge responsible for the threshold shift would scale with

the thickness. If the V_{th} shift remained constant for any $GdScO_3$ thickness, then the traps are likely to be located at the interface and the total amount of charge involved would be independent on the oxide thickness.

The CV measurements of conventional devices and of devices with 10 nm and 5 nm thick $GdScO_3$ layers are depicted in figure 8.7. For the conventional devices, only negligible V_{th} differences can be observed for measurements before and after positive bias stress. For the $GdScO_3$ diodes, the V_{th} shift of the device with 10 nm thick $GdScO_3$ layer is around 2 V, whereas for the 5 nm $GdScO_3$ device the V_{th} shift is approximately 1 V before and after application of positive bias stress.

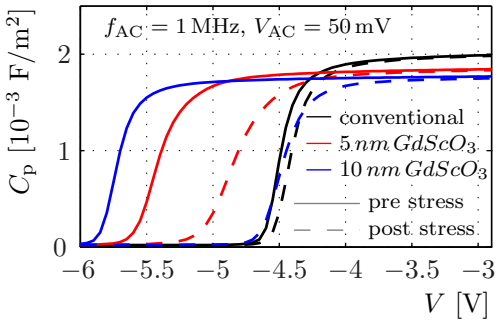


Figure 8.7: Threshold shifts of conventional HDiodes and MISHDiodes with 5 nm and 10 nm thick $GdScO_3$ layers.

According to the above considerations, the measurement data indicate that an observed V_{th} shift is due to traps related to the oxide, because for the conventional device the observed V_{th} shift are negligible. Furthermore, since the V_{th} shift of the device with 5 nm thick $GdScO_3$ layer is exactly half of the V_{th} shift of the device with the double as thick $GdScO_3$ layer, one can conclude that the traps are located within the oxide bulk: The thicker the oxide layer, the more traps exist and the higher the influence on the V_{th} shift.

According to equation 5.2, the amount of charge stored within the device before and after positive bias stress can be determined. The charge difference is - according to the above assumptions - proportional to the trap density. For the $GdScO_3$ devices, the analysis of the CV measurements yield a trap density of $8.4-11\cdot10^{17}$ cm^{-3}. This corresponds - if the traps were located at the interface - to an interface trap density between $6.5\cdot10^{11}$ cm^{-2} and $1.4\cdot10^{12}$ cm^{-2}. In fact, for gate dielectrics deposited on $III-V$ material (InGaAs), the minimum interface state density was in the low 10^{11} 1/eV/cm^2 region [109]. Also if compared to defect state densities of $1\cdot10^{10}$ cm^{-2} for the Si/SiO_2 interface [145], the results appear to be of a reasonable order of magnitude.

Energy Distribution of Traps The previous experiment has revealed that the traps are located within the $GdScO_3$ bulk at a density of approximately $1\cdot10^{18}$ cm^{-3}. The following experiment aims at the dependence of ΔV_{th} on the height of the applied positive bias. Hitherto, the bias was increased by constant steps of 1 V, starting out at 0 V. After having measured the capacitance after bias stress, the devices state was reset to the initial

condition by UV illumination. The state after the reset was measured as well.

Figure 8.8(a) holds all measurement curves, the ones recorded directly after bias stress consist of solid lines, the data belonging to after-illumination measurements are represented by dotted lines. The evaluated ΔV_{th} values are plotted over the bias stress applied in figure 8.8(b). For biases in the range of 0 V and 5 V, ΔV_{th} increases nearly linear. For higher biases ΔV_{th} saturates and converges to 3 V.

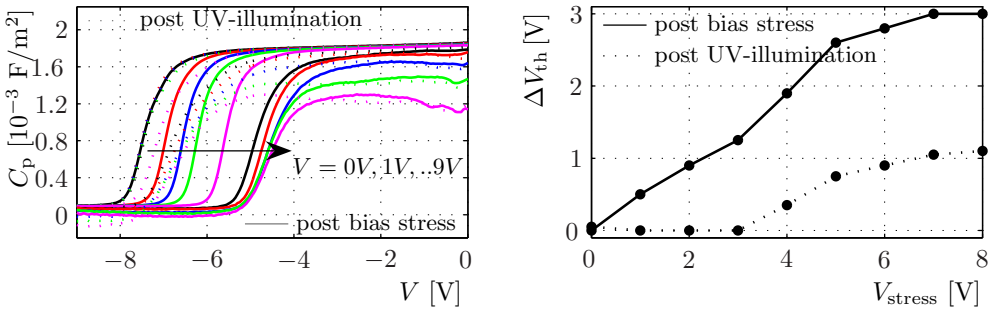


Figure 8.8: Shift of the CV curve (a) and extracted threshold shift (ΔV_{th}) of a $GdScO_3$ MISHDiode with increasing positive bias stress (b).

A closer look at the results for $0\,\mathrm{V} \leq V \leq 4\,\mathrm{V}$ - illustrated in figure 8.9(a) - reveals that the CV curves can be shifted back and forth almost perfectly, only at $V = 4\,\mathrm{V}$ the CV curve after illumination does not reach the initial curve. For $V > 4\,\mathrm{V}$, the stress-illumination-process is increasingly irreversible, as illustrated in figure 8.9(b). Not only that the V_{th} can not be reset to the initial value, also the capacitance of the on-state region drops increasingly and irreversibly.

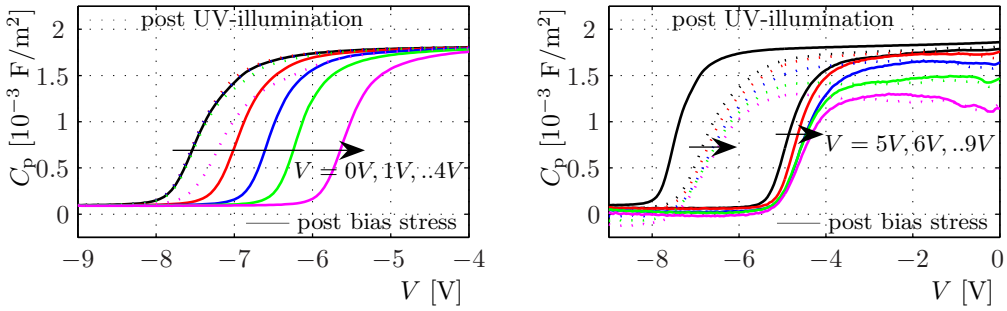


Figure 8.9: Separate illustration of figure8.8(a): $V_{\mathrm{stress}} \leq 4\,\mathrm{V}$ (a) and $V_{\mathrm{stress}} > 4\,\mathrm{V}$ (b).

The nearly linear increase of ΔV_{th} with V_{stress} can be explained with a uniform distribution of electronic states over the $GdScO_3$ band gap. The higher V_{stress}, the higher the energetic level of the electronic states to be occupied. At a certain V_{stress} level,

even the electronic states with the highest energetic level within the $GdScO_3$ band gap ($E_g = 5.5\,eV$) are filled. Thus, a further increase of V_{stress} does not shift V_{th} any more, and thus ΔV_{th} converges to its maximum value.

For $V_{stress} \geq 4\,V$, the results showed that UV illumination does not bring back the CV curves to the initial level. This is due to the limited photonic energy of the UV light (approximately 3.4 eV). Most likely, a light source with shorter wave length would "reset" the device even for $V_{stress} \geq 4\,V$.

A last issue to be discussed relates to the decreasing capacitance for V_{stress} greater than 4 V. One can only speculate that the dielectric constant of $GdScO_3$ degrades with increasing bias stress, and thus the total input capacitance of the device drops.

Relevance for Transistor Operation To investigate if the trapping effect observed is a relevant issue for HFETs and MISHFETs under operational conditions, the gate current of a typical HFET was measured with a positive drain source voltage (V_{ds}) also being applied. Figure 8.10 shows the IV curves measured with $V_{ds} = 0\,V, 1\,V, \ldots 5\,V$. The IV curve with its characteristic minimum at $V_{gs} = 0\,V$ shifts towards more positive values with increasing V_{ds}.

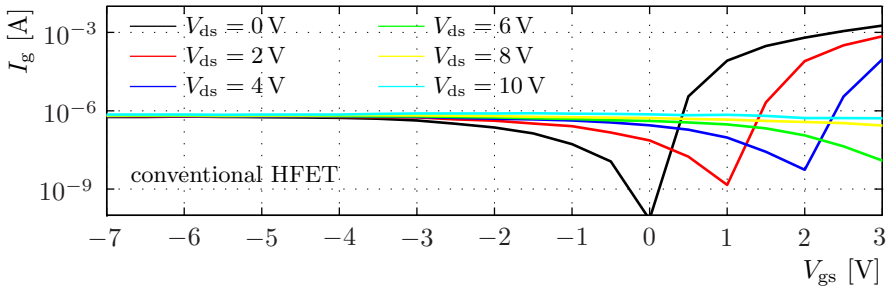


Figure 8.10: Gate current (I_g) as a function of gate source voltage (V_{gs}) for a conventional HFET with drain source voltage (V_{ds}) as parameter. The plot illustrates the influence of V_{ds} on the gate current: With increasing V_{ds} the current minimum shifts to more positive V_{gs} values.

The shift is due to the addition of half the V_{ds} value (for devices with symmetric drain and source access region) to the potential of the 2DEG underneath the gate. Thus, the effective potential difference that governs the diode is less positive than the applied V_{gs} if the device is operated with $V_{ds} > 0\,V$. As a consequence, the trapping of electrons into electronic states within the $GdScO_3$ film is an issue that can be neglected for MISHFETs under operational conditions.

The same argument also mitigates the problem of strongly (HFET) or moderately (MISHFET) increasing diode currents in the positive bias regime. Since the effective potential difference between gate electrode and 2DEG is likely to be negative under realistic operational conditions, the gate currents will be of the order to be found in the negative bias regimes of the corresponding diodes. If this reasoning holds true though, MISHFETs will not benefit from their symmetric IV curve as was argued in the introductory part.

Summary

The time constant of the exponential relaxation after positive bias stress is of the order of 1 h, whereas only a minor part of traps (around 25 %) is part of the relaxation process. The coefficient of the exponential relaxation after UV illumination is of the order of 1 min. Thus, UV illumination with subsequent waiting time of about 4 min is essential to bring back the device into a well defined initial state.

Most likely, traps are located within the oxide bulk. The bulk trap density is approximately $1 \cdot 10^{18}$ cm^{-3}. The electronic states of the $GdScO_3$ film are likely to be uniformly distributed over the band gap of 5.5 eV. UV light with a photonic energy of around 3.4 eV does not suffice to "reset" $GdScO_3$ devices if a high positive bias stress has been applied.

8.3 Sheet Carrier Concentration and Mobility

As was already discussed in the context of SiO_2 MISHFETs (see chapter 6), the coating of the semiconducting surface with a dielectric might impact the RF behavior of the device. Apparently, the deposition of the dielectric influences the properties of the 2DEG, although it is spatially separated from the dielectric by tens of nanometers.

To investigate the impact of the deposition of $GdScO_3$ on the 2DEG properties, the Impedance Spectroscopy method (IS) is applied to the MISHDiodes. Impedance Spectroscopy aims at gaining information regarding the charge carrier concentration (n_s) and the mobility (μ) of 2DEG charge carriers. The basic idea behind IS is to measure the impedance over a wide range of frequencies, typically in the range from kHz to MHz, and to fit a transmission line model to the measured data by varying parameters suitable to calculate the sheet carrier concentration (n_s), and mobility (μ). The relevant parameter to determine are the capacitance (C) and the resistance (R) as functions of the applied bias (V). The method is explained in depth in appendix B.2.

Experiment

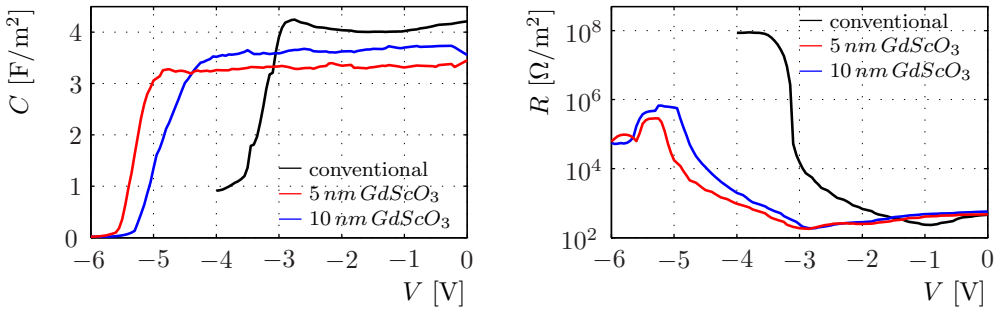
To investigate $GdScO_3$ MISHFETs by means of IS, heterostructure material grown by MOVPE was utilized to fabricate round HDiodes according the standard technology (see appendix A.3). The layer stack was based on a SiC substrate and consisted of a GaN buffer layer, a 20 nm AlGaN layer, and a 3 nm thick GaN cap layer. The ohmic contacts were made of a Ti/Al/Ni/Al stack annealed at 900 °C for 30 s. The Schottky contacts consisted of a Ni/Au metal stack.

For the MIS devices, $GdScO_3$ layers of 5 nm and 10 nm nominal thickness ($d_{\mathrm{EBE}}^{\mathrm{insul}}$) were deposited by means of electron beam evaporation (EBE) as described in appendix A.1. Subsequently, the devices were annealed at 500 °C for 10 min in O_2 atmosphere.

Results and Discussion

In the following, the parameter set ($C(V)$, $R(V)$, $G(V)$) to fit the experimentally determined impedance data to the transmission line model will be presented. Then n_s and μ, calculated from the fitting parameters, will be discussed.

Fitting Parameters The fitting routine determined the $C(V)$ functions which is depicted in figure 8.11(a). For the conventional device, the capacitance was $4.2\,\mathrm{mF/m^2}$ at $V = 0\,\mathrm{V}$, for the 5 nm MISHDiode it was 89 % and for the thicker one it was 80 % of the reference value. The threshold voltage (V_{th}) of the reference device was $-3.8\,\mathrm{V}$, for the MISHDiodes of 5 nm and 10 nm nominal thickness it was $-5.4\,\mathrm{V}$ and $-5.6\,\mathrm{V}$, respectively.



(a) Capacitance vs. bias

(b) Resistivity vs. bias

Figure 8.11: Results of Impedance Spectroscopy of $GdScO_3$ MISHDiodes: Fitting parameter capacitance (C) (a), and sheet carrier concentration (n_s) (b), both as a function of voltage (V).

The C levels of the MISHDiodes are as expected. Assuming a dielectric constant of 23, calculations yield actual thicknesses ($d^{\mathrm{insul}}_{\mathrm{Imp.Spec.}}$) of 5.4 nm and 10.3 nm, matching nearly perfectly the $d^{\mathrm{insul}}_{\mathrm{EBE}}$ values specified for the $GdScO_3$ deposition. The absolute level of C measured for the conventional device is higher though than the theoretical value for the 23 nm thick AlGaN/GaN layer.

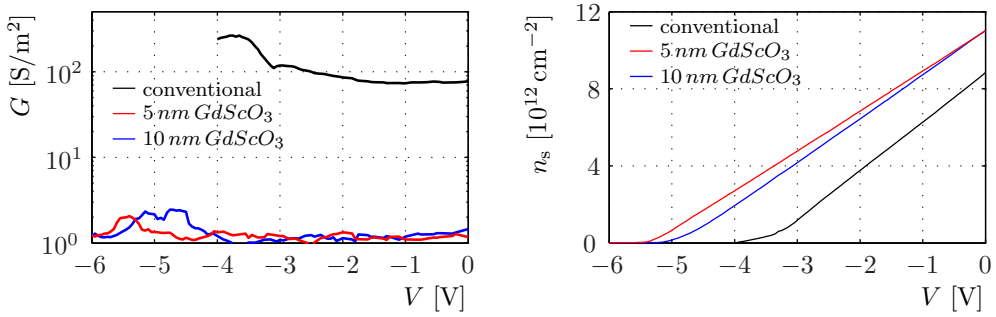
To fit the impedance data to the transmission line model, the $R(V)$ function depicted in figure 8.11(b) was determined. At $V = 0\,\mathrm{V}$, R was $457\,\Omega/\square$ for the HDiode, for the MIS devices R was 4 % and 24 % higher. The $R(V)$ function shows a minimum for the standard device ($235\,\Omega/\square$ at $-1\,\mathrm{V}$) and also for the MIS devices (around 20 %, lower at $-2.85\,\mathrm{V}$). At voltages near V_{th}, R rises to $88\,\mathrm{M}\Omega/\square$ for the reference device. For the MISHDiodes, R also rises, but their maximum values were two to three orders of magnitude lower. The R over V plots are illustrated in figure 8.11(b).

The values for 0 V agree well with results obtained from Hall measurements. The strong increase of R is due to the depletion of the 2DEG, and the highest values of R very well correspond to the residual drain currents one can measure for HFETs in the off-state. This is also in accordance with the fact, that for the MISHFETs the resistance of a

depleted 2DEG channel is around two orders of magnitude lower.

But the more interesting aspect is the minimum in resistance to be found for each of the device types. Since it can be assumed that R is inversely proportional to the product of n_s and μ, and that n_s increases monotonously with V, μ is likely to show a maximum as well. This will be discussed in the following.

But before - for the sake of completeness - the $G(V)$ function to fit the impedance data will be presented briefly. For the conventional device, a conductance (G) of $80\,\mathrm{S/m^2}$ was extracted for $V = 0\,\mathrm{V}$, which was relatively constant over V except for $-4\,\mathrm{V} < V < -3\,\mathrm{V}$ in which G increased rapidly to $240\,\mathrm{S/m^2}$. For both MIS devices, G remained at a level around $1\,\mathrm{S/m^2}$ over the whole voltage range, as can be seen in figure 8.12(a).



(a) Conductivity vs. bias

(b) Carrier concentration vs. bias

Figure 8.12: Results of Impedance Spectroscopy of $GdScO_3$ MISHDiodes: Fitting parameter conductivity (G) (a), and sheet carrier concentration (n_s) (b), both as a function of voltage (V).

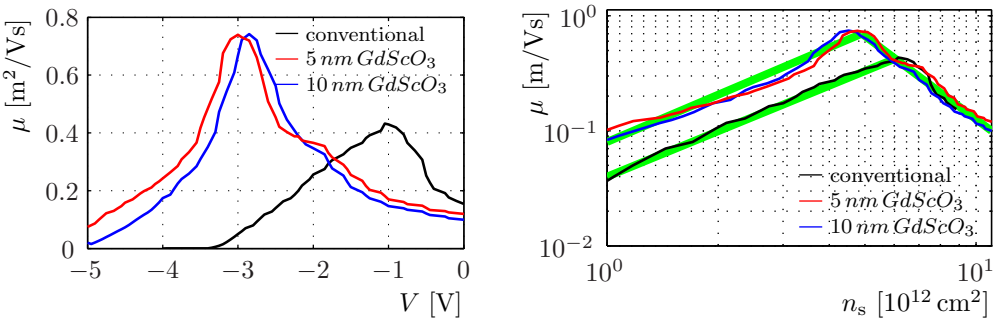
The results show the insulating property of $GdScO_3$, which remains constant over the applied voltage. In this sense, it supports the finding from the previous section 8.1, although the determined reduction of conductance is only two orders of magnitude.

Sheet Carrier Concentration and Mobility The sheet carrier concentration (n_s) was computed according to equation 5.2. At $V = 0\,\mathrm{V}$, n_s was $8.84 \cdot 10^{12}\ \mathrm{cm^{-2}}$ for the conventional device. For both MISHDiodes, n_s was 25 % higher than the reference value. The complete n_s function is plotted in figure 8.12(b).

According to the extracted data, the $GdScO_3$ layer can be attributed a passivation effect, a dependence of this effect on the thickness of the oxide layer is not apparent from the actual data.

As pointed out in appendix B.2, the mobility of the charge carriers on the 2DEG channel can be extracted from n_s and R data. Figure 8.13(a) contains the μ-V plots.

The mobility function of each device type reaches its maximum at voltages, that correspond to the V_{gs} values at which the best RF figures are measured (compare to the following section 9). This points at the possibility that not only the saturation velocity governs the RF behavior of HFETs. Thus, studying the low-field mobility allows



(a) Mobility vs. bias

(b) Mobility vs. carrier concentration

Figure 8.13: Results of Impedance Spectroscopy of $GdScO_3$ MISHDiodes: mobility of 2DEG carrier (μ) as a function of voltage (V) (a) and μ as a function of sheet carrier concentration (n_s) (b).

predictions concerning the RF performance of a device.

More insights can be gained by the plot μ over n_s in double logarithmic scaling, which is shown in figure 8.13(b). To guide the eye the bold green lines were drawn. It becomes apparent that for the MISHDiodes the maximum of μ is shifted towards higher values and towards more negative voltages, whereas the slopes of the curves remain unchanged.

To explain this shift, consider the following simple model. The total mobility μ is the result of the superposition of mobilities due to different scattering mechanisms. Equation 3.5 is an example to model the dependence quantitatively. For this discussion consider the simple case that the total mobility is the result of two scattering mechanisms being proportional and inversely proportional to n_s, respectively:

$$\mu = \frac{1}{an_s + b\frac{1}{n_s}}. \tag{8.1}$$

Figure 8.14(a) illustrates the above equation. As mentioned in section 3.1, impurity and piezoacoustic scattering diminishes the mobility of the 2DEG-carriers for low n_s-values, whereas this effect becomes less due to screening with increasing n_s. Thus, impurity and piezoacoustic scattering are represented by the n_s-proportional branch in figure 8.14(a). The $\frac{1}{n_s}$-branch represents interface roughness scattering. If the scattering mechanisms represented by the n_s-proportional branch become less, then the peak of the total mobility increases and occurs at a smaller n_s-value, as depicted in figure 8.14(b).

The results from Impedance Spectroscopy indicate a shift of the mobility-peak to higher μ-values at a smaller sheet carrier concentration. Thus it can be concluded, that either the piezoacoustic or the impurity scattering has become less by the coating of the semiconducting surface by $GdScO_3$.

Considering the impact on the former possibility, it is not likely that the $GdScO_3$-coating contributes to a reduction of piezoacoustic-related scattering, since the $GdScO_3$-layer is assumed to be amorphous, and thus the strain of the semiconducting layers should not be affected in such a way, that the piezoacoustic scattering would becomes less.

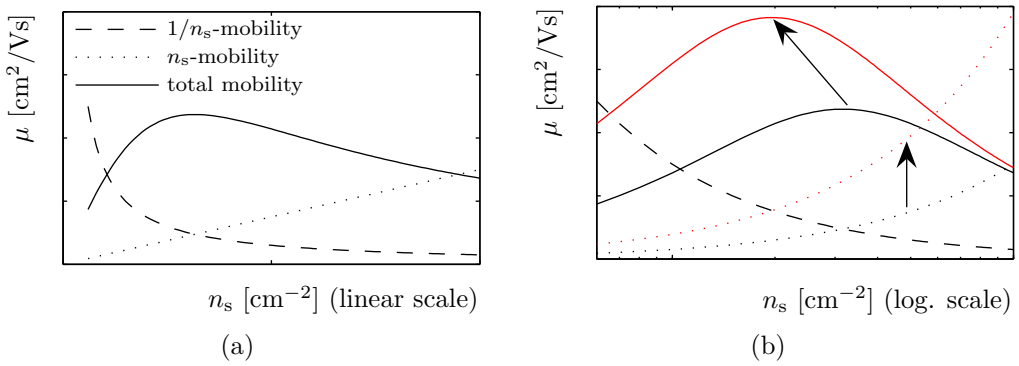


Figure 8.14: Impact of piezoacoustic scattering on mobility. The total mobility of the 2DEG carriers is modeled as the inverse sum of a $1/n_s$- and n_s-proportional mobility contribution, representing interface roughness and impurity/piezoacoustic scattering,respectively (a). A lowering of the impurity/piezoacoustic scattering will increase the n_s-related mobility and thus the total mobility will rise and its peak will shift to smaller n_s values (b).

Regarding the latter option, especially the impact of surface-near impurities might be mitigated by the $GdScO_3$-layer due to the screening of the Coulomb interactions of the charged surface and the interface states by electrostatic induction in the gate metallization of the MOSHFET as shown by Marso et al.[19]. Thus, it is reasonable to conclude, that the maximum mobility of charge carriers in the 2DEG increases due to the $GdScO_3$ insulating layer.

Chapter 9

Gadolinium Scandate Transistors

The previous Chapters presented important accomplishments on the way towards the fabrication of Gadolinium Scandate ($GdScO_3$) Metal-Insulator-Semiconductor Field-Effect Transistors (MISHFETs). At this point it is already known how to deposit and to anneal $GdScO_3$ layers to benefit from its insulating and dielectric properties. Furthermore, the dependence between $GdScO_3$ thickness and insulation on the one hand and thickness and capacitance on the other hand is known as well, and knowledge has been gained concerning the electronic states and the impact of $GdScO_3$ coating on the two-dimensional electron gas (2DEG) properties.

In the following, the main experiment of this work is presented: the realization of a $GdScO_3$ MISHFET utilizing GaN/AlGaN layers grown on Silicon Carbide (SiC). Besides the already known findings concerning gate-leakage reduction and capacitance increase - which should be confirmed in the following - we expect to learn about the DC, RF, and RF-power performance figures of a $GdScO_3$ MISHFET.

Experiment

To investigate $GdScO_3$ MISHFETs based on SiC substrates, structures with undoped and Si-doped AlGaN layers were used. The layer stack of the undoped devices consisted of a GaN and a 25 nm $Al_{0.3}Ga_{0.7}N$ layer with a 3 nm GaN cap layer on top. The AlGaN layer of the doped variant consisted of a 10 nm AlGaN / 5 nm AlGaN / 10 nm AlGaN substructure, whereas the thin layer was Si-doped at a concentration of $1 \cdot 10^{18}$ cm^{-3}. The material was grown by metal-organic vapor-phase epitaxy (MOVPE).

Transistors, round and square diodes, and van-der-Pauw patterns were processed according to the standard technology described in appendix A.3. The geometry of the devices is identical to those processed in the previous experiment described in section 8.1.

For the deposition of $GdScO_3$ layers, electron-beam evaporation (EBE) with subsequent annealing at 500 °C for 10 min in O_2 atmosphere was used. The nominal insulator thicknesses ($d_{\mathrm{EBE}}^{\mathrm{insul}}$) for the MISHFETs were 5 nm and 10 nm. Table 9.1 summarizes the main attributes of the different samples. Figure 9.1(a) and 9.1(b) illustrate the structure of the processed MISHFET, and figure 9.1(c) shows a SEM-picture of a MISHFET.

Sample ID	Si-doping	$GdScO_3$ thickness ($d_{\mathrm{EBE}}^{\mathrm{insul}}$)
Z10	none	0 nm
Z11	none	5 nm
Z03	none	10 nm
Y07	1e18 cm^{-3}	0 nm
Y06	1e18 cm^{-3}	10 nm

Table 9.1: $GdScO_3$ thickness and doping levels of MISHFETs on SiC substrate.

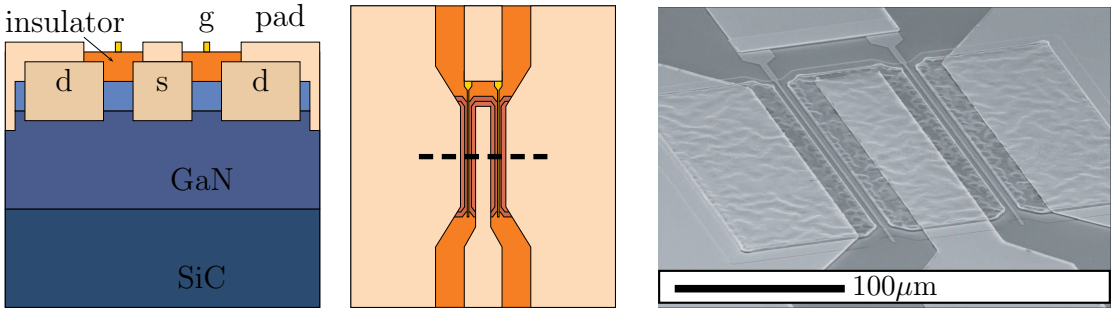


Figure 9.1: Profile (a), top-view (b), and SEM-picture of a MISHFET (c).

Electrical characterization of the devices was performed by means of current-voltage (IV), capacitance-voltage (CV), breakdown, pulsed IV, S-parameter, and Load-Pull measurements, according to the methods documented in appendix B.

Results and Discussion

Input Characteristic The results gained from CV measurements are illustrated in figures 9.2(a) and 9.2(b) for undoped and doped devices, respectively. The main quantities extracted from CV measurements are listed in table 9.2, including the sheet carrier concentration (n_{s}) and the effective thickness of the insulation layer ($d_{\mathrm{CV}}^{\mathrm{insul}}$), calculated by means of the model provided in section 5.1.

The CV results reveal, that the effective insulator thickness ($d_{\mathrm{CV}}^{\mathrm{insul}}$) extracted from the measurement data are significantly higher than the intended thickness for the EBE-deposition ($d_{\mathrm{EBE}}^{\mathrm{insul}}$). This indicates that the maturity of the EBE-process is yet to be improved, in particular the controllability of deposition rates needs to be increased. Nonetheless, in the following the $d_{\mathrm{CV}}^{\mathrm{insul}}$-values will be used as the effective thickness of the insulating layers.

Despite the rather thick $GdScO_3$-layers, the potential of $GdScO_3$ being used as gate dielectric becomes apparent: Even with a calculated effective thickness $d_{\mathrm{CV}}^{\mathrm{insul}}$ of 12.5 nm, the capacitance drop is only 15 % compared to conventional devices. To reach a similar improvement for SiO_2-insulated device, one had to reduce the insulation thickness down

Sample ID	C_p	$\lvert V_{th}\rvert$	n_s	d_{CV}^{insul}	$d_{CV}^{insul}/d_{EBE}^{insul}$
Z10 (ref.)	$2.4\,mF/m^2$	4.8 V	$6.8 \cdot 10^{12}\ cm^{-2}$	-	-
Z11	−26 %	+37 %	−6 %	12.5 nm	250 %
Z03	−15 %	+14 %	−6 %	25 nm	250 %
Y06 (ref.)	$2.5\,mF/m^2$	5.1 V	$7.2 \cdot 10^{12}\ cm^{-2}$	-	-
Y07	−30 %	+70 %	−5 %	30 nm	300 %

Table 9.2: Results of CV measurements of $GdScO_3$ MISHDiodes. The sheet carrier density (n_s) and the effective $GdScO_3$ thickness (d_{CV}^{insul}) extracted from the C_p values are also listed. The % values indicate an increase (+) or decrease (-) relative to the nominal thickness during EBE-deposition (d_{EBE}^{insul}).

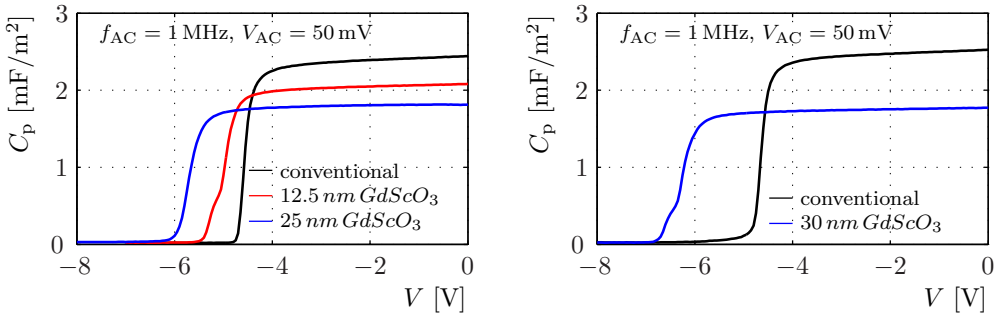


Figure 9.2: Capacitance-voltage (CV) characteristic of a conventional HDiode and $GdScO_3$ MISHDiodes with 12.5 nm and 25 nm effective insulator thickness (d_{CV}^{insul}) based on undoped GaN/AlGaN material (a), and of a HDiode and a $GdScO_3$ MISHDiode with $d_{CV}^{insul} = 30$ nm based on Si-doped material (b). The diode size was $(50\,\mu m)^2$.

to 2.4 nm and would still have to cope with a 20 % loss in capacitance (see section 6.2).

On the other hand it again becomes apparent, that a $GdScO_3$ coverage of the semiconductor surface does not yield significant passivation effects, which is a beneficial side-effect of SiO_2-insulated devices. The n_s data listed in table 9.2 even indicate a loss of around 5 %, although this reduction can also be due to measurement inaccuracies.

By means of low current measurements, the current-voltage characteristic was recorded. For undoped HDiodes with $(200\,\mu m)^2$-sized Schottky contacts, the maximum reverse current (I_{max}^{rev}) was measured to be $0.25\,\mu A$ at −8.0 V. Comparable measurements with 12.5 nm and 25 nm thick $GdScO_3$ layers yielded currents 3.9 and 4.4 orders of magnitude lower, respectively. For all device types, the IV curves showed a pronounced kink, which occurs at a bias of −4.7 V, −5.8 V, and −6.2 V for conventional, 12.5 nm, and 25 nm $GdScO_3$ devices, respectively. The maximum forward current (I_{max}^{forw}) was determined to be 33.5 mA for the conventional device, for the 12.5 nm and 25 nm $GdScO_3$ HDiodes the currents were 3.7 and over nine orders of magnitude lower, respectively. Figure 9.3(a) comprises the measurements that refer to the IV characterization of the undoped samples.

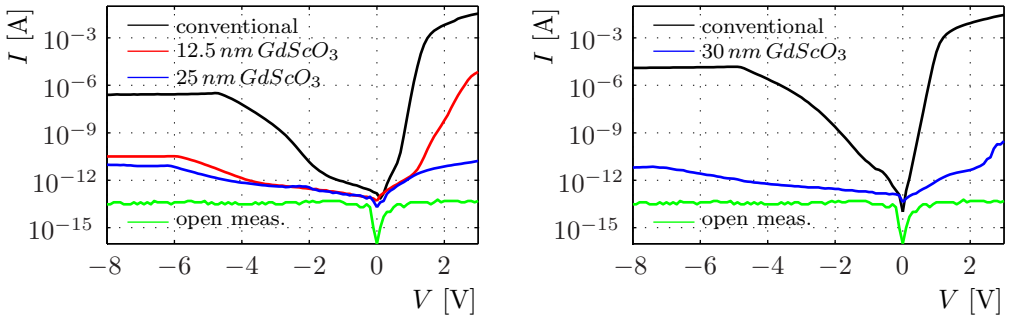


Figure 9.3: IV characteristic of a HDiode and $GdScO_3$ MISHDiodes with 12.5 nm and 25 nm effective insulator thickness ($d_{\mathrm{CV}}^{\mathrm{insul}}$) based on undoped GaN/AlGaN material (a), and of a HDiode and a $GdScO_3$ MISHDiode with $d_{\mathrm{CV}}^{\mathrm{insul}} = 30\,\mathrm{nm}$ based on Si-doped material (b). The diode size was $(200\,\mu\mathrm{m})^2$.

Concerning the doped samples, $I_{\mathrm{max}}^{\mathrm{rev}}$ was $1.2\,\mu\mathrm{A}$ for conventional $(200\,\mu\mathrm{m})^2$ HDiodes at $-8.0\,\mathrm{V}$. For MISHDiodes with a 25 nm $GdScO_3$ layer, the corresponding current was more than five orders of magnitude lower. Also for the doped samples, a kink in the IV curve was observed at $-4.7\,\mathrm{V}$ and $-6.7\,\mathrm{V}$ for the HDiode and the MISHDiode, respectively. The $I_{\mathrm{max}}^{\mathrm{forw}}$ of the conventional HDiode was 28 mA, for the 25 nm $GdScO_3$ device it was eight orders of magnitudes lower. The IV measurement results of the doped samples are depicted in figure 9.3(b).

The results indicate, that both $GdScO_3$ layers are an effective means to insulate the gate electrode. The experiment with undoped material showed that in the negative bias regime the reduction of the 12.5 nm device is similar to that of the device with 25 nm. For the positive bias range, the thicker layer clearly shows better insulating properties and its IV curve has the form to be expected for a MIS structure. But since the effective potential difference of gate and source at operating conditions of a HFET will be negative, the superior insulating properties of the thick $GdScO_3$ layer for positive biases will not be of much practical interest. In other words, both the 12.5 nm and the 25 nm $GdScO_3$ layers seem similarly appropriate for isolated-gate HDevices.

The experiment also indicated that $GdScO_3$ is a suitable means to insulate the gate electrode of doped devices. The gate current reducing effect is even higher than in the case of undoped devices: The gate current of the conventional HFET with doped layer is around one order of magnitude higher than for the conventional and undoped HFET. This difference can be explained by the highly doped AlGaN-layer, which acts as an additional channel capable to conduct gate electrons. The substitution of the Schottky barrier by a more effective MIS contact prevents the gate electrons to travel along this path, thus the current-reducing effect of the $GdScO_3$-layer is even higher for doped than for undoped structures.

Output characteristic The following results were gained from DC measurements of the output: For $V_{\mathrm{gs}} = 0\,\mathrm{V}$, the maximum drain current ($I_{\mathrm{d,max}}$) was $0.69 \pm 0.01\,\mathrm{A/mm}$

for all device types. Figure 9.4 illustrates the results.

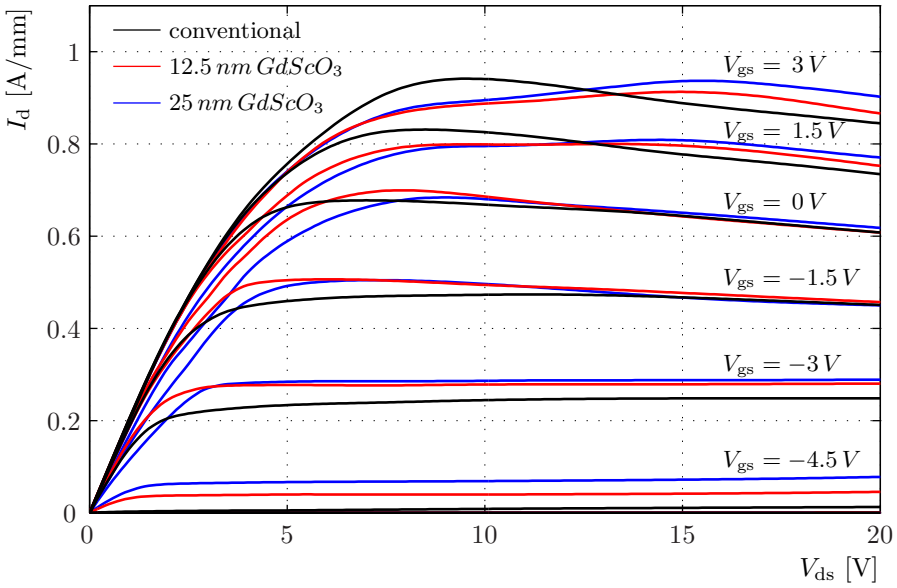


Figure 9.4: Output characteristic of a conventional HFET and 12.5 nm and 25 nm $GdScO_3$ MISHFETs.

The maximum transconductance ($g_{m,max}$) for the conventional HFET was 170.3 mS/mm, for the 12.5 nm $GdScO_3$ device $g_{m,max}$ dropped down to 94 % of the reference value, and the 25 nm device yielded 82 % - for all device types $g_{m,max}$ was computed for the drain source voltage at which $I_d\big|_{V_{gs}=0\,V}$ reaches its maximum. The Threshold voltage (V_{th}) of the conventional device was −5.5 V, for the 12.5 nm and 25 nm devices it was 10 % and 22 % more negative - as can be seen from figure 9.5(a).

The maximum output conductance ($g_{d,max}$) of the conventional device was 204 mS/mm. For the $GdScO_3$ devices, $g_{d,max}$ is 6 % and 18 % less. The knee voltage, i.e. the voltage at which I_d reaches its maximum ($V_{ds,sat}$) was 7 V for the conventional HFET, for the 12.5 nm and 25 nm $GdScO_3$ MISHFETs it was 8 V, and 9 V, respectively. The g_d-values calculated for $V_{gs} = 0$ V are plotted in figure 9.5(b).

The almost identical $I_{d,max}$-values of all devices are plausible considering the almost identical n_s-values extracted from CV measurement results. Thus, $GdScO_3$ can not be attributed a passivating property. The curves of the output characteristic are rather similar for all device types, pointing to a very similar capability to control the conducting channel. It also shows, that the heat dissipation property of the underlaying layer stack - which is basically due to the SiC layer - is not influenced by the use of $GdScO_3$.

The calculated g_m- and V_{th}-values support this view. The only slightly higher V_{th} values of the MISHFETs indicate the relatively low loss in C_{gs} due to the high-κ property of $GdScO_3$. From the differences in $g_{d,max}$ it can be concluded, that drain (R_d) and source resistance (R_s) are increasing with increasing $GdScO_3$ layer thickness. But the reason for the degraded parasitic resistance might also be the fact, that due to the applied process

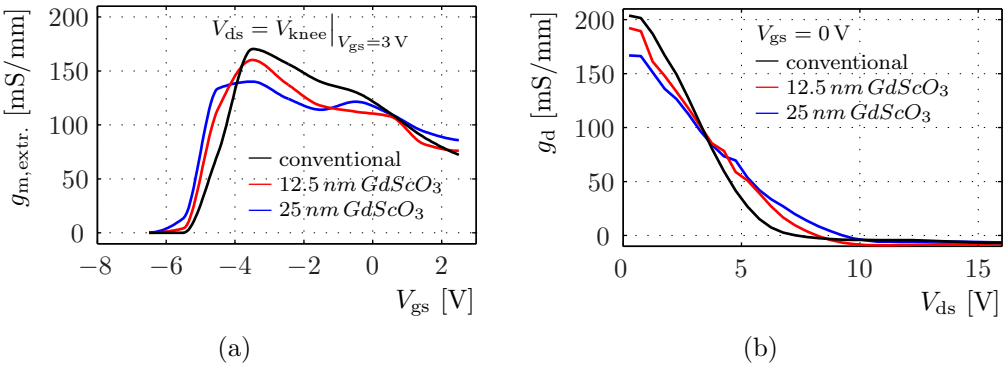


Figure 9.5: Transconductance (g_m) (a) and Output conductance (g_d) (b) of a conventional HFET and 12.5 nm and 25 nm $GdScO_3$ MISHFETs.

the contact-pads were coated by a thin $GdScO_3$-layer. Because of difficulties to wet-etch $GdScO_3$, the thin but insulating layer was tolerated - it is usually sufficient to scratch the contact needle through this layer to contact the metal pads of the drain, source, and gate electrodes. Nevertheless, an imperfect contact to the pads might be the reason for the observed decrease of $g_{d,max}$ of the MISHFETs.

Pulsed IV Measurements During the above discussion it was already noticed that $GdScO_3$ does not yield passivation effects: Neither does n_s increase if $GdScO_3$ is deposited (CV measurement), nor is an increased $I_{d,max}$ value noticeable (DC measurement). Within this context, pulsed IV measurements were performed, since it is a standard means to detect trap-related effects and thus can help to identify passivation mechanisms that mitigate the trap-related effects.

Figures 9.6(a) and 9.6(b) illustrate the results gained from pulsed IV measurements of a conventional HFET ($d_{ds} = 4\,\mu m$, $L_g = 0.9\,\mu m$) and a 25 nm $GdScO_3$ MISHFET ($d_{ds} = 3\,\mu m$, $L_g = 0.7\,\mu m$), respectively.

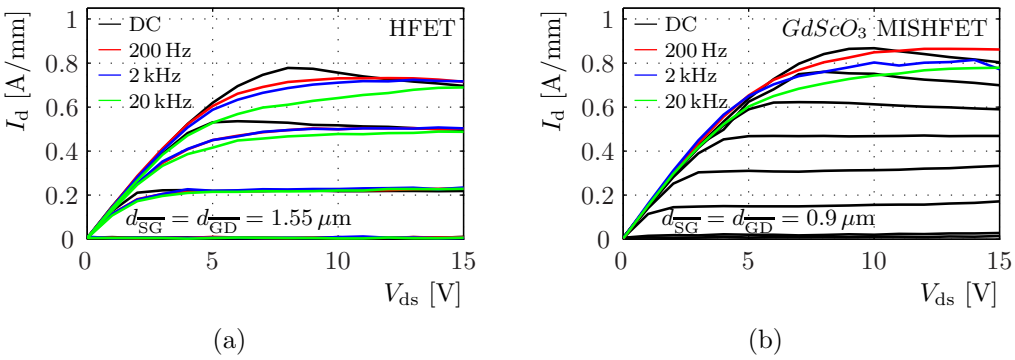


Figure 9.6: Pulsed IV measurement of conventional HFET (a) and a 25 nm $GdScO_3$ MISHFET (b).

The results concerning the HFET reveal, that the drain current decreases with increasing frequency of the pulses. This is a typical indication for the existence of trapping states [147]. Considering the results for the MISHFET, the same tendency is noticeable. Thus, it can be concluded that the deposition of $GdScO_3$ on top of the semiconductor surface does not contribute to a mitigation of trap-related effects. In other words, pulsed IV measurements confirm the previous finding that $GdScO_3$ can not be attributed any passivation effects.

Breakdown Measurements So far, the MISHFETs were characterized by means that operate the device at moderate operational conditions. For instance, DC measurements were conducted up to $V_{ds} = 20\,V$ and Load-Pull measurements used $V_{ds} = 25\,V$ at maximum. But one of the major advantages of GaN-based transistors is that they can be operated at very high voltages. To give a rough indication whether the $GdScO_3$-insulated devices can compete with conventional devices in the above sense, breakdown measurements were conducted.

In the case of devices with undoped AlGaN layer, the conventional HFET had an off-state breakdown voltage (V_{break}^{off}) between 75 V and 85 V. And for the MISHFETs, V_{break}^{off} was between 26 V and 29 V. For the Si-doped devices, V_{break}^{off} was around 93 V and 29 V for the conventional HFET and the MISHFET, respectively. The plots of the measurement results are depicted in figures 9.7(a) and 9.7(b) for the doped and undoped case, respectively.

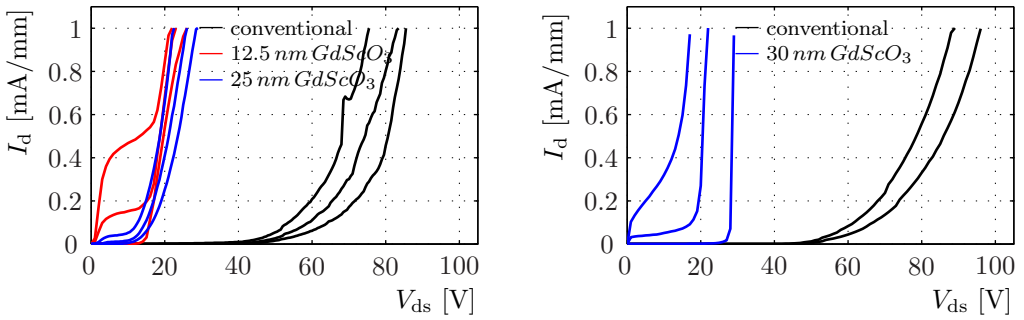


Figure 9.7: Off-state breakdown voltage (V_{break}^{off}) of undoped (a) and doped $GdScO_3$ MISHFETs (b).

The results reveal a great difference in high-voltage performance between MISHFET and HFET. Although the V_{break}^{off} values of the conventional devices are remarkably high for transistors not optimized for high-voltage operation (e.g. by applying the field plate technology), and despite the fact that the achieved MISHFET results are comparable to V_{break}^{off} values of HFETs fabricated at the IBN in recent years (Al_2O_3 substrates, comparable GaN/AlGaN structure and geometry [59]), the significant relative reduction is unacceptably high.

At this point, one can only speculate about the causes of the early breakdown mecha-

nisms in the $GdScO_3$ MISHFETs. It is known that crystalline layers suffer from a high concentration of bulk defects which limit the breakdown field. In this respect, amorphous dielectrics in general have fewer defects and thus withstand higher fields before breakdown [42]. It needs to be confirmed, that the annealing conditions were not such that the formally amorphous insulation layer has not (partially) changed its phase. Further investigations of this issue are mandatory to realize the good insulation and dielectric properties of $GdScO_3$ also for devices operated at high-voltages

S-Parameter Measurements S-parameter measurements were conducted to characterize the RF small signal properties of the MISHFETs relative to the reference HFET. Only the devices based on undoped material are considered. The cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}) were evaluated for devices with gate lengths from 300 nm to 900 nm for two working points. The tendencies of f_T and f_{max} with increasing L_g is best illustrated in figures 9.8(a) and 9.8(b), respectively. Important data is listed in table 9.3 to be used in the following discussion.

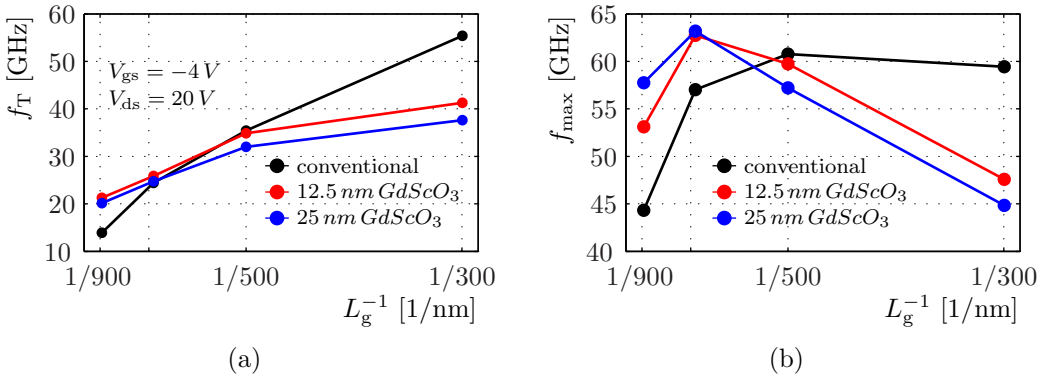


Figure 9.8: Cut-off frequency (f_T) (a) and maximum oscillating frequency (f_{max}) (b) of a conventional HFET and 12.5 nm and 25 nm $GdScO_3$ MISHFETs at $V_{gs} = -4$ V and $V_{ds} = 20$ V.

	$L_g = 500$ nm		$L_g = 700$ nm		$L_g = 900$ nm	
Sample ID	f_T	f_{max}	f_T	f_{max}	f_T	f_{max}
Z10 (ref.)	35.4 GHz	60.8 GHz	24 GHz	57 GHz	13.9 GHz	44.3 GHz
Z11 (12.5 nm)	−2 %	−1 %	+3 %	+11 %	+58 %	+20 %
Z03 (25 nm)	−10 %	−6 %	+8 %	+11 %	+45 %	+30 %

Table 9.3: Results of S-parameter measurements of $GdScO_3$ MISHDiodes. The % values indicate an increase (+) or decrease (-) relative to the value of the reference HDiode.

As is apparent from figure 9.8(a), the data points of the three device types can all be fitted well to a linear function, indicating that the common relation $f_T \propto \frac{1}{L_g}$ holds true. The slope of the linear fitting functions for the MISHFET data is smaller than that for

the conventional device. This can be explained by a lower saturation velocity of the electrons in the 2DEG for the MISHFETs. Apparently, the deposition of $GdScO_3$ has an impact on the properties of the spatially separated 2DEG. Nevertheless, the absolute f_T values of the MIS devices are promising. For $L_g = 900\,nm$, the MISHFETs have even significantly higher f_T values.

To judge the RF properties of a transistor to be used as a power-amplifying device, the attention needs to be drawn to f_{max}. Among other factors, f_{max} is mainly determined by f_T and the gate resistance (R_g) (see section 5.4). An increasing f_T will increase f_{max}, and the higher R_g, the smaller f_{max} will be. Assuming a rectangular cross-section of the gate, a reduction of L_g goes along with an increase of R_g, thus a shorter gate length will contribute to a f_{max} decrease (in devices optimized for highest frequencies, this dilemma is circumvented by "T"-shaped cross-sections).

The f_{max}-over-$1/L_g$ curves in figure 9.8(b) can now be explained as follows: For $L_g = 900\,nm$, the f_T values of the MISHFETs are higher than for the reference device, so is f_{max}. For long gate lengths, the f_{max}-limiting influence of R_g can be neglected. But with decreasing L_g the negative influence of R_d becomes dominant: for the MISHFET this "turn-around" can be already observed for L_g 500nm, whereas for the conventional device the R_g effect is dominant at a smaller L_g of 300 nm.

From a practical point of view, figure 9.8(b) can be interpreted as follows: Using a $GdScO_3$ insulation layer, the resulting MISHFETs can be used for amplification purposes at higher frequencies (63.2 GHz) than a conventional HFETs could (60.8 GHz). And in addition, this can be accomplished with an even larger gate length (700 nm versus 500 nm).

Load-Pull Measurements All Load-Pull measurements which will be described below have been performed under matched in- and output conditions at an oscillating frequency of 7.5 GHz. The following comparisons all refer to measurements performed at $V_{ds} = 25\,V$, $V_{ds} = -3\,V$, operated in class-A mode.

Concerning the output power (P_{out}), a value of 25.19 dBm was measured for the conventional HFET. For the 12.5 nm $GdScO_3$ MISHFET, P_{out} was +3.58 dB higher, the 25 nm $GdScO_3$ device showed an improvement of +3.34 dBm. The power gain of the conventional device was 11.21 dB at maximum, whereas for the 12.5 nm and the 25 nm $GdScO_3$ MISHFETs the gain was 44 % and 31 % higher, respectively. With regard to the power added efficiency, $\eta_{PAE} = 14\,\%$ was measured for the conventional HFET. For the 12.5 nm $GdScO_3$ MISHFET, η_{PAE} was 41.47 %, the 25 nm $GdScO_3$ device showed an η_{PAE} of 36.58 %. Figure 9.9 illustrates the results of the Load-Pull measurements.

According to equation 5.27, a P_{out}-increase is due to an increased saturated drain current ($I_{d,sat}$) and/or an increased breakthrough voltage (V_{break}). With respect to $I_{d,sat}$, the different device types show similar behavior, in particular this is due to the lacking passivation effect for $GdScO_3$. A difference in V_{break} can neither be made responsible for the observed P_{out} increase of the $GdScO_3$-devices, since the measurement results were all gained at (nearly) identical bias conditions.

But the increase in P_{out} can be explained by the impact a dielectric layer can have on the

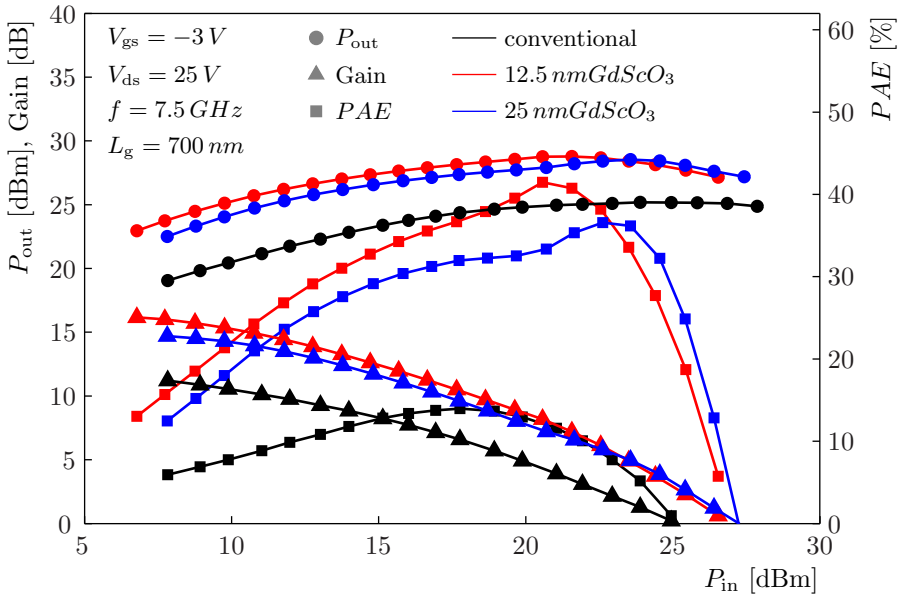


Figure 9.9: RF power performance of conventional HFET, 12.5 nm and 25 nm $GdScO_3$ MISHFETs at optimal V_{gs} (-3 V for each) and constant $V_{ds} = 25$ V. Maximum P_{out} is nearly double as high for MISHFET compared to conventional HFET, significant η_{PAE} increase for $GdScO_3$ MISHFETs.

gain, as was suggested in section 5.5: If the dielectric layer is highly insulating, the power provided at the device input (P_{in}) translates to a higher input voltage swing compared to a conventional device. Assuming that the transconductance (g_m) for both device types is of the same order, this will cause the drain current swing (ΔI_d) and drain-source voltage swing (ΔV_{ds}) to be increased, thus P_{out} will be higher as well, being proportional to ΔI_d and ΔV_{ds}.

The η_{PAE}-increase can be explained by using equation 5.30. The η_{PAE} increases with increasing η and $Gain$. As has been shown above, the introduction of a dielectric layer has beneficial impact on the $Gain$, and due to the reduction of the input currents, P^{DC} reduces, thus η increases. Thus, $GdScO_3$ insulation increases the ability of the transistor to deliver output power by a factor of two and increases the η_{PAE} significantly.

Summary

The experiment showed that the $GdScO_3$ MISHDiode-related findings from the previous chapters hold true for MISHFETs as well. In particular, using $GdScO_3$ as a gate dielectric is suitable to reduce the gate current significantly (up to six orders of magnitude) and to limit the drop of input capacitance common to MISHFETs (up to 50 % for SiO_2 insulators) to only a small loss (approximately 10 %). Due to the improved input capacitance, the MISHFET reaches the off-state at a gate source voltage only slightly higher than in the conventional case.

Since the output current is similar as in the conventional case, any passivation effect can

not be attributed to $GdScO_3$. Unchanged drain current and a slightly higher threshold voltage are also reflected by a transconductance that is only 10 % smaller than for a conventional HFET.

Although $GdScO_3$ does not passivate the semiconducting surface, it has a beneficial effect on the mobility of the charge carriers. Important RF properties like f_T and f_{max} are well improved and fulfil the expectations that are based on the higher g_m/C_{gs} ratio. As one of the most important results, the RF power output is more than doubled by the use of $GdScO_3$ as dielectric layer in MISHFETs, compared to the HFET.

Chapter 10

Hafnium Dioxide Transistors

After $GdScO_3$ was shown to be a suitable dielectric for GaN-based MISHFETs in the previous chapter, the attention is drawn to another potential dielectric in the following. Hafnium Dioxide (HfO_2) is one of the promising high-κ materials that might substitute SiO_2 in Si-based CMOS technology in the near future. Due to the high dielectric constant of HfO_2, which can be up to 25 % higher than for $GdScO_3$ [119, 50], it might serve as a dielectric for GaN-based MISHFETs as well. Although the first-order estimation of the band offsets of HfO_2 relative to GaN and AlGaN is not as promising as for $GdScO_3$ (see section 4.2), MISHFETs and HDiodes were fabricated to make sure not to miss out an interesting alternative.

Experiment

The material utilized for the experiment consisted of a GaN buffer layer with a 30 nm $Al_{0.3}Ga_{0.7}N$ film on top, grown on a SiC substrate by metal-organic vapor-phase epitaxy (MOVPE). By means of standard technology described in appendix A.3, square diodes and transistors were fabricated.

The diodes had square Schottky electrodes of sizes ranging from $0.625 \cdot 10^{-9}$ m to $40 \cdot 10^{-9}$ m. The transistors had varying gate lengths (L_g) from 0.3 μm to 2 μm. The used gate widths (W_g) were 100 μm and 200 μm. For the gates, a two-finger configuration was chosen. The distance between source and drain electrodes ranged from 2 μm to 4 μm.

The gate oxide of the fabricated MISHFETs was deposited by chemical vapor deposition (CVD) and had a nominal thickness ($d_{\mathrm{CVD}}^{\mathrm{insul}}$) of 5 nm. After deposition, the layer was annealed ex-situ at 700 °C for 10 min in nitrogen atmosphere by means of a rapid thermal annealing (RTP) oven. Conventionally processed devices without dielectric layer were processed to serve as a reference.

The devices were characterized electrically utilizing IV, CV, and DC measurements as described in appendix B.

Results and Discussion

Input Characteristic The gate-source capacitance (C_p) measured for a conventional HDiode was 3 mF/mm, for the MISHDiode the value was 3 % lower, which corresponds to an effective insulator thickness ($d_\mathrm{CV}^\mathrm{insul}$) of 2 nm if a dielectric constant of 23 is assumed. The threshold voltage (V_th) of the conventional device was −3.3 V, the MISHDiode had an absolute V_th value which was 9 % higher. Figure 10.1(a) illustrates the CV results. The sheet carrier concentration (n_s) extracted from the CV curves was $5.3 \cdot 10^{12}$ cm^{-2}, whereas the n_s value for the MIS device was 7 % higher.

The evaluated $d_\mathrm{CV}^\mathrm{insul}$ value deviated from the intended thickness $d_\mathrm{CVD}^\mathrm{insul}$ of 5 nm. The small insulating thickness in combination with the high dielectric constant yield a theoretical $C_\mathrm{p}/C_\mathrm{p}^\mathrm{HFET}$ ratio that is very close to unity. Thus, one might argue that such small dielectric layers can not be measured by means of CV measurements in principal. But the identified increase of n_s is a reliable indication that in fact a dielectric layer with passivation effect was deposited - which is also confirmed by Hall measurements and a higher drain current as discussed later. Thus it can be concluded that although deposition technology needs to be further optimized, a MIS device benefits from the high permittivity of HfO_2 in terms of an increase of the total capacitance.

The current-voltage (IV) measurements - illustrated in figure 10.1(b) - revealed a reverse gate leakage current ($I_\mathrm{max}^\mathrm{rev}$) of 1 μA for the conventional HDiode. For the HfO_2 device, $I_\mathrm{max}^\mathrm{rev}$ was reduced by one to two orders of magnitude. In the positive voltage regime, the IV curve indicates Schottky behavior for both device types.

Although the thickness of the insulation layer was extremely thin, the current reducing effect was clearly visible. Nevertheless, the leakage reduction of a SiO_2 device with a similarly thin dielectric layer proved to yield a more effective isolation (nearly three orders of magnitude, see section 6.2). It needs to be mentioned though, that the post-deposition annealing of the HfO_2 layer was not optimized. But from chapter 7 it is known that, post-deposition annealing is a crucial step for reaching good insulating properties. Thus, an optimization of the annealing parameters might further increase the insulating properties.

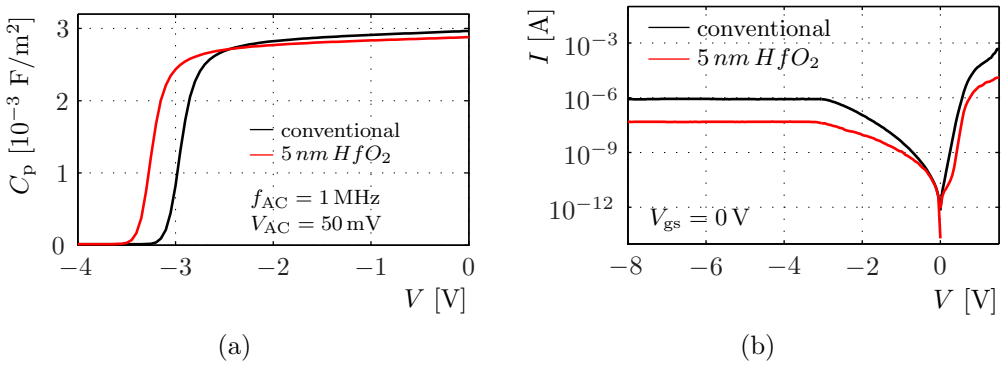
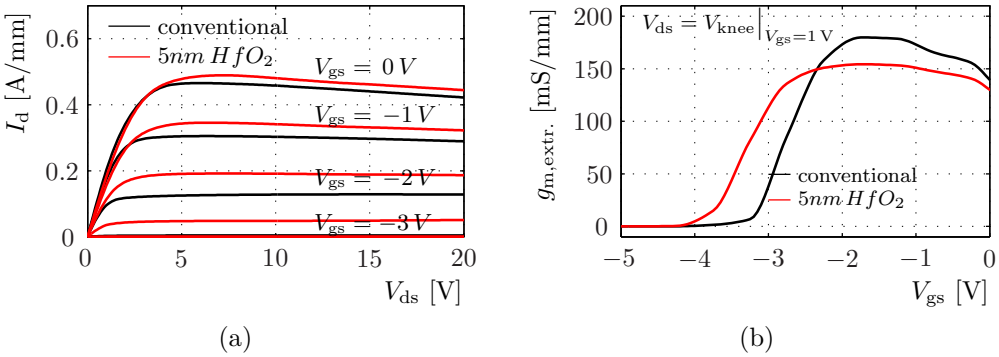


Figure 10.1: Leakage current (I) over bias (a) and capacitance (C_p) over bias (b) of a conventional HDiode and a 5 nm HfO_2 MISHDiode.

Output Characteristic The maximum drain current of the conventional device was 0.46 A/mm, the corresponding value of a MISHFET with identical geometry was 7 % higher. Figure 10.2(a) illustrates the output characteristic. The transconductance (g_m) was 179 mS/mm for the HFET, and for the HfO_2 device it was 14 % smaller. As can be seen from figure 10.2(b), the differences in V_{th} match with the V_{th} differences revealed by CV measurements.

The results indicate that the n_s increase detected by CV measurements effectively yields a higher drain current. It is likely, that both passivation of the active and the access region of the device contribute to the increase of drain current, as was shown in section 6.1. Thus, similar to SiO_2 devices and in contrast to $GdScO_3$ devices, HfO_2 can be attributed a passivation effect. The relative difference in C_p and g_m, 3 % and 14 %, respectively, indicate that for the HfO_2 device improved RF properties in terms of f_T and f_{max} can be expected.



(a) (b)

Figure 10.2: Output Characteristic (a) and transconductance (g_m) (b) of a conventional HFET and of a 5 nm HfO_2 MISHFET.

Summary

In summary, the experiment with HfO_2 MISHFETs showed only a moderate insulating effect if HfO_2 is incorporated into MISHFETs. In this sense, the pessimistic results of the first-order estimations of the band offsets (section 4.2) were confirmed empirically.

On the other hand it needs to be noted, that the deposited layer was extremely thin and that the annealing parameters - which has shown to be crucial for the insulating properties of $GdScO_3$ - were not optimized. Thus, an improvement of deposition technology and an optimization of the annealing parameters might improve the insulating properties of HfO_2 MISHFETs.

But at this point it appears unlikely that HfO_2 has the potential to outperform $GdScO_3$ for being used as gate dielectric in GaN-based MISHFETs. This becomes even more true since an additional passivation effect of HfO_2 is noticeable but too small to make up the inferior insulation properties of HfO_2 on GaN.

Chapter 11

Comparison of Gate Dielectrics

In this chapter, the main findings of the experiments with SiO_2 and $GdScO_3$ gate dielectrics will be compared. Since the devices to be compared were neither processed at the same time nor were they fabricated on identical layer structures, the absolute values of the measured quantities will most likely differ. Therefore, the performance of the MIS devices relative to their simultaneously fabricated reference devices will be compared.

Capacitance increase in heterostructure diodes Figure 11.1(a) illustrates the capacitance (C_p) of a MISHDiode normalized to the capacitance of a reference HDiode (C_p^{HFET}) for SiO_2 and $GdScO_3$ devices. Due to the high-κ property, the $GdScO_3$ HDiodes yield much better results: For an effective insulator thickness of 12 nm a $C_\mathrm{p}/C_\mathrm{p}^{HFET}$ ratio of 85 % was reached compared to 50 % for the SiO_2 HDiode. A dashed line was added to the respective data points to guide the eye. Following that line to smaller d^insul values it becomes apparent that there is still room for an C_p increase for $GdScO_3$ devices.

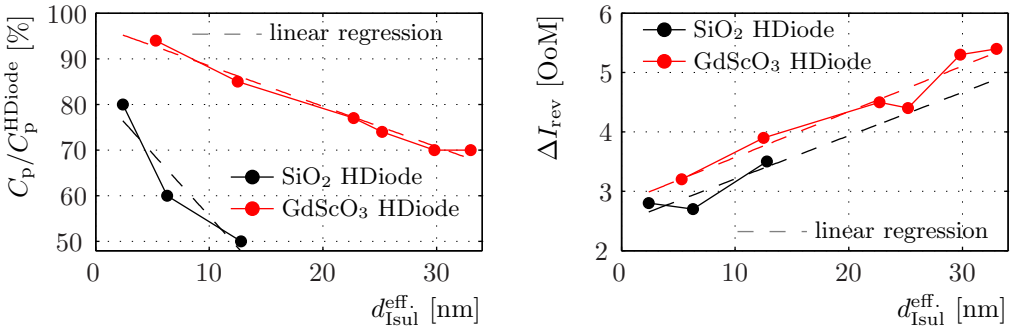


Figure 11.1: Comparison of capacitance ($C_\mathrm{p}/C_\mathrm{p}^\mathrm{HFET}$) (a), and reverse current reduction (ΔI_rev) (b) of SiO_2 and $GdScO_3$ MISHDiode for various effective insulator thicknesses (d^insul).

Leakage current reduction in heterostructure diodes To compare the insulating properties of SiO_2 and $GdScO_3$ utilized as insulation layer in MISHDiodes, the leakage reductions reached for various effective insulator thicknesses ($d_{\mathrm{CV}}^{\mathrm{insul}}$) are plotted in figure 11.1(b). As unit, "orders of magnitude (OoM)" was chosen. The dashed line, which represents a linear least squares fit, suggests that $GdScO_3$ yields a current reduction half an order of magnitude higher than SiO_2. And due to the superior dielectric properties of $GdScO_3$ - as discussed in the former paragraph - much thicker $GdScO_3$ layers can be used in MIS devices compared to SiO_2. Thus, utilizing $GdScO_3$ as a gate dielectric in MISHFETs, a much lower gate leakage current can be expected compared to SiO_2 MISHFETs.

Output characteristic of MISHFETs To discuss the differences in the DC output characteristics of SiO_2 and $GdScO_3$ MISHFETs, the impact of the insulating material on the sheet carrier concentration (n_{s}) and the threshold voltage (V_{th}) is considered in the following.

Figure 11.2(a) illustrates the dependence of n_{s} on d^{insul}. Apparently, with increasing thickness of the SiO_2 layer, the n_{s} values rise, which is due to passivation effects. On the other hand, the deposition of $GdScO_3$ does not have a significant effect on n_{s}. As a consequence, the drain currents of the SiO_2 MISHFETs rise significantly, whereas the maximum drain current for $GdScO_3$ devices remains more or less unchanged compared to the conventional HFET.

The other major factor to describe the output characteristics, V_{th}, is difficult to compare: A device with higher n_{s} results in a higher V_{th} - regardless of the V_{th} change related to other influences. Since the n_{s} values differ for the different materials and thicknesses, the exact cause for a V_{th} change can not be identified with the data available. But despite the problem of a quantitative analysis, the tendency is clearly observable. Due to the gate-source capacitance, a significantly smaller voltage needs to be applied to pinch-off the device in the $GdScO_3$ case compared to the case of SiO_2.

Thus, SiO_2 improves the output characteristic of a MISHFET by contributing to a higher drain currents (passivation effect), whereas $GdScO_3$ improves the output characteristic by a significantly smaller V_{th}.

RF small signal performance of MISHFETs Results of S-parameter measurements form the basis for a comparison of the influences of the alternative dielectrics on the RF performance. But due to the many parameter that have to match (layer structure, geometry, working point) comparable results were not available for a thorough comparison of f_{max} values.

Figure 11.2(b) illustrates the differences in f_{T} achieved for SiO_2 and $GdScO_3$ MISHFETs relative to their conventional counterparts. Apparently, the SiO_2 devices outperform the reference HFET for all gate lengths (L_{g}) values, whereas the $GdScO_3$ MISHFET shows only higher f_{T} values than the reference at $L_{\mathrm{g}} = 900\,\mathrm{nm}$. From this one can conclude that SiO_2 is more promising regarding a RF performance increase. But the discussion of f_{T} and f_{max} in section 9 has shown, that f_{T} is only a limited indicator for the improvement

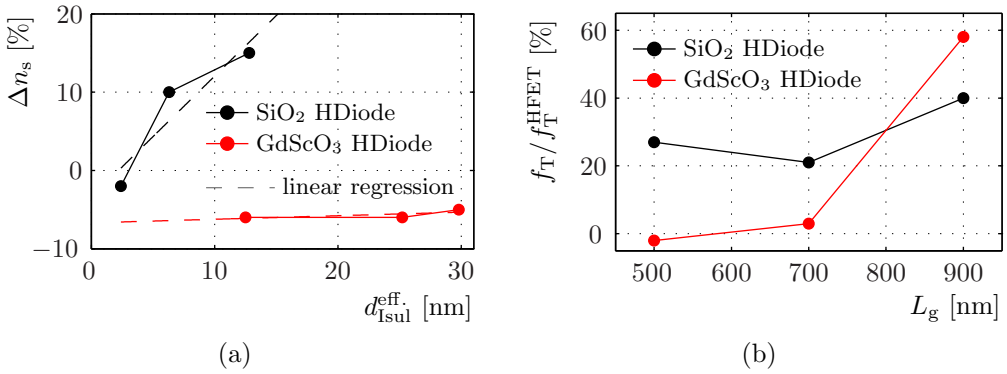


Figure 11.2: Comparison of sheet carrier concentration increase (Δn_s) for various effective insulator thicknesses (d^{insul}) (a) and increase of cut-off frequency (f_T) for various gate lengths (L_g) (b) of SiO_2 and $GdScO_3$ MISHFETs.

of the RF performance for devices dedicated to power amplification purposes.

RF large signal performance of MISHFETs The major conclusion to be drawn from the conducted experiments is illustrated in figure 11.3: The increase in RF output power (P_{out}) for a $GdScO_3$ MISHFET relative to a conventional HFET is higher (+133 %) than for a SiO_2 device (+99 %). Thus, $GdScO_3$ is a promising alternative to be utilized in MISHFETs for high-power amplifiers.

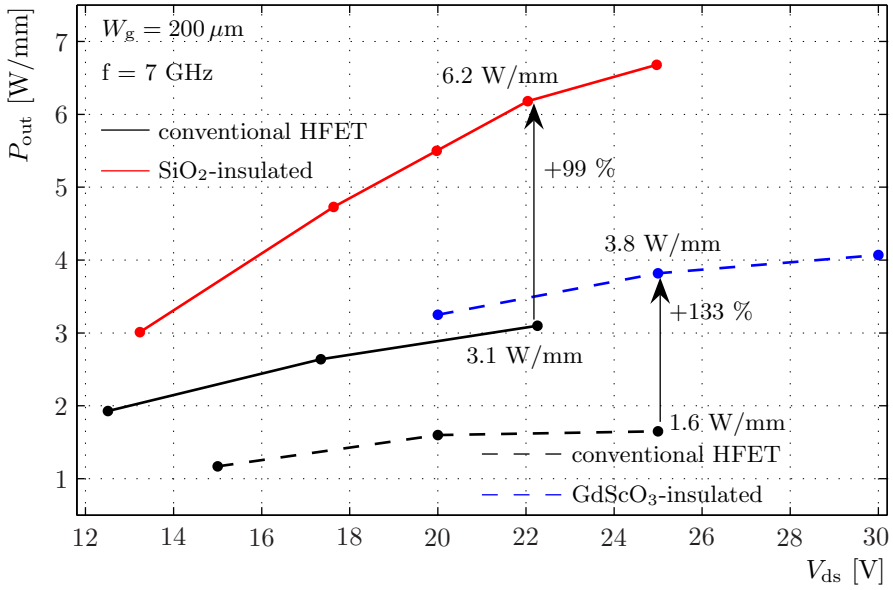


Figure 11.3: Comparison of RF output power (P_{out}) of SiO_2 and $GdScO_3$ MISHFETs.

Chapter 12

Conclusions and Outlook

In the following, the conclusion drawn from the various experiments presented in the experimental part of this thesis will be summarized. Then, an outlook will be given to the tasks yet to be accomplished. But first of all, the major prerequisites will be summarized briefly that enabled the experiments.

The first prerequisite was to establish a suitable technology. The existing processing technology for GaN/AlGaN devices on Al_2O_3 and SiC substrates was modified and expanded to fabricate MISHFETs. In particular, the integration of gate insulation layers as SiO_2, $GdScO_3$, and HfO_2 was accomplished, utilizing Plasma enhanced chemical vapor deposition (PECVD) for SiO_2, electron-beam evaporation (EBE), and chemical vapor deposition (CVD) for HfO_2.

The expansion of the available means and methods for electrical characterization was the second prerequisite. A setup to measure low currents through insulators was established and the impedance spectroscopy method was implemented as a means to extract capacitance, conductance, sheet resistance, sheet carrier concentration and carrier mobility by a single measurement.

The very first experiment included the fabrication of SiO_2-insulated MISHFETs and SiO_2-passivated HFETs. The MISHFET devices delivered a high output power densities of 6.2 W/mm at 7.5 GHz and were comparable with state-of-the-art SiO_2 MISHFETs. The comparative study showed, that the performance increase observed for MISHFETs can be partly explained by passivation effects.

Surface passivation prevents current to flow via the surface and thus contributes to the gate leakage reduction. Furthermore, passivation increases the sheet carrier concentration and thus raises the drain current and the output power level. But a principal drawback of MISHFETs became apparent as well. The incorporated insulation layer acts as an additional capacitance and thus decreases the gate source capacitance of the transistor, resulting in a loss of channel control.

In a further study, the thickness of a SiO_2 insulation layer was successfully reduced, yielding devices with an improved channel control. The experiments showed that a down-scaling of the SiO_2 insulator thickness is well feasible - reaching layer thicknesses down to 2.4 nm. It also turned out, that the passivation effect of SiO_2 on AlGaN is

dependent on the SiO_2 thickness - at least for thicknesses between 2 nm and 12 nm.

In parallel to the SiO_2-related experiments, pre-studies with $GdScO_3$ were performed. The major finding of this study was that post-deposition annealing of $GdScO_3$ in an oxygen atmosphere is crucial to achieve electrically dense layers. It showed, that a simple variation of temperature is not sufficient to reach high insulation properties.

The first experiments with Gadolinium Scandate Diodes revealed that the current reductions reached with $GdScO_3$ are closely related with the insulator thickness over a wide range of thicknesses ($3\,\text{nm} < d^{\text{insul}} < 33\,\text{nm}$). With the gained knowledge, first $GdScO_3$ heterojunction diodes (HDiode) were fabricated with various GaN/AlGaN layer structures on Al_2O_3 and SiC substrates. These devices helped to gain insight into the material properties of $GdScO_3$, as described in the following.

It could be observed, that $GdScO_3$ HDiodes show a CV hysteresis after a positive bias stress had been applied. This phenomenon was investigated in detail. In particular, relaxation time constants after positive bias stress (1 h), and after UV illumination (1 min) were determined; the traps were found to be located within the $GdScO_3$ film, not at the interface; the trap density was estimated to approximately $1 \cdot 10^{18}$ cm^{-3}; and the electronic states are likely distributed over the $GdScO_3$ band gap of 5.5 eV.

After having gained experience with $GdScO_3$, MISHFETs were fabricated for the first time. The devices fulfilled many expectations: a gate leakage reduction of around 6 orders of magnitude was reached, the drop of gate source capacitance was minimized, a potential usage at frequencies up to 60 GHz was shown, and the RF output power density was increased by 133 % compared to a conventional HFET. Despite one major drawback - the MISHFETs showed a relatively low breakdown voltage of around 30 V - the $GdScO_3$ MISHFETs proved to be a promising device for high power amplification purposes at high frequencies.

In a parallel study, HfO_2 MISHFETs were processed and characterized. The gate source capacitance was almost as good as for the conventional device, which was due to the high dielectric constant of 23 and due to the extremely thin insulation layer. But devices showed only a moderate insulation property - comparable to that which was also reached by SiO_2 devices. This empirical finding was also confirmed with theoretical considerations of the energyband alignment at a HfO_2/AlGaN interface, predicting a conductance band offset of only 0.58 eV. Therefore, HfO_2 was not considered a potential candidate for MISHFETs any more.

Finally, the comparison of the gate dielectrics SiO_2 and $GdScO_3$ showed, that a) the higher dielectric constant of $GdScO_3$ results in an improvement of the MISHFET channel control, b) SiO_2 benefits to a large extend from the surface passivation effect (higher drain currents, higher output power level), c) $GdScO_3$ reduces the leakage current five times better than SiO_2, d) $GdScO_3$ yields an even better output power increase than SiO_2, e) both SiO_2 and $GdScO_3$ MISHFETs suffer from a low breakdown voltage of approximately 30 V.

Outlook

The experiments conducted within this work have shown that the $GdScO_3$ MISHFET is a promising device to be used in high-power applications operated at high frequencies. Nevertheless, there are important issues which necessitate further investigations.

The most obvious weakness of the $GdScO_3$ (and also the SiO_2) MISHFETs is the early breakdown at voltages around 30 V, which is likely due to technological issues. A thorough investigation of the causes - e.g. by investigating the gate leakage mechanisms - might help to find ways to improve the breakdown characteristic.

The difficulties experienced during the deposition of the dielectric layers, in particular the difference between intended and effective thicknesses, is likely due to fact that ohmic contacts have already been processed. Rearranging of process steps, i.e. deposition of gate insulators before processing, yields other problems, e.g. precise etching of the dielectric material. Either way, the actually applied technology leaves plenty of room for optimization.

Although the results gained from the experiment with HfO_2 MISHFETs were not as promising, it is worth trying to optimize the annealing parameters for HfO_2 to increase the insulation property of HfO_2 MISHFETs. The experiences gathered from the studies of the post-deposition annealing conditions of $GdScO_3$ show, that this issue is crucial to achieve electrically dense dielectric layers.

Appendix

Appendix A

Processing Technology

This chapter documents the development of a technology to process MISHFETs, which incorporates gate oxides as SiO_2, $GdScO_3$, and HfO_2. A technology to process HFETs based on GaN/AlGaN-layers has been developed at the IBN within the last years. The task of this work is to expand the existing technology by elements specific to the novel dielectrics.

These specific tasks comprise in particular the deposition, which will be covered in section A.1. Furthermore, it turned out that the electron-beam lithography process had to be adjusted if gates were to be placed on top of the oxides. The work accomplished in this respect is documented in section A.2.

For the different oxides, the starting point for the development of deposition, etching, and electron-beam lithography in the context of GaN devices differed strongly. Regarding SiO_2, quite a few articles were published which describe technological aspects of fabricating SiO_2 MISHFETs. Moreover, the first SiO_2 devices fabricated at the IBN were processed by Juraj Bérnat, the predecessor of the author. Thus, the task was to expand and to optimize the SiO_2-related technology already established at the IBN.

In contrast to SiO_2, hardly any experience was available concerning the handling of $GdScO_3$. Although rare-earth scandates were suggested to be used in Si-based systems by some authors [50, 143, 144], there were not any devices fabricated yet. Least of all were there any attempts to incorporate ternary scandates into GaN-based devices. Thus, a technology to fabricate $GdScO_3$ MIS devices on a GaN basis had to developed from scratch.

In principle, the same as for the rare-earth scandates holds true for HfO_2. Although HfO_2 MOSFETs on a Si basis will be commercially available soon, there is not any documentation available on how to fabricate GaN-based HfO_2 MISHFETs. But as is reported in chapter 10, the results achieved with HfO_2 were not as promising, so only the very basic aspects of the developed technology will be documented in this chapter.

Following the discussion of deposition, etching and electron-beam lithography, section A.3 will present the entire process to fabricate MISHFETs. This will merge the technological knowledge of my predecessors and the knowledge gained within this work.

A.1 Deposition of Gate Dielectrics

Silicon Dioxide

Technology To deposit SiO_2, Plasma Enhanced Chemical Vapor Deposition (PECVD) is chosen. This deposition technique is a Chemical Vapor Deposition (CVD) process that utilizes a plasma to enhance chemical reaction rates of the precursors and thus operates at lower temperatures. In the CVD processes used in this work, the sample is exposed to the volatile precursors dichlorosilane ($SiCl_2H_2$) and nitrous oxide (N_2O), which react and decompose on the sample surface to produce the desired deposit. The volatile byproducts that are produced are removed by a H_2 gas flowing through the reaction chamber. The chemical equation for the above processes is:

$$SiCl_2H_2 + 2N_2O \quad \rightarrow \quad SiO_2 + 2N_2 + 2HCl.$$

Parameter Optimization As a standard routine, PECVD processes can be run in two modes for SiO_2 deposition, with defined parameters as precursor kind and flow, H_2 flow, temperature, pressure, and RF power. These standard programs needed to be modified to achieve reproducible thin films between 5 nm and 20 nm. In particular, two problems had to be solved: a) The reference growth rate of 8.5 nm/min is valid for 2″-wafers only, thus an adaptation to sizes of $(10\,\mathrm{mm})^2$ had to be made, b) the standard programs aimed at depositing layers with much greater thickness than needed for MISHFETs. Thus, the growth rate has to be reduced to enable the reliable processing of layers between 5 nm and 20 nm thickness.

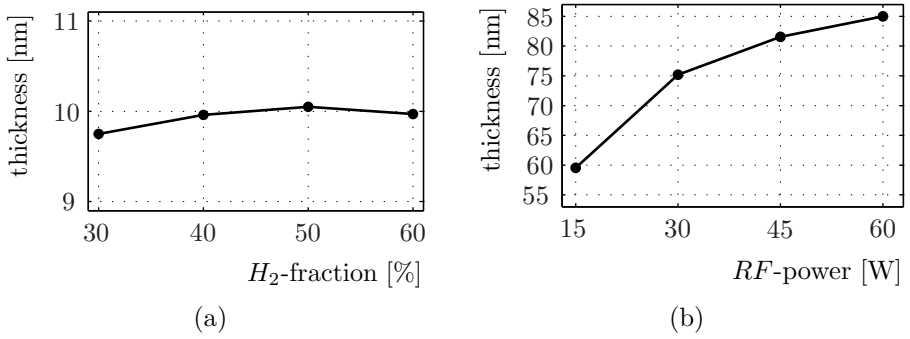
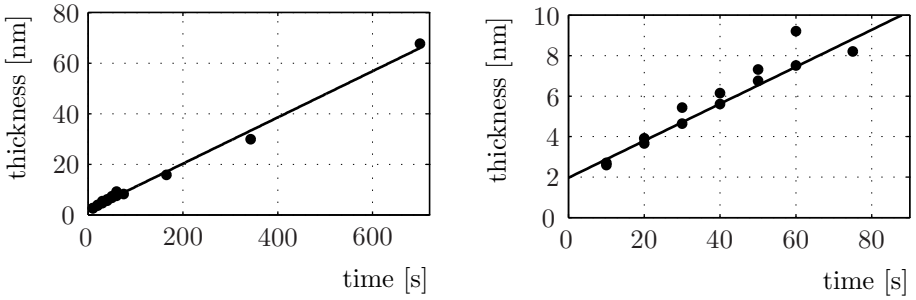


Figure A.1: Optimization of PECVD for thin SiO_2 films on $(10mm)^2$ samples. The Plots show the effect of a variation of RF power (a) and H_2 fraction on SiO_2 thickness (b).

By depositing SiO_2 on cleaned Si samples of $(1\,\mathrm{cm})^2$ size and subsequent measuring of the deposited SiO_2 thickness by means of ellipsometry the impact of H_2 flow and RF power on the SiO_2 growth was examined. Figures A.1(a) and A.1(b) illustrate the results for H_2 flow and RF power variations, respectively. It showed, that varying the H_2 flow did not have significant influence on the deposition rate, whereas RF power was an effective means to reduce the deposition rate by 30 %.

With these results, the deposition rate were determined next: the H_2 flows remained unchanged at 30 % and RF power was set to the lowest value of 15 W. Various deposition processes had been performed with time durations between 10 s and 700 s. The determined thicknesses are plotted against time in figure A.1. A linear regression analysis yields a deposition rate of 5.5 nm/min and an y-offset of 2 nm. The offset can be attributed to a 2 nm thick SiO_2 layer that has formed on the Si wafer surface before starting the PECVD process.



(a) large time scale (b) small time scale

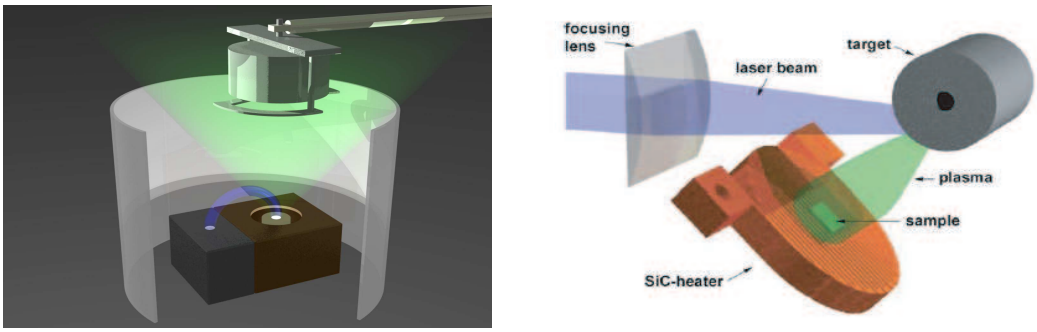
Figure A.2: SiO_2 deposition rates of optimized PECVD on $(10mm)^2$ samples. Process yields stable and linear deposition rates over a wide time span (a), making deposition of films below 10 nm feasible (b). RF power is 15 W.

In summary, a PECVD process was established that enables the stable and accurate deposition of less than 10 nm thick SiO_2 films on samples of $(10\,\mathrm{mm})^2$ size.

Gadolinium Scandate

Several techniques have been utilized to deposit $GdScO_3$ on Si substrates. Electron beam evaporation [143] and pulsed laser deposition [50] processes are well established at the IBN. Electron beam evaporation (EBE) utilizes a conventional deposition chamber which provides high vacuum conditions ($1 - 5 \cdot 10^{-6}$ mbar). For deposition of stoichiometric $GdScO_3$ thin films, a stoichiometric evaporation source is used, which is made from a mixture of the metal oxides. The process temperature depends upon the desired consistency of the layers, in this work temperatures in a range $400-600\,^{\circ}\mathrm{C}$ were used. The duration of the deposition is between $5 - 10$ min. Post-deposition and in-situ annealing in an O_2-atmosphere is the finishing step of the deposition process. For further details concerning the deposition process see [143] and [144]. Figure A.3(a) illustrates the setup.

Pulsed Laser Deposition (PLD) utilizes a KrF excimer laser (wavelength 248 nm, pulse width 20 ns and flounce of 2.5 J/cm^2) which is directed towards a stoichiometric sintered powder cylinder. Two different target-substrate geometries are feasible, the on-axis and the off-axis setup, the former is shown in figure A.3(b). The substrates are heated by a SiC resistive heater, with direct contact in on-axis setup, and radiation heating in off-axis setup. Deposition takes place in an oxygen or nitrogen atmosphere with a pressure of



(a) (b)

Figure A.3: Means to deposit $GdScO_3$. Electron-beam evaporation (provided by M. Roeckerath) (a) and pulsed lased deposition in on-axis geometry [144] (b).

$2 \cdot 10^{-3}$ mbar in on-axis and $1.2 \cdot 10^{-3}$ mbar in off-axis setup. By means of PLD, epitaxial and amorphous $GdScO_3$ and $DyScO_3$ films can be grown on different substrate materials, even in-situ deposition of multi layered films is possible, with the target material being changed during the experiment. For further information see [50].

A.2 Electron Beam Lithography

electron-beam lithography is not a critical issue in standard fabrication of GaN/AlGaN-based HFETs. But when attempting to process MISHFETs, severe difficulties arose performing electron-beam lithography. The utilized oxides, $GdScO_3$ and SiO_2, caused a strong deviation of the electron beam from the intended path by tens of micrometers, although the oxide layers were only a few nanometers thick and located underneath a 600 nm thick polymethyl methacrylate (PMMA) layer. Figure A.4 illustrates the resulting lateral misplacement of the gate structures by up to 30 μm.

This phenomenon - in the following denoted as "floating offset" - was successfully circumvented by using a 15 nm thick Ti metal coating on top of the PMMA layer, deposited by electron beam evaporation. The metal was removed after electron-beam exposure and prior to development by a 10 s dip into a 13.3 % aquatic HF solution.

But it showed, that this modification of the process caused the PMMA layer to crack, and a subsequent formation of short cuts during gate-metal deposition. Optical microscopy revealed the origins of this phenomenon: After the Ti-coated sample has been exposed to the electron-beam the sample surface appears unchanged (figure A.5(a)).

After etching the metal, the surface showed dark and light regions (figure A.5(b)). And after development, the light regions on the surface showed cracks, the dark ones did not (figure A.5(c)). Taking a closer look at a transistor in a dark region reveals a good development result (figure A.5(d)), whereas in a light region cracks can be observed emerging from structural endings (figure A.5(e) and A.5(f)). These cracks can cause short circuits if metal is deposited, as shown in figure A.5(g).

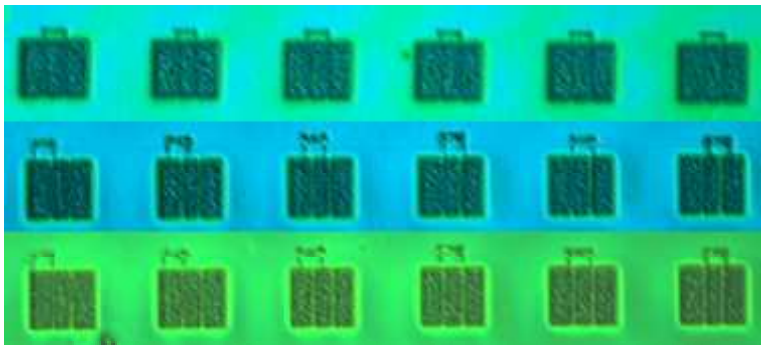


Figure A.4: Deviation of electron-beam due to charging effects. Each row above shows a PMMA-coated sample surface after electron-beam lithography and development. The structure forming a Π (the gate) is written by electron-beam lithography and is supposed to be located relative to the square regions (the ohmic contacts) as in the 1st row, which represents a conventional GaN/AlGaN-structure without insulating layer. For structures coated with $GdScO_3$ (2nd row) and SiO_2 (3rd row), an increasing deviation of the electron-beam pattern along the x-axis can be observed which can be attributed to charging effects.

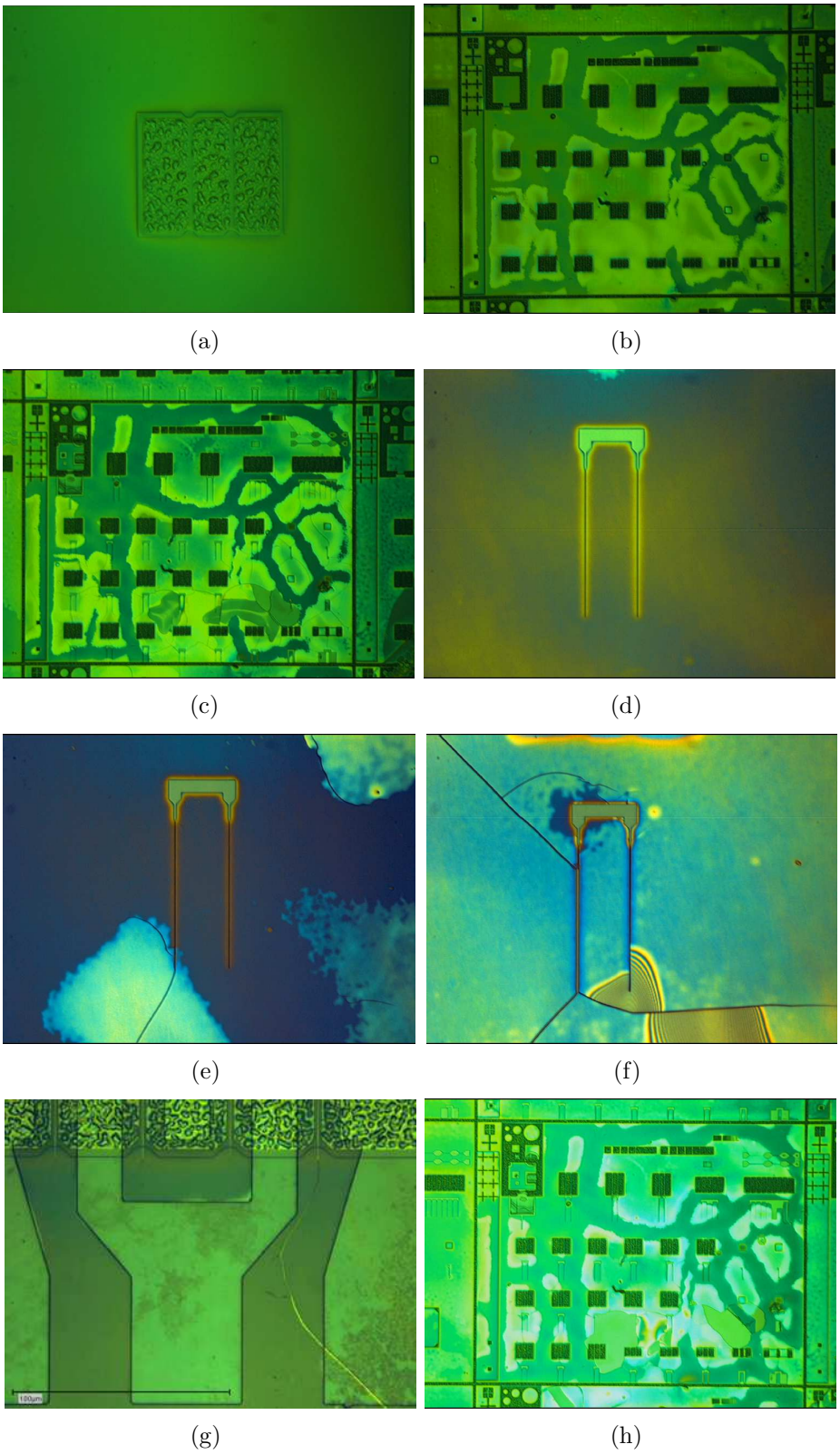
Thus it can be concluded, that at least the PMMA layer has cracked, if not other layers as well. To rule out the possibility that remains of Ti might have cracked, a second HF etch was performed in a 13.3 % aquatic HF solution for 25 s. Since the picture of the optical microscope did not change significantly (figure A.5(h)) one can conclude that Ti has been removed entirely with the first HF etch, thus remaining Ti is not what could have cracked.

To overcome the PMMA cracking problem, two Al_2O_3/GaN/AlGaN samples were prepared to test two alternative modifications of the process before and after electron-beam lithography. That means mesa etching and ohmic contact fabrication were performed, to ensure realistic processing conditions, and a 5 nm $GdScO_3$ layer was deposited by standard electron-beam evaporation.

The process modifications for the first sample included: The PMMA was pre-baked at higher temperature ($T_{\text{bake}} = 200\,^{\circ}\text{C}$) and for a longer time period ($\Delta t_{\text{bake}} = 10\,\text{min}$), the thickness of the Ti layer was reduced by two thirds to 5 nm, and the concentration of the aquatic HF solution was reduced to 4.4 %.

For the second sample, the following modification were chosen: 5 nm Cr instead of Ti to reduce the energies involved in the metal deposition process. To take away the Cr film after electron-beam lithography, commercially available chrome etch is used. As in the experiment with thinned Ti layer, the PMMA layers were baked at higher temperature and for a longer time period to make the structure more dense.

In the next step, electron-beam lithography was performed with a 320 μC/cm^2-dose and utilizing proximity correction. After the metal etching, the samples were developed in AR600-55 for 120 sec. Table A.1 summarizes all samples having been prepared in the context of PMMA cracking.



(a) (b)

(c) (d)

(e) (f)

(g) (h)

Figure A.5: Cracking of PMMA.

Sample	Oxide	T_{bake}	Δt_{bake}	metal	etchant	Δt_{etch}
1	none	180 °C	2 min	15 nm Ti	13.3 % aqu. HF	10 s
2	$GdScO_3$	180 °C	2 min	15 nm Ti	13.3 % aqu. HF	10 s
3	$GdScO_3$	200 °C	10 min	5 nm Ti	4.4 % aqu. HF	10 s
4	$GdScO_3$	200 °C	10 min	5 nm Cr	Cr etch	5 s

Table A.1: Parameter of experiment to circumvent PMMA cracking.

It showed, that samples processed according to the first process modification (Sample No. 3) still suffered from PMMA cracking, but to a much smaller extend than the originally processed samples (Sample No. 2). The samples processed according to the second modified process (Sample No. 4) did not show any PMMA cracking at all.

As an explanation of the PMMA cracking phenomenon consider the following. HF might diffuse through the 600 nm thick PMMA layer and react with the $GdScO_3$, the $GdScO_3$ layers might even be etched away locally. As a consequence the PMMA loosens. The light regions represent areas where PMMA has dissolved from the $GdScO_3$ and where the PMMA layer is under strain. In the darker regions, the PMMA still sticks to the $GdScO_3$. During development the strain distribution is changed in such a way that at structural endings the strain maximizes. As a consequence, cracks form and relieve the strain. The diffusion of HF through the PMMA might be eased by structural defects induced by the deposition of Ti, since evaporation of Ti involves rather high energy portions. This effect can be mitigated by minimizing the Ti thickness or by using Cr which corresponds with smaller kinetic energies when evaporated and deposited.

A.3 Processing Metal-Insulator-Semiconductor Devices

In the following, the standard process to fabricate MISHFETs is described. It is based on the latest GaN-related technology developed at the IBN [17] and incorporates the knowledge gained during the preparatory experiments with insulating materials as documented in the previous sections A.1 and A.2.

In a *preparatory step*, the wafer with the semiconductor layer stack is cut into pieces of $(10\,\text{mm})^2$ or $(12\,\text{mm})^2$. The latter size is suitable if it is planned to cut the sample into smaller pieces later in the process, e.g. to deposit insulators with different insulator thicknesses. To prevent damage to the semiconductor surface during cutting, the surface is protected by a thick layer of photo resist (AZ5214) which is baked at 90 °C for 5 min. After the cutting, a standard cleaning process (SCP) - which will be used quite frequently in the following - ensures the removal of the photo resist.

The SCP consists of soaking the sample sequentially into acetone and propanol, then the solvents are blown off in a nitrogen (N) flow, and a subsequent heating of the sample at 180 °C for 10 min ensures that remaining solvents evaporate completely. The bare semiconductor stack that forms the initial status of device processing is depicted in

figures A.7(a) and A.7(b).

The first processing step, namely *Mesa etching*, aims at separating the regions on the sample, where devices will be realized. The approach of choice is to dry etch the AlGaN layer in between the designated device areas by ion beam etching (IBE) for 10 min, as illustrated in figures A.7(c) and A.7(d). As a result, the conducting 2DEG can not form and thus the devices are separated electrically. Prior to etching, an etching mask is prepared on top of the cleaned sample, involving a standard lithography process (SLP) and a subsequent hardening of the resist by heating it at 110 °C for 10 min.

The SLP consists of the following sequence: Photo resist - AZ5214 is appropriate - is spun onto the surface at 4000 rpm and dried at 90 °C for 5 min, then the resist is exposed to ultra violet (UV) light at a dose of 7 mW/(cm^{2}s) for 4 s and developed in a $AZ400 : H_20$ (1 : 4) solution for 60 s. Then, the sample is thoroughly rinsed in distilled water for 5 min and then dried in a N flow. Plasma processing for 2 min at low power level (program 01) concludes the SLP.

An optional process sequence of the SLP removes the side resist at the edges of the sample: After the photo resist has been applied, the sample is exposed to ultra violet (UV) light at a dose of 7 mW/(cm^{2}s) for 24 s, using a positive mask leaving only the sides of the sample unprotected. A subsequent development in a AZ400 : H_2O (1 : 4) solution for 30 s removes the resist at the edges. Rinsing the sample in distilled water for 5 min and drying it in N flow concludes the optional processing sequence.

An intense and thorough *cleaning* routing follows the mesa etching, i.e. the probe is soaked sequentially into a HF : H_2O (1 : 4), a HCl : H_2O (1 : 4), and a NH_4OH : H_2O_2 (2 : 1) solution for 2 min, 2 min, and 10 min, respectively. After the sample has been rinsed in diluted water thoroughly, it is blown off with N and heated at 180 °C for 10 min.

To fabricate *ohmic contacts*, a SLP is performed, utilizing the ohmic contact layer of the mask set in use. For ohmic contact fabrication the SLP is slightly expanded: Prior to the development the sample is soaked in chlorobenzene for 3 min and dried off in a N flow afterwards. This treatment hardens the surface of the photo resist and a photo resist edge with negative slope will form during development.

A short dip of 10 s duration in a HCl : H_2O (1 : 4) solution is performed shortly before metal deposition. To further enhance the adhesion of the metal to the surface, Ar^+ sputtering is performed prior to metal evaporation. During the metallization step itself, 35 nm Ti, 200 nm Al, 40 nm Ni, and 100 nm Au is deposited sequentially, which is frequently used for ohmic contact metallization used for GaN/AlGaN HFETs. After deposition, a lift off is performed and the metal is annealed at 900 °C for 30 s in a rapid thermal annealing (RTP) oven. Figure A.6 shows the result of an AFM scan of the surface which reveals that annealing yields a rough surface with peaks up to 400 nm height. Figures A.7(e) and A.7(f) show the device in the actual status.

After ohmic contacts have been processed, the *insulating layer* can be deposited. Depending on the material used the adequate deposition method will be chosen. A detailed treatment of this issue has already been presented in section A.1 for SiO_2 and $GdScO_3$. As figures A.7(g) and A.7(h) illustrate, the dielectric material covers the whole surface,

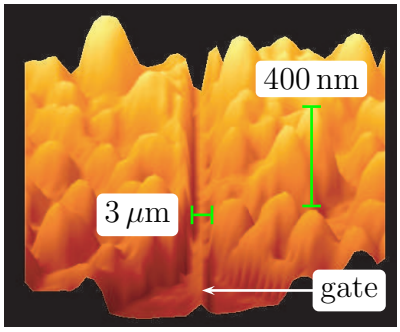
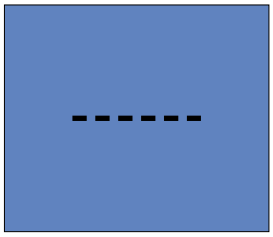


Figure A.6: AFM scan of ohmic contact surface after annealing at 900 °C.

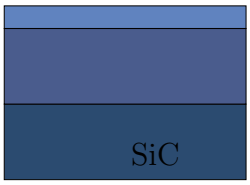
including the ohmic contact regions. But since the metal of the ohmic contacts has a very rough surface with peaks up to 400 nm, the dielectric material will not form a homogeneous insulating layer above the ohmic contacts. Therefore, etching of an additional window through a potential insulating layer to access the ohmic contacts is not necessary.

After deposition of the insulation layer and before processing the *gates* it is advised to perform a SCP. Then, the electron-beam lithography is prepared as discussed in section A.2, preventing PMMA cracking and electron-beam deviation due to charging effects. Three PMMA layers (600K, 200K, 600K) are spun onto the sample at 6000 rpm, each baked at 200 °C for 10 min. Afterwards, a thin Cr layer of 5 nm thickness is deposited. The electron-beam exposure is performed at a dose of 180 μC/cm^2 utilizing proximity correction. After electron-beam exposure, the Cr layer is removed by a 5 s dip in commercially available chrome etch. Then, the PMMA layers are developed in $AR600-55$ for 135 s, followed by rinsing the sample in propanol. A plasma processing for 2 min at a low power level is performed to remove potentially remaining PMMA from the developed regions. Then, the sample is ready for the deposition of 25 nm Ni and 100 nm Au, and a lift off step finishes the gate processing, as depicted in figures A.7(i) and A.7(j).

To enable comfortable access to the ohmic and Schottky contacts, metal *pads* with a geometry suitable for RF small-signal S-parameter measurements are fabricated in a final step. The SLP is applied here as well, utilizing the pad layer of the mask set in use. Afterwards, 25 nm Ti and 300 nm Au is deposited, which is commonly used for device pads. A lift off is performed as the final step. Figures A.7(k) and A.7(l) illustrate the completed MISHFET.



(a)



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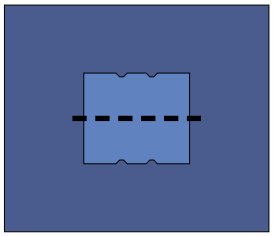

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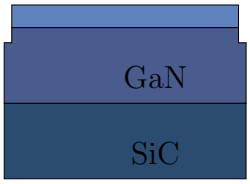

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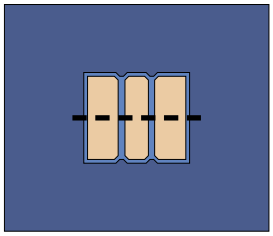
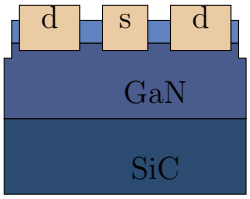


(e)



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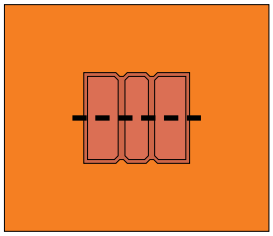

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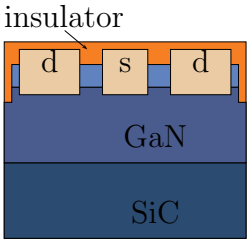

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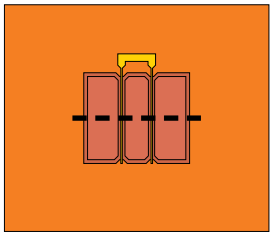
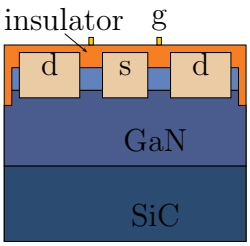
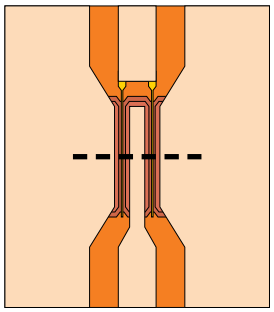


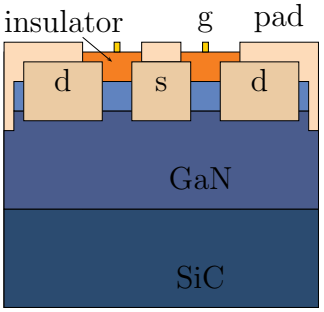
(i)



(j)



(k)



(l)

Appendix B

Electrical Characterization Methods

This chapter documents the standard means to characterize HFETs and HDiodes used in this work. According to the principles of the measurements, the chapter is divided into four sections. At first, the current-voltage (IV) measurement is introduced in section B.1, where either a distinct voltage is applied to the device under test (DuT) and the current is monitored or vice versa. Based on this principle, various measurement tasks can be accomplished, as the measurement of very low insulator currents, the characterization of the transistor output, the determination of the breakdown voltage, and the IV measurement under pulsed conditions.

Section B.2 covers the measurement of the complex impedance ($\underline{Z}$), which is measured by means of a testing bridge. The measured $\underline{Z}$ can then be interpreted assuming appropriate models. As a fast and simple application, the capacitance of the input of a HFET or a MISHFET can be extracted assuming a capacitance in parallel to a conductance to interpret the measured $\underline{Z}$. A more sophisticated method, namely the Impedance Spectroscopy, assumes a transmission line model to interpret $\underline{Z}$ which is measured over a broad range of frequencies.

S-parameter measurements are discussed in section B.3, which is a means to characterize the RF capabilities of HFETs. With this method, a small signal of given power is fed to the DuT, and the power of the output signal and reflected signals are measured. This enables to compute RF figures such as the cutoff frequency (f_T) and the maximum frequency of oscillation (f_max). The final section B.4 introduces the Load-Pull measurement, which is basically the measurement of the DuT as an amplifying means under large-signal conditions with matched in- and outputs.

The chosen structure of this chapter reflects the types of measurement equipment available at the IBN. For instance, any volt- or sourcemeter can serve for IV measurements, an impedance analyzer is a powerful means to fulfil the task of impedance measurements, a sophisticated measurement system built around a 110 GHz network analyzer makes S-parameter measurements feasible, and a complex system serves for RF Load-Pull measurements.

B.1 Current-Voltage Measurement

The application of a voltage to a device under test DuT and subsequent measurement of the resulting current - or vice versa, the injection of a current and monitoring the resulting voltage drop - is a fundamental technique in electrical characterization of devices. Nevertheless, there are specific aspects relevant for HFETs and MISHFETs that make it worthwhile to look at IV measurements in detail. Specific applications will be introduced, such as the measurement of leakage current through an insulator, the determination of input and output characteristics of HFETs and MISHFETs, and the distinction of the breakdown voltages of devices.

To perform IV measurements, one of the following instruments was used: a "Keithley 6430 Sub-Femtoamp Remote Source Meter", a "Keithley 2400 Source Meter", an "Agilent E5270A 8 Slot Parametric Measurement Mainframe", and a "HP 4155A Semiconductor Parameter Analyzer". The instruments were either controlled by means of "MATLAB 7.0" or "HP Vee 5.0", both running on a personal computer (PC) with a Microsoft Windows XP operating system. The measurement instruments were connected to the PC via an "Agilent 82357A USB/GBIP Interface Converter".

Measurement of Insulator Currents

Even for standard HFETs, there is the need to measure small currents. For instance, the gate leakage current can range from nA to μA, and the residual current between drain and source for a pinched-off HFET can be as low as some μA. But since this work aims at reducing the gate currents significantly, the need arises to measure currents down to several 100 fA.

Thus, the measurement setup must be chosen with greatest care to exploit the theoretical capabilities of the measurement equipment, in particular its measurement precision of 10 fA. Therefore, cables, connectors and the probing station need to be shielded against external influences (electromagnetic interference, mechanical vibrations, temperature changes), potential paths for parasitic currents must be minimized and the charging and discharging effects of the insulator need to be taken into account by appropriate hold and delay times.

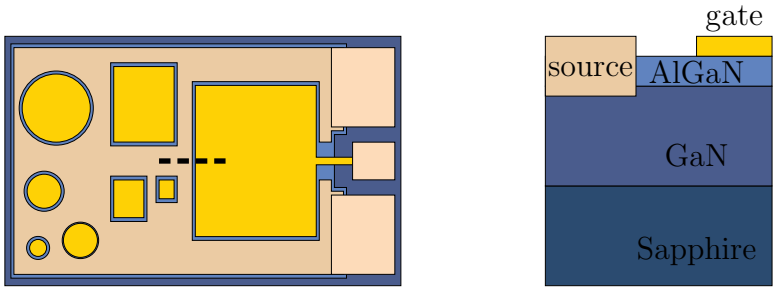
Measurement Setup and Execution Optimal results were achieved by using two Source-Measure Units (SMU) of the hp4155A, connected to a shielding box by triaxial cables. Within the shielding box, manipulators are connected by coaxial cables. Connectors should be cleaned from grease and other contaminants with organic solvents. After the set up, a period of several hours ensures that the measurement equipment warms up and settles to ideal operational conditions and that any residuals of the solvent evaporates.

The hold time of the hp4155A, i.e. the time period between triggering the measurement and the start of the measurement itself, is set to a value around 30 s to enable relaxation processes within the measurement facility and the cables. This is beneficial to prevent

the current minimum to shift to voltages other than 0 V. The delay time, i.e. the time period between the actual voltage has been applied and the start of the measurement itself, can be set to several seconds, depending on the measurement range: for currents remaining in the pA range a longer hold time is preferential, if the current rises from sub-pA to nA, then a shorter hold time will be the better choice.

The same holds true for the integration time, which is the time the measurement itself is performed and the measurement value is extracted by integration. For very small currents, an integration time of 640 ms is a good choice, whereas for currents spreading over some orders of magnitude the integration time should be smaller. Forward and reverse currents are measured separately, for either region the voltage sweep starts at 0 V.

Device under Test The objective is to get a quantitative measure for the insulating property of the gate dielectric under conditions comparable to those to be found in MISHFET devices. Therefore, round or square diodes made of the same layer stack as HFET or MISHFET are used as DuTs. Figure B.1 illustrates the diode configuration used.



(a) Top-view (b) Cross-section

Figure B.1: Schematic of a heterojunction diode. The square and round regions in (a) represent Schottky contacts, the surrounding area represents the ohmic contact. The dotted line drawn in figure (a) indicates the cross-section plotted in (b). From bottom to top the blue colored layers stand for substrate, GaN, and AlGaN layer.

Analysis The IV curve of a HDiode reveals a kink: When moving from 0 V towards more negative values, the slope of the current drops to nearly zero at a certain voltage ($V_{\mathrm{th}}^{\mathrm{IV}}$). The maximum reverse current ($I_{\mathrm{max}}^{\mathrm{rev}}$) is taken at a voltage below $V_{\mathrm{th}}^{\mathrm{IV}}$, typically at -8 V. In contrast to the determination of $I_{\mathrm{max}}^{\mathrm{rev}}$, the definition of the maximum forward current ($I_{\mathrm{max}}^{\mathrm{forw}}$) is somewhat arbitrary due to the exponential increase in the Schottky case and the still monotonically increasing current for MISHDiodes. Therefore, $I_{\mathrm{max}}^{\mathrm{forw}}$ is defined as the current to be measured at $V = 3$ V.

Characterization of Transistor Output

The determination of the output characteristic is a fundamental task in characterizing HFETs or MISHFETs. It not only provides essential information regarding the DC behavior of the device, it allows a first and rough estimation of RF properties as well. The output characteristic can be defined as the drain current (I_d) being a function of drain source voltage (V_ds) and gate source voltage (V_gs). The representation of the output characteristic in the form of I_d being plotted over V_ds for various V_gs values is a well known transistor chart.

The principle of determining the output characteristic is fairly simple: biasing the gate-source and the drain-source electrodes with V_gs and V_ds, respectively, determines the actual working point and I_d can be monitored. The working points are systematically sweeped through and for each point the monitoring procedure is repeated. In the ideal case, it is irrelevant whether V_gs is swept first followed by V_ds or vice versa. But if the device suffers from imperfections, e.g. if the drain current decreases after a larger V_ds has been applied (current collapse), then the order of V_ds and V_gs sweeps becomes relevant.

Setup and Execution The measurement setup consists of two source-monitor units (SMU) providing V_gs and V_ds to the gate source and drain source electrodes, respectively (Figure B.2). The sense functions of the SMUs providing V_ds serves to monitor I_d.

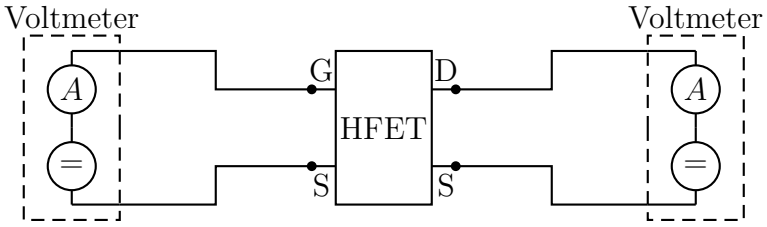


Figure B.2: Setup to characterize the output of HFETs and MISHFETs.

V_gs is swept from some volts beyond 0 V down to a level slightly underneath V_th. V_ds is varied from 0 V up to several tens of volts and should remain underneath breakdown voltage V_break. Since the currents to be measured are fairly high, specific arrangements (hold and delay times, shielding) do not need to be met. The SMUs are controlled by means of a "HP Vee" program running on a personal computer which is connected to the measurement facilities by a GPIB interface.

Although the sense function of the SMU providing V_gs yields I_g, the results must be treated with care: The actual setup is not meant to detect low currents through insulators. Thus, the necessary precautions (see section B.1) are not met and the measurements do not yield reliable I_g values for MISHFETs.

Analysis Analyzing the output characteristic provides many essential device information: The maximum drain current ($I_\mathrm{d,max}$) is taken from the output characteristics at a

certain gate source voltages, typically at $V_{gs} = 1\,V$ and $0\,V$. The maximum drain current holds information regarding sheet carrier concentration (n_s), carrier mobility (μ), and source resistance (R_s). The voltage at which I_d maximizes, namely the knee voltage (V_{knee}), denotes the borderline between linear (left of V_{knee}) and saturation region (right of V_{knee}) of the device.

The output conductance (g_d) is defined as the derivative of I_d with respect to V_{ds}. In particular, the maximum of g_d ($g_{d,max}$) is utilized as a measure to describe the DC characteristic in the linear region: Differences in $g_{d,max}$ can be related to differences in R_s and drain resistance (R_d). The mean g_d of the saturation region ($g^{sat}_{d,mean}$) is taken as a measure which can be related to the ability of the device to dissipate heat emerging from the conductive channel ($g^{sat}_{d,mean} = 0\,mS/mm$ can be interpreted as perfect heat dissipation).

The extrinsic transconductance ($g_{m,extr}$) is defined as the derivative of I_d with respect to V_{gs}. It is a measure of choice to quantify the ability to control the 2DEG channel. In particular, the threshold voltage (V_{th}) can be extracted from $g_{m,extr}$, and it also reveals the quality of the "on"- to "off"-state transition.

Determination of Breakdown Voltage

For HFETs and MISHFETs to serve as devices in RF power amplifiers, a high output voltage is crucial. The higher the drain source voltage the device can sustain, the higher the potential RF output power. The voltage to cause a physical breakdown of a pinched-off device under DC conditions (V^{DC}_{break}) is an appropriate figure of merit to estimate the potential output power performance of the device under RF conditions.

There are several ways to determine V^{DC}_{break}. The simplest method is to increase the drain voltage (V_{ds}) applied to a pinched-off HFET until the device breaks down. The disadvantage of this rather simple measurement is the destruction of the device. But the fact that the process of breakdown is accompanied by a sudden and strong increase of I_d opens up the possibility for a minor but effective modification: V^{DC}_{break} can now be defined as the gate drain voltage (V_{ds}) at which I_d of a pinched-off device ($V_{gs} < V_{th}$) reaches $1\,mA/mm$ (Note, that the breakdown is assumed to occur between the gate and drain electrode). At this point the process of breakdown has likely begun, but the device is not destroyed yet. If the measurement facility is fast enough to switch off the voltage source as soon as the I_d condition has been fulfilled, then the irreversible breakdown of the device can be prevented in most cases.

A more sophisticated method which is said to be even less destructive was proposed by Bahl and Alamo [12]. The authors inject a small but defined drain current (I_d) at off-state conditions. Then, they sweep the gate source voltage (V_{gs}) from the "on"- to the "off"-state conditions and monitor the drain source voltage (V_{ds}) during this transition. As the "on"- to "off"-state transition takes places, V_{ds} increases rapidly to a maximum which can be used as an estimate for the breakdown voltage. But experiments showed: Compared to the simple but modified approach, the likelihood of a device to be destroyed if the method of Bahl and Alamo is utilized is much higher.

Setup and Execution The setup is similar to the configuration used to characterize the output characteristic of a HFET as described in section B.1, but here a "hp4155A" facility was used: The two source contacts are connected to SMU1, which is set to the "common" mode. The gate and drain contacts are connected to SMU2 and SMU3 in voltage mode, respectively.

The gate source voltage is swept such that the device is driven from the "on"- to the "off"-state. The V_{ds} sweep ranges from 0 V to 100 V, which is the maximum range feasible for the used equipment. The I_{d} compliance is set to a value corresponding to 1 mA/mm, and the voltage source is instructed to cancel the voltage sweep in case the compliance is reached.

Analysis According to the above definition of V_{break}^{DC}, the analysis of the measured data is as follows: The first IV curve which relates to an "off"-state is identified and the voltage at which I_{d} reaches 1 mA/mm is taken. Then, V_{break}^{DC} is computed being the difference of V_{ds} and V_{gs}.

Measurement under Pulsed Conditions

The pulsed IV measurement method reveals insight into the effects caused by electronic states. For instance, this method serves to investigate the DC/RF dispersion phenomenon, i.e. the reduction of drain current (I_{d}) under higher frequency conditions compared to DC conditions.

Basically, the device is measured as in conventional DC output characterization measurements as described in B.1. But instead of biasing the gate with a constant voltage, a voltage pulse generated by a function generator is used. Thus, the drain current flows discontinuously as well. By variation of the frequency and the width of the pulses used, channel heating effects and drain current contributions due to trapping effects can be made visible.

Setup and Execution The setup of the pulsed IV system consists of the device under test (DuT), a frequency generator which can generate pulses from 100 ns to 1 s, an oscilloscope which detects the voltage drop over a resistor of typically 12 Ω (enabling the measurement of I_{d}), and the DC bias supply. A schematic measurement setup is shown in figure B.3.

To control the measurement, a PC is used running a "hpVee" program. The pulse sequences used in the standard routine has a frequency in the range between 200 Hz and 20 kHz and a duty cycle of 10 %. It needs to be noted, that since the measurement system causes a significantly high noise level, I_{d} should be above 20 mA to achieve a reasonable signal to noise ratio.

Pulses The pulse that is applied between the gate and source electrodes alternates between a quiescent level V_q and a working voltage level V. The V_q is a voltage level below

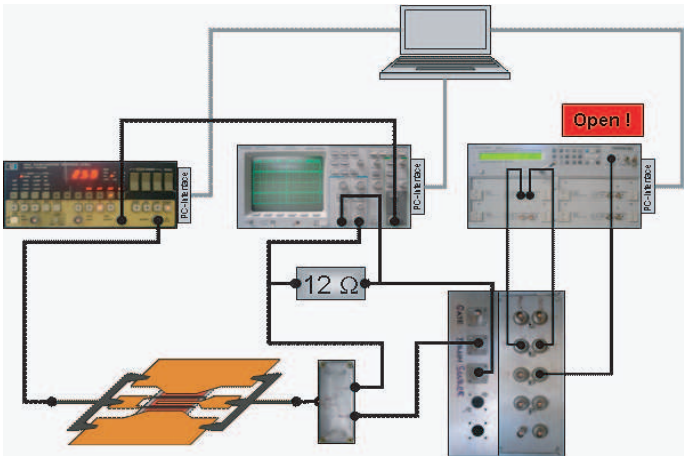


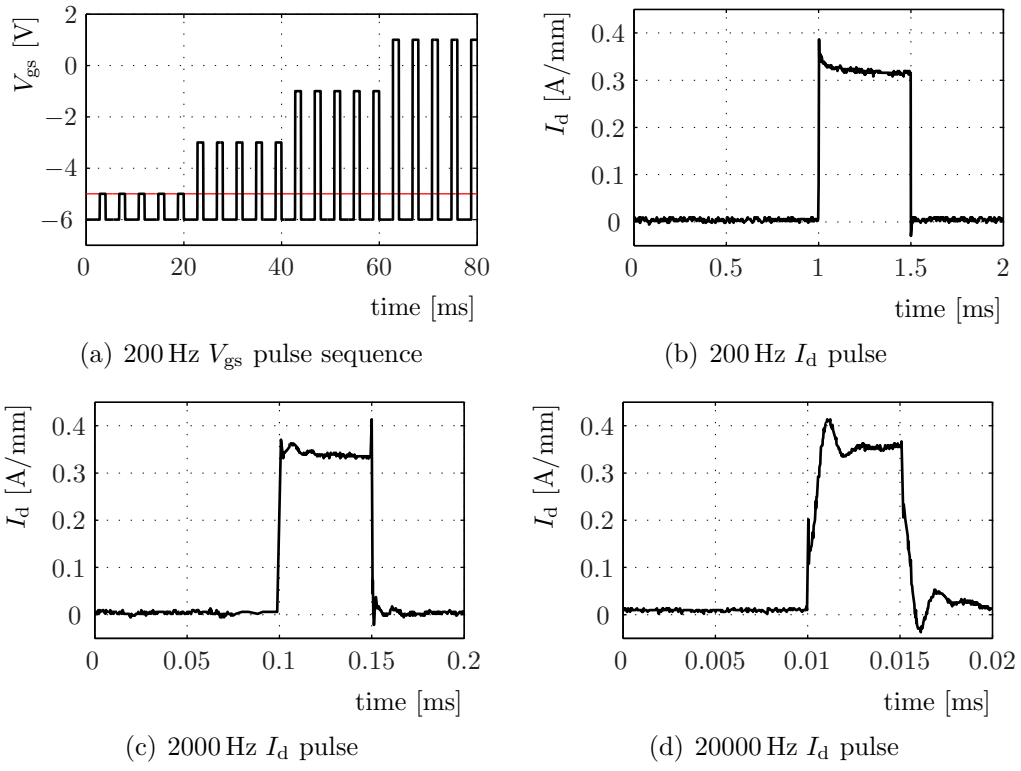
Figure B.3: Setup of pulsed current-voltage measurement.

the threshold voltage V_{th}, i.e. at the device is in the "off"-state. The working voltage is chosen above V_{th}, it corresponds to an "on"-state level of the device. Figure B.4(a) illustrates an ideal sequence of V_{gs} pulses with increasing V.

The time duration in which the bias level is above V_q is denoted with t_{pulse}, the period the bias level is at V_q is denoted t_q. Thus, the frequency of the generated signals (f) is $1/(t_{pulse} + t_q)$. The variation of t_q is an appropriate means to eliminate thermal effects within the device: For instance, if t_{pulse} is only 10 % of the entire period of the pulse $(t_{pulse} + t_q)$, then the device is in "off"-state most of the time and thus can not heat up as strongly as under DC conditions. The quantity $t_{pulse}/(t_{pulse} + t_q)$ is also denoted duty cycle. The parameter t_{pulse} enables to investigate the transient properties of the device: The longer t_{pulse} the more effective and noticeable transient processes will be.

Corresponding to the V_{gs} pulse, the drain current (I_{d}) also forms as a pulse. Figure B.4 illustrates pulses for commonly used frequencies at a duty cycle of 10 %. Apparently, the higher the frequency the more the form of the pulse deviates from the ideal square pulse. For the equipment used, 20 kHz is considered the highest frequency at which an acceptable pulse can be expected.

Analysis The measurement results can be interpreted as follows. If the drain current decreases with increasing frequency, then trapping states contribute to the DC current: For higher frequncies the transient processes related to the traps can not follow anymore and the associated flow of charge carriers deminishes. On the other hand, if the drain current level remains constant, then the influence of the traps that might exists do not have any influence on the electrical behavior of the device.



(a) 200 Hz V_{gs} pulse sequence

(b) 200 Hz I_d pulse

(c) 2000 Hz I_d pulse

(d) 20000 Hz I_d pulse

Figure B.4: Schematic of a bias pulse sequence to be applied to gate and source electrodes of a transistor (a), and resulting drain current pulses at 200 Hz (b), 2 kHz (c), and 20 kHz (d).

B.2 Impedance Measurement

This section covers the impedance measurement principle and discusses two important applications utilizing the impedance measurement for studying HFETs and MISHFETs, namely the capacitance-voltage (CV) measurement and the Impedance Spectroscopy (IS).

Principle

The impedance ($\underline{Z}$) can be defined as the total opposition a device or circuit offers to the flow of a current alternating with a given frequency. Various methods can be used to determine $\underline{Z}$: Bridge, Resonant, Current-Voltage, RF Current-Voltage, Network Analysis, and Auto Balancing Bridge (ABB) method [8].

Within the scope of this work, the ABB method is appropriate, since it covers the frequency range between 40 Hz and 110 MHz. The principle of the ABB can be best explained by means of figure B.5(a). The measurement circuit consists of an alternating voltage source (V_{osc}), two voltmeters (V_1, V_2), an IV converter amplifier with a shunt resistor (R), and the impedance to be measured ($\underline{Z}$).

The main idea of the measurement circuit is that the current flowing through R balances the current through $\underline{Z}$, thus maintaining the potential at the "low" point at zero volts (referred to as virtual ground). The current through R is controlled by the operation of the amplifier. Having maintained virtual ground potential at the "low" point, $\underline{Z}$ can be calculated using voltage measurement at the "high" terminal (V_1) and across R (V_2). For an in depth description of the ABB method and implementation details of the utilized Agilent 4294A Impedance Analyzer see [10].

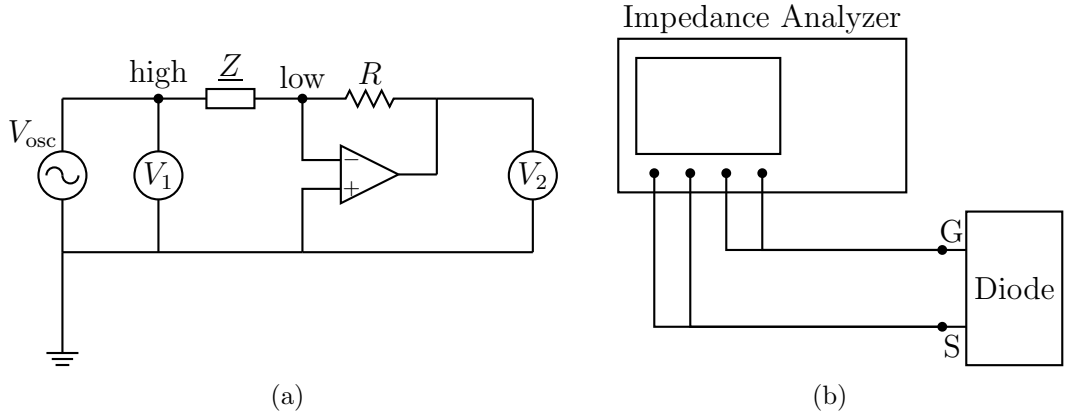


Figure B.5: Principle of the Auto Balancing Bridge (ABB) method (a) and setup of the impedance measurement system (b).

Setup and Execution To perform impedance measurement by means of the ABB method, the setup depicted in figure B.5(b) is used.

Capacitance-Voltage Measurement

The capacitance-voltage (CV) measurement is a frequently used means to study HDiodes, HFETs, and MISHFETs. Quantities like threshold voltage (V_{th}), total capacitance (C), sheet carrier concentration (n_{s}), AlGaN layer thickness (d^{AlGaN}), dielectric constant ($\epsilon_{\mathrm{r}}^{\mathrm{AlGaN}}$), insulator thickness ($d^{\mathrm{insul}}$), and dielectric constant of the insulator ($\epsilon_{\mathrm{r}}^{\mathrm{insul}}$) can be determined.

Setup and Execution In a first step, an impedance measurement as described above is performed. At this step, a critical aspect with the CV measurement method needs to be mentioned: Although at first sight the capacitance should be frequency independent, it does indeed vary with frequency in practice. Thus, the CV measurement needs to be executed at various frequencies, then a measurement is chosen whose frequency lies in the frequency range with nearly constant measurement results (For the HFET and MISHFET devices used, measurements at 1 MHz yields good results).

Analysis Then, the measured $\underline{Z}$ is interpreted as a parallel circuit of conductance (G) and capacitive susceptance (B), as depicted in figure B.6. This means that C can be calculated by solving the following system of equations:

$$\begin{aligned} \underline{Z}^{-1} &= G + jB \\ G &= \frac{R}{R^2 + X^2} \\ B &= \frac{-X}{R^2 + X^2} \\ X &= \frac{1}{2\pi f C}. \end{aligned}$$

By means of a built in function within the Agilent 4294A Impedance Analyzer the transformation $C \mapsto \underline{Z}$ can be performed automatically.

Figure B.6: Interpretation of measured impedance ($\underline{Z}$). In the context of CV measurements $\underline{Z}$ is interpreted as a parallel circuit of conductance G and capacitive susceptance B.

After having extracted C, the plot of C versus the applied voltage V reveals a function typical for a device incorporating a GaN/AlGaN heterojunction: For $V_{\mathrm{th}} < V \leq 0\,\mathrm{V}$, C remains nearly at a constant value. Within a short interval around V_{th}, C drops rapidly to significantly lower values. Figure B.7 illustrates a sample CV-curve of a diode based

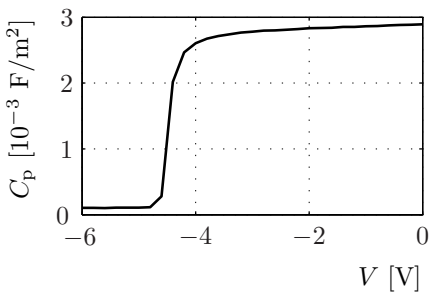


Figure B.7: Typical result of a CV measurement of a HDiode. The CV plot shows a significant capacitance drop at the threshold voltage (V_th). For voltages higher than V_th the capacitance remains nearly constant.

on a SiC/GaN/AlGaN layer stack, having a constant capacitance of $2.8 \cdot 10^{-3}$ F/m^2 and $V_\mathrm{th} = -4.7\,\mathrm{V}$.

Section 5.1 provides a detailed explanation of the typical form of the CV curve and provides the appropriate formal expressions to calculate the aforementioned characteristic quantities and figures. By studying the variation of the CV curve during a time series of measurements, one can gather information regarding V_th shifts and hysteresis effects. This knowledge gives insight for instance into the distribution of traps within the dielectric of a MISHFET, as was utilized in section 8.2.

Impedance Spectroscopy

One of the major tasks to characterize channel properties is to determine the sheet carrier concentration (n_s) and the carrier mobility (μ). Besides conventional methods as gated hall measurements and conductivity-capacitance measurements we applied a more sophisticated method, namely Impedance Spectroscopy (IS).

Principle The basic idea behind the IS is to measure the impedance over a wide range of frequencies, typically in the range from kHz to MHz, and to fit a theoretical model to the measured data by varying parameters suitable to calculate the sheet carrier concentration (n_s), and mobility (μ).

Transmission Line Model The model to be derived shall represent the electrical behavior of a HFET. Assuming high frequency conditions, the gate electrode and the two dimensional electron gas (2DEG) can be considered as an electrical transmission line, which has to be treated with methods known from high frequency engineering.

Discrete electrical devices are used to describe an infinitesimal small part of the electrical transmission line: a conductivity (G) and a capacitance (C) in parallel represent the electrical behavior of the AlGaN region underneath the gate electrode (and - if given - the dielectric layer of a MISHFET). A resistivity (R) and inductivity (L) represents an infinitesimal small part of the 2DEG and is modeled as a device in series to C and

G. Integration over the gate length yields an expression for the behavior of the entire transmission line.

The transmission line is considered "open", since the source contact will not be contacted. In direction towards the drain contact a discrete resistor (R_{cont}) models the behavior of the ohmic contact of the drain contact and the influence of the 2DEG that is not located underneath the gate electrode. Figure B.8 illustrates the above described model.

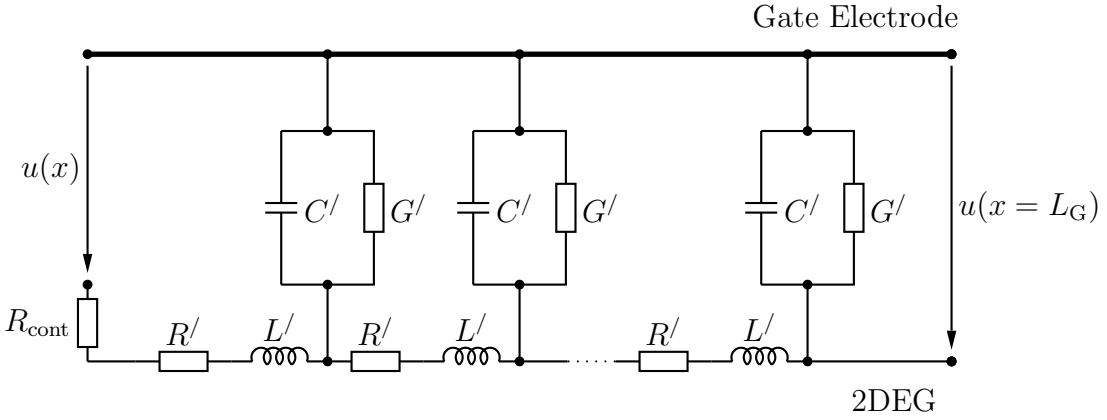


Figure B.8: Transmission line model (TLM) of a HFET or a MISHFET.

The following derivation will yield an expression for the complex impedance at the beginning of the transmission line as a function of the characteristic wave impedance and the propagation constant $Z_a = f(Z_L, \gamma)$. Application of Kirchhoff's laws yields

$$\begin{aligned} 0 &= u(x,t) - R^{'}\Delta x i(x,t) - L^{'}\Delta x \frac{\partial i(x,t)}{\partial t} - u(x+\Delta x,t), \\ 0 &= i(x,t) - G^{'}\Delta x u(x+\Delta x,t) - C^{'}\Delta x \frac{\partial u(x+\Delta x,t)}{\partial t} - i(x+\Delta x,t), \end{aligned}$$

which can be transformed to

$$\begin{aligned} -\frac{u(x+\Delta x,t) - u(x,t)}{\Delta x} &= R^{'} i(x,t) + L^{'}\frac{\partial i(x,t)}{\partial t}, \\ -\frac{i(x+\Delta x,t) - i(x,t)}{\Delta x} &= G^{'} u(x+\Delta x,t) + C^{'}\frac{\partial u(x+\Delta x,t)}{\partial t}. \end{aligned}$$

Letting $\Delta x \to 0$ yields

$$\begin{aligned} -\frac{\partial u(x,t)}{\partial x} &= R^{'} i(x,t) + L^{'}\frac{\partial i(x,t)}{\partial t}, \\ -\frac{\partial i(x,t)}{\partial x} &= G^{'} u(x,t) + C^{'}\frac{\partial i(x,t)}{\partial t}, \end{aligned}$$

and assuming $u(x,t)$ and $i(x,t)$ to be time-harmonic cosine functions,

$$\begin{aligned} u(x,t) &= Re\{U(x)e^{j\omega t}\}, \\ i(x,t) &= Re\{I(x)e^{j\omega t}\}, \end{aligned}$$

one gets

$$\begin{aligned} -\frac{\mathrm{d}U(x)}{\mathrm{d}x} &= (R^{'} + j\omega L^{'})I(x), \\ -\frac{\mathrm{d}I(x)}{\mathrm{d}x} &= (G^{'} + j\omega C^{'})U(x), \end{aligned}$$

which can be transformed into

$$\frac{\mathrm{d}^2U(x)}{\mathrm{d}x^2} = \gamma^2 U(x), \tag{B.1}$$

$$\frac{\mathrm{d}^2I(x)}{\mathrm{d}x^2} = \gamma^2 I(x), \tag{B.2}$$

where γ is the propagation constant

$$\gamma = \sqrt{(R^{'} + j\omega L^{'})(G^{'} + j\omega C^{'})}. \tag{B.3}$$

The differential equations B.1 and B.2 have the following solutions:

$$U(x) = U_0^+ e^{j\omega x} + U_0^- e^{j\omega x}, \tag{B.4}$$

$$I(x) = \frac{U_0^+}{Z_L} e^{j\omega x} - \frac{U_0^-}{Z_L} e^{j\omega x}, \tag{B.5}$$

where the terms indicated with $^{+(-)}$ are associated to a traveling wave in positive (negative) x-direction, and the characteristic impedance Z_L is defined as

$$Z_L = \sqrt{\frac{(R^{'} + j\omega L^{'}}{(G^{'} + j\omega C^{'}}}. \tag{B.6}$$

Division of B.4 by B.5 yields an expression for the impedance at any x value

$$Z(x) \equiv \frac{U(x)}{I(x)} = Z_L \frac{U_0^+ e^{-\gamma x} + U_0^- e^{-\gamma x}}{U_0^+ e^{-\gamma x} - U_0^- e^{-\gamma x}}. \tag{B.7}$$

Equation B.7 yields the following expressions for the impedance at the left and right end of the transmission line, $Z_a \equiv Z(x = 0)$ and $Z_e \equiv Z(x = L_G)$, respectively:

$$Z_a = Z_L \frac{1 + \frac{U_0^-}{U_0^+}}{1 - \frac{U_0^-}{U_0^+}}, \text{and} \tag{B.8}$$

$$Z_e = Z_L \frac{1 + e^{2\gamma L_G} \frac{U_0^-}{U_0^+}}{1 - e^{2\gamma L_G} \frac{U_0^-}{U_0^+}}. \tag{B.9}$$

Transforming B.8 and B.9 yields

$$\frac{U_0^-}{U_0^+} = \frac{\frac{Z_a}{Z_L} - 1}{\frac{Z_a}{Z_L} + 1} \tag{B.10}$$

$$\frac{U_0^-}{U_0^+} = \frac{\frac{Z_e}{Z_L} - 1}{\frac{Z_e}{Z_L} + 1} e^{-2\gamma L_G}. \tag{B.11}$$

Equations B.10 and B.11 set equal results in

$$\frac{\frac{Z_a}{Z_L}-1}{\frac{Z_a}{Z_L}+1} = \frac{\frac{Z_e}{Z_L}-1}{\frac{Z_e}{Z_L}+1}e^{-2\gamma L_G}. \tag{B.12}$$

In the following, the algebraic transformation of equation B.12 into the final expression B.13 is shown in detail:

$$\begin{aligned}
\frac{\frac{Z_a}{Z_L}-1}{\frac{Z_a}{Z_L}+1} &= \underbrace{\frac{\frac{Z_e}{Z_L}-1}{\frac{Z_e}{Z_L}+1}e^{-2\gamma L_G}}_{f}. \\
\frac{Z_a}{Z_L}-1 &= f(\frac{Z_a}{Z_L}+1), \\
\frac{Z_a}{Z_L}(1-f) &= 1+f, \\
Z_a &= Z_L\frac{1+f}{1-f}, \\
Z_a &= Z_L\frac{1+\frac{\frac{Z_e}{Z_L}-1}{\frac{Z_e}{Z_L}+1}e^{-2\gamma L_G}}{1-\frac{\frac{Z_e}{Z_L}-1}{\frac{Z_e}{Z_L}+1}e^{-2\gamma L_G}}, \\
Z_a &= Z_L\frac{(\frac{Z_e}{Z_L}+1)e^{2\gamma L_G}+\frac{Z_e}{Z_L}-1}{(\frac{Z_e}{Z_L}+1)e^{2\gamma L_G}-\frac{Z_e}{Z_L}+1}, \\
Z_a &= Z_L\frac{\frac{Z_e}{Z_L}+\frac{e^{2\gamma L_G}-1}{e^{2\gamma L_G}+1}}{\frac{Z_e}{Z_L}\frac{e^{2\gamma L_G}-1}{e^{2\gamma L_G}+1}+1}, \\
Z_a &= Z_L\frac{\frac{Z_e}{Z_L}+tanh(\gamma L_G)}{\frac{Z_e}{Z_L}tanh(\gamma L_G)+1}.
\end{aligned} \tag{B.13}$$

In the case of $Z_e \to \infty$, i.e. if the right side of the transmission line is open, equation B.13 simplifies to

$$\underline{Z} \equiv Z_a = \frac{Z_L}{tanh(\gamma L_G)}. \tag{B.14}$$

Adding a circuit element representing the contact resistivity R_{cont}, the expression for the transmission line model is

$$\underline{Z} = R_{\text{cont}} + \frac{\underline{Z}_{\text{L}}}{tanh(L_G\underline{\gamma})}, \tag{B.15}$$

where the characteristic wave impedance $\underline{Z}_{\text{L}}$ and the propagation factor $\underline{\gamma}$ are respectively defined as

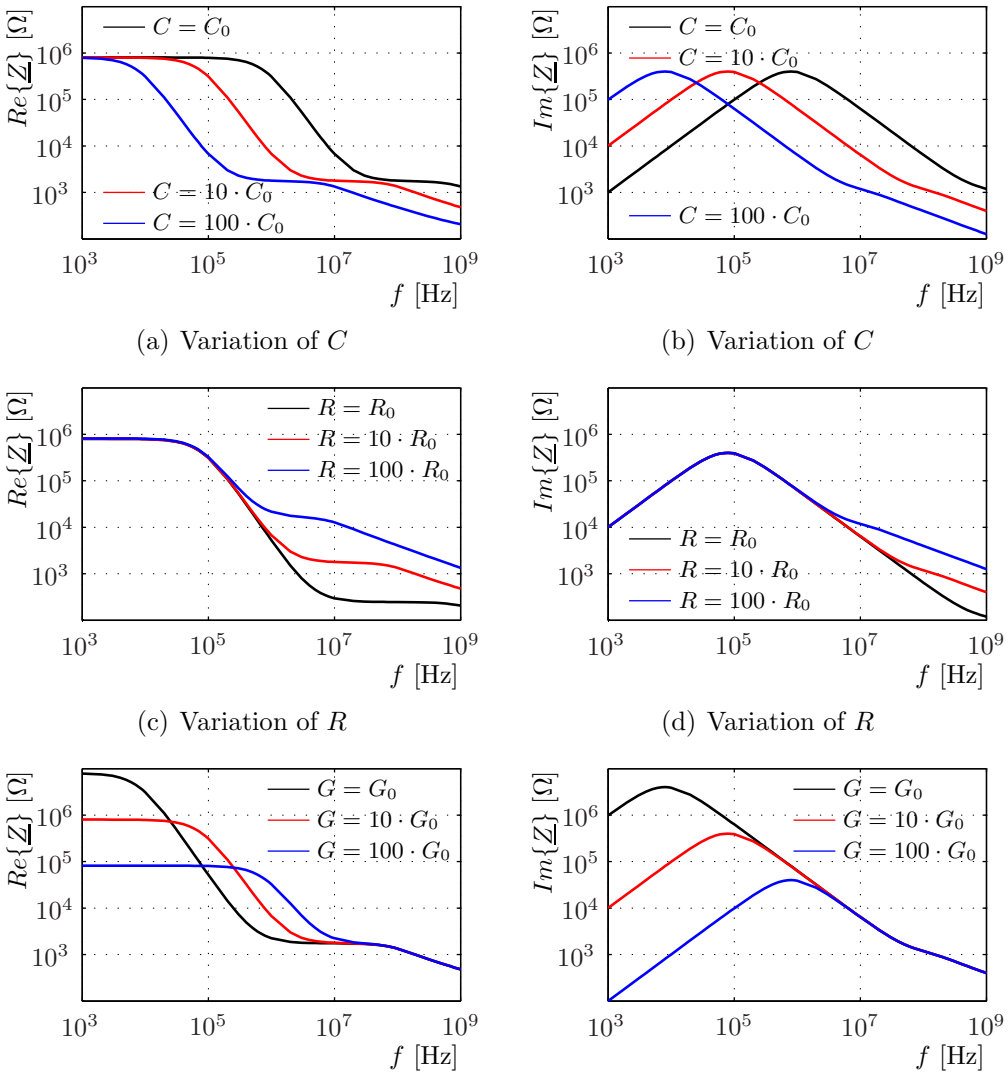
$$\underline{Z}_{\text{L}} = \sqrt{\frac{R}{G+j\frac{1}{2\pi f}}} \quad \text{and} \quad \underline{\gamma} = \sqrt{R(G+j\frac{1}{2\pi f})}.$$

In figure B.9, the real and imaginary part of $\underline{Z}$ are plotted over frequency (f). Apparently, the influence of the parameters C, R, and G can be clearly identified, increasing C shifts

the slope of the real part of $\underline{Z}$ towards smaller frequencies, an increasing R lifts up the right lower plateau of the function, and an increase of G raises the upper left plateau and shifts the slope in the direction of smaller frequencies.

Fitting The fitting algorithm implemented aims at finding suitable values for C, R, and G such that the fitting function matches the measured $\underline{Z}$ best in the sense of a least squares criterion. To make use of these distinct variations of the fitting function as shown in figure B.9 it is necessary to measure over a wide range of frequencies (from kHz to several MHz).

Another apparent fact is that $\underline{Z}$ takes values from of a broad interval of around four orders of magnitude. In addition, the values of C, R, and G have values from different regimes as well. These two facts were taken into account to implement an effective fitting algorithm, in particular the logarithm of $\underline{Z}$ was utilized, also the logarithm of the parameters $1/G$, C, and R was optimized, and the real and imaginary part of $\underline{Z}$ were processed simultaneously. An example of a fit is shown in figure B.10.



(a) Variation of C (b) Variation of C

(c) Variation of R (d) Variation of R

(e) Variation of G (f) Variation of G

Figure B.9: Dependence of impedance ($\underline{Z}$) on parameters of the transmission line model (TLM). Each plot illustrates the variation of $\underline{Z}$ if a single parameter of the TLM is varied from low (black) to medium (red) and finally to higher values (blue).

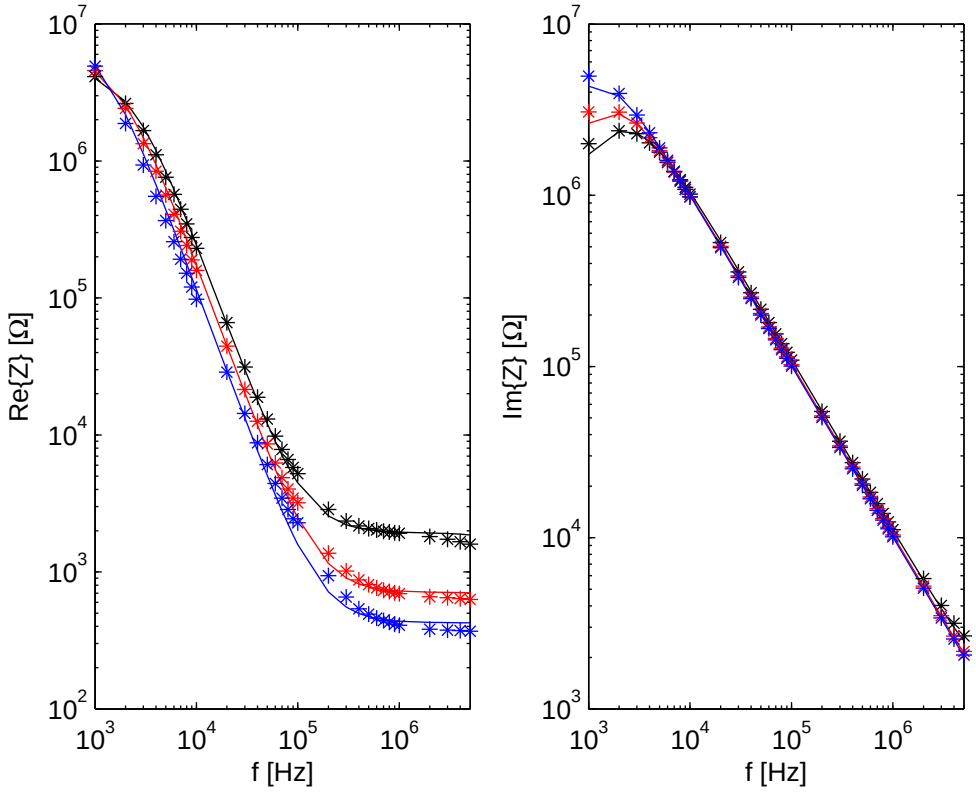


Figure B.10: Fit of theoretical impedance function to measured data. The different colors represent different biasing conditions.

B.3 S-Parameter Measurements

As a means to determine the behavior of the HFETs and MISHFETs under RF conditions, S-parameter measurements are performed. From S-parameters, important figures of merit as cut-off frequency (f_{T}) and maximum frequency of oscillation ($f_{\max}$) can be calculated.

Principle If a transistor is considered as a two port network, then an impedance matrix ($\underline{Z}$) can serve as a description of this network which relates voltages ($\underline{V}_{1/2}$) and currents ($\underline{I}_{1/2}$) at the input (1) and output port (2) of the device:

$$\begin{pmatrix} \underline{V}_1 \\ \underline{V}_2 \end{pmatrix} = \underbrace{\begin{pmatrix} \underline{Z}_{11} & \underline{Z}_{12} \\ \underline{Z}_{21} & \underline{Z}_{22} \end{pmatrix}}_{\underline{Z}} \begin{pmatrix} \underline{I}_1 \\ \underline{I}_2 \end{pmatrix}.$$

One way to characterize the device, i.e. to determine the elements of $\underline{Z}$, is to carry out

a sequence of four conventional IV measurements:

$$\underline{Z}_{11} = \frac{\underline{V}_1}{\underline{I}_1}\Big|_{\underline{I}_2=0}, \quad \underline{Z}_{21} = \frac{\underline{V}_2}{\underline{I}_1}\Big|_{\underline{I}_2=0}, \quad \underline{Z}_{12} = \frac{\underline{V}_1}{\underline{I}_2}\Big|_{\underline{I}_1=0}, \quad \underline{Z}_{22} = \frac{\underline{V}_2}{\underline{I}_2}\Big|_{\underline{I}_1=0}. \tag{B.16}$$

A crucial point of this approach is that "open" states have to be realized although this requirement is hard to meet under RF circumstances. A similar approach demands for a short circuit of one port, which becomes also critical if the measurements need to be carried out under RF conditions.

An alternative way is to describe the device by means of its scattering matrix ($\underline{S}$) which relates the power levels of the incident ($\underline{a}_{1/2}$) and reflected signals ($\underline{b}_{1/2}$) at the input (1) and the output port (2) of the device:

$$\begin{pmatrix} \underline{b}_1 \\ \underline{b}_2 \end{pmatrix} = \underbrace{\begin{pmatrix} \underline{S}_{11} & \underline{S}_{12} \\ \underline{S}_{21} & \underline{S}_{22} \end{pmatrix}}_{\underline{S}} \begin{pmatrix} \underline{a}_1 \\ \underline{a}_2 \end{pmatrix}.$$

The scattering parameters $\underline{S}_{11}$, $\underline{S}_{12}$, $\underline{S}_{21}$, $\underline{S}_{22}$ can be determined for all frequencies by performing the following measurement sequence:

$$\underline{S}_{11} = \frac{\underline{b}_1}{\underline{a}_1}\Big|_{\underline{a}_2=0}, \quad \underline{S}_{12} = \frac{\underline{b}_1}{\underline{a}_2}\Big|_{\underline{a}_1=0}, \quad \underline{S}_{21} = \frac{\underline{b}_2}{\underline{a}_1}\Big|_{\underline{a}_2=0}, \quad \underline{S}_{22} = \frac{\underline{b}_2}{\underline{a}_2}\Big|_{\underline{a}_1=0}.$$

The advantage of this concept is that neither of the ports needs to be in an "open" or "short" state which simplifies the task of characterizing the device drastically.

Setup and Execution Within the scope of this work, the S-parameters are determined utilizing a network analyzer system (hp 8510XF) with a frequency range from 2 GHz to 110 GHz (figure B.11).

A RF signal is generated by means of an Oscillator (HP 83651B, Synthesized RF source) ranging from 0.01 GHz to 50 GHz and is fed into a millimeter-wave controller (HP E7341A), which passes the signal either to the left or to the right test head of the system (HP E7352L/R). Through the ports of the test heads the incident signal is fed to the device under test (DuT). The reflected signal propagates in opposite direction: from the DuT via the ports into the test head.

By means of direction couplers the incident and the reflected signals are separated. The signals are then mixed with a common LO signal, which is generated by an oscillator having a frequency range from 0.01 GHz to 20 GHz (HP 83621B, Synthesized LO source). The resulting IF signals are then fed into the network analyzer (HP 8510C). The DuT is biased over a bias tee and a DC voltage source (HP 6626A DC Power Supply).

Analysis Having measured the S-parameters, various measures can be derived that characterize the amplification of the device: Maximum stable gain (MSG), maximum available gain (MAG), unilateral gain (GU), and current gain ($\underline{h}_{21}$). The formal expressions are listed in table B.1. The frequency at which $\underline{h}_{21}$ and MAG reach unity is

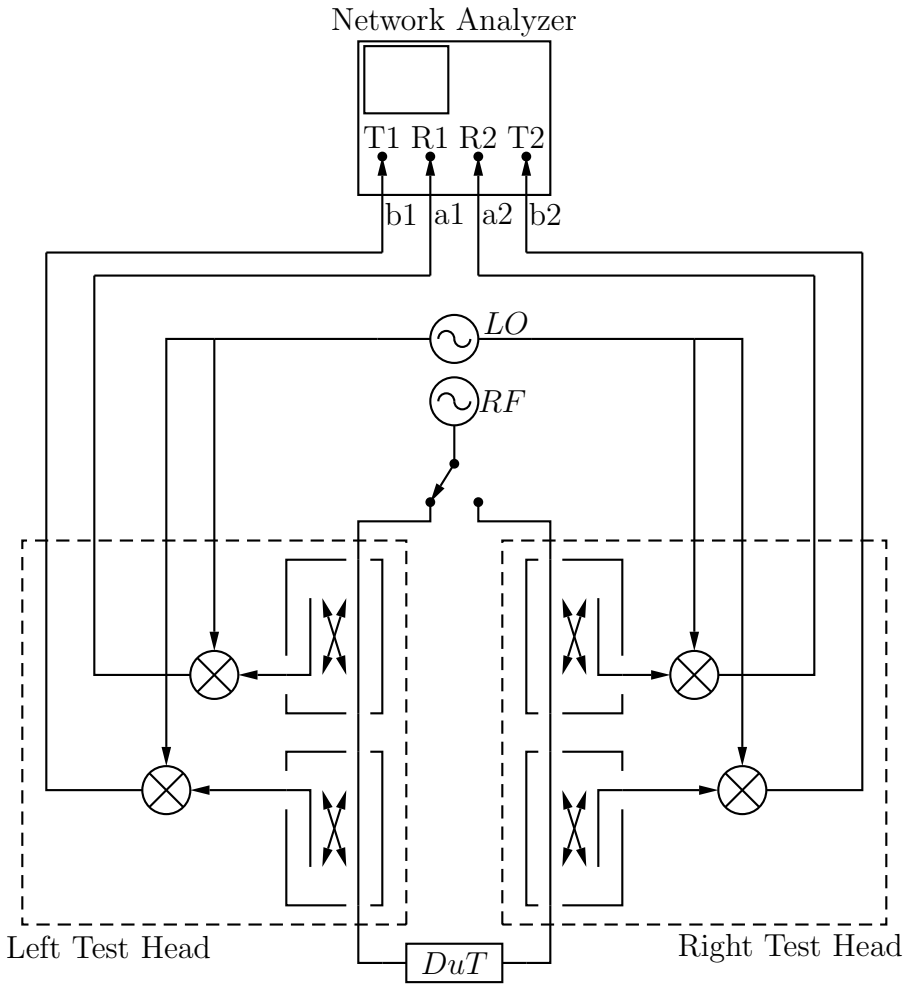


Figure B.11: Setup of the S-parameter measurement system [154] (the DC bias supply is not shown).

respectively defined as the cutoff frequency (f_{T}) and the maximum frequency of oscillation ($f_{\max}$).

Measure	Formal expression
Stability Factor	$K = \frac{1+\lvert\underline{S}_{11}\cdot\underline{S}_{22}-\underline{S}_{12}\cdot\underline{S}_{21}\rvert^2-\lvert\underline{S}_{11}\rvert^2-\lvert\underline{S}_{22}\rvert^2}{2\lvert\underline{S}_{12}\rvert\cdot\lvert\underline{S}_{21}\rvert}$
Maximum Stable Gain	$MSG = \left\lvert\frac{\underline{S}_{21}}{\underline{S}_{12}}\right\rvert$
Maximum Available Gain	$MAG = \left\lvert\frac{\underline{S}_{21}}{\underline{S}_{12}}\right\rvert \cdot (K - \sqrt{K^2-1})$
Unilateral Gain	$\mathrm{GU} = \frac{\left\lvert\frac{\underline{S}_{21}}{\underline{S}_{12}}-1\right\rvert^2}{2(K\cdot\left\lvert\frac{\underline{S}_{21}}{\underline{S}_{12}}\right\rvert-\mathrm{RE}(\frac{\underline{S}_{21}}{\underline{S}_{12}}))}$
Current Gain	$\underline{h}_{21} = \frac{-2\underline{S}_{21}}{(1-\underline{S}_{11})\cdot(1+\underline{S}_{22})+\underline{S}_{12}\cdot\underline{S}_{21}}$

Table B.1: Measures to be derived from S-parameter measurements.

B.4 Load-Pull Measurement

In section B.3 the RF properties of a device is characterized by means of S-parameter measurements. This measurement technique offers 50 Ω load and source impedances and feeds small-signals to the device in order to investigate the devices response as a function of the applied biasing conditions.

These restrictions are obstacles on the way to describe the devices RF behavior completely. Load-Pull measurements are a means to circumvent these limitations, i.e. the device can be investigated with matched source and load impedances and large-signals can be applied. As a result of Load-Pull measurements the output power (P_{out}), gain (G), and power added efficiency (η_{PAE}) of the device can be measured and extracted.

Setup The setup of the Load-Pull measurement system is as follows (see also illustration in figure B.12): A RF signal is generated by means of an oscillator (hp8350B Sweep Oscillator together with hp8359A Plug In [2.0 GHz - 20 GHz]) and sequentially amplified (hp495A Microwave Amplifier [7.0 GHz - 12.4 GHz]). The signal power can be modified additionally by means of two attenuators in series (controlled by Agilent11713A Attenuator/ Switch Driver).

The forward signal is then split by a direction coupler, coupling a power meter to measure the input power ($P_{\mathrm{out}}^{\mathrm{RF}}$, Channel A of hp438A Power Meter). A second direction coupler in line, which is sensitive to wave propagating in reverse direction, couples a power meter to measure the reflected power (P_{ref}, hp436A Power Meter). After having passed the coupling devices, the signal passes through a programmable tuner (Focus Microwaves Model 2604) and finally reaches the DuT input, which is connected to the measurement system by a RF probe station.

The output signal of the DuT is led to a second programmable tuner (Focus Microwaves Model 4006) and its power is measured by a power meter ($P_{\text{in}}^{\text{RF}}$, Channel B of hp438A Power Meter). Both the input and the output of the device are biased by a bias-T and a DC voltage supply. The programmable tuners are operated such that they form a matched circuit together with the DuT. A PC controls both tuners and records $P_{\text{out}}^{\text{RF}}$, $P_{\text{in}}^{\text{RF}}$, and the DC conditions.

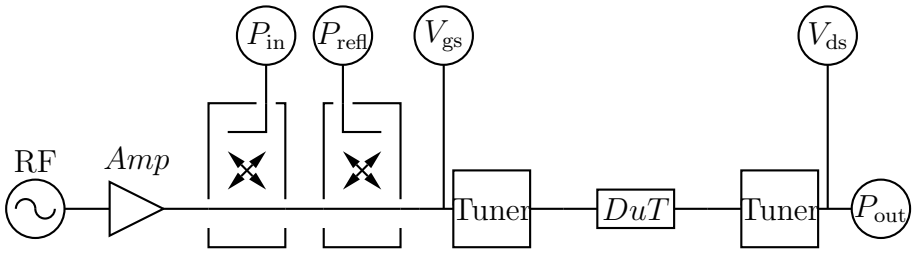


Figure B.12: Setup of the Load-Pull measurement system.

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List of Figures

List of Tables

Abbreviations

AC	alternating current
AFM	atomic force microscopy
BC – DLTS	backgating current deep level transient spectroscopy
CMOS	complementary metal-oxide-semiconductor
CV	capacitance-voltage
CVD	chemical vapor deposition
DC	direct current
DLTS	deep level transient spectroscopy
DuT	device under test
EBE	electron-beam evaporation
EOT	equivalent oxide thickness
EP	electronic polarization
FE	field emission
FET	field-effect transistor
FPIV	four-point current-voltage
FZJ	Forschungszentrum Jülich GmbH
GPIB	general purpose interface bus
GU	unilateral gain
HBT	hetero-bipolar transistor
HCl	hydrochloric acid
HEMT	high electron mobility transistor
HDiode	heterojunction diode
HFET	heterojunction field-effect transistor
IBE	ion beam etching
IBN	Institut für Bio- und Nanosysteme
IF	intermediate frequency
IS	impedance spectroscopy
ITRS	international technology roadmap for semiconductors
IV	current-voltage
LED	light emitting diode
LO	local oscillator
LP – MOCVD	low-pressure metal organic chemical vapor deposition
MESFET	metal-semiconductor field-effect transistor
MIS	metal-insulator-semiconductor
MISHDiode	metal-insulator-semiconductor heterojunction diode

MISHFET	metal-insulator-semiconductor heterojunction field-effect transistor
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MOVPE	metal-organic vapor phase epitaxy
PC	personal computer
PECVD	plasma-enhanced chemical vapor deposition
PLD	pulsed-laser deposition
PMMA	polymethylmethacrylat
PR	photo resist
RF	radio frequency
RTP	rapid thermal annealing
SCP	standard cleaning procedure
SEM	scanning electron microscope
SLP	standard lithography process
SMU	sense-monitor unit
SRR	side resist removal
TE	thermionic emission
2DEG	two-dimensional electron gas
TLM	transmission line model
UMTS	universal mobile telecommunications system
UV	ultra violet

Symbols

physical symbols:

η	basic efficiency
η_{PAE}	power added efficiency
$\eta_{\mathrm{PAE}^{\mathrm{max}}}$	maximum power added efficiency
μ	mobility
μ_0	low-field mobility
ν	carrier velocity
ν_{max}	maximum carrier velocity
ν_{sat}	saturation carrier velocity
χ	electron affinity
χ^{AlGaN}	electron affinity of AlGaN
χ^{GaN}	electron affinity of GaN
A	area
B	susceptance
C	capacitance
C'	capacitance per width
C_{gd}	gate-drain capacitance
$C_{\mathrm{gd}}^{\mathrm{insul}}$	gate-drain capacitance of insulator
$C_{\mathrm{gd}}^{\mathrm{HFET}}$	gate-drain capacitance of HFET
$C_{\mathrm{gd}}^{\mathrm{MISHFET}}$	gate-drain capacitance of MISHFET
C_{gs}	gate-source capacitance
$C_{\mathrm{gs}}^{\mathrm{HFET}}$	gate-source capacitance of HFET
$C_{\mathrm{gs}}^{\mathrm{MISHFET}}$	gate-source capacitance of MISHFET
C^{semic}	gate-source capacitance of semiconductor
C^{insul}	gate-source capacitance of insulator
C_{p}	gate-source capacitance in the context of diode CV measurements
C^{pad}	parasitic capacitance of pads
D	electric displacement
d^{AlGaN}	thickness of AlGaN layer
d^{semic}	thickness of semiconductor
d^{insul}	thickness of insulating layer
$d_{\mathrm{PECVD}}^{\mathrm{insul}}$	nominal thickness of insulating layer for PECVD deposition
$d_{\mathrm{EBE}}^{\mathrm{insul}}$	nominal thickness of insulating layer for EBE deposition
$d_{\mathrm{CVD}}^{\mathrm{insul}}$	nominal thickness of insulating layer for CVD deposition

$d_{\mathrm{CV}}^{\mathrm{insul}}$	thickness of insulating layer extracted from CV measurements
$d_{\mathrm{Imp.Spec.}}^{\mathrm{insul}}$	thickness of insulating layer extracted from impedance spectroscopy
$d^{\mathrm{GdScO_3}}$	thickness of $GdScO_3$ layer
$d^{\mathrm{SiO_2}}$	thickness of SiO_2 layer
d_{2DEG}	thickness of 2DEG
d_{ig}	distance between heterointerface and 2DEG
I	current
$I_{\mathrm{max}}^{\mathrm{rev}}$	maximum reverse current
$I_{\mathrm{max}}^{\mathrm{forw}}$	maximum forward current
E_{C}	energy level of lower conduction band edge
$E_{\mathrm{C}}^{\mathrm{AlGaN}}$	energy level of lower conduction band edge of AlGaN
$E_{\mathrm{C}}^{\mathrm{GaN}}$	energy level of lower conduction band edge of GaN
ΔE_{CBO}	conduction band offset
ΔE_{VBO}	valence band offset
E_{F}	fermi energy
E_{g}	band gap
E_{g}^{insul}	band gap of insulator
E_{g}^{oxide}	band gap of oxide
E_{g}^{semic}	band gap of semiconductor
E_{V}	energy level of upper valence band
E	electric field
ϵ_0	dielectric constant of vacuum
ϵ_{r}	relative dielectric constant
$\epsilon_{\mathrm{r}}^{\mathrm{AlGaN}}$	relative dielectric constant of AlGaN
$\epsilon_{\mathrm{r}}^{\mathrm{insul}}$	relative dielectric constant of insulator
f	frequency of oscillation
f_{T}	cut-off frequency
f_{max}	maximum frequency of oscillation
G	conductance
$G^{'}$	conductance per length
$Gain$	gain
g_{d}	output conductance
$g_{\mathrm{d,max}}$	maximum output conductance
$g_{\mathrm{d,mean}}^{\mathrm{sat}}$	mean output conductance in saturation region
g_{m}	transconductance
$g_{\mathrm{m,extr}}$	extrinsic transconductance
$g_{\mathrm{m,max}}$	maximum transconductance
$\underline{h}_{21}$	current gain
I_{d}	drain current
$I_{\mathrm{d,max}}$	maximum drain current
$I_{\mathrm{d,sat}}$	saturation drain current
I_{g}	gate current
j_{2DEG}	current density in 2DEG
$L^{'}$	inductance per length
L_{g}	gate length

MAG	maximum available gain
MSG	maximum stable gain
n	carrier concentration
n_{s}	sheet carrier concentration
$n_{\mathrm{s,max}}$	sheet carrier concentration at which mobility reaches maximum
$\underline{P}$	polarization
P_{in}	input power
$P_{\mathrm{in}}^{\mathrm{RF}}$	RF input power
P^{DC}	DC power
$P_{\mathrm{out}}^{\mathrm{RF}}$	DC output power
P_{out}	RF output power
p_{out}	output power density
R	resistance
$R^{'}$	resistance per length
R_{d}	drain resistance
R_{ds}	drain-source resistance
R_{input}	input resistance
R_{g}	gate resistance
R_{gs}	gate-source resistance
R_{s}	source resistance
$\underline{S}_{11}$, $\underline{S}_{12}$, $\underline{S}_{21}$, $\underline{S}_{22}$	scattering parameter
T_{bake}	temperature of bake
Δt_{bake}	duration of bake
Δt_{etch}	duration of etch
V_{break}	breakthrough voltage
$V_{\mathrm{break}}^{\mathrm{off}}$	off-state breakthrough voltage
V_{ds}	drain-source voltage
V_{gs}	gate-source voltage
V_{knee}	knee voltage, i.e. voltage at which I_{d} reaches maximum
V_{stress}	stress voltage
V_{th}	threshold voltage
$V_{\mathrm{th}}^{\mathrm{IV}}$	threshold voltage determined by IV measurement
$V_{\mathrm{th}}^{\mathrm{CV}}$	threshold voltage determined by CV measurement
W_{g}	gate width
$\underline{Z}$	complex impedance
$\underline{Z}_{\mathrm{L}}$	characteristic impedance

chemical symbols:

Ac	acetone
Al	aluminum
AlGaAs	aluminum gallium arsenide
AlGaN	aluminum gallium nitride
AlN	aluminum nitride
Al_3O_4	aluminum oxide
Al_2O_3	sapphire

Ar	argon
Au	gold
Cr	chrome
$DyScO_3$	dysprosium scandate
Dy_2O_3	dysprosium oxide
Fe	iron
Ga	gallium
GaAs	gallium arsenide
GaN	gallium nitride
Ga_2O_3	gallium oxide
Gd_2O_3	gadolinium oxide
$GdScO_3$	gadolinium scandate
HF	hydrofluoric acid
HfO_2	hafnium oxide
H_2	helium
H_2O_2	hydrogen peroxide
H_2O	water
InP	indium phosphite
KrF	krypton fluoride
MgO	magnesium oxide
N	nitrogen
Ni	nickel
NH_3	ammonia
NH_4OH	ammonium hydroxide
ScO_3	scandium oxide
Si	silicon
SiC	silicon carbide
Si_3N_4	silicon nitride
SiO_2	silicon oxide
Ti	titanium
TiN	titanium nitride
$(CH_3)_3Al$	trimethylaluminum
$(CH_3)_3Ga$	trimethylgallium
ZrO_2	zirconium oxide

List of Publications

[1] J. Bernát, D. Gregušová, G. Heidelberger, A. Fox, M. Marso, H. Lüth, and P. Kordoš, "SiO_2/AlGaN/GaN MOSHFET with 0.7 μm gate-length and f_{max}/f_t of 40/24 GHz," *Electronics Letters*, vol. 41, no. 11, pp. 667–668, 2005.

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Curriculum Vitae

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EDUCATION

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1995 - 2001	Study of Electrical Engineering and Information Technology, RWTH Aachen, focussed on Communications Engineering, external diploma thesis written at the ISI, ETH Zurich, graduated as Dipl.-Ing.
1991 - 1994	Secondary school (part II), Bremen
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1980 - 1990	Primary and secondary school (part I), Bremen

WORK EXPERIENCE

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