

Design and Analysis of Future Memories Based on Switchable Resistive Elements

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Preface

This dissertation arose during my work at the Institut für Werkstoffe der Elektrotechnik (RWTH Aachen) and at Forschungszentrum Jülich.

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Jakob Mustafa

June 2006

*Für meine Eltern,
meine Frau Lubna
und meine Tochter Lien*

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1. Introduction

The performance of information equipment, such as personal computers and workstations, is improving dramatically. This improvement was the main driving force behind new memory generations with very high capacities and very high speeds. Today we have memory capacities which were unimaginable some decades ago and the future may bring capacities which are unimaginable for us. Portable devices like PDAs, digital cameras, and smart cards require in the first place non-volatile memories with very high capacities.

Every advantage in some memory type is accompanied with one or more disadvantages. DRAMs have high capacities and relatively high speeds, but they are volatile and need to be refreshed every few milliseconds which raises their power consumption. SRAMs are the fastest memories but they are volatile and have the largest memory cell which reduces their capacities. Flash memories can have very high capacities and they are non-volatile but they are relatively slow.

None of the existing memory technologies satisfies all of the requirements simultaneously. It is therefore common practice to combine two or more types together to compensate weaknesses of any single type. This combination means that different chips have to be used in the system or different technologies have to be implemented on a single chip. This will add to the cost of the system or it may not be possible to combine several technologies together. Another important issue concerning memories is scalability which is determined by economic, technological, and physical limits.

A universal memory would be the solution for all or most memory problems. This memory would have a very high capacity, very high speed, very low power consumption and it would be non-volatile and scales better than existing technologies. Any new memory type with these specifications would face very hard challenges because it has to be superior to all well established technologies.

In the recent years, there have been great advances in the areas of new materials, nanotechnology, and molecular electronics. A universal memory can benefit and utilize these concepts. In the area of materials, resistive hysteretic switching (bi-stable or multilevel switching) has got a great attention. Resistive hysteretic materials change their resistance from one state to another according to an applied voltage and its polarity. A binary value or more are represented through the state of the material's resistance. This concept of data storing differs fundamentally from conventional concepts which are mainly charge based. It also scales better than existing technologies.

There is a great variety of resistive hysteretic materials which are still in the research phase. It

is still unknown which material is going to be the choice for the future. But all indications show that resistive memories are going to dominate.

A great advantage of resistive memories is that they can be scaled down into the nanometer range without scarifying their functionality. Nanotechnology is especially attractive for the constructions of very dense passive memory arrays with a very low cost. A passive memory array will always have higher densities and will be cheaper than an active memory array and it will be easier to manufacture. Nevertheless, passive arrays need more complex periphery circuits to control them in comparison to active arrays.

Resistive memories should not necessarily be made completely from new materials and technologies. As an intermediate solution, hybrid systems form current CMOS technology and the new technologies could be used. The next evolution step would be the combination of resistive materials with nano and molecular electronics.

Resistive memory elements can also be used to build logical functions. This is especially attractive for FPGA designs where lookup tables, which consist of static or non-volatile memory cells, can be replaced with resistive memory elements.

This work investigates utilizing hysteretic resistive elements in active and passive memories. Chapter 2 gives an overview of conventional memory technologies and emerging memory technologies. Chapter 3 is devoted for the analyses and simulation of resistive memories. In this chapter active and passive resistive memory designs are discussed. Some novel concepts concerning the design and optimization of resistive memories are also presented. Chapter 4 discusses the use of resistive elements to build logical functions in FPGAs.

This work was a part of the MOLMEM (Molecular Memory) which is a joint research project between Research Center Jülich, Research Center Karlsruhe, RWTH Aachen University, and Infineon. In this project, new materials and concepts for future memories were investigated.

2. Semiconductor Memories

Semiconductor memories exploit different physical states of a material or electronic device to represent information. Two well defined discrete states are needed at least to realize a memory function. The two states are assigned to the binary values “1” and “0”. Utilizing more states is also possible. In this case more than one bit of information can be stored in the same physical space.

Semiconductor memories are composed of three main architectural blocks: a cell array, a peripheral circuit, and an I/O unit circuit (Figure 1) [1].

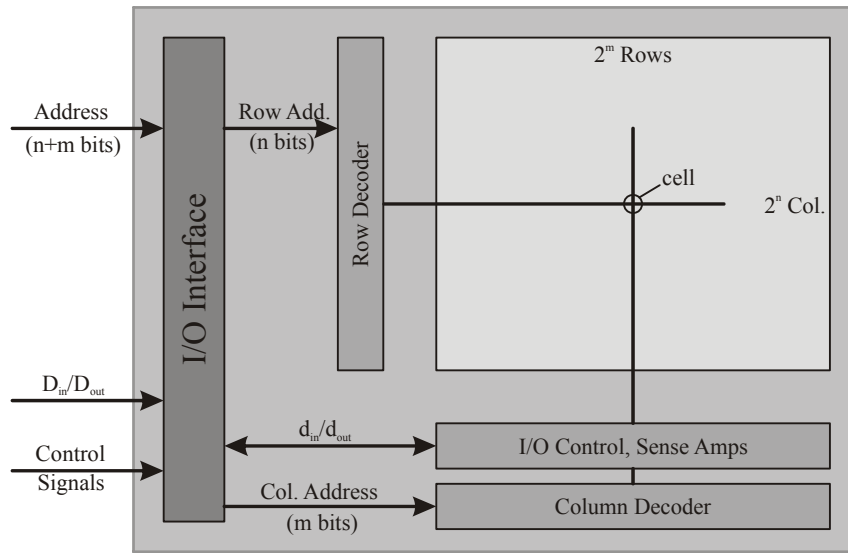


Figure 1: Memory architecture

The cell array contains the memory cells where the physical states are stored. The arrangement of the cells in an array structure reduces the number of control and sensing circuits since they are shared. An array comprising a matrix of 2^n rows and 2^m columns can store binary information of $2^{n+m+k-1}$ bits if each element can store k bits. Any cell can be accessed randomly by selecting its corresponding row and column. Memory arrays can be passive or active. Active memory arrays utilize an active element, typically a select transistor, to access the memory cell. In contrast, passive array memories lack an active element in the array.

The peripheral circuit is required to read and write the memory cells. This circuit includes address decoders, drivers, and sense amplifiers. The later is used to decide the states stored in the cells. The peripheral circuitry plays the role of a bridge between the memory cells and the I/O unit.

The I/O circuit is the interface of the memory to the external world. This block converts external input signals such as addresses, data inputs, clock, and control signals to the corresponding internal signals that control the peripheral circuit. It also converts internal signals to external signals as in the case of reading information from the memory.

There are several criteria, whereby semiconductor memories can be classified. For example, they can be classified according to the mechanism used to store information; like charge or polarization or resistance, or according to the material system used, or architecture, and so on. A common classification for memories concentrates on the write operation; like how fast a memory can be written to, or how many times write can be performed as can be seen in Figure 2.

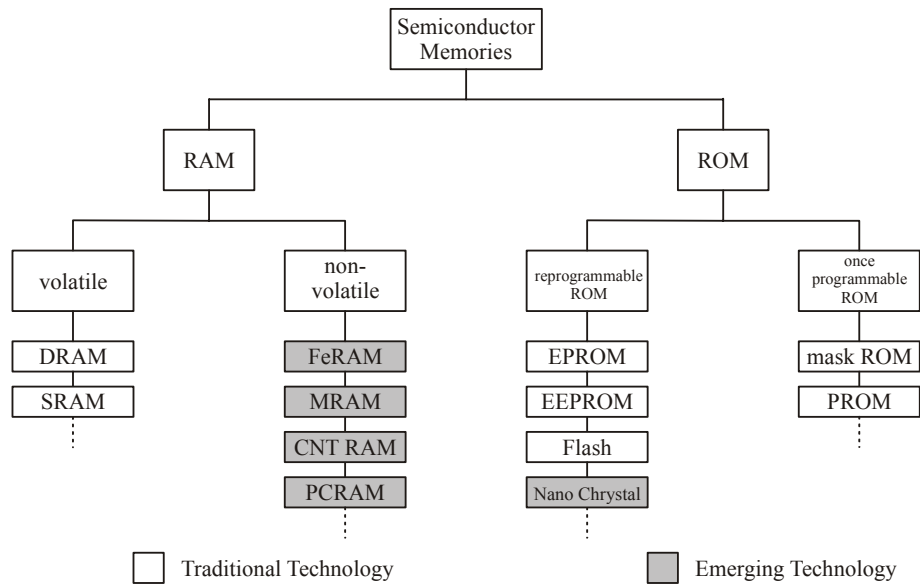


Figure 2: Categories of Semiconductor Memories

Following this classification, semiconductor memories can be categorized in random access memory (RAM) or read only memory (ROM). In RAMs, information is read from or written to any location of the memory with virtually no limit on the number of reads and writes, whereas it can be written only once or few times and read unlimitedly in a ROM. Additionally, writing and reading speeds are almost identical in RAMs but they are very different in ROMs, since writing takes much more time than reading.

The unshaded parts in Figure 2 represent standard well established memory technologies, while the shaded parts represent new emerging technologies. As can be seen, most of the emerging technologies fall under the category of RAM memories.

All standard memory technologies and most of the emerging memory technologies are from the active array type. Only few types of the emerging memories comprise passive arrays. Both approaches have advantages and drawbacks. Active memories tend to be faster and have

larger memory arrays but they face limits because of scaling problems and manufacturing complexity imposed on semiconductor devices. Alternatively, passive arrays can be scaled aggressively and can be manufactured by relatively simple means, which makes them more suitable for future nanotechnologies. Passive arrays suffer from high cross talking between array elements, which limits their array size severely and complicates reading and writing. In the following sections, conventional and emerging technologies are discussed in more detail.

2.1 Conventional Memory Technologies

Traditional memories are memories that use well established technologies and have been around for many years. The main principle of their function did not change over the years. They include volatile memories, once-programmable ROM memories, and most types of reprogrammable ROM memories.

2.1.1 Volatile Memories

According to Figure 2, RAM can be further classified as volatile and non-volatile. A volatile memory loses the stored information if the power supply is turned off, which is the case in dynamic random access memories (DRAMs) and static random access memories (SRAMs).

2.1.1.1 DRAM

The memory cell of a DRAM consists of a transistor connected in series to a storage capacitor as seen in Figure 3. The bitlines of vertically adjacent cells are connected together as well as the wordlines of horizontally adjacent cells. Information is stored as a charge on the cell capacitor. The presence of a charge represents the logic value “1” and its absence the logic value “0”. DRAMs have a low access time and very high density, which makes them suitable as main memories for digital devices.

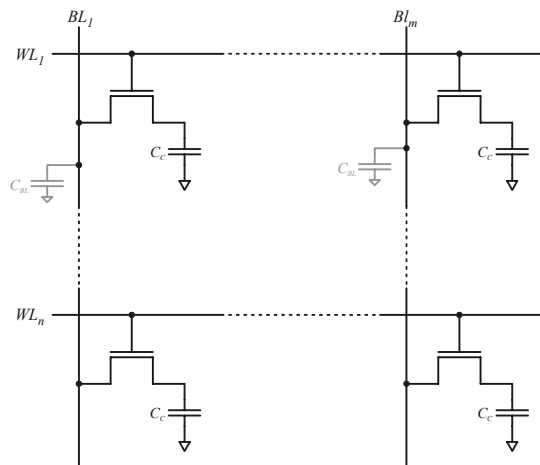


Figure 3: DRAM memory cell array

Data is written to a cell by holding the bit line at V_{DD} or GND ; afterwards, the cell transistor is activated, which causes the cell capacitor to be charged to V_{DD} or discharged to GND respectively as illustrated in Figure 4.

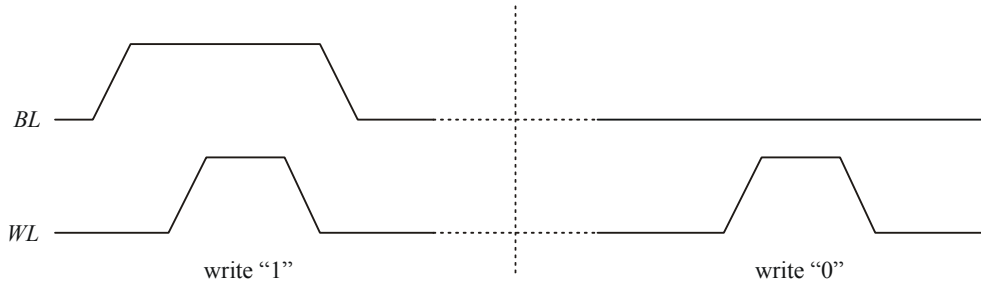


Figure 4: DRAM write operation

Reading is carried out by charging the parasitic capacitance of the bitline (C_{BL}) to $V_{DD}/2$ then disconnecting it from the bitline driver which makes it float (Figure 5).

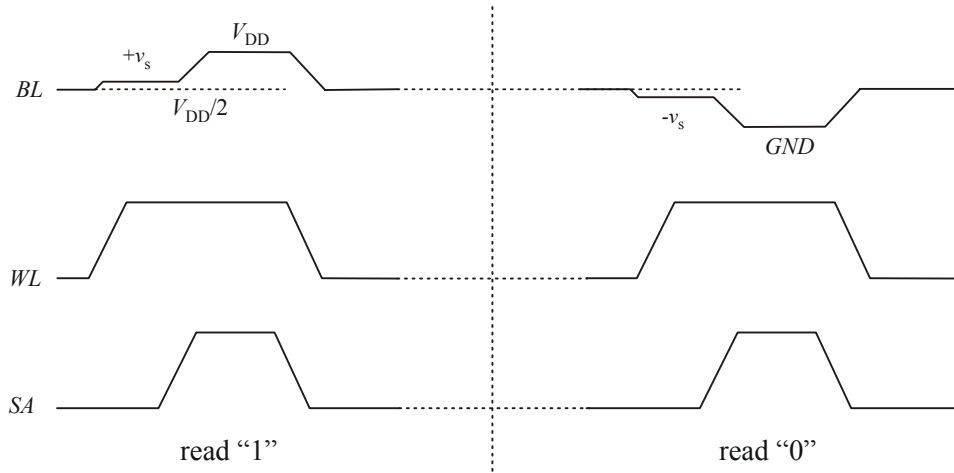


Figure 5: DRAM read operation

After that the cell transistor is activated. As a result, the charge on the cell capacitor and the parasitic capacitance of the bitline will be shared. Depending on the state of the cell capacitor, the bit line voltage would be raised or lowered by v_s . The voltage difference on the bitline before and after charge sharing ($\pm v_s$) is expressed as:

$$v_s = \frac{V_{DD}}{2} \cdot \frac{C_c}{C_c + C_{BL}} \quad (1)$$

The voltage at the bitline is compared to a reference voltage using a sense amplifier, which is activated by the signal SA . The sense amplifier decides whether a “0” or a “1” is stored in the cell. According to the decision, the sense amplifier sets the level of the bitline to V_{DD} or to GND to perform information write back.

Since the cell capacitor is not ideal, leakage current in the capacitor will lead to discharging the cell capacitor within few milliseconds and the information will be lost. To solve this

problem, all cell capacitors have to be refreshed before the charge falls to a level, which is not more detectable. This means, that after storing the information and while the charge is still detectable, the information is read and then written back to the memory cells.

2.1.1.2 SRAM

An SRAM cell is essentially a flip-flop circuit as can be seen in Figure 6. The nodes N1, N2 have either the voltages V_{DD} and GND , or GND and V_{DD} respectively. In the first case, the cell contains a “1” and in the second case a “0”. To store “1” in the cell, BL is hold at V_{DD} and BLB at GND and the transistors T5 and T6 are activated by the wordline (WL). This will disturb the cell for a short time, after which the new state will be programmed. Storing a “0” is similar, but this time the voltages on BL and BLB are exchanged.

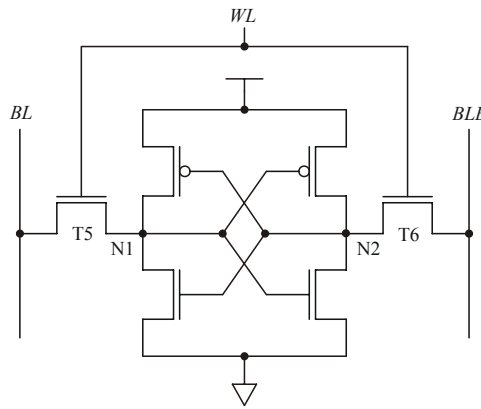


Figure 6: SRAM memory cell

The read operation is performed by detecting the polarity of a differential signal voltage developed on the data lines BL and BLB . No refresh operation is needed because the leakage currents at N1 and N2, if any, are compensated by a static current from the power supply, as long as V_{DD} is supplied. Compared to DRAMs, SRAMs have a much larger cell area but their access time is much shorter. For this reason SRAMs are used where access time is critical like in caches or supercomputer memories.

2.1.2 Programmable Memories

ROMs can be classified as once-programmable or reprogrammable devices. As the name indicates, a once-programmable memory is programmed once during fabrication (mask-based ROM) or after fabrication (programmable read only memory: PROM). Reprogrammable ROM devices, on the other hand, can be erased after having been programmed by exposing them to ultraviolet light in case of erasable programmable read only memory (EPROM) or by electrical means in case of electrically erasable read only memory (EEPROM). All cells in an

EPROM are erased simultaneously, whereas they are erased byte-wise in EEPROMs or block-wise in Flash memories.

2.1.2.1 Mask ROM/PROM Memories

Programming during fabrication is carried out by patterning the last metallization layer to define which memory cells are connected or disconnected to represent a “1” or a “0” as seen in Figure 7.

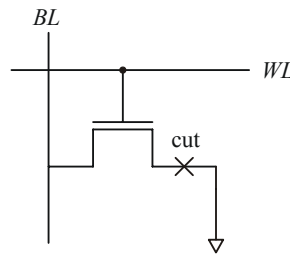


Figure 7: Mask ROM cell

In a PROM, the memory cells are always connected to *GND* through tiny fuses after fabrication. The connections can be broken by blowing the fuses. As it was the case by ROMs, the existence or non existence of a connection defines whether a “0” or a “1” is stored. Blowing a fuse is irreversible, which makes rewriting impossible.

2.1.2.2 EEPROM/Flash Memories

EEPROMs and Flash memories are very similar. The main difference between them is that EEPROMs can be erased and programmed byte-wise but Flash memories are programmed and erased block-wise. EEPROMs require a memory cell consisting of two transistors whereas only one cell transistor is required in flash memories. In general, flash memories have replaced EEPROMs because their cell size is smaller and they can have very large capacities.

The memory cell of a flash memory comprises a single MOS transistor with an additional floating gate as seen in Figure 8. The threshold voltage of the transistor is shifted depending on the trapped charge in the floating gate.

The floating gate is electrically isolated from its environment. But still it can be charged and discharged. The two typical mechanisms to transfer electric charges from and into the floating gate are the hot electron injection and the Fowler-Nordheim tunneling. Electrical charge transfer is carried out during writing only. The threshold shift due to the electric charge is expressed as:

$$\Delta V_T = -\frac{\Delta Q_{FG}}{C_{FC}} \quad (2)$$

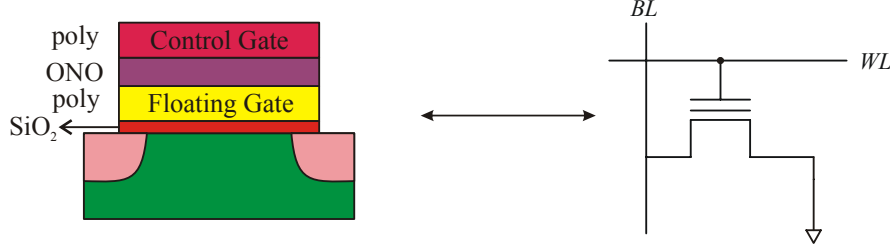


Figure 8: Flash memory cell

where ΔQ_{FG} is the shift of the floating gate charge and C_{FC} is the capacitance between the floating gate and the control gate. To read the cell, a voltage V_r , which is higher than low threshold and lower than the high threshold, is applied at the gate of the transistor as shown in Figure 9. If the cell has a low threshold voltage, current will flow in the transistor which will indicate that the stored value is “1”; otherwise, if the cell’s threshold is higher than the applied voltage, no current will flow which means that the cell contains a “0”.

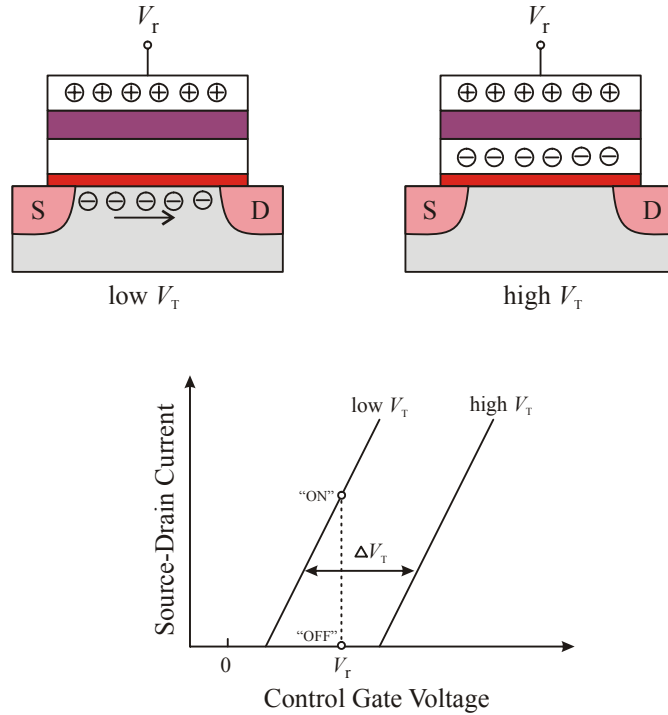


Figure 9: Flash memory read operation

2.1.2.3 Nitride Storage Memories

Scaling the tunnel oxide thickness of flash memory devices causes reduced reliability and data retention. The replacement of the floating gate with a localized trapping material can help alleviate this problem because only localized discharging takes place in the presence of oxide defects. SONOS (oxide-silicon nitride-tunnel oxide-silicon) flash memory cells have been proposed for years. The carriers are stored in the traps of the nitride layer between top and bottom oxide as shown in Figure 10 [2].

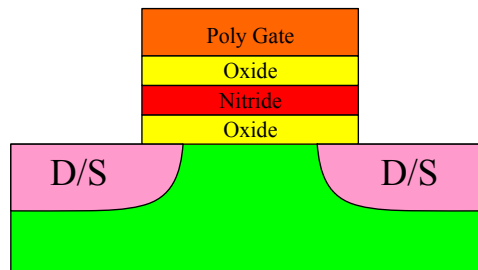


Figure 10: SONOS flash memory cell

SONOS cells offer several advantages over conventional floating gate memory cells like ease of manufacturing, insensitivity to oxide defects, and the non existence of floating gate coupling effect. However, the cell retention, the cell size and slow program/erase speed are still an issue. Recently SONOS cells have evolved into a 2-bits storage architecture (Multi-Bit Cell) by utilizing the localized charge trapping effect of nitride, which enables a memory cell to hold twice as much data as a standard memory cell, without compromising device endurance, performance or reliability. Figure 11 shows where the two bits are stored in such a cell. Trapped charge memories can be used in either NOR or NAND memory architectures.

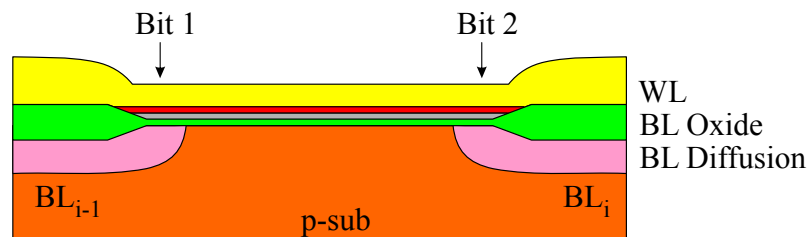


Figure 11: Storing 2 bits in one memory cell

Among numerous proposed cell architectures, NROM [3] and PHINES [4] are the most promising multi-bit cell Technologies. The structure of the two types is similar as can be seen in Figure 12.

The main difference between NROM and PHINES is the way they are programmed and erased [5]. The NROM is programmed using channel hot electron injection (CHE) and is

erased using hot hole injection which is generated by band to band tunnelling (BTBT HH), whereas the PHINES is programmed using BTBT HH of hot holes and is erased by Fowler-Nordheim tunnelling.

Table 1 shows the programming and reading scheme of an NROM cell. V_g , V_d , and V_s are the voltages of the gate, drain, and source respectively. As can be noticed the drain and source of the cell transistor are interchanged to perform reading and writing of the two bits. The device is read in the “reverse” direction compared to programming, by applying the read biases to WL (3 V) and left junction (1.5 V), and grounding the right junction. This reverse read maximizes the effect of the trapped charge on the window [5].

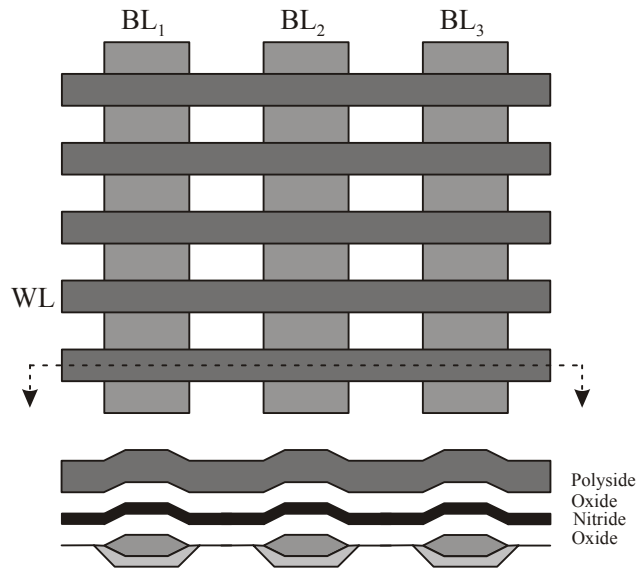


Figure 12: NROM and PHINES array structure

		Program (CHE)	Erase (BTBT HH)	READ (Reverse)
Bit 1	V_g	11V	-3 V	3 V
	V_d	5 V	7 V	0 V
	V_s	0 V	0 V	>1.5 V
Bit 2	V_g	11 V	-3 V	3 V
	V_d	0 V	0 V	>1.5 V
	V_s	5 V	7 V	0 V

Table 1: Typical bias conditions for program, erase, and read in a NROM cell

2.1.2.4 Multi Level Flash Memories

Usually, one bit of information is stored on the floating gate of a flash memory. According to the stored charge on the floating gate, the threshold voltage of the cell transistor is shifted as can be seen in Figure 13a. In the case of the multi level cell, two bits of information can be stored on the floating gate of the cell transistor. To achieve this, four states of charges are needed as seen in Figure 13b.

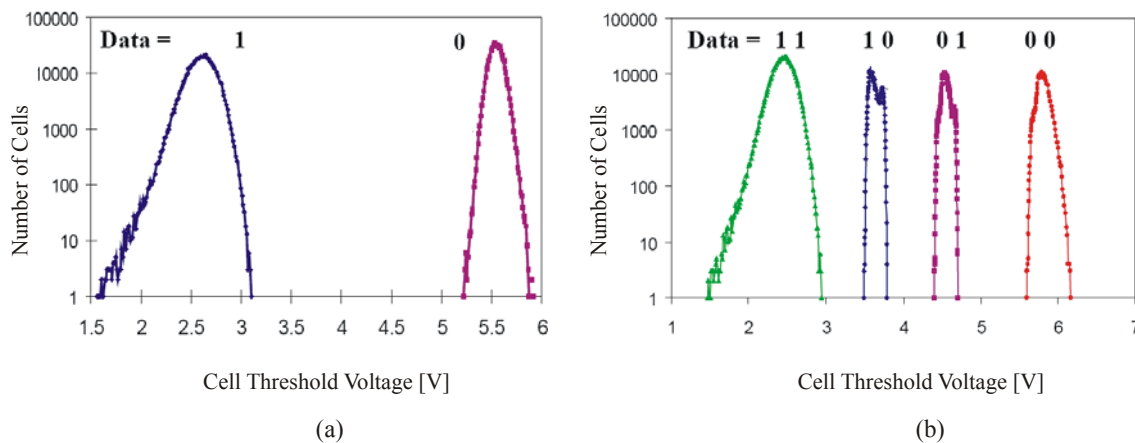


Figure 13: Single bit/cell array threshold voltage histogram [6]

Precision is the key to store two bits per cell. Programming a cell (charge placement) and reading (sensing) must be precisely controlled in order to have four states within a single transistor. Higher bit per cell densities are possible by even more precise charge placement control. Three bits per cell would require eight distinct charge states.

2.2 Emerging Memory Technologies

Almost all the emerging memory types are non-volatile memories. There is a great number of new memory concepts and materials that have been developed to replace conventional memory technologies. These emerging technologies focus on developing a universal memory which replaces all previous memory types. Future memories are non-volatile and reliable, additionally they have very high capacities, low power consumption, and very high data transfer rates.

2.2.1 FeRAM

Ferroelectric materials are characterized by reversible spontaneous polarization of a certain class of materials. There are a wide variety of crystals that show this kind of behavior like $\text{PbZr}_{1-x}\text{Ti}_x\text{O}_3$ (PZT), $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT) and $(\text{Bi,La})_4\text{Ti}_3\text{O}_{12}$ (BLT) [7, 8].

Spontaneous polarization arises due to noncentrosymmetric arrangement of ions in their unit cells which produces a permanent electric dipole moment associated with the unit cell. Adjacent dipoles also tend to orient themselves in the same direction to form a region called ferroelectric domain. The polarization response with the electric field of these materials is highly non-linear and exhibits a hysteresis loop as shown in Figure 14, which shows a perovskite unit cell of a ferroelectric material and a typical hysteresis curve.

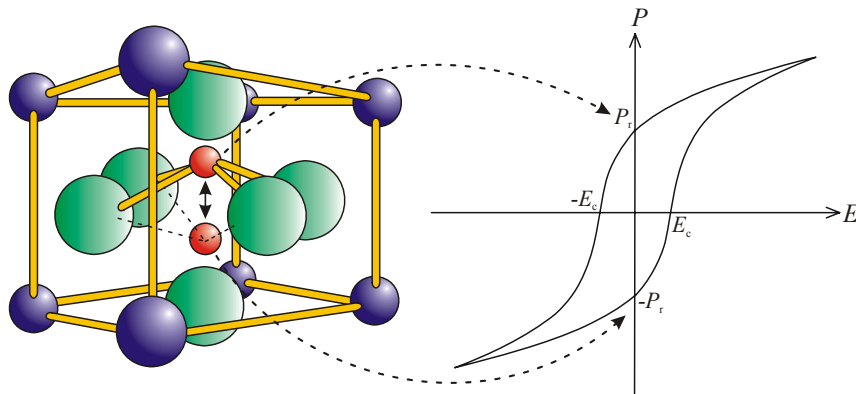


Figure 14: Ferroelectric unit cell and hysteresis loop

As applied electric field is increased, the ferroelectric domains which are favorably oriented with respect to the electric field grow at the expense of other domains. This continues until total domain growth and reorientation of all the domains is reached in a direction favorable to the external field. At this stage the material has a saturated polarization. If the electric field is removed at this point some of the domains do not reorient into a random configuration, thus leaving the material still polarized. This polarization is known as remnant polarization P_r . The

strength of the electric field required to return the polarization to zero is called the coercive field E_c . The net direction of the polarization is in the direction of the external electric field. If a capacitor configuration is used, two states of polarization can be achieved according to the applied field on the capacitor plates. From a digital point of view these two states can correspond to a stored '0' or '1'.

Ferroelectric materials can be used with a variety of memory architectures which are closely related to conventional memories like DRAM and Flash memories. A 1T-1C ferroelectric memory cell is shown in Figure 15.

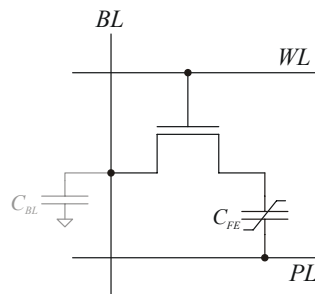


Figure 15: 1T-1C ferroelectric memory cell

This cell is similar to a DRAM cell with the exception of the plateline (PL) which has a variable voltage level to enable the switching of the polarization of the ferroelectric capacitor (FeCAP), whereas its level is fixed in a DRAM. To write a "1" in the cell, the BL is set to V_{DD} and the PL is grounded, then a pulse is applied at the wordline (WL) to activate the cell transistor (Figure 16a). Writing a "0" is accomplished in the same manner but this time the polarities of BL and PL are exchanged to reverse the polarization of the FeCAP (Figure 16b).

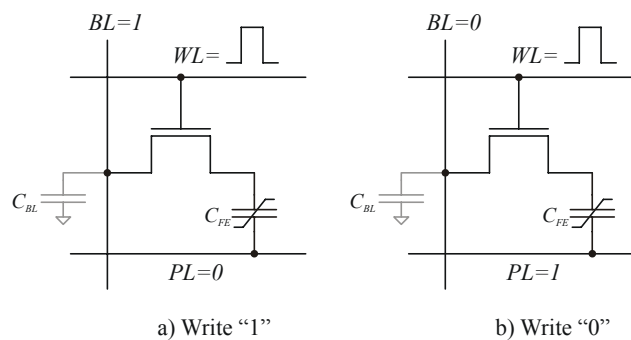


Figure 16: FeRAM write operation

Another possible architecture is the chain FeRAM (CFeRAM) [9] where the cell transistor and capacitor are connected in parallel and the cells are connected in series. Figure 17 shows two cell blocks of this memory type.

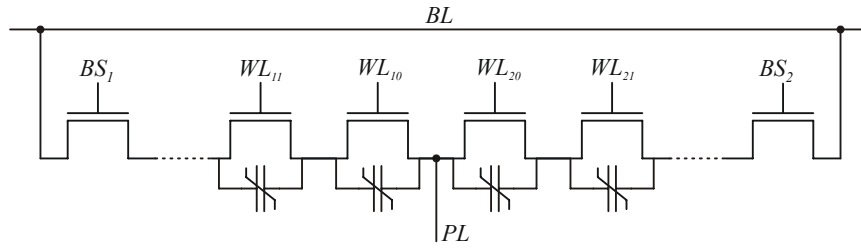


Figure 17: Chain FeRAM

This architecture is similar to that of a NAND-Flash and can achieve higher densities than the 1T-1C architecture but has a longer access time. In contrast to the conventional 1T-1C cell, accessing a CFerAM cell is accomplished by grounding the cell's WL and applying V_{DD} to all other neighboring cells, which short-circuits their corresponding FeCAPs. The voltage difference between BL and PL will only be dropped on the selected cell.

To read the content of the memory cell first the BL is grounded, then it is made floating, which means that it effectively represents a capacitance C_{BL} . After that the cell is selected by WL . Then PL voltage is raised from GND to V_{DD} . This would raise the voltage of BL in dependence of the polarization (data) stored in the FeCAP and the capacitance C_{BL} .

Other cell architectures like the 2T-2C [9, 10] cell and the 1T cell (FeFET) are possible. In a 2T-2C cell one bit is stored in two capacitors that always have opposite polarizations. Despite the fact that this cell type is very reliable, it is not attractive because of the cell size which is twice the size of a 1T-1C cell. A 1T cell (FeFET) is in principle a MOSFET transistor whose gate dielectric is ferroelectric. An advantage of this cell type is that the reading operation is nondestructive but the main disadvantage is the fact that the current achievable retention time is very short to be used in a nonvolatile memory [11]. A ferroelectric memory diode where the diode resistance is modulated through a ferroelectric effect has also been reported [12, 13].

2.2.2 MRAM

The development of magnetoresistive random access memory (MRAM) has been based on a number of significant ideas over the past 20 years, starting with Cross-tie Random Access Memory (CRAM) [14, 15] and continuing with new configurations. All types of MRAM use magnetization direction for information storage and the resultant resistance difference for information readout. The change of resistance of a material due to a magnetic field is called magnetoresistance. The magnetoresistance ratio is the quotient of the difference between maximum and minimum resistance values and the minimum resistance value.

There are three types of magnetoresistance. The first type is the anisotropic magnetoresistance

(AMR), which is the change in resistance with the angle between the magnetization and the electric current in a ferromagnetic metal. Figure 18 illustrates the method of data storage in the MRAM cell using AMR. The cell consists of two ferromagnetic films sandwiching a poor conductor, with the composite film etched into stripes as shown. A current through the stripe magnetizes magnetic material clockwise or counterclockwise when aided by a current (field) from an orthogonal strip line. Current in either strip by itself would not change the storage state. Thus, a single memory cell could be selectively written in a 2D array.

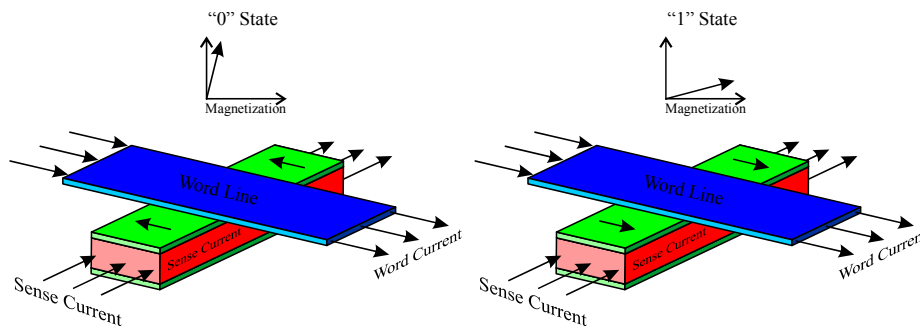


Figure 18: MRAM with AMR cell

Reading of this cell depends on the differential resistance of the cell, when a sense current is passed through it. Because the sense current creates a magnetic field which opposes the magnetization in one storage state, but has the same direction in the other state, the angle of rotation is different for a “1” or “0”. The magnetoresistance ratio of this cell type is about 2%.

Despite improvements in reading methods [16], the maximum differential resistance of this cell when it is read is about 0.5%. In real arrays with practical sense currents, this gives differential sense signals of 0.5 to 1.0 mV. These sense signals allowed 16K bit integrated MRAM chips to operate with a read access time of about 250 ns [17]. The write time for the MRAM was 100 ns.

The second type of magnetoresistance is the giant magnetoresistance. In this type data is stored in magnetic multilayer and the giant magnetoresistance (GMR) effect is used to read the stored data. This type has three times improvement of magnetoresistance than AMR and nine times improvement in reading access time. There are two types of devices that use the giant magnetoresistance effect, which are the spin valve (Figure 19) and the pseudo-spin valve devices (Figure 20).

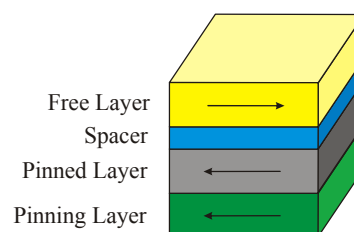


Figure 19: spin valve

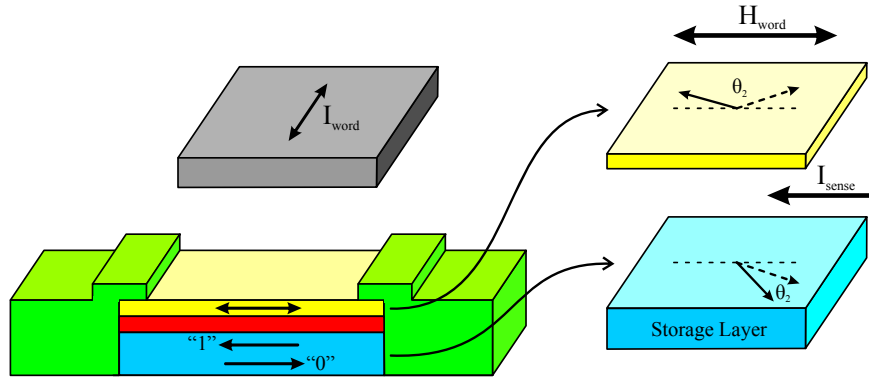


Figure 20: Pseudo spin valve

The third type of magnetoresistance uses spin dependent tunneling (SDT) or magnetic tunnel junction (MTJ) (Figure 21). These devices provide higher percentage magnetoresistance than AMR or PSV structures, and thus have the potential for higher signals and higher speed. SDT tunneling can achieve over 40% magnetoresistance [18, 19] compared to 6-9% magnetoresistance in good PSV cells.

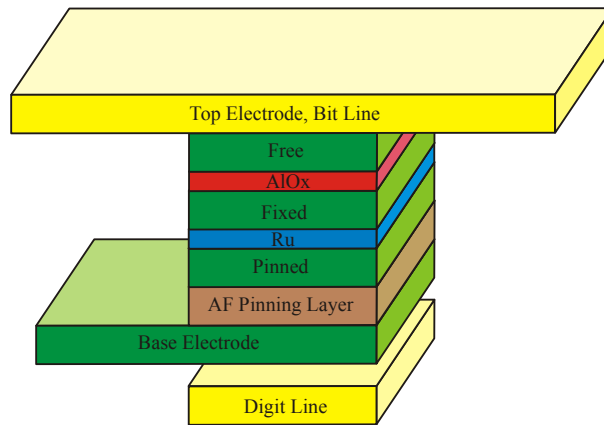


Figure 21: MTJ

Two types of architectures can be implemented using magneto resistive elements. Active architectures use one transistor and one magnetic resistive element and have a high performance. Passive architectures use a cross point memory architecture which has a high density.

2.2.3 Ovonic Unified Memory (OUM)/Phase change Memory (PCRAM)

PCRAM relies on phase transitions induced by nanosecond-scale heating and cooling of small volumes of chalcogenide films within the memory cell [20]. New chalcogenide alloys have been developed that are highly resistive semiconductors in the amorphous phase and highly conductive semimetals in the crystalline phase ($\text{Ge}_2\text{Sb}_2\text{Te}_5$ -GST) [21]. A two-terminal

memory element implementing the chalcogenide material can be fabricated. It operates by converting a small volume of the chalcogenide material back and forth between the crystalline and amorphous phases (Figure 22).

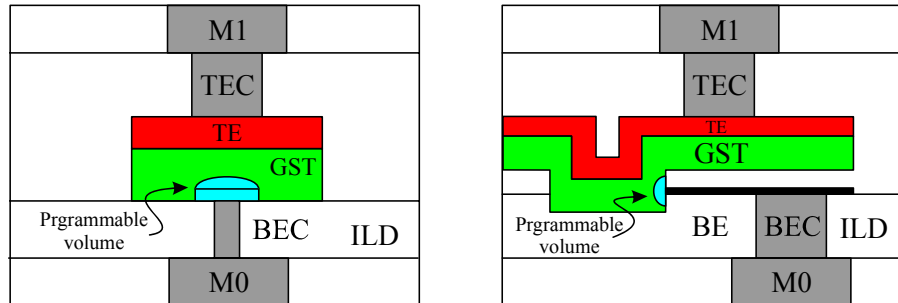


Figure 22: Two types of PCRAM cells

Phase conversion is accomplished by appropriate heating and cooling of the material. Once the chalcogenide material melts, the material loses all crystalline structure, and rapid cooling of the material to below its glass transition temperature causes the material to be locked into its amorphous phase. The amorphous phase is very stable near room temperature, but the rate of nucleation and growth of crystallites increases exponentially as the melting temperature is approached. To keep the material from recrystallizing during cooling, the cooling rate must be faster than the crystal nucleation and growth rate. To switch the memory element back to its conductive state, the material is heated to a temperature between the glass transition temperature and the melting temperature, causing nucleation and crystal growth to rapidly occur over a period of several nanoseconds [20]. This programming scheme is described in Figure 23.

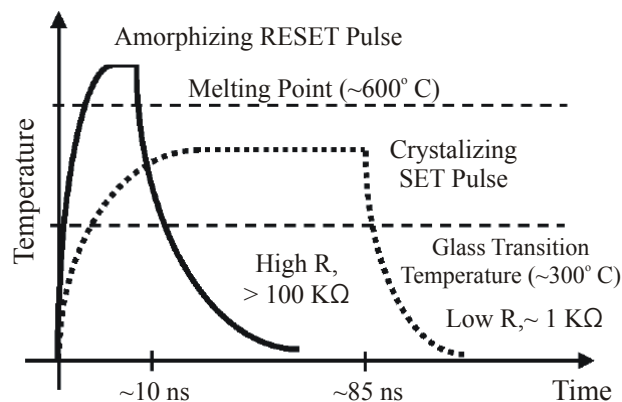


Figure 23: Typical cell cooling schedule [22]

There are three modes of operation for accessing a PCRAM memory element:

- Read:

The electric field is limited by applying a low voltage. A small current will pass if the material is in the amorphous state; in the crystalline phase, the applied voltage and the resistance of the contact will limit the current through the device. A ratio of two orders of magnitude is observed between the two currents allowing a very fast read circuit with high noise immunity to be implemented [20].

- Set:

The voltage must be high enough to ensure that the alloy will switch into a low impedance state. An intermediate current level will heat the material but not melt it. When the material is in the amorphous state, its resistance is too high to allow any significant current to pass. As a result, it would seem that when the material is in the amorphous phase that it would be difficult to pass sufficient electric current through the film in order to provide the necessary heat to alter the material's phase back to its crystalline state. However, when an electric field of approximately $3 \cdot 10^5 \text{ Vcm}^{-1}$ is applied, Poole-Frenkel conduction, combined with device heating, lowers the material's resistance and switches the chalcogenide film into a low impedance state that persists until the pulse is removed and the material cools [23].

- Reset:

The voltage must be high enough to ensure that the alloy will switch into a low impedance state with sufficient current to heat a portion of the material above its melting temperature. When the current is removed, the small volume of material that has melted will rapidly quench into the amorphous state.

In an array construction, either a transistor or a diode is required for switching the memory element (Figure 24). In order to achieve the smallest cell size, the diode selection device is preferred [24]. Given the fact that one is trying to sense change in resistance, parasitic series resistance as well as leakage current are very important.

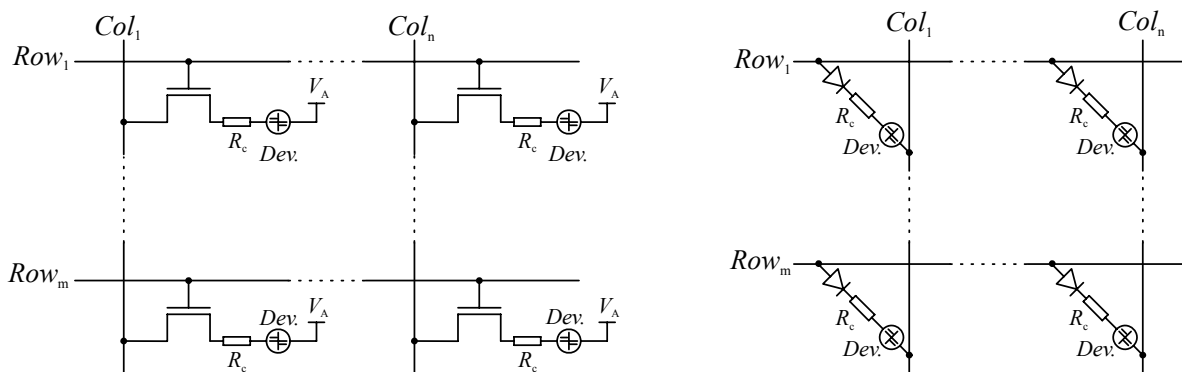


Figure 24: PCRAM transistor and diode array

The reset current of the cells and the thermal disturbs between adjacent cells are a concern for PCRAMs. Current studies show no significant thermal cross talking is expected at the 65 nm technology node. The reset current can be scaled down almost linearly by reducing the device

contact area [21]. The scaling projection shows that there are no physical limits to scaling down to the 22 nm node with a number of technical challenges being identified [24]

2.2.4 Conductive Bridge RAM (CBRAM)/Programmable Metallization Cell (PCM)

Programmable metallization cell memory utilizes electrochemical control of nanoscale quantities of metal in thin films of solid electrolyte [25]. Key attributes are low voltage and current operation, excellent scalability, and a simple fabrication sequence. Device formation involves the dissolution of silver or copper in a chalcogenide (e.g., germanium selenide, germanium sulfide) or oxide (e.g. tungsten oxide) base glass to form a solid electrolyte. A silver- or copper-containing layer and an inert electrode formed in contact with the electrolyte film creates a device in which information is stored via electric changes caused by the oxidation of the silver or copper metal and reduction of silver or copper ions in the electrolyte. These reactions result in stretching or shrinking of a metallic bridge, thereby creating or dissolving an electrically conductive channel [26] as can be seen in Figure 25. This occurs at an applied bias of a few hundred millivolts and can result in a resistance change of many orders of magnitude within a few tens of nanoseconds. A reverse bias of the same magnitude will reverse the process until the electrodeposited metal has been removed, thereby erasing the device [27, 28]. Sometimes this memory type is called conductive bridge random access memory (CBRAM) or solid electrolyte memory.

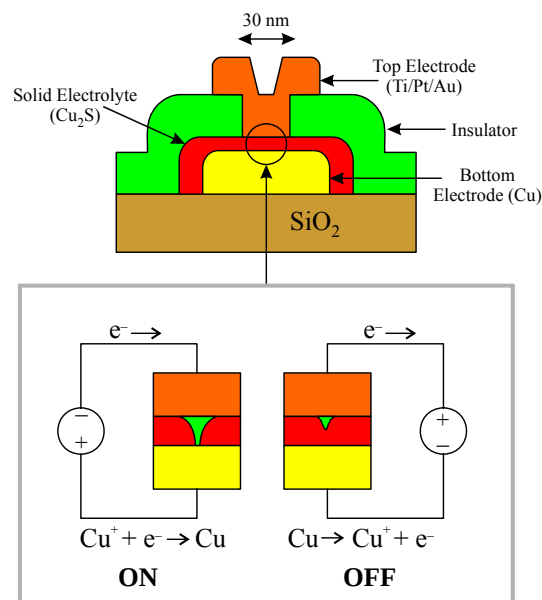


Figure 25: CBRAM structure, programming, and erasing

2.2.5 Polymeric Ferroelectric Memory (PFRAM)

This type of memory uses a thin film capacitor made from a polymeric ferroelectric material which has a dipolemoment (Figure 26). The data is stored by changing the polarization of the polymer [29].

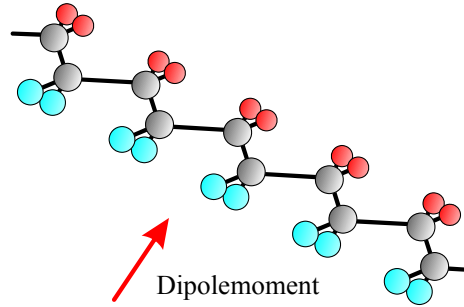


Figure 26: Polymeric ferroelectric material

The access and storage times of these memories is relatively slow which makes it compete rather with flash memories than with other emerging technologies. The polymer material is used in passive memory matrices where no access transistor is used. Moreover, up to eight layers can be stacked to make a high bit density microchip (Figure 27). The lack of an access transistor impose high demands on the ferroelectric properties of the polymer. Especially a sufficient squareness and a high stability of the hysteresis loop are required.

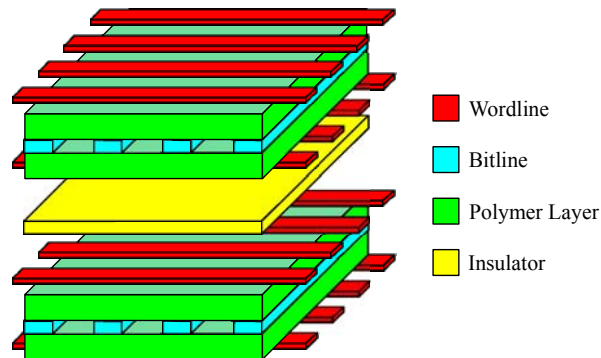


Figure 27: Polymeric ferroelectric stacked layers

2.2.6 Carbon Nanotube Memory (NRAM)

The basic design of the NRAM device consists of a suspended monolayer fabric of single walled nanotubes (SWNTs) as an electromechanically switchable, bi-stable device with well-defined “off” and “on” states (Figure 31) [30].

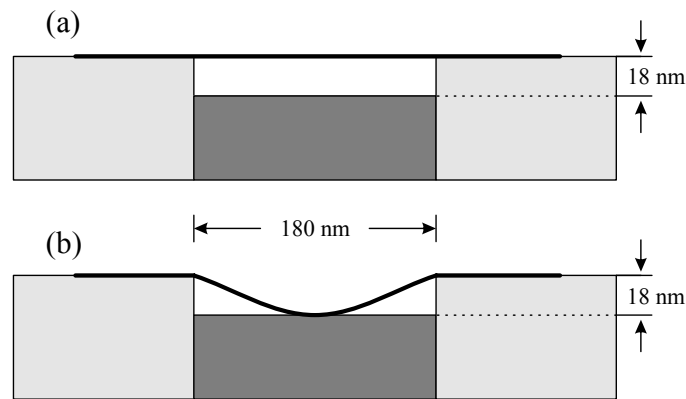


Figure 31: (a) SWNT “off” state, (b) SWNT “on” state

As shown in Figure 32, bistability arises from the interplay of the elastic energy, which produces a potential energy minimum at finite separation (when the nanotube fabric is freely suspended), and the attractive van der Waals energy, which creates a second energy minimum when the suspended SWNTs are deflected into contact with the lower actuating electrode.

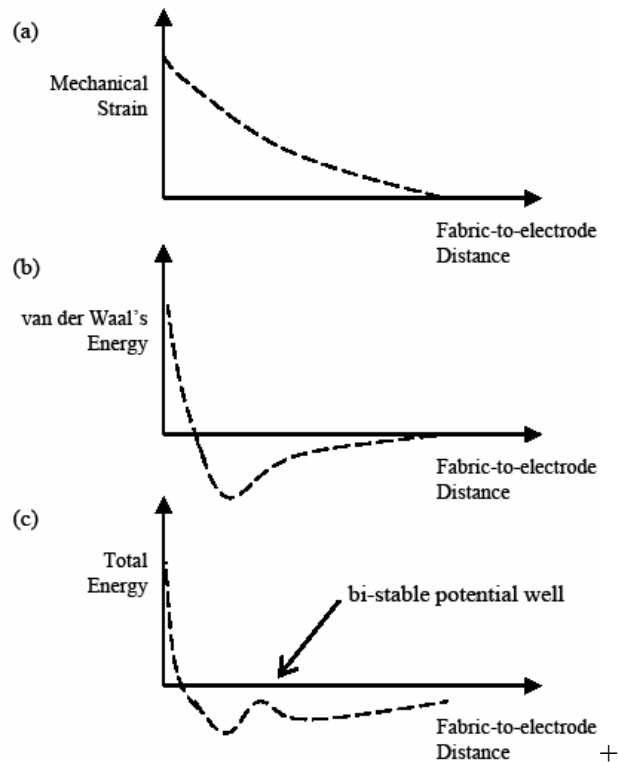


Figure 32: Interaction energies between the SWNT and the underlying metal electrode showing (a) mechanical strain, (b) attractive van der Waal's forces, and (c) resulting bi-stable potential well

These two minima correspond to well-defined “off” and “on” states; that is, the separated upper nanotube to lower electrode junction resistance will be very high, whereas the contact junction resistance will be orders of magnitude lower. A device element could be switched between these well-defined “off” and “on” states by transiently charging the nanotubes to produce attractive or repulsive electrostatic forces [31].

NRAM is constructed as a passive matrix array (Figure 33). In the current approaches the vertical lines are made from a conductive material (Ti/Pd) and horizontal lines are made from SWNTs [30]. Future approaches may use SWNT for the whole structure [31].

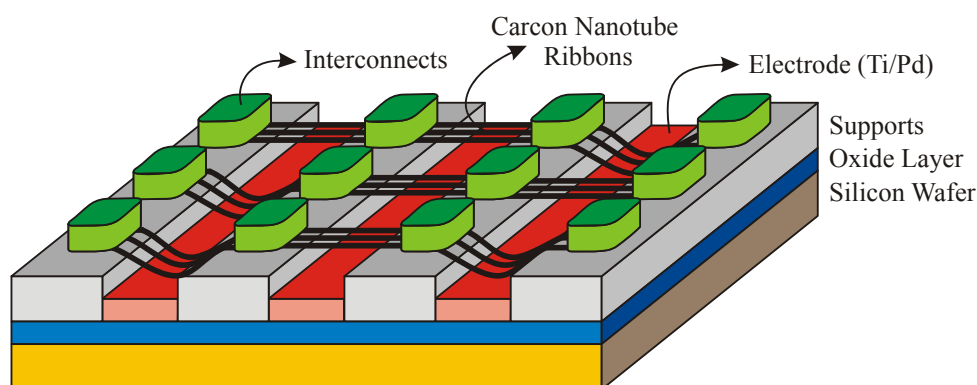


Figure 33: NRAM array

2.2.7 Molecular Memory

In this type of memories, a single device consists of a single layer of molecules or a single molecule that exhibits bi-stable resistance switching. These memory elements make use of physical effects which occur in a single molecule involving quantum mechanical effects. The switching is based on several kinds of mechanisms which can cooperate to achieve switching. Some of these mechanisms are [32]:

- a- Reduction-oxidation (redox) process where a neutral molecule can be changed to an ionized acceptor/donor group.
- b- Configuration change through a reversible rearrangement reaction.
- c- Conformation change where there are two stable conformations at room temperature.

In Rose Bengal for example, redox and conformational change of the molecules cause the conjugation modification, and as a result, the conductance of the molecules is changed (Figure 34) [33, 34].

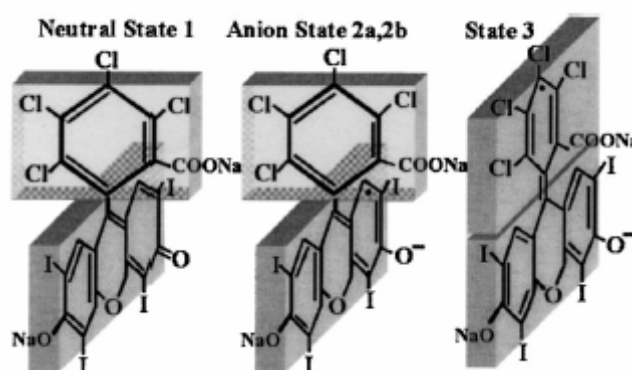


Figure 34: Chemical structure of Rose Bengal in its (a) neutral state, state 1, (b) reduced state without any conformational change, state 2a or state 2b, and (c) reduced state with conformational change, state 3.

Another example is the catenanes, which are molecules consisting of two interlocked rings (Figure 35). The interaction of different redox states makes it possible to rotate one ring within the other. The states of rotation can correspond to binary values [35].

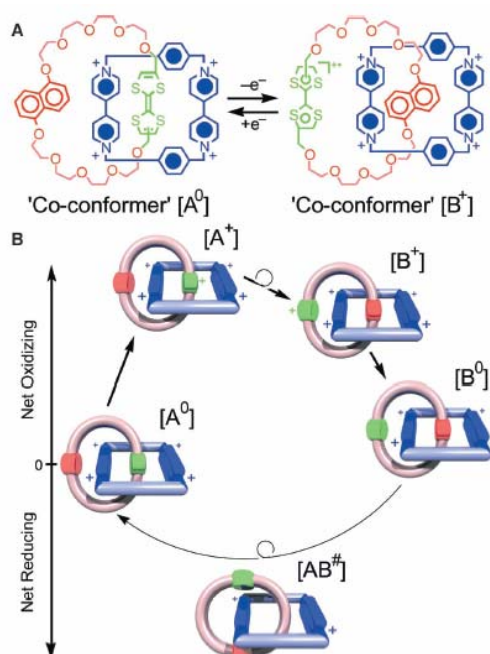


Figure 35: Molecular drawing of the bistable [2]catenane

The preferred architecture for this type of memory is the passive array, where very high densities can be achieved (Figure 36) [36]. Small arrays of these devices were demonstrated using imprint lithography (Figure 37) [37].

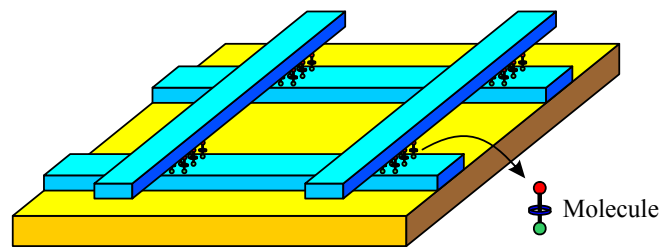


Figure 36: Molecular memory passive array

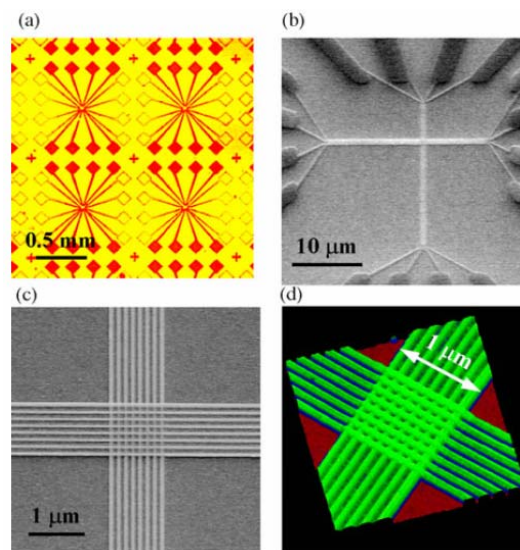


Figure 37: Molecular memory passive array demonstration

2.2.8 Resistive Polymer Memory (Field Driven Ionic Transport)

In this type of memories, which are very similar to the CBRAM, resistance switching takes place by forming/deforming a conductive bridge from ions rather than metal. In the case of a polymer doped with ions, the bridge formation happens due to the inter-phase ionic motion (Figure 38), molecular/ionic dissociation (Figure 39), or change of a valence state of ionic or molecular units [38].

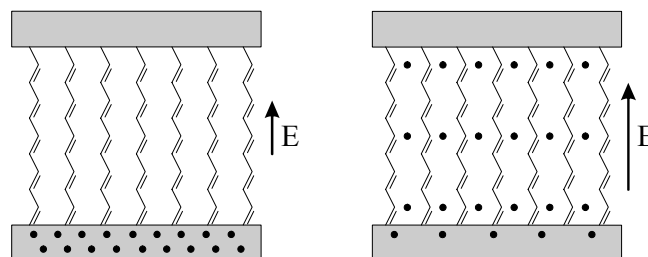


Figure 38: Inter-phase ionic motion and doping in electrical field

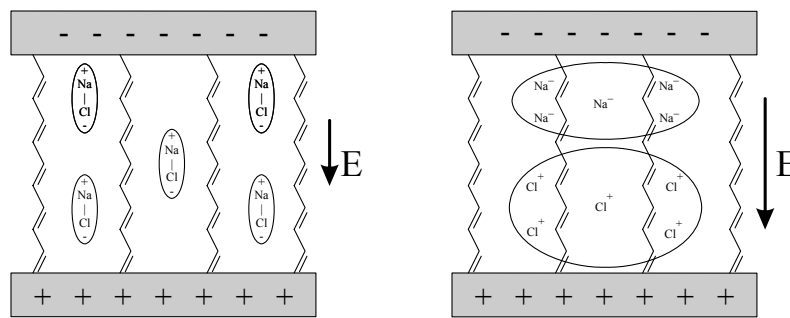


Figure 39: Dissociation of molecules, ions, intraphase ionic motion, and doping in electrical field [39]

In some polymers, where no external atoms or ions exist, a conductive bridge can be formed due to the interaction of strong donor-acceptor molecular units with the conjugated polymer to form a charger transfer complex [40].

An alternative structure of a polymer memory cell is the organic/metal/organic triple-layer structure between two metal electrodes as shown in (Figure 40) [41].

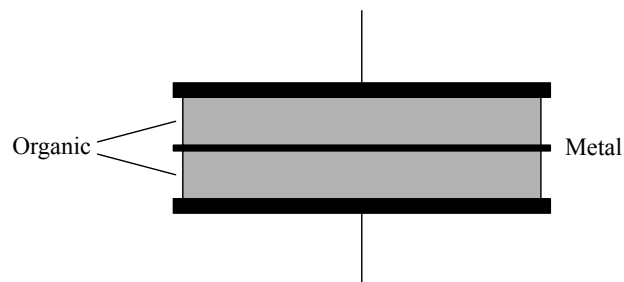


Figure 40: Organic/metal/organic memory cell

2.2.9 Insulator Resistance-Change Memory

This type of memory cells has a capacitor like structure. The insulator material is a perovskite oxide such as Cr-doped $(\text{Ba}, \text{Sr})\text{TiO}_3$ or SrZrO_3 [42-44]. The cell exhibits reproducible reversible resistance switching between two or multilevel resistance states (Figure 41, Figure 42).

The origin of resistance switching is still an open question. One of the possibilities is the bulk effect where a phase transition of perovskite takes place between insulating and conducting states, similar to the breakdown of charge-ordered insulating state in manganites induced by an electric field at a low temperature. The other is the interface effect, where voltage pulses reversibly alter the nature of potential barrier formed in the insulating (or semiconducting) perovskite in contact with metallic electrodes.

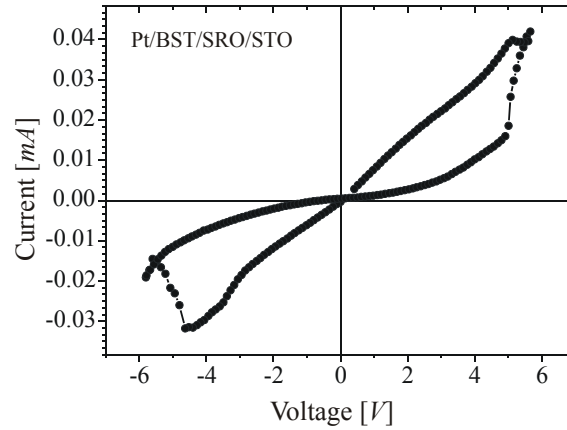


Figure 41: Hysteresis current/voltage behaviors *

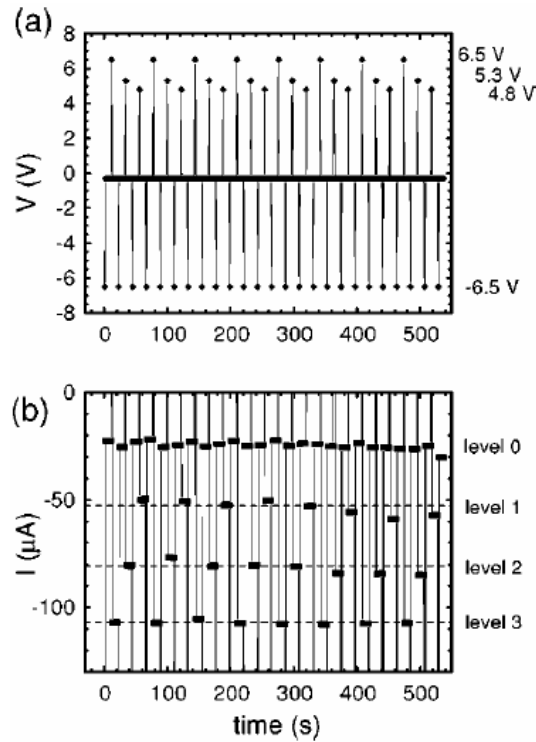


Figure 42: Multilevel switching in a Cr-doped SrZrO₃-based MIM cell operated at 77 K [42]. (a) The applied programming pulses, (b) The generated levels

2.2.10 Nano-Crystal Floating-Gate Flash Memory

A conventional flash memory stores data on a conductive floating gate as shown in Figure 43a. When the oxide gets too thin, it will develop leakage paths causing electrons stored in the floating-gate to leak out and the stored data would be lost [45, 46]. One way to alleviate the scaling limitations of the conventional floating gate device, while still preserving the fundamental operating principle of the memory, is to rely on distributed charge storage instead. Nanocrystal memories are one particular implementation of that concept. In a

nanocrystal nonvolatile memory (NVM) device, charge is not stored on a continuous floating gate, but instead on a layer of discrete, mutually isolated, crystalline nanocrystals or ‘dots’ typically made of semiconductor material [47]. This structure is presented in Figure 43b. Each dot will typically store only a handful of electrons; collectively the charges stored in these dots control the channel-conductivity of the memory transistor.

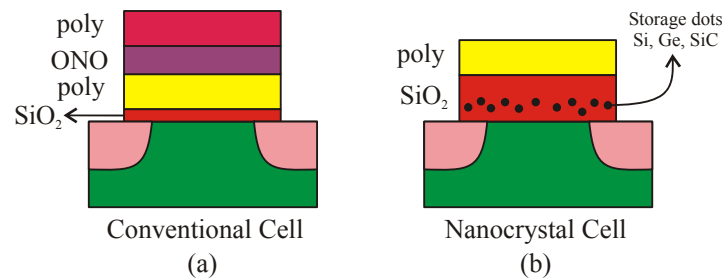


Figure 43: (a) Flash and (b) Nanocrystal cells

As compared to conventional stacked-gate NVM devices, nanocrystal charge-storage offers several advantages, the main one being the potential to use thinner tunnel oxides without sacrificing nonvolatility. Reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds.

There are other important advantages for this memory type over conventional types. First, nanocrystal memories use a more simplified fabrication process compared to conventional stacked-gate/floating gate NVM's by avoiding the fabrication complications and costs of a dual-poly process. Further, due to the absence of drain to floating gate coupling, nanocrystal memories suffer less from drain-induced-barrier-lowering (DIBL) and therefore have intrinsically better punchthrough characteristics. One way to exploit this advantage is to use a higher drain bias during the read operation, thus improving memory access time.

2.2.11 Single/Few Electrons Memories

Single/Few electrons memory is characterized by the confinement of electrons in a quantum dot by the Coulomb blockade. In such quantum dots, electrons are confined electrostatically in all three dimensions, forming a small island of electrons that is bounded on all sides by potential walls. The electron island can accommodate only an integer number of electrons, which occupy only certain discrete energy states. One implementation of a single electron memory device consists of a floating dot, where electrons are stored, and a narrow channel field-effect transistor (FET), which acts as an electrometer [48]. Figure 44 shows the device structure and its operation principle.

An electron is transferred between the floating dot and the channel through a tunneling barrier by applying a proper voltage to the control gate. The current in the channel is modulated by

charging or discharging a single-electron as shown in the figure. The major concern for single electron memories is the ability to operate at room temperature and the management of the impact of background charges [49].

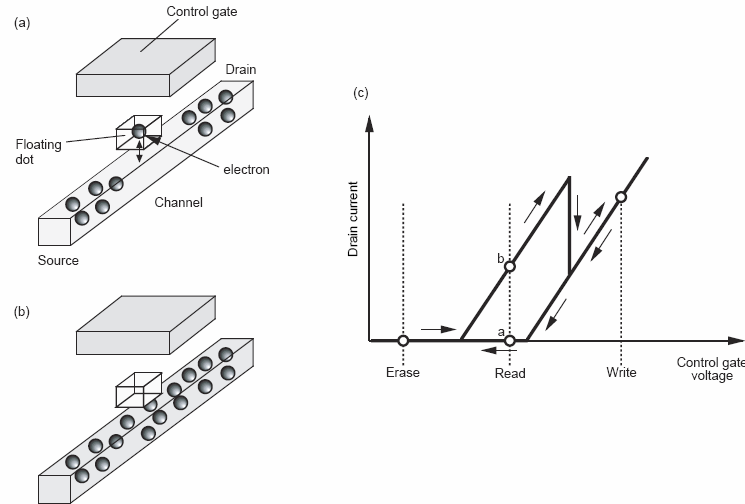


Figure 44: Single/Few electron memory principle [48]

2.2.12 Millipede Memory

Millipede memory is a thermomechanical scanning-probe-based data-storage. Information is stored as sequences of indentations and no indentations written in nanometer-thick polymer films using an array of AFM cantilevers (Figure 45). The presence and absence of indentations will also be referred to as logical marks [50]. Each cantilever performs write/read/erase operations within an individual storage field. Write/read operations depend on a mechanical x/y scanning of either the entire cantilever array chip or the storage medium.

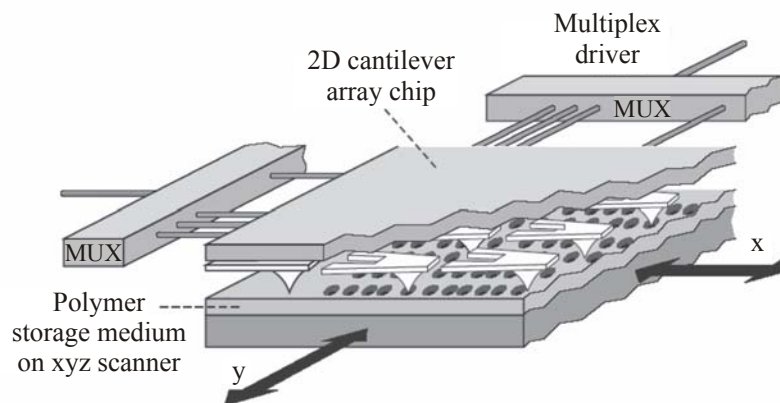


Figure 45: AFM Cantilever Array

Thermomechanical writing is achieved by applying a local force through the cantilever/tip to the polymer layer and simultaneously softening the polymer layer by local heating

(Figure 46). The tip is heated by application of a current pulse to a resistive heater integrated in the cantilever directly above the tip. Initially, the heat transfer from the tip to the polymer through the small contact area is very poor, but it improves as the contact area increases. This means that the tip must be heated to a relatively high temperature of about 400°C to initiate softening. Once softening has been initiated, the tip is pressed into the polymer, and hence the indentation size is increased.

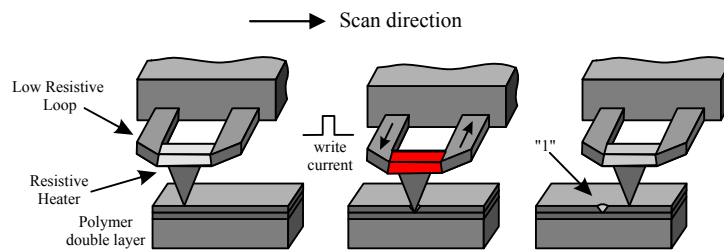


Figure 46: Millipede memory write operation

Imaging and reading are done using a thermomechanical sensing concept. To read the written information, the heater cantilever originally used for writing is given the additional function of a thermal readback sensor by exploiting its temperature-dependent resistance (Figure 47). For readback sensing, the resistor is operated at a temperature in the range of 150° to 300°C, which is not high enough to soften the polymer as in the case of writing. The principle of thermal sensing is based on the fact that the thermal conductance between heater platform and storage substrate changes as a function of the distance between them. The medium between the heater platform and the storage substrate (air) transports heat from the cantilever to the substrate.

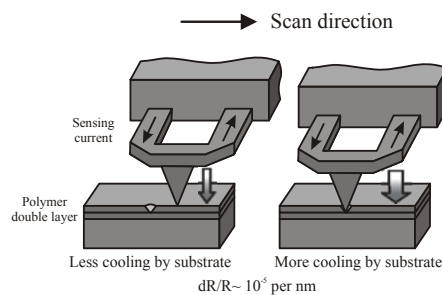


Figure 47: Millipede memory read operation[51]

When the distance between cantilever and substrate decreases as the tip moves into a bit indentation, the heat transport through the air becomes more efficient. As a result, the evolution of the heater temperature differs in response to a pulse being applied to the cantilever. In particular, the maximum value achieved by the temperature is higher in the absence of an indentation. As the value of the variable resistance depends on the temperature of the cantilever, the maximum value achieved by the resistance will be lower as the tip moves into an indentation: During the read process, the cantilever resistance reaches different

values, depending on whether the tip moves into an indentation (logical bit “1”) or over a region without an indentation (logical bit “0”).

Erasing can be selective or non selective, which means that individual bits or the whole storage fields can be erased. Selective erasing is achieved by using the pile-up effect [51]. Non selective erasing is accomplished by the thermal reflow of the storage fields by heating the medium to about 150° C for a few seconds [52]. This erasing process does not allow bit-level erasing; it will erase larger storage areas. However, in most applications single-bit erasing is not required anyway, because files or records are usually erased as a whole.

2.2.13 DNA Memory

So far, the most important emerging technologies have been discussed, but of course not all of them. Research continues and new materials and devices are developed. An exotic type of memories that have been reported recently is the DNA memory where DNA is used to realize the memory function [53].

3. Resistive Memories

3.1 Resistive Device Modeling

Since resistive switching is not fully understood, it is not possible to develop a mathematical model to describe it. Instead; experimental data is considered to approximate the behavior of the real device. Figure 48 shows the I/V curve of a real resistive hysteretic (bistable) element.

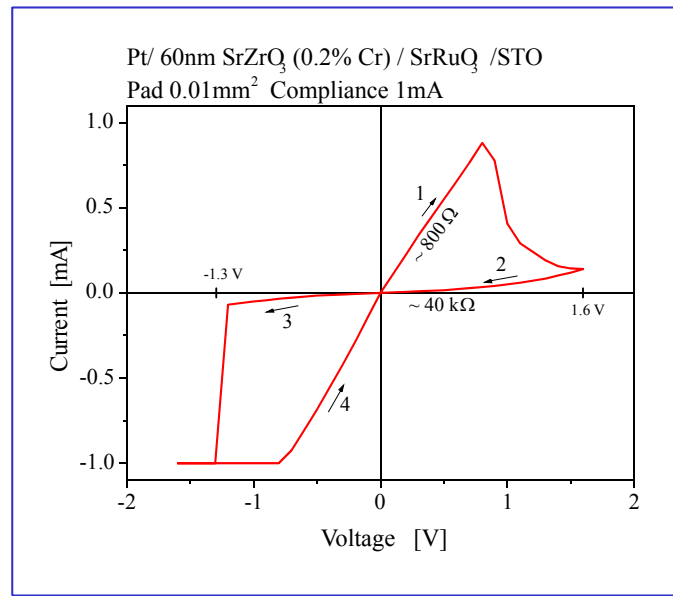


Figure 48: I/V curve of a resistive hysteretic element

From the figure we can extract the following important parameters: the forward and backward switching voltages (V_{sw1} and V_{sw0}) which do not necessarily have the same magnitude and the “on” and “off” resistances (R_{on} and R_{off}). The R_{on} and R_{off} values include the resistance of the resistive material and interfaces. The threshold voltages are mainly essential for the write process. For a successful write operation we have to ensure that the voltage drop across the resistive element exceeds these limits. The read operation on the other hand, depends mainly on R_{off} and R_{on} . A non destructive read operation has to be performed using lowered voltage levels (lower than the threshold voltages). Hence, only the values of R_{on} and R_{off} around the origin are considered. The read voltage is not allowed to exceed a certain experimentally determined value above which the stored state may be disturbed or altered.

Based on the previous discussion, an empirical electric model was developed which includes the parameters R_{on} , R_{off} , V_{th1} and V_{th0} as seen in Listing 1. The model is written using the simulation language SpectreHDL from CADENCE.

The simulation of the model in Figure 49 shows a high similarity between the simulated and the experimental data. More complex models need more understanding of the resistive hysteretic materials. For transient analysis in a first approximation a capacitor can be connected in parallel to the resistive elements. At the current time it is considered that the switching time is zero. This can be accepted if we assumed steady state analyses. Models for transient analyses on the other hand, need more information about the switching time. These switching times are not always given or experimentally extracted because the I/V curves are measured using slow voltage sweeps.

```

module SW_RES (p,n) (Ron, Roff, Vsw1,Vsw0)
node [V,I] p,n;

parameter real Ron = 800 from (0:inf); // [Ohm]
parameter real Roff = 40000 from (0:inf); // [Ohm]
parameter real Vsw1 = 1.0 from (-5:5); // threshold voltage from "off" to "on"
parameter real Vsw0 = 1.0 from (-5:5); // threshold voltage from "on" to "off"

{
real res=Ron;
analog
{
if (V(p,n)>=Vsw1) res = Roff;
if (V(p,n)<=-Vsw0) res = Ron;
I(p,n)<- V(p,n) / res;
}
}

```

Listing 1: Resistive hysteretic model using SpectreHDL

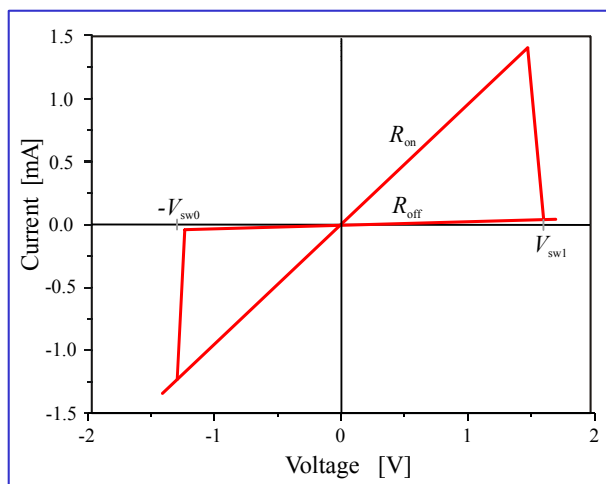


Figure 49: Simulated I/V behavior of the resistive element

3.2 Active Resistive Memories

All active Resistive Memories utilize a transistor to access or isolate each individual memory cell. The specific type of the resistive material used in the memory cell is not important as far as it is compatible with CMOS technology and the material's electrical characteristics fulfill the design constraints. There are a variety of memory architectures where active cells can be implemented.

The loads on the drivers in CMOS technology are usually of a capacitive nature. This capacitance stems from the interconnects' parasitic capacitance and the gate capacitance of the MOS transistors. The interconnects also have parasitic resistance and inductance. The inductance can be neglected in most cases and consequently, the interconnects are considered as distributed RC lines as depicted in Figure 50.

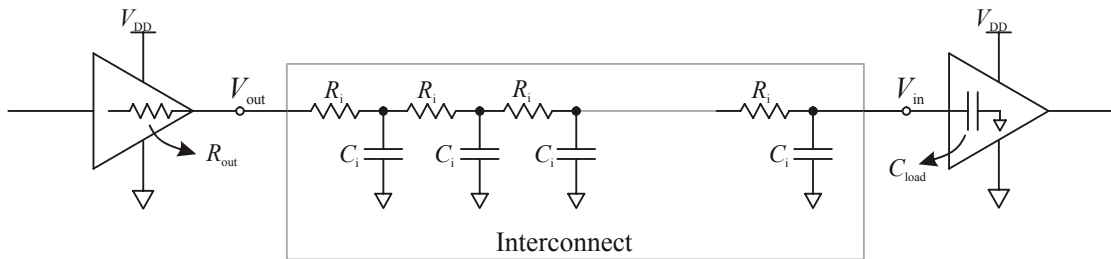


Figure 50: Interconnect representation as distributed RC sections, driver, and input capacitance

The drivers source/sink current to/from the interconnects to charge/discharge them to a certain voltage level. After reaching a steady state, no further current flows and the drivers are not loaded considering no leakage current exists. The main issue for the designer is to decide whether the charging/discharging time is adequate for a certain application and whether the current density does not exceed a certain predefined value to avoid thermal and electromigration damage [54]. Reaching the power supply voltage level or the ground level is always guaranteed ($V_{out}=V_{in}=\{V_{DD}, GND\}$). The time for charging or discharging an interconnect depends on its parasitic resistance and capacitance, the equivalent impedance of the source, and the lumped input capacitance of the subsequent stages connected to the driver [55, 56].

In resistive memories, the parasitic resistance of the interconnects and drivers play a major role in determining the voltage drop at the memory cell. The parasitic resistances of the different elements build a voltage divider with the memory cell which reduces the voltage drop at the resistive element as illustrated in Figure 51. The voltage drop in this case is simply expressed as:

$$V_{in} = \frac{R_{mem}}{R_{mem} + R_{out} + R_w} \cdot V_{DD} \quad (3)$$

where R_{mem} is the resistance of the memory cell, R_{out} is the equivalent resistance of the driver, and $R_W = \sum_i R_i$ is the interconnect lumped resistance.

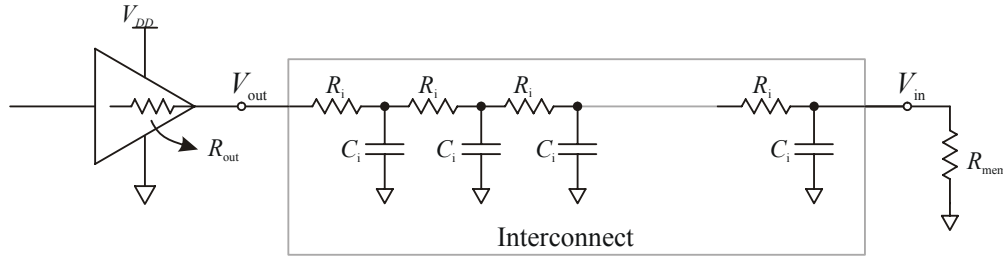


Figure 51: Interconnect representation as distributed RC sections, driver, and memory cell resistance

These considerations hold for all signal lines which are connected to the resistive elements. This fact imposes new restrictions on the CMOS technology, the design of the drivers, the memory architecture, and the type of the resistive material that can be employed in the memory cell.

3.2.1 NOR-Type Memory Architecture

The NOR architecture uses either a common constant voltage level for the platelines of the cells so that only two external contacts have to be made as seen in Figure 52a, or it uses a variable plateline common for the cells in a row (Figure 52b). The plateline is used in this case to reverse the polarity at the memory element. The NOR architecture is used in DRAMs, some types of Flash memories and FeRAMs [9].

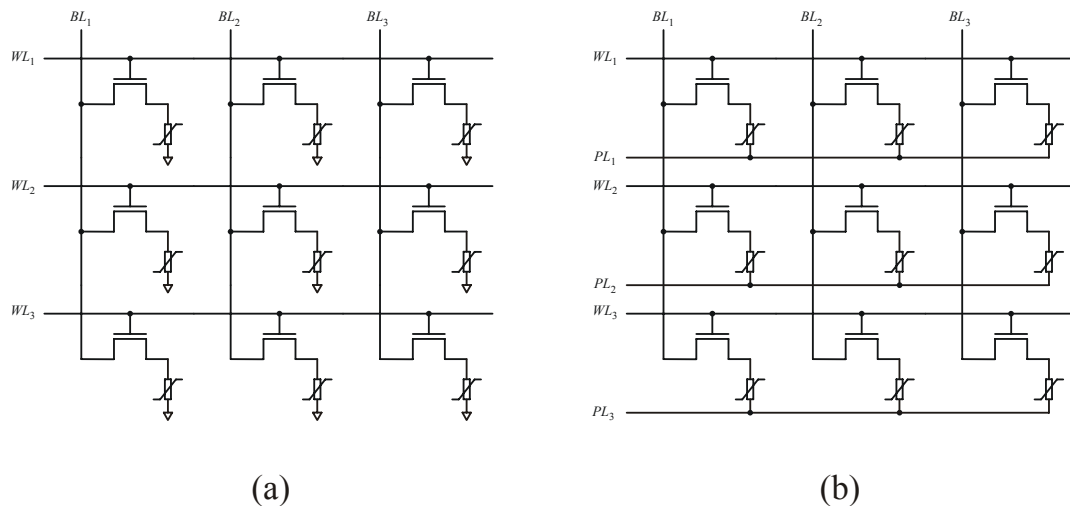


Figure 52: NOR memory array with (a) nondriven plateline and (b) driven plateline

The NOR-type architecture with driven plateline is the one suitable to be used in a resistive memory. To write a “1” into the cell, the bitline (BL) is set to V_{DD} and the plateline (PL) to GND , then a pulse is applied to the wordline to activate the access transistor (Figure 53a). Writing a “0” is accomplished similarly with the exception that the values of BL and PL are exchanged (Figure 53b).

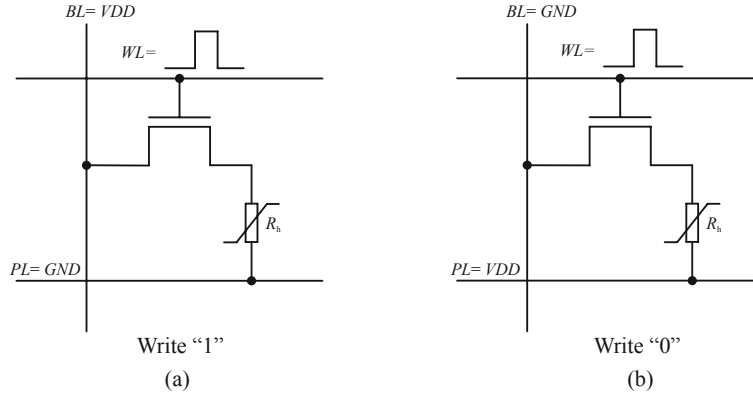


Figure 53: (a) Write a “1”, (b) Write a “0”

The equivalent circuit of the write operation in the steady state is shown in Figure 54. As can be seen, the parasitic resistances of the drivers, interconnects and transistors are considered.

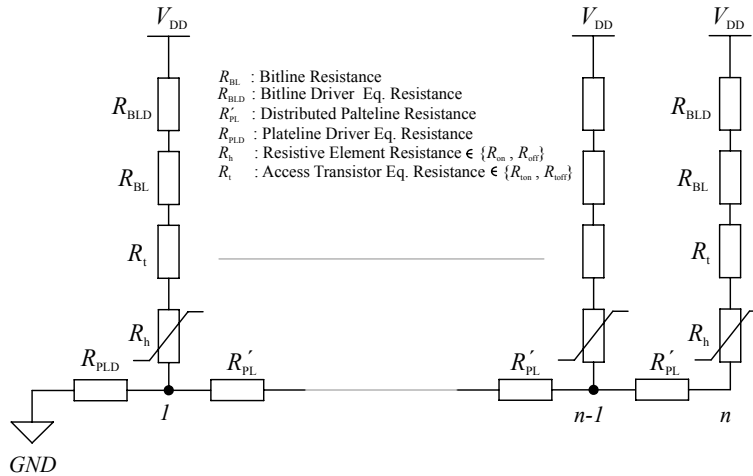


Figure 54: Equivalent circuit for the write operation

Since the plateline is common for all cells in a row, the voltage level is lowest at the furthestmost cell seen from the plateline driver. The voltage level depends on the distributed resistance of the plateline and the resistance of the branches of the memory cells ($R_{col} = R_h + R_{ton} + R_{BL} + R_{BLD}$). Figure 55 illustrates a simulation of the voltage level at the nodes 1 to n , where n is assumed to be 64, by using the values $R'_{pl} = \{0.1 \Omega, 1 \Omega, 2 \Omega, 3 \Omega\}$, $R_{PLD} = 1 \text{ k}\Omega$, $R_{col} = 10 \text{ k}\Omega$, and $V_{DD} = 1 \text{ V}$. It can be clearly seen, how the voltage level degrades the further

we move from the plateline driver. It can also be seen, that higher R'_{pl} values cause more degradation.

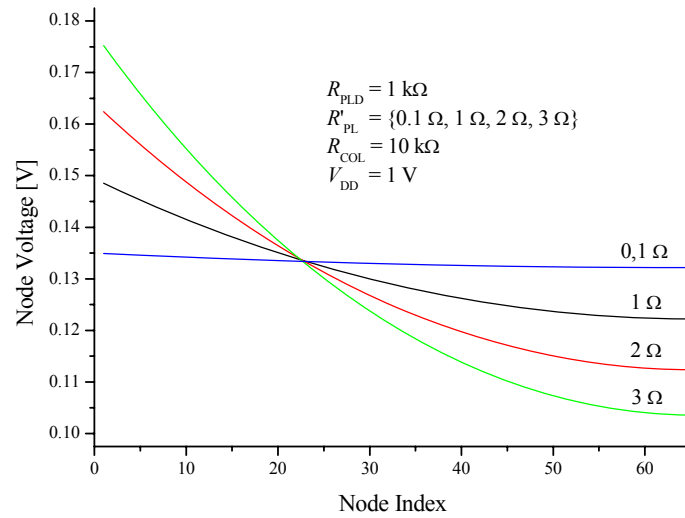


Figure 55: Voltage drop on the nodes 1 to 64 of the plate line for different R'_{pl} values

Figure 56 shows a simulation of the voltage drop at the furthestmost node, where the number of columns is varied from 1 to 64 and R'_{pl} is in the range $[0.1 \Omega, 10 \Omega]$. All other parameters are the same as in the last simulation.

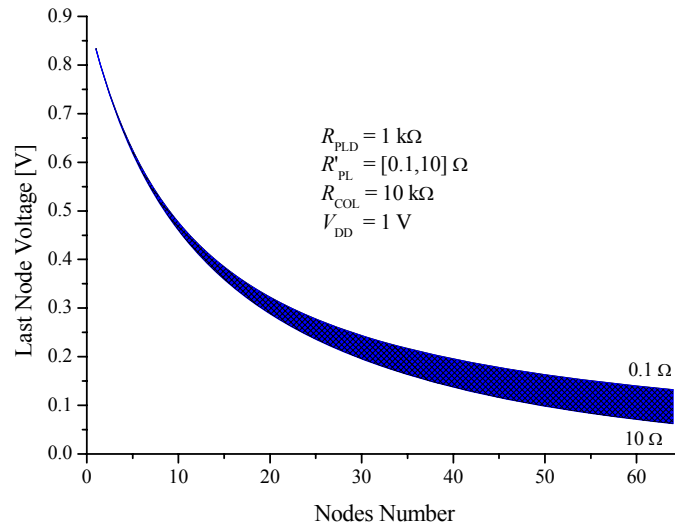


Figure 56: The voltage drop on furthestmost node for different number of nodes and different R'_{pl} values

It can be seen here that the resistance of the plateline does not play the most significant role in reducing the voltage of the nodes, but the number of the nodes (columns) connected to the

plateline and their resistance. This severe reduction of the voltage level with increasing number of columns is the main limiting factor for the NOR-architecture.

To facilitate the analysis, only the lumped resistance of the plateline is considered. This is valid if $(R_h + R_{BL} + R_{BLD} + R_{ton} \gg R_{PL})$, which is always the case. Now, all the branches to the memory cells with the exception of the accessed cell are combined in a resistor called R_{comb} (Figure 57a) which is expressed as:

$$R_{comb} = \frac{R_{BLD} + R_{BL} + R_{ton} + R_{on}}{n-1} \quad (4)$$

All cells are assumed to have the value “1” to produce the worst case. The resistors R_{BL} , R_{BLD} , and R_{ton} are combined to give R_{ser} . R_{PLD} , R_{PL} are summed up to give R_{PLC} . The resultant equivalent circuit is shown in Figure 57b.

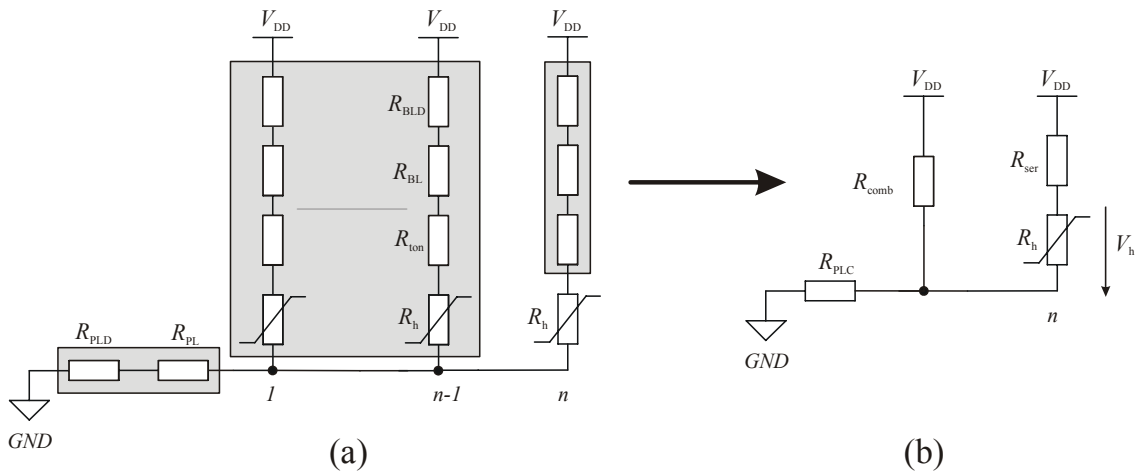


Figure 57: (a) Equivalent circuit of the writing circuitry, (b) Simplified circuit

The voltage drop across the resistive element V_h is expressed as:

$$V_h = \frac{V_{DD} \cdot R_h \cdot R_{comb}}{R_{comb} \cdot (R_{PLC} + R_{ser} + R_{on}) + R_{PLC} \cdot (R_{ser} + R_{on})} \quad (5)$$

The voltage across R_h must satisfy the relation $V_h > \max(V_{th0}, V_{th0})$ to switch from “0” to “1” or back.

In general, the resistances of the bitlines and platelines are much lower than the “on” resistance of the access transistor (R_{ton}) and the memory element (R_h); hence, they can be neglected. The resistance of the cell’s transistor depends mainly on the device geometry. In a memory array, we seek the smallest possible geometry, which leaves a little room for improvement.

There is more flexibility concerning the geometry of the drivers. By increasing the gate width of the driver transistors, the output resistance is decreased. However, there are limits for increasing the gate width of the drivers.

The stored states of the memory cells are read either by using a sense resistor (Figure 58a) or by using a current to voltage converter as seen in Figure 58b. We want to reduce the current as much as possible in the memory cells to reduce the load at the plateline drivers, thus a sense resistor would be preferred over a virtual ground principle. Furthermore, the virtual ground concept will occupy a larger area of the microchip.

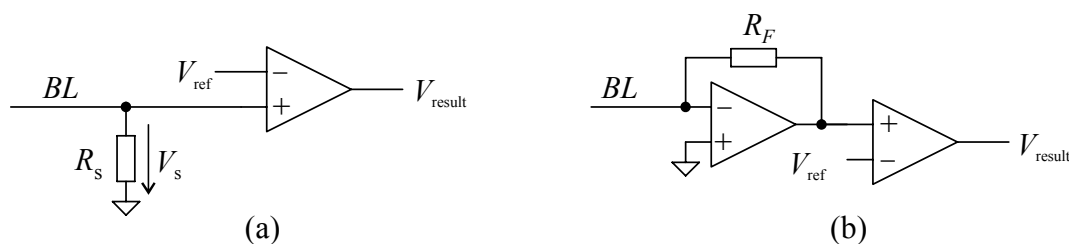
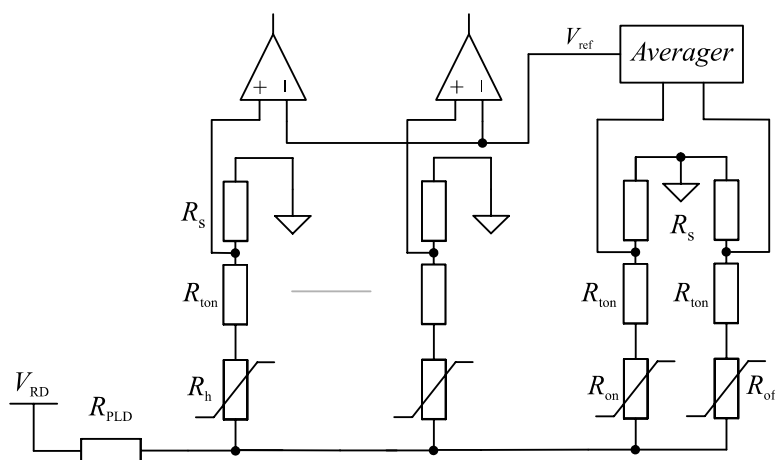


Figure 58: Cell Read by (a) a sense resistor or (b) current to voltage converter

To perform a nondestructive read, attention must be paid to the voltage drop at the memory cells during reading. This voltage is not allowed to exceed the threshold voltage for switching.

The voltage drop at the sense resistor is compared to a reference voltage to determine whether a “1” or a “0” are stored. According to the cells’ states in a row, the voltage of the plateline can change. To trace this change, the reference voltage should be generated from the same row. This can be accomplished by adding two cells to each row (Figure 59), so that one of them stores a “0” and the other stores a “1”. The voltage of the two cells is averaged using an averaging circuit. The average voltage is then used as the reference voltage.



* The resistances of the plateline and bitlines are ignored

Figure 59: Reference generation and read equivalent circuit

Most of the elements of the memory field have fixed parameters and the designer has no influence over them. The exceptions are the drivers, sense resistors, and the number of columns attached to a plateline. We are looking for an optimal value for R_s , by which the difference between the sensed voltages for a “1” and “0” is maximized. We consider all cells in the row contain “1”s with the exception of the cell under test. We assume realistic values for the fixed parameters and have R_s and n as parameters. As the simulation in Figure 60 shows, there is always a maximum that is shifted with the number of columns in the row. The maximum was found to be 0.11 V by $R_s=22.2 \text{ k}\Omega$ and $n=4$ and 0.10 V for $R_s=24.3 \text{ k}\Omega$ and $n=8$.

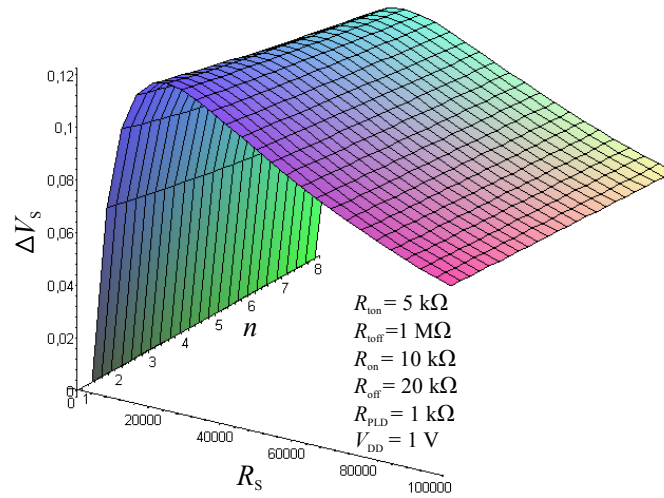


Figure 60: Curve shows the optimal values for ΔV_s depending on R_s and n . The maximum is found to be at $R_s=22,2 \text{ k}\Omega$ for $n=4$ and $R_s=24,3 \text{ k}\Omega$ for $n=8$

3.2.2 NAND-Type Memory Architecture

In the NAND-architecture (or Chain-Architecture) the cells are connected together in series and the resistive elements are connected in parallel with the cell transistors as seen in Figure 61. The NAND-architecture is widely used in high capacity Flash and FeRAM memories (Chain FeRAM) [9].

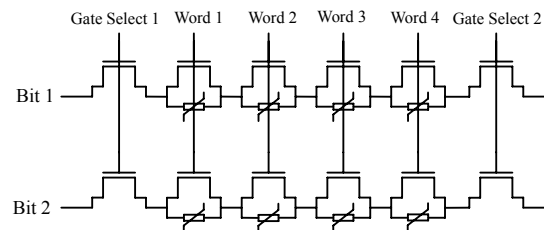


Figure 61: NAND memory array

A cross section of a block from this memory type is shown in Figure 62. The main advantage of this type is its high density because every source of a cell transistor is the drain of the adjacent cell transistor.

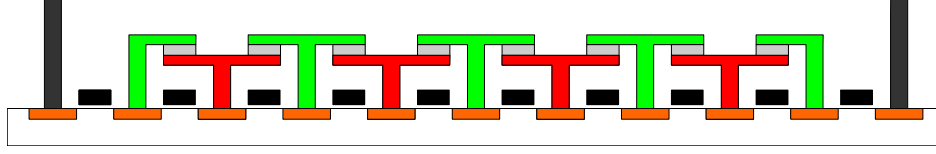


Figure 62: Cross section of a NAND-memory block

The equivalent circuit of a memory block is shown in Figure 63.

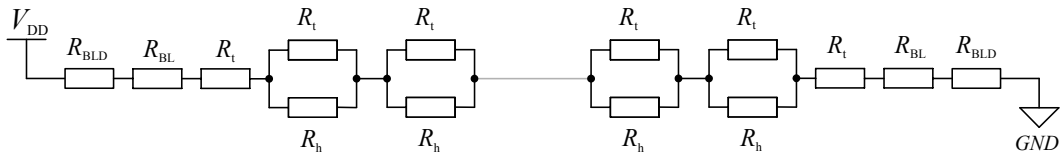


Figure 63: Equivalent circuit for NAND-architecture block

When a cell is accessed, its corresponding transistor is deactivated and all other transistors in the block are activated. This means that all memory elements in the block are overridden with the exception of the accessed cell, where the highest voltage falls. Because the bulk of the transistors is connected to GND and the sources have a voltage higher than GND , the transistors will suffer from the body effect [55] especially the one nearest to V_{DD} . This means that the threshold voltages of the will shift to higher values. This problem is partially avoided if the gate voltages (word signals) are high enough to switch all transistors into the saturation region and if the number of the transistors in a block is reduced which is assumed in this analysis.

The worst case for writing a cell is when it contains a “1” and all other cells contain “0”s which reduces the voltage drop at the accessed cell as illustrated in Figure 64.

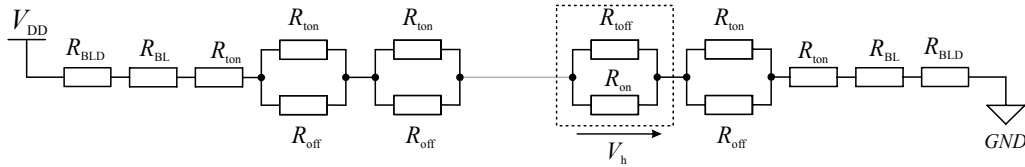


Figure 64: Equivalent circuit of the worst case writing in NAND memory

In this case the voltage drop across the resistive element is given by:

$$V_h = V_{DD} \cdot \frac{R_{toff} \parallel R_{on}}{(R_{ton} \parallel R_{off}) \cdot (n-1) + R_{toff} \parallel R_{on} + 2R_{BLD} + 2R_{ton} + 2R_{BL}} \quad (6)$$

As it was the case with the NOR-architecture, a sense resistor and a reference voltage generator are used to detect the states of the memory cells. The equivalent circuit for reading is shown in Figure 65. The resistance of the bitlines is not taken into account because of their relatively low values in comparison to the other resistances.

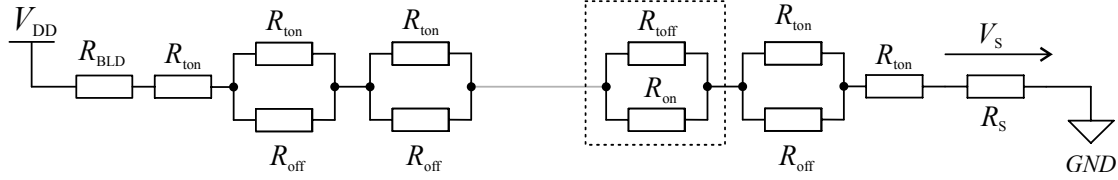


Figure 65: Equivalent circuit for reading

The voltage drop at the sense resistor is given by:

$$V_s = V_{DD} \cdot \frac{R_s}{(R_{ton} \parallel R_{off}) \cdot (n-1) + R_{toff} \parallel R_{on} + R_{BLD} + 2R_{ton} + R_s} \quad (7)$$

The sense voltage difference between a “1” and “0” $\Delta V_s = V_{s1} - V_{s0}$ has a maximum as shown in Figure 66 where ΔV_s is drawn as a function of the number of cells in a block (n) and R_s , which are parameters that the designer can control. The other values were set to realistic values matching the values used in the NOR-architecture simulation. There is always a maximum that is shifted with the number of cells in the block. The maximum was found to be 0.063 V by $R_s=38.7$ k Ω and $n=4$ and 0.044 V for $R_s=54.74$ k Ω and $n=8$.

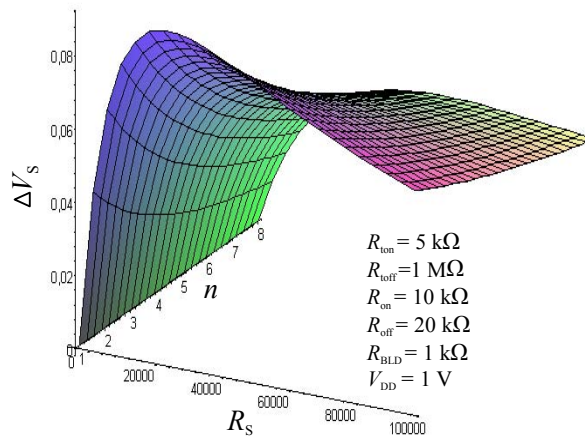


Figure 66: Curve shows the optimal values for ΔV_s depending on R_s and n . The maximum is found to be at $R_s=38,7$ k Ω for $n=4$ and $R_s=54,7$ k Ω for $n=8$

3.2.3 AND-Type Memory Architecture

In the AND architecture each cell is connected externally with two bitlines and one wordline (Figure 67). The AND architecture is rarely used but there are some flash memory types that utilize it [57].

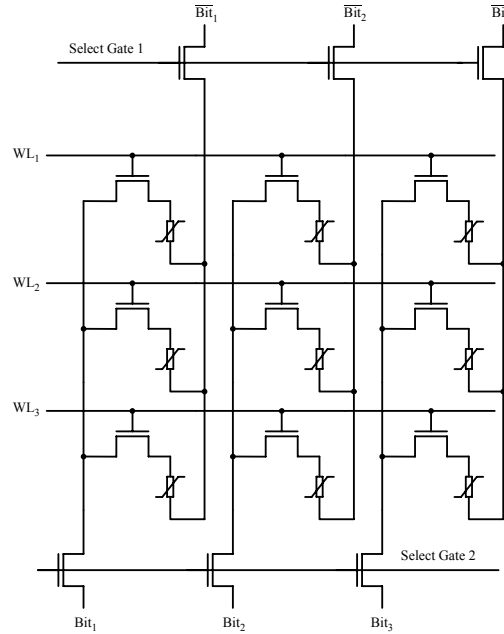


Figure 67: AND memory array

The AND-architecture is very similar to the NOR-architecture with the exception, that the plateline runs parallel to the bitline. In contrast to the NOR-architecture, the plateline driver only operates one memory cell at a time. The equivalent circuit for writing is seen in Figure 68. The lowest possible voltage drop at the resistive element is given by:

$$V_h = \frac{V_{DD} \cdot R_{on}}{R_{on} + R_{BLD} + R_{BL} + R_{ton} + R_{PL} + R_{PLD}} \quad (8)$$

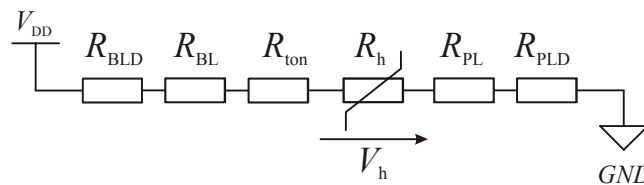


Figure 68: Equivalent circuit of the writing circuitry

The equivalent circuit for reading is shown in Figure 69. The parasitic resistance of the bitline and the plateline are neglected because of their relatively low values.

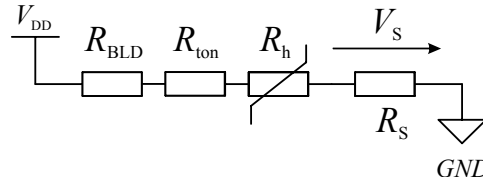


Figure 69: Equivalent circuit of the writing circuitry

As is the case of NOR- and NAND-architectures, $\Delta V_s = V_{s1} - V_{s0}$ can be maximized by choosing an optimal value for R_s which is given by:

$$R_s = \sqrt{(R_{off} + R_{ton} + R_{BLD})(R_{on} + R_{ton} + R_{BLD})} \quad (9)$$

The optimal value of R_s does not depend on the number of the cells in the row or block as it was the case by NOR- and NAND-architectures. By using the same values for the parameters as in the case of NOR and NAND, we find out that, the maximum is at $R_s = 20.4 \text{ k}\Omega$ where ΔV_s is 0.12 V as seen in Figure 70.

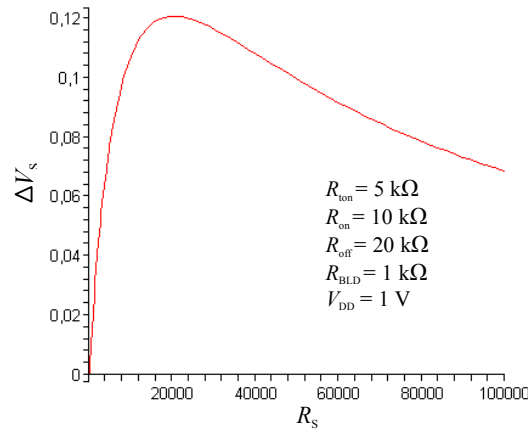


Figure 70: Curve shows the optimal value for ΔV_s depending on R_s .

The maximum is found to be at $R_s = 20.4 \text{ k}\Omega$

3.2.4 Architecture Comparison

By comparing the three memory architectures concerning the write operation, we can see that the AND-architecture is superior regarding the voltage drop at the memory cells (V_h). This voltage stays constant in the AND-architecture because it does not depend on the number of columns in the memory array as can be seen in Figure 71 and 72.

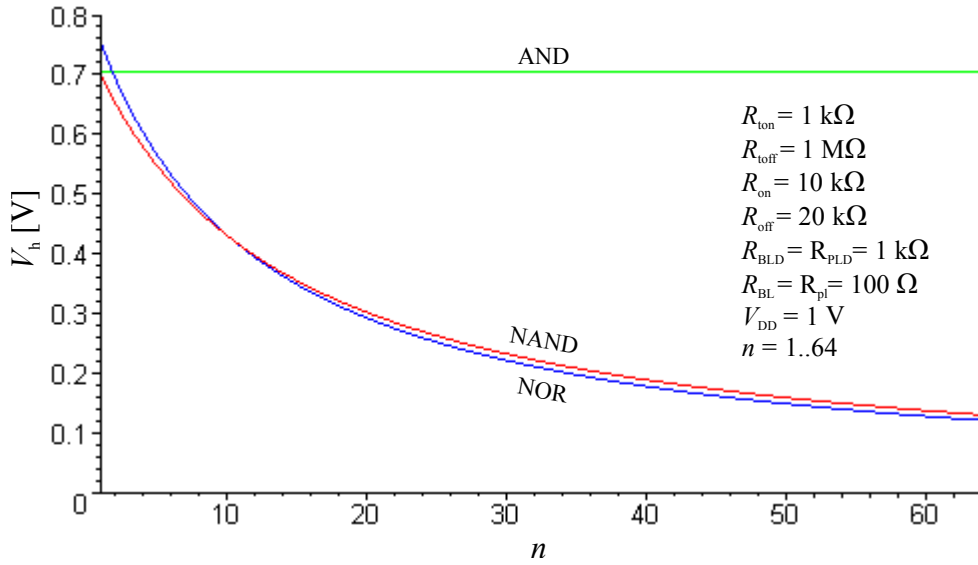


Figure 71: The write voltage drop in NOR-, NAND-, and AND-architecture with $R_{\text{ton}} = 1 \text{ k}\Omega$

It can also be seen that the NAND- and NOR-architectures have very similar voltage drops when the access transistor resistance is low ($R_{\text{ton}} = 1 \text{ k}\Omega$) as can be seen in Figure 71. By making the access transistor resistance higher ($R_{\text{ton}} = 5 \text{ k}\Omega$), the NOR-architecture performs better (Figure 72). For a number of columns under a certain limit, the NOR-architecture performs better than the AND-architecture also.

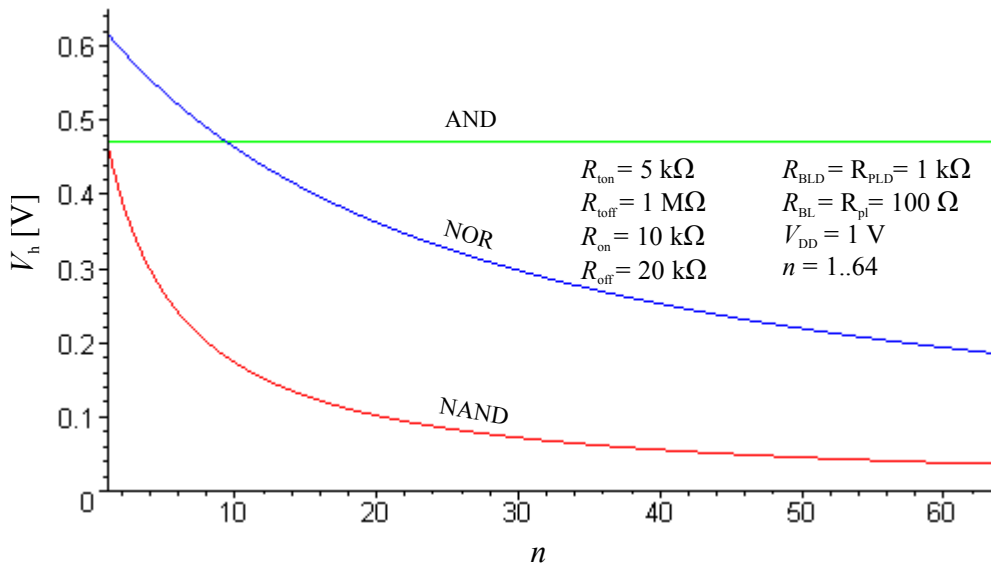


Figure 72: The write voltage drop in NOR-, NAND-, and AND-architecture with $R_{\text{ton}} = 5 \text{ k}\Omega$

Concerning the read operation, we find that in the three architectures, a maximum read voltage is obtained by choosing an optimal value for the sense resistor as was seen in Figures 60, 66, and 70. The voltages obtained in the NAND- and NOR- architectures are reduced with an increasing number of cells (Figure 60, 66), whereas they are constant in the AND-

architecture (Figure 70). Also, the voltages generated in the NAND-architecture are the lowest.

An important aspect that has to be concerned is the cell size. The cell size of the NAND-architecture is the smallest among all architectures even though it seems to be the worst architecture concerning V_h and the sense voltage. Having resistive materials with low threshold voltages makes the NAND-architecture an attractive alternative.

3.3 Novel Active Capacitive-Resistive Memory

Two new memory cells are introduced. The first one uses a capacitor in combination with the resistive element to enable the switching without the usage of a plateline. The second concept uses the plateline to generate a higher voltage than the supply voltage, which can be used if the resistive element has a higher switching threshold than the power supply. The two types are discussed in the following.

3.3.1 Nondriven Plateline Capacitive-Resistive Cell

In this cell type, a capacitor C_c is connected serially to the resistive element of the memory cell as shown in Figure 73. In this configuration the resistive element is accessed via the access transistor T and the capacitor C_c . This method eliminates the usage of a plateline to reverse the polarity at the resistive element.

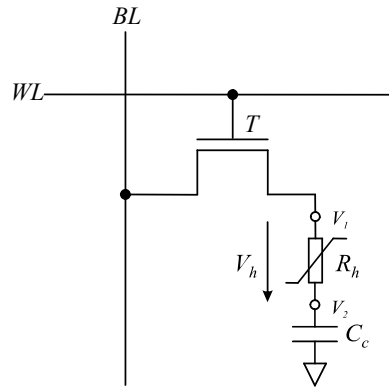


Figure 73: Non driven capacitive resistive memory cell

The equivalent circuit of the memory cell considering parasitic resistance of the transistor in the on state (R_t) and the parasitic capacitance of the resistive element (C_h) is shown in Figure 74.

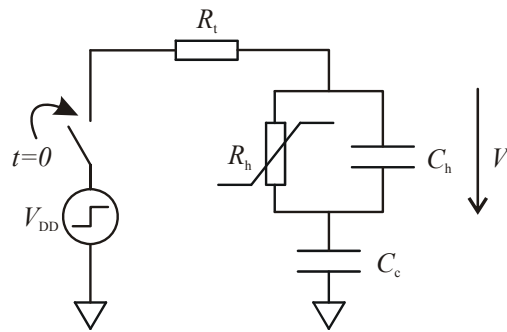


Figure 74: equivalent circuit of the non_driven memory cell

To write a “1” into the cell, the cell capacitor C_c is discharged, the cell is isolated, and the bitline is set to V_{dd} . After that, the cell transistor is activated, which generates a pulse at the resistive element that is given by:

$$V_h = \frac{V_{dd} \cdot R_h}{A} \left(\exp\left(\frac{(A-B) \cdot t}{C}\right) - \exp\left(\frac{-(A+B) \cdot t}{C}\right) \right) \quad (10)$$

where

$$A = \sqrt{(C_h R_h - C_c R_t)^2 + 2C_h R_h^2 C_c + R_h^2 C_c^2 + 2C_c^2 R_t R_h}$$

$$B = C_h R_h + C_c R_h + C_c R_t$$

$$C = 2C_h R_h C_c R_t$$

$$R_h \in \{R_{on}, R_{off}\}$$

The calculated step response of the circuit is shown in Figure 75. The calculation was made considering a constant R_h . As can be seen the parasitic elements have degraded the voltage drop across the bistable resistor.

Assuming R_t is much smaller than R_h , which is valid for many resistive elements and CMOS technologies, and C_h is much smaller than C_c , which can be technologically obtained, the step response can be simply described by:

$$V_h = V_{dd} \cdot \left(1 - \exp\left(\frac{-t}{R_h \cdot C}\right) \right) \quad (11)$$

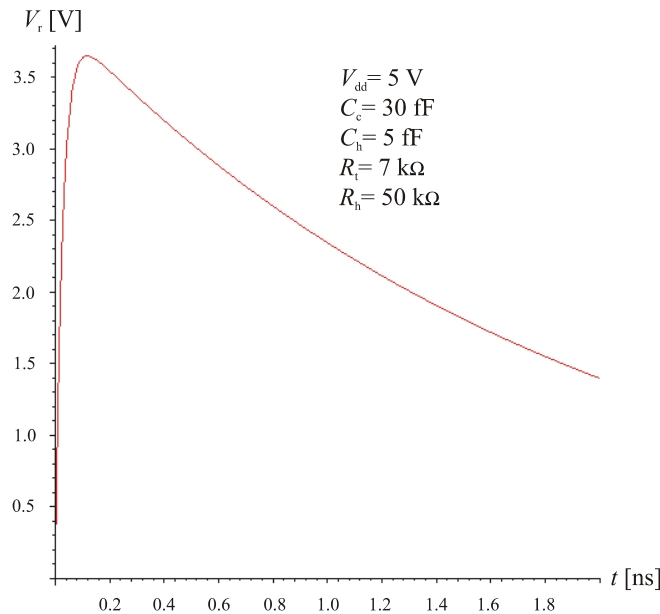


Figure 75: step response of the non driven capacitive resistive cell

It must be guaranteed that the time and voltage required for the switching process are met for the specific resistive material used in the design.

Writing a “0” is very similar but this time the cell capacitor is charged to V_{dd} , the cell is isolated, the bitline is set to GND , and then the access transistor is activated. This will generate a negative pulse across R_h which decays with the time constant $R_h \cdot C_c$. If there was a switching, the time constant changes from $R_{on} \cdot C_c$ to $R_{off} \cdot C_c$. In this analysis, we did not consider how the value of R_h changes during the switching. However, this is not significant as long as the worst case switching time is shorter than the worst-case RC time of the cell. A simulation of the above-mentioned write principle is shown in Figure 76. The signal *state* indicates which value the resistive element has.

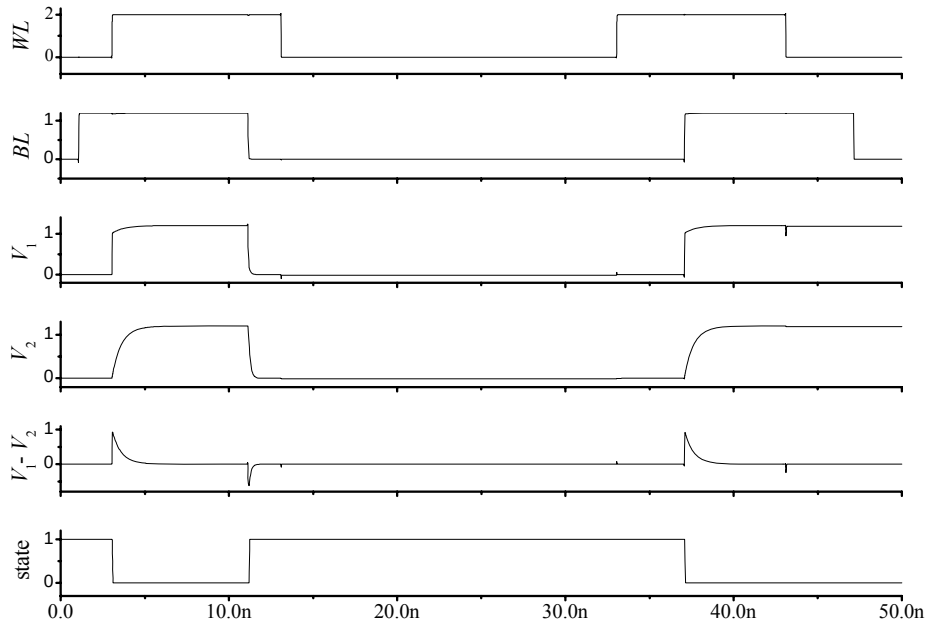


Figure 76: Write Simulation of the non driven capacitive resistive cell

This concept can be used with technologies where the voltage and switching time requirements are met (low voltage and short switching time). The CMOS technology considerations are the maximum usable technology voltage, the on-resistance of the access transistor, and the value of the parasitic capacitance of the bitline.

A new reading scheme is developed to read this cell type based on the RC time constant of the memory cell. The reading operation starts by charging the cell-capacitor to a voltage lower than the magnitudes of the threshold voltages V_{th0} and V_{th1} . This guarantees a non-destructive reading. After that, the bitline is discharged, and then the wordline is activated, which will cause the stored charge in the cell capacitor to flow in the parasitic capacitance of the bitline. The rate of the charge flow, and thus the voltage level on the bitline, depends on the state of the resistive element and has a time constant of $\tau = R_h \cdot (C_c + C_{BL})$. As a result, the capacitance

of a cell with a stored “1” will be discharged faster than that with a stored “0”. To differentiate between a “0” and a “1”, a reference cell is used, which has a fixed resistance with the value $(R_{\text{off}} + R_{\text{on}})/2$ (Figure 77).

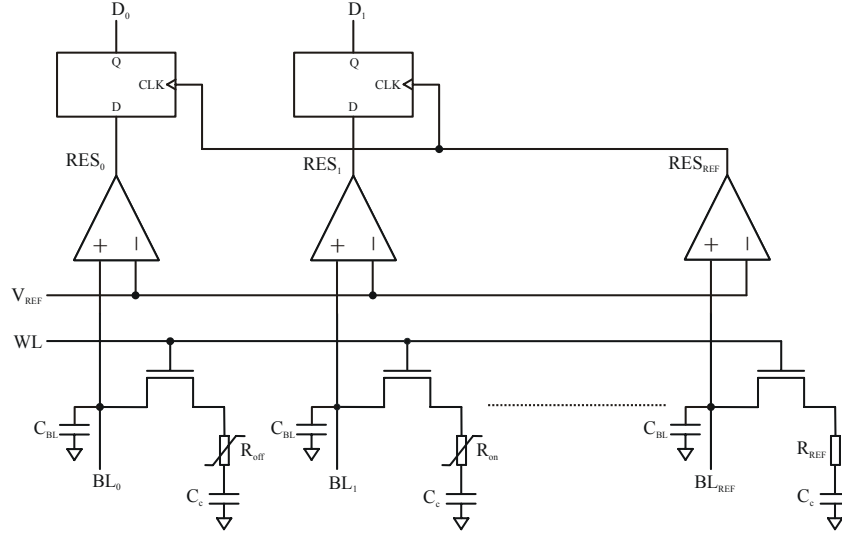


Figure 77: Schematic of the non driven capacitive resistive read operation

This cell will develop a voltage with a time constant, which is between the time constants of a cell with a stored “1” and a cell with a stored “0”. By comparing this voltage with certain predefined constant voltage level it can be seen that the cell with a stored “1” will reach this level first followed by the reference cell and at last the cell with the stored “0” as can be seen in the simulation in Figure 78.

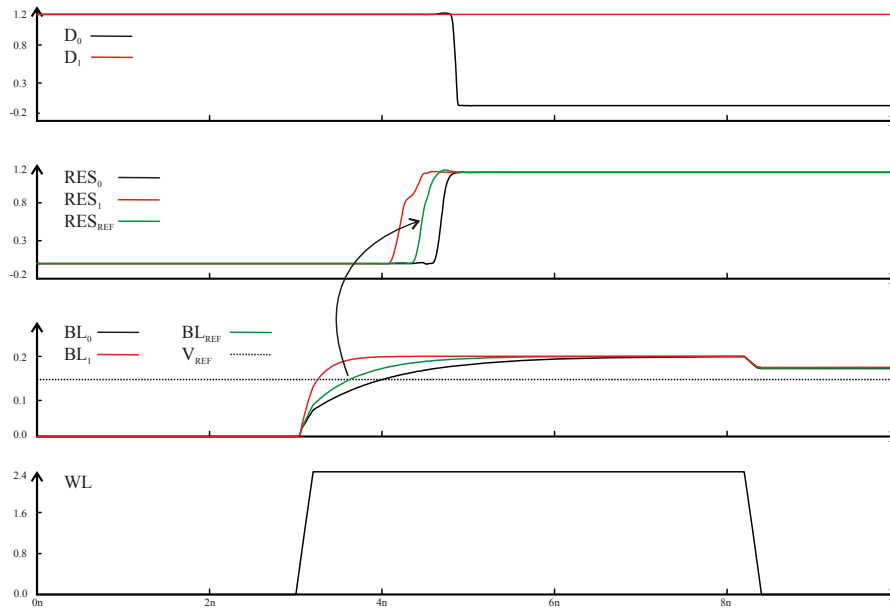


Figure 78: Simulation of the read operation

By letting the comparator of the reference voltage trigger flip-flops to store the current output of the other comparators, the cell information can be retrieved.

3.3.2 Driven Plateline Capacitive-Resistive Cell

This cell is identical to the non-driven cell type with the exception that the plateline is driven as seen in Figure 79, which means that its voltage level can be changed and the switching polarity is reversed.

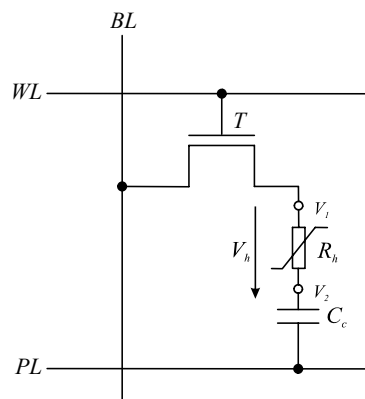


Figure 79: Driven capacitive resistive memory cell

This cell can be used to generate a pulse at the resistive element that is higher than the supply voltage. Figure 80 shows how writing is performed in this cell type.

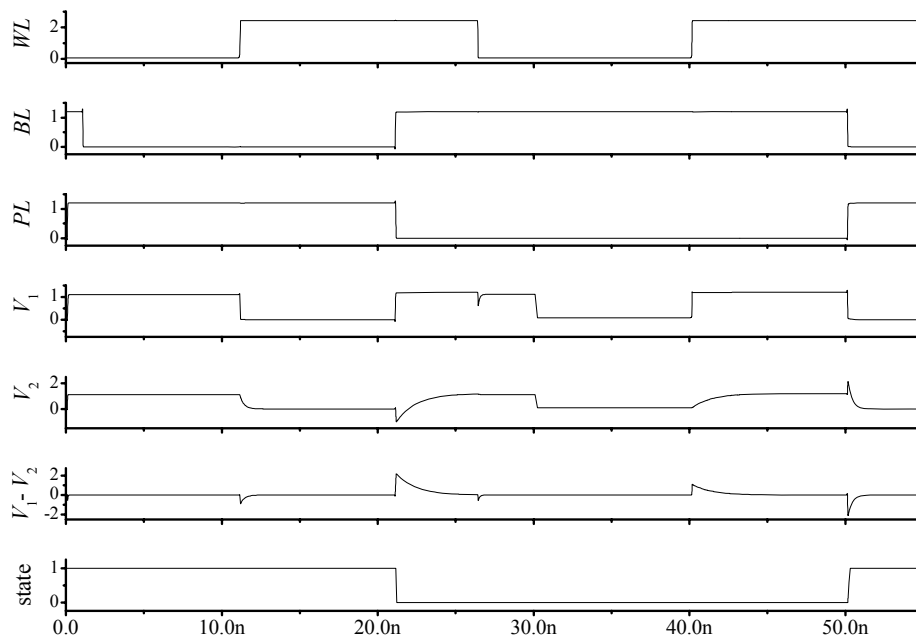


Figure 80: Simulation of driven capacitive resistive memory cell

To write a “1”, PL is set to GND , BL to V_{dd} , then the transistor is activated. This will charge the capacitor to V_{dd} . Now, we set the plateline to V_{dd} and the bitline to GND simultaneously which will cause the voltage V_2 to jump to $2V_{dd}$ resulting in a voltage drop of $-2V_{dd}$ across the resistive element. Writing a “0” is very similar but the signal levels of BL and PL are exchanged. This cell type is read similar to the non-driven type where PL is set to GND during reading.

3.4 Passive Resistive Crossbar Array Memories

Passive crossbar memory arrays are very attractive for future memory technologies because of the simplicity of their manufacturing and therefore, their inexpensive production. They constitute of vertical and horizontal conductive wires (interconnects) that sandwich a resistive bistable element in between at the crossing points as seen in Figure 81. This simple structure can be scaled down to few nanometer wire width, which makes it inevitable for nanotechnology.

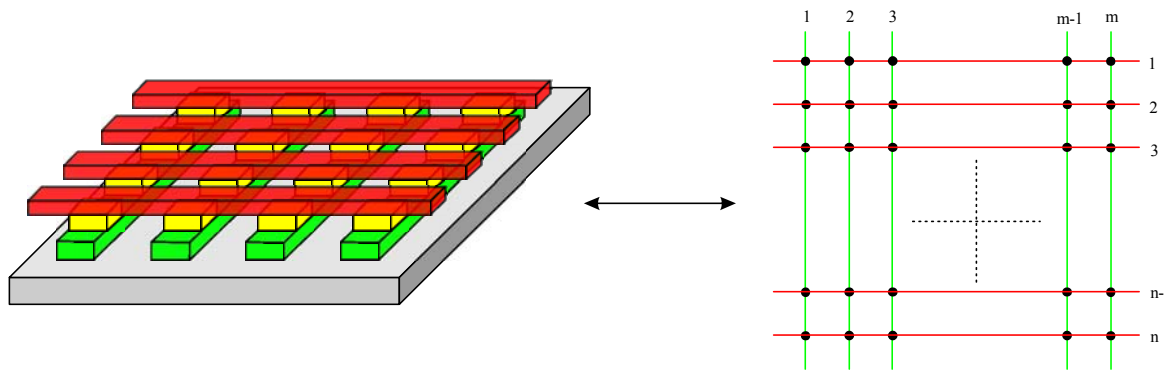


Figure 81: Passive Crossbar memory array

Passive crossbar arrays can not function without the use of active components due to their passive nature. Active components are required to control the read and write operations. The most suitable technology for high integration today is the CMOS technology. This means that for the next years, only a hybrid design that contains the passive matrix and CMOS is realistic [36].

It is important to choose resistive materials that are compatible with CMOS technology if we want to integrate the material into the CMOS processing to avoid damage because of elevated temperature or chemical reactions. This can be made by carrying out the CMOS process until the last metal layer which will be the bottom electrode for the resistive elements. After that, the resistive material is brought on the top of the metal, a last metal layer for the top electrode of the elements and for the connection to the underlying CMOS drivers is made and structured.

3.4.1 Principle Function of Crossbar Arrays

The resistance of interconnects is not considered in this section, which is only valid in cases where the resistance of interconnects is much lower than the resistance of the resistive material used and when the array is relatively small such that, the parasitic resistance can be

neglected. Furthermore, the resistance of the switches in the “on” state (R_{on}) is considered to be much higher than zero ($R_{on} \gg 0$) and $R_{off}/R_{on} \gg 1$.

3.4.1.1 “write” Operation

There are two schemes to write information into the memory cells which are the $V_{DD}/2$ and the $V_{DD}/3$ schemes. The choice of which of them to use depends mainly on the properties of the resistive material. If the threshold voltage for switching is well defined and the material is insensitive for voltages below the threshold then the scheme $V_{DD}/2$ would be preferred since it is easier to implement. Otherwise the $V_{DD}/3$ is used to reduce the distortion voltage on non accessed cells.

A convention is used here, which states that a “1” is written when the voltage difference between the top electrode and the bottom electrode is higher than the “0” to “1” switching threshold (V_{th1}) and the top electrode has a higher voltage than the bottom electrode. Further, a “0” is written when the voltage difference exceeds the “1” to “0” threshold (V_{th0}) and the top electrode has a lower voltage. In the following, the threshold voltage is considered to be the worst case threshold voltage which is $V_{th1} = \max(|V_{th1}|, |V_{th0}|)$ to guarantee that the device always switches to both states.

To write a “1” in a cell by means of the $V_{DD}/2$ scheme, the corresponding row of the cell is connected to V_{DD} and the corresponding column to GND . All other rows and columns are connected to $V_{DD}/2$ (Figure 82a).

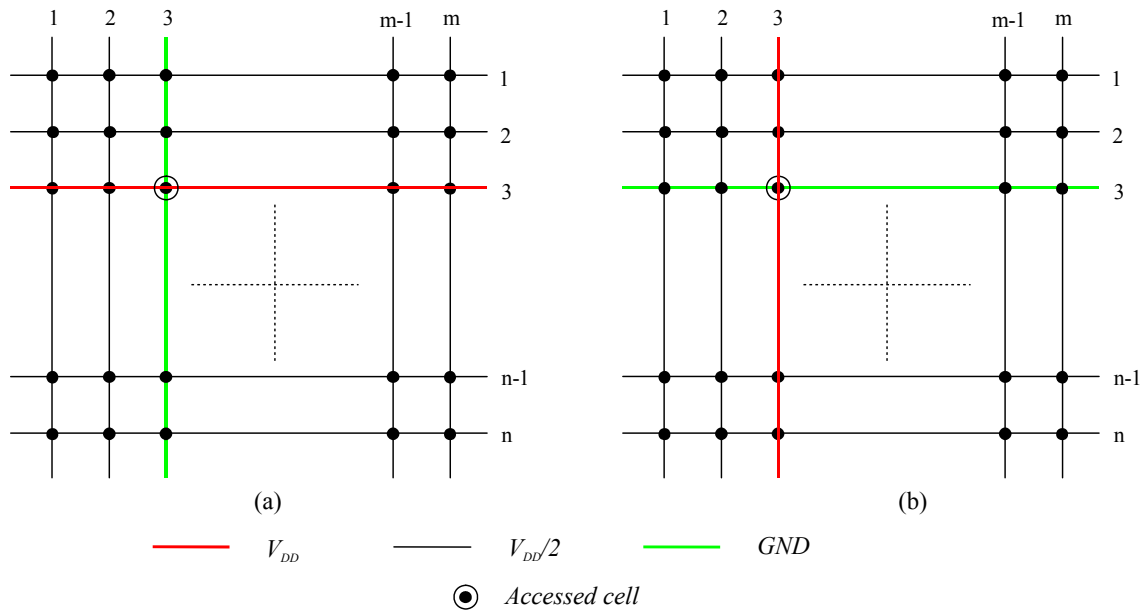


Figure 82: (a) write “1”, (b) write “0”

This means, that all non accessed cells in the row and column of the accessed cell encounter a voltage drop of $V_{DD}/2$ or $-V_{DD}/2$ and all other non accessed cells have a voltage drop of 0 V. Only the accessed cell encounters a voltage drop of V_{DD} . To write a “0”, the same procedure is followed with the exception, that the V_{DD} and GND are exchanged as seen in Figure 82b. The conditions for this scheme to work are that $V_{DD} > V_{sw}$ and $V_{DD}/2 < V_{dist}$, where V_{dist} is the maximum allowed distortion voltage drop across non accessed cells.

To write a “1” by using the $V_{DD}/3$ scheme, the corresponding row of the cell to be written is connected to V_{DD} and the corresponding column to GND as it was the case with the $V_{DD}/2$ scheme. In contrast to the $V_{DD}/2$ scheme, all other rows are connected to $V_{DD}/3$ and all other columns to $2V_{DD}/3$ as can be seen in Figure 83a. The voltage drop on all non accessed cells is $V_{DD}/3$ or $-V_{DD}/3$, which means, that the distortion voltage is reduced in comparison to the $V_{DD}/2$ scheme. Writing a “0” is similar but this time the voltages of the rows and columns are exchanged.

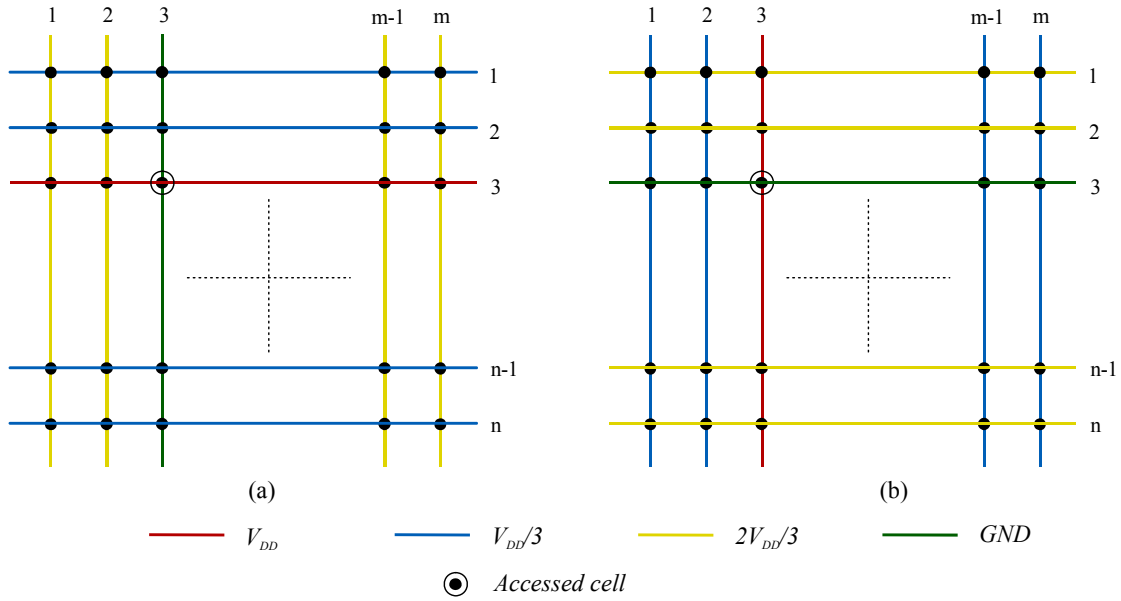


Figure 83: (a) write “1”, (b) write “0”

It is possible to write data to multiple cells in a row in both schemes but this cannot be performed simultaneously for the “1”s and “0”s. Hence, first we write the “1”s followed by the “0”s as can be seen in Figure 84 where an 8x8 array is assumed and the binary value “00110101” is written into the third row. The scheme used is the $V_{DD}/2$ scheme.

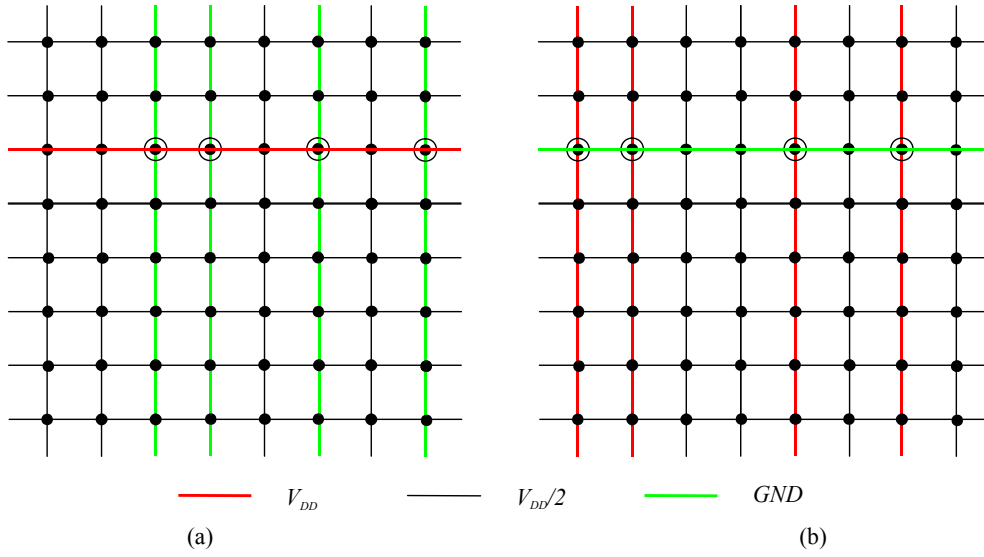


Figure 84: write “00110101” by (a) writing the “1”s then (b) writing the “0”s

3.4.1.2 “read” Operation

The read operation is performed by applying a voltage at the row we want to read (V_{RD}) and connecting all other rows to GND . The columns are connected to a current-to-voltage converter as seen in Figure 85. Ideally, the input of the operational amplifier has a voltage level of GND . Thus, it is called virtual ground.

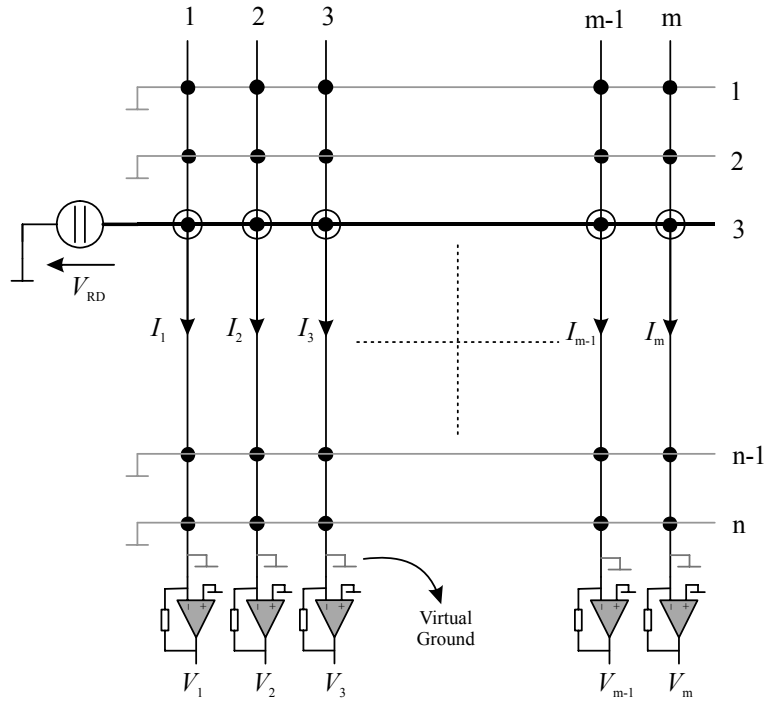


Figure 85: The “read” operation of an ideal passive crossbar

Because there is no voltage drop at the non accessed cells, they don't contribute to the currents $I_1..I_m$ and the output voltages are given by:

$$V_i = \alpha \cdot I_i = k \cdot \frac{V_{RD}}{R_i} \quad ; \quad R_i \in \{R_{on}, R_{off}\} \quad (12)$$

where R_i are the resistance values of the hysteretic resistors in the accessed rows and α is a factor that depends on the feedback resistor of the operational amplifier. The voltages V_i are compared to a reference voltage V_{ref} to determine the stored values in the cells. The reference voltage is ideally the average of the V_{11} and V_{00} voltages $V_{ref} = (V_{11} + V_{00})/2$, where V_{11} and V_{00} are the voltages generated from cells storing a "1" and a "0" respectively. If the positive voltage to the comparator is higher than V_{ref} , then the stored value is "1" and if it is lower, the stored value is a "0". An example for reading a row of the memory array is shown in Figure 86. The stored data in that row are "100000101.....111011001".

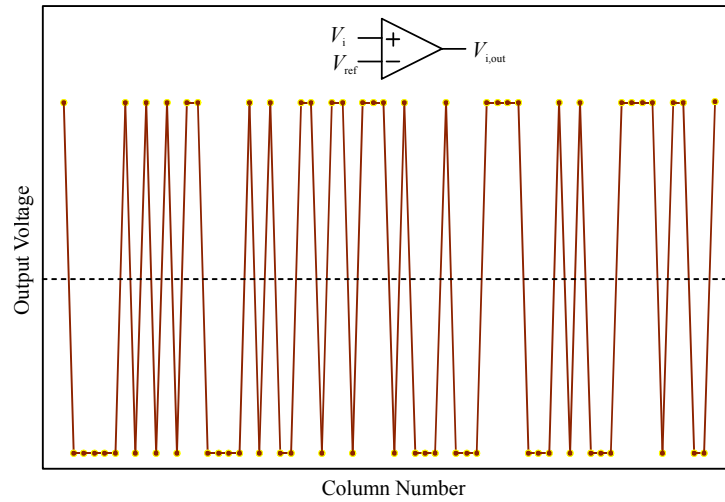


Figure 86: Read operation of an ideal passive crossbar

3.4.2 Storage Capacity of Crossbar Arrays with Ideal Switches

In section 3.4.1, it was assumed that the bistable elements have $R_{on} \gg 0$ and $R_{off}/R_{on} \gg 1$. If ideal or semi-ideal switches were used as bistable elements with no rectifying elements, the crossbar array storage capacity would be reduced. By comparing the two configurations in Figure 87, it can be seen that both of them provide the same result.

This means that the storage capacity is reduced because many configurations of the switches would be equivalent. Instead of the expected N^2 storage capacity of an $N \times N$ crossbar array, the real information capacity would be asymptotically between $N \log N$ and $2N \log N$ [58].

To counteract this situation, the resistive switches should not have a very high $R_{\text{off}}/R_{\text{on}}$ or a rectifying element such as a diode should be used to prohibit the current to flow in non accessed rows.

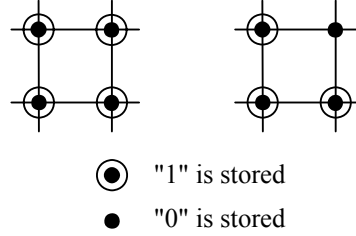


Figure 87: Two equivalent configurations of switches

3.4.3 Parasitic Elements

Real resistive elements and interconnects have parasitic components which are resistive, capacitive and inductive as seen in Figure 88. The parasitic components of interconnects are distributed over their length. Every infinitesimal length is modeled with the inductance L' , the capacitance C' , and the resistors R_s and R_p as shown in Figure 88a. For practical reasons, the interconnect is divided into finite number of sections where lumped elements are used. R_p is neglected when good isolators are used which is almost always the case. L' is also neglected because it is significant only if there are high current transients, which are not expected in a crossbar array.

The resistive element has the parasitic components R_{c1} , R_{c2} , C_p , and L_s as seen in Figure 88b. R_{c1} , R_{c2} are included in R_{on} and R_{off} resistances which are obtained experimentally. C_p is the capacitance between the two electrodes of the resistive element and is considered in the crossover capacitance of the interconnects. L_s is very small and can be neglected.

What is still important for the analyses of the crossbar is the parasitic capacitance and resistance of the interconnects. The parasitic capacitance and inductance are only important if transient analysis is performed.

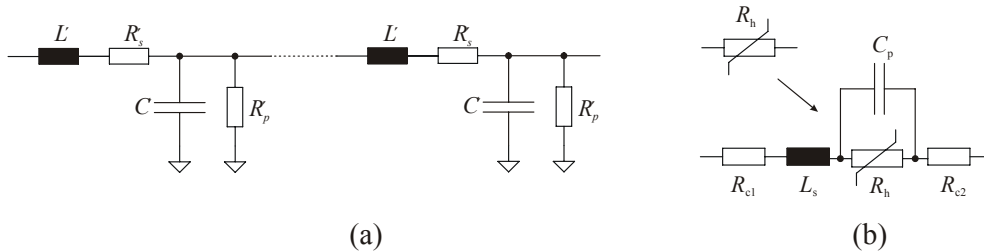


Figure 88: (a) Lumped parasitic components of an interconnect, (b) Parasitic components of a resistive element.

3.4.3.1 Parasitic Resistance

The voltage drop across the parasitic resistor reduces the voltage drop at the resistive elements and disturbs their function as will be seen later. The resistance of a line depends on the type of material used, the dimensions of the line, and the direction in which the current flows.

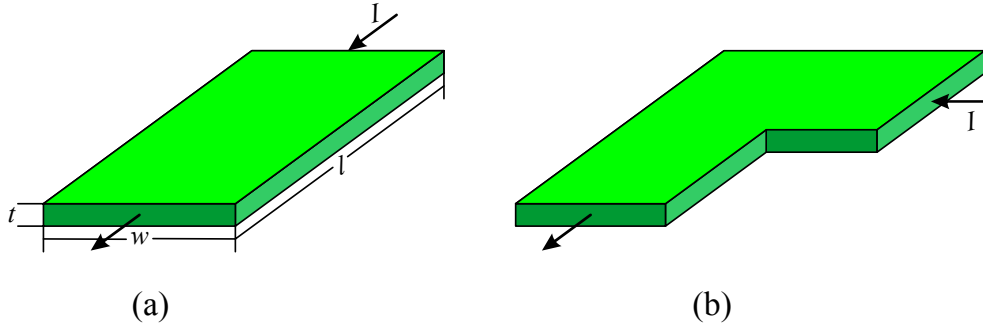


Figure 89: (a) Rectangular conductor, (b) Odd shaped conductor.

If we consider the interconnection line shown in Figure 89a, the total resistance of the line in the indicated current direction is found to be:

$$R = \rho \cdot \frac{l}{w \cdot t} = R_{sheet} \left(\frac{l}{w} \right) \quad (13)$$

where ρ is the characteristic receptivity of the interconnect, R_{sheet} represents the sheet resistivity of the line (Ω/square). For a typical metal layer in CMOS technology, the sheet resistivity is between 0.03-0.1 Ω/square , whereas the sheet resistivity of silicide is about 2- 6 Ω/square , and it is about 15-30 Ω/square for polysilicon [55]. Using the formula given above, we can estimate the total parasitic resistance of a wire segment based on its geometry. Typical metal-poly and metal-diffusion contact resistance values are between 20-30 Ω , while typical via resistance is about 0.3 Ω .

In cases where the interconnects are nonrectangular as in Figure 89b, approximations are used or a field simulation is performed to exactly calculate the resistance. In most short-distance metal interconnects, the amount of parasitic wire resistance is usually negligible. On the other hand, the effects of the parasitic resistance must be taken into account for longer wire segments.

3.4.3.2 Parasitic Capacitance

The parasitic capacitance depends on the geometry of the conductor and the neighboring conductors, and the permittivity of the material filling the space in between them. Figure 90 shows the capacitances of a multi-conductor system.

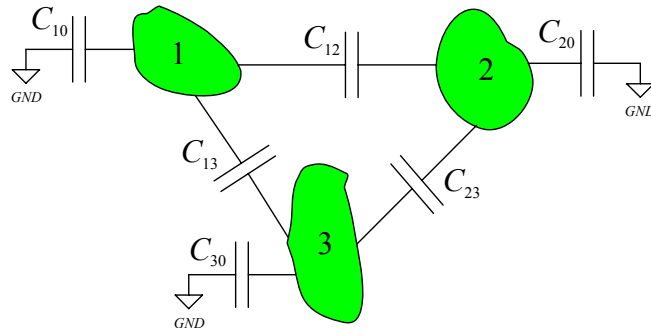


Figure 90: Multi-conductor System

C_{ij} is called mutual capacitance for $i \neq j$ and self capacitance if $j=0$. The total capacitance of a conductor in this system is indicated as:

$$C_{total,j} = \sum_{i=0} C_{ji} \quad (14)$$

In a crossbar we have three contributions to the capacitances as shown in Figure. 91 which are:

- 1- cross over capacitance
- 2- self capacitance (capacitance with ground)
- 3- coupling capacitance

Thus, the total capacitance of interconnect is given by:

$$C_{total} = C_{co} + C_{self} + C_{coup} \quad (15)$$

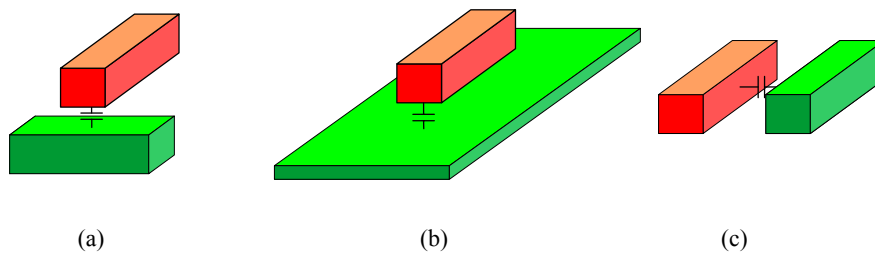


Figure 91: (a) crossover capacitance, (b) self capacitance, and (c) coupling capacitance

The capacitances include the capacitance from the faces opposite to each other and the fringing capacitances of the other faces.

It is not possible in most cases to find a closed and accurate formula to calculate the total capacitance of interconnects. Instead, a field simulation is performed on a small section of a crossbar and because of the regularity of the crossbar, multiplying the result with a factor

representing the area ratio provides the parasitic capacitance. The parasitic capacitance and resistance of an interconnect determine the signal propagation time over that interconnect.

3.4.4 Real Crossbar Arrays

As we have seen in sections 3.4.3, the interconnects are not ideal and contain parasitic elements. These elements have a great influence over the function of the passive array. By considering the interconnect resistances, the passive array would look as seen in Figure 92.

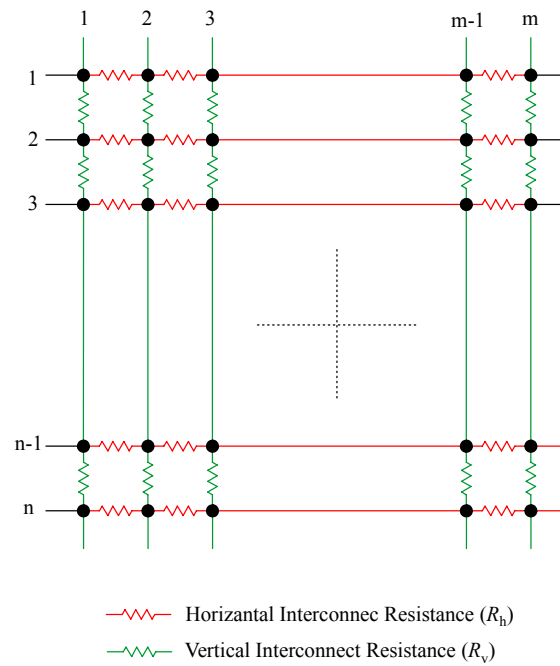


Figure 92: Passive array with parasitic elements

The transistors used to connect the different voltage sources and GND to the columns and rows in the array represent a voltage divider between the equivalent resistance of the transistors (R_t) and the equivalent resistances of the rows (Figure 93a) and columns (Figure 93b) which are R_{AR} , and R_{AC} respectively. This means that the voltages at the connection points to the array are degraded and does not match the voltages of the sources or GND . The amount of degradation is not constant since the equivalent resistances of the columns and rows change according to the stored information in the array.

The current to voltage converters have switches to connect/disconnect them during reading/writing (Figure 93c). The voltage drop at these switches would cause the voltage of the columns to be nonzero during reading. This causes a voltage drop at the non accessed cells and parasitic currents will flow in them and the generated output voltages would be distorted. Adding to this, the concept of current to voltage conversion (virtual ground) is not

practical due to the high currents that flow in the sources and interconnects (particularly the rows) and the size of the amplifiers.

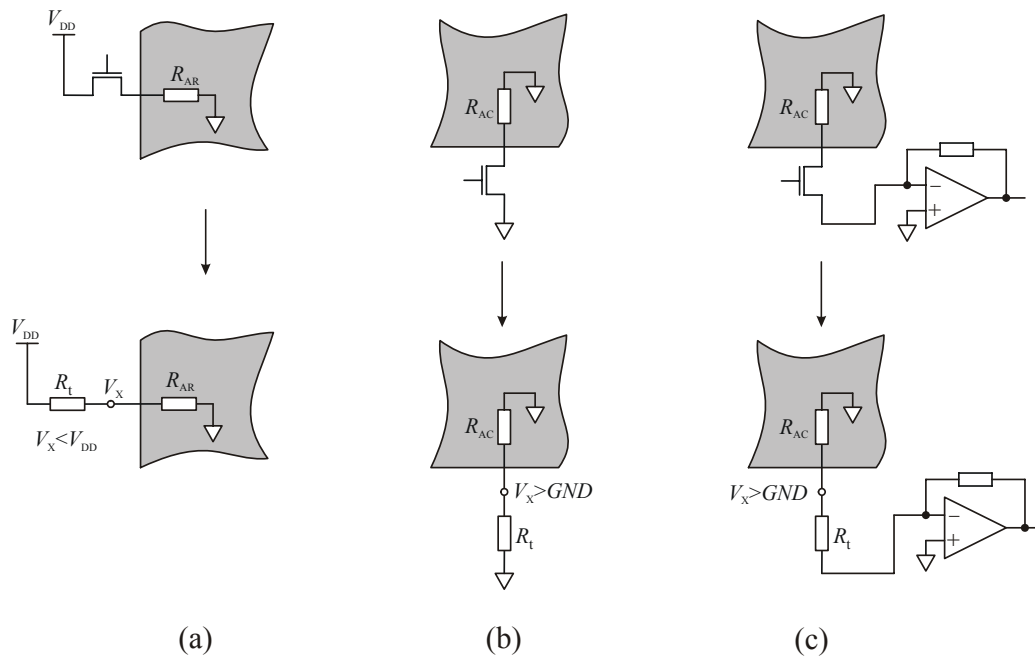


Figure 93: (a) Voltage degradation of V_{dd} and (b) GND
(c) Voltage degradation during reading

Since the resistance of the switches cannot be avoided, they can be utilized as a part of the sensing process in conjunction with a sense resistor that replaces the current to voltage converters as seen in Figure 94a. The voltage drop at both the sense resistor and transistor is taken to be the sense voltage (Figure 94b). This means at the same time that the voltage of the columns is nonzero during reading and we still have the problem of parasitic currents in the non accessed cells. However, these problems are eliminated or reduced by using a number of techniques as will be seen later.

For simplicity the parasitic elements are going to be considered implicitly and a new representation form is going to be used for the description of the resistive array as can be seen in Figure 95. Every rectangle represents a memory cell and its color or shading depends on the context. It may represent the data stored or the voltage drop at the cell or the generated voltage upon reading the cell...etc. Another point to consider is the amount of current allowed to flow in the columns and rows. If this current exceeds a certain value the interconnects would be thermally damaged or would be damaged due to electromigration. Table 2 lists the parasitic elements that are considered in the simulations of the resistive arrays.

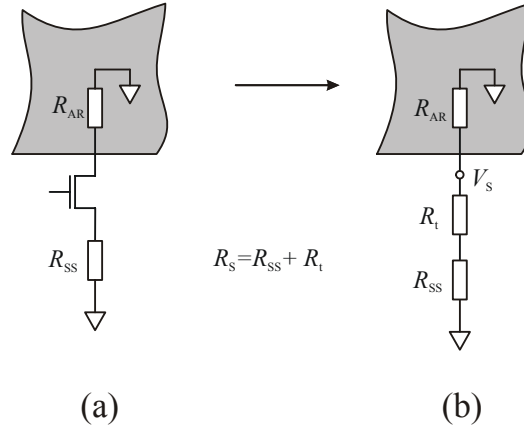


Figure 94: (a) Access transistor connected to a sense resistor, (b) The sense resistor and sense voltage

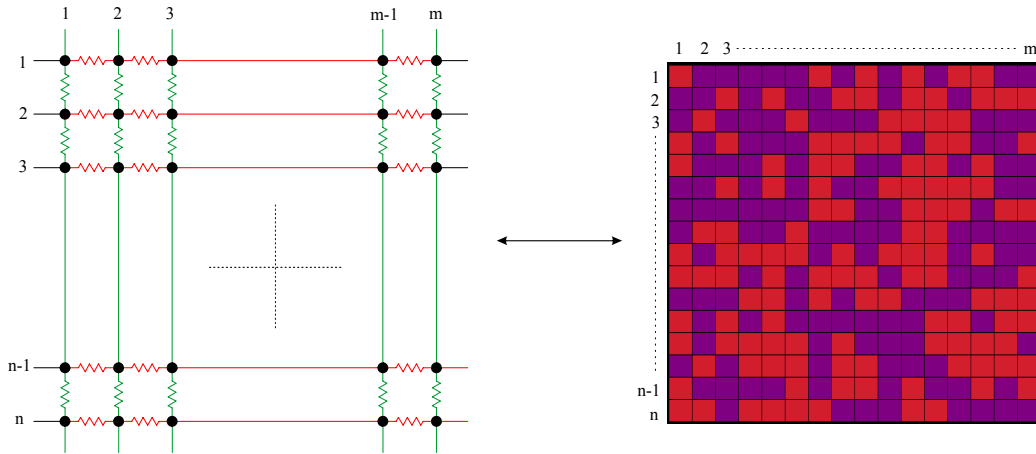


Figure 95: Equivalent representations of the crossbar array

Element	Meaning
R_h	Horizontal interconnect between two adjacent cells
R_v	Horizontal interconnect between two adjacent cells
R_s	Sense resistance
$R_{src} = R_t$	Resistance of the voltage source which are CMOS transistors
R_{AR}	Equivalent resistance of the rows
R_{AC}	Equivalent resistance of the columns

Table 2: The parasitic elements considered for the DC simulation

3.4.5 Simulation Basics

All electronic simulations tools today are based on SPICE (Simulation Program with Integrated Circuit Emphasis) [59]. SPICE was originally developed at the Electronics Research Laboratory of the University of California, Berkeley in 1975. The SPICE simulator uses modified nodal analyses (MNA) to describe and solve the electrical equations. MNA is an extension to the conventional nodal analyses, so that ideal voltage sources and inductors can be included in the circuit.

Different algorithms are used to translate all circuit analysis problems into a single or multiple simpler problems of calculating an operating point of a linear circuit. Such problems can then be solved efficiently by solving a linear simultaneous equation. For example non-linear circuits are solved using a Newton-Raphson algorithm, which linearizes non-linear elements in a circuit. Transient analysis is performed using different integration algorithms like trapezoid or Gear algorithms.

The Newton-Raphson algorithm is an efficient iterative root-finding algorithm. The idea of the method is as follows: one starts with a value which is reasonably close to the true zero or a guess of the zero which is denoted x_1 , then replaces the function by its tangent and computes the zero of this tangent. The zero of the tangent will typically be a better approximation to the function's zero, and the method can be iterated using [60]:

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)} \quad (16)$$

If the circuit we want to simulate contains resistors, voltage sources, and current sources only, it is not efficient to use the Newton-Raphson algorithm to iteratively solve the problem. A better and faster method would be to solve the problem using direct solving algorithms. Before solving the problem, it must be defined using MNA. When MNA is applied to a circuit, the result is a matrix equation of the form:

$$\mathbf{A} \cdot \vec{x} = \vec{z} \quad (17)$$

which is solved by separating $\vec{x}$ in the form:

$$\vec{x} = \mathbf{A}^{-1} \cdot \vec{z} \quad (18)$$

The $\mathbf{A}$ matrix has the dimensions $(n+m) \times (n+m)$ and has only known quantities. n and m are the number of nodes and the number of independent voltage sources respectively. $\vec{x}$ is a vector holding $(n+m)$ unknowns which are the voltages of the nodes and the current of the voltage sources. $\vec{z}$ is a vector holding $(n+m)$ knowns.

$\mathbf{A}$ is composed of 4 smaller matrices in the form:

$$\mathbf{A} = \begin{pmatrix} \mathbf{G} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{pmatrix} \quad (19)$$

The $\mathbf{G}$ matrix is $n \times n$ and is determined by the interconnections between the passive circuit elements (resistors). The $\mathbf{B}$ matrix is $n \times m$ and is determined by the connection of the voltage sources. The $\mathbf{C}$ matrix is $m \times n$ and is determined by the connection of the voltage sources. The $\mathbf{D}$ matrix is $m \times m$ and is zero if only independent sources are considered. Before starting with building the matrices, a reference node is selected which is usually ground, and indices are given to the remaining $n-1$ nodes.

In the $\mathbf{G}$ matrix, each element in the diagonal is equal to the sum of the conductance of each resistor connected to the corresponding node. The off-diagonal elements are the negative conductance of the resistors connected to the pair of corresponding nodes. Therefore a resistor between nodes 1 and 2 goes into the $\mathbf{G}$ matrix at location (1,2) and locations (2,1). This procedure is equivalent to the conventional nodal analyses.

The $\mathbf{B}$ matrix contains elements with the values 0, 1, or -1. Each location in the matrix corresponds to a particular voltage source (first dimension) or a node (second dimension). If the positive terminal of the i -th voltage source is connected to node k , then the element (i,k) in the $\mathbf{B}$ matrix is a 1. If the negative terminal of the i -th voltage source is connected to node k , then the element (i,k) in the $\mathbf{B}$ matrix is a -1. Otherwise, elements of the $\mathbf{B}$ matrix are zero. If a voltage source is ungrounded, it will have two elements in the $\mathbf{B}$ matrix (a 1 and a -1 in the same column). If it is grounded it will only have one element in the matrix.

As in the $\mathbf{B}$ matrix, the $\mathbf{C}$ matrix contains 0, 1, or -1 elements. If only independent sources are used in the circuit, the $\mathbf{C}$ matrix would be the transpose of the $\mathbf{B}$ matrix. The $\mathbf{D}$ matrix would be composed entirely of zeros if independent sources are used which is always the case used in the simulation of the resistive arrays.

What we still need to solve the system, is the $\vec{Z}$ vector which holds the independent voltage and current sources. $\vec{Z}$ is a combination of two smaller vectors $\vec{i}$ and $\vec{e}$ such that:

$$\vec{Z} = \begin{pmatrix} \vec{i} \\ \vec{e} \end{pmatrix} \quad (20)$$

$\vec{i}$ has a dimension of n and contains the sum of the currents through the passive elements into the corresponding node (either zero, or the sum of independent current sources). $\vec{e}$ has a dimension of m and holds the values of the independent voltage sources. After solving the system, the first n elements of $\vec{x}$ contain the voltages of the corresponding nodes and the next

m elements contain the current flowing in the corresponding voltage sources. To illustrate how this works, the small circuit in Figure 96 is analysed.

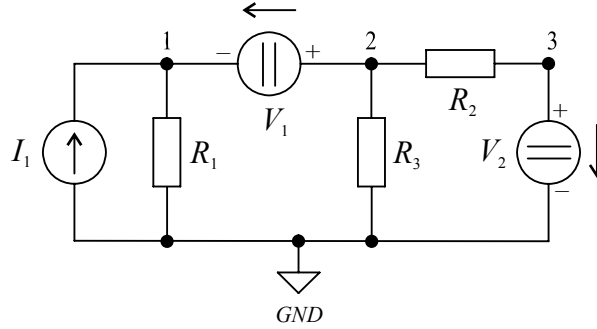


Figure 96: Simple circuit to illustrate MNA

For this circuit the matrices generated are:

$$\mathbf{G} = \begin{pmatrix} G_1 & 0 & 0 \\ 0 & G_2 + G_3 & -G_2 \\ 0 & -G_2 & G_2 \end{pmatrix} ; \quad G_i = \frac{1}{R_i} \quad (21)$$

$$\mathbf{B} = \begin{pmatrix} -1 & 0 \\ 1 & 0 \\ 0 & 1 \end{pmatrix} ; \quad \mathbf{C} = \mathbf{B}^T = \begin{pmatrix} -1 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix} ; \quad \mathbf{D} = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix} ; \quad \bar{\mathbf{z}} = \begin{pmatrix} I_1 \\ 0 \\ 0 \\ V_1 \\ V_2 \end{pmatrix} \quad (22)$$

Upon solving this system we get the voltages of the nodes 1 to 3 and the current in V_1 and V_2 .

The MNA methodology is used to analyse the resistive memory array. The simulations used to optimize the arrays are DC simulations because we are interested in the voltage levels on the different nodes in the first place rather than their transients. Using SPICE to simulate large arrays is very time consuming especially when large arrays are considered keeping in mind that a high number of simulations are required to optimize the array parameters which will be discussed later.

To accelerate the simulation, a software was developed to build the linear system using MNA methodology and then compressing the $\mathbf{A}$ matrix due to its high sparseness. Solving the system is performed by PARDISO linear solver [61], which is a direct solver for linear systems. The simulation speed is two to three orders of magnitudes higher than SPICE.

Table 3 shows a comparison between the time needed for the simulation of different array sizes using SPICE and the developed simulator.

Number of Array Cells	Special Software [s]	SPICE [s]	Acceleration Ratio %
100	<1	<1	1
1000	1	1	1
10000	2	120	60
100000	9	5040	560
250000	28	--	--
368640	40	--	--

Table 3: Comparison between the developed software and SPICE

3.4.6 Peripheral CMOS Circuits

In both active and passive arrays, a periphery is required to perform the read and write operations. The periphery of active memory arrays is well discussed in literature [1]. This periphery can not be used directly with passive arrays because we need multilevel operation for the drivers in passive arrays but only two levels in active arrays. Another aspect is the sense margin which is much higher for active arrays. Thus, the main differences are the drivers and their control circuits and the sense amplifiers. In the following, these circuits are discussed in more detail.

3.4.6.1 Write Operation Circuits

The circuits discussed here are used to write one bit of data to the memory using the VDD/3 scheme. By a simple modification multibits can also be written. Figure 97 shows the top cell for the writing circuits for a 16x16 array. The different blocks are used for decoding and driving the rows and column lines.

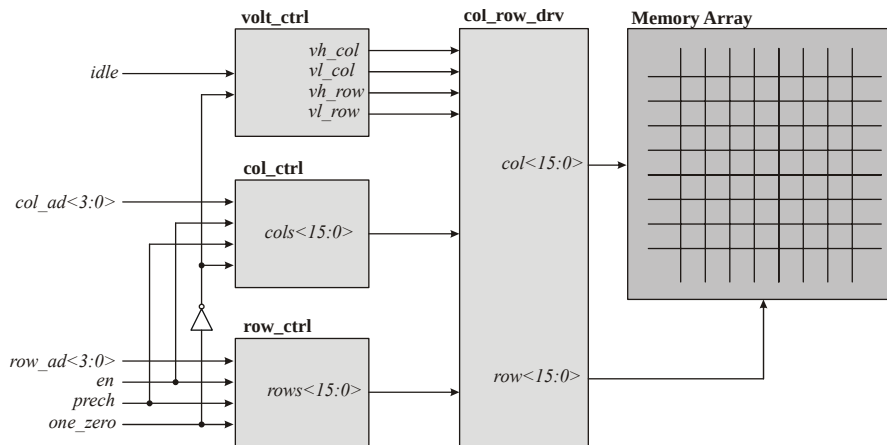


Figure 97: Top cell of the write circuit

The schematic of the block **volt_ctrl** is shown in Figure 98. This circuit generates four voltage levels, which are provided to the row and column drivers. The voltages are multiplexed to two lines because only two different voltages are required for the rows or columns. The signals *vh-row* and *vh-col* can have the voltages $3V_{dd}/2 + V_{thn}$ (*vdh_2_3*) or $V_{DD} + V_{thn}$ (*vdh*) and the signals *vl-row* and *vl-col* can have the voltages $V_{dd}/3 + V_{thn}$ (*vdh_1_3*) or *GND*. The term V_{thn} is the threshold voltage of an NMOS transistor. It is added to account for the voltage reduction at the source of the last driver transistor that is connected as a source follower.

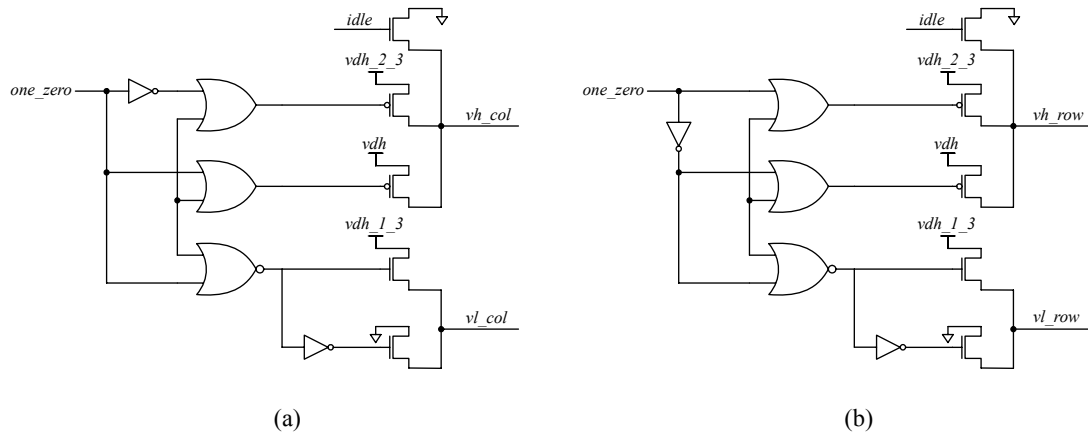


Figure 98: The voltage control block **volt_ctrl**

The schematic of the drivers of the rows and columns in block **col_row_drv** is shown in Figure 99. As mentioned before, the last stage of the driver is a source follower. A source follower is used to reduce the output resistance of the driver and because of the flexibility of controlling the output voltage [62, 63].

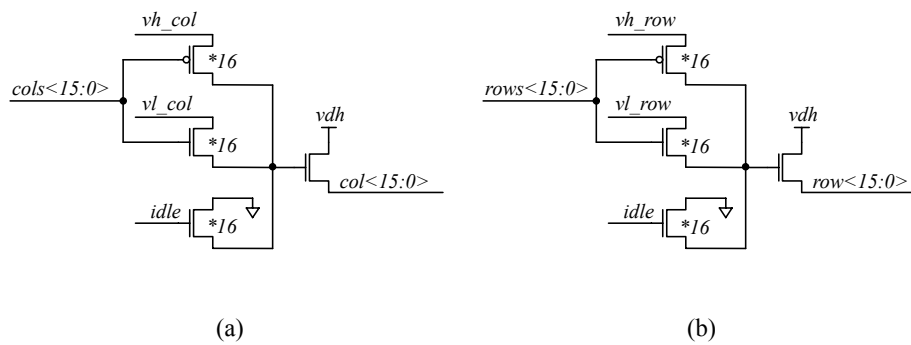


Figure 99: Column and row drivers

The selection of the voltages for the columns and rows is carried out via **col_ctrl** and **row_ctrl** blocks respectively. The schematic of the blocks is shown in Figure 100. Each block includes the decoders: **pullup_dec** and **pulldown_dec** which are shown in Figure 101 and 102. The **pullup_dec** pulls the selected address line high and lets all other lines floating. The

pulldown_dec on the other hand pulls the selected address high and lets all other lines floating.

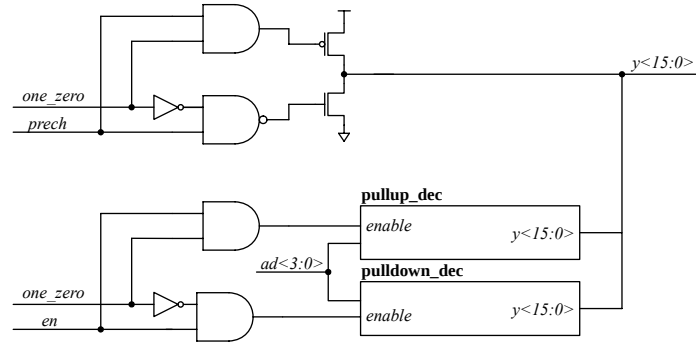


Figure 100: **col_ctrl** and **row_ctrl** schematic

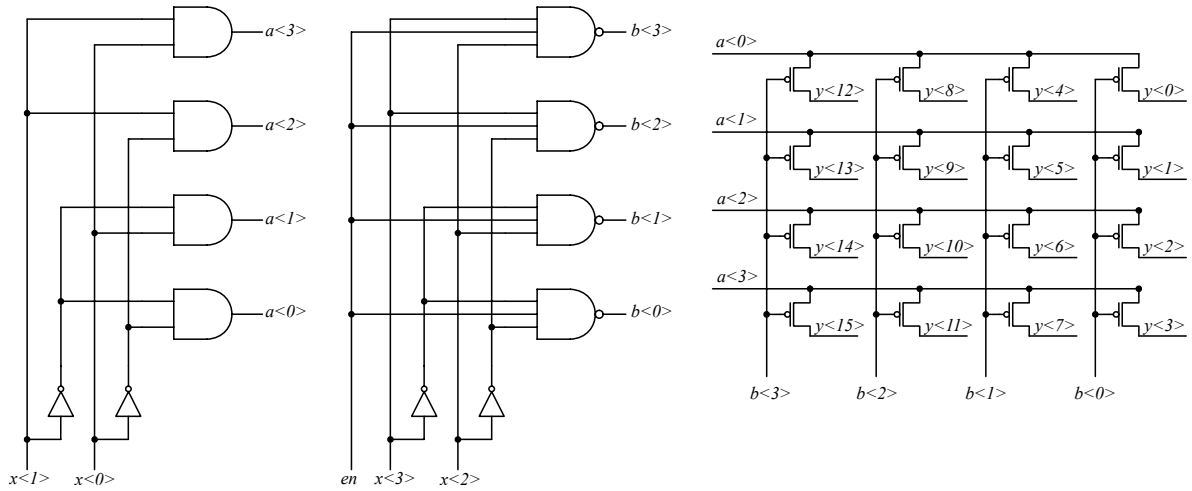


Figure 101: Pullup decoder **pullup_dec**

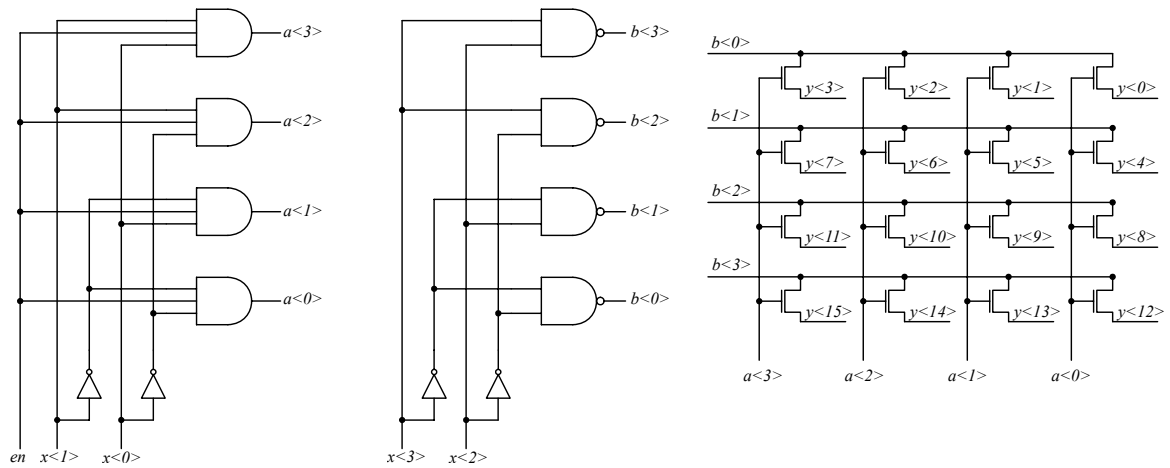


Figure 102: Pulldown decoder **pulldown_dec**

Figure 103 shows a simulation of writing a “1” in the cell in the 14th row and 13th column of the memory array. At first, the address lines are precharged with the signal *prech*. After that, the decoders are enabled to activate the required addresses using the signal *en* then write is performed when the signal *idle* is low.

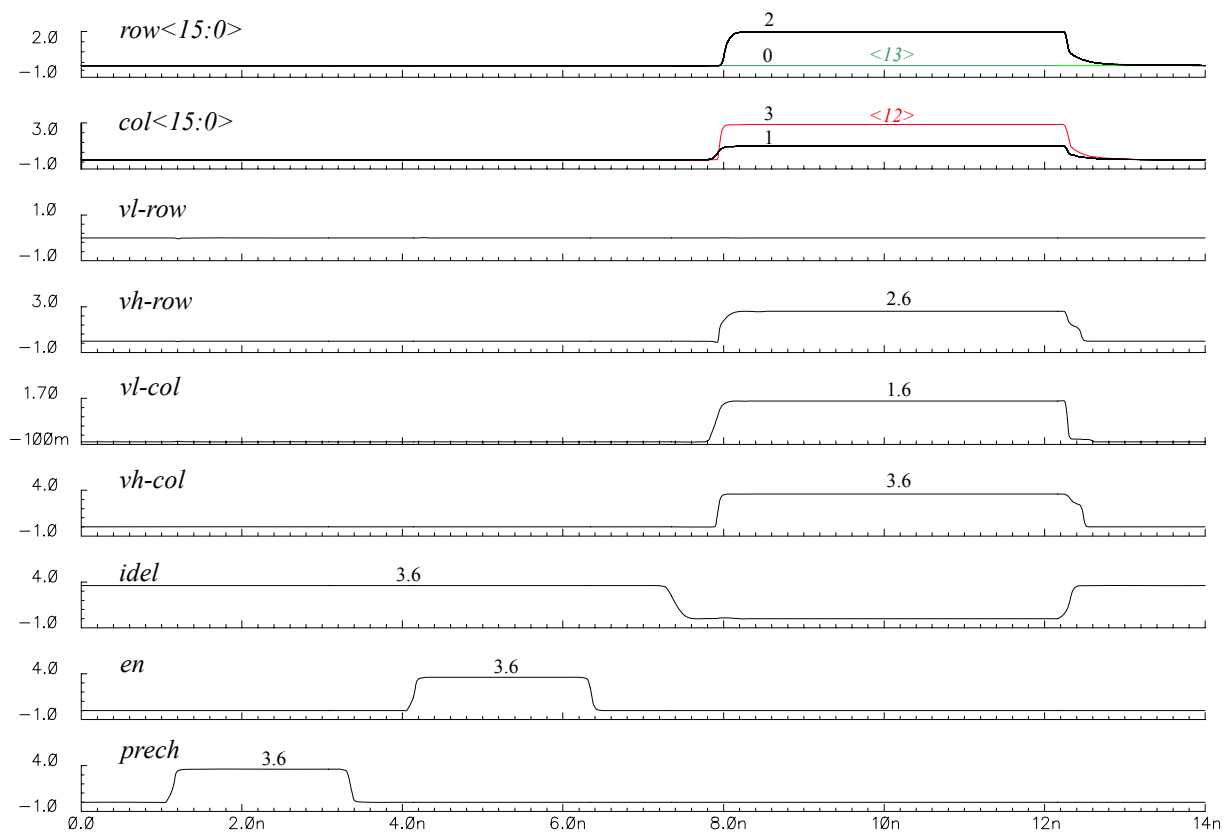


Figure 103: Simulation of the write circuit

3.4.6.2 Read Operation Circuits

The read operation uses a reduced voltage to activate the rows. The row to be read is activated and all other rows are left open. The sense amplifiers are shared by a group of columns to reduce their number. To accomplish this, the columns are connected to a multiplexer (analog switch), which selects one column from this group (Figure 104). The selected column is then compared with a reference value to determine the state of the corresponding memory cell. The reference voltage generation is discussed in more detail in section 3.4.8.

The sense amplifiers used to determine the stored values are very similar to conventional sense amplifiers. The main difference is the higher sensitivity because of the reduced sense margin which is much higher in DRAMs and SRAMs [1] than in passive resistive memories. This small margin is found in MRAMs which have a sense margin of few millivolts [64, 65]. The main problem encountered with the reduced sense margin is that it is comparable to the

offset voltage of the sense amplifier. This offset occurs because of mismatches of the used transistors due to uncertainties in each step of the manufacturing process [66].

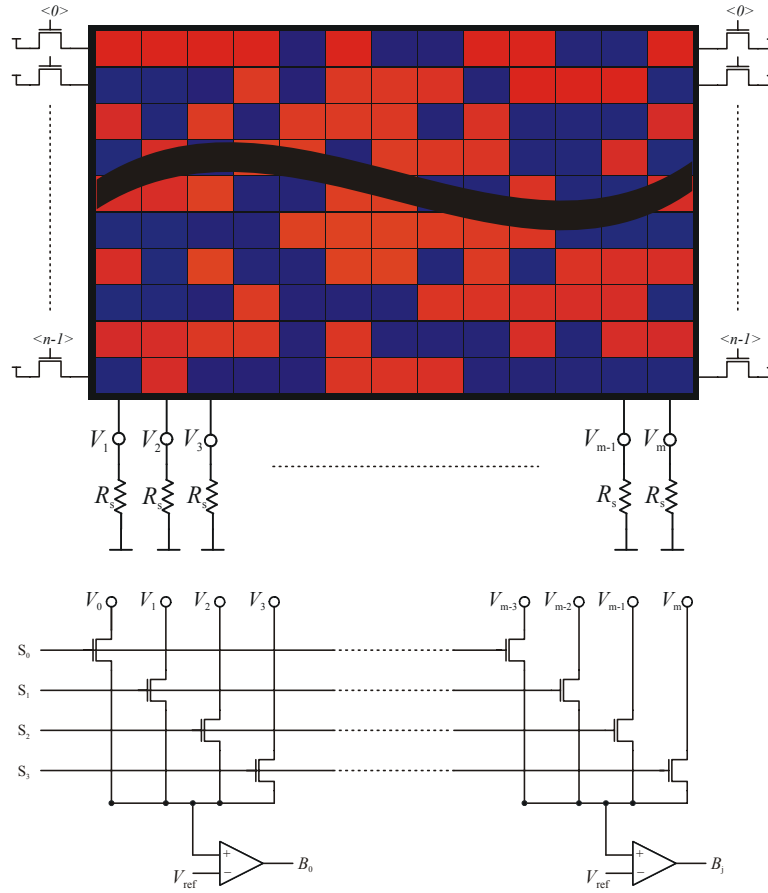


Figure 104: Read circuit schematic

The offset voltage can be reduced by using auto-zero op-amps as sense amplifiers. These amplifiers use techniques of offset cancellation to reduce the offset voltage to the microvolt range. The idea behind auto-zeroing is that the offset of the amplifier is stored on a capacitor then it is provided to the input in a next step as shown in Figure 105.

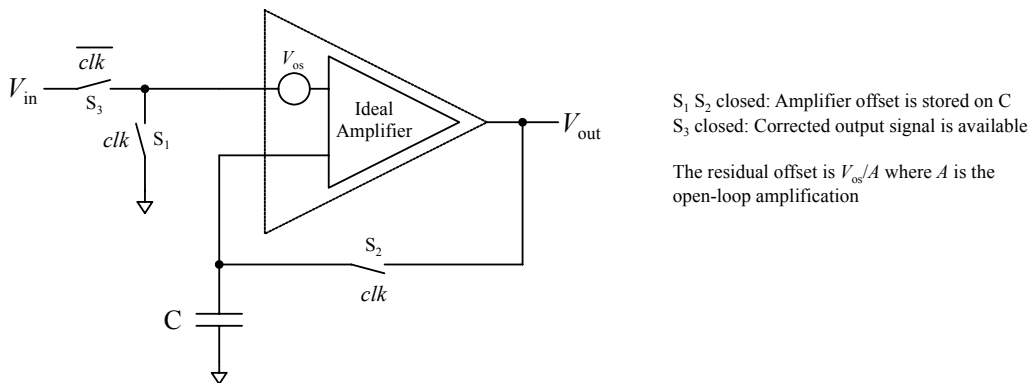


Figure 105: The Concept of auto-zeroing

Care must be taken to avoid the effect of charge injection when the MOSFETs are switched which is discussed thoroughly in literature [66, 67].

3.4.7 “Write” Simulation and Optimization

As was mentioned in the principle function of the crossbar array in section 3.4.1, there are two known writing schemes for passive crossbar arrays. Since the elements of the array and drivers are not ideal, we can expect that some kind of distortion would happen.

There are two conditions that have to be satisfied, so that the write operation works properly. First, the voltage drop on the accessed cells (access voltage) should exceed the switching threshold voltage of the cells. Secondly, the voltage drop on non-accessed cells (distortion voltage) is not allowed to exceed a certain value to ensure that the states of the non-accessed cells is not altered or disturbed.

Software was developed to investigate the access and distortion voltages and to optimize the size of the array accordingly. A snapshot of the simulation software is shown in Figure 106.

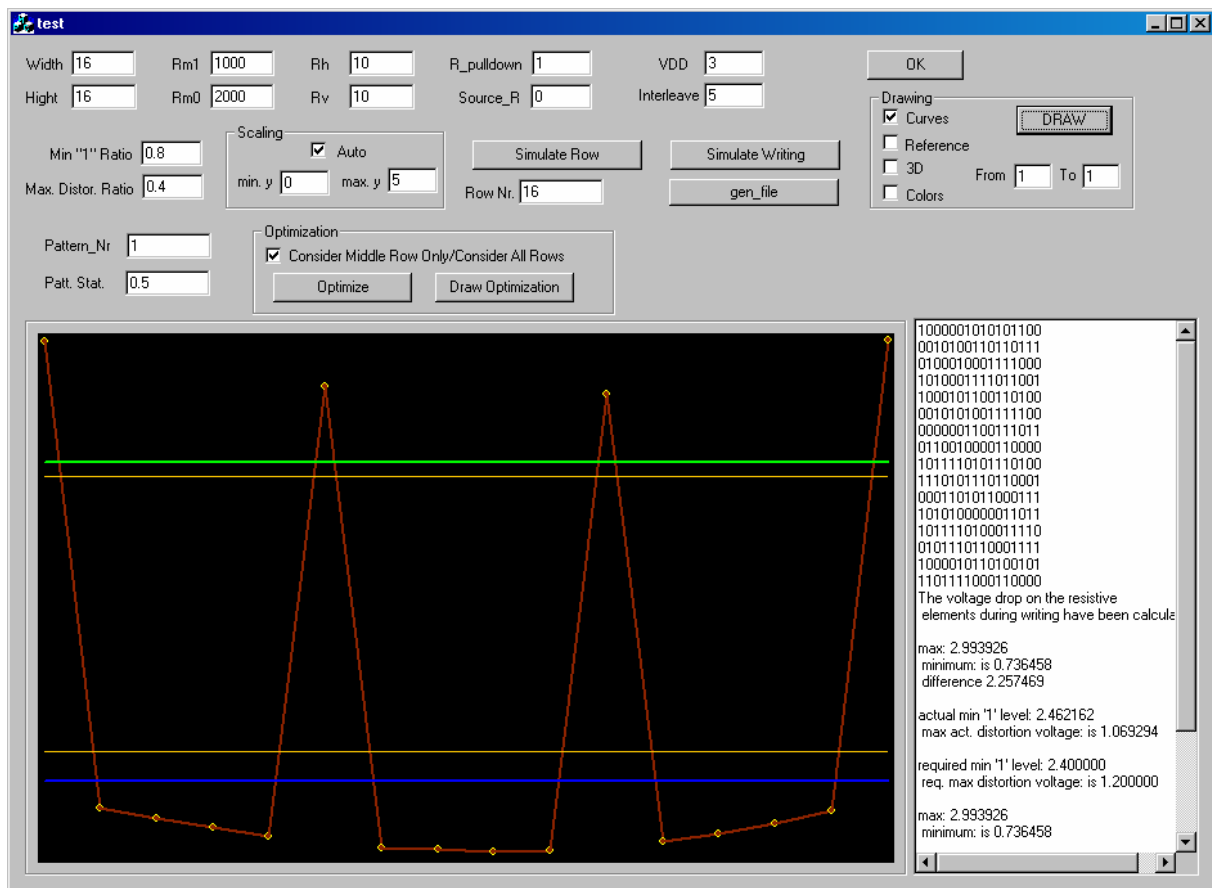


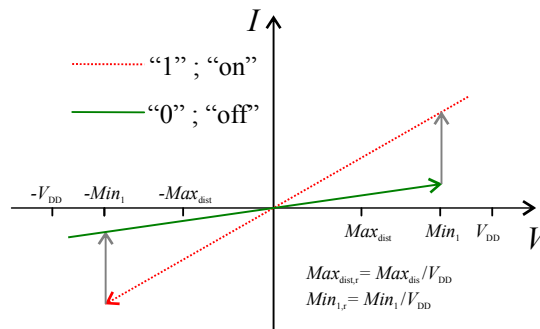
Figure 106: Simulation program snapshot

Table 4 explains the meaning of the most important fields in the software window.

Variable/Field Name	Explanation
W	The width of the memory field
H	The height of the memory field
R_{m1}	The “on” resistance of the resistive element
R_{m0}	The “off” resistance of the resistive element
R_h	The resistance of the interconnect between two horizontally adjacent cells
R_v	The resistance of the interconnect between two vertically adjacent cells
R_{pull}	The effective resistance of the pull down transistor
R_{src}	The effective resistance of the voltage source (pull up transistor)
V_{DD}	The supply voltage
<i>Interleave</i>	The interleaving factor which determines the distance between the accessed cells
$Min_{1,r}$	The ratio between the minimum voltage required for switching to V_{DD}
$Max_{dist,r}$	The ratio between the maximum allowed distortion voltage to V_{DD}
Row Nr.	The number of the row to be simulated in the “Simulate Row option”
Pat. Nr	Determines which pattern is filled in the memory matrix
Pat. Stat.	Some patterns use this variable to define statistical distribution
Consider middle row	Used through optimization and determines if the middle row only is used as a worst case or if all rows have to be tested

Table 4: Simulation program variables

The meaning of $Min_{1,r}$ and $Max_{dist,r}$ is illustrated in Figure 107. The ratio is used instead of direct values to make the simulations V_{DD} independent. The I/V curve used here is inverted in comparison to the one discussed in section 3.1, which is valid because it is just a polarity exchange.

Figure 107: The meaning of the Voltages $Min_{1,r}$ and $Max_{dist,r}$

3.4.7.1 Voltage Degradation

Figure 108 shows a simulation of the voltage drop on the memory cells when the first row is accessed. An interleaving factor of 5 is used in this simulation. As can be seen the voltage drop on the accessed cells is much higher than the voltage drop on non-accessed cells which must be always the case. The degradation of the voltage is also apparent. By moving from the sides toward the middle of the row, the voltage drop on the accessed cells decreases. This degradation of the voltage level is not allowed to fall below Min_1 . We conclude that the worst case for the access voltage is in the middle of the row.

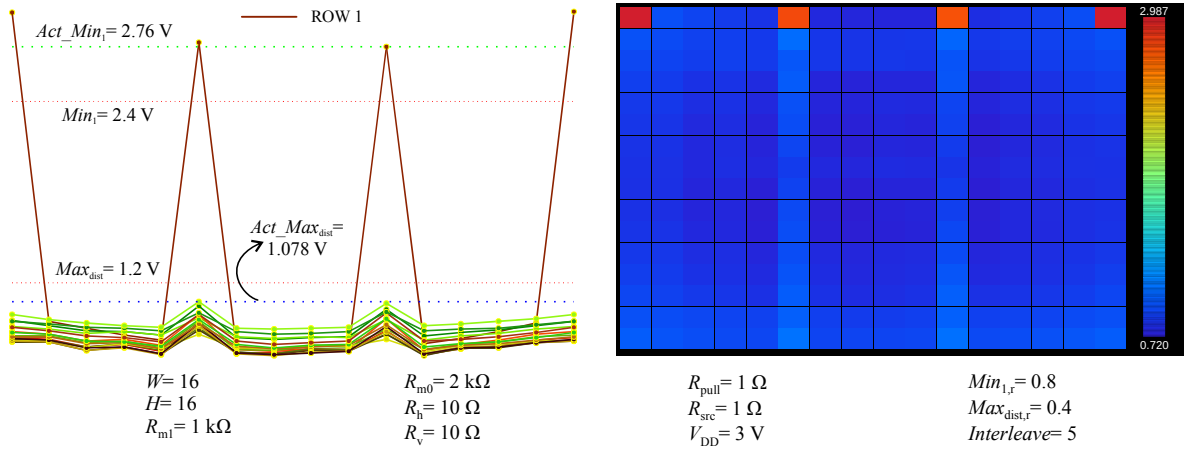


Figure 108: Voltage drops resulting from simulating the first row of the memory field

By comparing the simulation of accessing the first row with that of accessing the eighth row (the middle row) as shown in Figure 109, it can be seen that the voltage drops on the accessed cells are higher in the first row. The last row is equivalent to the first row because we have drivers at the top and bottom of the field. This means, that the worst case for the access voltage is in the center of the memory field.

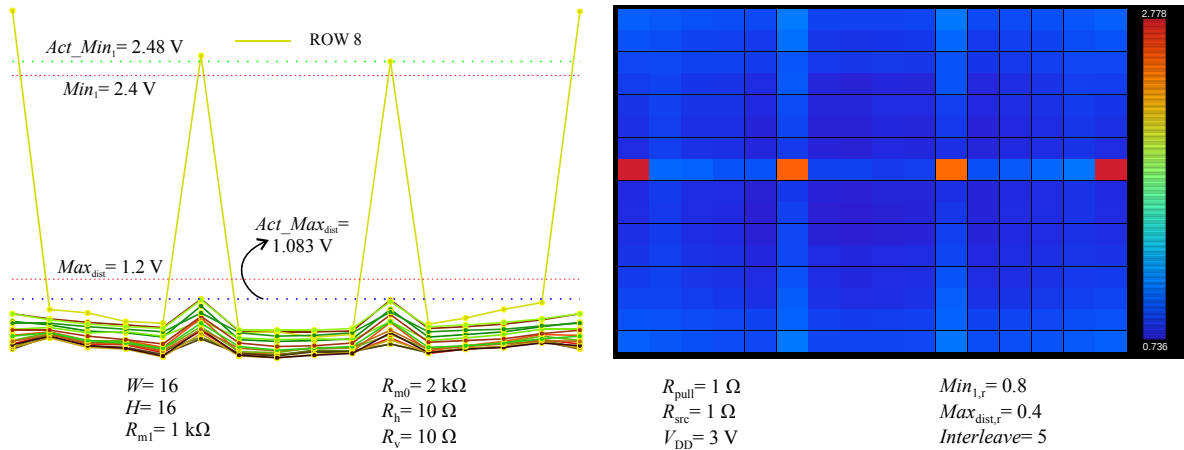


Figure 109: Voltage drops resulting from simulating the eighth row of the memory field

The distortion voltage has its maximum in the first and last rows of the memory field regardless of the accessed row. By comparing the worst case for the distortion voltage in Figures 108 and 109 we find that it is higher when the middle row is accessed.

From the previous discussion we see that for finding the worst cases, we only need to simulate the access of the middle row (or rows if H is even) and test if the access voltage in the middle row falls below Min_1 or if the distortion voltages at the cells in the first and last rows are higher than Max_{dist} . It must be noted that we assumed the existence of the drivers at top, bottom, right, and left sides of the memory field and that $V_{DD}/3$ scheme was used.

3.4.7.2 Interleaving

Interleaving is used for two reasons. First, it is used to access a subset of the row. For example, a row may contain 32 bits but write is performed byte wise. The second reason is to enhance the voltage level across the accessed cells. Every cell that is accessed draws current from the row and hence from the source. Having more accessed cells in a row means that more current would be drawn. Due to the parasitic source and row resistances, the voltage drop on all cells and especially at the cells in the middle of the row would be reduced.

To illustrate this, simulations are performed on a 48x32 array using an interleaving factor from 1 to 25 (Figure 110). All cells in the field are assumed to store “1”s and the column in the middle of the 16th row is always accessed. As can be seen, the access voltage is higher for higher interleaving factors but at the same time the distortion voltage is higher. The best case for the access voltage is when only one cell in the row is written.

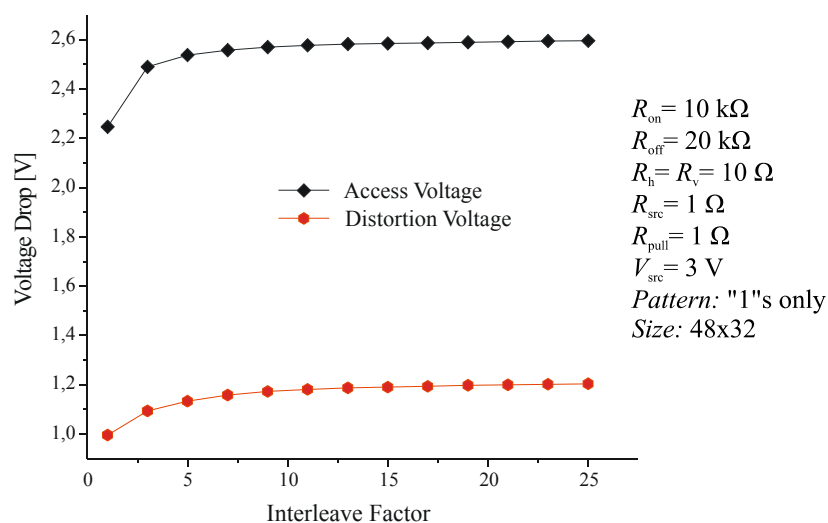


Figure 110: Effect of the interleave factor

For writing a word that has more bits than the number of bits accessed during writing due to interleaving, the write operation must be performed more than one time to write the whole word. This means that in such cases, the time for writing would be longer. Consequently, a trend between the interleaving factor, word length, and write time must be found.

3.4.7.3 Pattern Dependency

Another factor that influences the access and distortion voltages is the stored pattern in the memory field. The parasitic currents through the non-accessed cells reduce the current in the accessed cells and hence the voltage drops across them. If the non-accessed cells are low ohmic which means if they store “1”s, the access voltage across accessed cells is reduced. The data content of cells in the non-accessed rows influences the voltage drop also, but it is not as significant as the data content of the accessed row. The worst case for the voltage drop is when the memory field contains “1”s only. Figure 111 shows how the worst case voltage drop depends on the number of “1”s stored in the accessed row for a fixed interleaving factor of 5. All other cells of the field are assumed to contain “1”s.

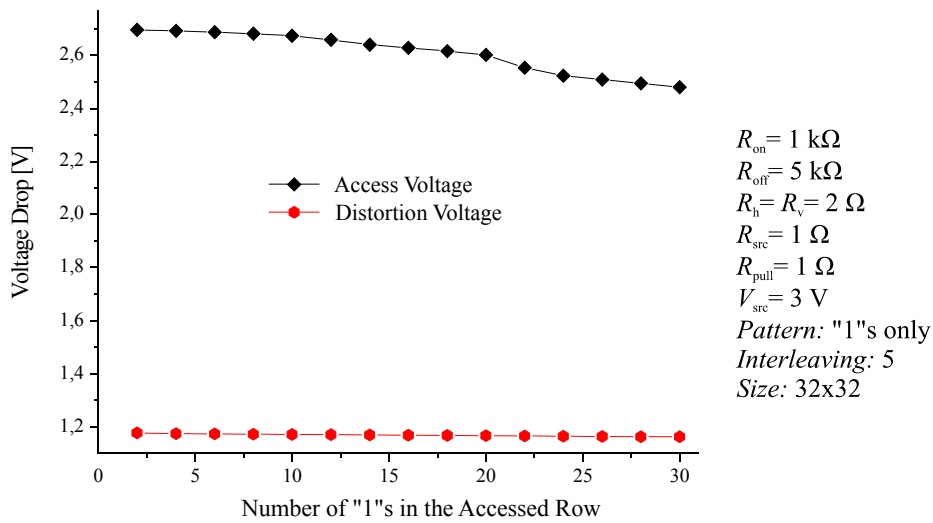


Figure 111: Effect of changing the number of “1”s in the accessed row

To reduce the effect of the pattern on the accessed cells, a pattern transformation can be performed before storing the data. This subject is discussed in detail in the read operation because the effect there is more severe.

3.4.7.4 Array Size Optimization

As we have seen in the last sections, there are many parameters that influence the access and distortion voltages. A very important issue is to determine the possible limits for the dimensions of memory field depending on predefined parameters. Some of the used

parameters are fixed and depend on the used technology like R_{on} , R_{off} , R_h , $Min_{1,r}$, $Max_{dist,r}$ and R_v . Other parameters like W , H , and the interleave factor are design dependent and can be varied. There is more than one possible maximum size for the memory field that functions error free.

To perform optimization we use a very important rule which states that the larger the matrix, the higher the voltage degradation. This applies for both the width and the height of the matrix. This trend simplifies the optimization process because we don't need to test every possible size of the matrix, but instead we search for the maximum limits. Any size that falls within these limits is a valid size.

The optimization starts by defining all required parameters with the exception of H and W . The condition for a functioning array is that the worst case voltages for the access voltage and the distortion voltages are not below or over the predefined voltages Min_1 and Max_{dist} respectively. Any violation of either condition is a decision point for the optimizer.

After defining the parameters a seed array of 8x8 elements is defined as seen in Figure 112. All elements of the array contain "1"s to produce the worst case for the write operation. The matrix is simulated and the violations of the conditions, if any, are detected.

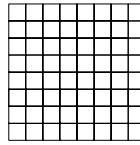


Figure 112: Seed Array

If there are no violations, the matrix is enlarged horizontally by a factor of 2 and a new simulation is performed. This procedure is repeated until a violation happens. At this point we have exceeded the maximum possible width for an eight column array.

The next step is to find this maximum width, which is performed by using successive approximation of the width as illustrated in Figure 113.

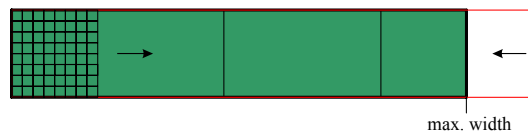


Figure 113: Finding the maximum width using Successive Approximation

The matrix with the maximum width is considered a base for the next simulation steps. The base matrix is divided into a predefined number of blocks which represent arrays with

different widths but the same height. All these arrays function error free because they are subarrays of the base array as seen in Figure 114.

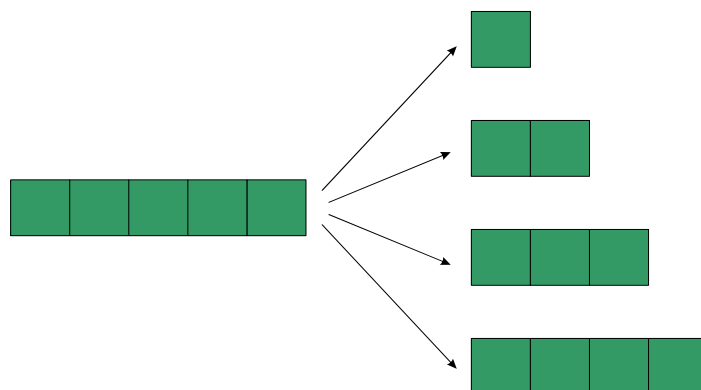


Figure 114: The base array is divided into subarrays

The next step is to find the optimal height for each of these subarrays, which is calculated using the same successive approximation procedure like before as illustrated in Figure 115.

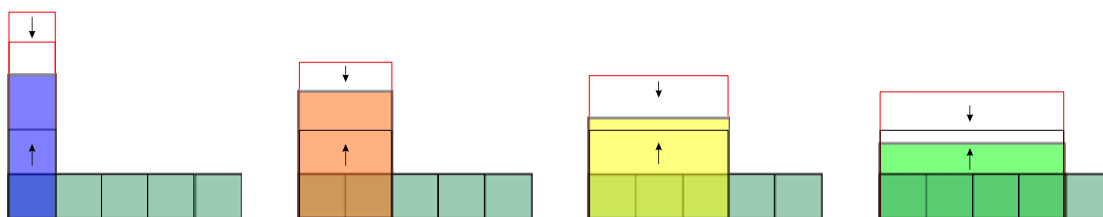


Figure 115: Finding the maximum height for the subarrays

As we mentioned before, the calculated dimensions represent maximum values and any array that has smaller dimensions will work error free. Thus, by combining the results of the optimizations as seen in Figure 116, we get a discrete curve. The area under this curve represents valid array dimensions. The curve steps can be made finer if we make more divisions for the base matrix.

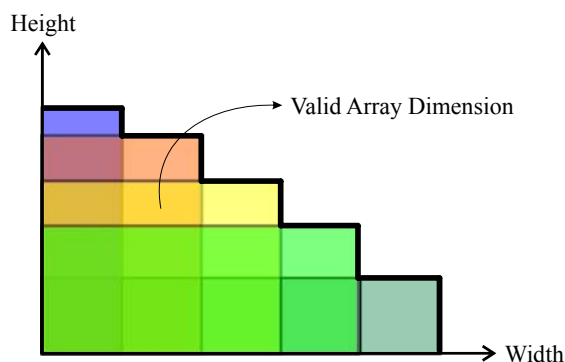


Figure 116: The union of the optimization results

The result of applying this optimization method using real values is shown in Figure 117.

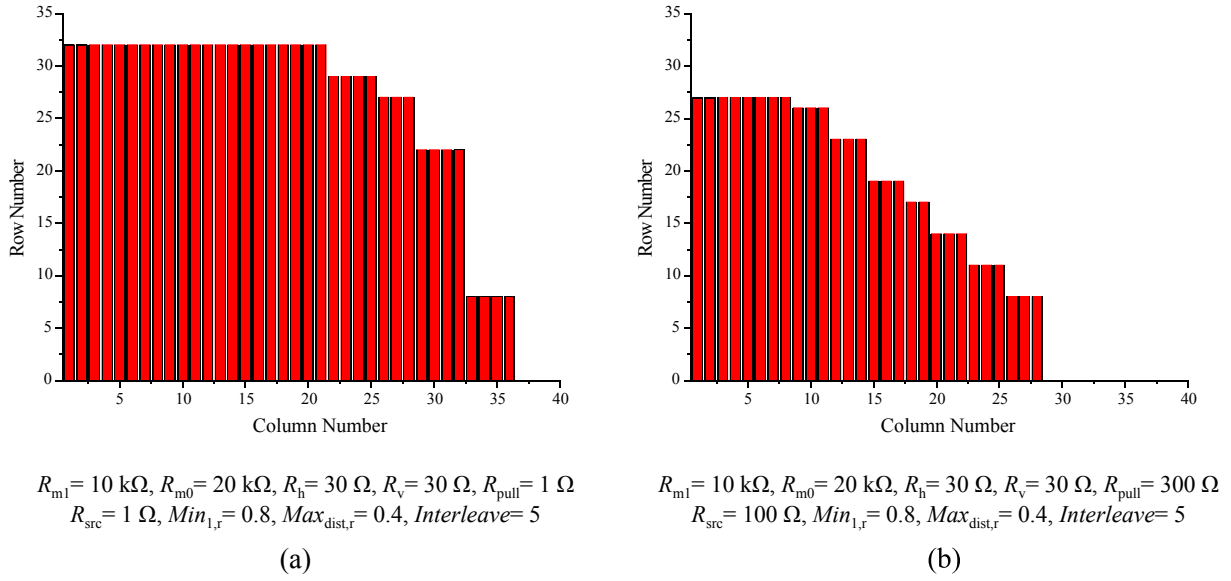


Figure 117: Optimization result using (a) $R_{\text{pull}} = R_{\text{src}} = 1 \Omega$ and (b) $R_{\text{pull}} = 300 \Omega$, $R_{\text{src}} = 100 \Omega$

By choosing another parameter as a variable, a 3D curve can be represented, under which the arrays function error free. Figure 118 shows an optimization by using R_{on} as a parameter and a population of 50%. As can be seen, the higher the R_{on} value the larger the size of the functioning arrays.

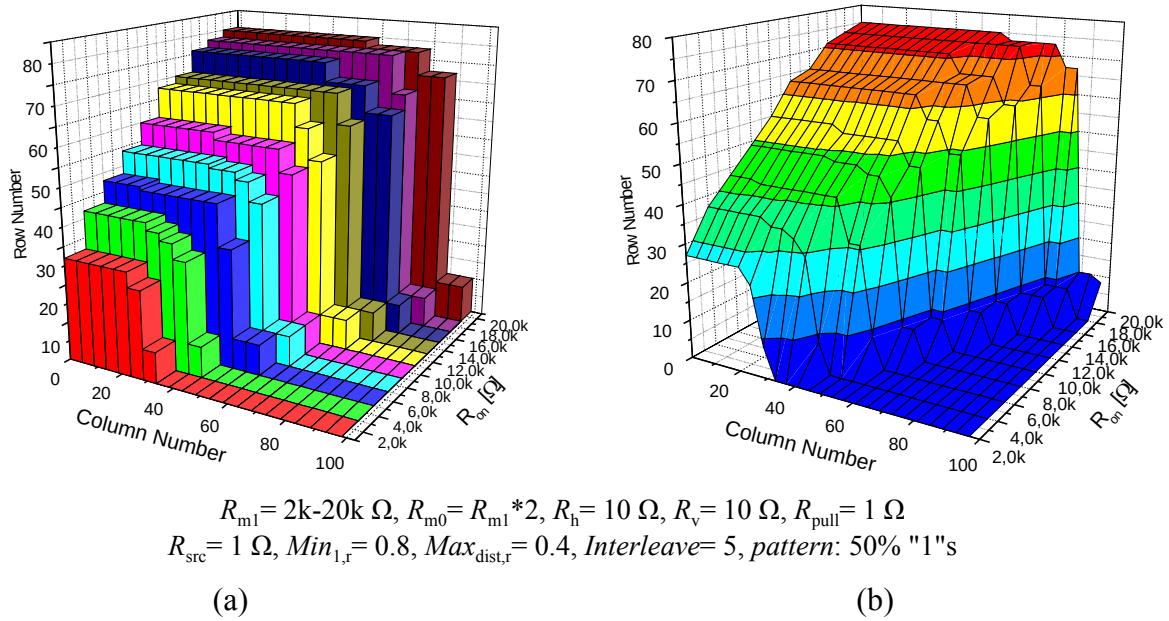


Figure 118: (a) Optimization result using R_{on} as a parameter and 50% population (b) The hull of the result under which the arrays function error free

By performing an optimization using the same value as in the last optimization with the exception of the population which is now 100%, we can see that the size of the arrays is reduced (Figure 119). This result emphasises the influence of the pattern on the size of the array.

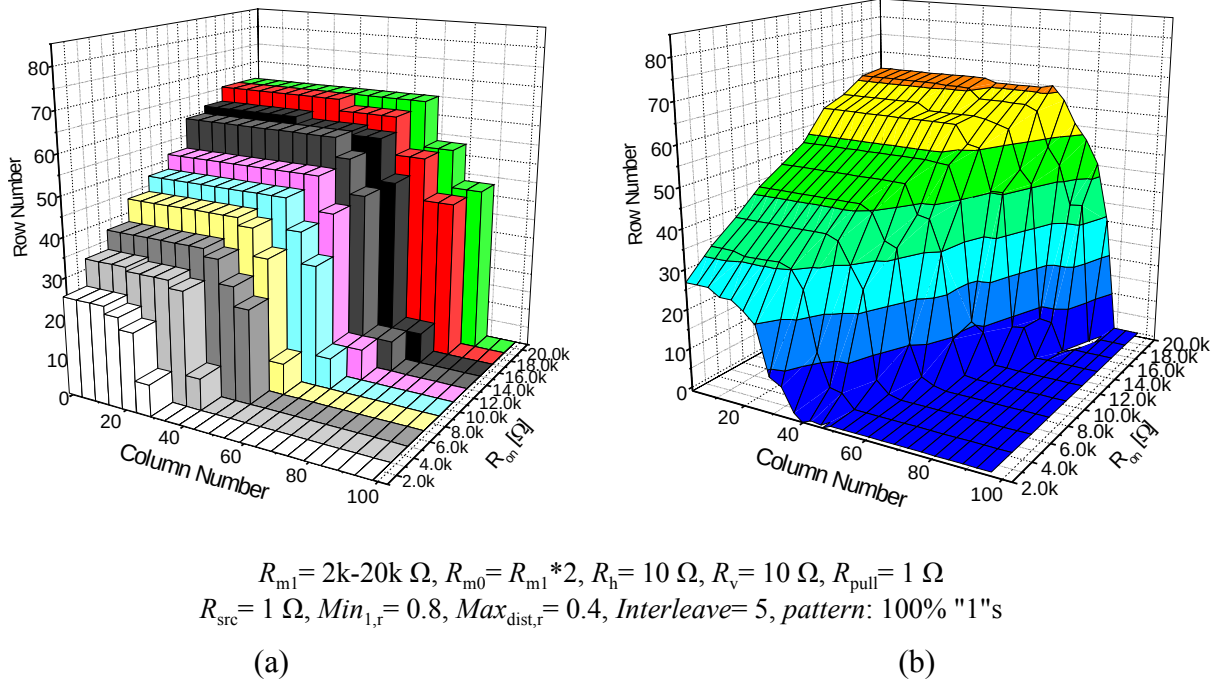


Figure 119: (a) Optimization result using R_{on} as a parameter and 100% population of the array, (b) The hull of the result

3.4.8 Read Simulation and Optimization

Two conditions have to be satisfied in order to obtain a correct read operation. The first condition is to have a non-destructive read operation, which means that the read operation does not alter the content of the read (accessed) cells and the non-accessed cells. The second condition is to have a sufficient voltage margin (sensing margin) to discriminate between a “1” and a “0”.

The first condition can be easily satisfied if a reduced voltage is used for reading. This voltage is equivalent to the maximum allowed distortion voltage in the write operation. The second condition is more complicated to satisfy and depends on many parameters. Some of these parameters are material dependent and others are design dependent.

Software was developed to investigate the sensing margin of the accessed cells and distortion voltages and to optimize the size of the array according to them. A snapshot of the simulation software is shown in Figure 120.

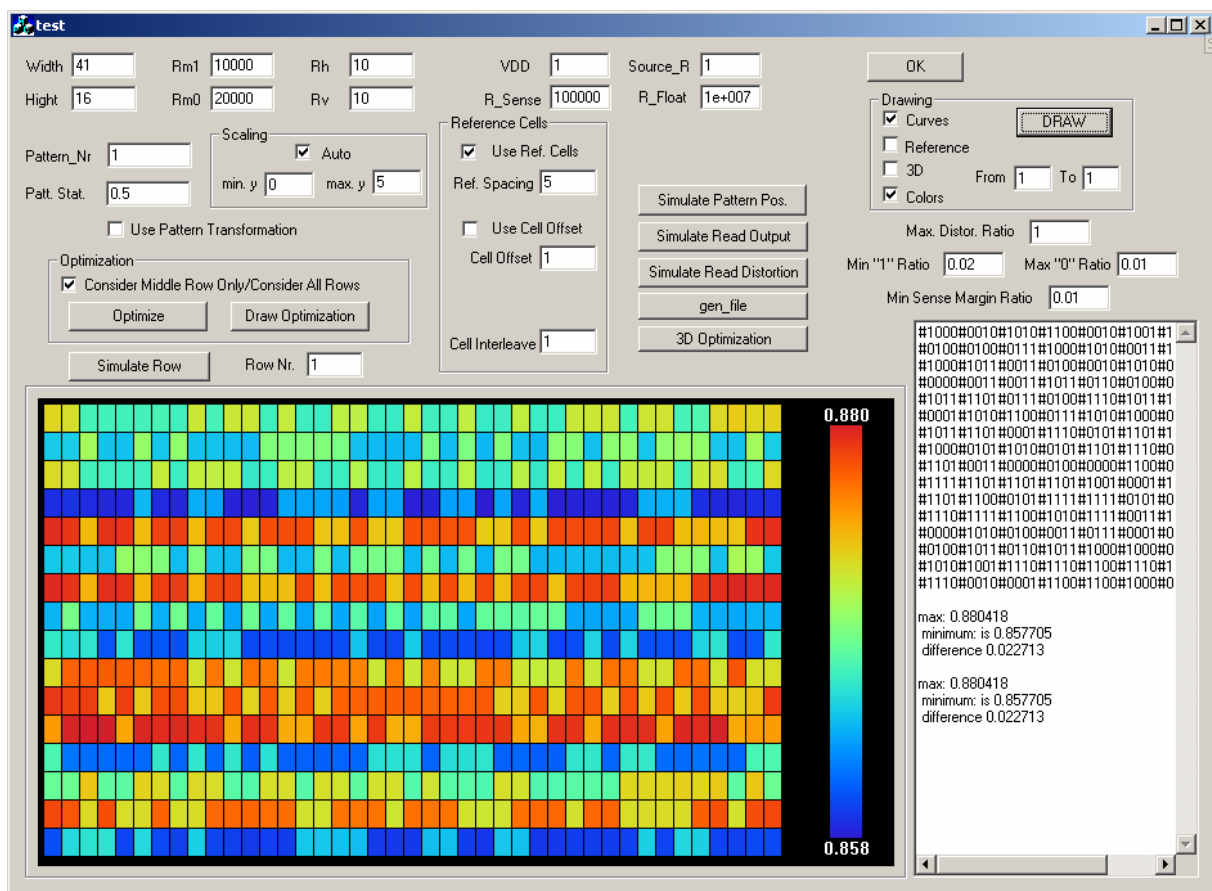


Figure 120: Simulation program snapshot

Table 5 explains the meaning of the most important fields in the software window.

Variable/Field Name	Explanation
W	The width of the memory field
H	The height of the memory field
R_{m1}	The “on” resistance of the resistive element
R_{m0}	The “off” resistance of the resistive element
R_h	The resistance of the interconnect between two horizontally adjacent cells
R_v	The resistance of the interconnect between two vertically adjacent cells
R_{src}	The effective resistance of the voltage source (pull up transistor)
R_{float}	The resistance from a node to GND when the node is floating
V_{RD}	The read voltage
Ref. Spacing	The distance between two adjacent reference cells
Min. Sense Margin	The minimum voltage required for switching to V_{DD}
Row Nr.	The number of the row to be simulated in the “Simulate Row option”
Pat. Nr	Determines which pattern is filled in the memory array
Pat. Stat.	Some patterns use this variable to define statistical distribution
Consider middle row	Used through optimization and determines if the middle row only is used as a worst case or if all rows have to be tested

Table 5: Simulation program variables

3.4.8.1 Sense Margin Degradation

In contrast to the read operation in the ideal case (section 3.4.1), the real read operation involves degradation of the voltage drop on the accessed cells and output voltages. In a pure resistive memory array, all memory cells are coupled with each other. This means that accessing any cell will influence all other cells in some way and vice versa. This happens because access/isolation elements like transistors or diodes don’t exist. We add to this that the interconnects are not ideal and there is a voltage drop across them. This voltage drop degrades the voltage levels in the rows and columns. The amount of degradation depends on many factors that are going to be discussed in detail later on. We will assume that we use access voltages which are equal or under the maximum allowed distortion voltage to guarantee a non-destructive reading.

Figure 121b shows the output voltages obtained by reading a row from a 64x16 memory array using one voltage source (Figure 121a). All non-accessed rows are left floating. The columns are connected to sense resistors from the top or bottom side depending on the position of the accessed row. If the row is in the upper half of the array, the top side is connected to sense resistors and the bottom side is left open. Otherwise, the bottom is connected to sense resistors and the top is left open. The connection/disconnection is performed using CMOS

transistors. The resistance of the transistors is considered as a part of the sense resistor as was shown in section 3.4.4. The degradation of the voltage levels is apparent and increases by moving away from the voltage source.

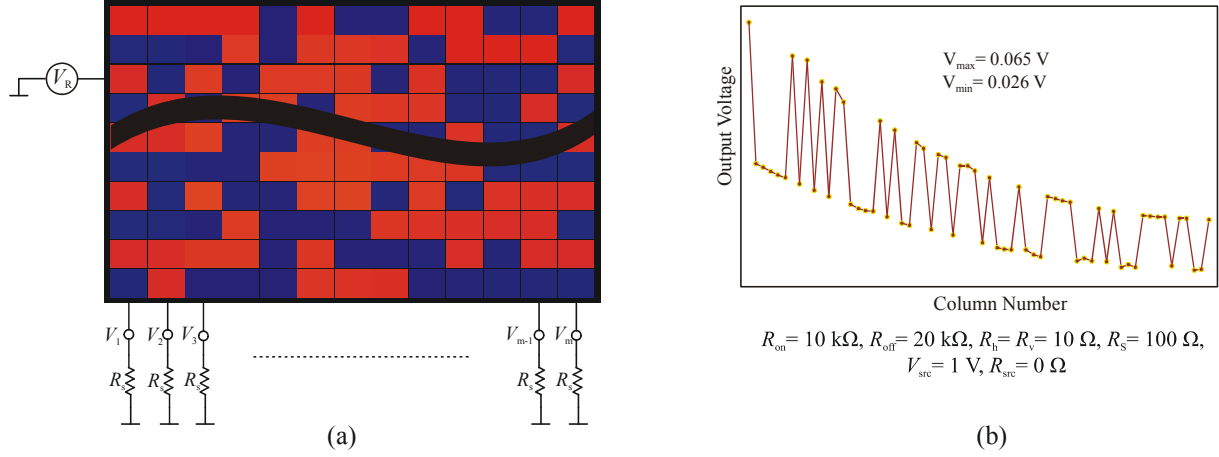


Figure 121: (a) Passive array connected to a single voltage source, (b) Simulation result of reading a row from the array

The voltage levels are improved by using a second voltage source at the other side of the row as can be seen in Figure 122.

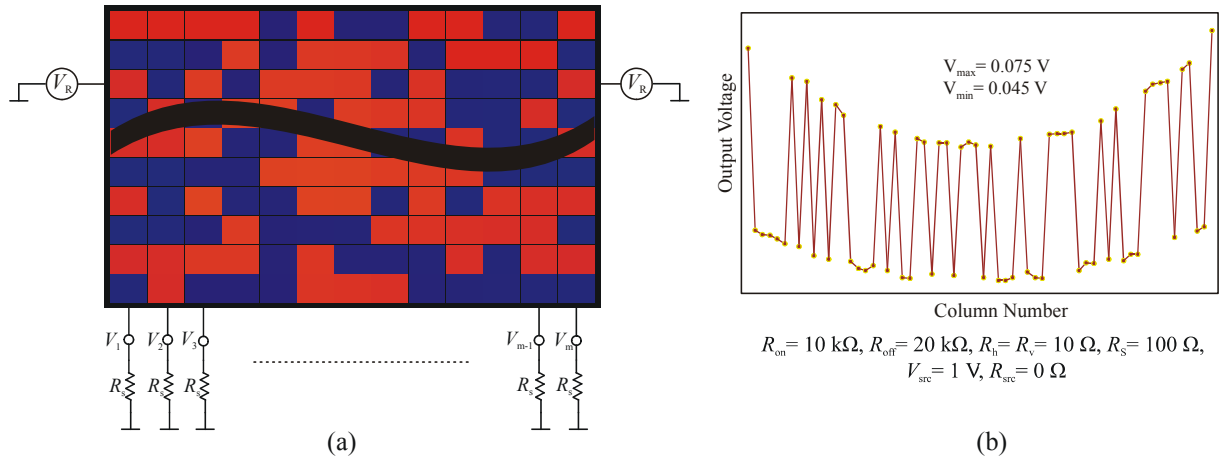


Figure 122: (a) Passive array connected to two voltage sources, (b) Simulation result of reading a row from the array

By choosing a relatively high value for the sense resistor ($R_s = 100 \text{ k}\Omega$) and keeping all other values, not only the values of the “1”s and “0”s degrade as in the previous case, but they are also shifted according to the row and its content (Figure 123).

It is essential to have a reference voltage to discriminate between the “1”s and “0”s. This reference voltage is ideally the average value of the “1”s and “0”s. As we have seen, using a

constant reference voltage is not possible because the values of the “1”s and “0”s vary strongly according to their location in the array and according to the distribution of the “1”s and “0”s. It is also important to have an acceptable sensing margin to perform reading even if we have a reference voltage which has a value between a “1” and a “0”.

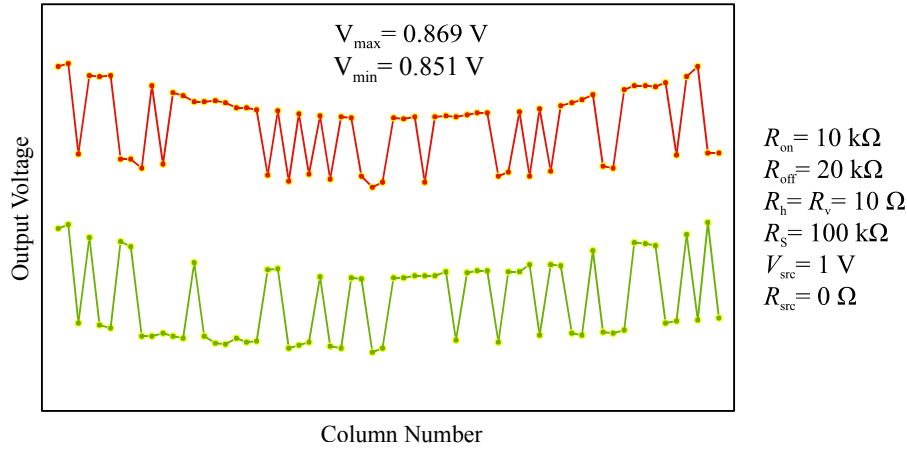


Figure 123: Simulation result of reading two rows from a passive array using relatively high R_s

3.4.8.2 Novel Reference Voltage Scheme

As we have seen in the previous section, a reliable reference voltage is inevitable to have a correct read operation. The cells in one row are locally strongly correlated regardless of the values of the sense resistors or the resistance values of the horizontal and vertical interconnects. This locality can be utilized to generate a reference voltage by dedicating some cells from each row to act as reference cells.

In this scheme every two horizontally adjacent reference cells generate a reference voltage for the cells between them as can be seen in Figure 124. The number of reference cells is determined depending on the grade of degradation of the output voltages. Higher voltage degradation will require more reference cells.

The values stored in the reference cells in a row are “1” and “0” (low and high ohmic) alternately. The first and last cells in a row are always reference cells. The horizontal position of the reference cells is identical in all rows, which constructs columns of reference cells (reference columns). Vertically adjacent reference cells have also values of “0” and a “1” alternately. Reference cells are physically the same as normal memory cells; however they are preprogrammed with constant values to generate the reference voltages. To generate the reference values, every two adjacent reference columns are connected together using two identical capacitors. The equivalent circuit of any two adjacent reference cells in any row is shown in Figure 125.

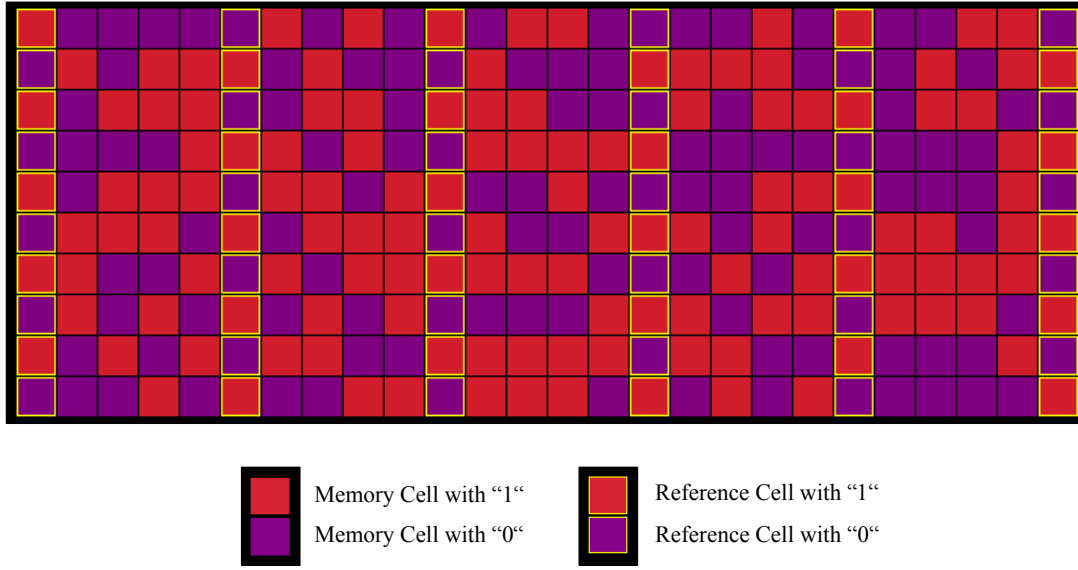


Figure 124: Passive array after the insertion of reference cells

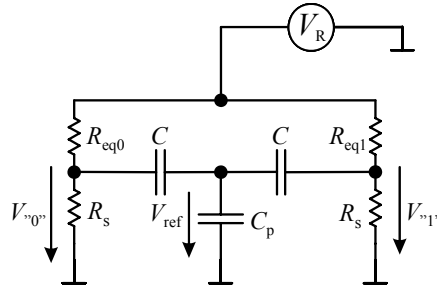


Figure 125: Equivalent circuit of generating the reference voltage

Capacitor C_p represents the parasitic capacitance of the interconnects and the input capacitance of the amplifier. When voltage is applied to the row, a voltage will develop on the sense resistors. In the steady state, the voltage developed on the sense resistors will not be affected by the capacitors and will represent either a “1” or a “0”. At this instance, the voltage on the common node of the capacitors (assuming an initial condition of 0 V) is given by:

$$V_{\text{ref}_i} = \frac{C \cdot (V_i + V_{i+1})}{2C + C_p} \quad (23)$$

By choosing a value for C , which is large enough, compared to C_p the reference voltage is approximated by:

$$V_{\text{ref}_i} = \frac{V_i + V_{i+1}}{2} \quad (24)$$

which is the average of the voltages generated by the two reference cells. Other means for generating the average value using op-amps are also possible.

Figure 126 shows a simulation of two rows of a 64x16 bits memory, which is an 81x16 crossbar array after inserting the reference cells, with a distance of 5 cells between them. Large circles indicate the positions of the reference cells. The horizontal lines in the simulation represent the local reference values generated for the reference cells. It can be clearly seen, that the reference values are adjusted according to the row position that has been read and the position of the reference cells in the row. The strong correlation between the reference cells and their horizontal neighbours is also apparent.

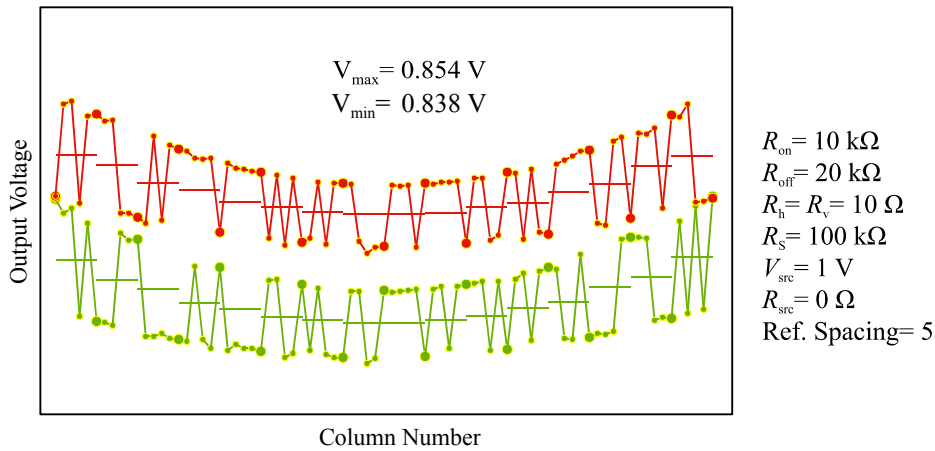


Figure 126: Simulation result of reading two rows from a memory array where reference cells are used to generate local references

To utilize this scheme, the circuit shown in Figure 127 is used. In this circuit the memory field is divided horizontally into segments. The memory columns between two adjacent reference columns are considered a segment. The cells in a segment are multiplexed to reduce the required number of amplifiers needed for sensing as a result the area of the memory is reduced.

This reference scheme facilitates the construction of large passive arrays which is important for future memory technologies where molecules and nano-wires are used. This concept can be extended to be used with any kind of passive arrays including those with diodes or zener-diodes.

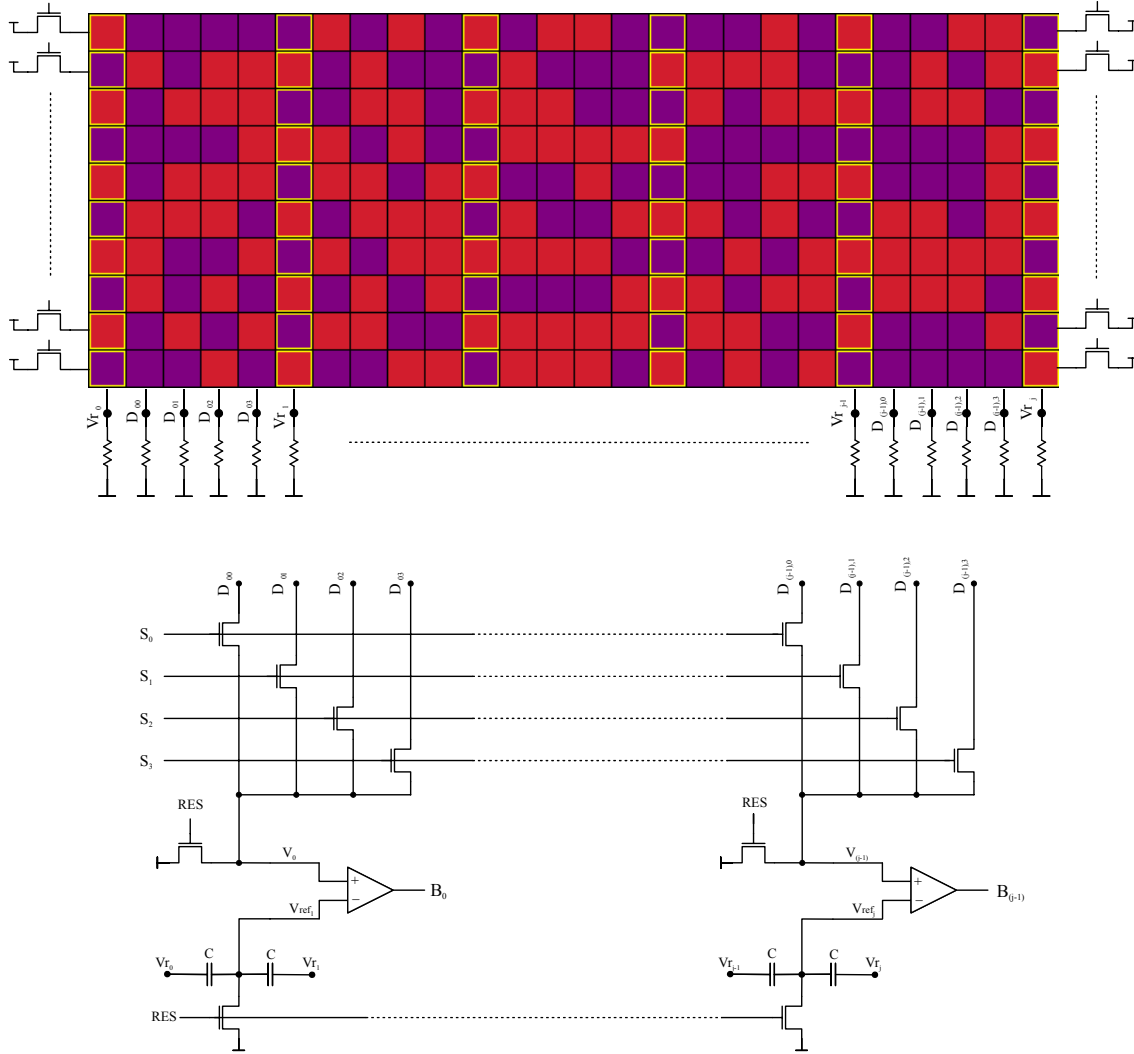


Figure 127: Circuit used to perform reading and reference voltage generation

3.4.8.3 Pattern Dependency

Like the case in writing to the memory field, the stored pattern influences the read operation. The influence of the stored pattern is more severe in the case of reading because of the use of sense resistors that have relatively higher values than the drivers in the write case. This means that the voltage drop at these resistors is higher which influences the other cells more. There are worst case patterns for the “1”s and “0”s that can be used to optimize the size of the arrays. A list of the patterns used is shown in Appendix A. To illustrate this we take the pattern shown in Figure 128a as an example. This pattern produces a worst case for the “1”.

The cell with the highest degradation is in the eighth row and ninth column. The output voltage of the row is shown in Figure 128b. It can be seen that the value of the “1” is more degraded than we would expect. This is due to the structure of the array. The “1”s at the sides of the row, reduce the current to the cell in the middle. Most of the current in the cells flow to

the sense resistors and does not diffuse to the neighboring columns because the columns corresponding to the cells with “1”s contain “0”s

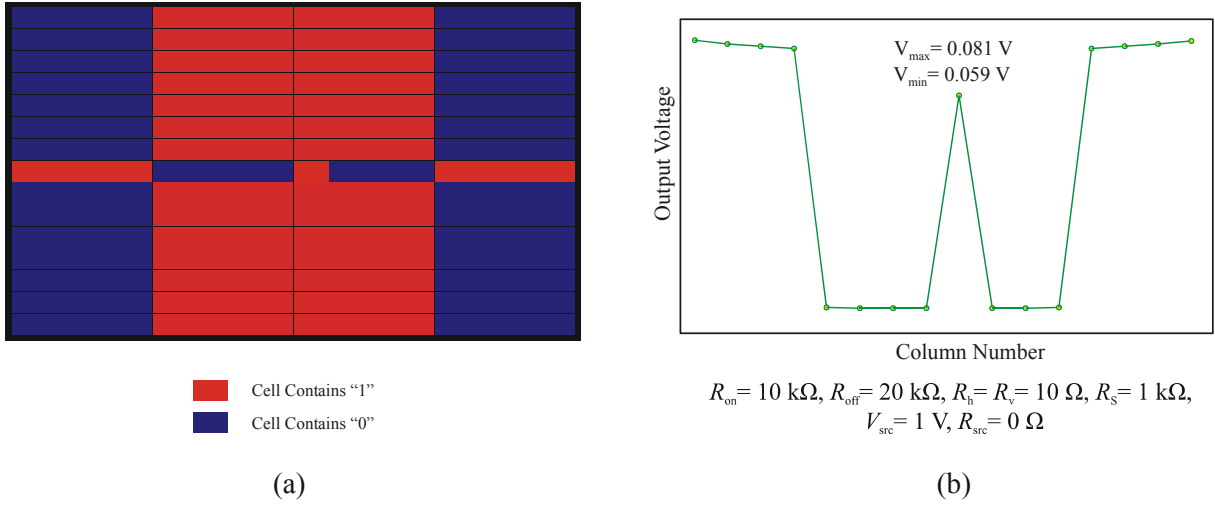


Figure 128: (a) Example of a worst case pattern for a “1”,
 (b) Simulation result of the row with the worst case

The current that flows through the worst case cell is diffused to the neighboring columns because they contain “1”s and they have a lower voltage because the neighboring cells of the worst case cell contain “0”s.

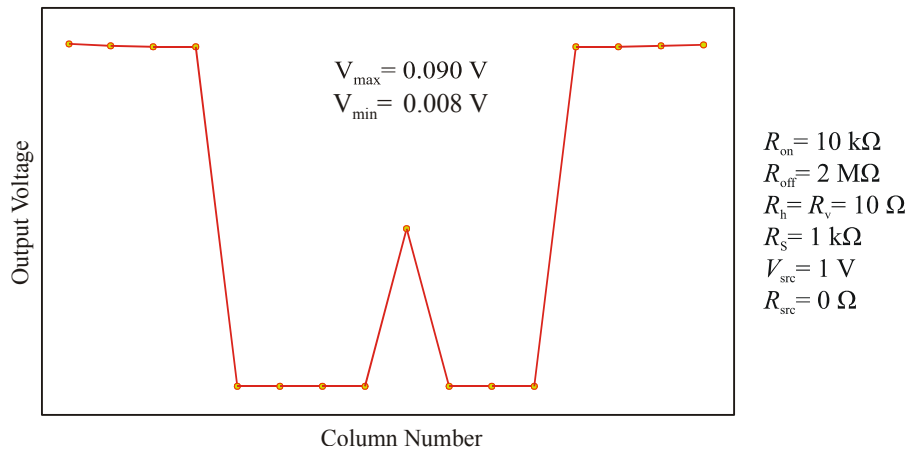


Figure 129: Simulation result of the row with the worst case using $R_{\text{off}} = 2 \text{ M}\Omega$

Increasing $R_{\text{off}}/R_{\text{on}}$ by making $R_{\text{off}} = 2 \text{ M}\Omega$ does not change the fact that the “1” in the middle is the worst case as seen in Figure 129. It shows also that the degradation is higher in this case. This means that by holding R_{S} and R_{on} constant and increasing R_{off} , the sense margin does not necessarily get higher as assumed in some literature [68]. In general the effect of the stored pattern is not discussed in literature. The worst cases are independent on any array parameters including the size of the matrix but they only depend on the pattern itself.

The relative amount of the degradation of the worst case is reduced by choosing a low value for the sense resistor as can be seen in Figure 130. This does not mean that the real amount is improved. There is a trend for the value of R_s where the amount and relative amount of the worst cases are maximized. This value of R_s is found by performing an optimization for the array size making R_s a parameter which is discussed later.

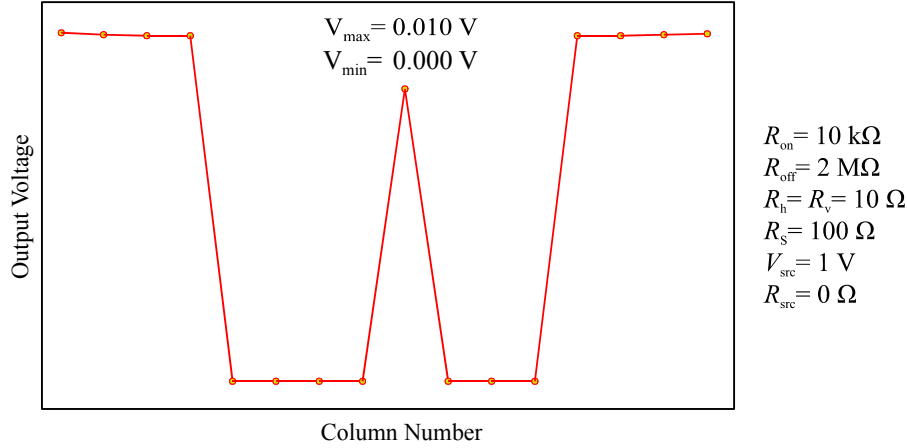


Figure 130: Simulation result of the row with the worst case using $R_{\text{off}}=2 \text{ M}\Omega$ and $R_s=100 \Omega$

Similar to the worst case for a “1”, there are patterns that produce worst cases for the “0”. A pattern that generates a worst case “0” is shown in Figure 131a. It can be seen that the value of the “0” in the middle is higher than the other “0”s (Figure 131b).

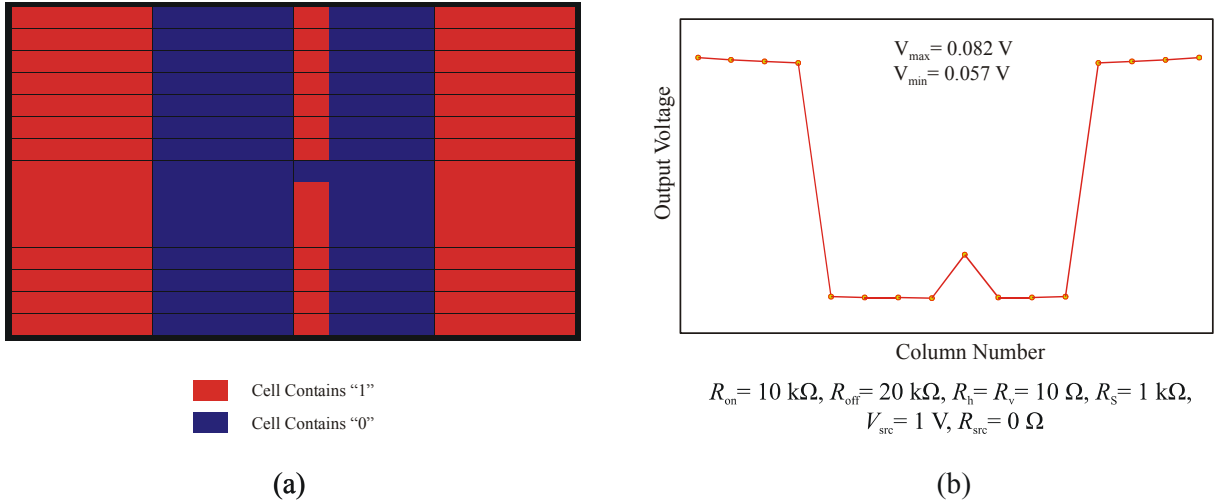


Figure 131: (a) Example of a worst case pattern for a “0”,
(b) Simulation result of the row with the worst case

By making $R_{\text{off}}=2 \text{ M}\Omega$, the value of “0” is degraded further as seen in Figure 132.

In general, the number of “1”s in a column or a row has a negative influence on the read operation. The same applies for the write operation. Thus, we need to reduce the number of “1”s as much as possible especially in the columns.

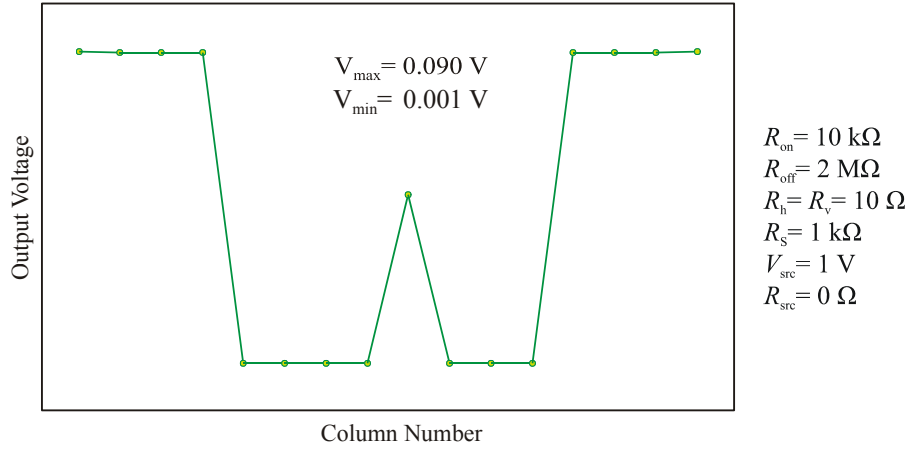


Figure 132: Simulation result of the row with the worst case using $R_{\text{off}} = 2 \text{ M}\Omega$

This procedure depends greatly on how the array is handled externally. If the array is written as a block then we have the whole information at once. By analyzing the information, we can avoid the worst cases by making some kind of transformation which reduces the number of “1”s in the rows and columns. An example for transformation would be inverting the content of the columns if the number of “1”s in the column is more than the number of “0”. This procedure requires an additional row where flags are stored to indicate whether a column is inverted or not. The transformation of the pattern in Figure 131 is shown in Figure 133.

Assuming that the array is written row wise externally, we cannot perform a transformation for the whole array because we have no information about the other rows. Instead we can transform a single row.

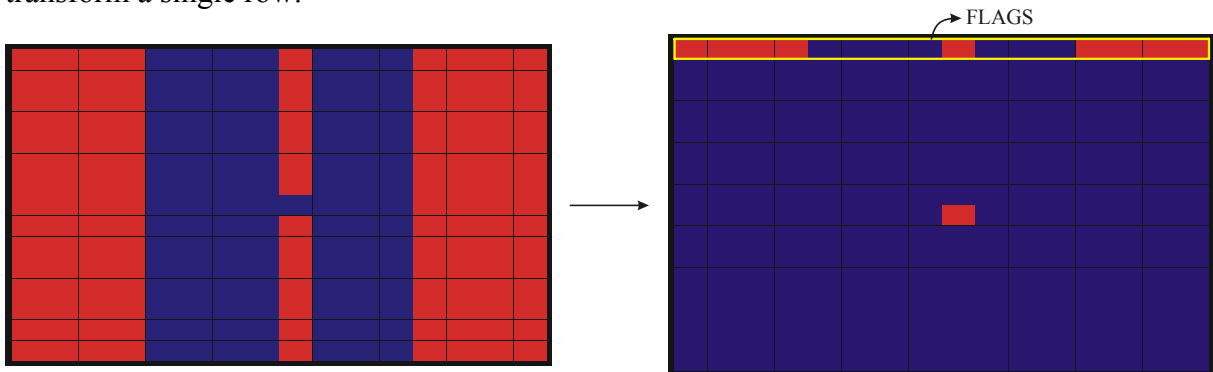


Figure 133: Pattern transformation

3.4.8.4 Array Parameter Optimization

As it was the case with writing, the optimal sizes of the arrays depend on the different parameters of the array. Most of the parameters are fixed and cannot be controlled by the designer. Some parameters, on the other hand, can be changed according to the design requirements. The size optimization procedure is very similar to that for write optimization. The difference between the two is that all worst case patterns are simulated in the read optimization whereas; only one pattern (array contains only “1”s) was simulated for the write optimization.

The most important parameter for optimizing the read operation is the value of the sense resistor. Choosing an optimal value for the sense resistor produces the largest possible arrays. This value cannot be directly calculated because it depends on the stored pattern, the interconnect resistance...etc. To find the optimal value for the sense resistor, a number of size optimization steps are performed using different values for R_s .

Figure 134 shows an optimization procedure for a constant R_{on} value and different R_{off}/R_{on} ratios. It can be seen that the optimal R_s value changes according to the ratio of R_{off}/R_{on} and it becomes steady for high ratios. It can also be seen that making the ratio higher produces larger arrays. As discussed before, using a relatively small value for R_s makes the voltage distribution more uniform but reduces the sense margin. Assuming the use of sense amplifiers with auto-zeroing technique, we can set the sense margin to few millivolts. This procedure will automatically produce larger arrays. This is shown in Figure 135, where an array with the same parameters as in the last optimization with the exception of the sense margin is simulated. The sense margin is set to 1 mV and R_{off}/R_{on} is set to 20. The optimal value for the sense resistor ($R_{s,opt}$) is found to be about 500 Ω .

Most of the violations during the optimization are due to the worst cases that are intentionally embedded in the array. A simulation is performed using the obtained optimal sense resistor value and pattern transformation to the columns. The pattern used has a random distribution with 50% “1” s population. The result of the simulation is compared to the result obtained from the last simulation at the same sense resistor value. The comparison is shown in Figure 136. It can be clearly seen that reducing the “1”s yields larger arrays which emphasizes the importance of pattern transformation.

From the previous discussion we conclude:

- 1- High values of R_s relative to the interconnect resistance are desired to reduce the degradation of the voltage levels. This also reduces the drivers' current and thus the size of the drivers. It also facilitates the design of the sense resistors because their

values would be relatively high. Very small values for R_s may be not realistic when we consider that NMOS switches are used which themselves have high on-resistance.

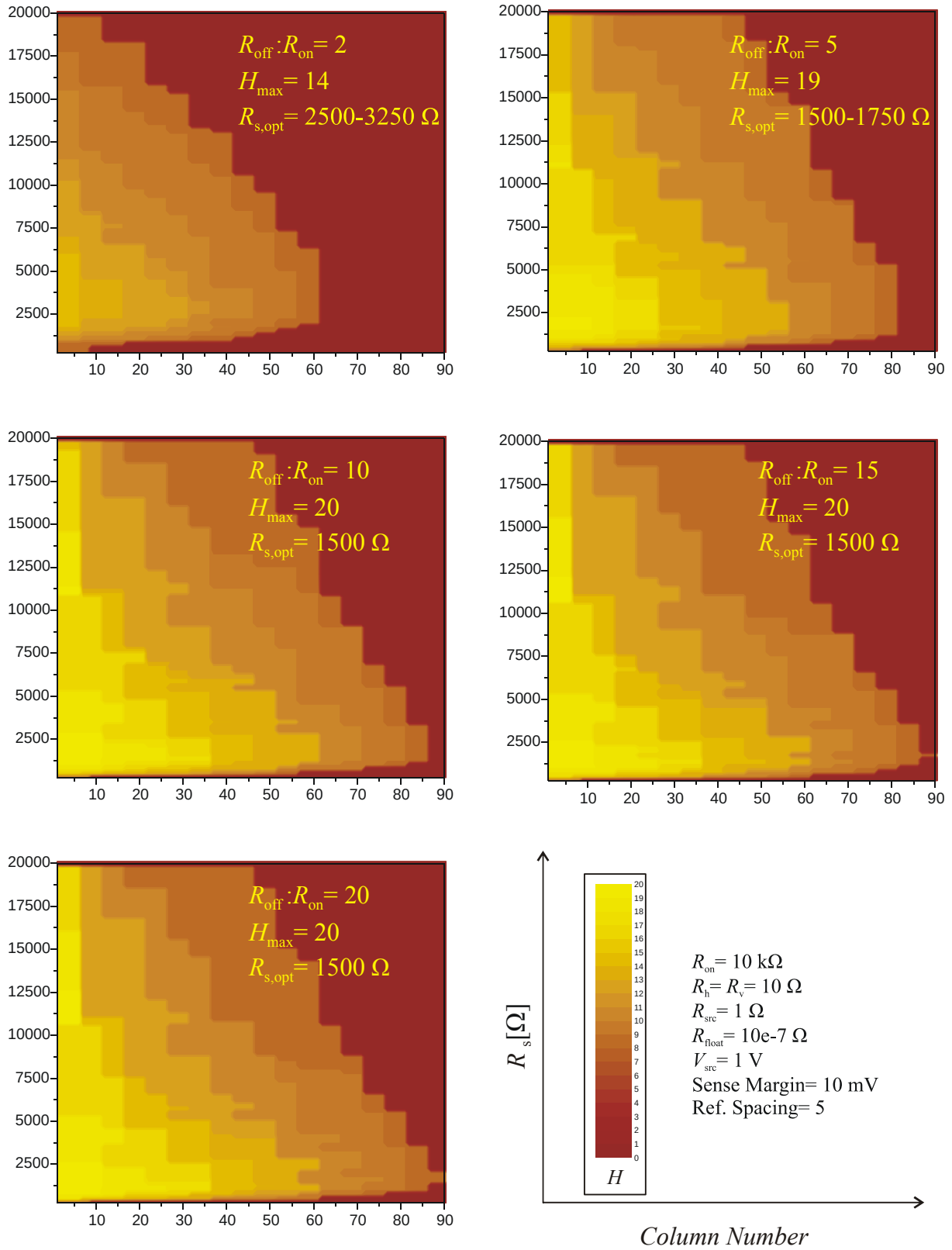


Figure 134: Calculation of R_s optimal values for different $R_{\text{off}}/R_{\text{on}}$ ratios

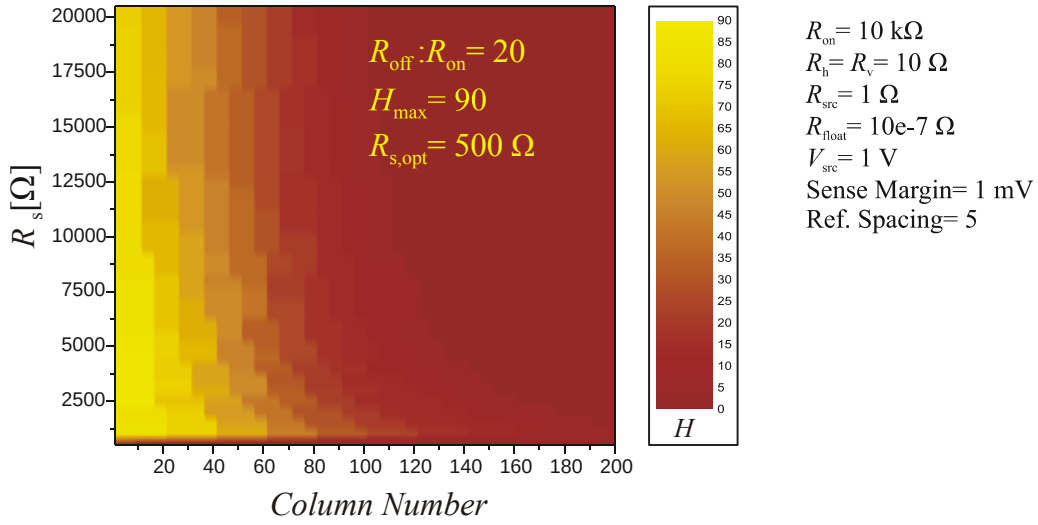


Figure 135: R_{s} optimization for $R_{\text{off}}/R_{\text{on}}=20$ and a sense margin of 1 mV

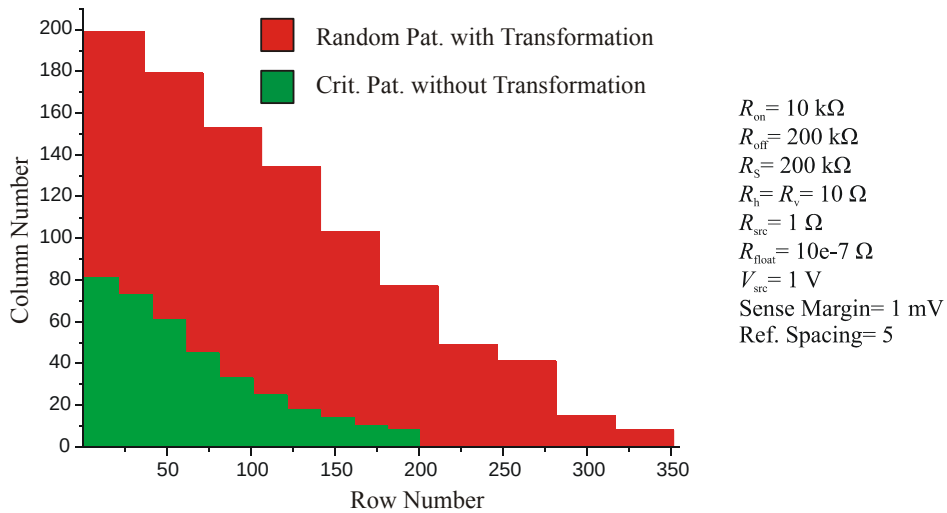


Figure 136: Comparison between random patterns with transformation and critical patterns without transformation

- 2- Reducing R_{s} and the sense margin at the same time yields larger arrays. The best case would be an R_{s} of 0 Ω and current measurement. This is not applicable in practice.
- 3- By setting a minimum sense margin, there is an optimal R_{s} that yields the largest possible arrays. This value depends mainly on R_{on} and less on the ratio $R_{\text{off}}/R_{\text{on}}$.
- 4- The size of the array is not directly proportional to $R_{\text{off}}/R_{\text{on}}$ ratio. Low $R_{\text{off}}/R_{\text{on}}$ yields a more uniform output voltage but with a reduced sense margin. On the other hand, high

$R_{\text{off}}/R_{\text{on}}$ ratios yield a higher coupling between the cells (higher noise) which means that the values of “1” and “0” are distorted.

- 5- Performing a pattern transformation to avoid worst cases where the values of the “0”s or “1” helps enlarging the arrays. Some extra bits of the memory are required for the back transformation.
- 6- The use of the novel reference voltage enables the construction of larger arrays.
- 7- The real size of the arrays is obtained by taking the intersection between the optimization results of the read and write operations.

3.5 Resistive Crossbar Arrays with Zener-Diodes

The passive arrays discussed before were pure resistive arrays. This is a major drawback for these memories because all cells were more or less coupled. The cell coupling reduced the sense margin and raised the distortion. The consequence was that the size of the fields was limited. By introducing an isolation element like a diode which can be a solid state semiconductor device or a molecular device [69], the coupling between the cells can be reduced. The I/V curves of an ideal and real diode are shown in Figure 137a and 137b respectively. The ratio of the break-down voltage to the forward-threshold voltage is very high.

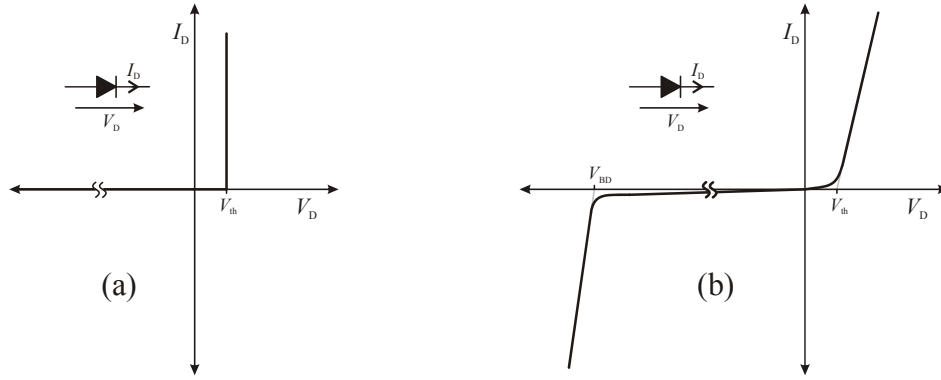


Figure 137: (a) Ideal diode I/V curve, (b) real diode I/V curve

A normal diode can be used in some memory types like the passive PCRAM [24]. In passive PCRAMs, the cell is programmed by controlling the magnitude and duration of a current pulse [20]. This means that polarity switching is not required. And the diode is used only for isolation. Other resistive memory types require polarity switching to program the cell. Having a normal diode is not sufficient to switch the polarity because a relatively high voltage would be required to perform the switching. The properties of a zener-diode are more suitable to be used in a resistive memory with polarity switching (Figure 138). Since the break-down voltage is not very high; it is simpler to control voltages for writing.

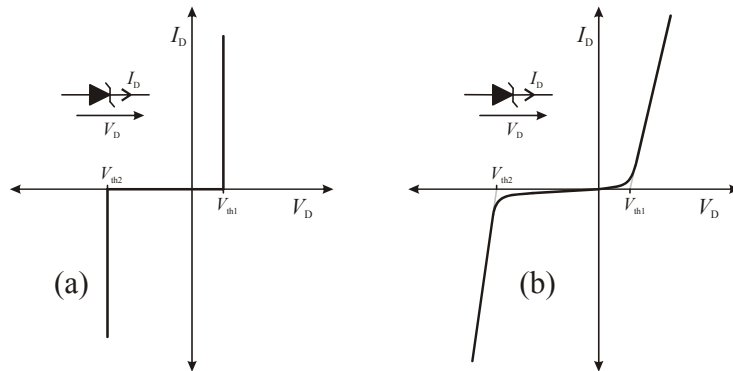


Figure 138: (a) Ideal zener-diode I/V curve, (b) real zener-diode I/V curve

The I/V curve resulting from combining the resistive hysteretic element with a zener-diode in the ideal case is shown in Figure 139. It can be seen that the switching voltages are shifted for the combined structure. In the region between $-V_{th1}$ and V_{th2} there is no voltage drop at the resistive element. The switching voltage of the hysteretic element is considered to be the one with largest magnitude of both V_{sw1} and V_{sw0} to guarantee switching in both directions and is called V_{sw} .

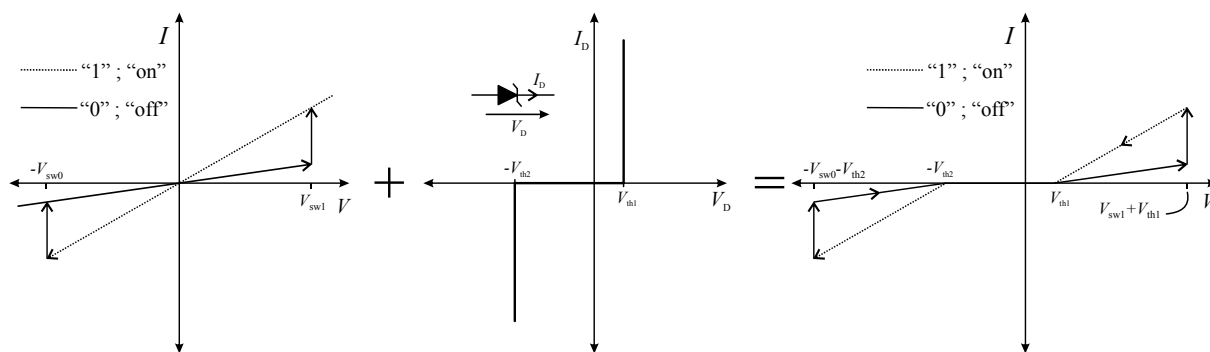


Figure 139: Serial Combination of a resistive and a zener-diode

A 3x3 array with zener-diodes is shown in Figure 140. It has the same structure as a pure resistive array. To facilitate the analysis, the components of the memory are shown in detail.

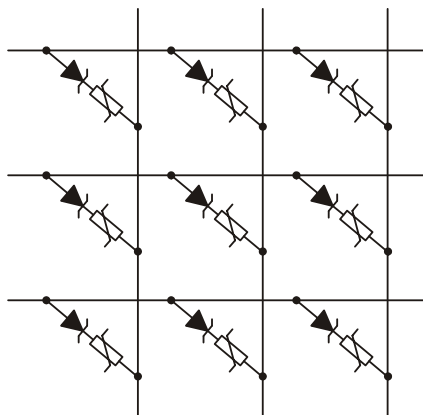


Figure 140: (a) 3x3 zener-diode passive array

The write and read operations for arrays with zener-diodes are discussed in detail in the following sections.

3.5.1 “Write” Operation Analysis

The write scheme discussed here is similar to the $V_{DD}/3$ scheme. To simplify the analysis, we consider an ideal zener-diode. The non-ideal case is simulated numerically later on. Figure 141a and 141b illustrate the write operation of a “0” and a “1” respectively.

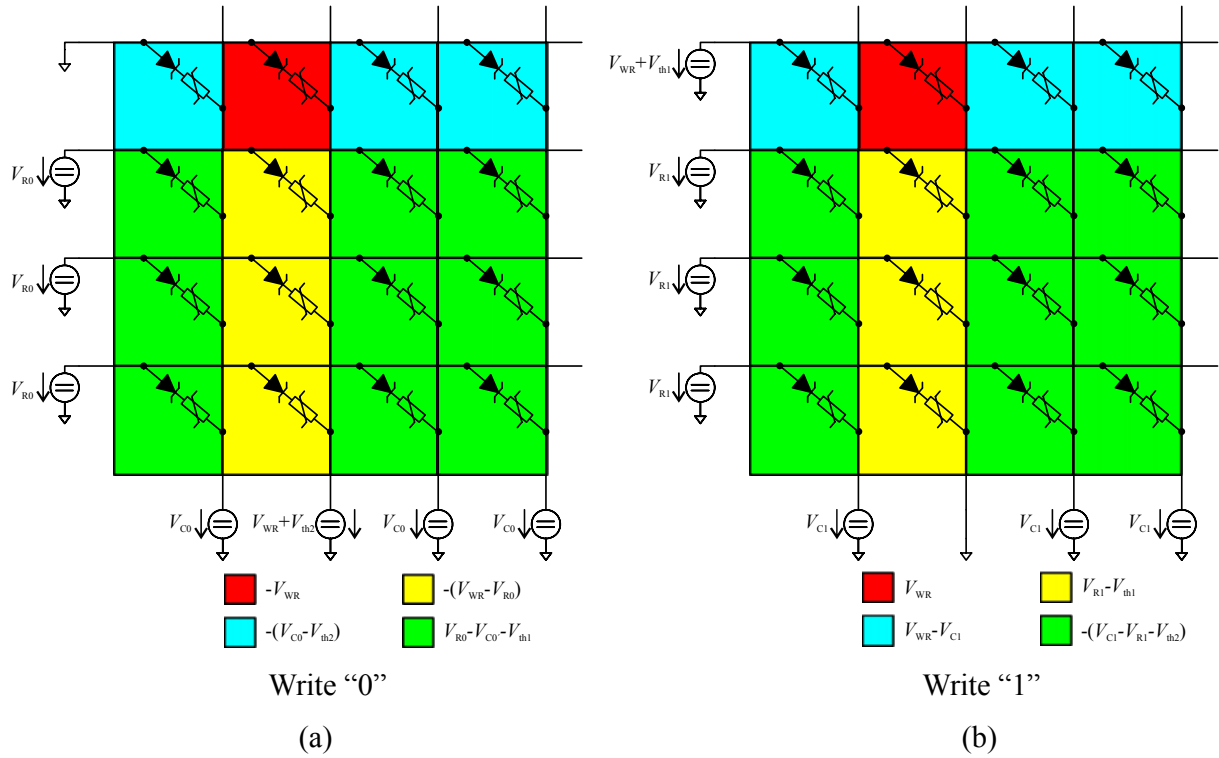


Figure 141: (a) Write “0”, (b) Write “1”

The voltages shown in Figure 141 represent the voltage drops on the resistive elements in the memory cells but not the voltage drops at the whole memory cell. The voltage drops on the idle-cells are assumed to be higher than V_{th1} and V_{th2} to produce the worst case where all the diodes conduct. If this was not the case, the whole voltage drop will be across the diodes and the resistive elements would have a 0 V voltage drop. This means that these elements are isolated.

To write a “0” into a cell or more cells, the corresponding row is grounded and a voltage of $V_{WR} + V_{th2}$ is applied to the corresponding column/columns. Non-accessed rows and columns are set to V_{R0} and V_{C0} respectively. The voltage drop across the resistive element in the accessed cell is V_{WR} regardless of the values of V_{C0} and V_{R0} . An essential condition for a successful write operation is that $V_{WR} > V_{th1} + V_{sw}$. At the same time the voltage drop at the memory cells is not allowed to exceed a predefined distortion voltage. We want to choose the voltages V_{R0} and V_{C0} , so that the magnitudes of the voltage drops across all resistive elements in the idle cells (non-accessed cells) are equal. This procedure also reduces the distortion voltage to the minimum. By setting V_{C0} and V_{R0} to the following values:

$$V_{C0} = \frac{V_{WR}}{3} - \frac{V_{th1}}{3} + \frac{2 \cdot V_{th2}}{3} \quad (25)$$

$$V_{R0} = \frac{2 \cdot V_{WR}}{3} + \frac{V_{th1}}{3} + \frac{V_{th2}}{3} \quad (26)$$

the distortion voltages on the resistive elements in the idle-cells become:

$$\frac{V_{WR}}{3} - \frac{V_{th1}}{3} - \frac{V_{th2}}{3} = |V_{C0} - V_{th2}| = |V_{WR} - V_{R0}| = |V_{R0} - V_{C0} - V_{th1}| \quad (27)$$

As can be seen the voltage drop is reduced more than it was using the $V_{DD}/3$ scheme in pure resistive memories.

Writing a “1” is very similar, but the voltages of the rows and columns are not simply exchanged as it is the case in the conventional $V_{DD}/3$ scheme, instead; the corresponding column/columns is/are grounded and a voltage of $V_{WR} + V_{th1}$ is applied to the corresponding row. The voltages V_{C1} and V_{R1} are set to:

$$V_{C1} = \frac{2 \cdot V_{WR}}{3} + \frac{V_{th1}}{3} + \frac{V_{th2}}{3} \quad (28)$$

$$V_{R1} = \frac{V_{WR}}{3} + \frac{2 \cdot V_{th1}}{3} - \frac{V_{th2}}{3} \quad (29)$$

This gives the same distortion voltage as it was in the write “0” case, which is:

$$\frac{V_{WR}}{3} - \frac{V_{th1}}{3} - \frac{V_{th2}}{3} = |V_{R1} - V_{th1}| = |V_{WR} - V_{C0}| = |V_{C1} - V_{R0} - V_{th2}| \quad (30)$$

Regardless of the used write scheme, the voltage drops across the resistive elements in the idle-cells are always reduced when diodes are used.

3.5.2 “Read” Operation analysis

As seen in Figure 142, the read operation is performed by applying a voltage V_{RD} at the row to be accessed and a biasing voltage V_{bias} at the non-accessed rows. All columns are connected to sense resistors.

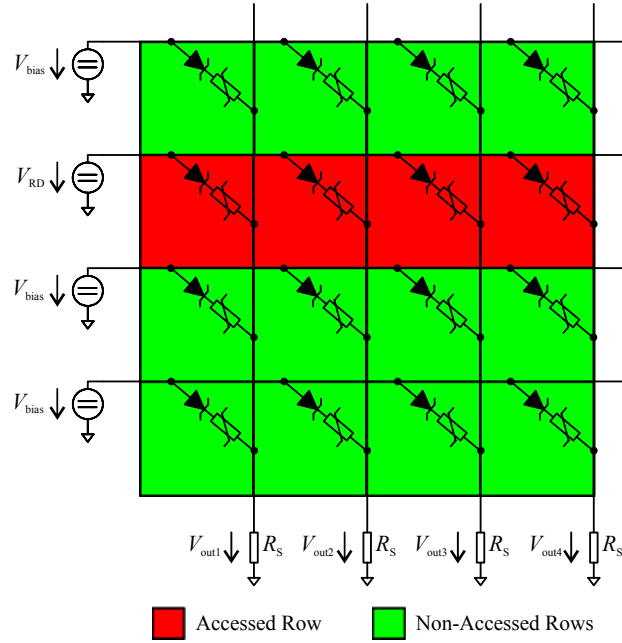


Figure 142: The read operation

To analyze the circuit we assume first that all cells in the non-accessed rows (idle rows) don't conduct. Under the previous assumption, the equivalent circuit for every cell in the accessed row is shown in Figure 143.

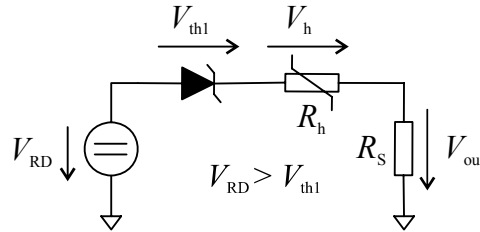


Figure 143: Equivalent circuit for the read operation

The output voltage V_{out} at the sense resistors is given by:

$$V_{out} = (V_{RD} - V_{th1}) \cdot \frac{R_S}{R_S + R_h} \quad ; \quad R_h \in \{R_{on}, R_{off}\} \quad (31)$$

And the voltage drop at the resistive elements V_h is given by:

$$V_h = (V_{RD} - V_{th1}) \cdot \frac{R_h}{R_S + R_h} \quad ; \quad R_h \in \{R_{on}, R_{off}\} \quad (32)$$

It is important that the voltage drop at the accessed resistive elements does not exceed the predefined distortion voltage during reading which means that $V_h < V_{dist}$ must always be satisfied. The worst case for the voltage drop on the resistive element occurs when $R_h = R_{off}$.

The previous assumption holds only when $-V_{th1} < V_{out} - V_{bias} < V_{th2}$ which guarantees that the zener-diodes in the idle cells are neither forward nor reverse biased. This means that V_{bias} is used to bias the diodes in the idle-cells in the non-conducting region. From the last inequality and by considering that V_{out} can have two states which are V_{out1} or V_{out0} depending on the stored information in the accessed cell, we have two conditions to be satisfied which are:

$$V_{out1} - V_{th2} < V_{bias} < V_{out1} + V_{th1} \quad (33)$$

$$V_{out0} - V_{th2} < V_{bias} < V_{out0} + V_{th1} \quad (34)$$

These conditions reduce to

$$V_{out1} - V_{th2} < V_{bias} < V_{out0} + V_{th1} \quad (35)$$

by considering that $V_{out1} > V_{out0}$. If V_{bias} is not in this range, a forward or backward biasing would exist and current would flow (leak) to the non accessed rows. It is not necessary to have an active driver for each row to apply V_{bias} ; instead we can use high ohmic resistors which are always connected to the bias voltage as seen in Figure 144. Due to their high resistance, these resistors don't disturb the drivers of the V_{RD} . At the same time the number of drivers is reduced and the row decoders and drivers are simplified.

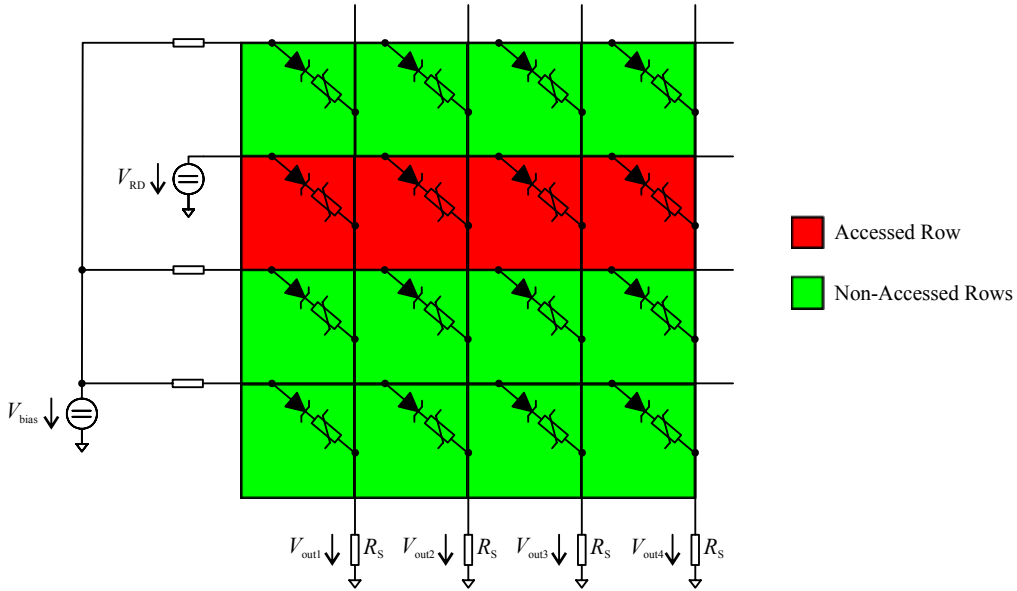


Figure 144: Replacing drivers with a single driver/ voltage source and resistors

The maximum difference between V_{out1} and V_{out0} is obtained when $R_S = \sqrt{R_{off} + R_{on}}$.

From the previous discussion we can follow the following steps to obtain the highest possible sensing margin and prevent current leakage:

- 1- An optimal value for the sense resistor is chosen using $R_s = \sqrt{R_{off} + R_{on}}$
- 2- The maximum allowed V_{RD} is determined depending on the distortion voltage. This is calculated by solving:

$$V_{RD2} = V_{dist} \cdot \frac{(R_s + R_{off})}{R_{off}} + V_{th1} \quad (36)$$

- 3- The maximum allowed V_{RD} is determined depending on V_{th2} and V_{bias} to ensure that no reverse biasing will occur. V_{RD} is calculated by solving:

$$V_{RD3} = (V_{th2} + V_{bias}) \cdot \frac{(R_s + R_{on})}{R_s} + V_{th1} \quad (37)$$

- 4- First, we consider that $V_{bias} = 0$ V. If $V_{RD2} < V_{RD3}$ then we use V_{RD2} as our read voltage to avoid exceeding the distortion limit. But if $V_{RD2} > V_{RD3}$ then we can make V_{RD3} higher by increasing V_{bias} under the consideration of the relation $V_{bias} < V_{out0} + V_{th1}$ to avoid that the diodes in the idle cells conduct.

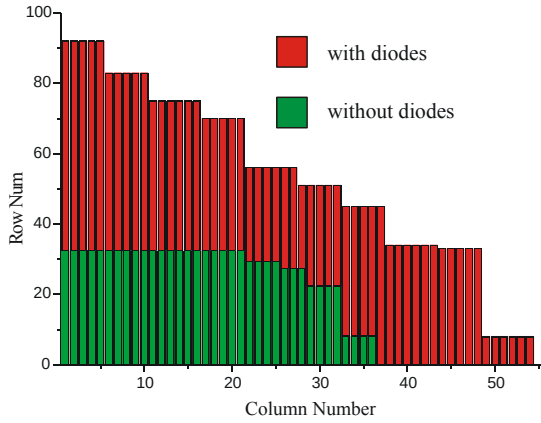
By setting $V_{bias} = 0$ V and $V_{th1} < V_{RD} < V_{th1} + V_{th2}$, it is always guaranteed that the current only flows in the accessed cells regardless of the value of R_s .

If the sense resistors have relatively high values which will not significantly influence the drivers used in the write operation, then they can be permanently connected to the columns. This procedure reduces the number of the used transistors and thus the area.

3.5.3 “Read” and “Write” Simulation

Real arrays with zener-diodes are simulated considering all parasitic elements. V_{th1} and V_{th2} are assumed to be 0.7 V and 1.3 V respectively. The optimal value for R_s was also used. The same maximum distortion voltage and minimum switching voltage were assumed as it was the case in the pure resistive arrays.

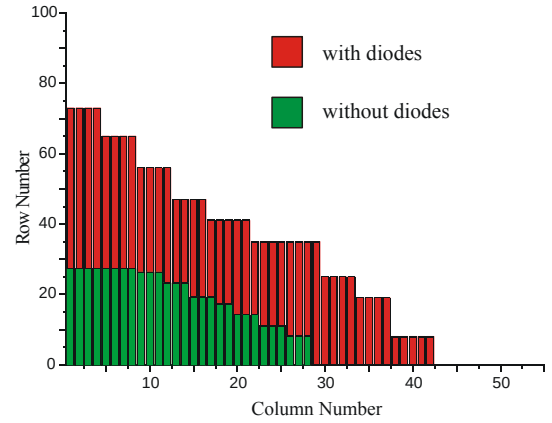
During writing, the parasitic resistance of the rows and columns degrade the voltage levels. As before, the worst case appears in the middle of the field. Figures 145a and 145b shows a simulation of a resistive array with and without diodes. The voltage scheme used is the $V_{DD}/3$ scheme. The improvement of voltage levels is apparent. The result can be further improved when the previously discussed scheme is used.



$$R_{m1} = 10 \text{ k}\Omega, R_{m0} = 20 \text{ k}\Omega, R_h = 30 \text{ }\Omega, R_v = 30 \text{ }\Omega, R_{\text{pull}} = 1 \text{ }\Omega$$

$$R_{\text{src}} = 1 \text{ }\Omega, \text{Min}_{1,r} = 0.8, \text{Max}_{\text{dist},r} = 0.4, \text{Interleave} = 5$$

(a)



$$R_{m1} = 10 \text{ k}\Omega, R_{m0} = 20 \text{ k}\Omega, R_h = 30 \text{ }\Omega, R_v = 30 \text{ }\Omega, R_{\text{pull}} = 300 \text{ }\Omega$$

$$R_{\text{src}} = 100 \text{ }\Omega, \text{Min}_{1,r} = 0.8, \text{Max}_{\text{dist},r} = 0.4, \text{Interleave} = 5$$

(b)

Figure 145: Simulation of a resistive array with and without diodes using (a) $R_{\text{src}} = 1 \text{ }\Omega$ and (b) $R_{\text{src}} = 100 \text{ }\Omega$

Figure 146 shows a read simulation performed using the same parameters used in section 3.4.8.4 in Figure 136 with the exception of the value of the sense resistor which is set to the optimal value of 44.7 k Ω . The pattern used is a random pattern with pattern transformation.

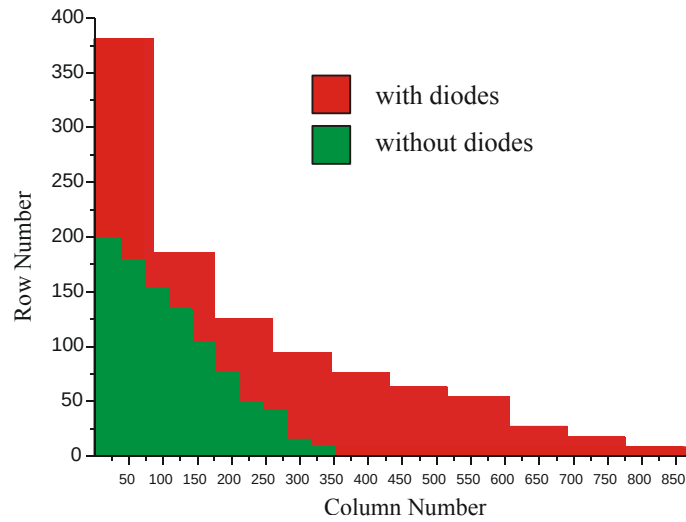


Figure 146: Comparison between two simulations with and without diodes

4 Resistive Crossbar Logic

Certain types of crossbars can be used to implement logical functions. Due to the passive nature of the crossbars, there are some functions that can not be implemented directly [70] like the inversion operation. The simplest passive logic circuits are the diode-resistor-logic (DRL). With this logic family we can implement the “AND” and the “OR” functions but no inversion can be performed. If inversion is required in the logic function, it has to be provided externally. An “AND” and “OR” gates with two inputs are shown in Figure 146.

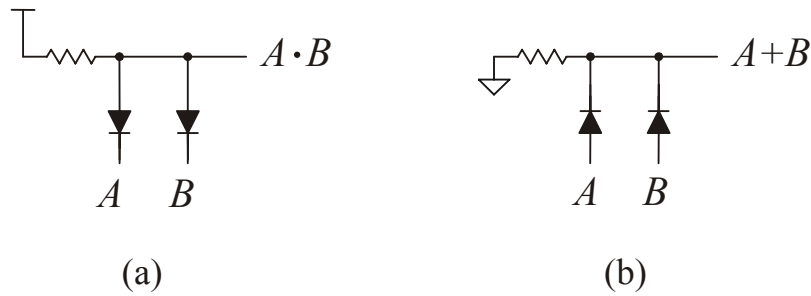


Figure 146: (a) AND gate (b) OR gate

The output of this logic family is always degraded which means that cascability is very limited. If there are many consecutive logic stages, we need to insert an active element every few stages to recover the signal level.

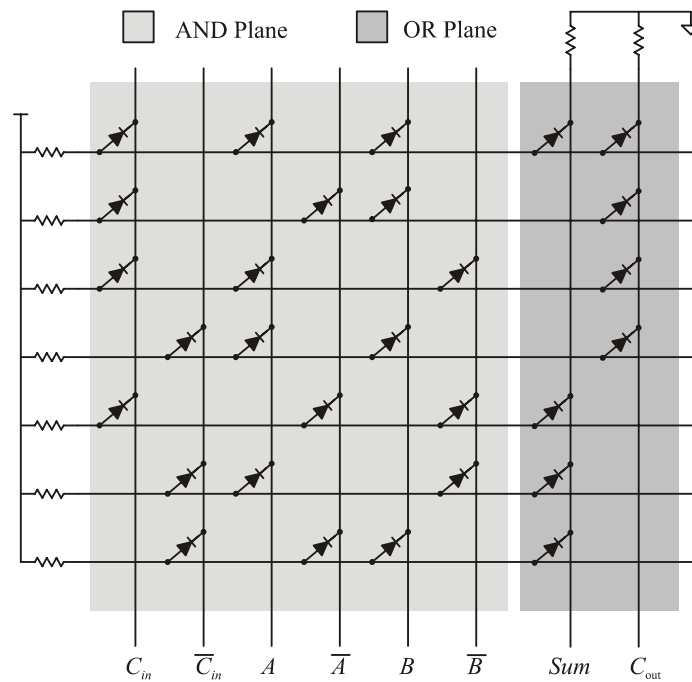


Figure 147: Full adder using a passive diode array

Logic functions can be implemented by programming a passive array which has elements with diode characteristics in the “on” state and high ohmic resistor characteristic in the “off” state. An example is shown in Figure 147 [71] where a full adder is implemented. The truth table of the adder is shown in Table 6.

C_{in}	A	B	Sum	C_{out}
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0

Table 6: Truth table of the full adder

By using a part of the array to implement the “AND” terms (min. terms) and another part for the “OR” terms (max. terms), any logical function can be implemented considering that the inversion of variables is provided externally. Again, this is a DRL which means that the outputs are degraded and have to be amplified using level shifters if consequent stages follow.

Another possibility to build logical functions is to use a memory where the truth table of the function is stored. This method is used in all modern FPGAs. There are 2^n possibilities to combine n number of variables in a logical function. The tables in FPGAs are of a small size where functions of usually three to four variables are stored. This means that the memory has 16 bits of information. The variables are considered addresses to the memory, which means that decoders are needed for the rows and columns of the memory as seen in Figure. 148

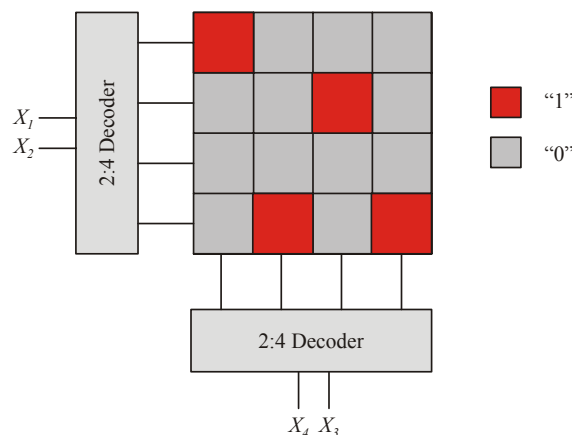


Figure 148: FPGA lookup table using resistive elements

Under certain conditions, the decoders can be simplified considerably. This is important because there is a large number of these lookup tables in an FPGA.

Decoders used for the addressing of resistive memory arrays in section 3.4.6 were complex multilevel decoders, which are not suitable to be used in FPGAs. We want to investigate the possibility of using decoders where only the addressed lines are actively pulled high or down and all other lines are floating. Figure 149 illustrates writing into one cell of 16-bit lookup table.

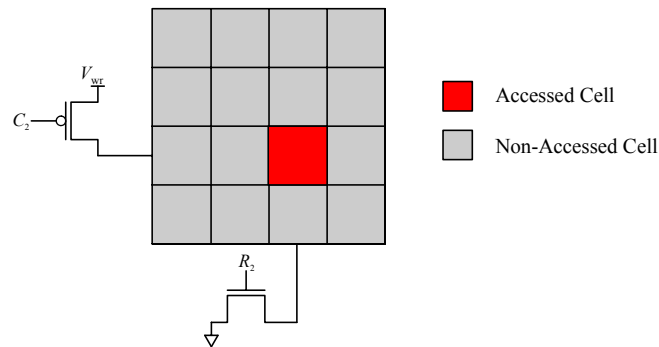


Figure 149: Write to one cell in a lookup table

Because all other address lines are floating, there are different voltage drops on the non-accessed cells. These voltages are not allowed to exceed a certain voltage which we called the distortion voltage. It is important to calculate the maximum distortion voltage in the lookup table to verify the feasibility of this method. Through simulations of different possible worst case patterns, it was found that there are certain patterns where the worst cases appear. These cases are equivalent and have a certain system which can be adopted for larger lookup tables where simulating every possible pattern would be a very time consuming job. Because of the small size of the arrays, parasitic resistances are ignored. The worst case patterns for writing the same cell as in Figure 149 are shown in Figure 150. These patterns generate the worst distortion voltage on a non-accessed cell.

As can be seen, the worst case is always at a cell containing a “0”. This is expected because the voltage drop is higher on a resistor with a high value rather than on a resistor with a low value considering the same constraints. The cell with the worst case is always in the accessed row or in the accessed column. If the cell is in the accessed row, all other cells in the column where the cell is contain “1”s and all cells in the accessed column (except the accessed cell which is irrelevant) contain “1”s. This is the case in patterns 1, 2, and 3 in Figure 150. If the cell is in the accessed column, all other cells in the row where the cell is, contain “1”s and all cells in the accessed row (ignoring the accessed cell) contain “1”s. This is the case in patterns 4, 5, and 6 in Figure 150. These patterns provide the lowest ohmic path to the cell with the worst case. By using the previous rules, worst cases for larger arrays can be found.

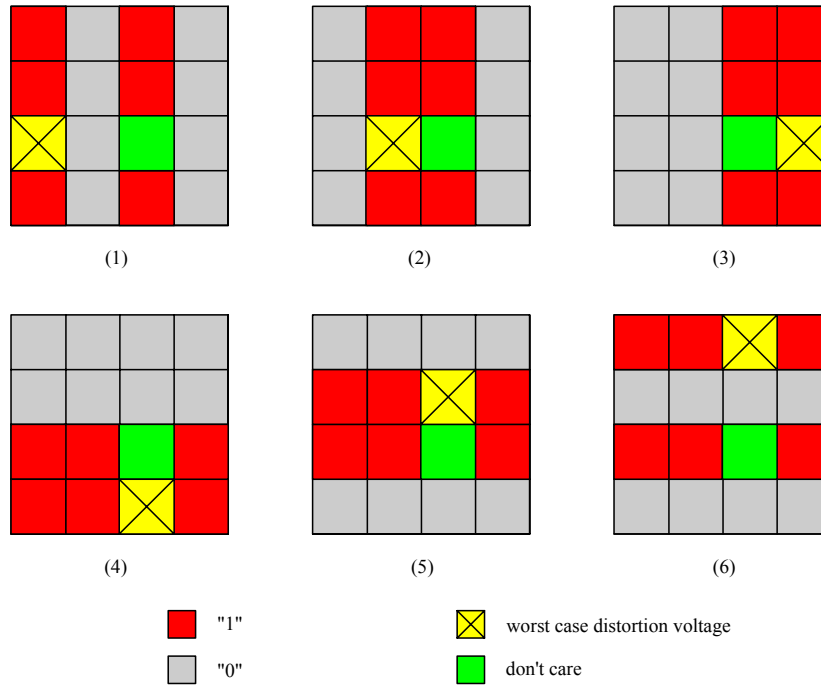


Figure 150: Worst case patterns for the write operation in Figure 149

Having the patterns with the worst case, we can calculate the voltage drop on the cell where the worst case is. If the voltage exceeds the distortion voltage, this kind of addressing can not be used. The main factor that affects the worst case voltage is the $R_{\text{off}}/R_{\text{on}}$ value. The higher this ratio is the higher is the distortion voltage. Table 7 shows the ratio $V_{\text{dist}}/V_{\text{wr}}$ for different ratios of $R_{\text{off}}/R_{\text{on}}$.

$R_{\text{off}}/R_{\text{on}}$	$V_{\text{dist}}/V_{\text{wr}}$
1.5	0.540
2	0.614
2.5	0.669
3	0.710
3.5	0.742
4	0.768

Table 7: The ratio $V_{\text{dist}}/V_{\text{wr}}$ for different ratios of $R_{\text{off}}/R_{\text{on}}$

Another issue concerning the lookup tables is the read operation and converting the signals to CMOS compatible levels. Figure 151 illustrates the read operation. The rows are driven from the same decoder that was used for writing. The columns are connected to the sense resistors via pass transistors. Only one of the sensed voltages is selected according to the address X_4X_3 . The sensed voltage is then compared to a reference voltage using a comparator. After that, the output of the comparator is buffered using an inverter.

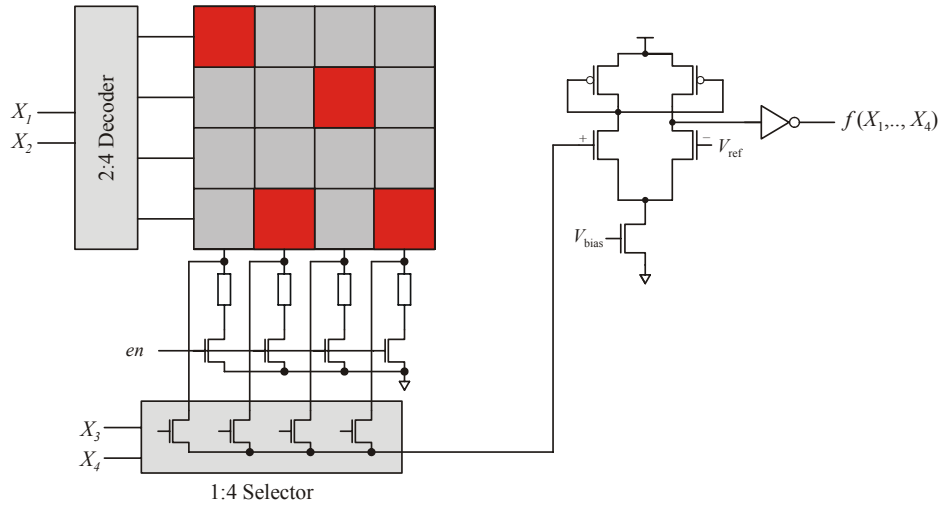


Figure 151: The read operation

A simulation of a full adder is performed using this concept. Two lookup tables are required to generate the output signals Sum and C_{out} from the input signals A , B , and C_{in} . The input signals of the decoders are set to: $X_1 = A$, $X_2 = B$, $X_3 = C_{in}$, and $X_4 = GND$. The simulation results are shown in Figure 152 and the contents of the lookup tables are shown in Figure 153.

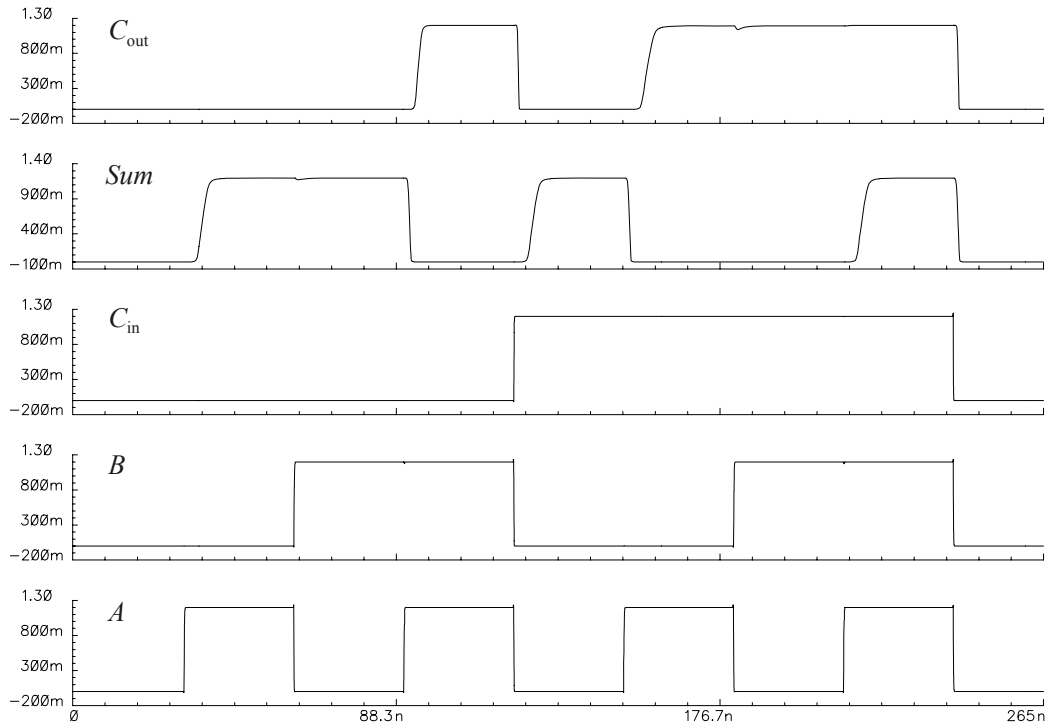


Figure 152: Simulation of a full adder using passive resistive LUTs

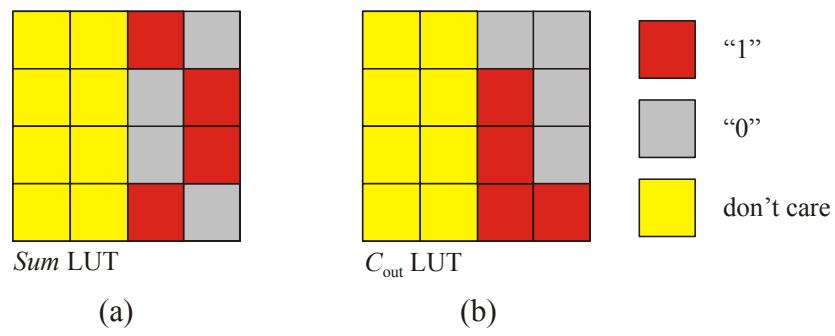


Figure 153: Lookup tables for (a) *Sum* and (b) C_{out}

5. Conclusions

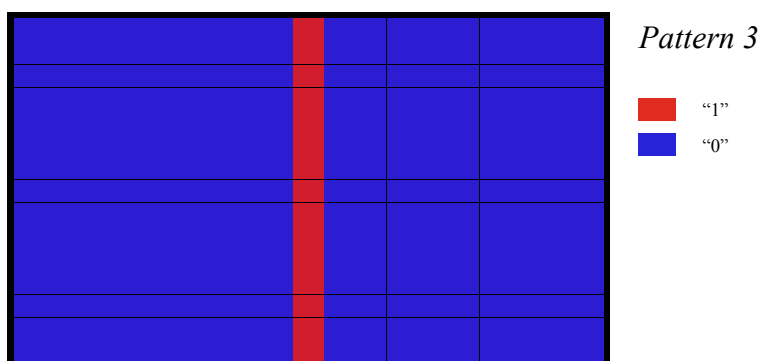
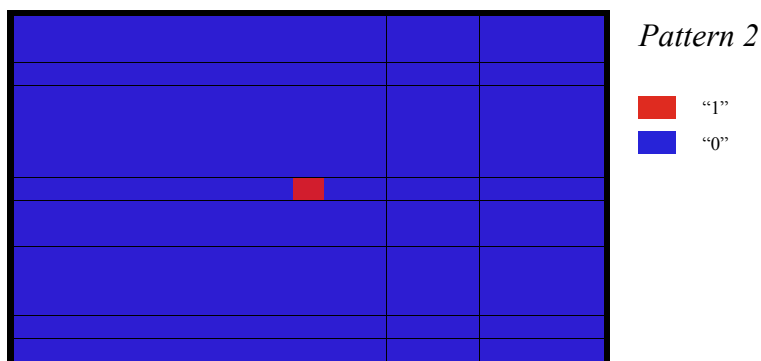
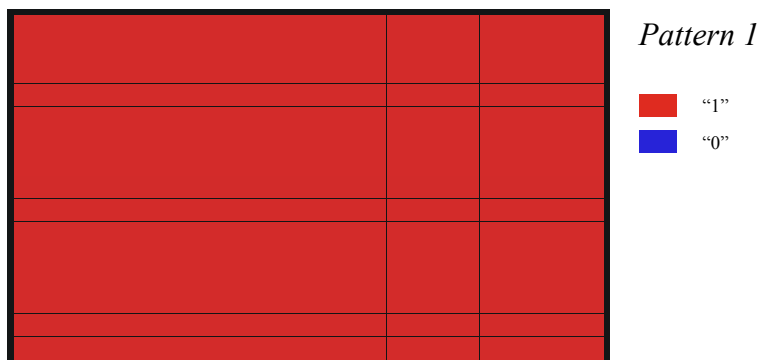
1. An empirical model has been developed to describe the behavior of the resistive hysteretic elements.
2. Different active memory architectures have been analyzed, simulated, and compared to find the most suitable architecture to be used for future active resistive memories. It has been found that the AND architecture is the architecture of choice for resistive memories.
3. A novel capacitive-resistive cell has been developed. The cell can be used with a fixed or a driven plateline. In the fixed plateline configuration, the voltage polarity across the resistive element is changed via the capacitor. In the driven plateline configuration the voltage drop across the resistive element can be raised higher than the supply voltage. A new read method, which depends on the time constant of the cell and bitline has been proposed and simulated.
4. Periphery circuits for the write and read operations in passive resistive memories have been elaborated. The periphery circuits for the write operation generate multilevel voltages which are required to write the information correctly and to reduce the distortion voltage on non-accessed cells.
5. Passive resistive memory arrays have been discussed thoroughly. The read and write operations of the memories have been analyzed and simulated. It has been shown that some ideas about passive resistive arrays have been misleading. An example is the determination of the optimal value of the sense resistor and that $R_{\text{off}}/R_{\text{on}}$ is the most important factor to achieve higher capacities. Software was developed to find the optimal size of the arrays for the write and read operations and to find the optimal sense resistor value that produces the largest reliable arrays.
6. A novel reference voltage scheme has been developed. The scheme utilizes the locality principle to generate the reference voltage, where dedicated reference cells in the memory rows are used to generate different reference voltages for the memory cells in the same row. Because of the high correlation between the reference cells and the neighboring cells in a row, more accurate reference voltages are obtained. The use of this scheme enhances the size of the resistive array. This scheme can be used with any type of passive memories.
7. Critical patterns that produce worst cases during reading have been elaborated. It has been shown that these worst cases can be avoided if a pattern transformation is applied

to the data before writing it. The data is transformed back upon reading using flags that are stored with the data. Because pattern transformation avoids the worst cases, larger arrays can be constructed. This concept is valid for all types of resistive memories.

8. The use of zener-diodes in combination with the resistive element has been discussed. The read and write operations have been analyzed and simulated. It has been shown that using diodes improve the voltage levels and reduce the distortion voltages which allow larger arrays to be constructed.
9. The usage of passive resistive elements in FPGAs has been examined. It has been shown that under certain circumstances, the write operation can be simplified considerably where only one row and one column are activated during writing and all other lines are left floating. A rule has been found to determine the critical patterns for writing for an arbitrary lookup table size. A test circuit that generates a logical function of a full adder has been constructed and simulated.

Appendix A: Read Test Patterns

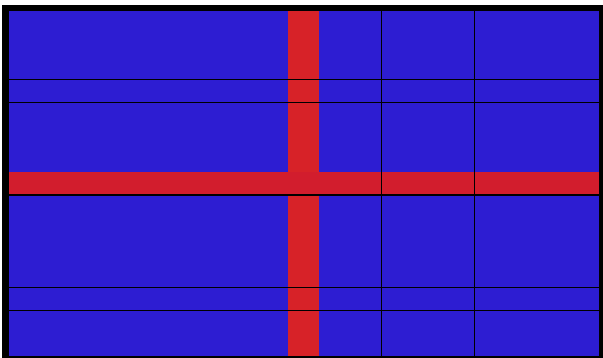
There are certain patterns that produce read operation worst cases for both “1”s and “0”s. The width and height of the patterns can be changed freely but the relative form of the pattern must be maintained. In the following, the most important patterns are illustrated:





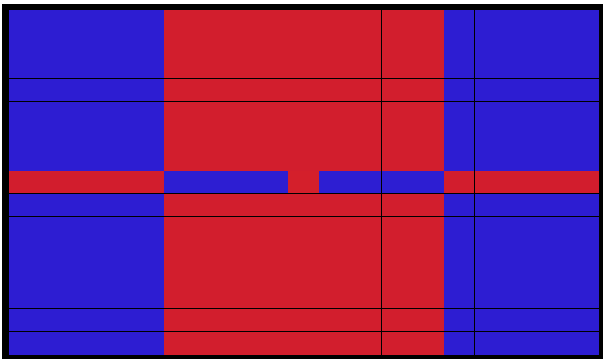
Pattern 4

“1”
“0”



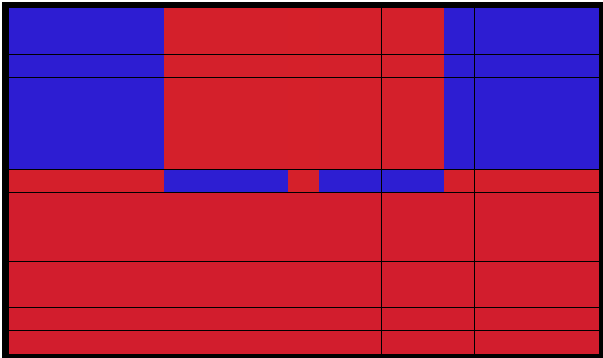
Pattern 5

“1”
“0”



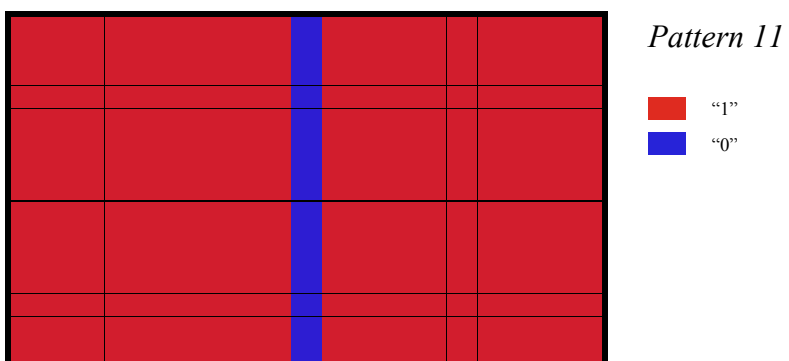
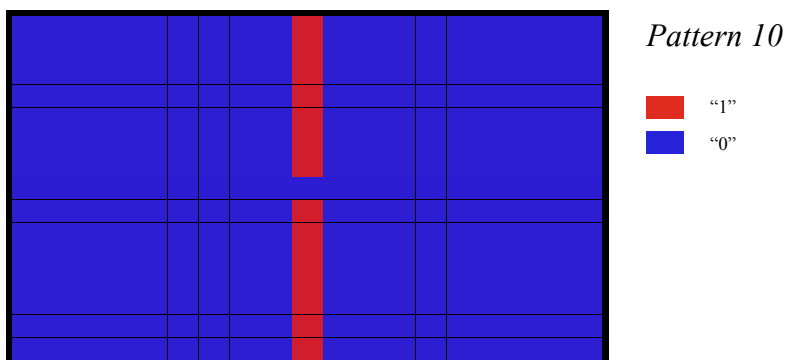
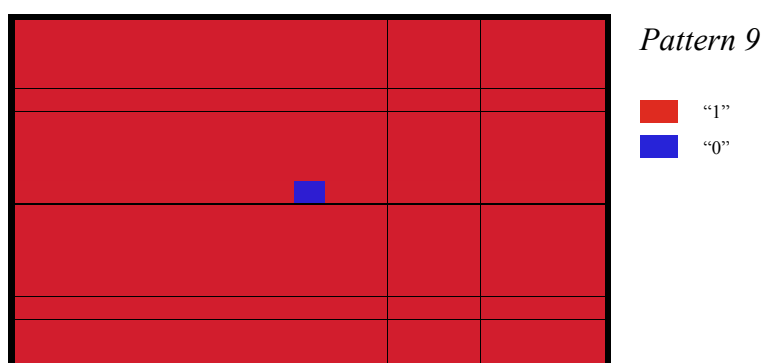
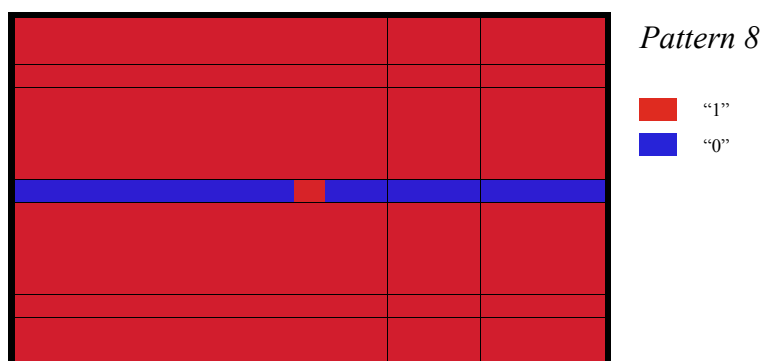
Pattern 6

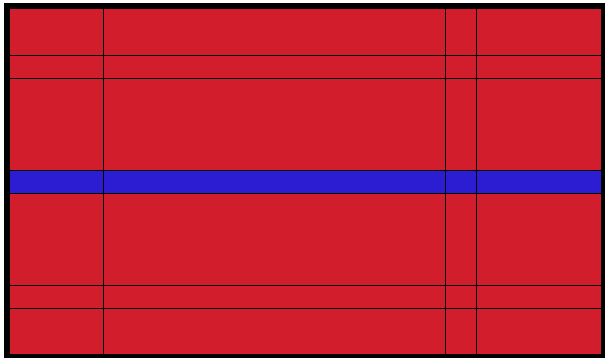
“1”
“0”



Pattern 7

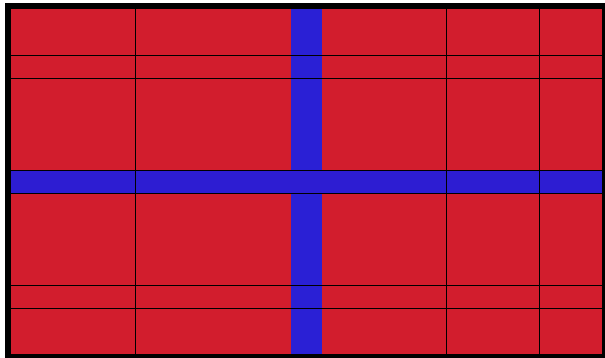
“1”
“0”





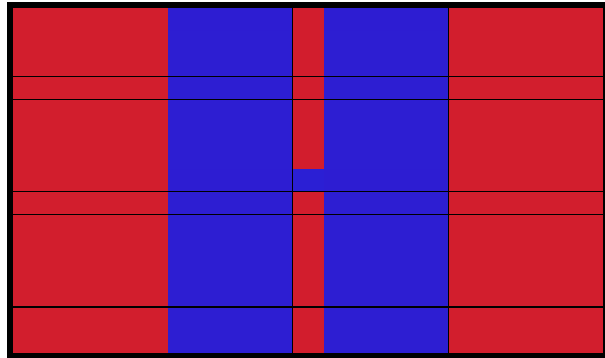
Pattern 12

“1”
“0”



Pattern 13

“1”
“0”



Pattern 14

“1”
“0”

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