A Low Cost PMU to Monitor Distribution Grids

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Abstract—Phasor Measurement Units have become more and more interesting for monitoring applications in distribution grids. For a large exploitation in medium and low voltage networks, however, a limited cost is required. Such specification, however, should not impact excessively the accuracy requirements, as it is expected that automatic control functionalities will run based on state estimation algorithms, which can be fed by PMU information. In this paper the design of a low cost PMU for distribution grids is proposed, and tested versus the IEEE c37.118.1-2011 standard for accuracy. The development of the low cost PMU is part of the Modular Intelligent Node (MIND) project, where distribution grid components and functionalities are implemented as modular interconnected nodes that run on general purpose hardware.

I. INTRODUCTION

Distribution systems are undergoing drastic changes. Renewable resources are installed at constant or growing rates, together with controllable storage and load units. Such components may be grouped under the name of Distributed Energy Resources (DERs), indicating units that can be monitored and controlled in real time to improve the efficiency of the grid and guarantee proper Power Quality (PQ) indexes. Such functionality requires advanced monitoring devices to serve state estimation algorithm. In last years, increasing interest gathered around the application of Phasor Measurement Units (PMUs) to distribution systems [1], [2], [3]. Among the main difficulties it should be considered the large cost, today associated to PMU units. To have full observability, it is necessary to install PMUs in a large number of primary and secondary substations, but with the current average cost, this will require a huge investement for Distribution System Operators (DSOs) [4]. Measurement infrastructure with sparse PMUs can be anyhow helpful for gathering better state estimation results and being able to compare the states of geographically deconnected grids. The PMU will be exploited mainly for steady state monitoring, therefore the specifications on the update rate may be also relaxed, for instance, up to 10 phasors per second or 1 phasor per second. In the EU fp7 project IDE4L, where state estimation was tested on three European distribution system operators, state estimation was updated every 1 minute [6]. This will also help to relax the communication infrastructure requirements to carry synchrophasor measurements. In this paper a LOw COst (LOCO) PMU solution is proposed. The LOCO PMU is located inside the MIND project proposed in [5]. The MIND project considers to build modular software components for automation of power system, that can be installed on heterogeneous hardware components and in particular, in low cost computation units

like Raspberry Pi or BeagleBone Black. In this way automation functionalities can be easily expanded and integrated exploiting common standard interfaces like IEC 61850. In this framework, the MIND projects also aims at developing low cost monitoring units, like PMUs and Smart Meters, as well as automatic controllers and aggregators. The LOCO PMU has to measure synchrophasors, frequency and Rate Of Change Of Frequency (ROCOF) with accuracy as close as possible to the requirements of the standards, but maintaining acceptable initial costs, in order to be massively installed for applications in distribution systems. Therefore, the effort is on the selection of adequate hardware and on "not demanding", but at the same time accurate, phasor computation algorithms, in order to be able to run on unexpensive computation units. Hardware components are needed for analog to digital conversion, phasor processing, communication and GPS time reference handling. Software components are required to manage the digital samples to calculate synchrophasors and encapsulate the information into IEC 61850 data protocol. Also, encryption and authentication functionalities are assigned in order to guarantee cyber-security features. In section II the full description of hardware and software components of the LOCO PMU is given. In section III the mathematical calculations to obtain the output of the PMU are presented. In section IV preliminary infomation on the testing procedures for the evaluation of the measurement uncertainty are given. Finally, in section IV the test results of the IEEE c37.118.1-2011 and c37.118.1a-2014 standards are presented.

II. PMU PROJECT AND COMPONENTS

The requirements for the low cost PMU are to provide synchrophasors, frequency and ROCOF with an accuracy and maximum delay as specified in the IEEE Std C37.118.1-2011, consequently updated in the C37.118.1a-2014. The requirements are that the amplitude of the maximum vector between the actual and the measured phasors, named TVE, and the maximum Frequency Error (FE) and the ROCOF Error (RFE), are smaller than a given threshold under specified testing conditions, as further detailed in section V. Such testing conditions, which are different for static and dynamic testing scenarios, include magnitude, frequency, phase angle and harmonic content variations. The testing condition proposed by the standard are designed around the current main application, that is wide area monitoring of transmission grids. However, PMU in distribution grids are probably going to be used for a totally different range of applications, that are mainly related to steady state monitoring via state estimation and fault detection. Furthermore, the information has to be collected from a large number of nodes, making reasonable to reduce the reporting rate to 1-10 frame per second. In this way the communication infrastructure, as well as the computation resources of the Phasor Data Concentrators (PDCs) are released from severe stress. Given these assumptions, the LOCO PMU was developped for reporting rates of 1 Hz, the IEEE standard requires to satisfy only the steady state testing procedure. The results of steady state tests are presented in section IV. In literature some low cost PMU, to be applied in distribution grids, are shown. In [2] an opensource software based PMU, which can run on diverse hardware platform, is described. In [7] a Digital Signal Processor (DSP) based low cost PMU is proposed and presented Total Vector Errors (TVEs) up to 0.57%. In [8] a PMU based on RPI, an external ADC hardware and non-DFT algorithm is shown, but the accuracy values are not presented. In [3] an architecture designed to pass test performances for M and P class is presented. In [9] an enhanced Interpolated-DFT FPGA based PMU is also described. The latter two approaches present high accuracy but also high computation requirements; this brings difficulties into expanding such approaches to low cost hardware units. The PMU developed in this paper is composed by three components.

- 1) A data acquisition board: namely the MCC USB 201, further presented in section II-A, which convert a voltage signal in the range \pm 10V to digital sampled values.In the current project, the LOCO PMU, does not include sensors and transducers, therefore their contribution is not considered in the evaluation of the uncertainty.
- 2) A measurement computation unit: namelly the Raspberry PI (RPI) 3. The communication libraries libiec61850 to send and receive data messages in Sampled Values format, according to the standard IEC 61850-90-5 were installed. Then the code to acquire the samples and calculate the synchrophasor, frequency and ROCOF was added on top.
- 3) A GPS module: connected to a GPS antenna, providing the Pulse Per Second (PPS) signal to the MCC USB 201 and the digital time information, in terms of Coordinated Universal Time (UTC) via Universal Asynchronous Receiver/Transmitter (UART) communication to the Raspberry PI 3. The GPS module is based on a MTK3339 chip which provides PPS errors less than 10 ns.

Considering an average cost of the RPI 3, the data acquisition board and the GPS module and antenna of, respectively, 35, 100, 60 euros and the cost of the remaining hardware such as SD card, power supply, box for substation environment and cables of about 50 euros. The total hardware cost is approximately 250 euros.

A. Analog to Digital Converter

The Analog to Digital Converter (ADC) MCC USB 201 includes eight 12 bit analog inputs in the range \pm 10V, with sampling rate up to 12.5 $\frac{kS}{s}$ per channel. The maximum sampling rate available is $100 \frac{kS}{s}$, but it has to be shared among the 8 available channels via a multiplexer. The datasheet specifies different contributions of the uncertainty, specified

as maximum errors. In particular, the gain error is 0.098 % of reading, the offset error is 11 mV, the error at full scale is 20.8 mV. The MCC USB 201 can be configured, with some open source C libraries, in order to acquire data when an external trigger signal is received. If the trigger signal is the PPS, it is possible to refer the calculated phasor to an absolute phase angle. However, a delay between the PPS impulse and the activation of the acquisition translates into a phase angle error. The datasheet specifies that the trigger latency is equal to 1 μ s plus a time between zero and 1 clock cycle, which lasts 10 μ s. 1 μ s can be always compensated as systematic error, whereas the further contribution, which may bring a maximum error equal to 0.3 crad, cannot be systematically evaluated.

B. Data models and protocols

The RPI runs the operative system Raspbian, which can operate the open souce libraries libiec6850, in order to send the measurements in the Sampled Value (SV) format, as recommended by the IEC 61850-90-5 standard for PMUs. The SV publisher is configured by means of the Substation Configuration Language (SCL) file, where the measurement data are mapped onto 61850 data models, which account of physical device, logical device, logical nodes, data object and data attributes. In order to be able to send PMU into Wide Area Networks (WANs), SV meassages are also encapsulated into UDP-IP packets.

III. SYNCHROPHASOR, FREQUENCY AND ROCOF ALGORITHMS

A. Frequency and ROCOF calculation algorithm

For the frequency calculation a zero-crossing detection algorithm was implemented in order to determine the period of the acquired signal and thus the frequency. Before running such algorithm, however, a low-pass filter is applied to the acquired signal in order to reduce the impact of noise and harmonics. The digital filter is a 3^{rd} order butterworth filter, with cut frequency equal to 70 Hz. Given, the relatively low order of the filter, chosen in order to maintain a small number of numerical calculation to be done in real time, the filter does affect the mangitude and phase angle of the first harmonic. Therefore, once the frequency and the ROCOF are calculated the filtered signal is discarded, whereas the original signal is again considered for the synchrophasor calculation in equation (3). Once the signal has been filtered the zerocrossing detection takes place. The acquired signal is scanned sample by sample looking for changes in sign, from positive to negative, identifying negative zero-crossing events. When the first occurrence of such event is detected we calculate the time at which it occurred, by interpolating the two samples, and store such value in a variable named Xpn₁. After the first zerocrossing detection we continue scanning the acquired signal vector looking for the next negative zero-crossing event. In order to avoid false events detections, due to, for example, measurement errors or noise, we set a minimum distance expected between two zero-crossing events of 12 ms. Once a new zero-crossing event is detected we calculate again the time at which it occurred by interpolating the two samples and store this value in a variable called Xpn_2 . Hence, the period of the acquired cycle (Tc_i) is calculated as the difference between Xpn_2 and Xpn_1 . Every time a new period is identified we store the calculated value in a result vector, increment the number of identified cycles counter (Nc) and overwrite Xpn_1 with the value stored in Xpn_2 . Once the whole acquired signal vector has been scanned we calculate the average frequency of the signal as the inverse of the mean period (1).

$$f = \frac{1}{Nc} \sum_{i=1}^{Nc} \frac{1}{Tc_i}$$
 (1)

The ROCOF is calculated as difference between the inverse of the period at the beginning and the end of the observation window (2).

$$ROCOF = \frac{1}{Tc_1} - \frac{1}{Tc_{Nc}} \tag{2}$$

Such approach permits to maintain a good frequency and ROCOF estimation in presence of noise and high harmonics in comparison to the approaches where frequency is based on the derivative of the phase angle measurement [10].

B. Phasor Calculation Algorithm

Digital samples are multiplied by a window function in order to improve the frequency spectrum of the signal. This improves the estimation of the phasor when the actual frequency is different from the nominal one. For the LOCO PMU, the flat top window function was selected, for its very flat frequency spectrum. The DFT and the multiplication to the flat top window is applied, as presented in equation (3).

$$X_k = \sum_{n=0}^{N-1} x_n \cdot FT[n] \cdot e^{-i \ 2\pi \ k \ nN}$$
 (3)

The calculated phase angle refers to the center of the observation window; from here, based on the measured frequency and the time duration of the observation window, the phase angle for a time tag corresponding to the start of the observation window is calculated.

C. Choice of measurement window

In order to maintain real time operation, it is required that in a total time equal or less than 1 second, the digital samples are extracted and processed in order to obtain synchrophasor, frequency and ROCOF, then the SVs are published. Therefore, the total duration of the observation window is slightly shorter than 1 second. It was evaluated that a conservative and proper duration, considering that the PMU can process up to 8 channels every second, was to observe a total of 44 cycles, which at nominal frequency of 50 Hz means a time window of 880 ms. The flat top window will have a 3 dB main lobe width of approximately 3.34 Hz. This mean that actual frequencies far apart from the nominal frequency will rapidly bring degradations of the estimated phasor. Therefore, in case the measured frequency exceed the range 50 Hz \pm 0.2 Hz,

only 6 cycles, that correspond to a 120 ms time windows, are considered. In this way the 3 dB main lobe width becomes approximately 24.5 Hz. Such feature permits to respect the accuracy requirements on TVE for large frequency variations, as detailed in section V.

D. Initialization and Operation

In order to better clarify the real time operation of the LOCO PMU, the diagram in Fig.1 specifies the real time operation schedule. When the LOCO PMU is started, it reads the configuration file for the acquisition, which includes the information on: which channels are to be considered; the sampling frequency (normally set to 10 kHz) the duration of the observation window (set as default to 880 ms); the SCL files to be read in order to find the communication protocols and data model definition and other minor parameters, are loaded. Subsequently, the RPI launches the acquisition with the request to wait for an external trigger, that is the PPS signal. When the PPS signal is received, the samples are acquired with a frequency of e.g. 10 kHz for a total duration of e.g. 880 ms and sent via USB to the RPI. At first, the samples are processed by a low pass filter, in order to remove high harmonics and noise content, which, otherwise, would deteriorate the performance of the zero crossing algorithm. The zero crossing algorithm is applied to obtain the time duration of the cycles. Based on such knowledge, frequency and ROCOF are calculated as explained in section III-A. If the measured frequency is near to the nominal one, all the samples are considered to calculate the synchrophasor. Otherwise, a reduced amount of samples are considered, considering the filtering behaviour of the window. The DFT is applied on the non-filtered signal samples multiplied by the flat top windows. The resulting phase angle is compensated considering the actual measured frequency in order to time tag the synchrophasor at the occurrence of the UTC second. Eventually the synchrophasors, frequency, ROCOF and time tag information are mapped into IEC 61850 data model and published trough SV and UDP-IP protocols.

IV. PRELIMINARY INFORMATION ON TESTS FOR COMPLIANCE WITH IEEE STD C37.118.1-2011

A. Review of standard requirements

The proposed PMU is tested for the steady state conditions of the class M of the IEEE Std C37.118.1-2011 and C37.118.1a-2014 standard. The section 5.5.4 of the 2011 standard specifies that measurements at reporting rates (Fs) lower than 10/s shall only be subject to steady-state requirements. In addition, such measurements are not subject to out of band rejection tests. However, the authors are aware that the standard, in section 5.4.1, requires the PMUs to provide, for 50 Hz systems, also reporting rates equal to 10/s, 25/s and 50/s. The tests are performed over durations of 6 seconds and the values presented are the maximum of TVE, Frequency Error (FE) and ROCOF Error (RFE) values. The test procedures are based on the standard IEEE Std C37.242-2013 for the procedures to assess steady-state compliance of a PMU.

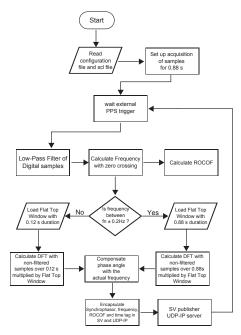


Fig. 1. flowchart of LOCO PMU real time operation

B. Test equipment

In this paper, the authors applied laboratory instrumentation, referring to manufacturer's datasheets and calibration certificates to determine their metrological perfomance. In particular, the signal generator are modelled in the software environment of the Real Time Digital Simulator (RTDS). The RTDS simulates power electrical systems with time resolution of 50 μ s. The RTDS has a dedicated electronic board, named GTSYNC, that can receive the time reference from GPS antennas, in terms of PPS or IRIG-B signals. In this way, the generated signal can be referred to the Coordinated Universal Time (UTC). The synchronization accuracy of the GTSYNC is 1 μ s. The digital signal obtained in RTDS are synthesized into analog signals, by the GTAO board. The digital to analog converter generates a signal in the range \pm 10V with 16 bit, yielding a Least Significant Bit (LSB) of 0.305 mV. Considering a sinusoid with 50 Hz frequency and peak value equal to 5V, the maximum quantization error, equal to LSB/2, may bring an amplitude error equal to 0.0031 %. The complete conversion of the simulation results into analog signal bring an average delay equal to 3.155 μ s, which is compensated in the post analysis. Such delay was calculated, based on the following statements in GTAO datasheet: the exchange of data packet between RTDS' simulation boards and GTAO requires 180 ns for serialization, each GT Tx/Rx pair introduces a 335 ns latency to transmit and receive the data, the fiber cable delay is 6 ns per meter (in our case the total length of the fiber optic cable is 20 meters). The Analog Devices AD669AR DAC requires 68 microseconds to convert data (for a 10 Volt step). Checking in details the DAC's datasheet it is possible to see that such time is a combination of the effects of slew rate,

which is 8 μ s for a step of 20 V and the glitch time (overshoot that is present in case of a change of the Least Significant Bit (LSB)), which is approximately 2.5 μ s. Considering that the signals generated for the steady states have relatively small derivatives over the 50 μ s simulation time steps (the transition from one time step to the other goes from zero to a maximum of 0.16 V for the case with the 50th harmonic or 200% of nominal magnitude), we can state that the time required by the DAC conversion is constant and equal to 2.5 μ s. The resulting delay brings a constant phase angle error equal to 0.099 crad, which is then compensated.

V. TEST RESULTS

In the following sections the results are presented. The errors provided are TVE, FE and RFE; however, for a better understanding of the uncertainty, the maximum Magnitude Errors (MEs) and Phase angle Errors (PEs) are also given. The results are shown for the cases with different magnitudes, phase angles, frequency and harmonic content. The IEEE Std C37.118.1-2011 also requires to verify the maximum latency of the PMU, defined as the maximum time interval between the data report time stamp, and the time when the data becomes available at the PMU output. The standard requires the latency to be below 5 seconds. Even tough only qualitatively verified, the LOCO PMU shows to have actual latency far below the specified limit.

A. Steady state compliance - Voltage and current magnitude

The tests on voltage magnitude require to check the output of the PMU versus the input when the voltage magnitude spans over a range of 80% to 120 % of the nominal voltage. Similarly the error is evaluated when the current is in the range between 10% and 200% of the rated current. The LOCO PMU only accepts voltage input, therefore it is assumed that a current transducer is exploited, in order to convert the nominal input current into $5/\sqrt{2} \approx 3.536$ V RMS. The values are kept constant for 6 seconds, during the test phase, and successively increased by 10 % of nominal value each time. Under this point of view, it makes sense, to show the tests where the input signal magnitudes span over the range 10% - 200%, considering that they cover both the voltage and current inputs. The test results are shown in Fig. 2. It is possible to verify that the specification of the IEEE standard for M class, that is Max TVE = 1%, is always respected. In particular, it can be noticed, that for small magnitudes (e.g. 10%) the TVE tends to increase, probably due to a scarce exploitation of the full scale input of the PMU. In fact the signals vary over the range \pm 0.5 V while the full scale input is \pm 10 V. In such case, the FE, which however is not mentioned in the standard for this test, becomes almost 5 mHz. In general, magnitude and phase angle errors have an average value different from zero. This may reveal presence of small systematic errors in the PMU that could be compensated. In particular, as specified in section II-A, voltage offset errors are in the range of few mV, which may bring to 0.10 - 0.20 ME. Furthermore, time delays between the trigger of the PPS and the acquisition of samples may bring some error in the phase angle. In section II-A we calculated a possible error up to 0.3 crad, however, it is possible to see that the maximum error is always below 0.1 crad.

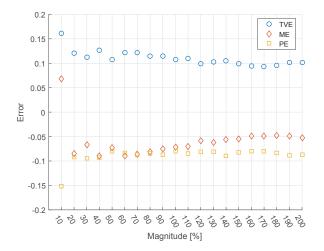


Fig. 2. TVE, ME and PE for test with magnitude variation. The y axis represents the percentage error for TVE and ME, while it represents the absolute phase angle error in crad for PE

B. Steady state compliance - phase angle

The standard IEEE Std C37.242-2013 states that the signal generated for testing purposes must be known with an uncertainty of less than 1 mrad (0.057 degrees). We expect, that once the phase compensation mentioned in section IV has been done, the aforementioned requirement is respected. The values are kept constant for 6 seconds, during the test phase, and increased by 0.3 radians each time, until a complete turn of 2π occurs. From the test results, shown in Fig. 3, it can be noticed that the TVE limit (in IEEE standards for M class is Max TVE = 1%) is always respected. In general all phase angles have scarce effect on TVE performances, which is always far below the 1 % limit.

C. Steady state compliance - frequency

For IEEE standards the frequency of the source should be known with an uncertainty of less than 0.1 mHz and the ROCOF should be less than 1 mHz/s. The signal magnitude, phase and frequency is kept constant for 6 seconds, during the test phase; then frequency is increased by 0.1 Hz each time to cover the range between 48 and 52 Hz. The test results, presented in Fig. 4, show that the TVE does not become greater than 0.25%, far below the limit of 1%; it can be seen that growing frequency leads to a slightly higher TVE, which is only due to a growing PE. Therefore, it is to be further verified the presence of systematic errors delays, and therefore phase angle errors, in the LOCO PMU. From Fig. 5 it is possible to see that the FE is always below 0.5 mHz, significantly less than the 5 mHz limit of the standard; and the RFE stays well below the limit of 0.1 Hz/s.

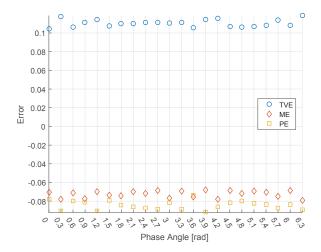


Fig. 3. TVE, ME and PE for test with phase angle variation. The y axis represents the percentage error for TVE and ME, while it represents the absolute phase angle error in crad for PE

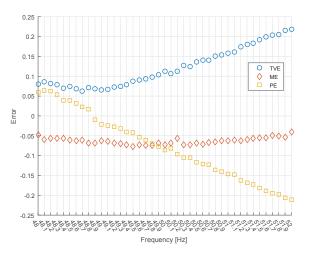


Fig. 4. TVE, ME and PE for test with frequency variation. The y axis represents the percentage error for TVE and ME, while it represents the absolute phase angle error in crad for PE

D. Steady state compliance - harmonics

The signal generator creates multiple harmonics, from the 2^{nd} till the 50^{th} of the nominal frequency. The magnitude of the harmonics are 10 % of the magnitude of the nominal input magnitude. These signals are generated in conjunction with a signal at nominal magnitude and frequency. The test results are presented in Fig. 6 and 7. The fulfilment of the standard requirement, which is maximum TVE less than 1% for M class PMUs, is met for all the harmonics, with a TVE actually below 0.20%. Also the maximum FE of 5 mHz/s is always respected.

VI. CONCLUSION

In this paper a PMU prototype, meant for distribution grids, was presented. The main design input were: a) low cost, therefore reduced amount of computation required, in order to be run into unexpensive hardware; b) standardized

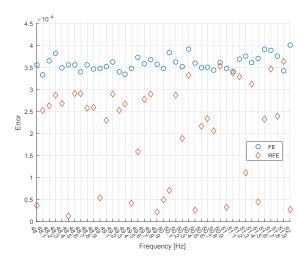


Fig. 5. FE and RFE for test with frequency variation. The y axis represents an error in Hz for FE, while it represents an error in Hz/s for RFE

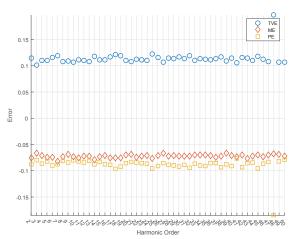


Fig. 6. TVE, ME and PE for test with different harmonic contributions. The y axis represents the percentage error for TVE and ME, while it represents the absolute phase angle error in crad for PE

communication interfaces via IEC 61850 standard; c) limited reporting rate in order to not congeste the scarce communication infrastructure available and to provide only steady state information, which is the one usually required for monitoring of distribution grids; d) fullfillment of IEEE accuracy standards. The LOCO PMU shows to respect such requirements. In particular, the steady state accuracy requirements are fulfilled with a large margin. The TVE is always below 0.25%; but such uncertainty can be further improved with further studies on systematic errors to be compensated. Among the novelties, with respect to the products already proposed in literature, is worth noting that the presented architecture does not exploit hardware with accurate internal clocks to synchronize signal acquisition. Instead, the external PPS signal is exploited to trigger acquisition and to maintain real time operation. This allow to further reduce the cost of the hardware components, given that DSP or micro-controllers are not needed. The

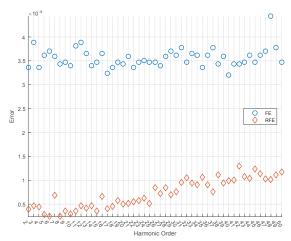


Fig. 7. FE and RFE for test with different harmonic contributions. The y axis represents an error in Hz for FE, while it represents an error in Hz/s for RFE

frequency and ROCOF estimation has been also optimized to reduce the issues in presence of noise and high harmonics.

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