Display Interfaces for the Control Unit of an Implantable Cardiac Pump

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Introduction

A cardiac pump consists of the implanted module providing monitoring of a heart rate and the external block providing processing and visualization of the logged data. One of basic elements of the external block is the graphic display. Coming from the sizes of device and quantity of displayed information, LCD and OLED displays are used as an output information device.

Presently the digital interfaces of image transferring are used for the small-size displays. The bit depth of information transmission depends on the depth of color of the image that we want to give. In black and white displays each pixel has from one to eight digits. In color displays it has from eight (RGB332) to 24 (RGB888) bits [1]. Figure 1 shows the type structure of graphic display control.

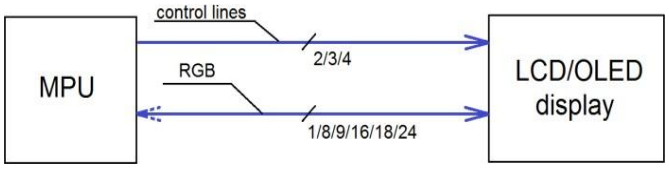


Figure 1: Typical connection of graphic displays

In the process of development restrictions and requirements, such as energy consumption, size, reliability, volume of the output information, cost etc., are imposed on a device. According to problem a developer make an optimal decision about the choice of hardware components. An interface, which will be used for data transmission, is chosen during work with graphic displays.

INTERFACES DESCRIPTION

A. Parallel interfaces

1. RGB interface:
Digital RGB interface has three timing signals - DOTCLK (PIXELCLK), HSYNC and VSYNC with frequencies of one pixel, line and frame transmission. Figure 2 shows the RGB transmission timing [2].

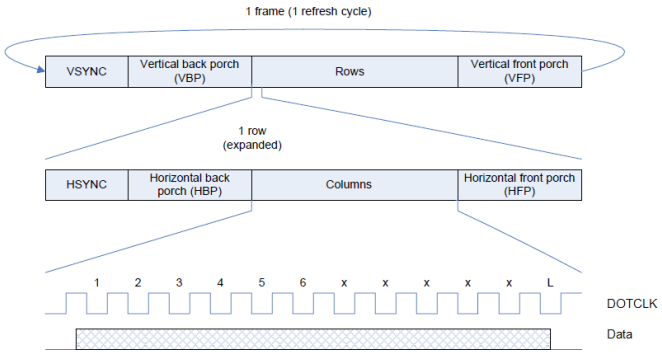


Figure 2: Frame and line timing parameters

To transmit a pixel color the parallel digital data bus is used. Width of bus is determined by colorize that we want to pass, or by restrictions of terminals. At the using of RGB interface, a width of data bus is 24 bits (RGB888). The feature of RGB interface work is transmission of full image frame. This method of image display is useful when it is necessary to change a picture on the screen constantly, for example, in the video transmission to screen.

2. System parallel interfaces.
For data transmission to a GPU it isn't always required to pass a full image. It is mostly necessary to change a small area of image on the screen. For this purpose Motorola and Intel companies created their own interfaces of graphic images transfer, which use registers of data transmission control in the RAM of GPU. The features of such interfaces are work with registers and delivery of control signal lines. The main difference between interfaces of Motorola and Intel companies is in the control signals. For the transmission of different color depth the different data bus width is used. We shall consider in detail every interface [3].

Intel 8080: Fig. 3 shows 8080-series bus interface [4]

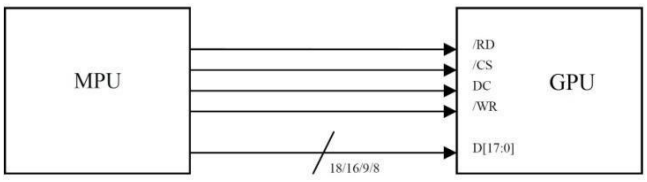


Figure 3: 8080-series Bus Interface

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The /WR and /RD signals are for indication writing to register and reading from register. The DC signal is used for designation of transmitted word type: command word (log.0) or data (log.1). The /CS signal is used for selecting chip of required device. There are timing performances of 8080 interface in the Table 1 [4]. Figure 4 shows the timing diagram of command/data writing [4].

Table 1: Parallel 8080, 6800 Timing Characteristics

Parameter	Min	Max	Unit
Clock Cycle Time (write cycle)	75	–	ns
Clock Cycle Time (read cycle)	450	–	ns
Pulse Width $\overline{CS}$ low (write cycle)	40	–	ns
Pulse Width $\overline{CS}$ high (write cycle)	25	–	ns
Data Access Time (READ)	250	–	ns
Output Hold time (READ)	100	–	ns
Pulse Width $\overline{CS}$ low (read cycle)	500	–	ns
Pulse Width $\overline{CS}$ high (read cycle)	500	–	ns
Rise time	–	4	ns
Fall time	–	4	ns

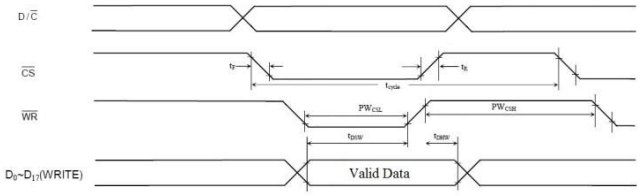


Figure 4: Parallel 8080-series Interface Timing Characteristics (write)

Motorola 6800: Fig. 5 shows 6800-series bus interface [1].

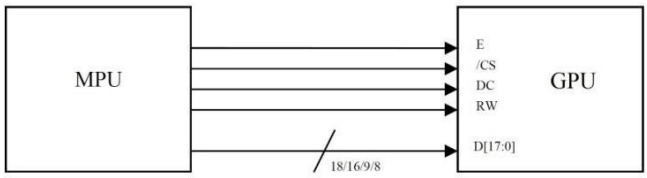


Figure 5: 6800-series Bus Interface

Unlike the Intel 8080 this interface is synchronous. For synchronization the E line, which latch data at the falling edge, is used. The RW control line is used for designation of read (log.1) or write (log.0) cycles. The DC signal is used for designation of transmitted word type: command word (log.0) or data (log.1). The /CS signal is used for selecting chip of required device. There are timing performances of Motorola 6800 interface in the Table 1 [4]. Figure 6 shows the timing diagram of command/data writing [4].

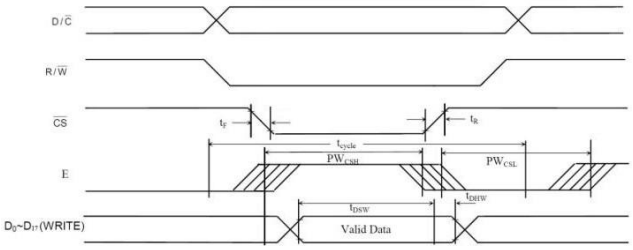


Figure 6: Parallel 6800-series Interface Timing Characteristics (write)

B. Serial system interface SPI

All considered interfaces had a parallel data bus. During resource lack the serial SPI interface is used for graphic data transmission. More often all this interface is used for black and white displays, which have a 1bpp capacity. There are 4-wire and 3-wire ways of data transmission by SPI.

4-wire SPI: Four flow lines are used for an information transfer. The SCLK signal is for data transmission clocking. The CS signal is used for selecting chip of required device. The SDI signal is used for data transmission. The SDC signal is used for designation of transmitted word type: command word (log.0) or data (log.1). In the process of one command word or data transmission 8 bits are used. There are timing performances of 4-wire SPI interface in the Table 2 [4]. Figure 7 shows the timing diagram of command/data writing [4].

Table 2: Serial Timing Characteristics

Parameter	Min	Max	Unit
Clock Cycle Time	75	–	ns
Chip Select Setup Time	2	–	ns
Chip Select Hold Time	10	–	ns
Clock Low Time	38	–	ns
Clock High Time	38	–	ns
Rise time	–	4	ns
Fall time	–	4	ns

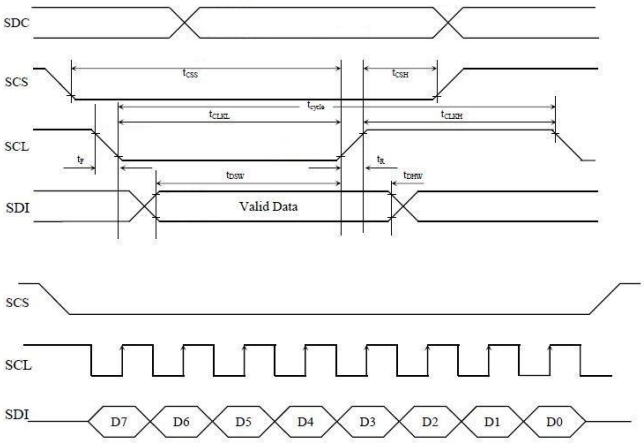


Figure 7: 4-wire Serial Timing Characteristics

3-wire SPI: Three flow lines are used for an information transfer. The SCLK signal is for data transmission clocking. The CS signal is used for selecting chip of required device. The SDI signal is used for data transmission. In the process of one command word or data transmission, 9 bits are used, and also the first bit points to a transmitted word type (command word or data). Figure 8 shows the timing diagram of command/data writing [4].

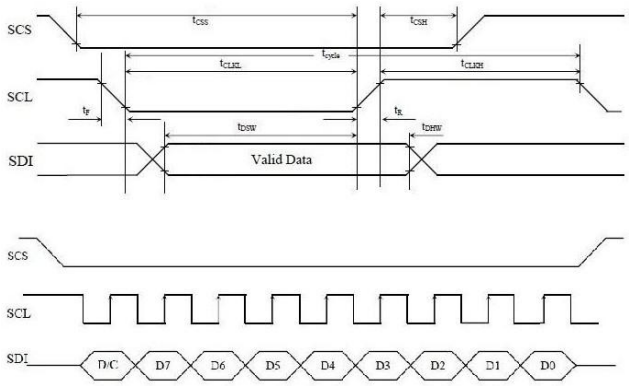


Figure 8: 3-wire Serial Timing Characteristics

Comparison of interfaces

Developing a device, it is necessary to understand, what interface will be optimal for this task. The basically criteria of interfaces comparison are memory, CPU time, number of wires and frame rate. There is comparing of interfaces in the Table 3.

Table 3: Comparison of interfaces

Interface / Criteria	RGB	Parallel 8/9 bpp	Parallel 16/18 bpp	SPI 4-wire
Memory	Bad	Good	Good	Good
CPU time	Good	Bad	Bad	Very bad
Number of wires	Bad	Middle	Bad	Good
Frame rate	Good	Good	Good	Bad

In considering each interface it is possible to select a few groups of the under development devices where its application will be optimal. The small-size devices with small output information scope are in the first group. Using of the internal MPU SPI unit is typical for such systems. The large-size devices with big output information scope are in the second group. Using of the parallel interface with the 16/18-bit data bus is the best variant for such systems. The small-size devices with big output information scope are in the third group. Using of the parallel interface with 8/9-bit data bus is typical for such systems. It should be taken that video controllers support transmission of bigger quantity of colors per pixel (16/18 bpp) in case of the 8/9- bit data bus. For this purpose we do two data sending instead of one, but we give up MPU time.

The classification given earlier is applicable to displays with internal video controller. In the absence of the internal GPU the RGB interface is used.

Conclusions

Comparing interfaces, we can note that everyone has advantages and disadvantages. When using parallel interfaces critical parameter is the MPU time. In the presence internal the MPU DMA unit we can transfer information to the display practically without using CPU time. The storage area which the DMA unit will transfer to a video controller is necessary for using this unit.

On the basis of the conducted research it has been decided to use for visualization of data of the Cardiac Pump the 8-bit Parallel Intel 8080 interface and color LCD with a 320x240 pixels screen resolution. Experiments were carried out and the MPU time was measured with and without using DMA. For display one-color rectangle at full screen size without using the DMA unit 15ms of MPU time and 1 byte of a memory were required. When using DMA ≈3us of MPU time and 75 Kbytes of a memory were required.

References

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Acknowledgment

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