All CVD Boron Nitride Encapsulated Graphene FETs

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Graphene is at the forefront of 2D material research, with many reports demonstrating the possibility of large area growth by means of chemical vapor deposition (CVD) [1]–[3]. Boron Nitride (BN) has been suggested to be the favorable substrate and encapsulation material for graphene devices as it preserves the intrinsic mobility performance [4]–[6]. However, the demonstration of BN-encapsulated graphene field effect transistors (GFETs) is so far limited to devices made from manually exfoliated flakes. Here, we report on CVD grown GFETs encapsulated by CVD grown BN with CMOS compatible nickel (Ni) edge contacts to the channel and discuss their performance.

CVD graphene grown on copper (Cu) foils was obtained from Graphenea while CVD BN on Cu foils was obtained from Graphene Supermarket. The CVD BN/graphene/BN (BN/G/BN) stack was fabricated using successive transfer and fishing steps after etching Cu with $FeCl_3$. AFM and Raman scans were performed to assess the thickness and quality of the stack. The total stack was ~16 nm thick (**Fig. 1**) and the encapsulated graphene showed typical G and 2D band signatures (**Fig. 2**). No characteristic Raman peak for hBN was found, suggesting an amorphous-like nature of the CVD grown BN. The BN was patterned with CHF_3 plasma while the graphene channel was etched in O_2 plasma by reactive ion etching (RIE). Edge contacts with sputtered Ni were deposited as described in [7]. 20 nm atomic layer deposited Al_2O_3 dielectric and 100 nm evaporated Al formed the top-gate stack (**Fig. 3** (a)). An optical micrograph of a fabricated GFET in coplanar waveguide layout is shown in **Fig. 3** (b).

Devices were electrically characterized in a Cascade probe station connected to an HP 4155B semiconductor parameter analyzer under ambient conditions. **Fig. 4** (a) shows the gate voltage dependent device resistance of a GFET with gate length (L_G) = 10 µm and channel width (W) = 20 µm. To extract field effect mobility (μ_{FE}) and contact resistance (R_C), the curve was fitted using the model described in [8]. Electron and hole mobilities of μ_{FE} = 3500 and 2500 cm^2/Vs and R_C value of ~2 kΩµm were observed. **Fig. 4** (b) shows the quasi-saturating output characteristics of the same device. The entire BN/G/BN stack was also characterized prior to patterning using non-contact near field terahertz (THz) spectroscopy for measuring the sheet resistance (R_{SH}) and mobility values of the graphene [9]. **Fig. 5** shows the cumulative probability distribution of the extracted THz mobility (μ_{THz}) extracted from the spectral THz transient response of the sample. The median of μ_{THz} was ~1500 cm^2/Vs, while the average μ_{THz} was ~ 2500 cm^2/Vs, which is in very good agreement with the electrical measurements. The average R_{SH} was ~500 Ω/sq. The devices were further characterized as voltage amplifiers in a resistive load scheme amplifier circuit (**Fig. 6** (a)). A 1 kHz input voltage signal was applied to the gate and the output voltage was monitored with a high impedance oscilloscope. Several devices were characterized in this configuration and the best voltage gain was measured to be approximately 6 dB for an applied offset gate-voltage of 3V at device dimensions of L_G = 10 µm and W = 10 µm (**Fig. 6** (b)).

In conclusion, we present all CVD BN/G/BN FETs which yield average mobility values of 2500 cm^2/Vs, R_{SH} in the range of ~500 Ω/sq and R_C ~ 2 kΩµm. Voltage gain of 6 dB is measured for these devices when configured in a low frequency signal amplifier circuit. These devices are the first demonstrations of such "all CVD" GFETs, with good mobility and voltage gain performance under ambient conditions. These results also demonstrate the graphene encapsulation properties of CVD BN, as the mobility does not degrade during device fabrication compared to conventional SiO_2 and device operation was possible under ambient condition. These results indicate the potential for future scalable and CMOS compatible all-2D devices and circuit architectures.

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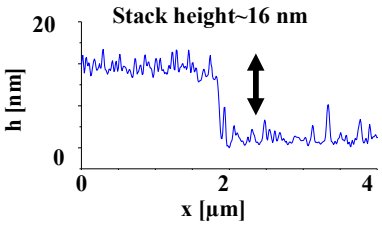

Fig. 1: AFM scan showing the total stack height observed to be around 16 nm (7-8 nm thick CVD BN on each side of the encapsulated CVD graphene)

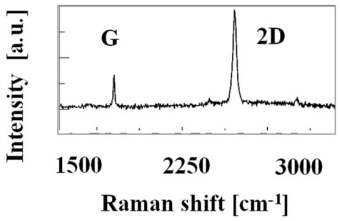

Fig. 2: Raman data showing that the stack formation does not deteriorate the quality of graphene (clear G & 2D peaks present), nonetheless, no sharp peak for BN was observed around 1370 cm^{-1} suggesting amorphous-like nature of BN films.

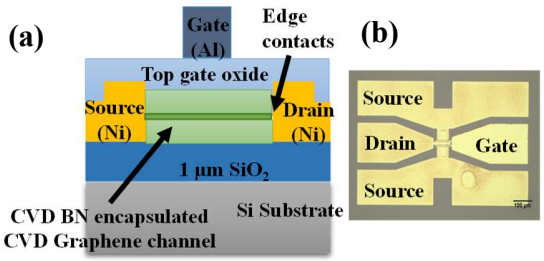

Fig. 3: (a) Cross sectional schematic of the device showing CMOS compatible edge contacts to graphene in this work. **(b)** Optical micrograph of typical final device in coplanar waveguide layout indicating source, drain and gate terminals.

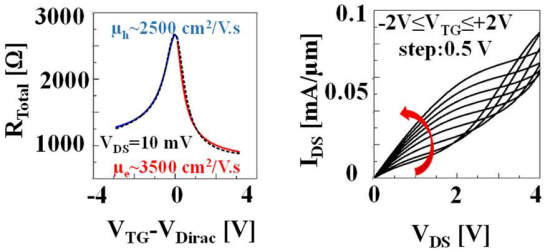

Fig. 4: (a) Low bias resistance of one GFET (L_G=10 µm, W=20 µm) as a function of top-gate voltage. Best fit to a model described in [8] gave electron and hole mobility values of 3500 cm^2/V.s and 2500 cm^2/V.s respectively. Dirac voltage V_D=0.12 V for this device. **(b)** Quasi-saturating output characteristics of the all-CVD BN encapsulated GFET (L_G=10 µm, W=20 µm).

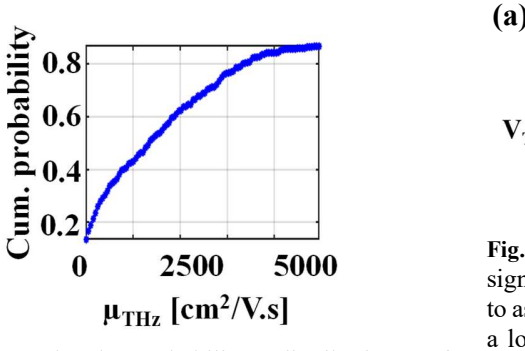

Fig. 5: Cumulated probability distribution of extracted THz mobility calculated based on non-contact THz mapping carried out on the CVD BN/G/BN stack prior to device fabrication. Median of mobility values is ~1500 cm^2/V.s while average mobility is ~2500 cm^2/V.s.

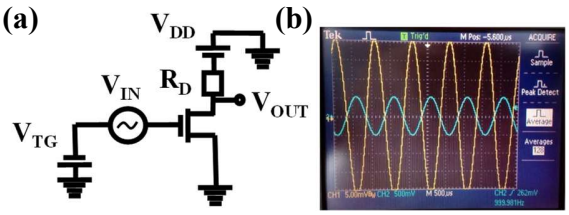

Fig. 6: (a) Simple schematic of a low frequency voltage signal amplifier circuit with resistive load scheme, used to assess the voltage gain performance of these devices; a load resistance (R_D) of 10 kΩ was mounted on the drain end. (b) Screen shot of Oscilloscope showing the highest measured voltage gain of ~6 dB at 1 kHz for a device with L_G=10 µm and W=10 µm respectively; applied signal is shown in blue while amplified output signal is shown in yellow on the screen. The applied AC input voltage was 20 mV_{PP} and the measured output voltage was 40 mV_{PP}.

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