

Optimized IGBT Turn-Off Switching Performance Using the Full Device Safe Operating Area

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Abstract—In this work, a multiple stage gate driver based on a switched gate resistor topology for an insulated-gate bipolar transistor (IGBT) is presented. An optimization procedure to reduce the turn-off switching losses while maintaining equal device stress is presented. The presented driver uses the maximum operating conditions of the IGBT in the entire operating range, while commercial drivers are usually designed for a worst case operating point. It is shown that, compared to a state of the art commercial gate driver, switching loss improvements are achieved when using the full device capability at partial load. An increase in efficiency by reducing switching losses in the partial load range represents a significant improvement for most power electronics converter applications because they are operated most of the time in the partial load range. The paper concludes with an evaluation of the measurement results, showing switching loss improvements of up to 50 % compared to a commercial gate driver in the partial load range.

I. INTRODUCTION

Power electronic converters are the key components of future electric vehicles (EVs) [1]–[3]. Today, efforts are still required to improve their power and weight densities to reduce costs. Several approaches to achieve this target are discussed widely in literature, for example modular converter concepts [4] or solutions based on wide-bandgap (WBG) power semiconductors [5], [6]. Besides the approach via different converter topologies, the packaging of power electronic converters plays an important role in finding optimized solutions. This includes embedded solutions with reduced parasitic elements [7], [8] and improved cooling concepts [9]–[11]. Furthermore, the utilization of existing power semiconductors can be increased by using more advanced gate driving techniques [12] and thermal management [13]–[17].

In hard-switching topologies, switching losses are a non-negligible factor in the loss balance. A commonly used gate driver topology is the push-pull output stage [18], [19]. This type of driver uses a fixed gate resistor, which is designed for the worst-case operating point and therefore resulting in a suboptimal performance in the remaining operation points. Therefore, the switching losses can be reduced over the whole operating range by employing more sophisticated gate driving techniques [20]–[22]. A voltage source driver (VSD) for insulated-gate bipolar transistors (IGBTs) that varies the gate resistance during the switching event is presented in [20], [23]–[25]. A current source driver (CSD) for IGBTs that

controls the gate current during switching to reduce switching losses is proposed in [21]. A commercially available CSD, which changes the gate current level during the turn-on event is given in [26]. In the work presented in [27], a gate driver using a voltage ramp instead of a step is used, which results in reduced turn-on losses and low transient overshoots. Although all of these suggestions present gate drivers, which result in reduced switching losses, they do not describe how to find optimum settings of the gate driving technique.

This paper presents the impact of a stepwise gate driver on the turn-off transients and introduces an optimization algorithm to find the stepwise gate driver settings. The effects of different driver settings on the turn-off event with regard to the turn-off switching losses and the transient voltage overshoots are described. Based on this, an optimization procedure is presented, which guarantees minimum switching losses, while the transient voltage overshoot remains within the safe operating area (SOA). The turn-off switching losses are compared to a reference driver, using a pull driver stage for the turn-off event. The switching loss extraction from the measurements is explained in detail in section II.

II. SWITCHING LOSS DETERMINATION

The switching losses are extracted from double pulse test measurements according to [28]. An automated test bench [29] is used to conduct measurements over a large operating range, including junction temperature variation [28]. The specifications of the investigated non-punch through (NPT) IGBT module are listed in Table I. The power module contains a half bridge with two paralleled dies on the low- and high side, with individual gate terminals. For all measurements in this work, only one die is used while the paralleled die is disabled

TABLE I
SEMICONDUCTOR DEVICE [20]

Property	Value
Nominal Voltage	800 V
Nominal Current	300 A per die
Technology	Planar gate NPT [19], [30]

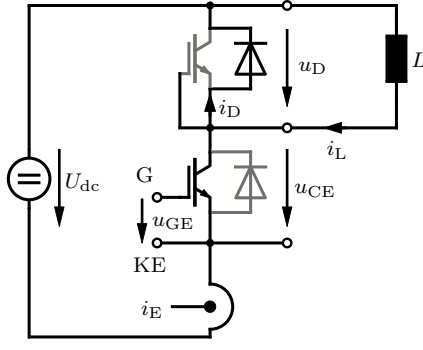


Fig. 1. Schematic of the double pulse test [20]

TABLE II
EMPLOYED MEASURING PROBES [21]

Symbol	Probe
u_{CE}	PMK Bumblebee
u_D	PMK Bumblebee
u_{GE}	Testec TT-SI 200
i_{gate}	Testec TT-SI 200 (R_{gate} as shunt)
i_E	T&M SBNC-A-2-01

by shorting the corresponding gate contact with the Kelvin emitter.

A. Measurement Setup

To calculate the switching losses of the device under test (DUT), the collector-emitter voltage u_{CE} and the emitter current i_E are recorded during the switching transient using an oscilloscope. Figure 1 shows a simplified circuit diagram with the measured voltages and currents. The collector-emitter voltage u_{CE} and the gate-emitter voltage u_{GE} are measured between the gate and Kelvin emitter (KE) contact of the IGBT module. A *LeCroy HDO6104* oscilloscope is used to record the measurements. This oscilloscope has a sampling rate of 2.5 GS/s and a vertical resolution of 12 bit. Table II lists the employed measurement probes.

B. Switching Loss Calculation

The switching loss extraction from the double pulse measurements is in accordance to the algorithm presented in [20], [21]. Figure 2 shows an exemplary turn-off transient, including the instantaneous dissipation power p_{SW} of the switch and the course of the corresponding integral E_{off} . The instantaneous power p_{SW} of the switch is calculated using

$$p_{SW} = u_{CE} \cdot i_E.$$

The corresponding turn-off energy E_{off} is then determined using

$$E_{off} = \int_{t_0}^{t_1} p_{SW} \cdot dt.$$

As shown in Fig. 2, the integration borders are defined using the left and right 5 % limits of the instantaneous power $\hat{P}_{SW,off}$.

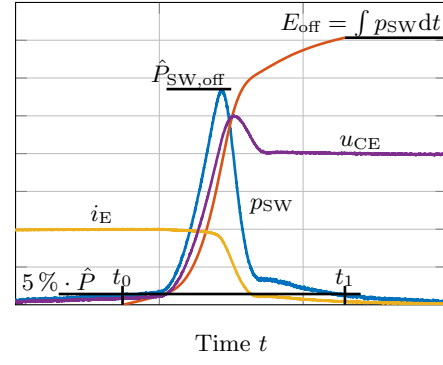


Fig. 2. Exemplary turn-off transient including the loss energy [20]

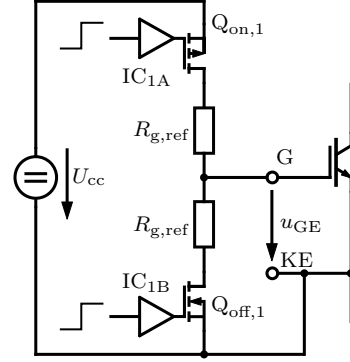


Fig. 3. Push-pull driver stage topology

III. DRIVER TOPOLOGIES

This section introduces the topologies, implementation and the operation principle of the reference gate driver and stepwise gate driver.

A. Reference Driver

The reference driver uses a push-pull driver stage with a gate resistance $R_{g,ref} = 14.2 \Omega$. The topology is shown in Fig. 3. The metal-oxide semiconductor field-effect transistor (MOSFET) $Q_{on,1}$ is used to turn the IGBT on, while the MOSFET $Q_{off,1}$ is utilized to turn the IGBT off. With a simple push-pull driver stage, the gate resistor must be designed for the worst-case operating point. It is not possible to change the driver configuration depending on the operating point, which results in unnecessarily high switching losses in the partial load range.

B. Stepwise Gate Driver

The stepwise driver used in this work is presented in [20], [21]. The driver output stage consists of five push-pull driver stages, which all have different gate resistors and are independently controlled by an field programmable gate array (FPGA). A circuit diagram of the output stage is shown in Fig. 4. The FPGA is clocked with 100 MHz, which results in a temporal resolution of 10 ns at which the gate resistance can be switched. An exemplary profile of the gate resistance

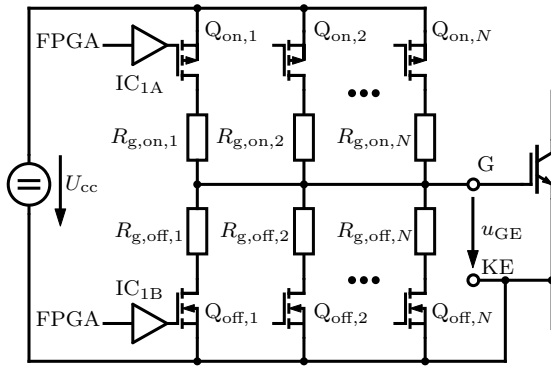


Fig. 4. Stepwise gate driver topology [20]

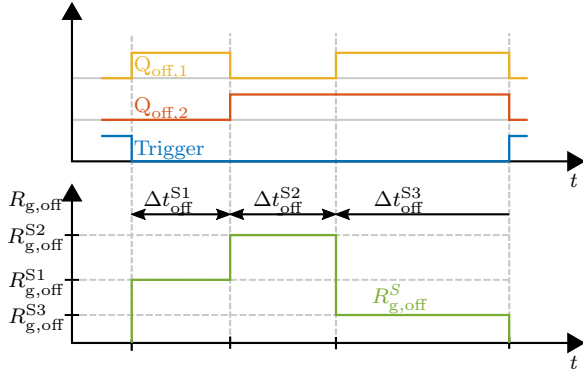


Fig. 5. Exemplary gate resistance profile

$R_{g,off}^S$ during a turn-off event is shown in Fig. 5. A switching event is divided into three stages. During the first stage, a small gate resistance $R_{g,off}^{S1}$ is used. Due to the small gate resistance, the IGBT gate is quickly discharged and the turn-off process is speeded up accordingly. After a defined time Δt_{off}^{S1} , the output stage switches to a larger gate resistance $R_{g,off}^{S2}$. During the third stage, a smaller gate resistor is applied at the time $t = \Delta t_{off}^{S1} + \Delta t_{off}^{S2}$ until the turn-off event is finished.

IV. INFLUENCE OF THE STAGES ON THE SWITCHING BEHAVIOR

The effects of the stepwise driver on the transient switching behavior are evaluated experimentally. The measurements are performed with different driver settings and the results are compared to the push-pull reference driver. A detailed investigation is shown in [20]. In this work, the turn-off behavior with two and three stages is investigated.

A. Two-Stage Turn-Off Event Behaviour

In two-stage operation, two different gate resistors are used. The effects of different values for the duration Δt_{off}^{S1} of the first stage are shown in Fig. 6 and Fig. 7. The measurements use a DC-link voltage $U_{dc} = 200$ V and a load current $I_{load} = 100$ A. The driver settings are listed in Table III. The time Δt_{off}^{S1} is increased in 10 ns steps. The Fig. 6 shows the collector-emitter voltage u_{CE} and the emitter current i_E . A higher duration of

TABLE III
TWO STAGE TURN-OFF DRIVER CONFIGURATION [20]

Stage S	$R_{g,off}^S$	Δt_{off}^S
S1	$R_{g,off,1} = 4.7 \Omega$	410 ns ... 440 ns
S2	$R_{g,off,3} = 33 \Omega$	∞

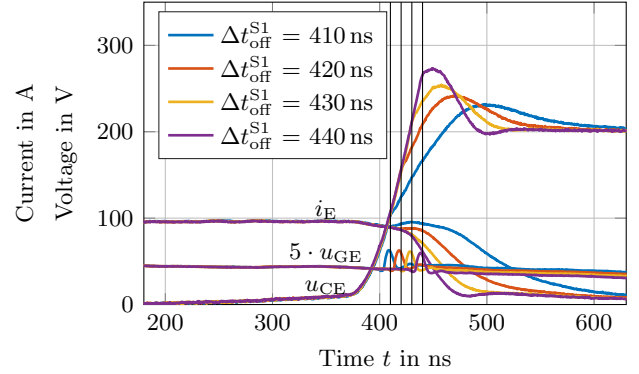


Fig. 6. Influence on the turn-off event waveforms for different durations Δt_{off}^{S1} of the first stage at $U_{dc} = 200$ V and $I_{load} = 100$ A [20]

the time Δt_{off}^{S1} results in a higher collector-emitter voltage overshoot $\hat{U}_{CE}$ and faster decaying of the emitter current i_E .

The Fig. 7 shows the instantaneous power dissipation p_{sw} of the switch and the integral of the instantaneous power dissipation which corresponds to the switching losses E_{off} . With a longer duration Δt_{off}^{S1} of the first stage, the turn-off switching losses E_{off} decrease. This is explained by the fact, that the gate is charged faster during a longer time using a smaller gate resistance $R_{g,off}^{S1}$, which in turn results in a shorter switching process. Different resistors $R_{g,off}^{S1}$ and $R_{g,off}^{S2}$ have quite small effects on the switching transient compared to different times Δt_{off}^{S1} , as described in [20], and are therefore not further discussed in this paper.

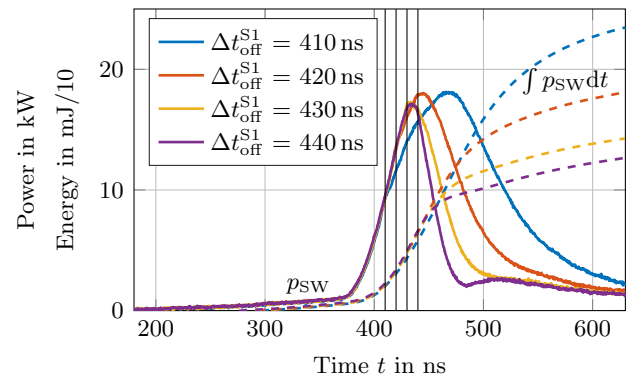


Fig. 7. Influence on the turn-off event losses for different durations Δt_{off}^{S1} of the first stage at $U_{dc} = 200$ V and $I_{load} = 100$ A [20]

TABLE IV
THREE STAGE TURN-OFF DRIVER CONFIGURATION [20]

Stage S	$R_{g,off}^S$	Δt_{off}^S
S1	$R_{g,off,1} \parallel R_{g,off,3} = 4.1 \Omega$	390 ns
S2	$R_{g,off,3} = 33 \Omega$	60 ns ... 160 ns
S3	$R_{g,off,1} \parallel R_{g,off,3} = 4.1 \Omega$	∞

B. Three-Stage Turn-Off Event Behavior

In the three-stage mode, the third stage is used to shorten the switching process. The examined driver settings are listed in Table IV. The corresponding measurements of the collector-emitter voltage u_{CE} and emitter current i_E are shown in Fig. 8. Due to the faster discharging of the gate during the third stage compared to the second stage, the slopes of the collector-emitter voltage u_{CE} and emitter current i_E become steeper. It is also seen, that at the beginning of the third stage, a bump in the collector-emitter voltage u_{CE} occurs that may be greater than the previous transient overshoot (e.g., with $\Delta t_{off}^{S2} = 60$ ns).

The corresponding turn-off losses can be seen in Fig. 9. As the Δt_{off}^{S2} duration decreases, a dent increases in the waveform of the instantaneous power loss p_{sw} . This leads to a reduction of the turn-off loss energy E_{off} with shorter duration Δt_{off}^{S2} .

V. OPTIMIZATION PROCEDURE

This section explains the optimization procedure to find the optimized stepwise driver profile. The aim of the optimization is to reduce the turn-off switching losses E_{off} as much as possible without increasing the collector-emitter voltage u_{CE} above the worst case value specified by the reference driver. First, the optimization criteria are explained, followed by the optimization procedure. The optimization procedure is divided into two iterations.

A. Constraints

The optimized driver profile should allow a turn-off event in which the collector-emitter voltage u_{CE} does not exceed a

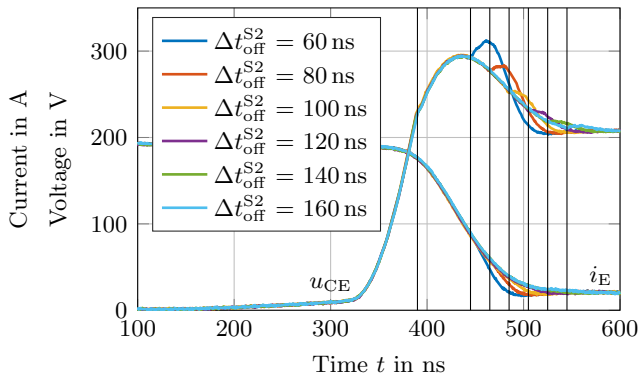


Fig. 8. Influence on the turn-off event waveforms for different durations Δt_{off}^{S2} of the second stage at $U_{dc} = 200$ V and $I_{load} = 200$ A [20]

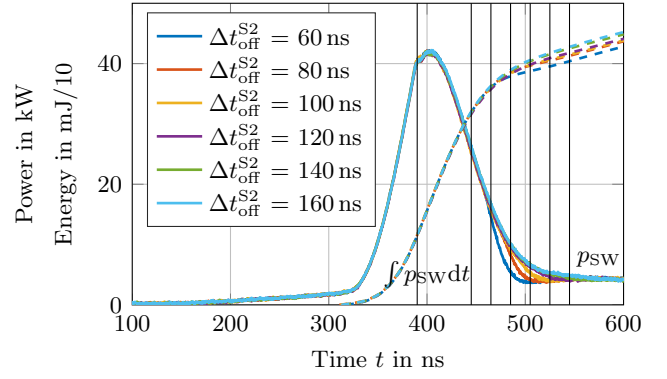


Fig. 9. Influence on the turn-off event losses for different durations Δt_{off}^{S2} of the second stage at $U_{dc} = 200$ V and $I_{load} = 200$ A [20]

maximum value of $\hat{U}_{CE,crit} = 520$ V. This value corresponds to the maximum value measured with the reference driver. The minimum gate resistance is $R_{g,min} = 3 \Omega$. A lower gate resistance causes oscillations in the gate emitter voltage u_{GE} and is therefore not considered.

B. First Optimization Iteration

In the first iteration, the best values for the gate resistance of the first and second stage and the duration of the first stage are searched.

The first optimization iteration starts with a safe operating point to avoid damage to the power module. The flowchart of the first optimization iteration is seen in Fig. 10. The minimum gate resistance $R_{g,off}^{S1} = R_{g,min}$ is used as gate resistance for the first stage. However, the duration Δt_{off}^{S1} of the first stage is initially set to 0 s so that the first stage, and therewith the small gate resistance, has no effect on the switching process. In the second stage, a gate resistor $R_{g,off}^{S2} = R_{g,ref}$ is used. Due to the initial conditions, the stepwise driver acts at first like the reference driver. This ensures that the condition for the maximum voltage overshoot $\hat{U}_{CE} \leq \hat{U}_{CE,crit}$ is satisfied.

In the following step, the duration Δt_{off}^{S1} of the first stage is increased until the overvoltage constraint is violated. Then, the resistance $R_{g,off}^{S2}$ of the second stage is increased and a new measurement is made. By increasing the resistance $R_{g,off}^{S2}$, the voltage overshoot decreases and the duration of the second stage can be increased again. These steps are repeated until the second stage gate resistance reaches $R_{g,off}^{S2} = R_{g,max} = 100 \Omega$. Since the collector-emitter overvoltage $\hat{U}_{CE}$ is monitored during the optimization and only rises slowly, the power module is not damaged. All valid measurements are stored and are used as initial setup for the second optimization iteration. If the duration of the first stage exceeds $\Delta t_{off}^{S1} \geq 1 \mu s$, it is assumed that the gate resistor can be used for the entire switching operation at the investigated operating point. In this case, the stepwise driver is used as a pull driver stage with a gate resistor $R_{gate} = R_{g,min}$. Therefore, there is no need for further optimization.

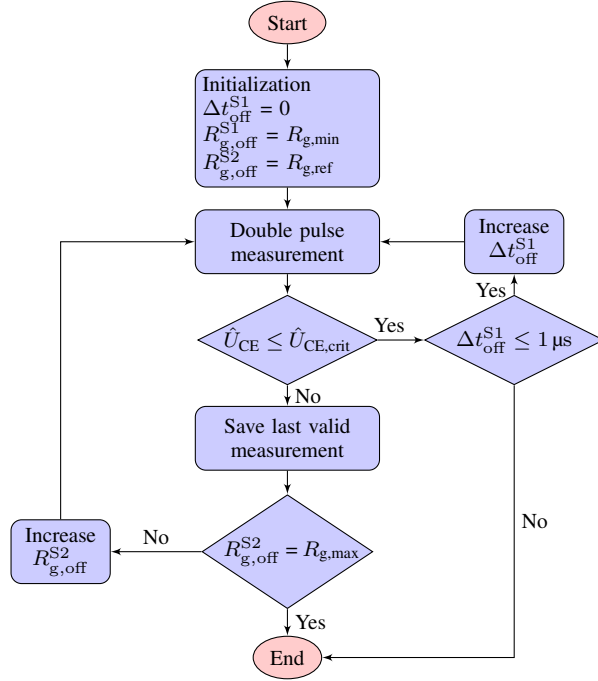


Fig. 10. First optimization iteration flowchart

C. Second Optimization Iteration

The second iteration step of the optimization procedure serves to find the optimal duration of the second stage. Therefore a third stage is used to accelerate the switching process after the voltage overshoot. The corresponding flowchart is shown in Fig. 11. As an initial setup, the gate resistor of the third stage is set to $R_{g,off}^{S3} = R_{g,min}$. The duration of the second stage Δt_{off}^{S2} is initially selected so that the third stage has no influence on the switching process (e.g., $\Delta t_{off}^{S2} = 500$ ns). All valid measurements from the first optimization iteration are used as initial values for the resistance of the first and second stage and for the duration of the first stage.

In the second optimization iteration, the duration Δt_{off}^{S2} of the second stage is reduced until the voltage overshoot of the collector-emitter voltage u_{CE} is greater than the maximum permitted value $\hat{U}_{CE,crit}$. If the duration Δt_{off}^{S2} reaches zero before the collector-emitter voltage overshoot is greater than the permitted value, the first iteration step was incorrectly optimized. Normally, the last valid measurement is saved and the next available measurement from the first optimization iteration is chosen. As already mentioned, the selection of the gate resistor $R_{g,off}^{S3}$ has a minor effect on the switching behavior. For this reason, the resistor $R_{g,off}^{S3}$ is used to make minor adjustments where the time resolution of the FPGA is not sufficient.

VI. RESULTS

The switching losses and peak voltages are extracted from the measurements resulting from the optimization procedure. All measurements of the optimization for the operating point with a DC-link voltage $U_{dc} = 400$ V and a load current

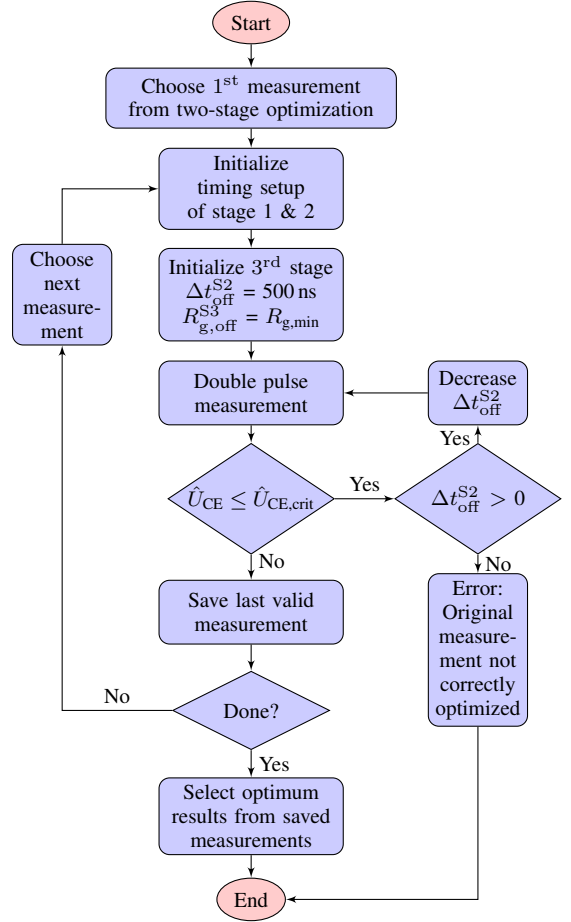


Fig. 11. Second optimization iteration flowchart

$I_{load} = 200$ A are shown in Fig. 12. The switching losses and peak voltages are extracted from the measurements made in the optimization. On the x-axis, the turn-off switching energy E_{off} normalized to the turn-off switching energy of the reference driver $E_{off,ref}$ is plotted. The collector-emitter voltage overshoot $\hat{U}_{CE}$ normalized to the worst case $\hat{U}_{CE,crit} = 520$ V is plotted on the y-axis.

Each individual dot represents a measurement resulting from the optimization procedure. Different colored dots represent different resistance sets, while dots with the same color use the same resistance set, although with different timing settings. The red dot represents the reference driver measurement. It is seen, that a Pareto front is formed by the measurements resulting from the optimization. This shows, that the optimization method achieves the optimal settings for the stepwise driver and that no further improvements are possible. It is also seen, that the stepwise driver results in lower switching losses even with the same overshoot as the reference driver.

Figure 13 shows the maximum collector-emitter voltage $\hat{U}_{CE}$ with a load current $I_{load} = 20$ A ... 300 A and a DC-link voltage $U_{dc} = 400$ V. The collector-emitter voltage overshoot $\hat{U}_{CE}$ is shown for the reference driver and for the optimized stepwise driver setup. Up to a load current of $I_{load} = 90$ A,

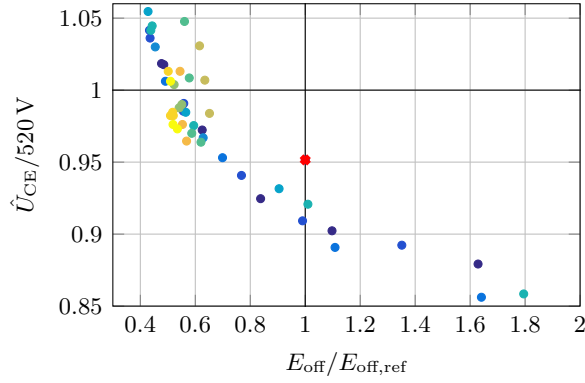


Fig. 12. Normalized collector-emitter voltage overshoot $\hat{U}_{CE}/520$ V vs. normalized turn-off switching losses $E_{off}/E_{off,ref}$. Operating point: $U_{dc} = 400$ V and $I_{load} = 200$ A

the stepwise driver is not used in stepwise operation, but as a pull driver stage using a gate resistor $R_{gate} = 3 \Omega$. With load currents $I_{load} > 90$ A, the collector-emitter voltage u_{CE} would exceed the allowed value $\hat{U}_{CE,crit} = 520$ V. Therefore, the stepwise driver optimization is used to reduced the collector-emitter voltage overshoots $\hat{U}_{CE}$ to a value lower than 520 V. The maximum collector-emitter voltage overshoot $\hat{U}_{CE}$ of the reference driver only gets close to the critical value at the maximum load current $I_{load} = 300$ A.

In Fig. 14, the comparison of the two drivers is shown regarding the turn-off losses E_{off} . The stepwise driver shows lower losses than the reference driver for every operating point. At a load current $I_{load} = 200$ A, the turn-off losses are measured to $E_{off,step} = 6.72$ mJ and $E_{off,ref} = 13.7$ mJ for the stepwise driver and reference driver, respectively, which equivalents to a reduction by 50 %. The reduced losses are explained with the fact that the reference pull driver stage configuration has to be designed for the worst case at maximum load condition, while the stepwise driver is able to adapt the driver profile to the given operating point.

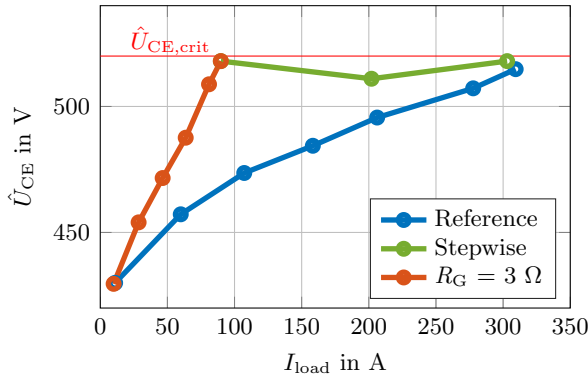


Fig. 13. Comparison of the proposed driver and reference driver regarding to collector-emitter voltage overshoot $\hat{U}_{CE}$ at different load currents I_{load} . Operating point: $U_{dc} = 400$ V and $I_{load} = 10$ A ... 300 A

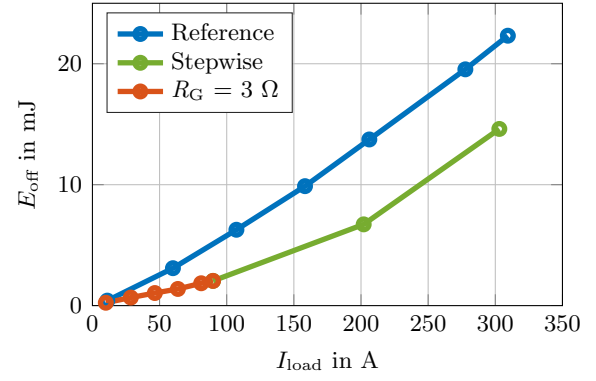


Fig. 14. Comparison of the proposed driver and reference driver regarding to turn-off energy E_{off} at different load currents I_{load} . Operating point: $U_{dc} = 400$ V and $I_{load} = 10$ A ... 300 A

VII. CONCLUSIONS AND OUTLOOK

In this work, a stepwise driver and optimization procedure utilizing the full device safe operating area has been introduced. First, the influence of different driver configurations on the turn-off event of a low voltage IGBT module was shown. A procedure for reducing switching losses whilst maintaining voltage overshoots below the critical values has been presented and verified. The turn-off losses are reduced by up to 50 % using the presented gate driver. To select the optimized driver profile, the load current and the DC-link voltage have to be measured. Usually these values are already measured in a converter, since they are required for safety and control. Therefore, no additional cost for sensors is required using the proposed driver. The stepwise driver generates steeper voltage and current slopes, which requires the effects on electromagnetic interference to be examined in the future.

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