Fourier-Domain Data-Converters: New Concepts for High Data Rate Wireless Transmitter Systems

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PhD Thesis

Oner Hanay

An arbitrary function continuous or with discontinuities, defined in a finite interval by an arbitrary capricious graph can always be expressed as as sum of sinusoids.

J.B.J. Fourier
1768 – 1830.

To my parents, my wife and daughter...

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Preface

The burgeoning demand on large modulation bandwidths pushes the recent mobile communication standards towards mmW frequencies. Even at these frequencies a high spectral efficiency is crucial in order to fully exploit the available channel capacity. State-of-the-art transmitter (Tx) topologies face challenges when employed for large modulation bandwidths in the range of several gigahertz. Because of the serialized high-speed data stream, the digital signal processing requires extremely high sampling rates for spectral shaping by oversampling and FIR filtering which sets a practical technological limitation. Besides, the digital-to-analogue conversion also takes place at this high sampling rate. In order to address these fundamental challenges, more advanced and expensive CMOS processes are required. Moreover, high sampling rates are associated with large power consumption and more complex circuits. Since 5G and beyond communication is aiming at a substantially increased data rate of up to 1Tbit/s, evolution cannot rely primarily on technological advances, also because CMOS scaling is coming to an end. Innovation on both conceptual as well as architectural level are thus necessary to meet the ambitious goals.

The goal of this thesis is to introduce a distinct data-converter concept, the Fourier-domain digital-to-analogue converter (FDDAC), demonstrated in a novel Tx architecture to overcome the limitations and bottlenecks in the analogue and the digital domain in typical Txs. The FDDAC concept exploits the relation between the discrete-time and inverse continuous-time Fourier transform to generate a wide modulation bandwidth

at virtually any frequency while reducing the sampling rate of the DSP and the data converters by up to two orders of magnitude. At the same time, without additional digital and analogue filtering, the FDDAC provides inherent spectral shaping. In the proposed FDDAC-based Tx the entire signal processing and analogue/mixed-signal circuits operate far from today's technological limitations while providing very wide modulation bandwidths, i.e. in the range of multiple gigahertz. This makes the proposed concept an enabling technology for extremely high data rate future wired and wireless communication.

The proposed data conversion approach is thoroughly analysed and employed in a transmitter prototype which is modelled in order to understand its capabilities and limitations. A first lab validation prototype is implemented based on commercially available off-the-shelf discrete components that demonstrated a modulation bandwidth of up to 100MHz at a maximum sampling rate of 25MSps achieving 400Mbit/s. Based on the gained practical experience, three integrated transmitters in a 65nm CMOS technology are implemented. Due to the architectural advances introduced by the FDDAC technique, a modulation bandwidth of up to 2GHz is targeted while the highest sampling rate in the Tx is 250MSps. Thus, the complete DSP including pseudo-random bit generation, modulation, FFT calculations and spectral shaping is cointegrated with the I/Q transmit cores and phasor tone synthesisers on a single die. The I/Q transmit cores are implemented based on 8bit I/Q RFDACs in the first two design iterations whereas the third design contains power efficient 9bit I/Q DACs, passive mixers and output amplifier buffers allowing a 18dB higher output power while reducing the power consumption and increasing the signal quality. The implemented Txs iteratively improve the demonstrated data rate from 2 to 8 Gbit/s while reducing the power consumption by a factor of 2 each iteration. The measured EVM values are 7.2% and 11.% for a 1 and 2 GHz QPSK signal, respectively, whereas they are 9.6% and 13.9% for the 1 and 2 GHz-wide 16QAM signal. The generated transmit signal fully comply with the spectral mask defined in the IEEE WiGig standard while surpassing the defined modulation bandwidth by 14%. Furthermore, the same hardware is used to replace a multitude of simultaneously operating conventional Txs which is demonstrated by generating 16 31.25 MHz modulated signals with a constant frequency spacing. The measured EVM values are as low as 2.2% and 2.5% for QPSK and 16QAM modulated signals, respectively. Finally, two mmW upconversion mixers are implemented in the same 65 nm CMOS technology demonstrating an outstanding conversion gain and operation bandwidth allowing to shift the output of the implemented transmitters to the 5G 28 GHz and 60 GHz ISM bands.

The proposed transmitter architecture has the potential to replace a multitude of transmitters in mobile communication devices while allowing substantially higher data rates at significantly reduced power consumption. Thus, the cost and complexity of handheld communication devices can be reduced remarkably by allowing the imple-

mentation of true multistandard transmitters. The developed concept will enable new consumer experience in applications such as wireless virtual reality, beyond 5G wireless communications, and extremely low latency high data rate applications. The demonstrated advances in combination with the presented vision have the potential to form beyond 5G communication standards and change the entire class of mobile communication devices.

Aachen, September 14$^{\text{th}}$, 2020

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List of Abbreviations

ACLR	Adjacent Channel Leakage Ratio . . . 3
ADC	Analogue-to-Digital Converter . . . 2
ADDLL	All Digital Delay-Locked-Loop . . . 91
AM	Amplitude Modulation . . . 9
BER	Bit Error Rate . . . 24
BW	Bandwidth . . . 30
CMOS	Complimentary Metal-Oxide-Semiconductor . . . 7
COLA	Constant overlap and add . . . 101
DAC	Digital-to-Analogue Converter . . . 2
DCDL	digitally controlled delay line . . . 91
DDS	Direct Digital Synthesis . . . 88
DEM	Dynamic Element Matching . . . 162
DFF	D-Type Flip-Flop . . . 108
DFT	Discrete Fourier Transform . . . 29
DLL	Delay-Locked Loop . . . 57
DNL	Differential Nonlinearity . . . 17
DNW	Deep N-Well . . . 153
DRC	Design Rules Check . . . 122
DSP	Digital Signal Processing . . . 3
EM	Electromagnetic . . . 99
ENOB	Effective Number of Bits . . . 17

EVM Error Vector Magnitude . . . 23
FBM Full-Bandwidth-Mode . . . 94
FCC *Federal Communications Commission* . . . 8
FDDAC Fourier-Domain Digital-to-Analogue Converter . . . 4
FDADC Fourier-Domain Analogue-to-Digital Converter . . . 45
FFT Fast Fourier Transform . . . 37
FIFO First-in, First-out . . . 103
FIR Finite Impuls Response . . . 28
FM Frequency Modulation . . . 9
FMC FPGA Mezzanine Card (connector type) . . . 71
FoM Figure-of-Merit . . . 44
FPGA Field Programmable Gate Array . . . 70
FT Fourier Transformation . . . xviii
FWA Fixed Wireless Access . . . 1
GSG Ground-Signal-Ground . . . 196
GSSG Ground-Signal-Signal-Ground . . . 132
GUI Graphical User Interface . . . 138
HBM Half-Bandwidth-Mode . . . 49
HDL Hardware Description Language . . . 102
IC Integrated Circuit . . . 5
IDFT Inverse Discrete Fourier Transform . . . 30
IEEE Institute of Electrical and Electronics Engineers
IF Intermediate Frequency . . . 21
IIP Input Intercept Point . . . 196
IoT Internet of Things . . . 47
IFT inverse Fourier Transform . . . 29
INL Integral Nonlinearity . . . 17
IRR Image Rejection Ratio . . . 178
ISI Inter-Symbol Interference . . . 24
ITU *International Telecommunication Union* . . . 8
LDO Low-Dropout Regulator . . . 75
LSFR Linear Shift Feedback Register . . . 86
LO Local Oscillator . . . 16
LSB Least Significant Bit . . . 106
LUT Look-Up Table . . . 124
LVDS Low-Voltage Differential Signaling . . . 71
mmW Millimetre-Waves . . . 3
OFDM Orthogonal Frequency Division Modulation . . . 25
OOK On-Off Keying . . . 10
OSR Over-Sampling Ratio . . . 13
PA Power Amplifier . . . 21
PAPR Peak-to-Average Power Ratio . . . 133

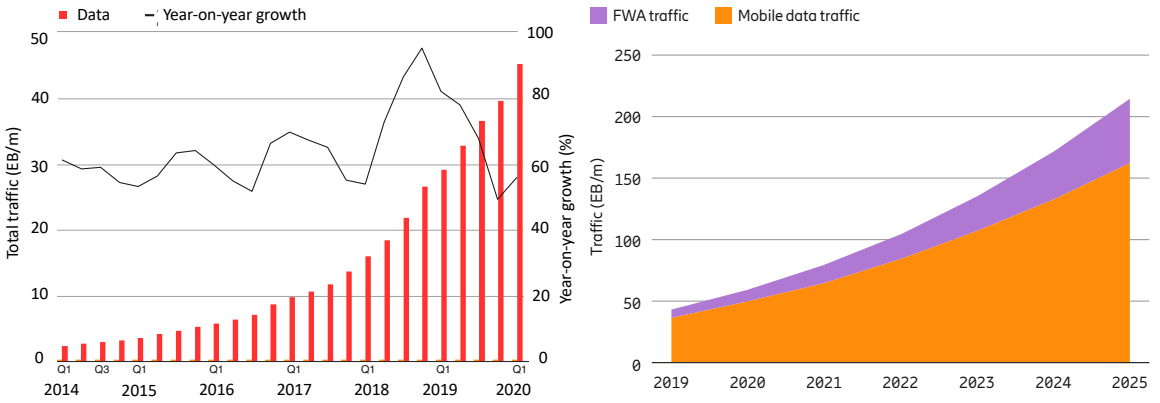
PCB	Printed Circuit Board	70
PDF	Probability Density Distribution Function	168
PLL	Phase-Locked Loop	48
PM	Phase Modulation	9
PSD	Power Spectral Density	52
PSRR	Power Supply Rejection Ratio	75
PRBS	Pseudo Radom Bit Stream	100
PVT	Process, Voltage, Temperature	173
QAM	Quadrature Amplitude Modulation	14
QFN	Quad Flat No-Leads (IC package)	96
QPSK	Quaternary Phase-Shift Keying	100
RF	Radio Frequency	9
RF-DAC	Radio Frequency Digital-to-Analogue Converter	23
RMS	Root Mean Square	135
RRC	Root Raised Cosine	14
RX	Receiver	
SAR	Successive Approximation Register	18
SFDR	Spurious-Free Dynamic Range	12
SMD	Surface Mounted Device (on PCB)	
SNR	Signal-to-Noise Ratio	12
SSB	Single Side-Band	20
TX	Transmitter	
VCO	Voltage-Controlled Oscillator	22
VSA	Vector Signal Analyser	133

Chapter 1

Introduction

Mobile communication is an indispensable part of our society. The demanded mobile data rate and the number of end user devices continue to grow exponentially. Fig. 1.1 depicts the trend of the mobile data traffic in exabytes per month for the last 7 years, as stated in the Ericsson mobility report from 2020 [1]. The year-on-year growth until today is in average approximately 60%. Based on this trend, Fig. 1.1b predicts the increase of the mobile and Fixed Wireless Access (FWA) traffic within the next 5 years, where the mobile traffic is expected to almost quadruple.
In order to satisfy the markets demands, upcoming mobile communication standards such as 5G combine a wide variety of wireless communication applications which previously have been defined separately, within a single standard definition [2]. Thereby, a multitude of modulation schemes, bandwidths, and carrier frequencies shall be covered in modern hand-held devices. Moreover, the mobile communication moves to higher frequencies, where a wide bandwidth can be allocated in order to attain the required high data rates. However, the 5G standard foresees various transmit frequencies such as the sub-6 GHz range with the intention to ensure rural coverage, whereas in urban

areas the communication bands in the 28 GHz range are utilised in order to allocate a wide modulation bandwidth and, hence, achieve high data rates [3]. Despite that, in areas of high population density, the capacity restrictions of 28 GHz 5G frequencies can be overcome by the introduction of high performance indoor access points, so called femto-cells [4], in the 60 GHz range as stated in the *802.11ad* standard [5].
Mobile devices need to follow the trends set by the market. Therefore, the number of functionalities as well as the performance of the wireless transmitters have to be increased while being able to be fit in a small form factor with a reasonably low power consumption. In this regard, new transmitter topologies need to be developed which are able to achieve a very wide modulation bandwidth and high data rates while being fully integrated, ideally, in a single IC. At the same time, these transmitters shall support a multitude of modulation bandwidths from megahertz to gigahertz range as well as various transmit frequencies frequencies up to 60 GHz.



(a) Mobile data traffic trend in the past including the year-on-year growth [1].

(b) Forecast for the global mobile data traffic and FWA traffic growth [1].

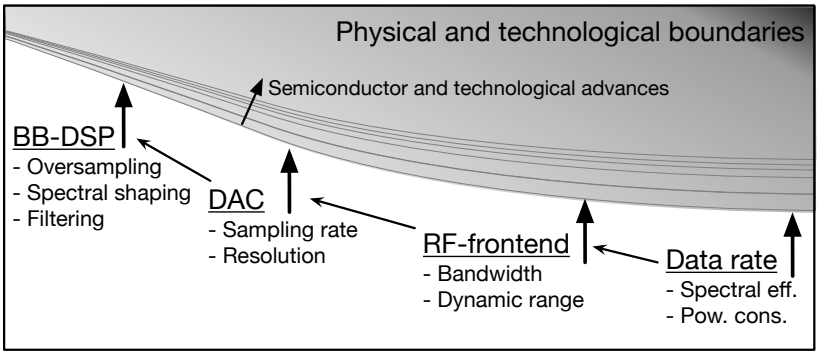
Figure 1.1: Trends of mobile data traffic in the past and forecast for the future.

In the last decades, integrated digital circuits have significantly benefitted from the advances in complementary metal-oxide-semiconductor (CMOS) scaling. Functionality densities and operating frequencies have been heavily increased, while - by additionally reducing the supply voltage - the power consumption per operation largely decreased. Consequently, many functions, which were performed in the analogue domain before, have been moved into the digital domain. With this shift of functionalities to digital, the requirements on the key components of integrated transmitters increased simultaneously: the data converters, i.e. the Digital-to-Analogue Converter (DAC) and Analogue-to-Digital Converter (ADC).
In wireless communication systems the digital baseband data is translated into the analogue domain and modulated onto a carrier frequency in order to be transmitted. A typical DAC-based transmitter requires preprocessed digital baseband signals in order to comply with the given specifications of the specific standard regarding spurious

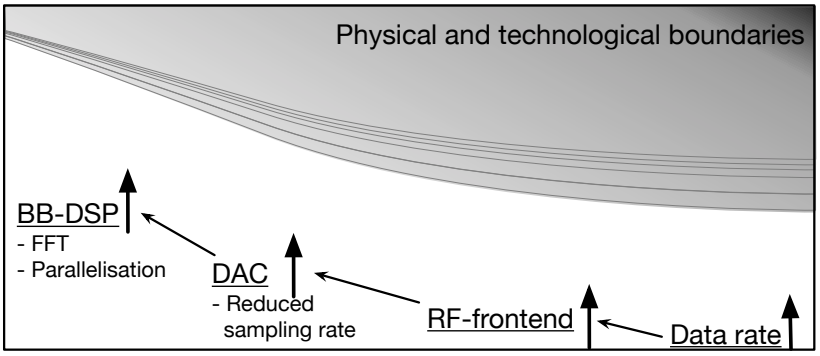
emissions [6]. Therefore, oversampling and filtering of the digital baseband signal is necessary [7]. This increases the sampling rate of the DACs which becomes a bottleneck, especially, for high coherent bandwidths in the gigahertz range. Accordingly, the Digital Signal Processing (DSP) needs to operate at extremely high sample frequencies, thus modern transmitters require an additional optimised DSP chip alongside with the analogue transmitter frontend [8]. For a baseband bandwidth in the gigahertz range, the digital filters need to be clocked in the order of multiple gigahertz. High sampling rates come along with increased power consumption, larger chip area, and especially increased circuit complexity due to the extremely demanding timing requirements.
There are several approaches to increase the sampling rate of a DAC. A commonly used approach is time interleaving which utilises N DAC cores, where each operates at a sampling rate of $1/N$ [9]. The interleaving architecture increases the requirements regarding the timing between the several DAC cores and requires extremely low jitter clock signals. Even though there are DACs with sufficient sampling rate, the performance of the dedicated DSP for spectral shaping remains an additional bottleneck.
State-of-the-art high-speed transmitters provide an Adjacent Channel Leakage Ratio (ACLR) of up to $-80\,\mathrm{dBc}$ when the transmit bandwidth is limited to a few tens of megahertz [10]. If the bandwidth is increased to several gigahertz, the dynamic range decreases rapidly, and in return the achievable ACLR falls below $-30\,\mathrm{dBc}$ [11]. Fig. 1.2a depicts the relation of the components in the transmitter chain. In order to increase the data rate, all building blocks within the chain need to be improved. There are conventional transmitter topologies and DACs which can achieve wide modulation bandwidths, although these are based on "brute-force" methods with extreme complexity, high power consumption, and high production cost [7, 8, 12, 13]. Furthermore, their development depends on the advances in CMOS technologies. Therefore, wireless transmitters for 5G and beyond standards, which support a tremendously wide modulation bandwidth and transmit frequencies from several hundred megahertz up Millimetre-Waves (mmW)s, can only be implemented at the cost of significant trade-offs when conventional transmitter topologies are used.

1.1 Goal and contribution of this work

The aim of this work is to develop a new type of wireless communication transmitter based on a novel data converter concept which breaks through the technological limitations and boundaries being faced by conventional approaches. This concept exploits the properties of the continuous Fourier transform to convert a wideband arbitrary signal with high resolution from the digital to the analogue domain.
The evolution in today's mobile communication devices is limited by technological and physical boundaries. Therefore, the achievable data rate from generation to



(a) State-of-the-art transmitters operate at the edge of technological limitations.



(b) FDDAC approach relaxes the operation speeds of the blocks in the complete transmitter chain.

Figure 1.2: Design space of conventional transmitters operating at technological limitations versus the proposed FDDAC technique.

generation evolves depending on technological advances in minor steps while the complexity, cost and the power consumption steadily increase. The Fourier-Domain Digital-to-Analogue Converter (FDDAC) based data conversion concept, introduced in this thesis, exploits the properties of the continuous Fourier transform to convert a wideband signal with high resolution from the digital to the analogue domain. It is able to output an arbitrary signal at virtually any carrier frequency while reducing the sampling frequency as well as the digital and analogue signal processing and filtering requirements by up to two orders of magnitude. Moreover, it eliminates the necessity of oversampling and digital filtering while sustaining spectral shaping. The concept fundamentally changes the transmitter chain which allows a tremendous performance boost for the same technological and physical boundaries compared to state-of-the-art transmitter architectures, as shown in Fig. 1.2b. Thus, it allows converting ultrawideband signals while substantially reducing the required power. This approach is developed, thoroughly analysed, and proposed for the first time in this thesis. It is implemented in a fully integrated transmitter that is able to

generate a wide modulation bandwidth of up to 2 GHz allowing extremely high data rates of up to 12 Gbit/s. The complete transmitter including the baseband processor and the analogue-mixed-signal components are cointegrated on the same Integrated Circuit (IC) in a well established and commercially available 65 nm CMOS technology. Furthermore, the FDDAC-based transmitter is able to replace a multitude of dedicated narrowband transmitters in order to cover different communication standards and worldwide frequency bands. In addition to the FDDAC-based transmitter topology, two mmW upconversion circuits are comprehensively investigated, implemented and characterised. By combined measurements with the FDDAC-based transmitter ICs and the implemented upconversion circuits, it is demonstrated that wide modulation bandwidths allowing extreme high data rates can be achieved in the frequency ranges below 6 GHz, in the 5G frequencies around 28 GHz, and in the ISM band at 60 GHz. This work is expected to have a substantial and far-reaching impact in the fields of integrated circuits and future communications. Besides, it contributes to a substantial reduction in power consumption and production prices and, hence, on the availability of transmitters and their application. It, therefore, has a profound impact on how people will communicate and interact with each other.

1.2 Thesis outline

This work is structured as follows:

- Chapter 2 presents a brief overview on the fundamentals of wireless communication systems. The conventional transmit and receive chains are analysed in order to localise their systematic limitations and bottlenecks.

- Chapter 3 introduces the FDDAC approach adapted in a transmitter system which aims to overcome the systematic bottlenecks and limitations of state-of-the-art transmitters. The principle of the proposed approach is derived mathematically in a general form in order to analyse its spectral shaping capabilities and the achievable performance. Furthermore, a system-level model of a multistandard prototype is presented which is able to generate a modulation bandwidth of up to 2 GHz in the sub-6 GHz range that can be upconverted to mmW frequencies if required. The required baseband data processing is presented and analysed. A system model of the prototype is implemented in order to analyse the effects of the nonidealities of the utilised subblocks on the complete transmitter system. Thereby, a design space exploration is carried out and the specifications of the requires subblocks are derived in order to achieve a reasonable transmitter performance.

- Chapter 4 presents the first hybrid prototype transmitter based on discrete off-the-shelf components employing the proposed technique. The signal processing for the FDDAC approach is performed on an FPGA. It demonstrates the feasibility and advantages of the proposed approach and delivers a first proof-of-concept.

- In Chapter 5, the challenges towards the CMOS integration are analysed. The FDDAC approach requires simultaneous generation of equidistantly spaced frequencies. Therefore, several frequency synthesis approaches are analysed. Furthermore, the cointegration of the analogue-mixed-signal components alongside with the DSP is discussed. The integrated DSP shall provide the complete baseband signal processing in order to omit any necessity for high-speed interfaces.

- Chapter 6 presents the first integrated FDDAC-based transmitter in a standard 65 nm CMOS technology which demonstrates a data rate of up to 4 Gbit/s and a modulation bandwidth of up to 2 GHz. The implementation of the complete transmitter including the floor plan, integrated DSP, and RF-DAC based I/Q transmit cores is presented in detail. The IC is packaged and mounted on a PCB, whereas, the output is characterised through on-wafer probing. The measurement results of two different ICs are presented, whereas the second design contains improved frequency synthesis blocks and achieves outstanding performance.

- In Chapter 7, a power efficient, high performance, and high output power FDDAC-based transmitter is presented. This is achieved by a structural change in the I/Q transmit cores which are based on individual DACs, mixers, and output amplifier buffers instead of RF-DACs. Furthermore, the output-biasing is integrated on-chip and the differential output is bonded such that it can be accessed over the PCB instead of using on-wafer probing. A data rate of up to 8 Gbit/s is demonstrated.

- Chapter 8 introduces the implementation of two mmW upconversion mixers in 65 nm CMOS for the frequency ranges of 28 and 60 GHz. These upconversion mixers are specifically designed to be integrated alongside with the sub-6 GHz FDDAC-based transmitter. Both mixers are fully characterised by on-wafer measurements and demonstrate outstanding performance. Furthermore, the transmitter presented in Chapter 7 is measured in combination with the 28 GHz mixer.

- Chapter 9 highlights the achievements of this thesis and draws a conclusion. Furthermore, a brief outlook on the possible future research, potential improvements, and application areas are discussed.

Chapter 2

Fundamentals of wireless communication systems

This chapter gives an overview on modern wireless telecommunication systems implemented in Complimentary Metal-Oxide-Semiconductor (CMOS) with regard to wideband modulation and channel effects. The main emphasis is laid on the transmitters from the perspective of an analogue-mixed-signal circuit designer. The fundamentals, basic principles, system-theoretical, and mathematical explanations of conventional state-of-the-art transmitters are presented. Thereby, the transmitter and receiver chains are partially analysed. Based on the presented analyses of the fundamentals, the systematic bottlenecks and limitations of common state-of-the-art transmitters are localised and understood. This thesis introduces the Fourier-domain data-conversion technique as a new class of data converters which aims to overcome those limitations and bottlenecks allowing extremely wide modulation bandwidth and data rates with a competitively high spectral efficiency.

2.1 Fundamentals of modern wireless transceivers

A wireless transceiver transmits and receives information over a distance via electromagnetic waves. This requires a certain channel bandwidth in the frequency spectrum which is a finite resource and is shared by several communication standards. In order to enable the simultaneous and interference-free operation of multiple services, there are strict regulations which define the usable frequency band, maximum transmit power, maximally allowed transmission power out of the band, *etc.* These specifications are derived and controlled by governmental organisations, *e.g.* the *International Telecommunication Union* (ITU) worldwide, the *Federal Communications Commission* (FCC) in the USA, or the *Bundesnetzagentur* (BNetzA) in Germany. Fig. 2.1 shows the spectral mask of the *IEEE Std. 802.11ad* standard for the 60 GHz ISM band for very high throughput communications [5]. There are four communication channels each providing a bandwidth of 2160 MHz. The spectral mask defines the maximum allowed transmit power inside and outside the corresponding frequency band. In this example, the spectral mask has a steep decay of 17 dB within the 260 MHz guard space between two channels. Thereby, the leakage of spectral power to the neighbour channel is limited. The out-of-band spurious emissions are limited to 30 dB less than the relative transmit power. The physical layer of the standard utilises a modulation bandwidth of 1.76 GHz in the single-carrier mode for the given spectral mask preserving 400 MHz guard space between two channels.

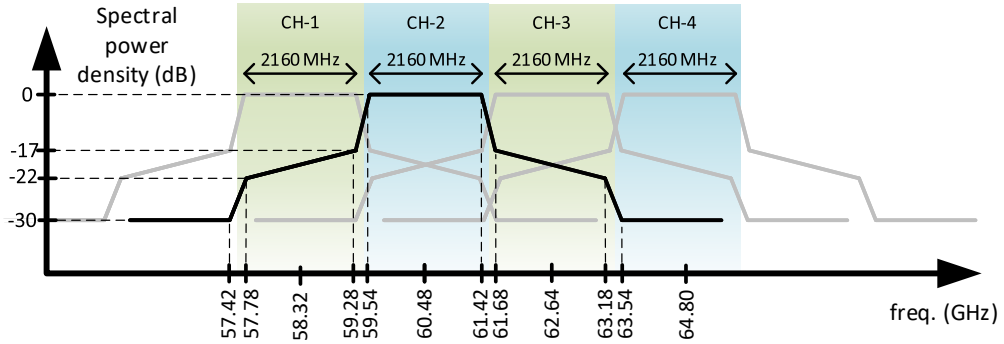


Figure 2.1: Spectral emission mask of the *IEEE Std. 802.11ad* standard for the 60 GHz ISM band.

In general, the information to be transmitted is available as a series of logic states in a digital form, namely a bit-stream. The sequence of these bits is translated into a sequence of symbols which have a distinguishable representation in the analogue domain. The amplitude, phase, or frequency of a analogue voltage or current signal can be changed in order to map the symbols to an analogue representation. The signal that carries the information is then sent wirelessly via electromagnetic waves travelling through a channel that might have changing conditions. At the receiver side, the

electromagnetic waves effected are received and the symbols which were previously mapped to the frequency, phase, or amplitude are reconstructed. Consequently, the received symbol sequence is used to reconstruct the initial bit-stream. A typical transmitter chain contains digital, analogue-mixed-signal and Radio Frequency (RF) or Millimetre-Waves (mmW) block. Conventionally, the baseband signal is processed in the digital domain. The analogue-mixed-signal blocks perform the conversion from the digital to the analogue domain. The RF or mmW frontend converts the frequency of the signal to the desired communication band and amplifies it so that the signal can be fed to the antenna. It sends the electromagnetic waves through the channel. On the receiver side, the chain operates in the reverse order.

2.1.1 Digital modulation and baseband signal processing

A digital modulator maps the initial bit-stream onto a sequence of symbols s_i of a certain modulation scheme M as shown in Fig. 2.2.

$$s_i \in M : \{s_1, s_2, s_3, ...s_N\} \tag{2.1}$$

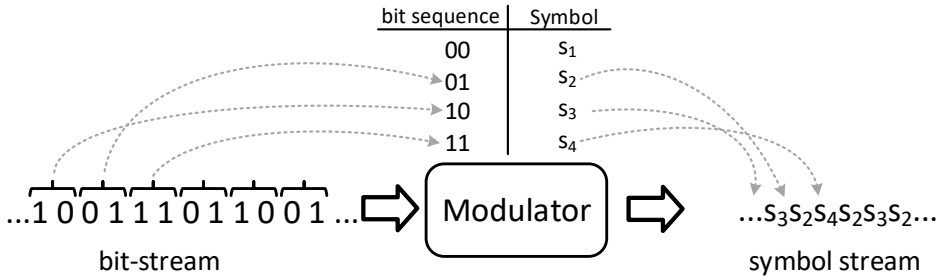
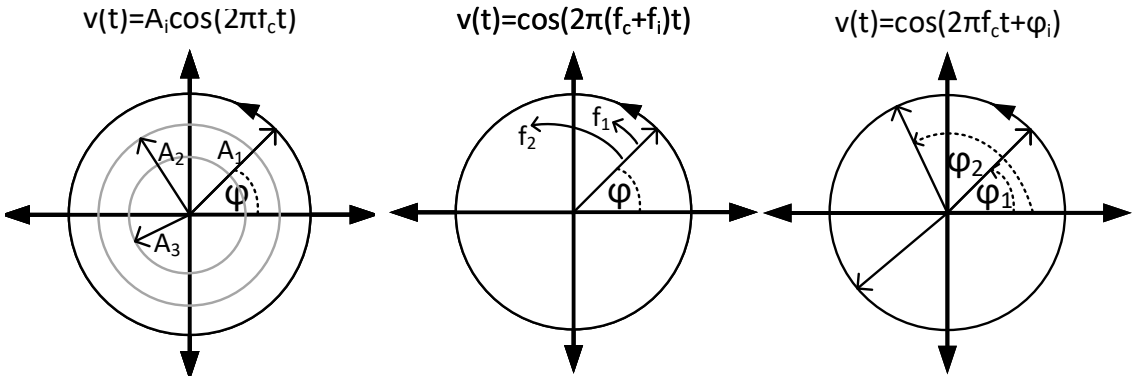


Figure 2.2: Bit-stream mapped to a modulation scheme with four symbols.

The amount of information in terms of bits carried by a single symbol is $\log_2(N)$ where N is the number of available symbols in the used scheme. The symbols are used to modulate the transmit signal. Fig. 2.3 shows different properties of a transmit signal which can be changed in order to have distinguishable representations for each symbol. The modulation type shown in Fig. 2.3a is the Amplitude Modulation (AM) where the amplitude of a signal at the carrier frequency is varied. There is a defined amplitude level for each symbol in the modulation scheme. In Fig. 2.3b the Phase Modulation (PM) is illustrated. Here, the symbols are mapped to the phase of the signal. The phase of the carrier frequency is shifted depending on the symbol being transmitted. Lastly, the Frequency Modulation (FM), as shown in Fig. 2.3c, changes



(a) Amplitude modulation. (b) Frequency modulation. (c) Phase modulation.

Figure 2.3: Modulation types visualised by a phasor at the carrier frequency, f_c.

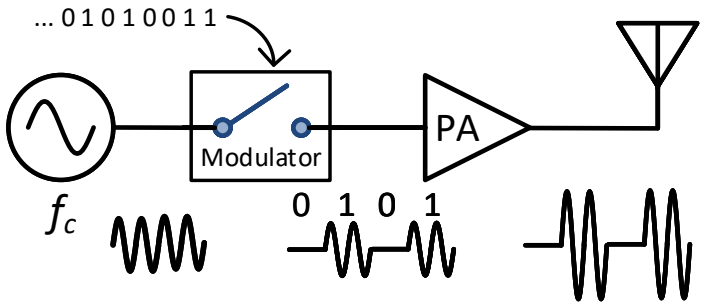


Figure 2.4: Simplified block diagram of the OOK transmitter.

the actual transmit frequency depending on the symbols. On-Off Keying (OOK) as a modulation scheme is the simplest form of AM. The modulation scheme provides two symbols and, hence, two amplitude levels, where each symbol carries a single bit of information. Logic high or low states are distinguished by the existence or lack of the transmitted signal. On the receiver side, a bit-stream is regenerated by demodulating the symbol sequence. Fig. 2.4 shows a block diagram of a simplified OOK transmitter which can be implemented with a comparatively low number of blocks and complexity. The transmitter does not require a special baseband signal processing. A frequency source generates the carrier frequency, f_c, which is fed to a switch. The bit-stream modulates the switch which leads to the two amplitude levels. The symbol rate, f_{symb}, equals the bitrate since the information per symbol is 1 bit. The modulator operates as a mixer and zero-order hold Digital-to-Analogue Converter (DAC) which converts the bit-sequence into the analogue domain and multiplies it with the carrier frequency. The symbol sequence in the baseband is a band-limited real signal with the sampling rate of f_{symb}. The Nyquist rate, f_{Nyq}, is half the sampling rate. The spectrum of a real signal is mirrored across the y-axis. Thus, the information in the positive and negative frequency components is identical. The DAC changes the representation of the signal

in the frequency-domain besides performing the digital-to-analogue conversion. The digital signal is present in a sampled and band-limited domain, whereas the analogue one is a continuous-time signal without a band limitation. The zero-order hold DAC keeps the amplitude of the signal constant for the duration of the hold time, T_h, which changes the shape of the signal. Consequently, a transfer function for the zero-order hold block can be derived as mentioned in [14]. The impulse response of the transfer function can be found by multiplying a Dirac delta sequence with the function, $h(t)$:

$$h(t) = \begin{cases} 1, & 0 < \mathrm{t} < T_h \\ 0, & t < 0 \text{ and } t > T_h \end{cases}. \tag{2.2}$$

The switch which operates as a DAC in this particular case, usually keeps its output constant until a new input is sampled. This leads to $T_h = T_{symb}$. Thereby, the frequency-domain transfer function, $H(\omega)$, can be given by a Fourier transform of $h(t)$:

$$H(\omega) = \int_{t=0}^{t=\infty} h(t)\mathrm{e}^{-j\omega t}\mathrm{d}t = \frac{1}{T_{symb}} \int_{t=0}^{t=T_{symb}} 1\mathrm{e}^{-j\omega t}\mathrm{d}t = \frac{\sin(\pi f T_{symb}))}{\pi f T_{symb}}\mathrm{e}^{-j\omega t/2}. \tag{2.3}$$

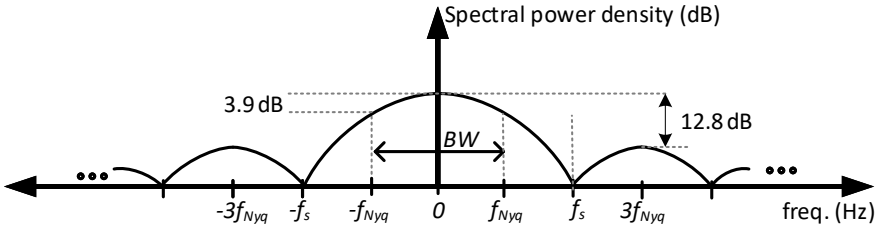


Figure 2.5: Spectral power density of the OOK signal shaped by the transfer function of the zero-order hold digital-analogue converter.

Fig. 2.5 shows the spectral power density of the random OOK symbol sequence in the analogue domain after sample-and-hold. The random baseband signal which corresponds to a digital white noise is transformed by the transfer function of the sample-and-hold block. The impulse response of a sample-and-hold block in the frequency-domain is a *sinc* function with $\mathrm{sinc}(x) = \sin(x)/x$. The characteristics of the *sinc* function depend on the hold time and sampling rate. The amplitude of the signal is attenuated by 3.9 dB at the Nyquist frequency compared to DC which is the centre of the band. Moreover, the attenuation has maxima at even multiples of the Nyquist frequency, f_{Nyq}, and the first side-lobe is attenuated by 12.8 dB relative to the signal power at DC. Fig. 2.6 shows the spectral power density after the frequency upconversion. The Nyquist replicas of the digital signal are *sinc* shaped but still present in the analogue domain which leads to a broad transmit signal bandwidth. All Nyquist

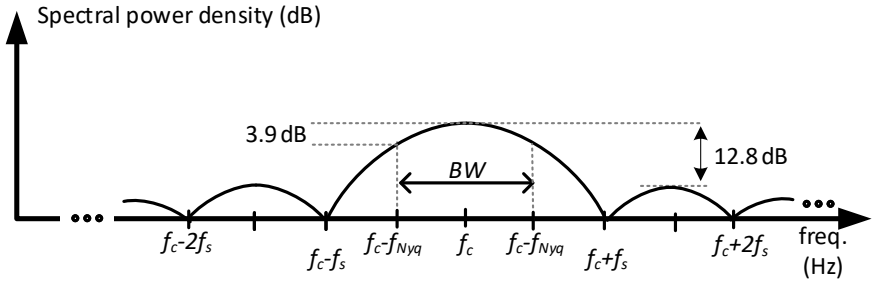


Figure 2.6: Spectral power density of the OOK signal sequence after the upconversion to the carrier frequency f_c.

replicas carry the same information, although they occupy a tremendous bandwidth. Thus, the spectral efficiency, η_{TX}, of an OOK transmitter is relatively low which is measured in bits per second per hertz of utilised bandwidth:

$$\eta_{TX} = \frac{d\ (\text{bit/s})}{\text{BW}\ (\text{Hz})}. \tag{2.4}$$

Besides the spectral efficiency, the Hartley-Shannon criteria (2.5) sets an upper boundary for the channel capacity in a noise-limited environment where S is the signal power and N is the noise power.

$$C = \text{BW} \log_2 \frac{S}{N} \tag{2.5}$$

Consequently, the baseband symbol sequence with a limited bandwidth can be transmitted without loss of information by using the same limited bandwidth in the analogue domain as well as in the channel. Thereby, the finite frequency spectrum can be used more efficiently. Another term used in this context is the Adjacent Channel Leakage Ratio (ACLR) which defines the signal power leaked to the neighbour channel which is placed next to the actual band. In this particular case utilising the sample-and-hold transfer function, the power of the transmit band at the edge of a neighbour channel is 3.9 dB less than transmit signal power. They disturb each other by reducing their in-band Spurious-Free Dynamic Range (SFDR) to 3.9 dB considering both channels transmitting at the same power level. This drastically reduces the Signal-to-Noise Ratio (SNR) in both transmit bands and, hence, reduces the channel capacity significantly.

The signal power is concentrated in the actual bandwidth and the Nyquist replicas need to be attenuated in order to increase the spectral efficiency. This is achieved by Digital Signal Processing (DSP) performing oversampling and filtering. Fig. 2.7 shows the spectrum of the baseband signal after the oversampling and filtering steps. The grey underlaid area shows the bandwidth limitation caused by the finite sampling rate. The arrows outside the greyed areas show the replicas which are mirrored versions of the actual signal. By zero padding and oversampling, the initial information of the

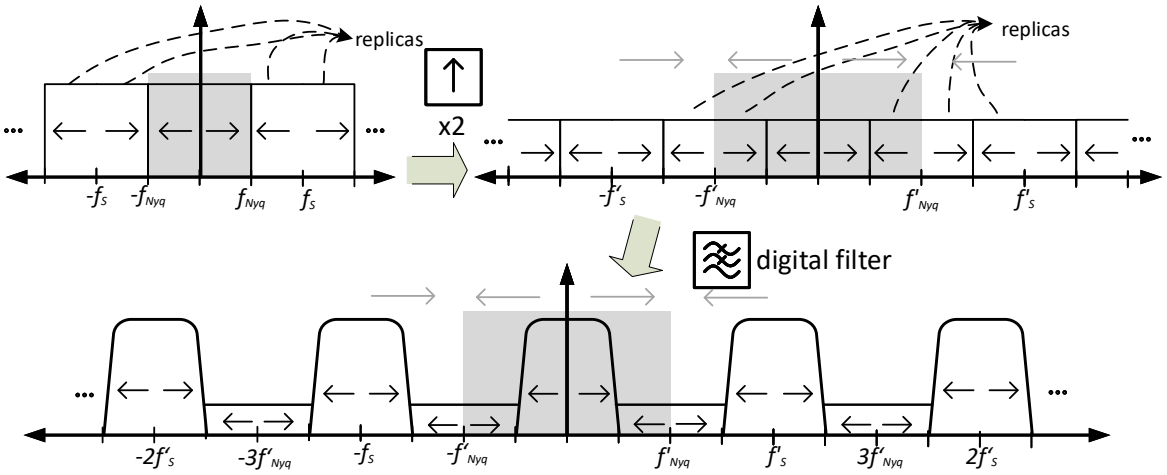


Figure 2.7: Baseband signal processing with oversampling and filtering and their visualisation in the frequency-domain.

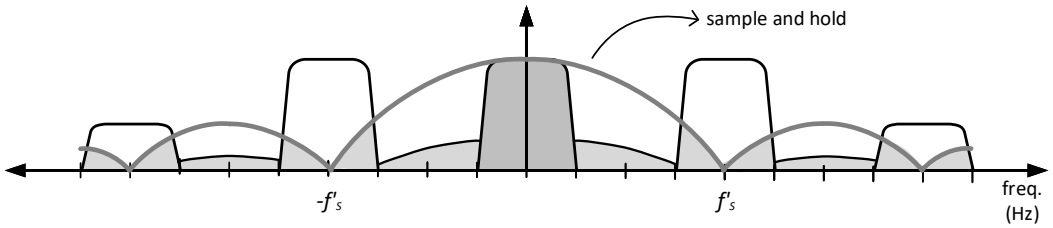


Figure 2.8: Spectrum of the processed baseband signal after sample-and-hold.

signal is not changed, although the band limitation is shifted to higher frequencies with the same factor as the Over-Sampling Ratio (OSR). With the increased sampling rate and the shifted Nyquist frequency, a digital filter can be utilised shaping the signal in the extended and greyed area. Accordingly, a low-pass filter is used to attenuate the replicas. However, a digital filter is implemented with regard to a normalised sampling frequency. The filter characteristic is mirrored at the Nyquist rate as well and it repeats itself. Therefore, the digital filtering of the baseband signal applies only in the Nyquist range. Thus, there are still Nyquist replicas of the transmit band which are further attenuated by the transfer function of the sample-and-hold behaviour of the DAC. Fig. 2.8 shows the spectral power density of the oversampled and filtered baseband signal after the DAC. The *sinc* shaping additionally reduces the out-of-band emissions which can be filtered out by an analogue filter. However, a high OSR moves the Nyquist replicas to higher frequencies so that the analogue filter specifications are relaxed. On the other hand, a high OSR increases the DSP and DAC sampling speed which creates new bottlenecks, especially for wide bandwidth applications. A modulation bandwidth in the gigahertz range, *e.g.* 2 GHz and a reasonable OSR of 4 consequently requires digital filters and DAC sampling speeds of 8 Gbit/s.

On the receiver side, an additional filter is required to isolate the receive band and attenuate any other signal power outside the band. Therefore, a series of analogue and digital filters with different properties such as channel and band filtering are used. Both the digital filters applied in the transmitter and receiver shall be matched to each other in order to provide a flat frequency response. Therefore, Root Raised Cosine (RRC) filters are utilised. By filtering the signal twice in the transmitter and in the receiver with a RRC filter, the obtained overall transfer function equals to a raised cosine filter which results in a flat frequency response.

2.1.2 Complex modulation

The baseband symbol sequence considered so far is a real valued signal modulating the amplitude, phase, or frequency of the carrier signal. A real signal carries the same information on the positive and negative frequency components. Thus, in case of the OOK transmitter example, the left and right hand side of the transmit band contains the same information. Consequently, the channel capacity for a given frequency band is not fully utilised. A complex-valued baseband signal contains symbols, $\underline{s}[k]$, with a complex value:

$$\underline{s}[k] = A_I[k] + jA_Q[k] \text{ with } k \in \mathbb{N}, \tag{2.6}$$

where A_I and A_Q are the amplitudes of the real and imaginary parts. The amplitude modulation of two different signal types, namely real and imaginary, spans a two dimensional plane in which the symbols are placed. The symbols contain the imaginary unit, j, which equals to $e^{jpi/2}$,*i.e.*, a phase shift of 90°. Thereby, the real signal defines the x-axes and the imaginary part the y-axis, respectively. This modulation scheme in general is referred to as I/Q modulation. Depending on the number of symbols, there are different Quadrature Amplitude Modulation (QAM) orders. Fig. 2.9 shows the constellation diagram of 16QAM. Furthermore, the symbols of other modulation schemes such as AM, PM, and FM can be mapped to the QAM plane. Alternatively, the complex symbols can be represented by a polar expression with an amplitude, A, and a phase, ϕ. It is a combination of AM and PM:

$$\underline{s}[k] = A[k]e^{j\phi[k]}. \tag{2.7}$$

The modulation of complex symbols on a carrier signal can be performed by several methods. Consequently, a polar modulator as shown in Fig. 2.10 modulates the carrier signals amplitude and phase at two different points. However, a crucial challenge is the timing mismatch approximated by τ in the block diagram since the amplitude and the phase corresponding to a symbol shall be set in the same time. Another and a more common modulation technique is based on the Cartesian representation of the symbols.

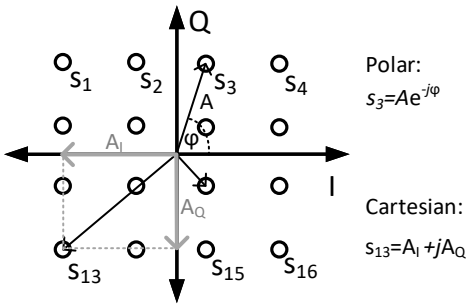


Figure 2.9: Constellation diagram of a 16QAM scheme.

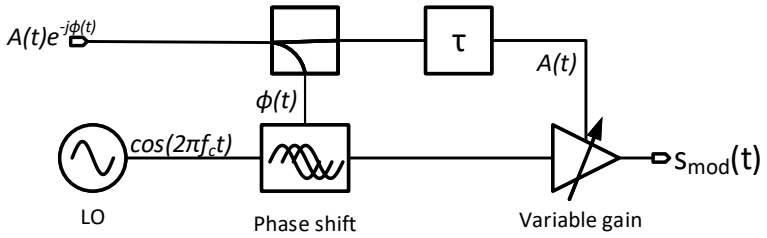


Figure 2.10: Simplified block diagram of a polar transmitter with two point modulation; phase modulation and amplitude modulation.

The complex baseband symbol sequence in the continuous-time can be calculated by multiplying the digital symbol sequence by a series of Dirac impulses with a spacing of T_{symb}. These Dirac impulses are convolved the function $h(t)$:

$$\underline{s}(t) = I(t) + jQ(t) = \left(\sum_{k=0}^{\infty} \underline{s}[k]\delta(t - kT_{symb}) \right) * h(t), \tag{2.8}$$

where I and Q are the amplitudes of the real and imaginary signal. The carrier signal, $\underline{s}_c$, at the frequency, f_c, is represented in the complex domain as a phasor:

$$\underline{s}_c(t) = \mathrm{e}^{j2\pi f_c t} = cos(2\pi f_c t) + j\sin(2\pi f_c t). \tag{2.9}$$

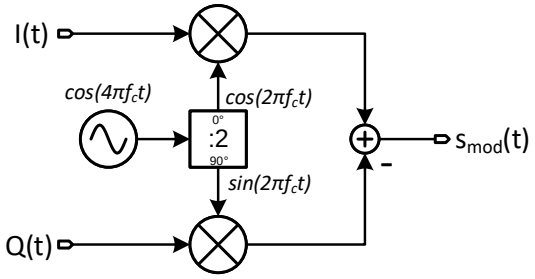


Figure 2.11: Block diagram of an IQ modulator.

The upconversion of the complex baseband signal to the carrier frequency is calculated by a multiplication with the complex representation of the carrier signal. Thereby, the complex valued upconverted signal is:

$$\begin{aligned} s_c(t) &= \mathrm{e}^{j2\pi f_c t}[I(t) + jQ(t)] \\ &= I(t)cos(2\pi f_c t) + jI(t)\sin(2\pi f_c t) + jQ(t)cos(2\pi f_c t) - Q(t)\sin(2\pi f_c t). \end{aligned} \tag{2.10}$$

A transmitter only transmits the real part of the signal. Thus, the real part of the given expression fully defines the transmit signal.

$$\Re(\underline{s}_c(t)) = I(t)cos(2\pi f_c t) - Q(t)\sin(2\pi f_c t) \tag{2.11}$$

With the given expression, an I/Q transmitter can be implemented by utilising two AM transmitters which use Local Oscillator (LO) signals with a 90° phase shift in order to implement the *sines* and *cosines* terms. Fig. 2.11 illustrates a simple implementation of the I/Q modulator. The baseband signals $I(t)$ and $Q(t)$ are digitally processed and converted into the analogue domain. The multiplication with the LO is carried out by two mixers for the in-phase I and quadrature Q signal.
The complex valued baseband is filtered by an appropriate complex valued digital baseband filter for spectral shaping as described in the Section 2.1.1. Digital signal processing for complex valued signals requires at least a doubling of the digital blocks processing speed. Additionally, cross coupling between the real and imaginary signals might further increase the number of operations and blocks required in the digital domain.

2.1.3 Digital-to-analogue converters

The digital-to-analogue converter is one of the core components used in a wide variety of electronic devices where information is processed and stored digitally. Especially in wireless transmitter systems, the DACs need to fulfil certain specifications. Depending on the modulation type, digitally processed phase and/or amplitude information is translated into the analogue domain. In case of the I/Q transmitter, two DACs for the in-phase and quadrature signal paths are required. In communication systems, the modulation bandwidth and modulation order can be increased in order to achieve higher data rates. In turn, the sampling rate and the dynamic range of the DACs need to be enhanced. The dynamic range of a DAC is limited by multiple factors. A digital signal is usually represented in a binary form where each word contains a certain number of bits, i.e. the resolution. The resolution in digital systems is limited which leads to a quantisation error when converted into the analogue domain and vice

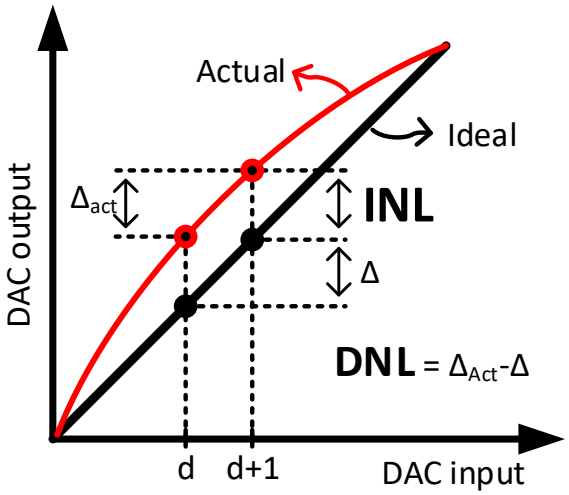


Figure 2.12: DAC input vs. output showing DNL and INL effects.

versa. The quantisation error reduces the SNR which can be calculated as follows:

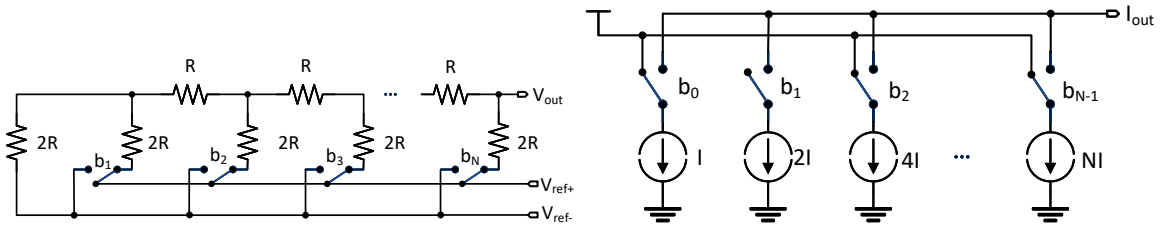
$$\text{SNR} = 6.02N + 1.761, \tag{2.12}$$

where N is the resolution in effective number of bits. The performance of a DAC is effected by several error sources which can be divided in two groups, namely static and dynamic errors. All nonidealities which appear while a constant input is set and the DAC output is at DC are considered static errors. Ideally, the output signal linearly follows the digital input code. Hereby, each LSB increment of the input word with a word-length of N corresponds to a voltage increment of $\Delta V_{LSB} = V_{FS}/(2^N)$ where V_{FS} is the full-scale voltage swing at the output. Deviations from this ideal curve are measured by the Integral Nonlinearity (INL) and the Differential Nonlinearity (DNL). As illustrated in Fig. 2.12, DNL compares the increment per LSB in the digital input with the actual increment in the output voltage ΔV_{act}. The DNL is calculated for each input increment by $\Delta V_{act} - \Delta V_{LSB}$. Ideally the DNL equals to zero. On contrary, the Integral Nonlinearity (INL) is defined by comparing the generated DAC output to a linearised approximation with infinite quantisation steps. Thereby, the INL of an ideal DAC, with a limited number of quantisation steps, moves between $-0.5 \times \Delta V_{LSB}$ and $0.5 \times \Delta V_{LSB}$. The discussed static errors caused by a multitude of mechanisms lead to a reduction of the Effective Number of Bits (ENOB) compared to the implemented resolution in an ADC or DAC. The ENOB can be calculated as follows, [15]:

$$\text{ENOB} = resolution - \log_2(\max(INL_{max}, DNL_{max})) - 1. \tag{2.13}$$

The dynamic errors describe nonidealities which appear while the DAC operates at a

certain sampling speed with varying input words. The SNR of a DAC can be limited by analogue thermal noise such that the noise power is larger than the power level of the least significant bits. This would cause the thermal noise floor being above the quantisation noise limiting the dynamic range. Distortions introduced by the DAC are measured by applying a digital sinusoidal input in so called single-tone measurement. Nonideal INL and DNL lead to distortion which, in turn, creates harmonics and, hence, reduces the SFDR. Additional dynamic error sources are glitches appearing while sampling a new input code or word dependent effects such as varying settling times.
In literature, there are several types of DAC implementations which generate an output signal based on voltage [16], current [17] or charge [18]. The simplest single-bit voltage based DAC is a switch connecting or disconnecting a voltage source to an output. The digital input is used to change the transfer characteristic, *e.g.* resistance of a device. Nonlinear devices such as transistors or diodes are commonly used as switches. In order to increase the number of bits, i.e. discrete voltage levels at the output multiple switches and voltage sources are required. Fig. 2.13a shows a voltage divider based R2R DAC [19]. The switches in the voltage divider are set based on the digital word. Accordingly, the output voltage represents the DAC input in the analogue domain. The integration of well-controlled resistances in modern CMOS technologies is impractical due to process variations and mismatch effects, thus resistive voltage divider based DACs have several disadvantages. To overcome those disadvantages, calibration techniques and error correction methods need to be applied. Therefore, the integration of resistor based DACs consumes high chip-area, delivers bad matching and does not scale well with the technology [15]. Another disadvantage is the limited switching speed reducing the sampling rate. Charge based architectures successively integrate certain amounts of charge on a capacitor which corresponds to a voltage. After the integration step, the capacitance is connected to a buffering circuit, *e.g.* an operational amplifier which translates the charge into a voltage or current. The additional circuit is required to accomplish a high input impedance in order to not load the charge integrating capacitor. Successive Approximation Register (SAR)-DACs based on charge integration can deliver extraordinary resolution [15, 20]. Therefore, charge based DACs can be implemented with low area and power consumption. However, the required overhead of operation cycles such as integration and buffering limits the operation speed.
Fig. 2.13b shows a current-steering based DAC which generates a certain output current depending on the applied digital word which is transformed to a voltage using a resistor. The current sources are implemented by transistors where the output current of each cell is adjusted by sizing the transistors. Furthermore, the transistor as the main device in the CMOS technology scales with the feature size and enables performance increase with advances in the modern CMOS technology such as higher packing density. The process variations and the element matching can be controlled up to a certain level and further error correction and calibration methods can be applied. In [21], it is suggested to use binary-weighted current source cells implementing the DAC such that the bits of the digital word are directly applied to the switches. This method



(a) Simplified schematic of a R2R voltage divider based DAC.

(b) Simplified schematic of a current-steering DAC.

Figure 2.13: Integrated DAC types.

demands the minimum number of switches and simplified routing. However, the increment of one least significant bit in the input word might lead all bits to flip, *e.g.* the change from 01111 to 10000. This leads to a high switching activity and glitches might occur at the output creating an additional source of nonlinearity. Alternatively, unary sized current cells can be utilised. This approach requires signal processing on the digital input word, *i.e.* thermometer coder, in order to determine the actual number of current cells to be connected to the output. Thereby, the complexity and the routing overhead increases. As a trade-off, a segmented architecture can be used which involves a combination of binary and unary-weighted cells [22]. Transmitters targeting several gigahertz of modulation bandwidth require DACs with demandingly high sampling rates while proving a high dynamic range and linearity. However, the switching speed of transistors is constraint due to technological limitations. There are several approaches to increase the sampling rate of a DAC. A commonly used approach is time interleaving which enables the use of a number N of DAC cores, each of them operating at a sampling rate of $1/N$ [9]. The N DAC cores form in cohesion a time-interleaved DAC which can transmit a signal above the first Nyquist rate [23]. Nevertheless, the interleaving architecture further increases the restrictions regarding the timing between the several DAC cores and requires extremely low jitter clock signals. To overcome this problem, internal delay-correction structures and calibration algorithms have to be implemented.

2.1.4 Frequency upconversion circuits

The modulated analogue baseband signal around DC is shifted to the carrier frequency by an upconversion circuit, *i.e.* a mixer. In case of an upconversion mixer, two signals, namely the LO and IF are multiplied to generate the output signal. Fig. 2.14 shows the block diagram of a mixer and its single switch based implementation. Considering the LO signal as a sinusoidal tone, the switch conducts for the positive half wave and is nonconductive for the rest of the time. Thereby, both signals are multiplied. The

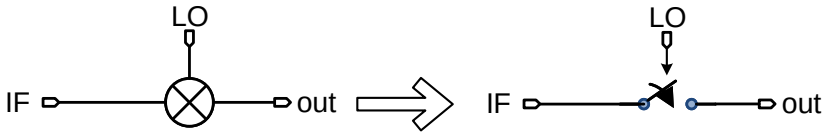


Figure 2.14: Simplified block diagram of a mixer and its single switch based implementation.

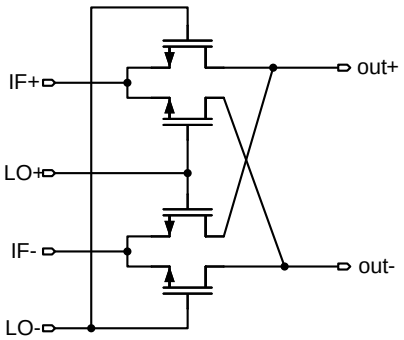


Figure 2.15: Schematic of a double-balanced passive Gilbert mixer, switches are replaced by transistors.

baseband signal fed to the IF input of the mixer has a certain bandwidth, in turn, it has frequency components greater than zero. For simplicity, the baseband signal is considered as a sinusoidal at the frequency, f_{IF}. The output of the mixer is calculated as follows:

$$out = k_1(t)\cos(2\pi f_{LO}t)k_2(t)\cos(2\pi f_{IF}t) \tag{2.14}$$

$$= \frac{k_1(t)k_2(t)}{2}\left[\cos(2\pi(f_{LO}-f_{IF})t) + \cos(2\pi(f_{LO}+f_{IF})t)\right], \tag{2.15}$$

where $k_1(t)$ and $k_2(t)$ are the amplitudes of the multiplied signal. The mixer generates two output components at the sum and difference of the two input frequencies, namely upper-side band (USB) and lower-side band (LSB). Considering the single-ended IF input has a DC offset, the mixing product with the LO leads to an additional signal besides the LSB and USB at the output. The so called LO feed-through defines the leakage of the LO signal power to the output. Differential signalling is commonly used to suppress DC offsets which leads to differential mixer structures compensating the LO feed-through. A famous example is the double-balanced Gilbert-cell as depicted in Fig. 2.15, [24]. It utilises a differential IF and LO inputs.
Single Side-Band (SSB) mixers are utilised for complex valued baseband signals or in order to reject the signal power at an image frequency. These mixers are based on the

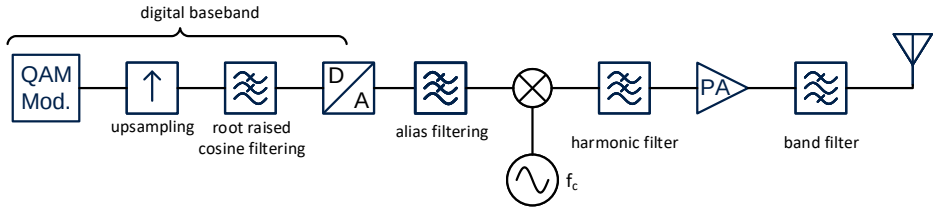
following trigonometric identities:

$$\sin(2\pi(f_{LO} \pm f_{IF})t) = \sin(2\pi f_{LO}t)\cos(2\pi f_{IF}t) \pm \sin(2\pi f_{IF}t)\cos(2\pi f_{LO}t), \quad (2.16)$$

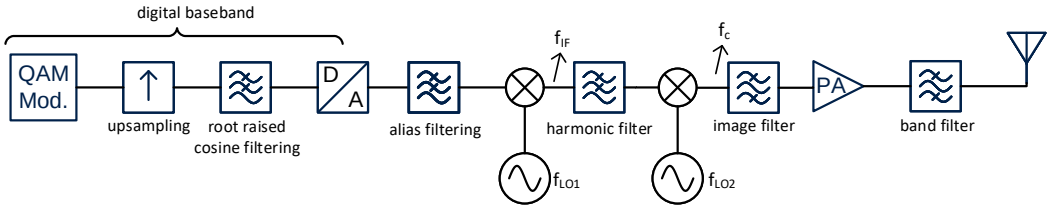
$$\cos(2\pi(f_{LO} \pm f_{IF})t) = \sin(2\pi f_{LO}t)\sin(2\pi f_{IF}t) \mp \cos(2\pi f_{IF}t)\cos(2\pi f_{LO}t). \quad (2.17)$$

A SSB mixer contains two mixing blocks each mixing in-phase and quadrature components of the LO and Intermediate Frequency (IF) tones to generate a single output tone at the sum or difference frequency. A SSB mixer additionally requires an LO tone with 90° phase shift considering the complex baseband signals in-phase and quadrature signal. Detailed analyses on CMOS integrated upconversion circuits can be found in [25].

2.1.5 Transmitter architectures



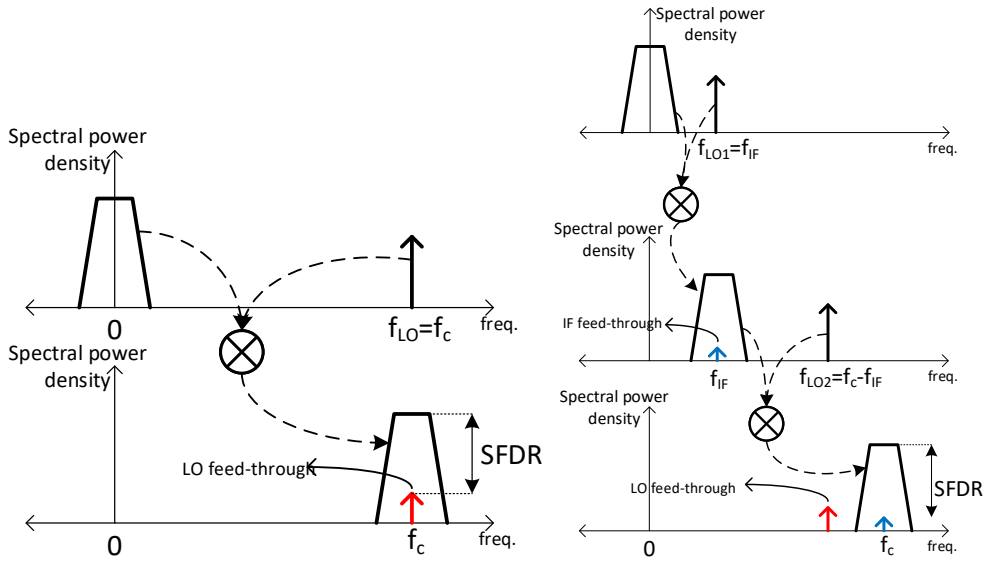
(a) Homodyne transmitter.



(b) Heterodyne transmitter.

Figure 2.16: Block diagrams of transmitter types with different frequency upconversion steps.

Transceiver architectures can be divided in several classes by their frequency conversion steps. A direct transmitter shifts the modulated and filtered baseband signal in a single step to the carrier frequency as shown in Fig. 2.16a. The digital baseband signal processing contains the modulation, upsampling, and RRC filtering in order to suppress Nyquist replicas and reduce out-of-band emissions. The filtered digital baseband signal is translated into the analogue domain, alias filtered, and upconverted by a single mixer. Linearity restrictions of the DAC and mixer generate, besides to the wanted output signal, mixing products which are filtered in the harmonic rejection filter. The signal is amplified by the Power Amplifier (PA), band-filtered, and transmitted.



(a) Homodyne. (b) Heterodyne.

Figure 2.17: Visualisation of the upconversion steps in the homodyne and heterodyne transmitter approaches.

Fig. 2.17a illustrates the mixing process. In a direct transmitter, the LO frequency is the carrier frequency f_c which leads to several disadvantages. As shown in the figure, any LO feed-through introduced by the mixer leads to a spurious tone in the transmit band, reducing the in-band spurious-free dynamic-range SFDR and, hence, according to Shannon limiting the maximum available modulation order. Additionally, the LO synthesis blocks, *e.g.* a Voltage-Controlled Oscillator (VCO) is effected by pulling since the PA amplifies the transmit signal being at the same frequency as the VCO. However, the pulling effect can be weakened by running the VCO at double the transmit frequency and utilising a frequency divider. Thereupon, the power consumption of the LO synthesis blocks and the circuit complexity increases.
As shown in Fig. 2.16b, a heterodyne transmitter utilises two or more upconversion steps. The baseband signal is first moved to an Intermediate Frequency (IF) so that it can be moved to the carrier frequency with a second mixer. The second LO frequency is $f_{LO2} = f_c - f_{LO1}$. The upconversion steps are illustrated in Fig. 2.17b. The IF can be a reasonably low-frequency so that the IF feed-through is well-controlled and the in-band SFDR is not effected. In a second step, the band at IF with the well-controlled and low IF feed-through is moved to the carrier frequency. Hereby, any feed-through of the second LO is not in the transmit band. Alternatively, a digital low IF can be introduced so that the DAC directly produces the baseband signal at the IF. This approach is able to generate the band at IF without any LO leakage. Consequently, the DAC sampling rate and thereby its complexity and power consumption are increased. Additionally, both LOs operate at different frequencies which are not close to the

carrier frequency such that they are not effected by the pulling effect caused by the PA. Nevertheless, in a heterodyne transmitter the selection of the IF and LO frequencies in combination with possible spurious tones generated by DAC need to be designed carefully. [26] introduces a semiautomated optimisation method on the selection of the IF and LO frequencies for a digital-IF heterodyne transmitter considering harmonic mixing products which might create spurious tones close to the transmit band.
Besides the given architectures, there are different types of transmitter such as fully digital transmitters [27] which digitally upconverts the signal to the transmit frequency so that the DAC generates directly the transmit signal at the carrier frequency. Furthermore, there are polar transmitters which modulate the amplitude and phase of a signal instead of using in-phase and quadrature signals. Additionally, the Radio Frequency Digital-to-Analogue Converter (RF-DAC) integrates the DAC and mixer in a single block creating the RF-DAC based transmitter type. Further analysis on various transmitter architectures can be found in [28].

2.1.6 Transmitter performance

The performance of a transmitter can be characterised by means of different metrics, *i.e.* power consumption, transmit power, spectral efficiency, symbol rate, error vector magnitude, *etc.* In this thesis, the power consumption, P_{diss}, covers the DSP and the analogue-mixed-signal components without including the PA. Furthermore, the power efficiency, P_{η}, can be given in Joule per bit that is converted into the analogue domain and ready to transmit at a specific carrier frequency.

$$P_{\eta} = \frac{d\ (\text{bit/s})}{P_{diss}} \tag{2.18}$$

The Error Vector Magnitude (EVM) is measured at the transmitter output feeding the signal into an ideal receiver which demodulates the signal and generates the constellation diagram. The transmitted symbols might be corrupted due to nonidealities in the transmitter. Fig. 2.18 shows the ideal placing of the expected symbols versus the actual received symbols. The EVM is calculated in dB or in percentage as follows:

$$EVM(\text{dB}) = 10\log_{10}\left(\frac{P_{error}}{P_{ideal}}\right), \tag{2.19}$$

$$EVM(\%) = \sqrt{\frac{P_{error}}{P_{ideal}}} \times 100\%. \tag{2.20}$$

In general, the bandwidth and modulation order define the raw data throughput of the communication system. Furthermore, coding is applied on the transmitted bits for error

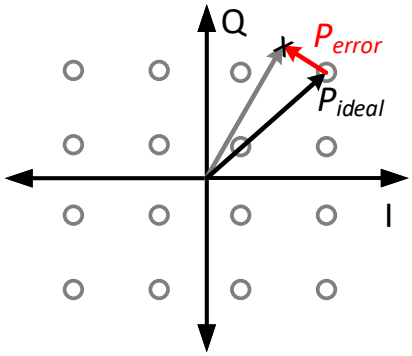


Figure 2.18: Visualisation of the misplaced received symbol in the ideal constellation diagram and the comparison between the ideal signal power and the error power.

correction and recovering of incorrect transmitted symbols. The EVM performance of the transmitter defines the required coding overhead in order to maintain a certain Bit Error Rate (BER). Therefore, a good EVM performance is crucial to increase the net data rate for the same bandwidth and modulation order.

2.2 Channel characteristics

The transmit signal propagates through a physical channel and is received by a receiver. For mobile communication devices, the channel is changing over time since one of the devices, either the receiver or transmitter or even both, can be moved. The varying channel characteristics influence the signal and thus the transmitter and/or the receiver are designed to compensate the effects. Depending on the distance between the transmitter and receiver, the free space loss reduces the signal power. Changing medium in the channel leads to a dynamically varying signal attenuation between TX and RX. Therefore, the transmit power shall be sufficiently large such that the reduced signal power still provides a certain SNR in order to not loose information. Another important effect is the multipath fading. This describes the signal being reflected by surfaces with different properties such as concrete, metal plates, *etc.* on its way to the receiver. Thereby, each signal component from a different path sees a varying phase and amplitude changes. Collectively, this leads to an amplitude and phase variation over the signal bandwidth where the former leads to corrupted signal levels and the latter can introduce a frequency dependant group delay causing Inter-Symbol Interference (ISI). In order to guarantee communication under the influence of multipath fading, equalisers are implemented in the receivers which apply the inverse of the channel transfer function [29, 30]. Since the channel might change over time,

the equalisers estimate the channel characteristics iteratively and match their transfer functions. Therefore, a certain portion of the channel need to be used for pilot tones or known sequences are transferred which reduces the spectral efficiency. Furthermore, wide bandwidth communication standards utilising several hundreds of megahertz of modulation bandwidth require high power and complex equalisers of which the feasibility becomes critical [31]. On the other hand, modulation schemes such as Orthogonal Frequency Division Modulation (OFDM) use multiple subcarriers with a fraction of the actual bandwidth in order to increase the robustness against the channel effects. Here, the modulation speed of each subchannel is reduced to a fraction which, in turn, leads to significantly reduced symbol rates being more robust against the group delay distribution caused by the channel. Furthermore, amplitude deviations over the smaller subchannels are negligible and can be corrected. However, OFDM requires higher computation power on the signal processing. Furthermore, the demand of pilot tones and the cyclic prefix consumes a certain portion of the spectrum reducing the spectral efficiency. Wireless communication using several gigahertz of bandwidth is established at higher frequencies. The 5G standard employs mmW frequencies in the 28 GHz range. On the other hand, the upcoming generation of *WiFi* referred to as *WiGig* uses the ISM frequencies at 60 GHz [5]. At those high frequencies, the free space loss plays a significant role and especially at 60 GHz there is the resonance frequency of O_2. Consequently, the line of sight connection is the dominating path for wide bandwidth communications at mmW frequencies [31].

2.3 Discussion

In the last decades, digital circuits have benefited from the technological advances in CMOS scaling. Thereby, functionality densities and operating frequencies are heavily increased, while the power consumption per operation largely decreased. Consequently, many functions, which were performed in the analogue domain before, have been moved into the digital domain. With this shift of functionality to digital, the requirements on one of the key components of integrated circuits has increased simultaneously: the data converters, *i.e.* the DAC and ADC. In contrast to digital circuits, the scaling of CMOS technology has resulted in mainly negative effects on pure analogue circuits: Smaller supply voltages reduce the dynamic range which, in turn, require modified or new analogue circuit design techniques. In addition, larger process variations must be tolerated. Obviously, the only advantage of modern CMOS technologies is the increased transit frequency of the transistors and the scaled digital circuitry of analogue-mixed-signal components. This enables the implementation of analogue circuits at higher operation frequencies while simultaneously using digitally enhanced analogue circuits.
Data rates in wireless communication increase steadily to satisfy the markets demands.

Therefore, either the modulation order or rate must be increased where the former is limited by the channel capacity and the latter by the finite frequency spectrum. Consequently, the spectral efficiency of a transmitter is one of its key property. A wide transmit bandwidth can be allocated at higher carrier frequencies which leads to new communication standards such as 5G and *WiGig* [5] that utilise mmW frequencies along the RF in the sub-6 GHz range.
A conventional transmitter architecture is based on a baseband digital signal processing block followed by digital-to-analogue converters and frequency upconverters. Prior to the step of digital-to-analogue conversion, the baseband signal needs to be oversampled to shift the Nyquist replicas out of the desired band and it needs to be digitally filtered to comply with the given specifications of the specific standard regarding out-of-band emissions. For a modulation bandwidth in the gigahertz-range, the digital baseband filters need to be clocked in the order of multiple gigahertz due to oversampling. Accordingly, the oversampled and filtered baseband signal is then fed to a DAC which is required to handle the given sampling rate. High sampling rates come along with increased power consumption, larger chip area, and especially increased circuit complexity due to the extremely demanding timing requirements. Even though DACs with a high sampling rate are demonstrated, the performance of the dedicated Digital Signal Processing (DSP) for conditioning of the baseband signal remains a bottleneck. State-of-the-art transmitters based on DACs provide an ACLR of up to −80 dBc for a limited bandwidth [10]. If the bandwidth is increased to several gigahertz, the dynamic range decreases rapidly and, in turn, the achievable ACLR falls below −30 dBc [11].

2.4 Conclusion

The implementation of transceivers which can cope with the demanded data rates and features require cutting edge technologies for all required blocks. The components of modern transmitters operate at the technological boundaries in order to achieve a wide modulation bandwidth in the gigahertz rage. The FDDAC-based approach introduced in this thesis has several advantages while being able to convert virtually any baseband signal to the analogue domain. No oversampling and dedicated digital baseband filtering is required to reduce the spectral power of Nyquist replicas. The digital baseband signal processing and the digital-to-analogue conversion is based on parallel operation in the Fourier-domain. Thereby, the sampling rates in both domains can additionally be reduced. This allows the implementation of transmitters achieving up to two magnitudes higher bandwidth compared to their conventional counterparts using the same sampling rates. The enhancement originates rather from an architectural novelty than improvements on circuit and block level.

Chapter 3

Fourier-domain data converters and transmitter system design

This chapter introduces the concept of the Fourier-domain data-converters which exploits the relation between the time-domain signal and its representation in the Fourier-domain. The main focus is laid on the Fourier-domain digital-to-analogue conversion. However, a similar concept realising an analogue-to-digital conversion is presented as well but not thoroughly investigated. The principle of the proposed data converter is derived mathematically in a general form in order to analyse the capabilities and limitations of the system. Furthermore, the introduced approach is embedded in a transmitter design which allows extremely wide modulation bandwidths, *i.e.* in the gigahertz range. A transmitter prototype for very high data rates and bandwidth is introduced which can operate in the sub-6 GHz frequency range and can extend its transmit frequency by utilising additional upconversion circuits up to the mmW frequencies if required. A system-level model of the transmitter prototype is implemented in *Matlab*® and in the circuit simulation tool *Cadence Virtuoso*® using

VerilogAMS in order to estimate the performance based on the quality and specifications of the used subblocks. Thereby, the system-level description of the proposed prototype is also used to explore the design space for an integrated and discrete components based implementation. Furthermore, the model is used to estimate a realistic transmitter performance by feeding it with performance parameters encountered in the literature. Finally, the specifications of the subblocks are derived to achieve a certain transmitter performance which will be considered for the integrated circuit design.

3.1 Fundamentals of the proposed Fourier-domain data-converters

A DAC converts the digital input signal into its analogue equivalent regardless the initial signal domain. Usually, it operates as a zero-order-hold element. As described in Chapter 2, the zero-order-hold transfer characteristic filters the band-limited digital signal and leads to Nyquist replicas which occur as out-of-band emissions. Therefore, oversampling and filtering are necessary [7] which require an increased sampling rate of the DACs and, in turn, creates a bottleneck for high bandwidths. Accordingly, the DSP block needs to operate at extremely high sample frequencies in the order of several GSps. Thus, modern transmitters require an additional and optimised DSP-chip integrated on a different CMOS technology especially optimised for digital circuits alongside with the analogue transmitter frontend chip. Alternatively, the multicarrier transmitter approach uses multiple subbands at a fraction of the actual bandwidth which are processed separately in order to reduce the DSP constraints [12]. However, this approach has several disadvantages such as the reduced spectral efficiency due to the overhead in the subbands and the necessity of multiplexers. State-of-the-art single-carrier transmitters employ spectral shaping filters with a limited number of taps and oversampling and, hence, they deliver poor spectral purity and require further handling for Nyquist replicas such as analogue filters [7, 32]. Alternatively, [33] and [34] introduce the Finite Impuls Response (FIR)-DAC technique where the DSP is partially integrated within the DAC. This is achieved by upsampling the digital input stream according to the OSR which is then applied to a shift-register that realises the z^{-1} delay in the z-domain. The actual DAC is implemented as often as the number of FIR filter taps and they are weighted according to the filter coefficients scaling. The digital filtering is thereby realised while the signal is transferred into the analogue domain. However, the weighting of the implemented DACs corresponding to the filter coefficients leads to significantly high ratios between the LSB of the smallest coefficient and the MSB of the largest coefficient. Hence, the required dynamic range, *i.e.* the resolution limits the performance of the FIR-DAC. The implementations, [33, 34],

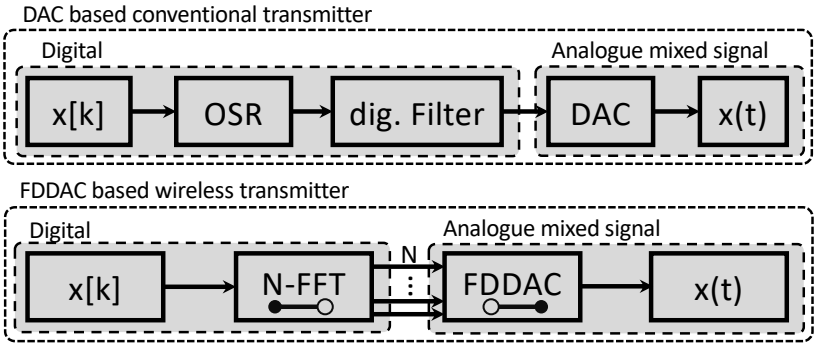


Figure 3.1: Comparison of the operation principle of a conventional DAC-based transmitter and the proposed FDDAC-based transmitter [35] ©2020 IEEE.

show that the FIR-DACs are limited in the achievable bandwidth, spectral shaping performance and number of bits.
However, transmitters with several gigahertz of bandwidth which alleviate both limitations in the analogue-mixed-signal and the digital domains have not yet been reported. Fig. 3.1 shows a comparison of a conventional DAC-based transmitter versus the proposed FDDAC-based transmitter, as stated in the patents [36–38]. The proposed Fourier-domain FDDAC overcomes the bandwidth, spectral purity, and DSP speed limitations by adopting a new approach in the representation of the baseband signals in contrast to conventional DACs. Instead of representing the DAC input-signal in the time-domain, the proposed data converter concept advantageously exploits the relationship of the discrete Fourier- and inverse continuous Fourier- transform between the time and the frequency-domain: A predefined number of discrete Fourier coefficients of the digital representation of any time-domain signal is first calculated. These complex coefficients are then simultaneously modulated onto the same number of high frequency carriers forming, in this way, the time-domain signal which might be shifted upwards in the spectrum by any desired offset frequency or by the carrier frequency. If carried out by carefully considering the nonperiodic nature of an arbitrary communication signal and by exploiting the properties of the continuous inverse Fourier Transform (IFT), a faithful frequency-shifted time-domain signal can be generated at an arbitrary as well as high output frequency. Therefore, relatively simple DACs are used to modulate the slowly varying Fourier coefficients onto the equidistantly spaced tones. This architecture, composed by DACs which modulate Fourier coefficients onto tones, is termed as Fourier-domain Digital-to-Analogue Converter or in short FDDAC. Fig. 3.2 visualises the representation of the baseband information at different points within the FDDAC-based transmitter. The first graph shows a sequence of complex-valued time-domain signals at a certain sampling rate of which N samples are converted into the frequency-domain by an appropriate Discrete Fourier Transform (DFT) which, in turn, results in the same number of complex Fourier coefficients. The Fourier coefficients represent power levels at distinct frequencies such that any offset frequency

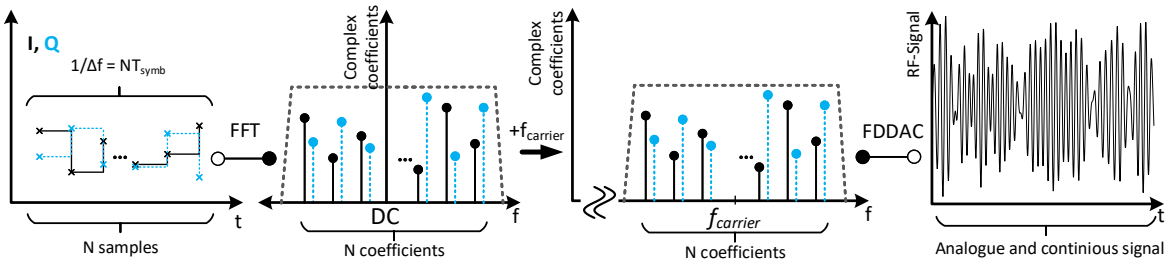


Figure 3.2: Representation of the signal domain transitions in the FDDAC-based transmitter.

can be added to change the frequency of the signal. These coefficients are fed to the FDDAC which reconstructs the initial digital input signal in the analogue domain with a deliberate frequency shift.
At this point it is important to state the difference between a conventional OFDM-based transmitter and the proposed FDDAC principle. An OFDM-based transmitter utilises an IFT or FT on the transmitter side and transmits parallelised time or frequency information, respectively. Whereas, the counter operation, namely the FT or IFT, is firstly performed in the receiver and the frequency or time-domain information is reconstructed. On contrary, the FDDAC-based approach contains both the FT and the continuous inverse FT on the transmitter side, hence, the digital input signal and the analogue output signal are in the same domain.
The FDDAC is able to convert any Nyquist-sampled complex time-domain signal into the analogue domain. A QAM baseband signal, $\underline{x}_k$, sampled at the Nyquist rate, $1/T_{symb}$, consisting of a real and imaginary part, $x_{re,k}$ and $x_{im,k}$, is assumed to investigate the principle of the FDDAC. The index k represents the time-domain samples and $1/T_{symb}$ corresponds to the Bandwidth (BW). To perform a complex-valued N-point DFT, N samples of the complex baseband signal $\underline{x}_k$ are parallelised and fed to an appropriate DFT-block. The representation of the time-domain signal, $\underline{x}_k$, in the frequency-domain, $\underline{X}_i$, can be calculated as follows:

$$\underline{X}_i = \sum_{k=0}^{N-1} \underline{x}_k e^{-j2\pi ik/N} \quad i,k \in \mathbb{N}. \tag{3.1}$$

The time-domain signal is represented by N complex-valued Fourier coefficients. The sampling rate of the Fourier coefficients is reduced by the factor N, respectively to N/T_{symb}. In order to reconstruct the time-domain samples $\underline{x}_k$ without loss of information, a discrete inverse Fourier transformation Inverse Discrete Fourier Transform (IDFT) can be utilised:

$$\underline{x}_k = \frac{1}{N} \sum_{i=0}^{N-1} \underline{X}_i e^{j2\pi ik/N}. \tag{3.2}$$

The sum is executed for different k values in order to reconstruct the k^{th} time-domain sample. The IDFT can be rewritten for different k values in the following form:

$$\begin{bmatrix} \underline{x}_0 \\ \underline{x}_1 \\ \underline{x}_2 \\ \vdots \\ \underline{x}_{N-1} \end{bmatrix} = \frac{1}{N} \begin{bmatrix} e^{j2\pi 0/N} & e^{j2\pi 0/N} & e^{j2\pi 0/N} & \dots & e^{j2\pi 0/N} \\ e^{j2\pi 0/N} & e^{j2\pi 1/N} & e^{j2\pi 2/N} & \dots & e^{j2\pi (N-1)/N} \\ e^{j2\pi 0/N} & e^{j2\pi 2/N} & e^{j2\pi 4/N} & \dots & e^{j2\pi 2(N-1)/N} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ e^{j2\pi 0/N} & e^{j2\pi (N-1)/N} & e^{j2\pi 2(N-1)/N} & \dots & e^{j2\pi (N-1)^2/N} \end{bmatrix} \begin{bmatrix} \underline{X}_0 \\ \underline{X}_1 \\ \underline{X}_2 \\ \vdots \\ \underline{X}_{N-1} \end{bmatrix}. \tag{3.3}$$

The matrix containing the $e^{j2\pi ik/N}$ expressions represents time discrete phasors of the IDFT with different rotation speeds depending on the parameters i in horizontal direction, k in the vertical direction, and the number of the DFT length N. The phasors inherit new positions at each sampling point k. The sum of the products with the corresponding Fourier coefficients reconstruct the time-domain samples. The expression $e^{j2\pi ik/N}$ is substituted by the identity, $e^{jx} = \cos(x) + j\sin(x)$, and the complex-valued Fourier coefficient is replaced by $\underline{X}_i = X_{i,re} + jX_{i,im}$ so that the IDFT can be rewritten as:

$$\begin{aligned} \underline{x}_k = \frac{1}{N} \sum_{i=0}^{N-1} & X_{i,re} \left(\cos\left(\frac{2\pi ik}{N}\right) + j \sin\left(\frac{2\pi ik}{N}\right) \right) + \\ & X_{i,im} \left(j \cos\left(\frac{2\pi ik}{N}\right) - \sin\left(\frac{2\pi ik}{N}\right) \right). \end{aligned} \tag{3.4}$$

The next step towards the FDDAC is to transform the phasors with discrete steps, as illustrated in the phasors matrix in (3.3), determined by $k \in \mathbb{N}$ into their continuous counterparts, by $k \to t \in \mathbb{R}$. Fig. 3.3 shows the discrete phasors and the continuous sine- and cosine-tones which represent their counterparts in the continuous-time. This step is considered as the transformation from an IDFT to a continuous-time inverse Fourier transformation. The phasors in the first row of the phasor matrix with $i = 0$ represent the DC frequency component. The next $N/2$ phasors are the positive frequency components up to the Nyquist frequency. The remaining $N/2-1$ phasors represent the negative frequency components which appear to rotate in the opposite direction. The continuous phasors can be represented by sine- and cosine-tones which are equidistantly spaced in frequency with a frequency offset of $\Delta f = BW/N$ which corresponds to N/T_{symb}. Hereby, the phasors representing the negative frequencies are reproduced with sinusoidal tones above the Nyquist frequency. However, all transformed continuous phasors are at the exact same positions as their discrete counterparts, as shown in the matrix for certain sample points in time. Namely, for:

$$t_{samp} = kT_{symb}. \tag{3.5}$$

The complex valued continuous-time inverse Fourier transform using sine and cosine expressions can be written as:

$$\underline{x}_t = \frac{1}{N}\sum_{i=0}^{N-1} X_{i,re}\left(\cos\left(2\pi f_i t\right) + j\sin\left(2\pi f_i t\right)\right) + X_{i,im}\left(j\cos\left(2\pi f_i t\right) - \sin\left(2\pi f_i t\right)\right), \tag{3.6}$$

$$\text{where,} \quad f_i = i\frac{BW}{N}.$$

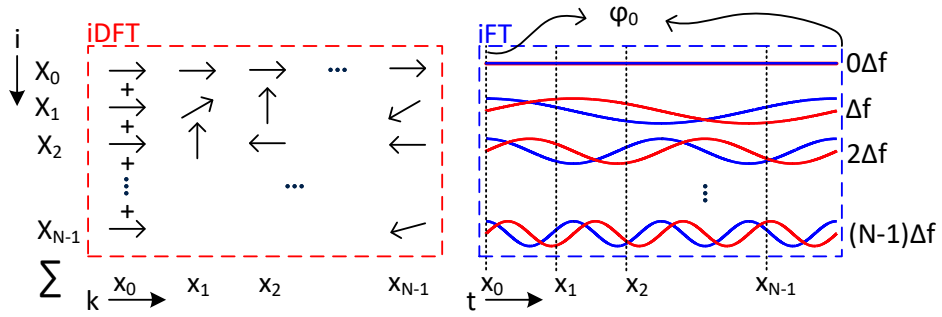


Figure 3.3: Conversion of the discrete phasors of the iDFT (left) into the continuous phasors of the inverse Fourier Transformation (FT) (right) implemented by sinusoidal tones [35] ©2020 IEEE.

At the time points as stated in (3.5), the summation of the weighted sine and cosine signals represents exactly the time-domain samples. Between these time points there is a smooth and continuous transition while reconstructing the time-domain samples. Hence, in contrast to a sample-and-hold block, the transition between the two samples is formed by the summation of sinusoidal tones with frequencies within the desired BW. This relation leads ideally to an intrinsic band-filtering characteristic. Thus, no spectral out-of-band emissions exist in theory. In contrast to all other DAC-based transmitters, no additional oversampling or band-filtering is necessary. This property is one of the key advantages of the proposed FDDAC-based transmitter. Therefore, it is possible to implement the FDDAC by weighting a set of continuous tones with the complex Fourier coefficients once, such that the N time-domain samples are reconstructed without any additional sampling. Therefore, the proposed data conversion technique ideally delivers a spectrally pure output signal while no dedicated DSP for oversampling and filtering of the Nyquist replicas is required. This further eliminates the speed restrictions on the DSP block. Fig. 3.4 shows the qualitative course of the reconstructed signal where the N samples are reconstructed with continuous transitions in between. Consequently, the sampling rate of the signal weighting blocks is reduced by a factor of NOSR.
Furthermore, any offset frequency, f_{offset}, can be added to all bin frequencies, f_i, to directly reconstruct the digital baseband signal at virtually any carrier frequency. In a

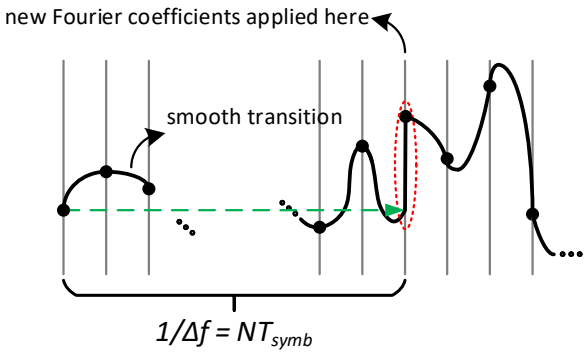


Figure 3.4: continuous-time inverse Fourier transform reconstructing N time-domain samples.

real system, it is sufficient to transmit the real part of the inverse and continuous-time Fourier transformation. The output signal of the FDDAC-based transmitter can be given as follows:

$$x_{f_{offset}}(t) = \sum_{i=0}^{N-1} X_{i,re} \cos(2\pi f_i t) - X_{i,im} \sin(2\pi f_i t), \quad \text{where} \quad f_i = i\frac{BW}{N} + f_{\text{offset}}. \tag{3.7}$$

The relation shown in (3.7) can be adapted in a transmitter system by utilising multiple, namely N, simultaneously operating conventional transmitters modulating the complex Fourier coefficients on equidistantly spaced tones around the carrier frequency which represent the bins of the IFT. Therefore, N complex digital input signal samples are stored and fed to a DFT block parallelly. A new set of N Fourier coefficients, $X_{i,re}$, $X_{i,im}$, is calculated by the complex-valued DFT with a rate of BW/N. These coefficients are fed to the FDDAC which contains N transmit cores that can be implemented either as polar or I/Q transmitters which modulate the complex coefficients on the equidistantly spaced tones. In this work, an I/Q based transmit core is utilised due to its simplicity and inherent timing advantages. The output of each I/Q transmit core which together implement the FDDAC seen individually occurs like random modulation with a sinc shape in frequency-domain as discussed in Chapter 2. The spectral shaping and proper operation of the proposed FDDAC is only given when all I/Q transmit cores operate simultaneously where each contributes to the complete modulated band. Furthermore, at the instant when the coefficients are set to the I/Q transmit cores, all bin frequencies need to be at zero-phase, ϕ_0. The summed output of the FDDAC delivers the first time-domain sample which was processed by the DFT. The continuous phasors rotate and, in return, all time-domain samples are reconstructed without any other switching actions and with smooth transitions between the N samples. Hence, it implements an intrinsic ideal filtering of the analogue output signal. All continuous phasors move

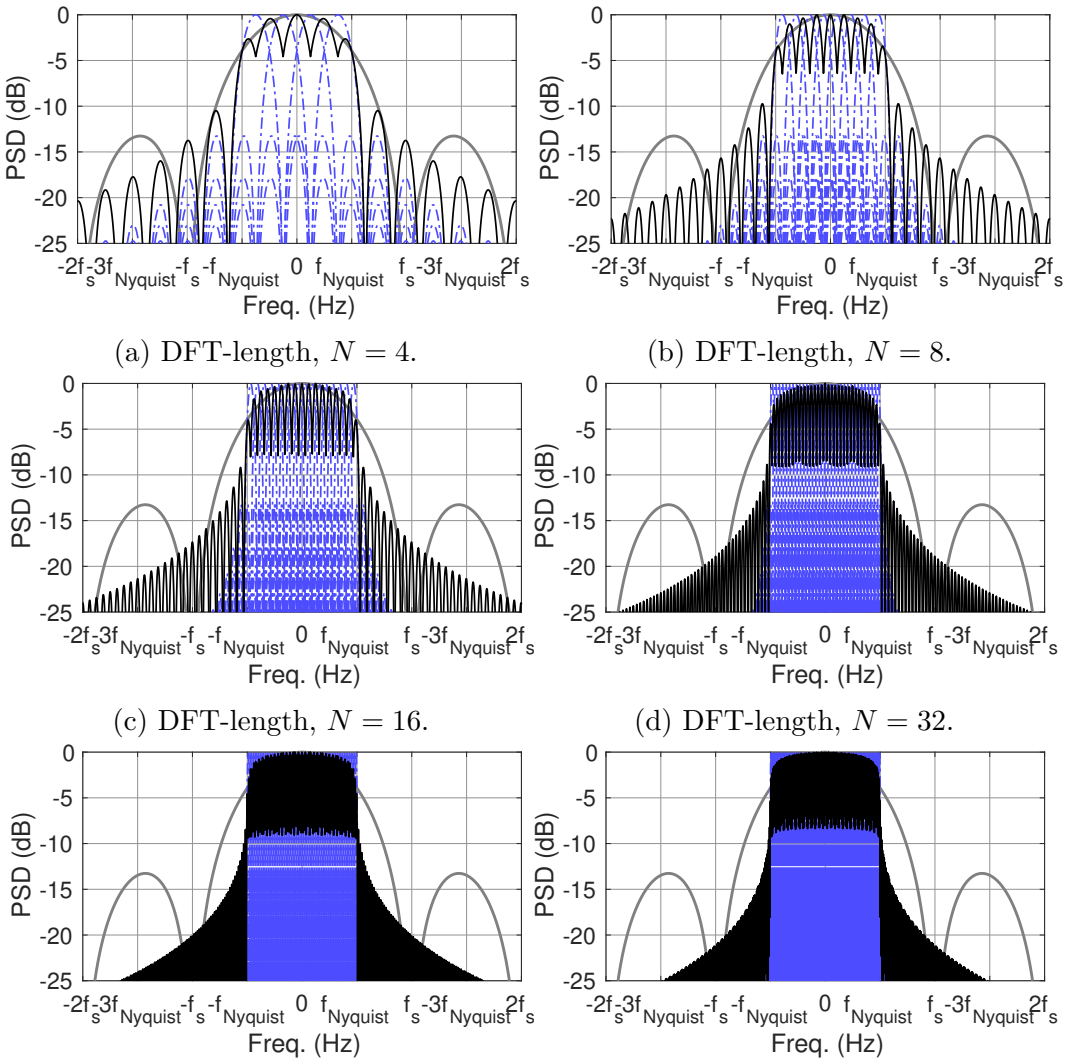
to zero-phase, ϕ_0 after the N^{th} time-domain sample of the actual coefficient set is reconstructed. Meanwhile, the next N time-domain samples are parallelised and processed by the DFT creating a new set of Fourier coefficients.
The initial DFT is performed on a limited number N of samples which are assumed to be periodic such that the N samples are infinitely repeated. After the last time-domain sample is reconstructed, the output signal of the FDDAC moves towards the first time-domain sample of the actual coefficient set. At the time when all phasors return to zero-phase simultaneously, a new set of Fourier coefficients is applied to the I/Q transmit cores. At this moment in time, the output of the FDDAC jumps to the first sample of the new time-domain samples of the new Fourier coefficient set. These relations lead to a discontinuity, as shown in Fig. 3.4. However, the digital input signal which will be converted into the analogue domain is random and not periodic such that the Fourier coefficients need to be recalculated and updated after the first N samples are reconstructed. This discontinuity causes spurious emissions out of the desired frequency band if not handled properly as described in Section 3.1.2.

3.1.1 Analyses of the spectral shaping capabilities of the FDDAC approach

The I/Q transmit cores operate at a sampling rate of BW/N without oversampling and filtering. Each I/Q transmitter processes a band-limited digital random signal, *i.e.* i^{th} Fourier coefficient. In turn, the spectral output of each transmit core is digital white noise which is filtered with the transfer function of the zero-order sample-and-hold as previously discussed in Chapter 2. Consecutively, the spectral power density of the FDDAC output can be calculated by the superposition of the transfer characteristics of N I/Q transmit cores. The Fourier coefficients are modulated on the phasor tones at frequencies f_i, hence, the complete transmitters spectral power density, PSD_{tx}, can be calculated by the convolution of the bin frequencies with the zero-order-hold transfer function, *sinc*, in the analogue domain. The *sinc* function depends on the bandwidth, BW and the DFT-length N.

$$PSD_{tx}(f) = \sum_{i=0}^{N-1} \left[\delta(f - f_i) * \frac{\sin(\pi f T_{symb} N)}{\pi f T_{symb} N} \mathrm{e}^{-j\pi f t} \right] \tag{3.8}$$

Increasing the number of bins reduces the bandwidth processed by each individual transmit core. Thereby, the sample-rate of the Fourier coefficients are reduced which, in turn, leads to a contraction of the *sinc* function by factor N. Fig. 3.5 illustrates a comparison for different numbers of bins between the calculated spectral power density of a conventional DAC without oversampling and filtering and the FDDACs output



(a) DFT-length, $N = 4$.

(b) DFT-length, $N = 8$.

(c) DFT-length, $N = 16$.

(d) DFT-length, $N = 32$.

(e) DFT-length, $N = 64$.

(f) DFT-length, $N = 128$.

Figure 3.5: Calculated output spectrum of a conventional DAC sampling at Nyquist frequency illustrated in grey. The PSD of the each I/Q transmit core implementing the FDDAC bins are shown in blue. The calculated output PSD of the complete FDDAC sustained by the superposition of the individual transmit cores is shown in black.

spectrum. The transmit cores processing a narrower bandwidth facilitate a narrow *sinc* as their transfer functions with faster declining side-lobes such that the complete output based on their superposition delivers already an improved spectral efficiency. Note that the discontinuities are not tackled yet. Furthermore, the main-lobe of the *sinc* function is placed exactly at the bin frequency where the minima with the highest attenuation are exactly placed on all other bins.

The calculated output spectra of the FDDAC for different bin numbers and DFT-length is compared to a single DAC which samples a nonoversampled input signal. Fig. 3.6 depicts the attenuation of the out-of-band emissions. The attenuation is evaluated at two specific points:

1. At the point where the first side-lobe of the conventional DACs output power spectral density has its maximum.

2. At the frequency $f_{Nyq+0.1BW}$ which describes a frequency distance to the edge of the modulation band of 10% of the actual bandwidth. The out-of-band-emissions are evaluated by an offset frequency of 186 MHz for the WiGig single-carrier transmit scheme with a modulation bandwidth of 1.86 GHz. Considering the frequency offset of 186 MHz as guard space between two communication channels the evaluated attenuation delivers the ACLR at the give frequency point.

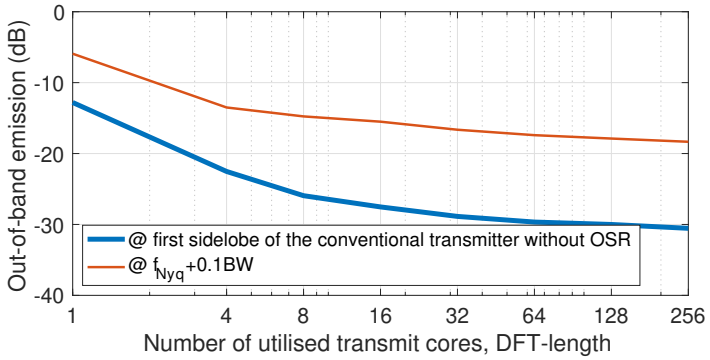


Figure 3.6: Simulated ACLR of the FDDAC transmitter for different DFT-lengths evaluated at different offset frequencies.

The x-axis shows the number of bins, where 1 corresponds to the conventional DAC-based transmitter with no oversampling and filtering. With increasing number of bins the out-of-band-attenuation decreases. Nevertheless, each bin is physically implemented by an appropriate I/Q transmit core with its corresponding LO frequency implementing the phasor tone. The trade-off is between the hardware complexity of the FDDAC versus the achievable spectrum shaping capability. However, the graph shows that the out-of-band emissions are attenuated with a steep decay for up to 16 bins. Furthermore, compared to the conventional DAC the signal power at the first side-lobe is reduced more distinctly. All in all, the number of 16 bins seems to be a sweet-spot since the improvement of the attenuation for higher number of bins shows a less distinct change. This relation further proves the benefit of the FDDAC which is able to generate a signal with significantly reduced out-of-band emissions.
Additionally, the introduced delay, τ_{conv}, of the proposed digital-to-analogue conversion technique depends on the DFT-length, N, and the symbol rate, $1/T_{symb}$. It can be

calculated as follows:

$$\tau_{conv} = NT_{symb}. \tag{3.9}$$

A reasonably low N is selected for practical reasons in the realisation of the FDDAC-based transmitter. In case of a conventional oversampling and filtering technique, the length of the digital FIR filter which contributes to the conversion delay is greater.

3.1.2 Baseband digital signal processing and windowing

The spectral mask illustrated in Fig. 2.1 shows that the WiGig standard requires a reduction of out-of-band emissions to -17 dBc at an offset of approximately $0.14BW$ from the edge of the band which translates to an offset of 260 MHz for a modulation bandwidth of 1.86 GHz. The FDDAC approach significantly reduces the out-of-band emissions far away from the actual band. However, the spectrum contains spurious emissions at frequencies close to the band due to the glitches that appear when a new set of Fourier coefficients are sampled. Fig. 3.6 shows the spectral power evaluated at an offset of $0.1BW$ to the band. It shows a compelling decay up to a DFT length of 8, although it continues with a slow decay. In order to fulfill the requirements of the spectral mask for this exemplary selected standard, a large DFT-length in the order of 128 or 256 shall be used. This requires the same number of physically implemented simultaneously operating I/Q transmit cores and the corresponding number of LO frequencies. Thus, the implementation becomes impractical.
A deliberate constant overlap-add windowing is utilised in order to further reduce the out-of-band emission and improve the spectral shaping. Thereby, the signal power is fading in and out causing an artificial periodicity of the input time-domain sequence. Windowing is a well-known technique in short-time-DFT based systems [39–41]. Here, a 50% constant overlap-and-add window is used to ensure the signal integrity, as shown in Fig. 3.7. The window functions with different lengths, *i.e.* 16 and 32 and their delayed copy add to a constant number as an overall weighting factor which only performs a linear scaling on the signal. The time-domain digital symbol sequence is divided in two paths delayed and nondelayed, respectively. Both signals are multiplied by the corresponding window functions and their DFT is calculated. Thereby, the window function attenuates the signal power such that the discontinuities appear at the maximally attenuated points of the windowed sequences.
Fig. 3.8 depicts the block diagram of an extended approach that introduces the window function by utilising the FDDAC twice. The DFT is performed by a Fast Fourier Transform (FFT) block which is commonly used in various DSP units. Two FDDACs operate simultaneously where one is processing the delayed and the other is processing the nondelayed windowed signal, respectively. For further explanation, each $N/2$ symbols in the symbol sequence are summed to a group and denoted with numbers. In

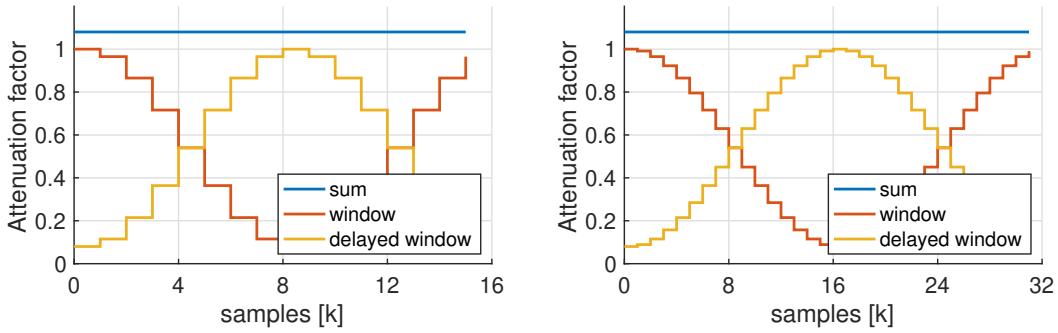


Figure 3.7: Hamming windows with different lengths, their delayed copy, and sum.

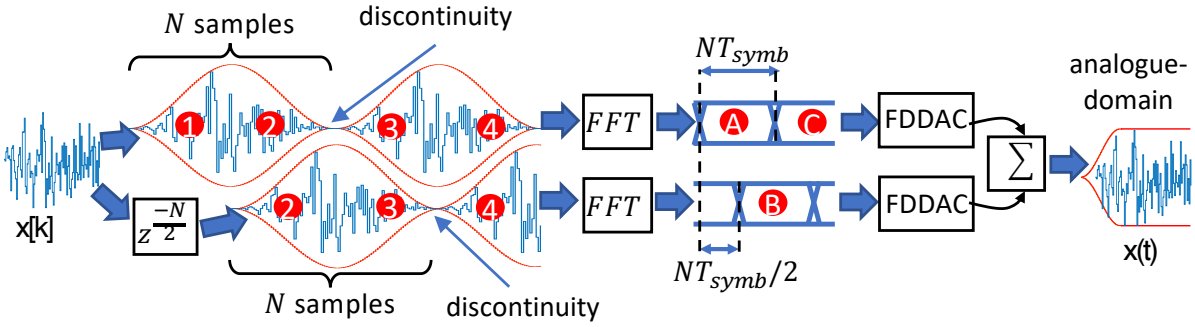


Figure 3.8: Signal processing technique to include windowing with constant overlap-add and reconstruction by utilising a single FDDAC.

the upper nondelayed path, the first N samples contain the symbols ① and ②, whereas the first N samples of the delayed path contain the symbols ② and ③. Thus, the FFT block in the lower path starts the calculation of the Fourier coefficients with a delay of $T_{symb}N/2$. The signal in the analogue domain is reconstructed by two individual FDDACs where the second one is operating with delayed phasors. All phasors of the additional FDDAC in the delayed path have an offset delay of $T_{symb}N/2$ since the same delay is experienced by the FDDAC inputs which are the Fourier coefficients of the delayed FFT. Each FDDAC path reconstructs N samples of which the first and last samples are maximally attenuated. Ideally, the first and last samples have a value of zero. As the reconstruction continues based on the coefficients Ⓐ, the upper FDDAC in the nondelayed path reconstructs the samples in ① and ②. Thus, the analogue signal amplitude fades in and out. When the phasors complete the rotation cycle such that a new set of Fourier coefficients, Ⓒ, can be applied, the reconstructed signals amplitude is already decreasing. Due to the expected periodicity of the IFT, the output of the FDDAC moves to the first time-domain sample of the actual Fourier-domain set, Ⓐ, which is ideally zero. The next set of Fourier coefficients represents the time-domain samples ③ and ④ which are windowed as well and the first sample is zero. Therefore, the output of the FDDAC remains zero at the instant when the new set of Fourier

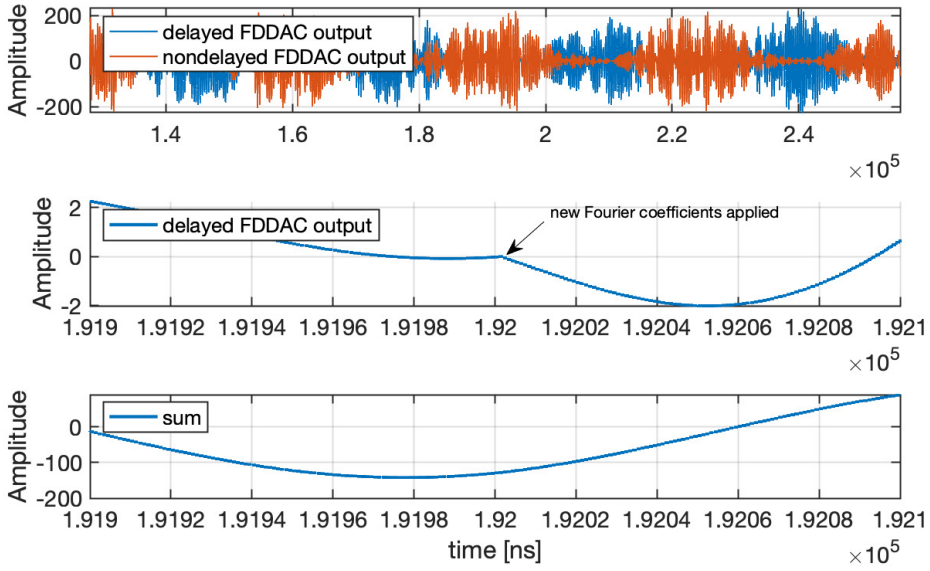


Figure 3.9: The analogue output of the delayed and nondelayed FDDAC, the remaining discontinuity after windowing and the summed output.

coefficients are applied. In turn, there is ideally no discontinuity. Meanwhile, the same operation is performed in the delayed path where the Fourier coefficients Ⓑ are applied to the FDDAC. This leads to the reconstruction of the first sample of the time-domain sequence ② such that the time-domain outputs of both FDDACs can be directly summed in order to achieve the constant-overlap-add characteristic. Fig. 3.9 shows the reconstructed analogue signal from the delayed and nondelayed paths. The amplitude of the delayed FDDAC remains at zero when a new coefficient set is applied. However, the slope of the analogue output signal still contains a discontinuity. Signal power at this instant is strongly attenuated and the discontinuity is negligible. The complete reconstructed analogue time-domain output signal is obtained by the summation of the two FDDAC outputs. Therefore, the discontinuities in the reconstructed signal appear at the points where one of the window functions provides the highest attenuation and the other provides lowest attenuation so that the amplitude and slope of the discontinuity compared to the other signal path become negligible.
The second FDDAC introduced by the windowing and the additionally required delayed phasor tones lead to at least a doubling of the circuit complexity and power consumption. Therefore, it is desirable to process the Fourier coefficients of both windowed FFTs in a single FDDAC. Fig. 3.10 shows the baseband signal processing required for the implementation of the transmitter based on a single FDDAC with windowing. Since the goal is to reduce the number of FDDACs, the Fourier coefficients of both paths shall be fed to a single FDDAC. Consecutively, the signal summation should be performed

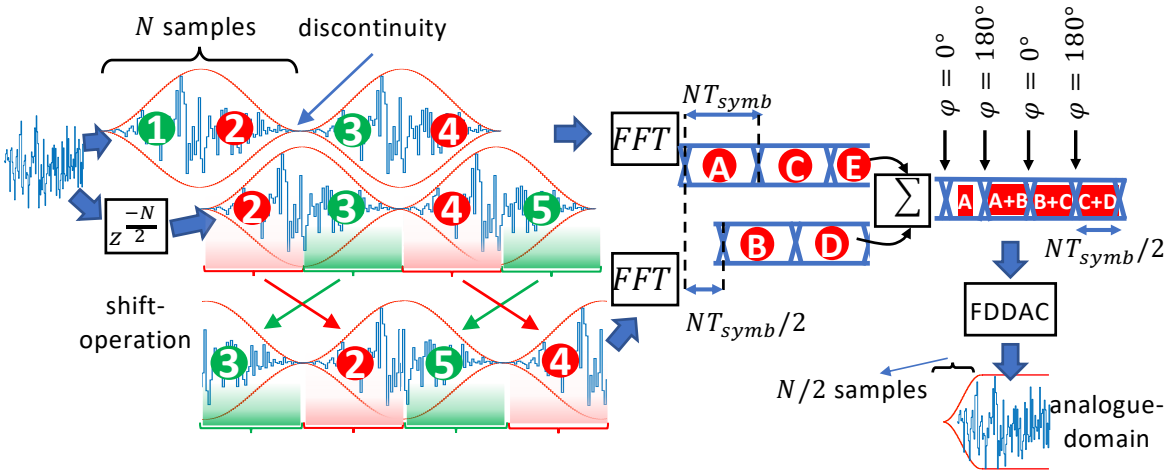


Figure 3.10: Signal processing technique to implement windowing with constant overlap-add and reconstruction by utilising a single FDDAC [35] ©2020 IEEE.

before the FDDAC stage in the frequency- and digital-domain instead of in the time- and analogue-domain. Each FFT block provides a set of N Fourier coefficients every NT_{symb}, whereas there is a time-delay between the two FFT blocks. The upper FFT delivers the first set of coefficients named Ⓐ representing the time-domain information ① and ② in the upper path. When all phasors of the FDDAC are at zero-phase simultaneously, the coefficients Ⓐ are applied.
The FDDAC reconstructs the time-domain signal ①. Since the window function attenuates and changes the time-domain samples, perfect reconstruction can only be guaranteed by the constant-overlap-and-add criterion. Therefore, the coefficients of the delayed path are required. At the instant, when the reconstruction of the $N/2^{th}$ sample appears at the FDDAC output, the lower FFT block provides the Fourier coefficient set Ⓑ which represents the time-domain symbols ② and ③ in the lower delayed path. The constant overlap and add criteria can be fulfilled when reconstructed properly and added to the time-domain signal from the coefficients Ⓑ. Considering the time duration of NT_{symb} as a complete period where all phasors start rotation at zero-phase with different speeds and achieve zero-phase at the end, this can be seen as if the Fourier coefficients are calculated and applied to the FDDAC at the phases 0° and 180° for the nondelayed and delayed paths. When the coefficients Ⓑ are applied to the same FDDAC, at the instant when they are calculated, all phasors have been rotating for a time of $NT_{symb}/2$ so that the first reconstructed sample of the Fourier coefficient set Ⓑ will be the first sample of ③. Nevertheless, at this point in time, the nondelayed reconstruction delivers the first time-domain samples of ② from the upper path. Hereby, a systematic Inter-Symbol Interference (ISI) is introduced since two differently weighted independent samples are summed. Therefore, the windowed and delayed signal in the

time-domain needs to be permuted before being fed to the FFT. The shift operation shown in Fig. 3.10 changes the left and right part of the windowed signal. The cyclic nature of the inverse continuous Fourier transformation implemented by the FDDAC leads the correct samples to be reconstructed. Furthermore, the Fourier coefficients being fed to the FDDAC are updated by any change coming from the upper or lower FFT blocks, such that the sampling rate of the single FDDAC becomes $2f_{symb}/N$. In this way, the windowing is applied, the signals are added in the frequency-domain, and they are reconstructed on a single FDDAC without generating any glitches while the sampling rate of the FDDAC is doubled.

3.1.3 Analysis of windowing and effects on the output power spectral density

Windowing is used in the FDDAC for two reasons, namely to attenuate the glitches during switching between coefficient sets and increase the frequency selectivity of the bins. However, the effect on the output spectrum shall be evaluated to understand and analyse the involved mechanisms. Usually, windowing is used when processing continuous-time analogue signals to increase the frequency resolution of the DFT. A feasible DFT implementation processes a finite number, N, of samples. It is further assumed that the sequence of N samples are repeated periodically. The reciprocal value of the complete sample time, $1/\left(NT_{sample}\right)$, defines the frequency resolution of the DFT. The bins of the DFT emulate a bank of bandpass filters with a certain filtering characteristic, where each is centred at multiples of the resolution frequency, *i.e.* the bin frequencies. However, the bandpass filtering characteristic is not ideal and it depends on the applied window type. A DFT without any windowing is assumed to use a rectangular window having a constant weighting factor of one. For a sufficiently high DFT-length, N, the rectangular window behaviour approximates a *sinc* function. Fig. 3.11 illustrates the bandpass filters implemented by the bins for an exemplary DFT-length of 8 where the upper graphs depict the Fourier transformed of the rectangular window and the lower graphs depict the Fourier transformed of the Hann window. In this particular case, the input signal of the DFT is a Nyquist-sampled band-limited symbol sequence. Therefore, the filtering of the bands are shifted cyclically. This behaviour shows the frequency selectivity of the bins.
Assuming a digital signal at a single frequency rather than a random modulated signal, the frequency selectivity effect can be explained. The Fourier transform of the rectangular window has its maximum, main-lobe, at the centre frequency of the actual bin. The attenuation is infinite at the frequencies of all other bins. If the initial signal had only frequency components centred at one or multiple bin frequencies, the DFT would output spectral power components concentrated at the same single or multiple

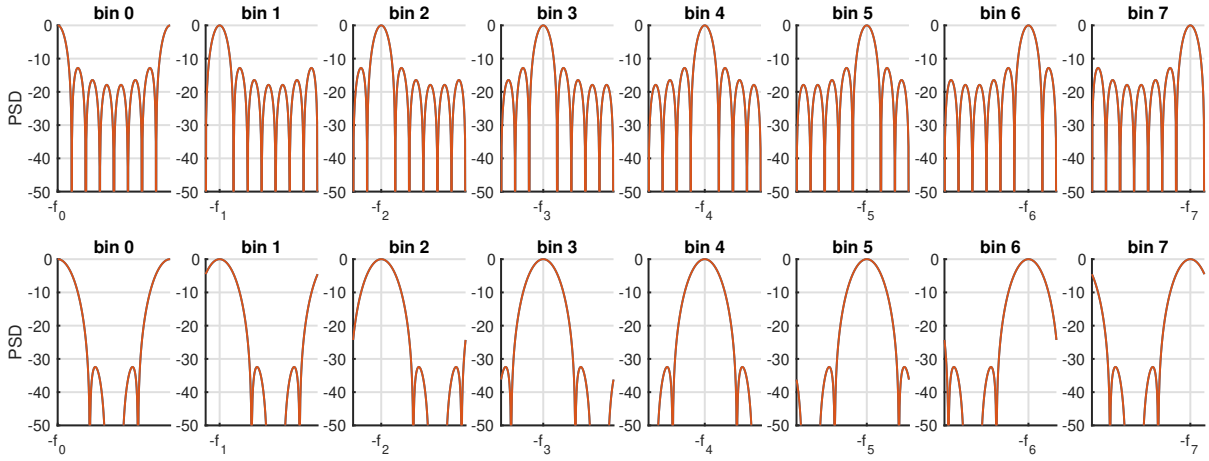


Figure 3.11: Fourier transform of rectangular (top) and Hann (bottom) window functions placed at the bin frequencies of an 8 point DFT .

bins. Consequently, no signal power leaks to the adjacent bins. If the initial signal has a frequency between two bins, a large portion of power would leak into all other bins. Power also leaks cyclically beyond the band edges due to the cyclic characteristic of the band-limited frequency-domain. Based on the use case, different windows are analysed to showcase their performance improvements. The Fourier transformation of the Hann window, shown in the lower graphs of Fig. 3.11, yields a broad main-lobe with double the width. The frequency selectivity is important if the FDDAC-based transmitter is used to transmit several narrowband signals simultaneously. Windowing increases the frequency selectivity. Thus, multiple narrowband signals can be transmitted using a single FDDAC transmitter without interfering each other.
The second effect of the windowing is seen once the signal is converted into the continuous-time analogue domain by the FDDAC. A new set of coefficients are sampled when the window function attenuates the signal power nearly to zero such that no sampling discontinuity appears. Nevertheless, at the sampling point the slope of the signal might still change due to the discontinuity in the slope of the signal. This significantly reduces the out-of-band spectral emissions. The proposed approach utilises the windowing functionality in discrete time-domain in order to improve the spectral efficiency in the continuous-time analogue domain after the IFT performed by the FDDAC. Thereby, the filtering characteristic of each bin is changed by the applied window. Multiplication in the time-domain with a window function corresponds to a convolution in the frequency-domain with the Fourier transform of the window function, $\mathcal{F}(win)$. The spectral power density of the delayed and nondelayed path, $PSD_{tx,win}$, can be calculated as follows:

$$PSD_{tx,win}(f) = \sum_{i=0}^{N-1} \left[\delta(f - f_i) * \mathcal{F}(win)\right]. \tag{3.10}$$

Alternatively, the analogue signal generated by the FDDAC can be mathematically described including the discontinuities at the time when a new set of Fourier coefficients are applied. Therefore, (3.1) is extended to cover multiple DFTs:

$$\underline{X}(i,m) = \sum_{m=-\infty}^{\infty} \left[\sum_{k=0}^{N-1} \underline{x}(kT_{symb} + mT_F) e^{-j2\pi ik/N} \right] g(t - mT_F). \tag{3.11}$$

Hereby, the Fourier coefficients with the index i of the m^{th} DFT are calculated. The FDDAC outputs a continuous-time signal defined for each DFT duration of $T_F = NT_{symb}$:

$$\underline{x}(t) = \sum_{m=-\infty}^{\infty} \left[\sum_{i=0}^{N-1} \underline{X}(i,m) e^{j2\pi f_i t} \right] g(t - mT_F), \tag{3.12}$$

where the piecewise defined function $g(t)$ is 1 for $0 \leq t < T$. The Fourier coefficients $\underline{X}(i,m)$ are replaced by equation (3.11):

$$\underline{x}(t) = \sum_{m=-\infty}^{\infty} \left[\sum_{i=0}^{N-1} \left(\sum_{k=0}^{N-1} \underline{x}(kT_{symb} + mT_F) e^{-j2\pi ik/N} \right) e^{j2\pi f_i t} \right] g(t - mT_F). \tag{3.13}$$

The expression $e^{-j2\pi ik/N}$ can be rewritten to $e^{-j2\pi f_i k T_{symb}}$ and multiplied with the term $e^{j2\pi f_i t}$ which results in:

$$\underline{x}(t) = \sum_{m=-\infty}^{\infty} \left[\sum_{i=0}^{N-1} \left(\sum_{k=0}^{N-1} \underline{x}(kT_{symb} + mT_F) e^{j2\pi f_i (t - kT_{symb})} \right) \right] g(t - mT_F). \tag{3.14}$$

By moving the term $\underline{x}(kT_{symb} + mT_F)$ out of the sum over k and swapping the sums, the following arithmetic series equation can be used:

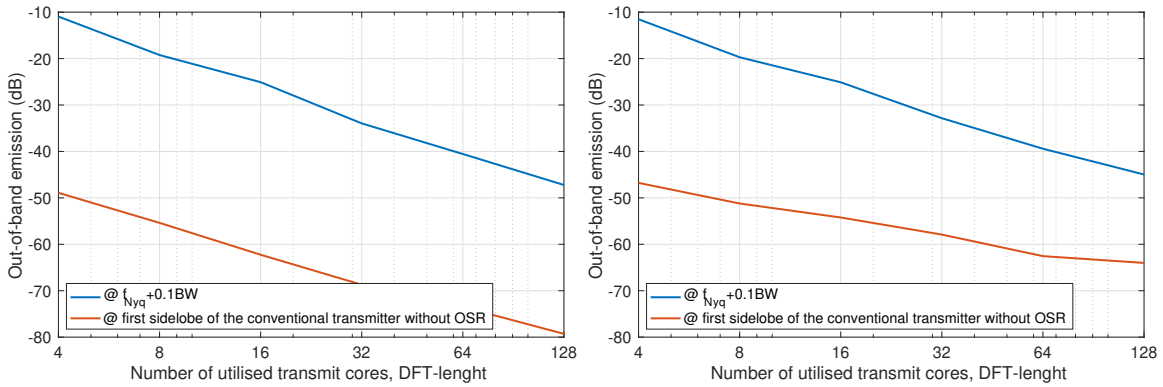
$$\sum_{i=0}^{N-1} a^i = \frac{a^N - 1}{a - 1}. \tag{3.15}$$

The term i of $f_i = i\Delta F$ is moved to the exponent such that the equation (3.15) can be used. Thereby, the inner sum over i can be eliminated.

$$\underline{x}(t) = \sum_{m=-\infty}^{\infty} \left[\sum_{k=0}^{N-1} \underline{x}(kT_{symb} + mT_F) \frac{e^{j2\pi \Delta f (t - kT_{symb})N} - 1}{e^{j2\pi \Delta f (t - kT_{symb})} - 1} \right] g(t - mT_F). \tag{3.16}$$

Substituting Δf by $1/NT_{symb}$ the following expression is gathered:

$$\underline{x}(t) = \sum_{m=-\infty}^{\infty} \left[\sum_{k=0}^{N-1} \underline{x}(kT_{symb} + mT_F) \frac{e^{j2\pi \frac{t - kT_{symb}}{T_{symb}}} - 1}{e^{j2\pi \frac{(t - kT_{symb})}{NT_{symb}}} - 1} \right] g(t - mT_F). \tag{3.17}$$



(a) Hann window.

(b) Hamming window.

Figure 3.12: Simulated ACLR of the FDDAC transmitter for different FFT-lengths and window types.

The given expression fully describes the behaviour of the FDDAC-based transmitter including windowing, input signal type, and the DFT-length. Thereby, effects introduced in the discrete or continuous time-domain are considered. Furthermore, it can be translated into the frequency-domain to analyse the windowing performance mathematically. Besides that, this work includes numerical system models and simulations which are further used to analyse the effects of windowing on the system performance. Fig. 3.12 shows the relative signal power of the out-of-band emissions for different window types. By windowing, the spectral power in close proximity of the band is reduced even more. Additionally, increasing the DFT-length further improves the spectral shaping performance. However, the ACLR specifications given in the WiGig spectral mask can be achieved by a DFT-length of 8 where the suppression at $0.1BW$ already reduces to $-20\,\mathrm{dBc}$.

3.1.4 Fourier-domain analogue-to-digital converter based receivers - an outlook

The main emphasis of this work is laid on the transmitters for high data rate wireless transceiver systems. A proper Analogue-to-Digital Converter (ADC) is required in order to receive a wideband modulated signal. Therefore, a sampling rate of at least double the bandwidth with sufficient dynamic range must be provided. [42] provides the so-called Walden Figure-of-Merit (FoM) for state-of-the-art ADCs published in the highly reputed literature which is reproduced in Fig. 3.13. It is calculated by dividing the product of effective-number-of-bits and the sampling rate by the total

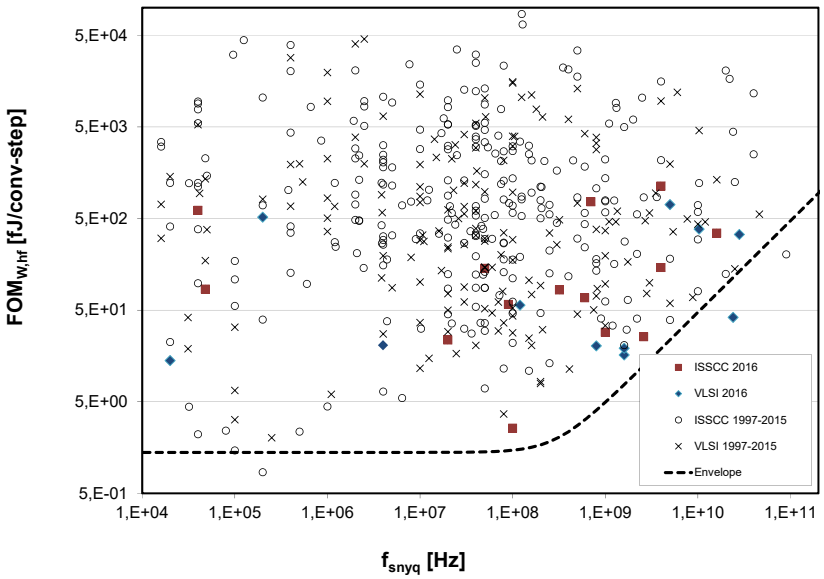


Figure 3.13: Walden FoM of state-of-the-art ADCs [42, 43].

power dissipation. Thereby, the FoM represents the power consumed to convert one bit from the analogue to the digital domain.
The lower boundary of the FoM is constant up to a certain sampling rate, approximately 200 MHz. For higher sampling rates it increases rapidly. Therefore, it seems to be advantageous to implement multiple ADCs which operate at lower sampling rates and thus achieve an overall better FoM compared to a single ADC operating at much higher speed. Several approaches such as time interleaving and their advantages and disadvantages are discussed in the literature. A summary of state-of-the-art ADC types can be found in the master thesis [43]. Furthermore, this master thesis discusses an ADC technique exploiting a similar principle as the FDDAC. A receiver structure is implemented based on multiple ADCs, each processes only a certain frequency portion of the input signal. Together they implement an analogue-to-digital conversion sampling the Fourier coefficients of the input analogue signal. Consequently, the DSP-block calculates the IDFT of the Fourier coefficients in order to reconstruct the analogue time-domain signal. Fig. 3.14 shows a simplified block diagram of the Fourier-Domain Analogue-to-Digital Converter (FDADC) based receiver. The sampling rate of the ADCs is reduced by $2M$ for M bins, whereas the number of the utilised ADCs is increased by the same number. The analogue input signal at any arbitrary frequency is fed to I/Q downconversion mixers moving each subchannel corresponding to the bin frequency to DC. The downconverted signal is weighted and integrated realising a lowpass filter. The ADCs sample the mean value of the signal power which is concentrated in a certain frequency range and, hence, the Fourier coefficients.
A transceiver system based on a FDDAC and FDADC can transmit and receive a wideband modulated signal. The utilised mixed-signal blocks such as the ADCs

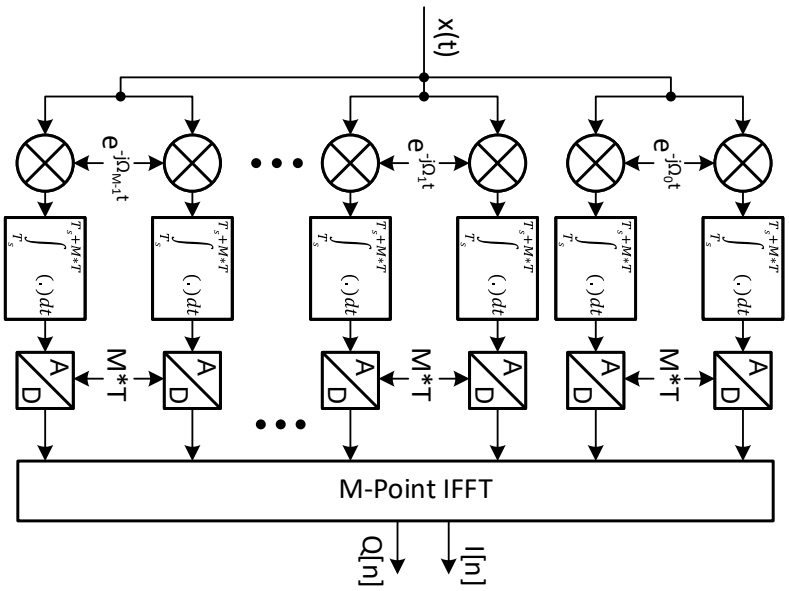


Figure 3.14: Simplified block diagram of the FDADC-based receiver [43].

and the DACs sample at a significantly lower speed than conventional converters. Advantageously, the phasor tones of the transmitter can be reused for the receiver if the number of utilised bins in the transmitter and receiver is selected identical, $M = N$.

3.1.5 Discussion

The proposed FDDAC approach requires barely a fraction of the sampling rate regarding the digital signal processing and sampling speed of the DAC cells compared to a conventional transmitter while being able to process complex wideband signals. The required sampling and DSP speeds can be reduced by up to two orders of magnitude for the same bandwidth. Hereby, the design complexity of both the DSP and analogue-mixed-signal circuit blocks such as the DAC cells and buffering trees is reduced significantly. Furthermore, no digital filtering with high oversample ratios is needed, since the continuous inverse Fourier transformation intrinsically performs a bandpass filtering which is improved by the introduction of the window function. The theoretical examination of the proposed concept demonstrates its spectral shaping capabilities in terms of reduced out-of-band emissions. The listed properties of the FDDAC-based data converter are promising for the application in low-power and wide modulation bandwidth transmitters. Thus, high data rates and increased dynamic range even for modulation bandwidths in the gigahertz range can be achieved. At the same time, digital signal processing is greatly relaxed compared to all state-of-the-art transmitters.

Consequently, the proposed approach targets and overcomes the limitations both in the DSP blocks and in the mixed-signal/analogue components such as DACs. In general, the proposed digital analogue conversion technique can be applied for a wide variety of applications where a wideband coherent digital signal needs to be converted. Furthermore, the introduced delay in the signal processing and digital-to-analogue conversion is considerably low which makes the FDDAC-based transmitter an eligible candidate for high data rate low latency wireless communication systems. A similar technique can be applied for the receiver which, in turn, enables a complete transceiver system based on Fourier-domain data converters.
Nevertheless, the simultaneous generation of N equidistantly spaced frequencies can be a challenge to be considered in integrated circuits. Providing those signals from external sources even for a proof-of-concept is not feasible since a high number of I/O pins need to be reserved for that. Chapter 5 presents various methods to integrate the frequency synthesis for the phasor tones. Furthermore, the complete FDDAC, the DSP and the frequency synthesis blocks need to be synchronised at specific sample points of the complete transmitter. Besides omitting several limitation and bottlenecks of conventional transmitters, the proposed topology comes with new challenges and increased design complexity on system-level. In the next subchapter, a transmitter prototype will be examined in order to understand and analyse the performance of the FDDAC-based transmitter with nonideality effects of the used system components.

3.2 System-level study

The main objective of the FDDAC-based transmitter is efficiently converting a wideband complex-valued digital signal into the analogue domain. Additionally, a frequency shift can be implemented easily. Modern wireless communication standards such as the fifth generation (5G) evolve to all-in-one solutions combining previously different communication standards. 5G covers a wide variety of services which span from narrowband Internet of Things (IoT) communications to very high data rates. Currently, 5G standards utilise communication in the already congested sub-6 GHz range to ensure rural coverage at reduced bandwidths and the mmW frequencies around 28 GHz for urban and midrange high data rate communication [44, 45]. However, the unlicensed ISM band at 60 GHz provides wider available spectrum for even higher bandwidth which can be used in order to overcome the capacity restrictions of the 28 GHz band. In combination with the significant channel losses due to the resonance of O_2 in the air, the 60 GHz frequency band is crucial for high-density femto-cells in overpopulated urban areas [46, 47]. Consequently, several standards need to be operated in modern hand-held devices which introduce carrier frequency relocation from several hundred megahertz up to the mmWs. Therefore, multistandard transmitter architectures are

required in order to achieve manageable production cost. In this regard, the proposed FDDAC-based transmitter is used to directly reconstruct the transmit signal in the sub-6 GHz range, in turn, the transmitter architecture in this particular case is direct transmission. However, the generated signal in the sub-6Hz range can be upconverted to either the 28 GHz or 60 GHz mmW frequencies, if demanded. Thereby, the architecture is changed to a heterodyne transmitter. Fig. 3.15 shows the block diagram of the

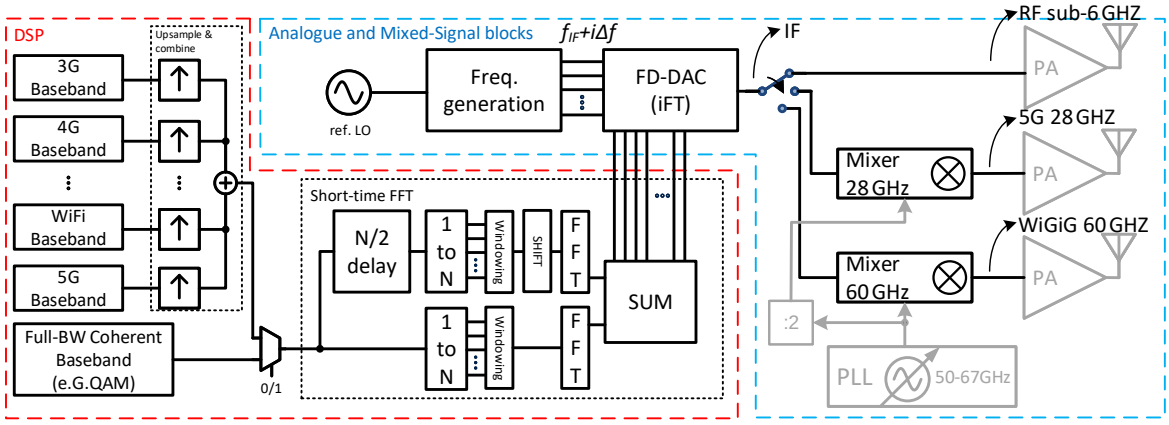


Figure 3.15: Block diagram of the proposed FDDAC-based transmitter prototype.

FDDAC-based transmitter prototype. Competitive integrated transmitters for wide modulation bandwidth [7] based on conventional approaches depend on very advanced technology nodes which, significantly, improve the performance of integrated digital circuits. However, this is not necessarily required due to the architectural benefits in DSP and sampling rates of the proposed digital analogue conversion technique. The main goal of this thesis is the integrated implementation of the transmitter in a fairly modern CMOS process such as the 65 nm TSMC Low Power (LP) RF technology. It is commonly used and well established since 2005. The transmitter is divided in two main blocks, namely the DSP and the analogue-mixed-signal. It uses a single FDDAC which can convert a wideband modulated digital signal or multiple narrowband signals of different standards into the analogue domain. Depending on the transmit band, the output signal of the FDDAC can either be directly transmitted in the sub-6 GHz range or shifted to the desired carrier frequency by a corresponding upconversion mixer. Thereby, the operation mode toggles between homodyne and heterodyne transmitter as described in Chapter 2. The transmit signals are then fed to different Power Amplifiers (PAs). The implementation of the greyed out PAs and the mmW Phase-Locked Loop (PLL) is not a matter of this thesis and is not further considered. The PAs are considered as ideal components. A single PLL directly generates the LO of the 60 GHz mixer, whereas the same signal at half the frequency is fed to the 28 GHz mixer. Therefore, the design and architecture of the upconversion mixers shall be considered wisely to reduce the fractional bandwidth of the single mmW Phase-Locked Loop (PLL) generating the LOs. The frequency range of both LO signals further depends on the

FDDAC output frequency considered as IF in the heterodyne mode. The IF signal to be upconverted is in the sub-6 GHz range and specifically selected to be centred at 3 GHz to 5 GHz. The third harmonic of the lowest frequencies of the modulated band shall provide a sufficiently high distance to the highest frequency components of the band in order to suppress distortions. The IF is set at a reasonably high frequency due to the wide modulation bandwidth. Consequently, the smallest fractional tuning range for the mmW-PLL can be achieved by implementing the 28 GHz upconversion block as a lower-side band mixer and the 60 GHz upconversion block as an upper-side band mixer. Thereby, the fractional bandwidth of the required mmW-PLL is below 30%. The highest modulation bandwidth for the targeted standards is supported in the 60 GHz band where WiGig offers a single-carrier modulation bandwidth of up to 1.86 GHz. Therefore, the modulation bandwidth of the sub-6 GHz FDDAC is selected to be 2 GHz. Additionally, the DFT-length is set to 16 which is a trade-off for the hardware complexity and the achievable spectral shaping performance. Thereby, the equidistant spacing of the phasor tones is 125 MHz. Furthermore, the DFT-length can be reduced to 8 which leads to a modulation bandwidth of 1 GHz. This operation modus is referred as the Half-Bandwidth-Mode (HBM). In this mode, the transmit frequency can easily be changed by multiples of 125 MHz by varying the used I/Q transmit cores within the FDDAC.
The FDDAC block receives the preprocessed Fourier coefficients from the digital block and the equidistantly spaced frequencies implementing the phasors then directly reconstructs the analogue output signal with a frequency shift. The output frequency of the FDDAC is processed by multiple I/Q transmit cores and needs to be synthesised simultaneously and, hence, the maximum output frequency is limited by the utilised technology. Furthermore, the frequency synthesis block performs the synchronisation of the synthesised tones.
For carrier frequencies in 28 GHz and 60 GHz, the channel provides reduced multipath fading. Especially for the latter, in most cases the line of sight connection dominates. Therefore, single-carrier transmit schemes gain repeatedly importance in nowadays communication standards [48, 49]. The single-carrier transmit scheme is also supported by the WiGig standard in 60 GHz bands [5]. A single-carrier transmitter based on the FDDAC can be easily implemented by feeding the raw bit-stream into a digital modulator and considering the complex symbol sequence as the input signal to be converted into the analogue domain. This is considered as the coherent full-bandwidth modulation. The proposed data converter approach utilised in a transmitter can be used to transmit multiple narrowband communication signals instead of one single coherent band. Therefore, multiple narrowband communication standards can be processed on corresponding DSP blocks and upsampled to the Nyquist frequency of the operation bandwidth of the FDDAC. As illustrated in Fig. 3.16, each communication band is than multiplied in the digital domain with a corresponding digital LO signal to arrange them within the transmit bandwidth of the utilised FDDAC. The sum of multiple rearranged bands is than converted simultaneously into the analogue

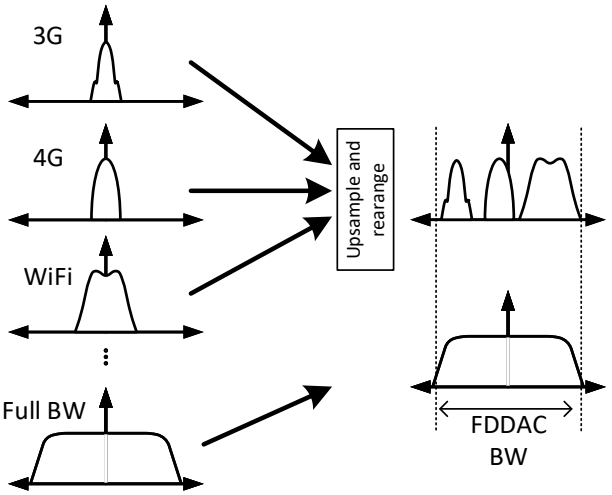


Figure 3.16: Visualisation of different transmit schemes of the FDDAC transmitter.

domain to their corresponding transmit frequencies. Besides the ability of transmitting multiple narrowband signals, the main focus in this thesis is laid on the single-carrier full bandwidth modulation. The wide modulation bandwidth perfectly embodies the capabilities of the proposed data conversion technique.

3.2.1 System-level modelling of the FDDAC-based transmitter and design space exploration

The proposed prototype is implemented based on models with different abstraction degrees in order to perform system-level simulations. These simulations are carried out to analyse the prototype and, especially, the new FDDAC in a real transmitter architecture. One of the main advantages of system-level simulations is their simple reconfigurability which can easily be adapted to structural changes in order to evaluate different topologies. Furthermore, the required computation power and, hence, the simulation time is significantly less compared to a direct implementation on transistor level. The model of the prototype is used to estimate the performance of the complete system which is measured in terms of EVM and the spectral purity of the generated output signal. Considering the utilised blocks as ideal components without any performance limitations, an upper boundary for the transmitter performance is determined. The utilised ideal blocks are then successively replaced by models representing realistic and physically available performances and nonidealities in order to localise possible systematic bottlenecks which, in particular, needs to be considered for implementation. The system-level model is further used to derive the specifications for each subblock in order to remain a certain performance.

Fig. 3.17 illustrates the block diagram of the model of the proposed transmitter. It contains several blocks and their nonidealities are considered in the model. The model is implemented in *Matlab*® based on sampled discrete-time simulations. Thus, the time step of the simulation is selected to be several magnitudes lower than the symbol duration which approximates the continuous-time.

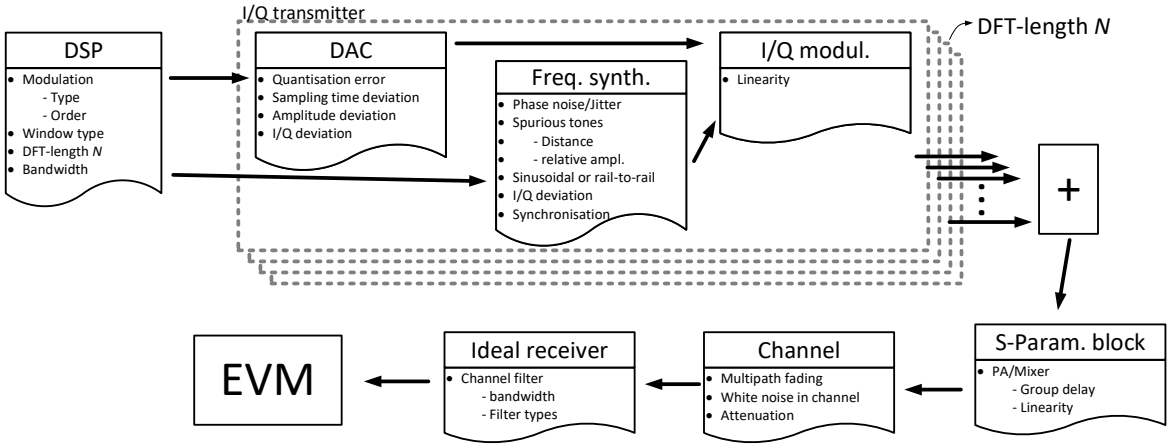
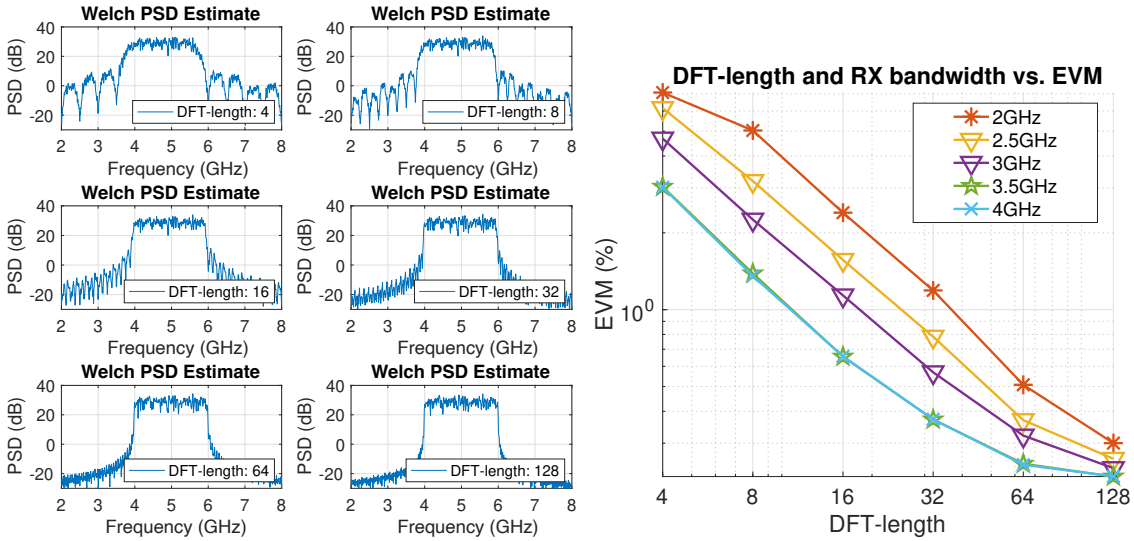


Figure 3.17: Block diagram of the system model of the FDDAC-based transmitter containing different building blocks and their considered nonidealities.

In the system-level simulation, the DFT-length and, hence, the number of the implemented I/Q transmit cores, the modulation-order and modulation-type alongside with the carrier frequency in the sub-6 GHz range can be changed. The baseband signal is based on a pseudorandom bit-stream which is modulated by the quadrature amplitude I/Q modulator as described in Chapter 2. The modulation bandwidth is 2 GHz although it can be changed easily. Furthermore, multiple narrowband signals can be fed to the transmitter model instead of a coherent baseband signal occupying the complete modulation bandwidth of the FDDAC transmitter. After each simulation, the EVM performance and output spectrum of the complete FDDAC is examined. The transmitter model further includes random seed generation for every simulation iteration. Thereby, random processes which follow a certain distribution can be analysed by running the simulation multiple times.
The system-level model assumes that the digital signal processing containing the windowing and FFT blocks are processed with a sufficiently high word-length such that no overflows, truncations and significant quantisation errors exist. The window type applied in the DSP can be changed to investigate the effects in correlation to other nonidealities. The default window used is a Hann window.

3.2.2 Model-based transmitter analysis

3.2.2.1 DFT-length versus the receive filter bandwidth



(a) Output spectra for different DFT-length.

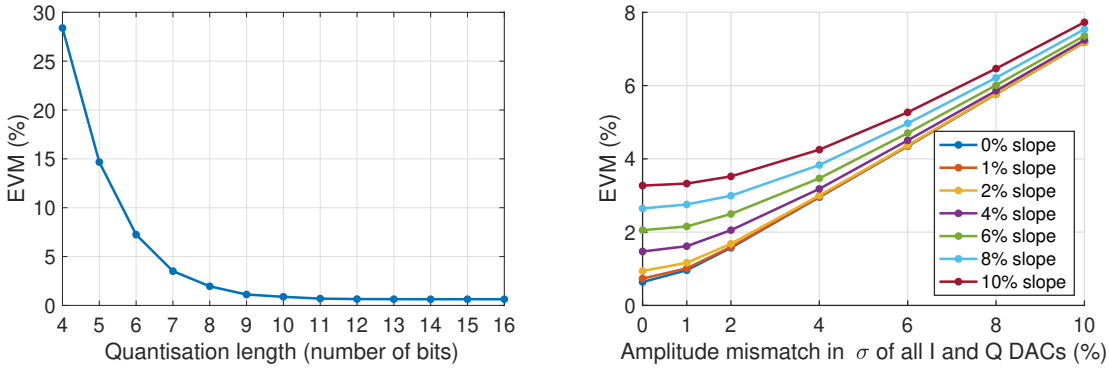
(b) Simulated EVM.

Figure 3.18: Simulated output spectrum for varying DFT-length and an the corresponding EVM performance according to receive the filter bandwidth.

The modelled prototype utilises a bandwidth of 2 GHz with a modulation order of 16QAM which relates to a data rate of 8 Gbit/s and a symbol duration of 500 ps. The output frequency in the sub-6 GHz range spans between 4 GHz to 6 GHz. Fig. 3.18 shows the simulated Welch Power Spectral Density (PSD) at the output of the FDDAC and the EVM for different DFT-lengths. Furthermore, the bandwidth of the ideal bandpass filter is varied which is used in the ideal receiver that calculates the EVM. As discussed previously, a low DFT-length leads to elevated out-of-band emissions which apparently carry information and need to be processed by the receiver. In order to achieve a low EVM for a low DFT-length the receive bandwidth needs to be significantly higher than the actual modulation bandwidth. For increasing DFT-length the out-of-band emissions decay and, hence, a narrowband receive filter results in a good EVM performance. However, the necessity to increase the receive filter bandwidth in order to achieve a reasonable high EVM performance translates into a degradation in spectral efficiency. As discussed previously, the introduction of windowing reduces the out-of-band emissions significantly. Nevertheless, a minimum DFT-length of 8 shall be selected to limit the out-of-band-emissions and to not exceed the WiGig transmit mask. A maximum DFT-length of 16 is chosen for the integrated implementation of

the FDDAC-based transmitter. Thereby, the spectral efficiency is improved and the receive filter does not need to be significantly larger than the modulation bandwidth.

3.2.2.2 DAC quantisation and mismatch effects versus EVM performance



(a) For different quantisation lengths of the DACs.

(b) Varying amplitude mismatches and constant amplitude slopes over the bins.

Figure 3.19: Simulated EVM for nonidealities introduced by the DACs such as the quantisation error, amplitude mismatches, and constant slopes.

The quantization noise introduced by the I/Q DACs in the transmit cores is examined. The DSP calculates the Fourier coefficients with a 32-bit accuracy in *Matlab*® which is considered as ideal. The utilised DACs are fed with the truncated coefficients with a word width that matches the number of bits of the implemented DACs. Furthermore, proper scaling before truncation is applied on the Fourier coefficients to reduce the quantization error to a minimum. The EVM performance of the complete transmitter is evaluated by keeping all other components ideal and sweeping the quantization length. Fig. 3.19a shows the simulated EVM. As described in Chapter 2, the implementation complexity of a DAC strongly depends on the achievable effective number of bits. In this particular test case, a DFT-length of 16 is utilised. The EVM improves drastically up to 10-bits and for increasing quantisation length, a saturation in the improvement is observed. Fig. 3.20 shows the output spectrum of the FDDAC-based transmitter for different quantisation lengths. A severe limitation of the quantisation length to 4-bits leads to a minor deterioration of the spectral purity. The close-by spectral components remain unchanged even tough the out-of-band emissions and, especially, the signal power at frequencies far away from the band increase.
Fig. 3.19b shows the effects of amplitude mismatches of the DACs on the EVM. Here, each I and Q DAC amplitude is varied separately. The applied variation follows a Gaussian distribution with a mean value of 100% which represents the ideal full

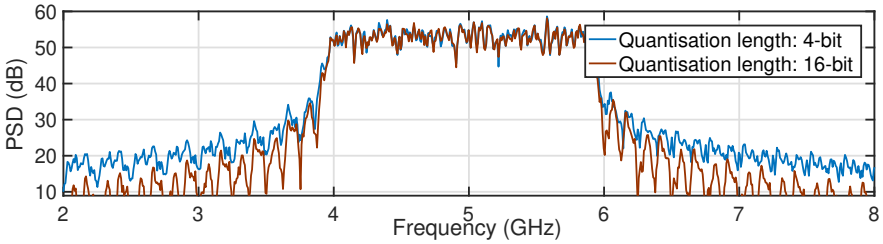


Figure 3.20: Simulated PSD of the FDDAC-based transmitter for different quantisation length.

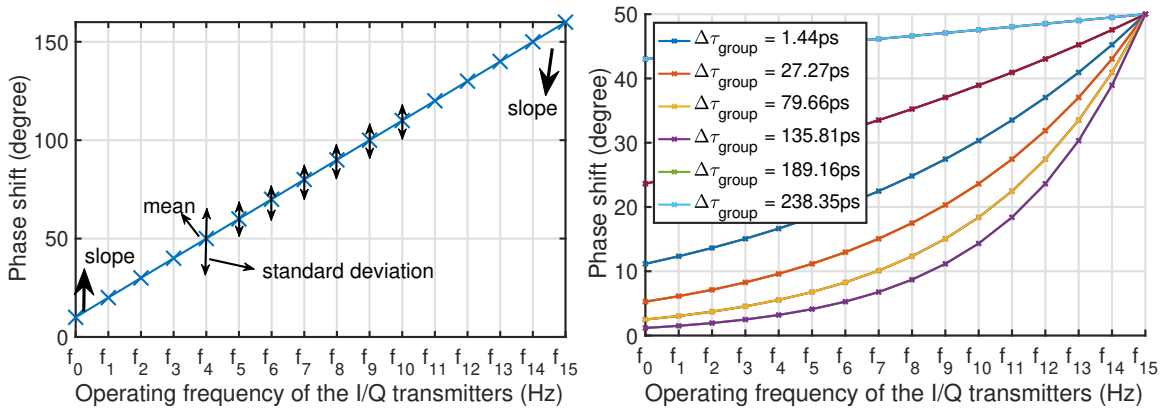
swing amplitude at the given standard deviation σ which is varied in the simulation. Additionally, an amplitude gradient is modelled which weights the bin operating at the lowest frequency with 100% and applies a linearly decreasing slope with a total amplitude difference of up to 10%. The simulation results stress on the importance of matching between the applied DACs. However, amplitude gradients over the bins are less critical compared to the normal distributed amplitude mismatch although their effect is not negligible and needs proper controlling such as calibration methods.

3.2.2.3 Deviations in the phase transfer functions of the utilised I/Q transmit cores

The synchronised and ideal phasor tones are modulated by the complex Fourier coefficients converted into the analogue domain by an I/Q modulator. The output of each bin experiences a different phase shift due to the varying frequencies of the phasor tones. The phase transfer function of the applied I/Q modulators or any other components on the signal path deviates over frequency and shows a mismatch from one to another I/Q transmitter core. This phase deviation over the I/Q transmit cores needs to be analysed besides the amplitude deviations and gradients considered so far. The group delay, τ_{group}, is calculated as follows:

$$\tau_{group}(\omega) = \frac{\mathrm{d}\phi(\omega)}{\mathrm{d}\omega}, \tag{3.18}$$

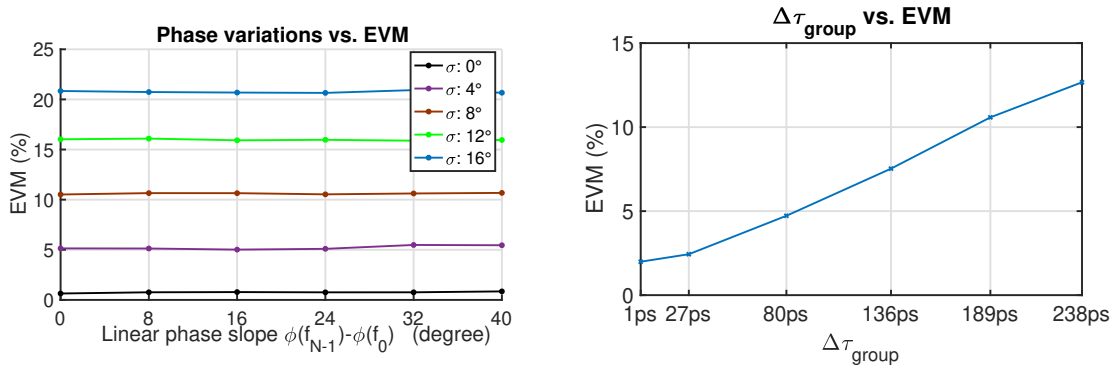
where the first derivative of the phase transfer function $\phi(\omega)$ represents the group delay. The group delay difference in the band, $\Delta\tau_{group}$, leads to Inter-Symbol Interference (ISI) and, hence, needs to be reduced to a fraction of the symbol duration, T_{smyb}, [50]. For a constant group delay, the phase over frequency shall be linear. Therefore, several types of phase characteristics are modelled. Fig. 3.21a shows a linear phase over frequency with different points showing the operating frequencies of the I/Q transmit cores. The slope of this curve can be linearly adjusted. The circuits contributing to the



(a) Linear phase transfer function with a constant slope and distributed deviations.

(b) Exponential nonlinear phase transfer functions resulting in different $\Delta\tau_{group}$.

Figure 3.21: Different phase transfer function types and nonidealities modelled.



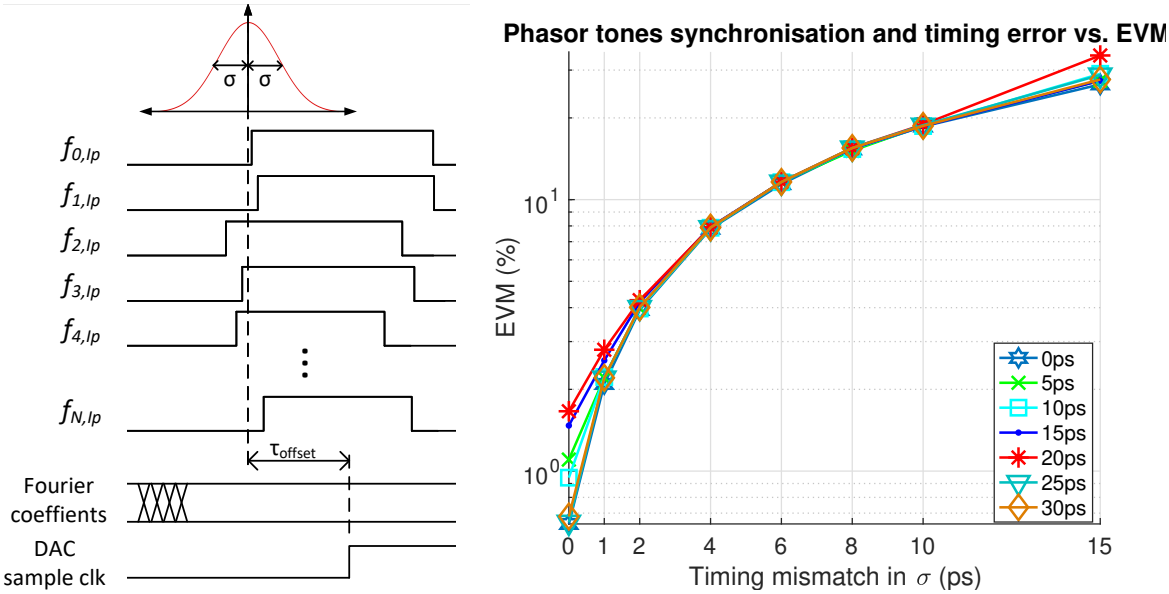
(a) Normal distributed phase along varying linear phase slopes as described in 3.21a.

(b) Exponential nonlinear phase transfer functions as described in 3.21b .

Figure 3.22: Simulated EVM for a linear phase transfer function with bin-to-bin variations and exponential nonlinear phase transfer functions leading to ISI.

phase noise might have certain inequalities from one bin to another due to production tolerances. Therefore, the phase delay added in each bin is normally distributed with a given standard deviation, σ, around the mean value preset by the linear phase transfer function, as shown in Fig. 3.21a. The deviation of the phase from the mean value leads to nonlinearities which, in turn, lead to a nonconstant group delay contributing to ISI. Additionally, Fig. 3.21b illustrates exponential nonlinear phase transfer characteristics. The gathered group delay is varying over frequency, where the calculated group delay deviation is given as $\Delta\tau_{group}$ in the graph as well.
Fig. 3.22 depicts the simulation results based in different phase transfer characteristics.

Fig. 3.21a shows the simulated EVM where the slope of the linear phase is varied. The EVM is not effected as long as the transfer function is linear. However, the mismatch in the phase transfer function being normally distributed for each I/Q transmitter worsens the signal quality. With increasing σ, the nonlinearity of the phase transfer function increases, in turn, the group delay variance over the transmit band increases. Fig. 3.21b illustrates the simulation results for an initially exponential and, hence, nonlinear phase transfer function. The results underline that increasing the group delay difference, $\Delta\tau_{group}$, effects the FDDAC-based transmitter as well and needs to be reduced to a certain level in order to not bottleneck the final transmitter performance.



(a) Synchronisation mismatch among the phasor tones; normal distribution and timing offset.

(b) Simulated EVM for varying timing mismatches.

Figure 3.23: EVM dependency on the timing mismatch including normal distributed misalignment and timing offset.

3.2.2.4 Synchronisation of the phasor tones among each other and relative to the sample time of the I/Q transmit cores

Another significant parameter which explicitly needs to be characterised is the synchronisation performance of the phasor tones among each other and the alignment to the sampling time of the DACs. It might be necessary to additionally include closed-loop

delay control circuits such as Delay-Locked Loops (DLLs) to synchronise the rising edges of the in-phase phasor tones depending on how the phasor tones are synthesized. Fig. 3.23a shows the delay mismatch types considered in the model. It is assumed that the in-phase and quadrature phasor tones preserve the 90° phase shift although in each bin the phasor tone experiences a different Gaussian distributed delay of which the standard deviation σ is varied. These delays are randomly generated for each simulation and multiple runs are performed to average the results. The delays remain constant which means that these synchronisation mismatches are constant errors for each simulation. Furthermore, an offset delay τ_{offset} is introduced modelling a constant delay difference between the mean time of the phasor tones synchronisation point and the DACs sampling time. Hereby, it is considered that there is no additional delay added by the DAC and the I/Q modulator block which multiplies the DAC output with the phasor tones. Fig. 3.23 shows the simulated EVM performance. Based on these simulations, it is obvious that the synchronisation of the phasor tones among each other is crucial since increasing σ has a severe effect compared to the offset delay τ_{offset}. However, it is important to mention that a standard deviation of $\sigma = 4\,\text{ps}$ does not denote the maximum delay mismatch. Multiple simulations are performed for a DFT-length of 16 with each σ value. The observed maximum delay difference between the phasor tones is approximately 4σ. However, the constant delay mismatch can be significantly reduced with a closed-loop synchronisation block.

3.2.2.5 Constant and distributed I/Q phase misalignments

To this point, it was assumed that the the in-phase, I, and quadrature, Q, components of the phasor tones have the same delay mismatch. However, in a real system either integrated or based on of the-shelf-components it is not possible to guarantee that the phase relation between the I and Q signals remains 90°. The frequency synthesis block which is the source of the phasor tones can generate the tones already with a constant I/Q phase error. Furthermore, both signals travel different and probably not perfectly identical paths which can result in different I and Q delays within the implemented I/Q transmit cores. Furthermore, the N frequency sources generate the signals with deviating initial I/Q phase errors. In this scenario the I/Q phase error varies for each I/Q transmit core. Therefore, the model considers these two types of phase error. A constant phase error of 0 to 4° is added to all phasor tones. Additionally, a normal distributed I/Q phase mismatch is implemented of which the standard deviation, σ, is swept. Fig. 3.24 illustrates the EVM of the FDDAC transmitter for various I/Q phase deviations. Based on the results, both the constant and Gaussian distributed phase errors effect the performance of the transmitter and need to be kept limited.

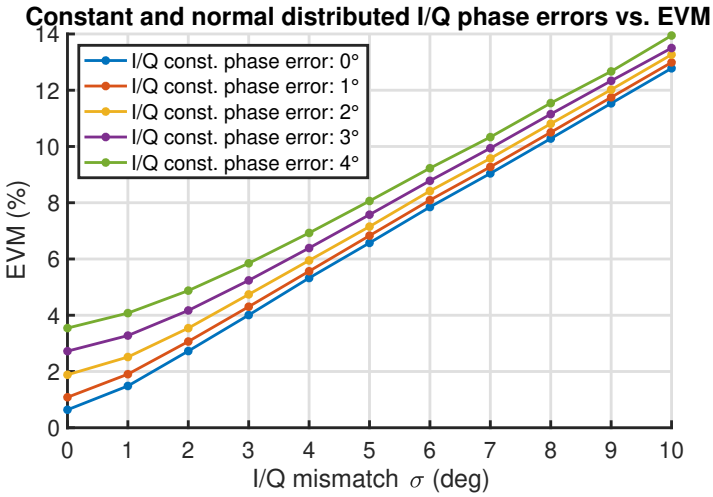


Figure 3.24: Simulated EVM performance versus different types of I/Q errors.

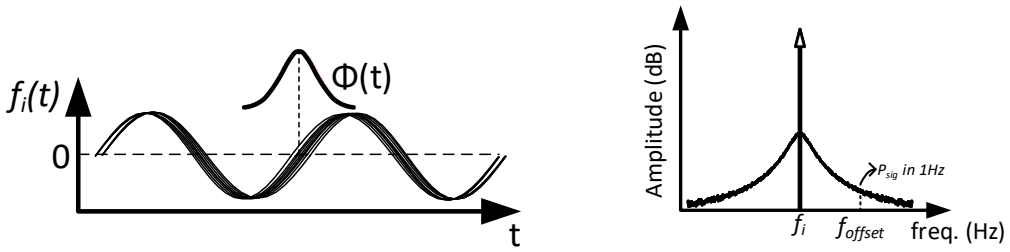
3.2.2.6 phase noise and spurious tones

The synchronisation of the phasor tones strongly impacts the transmitter performance. Therefore, it is important to further analyse the phasor tones and the effect of their nonidealities on the transmitter performance. The frequency synthesis block simultaneously generates equidistantly spaced phasor tones. In addition to the normal distributed constant timing mismatches, and the timing offset, τ_{offset}, the modelled frequency synthesis block takes into account phase noise, spurious tones at different power levels and frequency distance to the considered tone, constant I/Q phase errors and different type of the tones either sinusoidal or rectangular. The phasor tones are continuous wave signals at specific frequencies in the sub-6 GHz range. Especially, the phase noise and spurious tones which lead to a periodic and random jitter need to be analysed carefully since they represent a dynamically varying phase and timing error. Considering a signal at the frequency, f_i, the phase noise can be modelled as follows:

$$f_i(t) = sin\left(2\pi f_i t + \phi(t)\right). \tag{3.19}$$

Here, a phase offset, $\phi(t)$, is added which follows a stochastic distribution process which depends on the frequency generation block. Fig. 3.25a shows the phase noise in the time-domain which relates to a cycle-to-cycle jitter that leads to a change in the instantaneous frequency. phase noise, $\mathcal{L}(f)$, is measured and characterised in the frequency-domain, as shown in Fig. 3.25b, by the relative signal power dBc/Hz to carrier frequency and an offset frequency, f_{offset}:

$$\mathcal{L}(f) = \frac{\text{Signal power in 1 Hz}}{\text{Integrated signal power}}. \tag{3.20}$$



(a) Illustration of a sinusoidal tone with normal distributed jitter.

(b) Jitter in frequency-domain represented as phase noise.

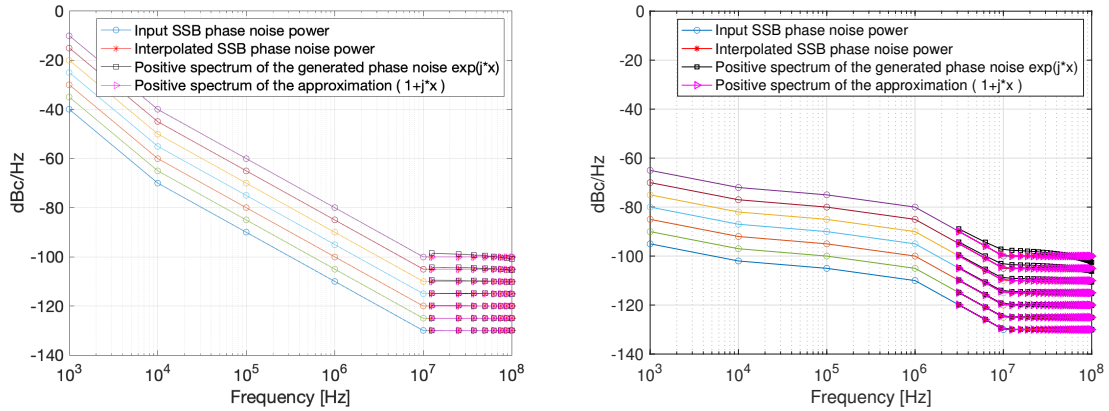
Figure 3.25: Jitter in the time-domain and phase noise in the frequency-domain.

Frequency synthesisers usually contain an oscillating block which is controlled in a closed-loop system to oscillate at the desired frequency. However, different types of oscillators such as ring-oscillators and Voltage-Controlled Oscillators (VCOs) and their combination with various closed-loop control topologies lead to different phase noise characteristics, respectively [51, 52]. As described in [53], the phase noise behaviour of a free-running feedback oscillator can be divided in three sections. The phase noise performance in the close proximity to the oscillation frequency is limited by the flicker noise introduced by the gain stage. The flicker noise exhibits a decay of approximately 30 dB per decade. The phase noise in the second section is dominated by the quality factor of the oscillation and can be approximated with a slope of 20 dB per decade. For an increasing frequency offset to the oscillation frequency the phase noise becomes flat and is determined by thermal noise. Moreover, in the system model of the FDDAC transmitter independent noise on each I and Q phasor tones are assumed. In the model, two vectors are used to define the phase noise characteristics. The frequency vector, V_f, defines the offset frequencies at which the phase noise values, V_{pn}, in dBc/Hz are given in Table 3.1.

V_f	= [1e3	10e3	100e3	1e6	10e6	100e6]	(Hz)
$V_{pn,fr}$	= [-30	-60	-80	-100	-115	-120]	(dBc)
$V_{pn,PLL}$	= [-85	-92	-95	-100	-115	-120]	(dBc)

Table 3.1: Modelled phase noise vectors.

The given vectors approximate the phase noise characteristic of a free-running VCO, $V_{pn,fr}$, with different slope regions as discussed previously. However, a proper PLL improves the phase noise performance of a free-running oscillator up to a certain offset frequency defined by the bandwidth of the loop filter acquired in the PLL. The improved phase noise is given by the vector $V_{pn,PLL}$. Thereby, different phase noise characteristics are tested in order to model the impact of the phase noise performance of



(a) Free-running VCO phase noise $V_{pn,fr}$. (b) VCO with PLL phase noise $V_{pn,PLL}$.

Figure 3.26: Different phase noise characteristics at various levels.

an oscillator with and without a closed-loop system. Note that both phase noise vectors provide $-100\,\mathrm{dBc/Hz}$ at 1 MHz offset frequency although the $V_{pn,PLL}$ has comparably reduced noise power at low offset frequencies. Fig. 3.26a and 3.26b show phase noise curves which are moved along the y-axis for different simulations. The phase noise is applied on each in-phase and quadrature phasor tone using the function described in [54]. Here, the phase noise curve is interpolated between the given points. Therefore, a filter is generated to provide a transfer function according to the interpolated input. Consequently, the filtered white noise is added to the complex input signal where the phase noise power is normalised and scaled depending on the power of the input signal. Transient phase noise simulations require extremely high computation power, especially considering the simulation time which needs to be sufficiently long. Here, the simulations are carried out for 163840 symbols which translates to 81.92 us. With the given simulation time, phase noise effects as close as 12 kHz offset frequency are considered.

Fig. 3.27 shows the phase noise simulation for varied phase noise levels. The reference point, phase noise at 1 MHz, for both cases a free-running and a controlled oscillator are varied and the achieved EVM performance is plotted. The oscillator controlled by a PLL delivers relatively better performance since the free-running oscillator has unfiltered phase noise at low frequencies. This relation is not typical to the proposed FDDAC-based transmitter, although it shows the importance of a proper signal synthesis for a transmitter with extreme wide modulation bandwidth.

Fig. 3.28 shows the EVM performance versus the phase noise performance for varying timing mismatches. The graph shows that the timing mismatch limits the EVM performance for phase noise performances better than $-95\,\mathrm{dBc}$ at 1 MHz. On the other hand for deteriorating phase noise performance the timing mismatch becomes negligible.

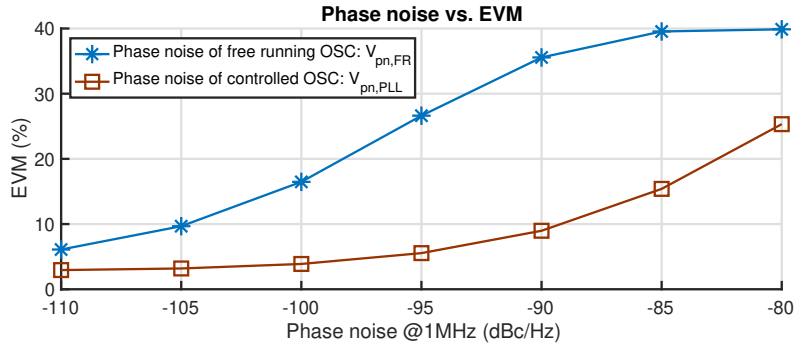


Figure 3.27: Simulation results showing the calculated EVM for varying phase noise measured at 1 MHz offset frequency for the two different characteristics shown in 3.26.

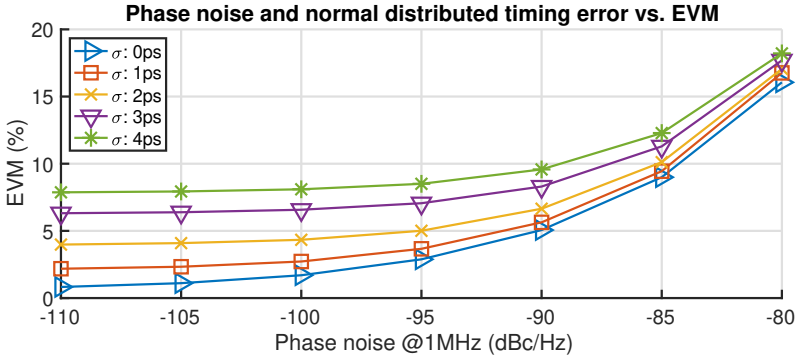


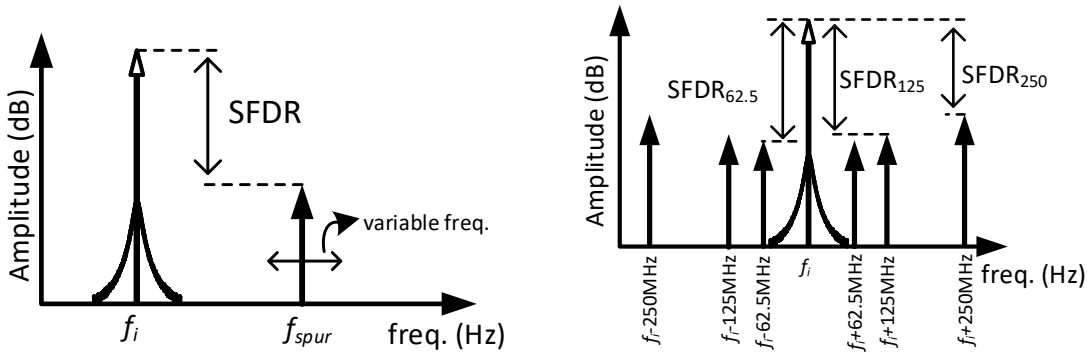
Figure 3.28: Simulated EVM performance over phase noise performance for varying timing mismatches.

Spurious tones are deterministic signals with a concentrated power at a specific frequency which superimpose with the actual signal. The presence of a single or multiple spurious tones limits the Spurious-Free Dynamic Range (SFDR) of the actual signal. SFDR is measured in the frequency-domain in a certain frequency range around the desired signal and is given in dBc which is the power difference between the power of the desired signal versus the highest spurious tone power. For a signal at the frequency, f_i, the spurious tones can be modelled as follows:

$$f_i\left(t\right) = sin\left(2\pi f_i t\right) + A_{spur,1} sin\left(2\pi f_{spur,1} t + \phi_{spur,1}\right). \tag{3.21}$$

In the given example, a single spurious tone at the frequency, $f_{spur,1}$, with an amplitude of $A_{spur,1}$ is added to the actual signal. The model-based design space exploration and evaluation of the FDDAC-based transmitter are performed for a DFT-length of 16 and a modulation bandwidth of 2 GHz. Thus, the frequency spacing between the simultaneously persisting phasor tones is 125 MHz. Depending on the physical spacing

of the I/Q transmit cores and the frequency generation blocks it is possible that the phasor tones suffer from leakage. In this case, spurious tones at multiples of a 125 MHz frequency offset would be generated. Furthermore, additional spurious tones can be generated directly in the frequency generation block. In order to understand the effect of the frequency of the spurious tones, each phasor tone is generated with a spurious tone at varying frequencies and constant SFDR, as shown in Fig. 3.29a. Fig. 3.29b shows the simulation setup with multiple spurious tones at different frequency offsets. The spurious tone at a distance of 250 MHz is added since it is the DAC update rate in this configuration. When all DACs sample at the same time, a peak current will be conducted from the supply which can cause a supply bouncing leading to spurious tones. The remaining spurs at 62.5 MHZ and 125 MHZ model the leakage from the phasor tones of the adjacent I/Q transmit cores and spurious tones generated in the frequency synthesis block, respectively. The levels of all spurious tones are predefined and their scaling is swept in order to show the impact on the transmitter performance.



(a) Variable frequency and amplitude spur. (b) Modelled spurious tones at various offsets.

Figure 3.29: Different types of modelled spurious tones.

Fig. 3.30 shows the EVM of the transmitter where each I and Q phasor tone has one spurious tone with the given SFDR and the distance to the actual frequency. Interpreting the simulation results, it is apparent that the placing of the spurious tones in the frequency does not have a significant impact. However, the EVM slightly degrades when the frequency of the spur is 125 MHz away from the actual tone. Furthermore, the SFDR of the phasor tones has a severe impact on the achieved EVM. Therefore, additional simulations are performed where spurious tones as depicted in Fig. 3.29b are applied to the phasor tones. The scaling is swept as follows:

$$\mathrm{SFDR}_{62.5} = 37\,\mathrm{dB} + A_{scale},\ \ \mathrm{SFDR}_{125} = 35\,\mathrm{dB} + A_{scale},\ \ \mathrm{SFDR}_{250} = 32\,\mathrm{dB} + A_{scale}. \tag{3.22}$$

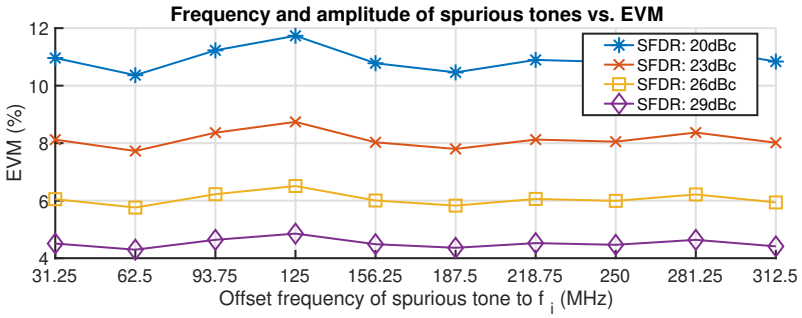


Figure 3.30: Simulated EVM of the FDDAC-based transmitter according to the offset frequency and amplitude of one single spur per phasor tone.

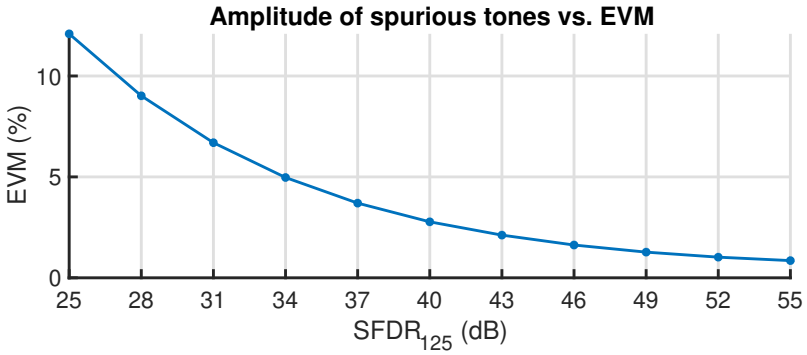


Figure 3.31: Simulated EVM versus the SFDR of the phasor tones. Note, that all spurious tones shown in 3.29b are scaled relative to the spur at 125 MHz.

The simulation results are summarised in Fig. 3.31. The scaling value, A_{scale}, is swept which changes the amplitude of all spurious tones. The graph shows the obtained EVM performance versus the SFDR evaluated at a frequency offset of 125 MHz.

3.2.3 Transmitter performance estimation and definition of subblock specifications

The FDDAC-based transmitter is modelled by taking into account different kinds of nonidealities. The model is used to understand the design space in terms of specifications of the used subblocks by evaluating the EVM and output spectrum for various specifications. Furthermore, it is used to localise bottlenecks which might severely effect the transmitter performance compared to other nonidealities. The knowledge base gained by the system simulations will be used for the following steps:

1. The novel transmitter approach is analysed and implemented based on numerical models of electronic blocks. The FDDAC-based signal processing, the modelled transmitter, and the appropriate demodulation of the generated signal demonstrates a first software based proof-of-concept.

2. Understanding the new concept and localisation of the bottlenecks severely limiting the transmitter performance in terms of EVM and spectral shaping performance.

3. A literature survey will be carried out to estimate the achievable performance of the utilised subblocks which, in turn, are used to feed the model with more realistic parameters. Thereby, realistic system specifications can be assumed.

4. Avoidance of over-engineering which means if one of the specifications already limits the performance in such a way that other specifications can be relaxed without decreasing the overall system performance. This information can be used to simplify the components which require most of the chip-area, power or design complexity.

5. Postmeasurement debugging and analysis. Any unexpected deviation during the measurement process can adapted to the model. For example it is possible to include the S-parameter models of the used filters, amplifiers, and bias-tee easily to simulate their effects.

3.2.4 Specifications of subblocks versus transmitter performance

The main target of the thesis is the implementation of a highly integrated FDDAC-based transmitter prototype in a modern CMOS technology as introduced in Section 3.2. The components which are included into the prototype such as the DSP, generation of the phasor tones, DACs, I/Q modulators and several different components have a strong impact on the transmitter performance. Therefore, a detailed literature survey is carried out and experimental circuits are designed to find the performance limitations of these blocks in the used CMOS technology. These specifications are fed into the generated model which, in turn, delivers a reasonable performance expectation.
The proposed technique does not require a high-speed DSP. For the targeted 2 GHz modulation bandwidth and the DFT-length of 16, the DSP operates at 250 MHz. Compared to the DFT processors introduced in [55] and [56], the required FFT blocks can easily be integrated due to the significantly lower DFT-length and intended sampling rate. The DAC and I/Q modulator can also be implemented in a single block by using a Radio Frequency Digital-to-Analogue Converter (RF-DAC), [57].

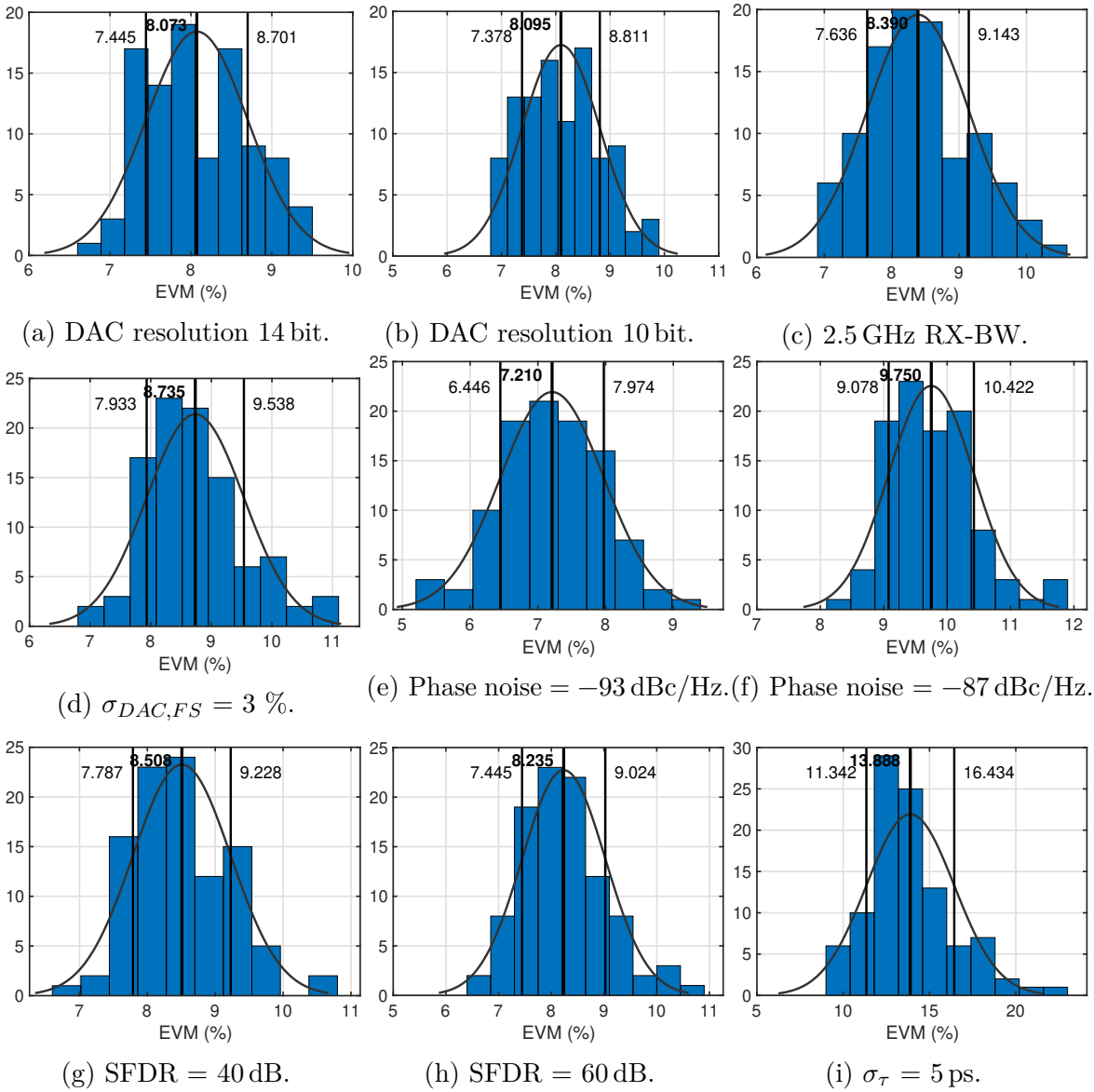
There is a multitude of publications showing the advantages and achieved performance of RF-DACs. [58] introduces a 13-bit I/Q RF-DAC with up to 154 MHz modulation bandwidth and a well controlled linearity. The matching between the I and Q DACs across the bins is assumed to have a normal distributed full-scale amplitude deviation, $\sigma_{DAC,FS}$, of less than 2%. Additionally, the amplitude of the DACs is varied over the bins by 2% to model frequency-dependent amplitude variations. Linear changes of the phase transfer function do not effect the transmitter performance although the deviations from bin to bin are considered by the normally distributed deviation $\sigma_{\phi(f)}$. The system-level simulations show that restrictions originating from the phasor tone synthesis severely limit the overall transmitter performance. The model measures the performance of the frequency synthesis in terms of the phase noise, SFDR, and the synchronisation performance. [59] demonstrates a VCO-based PLL with a phase noise of −140 dBc at 1 MHz. [60] demonstrates a ring-oscillator-based PLL with a phase noise of −109 dBc at 1 MHz. A conservative and pessimistic PLL phase noise characteristic of −90 dBc at 1 MHz offset frequency is assumed since multiple frequency sources need to be integrated. The SFDR of each phasor tone is 50 dBc limited by the 6 spurious tones as discussed previously. The initial parameter setup of the system-level model is listed in Table 3.2

DAC resolution	$\sigma_{DAC,FS}$	DAC slope	$\sigma_{\phi(f)}$	$\tau_{offset,const.}$	σ_{τ}	const. I/Q err.
14 bit	2%	2%	1°	2ps	2 ps	<3°

phase noise @ 1 MHz	SFDR phasor tones	Noise floor	RX filter BW
−90 dBc	>50 dB	55 dB	4 GHz

Table 3.2: Initial parametrisation of the FDDAC-based transmitter model.

The system-level simulations are sampled for 100 Monte Carlo runs, where the non-idealities follow the given distributions and the limits in the initial parameter setup. Fig. 3.32a shows the sampled EVM performance and the fitted Gaussian curve where the mean value is 8%. The previous analyses on the subblocks and the impact on the overall transmitter performance anticipates that certain design parameters bottleneck the achievable EVM. The remaining parameters can be relaxed without sacrificing the overall performance in case the restrictive parameters, $\sigma_{DAC,FS}$, $\sigma_{\phi(f)}$, $\tau_{offset,const.}$, and the phase noise cannot be improved. Fig. 3.32b shows the performance sampled for a reduced DAC resolution of 10 bits which significantly reduces the DAC complexity without increasing the EVM. The sampling from Fig. 3.32c is gathered by additionally reducing the receive filter bandwidth to 2.5 GHz. Furthermore, a mismatch between the DACs of up to 3% can be tolerated which in average only leads to an increment of the EVM by 0.04%. The sampled results are shown in Fig. 3.32d. Alternatively, the transmitter performance is analysed by changing only the limiting parameters in



(a) DAC resolution 14 bit. (b) DAC resolution 10 bit. (c) 2.5 GHz RX-BW.

(d) $\sigma_{DAC,FS} = 3$ %. (e) Phase noise = −93 dBc/Hz. (f) Phase noise = −87 dBc/Hz.

(g) SFDR = 40 dB. (h) SFDR = 60 dB. (i) $\sigma_\tau = 5$ ps.

Figure 3.32: Monte-Carlo sampling of the transmitter performance based on 100 runs for different parameter sets. (a) Initial parameter setup, (c) - (d) consecutive changes added to the initial setup, (e) - (i) initial setup with single parameter variation.

the initial set in order to examine the performance gain if the limiting parameters could be improved. Fig. 3.32e shows the sampled EVM for a phase noise performance which is improved by 3 dB to 93 dB. It leads to an average EVM of 7.2%. In contrast, a reduction of the phase noise performance by 3 dB to 87 dB increases the EVM to 9.75% as shown in Fig. 3.32f. The variation of the SFDR does not significantly effect

the EVM performance as shown in Fig. 3.32g and 3.32h. One of the most significant parameters limiting the transmitter performance is the synchronisation of the phasor tones among each other. Therefore, the parameter σ_τ which represents the synchronisation performance is changed while keeping the remaining parameters as in the initial setup. Fig. 3.32i shows the Monte-Carlo sampling for $\sigma_\tau = 5\,\text{ps}$. The average EVM is thereby increased to nearly 14%.

3.2.5 Discussion

The FDDAC is adapted into a transmitter topology and its performance is analysed. Therefore, a system-level model is created which takes various nonidealities originating from different subblocks into account. The top-down design methodology allows to perform simulations at certain abstraction levels by using a significantly less computation power compared to transistor level simulations. It further enables reconfigurability. Thereby, different DFT-lengths and modulation bandwidths can be adapted. Simulation times in millisecond range can be achieved to analyse the effect of phase noise at low-frequency offsets. The simulations lead to a deeper understanding of how the performance of each subblock effects the transmitters EVM and output PSD. Initially, isolated single parameter sweep simulations are performed considering the remaining subblocks as ideal. Thereby, potential bottlenecks are localised. Additionally, a literature survey is carried out and based on that an initial set of parameters reflecting the achievable performance of each subblock is estimated. The system-level model parametrised with conservatively assumed subblock performances from the literature proves that a modulation bandwidth of up to 2 GHz can be achieved in the targeted technology. The EVM performance of the transmitter correlates to the data rate. In order to maintain a certain Bit Error Rate (BER), coding is applied which, in turn, occupies a large raw data rate overhead if the EVM performance is not sufficient.
Furthermore, the system-level model is used to define the specifications of the subblocks without overengineering single blocks if the performance is already limited by other parameters. In this particular case, the specifications can be relaxed without distinctly sacrificing the transmitter performance. Alternatively, the potential performance gain is analysed in case the limiting parameters can be improved. The experience gained by the model-based simulations will be used in further integration steps of the transmitter. The FDDAC is based on multiple I/Q transmit cores which need to be operated fully synchronised since any deviation in the phase and timing relation leads to a significant drop in the performance. Moreover, the phase noise performance plays an important role, yet this is not exclusive to the FDDAC approach. It mainly originates from the utilised wide modulation bandwidth.

3.3 Conclusion

This chapter introduced to the Fourier-domain digital-to-analogue converter. Initially, the fundamentals, working principles, opportunities and limitations are analysed based on a system theoretical and mathematical methodology. The exploitation of the relation between the DFT in the band-limited frequency-domain and the IFT in the continuous-time analogue-domain leads to conceptual advantages compared to conventional digital-to-analogue converters. The FDDAC approach enables the digital-to-analogue conversion of a wide bandwidth digital signal by omitting oversampling and filtering in the digital domain and yet generating a clean and spurious free analogue output signal. The output can be reconstructed at any arbitrary frequency. The FDDAC approach simplifies the digital signal processing by omitting the FIR filters and oversampling by replacing them with parallelised FFT blocks. Additionally, the sampling rate in the analogue-mixed-signal components such as the DACs are reduced, by up to two orders of magnitude. Accordingly, the concept allows converting wideband signals while substantially reducing the required power. It can further replace a multitude of dedicated narrowband transmitters, such as the ones used in cellular phones to cover different communication standards and worldwide frequency bands with only one highly reconfigurable and power-efficient Fourier-domain digital-to-analogue converter.
The FDDAC is a promising approach to be employed in wireless transceiver applications. Therefore, the concept is adapted within a transmitter prototype which targets a DFT-length of up to 16 and a modulation bandwidth of up to 2 GHz. A system-level model is implemented which is used to understand the FDDAC-based transmitters performance based on the specifications of the used subblocks. Thereby, possible limitations could be localised and a design space exploration could be carried out. Furthermore, the model is used to derive the specifications of the blocks in order to achieve a certain performance. The targeted application is *WiGig* at 60 GHz utilising a single-carrier modulation bandwidth of up to 1.76 GHz.
One of the advantages of the new FDDAC-based approach is that it uses blocks which are already employed in the conventional transmitter design. However, here multiple I/Q transmit cores with their dedicated frequencies regarding the IFT contribute simultaneously to the reconstruction in the analogue domain. The dedicated phasor tones are implemented by frequencies with equidistant spacing which turn to be a potential bottleneck if not synchronised properly across all I/Q transmit cores or no sufficient phase noise performance is available. The targeted wide modulation bandwidth of 2 GHz requires appropriate performance of the subblocks such as DACs, I/Q modulators, frequency synthesisers, *etc.* A hybrid FDDAC transmitter prototype might be useful in order to gain practical experience with the new approach before the integration step and to evaluate the developed system-level model.

Chapter 4

Hybrid FDDAC-based transmitter for sub-6 GHz applications

This chapter introduces the first hybrid FDDAC-based transmitter implementation. The proposed transmitter architecture is modelled and the specifications of several subblocks are analysed for a modulation bandwidth of up to 2 GHz. However, the FDDAC approach requires those subblocks to operate simultaneously in order to generate a coherent and wideband output signal. In the hybrid implementation, commercially available components are used to implement the transmitter which allows to focus the study on the simultaneous operation of multiple I/Q transmit cores rather than the performance of each subblock. Therefore, the hybrid implementation targets a modulation bandwidth of up to several 100 MHz and a limited DFT-length of 8. Furthermore, it offers simple trouble-shooting, tuning opportunities and fast redesign cycles compared to an integrated design.

4.1 Design space exploration for the hybrid FDDAC-based transmitter

Fig. 4.1 shows the block diagram of the hybrid Printed Circuit Board (PCB) based FDDAC transmitter implemented using commercially available off-the-shelf components. The targeted specifications are listed in Table 4.1.

Requirement	Value
DFT-length (number of I/Q transmitter cores)	8
Modulation bandwidth BW	up to 100 MHz
Frequency range	2.4 to 2.5 GHz (extendable)
DAC update rate f_u	max. 25 MHz
Modulation order	min. 16 QAM

Table 4.1: Hybrid FDDAC specifications.

The digital signal processing is performed on a Field Programmable Gate Array (FPGA) board, namely the *Xilinx Virtex-7*® XC7VX485T evaluation board. The FPGA and the components on the PCB are controlled over the USB-to-UART interface of the evaluation board by a host computer running *Matlab*®. A serial port is used to communicate with the FPGA board using USB. The relatively slow UART interface can further be used to transfer and store raw data on the FPGA which then is processed and forwarded to the FDDAC. Additionally, over a secondary SPI interface between the FPGA and the FDDAC the discrete components on the board can be setup and controlled. The FDDAC consists of multiple I/Q transmit cores each based on two

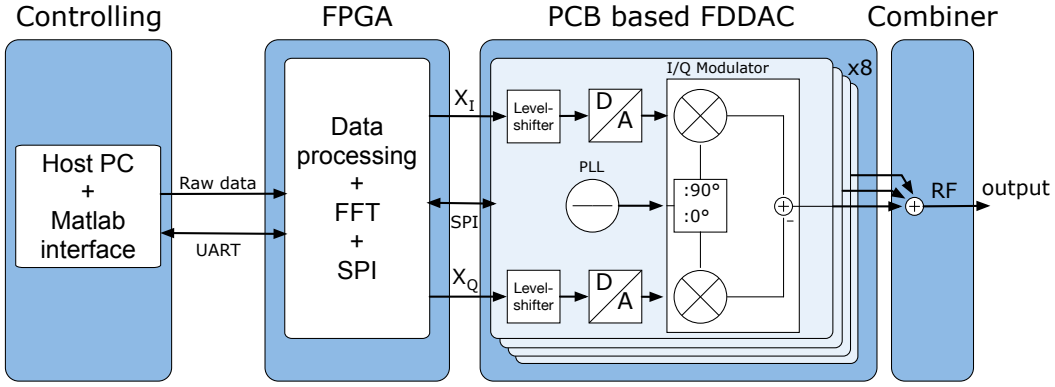


Figure 4.1: Block diagram of the PCB based and FPGA assisted hybrid FDDAC-based transmitter.

DACs for I and Q. A frequency source generates the LO signals with 90° phase shift representing the phasor tone. The I/Q modulator modulates the DAC output onto the corresponding phasor tones. The output of the I/Q modulators are summed to attain the reconstructed analogue output signal at the desired frequency. Table 4.2 shows the selected components. The utilised DAC, DAC5652, provides a resolution of 10 bit for I

Component	Function	Reference
LMX2572	PLL for phasor tone generation	[61]
DAC5652	I/Q DAC sampling the Fourier coefficients	[62]
TRF370417	I/Q modulator modulating the DAC output on the phasor tone	[63]
SN65LVDT388	LVDS receivers to convert the differential information signal into a single-ended one	[64]

Table 4.2: Core components of PCB based hybrid design.

and Q where the input words are sampled either subsequently using a single 10-bit input or parallel using two 10-bit inputs. The former option has the advantage of using less data lines between the FPGA and PCB while sacrificing transmit speed. The Fourier coefficients are updated with a data rate of 25 MHz considering the maximum BW and the DFT-length. In total, $8 \times 10 \times 2$ bits need to be transferred to the DACs within a time window of $1/(25\,\text{MHz})$. The *Xilinx Virtex-7*® FPGA VC707 evaluation board accommodates several high-speed communication interfaces like GTX, SFP+, gigabit Ethernet. These I/O ports do not provide the number of the required parallel lanes for the communication between the hybrid FDDAC and the FPGA board. Additionally, the evaluation board provides two FPGA Mezzanine Card (FMC) expansion connectors with 160 and 116 single-ended connections of which one is accessed by a break-out board. The used FPGA board only supports low-voltage output, where the logic high is represented by 1.8 V, in contrast, the DACs require at least a voltage of 2 V. Therefore, the Fourier coefficients are provided using Low-Voltage Differential Signaling (LVDS) by the FPGA. These signals are received by a level-shifter and LVDS-converter, TRF370417, on the PCB. The level-shifted and single-ended signals are fed to the I/Q DACs.
Based on system-level simulations, the synchronisation, of all PLLs generating the phasor tones among each other and to the DAC sampling time needs to be considered properly. Therefore, a single reference signal is utilised which is provided to the FPGA in order to calculate the Fourier coefficients and routed to all PLLs as a reference signal. Thus, the FPGA and the phasor tone generation operates synchronously. However, the digitally controlled delay tuning of the PLLs can be used for proper timing alignment.

4.2 Implementation of the PCB based hybrid FDDAC-based transmitter

Fig. 4.2 shows the block diagram of the single PCB hybrid FDDAC implementation. A previous version based on multiple stacked PCBs exhibited severe shortcomings in terms of supply instability and noise. In order to overcome those limitations, especially regarding the insufficient supply voltage stability, a PCB design is implemented which accommodates all 8 I/Q transmit cores on a single 4 layer FR-4 board which measures 320 mm×90 mm. A detailed discussion of this work is presented in [65, 66].

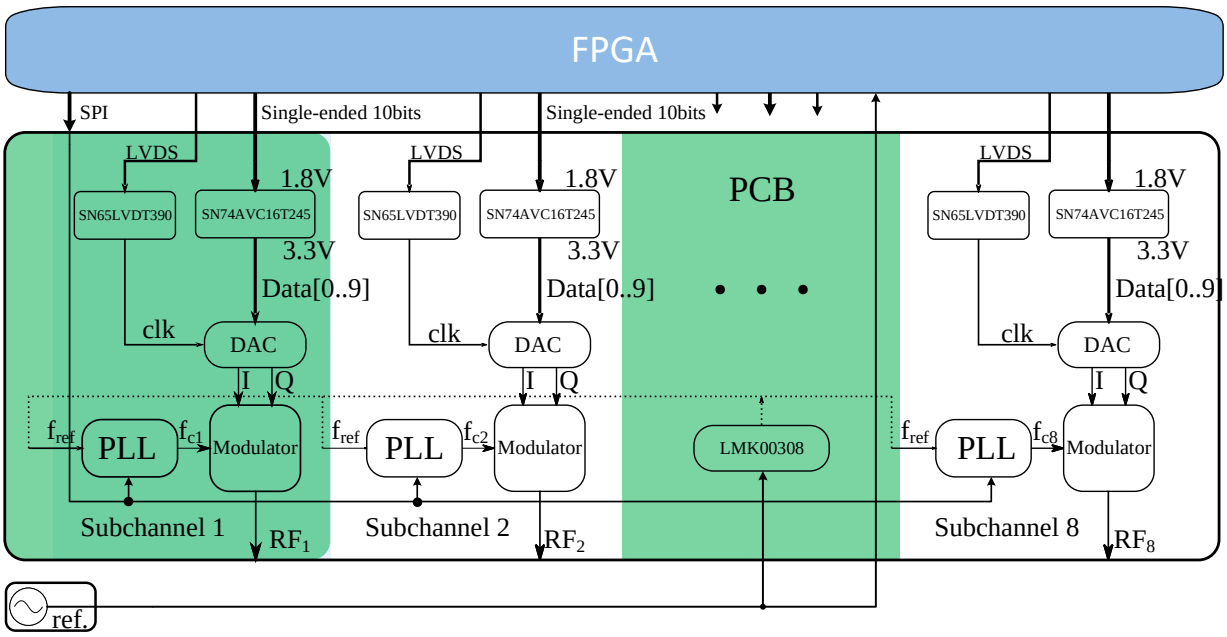


Figure 4.2: Block diagram of the single PCB implementation of the hybrid FDDAC-based transmitter.

The LMX2572 from Texas Instruments is chosen as a PLL on the individual bins of the FDDAC. It offers the ability to adjust the phase of its output digitally with a very high resolution. Additionally, it comes with a *sync* pin which can be used to align the rising edges of all phasor tones to the sampling time of the DACs. The fractional-N synthesizer covers a wide range from 12.5 MHz to 6.4 GHz. The PLL requires an external loop filter which has not to be of a high order if the loop bandwidth is narrow [61]. Therefore, a second-order loop filter with a maximum bandwidth of 100 kHz is implemented as suggested in the data sheet. The values for the loop filter components depend on the VCO gain, K_{VCO}, charge pump gain, K_{pd}, main divider ratio, N, which are constant for a given input and output frequency. The loop bandwidth, ω_p, and phase margin, ϕ_p, were swept over a specific range to get the resistor and capacitor values as close as

Frequency	C_1	R_1	C_2	ω_p	ϕ_p
2.406 25 GHz	9.09 nF	475 Ω	1.6 nF	95.05 kHz	47.61°
2.418 75 GHz	11 nF	432 Ω	2 nF	85.4 kHz	47.15°
2.431 25 GHz	9.1 nF	470 Ω	1.8 nF	91.36 kHz	45.78°
2.443 75 GHz	10 nF	464 Ω	1.6 nF	92.43 kHz	49.24°
2.456 25 GHz	11 nF	442 Ω	1.8 nF	87.34 kHz	48.88°
2.468 75 GHz	9.09 nF	475 Ω	1.8 nF	90.69 kHz	45.76°
2.481 25 GHz	7.5 nF	523 Ω	1.5 nF	99.29 kHz	45.6°
2.493 75 GHz	10 nF	453 Ω	2 nF	85.77 kHz	45.6°

Table 4.3: Values of discrete elements corresponding to the output frequency and the resulting phase margin and loop bandwidth [68].

possible to the components of E96-series [67] since the loop filters are implemented by discrete components. The sizes of the loop filter components for each frequency are given in Table 4.3. Note that the selected frequencies represent the phasor tones with an equidistant spacing equal to the targeted bandwidth divided by the DFT-length, namely 100 MHz/8 = 12.5 MHz. The PLLs are configured over the SPI which is generated on the FPGA. A single SPI interface is used to configure all 8 PLLs.
The acquired PLL has two outputs where one is fed to the I/Q modulator and the other to a secondary output for monitoring purposes. The output of the PLL does not provide the 90° phase shift. Thus, the used I/Q modulator is specifically selected to have its own 90° phase shift.
The I/Q modulator, TRF370417, from Texas Instruments is used to modulate the analogue Fourier coefficients on the LO input provided by the PLL. A common-node voltage of 1.7 V has to be applied on the I/Q inputs to provide optimum performance. This can be realised by a resistor network as mentioned in [63]. The operation range of the modulator spans from 50 MHz to 6 GHz. Furthermore, the output is matched to 50 Ω. An appropriate power combiner providing a sufficiently high isolation between the port can be used to sum the output of the bins sustaining the reconstructed signal in the analogue RF domain.
The data lines to the FPGA are separated in order to further isolate the bins from each other. The number of available IO pins on the break-out board attached to the FMC connector is limited to 160 single-ended connections. Therefore, the new sampling scheme involves a single-ended connection instead of LVDS. Additionally, the DACs sample over the single 10-bit input the real, I, and the imaginary, Q, coefficients subsequently. In total, 80 data lines are reserved to address the 8 I/Q transmit cores which requires 20 reference clock cycles of the FPGA in order to sample all Fourier coefficients. The single-ended communication instead of the LVDS is prone to bit-errors even though the sampling rate on the data lines between the FPGA and the FDDAC

are reduced. The negative input of the LVDS receivers are set to 0.9 V which is half of the voltage swing on the data lines. Thus, the LVDS receivers are used as level-shifters only. The clock signals sampling the data and finally triggering all DACs to convert the sampled words into the analogue domain are still provided using LVDS connections from the FPGA.

4.2.1 Reference clock distribution

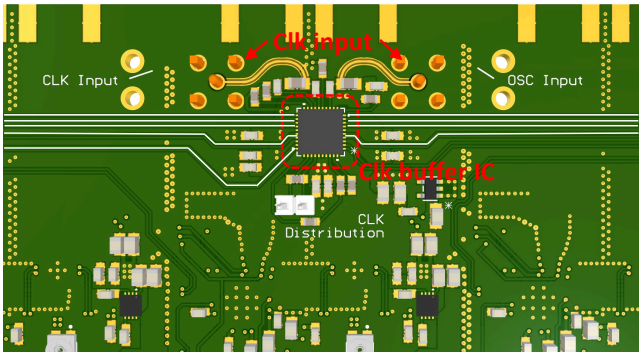
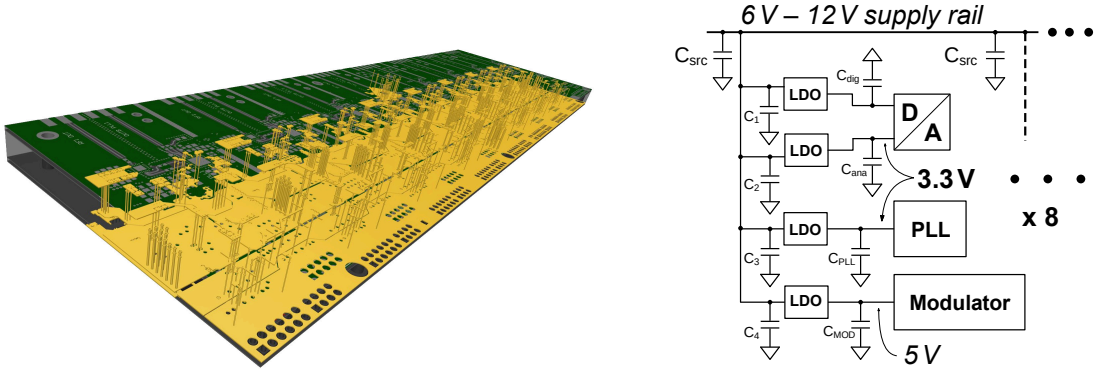


Figure 4.3: Back side of the PCB showing the placing of the clock buffer and the equal length routing.

A 100 MHz reference signal is provided through a power splitter to the FPGA board and to the FDDAC board. On the FPGA board, integrated PLLs are used to generate the required operating frequency which is synchronous to the reference. Multiple PLLs with the ability to synchronise their output to the reference are used on the FDDAC board. Therefore, it is important to deliver all reference signals to all PLLs with the same delay. This is achieved by using a distinct clock buffer, LMK00803, with 8 differential clock outputs [69]. It is placed in a central position on the back side of the PCB. However, the routing distance to the 8 I/Q transmit cores differs and causes a delay discrepancy. Fig. 4.3 shows the placing of the clock buffer and the length tuned reference signal distribution lines feeding the PLLs.

4.2.2 Supply voltage distribution

The supply voltage stability is one of the main reasons for the PCB redesign. Therefore, several optimisations regarding the supply voltage are introduced. In the stacked implementation, supply voltages have been forwarded to higher levels using the pin header based connections. The redesign accommodates all bins on a single 4-layer



(a) 3d graphic of the 4-layer PCB illustrating the power planes.

(b) Supply voltage distribution in a single I/Q transmit core. Several LDOs and decoupling capacitors are used.

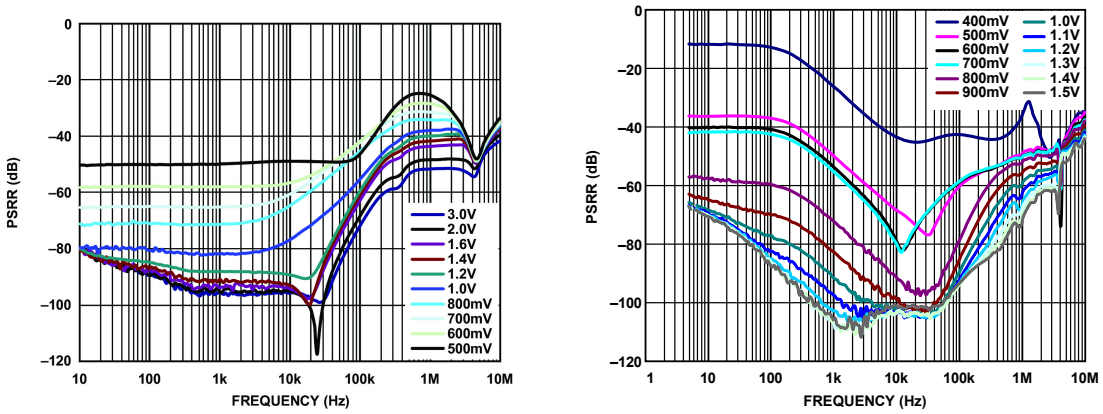
Figure 4.4: Supply distribution on the hybrid FDDAC PCB [65] ©2019 IEEE.

board. The amount of layers enables a higher routing density and also the introduction of power planes on the inner metal layers. In general, three major concepts are used to improve the supply voltage stability:

- Power planes deliver a low impedance source for different power consuming blocks. The input supply rail and supply rails of the I/Q transmit cores are on separated power planes.
- A tree of Low-Dropout Regulators (LDOs)s is used to isolate the supply of several blocks from the main rail.
- Attaching decoupling capacitors of different types and sizes in each supply domain before and after the LDOs.

Fig. 4.4a shows the large power planes representing the input supply rail. The input is applied at a single point and can be in a range from 6 V to 12 V. Several LDOs with different output voltages are used to generate the required 1.8 V, 3.3 V, and 5 V. Fig. 4.4b shows the block diagram of the power supply tree of a single I/Q transmit core. The voltages of the PLL and DAC within each I/Q transmit core are individually generated by different LDOs, ADP7118 [70]. Fig. 4.5a shows the Power Supply Rejection Ratio (PSRR) performance for different overdrive ratios. The PSRR describes the isolation of the supply noise between the output and the input of the LDO. In this way, significant current peaks taken by the DAC lead to a supply noise on its own supply domain. Nevertheless, the other blocks such as the PLLs are isolated by their own LDOs. Since the used I/Q modulators have a high power consumption, they are supplied by the LDO, ADM7150 [71]. The PSRR performance is shown in Fig. 4.5b.

Linear LDOs have a high power consumption when the overdrive voltage is increased. However, the PSRR also improves. Switching type regulators are not used even though a higher efficiency could be achieved. They add additional digital noise to the complete transmitter and require complex external passive networks. Thereby, power efficiency is sacrificed for the sake of voltage stability and simplicity. Additionally, in each supply domain decoupling capacitors are used to reduce the noise on the supply voltages.



(a) PSRR performance of the ADP7118 at 3.3 V output voltage [70].

(b) PSRR performance of the ADM7150 at 5 V output voltage [71].

Figure 4.5: PSRR performance of the used LDOs for varying overdrive voltages.

4.2.3 Wilkinson 8-to-1 Power combiner

Regarding the FDDAC approach, the reconstructed analogue signal is gathered after the summation of all modulated phasor tones which are generated by the transmitter PCB. Therefore, an additional block is required that is able to provide a 50 Ω load to each I/Q modulator and sum the output signals. Furthermore, the combiner shall achieve a sufficient isolation between the ports and deliver appropriate matching regardless the operation point of the other modulators since no information about load modulation is provided. Therefore, a Wilkinson combiner is implemented. In total, seven 2-to-1 combiners are required in order to combine 8 signals. Fig. 4.7a shows the schematic of the combiner. Initially, a one 2-to-1 combiner is designed to cope with the defined transmitter parameters such as the centre frequency at 2.45 GHz. The implemented combiner is then cascaded to achieve the required combination ratio. Fig. 4.6 shows the complete hybrid FDDAC PCB with the 8 bins and the attached Wilkinson combiners. The outputs which will be fed to the combiner are placed on the long edge of the PCB. The area of the substrate shall be kept small in order to

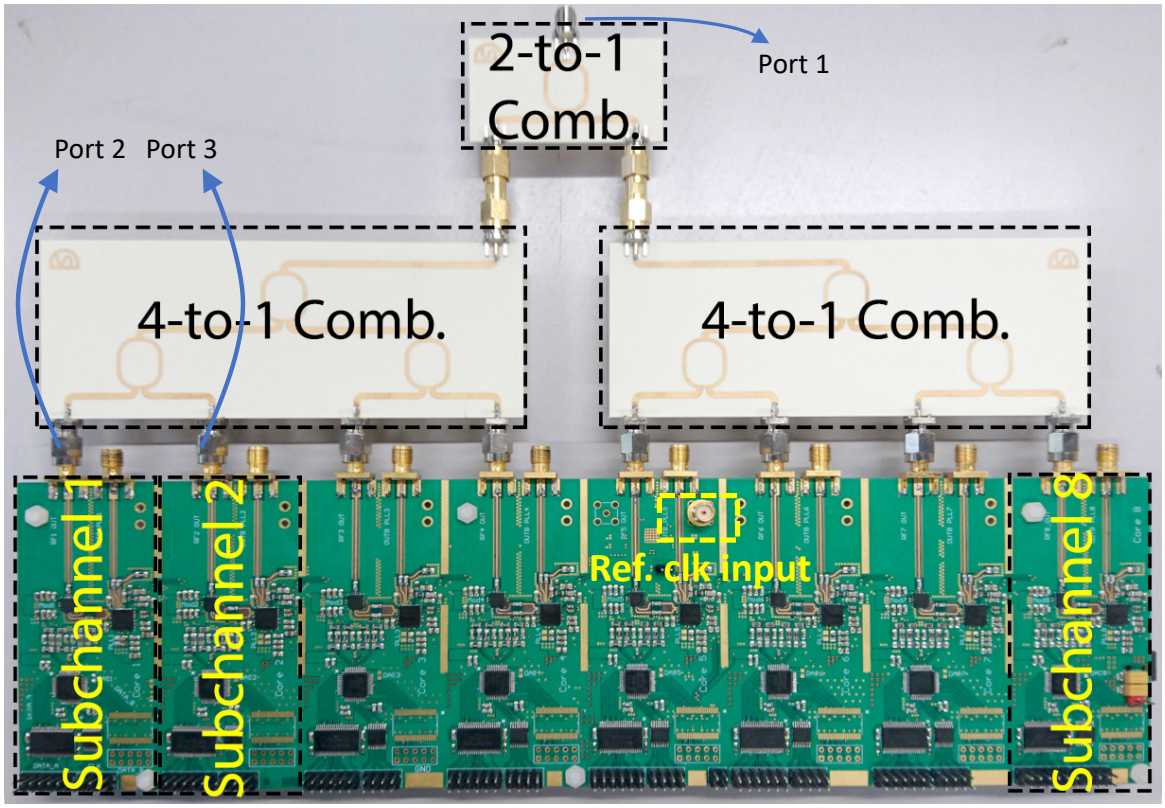
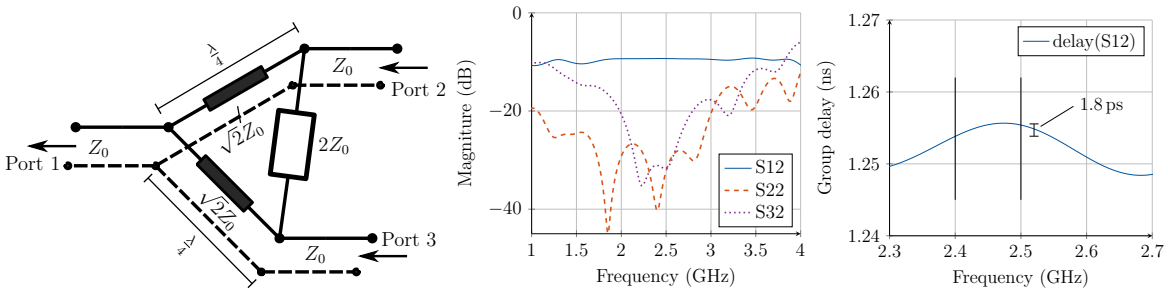


Figure 4.6: Photograph of the single PCB hybrid FDDAC-based transmitter including the 8-to-1 Wilkinson combiner.

achieve homogenous etching. Therefore, the 8-to-1 combiner is divided in three different segments, namely two 4-to-1 and one 2-to-1 combiners. The Wilkinson combiners are designed on a Rogers substrate using *Keysight ADS*® EM simulation tool. Fig. 4.7 shows the simulation results of the 8-to-1 combiner including the SMA connectors in the interstage. As expected, the transmission loss is flat and close to −9 dB and the isolation between the input ports is better than −30 dB. Another significant parameter is the group delay of which the deviation within the 100 MHz of transmit bandwidth is less than 1.8 ps.

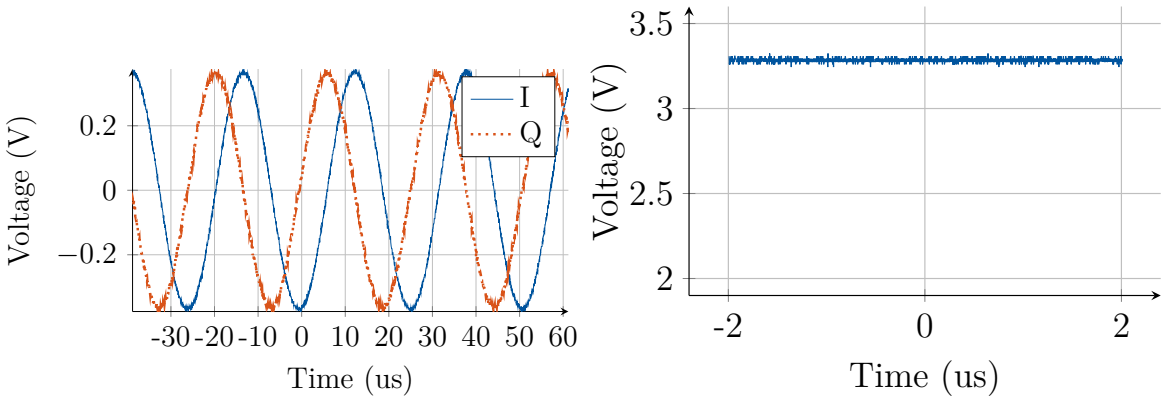
4.3 Measurement results and discussion

The single-board hybrid FDDAC introduced several methods to improve the supply stability in the complete system. In order to characterise that, all DACs are activated and a digital sinusoidal tone is provided by the FPGA. Fig. 4.8a shows the measured



(a) Schematic. (b) Insertion and transmission loss. (c) Group delay.

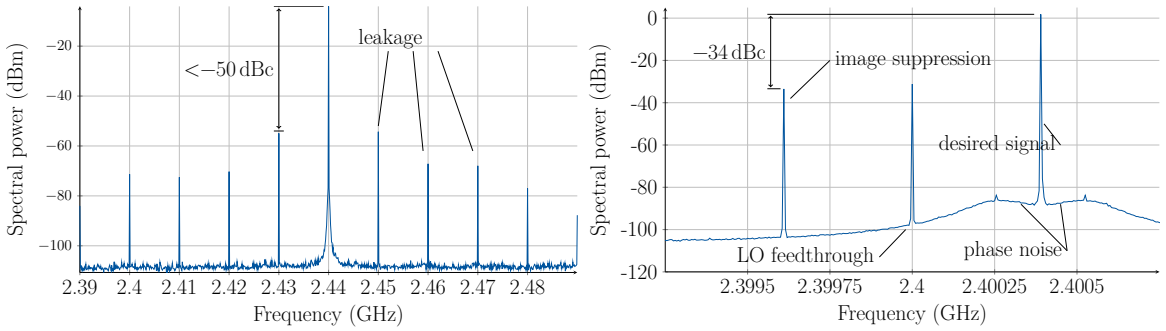
Figure 4.7: Schematic of a single Wilkinson power combiner and simulated S-parameters of the 8-to-1 Wilkinson combiner [65] ©2019 IEEE.



(a) Measured DAC output. (b) Measured supply voltage of the DAC.

Figure 4.8: Measured transient signals at the DAC output and supply pins while all 8 I/Q transmit cores are activated and sampling the digital sinusoidal tones.

transient sinusoidal signals at the output of one DAC while the remaining 7 are operating as well. Fig. 4.8b shows the supply voltage of the DAC in the mean time. Compared to the previous stacked hybrid FDDAC, the supply stability in the single-board implementation has been improved drastically. The peak-to-peak voltage swing is reduced from approximately 400 mV to less than 10 mV.
Fig. 4.9a shows the measured output spectrum of the PLL in the fifth I/Q transmitter. The frequencies of the PLLs are locked at frequencies between 2.4 GHz and 2.48 GHz with an equidistant spacing of 10 MHz. The measured spectrum shows besides the actual signal at 2.44 GHz, the leakage of the adjacent I/Q transmit cores. The leaked LO power of the adjacent bins has the highest power. Nevertheless, the amplitude of the leakage is low which leads to an SFDR of at least 50 dBc. A single-tone measurement is performed to analyse the performance of the I/Q transmit cores once all PLLs are locked. Therefore, a measurement setup is created where all bins are activated sampling



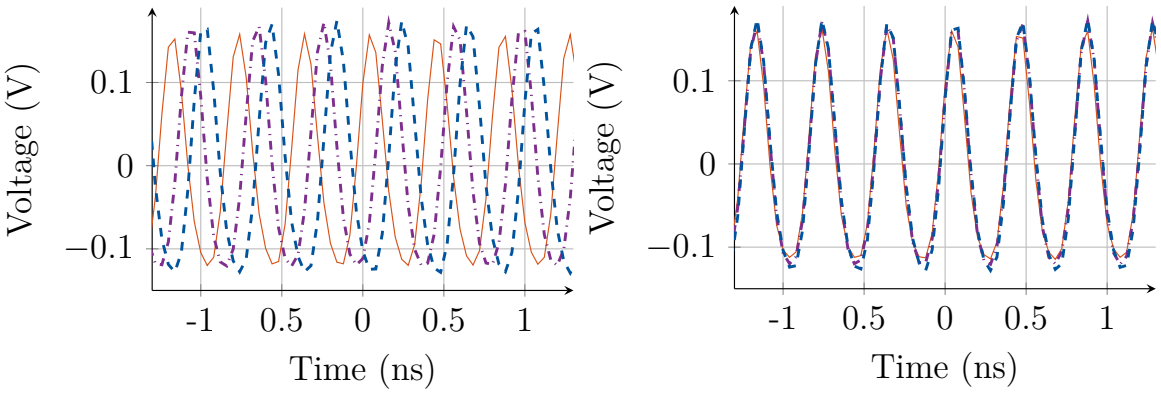
(a) Leakage and crosstalk of adjacent PLLs. (b) PSD of the single-tone measurement.

Figure 4.9: Measured PSD for different test setups.

the digital input whereas the output of one single I/Q modulator is fed to a signal and spectrum analyser. Fig. 4.9b shows the measured spectrum. In addition to the wanted mixing products, the image signal and the LO feedthrough can be observed. However, the unwanted signals provide a power of 34 dB less compared to the actual output. The performance of a single I/Q modulator can be improved for better image-rejection or less LO feedthrough. However, it is sufficient to demonstrate the FDDAC approach since one of the main advantages of the FDDAC transmitter is that it significantly relaxes the requirements per bin.

The FDDAC approach requires proper synchronisation which is achieved by providing the same reference signal to the DSP and the PLLs on the PCB. Additionally, phasor clocks and the sampling time of the DACs need to be aligned. Initially, all PLLs are programmed to generate the equidistantly spaced frequencies representing the phasor tones. After proper locking of the PLLs, a *sync* signal is sent to all PLLs such that the rising edge of the output signal is aligned with the next rising edge of the reference signal. The reference signal on the PCB is buffered by a distinct clock buffer and routed to the PLLs. The routing is done by length tuned lines. Thus, the delay from the clock buffer to each PLL is matched. Fig. 4.10 illustrates the synchronisation. Therefore, the output of three PLLs which are locked to the same frequency are sampled by a high-speed oscilloscope before and after sending the *sync* pulse. Once all 8 phasor tones are synchronised among each other, the DACs sampling time needs to be aligned to the same synchronisation point. This is achieved by the implementation of two different tuning mechanisms, namely a coarse and a fine tuning. The coarse tuning is performed by shifting the clock which triggers all DACs by the reference cycle of the FPGA, *i.e.* 5 ns. The fine tuning is achieved by the delay adjustment functionality integrated into the FPGAs IO ports with a step size of 75 ps. The tuning can be precisely performed by measuring and comparing the PLL and DAC outputs with a high-speed oscilloscope. However, it is also possible to adjust the tuning by observing the achieved EVM performance and sweeping through the tuning range.

The FPGA is set to process the actual baseband signal for the FDDAC approach once



(a) Before the *sync* pulse.

(b) After the *sync* pulse.

Figure 4.10: Measured PLL output signals at 2.45 GHz showing the synchronisation performance.

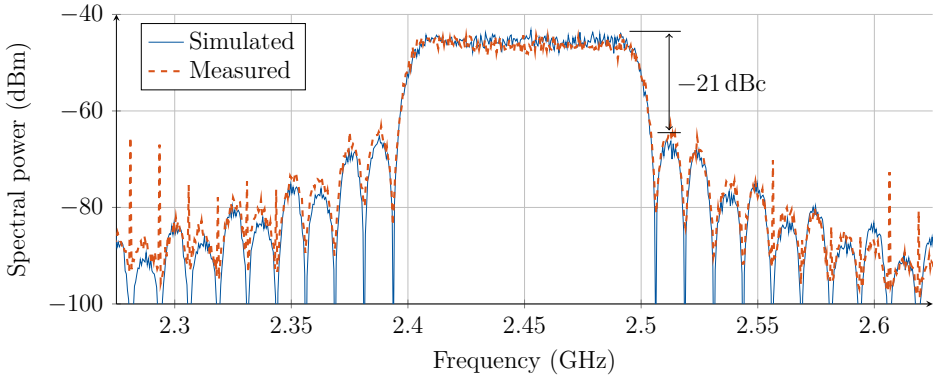
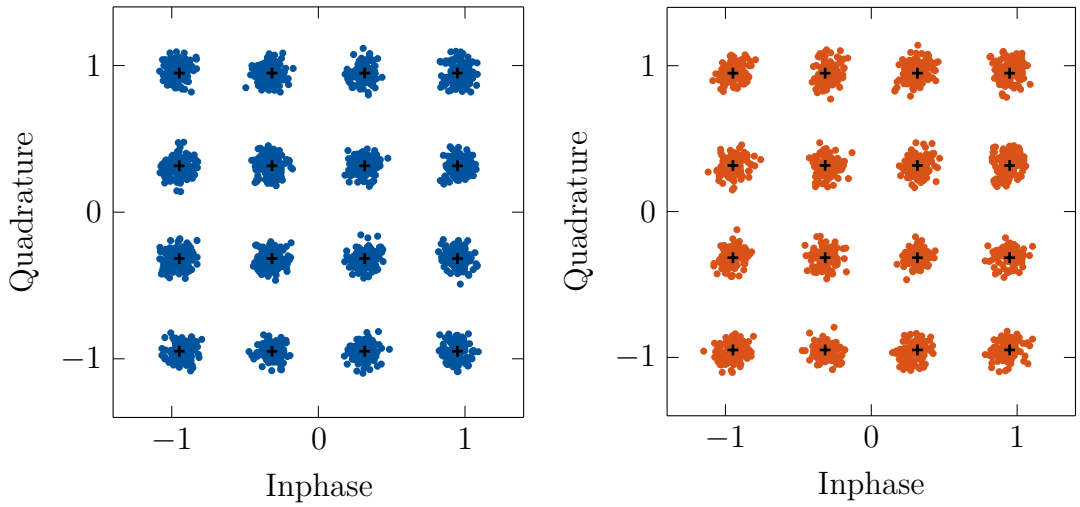


Figure 4.11: Measured spectral power density at the output of the hybrid FDDAC for a modulation bandwidth of 100 MHz.

the synchronisation of the phasor tones and the DAC sampling time is established. In general, a random bit stream is generated which is modulated by a certain modulation scheme, split in delayed and nondelayed paths, windowed and the FFT is calculated. Fig. 4.11 shows the output spectrum of the hybrid FDDAC measured at the output of the 8-to-1 Wilkinson combiner. The measured and simulated spectra match very well. The measured spectrum demonstrates the spectral shaping capability of the FDDAC approach which reduces the first side-lobe to −21 dBc close-in to the band which is limited by the DFT-length. The spectral power far out-of-band is significantly reduced without generating any Nyquist replicas.
Fig. 4.12 shows the simulated and measured constellation diagrams for a modulation bandwidth of 100 MHz and 16QAM. The simulation results are generated with the system-level model of the FDDAC-based transmitter as discussed in Chapter 3.2. The parameters for the nonidealities are extracted by the measurement results of the single



(a) Simulated, EVM = 8.2%.

(b) Measured, EVM = 8.5%.

Figure 4.12: Measured and simulated constellation diagram for 16QAM with a modulation bandwidth of 100 MHz.

PCB hybrid FDDAC transmitter. The model predicts the measured performance accurately. In conclusion, the first implemented hybrid prototype achieved an EVM performance of up to 8.5 % for a modulation bandwidth as high as 100 MHz.

4.3.1 Hybrid FDDAC-based multistandard transmitter

In Chapter 3.2, a prototype for an integrated multistandard transmitter is proposed. It operates as a direct transmitter in the sub-6 GHz frequency range. The output can be shifted to higher frequencies if required. Therefore, a mmW upconverter block can be added to the output of the hybrid FDDAC-based transmitter which shifts the transmit frequency. A similar measurement setup is created with the hybrid FDDAC prototype and a CMOS mmW upconversion mixer. A detailed discussion of the mixer is given in Chapter 8.3. Fig. 4.13 shows the block diagram of the measurement setup.
The output of the combiner is directly connected to a *Rohde & Schwarz FSW26* signal analyser up to 26.5 GHz. In this configuration, the performance of the FDDAC hybrid prototype at 2.45 GHz is measured. The signal is then fed to the integrated mmW upconverter via a balun since the mixer requires a differential input. It upconverts the carrier frequency to the 5G mmW bands around 28 GHz. Fig. 4.14 depicts the measured constellation diagrams which show the achievable EVM performance for different frequency bands by utilising the highest modulation bandwidth of the hybrid FDDAC transmitter, namely of 100 MHz. In Fig. 4.15, the corresponding power

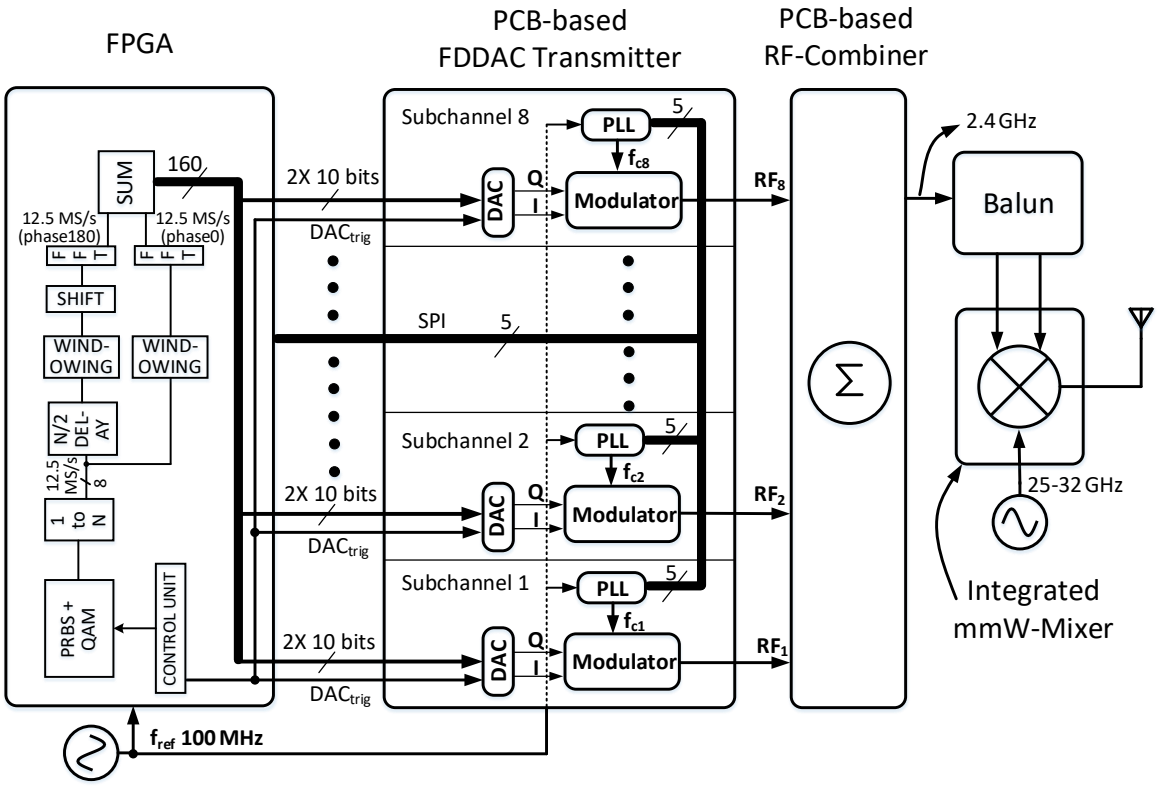


Figure 4.13: Block diagram of the hybrid FDDAC prototype with the integrated 28 GHz upconversion mixer.

spectral densities at different carrier frequencies are shown. The maximum carrier frequency that can be shown is limited by the measurement equipment capabilities which cannot exceed 26.5 GHz.

As illustrated in Tab. 4.4, the proposed approach utilises a significantly lower sampling rate compared to the modulation bandwidth, whereas [72, 73] require a much higher sampling rates for a lower modulation bandwidth. Especially for hybrid FDDAC prototype, the modulation bandwidth is limited by the interface speed rather than the structure since the DACs can operate up to 270 MSps, which means, 1.08 GHz of bandwidth can be achieved. Increasing the bandwidth and, hence, the update rate of the Fourier coefficients leads to bit errors caused by the single-ended data lines between the FPGA and the PCB. However, the FPGA provides only a limited number of IO pins.

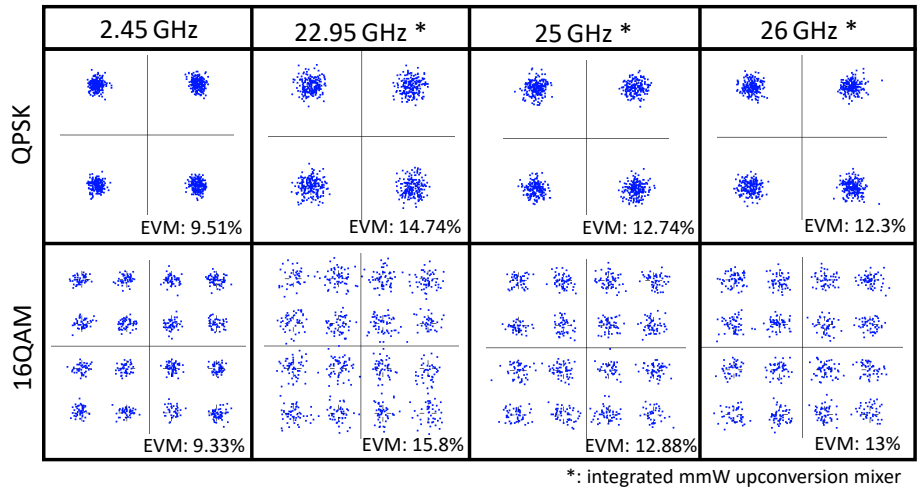


Figure 4.14: Measured constellation diagram for QPSK and 16QAM at different carrier frequencies with and without the mmW integrated upconverter circuit.

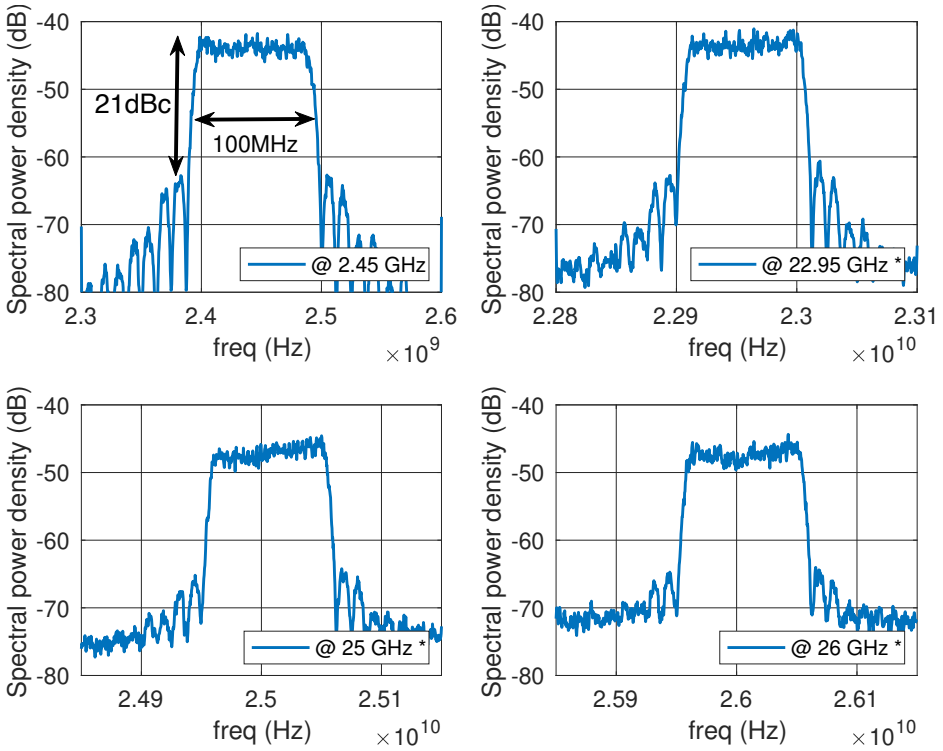


Figure 4.15: Measured spectra at the output of the hybrid prototype, 2.4 GHz, and at different frequencies after upconversion by the integrated mixer.

	This work	MTT'18 [72]	MTT'13[73]
TX-Architecture	FDDAC	FPGA	polar-LINC
Nyquist filtering	**yes/ intrin.**	No	Yes
Analogue output	Yes	No	Yes
Modulated band. (MHz)	up to **100**	up to 48	up to 6
f_{out} (GHz)	2.4, 23-28	0.1-5.12	1.95
Sampling rate (MHz)	**25**	10240	92
EVM (%)	12.8 @ 26 GHz, 8.4 @ 2.45 GHz	4 @ 5.12 GHz	6.2 @ 1.95 GHz
ACLR (dBc)	-21	-35	-36

Table 4.4: Comparison of the proposed mmW hybrid FDDAC-based transmitter with recently reported hybrid transmitters.

4.4 Conclusion

The discussed hybrid transmitter based on commercially available off-the-shelf components is the first transmitter employing the FDDAC technique. It demonstrates the prospects of the FDDAC data conversion approach. Multiple conventional I/Q transmit cores operate simultaneously performing the digital-to-analogue conversion and the analogue inverse Fourier transform. The required DSP complexity, DAC sampling rate and the constraints on the I/Q transmit cores in terms of bandwidth are relaxed significantly. The PCB-based FDDAC transmitter alongside with the DSP can be cointegrated with a dedicated mmW upconversion mixer in a modern CMOS technology. Thereby, the interface limitation can be overcomed and a modulation bandwidth in the gigahertz range can be achieved.
However, this hybrid prototype explicitly shows the importance of a proper power supply. Additionally, the synchronisation and especially proper alignment of the phasor tones and DACs sampling time plays an important role in order to achieve a good transmitter performance. In this design, the alignment was performed digitally and the loop was closed by monitoring the alignment on the oscilloscope. This approach is time consuming and can only be used in a hybrid system since the signals at various points on the PCB can be accessed. For an integrated implementation, a closed-loop system should perform the synchronisation and alignment of the phasor tone and the DACs sampling time.

Chapter 5

Challenges towards CMOS integration of the FDDAC-based transmitter

The operation principle of the FDDAC has been derived and analysed on a system-level in Chapter 3. A first prototype in form of the hybrid implementation is presented which serves as proof-of-concept. The main contribution of this thesis is the introduction and the adoption of the FDDAC in a modern multistandard high data rate transmitter as stated in Section 3.2. Therefore, a fully integrated and competitive CMOS transmitter shall be implemented which breaks through the limitations of the hybrid implementation and shows the real potential of the approach. In this chapter, the challenges of the proposed FDDAC-based transmitter approach as well as several design methodologies towards the CMOS integration are discussed. The emphasis is laid on the implementation of an integrated FDDAC-based transmitter in 65 nm CMOS operating in the sub-6 GHz range.

5.1 DSP and data interface

The main bandwidth limitation of the hybrid FDDAC-based transmitter originated from the interface between the data processing FPGA board and the I/Q transmitters on the PCB. Preprocessed Fourier coefficients can be transmitted to the integrated IC if the appropriate signal processing is not included on the chip. However, this leads to a similar bottleneck as faced in the hybrid implementation. 16 I/Q transmit cores require at least 8 bit of I and Q data with a sampling rate of 250 MHz. Thus, an interface with a data rate of 64 Gbit/s is required. Alternatively, the raw data can be fed to the IC such that the processing is performed on-chip. The integrated transmitter is able to transfer a raw data rate of up to 8 Gbit/s regarding the modulation bandwidth of up to 2 GHz and a modulation order up to 16QAM. The implementation of such a high-speed interface is out of the scope of this thesis. Furthermore, it is not necessary to demonstrate the capabilities of the new architecture. Therefore, either a memory, *i.e.* a SRAM or a random data generation method shall be integrated. The former has the advantage that a known sequence is repeated periodically. However, the size of the integrated memory must be large enough to store a certain sequence length which would consume a significant silicon area. A pseudorandom data generation based on Linear Shift Feedback Register (LSFR) is fairly small in size and large sequence lengths can be achieved. Furthermore, it is possible to reset the LSFRs with a known initial value such that the sequence is known. While random data can be generated on the IC, a communication interface cannot be omitted. It is required to reset or set the transmitter into different modi as well as to control several blocks on the IC.
One of the main advantages of the FDDAC principle is its intrinsic spectral shaping capability. It does not require high OSR and FIR filters in the digital domain in order to process the transmit signal. In fact, high performance FFT blocks with reasonably low lengths are used. The targeted modulation frequency is 2 GHz. The number of the required I/Q transmit cores correlates with the DFT-length which is selected to be 16. Thus, two FFT blocks with a length of 16 are required which operate at 125 MHz. During the design space exploration, several digital blocks have been implemented in the targeted technology. In the 65 nm CMOS technology, it is to implement a single FFT and operate it at double the speed and, hence, reduce the required chip area.

5.2 Analogue-mixed-signal implementation in CMOS

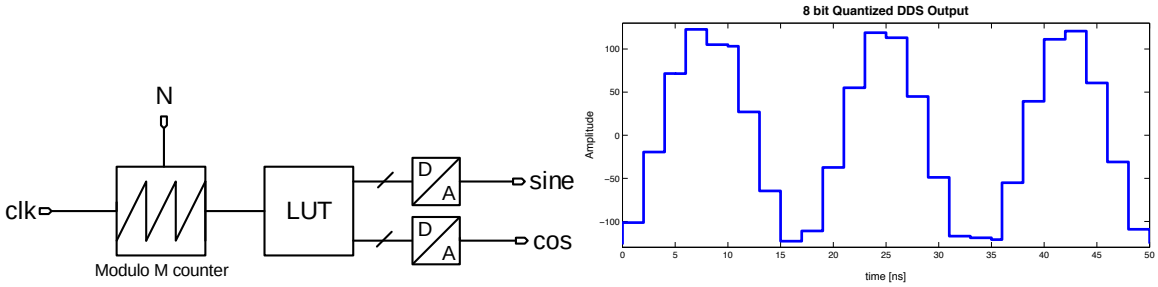
The FDDAC-based transmitter integrates a total of 16 simultaneously operating I/Q transmit cores, where each provides a modulation bandwidth of 125 MHz. The sampling speed is 250 MHz. System simulations predict that the phase transfer function,

matching, equal output power, and timing of the I/Q transmit cores are crucial for the transmitter performance. Furthermore, a minimum quantisation length in terms of resolution is required per I/Q transmitter. One of the most critical challenges of the FDDAC-based transmitter is the summation of the I/Q transmitter outputs which results in the final reconstructed signal. The IC should provide a single differential output which already contains the combined and summed outputs of the bins. The on-chip power combination in the sub-6 GHz is performed by summing the output currents at a single differential node. Nevertheless, the I/Q transmit cores need to be designed with a special care since their outputs shall not modulate each other.
The I/Q transmitter can be implemented by RF-DACs which simplify the time alignment of the coefficients and the LO signals. It is a single block performing the digital-to-analogue conversion of the Fourier coefficients as well as the mixing process. In order to maintain the timing criteria, the synchronised coefficients and phasor tones are provided to the RF-DAC-cells which instantly process the information without disturbing the synchronisation. Consequently, the RF-DAC based implementation is preferable for the first integrated implementation. Nonetheless, the output impedance of each RF-DAC must be sufficiently high in order to combine the outputs at a single node. Alternatively, separate DACs, mixers and output amplifiers can be used to implement the I/Q transmit cores. This leads to the advantage that the subblocks can be optimised for best performance. The DACs and mixers shall provide sufficiently high linearity and good matching performance. The output amplifier buffers need to drive the same node. Therefore, these blocks must shall not modulate each other.
According to the transmitter prototype presented in Section 3.2, the output of the FDDAC-based transmitter will be connected either to upconversion circuits or directly fed to the output in the sub-6 GHz range. The upconversion circuits and the FDDAC-based transmitter can be implemented simultaneously. Therefore, the output of the transmitter must be accessed directly in the sub-6 GHz range. A linear phase and flat amplitude response must to be provided over the large fractional bandwidth which can be achieved by the on-wafer probing. Compared to bonding in a package, wafer probing adds significantly less parasitic capacitances and inductances which simplifies the design process. However, wafer probing significantly complicates the measurement setup since the IC must be accessed both over bondwires for supply voltages and digital IO and the probing tips to access the output signal. Furthermore, a bonded transmitter is preferred in order to allow field testing in a later step.

5.2.1 Phasor tone generation

The simultaneous generation of the equidistantly spaced phasor tones is one of the challenges of the FDDAC approach. Each I/Q transmit core requires in-phase and quadrature LO tones. The system simulations predict that the performance of the

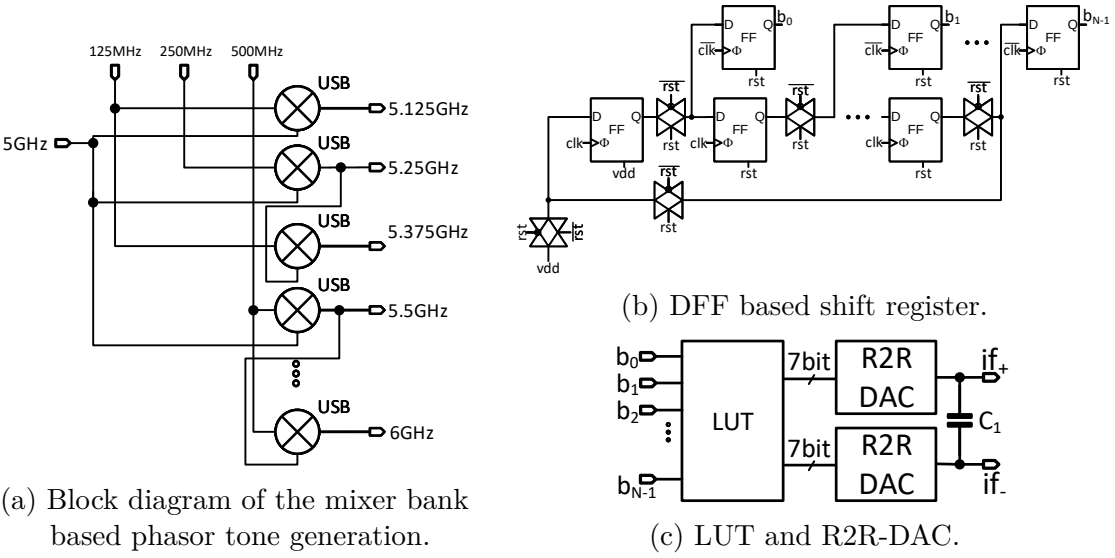
equidistantly spaced tones, in terms of I/Q imbalance, spurious tones, phase noise, synchronisation, *etc.*, has a great impact on the overall transmitter performance. A design space exploration is carried out and several frequency synthesis approaches are implemented and analysed. The examined methods generate the phasor tones directly at the required transmit frequency or at baseband/IF which are upconverted in an additional step by a single LO.
Fig. 5.1a shows the block diagram of a Direct Digital Synthesis (DDS) block which requires a single clock input. The modulo M counter outputs the actual phase of the output signal. The phase increment of the counter is set by N. The output of the counter is fed to two LUTs which output the cosine and sine values based on the input address. The output frequency is given as follows: $f_{DDS} = f_{clk}\frac{N}{m}$.



(a) Simplified block diagram of the DDS. (b) DDS output in analogue domain.

Figure 5.1: DDS-based frequency synthesis.

The maximum output frequency of a DDS is limited by $f_{DDS} < f_{clk}/2$. Furthermore, the output signal approximates a rectangular signal for high output frequencies rather than a sinusoidal signal which, in turn, might lead to in-band harmonics reducing SFDR. The sampled DDS output further contains spurious tones at the frequencies $f_{clk} \pm f_{DDS}$. The frequency planning must be optimised with special care on the harmonic mixing products of these spurious tones. For a given bandwidth and a transmit frequency, the DDS clock as well as the IF generated by the DDS are selected based on an optimisation process [26].
One of the main advantages of the FDDAC-based transmitter is the reduction of the DSP speed. Therefore, the clock frequency and the maximum output frequency of the DDS are limited. The DDS as a frequency source for the FDDAC-based transmitter can be used for a relatively small modulation bandwidth. Such a frequency synthesizer is designed and integrated in the 65 nm CMOS technology [74]. The 8-bit output converted into the analogue domain is shown in Fig. 5.1b. The frequency is 400 MHz. The digital components operate at a clock frequency of up to 1.2 GHz. Very high performance custom designed adders are implemented in order to achieve the clock speeds of the counter. However, the IF generated by multiple DDS, need to be converted into the analogue domain requiring additional DACs with high sampling rates. [75] presents a transmitter architecture mixing, the IF generated by a DDS, the



(a) Block diagram of the mixer bank based phasor tone generation.

(b) DFF based shift register.

(c) LUT and R2R-DAC.

Figure 5.2: Blocks utilised in the phasor tone synthesiser [76]©2016 IEEE.

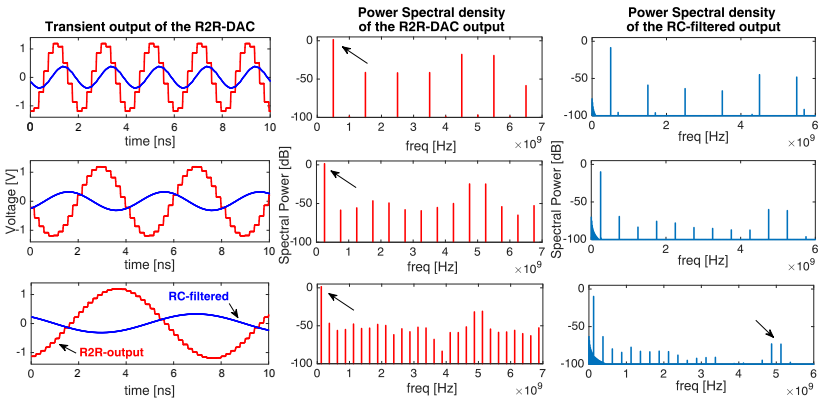
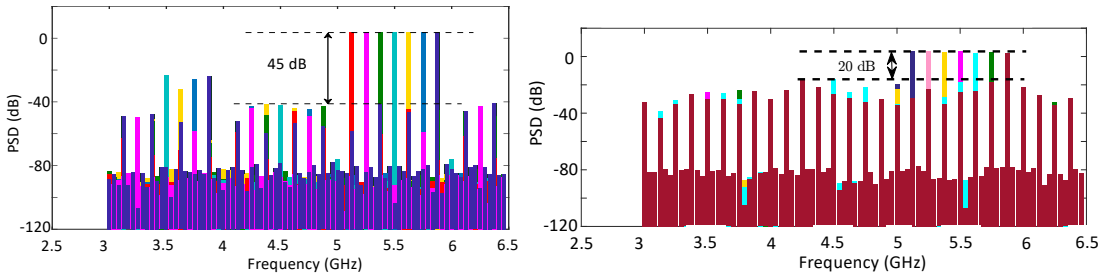


Figure 5.3: low-frequency tones at the output of the R2R-DAC [76]©2016 IEEE.

real and complex Fourier coefficients, c_{re} and c_{im}, and the LO signal within a single block.

Fig. 5.2a shows the block diagram of the mixer based phasor tone synthesis topology. Detailed discussion on the implementation and analysis of this approach can be found in [76–78]. The proposed frequency synthesis solution is based on SSB mixers. It is capable of simultaneously generating 16 phasor tones with a uniform frequency spacing of 125 MHz between 4 GHz and 6 GHz. The principle is based on the generation of low-frequency sinusoidal tones at the frequencies 125 MHz, 250 MHz, and 500 MHz from a single clock input at 5 GHz. Consequently, a SSB mixer bank is used to generate



(a) At the output of the mixer bank. (b) After nonlinear amplification.

Figure 5.4: Simulated PSD of the mixer based phasor tone synthesiser [78].

mixing products at the frequencies of the phasor tones. The mixers also generate the mixing products of the harmonics. The LO is a rectangular signal which switches from rail-to-rail. Thus, its PSD contains odd number harmonics which are at sufficiently high frequencies such that they do not limit the in-band SFDR. However, the harmonics of the low-frequency mixer inputs at 125 MHz, 250 MHz, and 500 MHz directly effect the in-band SFDR. Therefore, the low-frequencies are approximated as sampled sinusoidal tones which exhibit attenuated harmonics. Two different methods on the generation of the low-frequency sinusoidal tones have been investigated. Fig. 5.2b and 5.2c show the block diagrams of the bit shifter and the R2R DACs generating the actual sinusoidal tones. During the reset phase, a single logic high is written to the first DFF which is then cyclically shifted by the clock. The number of the DFFs defines the frequency. The output of the shift register is fed to the LUT which contains the amplitude information of the sine and cosine tone. Fig. 5.3 shows the low-frequency sinusoidal tones in the time and frequency domain. The RC filter formed by the R2R DAC and the capacitor C_1 attenuates the sampling artefacts.
The low-frequency sinusoidal tones are alternatively generated by a current DAC where the LUT values have directly been implemented into the transistor sizing. Thereby, overall complexity, silicon area, and power consumption could be significantly reduced. Fig. 5.4a shows the output of the mixers for 8 phasor tones above 5 GHz. The in-band SFDR is better than 45 dB. Nonetheless, the output of the analogue mixers need to be amplified to a rail-to-rail switching signal. Unfortunately, the nonlinear clipping amplifiers reduce the SFDR significantly [77, 78].

5.2.1.1 Discussion

Several methods on the synthesis of the phasor tones are discussed. The DDS-based method is fully digital and, hence, scales well with technology. However, it either requires additional DACs or new transmitter concepts to process the digital IF signals.

Moreover, the output frequency is constraint by the digital clock. Additionally, the phase noise of the digitally generated signal must be analysed. Consequently, the DDS-based frequency synthesis method is rather suited for narrow modulation bandwidths. The targeted bandwidth of 2 GHz is impractically large for this method.
Alternatively, the mixer based frequency synthesis method is promising since it directly generates the phasor tones. The implemented and postlayout simulated frequency sources deliver outstanding performance in terms of SFDR, power consumption, and phase noise. However, the analogue mixer outputs shall be amplified to a rail-to-rail signals, *i.e.* for an RF-DAC based I/Q transmitter. Thus, nonlinear clipping amplifiers are utilised. The harmonic tones and the sampling artefacts are amplified by the nonlinear buffering which limit the final SFDR. The synthesised phasor tones can be directly used without buffering stage by the utilising I/Q transmit cores based on separate DACs and mixers that the unbuffered mixer output can be fed to the mixers. Frequency multipliers are well suited for synthesizing equidistantly spaced tones, whereas the performance decreases by increasing the multiplication factor [79]. In this particular case, a 125 MHz reference shall be multiplied with values between 32 and 48. Frequency dividers are not suitable since phasor tones shall be spaced equidistantly.
The entire frequency synthesis block needs to be integrated on the same chip. Ring-oscillator-based PLLs reported in literature show outstanding performance. In [80, 81], integrated PLLs which require 0.0021 mm^2 and 0.084 mm^2 area in 65 nm CMOS process are demonstrated. The power consumption is 1.82 mW. The achieved phase noise performance at 1 MHz offset frequency is as low as −108 dBc/Hz which is significantly better than what is assumed in the system simulation. Therefore, the ring-oscillator-based integrated PLL is selected to be implemented for the frequency synthesis block. It can be placed multiple times on a single transmitter chip with reasonable performance due to its small size and low power consumption. However, this PLL type has an inherit drawback in terms of phase noise at high frequencies. Thus, the PLLs operate at half the frequency followed by a DLL-based multiplier. In this configuration, a trade-off for the overall SFDR and phase noise performance is achieved.
All phasor tones need to be synchronised with the Fourier coefficients regardless of the frequency synthesis method. The synchronisation is performed by 16 All Digital Delay-Locked-Loop (ADDLL). They are based on 8-bit digitally controlled delay lines (DCDLs). The counter-based synchroniser controller detects the delay difference between the output of the in-phase phasor tone at the output of the DCDL and a

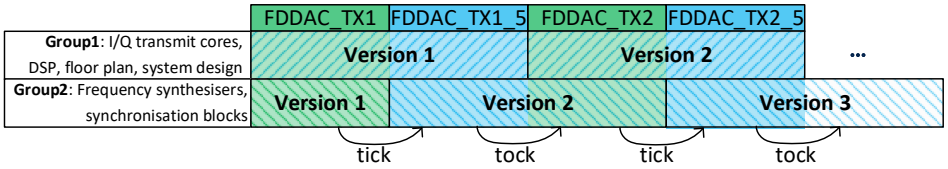


Figure 5.5: Adapted tick-tock model-based design strategy.

reference signal. An overall resolution of up to 1.5 ps can be achieved. The complete frequency synthesis block containing the ring-oscillator based PLLs as well as the synchronisation ADDLLs are implemented in [82].

5.3 Design strategy

The complete transmitter is a complex system including several blocks which need to be operated simultaneously. The well-known components are integrated within the FDDAC transmitter for the first time. Furthermore, the design cycle of the CMOS process is longer compared to the hybrid PCB design. Thus, an adapted version of the tick-tock model as a design approach is chosen [83]. Fig. 5.5 shows the roadmap with several versions of the used subblocks. The I/Q transmit cores, DSP, floor plan, and the system design implemented by the author and the frequency synthesis block are summed as two different block groups, Group 1 and Group 2, respectively. Initially, the first IC is implemented with the first versions of both groups. In every tick-cycle, the components in Group 1 receive a major update, whereas the components in the Group 2 only receive minor updates. The opposite is applied in every tock cycle. Thereby, it is possible to include innovations in both groups without increasing the fail risk.

5.4 Conclusion

The hybrid FDDAC-based transmitter served as a lab validation prototype. In order to show the full potential of the approach, the integration in a modern CMOS technology is targetted. However, the proposed concept also creates new challenges which need to be solved. This chapter contains the outcome of the design space exploration in the 65 nm CMOS process. The DSP block performing the baseband processing for 2 GHz of modulation bandwidth can be integrated on-chip. The transmitted data is generated by on-chip pseudorandom generators instead of implementing a high-speed interface. The frequency synthesis and synchronisation is crucial for the overall performance of the transmitter. Several methods for the phasor tone generation have been implemented and characterised with unsatisfactory results for the targeted modulation bandwidth. Therefore, multiple ring-oscillator based PLLs will be developed. The output of 16 I/Q transmit cores need to be summed on-chip and delivered to the output either by bonding or wafer probing. Additionally, a roadmap is presented which foresees several design iteration, where the aim is to improve the performance in terms of signal quality and data rate while consequently reducing the power consumption.

Chapter 6

CMOS integrated high data rate FDDAC-based transmitter up to 8 Gbit/s

This chapter introduces the first CMOS integrated FDDAC-based transmitter. It covers the floor plan, system design, circuit implementation and analysis of multiple digital and analogue-mixed-signal blocks, and their cointegration in a 65 nm CMOS process. Furthermore, simulation and measurement techniques are introduced to evaluate large and complex systems. The circuit design is carried out based on system-level simulations and the derived specifications of each subblock. The transmitter design includes several levels of fail-safe modes which is included into the system design. The implemented transmitter, *FDDAC_TX1*, is fabricated and fully characterised. The transmitter IC generates a wideband modulated signal in the sub-6 GHz frequency range which optionally can be shifted to mmW frequencies by additional mixer stages.

6.1 Design and analyses of the integrated FDDAC-based transmitter

The FDDAC-based transmitter utilises well-known components such as I/Q modulators, DACs and, frequency synthesisers which are employed in conventional transmitters. It is able to efficiently generate a wide coherent modulation bandwidth due to the fundamental change in the signal representation. However, the challenge of the FDDAC-approach is that the components need to be implemented multiple times in a single transmitter IC and operated simultaneously while being well coordinated and synchronised. Thereby, multiple transmit cores perform an inverse Fourier transform in the analogue domain. Thus, the primary emphasis of the first integrated prototype is to exhibit a proof-of-the-concept and deliver a feasibility study. Table 6.1 presents the targeted specifications of the first integrated prototype which based on the system-level model shall deliver an EVM of approximately 10 % for a modulation bandwidth of 2 GHz and 16QAM in the sub-6 GHz frequency range.

DAC resolution	$\sigma_{DAC,FS}$	DAC slope	$\sigma_{\phi(f)}$	σ_{τ}	$\tau_{offset,const.}$
8 bit	<2 %	<2 %	<2°	<2 ps	<5 ps

phase noise @ 1 MHz	SFDR phasor tones	const. I/Q err.	I/Q MM
>−90 dBc	>30 dB	3°	<3°

Table 6.1: Assumed subblock specifications of the first integrated FDDAC-based transmitter.

A maximum DFT-length of 16 is selected, in turn, the same number of I/Q transmit cores are physically implemented which lead to a modulation bandwidth of 2 GHz when they are used in the Full-Bandwidth-Mode (FBM). On contrary, the transmit mode can be set to the Half-Bandwidth-Mode (HBM) where the DFT-length is reduced to 8. In this mode 8 adjacent I/Q transmit cores are utilised which leads to a modulation bandwidth of 1 GHz. This additionally introduces a fail-safe level in case not all I/Q transmitters are operating as expected.

6.1.1 Top-down design methodology and chip floor plan

Fig. 6.1 presents the simplified block diagram of the integrated FDDAC-based transmitter. It utilises multiple simultaneously operating I/Q transmit cores each modulating the Fourier coefficients on equidistantly spaced LO frequencies. The modulation

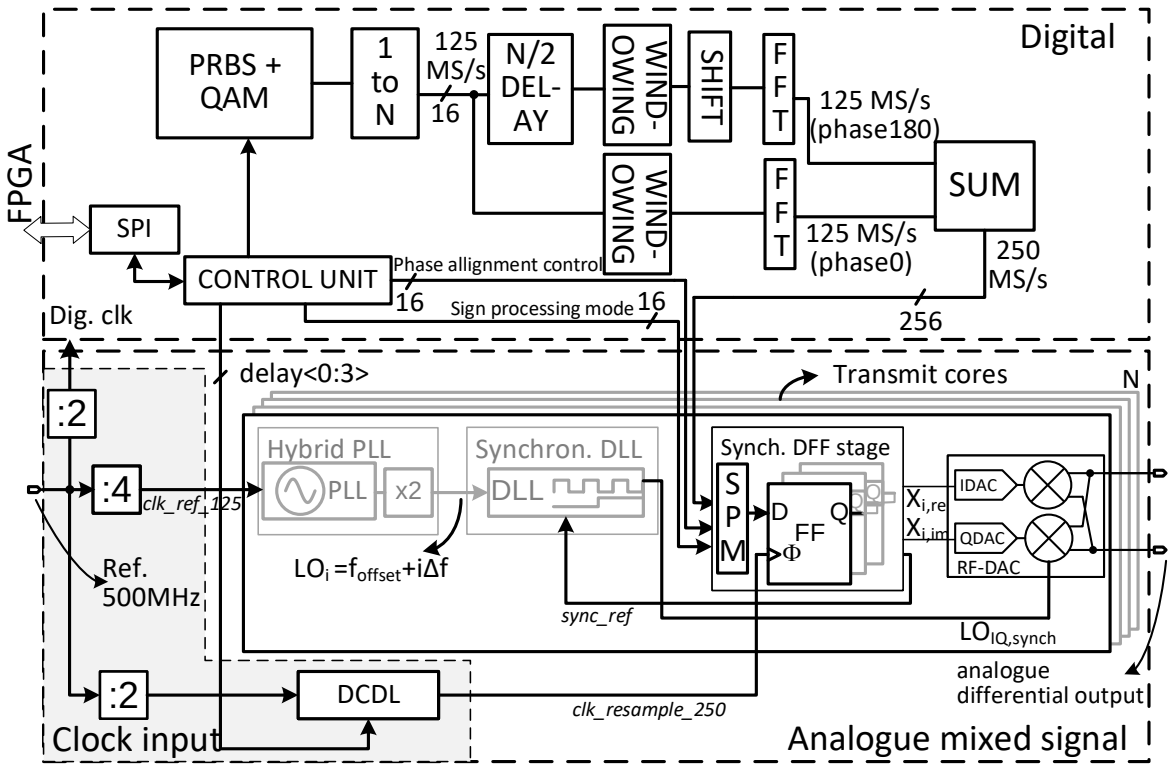


Figure 6.1: Simplified block diagram of the integrated FDDAC-based transmitter.

bandwidth of the hybrid FDDAC prototype, as discussed in Chapter 4, has been bottlenecked by the parallel interface speed between the FPGA and the I/Q transmit cores on the PCB. Thus, the DSP that calculates the Fourier coefficients and performs the signal processing is cointegrated on the same chip alongside with the I/Q transmit cores. Thereby, bandwidth limitations originating from the interface can be omitted. In contrast to a conventional approach involving oversampling and digital filtering, the integrated DSP of the FDDAC-based transmitter operates at 250 MHz which is a fraction of the supported modulation bandwidth of 2 GHz. Thus, the DSP is not limited by the technology. Furthermore, it must be guaranteed that the I/Q transmit cores, the signal synthesis, and the digital processing operate in a synchronous mode which especially becomes crucial for the increased modulation bandwidth. For the integration of such a complex system, the top-down design methodology is used. Therefore, in Section 3.2 the system-level model of the complete transmitter is implemented to derive the specifications of the subblocks. Based on the obtained specifications, the initially available silicon area is populated and allocated in terms of chip area. The 65 nm CMOS process from *TSMC* is accessed via *Europractice* with a silicon block size of 1.9x1.9 mm^2. However, the available chip area for the FDDAC transmitter is restricted to 1.9x1.3 mm^2. Thereby, the available number of pads, packaging, and overall signal flow of the FDDAC transmitter needs to be defined by considering the

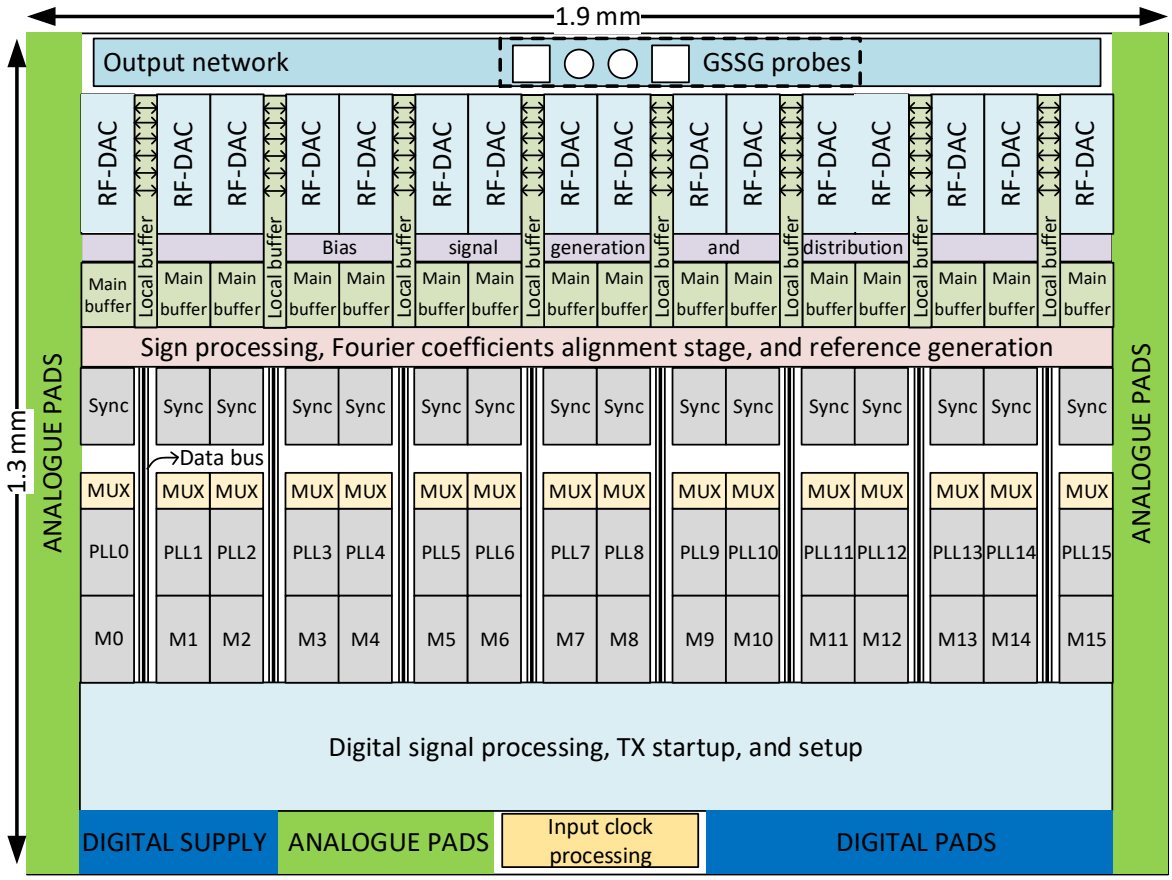


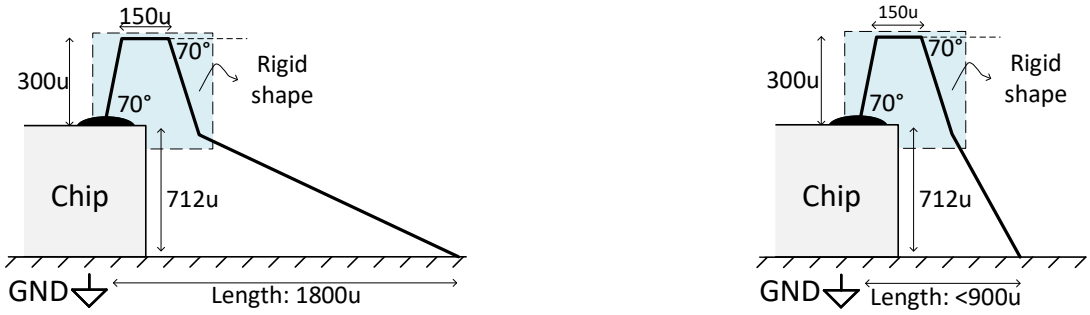
Figure 6.2: Floor plan of the FDDAC-based transmitter.

physical dimensions. The selected technology and the manufacturing house support various Quad Flat No-Leads (QFN) packaging types. Since the transmitter can be accessed from almost 3 edges of the IC, only 3/4 of the QFN pins can be used. Fig. 6.2 depicts the floor plan of the proposed integrated implementation of the transmitter. Three edges of the available chip area are covered with bond pads which will be bonded to the QFN package. The edge of the transmitter which lays inside the block is used for the differential output pads that are probed directly on-wafer. Consequently, no bondwires are used for the output. The high fractional bandwidth at the output of the modulator is accessed by differential high frequency probes. The lid of the package needs to be opened after soldering the IC on an appropriately designed PCB. The shown floor plan additionally takes into account that the output pads can be probed by a specific probing needle without touching the cavity of the QFN package. Accordingly, the probing pads and the IC placing within the package are designed with regard to physical restrictions.
The integrated DSP unit is placed on the lower edge with the required digital I/O pads. The analogue and digital pad rails are separated where the latter requires additional

pads for power-on-control and separate supply pads that are required for the integrated level-shifters of the I/O pads which, in turn, leads to an overhead of pads. Therefore, all I/O pads are placed on the same rail on the bottom right quarter. On the bottom left quarter, solely additional digital core supply pads are placed. The digital block accommodates the random data generation, modulators for different modulation types, FDDAC related signal processing, and it provides control signals for several blocks on the chip. The implemented custom serial interface is used to communicate with the integrated digital block which controls the start-up sequences and fail-safe blocks on-chip. The data bus of two I/Q transmit cores are summed and routed to the I/Q transmitter blocks which are based on RF-DACs and contain several buffering stages, namely main buffer and locally distributed buffers for LO and digital Fourier coefficients. The DSP supports a signed signal processing. In order to reduce the routing complexity between the DSP and the I/Q transmit cores, the sign processing is handled at the input of the RF-DACs. The sign processing and reference generation block receives and processes the Fourier coefficients of eight digital buses each delivering the data for two I/Q transmit cores. It generates a differential representation of the coefficients, aligns them by a clock signal, and provides the differential and aligned coefficients simultaneously to the RF-DACs. Additionally, a reference signal is generated by the same clock signal which is fed to the synchronisation blocks to synchronise the phasor tones. The analogue-mixed-signal supply voltages and required bias currents are supplied by the bond pads placed on the two opposite edges. As discussed in Chapter 5, the implementation of the frequency synthesis blocks is not part of this thesis. However, in the system-level simulations and the floor plan those blocks are considered in order to define the physical dimensions based on the required performance specifications. The grey blocks, namely M0-M15 (DLL-based multipliers), PLL0-PLL15 (ring-oscillator-based PLLs), and Sync (DLL-based synchronisation), are implemented in [82]. Two different frequency synthesizers have been integrated in order to allow a fail-safe option. Therefore, several multiplexers and demultiplexers are implemented and controlled by the digital block to select one of the frequency sources and to set a certain constant delay value to the synchronisation blocks. Consequently, several levels of fail-safe stages are implemented on the system and hardware levels. The height of each of the 16 I/Q transmit cores as well as the frequency synthesis blocks is limited to 98 um by the available width of the block. The reserved area in the frequency synthesis block per phasor tone is $0.04\,\mathrm{mm}^2$.
The presented floor plan is mainly used to analyse the signal flow and the available area for each block. It additionally stresses on the importance of signal integrity within the complete transmitter. Thus, the digital block and the frequency synthesisers use the same reference signal. The reference signal is received and processed in the input clock processing block which is placed on the bottom edge.

6.2 Packaging and bondwire consideration for mixed-signal circuits

The digital I/O operates at extremely low frequencies, hence, they are not effected by the bondwire inductances. However, digital and analogue supply voltages, the GND connections, and the LO input are effected by the bondwire inductivity. Therefore, a proper bondwire definition needs to be generated and considered in the design process. The IC is placed in a QFN48 package and bonded for measurement. The inductance

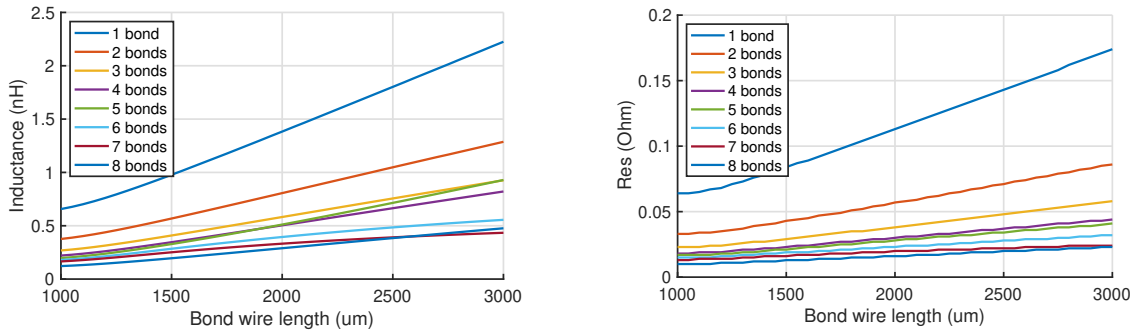


(a) Chip to QFN pin bondwire.

(b) Down bond.

Figure 6.3: Simulated bondwire shapes for inductance estimation.

value of the bondwire depends on its wire-length, diameter, and the shape of the actual bondwire. Additionally, parallel bondwires can be used to reduce the inductance. However, this is limited by the mutual inductance of two adjacent bondwires. In order to characterise the bonding, the *Keysight ADS®* software and the *Passive-RF Bondwires* library is used which allows to create manually defined bondwire shapes. Fig. 6.3 shows two different bondwire types. The ball-wedge bonding technique leads to a characteristic form [84]. The IC substrate is thinned to approximately 700 um for packaging. The bondwire leaves the pad on the chip at an angle of 90°. It is then bent down and connected to the QFN package. Here, the curvature of the bondwire at the chip side is approximated by straight lines at 70°. The characteristic shape is modelled as a rigid form and, hence, it is not effected by the variation of the bondwire length. Fig. 6.3a shows the bonding to the QFN package pins and Fig. 6.3b shows the down bond used for GND connection. Depending on the actual positioning within the QFN package, the bondwire length to the pins might vary according to angle of azimuth. Nevertheless, the down bonds connecting the GND plane of the package are shorter and, hence, they allow relatively lower inductance values. Fig. 6.4 shows the simulated bondwire characteristics using the presented model at 500 MHz. It is assumed that the IC is placed at the centre of the QFN package. Multiple bondwires are spaced 100 um apart from each other and the separation angle is 10°. Thereby, the larger spacing of the pins on the QFN package compared to the pads on the IC is modelled.



(a) Inductance of bondwires.

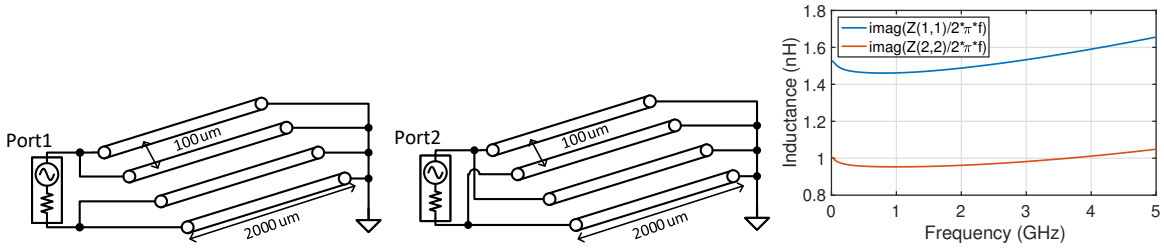
(b) Resistance of bondwires.

Figure 6.4: Simulated bonding parasitics for varying length and different numbers of parallel bonds.

The simulations are carried out at different frequencies, whereas the simulation results shown here are captured at 500 MHz due to the main aggressors which modulate the supply at a maximum frequency of 500 MHz. The bondwire inductance is reduced by parallel bonding, even though it does not behave as linear as the resistance due to the mutual inductance.
When the IC with a block size of 1.9 mmx1.9 mm is placed in the centre of a QFN48 package, the obtained bondwire length varies between 1600 um and 2600 um. Therefore, the simulated inductance value of a single bondwire connection varies between 1.2 nH to 2 nH. Consequently, for critical input signals such as supply voltages and the input clock, the inductance of the bondwires are estimated considering the floor plan and the bonding diagram.
The supply voltage and GND signals are connected via multiple bondwires. Even though down-bonds are used for the GND connection, both supply and GND bondwires are placed side-by-side. Therefore, a structure containing four parallel wires is Electromagnetic (EM) simulated. Fig. 6.5 shows the simulation setup in order to characterise the inductance of an alternating and nonalternating interconnection scheme. The simulation results suggest that the mutual coupling can be minimised by connecting the GND and supply wires alternately. Therefore, the bondwires for supply and GND are placed alternately.

6.3 Integrated digital signal processing

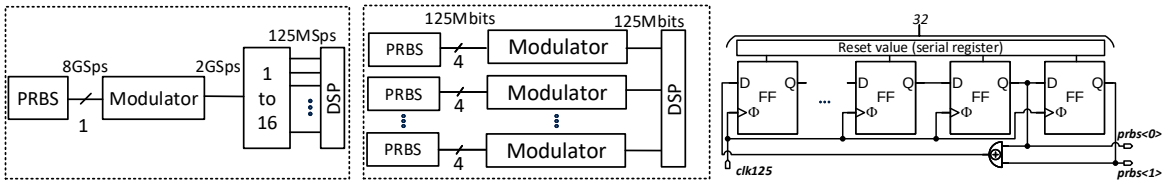
The FDDAC-based transmitter requires a specific DSP block capable of processing a transmit data rate of up to 8 Gbit/s. The random data to be transmitted is generated using Linear Shift Feedback Register (LSFR) within the dedicated DSP block as



(a) Grouped bondwires. (b) Alternating bondwires. (c) Simulation results.

Figure 6.5: Test-bench of different interconnection types for supply and GND signals and simulated inductance.

discussed in Chapter 5. The random bitstream is translated into symbols of a complex modulation scheme, i.e Quaternary Phase-Shift Keying (QPSK) or QAM with a maximum sampling rate of 2 GSps. The integrated transmitter supports a DFT-length of 16 in the FBM and 8 in the HBM. Thus, the symbol stream which exists at a sampling rate of 2 GSps or 1 GSps is parallelised to 16 or 8 lanes, respectively where each lane exhibits a sampling rate of 125 MSps. Fig. 6.6 compares the parallel and serial generation of the pseudorandom bit stream. Fig. 6.6a illustrates a single LSFR-based generator which operates at 8 GSps and outputs a single bit which is fed to a modulator and parallelised afterwards. The approach shown in Fig. 6.6b relies on a parallel generation of the random bit streams. Therefore, each Pseudo Radom Bit Stream (PRBS) block generates four bits at 125 MSps which are fed to multiple modulators generating the symbols directly in parallel. Thereby, the overall sampling rate in the DSP block can be reduced. However, a high-speed interface to replace the PRBS block which directly outputs the bit stream in a parallel manner can be added to the system. Fig. 6.6c shows the block diagram of a 32 bit LSFR. The digital block



(a) Single 1 bit PRBS at 8 Gbit/s. (b) Multiple 4 bit PRBS at 125 MSps. (c) 32 bit LSFR.

Figure 6.6: Comparison of parallel and serial PRBS generation.

contains 32 LSFRs where each contributes two bits. In the reset phase of the complete DSP, a predefined bit sequence is written to each LSFR which is stored in a register. Additionally, these registers containing the reset values are controlled by the serial interface, such that, the pseudorandom sequence can be manipulated. The output of two LSFRs is used in one modulator where each two bits modulate the real and complex

parts depending on the modulation scheme. Fig. 6.7 shows a simplified block diagram of the digital functionalities integrated in the DSP of the *FDDAC_TX1*. The random bit stream is modulated by programmable modulators which support different modulation schemes. The symbols are fed into the FDDAC related DSP which is implemented twice using a DFT-length of 8 and 16 for the HBM and FBM, respectively. The DFT calculation is performed by FFT blocks. The time-domain symbol sequence is divided in two paths and multiplied with 50 % Constant overlap and add (COLA) windows. The delayed and nondelayed paths are converted into the Fourier-domain. The Fourier coefficients of the delayed path are permuted and added to the coefficients of the nondelayed path as described in Chapter 3.1 in order to reconstruct the time-domain signal of both paths using a single FDDAC. The update rate of the Fourier coefficients is 125 MHz. Nonetheless, the addition of the coefficients is performed in an alternating manner as described in Chapter 3. This leads to a doubling of the update rate of the coefficients, namely to 250 MHz. Thereby, the maximum sampling speed in the DSP at the output of the FFT blocks becomes 250 MHz. The FFT block which calculates the Fourier coefficients of the delayed and nondelayed paths can easily be pushed to operate at 250 MHz. Thus, a single FFT block for each length is implemented which calculates the delayed and nondelayed Fourier coefficients alternately. In case the HBM is active, only 8 coefficients are generated, whereas the remaining ones are set to zero. The programmable band-selection block is used to shift the 8 Fourier coefficients among the 16 bins which allows to change the output frequency in discrete steps by means of the equidistant phasor tone spacing, $\Delta f = 125\,\text{MHz}$. Depending on the transmit mode, the Fourier coefficients are provided to the output multiplexers which select between the test signals generated by an appropriate subblock or the Fourier coefficients. The DSP including the windowing and FFT blocks use two's complement arithmetic which needs to be translated to the representation compatible with the sign processing blocks of the I/Q transmit cores. The output signal format acquires 7 bit for the amplitude and 1 additional bit to determine the sign of the signal. Subsequently, all output signals for each bin can be activated and deactivated in order to test single I/Q transmit cores. In the final step, all coefficients are stored in a register stage which enables synchronous updating of the digital output. The system simulations predict that the synchronisation of the phasor tones among each other and the alignment to the DAC sample time are crucial for the transmitter performance. Therefore, the transmit cores generate a reference signal as they sample and convert the Fourier coefficients. This reference signal is then provided to the synchronisation blocks such that the phasor tones are aligned to its rising edge. The reference edge signal is generated in the DSP and provided to the transmit cores in the same way as the Fourier coefficients which are updated at the phases, $\phi = 0°$, and $\phi = 180°$, of the FDDAC approach. Since the 16-point FFT and 8-point FFT processors have different latencies, the $reference\_edge$ signal needs to be programmable. Fig. 6.8 shows the coefficients and the two modi of the reference edge signal. Consequently, the alignment of the phasor tones can be shifted by 180° to match the right coefficient sampling time.

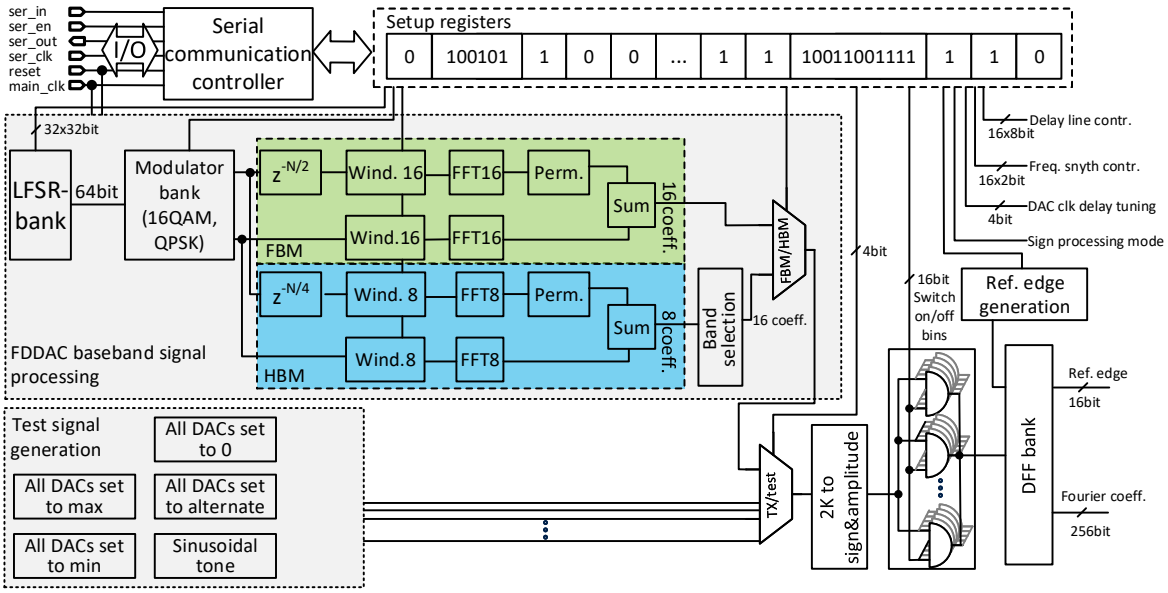


Figure 6.7: Block diagram of the integrated DSP including only core functionalities.

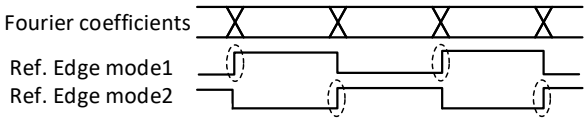


Figure 6.8: Two different modi of the $reference\_edge$ specifying the phase, $\phi = 0°$, of the Fourier coefficients.

The integrated DSP is implemented in several steps as follows:

1. The Hardware Description Language (HDL) *Verilog* and *VHDL* are used to implement the DSP block with the required functionalities. Initially, the signal integrity and functionality is tested on an ideal level. The verification of the signal processing is carried out by the previously introduced *Matlab*®-based system model. Therefore, the simulation results of the complete DSP block are saved bitwise and replace the ideal signal processing in the system model. Thereby, also the effects of the actual DSP can be analysed and optimised.

2. Physical implementation of the digital functionalities is carried out using the software *Cadence Encounter*® by the consecutive steps synthesis and place and route. Synthesis: Generates a gate-level circuit which is based on the available components in the technology. Place and route: Places the gates in a defined area and routes the connections between them with regard to gate internal delays and RC-based parasitic effects introduced by the routing. Additionally, the signal integrity and proper operation is analysed by generating the clock

tree. The automated optimisation process tries to satisfy the setup and hold timing requirements for each block. In order to accomplish the requirements, an optimisation process is used to redesign the clock tree and resize the used gates. These optimisation processes require proper definition of several constraints such as the targeted clock speed, different clock domains, the input waveforms, load capacitances of the output drivers, *etc.* If necessary, the initial HDL code, the reserved area, or the constraints need to be adjusted in order to meet the required specifications.

3. Back-annotated simulations. The initial functionality which is implemented based on the available logic-gates including all supportive gates and delays introduced by the place and route operation are tested. The added delay by the gates and routing is taken into consideration during the simulation. It further checks if any setup and hold violation appears in the internal nodes which might lead to malfunction. The back-annotated simulations are performed for all possible configurations of the DSP including any possible transition from one mode to another.

6.3.1 Digital I/O

The communication with the integrated digital block is implemented by a custom serial interface. It is used to setup the transmitter into different transmit modi, *i.e.* changing DFT-length, switch on or off analogue circuit blocks, and control the functions already implemented in the digital block. Thus, the communication speed does not need to be high. In fact, the serial interface is clocked by a fraction of the speed of the actual digital block in order to increase the robustness of the communication and reduce its area consumption after place and route. The communication is controlled by an external FPGA on which a serial communication controller, ser_{TX}, is implemented. During the power-on of the IC, the interface ser_{RX} on the IC needs to be reset which leads the registers to sample predefined initial states. The communication is initiated by the FPGA which transmits 40-bit words bit-by-bit over a single line to the IC. The word-length is predefined on the IC. Fig. 6.9 shows simulated signals of the interface between the FPGA and the IC. The integrated interface samples the serial input signal, $serial\_in$, with the rising edge of the interface clock, $serial\_clk$, and stores it in a 40-bit First-in, First-out (FIFO) shift register, $deser\_fifo$. After the transmission of the defined number of bits, the enable signal, $serial\_en$, is set to logic high for one period of $serial\_clk$ which triggers the interface controller on the IC to interpret the transmitted 40-bit word. The 40-bits are divided in two parts, the 8 MSB are considered as the address of a register and the remaining 32 bits are the actual payload that carry the information. Therefore, a total of 256 different 32-bit registers can

be addressed and manipulated. After the received 40-bits are processed, the FPGA starts immediately to transmit the second word. In the meanwhile, the first word is transferred back over *serial_out* by the interface controller on the IC. It is sampled by the FPGA in order to control if the initial transmission to the IC was performed correctly. If the parity check fails, the failed transmission is repeated by the controller on the FPGA. If the final communication is performed correctly and no additional communication is requested, the complete ser_{TX} module on the FPGA stops working. It also switches of the *serial_clk* in order to not inject any digital noise to the IC. The *ser_clk* is set to 200 kHz. The reference is generated on the FPGA which is not

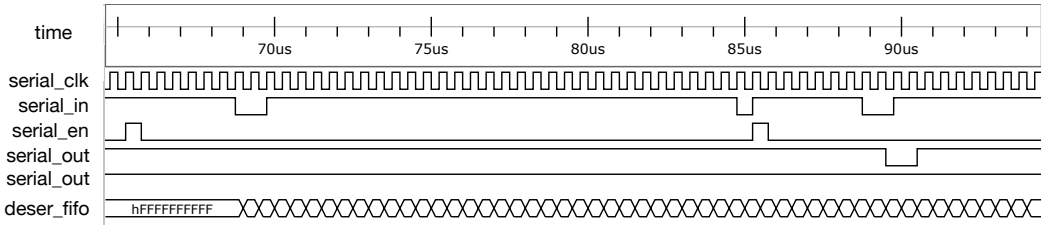


Figure 6.9: Simulated signals between the interface controllers ser_{TX} and ser_{RX} on the FPGA and IC.

synchronised with the main clock of the on-chip DSP. However, the registers which are manipulated by the serial interface are used by blocks operating with the main clock. Therefore, the registers need to be resampled by the main clock in order to prevent cross clock domain timing issues and enable *Cadence Encounter*® to properly optimise the timing and clock tree.

6.3.2 FDDAC-based transmitter related data processing

The FDDAC approach which performs an analogue inverse Fourier transformation requires a specific DSP which in the first place generates the Fourier coefficients of any signal present in the time-domain. In this particular case, a modulated symbol sequence is multiplied with window functions and its DFT is calculated. Hence, one of the crucial components of the signal processing is the actual FFT processor. In contrast to FIR filters in conventional transmitters, it can be implemented extremely efficient and allows tremendous high data throughput thanks to parallelisation [85, 86]. An FFT block can be implemented using the Radix-2 algorithm based on multiple stages of butterfly elements as proposed by Cooley and Tukey in [87]. The FFT samples a vector of time-domain samples and processes them parallelly. This technique is widely used and can achieve very high data throughput speeds. However, the FFT block generated by *Matlab*® utilises the streaming Radix-2^2. It keeps the multiplication

complexity and preserves butterfly elements while saving resources compared to a streaming Radix-2 implementation by factoring and grouping the FFT equation [88]. Furthermore, after each multiplication with the twiddle factors, the product is divided by 2 with the intention to keep the word-length and prevent overflows which leads to the same word-length at the output of the FFT. The high-speed implementation of the FFT comes at the cost of large chip area. However, the high data throughput performance of the FFT blocks, in turn, enables the calculation of the DFT of both the delayed and nondelayed paths on a single FFT processor. Thus, a single FFT block is used operating at double the frequency, namely 250 MHz and sampling alternately the delayed and nondelayed path which reduces the required area. Consequently, two FFT blocks with different lengths, 16 and 8 points, are implemented using *Matlab-Simulink®*. The integrated *HDL Coder* software is used to generate synthesizable HDL code which is included into the DSP of the FDDAC transmitter.
The system simulations, presented in Chapter 3, assume the signal processing to be ideal. The quantisation length is considered and varied at the input of the DACs. The I/Q transmit cores of the FDDAC_TX1 support a quantisation length of 8 bit. Thus, the signal processing needs to be performed at a sufficiently high word-length in order to avoid overflows and truncation leading to errors. The word-length of the symbols is 3 bit in two's complement representation and, hence, decimal numbers from -4 to +3 can be represented. Thus, the modulator supports 16QAM and QPSK with different scaling factors. Fig. 6.10 shows the varying word-length in different stages

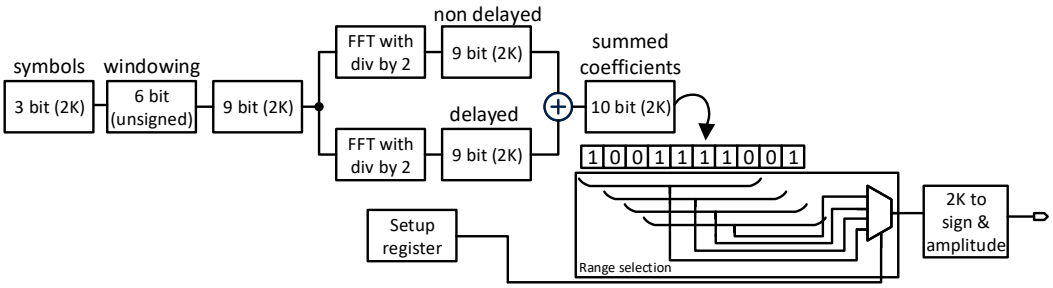


Figure 6.10: Word-length variation across the blocks in the DSP.

of the DSP. A multiplication or addition leads to an increase of the word-lengths. The 3-bit symbols are multiplied by a window function with 6-bit resolution, in turn, the FFT block is fed with 9-bit time-domain samples. The FFT generates Fourier coefficients of a word-length of 9-bits. However, the delayed and nondelayed paths are summed resulting in a final coefficient resolution of 10-bits in two's complement representation. The I/Q transmit cores require 8-bit numbers in signed representation. Therefore, the 10-bits are truncated by selecting a certain range of 8 bit depending on the value saved in the setup register, *range*. Furthermore, based on the modulation type and the transmit mode either HBM or FBM, optimally scaled versions of the window function are used automatically which are stored in the digital block. Thereby,

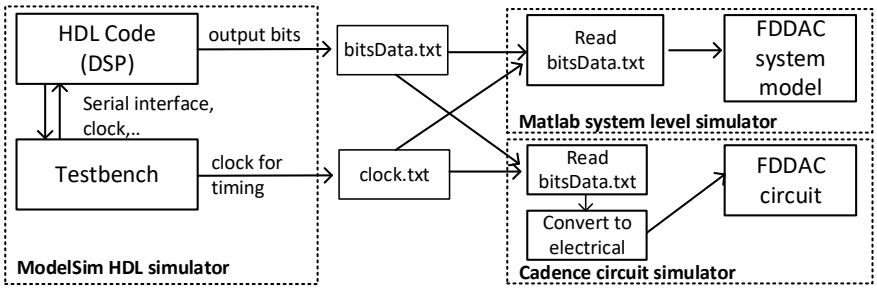


Figure 6.11: DSP and analogue-mixed-signal cosimulation using different software and data handling.

		8FFT				16FFT			
Range		0	1	2	3	0	1	2	3
QPSK_red	EVM (%)	6.5	4.6	3.8	70.3	6.9	5.3	4.6	62.6
	Power (dB)	-20	-14.6	-8.5	-3.7	-18.9	-12.7	-6.7	-1.4
QPSK	EVM (%)	4.2	3.8	17.5	65.5	5.6	4.5	17.9	67
	Power (dB)	-17	-11	-5.3	-2.3	-15.3	-9.2	-3.3	0
16QAM	EVM (%)	9.5	6.3	4.0	40.1	9.8	6.7	5.6	62
	Power (dB)	-19	-13.4	-7.4	-3.2	-17.6	-11.6	-5.6	-0.91

Table 6.2: System simulation results containing the integrated DSP for varying truncation ranges of the Fourier coefficients.

the accuracy is increased and the quantisation errors are reduced to a minimum. The complete DSP is simulated within *Mentor Graphics ModelSim*®. In order to verify the functionality, a test-bench is generated which communicates with the DSP over the serial interface for configuring the current state of the DSP. The ideal simulation results are written to external files alongside with the clock signals which are read and processed in the system-level or circuit simulators as shown in Fig. 6.11. Thereupon, the actual DSP can be considered in the system-level simulation enabling proper scaling of the window functions such that EVM can be optimised for each modulation type and transmit mode. Table 6.2 lists the results of the system simulation based on the data generated by the DSP in terms of EVM and the relative RMS power at the output of the transmitter. The DSP is set in different modi and the parameter, *range*, in the setup register is changed over the serial interface. The highest obtained power level is normalised to 0 dBm. Increasing the range value truncates the MSBs of the coefficients which leads to high absolute word errors, in turn, EVM drops significantly. In contrast, reducing the range value truncates the Least Significant Bit (LSB)s of the coefficients leading to errors and reducing the overall output power of the transmitter. However, a deliberate sweet spot can be found for each transmit mode achieving good EVM performance as well as output power level.

6.3.2.1 Test signal generation

The subblock for test signal generation provides different signals which are used to characterise certain parts of the complete transmitter. A single-tone measurement can be performed to characterise the I/Q imbalance, linearity and LO-feed through for each I/Q transmitter. Therefore, a sinusoidal tone at 1/128 of the DSP frequency, namely 250 MHz, is generated. One quarter period of the sine wave is saved in a LUT which is used to generate the complete sine and cosine sequences. These signals can be switched on and off for a single I/Q transmit core to analyse its isolated performance. Additionally, the digital words sent to the I/Q transmit cores can constantly be set to the highest possible value. In combination with the ability to activate single bins, each frequency source and its spurious tones can be measured. Therefore, it is possible to characterise the frequency synthesis blocks at each frequency independently.

6.3.2.2 Physical implementation and back-annotated simulations

The physical implementation of the DSP involves the translation from HDL to a circuit based representation on logic-gates available in the used technology. This also allows a first estimation of the required silicon area considering only the logic-gates. Consequently, the placing and routing of the logic-gates is performed. Therefore, different types of constraints are set, *i.e.* the shape of the digital block with additional which contains additional area margin compared to the first estimation, locations of the I/O ports of the digital block, the load capacitances seen by the outputs, the driving strengths of the inputs, the required clock speeds, and different clock domains. The long edge of the digital block measures 1537 um which leaves sufficient area for additional pads and circuitry as shown in Fig. 6.2. The width is adjusted such that an initial area utilisation of 65 % is achieved. Accordingly, the width is set to 153 um. Based on these definitions, the logic-gates are placed and routed within the defined shape while taking into account the internal delay of the logic-gates and the RC extracted delay of the routing lines. The clock tree and the gates are optimised by adding or changing the driver strength of additional buffers and logic-gates in order to meet the timing constraints and guarantee the signal integrity. The optimisation algorithms considers mismatch, process, and supply voltage variations. Fig. 6.12 shows the final layout of the integrated digital block. The remaining area after routing and timing is filled with decoupling capacitors to stabilize the digital supply voltage. The clearance along the lower corner is introduced to allow additional area for the input clock recovery and reference signal distribution circuits. The data required by two I/Q transmitters such as the Fourier coefficients, digital delay line tuning bits, and additional control bits are summed to a bus. The routing reduces the available silicon area for the frequency

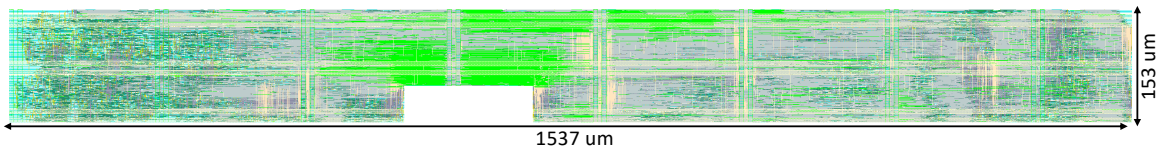
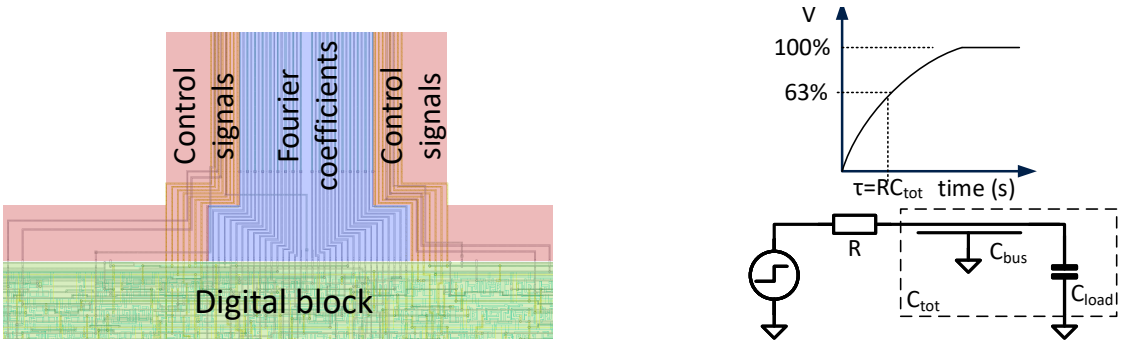


Figure 6.12: Final layout of the integrated DSP block.



(a) One of the 8 digital buses connecting the digital block with the I/Q transmit cores.

(b) Sim. setup to estimate the load cap. driven by the digital drivers.

Figure 6.13: Communication bus from the digital block to the I/Q transmit cores and simulation setup to estimate the capacitive load.

synthesiser. Thus, the required area for the routing from the digital block to the I/Q transmit cores are minimised. Fig. 6.13a shows one of the 8 implemented digital buses.

The Fourier coefficients are updated at a sampling rate of 250 MSps and they are routed over a distance of 570 um. Thus, the bus is implemented with alternating metals to reduce the coupling capacitance. Furthermore, the bus layout is extracted using *Calibre*® parasitic extraction (PEX) and the input capacitance of each Fourier coefficient bit including the input stage of the I/Q transmitters is determined. Therefore, a pulse signal over a known resistance is injected and the rise time is monitored which is used to estimate the total capacitance to be driven by the output drivers of the digital block. The estimated load capacitance is 260 fF. The coefficients are resampled at the I/Q transmitters by the signal, *clk_resample*. This sampling clock is synchronised with the digital clock since they are derived from the same signal source. Additionally, the phase of *clk_resample* can be adjusted such that the internal delay of the digital block can be corrected. The total period of 4 ns is shared by the DSP-output uncertainty, the setup and hold time of the D-Type Flip-Flops (DFFs) at the input of the I/Q transmitters as well as a certain overhead. However, all Fourier coefficient bits need to be updated during a short period of time since any uncertainty shall die out before the I/Q transmitters input stage, *i.e.* DFFs can start sampling. The coefficients are resampled within the digital block before they are fed to the output. Additionally, the

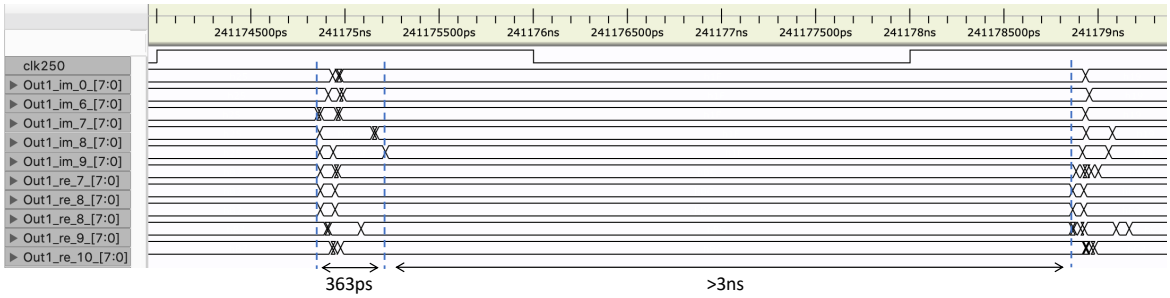


Figure 6.14: Back-annotated simulation results showing the settling of the Fourier coefficients at the output of the digital block.

output timing is constraint to be ready to sample within less then one quarter of the period, *i.e.* 1 ns. Fig. 6.14 shows the back-annotated simulation results for the worst case PVT variations considering the actual delays of the physically implemented block. The shown coefficients settle during a period of 362 ps with a maximum delay of 1 ns. The remaining time, 3 ns, of the period is preserved for the setup and hold time of the succeeding custom designed stage.

6.4 Clock input and reference signal distribution

The complete transmitter requires a single reference signal which is used to derive the main clock of the DSP, the trigger clock of the DAC, and the reference signal of the synchronisation as well as the frequency synthesis blocks. The highest frequencies required are the digital clock and the DAC clock which is 250 MHz. The DFF-stage which utilises the sign processing and the alignment of the Fourier coefficients requires a clock with a 25 % duty cycle. Thus, double the frequency, namely 500 MHz, is fed to the IC as an input. Consequently, the complete transmitters modulation bandwidth as well as its output frequency can be varied by changing the reference clock of the IC. Fig. 6.15 shows the integrated input clock processing block. The external frequency source provides a reference signal at a certain power which is connected to the PCB by a SMA connector. The signal on the PCB is routed via a 50 Ω line to a 50 Ω SMD shunt resistance which is placed as close as possible to the IC in order to provide good impedance matching. The signal is then provided to the QFN package. A single bondwire feeds the input clock to the IC which provides a high input impedance. The simulated bondwire inductance is 1.8 nH, whereas the pad capacitance is 600 fF. An on-chip regeneration buffer cancels out the DC level by a DC-block capacitor. The inverter-based buffer is biased at the trip voltage. It amplifies the input and generates a rail-to-rail switching signal. As shown in the floor plan in Fig. 6.2, the

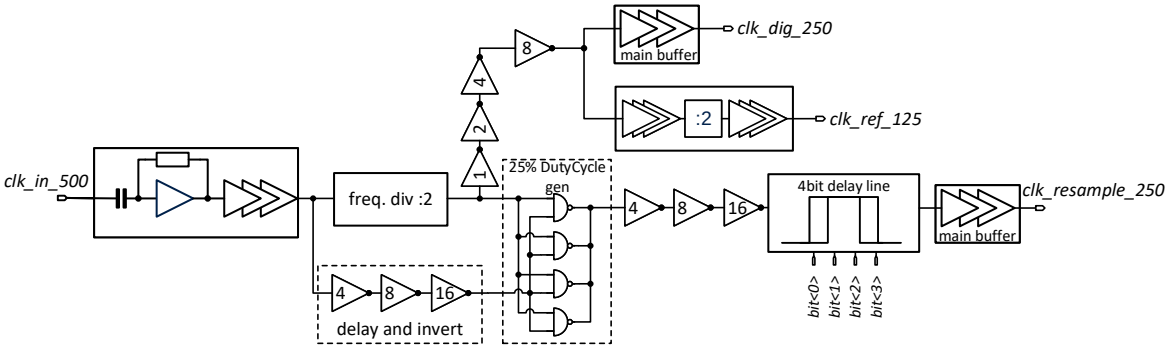


Figure 6.15: Block diagram of the integrated input clock processing unit.

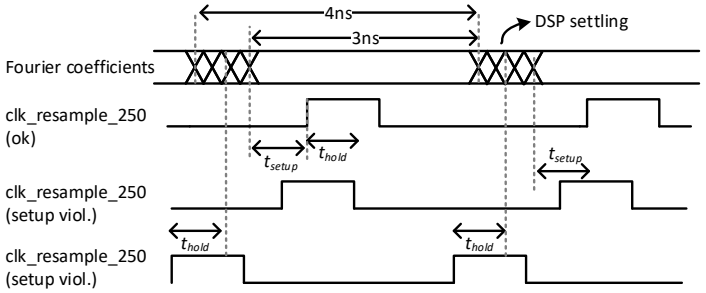
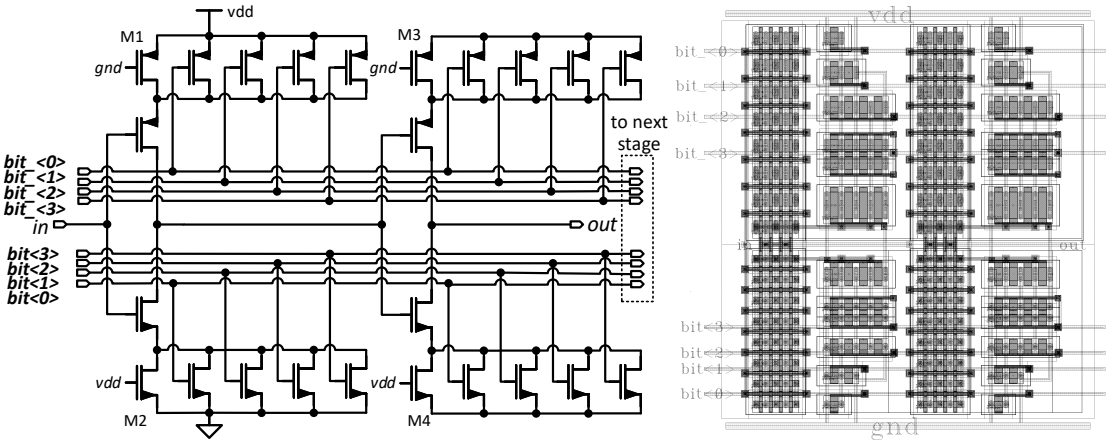


Figure 6.16: Settling uncertainty of the Fourier coefficients generated by the DSP versus the delay programming of the *clk_resample_*250 signal. The setup and hold times of the DFF-stage must be satisfied.

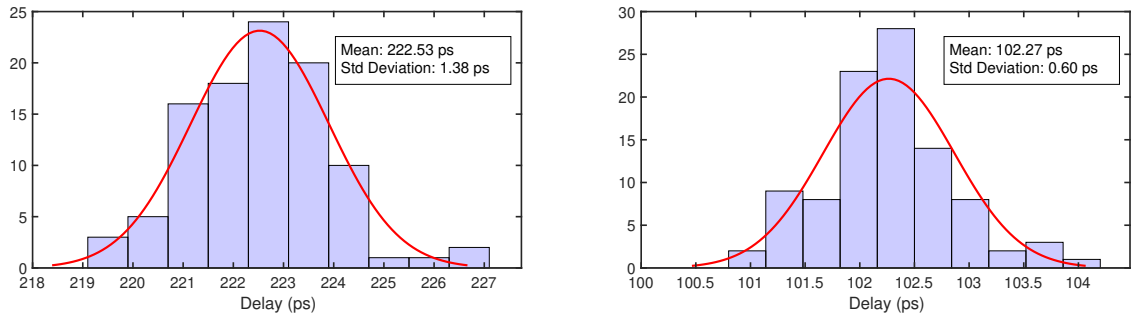
input clock generation is placed close to the digital block. In fact, the digital block is designed with a cut-out in order to preserve the required area for the clock input circuits. It uses its own supply domain and has closely placed decoupling capacitors around the buffers to stabilise the supply voltage. The input frequency is divided by two, buffered, and fed to the digital block. A copy of the divided input signal is routed to a secondary divider which, in turn, outputs a signal at 125 MHz. It is the reference of the integrated frequency synthesis blocks. As this signal is the reference of the PLLs, its noise characteristic sets the lower boundary for the PLLs in-band phase noise [89]. As mentioned previously, the I/Q transmitter cores require a clock signal with 25 % duty cycle which is used to resample the digital Fourier coefficients in the DFF-stage. It is generated by NAND gates that receive the input clock and its copy which is divided by two. The nondivided signal is fed through an inverter chain to invert the signal and to match its delay to its divided counterpart. The NAND gates generate the 25 % duty cycle clock signal, namely *clk_resample_*250 ,which will be routed to the I/Q transmitters. The delay of this particular signal is programmable in order to control the delay differences caused by routing and the unequal clock trees.
Fig. 6.16 shows the settling time of the digital coefficients generated by the DSP. The signal, *clk_resample_*250, must be positioned such that certain setup and hold times,



(a) Schematic. (b) Layout.

Figure 6.17: Schematic and layout of one 4 bit digitally controllable delay cell.

t_{setup} and t_{hold}, of the resampling stage are not violated. Furthermore, two examples are shown where each one of these constraints are violated. Therefore, the programmable delay line must cover a total tuning range of at least 4 ns in order to guarantee correct sampling of the Fourier coefficients. The programmable delay is realised by a digitally controlled delay line (DCDL). The digital block provides 4 bits which are accessible by the serial interface with the intention to tune the DCDL. Fig. 6.17a shows the schematic and layout of the 4-bit single delay cell. It is based on a current starving inverter. Each cell uses two inverters to keep the polarity between the input and output. Both inverters are supplied to a binary-weighted current limiting bank to GND and supply. The PMOS transistors provide a double W/L ratio compared to the NMOS transistors in order to drive a symmetric signal with equal rise and fall times. The control bits are directly connected to the NMOS transistors, whereas the inverted counterparts are fed to PMOS transistors. Fig. 6.17b shows the layout of the programmable delay cell which provides control words and the output signal directly to the next stage. Thus, the implementation of a delay line does not require any additional top-level routing. When the code word equals to 0, the inverters are maximal starved. In this case, the driving strength of the inverters is limited by the always-on transistors M1-M4. For increasing code words, the driving strength of the inverters increase and the delay of the cell is reduced. Fig. 6.18 shows the simulated delay of a single delay cell for the minimum and maximum delay, 102 ps and 222 ps respectively. Each simulation is performed 100 times including mismatch variations of the used transistors. The obtained delay deviation over mismatch is negligible. However, the achievable delay difference per cell is 120 ps, thus in total 35 delay cells are implemented in a delay line in order to achieve a total delay difference of 4.2 ns in the ideal case.
Fig. 6.19 shows the cascaded delay cells. The covered range of the delay line is tested under deviating process corners and different temperatures in order to ensure the



(a) Control word: 0000.

(b) Control word: 1111.

Figure 6.18: Delay deviation over transistor mismatch for the lowest and highest delay.

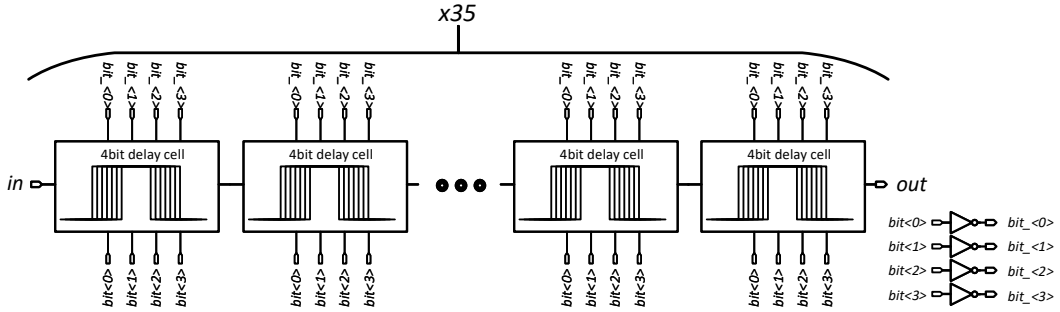


Figure 6.19: Schematic of the complete DCDL based on 35 delay cells.

delay coverage. Fig. 6.20 shows the simulated absolute delay difference of the signal, *clk_resample_*250, based on layout extracted cells over all code words. In all cases, the controllable delay range is above 4 ns.

6.4.1 Reference signal distribution and routing delay

The coefficients and additional digital signals of two transmit cores are distributed by a single bus. Thus, the resampling clock needs to be routed to 8 different points distributed across the IC. The routing delay of the PLL references are not controlled since the LO tones at the input of the I/Q transmitters are synchronised by a separate block. However, the synchronisation and the sampling in the I/Q transmit cores is triggered by the signal *clk_resample_*250. Thus, the routing delays need to be considered. Any delay deviation caused by the routing leads to systematic alignment errors increasing σ_τ and strongly effecting the EVM of the complete transmitter. Therefore, the routing is EM simulated using *Keysights Momentum uW*®. Fig. 6.21 shows two different routing types. A tree structure is shown in Fig. 6.21a which ideally

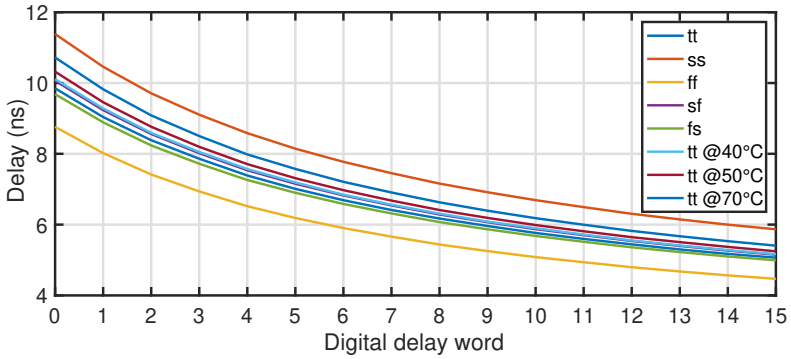
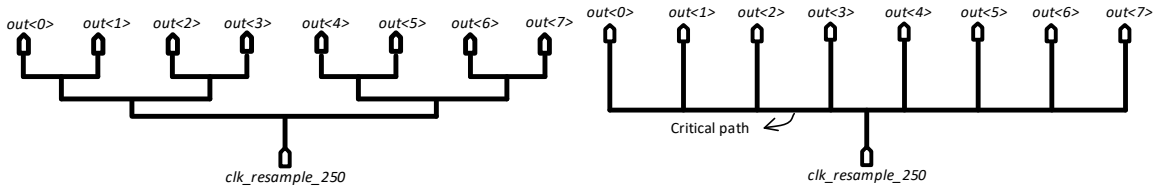


Figure 6.20: Simulated absolute delay of the complete DCDL over digital word including process and temperature variation.

leads to no delay deviation between its outputs. However, the routing of the tree is not suitable due to the floor plan restrictions. Alternatively, the structure from Fig. 6.21b is implemented. The critical path illustrates the routing which mainly contributes to the delay deviation. Two different layouts are implemented and EM simulated, where the one uses metal 7 to route the critical path and the other metal 9 using the exact same shape. The *S*-parameter models generated by the EM simulation are used in *Cadence Virtuoso*® to characterise the delay deviation. A strong buffer, with an output stage of 284 minimum sized inverters, drives the *clk_resample_250* signal within the input clock processing block. The simulated rising edges of the resampling clock is presented in Fig. 6.22. The significantly higher thickness of the metal 9 which is 3.4 um compared to 0.22 um for metal 7 leads to lower resistances and, hence, reduced RC delay. Consequently, the routing is implemented by metal 9.

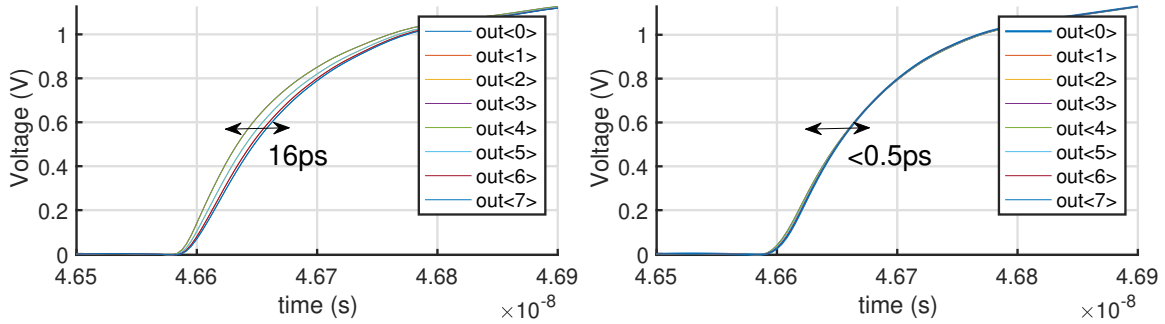


(a) Tree structure. (b) Simple routing.

Figure 6.21: Different routing approaches for *clk_resample_250*.

6.4.2 Cointegration with Frequency synthesisers

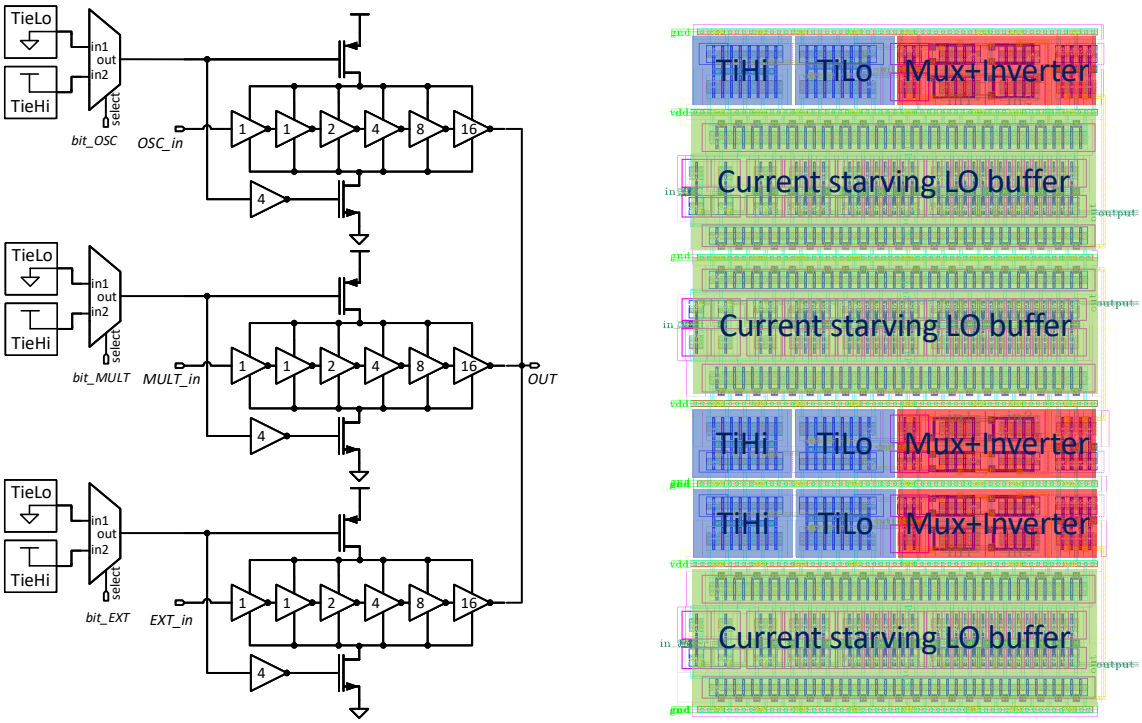
Even though the design and implementation of the encapsulated frequency synthesis and synchronisation blocks are not part of this thesis, the cointegration, top-level supply



(a) Critical path on metal 7.

(b) Critical path on metal 9.

Figure 6.22: Simulated delay deviation of the resample clock after the routing using different metal layers for the critical path.



(a) Schematic.

(b) Layout.

Figure 6.23: Schematic and layout of LO multiplexer which selects the frequency source of the I/Q transmit cores.

routing, estimation of bonding inductances, design and implementation of decoupling capacitors, as well as supportive blocks have been implemented. The transmitter contains 16 frequency synthesiser circuits, whereas the lowest 10 frequencies contain a secondary synthesis block which can be activated if the first approach fails, [82].

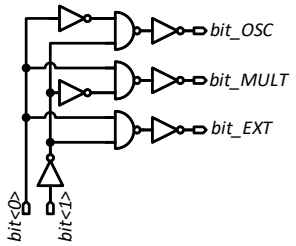
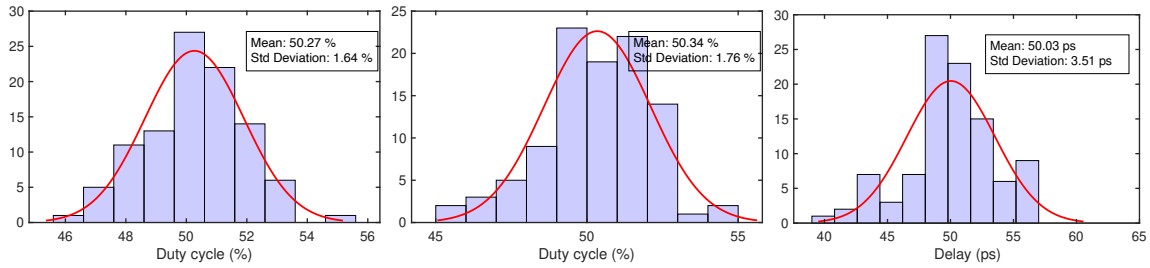


Figure 6.24: Schematic of the hot-one coder.

bit<1>	bit<1>	Output
0	0	bit_OSC
0	1	n/a
1	0	bit_EXT
1	1	bit_MULT

Table 6.3: Logic table.

Additionally, one single phasor tone divided in its I and Q components is fed into the transmitter from an external source in order to replace one phasor tone if the primary and secondary frequency synthesis block for one I/Q transmit core do not work properly. The external tone is routed to each I/Q transmit core. Consequently, a high-speed multiplexer, as shown in Fig. 6.23, is implemented in order to select which frequency source passes through.
The high-speed LO buffers with increasing inverter strength lets the input signal pass when their supply and GND transistors are enabled. Therefore, a low-speed multiplexer lets either the output of a TiHi or TiLo signal pass to the enable transistors. Thereby, no transistor gate is directly connected to the supply rails which, in case of high supply voltage swing, might damage the gates. The digital block delivers 2 bits per bin to control the LO-multiplexers. The bits are coded by a hot-one coder, as shown in Fig. 6.24, to enable a single LO-Buffer at a time. Since each of the phasor tones contain I and Q components, the complete multiplexer is implemented twice per bin. The layout is optimised for symmetry and matching. By flipping and attaching the presented layout to its bottom edge, identical buffers are obtained considering the proximity effect. Fig. 6.25 illustrates the duty cycle and the delay difference between I- and Q-paths at the output of the multiplexer. It is characterised with a phasor tone at 5 GHz and the results are sampled over mismatch and process variation. The duty cycle deviation is well-controlled and negligible. However, a discrepancy in the delay distribution between I versus Q-paths is observed. For a 5 GHz tone, the delay difference between I and Q-path is ideally 50 ps. The detected deviation originates from the small-sized inverters at the input of the buffer chain. Nevertheless, the reduced inverter size is required in order to provide the least possible capacitive load to the preceding driver stage since the high frequency signals tend to fade out. Therefore, the cost of increased I/Q phase error up to 6° of standard deviation is taken which based on the system simulations reduces the EVM of the complete transmitter to up to 7%.



(a) Duty cycle of I output. (b) Duty cycle of Q output. (c) I versus Q delay mismatch.

Figure 6.25: Simulated duty cycle and delay difference between the I- and Q-paths of the LO-multiplexer for a phasor tone at 5 GHz.

6.5 RF-DAC based I/Q transmit core design

The I/Q transmit cores modulate the Fourier coefficients which are calculated by the integrated DSP, onto phasor tones which are represented by equidistantly spaced LO signals with in-phase and quadrature components. Regarding the system simulation, it is crucial for the FDDAC approach that all I/Q transmit cores operate synchronously. Fig. 6.1 shows the block diagram of the complete transmitter. The signals from the digital block are resampled at the DFF-stage using the signal *clk_resample_*250. Its rising edge defines the point in time at which all signals are synchronised and aligned. The delay of the phasor tones synthesised in the preceding blocks is controlled by synchronisation DLLs, [82], which receive the $reference\_edge$ resampled by *clk_resample_*250, as shown in Fig. 6.16. After resampling, it is referred to as $sync\_ref$. Fig. 6.26 shows the schematic of the DFF-stage containing the sign processing blocks, $sync\_ref$ generation, and the resampling of the differential coefficients. The coefficients and the $reference\_edge$ signal experience the same delay as they are resampled by identical DFFs. Thus, at the dashed line, all coefficients and LO tones are synchronised and aligned. Consequently, any timing mismatch and delay deviation in the succeeding blocks must be controlled strictly since additive delay mismatches are not corrected past the dashed line.
Based on the system simulation, each of the I/Q transmit cores is implemented with a quantisation length of 8 bit. The RF-DAC as a building block combines the digital-to-analogue conversion and the mixing process within a single block, [90], which is its most significant advantage for the FDDAC approach. The digital coefficients and the LO signals, aligned in time, are processed within a single block compared to a transmitter chain of complex DACs, I/Q mixers, *etc.* Thus, it is not necessary to investigate timing alignment across multiple blocks. Furthermore, the RF-DAC can directly output high power at the transmit frequency which omits additional output drivers [58, 91].
The RF-DAC is commonly implemented based on current-steering DAC cells com-

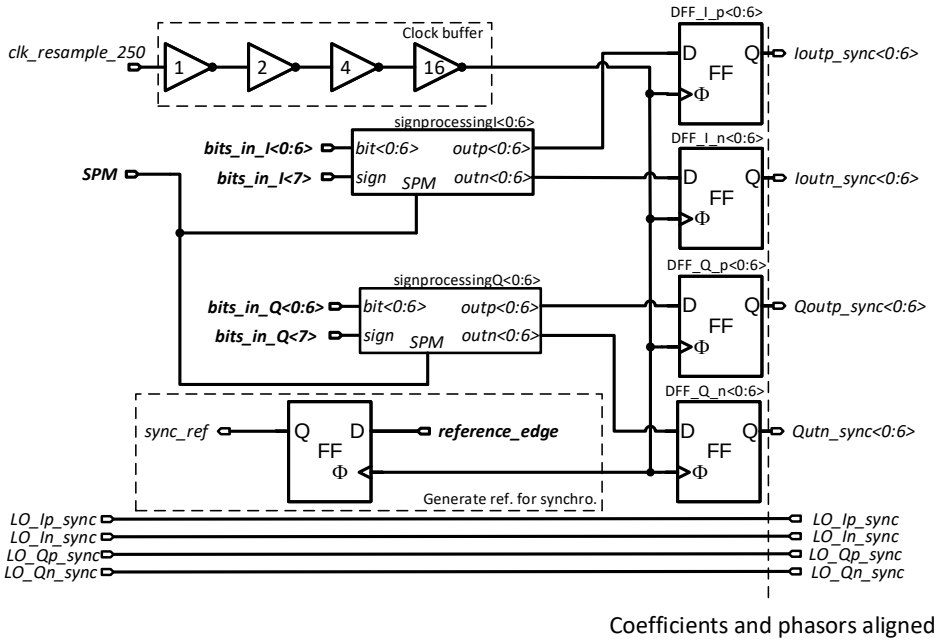
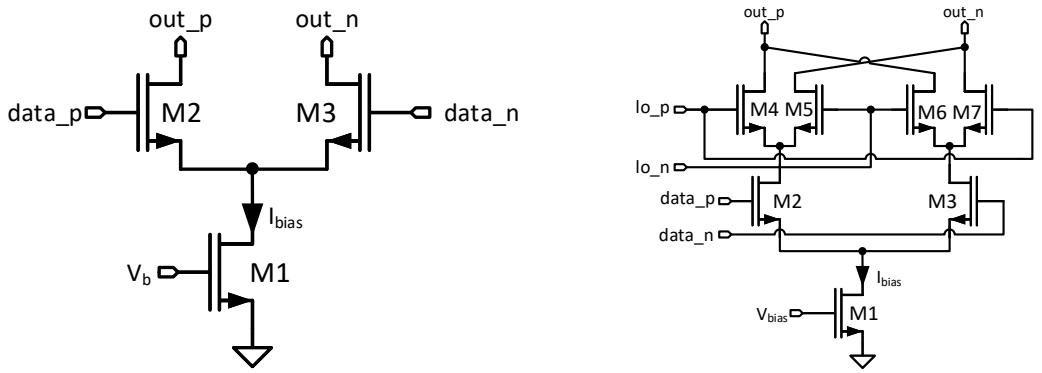


Figure 6.26: Simplified block diagram of the DFF-stage including the sign processing and the generation of $sync\_ref$.

bined with a passive mixer structure modulating the LO directly on the DAC current. The current-steering DAC cell, as introduced in Section 2.1.3, comes with several advantages such as high switching speed, scalability in CMOS process, and transistor matching performance which are valid for the current-steering RF-DAC cells as well. Fig. 6.27 shows a current-steering DAC cell and its extended counterpart, an RF-DAC cell. The transistor M1 in both cases acts as a current source setting a certain bias



(a) Schematic of a current-steering DAC cell. (b) Schematic of a RF-DAC cell.

Figure 6.27: Comparison of current-steering DAC and RF-DAC cells.

current *I_bias* which is steered by the transistors M2 and M3 depending on the input data. Apparently, the RF-DAC cell additionally utilises the transistors M4-M7 which implement a double-balanced mixer. The output of the shown RF-DAC cell is ideally an alternating current with the frequency of the LO signal where the differential input data sets the polarity of the output signal. Furthermore, the location of the data and LO input is not limited by the shown example, hence, they can be swapped. The cells of the complete RF-DAC can be implemented as unary-, binary-weighted cells, or a combination of both in order to achieve a certain number of quantisation steps. Unary-weighting is preferable since it provides improved device matching as well as lowering the power of glitches at the output while switching, [92]. Additionally, the cells can be addressed in a binary or unary manner. However, the complete FDDAC would require 16 times 256 cells each per I and Q DAC which, in turn, translates to a total of 8192 cells which need to be addressed individually. Additionally, the LO tones and digital words must be buffered for each cell. binary-weighted cells require binary-weighted driver buffers which assure same driving behaviour for varying cell sizes.

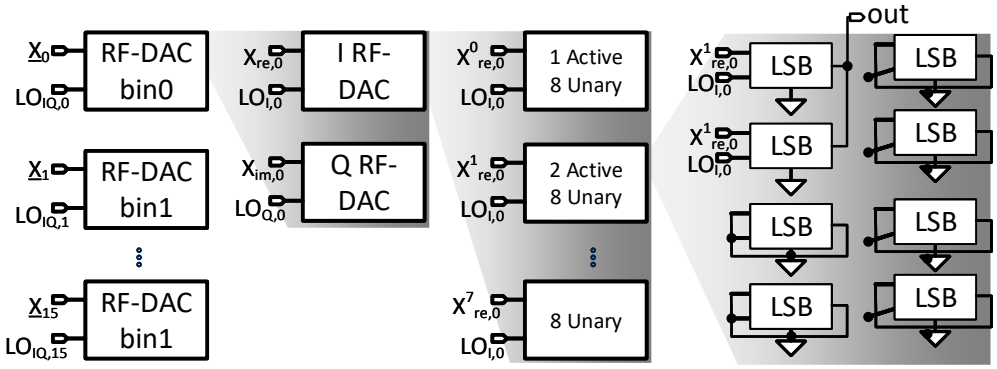


Figure 6.28: Integrated RF-DAC architecture based on pseudounary cells.

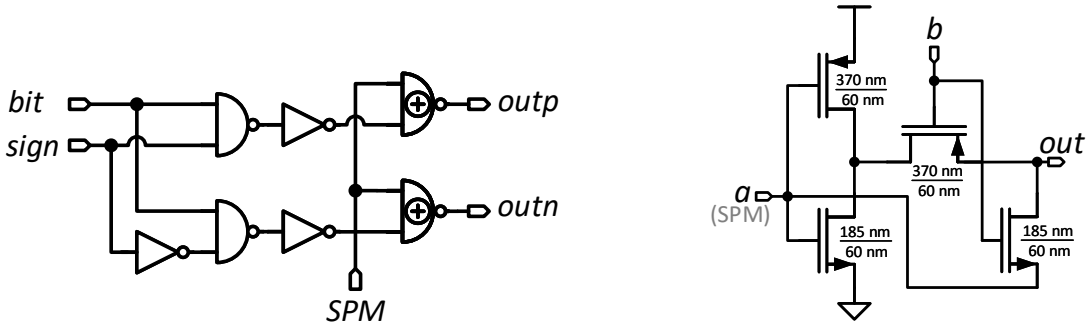
Fig. 6.28 illustrates the pseudounary-weighted cell architecture of the RF-DACs in the FDDAC transmitter. Unary-weighted cells based on 8 LSB cells are implemented which generate an output current equivalent to 8-fold of the LSB current. For the 3 LSBs, the same unary-weighted cell is used where only 1, 2 or 4 subcells are internally connected to the output. Thereby, in total 17 LSB cells are implemented but not used which leads to an area overhead of 6.6 % per I/Q DAC. In contrast, the number of total cells which need to be addressed and buffered in the complete FDDAC transmitter is reduced to 1088 which is nearly a reduction by a factor of 8. The reduction of total cells directly correlates with the power consumption of the transmitter and reduces it since the LO buffering can be simplified. The 3 MSB cells are implemented as multiples of the pseudounary cell. Furthermore, the cells are addressed in a binary manner. All pseudounary RF-DAC cells provide the same capacitive load at the data and LO input ports, in turn, equally sized buffers are used for all pseudounary cell. Thereby, the

internal delays are equalised.
The differential and double-balanced RF-DAC cells can provide outstanding LO suppression, [58]. Therefore, the input data should be switched perfectly differential since any DC component of the data mixed with the LO leads to an LO feedthrough. Conventionally, the 8-bit signed coefficients from the DSP represent numbers from -128 to 127. By adding 127 to each output word and representing the sum as an unsigned number, the coefficients vary between 0 and 255. The obtained unsigned representation is then transformed to the differentially switching data scheme by flipping each bit for the negative part. The word-length of 8-bits represents $2^8 = 256$ amplitude levels. For simplicity, these levels are represented by 256 differential unary cells. Table 6.4 shows the conventionally used differential words and the value of the RF-DAC output. It allows each 128 positive and negative output levels. However, zero output cannot be represented. Additionally, the number of the cells equals to the representable levels, namely quantisation levels.

word_p	word_n	word_p	word_n	output
11111111	00000000	255	0	+255
⋮	⋮	⋮	⋮	⋮
10000000	01111111	128	127	+1
01111111	10000000	127	128	-1
⋮	⋮	⋮	⋮	⋮
00000000	11111111	0	255	-255

Table 6.4: Fully differential switching scheme used in current-steering DACs.

The RF-DAC implemented in this thesis introduces a new switching scheme. The coefficients are calculated in two's complement and translated into a format with one dedicated sign bit and 7 amplitude bits. Thereby, the amplitude varies between 0 and 127 of which the sign can be positive or negative. Instead of using 256 always on and differentially operating cells, only 127 cells are utilised where each cell supports 4 different states. Each cell either provides a positive or negative output current and, hence, two different representations for zero. The amplitude bit and the corresponding sign bit are processed depending on the control bit, SPM, that sets the the sign processing mode. Thus, the $data_n$- and $data_p$-bits which control the current-steering of the binary addressed differential RF-DAC cells are obtained. Table 6.5 shows the corresponding logic table. Each cell generates either a positive or negative output current when the cell is active. In order to represent the output value of zero, both data bits are set to 1 or 0, in turn, the differential output ports either deliver the same current, namely $I_{bias}/2$, or no current at all. With this method, the zero value at the output has two representations and the RF-DAC signal moves between negative 127 and positive 127 with steps of 1 LSB current. Consequently, the number of required cells



(a) Schematic of SPM block per bit. (b) Schematic of XNOR.

Figure 6.29: Block diagram of the SPM unit and the schematic of the 4 transistor XNOR.

is further reduced by a factor of 2 which also reduces the area and power consumption of the RF-DAC by the same amount. However, this approach should be applied on double-balanced RF-DAC cells to provide differentiality regardless of the SPM and the input data.

SPM	sign	amp	data_p	data_n	out
0	0	0	0	0	0
0	0	1	1	0	+1
0	1	0	0	0	0
0	1	1	0	1	-1
1	0	0	1	1	0
1	0	1	1	0	+1
1	1	0	1	1	0
1	1	1	0	1	-1

Table 6.5: Differential switching mode based on the presented sign processing technique.

Fig. 6.26 shows the sign processing blocks within the complete DFF-stage which is designed to fit in an area of only $86 \times 14\,\mathrm{um}^2$ including the DFFs. The bits representing the amplitude and the sign are fed to custom logic-gates, as shown in Fig. 6.29 which output the differential data to be resampled by the DFF and sent to the RF-DAC cells. The logic is based on NAND-gates which are the preferred logic in CMOS since both PMOS and NMOS transistors are sized equally.
The SPM input is directly driven by the DSP block. It is programmable via the serial interface for each bin. Fig. 6.29b shows the schematic of the custom XNOR gate which is designed to be extremely small using only four equally sized transistors. It has the same size as the NAND gate. The custom XNOR gate is based on an inverter and two single-transistor transmission gates. If the SPM-bit is logic high, the output state logic

low is conducted by a PMOS and the output state logic high by an NMOS transistor. In this particular case, the output voltage swing moves between $V_{dd} - V_{th,lvt}$ and $V_{th,lvt}$. Therefore, it must be guaranteed that under process and mismatch variations the DFFs will be able to resample the output with a reasonable setup and hold time. Based on simulations, the maximum delay variation of the sign processing is below 100 ps. The setup time of the succeeding DFF stage is simulated to be 250 ps. Consequently, the clk_ref_250 signal can be adjusted such that all coefficients of the 16 bins can be resampled correctly.

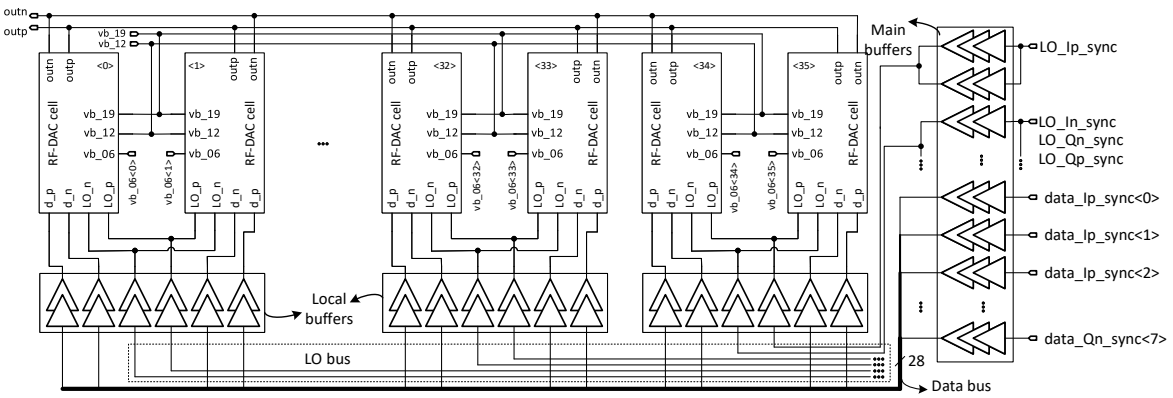


Figure 6.30: Block diagram of the RF-DAC including the locally distributed and main buffers.

Fig. 6.30 shows a simplified block diagram of one I/Q RF-DAC without the DFF-stage, bias voltage handling, and the distributed decoupling capacitors. The buffering concept is based on two stages, namely the main buffers and the local buffers which are placed next to the cells. In total, 38 pseudounary RF-DAC cells are implemented within a single I/Q transmit core, where each requires three bias voltages. Fig. 6.31 shows the layout of two back-to-placed I/Q RF-DACs sharing the same data bus and the differential output network. The blocks in the upper RF-DAC are named after their functions, whereas in the lower RF-DAC various signal paths are shown by means of arrows. The internal routing delays are considered and balanced since the signals prior to a block, travelling a longer path, experience the shorter travelling distance while succeeding the block. The bias voltages are routed between the main buffers and the RF-DAC cells. All buffers and RF-DAC cells are surrounded by decoupling capacitors to stabilise the supply voltage and to keep the biasing voltages stable versus the local GND.

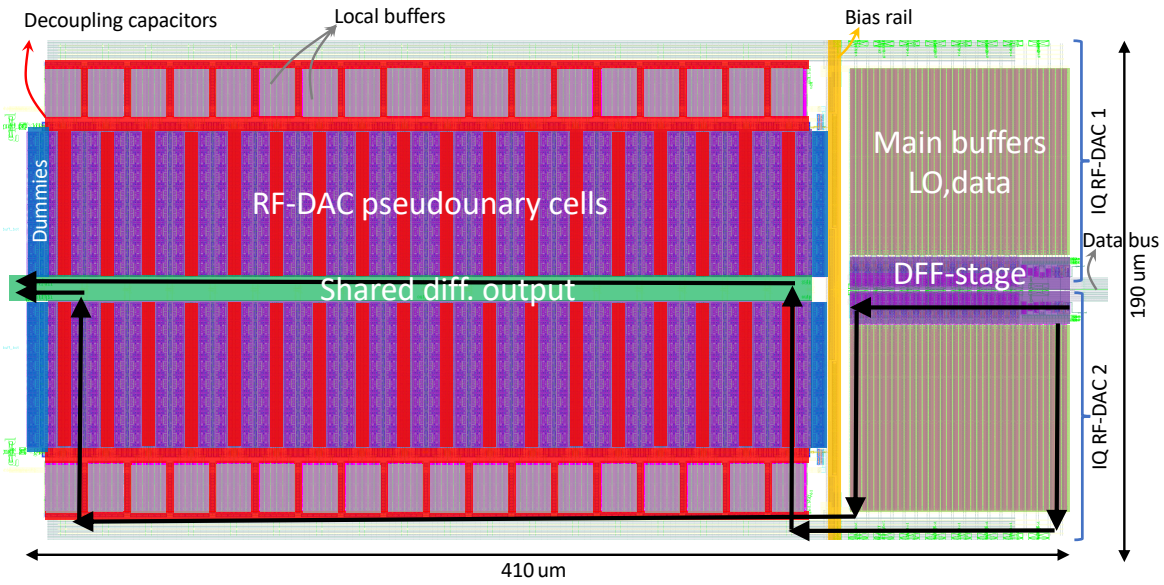
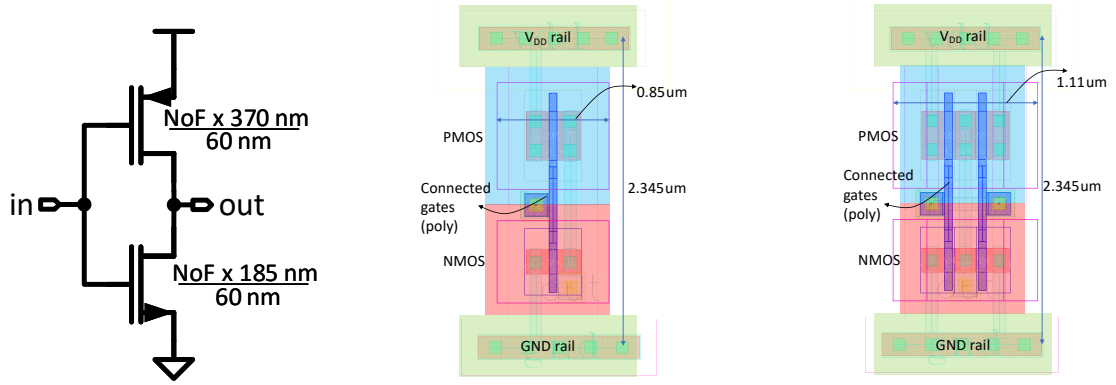


Figure 6.31: Layout of two I/Q RF-DACs sharing the same differential output and input bus. The upper RF-DAC presents various blocks and the lower RF-DAC shows possible signal paths in the IQ RF-DAC.

6.5.1 Buffer stages

Buffers in different sizes and driving strengths utilised in the complete design are based on inverters as shown in Fig.6.32. The transistor length is set to 60 nm which is the smallest size available in the technology. Thereby, the highest driving strength and the lowest input capacitance is obtained. The minimum gate width of the technology is 120 nm, although the chosen rail distance of 2.345 um allows the NMOS width to be 185 nm and PMOS width 370 nm. The PMOS gate at double the width of the NMOS gate leads to equal rise and fall times. The gates of both transistors are routed by extending the gate poly layers such that they are connected by a single via from metal 1. This routing is not beneficial since the poly layer has a significantly higher sheet resistance compared to metals, although the given layout is optimised for a minimal area consumption while complying with the Design Rules Check (DRC) rules. Fig. 6.32c shows the layout of an inverter with two finger transistors. Due to the finger structures, the width of the layout does not increase proportionally. Inverter chains share the same supply and GND rail which also include the P-substrate and N-well connection. Furthermore, multiple inverter chains can be placed next to each other by mirroring and overlapping the rails.
The data and LO signals are ideally aligned at the input of the main buffer stage. Thus, the buffering of all coefficients and the LOs are performed by equally sized inverter chains in order to keep the synchronisation. Consequently, the buffers are designed for



(a) Schematic. (b) Layout NoF=1. (c) Layout NoF=2.

Figure 6.32: Schematic of a CMOS inverter and layout variations for different number of fingers.

the highest frequency in the system which is the LO signal at the highest frequency bin, namely 5.875 GHz. Therefore, the first element in the chain is a minimum-sized inverter, whereas the output stage has 128 fingers. The size of the inverters increases exponentially with, 2^{α}, where α is the position in the chain which leads to a doubling of fingers.
The LO signals are buffered by two parallel main buffers. Additionally, 7 differential data signals each for the I and Q RF-DACs are buffered. In total, 36 main buffers are placed at the input of each I/Q RF-DAC. The buffered differential LO and data signals are routed to the RF-DAC cells. The main buffers drive the internal routing bus which is connected to the local buffers. The local buffers are specifically designed to drive the RF-DAC cells transistor gates for the LO and data signals. The load capacitance of the data input is double the load of the LO input due to the design of the RF-DAC cells. Therefore, a single local buffer drives two RF-DAC cells, whereas the LO buffer is shared by two cells. The buffering allows to keep the alignment between signals and obtain equal rise and fall times. However, the cost of this architecture is its high power consumption due to the buffering of the signals for each cell. The buffers per I/Q RF-DAC consumes up to 80 mW depending on the LO even though the bare number of cells is reduced by a factor of 8 using pseudounary cells and by an additional factor of 2 using the presented sign processing method.

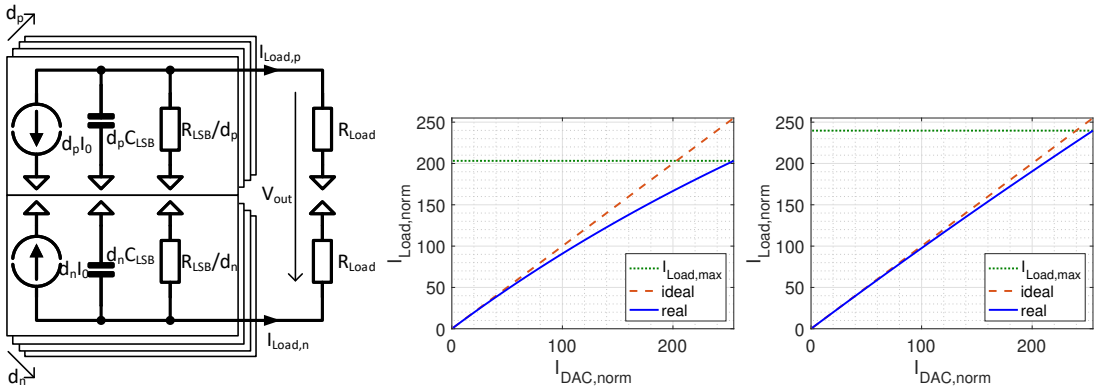
6.5.2 Pseudounary RF-DAC cells

The linearity of a current-steering RF-DAC is determined by multiple constant and dynamic effects. The main contributors can be summarised as the finite output

impedance of the current-steering cells, glitches during switching, and the process mismatch. At low frequencies, the constant errors limit the achievable SFDR, whereas with increasing frequency the dynamic errors dominate. The finite output impedance of the current-steering cells leads to distortion and, hence, a nonlinear relation between the applied word, d, and the output current as pointed out in [93–95]. The output impedance and the current of an LSB cell is examined in order to characterise this behaviour. Fig. 6.33a shows a simplified equivalent circuit of a current-steering cell that acts as a current source with a finite output impedance, $\underline{Z}_0 = R_{LSB} \parallel 1/j\omega C_{LSB}$, and a certain output current, I_0. In case of the RF-DAC, each cell becomes an AC current source where the amplitude is I_0 and the frequency is set by the LO. The output current of a certain number, d, of activated cells becomes ideally $I_{dac} = dI_0$, whereas the resulting output impedance reduces to $\underline{Z}_0/d$. However, the actual current, $I_{Load,n}$, delivered to a load resistance, R_{Load}, can be expressed as follows:

$$I_{load} = I_0 \frac{d}{1 + R_{Load}/(d\underline{Z}_0)}. \tag{6.1}$$

At low frequencies the capacitive part of the output impedance can be neglected, in turn, the linearity depends on the real part only. Fig. 6.33b and 6.33c show the load current at DC for a load resistance of 50 Ω and two different LSB cell output impedances, namely 50 kΩ and 200 kΩ. If $R_{Load} << dR_{cell}$ is not valid, I_{Load} has a



(a) Equivalent schematic. (b) R_{LSB}=50 kΩ. (c) R_{LSB}=200 kΩ.

Figure 6.33: RF-DAC linearity based on the output impedance and load.

nonlinear relation to the applied word. The nonlinearity can be controlled by a proper digital predistortion. Thereby, the maximum output current is set to $I_{Load,max}$ and the digital words are mapped to predefined values by a Look-Up Table (LUT) to obtain a linear increment while sacrificing the achievable ENOB. In this particular transmitter based on the FDDAC approach, 16 individual I/Q RF-DACs drive into the same node. Therefore, the predistortion needs to be performed for each complex coefficient pair based on multiple LUTs depending on the amplitudes of all 16 complex coefficients.

The, first integrated FDDAC transmitter does not contain digital predistortion methods to simplify the overall system. However, a sufficiently high output impedance at low frequencies can be obtained by several techniques such as cascode stages or improved current sources, *i.e.* Wilson current source. These techniques, however, form a trade-off between the imaginary and real parts of the output impedance. The RF-DAC cells operate in a frequency range from 4 GHz to 5.875 GHz. For a fixed load resistance, *i.e.* differential 100 Ω, the required output impedance of a single cell can be calculated depending on the total number of cells and the linearity restrictions. The FDDAC approach is implemented by a total of 16 8-bit I/Q RF-DACs driving into the same node which further tightens the linearity restriction of the complete FDDAC. In terms of resolution, the total number of cells in the complete FDDAC corresponds to a single RF-DAC with a resolution of $8 + \log_2 16$ where 16 is the number of bins. The prototype targets a conservatively high linearity and sacrifices output power since the focus is laid on demonstrating the feasibility of the approach rather than achieving a high output power.
Fig. 6.34 shows the schematic of one LSB cell with the corresponding transistor sizes of which 8 are combined to form a pseudounary cell. The architecture is initially presented in [96] as a DAC cell and extended to an RF-DAC cell in [10]. It increases the dynamic output impedance at high operation frequencies and reduces its dependency on the applied word. This is achieved by introducing bleeding currents. The transistor M1 acts as a current source. It is fairly large sized in order to improve the transistor matching. Furthermore, dummy transistors are placed around M1 which improves the proximity matching between the cells independent of their position in the arrays. The output current is set to approximately 25 uA per LSB cell which can be adjusted by changing the bias point of M1. The LO-pair M2 and M3 steer the current in the differential branches. The data transistors are implemented in a double-balanced structure. In order to increase the output impedance, the differential LO-pair is placed as far as possible from the output. The output is connected through thick-oxide transistors, M8 and M9, which operate in saturation region in order to isolate the internal nodes, ϕ_n and ϕ_p, from the voltage swing at the output. The thick-oxide transistors at the output stage further allow a high biasing voltage, 3.2 V, for the output of the RF-DAC cells. The gained voltage headroom is used to operate M8 and M9 in deep saturation as well as setting the DC operation point at the node ϕ close to the 1.2 V. The transistors M10-M15 form the bleeding current branches. The bleeding current is set to approximately 5 % of the output current. Thereby, the output stage is not switched off completely. It is barely conducting in any case which reduces the dynamic change in the output capacitance. The maximum DC current obtained when the SPM is set to 1 and all cells including the bleeding currents are activated, can be calculated by $(2 \times 16 \times 128 \times 25\text{uA}) \times 1.1 = 112\,\text{mA}$ from the high output supply voltage. It includes 16 I/Q RF-DACs where each contains 128 LSB cells. If the SPM is set to 0, the word independent minimum DC current is defined by the bleeding current wich is approximately 10 mA. The different modi for the sign processing changes the

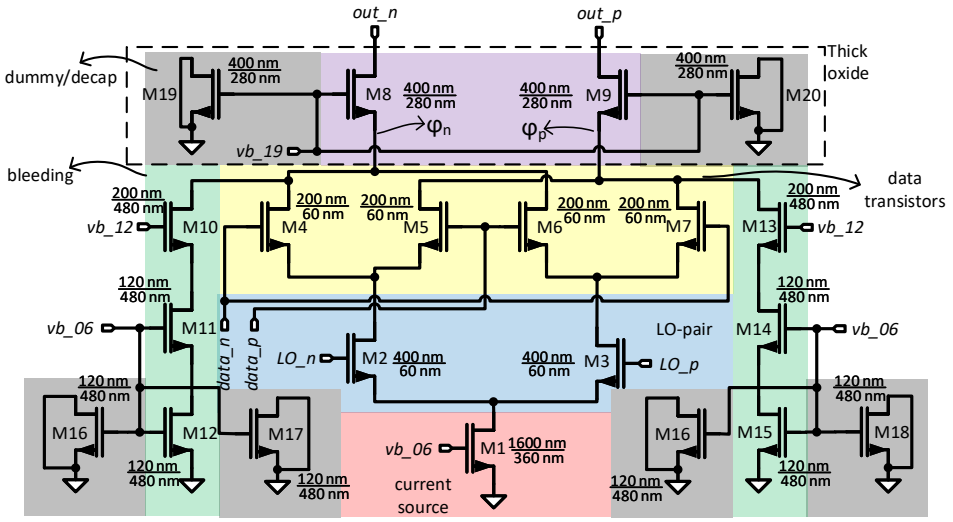


Figure 6.34: Schematic of the current-steering LSB cell including bleeding and dummy transistors.

switching behaviour of the utilised RF-DAC cells. The activated RF-DAC cells receive, independent of the SPM, differential data signals. The data transistors of the remaining not activated cells in the positive and negative branches are all switched on or off which results in zero differential output. If the SPM is set to 0, the output impedance and the DC current of *outn_n* and *outn_p* dynamically changes with regard to the applied word. On contrary, if the SPM is set to 1, the DC output current is constantly set to maximum which increases the DC power consumption. However, the output impedance variation depending on the applied word is significantly reduced since all branches conduct constantly, although the output current as well as the output power reduces slightly since the output impedance constantly moves on the lower end.
Fig. 6.35 shows various bias voltage sweeps performed on a single LSB RF-DAC cell with an ideal LO at 5 GHz. Note that the bias voltage, *vb_06*, of the current source, when swept in the range from 0.5 V to 0.68 V, enables a linear tuning of the maximum output current of each cell. In fact, this bias voltage is used to tune the output power of each cell or the cells in one I/Q RF-DAC operating at a certain frequency. The bias point of the thick-oxide transistors, *vb_19*, shall not be varied since it is set properly such that the transistors operate in saturation region. The bias voltage *vb_12* is introduced to switch off the bleeding current if necessary. Any variation of this bias point around the targeted 1.2 V is negligible.
Fig. 6.36a shows the DC current of an LSB cell sampled over transistor mismatch. The standard deviation of the variation is less than 4 % of one LSB current. In order to simulate the mismatch performance of a complete I/Q RF-DAC, the bias voltages are provided by ideal sources and the output voltage is delivered by an ideal bias-tee. The load is differential 100 Ω. Fig. 6.36c and 6.36b show the simulated ENOB and SFDR

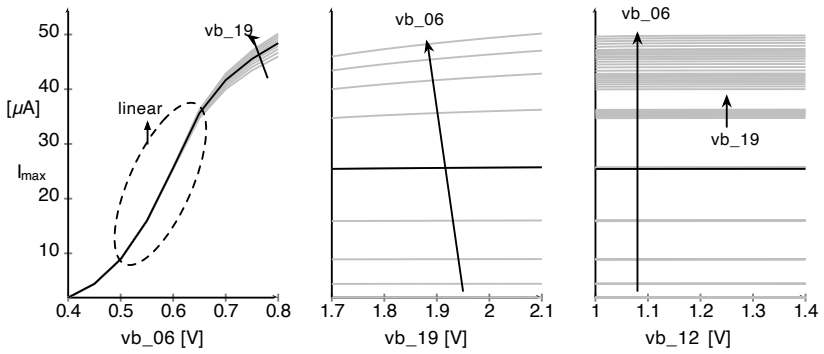
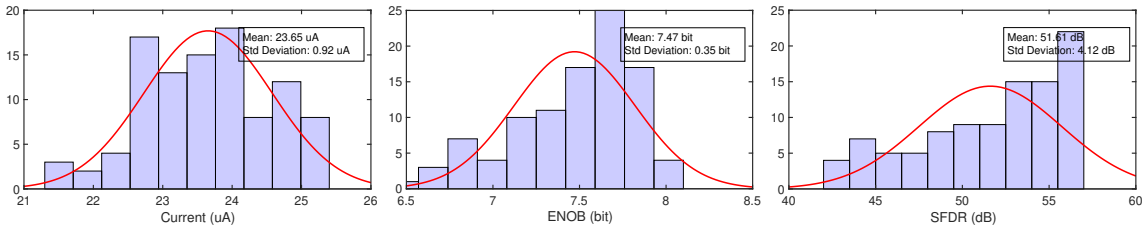


Figure 6.35: Simulated maximum DC current of the RF-DAC LSB cell for various bias voltage sweeps [97].



(a) DC current source. (b) ENOB. (c) SFDR.

Figure 6.36: Mismatch simulations of a single I/Q RF-DAC at DC and with a sinusoidal digital input. ENOB and SFDR are evaluated within $f_{LO} \pm 125\,\text{MHz}$.

of one postlayout extracted I/Q RF-DAC including mismatch of all transistors in the SPM mode 0. The sinusoidal digital tone at 2 MHz is sampled at 250 MSPS. The LO signal of the RF-DACs is provided by an ideal source at the frequency of 5 GHz.

6.5.3 Biasing circuits and distributed decoupling capacitors

Simulation results show that the output power of the RF-DACs decrease for increasing the LO frequency. Additionally, the shared differential output network, as shown in Fig. 6.31, introduces a significant capacitive load at the output of the RF-DACs which, in turn, leads to a reduction of the output power as well as forming an additional lowpass filter characteristic. Therefore, it is crucial to include an amplitude correction method. Thus, the current source of each cell is tuned by changing the bias point in a certain range. This is achieved by providing two different input currents, *bias_i_1* and *bias_i_2*, to the IC. The currents are converted to voltages by diode connected MOS transistors. The bias current has the advantage over a bias voltage that any on-chip GND bouncing is directly coupled to the generated voltage. Thus, a stable on-chip

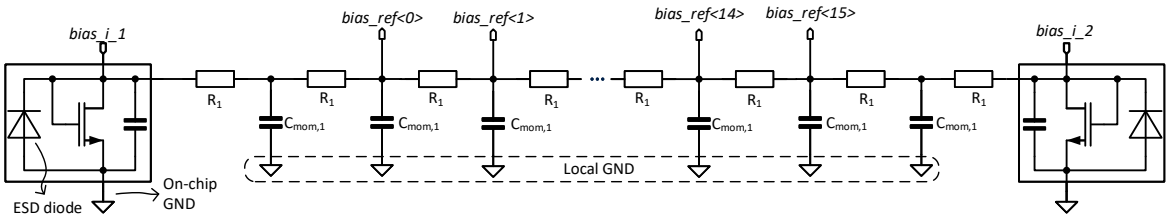


Figure 6.37: Schematic of the resistive bias slope generation circuit with two input bias currents.

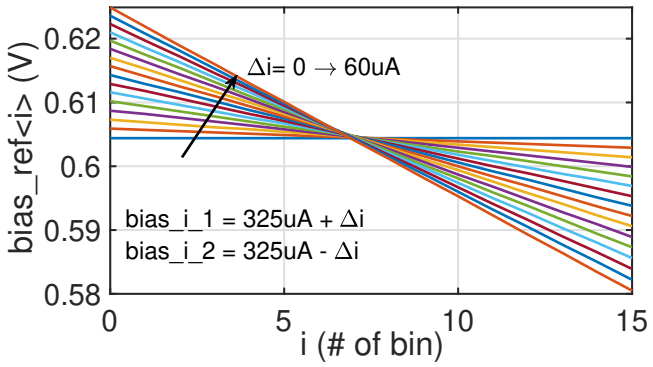
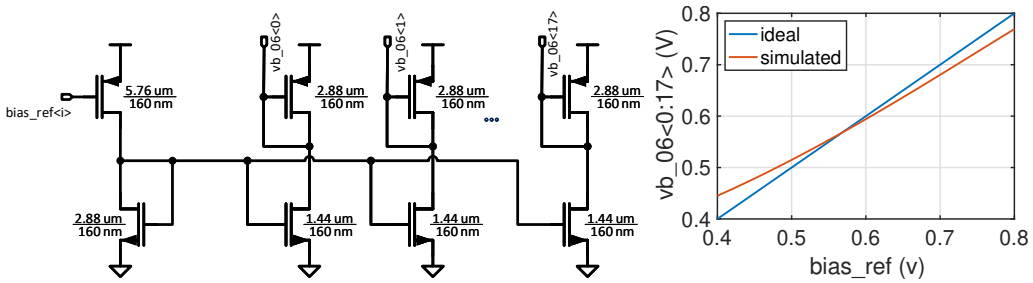


Figure 6.38: Reference voltages fed to 16 I/Q transmit cores.

bias voltage versus the appropriate on-chip GND is obtained. The current inputs are placed on two edges of the IC. A series of resistors and shunt capacitors, as shown in Fig. 6.37, are used to create 16 linearly gradating bias voltages where each is delivered to one I/Q transmit core. This allows to linearly tune the amplitude deviation of the output. Each of the $bias\_ref$ signals are coupled by a large capacitive bank to the local GND in close proximity of the I/Q RF-DACs. Thereby, the voltage routing over a long distance can be tolerated. Fig. 6.38 shows the $bias\_ref <: 15 >$ voltage for the 16 I/Q transmit cores. A linear voltage slope across the I/Q transmit cores can be generated by varying the biasing current.
Each $bias\_ref$ is connected to 256 LSB current sources and bias voltage decoupling capacitors banks which are distributed inside the cells and around the routing lines to the pseudounary cells. The large of gate area connected to the reference voltage draws gate currents caused by gate tunnelling and charge injection which, in turn, distort the linear gradation between the bias voltages. Additionally, a direct connection of the reference voltages over an RC network results in poor isolation between the RF-DACs operating at different frequencies among each other such that the charge injection to the reference node is directly fed to the adjacent RF-DACs. Therefore, in each I and Q RF-DAC the circuit shown in Fig. 6.39a is implemented to copy the reference voltage to the 18 pseudounary RF-DAC cells and isolate the bias voltages from the



(a) Schematic of reference voltage copying circuit. (b) Input reference voltage versus output voltage.

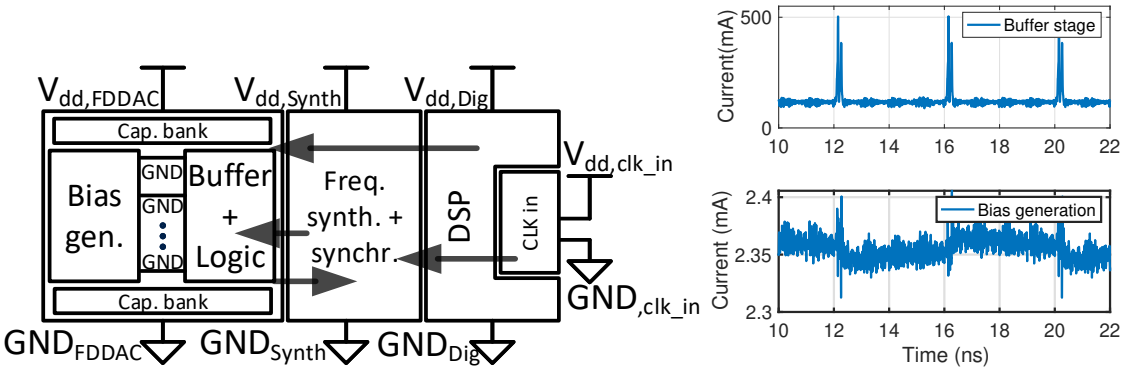
Figure 6.39: Schematic and simulation results of the reference voltage copying circuit.

resistive bias slope generation network. The voltage copying circuit utilises fairly large transistors with a large gate area to improve matching. It comes at the cost of high DC power consumption. Each voltage copy circuit consumes approximately 1.25 mA which results in 24 mW for the 16 I/Q transmit cores. Fig. 6.39b shows the simulated copied voltage depending on the input voltage. The slope of the output voltage deviates from the ideal line. However, the transfer function remains linear.

6.5.4 Supply domains and power budget

Fig. 6.40a shows the different supply domains implemented on the transmitter IC. The supply and GND of the DSP block is separated from the remaining blocks in order to isolate the digital noise from the analogue-mixed-signal blocks. The digital block contains distributed decoupling capacitors within the actual design. The input clock needs to be placed on an additional supply domain due to the restriction of the floor plan. Furthermore, the ring-oscillator-based frequency synthesisers as well as the synchronisation blocks operate in their own supply domain. The RF-DAC-based I/Q transmit cores contain a high amount of data and LO-buffers. Furthermore, the FDDAC-based transmitter approach demands on fully synchronised transmit cores operating at equidistantly spaced frequencies. All phasor tones and the resampling of the coefficients is aligned which leads to a simultaneous activity with a periodicity of 4 ns. Accordingly, the supply domain of the FDDAC suffers from current peaks which, in turn, lead to supply instability caused by the IR drop as well as the inductance of the bondwires. The system simulations for verification contain the bondwire inductances as modelled in *Keysight ADS*®. The ground of the FDDAC, GND_{FDDAC}, is provided by each 6 down bonds on the top and bottom edges. The supply voltage, $V_{dd,FDDAC}$, is connected via 5 bondwires on both edges. Consequently, the simulated bondwire inductance is 300 pH for GND and 600 pH for supply connected to two edges of the

IC. The voltage swing caused by the inductance is stabilised by large capacitor banks placed close to the supply pads. These capacitor banks are based on MOS gates capacitors. Each capacitor bank is based on building units, each measures 10x10 um and provides a simulated capacitance of 1.34 pF which slightly decreases with increasing frequency. Capacitor banks of each 222 units is implemented on the top and bottom edges resulting in a total decoupling capacitor value of 595 pF. These banks supply two internal domains which share the same GND, namely the buffers including the logic circuits and the analogue circuits such as the bias generation blocks. The IR drops caused by peak currents are compensated by distributed local capacitors. This approach further isolates the main aggressors, namely buffer stages and logic circuits implemented in the I/Q transmit cores, from the analogue circuits.



(a) Block diagram of the implemented supply domains. (b) Current consumption of two I/Q RF-DACs from an ideal source.

Figure 6.40: Supply domains including signal handovers and the current consumption of the RF-DACs.

The arrows in Fig. 6.40a show the signal forwarding across the supply domains. Unfortunately, the simulation of the complete system regarding the various on-chip supplies and signal flow between the domains cannot be carried out due to several reasons. The technology does not allow the access to the digital standard cells. Moreover, the number of transistors and nodes is impractically high to simulate the complete FDDAC alongside with the frequency synthesis blocks on the existing IT and computing infrastructure.
Fig. 6.40b shows the simulated current consumption of two extracted I/Q RF-DACs from an ideal voltage source. The bias generation circuits consume a DC current without significant peaks. The LO of the simulated RF-DACs are 5 GHz and 5.125 GHz. The DC current consumed by the buffer stages and the logic-gates is 105 mA which is dominated by the LO buffers operating at high frequencies and scales with the frequency. The RF-DACs sample the digital input at a sampling rate of 250 MHz and the LOs are perfectly aligned at the same sampling point. This leads to current peaks of up to 375 mA above the DC current for the two RF-DACs with a period of 4 ns.

For 16 RF-DACs, the current peaks add up to 2 A above the DC power consumption of approximately 870 mA. These current peaks lead to a voltage swing over the bondwire inductances and IR drop which needs to be considered in the full-system simulation. The decoupling capacitors stabilise the on-chip voltages between GND and supply. However, different supply domains with several on-chip GNDs might swing differently leading to increased jitter and timing errors by the appearance of signal handovers across the supply domains. Furthermore, the FDDACs are fully differential which suppress common-mode variations caused by the unstable supply.
The supply voltage of the output of the RF-DACs is delivered via the bias-tees. It strongly depends on the SPM and the applied data.

6.6 Top-level implementation and full-system simulations

The top-level design contains the frequency synthesis and the synchronisation blocks implemented in [82]. The entire frequency synthesis block is integrated on the same chip. The ring-oscillator-based PLL is selected due to its low power consumption and small size. Accordingly, it can be placed on a single transmitter chip with a reasonable performance multiple times. However, this PLL type has an inherit drawback in terms of phase noise at high frequencies. Thus, the PLLs operate at half the frequency followed by a DLL-based multiplier. In this configuration, a trade-off for the overall SFDR and phase noise performance is achieved. The DCDLs in the ADDLLs are controlled by 8-bits. The counter-based synchroniser controller detects the delay difference between the output of the I-path of the DCDL and the reference signal which operates at 125 MHz. An overall resolution of 1.5 ps has been achieved in simulations. The phase aligned differential $LO_{IQ,synch}$ signals are then sent to the RF-DACs.
The complete FDDAC transmitter contains a tremendous high number of transistors which need to be extracted and simulated in order to estimate the system performance. Unfortunately, it is not possible to run such complex simulations with the IT infrastructure available. Therefore, several approaches are implemented to simulate the complete transmitter in *Cadence Virtuoso*®. A multitude of blocks used in the complete system are modelled using *VerilogA*. A detailed analysis and discussion of the system modelling is presented in [97, 98]. The models have been implemented in different abstraction levels leading to a trade-off between the accuracy and the required computation speed. The highly abstracted low-level models are used to simulate interconnections and check the system integrity. The more accurate high-level models require a slightly increased computation power. Nevertheless, the obtained simulation results are closer to the actual system. Furthermore, the models allow to simulate the complete transmitter

while focussing on certain blocks which can be isolated and simulated in, *i.e.* parasitic extracted mode. Thereby, the performance and the impact of these blocks on the overall system performance can easily be estimated.
However, actual circuit simulations are required in order to estimate the effect of supply domains and correctly simulate S-parameter based blocks such as EM-simulated passives or components which are used in the measurement setup. In order to improve the simulation speed, the layout of each RF-DAC contains the top-level routing for supply and GND connections as well as certain parts of the bias delivery networks such as the RC bias slope network. This allows to extract smaller subcells rather than the 16 I/Q transmit cores at once leading to comparably smaller netlists. The most significant advantage here is that those blocks forward the signals from one extracted block to the next one which, in turn, allows the investigation of their effects of the the supply tree and the distributed decoupling capacitors in addition to the capacitor banks. Additionally, IR drops occurred at the supply routing across the 16 I/Q transmitters can be catched and the effects on the system performance is judged. Two I/Q RF-DACs sharing the same input bus and the same connection to the output routing network, as shown in Fig. 6.31, are extracted as a single block and used 8 times. The following system simulations are based on postlayout extracted RF-DACs.

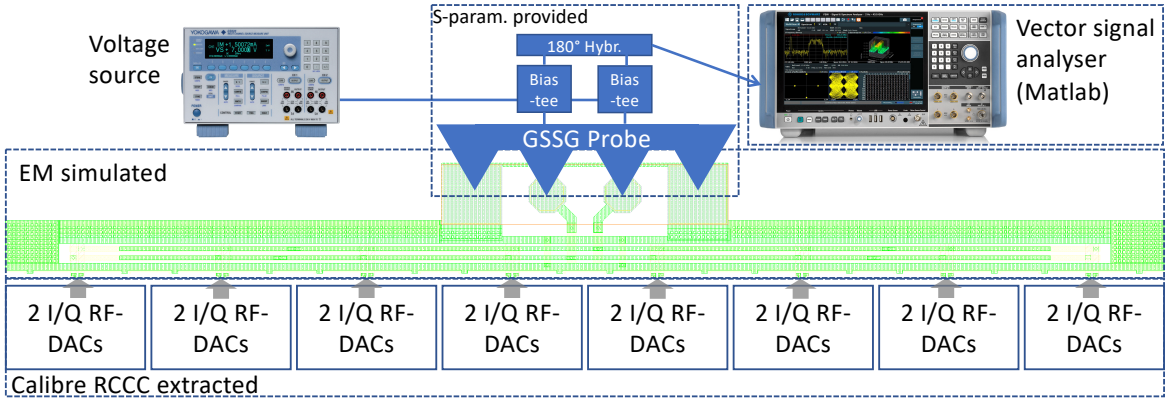
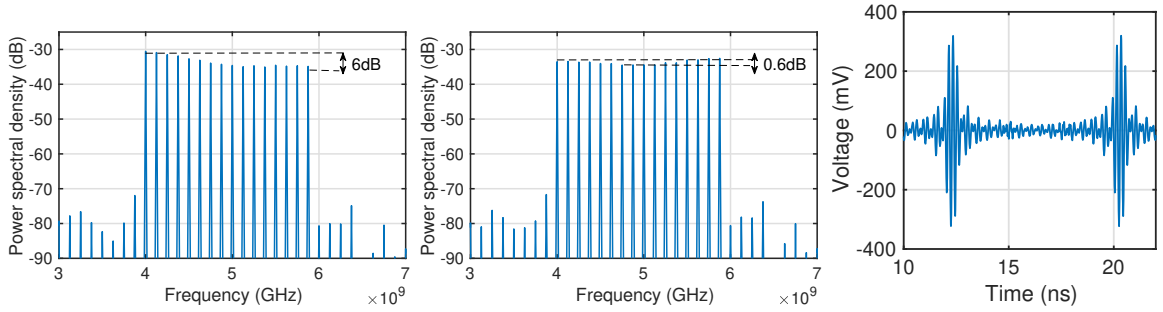


Figure 6.41: Implementation of the output routing passive including the bond pads, external bias-tees, and the measurement setup.

The output of the FDDAC-based transmitter is probed on-wafer by differential Ground-Signal-Signal-Ground (GSSG) probes. The high modulation bandwidth of 2 GHz in the sub-6 GHz range results in a high fractional bandwidth. On-wafer probing in combination with ultrawideband external bias-tees is used to ensure a flat frequency response and linear phase relation over the entire modulation bandwidth. The phase transfer characteristics and low group delay deviation is crucial due to the high modulation bandwidth. The outputs of the RF-DACs are connected to an EM simulated passive network and accessed over LOW-C pads available in the technology, as shown in Fig. 6.41. The S-parameters of the additional components are measured and included

in the test setup. The output is connected to measurement equipment with Vector Signal Analyser (VSA) capability such as the *Rohde und Schwarz FSW* signal spectrum analyser or a high-speed oscilloscope.
The parasitic capacitance of the output routing network as well as the capacitive part of the output impedance of the 16 8-bit I/Q RF-DAC cells reduce the output AC swing. In fact, the AC current at LO frequencies from 4 GHz to 5.875 GHz delivered to the load is considerably less compared to the DC current of the acquired RF-DAC cells. The significantly reduced output power increases the linearity which is already designed conservatively. Moreover, the output power decreases with increasing frequency. Fig. 6.42a shows the simulated output spectrum of the complete FDDAC transmitter where each RF-DAC is sampling the highest positive digital word instead of the Fourier coefficients. In this particular mode, referred to as *all_dac_set_max* and implemented in the DSP as well, the SPM value does contribute to the behaviour since all cells are activated. The PSD exhibits 6 dB of an amplitude deviation over the output frequency



(a) No bias correction. (b) With bias correction. (c) Transient waveform.

Figure 6.42: Full-system simulation in the *all_dac_set_max* mode.

range. Fig. 6.42b depicts the PSD when the correct bias currents are applied to equalise the amplitude deviation. The remaining deviation of 0.6 dB is mainly caused by the unequal lengths of connections of the output routing network. However, the obtained variation of 0.6 dB is negligible for the transmitter performance according to the system simulations. Fig. 6.42c shows the transient output in the *all_dac_set_max* mode. The peak-to-peak output voltage over 100 Ω achieves 644 mV which, in turn, translates to a peak output power of 4.15 mW or approximately 6 dBm. Despite that, during the operation of the FDDAC the amplitude probability density function of the Fourier coefficients is concentrated at 30 % to 60 % of the full-scale. Additionally, the peak voltage can only be achieved at certain time points due to additive superposition. The usable range of the FDDAC is comparably lower than the highest peak-to-peak voltage. Additionally, the QAM already has a high Peak-to-Average Power Ratio (PAPR).
Fig. 6.43 shows the simulated PSD of the single-tone stimulation with a digital sinusoidal tone at 2 MHz. This simulation is based on postlayout extracted blocks including the S-parameters of the passives as well as the external measurement setup. Further-

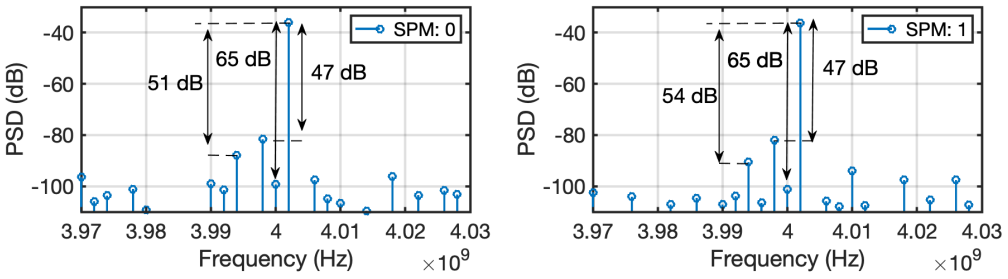
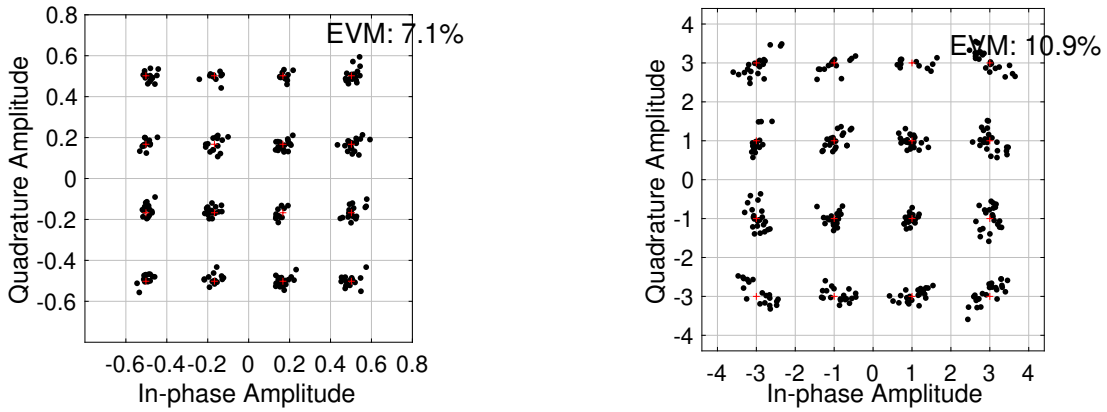


Figure 6.43: Simulated PSD of the full-system simulation output with one I/Q transmit core sampling a sinusoidal digital tone.

more, the supply voltages and bias currents are provided by the modelled bondwire inductances and the on-chip decoupling capacitors. The I/Q transmit core at 4 GHz is characterised in both sign processing modi. The output power at the desired frequency is −37 dBm. The LO feedthrough is less than −65 dBc and the third-order harmonic of the sinusoidal tone exhibits signal powers of −51 dBc and −54 dBc less than the fundamental tone depending on the SPM modi. Furthermore, the PSD exhibits an image-rejection of 47 dB due to the imperfection in the output routing of the I and Q RF-DACs. Nevertheless, for the assumed system parameters, the given I/Q imbalance of the RF-DACs is not limiting the performance of the complete transmitter. Moreover, the obtained signal power at the output is approximately −36 dBm. The SPM does not effect the output power, although the linearity is slightly improved if the SPM is set to 1.

As described in Section 6.3, the DSP is simulated separately and its output is read by the *Cadence*® test-bench during the simulation. The differential output of the full-system simulation is sampled and saved such that the VSA can be performed outside *Cadence*®. The VSA is utilised by an adapted version of the system model in *Matlab*®. The frequency synthesis block within the full-system simulation however is modelled by dedicated *VerilogA* models which support periodic jitter, *i.e.* spurious tones, phase noise, I/Q imbalance, and timing errors. The models of the synchronisation blocks and frequency sources do not contain any settling time or locking behaviour as this would increase the simulation time. They immediately start at the predefined specifications. Fig. 6.44 shows the simulated constellation diagrams in the HBM where the bins 0-to-7 are utilised. The simulation is based on the postlayout extracted FDDAC.

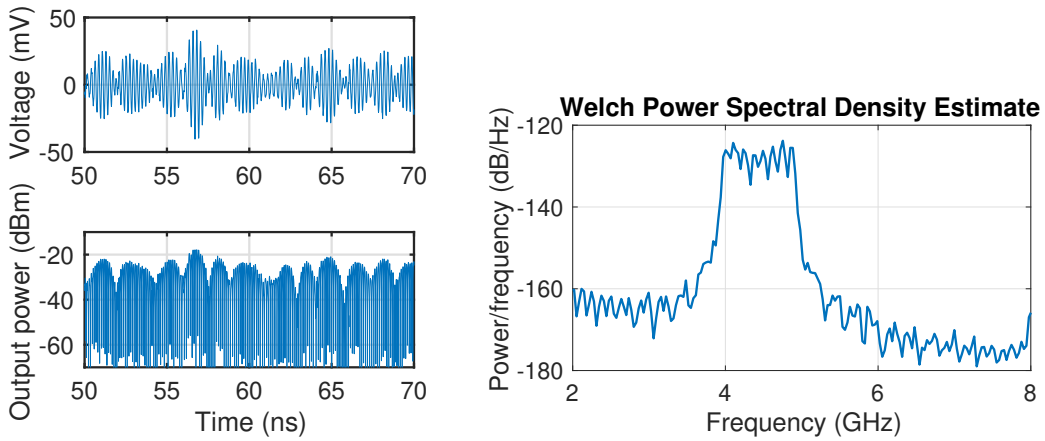
The performance of the frequency synthesis block is set, as shown in Table 6.1, based on system simulations. The EVM performance deteriorates from 7.1 % to 10.9 % when taking into account the inductance of the bondwires in combination with the on-chip decoupling capacitors. The transient output signal and the instantaneous power sampled at the differential 100 Ω load is shown in Fig. 6.45a. The peak power is −17.19 dBm, whereas the RMS power is −25.81 dBm. Fig. 6.45b shows the simulated PSD of the transient output signal.



(a) HBM with ideal supply.

(b) HBM including bondwire inductances.

Figure 6.44: Simulated constellation diagrams of the complete transmitter in the HBM with and without the effects of the on-chip supply.



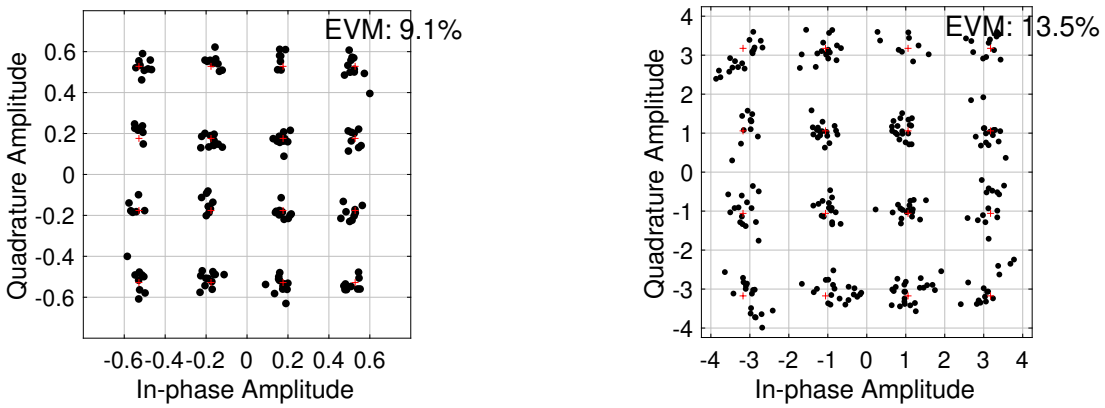
(a) Trans. output and inst. power.

(b) Simulated PSD.

Figure 6.45: Simulated output char. of the FDDAC-based transmitter in the HBM.

Fig. 6.46 shows the simulated constellation diagrams in the FBM. Here, the modulation bandwidth is 2 GHz which results in a data rate of 8 Gbit/s. The estimated EVM including the bondwire inductance is 13.5%. Fig. 6.47a shows the transient output and the instantaneous output power. The peak power is −15.5 dBm and the Root Mean Square (RMS) power is −23.6 dBm. The PSD shown in Fig. 6.47b exhibits a low-frequency resolution since transient simulations are executed for a relatively short time. However, the spectral shaping and the modulation bandwidth show the expected behaviour.

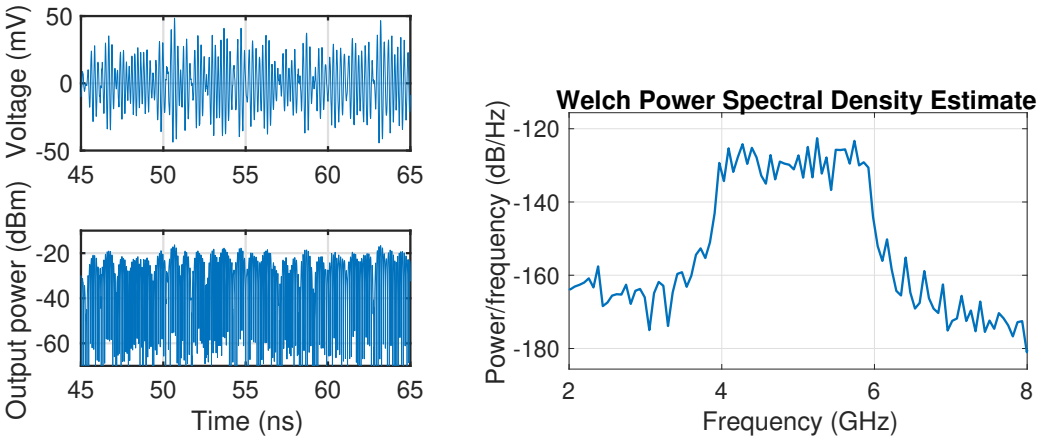
The simulated constellation diagrams in the HBM and FBM both show performance degradation when the bondwire inductances are included in the top-level simulation. The main cause for this is rather the voltage swing generated by the bondwire inductiv-



(a) FBM with ideal supply.

(b) FBM including bondwire inductances.

Figure 6.46: Simulated constellation diagrams of the complete transmitter in the HBM with and without the effects of the on-chip supply.



(a) Trans. output and inst. power.

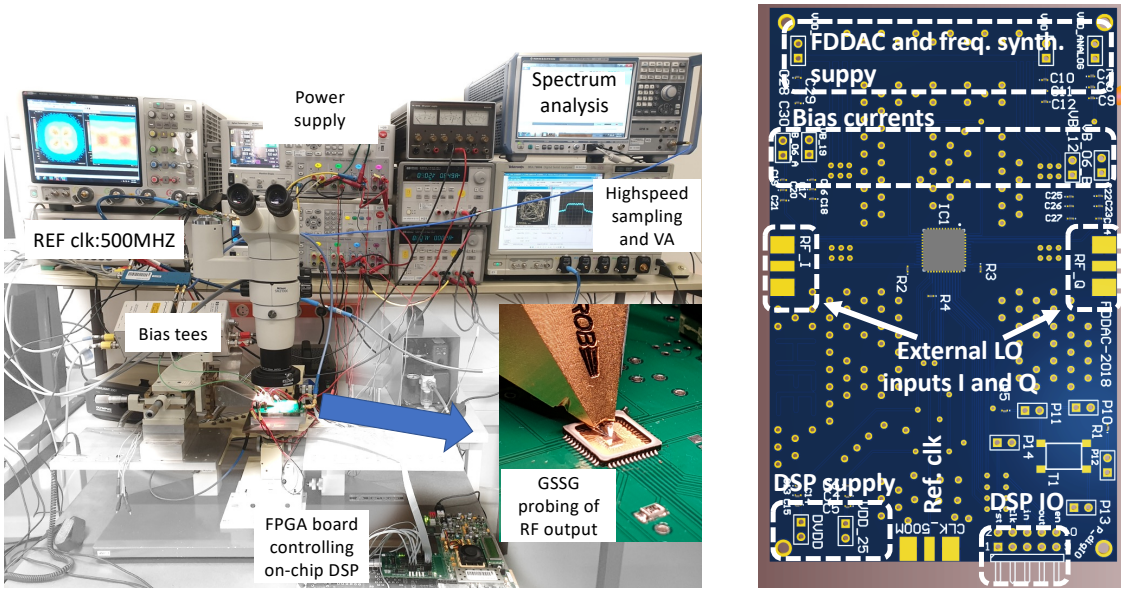
(b) Simulated PSD.

Figure 6.47: Simulated output char. of the FDDAC-based transmitter in the FBM.

ity than the internal IR drops. Therefore, the performance of the complete transmitter could be improved by adding additional decoupling capacitors close to the supply pads. However, the available silicon area is limited.

6.7 Physical verification and measurement setup

The first integrated FDDAC-based transmitter is measured using a hybrid setup where the output is probed on-wafer using differential GSSG probes, whereas the digital



(a) Photograph of the measurement setup.

(b) PCB providing supply, reference clock, and digital I/O.

Figure 6.48: Photograph of the on-wafer measurement setup and the utilised PCB.

I/O, supply voltages, bias currents, and input clock are provided through the PCB. The measurement setup and the implemented PCB are shown in Fig. 6.48. The QFN package is mounted on an appropriately designed PCB and the lid of the package is opened for probing. However, the PCB which contains components on the top and bottom layer must physically be fixed on the wafer probing station in order to align the probing tips. For this purpose, an aluminium block is designed which can be mounted on the chuck of the probing station. The PCB is screwed in, whereas the area underneath the package is additionally supported by a platform to prohibit any tension while probing. On the PCB, the supply voltages as well as the bias currents are stabilised with several capacitor banks. Additionally, different sizes, footprints, and capacitor types are added to ensure the stabilisation of the voltages over a large frequency range.
The input clock at 500 MHz is provided by a reference oscillator with outstanding phase noise performance. In total, 4 supply voltages and 4 bias currents are connected to the PCB and the bias-tees. The spectral analysis is performed by *Rohde und Schwartz FSW26*. However, the analysis bandwidth of the VSA in the FSW is limited to 160 MHz. Therefore, a high-speed oscilloscope, namely *Tektronix DSA70604*, is used which provides a sampling rate of up to 25 GSps. Its analogue input bandwidth spans up to 6 GHz. Furthermore, the device comes with a VSA tool with limited but sufficient capabilities. The manufactured IC is controlled by an additional FPGA board.

6.7.1 FPGA-based transmitter IC controller

The first monolithically integrated DSP is used to set the transmitter in different modi and adjusts settings of several blocks, such as selecting the sign processing mode or changing the delay of the resampling clock. Fig. 6.49 shows the block diagram of the communication setup. The DSP including the serial interface communicates over 5 digital I/O ports which are provided by an appropriate serial interface transmitter implemented on the *Xilinx Virtex-7*® FPGA. However, it is required to change the setup of the IC dynamically during the measurement in order to calibrate and characterise various modes. Therefore, an additional communication between the FPGA and a host PC is essential. A dedicated USB controller chip on the FPGA evaluation board opens a COM port which is accessed via USB and translates the communication stream from the PC into UART that is sent to the FPGA. The input provided over the PC to the FPGA is processed in the $uart_{rcv}$ block within the ser_{tx} block. The register

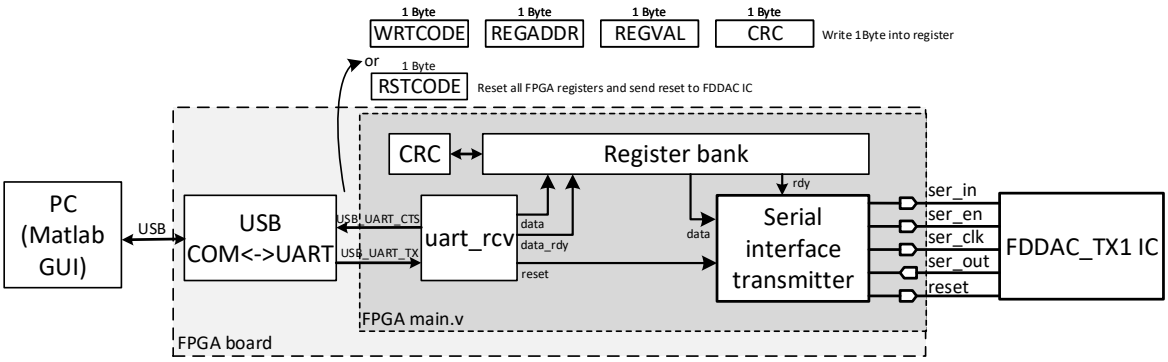


Figure 6.49: Block diagram of the communication chain from the host PC to the integrated IC over the FPGA board.

bank contains 8-bit registers, whereas 5bytes equal to 40-bits shall be transferred to the IC consecutively. In order to write one register, 4 bytes are transmitted from the PC including the write command, the address of the register, the byte as a payload and a CRC checksum. By setting a certain *data_rdy* register, the serial interface transmitter, ser_{tx}, is triggered and starts communication. The host PC can also reset all registers on the FPGA by a dedicated command word which also is passed through to the FDDAC IC by the serial transmitter. In case the last command was successfully transmitted to the IC, and there are no new commands from the host PC in the queue the complete communication to the chip is stopped by the FPGA. This also includes the serial interface clock, *ser_clk*. Consequently, digital switching noise at low frequencies can be omitted. Additionally, a Graphical User Interface (GUI) is implemented which contains multiple sets of predefined commands in order to simplify the setup and debugging of the IC.

6.7.2 Measurement results

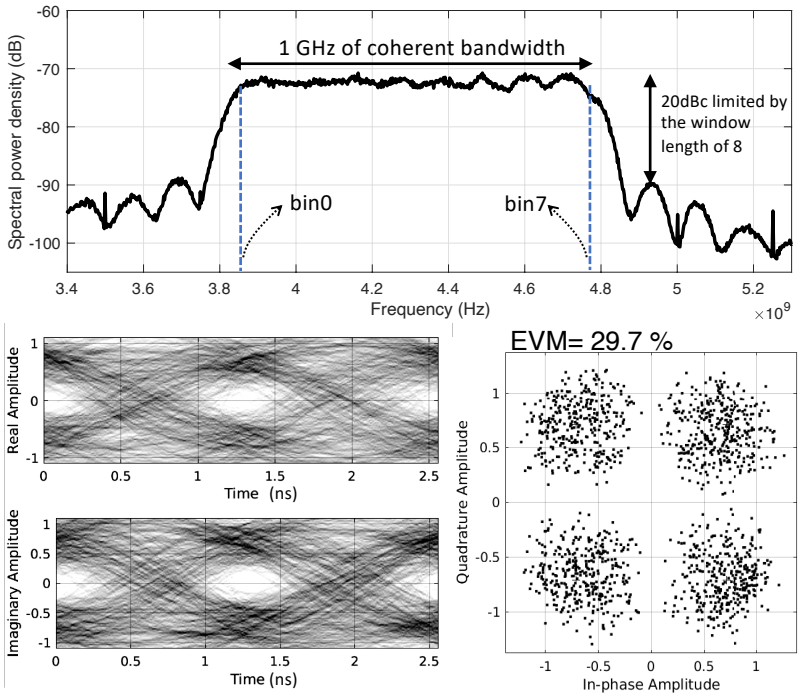
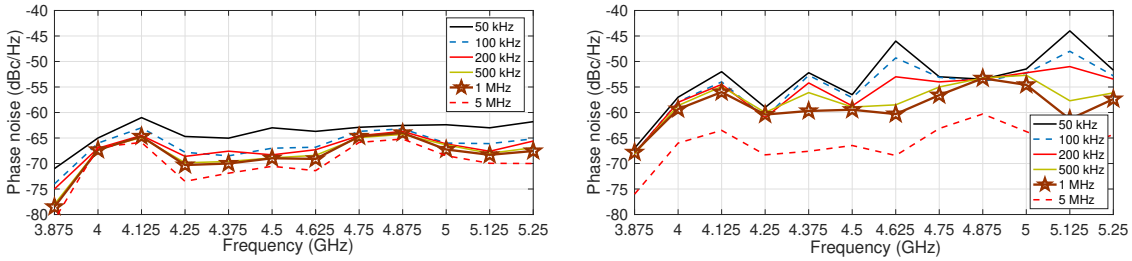


Figure 6.50: Measurement results of the FDDAC-based transmitter in the HBM [35] ©2020 IEEE.

The first FDDAC-based transmitter demonstrates the flexibility of the proposed concept and has been implemented for 16- and 8-point-FFT FBM and HBM corresponding to a bandwidth of 2 GHz and 1 GHz, respectively. The hardware validation and the proof-of-concept is successfully demonstrated by the results in Fig. 6.50 which shows the measured constellation diagram of a QPSK modulated signal with 1 GHz of coherent modulation bandwidth. The measured EVM for the first integrated prototype is 29.7 % in the HBM. The FBM could not be measured since all 16 PLLs generating the phasor tones do not work at the same time. Especially, the PLLs at higher frequencies could not be locked properly. The measured EVM deviates from the simulation results due to the degraded overall performance of phasor tones.
Fig. 6.51 shows the measured phase noise of the phasor tones evaluated at various offset frequencies. The average phase noise evaluated at at 1 MHz offset to the phasor tones is −70 dBc/Hz or −60 dBc/Hz depending on the activity of the synchronisation block. Unfortunately, the phase noise performance is up to 30 dB worse than what was initially assumed in system simulations.
Fig. 6.52a shows the measured PSD in the *all_dac_set_max* mode where the RF-DACs are set to the full-scale and the synchronisation blocks are switched off. The phasor tones of bins 0-to-7 are fed directly to the output. The in-band SFDR is less than 20 dBc.

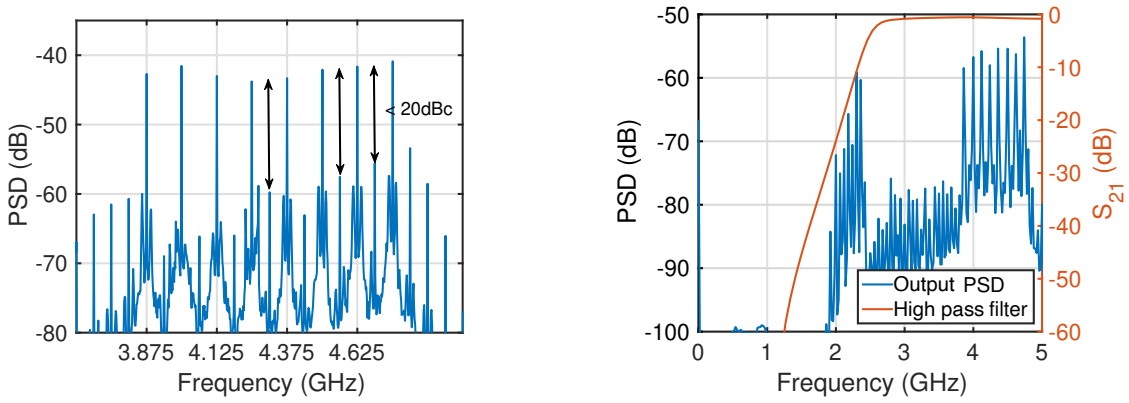
It is limited by spurious tones with an offset frequency of 62.5 MHz to the phasor tones. Moreover, the power of the phasor tones vary by 4 dB after the slope correction. Fig. 6.52b shows the highpass filtered PSD of the same bins over a large frequency span. The phasor tones exhibit spurious tones at half the frequencies. The amplitudes of these spurious tones are significantly higher than the fundamental tones. Therefore, the output is fed via a highpass filter to the spectrum analyser as well as to the high-speed oscilloscope for the VSA. Furthermore, the second frequency synthesiser based on frequency multipliers and the external LO input turned out as nonfunctional. The single-tone measurement mode is used to characterise the performance of each I/Q transmit core. The DSP generates sinusoidal tones at 250/128 MHz with a sampling rate of 250 MSps. Fig. 6.53 shows the output PSD of the bins 1-to-8 where the phasor tones are modulated with sinusoidal digital tones at approximately 2 MHz. The single-tone measurement shows the imperfect performance of the transmit cores realising the bins. The LO-feed through is better than −36 dB. The power of the third-order harmonic of the sinusoidal tone which is introduced by the nonidealities of the RF-DAC is more than 33 dB less compared to the fundamental tone. The I/Q phase and amplitude mismatch of the phasor tones in the worst case leads to an image-rejection of −17 dB. The DSP is able to move the modulated output band in the HBM in discrete steps of 125 MHz by utilizing a different set of bins. Fig. 6.54 shows the output spectrum of the FDDAC transmitter utilising the bins 1-to-8. Furthermore, the intrinsic filtering capabilities of the Nyquist replicas are demonstrated. The dashed grey line shows the spectrum for random modulation on each bin at Nyquist rate which leads to a superposition of multiple sample-and-hold transfer characteristics, namely *sinc* functions in the spectrum. Spectral shaping in the transmit band is achieved by applying the proper baseband processing of the FDDAC transmitter including the windowing approach. The sampling rate is not changed. The out-of-band emissions are reduced to −20 dBc as simulated in Chapter 3.1. In this particular case, the attenuation of the out-of-band emissions is limited by the window length of 8 and matches well with the results of the system simulations.



(a) Synchronisation block disabled.

(b) Synchronisation block enabled.

Figure 6.51: Measured phase noise performance of the frequency synthesisers over the bin frequencies evaluated at various offset frequencies [82].



(a) Phasor tones for bins 0-to-7. (b) Highpass filtered phasor tones.

Figure 6.52: Measured phasor tones for the bins 0-to-7 in the mode *all_dac_set_max*.

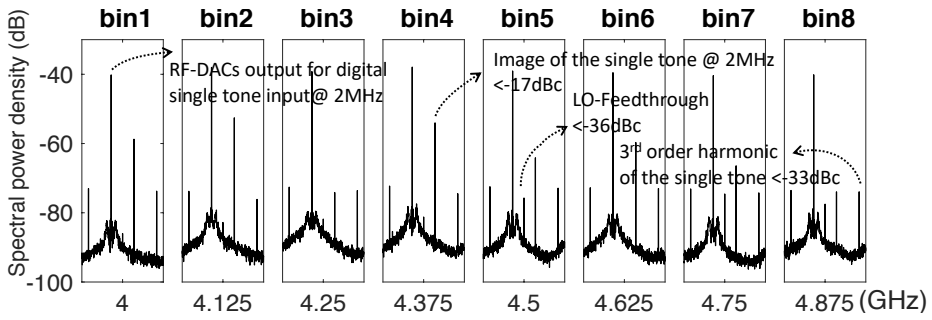


Figure 6.53: Meas. PSD of sinusoidal single-tone modulation on the bins 1-to-8 [35] ©2020 IEEE.

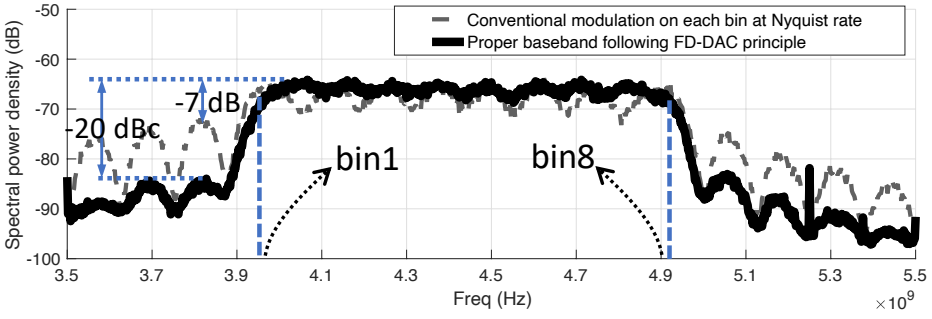


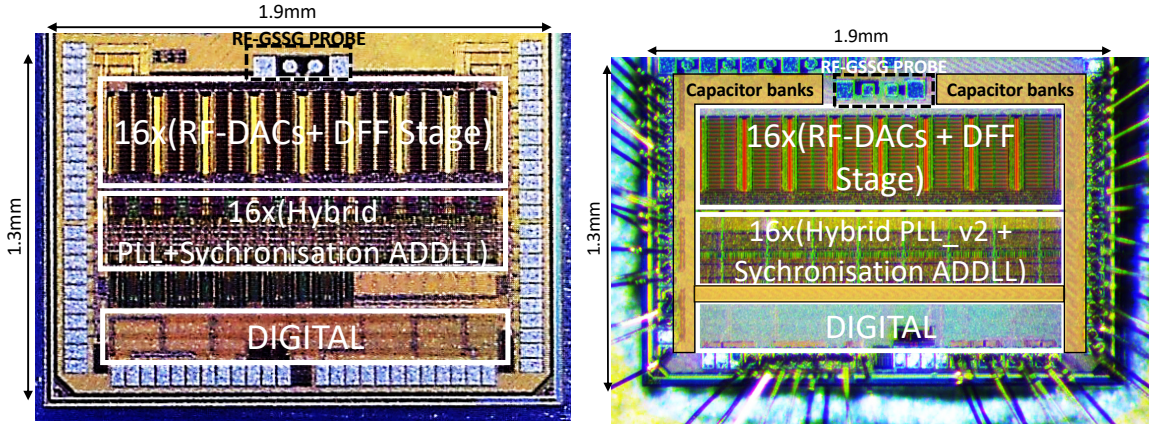
Figure 6.54: Spectral shaping performance of the FDDAC transmitter vs. Nyquist rate modulation on each bin [35] ©2020 IEEE.

6.7.3 Discussion: *FDDAC_TX1*

The measurement results reveal a significant deviation from the initially estimated performance of the frequency synthesis blocks [82]. The measured phase noise and SFDR are included in the system simulation in order to reproduce the measured transmitter performance. The system simulation confirms that the obtained performance drop is caused by the actual phase noise performance of the frequency synthesisers. However, the performance, shown in Fig. 6.50, for the given bandwidth is still competitive and proves the robustness of the FDDAC-based transmitter. The DSP is fully operating and performs as simulated. Furthermore, the communication between the transmitter IC and the host PC is extremely stable. The digital delay tuning of the *clk_resample_*250 signal works as expected. In all cases, a certain setup can be found that the coefficients are sampled correctly. The performance of the RF-DACs, as it could be measured, shows, if any, minor degradation compared to simulation results. The average LO feedthrough is better than −43 dB. The power of the third-order harmonic at full-scale is in average more than 40 dB lower than the fundamental tone. The main contributors deteriorating the performance of the complete transmitter are the lack of stable supply voltages, especially in the frequency synthesis part, unpredictable supply domain crossings which could not be simulated, and restrictions originating from the floor plan. Furthermore, the nonidealities of the synthesised tones also effect the synchronisation blocks by means of phase noise, IQ imbalance, and locking performance. Consequently, the phasor tones bottleneck the performance of the complete transmitter.
After compiling the measurement data, it is decided to implement a redesigned IC, namely *FDDAC_TX1.5*. The design iteration follows the tick-tock approach as discussed in Chapter 5. The I/Q transmit cores, DSP, floor plan, and system design implemented by the author are mostly unchanged. On contrary, the frequency synthesis blocks are redesigned for improved performance [82]. The on-chip decoupling capacitors of the I/Q transmit cores have been increased by a factor of 4 GHz, *i.e.* to 1.8 nF. Thus, the performance drop which is obtained after including the bondwire inductances in the full-system simulation, is minimised. Additionally, a significant amount of decoupling capacitors are added to the supply domain of the frequency synthesis blocks in order to improve the on-chip supply. Furthermore, computing power hungry system simulations could be carried out on updated IT and computation infrastructure which suggested optimisation potential in the supply domains. Therefore, the input clock processing block and the frequency synthesizers have been moved to the same supply domain. A supply domain, only for the ring oscillators, is introduced which shares the same on-chip GND with the remaining frequency synthesis block. Finally, the output frequency range has been reduced to lower frequencies, *i.e.* to 3 GHz to 4.875 GHz. The equidistant frequency spacing and the modulation bandwidth is sustained. Additionally, the PCB has been updated to provide the supply voltages of different domains separately. The

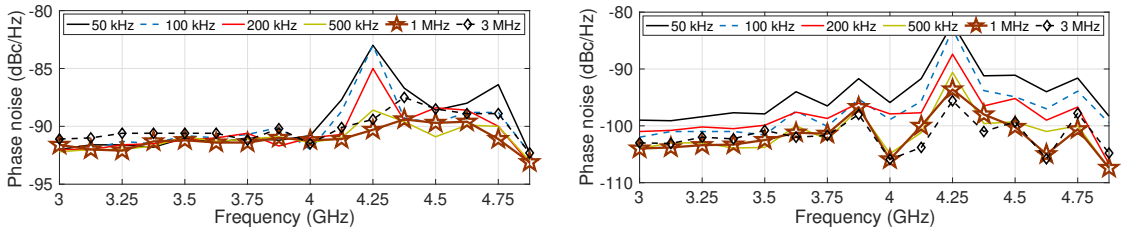
size of the on-PCB decoupling capacitors is increased and they are moved as close as possible to the IC.

6.7.4 Measurement results of the *FDDAC_TX1.5*



(a) Chip micrograph of the *FDDAC_TX1*. (b) Chip micrograph of the *FDDAC_TX1.5*.

Figure 6.55: Chip micrographs of the FDDAC-based transmitters with RF-DAC based I/Q transmit cores.

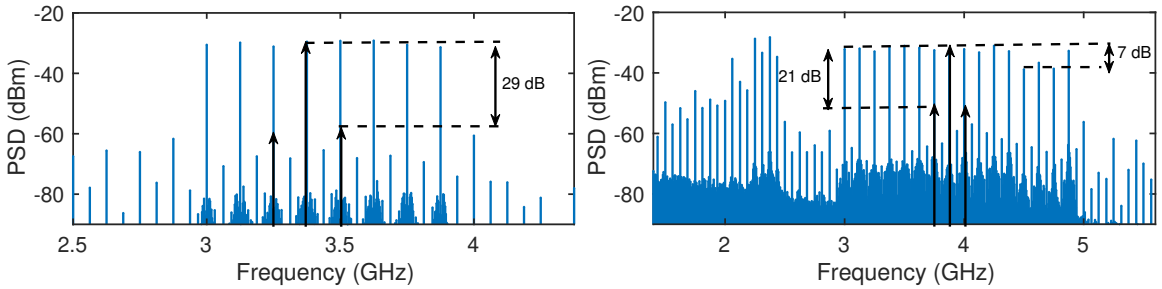


(a) DSP activated including FFT-processors. (b) Reduced DSP activity.

Figure 6.56: Measured phase noise performance of the frequency synthesisers over the bin frequencies evaluated at various offset frequencies [82].

Fig. 6.55 shows the chip micrographs of the *FDDAC_TX1* and the *FDDAC_TX1.5*. The chip area and the floor plan remains unchanged, whereas the additional area for the decoupling capacitors is released by omitting the multiplier based frequency synthesis blocks and the additional LO input which turned nonfunctional. Fig. 6.56 shows the measured phase noise of the PLLs in the bins 0-to-15 evaluated at different offset frequencies. Prior to the measurement, the system is locked and the synchronisation blocks are stopped. Fig. 6.56a depicts the results with active DSP as it is required

for the FDDAC-based transmitter. The redesigned frequency synthesis block provides a phase noise performance that matches the initial estimation which was based on the simulation results presented in [82], even with the active DSP. Fig. 6.56b shows the measured phase noise performance with reduced DSP activity. The digital noise coupled to the reference signal and injected into the substrate as well as the complete system increases the phase noise. Nonetheless, the digital noise from the DSP effects the phase noise outside the filter bandwidth of the PLLs which could not be eliminated due to the floor plan restrictions. Moreover, the synchronisation blocks have been redesigned for improved performance as well. Furthermore, the DSP provides control bits which are used to freeze the state of the counter inside the synchronisation blocks. Thus, its effect on the phase noise due to the expected back-and-forth behaviour can be minimised by stopping its activity once the system is fully synchronised.



(a) Bins: 0-to-7. (b) Bins: 0-to-15, over large span.

Figure 6.57: Measured PSD of the phasor tones in *all_dac_set_max* mode.

Fig. 6.57 shows the measured PSD in the *all_dac_set_max* mode. The redesign reduces the power of the in-band spurious tones. In the HBM, utilising the lowest 8 bins, an in-band SFDR of 29 dB is achieved. On contrary, the in-band SFDR reduces to 21 dB in the FBM. Even though a certain number of frequency synthesisers, especially in the low-frequencies, perform as expected, activating all phasor tones for the FBM leads to a performance drop. Moreover, the phasor tones at high frequencies exhibit an amplitude deviation of up to 7 dB when all 16 phasor tones are activated simultaneously. The power of the spurious tones at half the desired frequencies is 20 dB less than the actual phasor tones considering the lowest 8 frequencies. Nonetheless, the power of the spurs increases for higher phasor tone frequencies. Consequently, the *FDDAC_TX1.5* is measured without highpass filtering the output.

The performance of the output power equalisation is measured for different output frequency ranges as shown in Fig. 6.58. In the HBM, two frequency ranges are characterised, *i.e.* bins 0-to-7 and bins 4-to-11. This method allows to fully equalise the power levels of the modulated band in the HBM and in the FBM. However, the measured power decay for increasing frequencies is higher than simulated. Thus, the amplitude equalisation must be used with slightly higher bias current differences, ΔI_{bias}, than simulated which is within the considered headroom margin. The in-band

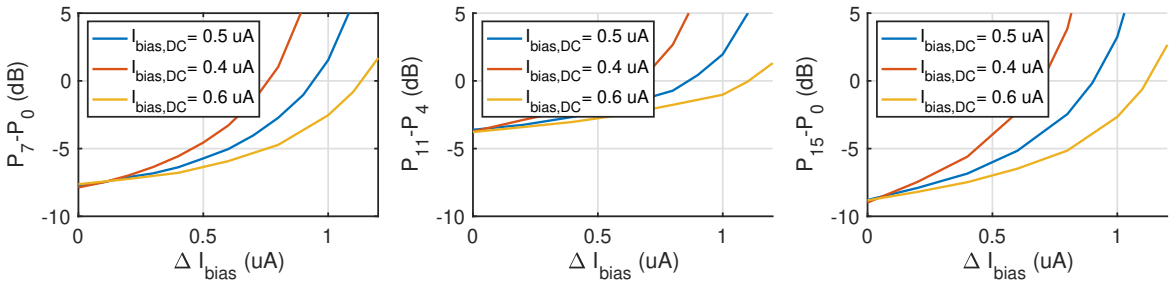


Figure 6.58: Measured characteristic of the linear equalisation.

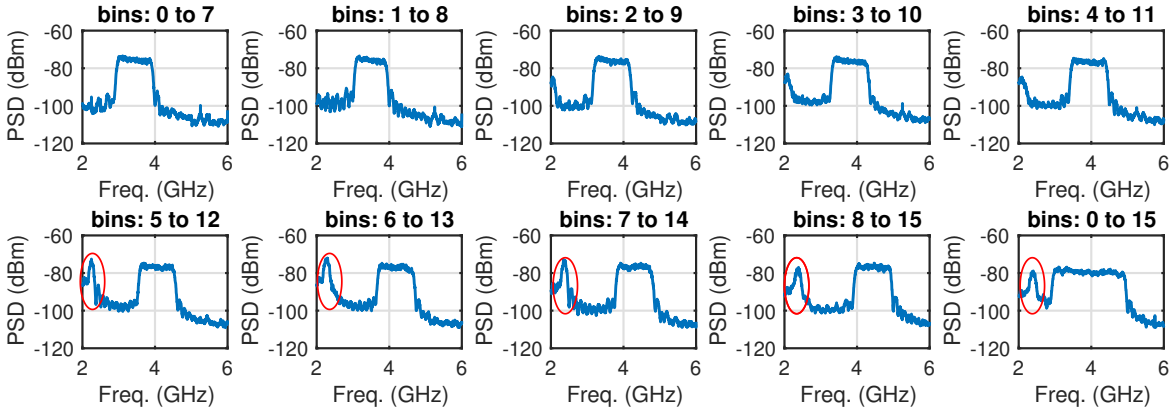
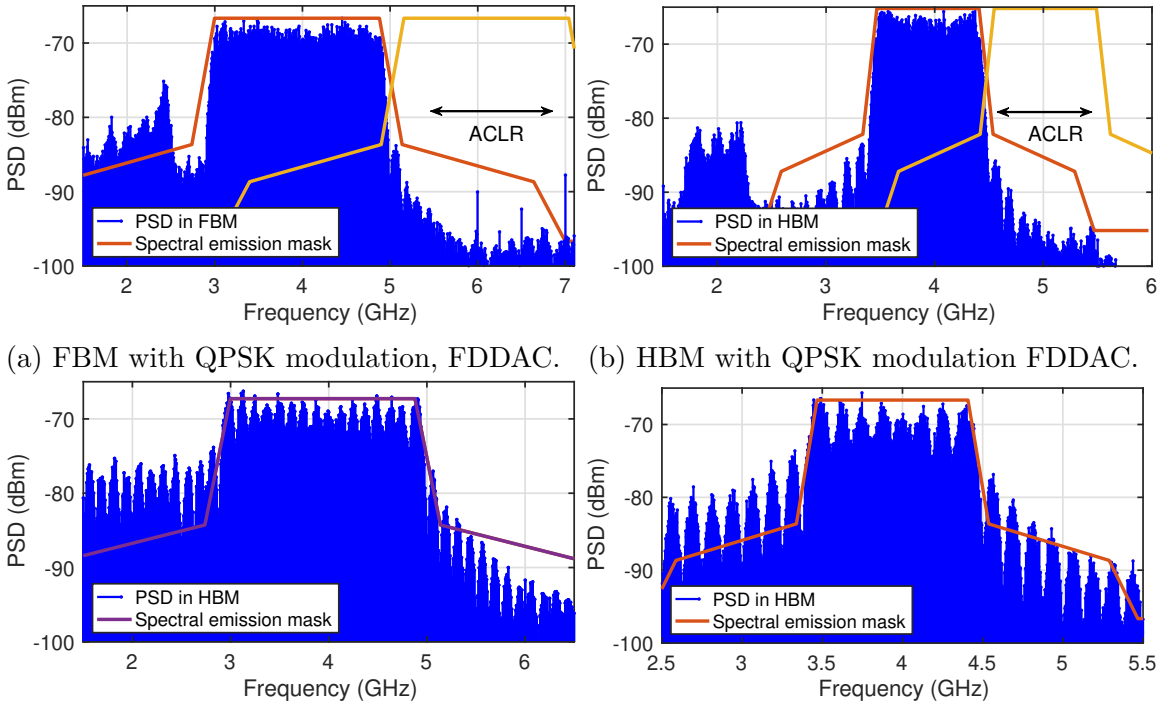


Figure 6.59: Measured output spectra in the HBM and the FBM.

amplitude deviation that originates from the frequency synthesis block cannot be corrected by the linear equalisation slope.
Fig. 6.59 shows the PSD of the modulated FDDAC output for varying frequency ranges and bandwidths. The spurs of the phasor tones at half the frequency leads to out-of-band emissions at low frequencies. The WiGig *IEEE Std. 802.11ad* mentioned in Chapter 2 offers a single-carrier modulation scheme with a bandwidth of 1.86 GHz per channel. Fig. 6.60a shows the measured PSD in the FBM for 2 GHz modulation bandwidth including the spectral mask of the WiGig standard as stated in [5]. The obtained results demonstrate the spectral shaping capabilities of the FDDAC-based transmitter which fulfills the requirements in the close proximity of the transmit channel. Note that the modulation bandwidth is approximately 13.7%-wider than stated in the standard which leads to an improved spectral efficiency. In the FBM, the spectral mask is only violated by spurs originating from the frequency synthesis blocks. In the HBM, as shown in Fig. 6.60b, the spectral mask is constricted by a factor of two due to the narrower modulation bandwidth. The reduced DFT-length of 8 provides a relatively less distinct spectral shaping. However, it fully satisfies the constricted emission mask as estimated in Chapter 3. Fig. 6.60c and 6.60d depict the PSD for random modulation at the same sampling rate on each I/Q transmit core rather than



(a) FBM with QPSK modulation, FDDAC.

(b) HBM with QPSK modulation FDDAC.

(c) FBM with random modulation.

(d) HBM with random modulation.

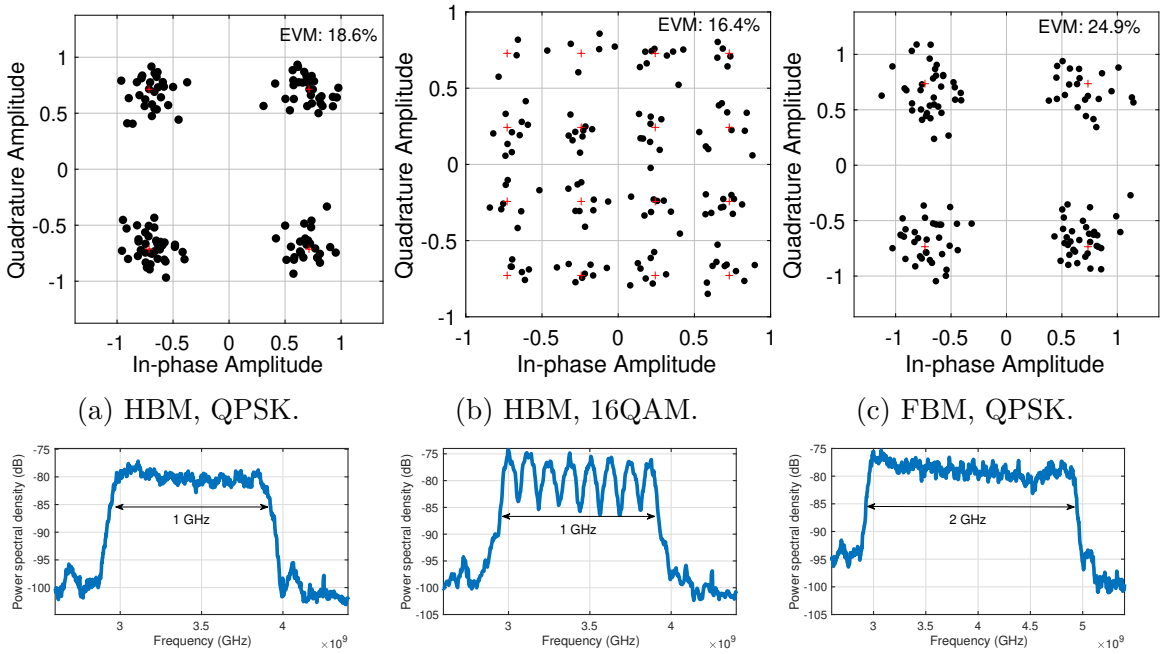
Figure 6.60: Measured PSD in the FBM and HBM including the spectral emission mask of WiGig *IEEE Std. 802.11ad* [5] and its constricted version.

applying the correct FDDAC related DSP. The measured spectra is the superposition of multiple sample-and-hold transfer functions. This exemplifies the spectral shaping performance of the presented technique without increasing the sampling rate. Table 6.6 lists the in-band RMS signal power, P_{rms}, as well as the ACLR for certain modulation schemes based on the presented WiGig spectral mask. The ACLR is evaluated for an adjacent channel with an identical bandwidth placed at the right side of the actual band. The measured ACLR is partially limited by spurious tones. The table presents the results for the FDDAC-operation and random modulation on the I/Q transmit cores. The measured and deembedded RMS output power is−24 dBm and −22 dBm in the HBM and FBM which perfectly matches the simulation results. The measurements are carried out in the sign processing mode 0 which sets both data bits to zero if the RF-DAC cells is deactivated. Thereby, the power consumption is reduced at the cost of the variable output biasing current. However, this leads to slightly increased spurious tones at the sampling frequency of the RF-DAC and its multiples, *i.e.* 250 MHz, 500 MHz *etc.* Additionally, the obtained output power is approximately 0.4 dB higher which is negligible.

Fig. 6.61 illustrates the measured constellation diagrams and the appropriate spectra for different modulation types and bandwidths. The best measured EVM is achieved in the

		P_{rms} (dBm)	FDDAC ACLR (dB)	Random ACLR (dB)
HBM 0-7	QPSK	-25.2	-28.55	-19.21
	16QAM	-24.36	-28.76	-21.02
HBM 4-11	QPSK	-24.58	-28.57	-18.73
	16QAM	-23.62	-28.94	-20.84
FBM	QPSK	-22	-28.34	-22.6
	16QAM	-21.14	-28.8	-24.8

Table 6.6: Measured RMS signal power within the modulation band, ACLR calculated based on the spectral mask shown in Fig. 6.60.



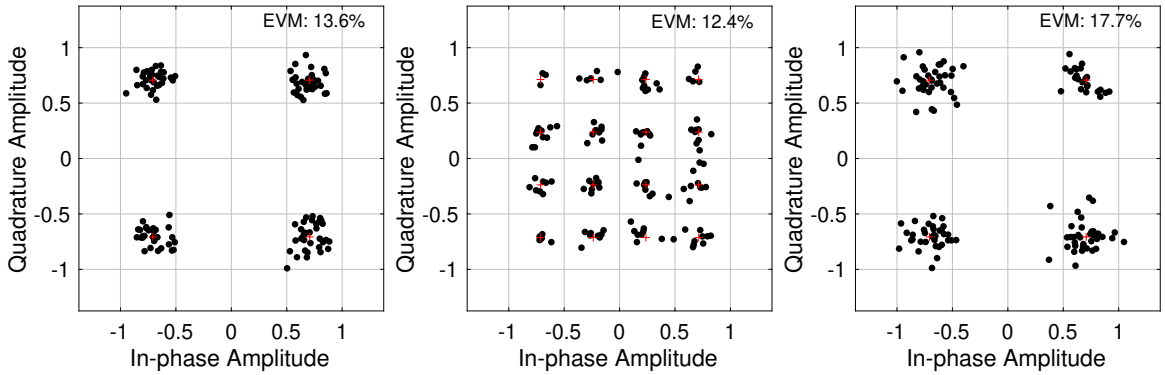
(a) HBM, QPSK. (b) HBM, 16QAM. (c) FBM, QPSK.

(d) PSD of HBM utilised over bins 0-to-7. (e) PSD of HBM utilised over bins 0-to-7. (f) PSD of FBM utilised over bins 0-to-15.

Figure 6.61: Meas. constellation diagram and PSD of the FDDAC-based transmitter.

HBM for the modulation order 16QAM. It is 16.4%, whereas the simulated estimation was 10.9%. The 1 GHz modulation bandwidth utilises the bins 0-to-7. Thus, the modulated band is between 2.9375 GHz and 3.9375 GHz which can be shifted to higher frequencies by discrete steps of the phasor tone spacing as shown in Fig. 6.59. The PSD of the 16QAM signal exhibits a nonflat behaviour which is caused due to a minor error in the appropriate modulator within the DSP. It does not generate perfectly random symbols which leads to a nonuniform power distribution. The improved frequency synthesis block is able to generate all 16 phasor tones simultaneously. Thus, the FBM with up to 2 GHz modulation bandwidth is demonstrated successfully. Fig. 6.61c shows

the measured constellation diagram of a QPSK modulated coherent signal with a data rate of 4 Gbit/s. The measured EVM is 24.5%. Fig. 6.61f shows the corresponding PSD. It exhibits an amplitude deviation towards the end of the bandwidth which could not be corrected with the on-chip linear equalisation method. The observed EVM performance discrepancy is mainly caused by constant errors such as the SFDR limitations and I/Q imbalance of the generated phasor tones. Fig. 6.62 shows the equalised constellation diagrams. The equaliser is based on a 21-tap FIR filter which is trained with an initial sequence. Therefore, the varying I/Q imbalances of the phasor tones as well as any amplitude decay is corrected which leads to the shown performance. With equalisation, the measured results match well with the simulated estimation. In the HBM, an EVM of 12.4 % can be achieved. Moreover, a significant improvement can be denoted in the FBM where the EVM is improved to 17.7%.



(a) HBM, QPSK. (b) HBM, 16QAM. (c) FBM, QPSK.

Figure 6.62: Measured constellation diagrams of *FDDAC_TX1.5* after equalisation.

Fig. 6.63 shows the captured EVM performance of the *FDDAC_TX1.5* for different modulation types and frequency ranges in the HBM. The DSP utilises a different set of I/Q transmit cores in order to shift the frequency. Apparently, the EVM deteriorates with increasing frequency due to the descending phasor tone performance such as the increased I/Q imbalance, reduced SFDR, and timing misalignments.

6.8 Discussion

The enhancements in the supply domains and the improved frequency synthesis blocks significantly increased the performance of the complete transmitter. The measured results match well with the simulations. The RF-DAC-based I/Q transmit cores employed in the FDDAC approach are fully suitable and achieve competitive results. The transmitter is able to generate a coherent modulation bandwidth of up

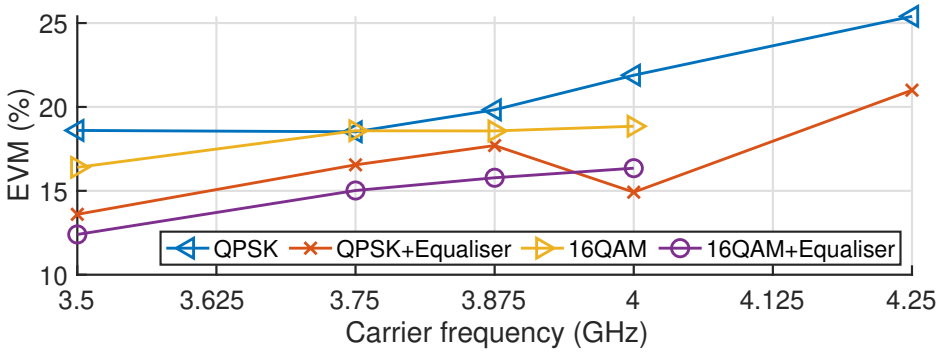
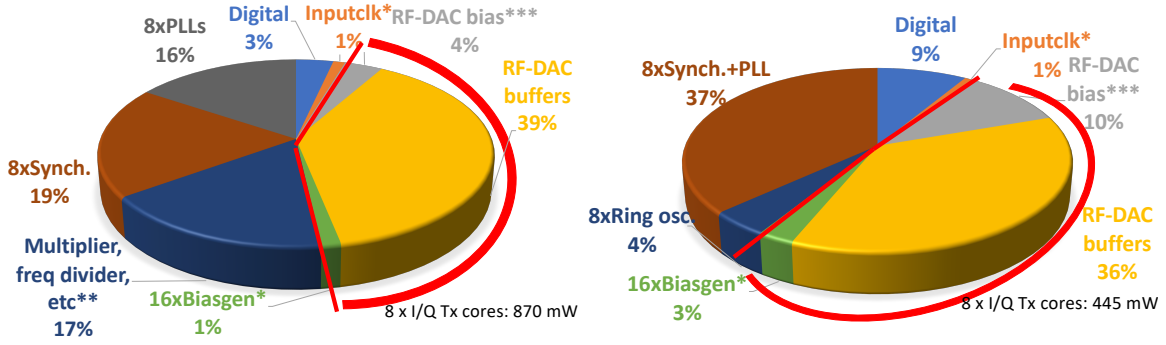


Figure 6.63: Measured EVM in the HBM over different carrier frequencies for QPSK and 16QAM with and without equaliser.



(a) *FDDAC_TX1*, P_{total} : 1996 mW. (b) *FDDAC_TX1.5*, P_{total} : 882 mW.

Figure 6.64: Power consumption break down of the FDDAC-based ICs in the HBM. *:Estimation, **:Uncontrollable due to voltage instability, ***:SPM=0.

to 2 GHz. The measured spectra in the HBM and FBM demonstrate the spectral shaping capabilities of the FDDAC-based transmitter approach. They fulfill the requirements for the single-carrier mode in the *WiGig* standard even though the implemented transmitter supports a 14 % wider modulation bandwidth than stated in the specification. Moreover, the implementation allows a programmable output frequency which can be changed in discrete steps. However, the complete system is still bottlenecked by the frequency synthesis blocks. This especially becomes clear when the equalisation is introduced which is able to correct the I/Q imbalance of the phasor tones. Furthermore, the in-band SFDR is limited by spurious tones. On contrary, the presented implementation successfully demonstrates that the multiple ring-oscillator-based PLLs can be integrated on the same IC with good phase noise performance. The encountered bottlenecks such as the I/Q imbalance, duty cycle mismatch which leads to amplitude variations, and synchronisation missalignments can be controlled by introducing additional blocks.
The RF-DAC based I/Q transmit cores process the previously aligned LO and Fourier

coefficients in a single block. Thus, no additional timing mismatch is added to the signals. However, the price is paid in the power consumption since the phasor tones are buffered for a large number of RF-DAC cells. Several methods are presented in order to reduce the number of the utilised RF-DAC cells which decreases the power consumption. Fig. 6.64 compares the power budget break down of the first two integrated FDDAC-based transmitters in the HBM. The *FDDAC_TX1* requires relatively high supply voltages in order to operate the frequency synthesis blocks which is caused by the unstable on-chip supply voltage. The overall power consumption is nearly 2 W in the HBM, whereas the I/Q transmit cores use 870 mW. In the first design iteration, the total power consumption is reduced by a factor of two, *i.e.* to 882 mW. This is achieved by the improved frequency synthesis block which operates at the nominal voltage [82]. Furthermore, the reduced phasor tone frequencies and improved rise and fall times decrease the power consumption of the I/Q transmit cores by nearly factor two, *i.e.* to 445 mW. However, the LO-buffering preserves a large portion in the power break down in both chips. The total power consumption in the FBM increases to 1720 mW, whereas the I/Q transmit cores contribute with a power consumption of 768 mW.

6.9 Conclusion

The first integrated FDDAC prototype successfully demonstrates the capabilities of the analogue inverse Fourier-transform-based data conversion employed in a transmitter. Conventional transmitter architectures often operate at the edge of the technological limitations in order to satisfy the specifications of today's communication standards. The proposed architecture delivers competitive performance while operating at much lower sampling rates which relaxes the constraints on both the DSP and the analogue-mixed-signal blocks. This allows the cointegration of the complete DSP for a data rate of up to 8 Gbit/s onto the same IC as the I/Q transmit cores as well as the frequency synthesis blocks. The flexible design integrates a programmable modulation bandwidth of 1 GHz or 2 GHz with various modulation schemes in the sub-6 GHz frequency range. It can be shifted in discrete steps by utilising a different set of I/Q transmit cores. In the first design iteration, the performance of the transmitter is significantly improved which allows doubling of the measured data rate. Moreover, the power consumption is reduced by a factor of two. The measured transmitter specifications match well with the system simulations and estimations. Additionally, the first prototypes demonstrate the spectral shaping capabilities for a very large modulation bandwidth. However, the power consumption of the I/Q transmit cores can be further improved by adopting individual DACs and mixers rather than RF-DACs which require a large portion of the power budget for the LO-buffering.

Chapter 7

High data rate FDDAC-based transmitter up to 12 Gbit/s

The first prototypes of the integrated FDDAC-based transmitter showcase the competitive performance of the new digital-to-analogue conversion technique while requiring a fractional of the sampling rate compared to conventional transmitters. This chapter builds on the experience gained on the integrated design of the FDDAC-based transmitters and targets to lower the power consumption while improving the transmitter performance. The I/Q transmit cores in the RF-DAC based structure contribute a significant amount to the overall power consumption. This chapter introduces a new implementation of the I/Q transmit cores based on extremely power efficient 9-bit I/Q DACs combined with I/Q mixers and output amplifier buffers. Thereby, the power consumption is further minimized and the targeted data rate is increased to 12 Gbit/s. Additionally, a conventional transmit mode is integrated which allows the utilisation of each I/Q transmit core as a stand alone transmitter. Consequently, the proposed IC demonstrates a true multistandard transmitter.

7.1 Design and analysis of the integrated FDDAC-based transmitter

The RF-DAC combines several building blocks of the I/Q transmitter chain into a single component. This allows inherent timing of the phasor tones and the Fourier coefficients. However, the phasor tones at frequencies above 3 GHz need to be buffered and routed to all cells which reserve a big portion of the power budget. The third implemented IC follows the tick-tock design strategy where the frequency synthesis blocks from *FDDAC_TX1_5* have received only a minor update, whereas the I/Q transmitters, DSP-block, system design as well as the overall floor plan have received a major revision. Table 7.1 presents the specifications and the assumptions for the subblocks. Based on the measured results discussed in Chapter 6, the estimated phase noise performance is significantly improved. Furthermore, the timing offset, $\tau_{offset,const.}$, is estimated to be larger due to the architectural change.

DAC resolution	$\sigma_{DAC,FS}$	DAC slope	$\sigma_{\phi(f)}$	σ_τ	$\tau_{offset,const.}$
9 bit	<1 %	<1 %	<2°	<1 ps	<10 ps

phase noise @ 1 MHz	SFDR phasor tones	const. I/Q err.	I/Q MM
>−100 dBc	>35 dB	<1°	<2°

Table 7.1: Subblock specifications and assumptions for the *FDDAC_TX2*.

7.1.1 Floor plan of the *FDDAC_TX2*

Fig. 7.1 shows the updated floor plan. The complete block which measures 1.9x1.9 mm^2 is occupied by the transmitter. This allows bondwire access to all 4 edges. Furthermore, the output of the transmitter is bonded via the QFN48 package. The I/Q transmit cores are implemented by 9-bit I/Q DACs, passive mixers, and output amplifier buffers. Integrated inductors are used to bias the output of the amplifier buffers which omits the use of external bias-tees. The supply voltage of the I/Q transmit cores as well as the output biasing point are stabilised by large and high density capacitor banks. The digital block integrates additional functionalities which leads to an increased size. Furthermore, the position of the input clock processing is changed such that the reference clocks are not routed over the DSP. Additional high density capacitor banks are placed between the digital block and the frequency synthesizers to stabilise the supply voltage of the frequency synthesis blocks. The MOS capacitors close to the

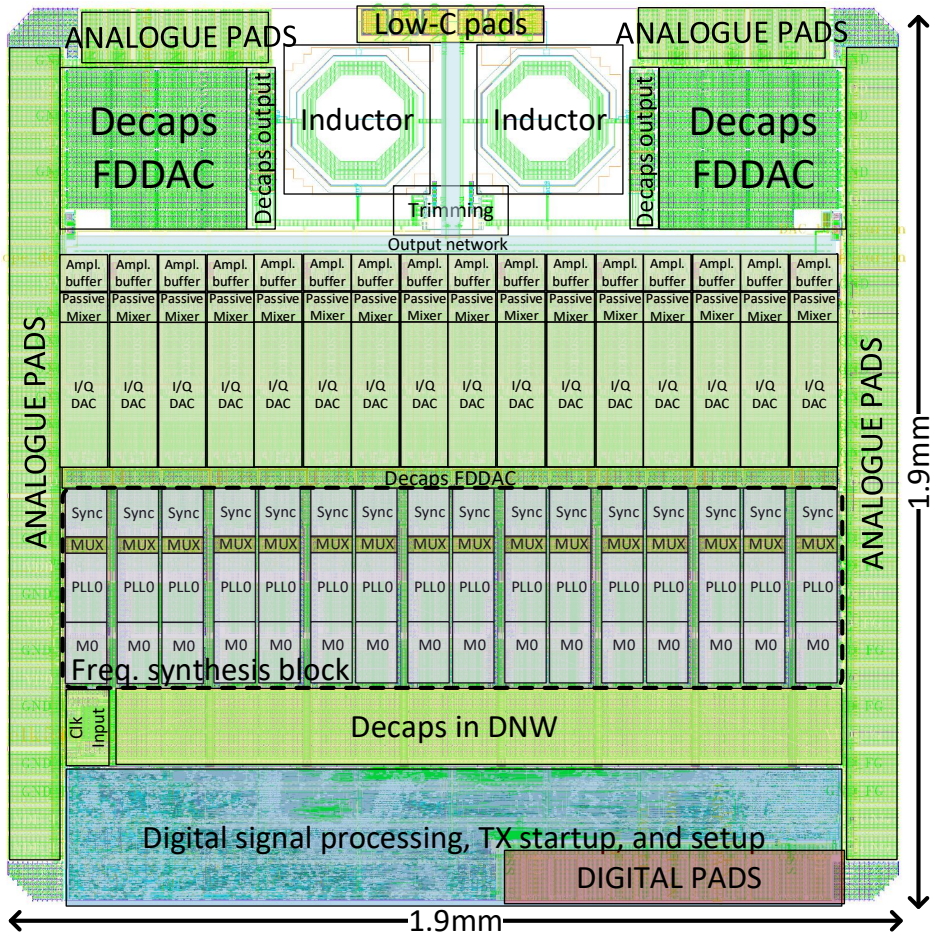


Figure 7.1: Floor plan and top-level layout of the *FDDAC_TX2*.

digital block are placed in Deep N-Well (DNW) in order to improve the substrate isolation from noise injected by the digital block. Additionally, the placing of the capacitors is planned to increase the distance between the PLLs and the digital block.

7.1.2 Integrated digital signal processing

The updated DSP block extends the functionalities implemented in the previous design as presented in Chapter 6. The quantisation length of the I/Q transmitters is increased to 9 bits. Furthermore, the modulation order of 64QAM is added to the system which leads to a maximum data rate of 12 Gbit/s. The number of simultaneously operating PRBS generators is increased to generate the additional bits for the higher modulation order. Thus, the scaling of the I/Q modulators and the windowing is

adapted. Additionally, the FFT blocks are redesigned to support an input and output word-length of 11 bits. Thereby, the accuracy of the DSP internal calculations is increased. However, the output is then truncated to 9 bits. The arithmetic operations of the previous DSP have been performed without overflow handling. The second version of the DSP introduces overflow handling. If the addition of two numbers is larger than the representable maximum which generates a carry-bit at the MSB, the sum is replaced by the highest representable number. Thereby, the DSP calculation accuracy is maximised. Moreover, the frequency of the digital sinusoidal tone which is used to characterise the I/Q transmit cores is programmable.
The complete FDDAC transmitter consists of 16 individual I/Q transmit cores that can be operated as conventional transmitters. The second version of the DSP includes the complete baseband processing for a conventional transmitter which supports a modulation order of up to 16QAM. The baseband signal is generated by the same PRBS generators oversampled and sent to the integrated 64-tap complex-RRC filters. The sampling speed of the digital block is unchanged and, hence, the integrated FIR filters operate at a maximum frequency of 250 MHz. The modulation bandwidth in the conventional mode is 31.25 MHz considering an OSR of 8. The maximum data rate in this mode is 125 Mbits. The baseband signal processing for the conventional mode is implemented once, whereas the modulated signal can be fed to selected I/Q transmit cores. Furthermore, the DSP controls the blocks implemented in the transmitter system. Therefore, additional commands and control bits are added.

7.1.2.1 Physical implementation and back annotated simulations

The size of the digital block has increased from 0.22 mm^2 to 0.38 mm^2. The main contributors are the included FIR filters for the conventional mode and the increased word-lengths of the FFT processors. The word-length increase requires adders and multipliers which are optimised for speed, regardless the larger area consumption. The synthesis, place, and route optimisation steps are performed with similar constraints with regard to the resampling at the input of the DACs. After place and route, the implemented DSP block is analysed with the back annotated delays introduced by the gates and the routing. It fulfils the constraints and without any timing violations.

7.1.3 Clock input and reference signal distribution

Fig. 7.2 shows the layout of the input clock processing block. It is placed in a DNW structure since the digital block is in close proximity. The used subblocks are kept, although the floor plan is changed such that the output is not routed over the digital

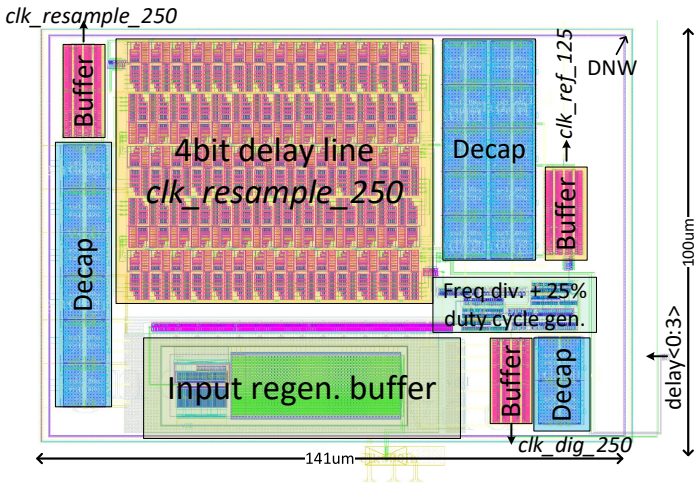


Figure 7.2: Layout of the input clock processing block.

block. The supply is shared with the frequency synthesizer blocks and is supported by more than 1.5 nF on-chip decoupling capacitors. The capacitor banks are based on a combination of MOS and custom designed MOM metal structures maximising the capacitance density to 107 nF/mm^2. However, additional 18 MOS capacitors with a total capacitance of 24 pF are placed around the buffers and delay line. The generated *clk_resample_*250 is routed by a tree routing structure since large metal widths and thick top-metals could not be used due to the high density of the design.

7.2 Low power I/Q transmit core design

The I/Q transmit cores are redesigned with regard to reduce the power consumption while increasing the transmitter performance. Fig. 7.3 shows the block diagram of the I/Q transmit core. In contrast to the RF-DAC based implementation, inherent synchronous operation is not granted by the system. However, the system simulations show that the synchronisation of the phasor tones among each other effects the system performance significantly more than any offset between the aligned coefficients and aligned phasor tones. The offset timing error, τ_{offset}, might be slightly larger when the I/Q transmit core is based on individual DACs, mixers, and output amplifier buffers. On the other hand, the implementation of the transmit chain based on individual building blocks has the advantage that each block can be optimised for certain specifications. Fig. 7.4 illustrates the layout of one I/Q transmit core. The height of the block is limited to approximately 100 um since it will be placed 16 times. The DACs provide 9 bit quantisation length and are optimised for linearity, matching,

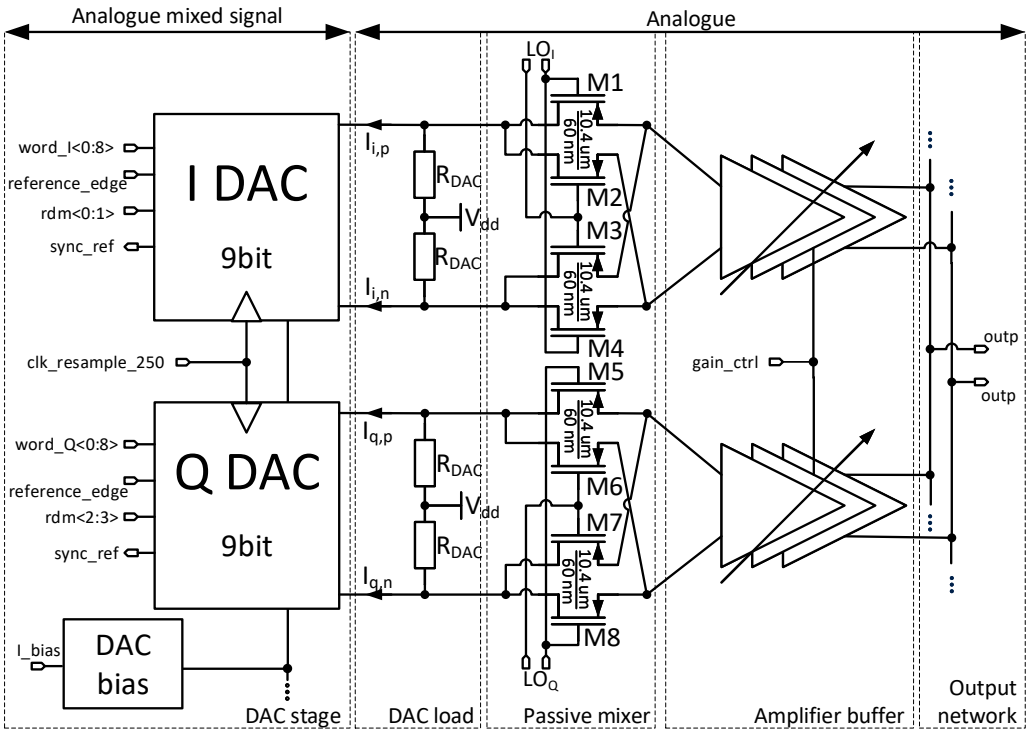


Figure 7.3: Block diagram of the redesigned I/Q transmit chains including I/Q DACs, passive mixers, and tunable gain output amplifier buffers.

and low power consumption. The output of the DACs are used in an internal node eliminating the linearity restrictions originating from the summation of the 16 RF-DAC outputs. The DAC current is converted into a voltage by resistors and fed to a passive mixer optimised for linearity. Each phasor tone, $LO_{I,i}$ and $LO_{Q,i}$ is only buffered and routed to one Gilbert quad with reasonably small gate sizes. Thereby, a large portion of the power budged consumed by the RF-DACs LO-buffers can be omitted. The output amplifier buffers generate a considerably higher output power and are optimised to drive into the same node without modulating each other. In order to correct linear amplitude deviation at the output of the amplifiers over the frequency, the analogue gain tuning by the signal, *gain_ctrl*, is implemented. Additionally, the output biasing of those amplifier buffers is provided by on-chip inductors which eliminate the necessity of external bias-tees.

7.2.1 9-bit I/Q DAC design

Fig. 7.5 illustrates the block diagram of the current-steering DAC. It is based on pseudounary cells. The switching scheme is fully differential, as shown in Table 6.4, and

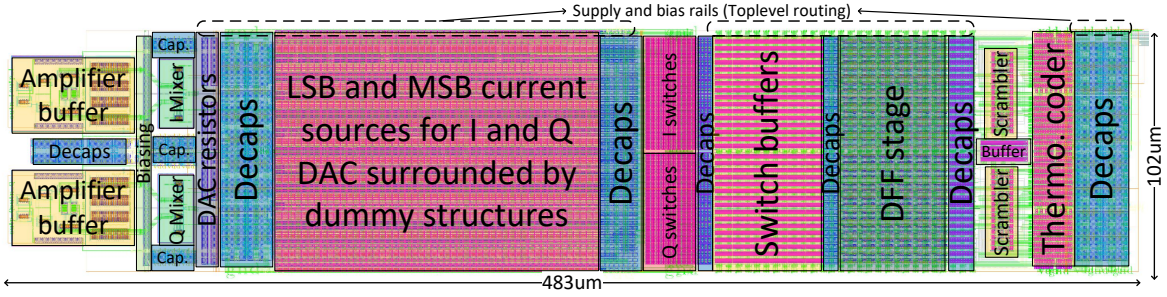


Figure 7.4: Layout of the complete redesigned I/Q transmit chain.

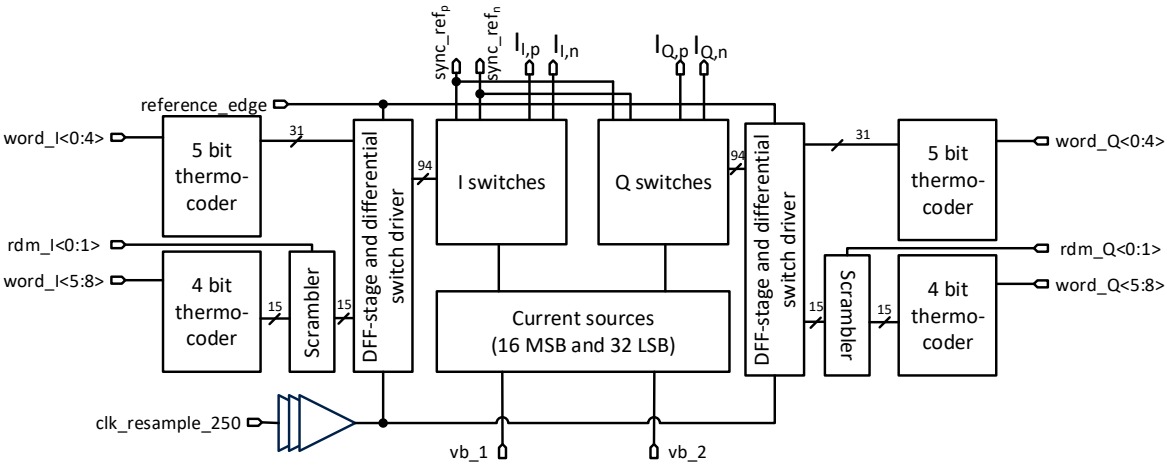
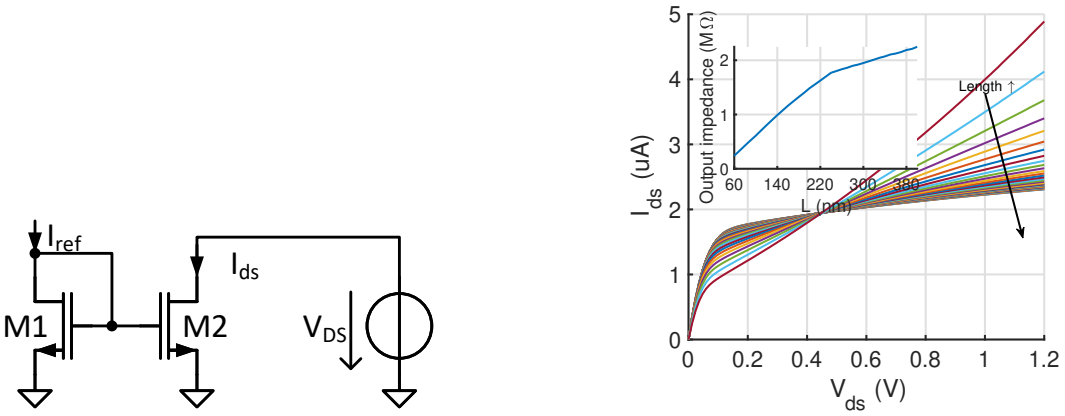


Figure 7.5: Simplified block diagram of the 9 bit I/Q DAC including the thermo-coder and DEM, and DFF-stage.

discussed in Section 6.5. In total, 15 MSB and 31 LSB current sources are implemented. Fig. 7.4 shows the detailed layout of the DAC. Thermometer coder are implemented to individually address 31 LSB and 15 MSB switches. The 5 LSB bits of the input word are fed to a 5-bit thermometer coder and the remaining 4 MSB are fed to a 4-bit thermometer coding block. The latter is fed through a scrambler stage introducing dynamic element selection which improves the linearity of the DAC considering the mismatch of the current sources. The processed input word is resampled by the DFF stage which is triggered by the clock signal *clk_resample_*250. Each I/Q DAC utilises a central buffer to amplify the resampling clock for all DFFs. The differential outputs of the DFF-stage are fed to the switch buffers and the actual switching stage which steers the current depending on the input data to the positive or negative output. Furthermore, the analogue and digitally switching components are separated in layout. The outputs of the current sources are routed to the switches which are placed close to the switch buffers. The output of the switches consequently is routed back over the current source bank to the resistive stage which performs the current-to-voltage



(a) Simple CMOS current mirror. (b) Sim. output current and impedance.

Figure 7.6: Schematic of a simple current source and simulated output characteristics.

conversion. The top-level supply and bias routing is included in the layout of the bins which allows the simulation of the entire supply mesh by only extracting one bin. The voltage stability is ensured by locally distributed decoupling capacitors that are placed at the intersects of the subblocks.

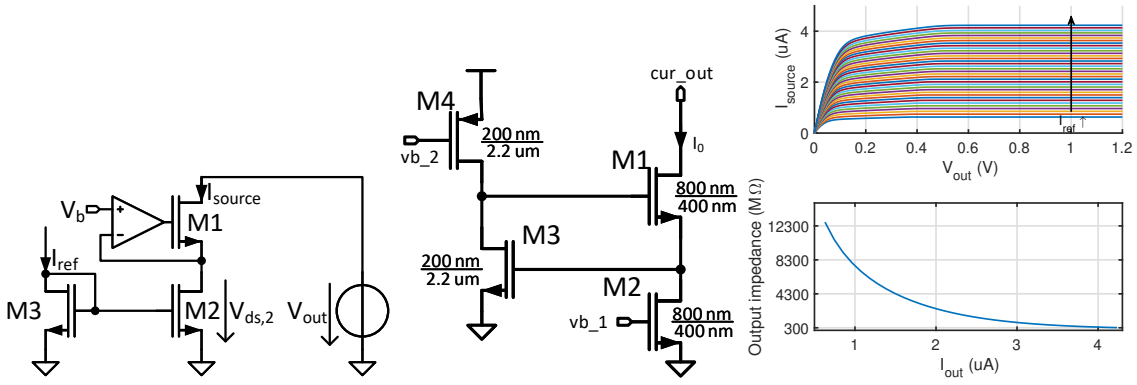
7.2.1.1 Current source design

A current-steering DAC generates a certain output current based on the applied digital word. The output current is fed to a resistive stage which generates a voltage swing. The linearity, as in the case of the RF-DAC, depends on the output impedance of the current sources. A current source ideally provides an infinite output impedance which leads to a constant current over varying output voltages. In CMOS, a current source is usually implemented by a current mirror which is biased by a reference current that is copied to one or multiple current sources. The copied currents can be adjusted by changing the W/L ratios of the reference transistor and the current source transistor. A simple CMOS current mirror can be implemented by two transistors as shown in Fig. 7.6a. M2 acts as a current source for output voltages above the saturation voltage $V_{ds,sat}$. Modern planar CMOS processes which scale down the channel-length of the transistors suffer from channel-length modulation. It can be described by λ which leads to a dependency of the drain current based on the output voltage, V_{ds}, even though the transistor is in the saturation region:

$$I_D = K'(V_{gs} - V_{th}(1 + \lambda V_{ds})). \tag{7.1}$$

Fig. 7.6b shows the simulated output current over V_{ds} and different gate lengths. Increasing the length of the transistor increases the output impedance by reducing the channel-length modulation. The advantage of the simple current mirror is its large output voltage swing which is required to be above $V_{ds,sat}$. There are several approaches to increase the output impedance of CMOS current sources such as cascode or Wilson current mirrors. The trade-off basically is between the usable output voltage swing versus the achievable output impedance and the power consumption as well as the complexity. Fig. 7.7a shows the current mirrors utilised in the I/Q DACs. It is a cascode current source which includes an active feedback to regulate the voltage across M2. In literature, this topology is also referred to as enhanced current mirror [99]. The feedback amplifier senses the voltage, $V_{ds,2}$ and controls the gate voltage of M1. This topology requires an additional bias voltage, V_b, and the feedback amplifier. Nevertheless, the feedback can be implemented by a single transistor. Fig. 7.7b shows the schematic of the current source with the appropriate transistor sizing implemented as the LSB current source within the DAC. The transistor, M3, acts as the feedback amplifier. The output impedance depends on the gain, A, of the feedback amplifier and can be expressed as follows:

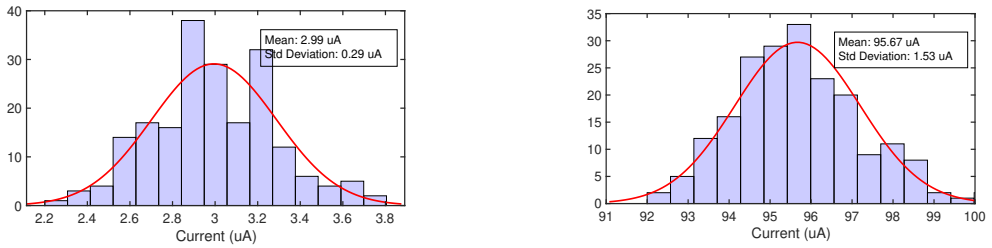
$$R_{out} = g_{m,1} r_{ds,1} r_{ds,2} (1 + A). \tag{7.2}$$



(a) Enhanced current mirror. (b) Schematic. (c) Simulation results.

Figure 7.7: Enhanced current mirror, schematic implementation, and simulation results.

Fig. 7.7c shows the simulated output current versus the output voltage for various output current levels. With increasing output current, the simulated output impedance reduces. The LSB current source is designed to provide approximately 3 uA. At the targeted current level, the output impedance is slightly below 1 GΩ which is approximately 500 times higher than the simple current mirror. The output swing of the enhanced current mirror is limited by $V_{out} < V_{th} + 2V_{ds,sat}$ which in this case



(a) LSB current source. (b) MSB current source.

Figure 7.8: Simulated LSB and MSB current sampled over process variations.

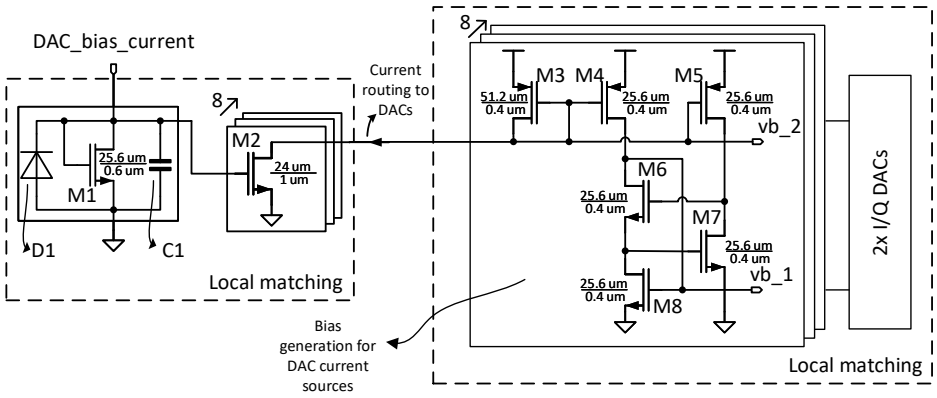
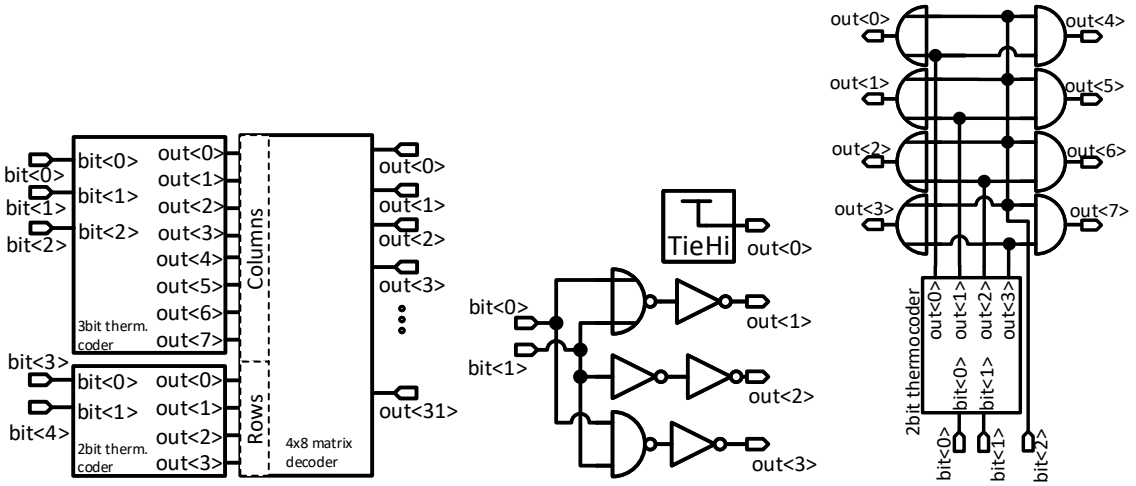


Figure 7.9: Biasing circuit for 16 I/Q DACs placed across the entice chip.

corresponds to V_{out} <0.7 V. Consequently, the differential DAC output swing is limited to be between 0.7 V and 1.2 V which, in turn, leads to the differential DAC full swing of 1 V peak-to-peak. In order to increase the DACs full-scale peak-to-peak voltage, wideswing enhanced current sources can be used which reduce the minimum output voltage to $V_{out} < 2V_{ds,sat}$. However, the wideswing enhanced current source requires an additional branch increasing the power consumption and the circuit complexity. Note that the LSB current cells are implemented 511 times in each I and Q DAC.
The length of the transistors M4 and M3 are selected to be large to reduce the biasing current in the feedback amplifier branch. Additionally, the current source transistors, M1 and M2, are sized fairly large to improve the transistor matching. Fig. 7.8 shows the simulated output current of the LSB and MSB sources sampled over mismatch. The MSB current source consists of 32 parallel LSB cells. The standard deviation of the LSB current is 10 % of its absolute current value. The standard deviation of the MSB current sources is nearly 50 % of one LSB current. The 16 I/Q DACs are placed across the chip as shown in Fig. 7.1. Fig. 7.9 shows the block diagram of the DAC biasing circuit. The *DAC_bias_current* is supplied from an external source over the QFN package. In addition to the ESD protection circuits included in the pads from the technology, the ESD diode, D1, is used. The capacitor, C1, shall stabilise the



(a) Block diagram of the 5 bit thermometer coder.

(b) Schematic of 2 bit thermometer coder.

(c) Schematic of the 3 bit thermometer coder.

Figure 7.10: Block diagrams of the implemented thermometer coders.

node versus the on-chip GND. The reference current is copied to the 8 branches in close proximity of the input pad. In order to improve matching, the current mirror is implemented by fairly large transistors and several dummy transistors are added to reduce the proximity effect. The mismatch of the copied reference currents leads to a standard deviation of the LSB currents of approximately 0.6 % of one LSB current which is negligible. The copied currents are routed to 8 large sized biasing circuits each supplying two I/Q DACs. The biasing circuits are placed close to the current mirror banks of the DACs. Thereby, local matching between reference input and the copied currents as well as the biasing circuit and the actual current sources in the DACs can be guaranteed.

7.2.1.2 Thermometer coder and dynamic element matching

The 9-bit DAC is implemented in a pseudounary manner. Thus, the 9-bit binary input needs to be translated by thermometer coders in order to individually address the 32 LSB and 16 MSB cells. Fig. 7.10a shows the block diagram of the complete thermometer coder including the 4x8 matrix decoder. The coded 4- and 8-bit outputs are fed to a row-column decoder which generates the final thermometer coded 32 bits. The 5 least significant input bits are fed to two subthermometer coders which process 2- and 3-bits to generate 4 and 8 coded bits. Fig. 7.10b shows the schematic of the 2 bit coder. The binary input value is equal to or larger than 0. Therefore, $out < 0 >$ is always logic high. It is derived from a tie-high block. The remaining output is

calculated by a simple logic-gate combination. The 3-bit subthermometer coder is based on the 2-bit coder which processes the lowest two bits. The third input bit and the output of the 2-bit thermometer coder are fed to AND and OR gates which than generate the 8 coded output bits.
Fig. 7.11 shows the schematic of the row-column decoder. The logic cells are provided with the row, column, and the previous row bits. If the row-bit is logic high, the outputs of al logic cells in a row are activated. If the actual row-bit is not logic high, then the column and previous row are evaluated. In case the previous row was active, the column bit defines the output. The remaining 4 MSB bits of the input word are fed

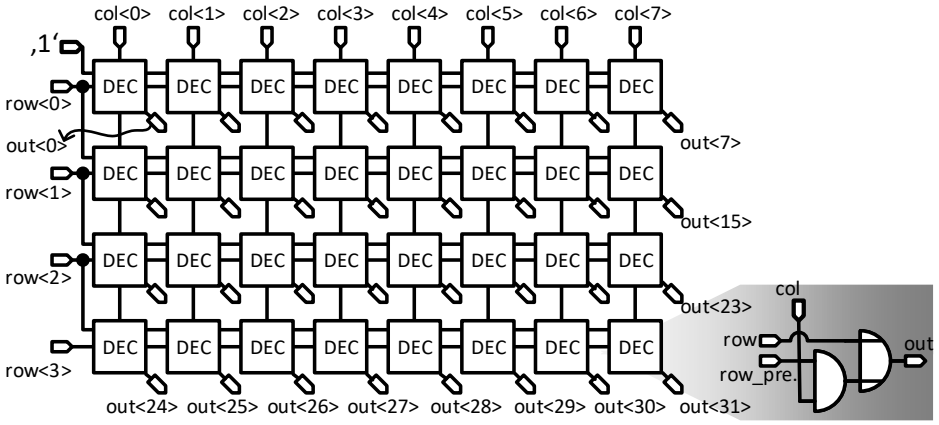


Figure 7.11: Block diagram of the 4x8 row-column decoder and the 32 thermometer coded outputs.

to a secondary 5-bit thermometer coder of which only the first 16 output bits are used. The current sources of the DAC are designed in order to reduce the mismatch effects up to a certain point. The produced DAC exhibits random mismatches distributed across the cells which leads to repeated constant errors depending on the applied word. Dynamic Element Matching (DEM) is able to average out these constant errors and reduce their word dependency [100]. The DEM can easily be implemented in a unary DAC by randomly scrambling the output of the thermometer coders. Thereby, different combinations of cells are activated for the same input word. Consequently, word dependant errors are averaged which leads to improved SFDR at the output of the DAC. On contrary, this approach increases the overall noise floor.
In this work, a pseudounary segmentation is used. The application of the scrambler on the MSB and LSB bits as well as the scrambler specifications have been analysed at system-level in order to implement the DEM with the smallest possible area and power consumption while gaining its benefits. In the system simulations, the previously simulated mismatch performance of the MSB and LSB current sources are used. The results predict that scrambling on the MSB current cells obtains better performance. Additionally, the scrambling performance in terms of the number of possible input to output mapping routes are of less importance. Consequently, a MUX-based two-stage

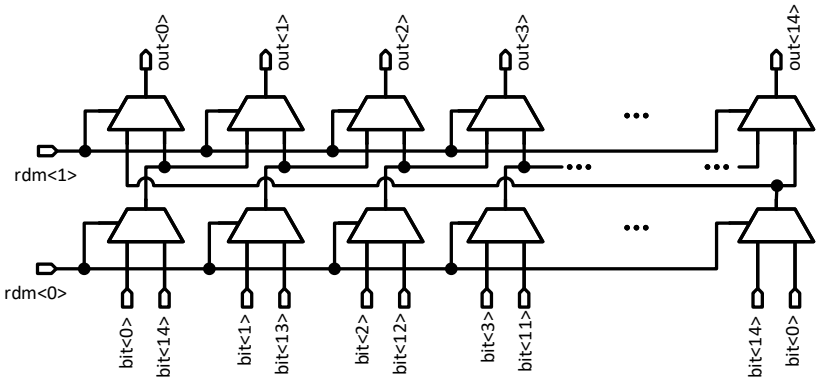


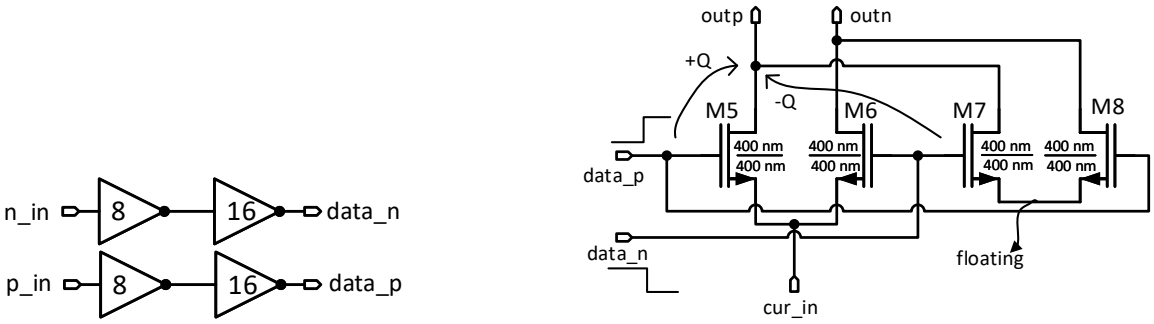
Figure 7.12: Block diagram of the MUX-based two stage scrambler.

scrambler is implemented. Its block diagram is illustrated in Fig. 7.12. Each scrambler input can be mapped to 4 different outputs depending on the random input bits which are generated in the DSP. The scrambler is based on passive MUX structures. The input is driven by the thermometer coder and the output is resampled by the DFF stage. Thus, the layout and circuit design is implemented carefully. Additionally, the complete input data processing chain which contains the thermometer coders, scramblers, and the DFF stage is simulated to operate at least at 500 MHz across all technology corners and mismatch.

7.2.1.3 DFF stage, switch buffers, and synchronisation

A total of 46 DFFs are implemented for each I and Q DAC. These are sampling 15 MSB bits and 31 LSB bits. The always-one bits are not sampled. Furthermore, the $reference\_edge$ signal from the DSP is sampled within the DFF stage. This step allows the synchronisation of the Fourier coefficients with the reference signal which is fed to the synchronisation block to align with the phasor tones. However, the Fourier coefficients at the output of the DFF-stage are routed through switch buffers and sent to the switches. The output of the switches is provided to the passive mixer. The reference signal needs to be aligned with the Fourier coefficients in the analogue domain at the input of the passive mixers. Therefore, the resampled $reference\_edge$ at the output of the DFF is fed to the same switch buffer and sent to the synchronisation blocks instead of the DAC switches.
The delay of the $clk\_resample\_250$ is set in the input clock processing block. It is routed by a tree structure to 16 I/Q DACs which leads to perfectly aligned clocks. Consequently, the delay deviation of the input buffer over mismatch is crucial since it would systematically increase the timing mismatch, σ_τ, significantly deteriorating the EVM of the transmitter. The clock buffer is implemented by fairly large transistors

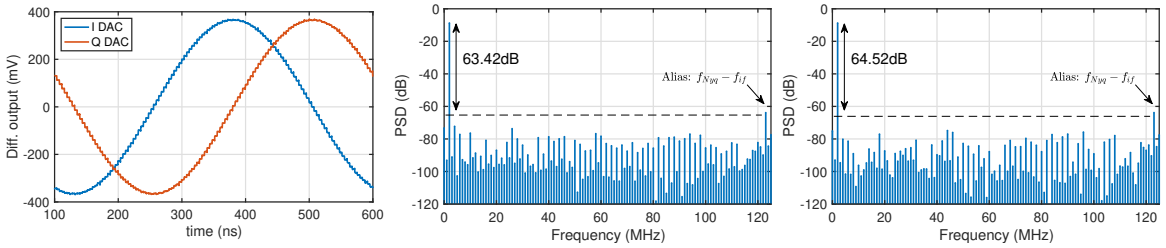
which leads to less than 0.5 ps standard deviation of the delay. The buffered resampling clock is fed to all DFFs that resample the preprocessed digital words.
Fig. 7.13a shows the switch buffers which drive the actual DAC switches. The differential data is generated by the DFF. It needs to be buffered and routed to the switch without disturbing the differentiality. The switch buffer is fairly large in order to provide a low-delay discrepancy between the positive and negative data signals regarding the mismatch variations. Fig. 7.13b shows the schematic of the LSB switch. The current is delivered by the current source bank. The current-steering is performed by the transistors M5 and M6. However, any misalignment in the rise and fall times of the buffers leads to a charge injection from the gates to the drains, *i.e.* the output of the DAC. The auxiliary transistors M7 and M8 are added in order to compensate for the injected current. Hence, they do not contribute to the output current and effect the output impedance of the current-steering cells since their source is floating. The



(a) Switch buffer. (b) LSB switch.

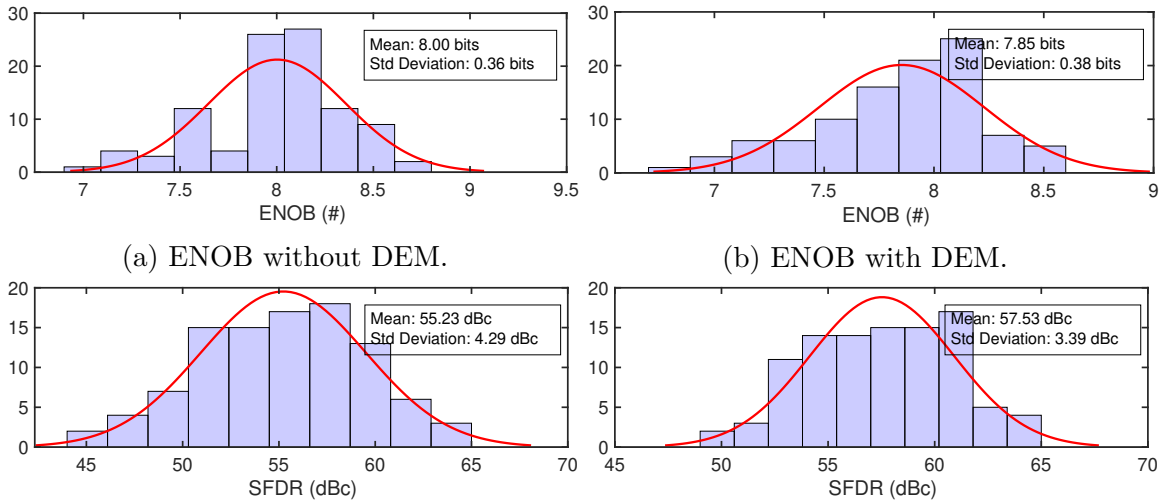
Figure 7.13: Schematic of the switch buffer and LSB switch.

MSB switches carry 32 times the current of the LSB switches. Nonetheless, they are sized by a factor of 8 larger compared to the LSB switches. The switch buffers of the LSB switches are loaded by capacitors to exhibit similar rising and falling times as the larger MSB switches.
Each I and Q DACs output is fed to a resistive stage as shown in Fig. 7.3. The poly resistors are connected to the supply. Increasing current at the DAC output results in a voltage drop. At full swing all current sources are connected to the positive or negative output which corresponds to 511 times 3 uA of output current. The resistor at the output of the DAC is 255 Ω. Thus, the minimum output voltage of the DAC is 0.8 V which is above the voltage swing requirement of the utilised current mirrors. Furthermore, the differential full swing is 0.8 V with a common-mode-voltage of 1 V.
Fig. 7.14 shows the postlayout simulated output of the I/Q DAC for a sinusoidal digital input. The differential transient output signal almost achieves 800 mV peak-to-peak. Moreover, the spectrum of the transient output signal is calculated which shows an SFDR of above 60 dBc. The calculated ENOB for the postlayout simulated I and Q DACs is 8.75 and 8.92 bit, respectively. The sampling rate of the DACs is 250 MSps



(a) Transient output. (b) PSD of I DAC. (c) PSD of Q DAC.

Figure 7.14: Postlayout simulated DAC output characteristics.

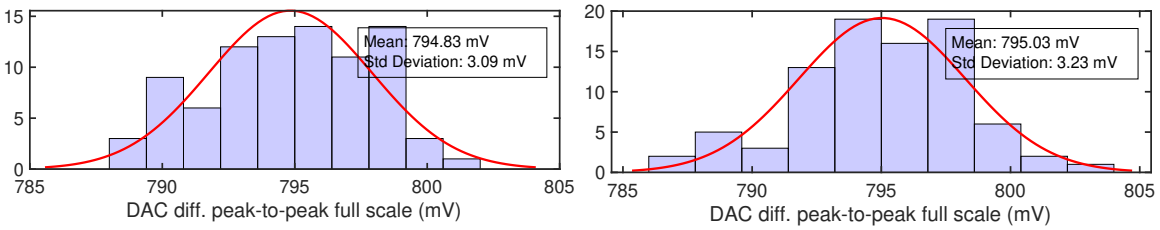


(a) ENOB without DEM. (b) ENOB with DEM.

(c) SFDR without DEM. (d) SFDR with DEM.

Figure 7.15: SFDR and ENOB sampled over transistor mismatch, Monte Carlo simulation with and without DEM.

and, hence, an alias tone appears at the frequency $f_{Nyq} \pm f_{if}$.
Fig. 7.15 shows the simulated DAC performance over mismatch with and without scrambler. Therefore, the output of only the I DAC is characterised. The mean value of the ENOB reduces to 8 bit in the presence of process and transistor mismatch. Furthermore, the ENOB is not significantly effected by the scrambler. However, the calculated in-band SFDR improves by approximately 3 dB in average which is an expected behaviour since the DEM averages out constant errors. The mismatch of the DAC amplitudes have been analysed in the system simulation. The maximum deviation, defined in Table 7.1, is limited to less than 1 % of the full-scale in order to not bottleneck the system performance by the presence of the assumed nonidealities of the remaining blocks. Fig. 7.16 shows the simulated amplitude mismatch of the utilised DAC. The standard deviation is less than 3.5 mV which corresponds to less than 0.5 % full-scale.



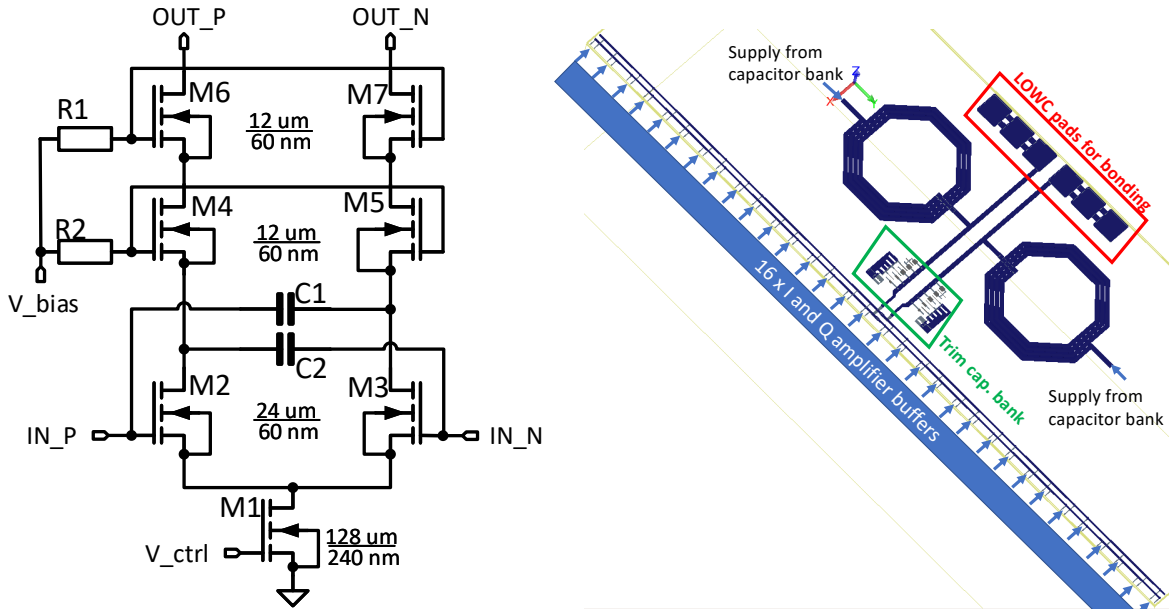
(a) I DAC.

(b) Q DAC.

Figure 7.16: Simulated amplitude variation over process.

7.2.2 Passive I/Q mixer and Output amplifier buffer

The passive I/Q mixers are shown in Fig. 7.3. The LO signals are buffered at the output of the synchronisation blocks and routed over a distance of approximately 450 um over the DAC. The passive mixers are implemented by PMOS transistors due to the high common-mode-voltage of the DAC. The transistors are placed in a triple-well structure where their bulks are connected to the supply. The passive mixer operates with 50 % duty-cycle LO signals. Thus, the differential output of each I and Q mixer is either connected to the positive or negative I and Q DAC. Due to the duty-cycle, the I- and Q-path exhibit an overlap. The passive mixers do not provide linear voltage addition at the output and, hence, the summation of the I- and Q-path cannot be performed at the mixer output. In order to sum the mixer output, LO signals with a duty cycle of 25 % are required which necessitates the synthesis at double the phasor tone frequency. Fig. 7.17a shows the schematic of the output amplifier that is implemented 32 times since the I- and Q-paths of each I/Q transmit core are separated. The signals are summed at the output of the buffers by the passive output network as shown in Fig. 7.17b. This network additionally supplies the output bias of the amplifiers. The bias point of the transistor M1 is controlled to adjust the output power. It is generated by a similar bias voltage slope as introduced in Chapter 6. Thus, a linear amplitude equalisation can be applied. The transistor M2 and M3 form the input stage. Their bias point is set by the common-mode-voltage of the DACs which is 1 V. The crosscoupled capacitors, C1 and C2, are added to boost the available gain. The transistors M4-M7 form the cascode stage. They are biased through the resistors R1 and R2. The output bias of the buffer is provided by on-chip inductors. The design of the output amplifiers is optimised for sufficient linearity, linear phase transfer function, and the ability to drive into the same node without modulating and disturbing each other.
The linearity of the I/Q transmit core depends on multiple factors. Initially, each block is designed to achieve a certain linearity. However, the SSB mixer which is controlled by rectangular LO signals leads to an additional limitation. A single-tone simulation is performed in order to analyse the linearity of the complete transmit chain. Therefore, the DACs generate an in-phase and a quadrature sinusoidal signal at a low

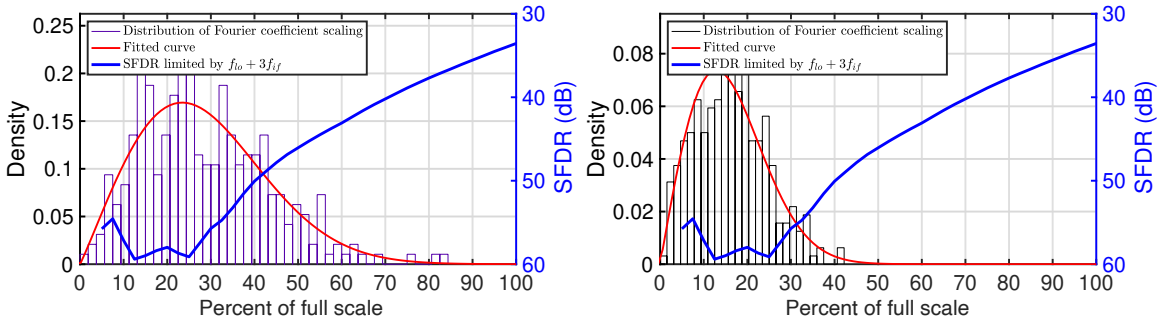


(a) Schematic of the output amplifier buffer.

(b) EM simulated passive output network.

Figure 7.17: Schematic of once output amplifier buffer and the passive output network.

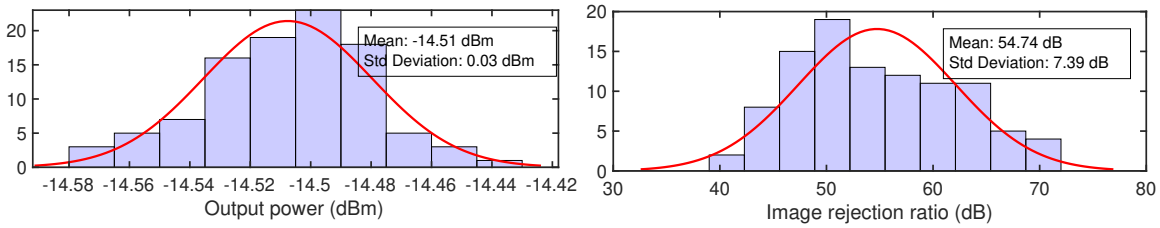
IF which is upconverted by the mixer and fed to the amplifier stage. The amplifier stage contains 32 amplifiers, all driving into the output node. All amplifiers operate at the DC bias point, whereas only the amplifiers of the actual I/Q transmit core receive an input signal. In order to speed up the simulation, the DAC is simulated in schematic mode. Its output is varied between 0 % to 100 % of the max DAC full-scale. All remaining blocks are simulated including postlayout parasitics. The wanted mixing product is in the LSB, namely at $f_{LO} - f_{IF}$. The nonlinearity of the components lead to third-order harmonics at $3f_{IF}$ at the output of the DAC, at $f_{LO} \pm 3f_{IF}$ at the output of the I and Q mixers, and $f_{LO} + 2f_{IF}$ at the output node which is the sum of the I- and Q-paths. However, the SFDR of the complete chain is not limited by the third-order nonlinearity originating from the DAC output. Due to the third harmonic of the rail-to-rail switching LO, the passive mixer generates, besides the wanted signal, a tone at the frequency $3f_{LO} + f_{IF}$. Any additional nonlinearity, *i.e.* introduced by the mixers or the amplifier buffers, leads to third-order intermodulation between $f_{LO} - f_{IF}$ and $3f_{LO} + f_{IF}$. The intermodulation product leads to a strong tone at the frequency $-f_{LO} - 3f_{IF}$. However, the summed amplifier output is a real signal such that the generated mixing product is folded to positive frequencies generating a spurious tone at the frequency $f_{LO} + 3f_{IF}$. Based on simulations, this harmonic mixing product limits the SFDR of the I/Q transmit chain. Fig. 7.18 shows the simulated SFDR. The amplitude of the sinusoidal tone is varied as a function of the



(a) PDF of QPSK Fourier coefficients.

(b) PDF of 16QAM Fourier coefficients.

Figure 7.18: Simulated SFDR limited by the nonlinear mixing product at $f_{LO}+3f_{IF}$ depending on the DAC swing. The graphs further show the probability density functions of the Fourier coefficients for different modulation types.



(a) Amplitude deviation.

(b) Image-rejection ratio.

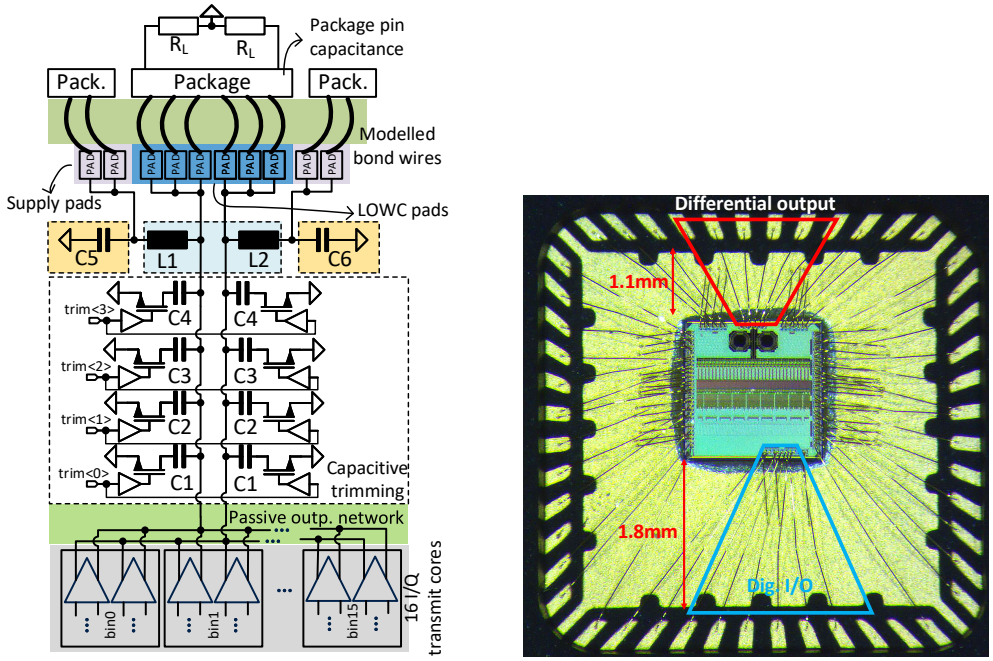
Figure 7.19: Mismatch performance of the complete I/Q transmit core.

maximum available DAC full-scale. If the amplitude of the sinusoidal tones approaches full-scale, the spurious tone at $f_{LO}+3f_{IF}$ limits the SFDR to 35 dBc. Furthermore, the graphs show the amplitude Probability Density Distribution Function (PDF) of the scaling of the Fourier coefficients as a function of the DACs full-scale. The absolute values of the complex Fourier coefficients are evaluated in two different modulation modi. The Fourier coefficients generated by the FDDAC approach exhibit with high probability low amplitudes. Especially, higher modulation orders lead in average to lower amplitudes of the coefficients which, in turn, leads to increased SFDR during the operation of the transmitter.

Fig. 7.19 shows the simulation results of the complete I/Q transmit core including mismatch in all components. The simulated amplitude deviation over mismatch is negligible. The image-rejection ratio is evaluated for ideal LO signals. The image-rejection of the I/Q transmit core is better than −45 dB.

7.3 Top-level implementation and full-system simulations

Fig. 7.20a shows the block diagram of the output stage. The complete design integrates 16 I/Q transmit cores, where each utilises two output amplifier buffers for the I- and Q-path. The 32 simultaneously operating amplifier buffers drive into an EM-simulated passive differential output network. The amplifier output bias current is delivered via the same network. Two peaking inductors are integrated on the IC which at the same time supply the bias voltage of the amplifiers. The bias voltage is connected to the IC via two bondwires for each inductor. As shown in Fig. 7.1, large capacitor banks are placed in close proximity of the inductors in order to couple the supply voltage to the on-chip ground. The size of the inductors are tuned with the main emphasis being laid on a flat amplitude response. The bondwires connecting the output of the buffers introduce a series inductance which effects the transfer characteristics significantly. Therefore, 3 bondwires for each the positive and negative outputs are used to reduce the series inductance. However, this comes at the cost of increased pad capacitance since multiple pads on the chip and pins of the package are used. The capacitive load leads to a decay of the output power with increasing frequency. The output pads are implemented employing the low capacitance pads, LOWC pads, available in the technology. They provide a substantially lower capacitance compared to the standard pads from the analogue bond pad library. On contrary, these pads do not contain any ESD protection circuits. Thus, the layout and schematic design is carried out with special care. The IC is placed staggered to the top with the intention to further reduce the series inductance by lowering the bondwire length, as simulated in Chapter 6. The bonding specifications of the production facility foresee at least 1 mm distance between the IC and the QFN pins. The displacement leads to significantly increased bondwire inductances on the opposite edge. Nonetheless, the digital I/O ports placed on the opposite edge operate at a much lower speed, hence, the increased inductance can be tolerated. The bonding process is handled in a nonautomated and non-high-volume production line which cannot be perfectly controlled. Therefore, trimming capacitors are included to tune out any unpredictable deviation from the defined specifications for the bonding. Four binary-weighted MOM capacitors, C1 to C4, are added to both differential output lines. Depending on the 4-bit programmable word, a certain combination of the capacitors are connected to the on-chip GND. NMOS RF-transistors are used as switches that always operate at the same DC point, GND, since the bias voltage is blocked. The code word which is provided by the DSP is resampled by local buffers in order to minimise any digital noise or coupled voltage swing.
The amplifier buffers in combination with the EM simulated output network, the capacitive trimming bank, the inductors, on-chip pad capacitances, the bondwires modelled as presented in Section 6.2, and pin capacitances of the QFN package are

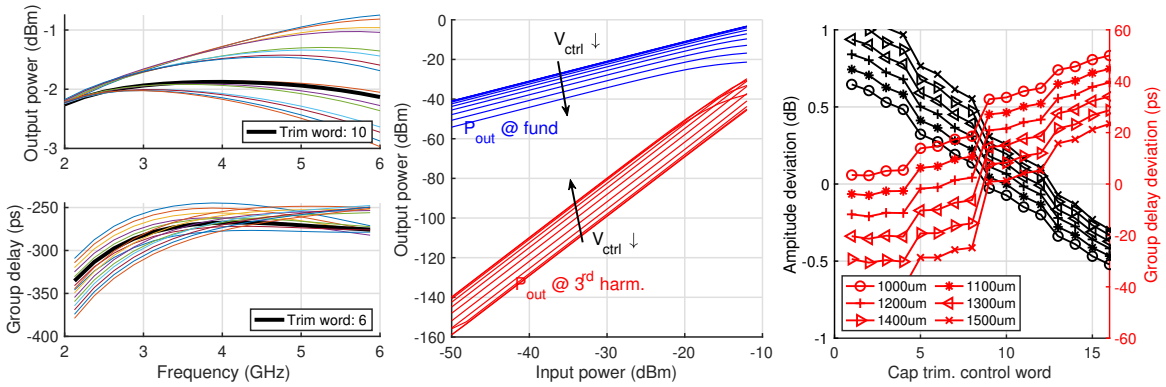


(a) Simplified block diagram of the passive output network including the trimming capacitor bank and bonding.

(b) Photograph of the bonding setup, the lid of the QFN package is opened.

Figure 7.20: Simplified block diagram of the output passive network on-chip and the bonding scheme of the IC.

simulated in *Keysight ADS*® to characterise the phase and amplitude transfer functions. The implemented tuning range covers a variation of the IC displacing in the range of 900 um to 1500 um. The displacement is measured as the distance between the top edge of the QFN package and the IC. Moreover, this takes into account varying bondwire lengths due to the changing azimuth angles. Fig. 7.20b shows a photograph of the actual produced and bonded IC. The staggered positioning is within the expected variations. Fig. 7.21a illustrates the simulated amplitude and group delay over frequency for various capacitor bank trimming values from 1 to 16. In this case, the distance between the IC and the top edge of the QFN package is assumed to be 1100 um. The simulation shows that there are two optimum points each for the lowest achievable amplitude and the group delay deviation over the entire modulation bandwidth of 2 GHz. The group delay deviation can be reduced to less than 4 ps by selecting the trimming word 6. In order to minimise the amplitude deviation, the trimming word shall be set to 10 which allows achieving nearly a constant amplitude transfer function. The system simulations predict that the group delay is much more important for the transmitter performance. Therefore, the trimming capacitor bank is used to mainly tune and minimise the group delay deviation. The amplitude deviation is corrected by the linear control voltage



(a) Simulated amplitude and group delay deviation for the actual displacement of the IC.

(b) Simulated output power at the fundamental and 3^{rd}-order tones over input power for varying V_{ctrl}.

(c) Ampl. and group delay deviation over the control word and varying IC placement uncertainty.

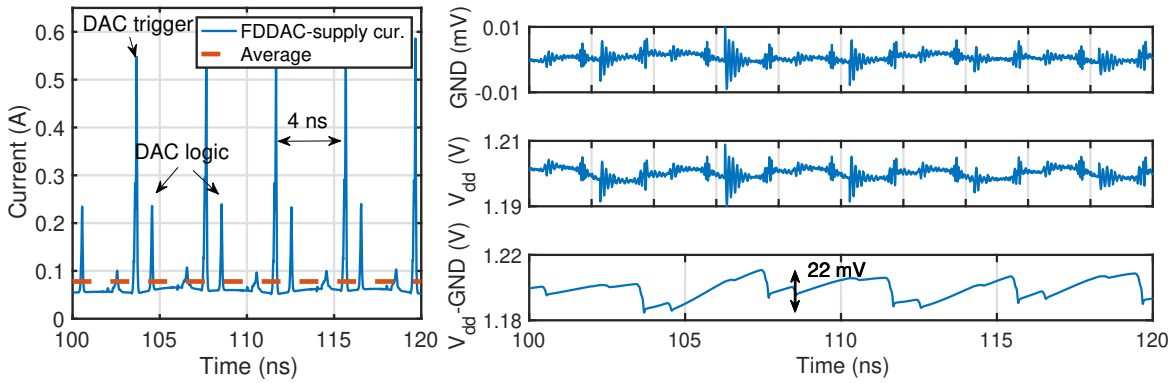
Figure 7.21: Simulated characteristics of the output amplifier buffers including the on-chip passives, trimming capacitor bank, bondwire, and package parasitics.

slope. Fig. 7.21b depicts the simulated output power of the amplifier buffer operating at 4 GHz. The power levels at the fundamental tone and its third harmonic are shown over the input power sweep for varying control voltages. By varying the control voltage, the output power can be tuned in a range of up to 10 dB. However, changing the control voltage of the amplifier buffer in order to reduce its output power increases its nonlinearity. This is shown by the third-order harmonic of the fundamental which gains in power when the amplitude of the fundamental is reduced. Therefore, the tuning range of the amplifier buffers shall not be excessively used. Fig. 7.21c shows the simulated amplitude and group delay deviation over the entire modulation bandwidth over code words for varying displacement of the IC within the package. In all cases, a trade-of can be found which allows a minimised group delay deviation at the cost of a minor amplitude deviation. The maximum amplitude deviation obtained in simulations is within ±1 dB which can be corrected by the control voltage without significantly reducing the linearity of the output buffers.

7.3.1 Supply domains and power budget

The simulated DC power consumption of one 9-bit I/Q DAC including the biasing circuits and the generated output current is 6.6 mW. Consequently, the total power consumption of 16 I/Q DACs is 105.5 mW. The DAC integrates a series of logic-gates which consume strong peak currents and current sources which exhibit a constant DC

current consumption. Therefore, the supply domains are internally separated. They share the same GND. However, a large number of logic-gates are triggered by the signal *clk_resample_*250. This leads to a high peak current of 62 mA that is consumed with a periodicity of 4 ns. The IR drops introduced by the on chip routing are compensated by distributed capacitors placed close to the actual current sinks. Thus, in each I/Q transmit core, $62\times10\times10\,\mathrm{um}^2$ of MOS gate area with a total capacitance of 87 pF is distributed. The I/Q transmit cores are the core components where all signals from different supply domains are processed. Consequently, the on-chip ground bouncing shall be minimised in order to avoid sampling issues and increased phase noise of cross supply-domain signals. The I/Q transmit cores use a common GND which is supplied by 26 down bonds. These are spread around 3 edges of the IC in order to reduce the mutual inductance. The bondwires are divided in two subgroups and analysed with the presented models in Section 6.2. The bondwire groups, connected from the two sides, provide each approximately 150 pH. The supply domain of the DACs is referred to as FDDAC-supply. It is connected by 14 bondwires which result in 400 pH of series inductance. Fig. 7.1 shows the large capacitor banks of the FDDAC-supply domain placed on the sides of the inductors. Each of these two capacitor banks contains $837\times10\times10\,\mathrm{um}^2$ MOS gate area and custom MOM capacitor structures from metal 3 to metal 9. The simulated capacitance value of each bank is above 1.5 nF.
The DC power consumption of one amplifier buffer is approximately 13.9 mW. The total power consumption of the 32 buffers is below 440 mW supplied by 2.3 V. The applied voltage slope to equalise the output power leads to a reduction of the DC power consumption since the equalisation is performed by reducing the DC current and, hence, the output power. The power consumption of the output amplifier buffers dominate the I/Q transmit cores. However, the average output power is increased by more than 18 dB compared to *FDDAC_TX1.5*. The peak modulated output power is above +4 dBm. Additionally, the consumed current only has a DC component which simplifies its handling over bondwires.
The DSP uses its isolated supply domain with a dedicated GND connection. It is not yet optimised for power efficiency. The estimated power consumption is 61 mW which further depends on the activated mode of the DSP. The frequency synthesis blocks are placed between the DSP and the I/Q transmit cores. The decoupling capacitor of the frequency synthesis blocks are designed similar to the FDDAC-supply capacitor banks. As illustrated in Fig. 7.1, the capacitors are placed next to the DSP block. Thus, these capacitors are implemented within an NWELL structure to isolate any digital noise coupling though the substrate. Moreover, the complete DSP block is surrounded by a secondary NWELL (n-p-n-p-n) structure which additionally increases the distance of the neighbouring blocks and introduces further substrate isolation. Moreover, the peak periodic current taken by the FDDAC-supply leads to ground bouncing. Based on full-system simulations it is decided to separate the GND of the I/Q transmit cores and the frequency synthesis blocks [82].



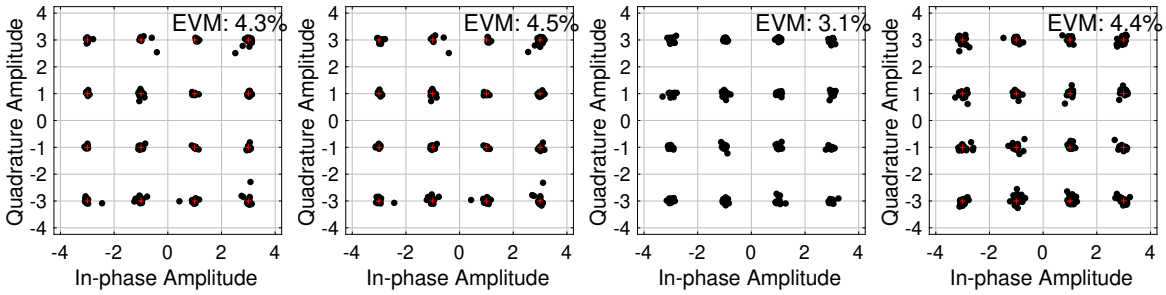
(a) Current consumption from the FDDAC-supply.

(b) Simulated supply and GND voltages in the FDDAC-supply domain including bondwire inductances.

Figure 7.22: Trans. postlayout sim. of 16 I/Q transmit cores in the FBM including parasitics, bondwire inductances, and the on-chip decoupling capacitors.

7.3.2 Full system simulations

The full-system test-bench includes the postlayout extracted I/Q transmit cores with supply rail forwarding, the fully EM simulated output network, and the DSP as described in Section 6.3.2. The netlist, in this particular case, contains more than 5 million nodes and more than 630 000 transistors which requires extremely high computation power. The I/Q DACs are one of the most critical blocks due to the high peak current consumption which need to be simulated carefully. However, the DACs also contribute a comparably large number of transistors and nodes in the complete netlist, especially when they are extracted with all parasitic capacitors and resistors (RCCC). Nonetheless, these blocks are analysed in an isolated environment including fully extraction and Process, Voltage, Temperature (PVT) variations. Based on the simulations, the DACs do not bottleneck the overall transmitter performance in all cases. Therefore, the DACs in the complete system are extracted only to include the parasitic node capacitors and the coupling capacitors which does not add a significant amount of additional nodes to the system as it is the case in the RCCC extraction.
The on-chip supply voltage variation is analysed in the FBM, where all 16 I/Q DACs are active and the highest peak currents are expected. Fig. 7.22 shows the simulated FDDAC-supply domain considering the bondwire inductance as described in Section 7.3.1 and the decoupling capacitors. Fig. 7.22a shows the sum of the current delivered by all bondwires. The current peaks up to 600 mA, whereas the average current is 92 mA. The peaks are obtained every 4 ns due to the DAC sampling rate. The first current peak that is lower in amplitude appears when the DSP provides the coefficients which leads to activity in the thermometer coder and the DEM blocks. However, the large peak is triggered by the resampling clock activating all DFFs and



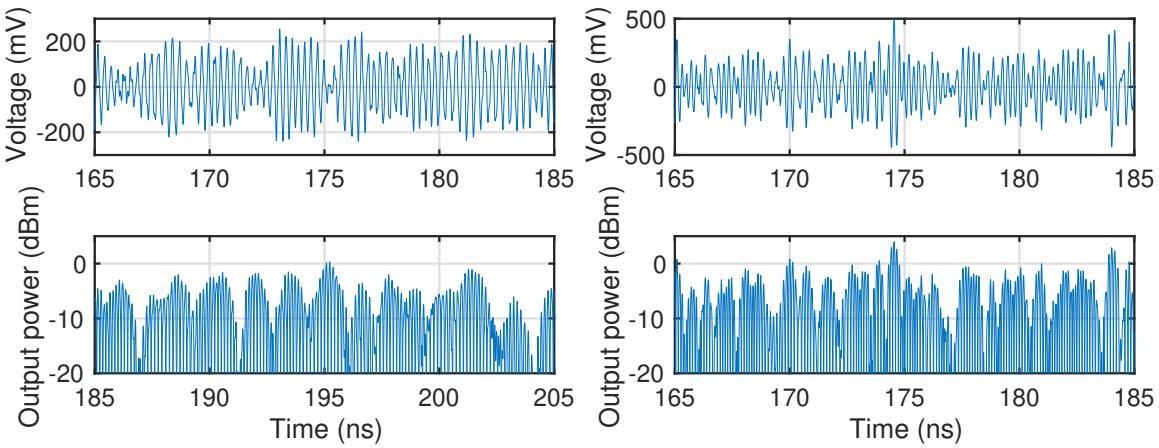
(a) HBM, ideal supply. (b) HBM w. bonding. (c) FBM, ideal supply. (d) FBM, w. bonding.

Figure 7.23: Simulated constellation diagrams of the complete transmitter with and without the effects of the on-chip supply.

switch buffers simultaneously. Fig. 7.22b depicts the on-chip GND and V_{dd} voltages showing up to 20 mV peak-to-peak swing. However, relative to the on-chip GND, the supply voltage is in average 1.2 V with a peak-to-peak swing of 22 mV that appears to have a periodicity of 4 ns.
The I/Q transmit cores are fully differential. Thus, the common-mode voltage swing of less than 22 mV does not effect the linearity of the components in the I/Q transmit cores. The complete system is simulated in the HBM and FBM mode with and without the bondwire inductances in order to characterise the effect of the supply voltage swing. The frequency synthesis blocks are replaced by their dedicated *VerilogA* models, as mentioned in Chapter 6, which are parametrised based on the values in Table 7.1. The results are presented in Fig. 7.23. The simulated EVM performance is significantly improved compared to the *FDDAC_TX1*. This is based on the improved estimation of the performance of the frequency synthesis blocks, increased linearity of the I/Q transmit cores, and the quantisation length of the DACs. The outstanding common-mode rejection ratio of the I/Q transmit cores in both transmit modi leads to slightly decreased EVM when the bondwire inductances are taken into account.
Fig. 7.24 shows the simulated transient output signal of the transmitter at the 100 Ω differential load considering the bonding, the packaging and an ideal balun. The instantaneous power peaks up to +3 dBm and +6 dBm in the HBM and FBM.

7.4 Physical verification and measurement setup

Fig. 7.25 shows a photograph of the measurement setup. The PCB with the transmitter IC and the balun are directly attached to the vector signal analyser by SMA adaptors. Fig. 7.26a illustrates the implemented PCB and the hybrid balun. The 4-layer FR4



(a) HBM, P_{rms} =−7.2 dBm. (b) FBM, P_{rms} =−4.4 dBm.

Figure 7.24: Simulated transient output of the FDDAC-based transmitter and the instantaneous output power in the HBM and FBM.

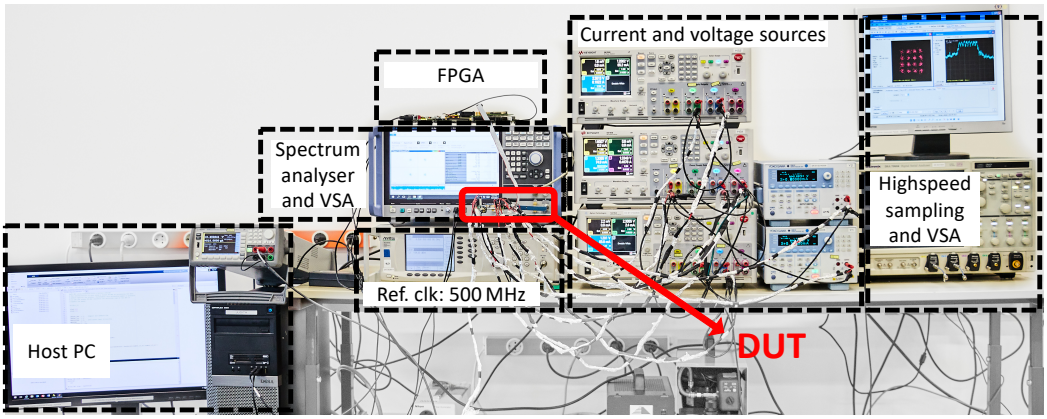
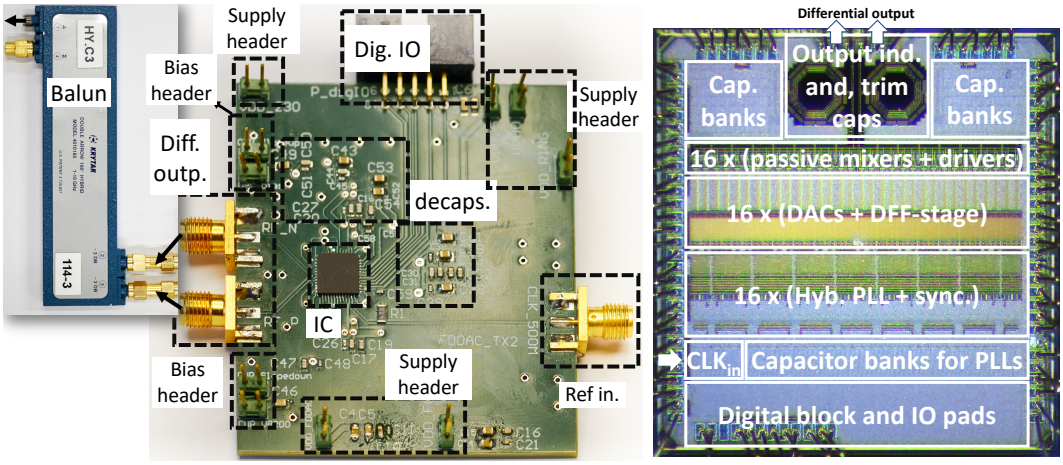


Figure 7.25: Photograph of the measurement setup.

PCB has GND planes on the top and bottom layers, whereas the internal layers are used for the supply voltages of the ring oscillators, PLLs, and the FDDAC-supply domain. The top and bottom layers are populated with decoupling capacitors. Large tantalum capacitors are placed on the bottom of the PCB next to the supply headers, whereas the ceramic SMD capacitors with a smaller size and higher resonance frequency are placed as close as possible to the IC. The clock input at 500 MHz is generated by a reference oscillator. The input clock processing block is designed for 0 dBm input power. However, the reference oscillator is set to 4 dBm due to cable and connector losses which have not been taken into account during the schematic design. The differential output of the FDDAC transmitter is routed by 50 Ω coplanar lines on the PCB and connected via SMA connectors to the external *Krytar* 180° hybrid balun. The PCB is designed regarding the physical dimensions of the balun such that the SMA connectors

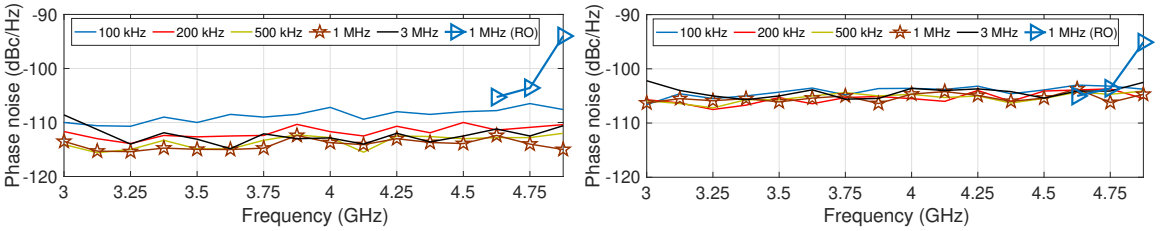


(a) Photograph of the implemented PCB carrying the *FDDAC_TX2* IC as the DUT.

(b) Chip micrograph occupying $1.9 \times 1.9\,\mathrm{mm}^2$ chip area.

Figure 7.26: Photograph of the PCB with the hybrid balun and the chip micrograph.

are directly attached to the hybrid without any additional cables. The attenuation of the hybrid balun, on-PCB routing, connectors, and adaptors is approximately 2 dB. The single-ended output of the balun is directly fed to a *Rohde und Schwarz FSW44* with a signal analysis bandwidth of up to 4 GHz. The transmitter chip is controlled by the host PC which establishes a connection with the FPGA board that contains the custom ser_{tx} module to communicate with the IC as presented in Chapter 6. Fig. 7.26b depicts a chip micrograph and the bonding scheme is presented in Fig. 7.20b.

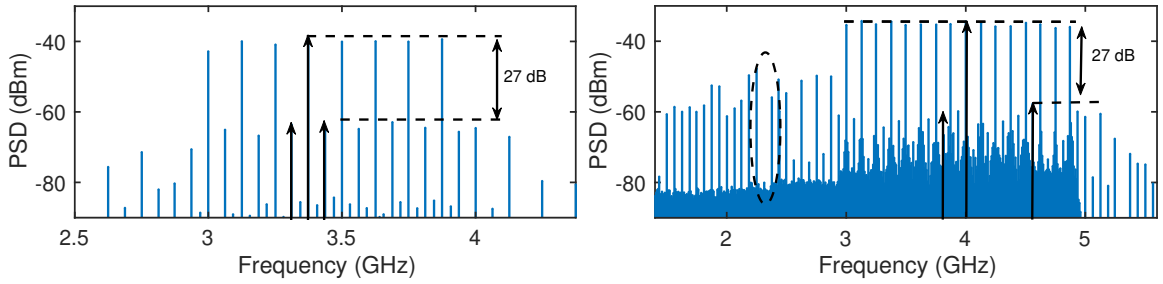


(a) Reduced DSP activity.

(b) DSP active including FFT-processors.

Figure 7.27: Meas. phase noise performance evaluated at various offset frequencies including the ring-oscillator-based PLLs for the 3 highest freq. tones [82].

Fig. 7.27 shows the measured phase noise of the hybrid-PLLs evaluated at various offset frequencies with and without DSP activity. Moreover, the measured phase noise at 1 MHz offset of the secondary ring-oscillator-based synthesiser is shown for the highest 3 frequencies. The phase noise of the hybrid-PLLs is reduced by approximately 10 dB compared to the *FDDAC_TX1.5*. This is achieved by the changes in the floor



(a) Bins: 0-to-7.

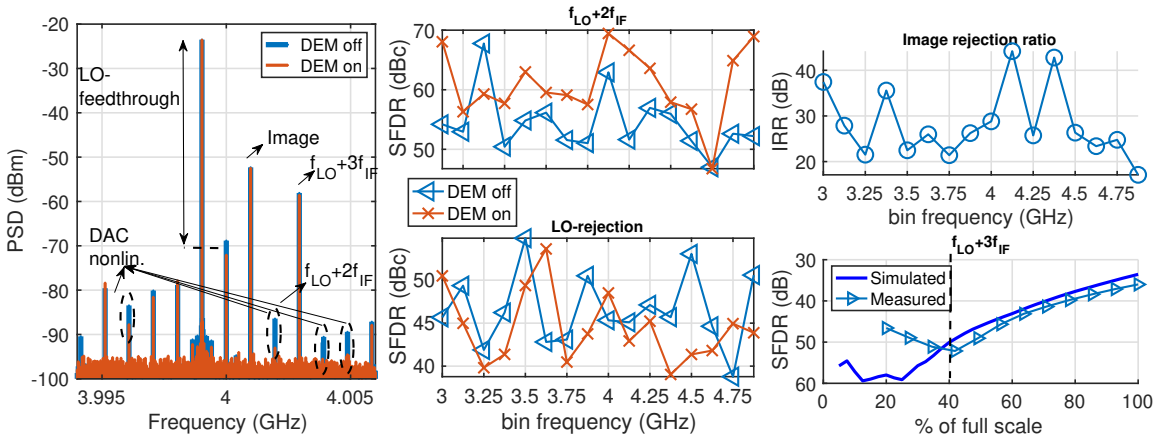
(b) Bins: 0-to-15, over large span.

Figure 7.28: Measured PSD of the phasor tones in *all_dac_set_max* mode.

plan and added capacitor banks, even though the frequency synthesis circuits remain mostly unchained [82]. The input clock processing block is placed such that neither the supply nor the generated reference clocks cross over the DSP which reduces the noise in the reference signal and, hence, directly effects the in-band noise of the PLLs. The initially estimated phase noise of 100 dBc at 1 MHz, given in Table 7.1, is met over the entire modulation bandwidth.

Fig. 7.28 depicts the measured PSD for the *all_dac_set_max* mode. In the HBM and FBM which utilise 8 and all 16 phasor tone generators, the measured SFDR is limited to 27 dBc by spurious tones at an offset frequency of 62.5 MHz with respect to the phasor tones. Furthermore, the hybrid PLLs that include frequency multipliers, generate unwanted spurious tones at half and double the desired output frequencies. Note that the spurs of the tones at higher phasor tone frequencies are more distinct. The phasor tone of bin 15 is at 4.875 GHz. It generates a strong spurious tone at 2.4375 GHz which exhibits almost the same signal power as the phasor tone of the bin 0 at 3 GHz. This leads to significant spurious emissions at the left hand side of the modulated band that interfere with the wanted output signal. The transmitter contains a secondary frequency source which is a ring-oscillator-based PLL that directly generates the phasor tone at the wanted frequency that does not contain spurs at half or double the desired frequency. Unfortunately, these PLLs turned out not to work properly [82]. In order to achieve proper locking of the PLLs at certain bins, the supply voltages of the frequency synthesis blocks are manually tuned. In the FBM, as shown in Fig. 7.28b, the phasor tones of the bins 13-to-15 could be generated by the ring-oscillator-based PLLs instead of the hybrid-PLLs which, in turn, do not generate the high power spurious tones at frequencies close to the lower end of the modulated band. The dashed ellipse in Fig. 7.28b shows the lack of unwanted spurs at half the phasor tone frequencies. The inferior phase noise of the ring-oscillator-based PLL, especially for the bin 15, compared to the hybrid-PLL is tolerated since the spurious tone at half the frequency has a more severe impact on the transmitter performance.

Furthermore, the integrated DSP includes a LUT which stores a 9-bit sinusoidal tone. It can output digital sine and cosine tones at a fraction of the DSP speed,



(a) PSD of the signal generated by the I/Q transmit core operating at 4 GHz with and without DEM.

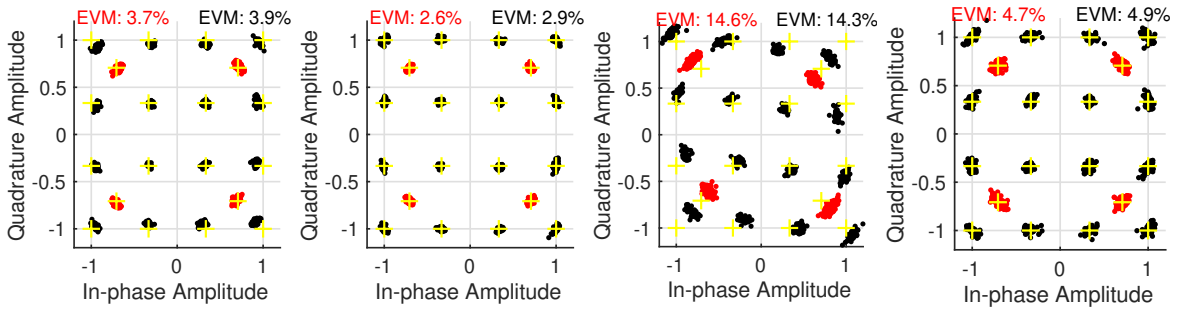
(b) Meas. SFDR limited by the LO feedthrough and the third harmonic of f_{IF} introduced by the DAC.

(c) Top: Meas. image-rejection over phasor tones. Bottom: SFDR limited by the mixing product at $f_{LO} + 3f_{IF}$.

Figure 7.29: Measured PSD of one I/Q transmit core illustrating several spurs which limit the SFDR and the compiled results for all 16 bins.

namely 250 MHz, instead of the Fourier coefficients. Thereby, the performance of a single I/Q transmit core can be analysed in an isolated manner. Fig. 7.29a shows the PSD of the I/Q transmit core operating at 4 GHz, sampling a sinusoidal tone at the frequency of 250/256 MHz with and without DEM. The PSD is measured at the output of the IC which contains the nonidealities originating from the frequency synthesisers, DACs, passive mixers, amplifier buffers, and the passive output network. The DEM reduces the power of the spurious tones generated by the DAC by slightly increasing the noise-floor. The third harmonic of the sinusoidal tone, generated by the DAC, leads to a spurious tone at $f_{LO} + 2f_{IF}$ at the output which is measured for all 16 bins, as shown in Fig. 7.29b (top), with and without DEM. With DEM, the power of the DAC spurs are in average reduced by 6.6 dB. The LO feedthrough for the bin at 4 GHz is −45 dBc with DEM and −48 dBc without DEM. It is slightly increased by the DEM due to the higher switching activity which leads to charge injection to the output and thereby a DC component of the digital input causing the feedthrough. Fig. 7.29b (bottom) shows the measured LO-rejection for all 16 bins with and without DEM. The image-rejection ratio in this particular case, measured for the bin at 4 GHz, is 29 dB. As expected, it is not effected by the DEM. Fig. 7.29c (top) shows the measured Image Rejection Ratio (IRR) for all 16 bins. The complete I/Q transmit cores excluding the frequency synthesisers are simulated over PVT, where an IRR of better than 45 dB is ensured in all cases. Thus, the source of the I/Q mismatch is localised to be in the frequency synthesis block which contains minimally sized buffers in the signal path

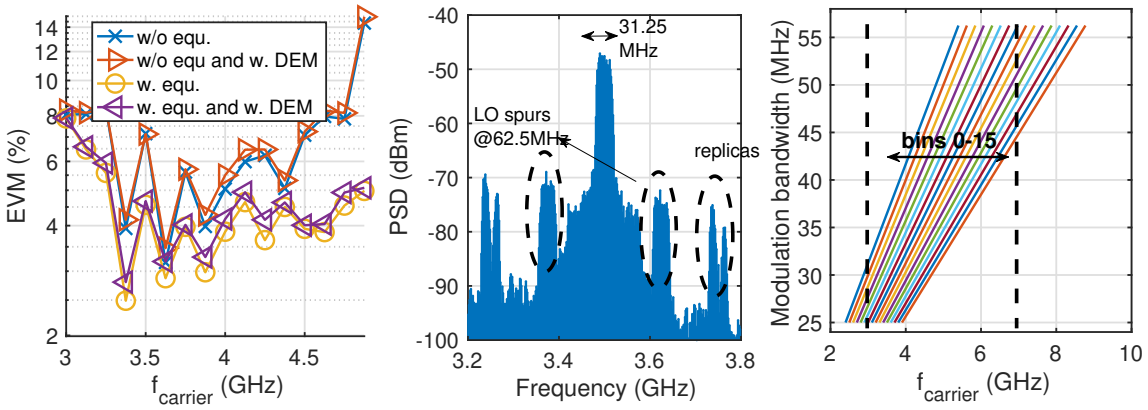
leading to strong I/Q imbalances. Besides the image signal, the SFDR is limited by the mixing product at the frequency $f_{LO} + 3f_{IF}$ as described in Section 7.3. However, the sinusoidal tone in this particular measurement case spans over the full-scale of the DAC. Fig. 7.29c (bottom) shows the measured and simulated SFDR limited by the mentioned tone. In the measurement, the DAC bias current is scaled in order to vary the swing of the sinusoidal tone. The measured SFDR matches the simulated curve up to a reduction of the amplitude to 40 % of the full-scale. However, tuning the DAC bias current also changes the DC point of the amplifier buffers which leads to a deviation of the measured curve compared to the simulation for amplitudes less than 40%.
The *FDDAC_TX2* contains 16 I/Q transmit cores in order to implement the FDDAC-based transmitter which can be utilised as conventional transmitters. Since the complete system is implemented in order to operate simultaneously, the 16 conventional transmitters can be utilised altogether. Fig. 7.30 shows the measured constellation diagrams for QPSK and 16QAM with a modulation bandwidth of 31.25 MHz with and without equalisation. The bins 7 and 15 which correspond to carrier frequencies of 3.875 GHz and 4.875 GHz are exemplary selected and analysed. The measured EVM of the bin 7 without equalisation is 3.9%. The equaliser is implemented by a 21-tap filter which slightly improves the EVM to 2.9%. However, bin 15 shows a significantly higher I/Q mismatch which leads to a distorted constellation diagram which can be corrected by the equaliser. Additionally, the increased phase noise leads to higher EVM which cannot be corrected by the equaliser. Fig. 7.31a shows the compiled



(a) $f_c = 3.875\,\text{GHz}$, w/o equalisation. (b) $f_c = 3.875\,\text{GHz}$, with equalisation. (c) $f_c = 4.875\,\text{GHz}$, w/o equalisation. (d) $f_c = 4.875\,\text{GHz}$, with equalisation.

Figure 7.30: Meas. constellation diagrams in the conv. transmit mode for bins 7 and 15 at the corresponding carrier frequencies with and without equalisation.

measurement results presenting the obtained EVM for all 16 bins with and without equalisation and DEM. The best obtained EVM is 2.49 % with equalisation and 3.19 % without equalisation. The DEM does not effect the performance since the linearity of the DACs does not limit the obtained performance. The equalisation corrects constant errors such as I/Q mismatch and group delay deviations, whereas dynamic errors



(a) EVM evaluated for all 16 I/Q transmit cores.

(b) Meas. PSD of bin 4 in the conv. transmit mode.

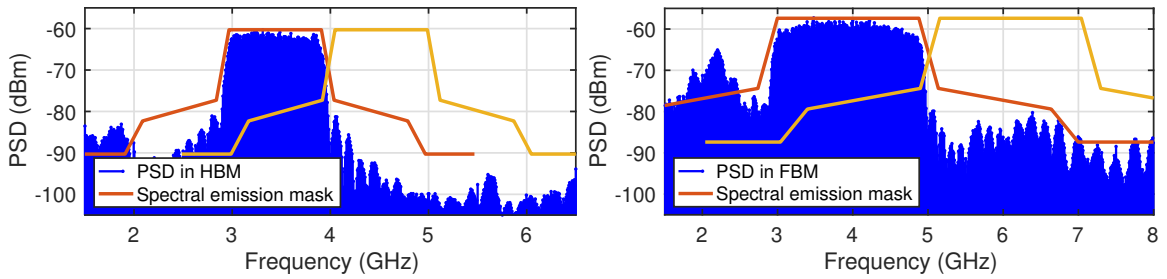
(c) Achievable carrier frequencies and bandwidths.

Figure 7.31: Measured PSD of one I/Q transmit core illustrating several spurs which limit the SFDR and the compiled results for all 16 bins.

caused by spurious tones, phase noise, *etc.* cannot be corrected. Fig. 7.31b presents the PSD measured in the conventional transmit mode. The band shaping is achieved by an OSR of 8 and digital RRC filtering which is fully integrated in the on-chip DSP. The Nyquist replicas are present at ±250 MHz which is the sampling rate of the DACs. Moreover, the spurs of the LO signal at 62.5 MHz lead to spurious emissions around the modulated band. The I/Q transmit cores are designed to operate up to a sampling frequency of 500 MHz. Furthermore, the integrated DSP is implemented for the worst case conditions and, hence, it can be pushed to operate at higher frequencies. Thus, the main input clock of the complete transmitter system is varied to change the modulation bandwidth in the conventional mode and the carrier frequencies of the I/Q transmit cores. The input clock is varied between 400 MHz and 900 MHz which corresponds to a modulation bandwidth between 25 MHz to 56.25 MHz. The achievable bandwidths and corresponding carrier frequencies are presented in Fig. 7.31c, whereas the dashed lines mark the tuning ranges of the hybrid-PLLs. However, various modulation bandwidths at carrier frequencies between 2.4 GHz and 6.3 GHz have been demonstrated.

7.4.1 FDDAC-mode

Fig. 7.32 shows the PSD in the HBM and FBM including the spectral mask of the WiGig specification. With the linear amplitude correction, a flat frequency response is obtained which leads to negligible amplitude deviation over frequency. At lower frequencies, the spectral mask is violated by the spurious emissions of the frequency synthesis block. However, in close proximity of the band, the spectral shaping capabilities are

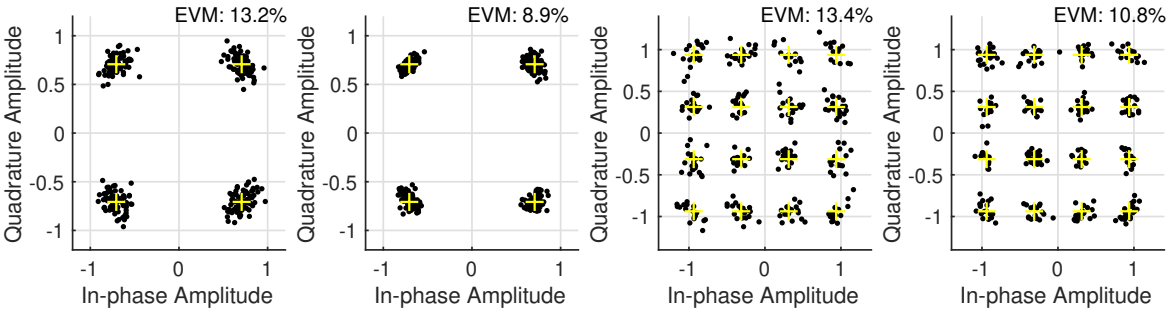


(a) Measured PSD of the HBM.

(b) Measured PSD of the FBM.

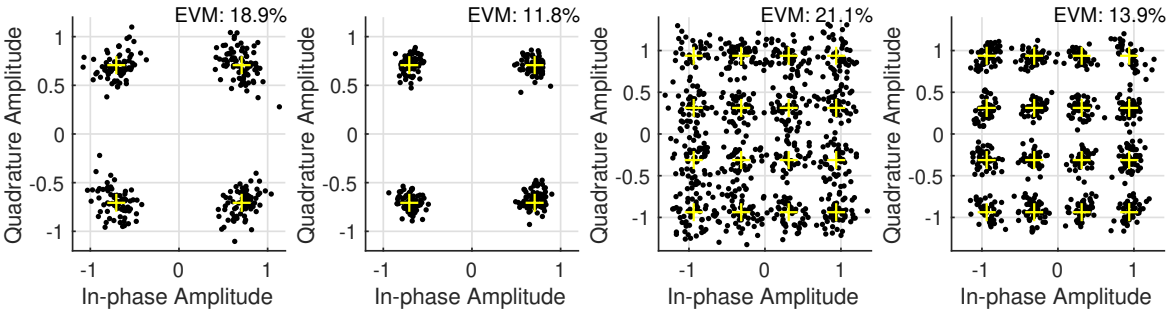
Figure 7.32: Measured PSD and the spectral mask of the WiGig standard [5].

further improved compared to *FDDAC_TX1.5* due to a reduced timing mismatch of the phasor tones. Note that the modulation bandwidth is approximately 13.7 % wider than stated in the spectrum for the given spectral mask.
Fig. 7.33 presents the measured constellation diagrams for QPSK and 16QAM in the HBM with and without equalisation utilising a modulation bandwidth of 1 GHz. In the HBM, the constellation is examined for the bins 5-to-12, since these bins achieve the best performance in the conventional mode without equalisation. The 21-tap equalisation is partially able to correct the I/Q mismatches of the utilised bins. Moreover, the equaliser is able to correct any constant timing mismatch between the phasor tones. Unfortunately, some of the synchronisation blocks suffer from strong back and forth issue which leads to an incorrect alignment. This has been foreseen in the design process and 16 specific control bits are added to the DSP in order to freeze the state of the control loop of certain synchronisation blocks independently. Therefore, a constant timing offset remains after freezing the states of the synchronisation blocks which suffer from the back and forth issue. This limits the measured EVM without equalisation. The equaliser integrated in the VSA tool considers the constant timing errors as a group delay deviation and corrects it. Once the equaliser matches the actual timing offset, it can be used for different modulation schemes and transmit modes. Thereby, the performance limitation of the synchronisation blocks can be examined and partially eliminated by the equaliser. The EVM without equalisation is 13.2 % and 13.4 % for QPSK and 16QAM, respectively. However, with equalisation they drop to 8.9% and 10.8%. Furthermore, the transmitter is able to change the output frequency in the HBM in discrete steps of 125 MHz by changing the utilised bins from 0-to-7 to 8-to-15. The EVM performance is measured for different sets of bins. The results are presented in Table 7.2. The best obtained EVM with equalisation is 7.2 % for the bins 0-to-7 and without equalisation 13.2 % for the bins 5-to-12.
Fig. 7.34 presents the measured constellation diagrams in the FBM with and without equalisation utilising a modulation bandwidth of 2 GHz for QPSK and 16QAM. The phasor tones of the bins 0-to-12 are generated by the hybrid-PLLs, whereas the highest frequency bins 13-to-15 receive the LO signal from the ring-oscillator-based PLL. The



(a) QPSK, w/o eq. (b) QPSK, with eq. (c) 16QAM, w/o eq. (d) 16QAM, with eq.

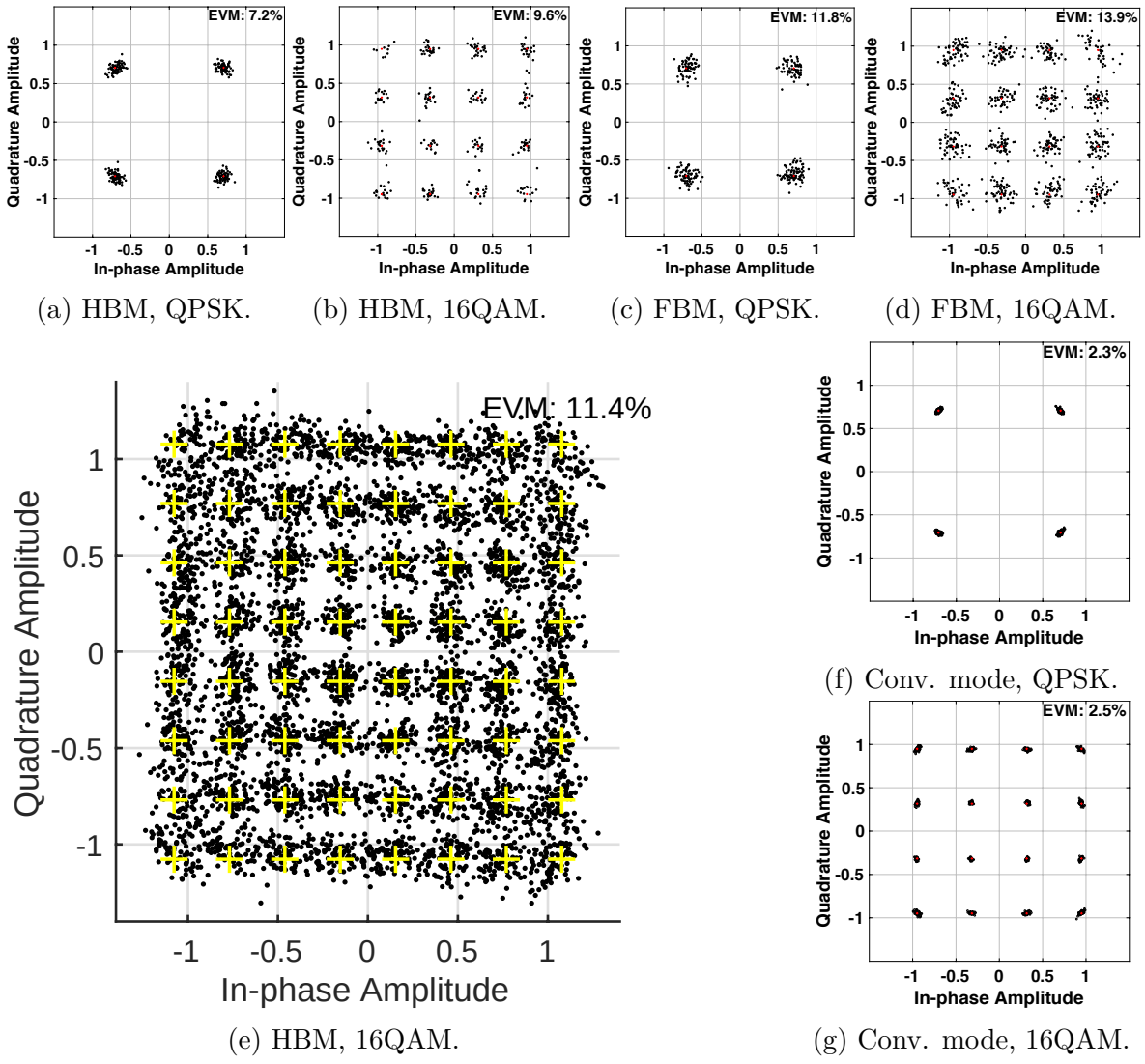
Figure 7.33: Measured constellation diagrams of the FDDAC-based transmitter for a modulation bandwidth of 1 GHz in the HBM for QPSK and 16QAM with and without equalisation. The bins 5-to-12 are utilised.



(a) QPSK, w/o eq. (b) QPSK, with eq. (c) 16QAM, w/o eq. (d) 16QAM, with eq.

Figure 7.34: Measured constellation diagrams of the FDDAC-based transmitter for a modulation bandwidth of 2 GHz in the FBM for QPSK and 16QAM with and without equalisation.

measured EVM without equalisation is slightly higher than in the HBM since all 16 bins are active and all timing errors as well as I/Q mismatches of the phasor tones effect the performance. The measured EVM without equalisation is 18.9 % and 21.1 % for QPSK and 16QAM. However, with equalisation which is able to correct the constant timing and I/Q mismatches, the performance can be improved to 11.8 % and 13.9 % for QPSK and 16QAM, respectively.
Fig. 7.35 shows the best measured constellation diagrams for different modulation orders and various transmit modi including equalisation. For a modulation order of 64QAM the best obtained EVM is 11.4 %. Furthermore, the best achieved EVM in the conventional transmit mode for a modulation bandwidth of 31.25 MHz are 2.3 % and 2.5 % for QPSK and 16QAM, respectively.
Besides the measured EVM performance, Table 7.2 lists the output power for different frequency ranges and modulation types in the HBM as well as in the FBM without linear amplitude correction. The measured amplitude decay is higher than simulated



(a) HBM, QPSK. (b) HBM, 16QAM. (c) FBM, QPSK. (d) FBM, 16QAM.

(e) HBM, 16QAM.

(f) Conv. mode, QPSK.

(g) Conv. mode, 16QAM.

Figure 7.35: Best measured constellation diagrams for different modulation orders in various transmit modi with equalisation.

which is due to the larger than the estimated parasitic capacitances of the QFN package and the soldering to the PCB. The RMS power, P_{rms}, of the modulated band in the HBM for 16QAM varies between $-6.47\,\text{dBm}$ to $-13.35\,\text{dBm}$ for varying frequency ranges, whereas the simulated value is $-7.2\,\text{dBm}$. In the FBM the measured RMS power for 16QAM is $-4.42\,\text{dBm}$, whereas the simulated value is $-4.4\,\text{dBm}$. The linear voltage slope generated by two bias currents and an RC network sets the control voltage, V_{ctrl}, of the output amplifier buffers in order to equalise the amplitude deviation. Therefore, the output power of the I/Q transmit cores at lower frequencies have been reduced which, in turn, leads to a lower output power and a reduction of the power

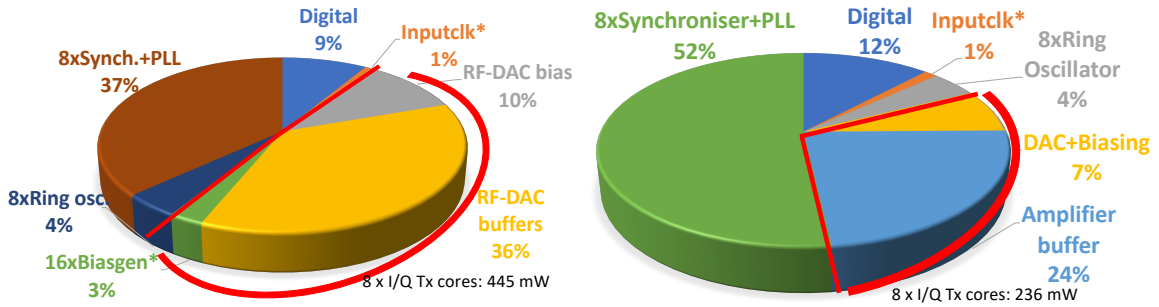
	QPSK				16QAM			
	EVM (%)		Output (dBm/dB)		EVM (%)		Output (dBm/dB)	
bins	no equ.	equ.	P_{rms}	ACLR	no equ.	equ.	P_{rms}	ACLR
0-7	15.87	7.28	-7.46	-36.06	15.03	9.86	-6.47	-36.86
1-8	14.75	8.71	-8.68	-35.58	18.67	12.09	-7.67	-36.7
2-9	16.62	9.89	-9.98	-36.99	17.64	11.86	-8.86	-38
3-10	16.52	13.27	-9.11	-36.68	17.91	14.68	-8.12	-37.7
4-11	16.73	8.74	-10.36	-36.88	24.29	13.29	-9.62	-37.87
5-12	13.20	8.91	-11.4	-33.4	13.45	10.87	-10.61	-33.67
6-13	13.82	9.90	-12.6	-30.59	14.66	10.81	-11.67	-31.96
7-14	14.74	9.96	-13.5	-32.27	15.56	12.19	-12.73	-33.05
8-15	17.85	13.62	-14.42	-29.42	19.18	15.29	-13.35	-31.27
0-15	18.98	11.84	-5.27	-27.83	21.18	13.91	-4.42	-27.81

Table 7.2: Measured EVM with and without equalisation, RMS output power, and the ACLR for QPSK and 16QAM in the HBM for various bins and the FBM.

consumption of the output amplifier buffers. In order to achieve a flat frequency response, the RMS power of the modulated band in HBM and FBM have been reduced to approximately −12.5 dBm. Furthermore, the trimming capacitor bank is digitally tuned for each frequency range and bias slope setting in order to minimise the group delay deviation. Thereby, the measured EVM without equalisation is further improved. Additionally, the ACLR is calculated by utilising the WiGig spectral mask and its contracted version for the HBM mode on the right hand side of the modulated band, as shown in Fig. 7.32. Compared to the *FDDAC_TX1.5*, the obtained ACLR is improved due to the reduced timing mismatch, high output power of the I/Q transmit cores and reduced out-of-band spurious signals generated by the frequency synthesis blocks.

7.4.2 Power consumption

Fig. 7.36 shows the power break down comparison between the *FDDAC_TX1.5* and *FDDAC_TX2* in the HBM for a modulation bandwidth of 1 GHz. The total power consumption of the transmitter is reduced from 882 mW to 771 mW, whereas the power consumption of the I/Q transmit cores based on the power efficient DACs is reduced by nearly a factor of 2 from 445 mW to 236 mW. In addition to the reduced power consumption, the RMS output power of the transmitter is increased by approximately 18 dB.
Table 7.3 lists the measured and estimated power consumption of several subblocks for the three implemented transmitters. In the HBM, the power consumption of the ring



(a) *FDDAC_TX1.5*, P_{total} : 882 mW. (b) *FDDAC_TX2*, P_{total} : 771 mW.

Figure 7.36: Power consumption break down of the FDDAC-based ICs in the HBM. *:Estimation.

oscillators is divided by 2 since they cannot be fully deactivated and still consume current due to active branches [82]. In the FBM, the *FDDAC_TX2* consumes 1.6 W for a data rate of 8 Gbit/s and modulation bandwidth of 2 GHz. The power consumption of the frequency synthesis blocks have been reduced in the transition from the *FDDAC_TX1* to *FDDAC_TX1.5*. For *FDDAC_TX2*, the frequency synthesis blocks remain mainly unchanged, in turn, the power consumption is not significantly changed. The I/Q transmit cores benefit from the frequency scaling in the first transition and from the architectural changes in the second transition. Compared to the first IC, the I/Q transmit cores of *FDDAC_TX2* require nearly a quarter of the initial power while providing 18 dB more output power, DEM, increased resolution, and better performance in terms of linearity and SFDR.

7.5 Discussion

The presented transmitters demonstrate that the FDDAC-approach allows to integrate a complete transmitter which can generate a coherent modulation bandwidth of up to 2 GHz and a data rate of up to 12 Gbit/s with outstanding spectral shaping capabilities in a relatively cheap 65 nm CMOS technology. Thereby, the complete baseband signal processing, PRBS-based data generation, analogue-mixed-signal components such as the DACs, mixers, amplifier buffers alongside with the frequencies synthesis blocks are integrated on the same IC with a silicon area of less than $1.9 \times 1.9\,\text{mm}^2$.
The phase noise performance of the frequency synthesis block has been improved in the presented design iterations such that it is not limiting the performance of the complete transmitter in the *FDDAC_TX2*. However, the frequency synthesis still comprises in-band spurious tones, especially at offset frequencies of 62.5 MHz and 125 MHz which limit the in-band SFDR. Furthermore, the hybrid-PLLs generate unwanted spurious

	FDDAC_TX1	FDDAC_TX1.5		FDDAC_TX2	
	HBM	HBM	FBM	HBM	FBM
Digital (mW)	70.4	78	78	92.4	103.2
Inputclk* (mW)	22.4	9.6	9.6	9.6	9.6
RF-DAC output bias*** (mW)	72	89.6	89.6	-	-
RF-DAC buffers (mW)	770	330	655.2	-	-
Biasgen* (mW)	28	24	24	-	-
Multiplier, freq divider, [etc].** (mW)	336	-	-	-	-
Synch. + PLL (mW)	697.2	331.2	825.6	399.6	947.5
Ring oscillators (mW)	-	19.5	39.1	33.6	68.4
DAC + Biasing (mW)	-	-	-	55.6	131.3
Amplifier buffer (mW)	-	-	-	180.5	356.5
Total I/Q transmit cores (mW)	870	443.6	768.8	236	488.7
Total (mW)	1996	881.9	1721.1	771.3	1616.5

*:Estimation, **:Uncontrollable due to voltage instability, ***:SPM=0.

Table 7.3: Power consumption comparison between the ICs in the HBM and FBM.

tones at half and double the phasor tone frequencies. This effect becomes more distinct for high phasor tone frequencies which leads to out-of-band spurious emissions in close proximity of the modulated band that interfere with the output signal and violate the spectral mask. These spurious tones are mainly caused by the cross-coupling between the PLLs over supply-rails, lack of sufficient supply rejection, and process variations which can be overcome by potential circuit design improvements in terms of PVT. In order to reduce the spurious emissions in further design iterations, additional supply controllers, *i.e.* LDOs, can be implemented for each frequency synthesiser in a tree structure, as presented in the PCB-based hybrid implementation in Chapter 4.
The I/Q transmit cores are characterised by measurements of the conventional transmitter mode and the single-tone analysis. The performance in terms of linearity, output signal power, and SFDR is outstanding and matches well with the simulations results. Especially, the power efficient DACs can be reused in future design iterations targeting a wider modulation bandwidth and improved signal quality. The conventional transmit mode with 16x31.25 MHz single-carrier signals achieve an EVM of up to 2.5 % for 16QAM. By tuning the input clock, the modulation bandwidth and transmit frequency have been varied between between 25 MHz to 56.25 MHz and 2.4 GHz to 6.3 GHz which stresses on the flexibility of the FDDAC-based transmitter. However, a significant I/Q mismatch deviation over the bins is observed which can be corrected by equalisation in the VSA. Although, in the FDDAC-mode the varying I/Q mismatches of the bins deteriorate the achievable performance with and without equalisation. The measured I/Q mismatch originates from the frequency synthesis blocks that contain minimally sized inverter chains leading to delay deviations between the I- and Q-paths. However,

this can be tuned in a redesigned IC by introducing digitally controlled delay lines in the I- and Q-paths in order to tune the I/Q mismatch. Moreover, the parasitic capacitors introduced by the package and soldering is slightly higher than the estimated values in simulations which leads to a more distinct amplitude decay at the output of the transmitter over the modulation bandwidth. The integrated linear amplitude correction slope in combination with the digitally controlled trimming capacitor bank are able to bear a flat frequency response at the cost of a slightly reduced output power and linearity. Nevertheless, the large tuning range of the trimming capacitors is digitally controlled in order to reduce the group delay deviation of the output passive network even with the parasitic capacitors of the package that are higher than estimated which, in turn, leads to an improved EVM without equalisation. In order to correct the amplitude deviation without sacrificing the linearity and output power, a digital predistortion can be implemented in the DSP instead of the analogue linear amplitude correction by simply multiplying each Fourier coefficient with a scaling factor.
The synchronisation DLLs at certain frequencies do not lock properly which leads to an increased timing mismatch σ_τ [82]. As investigated in Chapter 3, the timing mismatch heavily bottlenecks the transmitter performance. However, this has been foreseen and dedicated control bits in order to freeze the closed-loop controller are implemented in the integrated DSP. Thus, the DLLs can be forced to keep the actual state. Thereby, any dynamic error due to lack of locking is omitted. The effected DLLs are repeatedly started and stopped in order to achieve a minimised timing mismatch after freeze. The equaliser within the VSA device is able to detect the remaining constant timing mismatch as a group delay deviation and correct it. This has been verified by analysing the transfer characteristics of the equaliser. The measured transmitter performance is significantly improved by a simple 21-tap equaliser since the synchronisation error and the I/Q mismatch deviation which bottleneck the performance are constant errors. In a further design iteration, the actual state of the closed-loop of the DLLs shall be read out by the DSP in order to digitally tune the delay lines after freezing. A digital tuning of the delay lines has been implemented in the *FDDAC_TX1* without the readout functionality but it has been discarded in the continuous designs in order to reduce the routing complexity. The I/Q and timing mismatch correction can be implemented by controlling the DCDLs for the I- and Q-path of the synchronisation DLLs individually. Thereby, the results without equalisation can be remarkably improved.
Table 7.4 shows a comparison with state-of-the-art transmitters which utilise a wide modulation bandwidth. In contrast to the compared transmitters, the FDDAC-based transmitter integrates the complete DSP on the same chip using a relatively larger technology node while allowing the highest modulation bandwidth. The conventional transmitters based on various architectures, as shown in the table, require a dedicated DSP unit in order to process the baseband signal in terms of oversampling, filtering, and spectral shaping. In [12, 13], externally preprocessed baseband signals are used, whereas in [8] an additional baseband-IC is implemented. In [7], an FIR filter with a relatively low number of taps is integrated which allows limited band shaping

capabilities. This is due to the high sampling rate that is required in conventional transmitters. The FDDAC technique, compared to the competitors, is able to generate a wide modulation bandwidth of up to 2 GHz including spectral shaping with an overall sampling rate that equals to a fraction of the bandwidth, namely 250 MHz. Thus, the complete transmitter can be implemented on the same IC even using a larger technology node. Moreover, the intrinsic spectral shaping capability of the proposed and demonstrated data conversion technique allows to comply with the spectral mask intended for a single-carrier modulation bandwidth of 1.76 GHz. This is a 13.7 % higher spectral efficiency than stated in the WiGig standard. The power consumption of the FDDAC-based transmitter is continuously decreased over the design iterations. In the FBM, the *FDDAC_TX2* requires 75 pJ per bit including the DSP. The required chip area including the frequency synthesisers and DSP is less than 3.6 mm^2.

7.6 Conclusion

The *FDDAC_TX2* significantly improves the transmitter performance in terms of output power, signal quality, and added functionalities. Especially, the included conventional transmitter mode stresses on the flexibility of the FDDAC approach which enables a true multistandard transmitter. It is demonstrated that various modulation bandwidths in a wide frequency range can be transmitted simultaneously. Moreover, the performance in the FDDAC mode is notably improved achieving a minimum EVM of 7%. A raw data rate of up to 8 Gbit/s has been measured, whereas the integrated DSP is capable of processing a data rate of up to 12 Gbit/s. The updated I/Q transmit cores which are based on power efficient DACs and mixers instead of RF-DACs improve the power efficiency by a factor of 2 while generating 18 dB higher output power. The presented FDDAC-based transmitter is able to replicate multiple conventional transmitters or generate a wide coherent modulation bandwidth in the sub-6 GHz range. The output of the presented IC can either be transmitted directly or upconverted to mmW frequencies since a modulation bandwidth in the gigahertz range can only be reserved at higher carrier frequencies. The transmitter prototype presented in Chapter 3 utilises the sub-6 GHz FDDAC IC in a heterodyne structure with mmW upconversion mixers which are analysed and implemented as presented in Chapter 8.

	This work						
Metric	FDDAC_TX1	FDDAC_TX1.5	FDDAC_TX2	ISSCC'17[12]	ISSCC'19[7]	JSSCC'18[13]	JSSCC'14[8]
CMOS techn.	65nm			28nm	28nm	28nm	40nm LP
TX-archi.	FD-DAC based high-IF output			Multilevel Outphasing	Digital Polar	Digital Polar	Heter. I/Q transmitter
DSP on-chip	**yes**			no	4-tap FIR spectral shaping	no	no - separate BB-IC and RF-IC (Coax. interf.)
Spectral shaping	**yes intrinsically**			yes / preprocessed	no	no	yes
ON-chip LO synthesis	**yes**			no	no	no	yes
Modulation	QPSK	QPSK, 16QAM	QPSK, 16QAM, 64QAM	64QAM	16QAM	QPSK	64QAM
Calibration	no		Output trim cap.	no	no	yes	yes
Modulated bandwidth / signal type	single-carrier 1 GHz	single-carrier / 1 GHz, 2 GHz	single-carrier / 1 GHz, 2 GHz, 16x31.25 MHz	400 MHz (20x20 MHz bands)	2x1.76 GHz single carrier (H/V polarity)	single-carrier/ up to 5 GHz	1.76 GHz/ single-carrier
$f_{sampling}$ (GHz)	**0.25**			1.8	7.04	up to 5	2.64
P_{DC}*** (mW)	HBM: 1100*	HBM: 530, FBM:846	HBM: **331**, FBM: **601**	670	272	210	1190 (RF-IC only)
P_{DC} including LO-Synthesis (mW)	HBM: 1996	HBM: 882, FBM: 1721	HBM: 771, FBM: 1616	-	-	-	-
Area (mm^2)	1.34 (active area)		3.6 (including pads)	2.2	3.24	3.9**	BB-IC: 6.82**, RF-IC: 26.32**
EVM no equ. / equ. (%)	BW 1 GHz: 29.7/-	BW 1 GHz: 18.6/13.6 BW 2 GHz: 24.9/17.7	BW 16x31.25 MHz: **3.19/2.3** BW 1 GHz: **13.2/7.2** BW 2 GHz: **18.9/11.8**	3.6/- (BW = 20 MHz)	8.6/-	23.7/-	7.1/-
Output frequency (GHz)	3.8-5.8	2.9375-4.8125 (with mixers: 22-30 and 50-67)		0.35 - 2.6	60.48 - 64.8	56-64	57.4-65.7

*: without PPLs, DSP, PRBS. **:RX and TX, ***: including DSP, HBM: Half bandwidth mode (1 GHz), FBM: Full bandwidth mode, (2 GHz).

Table 7.4: Comparison of the proposed FDDAC-based transmitter with recently reported wireless transmitters.

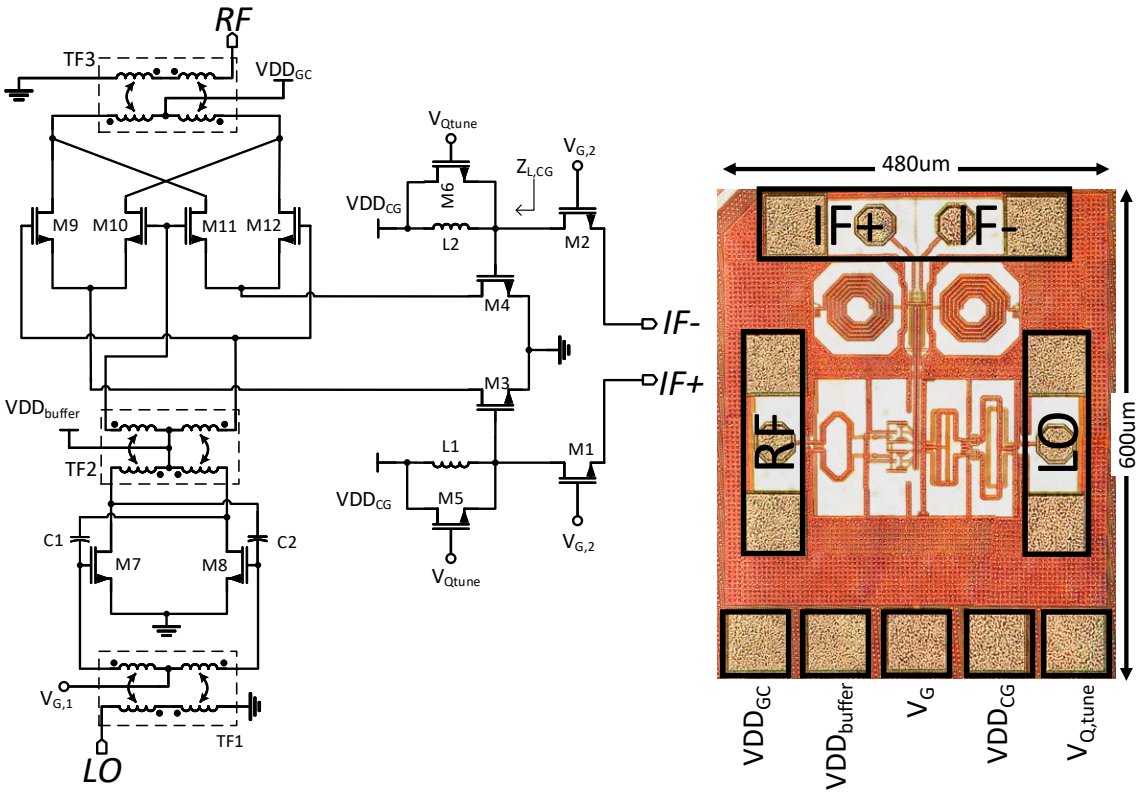
Chapter 8

Integrated mmW upconversion mixer in CMOS

This thesis introduces a new data conversion technique, namely the Fourier-domain data converters. A transmitter prototype based on the FDDAC approach is presented. It utilises a heterodyne architecture, where an FDDAC-based transmitter generates a large modulation bandwidth in the sub-6 GHz frequency range. At this frequency range, the large modulation bandwidth can be used to output multiple narrowband signals or alternatively the I/Q transmit cores can be utilised in the conventional transmit mode. However, a large modulation bandwidth, *i.e.* dedicated spectrum, is only available at high transmit frequencies. This chapter is about the implementation of two mmW upconversion circuits which are used to shift the modulated output of the presented transmitters to 5G 28 and 60 GHz ISM bands. The upconverters are implemented in the same CMOS process to allow the cointegration with the FDDAC-based transmitter alongside the DSP and frequency synthesisers in future design iterations.

8.1 Integration of mmW upconversion circuits

Currently, 5G standards utilise communication in the already congested sub-6 GHz range to ensure rural coverage at reduced bandwidths and the millimetre-wave (mmW) range around 28 GHz for urban high data rate communication [44, 45]. Additionally, the unlicensed ISM band at 60 GHz provides a wide bandwidth which can be used in order to overcome the capacity restrictions of the 28 GHz band. The FDDAC-based transmitter prototype presented in Fig. 3.15 in Section 3.2 contains upconversion circuits for 28 GHz and 60 GHz bands.



(a) Schematic of the CMOS IF-to-mmW upconverter with integrated LO-Buffer, RF, and LO baluns.

(b) Chipmicrograph of the fabricated mixer.

Figure 8.1: Integrated 60 GHz upconversion mixer.

The output of the FDDAC-based transmitter, considered as IF, is directly fed to a mixer's input which needs to provide a suitable input impedance and good matching at least up to the 3rd harmonic since the input impedance directly effects the linearity of the RF-DACs and the output amplifier buffers [101]. Furthermore, the upconversion circuits shall provide sufficient IF-bandwidth in the range of several gigahertz [47] and the RF output is required to cover the complete 60 GHz ISM/WiGig (IEEE802.11ad)

bands from 57 GHz to 66 GHz as well as the 5G frequencies between 25 GHz and 29 GHz. The conversion gain is one of the most important properties, especially, when the output is in the mmW-range. A high conversion gain relaxes both the constraints on the preceding transmitter and on the following PA stages. The degree of integration of the complete transmitter needs to be as high as possible in order to reduce the production cost. Thereby, the feasibility of high performance and chip-area-efficient standard CMOS upconverters is essential such that they can be cointegrated with the complete transmitter.
The Gilbert-cell is a popular mixer topology where both the IF and LO signals are fed to the gates of common-source transistors or Gilbert-quad transistors. In [102], the IF input is directly fed to the gates of the common-source stage and, hence, the input matching is provided for low fractional bandwidth. In terms of broadband matching, especially in this particular case where the IF input is centred at 4 GHz to 5 GHz and shall be matched up to the 3^{rd} harmonic, it is not beneficial to feed the signals to the gates. To overcome the bandwidth limitation, [103] introduces a resistive feedback input stage which, in turn, leads to a trade-off between conversion gain and the input impedance. In [104], a SiGe process is used to achieve outstanding conversion gain at high output power. Nevertheless, the adoption of a SiGe process increases the production cost significantly for high volume applications.

8.2 Integrated 60 GHz upconversion mixer

The proposed mixer uses a common-gate IF input stage to enable broadband impedance matching from DC up to 18 GHz. The common-gate stage is connected via quality-tuned inductive peaking to the common-source transistors of the Gilbert-cell as shown in Fig. 8.1a. The quality-tuning is used to control the gain versus the 3-dB IF-bandwidth. Moreover, the transformer based LO- and RF-baluns are integrated on-chip to improve the impedance matching. The measured performance of the mixer reveals an outstanding conversion gain up to 17.6 dB for a standard CMOS upconversion circuit with reasonable LO pumping power in the mmW-range, together with a broadband IF input matching while retaining the required operation bandwidth.

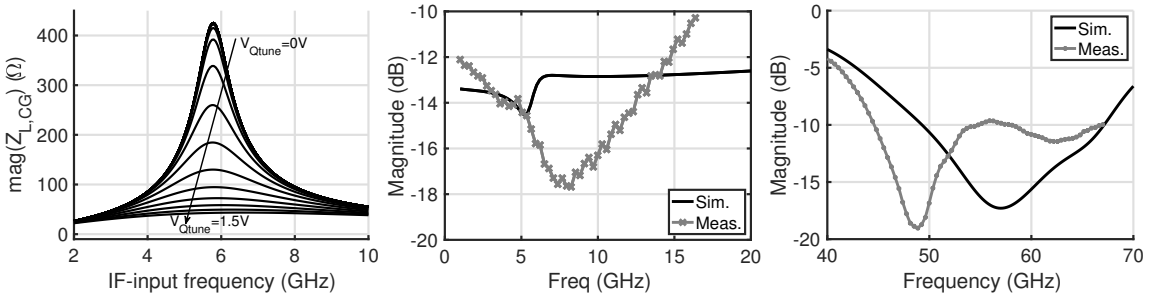
8.2.1 Gain-bandwidth tuning and input stage

The common-gate stage at the IF input provides a precisely controllable broadband matching due to its input impedance dominated by $1/g_m$. The pseudodifferential common-gate stage does not deliver any current gain. Thus, it is used as impedance

transformer establishing a voltage gain. The load impedance, $Z_{L,CG}$, seen by the common-gate stage is set by the LC shunt resonance formed by the gate capacitance of the transistors, $M2$ or $M3$, and the shunt inductances, $L1$ or $L2$. Considering $M5$ and $M6$ as controllable resistances, the quality factor of the inductances and, hence, the bandwidth of the resonators are tunable. The increased bandwidth goes along with a reduced magnitude of the resonator impedance. In combination with the impedance transforming common-gate stage, the bandwidth extension results in a lower voltage gain. Fig. 8.2a shows the magnitude of $Z_{L,CG}$ at different tuning voltages based on EM-simulated passives and routing. The transistors $M5$ and $M6$ are reverse biased for $\mathrm{V}_{Qtune} = 0\,\mathrm{V}$. Their drain and source terminals are DC-wise shorted and connected to the voltage VDD_{CG}. Thus, the original quality factor of the resonator is not significantly reduced. The supply voltage, VDD_{CG}, of the common-gate stage sets the operating point of the common-source transistors, M3 and M4, while, the gate voltage $V_{G,2}$ of the common-gate transistors, M1 and M2, is derived from the input bias V_G.

8.2.2 Inductive-coupled transformers and LO-buffer

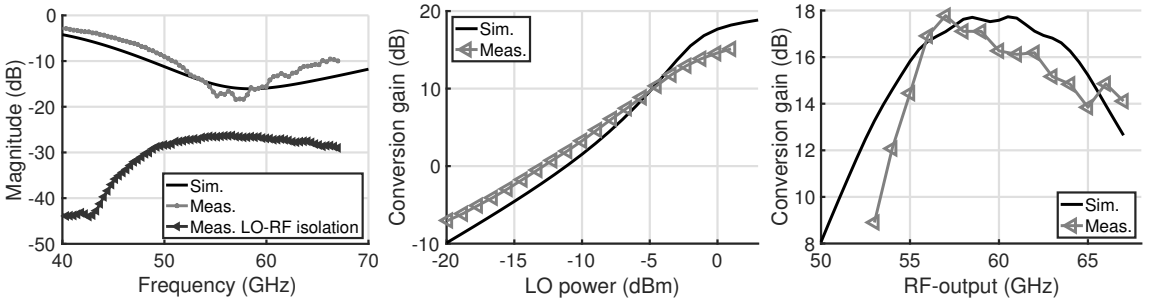
The complete design integrates three stacked centre-tapped low-k inductive transformers of which $TF1$ and $TF3$ serve as baluns, as shown in Fig. 8.1a. The output transformer is designed to transform the 50Ω load to a high impedance so that the Gilbert-quad can generate the desired output voltage swing. Beside the physical dimensions of the transformers, an additional capacitance is added in shunt to the RF output and LO input pads introducing an additional design parameter to improve the matching bandwidth. Both baluns are implemented with respect to minimising the phase and amplitude deviations in order to improve the isolation between the ports.
The integrated LO-buffer is a differential transformer based amplifier. The input and output matching of the LO-buffer is employed by low-k transformers with high aspects ratios in order to reduce the occupied chip-area. The supply voltage of the buffer, VDD_{buffer}, is reused to set the DC-level of the amplified LO signal. Moreover, the transistor size of the LO-buffer is chosen similar to the Gilbert-quad to keep the impedance transformation ratio low with the intention to reduce losses in the interstage matching. The DC point of the buffer is set by $V_{G,1}$ which is derived from the input bias voltage V_G. Cross-coupled neutralisation capacitors, $C1$ and $C2$, are added to the LO-buffer to maximize its gain. The simulated peak gain is +7 dB at 55 GHz LO.



(a) Simulated magnitude of $Z_{L,CG}$ for varying tuning voltages.

(b) Reflection coefficient of the differential IF input.

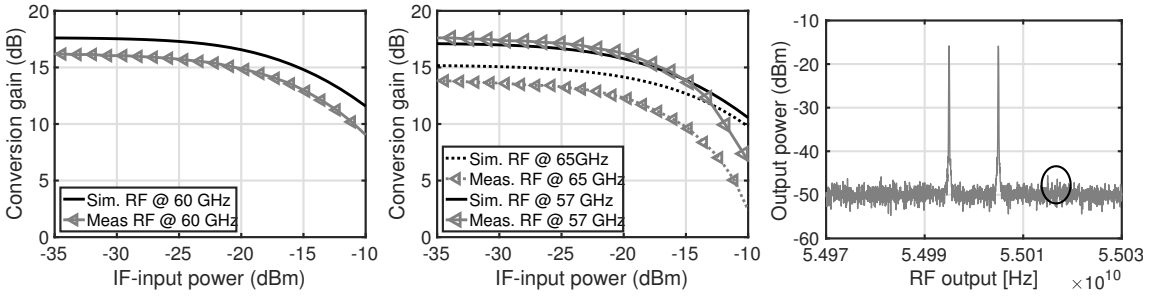
(c) Return loss at the LO input port.



(d) Return loss of RF and isolation LO to RF.

(e) Conv. gain vs. LO power @55 GHz.

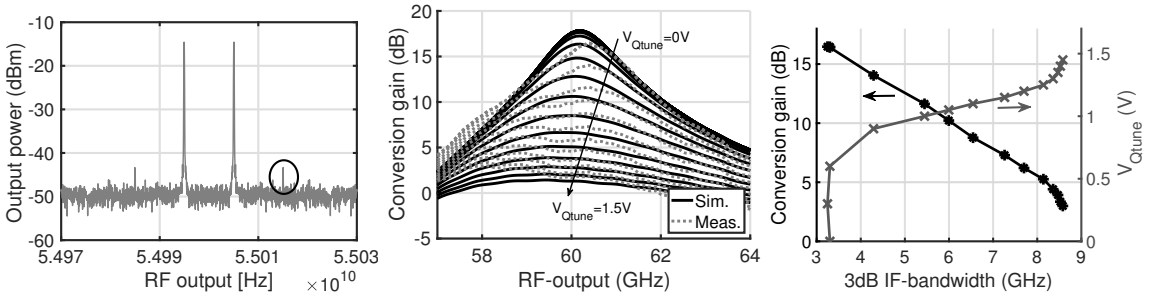
(f) Conv. gain vs.LO-frequency @1 dBm.



(g) CG over IF pow. sweep for LO @ 55 GHz.

(h) CG over IF pow. sweep for LO @ 52 and 60 GHz.

(i) RF-spectrum of the two-tone meas. P_{in}= -27 dBm.



(j) RF-spectrum of the two-tone meas. P_{in}= -26 dBm.

(k) CG over IF tuning, LO @ 55 GHz.

(l) Max. CG vs. 3-dB IF-bandwidth over tuning.

Figure 8.2: Simulation and measurement results of the 60 GHz upconversion mixer.

8.2.3 Measurement results

The circuit characterisation is carried out on-wafer up to 67 GHz using *Keysight's PNA-X* network analyser. The LO input and the RF output are connected via Ground-Signal-Ground (GSG) probing pads, as shown in Fig. 8.1b. A differential GSSG probing pad is used for the IF connection which is generated by the PNA-X in a single-ended manner and fed through an external 180°-hybrid with an operating frequency range from 1 GHz to 18 GHz. Fig. 8.2b shows the reflection coefficient of the differential IF input. The simulated magnitude of the insertion loss is below -12 dB up to 30 GHz. The measured reflection coefficient is characterised up to 18 GHz and it is below -10 dB, which is limited by the used external balun.
Fig. 8.2c and 8.2d present the measured and simulated reflection coefficients at the LO input, the RF output ports, and the isolation between LO- and RF-ports. The integrated LO-balun and the LO-buffer are designed to provide best matching at 55 GHz. The measured reflection coefficient shows a minor shift to lower frequencies due to the increased shunt capacitance in the tolerable region of process variation. Nevertheless, the frequency range from 45 GHz to 67 GHz serves good matching with a return loss better than 9.8 dB. The mixer's output is matched to 50 Ω in order to provide maximum power transfer to the load. The measurement results show a good agreement with the simulated reflection coefficients where the -10 dB bandwidth spans between 50 GHz-70 GHz simulated and 52 GHz-67 GHz measured, respectively.
The isolation between the LO- and RF-port is measured to be better than 26 dB in the band of interest, although the LO-buffer is active and provides gain. Fig. 8.2e shows the dependency of the conversion gain on LO power. The maximum LO power that can be delivered to the mixer up to 62 GHz is +1 dBm. Fig. 8.2f shows the conversion gain for different LO frequencies at a fixed LO power of 0 dBm resulting in different RF. The maximum conversion gain of 17.6 dB is measured at an LO frequency of 52 GHz, a single-tone IF input at 5 GHz with a power level of -30 dBm, and 57 GHz RF output. The frequency shift in the LO input reflection coefficient, as shown in Fig. 8.2c, leads to a stronger power transfer at the lower LO frequencies which translates to a higher conversion gain at lower frequencies, as shown in Fig. 8.2f. Nevertheless, the experimentally verified 3-dB bandwidth is 55 GHz-64.5 GHz, whereas the bandwidth for where the conversion gain is above 10 dB can be given as 52.5 GHz-67 GHz which fully covers the targeted ISM/WiGiG bands.
The input-referred 1-dB compression point (P_{1dB}) is verified for different RF frequencies. As shown in Fig. 8.2g and Fig. 8.2h, the measured input referred P_{1dB} is -20.5 dBm. At the P_{1dB} point, the RF output power at 57 GHz is -2.9 dBm, whereas the saturated output power is slightly lower than -1 dBm.
The input-referred 3^{rd} order Input Intercept Point (IIP) is measured by using an external 50 GHz source with a limited maximum output power since the two internal sources of the *PNA-X* are combined in order to generate the two-tone IF input with a

Ref.	Process	CG (dB)	f_{IF} BW (GHz)	P_{LO} (dBm)	P_{DC} (mW)	P_{1dB} outp. ref. (dBm)	Area (mm^2)
[102]	90 nm CMOS	-8	18-22	3	11	-19	0.45
[103]	65 nm CMOS	6.2	3-9.5	0	17.8	-5.8	0.41
[104]	180 nm SiGe	27	DC-10	n/a	495	+13	1.12
[105]	130 nm SiGe	-2.5	n/a	0	27	n/a	0.22
[106]	90 nm CMOS	0.78	DC-3.8	5	44.3	-11.7	0.74
[107]	90 nm CMOS	6	DC-1.4	n/a	12.1	n/a	0.52
This work	65 nm CMOS	**17.6**	**3.5-6.7** to **0.9-9**	0	w/o LO-buf.: 47.92, tot.:98.46	**-2.9**	**0.288**

Table 8.1: Comparison table of recently reported 60 GHz upconversion mixers.

frequency offset of 10 MHz. Fig. 8.2i and Fig. 8.2j show the output spectra at different input power levels, *i.e.* -27 dBm and -26 dBm. In theory, the IIP3 should be measured for input power levels much smaller than the P_{1dB}. However, due to the noise floor of the measured spectra, the intermodulation products become reliably detectable at the given input power levels. By extrapolation, the IIP3 is calculated as -12 dBm, whereas, in this particular case, the gain is +14.2 dB and the input referred P_{1dB} is -21 dBm which matches well with the simulation.
The IF-bandwidth and the maximum achievable conversion gain are tuned by the variable quality factor of the inductive peaking stage in the interstage. The voltage, V_{Qtune}, is varied from 0 to 1.5 V and the conversion gain over the RF is plotted in Fig. 8.2k. Here, the LO frequency is kept constant at 55 GHz and the IF is swept. The resulting RF varies with the swept IF. The centre frequency of the IF band is simulated and designed to be slightly above 5 GHz. As designed and simulated, the measured curves depict the maximum gain at 5.5 GHz IF which translates into 60.5 GHz RF output. Fig. 8.2l shows the compiled measurement results illustrating the trade-off between conversion gain and achievable IF-bandwidth which can be tuned linearly for different control voltages, V_{Qtune}.
The comparison to state-of-the-art mixer circuits given in Table 8.1 shows that the proposed design exhibits excellent conversion gain, even though introducing a tunable and wide IF-bandwidth for standard CMOS. A similar conversion gain is achieved by employing processes like SiGe combined with additional amplification stages which

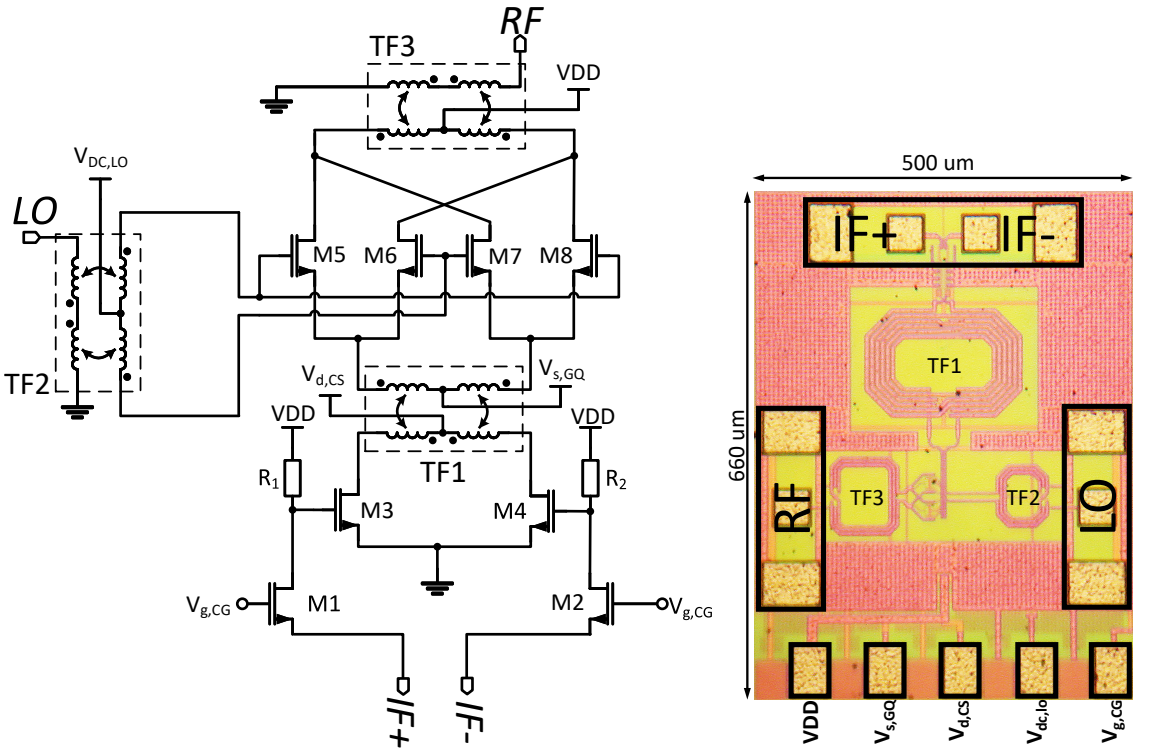
leads to a significantly increased power consumption [104]. Furthermore, the occupied die area is the smallest while including the LO- and RF-baluns, the LO-buffer, pads, and tuneability.

8.2.4 Discussion

A flexible, compact, high variable-gain, and variable-bandwidth IF-to-mmW mixer in a 65 nm standard CMOS technology is implemented. The occupied die size is 0.28 mm^2 including the LO-buffer and baluns which makes the proposed mixer a promising candidate for fully integrated multistandard transmitters in standard CMOS. The integrated LO-buffer accomplishes high conversion gain at reasonable LO input drive levels. The conversion gain versus bandwidth tuning can be controlled digitally in further integration. The ability to integrate the IF-to-mmW mixer along with the baseband signal processing and the FDDAC-based transmitter on the same chip omits the necessity of implementing circuits on special materials. Hence, the production cost and complexity of mobile communication devices can be reduced significantly. Furthermore, the IF and RF bandwidth of the proposed mixer is fully compliant with the 60 GHz ISM/WiGig bands.

8.3 Integrated 28 GHz upconversion mixer

Fig. 8.3a shows the schematic of the proposed 28 GHz upconversion mixer. The transistors M1 and M2 form the common-gate IF input stage and matching as in the 60 GHz mixer. The DC voltage gain of this stage is defined by the selection of resistances, R1 and R2, and the input impedance. R1 and R2 are 322 Ω, thus, the common-gate stage is used as impedance transformer with voltage gain. The amplified input voltage is applied to the gate of the common-source transistors, M3 and M4. The supply voltage, VDD, of the input stage is connected via the resistors and it also sets the bias voltage of the common-source transistors considering the DC current taken by the transistors M1 and M2. The resistors and the gate capacitances of M3 and M4 at the node V_1 form a lowpass filter which leads to a frequency dependency of the voltage gain of the input stage. Although, the input matching can be achieved for a large bandwidth, the voltage gain from IF input to the gate of the common-source stage shows a decay for increasing frequency. In order to achieve a high overall conversion gain, the values of both the resistances R1 and R2 and g_m of the common-source stage are increased which comes along with an excess of gate capacitance. There is a trade-off which reduces the cut-off frequency and the usable IF bandwidth if the conversion gain



(a) Schematic of the proposed CMOS IF-to-mmW upconverter with integrated RF and LO baluns.

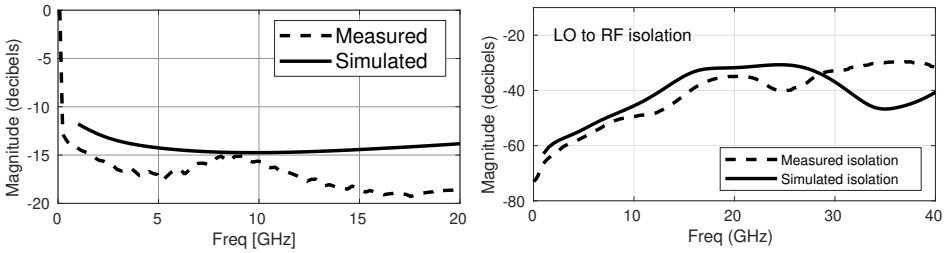
(b) Chipmicrograph of the fabricated mixer.

Figure 8.3: Integrated 28 GHz upconversion mixer.

shall be maximised. In order to overcome this trade-off, a series inductance is added to the drain of the common-source transistors, namely M3 and M4. By proper sizing of the series inductor, the common-source stage is resonated at a frequency above the 3 dB point of the lowpass filter at node V_1. Subsequently, the amplitude decay is compensated widening the IF bandwidth. The series inductor is realised by the transformer TF1. By setting the primary and secondary inductances and the coupling factor, an equivalent series inductance can be realised which is used for the peaking. This transformer also isolates the bias points of the common-source transistors and the Gilbert quad in order to achieve transistor stacking which are DC-wise not connected. Accordingly, the supply voltage can be set to 1.2 V and yet a high overdrive voltage for the stacked transistors can be maintained without limiting the output swing. The upconversion mixer is designed to output the LSB mixing product. The complete design integrates three stacked centre-tapped low-k inductive transformers of which $TF2$ and $TF3$ serve as baluns. Both baluns are implemented with respect to minimise the phase and amplitude deviations in order to improve the isolation between the ports.

8.3.1 Measurement results

The circuit characterisation is carried out on-wafer up to 40 GHz using *Keysight's PNA-X* network analyser. The LO input and the RF output are connected via GSG probing pads, as shown in Fig. 8.3b. A differential GSG probing pad is used for the IF connection which is generated by the PNA-X in a single-ended manner and fed through an external 180°-hybrid. The frequency range of the utilised hybrid is between 1 GHz to 18 GHz. Fig. 8.4a shows the reflection coefficient of the differential IF input. The simulated magnitude of the insertion loss is below -12 dB up to 30 GHz. The measured reflection coefficient is characterised up to 18 GHz and it is below -10 dB.

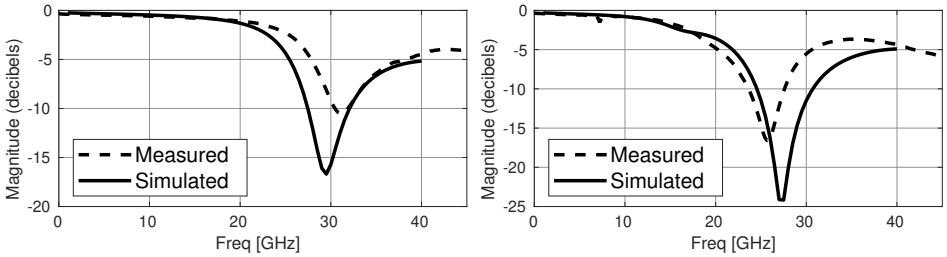


(a) Magnitude of the IF input reflection coefficient.

(b) Isolation between the LO input and RF output ports.

Figure 8.4: Meas. and sim. magnitude of the IF input reflection coefficient and the isolation between the LO input and RF output ports.

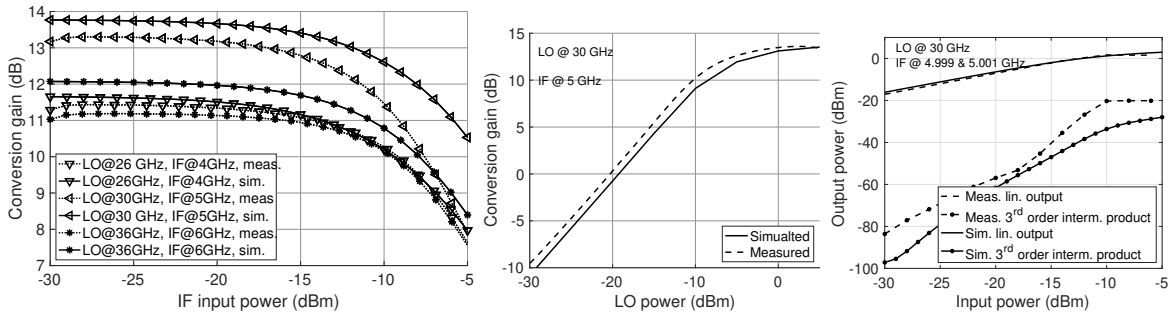
Fig. 8.4b illustrates the measured and simulated LO-to-RF isolation which is better than 30 dB. The reflection loss of the LO and RF ports are shown in Fig. 8.5. Besides the slight frequency shift, the measured curves match the simulation. Fig. 8.6a and 8.6b shows the measured CG over IF and LO power. The highest measured conversion gain is 13.8 dB. The IF input referred 1 dB compression point is at −12 dBm. A two tone measurement could be performed at the given frequencies. Fig. 8.6c shows the simulated and measured linear and third-order intermodulation product at the output



(a) LO input.

(b) RF output.

Figure 8.5: Meas. and sim. reflection coefficients of the LO input and RF output.



(a) CG vs. IF input power. (b) CG vs. LO power. (c) Third-order intermodulation.

Figure 8.6: Meas. and sim. CG vs. IF input power, CG vs. LO power, and two-tone analysis based linear output power vs. third-order intermodulation.

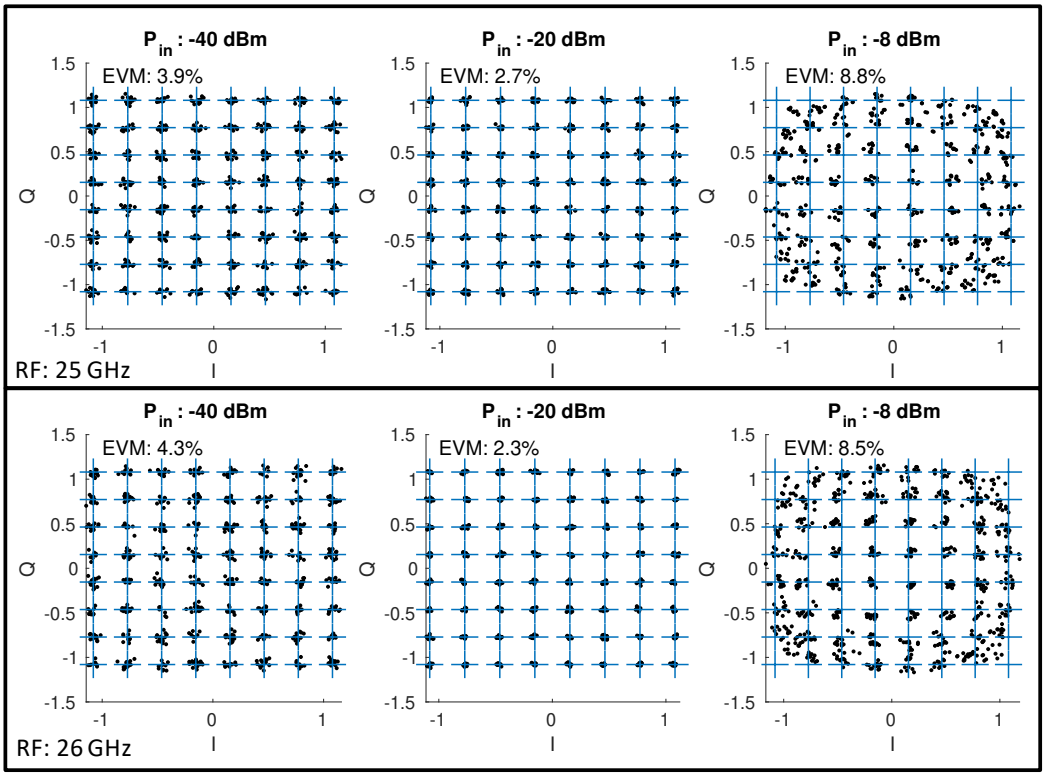


Figure 8.7: Measured constellation diagram for a 64QAM signal upconverted from 5 GHz to 25 GHz and 26 GHz at different input IF power levels.

of the mixer. The IIP3 point can be given as approximately 0 dBm.
In addition to the *S*-parameter measurements, a modulated IF signal is fed to the mixer which is upconverted to the mmW frequencies. The output of the mixer is demodulated by the VSA tool of the *Rohde und Schwarz FSW26* in order to characterise the EVM

performance. However, the maximum frequency which can be measured is limited by the utilised VSA to 26.5 GHz. Nevertheless, a 64QAM signal at a maximum bandwidth of 50 MHz is generated by a vector signal generator at 5 GHz carrier frequency. The LO is set to 30 GHz or 31 GHz which, in turn, leads to an RF of 25 GHz or 26 GHz, respectively. Fig. 8.7 shows the demodulated constellation diagrams for various input power levels. The upper row depicts the demodulated constellation diagram of the RF signal at 25 GHz and the lower row shows the demodulated constellation diagrams of the RF signal at 26 GHz. The best measured EVM is 2.3 %. Note that −8 dBm average input power which is above the 1-dB compression point leads to a deteriorated EVM. Furthermore, the mixer is used to upconvert the output of the hybrid FDDAC which is capable to generate a modulation bandwidth of up to 100 MHz. The measurement results are presented in Chapter 4.

8.3.2 Measurements with the *FDDAC_TX2* IC

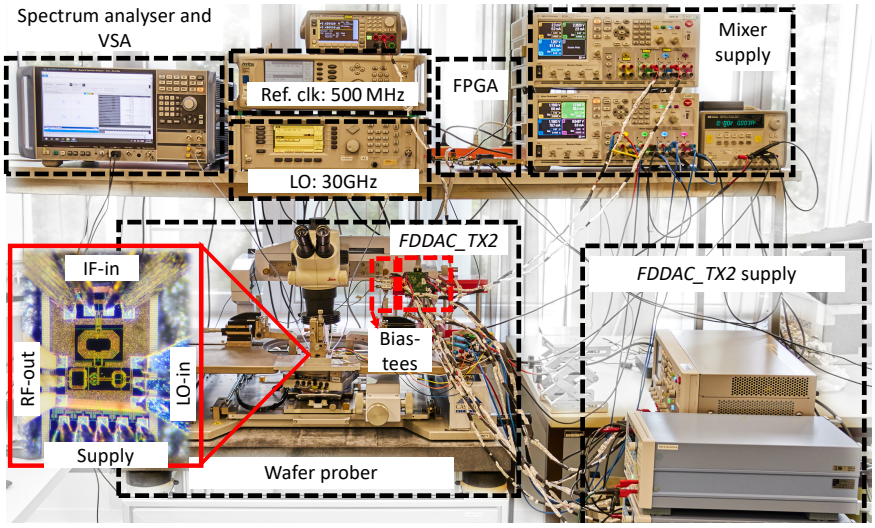


Figure 8.8: Photograph of the setup with the *FDDAC_TX2* and the 28 GHz mixer.

For the measurement of the *FDDAC_TX2*, a signal and spectrum analyser, namely the *Rohde und Schwarz FSW44*, have been employed. As mentioned in Chapter 7, this device provides an VSA bandwidth of up to 4 GHz at carrier frequencies of up to 44 GHz. Fig. 8.8 shows the measurement setup which allows the combined measurement of the FDDAC-based transmitter with the 28 GHz upconversion mixer. It contains two synchronised reference oscillators, the VSA tool, the FPGA-board, and the supply and current sources for both ICs which have been placed around the wafer prober in order to keep the cable lengths short. Fig. 8.9 depicts the block diagram of the measured ICs. The differential output of the transmitter IC is connected via two biatees to the

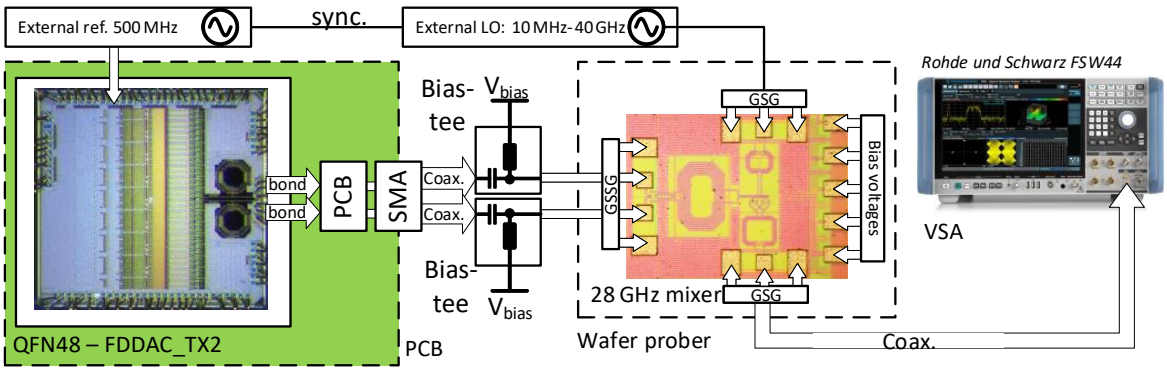
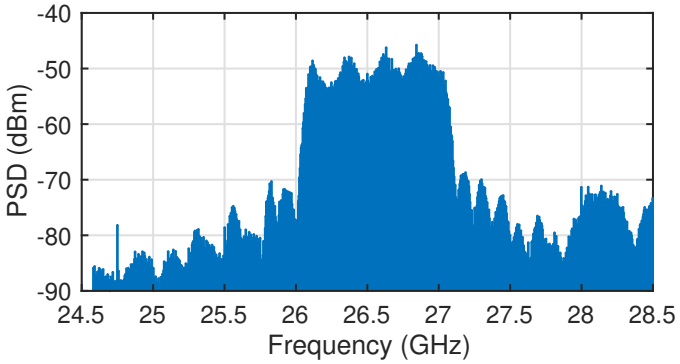
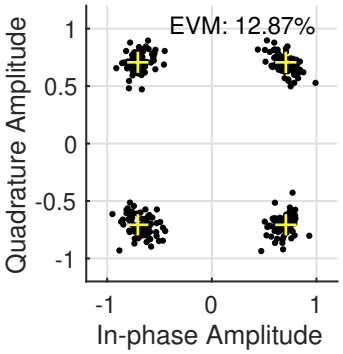


Figure 8.9: Meas. setup of the *FDDAC_TX2* with the 28 GHz upconversion mixer.

differential input of the upconversion mixer IC. The bias-tees are required to set the correct input common-mode voltage of the mixer which is placed in a wafer prober. Fig. 8.10a presents the PSD of the modulated signal after upconversion. In this case, the FDDAC-based transmitters output is considered as a high IF at 3.4375 GHz. The LO of the mixer is set to 30 GHz which, in turn, results in an output frequency of 25.5625 GHz at the output of the mixer. The balun is integrated within the upconversion circuit which leads to a single-ended output that is connected to the VSA.



(a) PSD, $f_{carrier}$ =26.5625 GHz.



(b) Constellation diagram.

Figure 8.10: Measured PSD and constellation diagram of the QPSK modulated signal with a modulation bandwidth of 1 GHz generated by the *FDDAC_TX2* at an IF of 3.4375 GHz and upconverted to 26.5625 GHz.

The measured PSD contains an amplitude ripple which is caused by the used coaxial cables and bias-tees used in the differential interface between both ICs which are neither identical nor matched well. Therefore, the constellation is measured with the integrated equaliser in the VSA-tool. Fig. 8.10b shows the achieved results at the output of the upconversion mixer.

8.3.3 Discussion

The proposed mixer achieves a comparably high conversion gain of up to 13.3 dB in a standard CMOS technology. Furthermore, it provides a wide IF bandwidth from 2 GHz to 8 GHz. The IF bandwidth extension is achieved by an interstage transformer which additionally isolates the DC operating points in the stacked design. Thus, high overdrive voltages of the stacked transistors can be maintained even in a low-voltage power-efficient CMOS process. The power consumption is 78.5 mW and the total die size is 0.33 mm^2 including LO and RF baluns. Furthermore, the performance of the mixer has been demonstrated with narrowband signals with a modulation bandwidth of up to 50 MHz and wideband FDDAC-signals with a modulation bandwidth of up to 1 GHz. The presented results are promising and the upconversion mixer can be cointegrated with the FDDAC-based transmitters on a single die.

8.4 Conclusion

This chapter introduced two integrated mmW upconversion mixers for the frequencies around 28 GHz for 5G applications and around the 60 GHz ISM band. The measured performance is competitive and demonstrates the feasibility of mmW RF-frontends in the used CMOS technology. With the proposed design techniques, outstanding conversion gain and IF bandwidth can be achieved. The heterodyne transmitter prototype, as shown in Section 3.2, generates the modulated wideband signal in the sub-6 GHz range. Thus, the mixed-signal components operate at low frequencies where the utilised technology allows rail-to-rail switching. Furthermore, the wide modulation bandwidth can be used to simultaneously transmit multiple narrowband signals in the sub-6 GHz range, whereas the output frequency shall be upconverted to the mmW frequencies in order to allocate a large modulation bandwidth. The upconversion mixers are specifically designed to be integrated with the FDDAC-based transmitters in a next iteration. Thus, the IF bandwidth and power as well as the differential inputs are matched to the output of the FDDAC-based transmitter. This has been demonstrated by combined measurements, where the implemented upconversion mixer is utilised to process the output signal of the FDDAC-based transmitter IC. Consequently, the complete transmitter chain for a modulation bandwidth of up to 2 GHz including the digital modulation of raw data, DSP and spectral shaping, DACs, I/Q modulators in the sub-6 GHz range, phasor tone generation, and the mmW frontends have been demonstrated in this thesis and can be cointegrated in 65 nm CMOS technology on the same IC. Thus, the transmit frequency of the proposed transmitter can be set to sub-6 GHz frequency range, 5G frequencies around 28 GHz, and 60 ISM band.

Chapter 9

Conclusion and Outlook

9.1 Conclusion

This thesis introduces the Fourier-domain data conversion technique which completely changes the transmitter chain. Thereby, the utilised components are moved away from the technological and physical boundaries. This leads to an enormous boost in achievable data rates and modulation bandwidths compared to state-of-the-transmitter topologies operating at the same technological boundaries while simplifying the complete transmitter system extensively.
The proposed technique is analysed mathematically and a transmitter prototype is developed as well as modelled at system-level in order to investigate the advantages and challenges of the new approach. The main advantages of the FDDAC technique are its intrinsic spectral shaping capabilities and the reduced sampling rate in the entire system. The modelled prototype is used to explore the design space and investigate the utilised subblocks in terms of their specifications and the effect of nonidealities on

the complete transmitter performance. It is further used to formulate various sets of subblock specifications in order to achieve a competitive performance.
A first hybrid prototype based on commercially available off-the-shelf components employing the new approach is implemented and a modulation bandwidth of up to 100 MHz with 16QAM is demonstrated. Due to the architectural benefits of the approach the complete transmitter for a modulation bandwidth as high as 2 GHz has been integrated in a single IC including the DSP and analogue-mixed-signal components in a well established commercially available 65 nm CMOS technology. Fig. 9.1 shows the measured data rates of the three different ICs and the hybrid implementation as well as the obtained total power consumptions:
The *FDDAC_TX1* is the first integrated transmitter employing the new technique. It contains 16 I/Q transmit cores based on RF-DACs, the entire frequency synthesis blocks for 16 equidistantly spaced phasor tones, and the complete DSP unit. This transmitter has been fully characterised by measurements and achieves a modulation bandwidth of up to 1 GHz in the HBM with QPSK which results in a raw data rate of 2 Gbit/s.
The *FDDAC_TX1.5* introduces improved frequency synthesisers for the phasor tone generation. The power consumption of the transmitter IC including the frequency synthesisers could be reduced while operating in the FBM with double the modulation bandwidth, namely 2 GHz, and QPSK which results in 4 Gbit/s of raw data rate. However, the transmitter has also been demonstrated to achieve 4 Gbit/s in the HBM with 16QAM and 1 GHz modulation bandwidth.
Finally, the *FDDAC_TX2* introduces an architectural change in the I/Q transmit cores adapting extremely power-efficient I/Q DACs, passive mixers, and amplifier buffers. Thereby, the power consumption of the complete IC could further be reduced while increasing the resolution of the transmitter from 8 to 9 bit, improving the transmitter performance, and increasing the average output power by approximately 18 dB. The *FDDAC_TX2* has been measured in the FBM with a modulation bandwidth of 2 GHz and 16QAM which, in turn, translates to a raw data rate of 8 Gbit/s. However, the integrated DSP provides a maximum modulation order of 64QAM such that the highest possible data rate is 12 Gbit/s. The best achieved EVM is 7%.
The spectral shaping capabilities of the implemented transmitter have been demonstrated by the achieved compliance with the spectral emission mask defined in the physical layer of WiGig for a single-carrier transmission with a modulation bandwidth of 1.76 GHz. The outstanding spectral shaping performance of the FDDAC-based transmitter allows fitting the full 2 GHz single-carrier modulated signal in the given spectral mask which surpasses the bandwidth defined in the standard as well as the targetted spectral efficiency by approximately 13.7%.
In combination with the ability to generate a wide modulation bandwidth that can contain a coherent modulation or a multitude of narrowband signals, the I/Q transmit cores of the FDDAC-based transmitter can be utilised as simultaneously operating conventional transmit chains as well. Therefore, the integrated DSP of the *FDDAC_TX2*

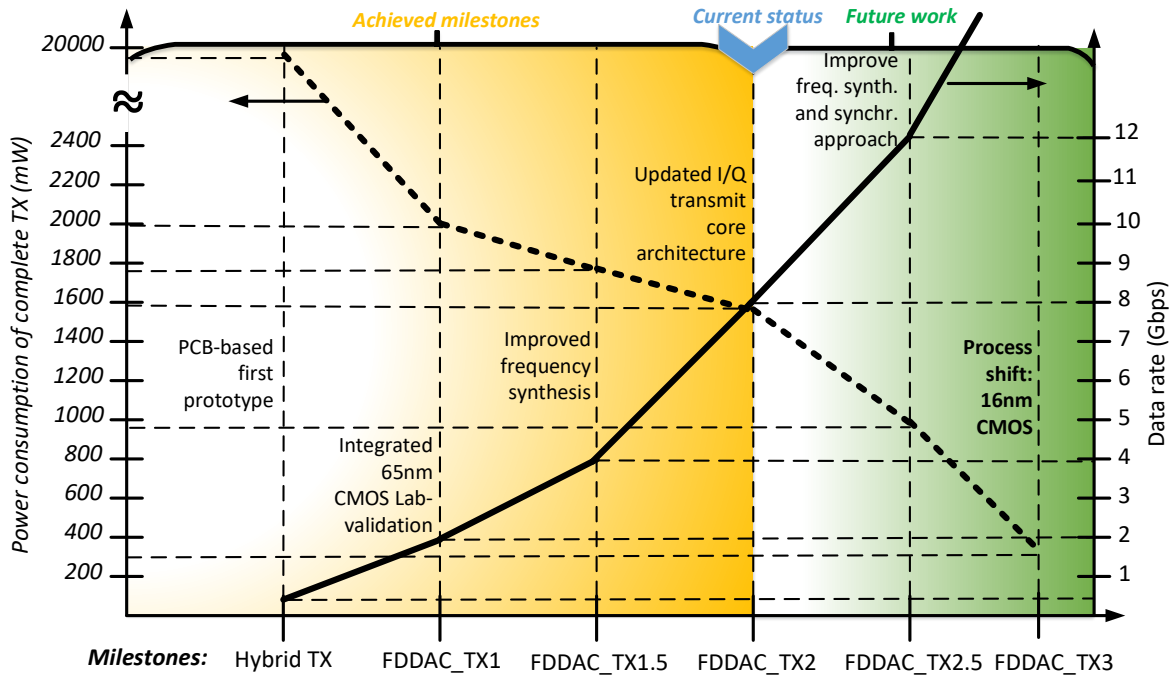


Figure 9.1: Achieved milestones of the thesis and future work showing and predicting the increased data rate over the design iterations while required power is continuously reduced.

supports a conventional transmit mode. Thus, the DSP accommodates a digital modulator, oversampling, and a 64-tap digital complex FIR filter that is used to generate up to 16×31.25 MHz modulated signals simultaneously. The carrier frequencies are defined by the phasor tones of the bins. By tuning the single reference clock of the transmitter IC, the modulation bandwidth is varied between 25 and 56.5 MHz while the carrier frequencies vary in a range between 2.4 to 6.3 GHz. This emphasises the flexibility of the implemented FDDAC topology and demonstrates a true multistandard transmitter.

In addition to the sub-6 GHz transmitters ICs, two mmW upconversion circuits have been implemented in the same CMOS technology, which are specifically designed to upconvert the output of the FDDAC-based transmitter to 5G frequencies around 28 GHz and 60 GHz ISM bands. These upconversion mixers achieve competitive performance in standard CMOS in terms of conversion gain and operation bandwidth as well as fully supporting the 5G mmW frequencies and the complete ISM band at 60 GHz.

In conclusion, this thesis proposed a revolutionary and disruptive approach to break through the limitations of conventional transmitters. The proposed technique is employed in a fully integrated transmitter including the digital modulation of a random bit sequence, digital signal processing as well as the calculation of the Fourier coefficients, the conversion from the digital to the analogue domain by the actual FDDAC,

and finally the upconversion from high IF to mmW frequencies. Consequently, this thesis emphasises on the advantages and capabilities of the proposed approach by demonstrating and achieving the goal of this thesis which is the development of a new type of wireless communication transmitter based on the novel data converter concept that overcomes the limitations of conventional transmitters regardless the utilised technology.
The presented transmitter architecture has the potential to replace a multitude of transmitters in mobile communication devices while allowing substantially higher data rates at significantly reduced power consumption. Thus, the cost and complexity of handheld communication devices can be reduced remarkably by allowing the implementation of true multistandard transmitters. Furthermore, applications which have been depending on wired communications can be implemented wirelessly due to the extreme high data rates that can be delivered with the proposed technique. In general, the developed concept will enable new consumer experience in applications such as wireless virtual reality, beyond 5G wireless communications, and extremely low latency high data rate applications. The demonstrated advances in combination with the presented vision have the potential to form beyond 5G communication standards and change the entire class of mobile communication devices.

9.2 Outlook

The achieved milestones of this thesis, as presented in Fig. 9.1, show the gradually improvements of the FDDAC-based transmitter. Based on the experience, gained during the implementation and characterisation of the transmitter ICs, it becomes clear that the technological limitation of the 65 nm CMOS technology in terms of maximum data rate and power efficiency are not achieved yet. In the following design iteration, digitally assisted tuning and calibration methods, as discussed in Chapter 7, can be implemented in order to remarkably improve the transmitter performance. Furthermore, the frequency synthesis blocks can still be optimised in terms of SFDR and robustness. Therefore, various closed-loop frequency synthesis methods can be investigated which might also deliver directly synchronised phasor tones omitting the necessity of the synchronisation ADDLLs. Thereby, the achievable data rate can be substantially increased while further reducing the power consumption of the complete transmitter. Moreover, the implemented upconversion circuits can be cointegrated with the transmitter enabling a programmable carrier frequency in three different frequency ranges, namely sub-6 GHz, 28 GHz, and 60 GHz. A single mmW PLL should be investigated and integrated on the same IC in order to synthesise the LO of the upconversion mixers. Additionally, a high-speed data interface should be integrated to send raw data to the integrated DSP on the IC. By implementing an industrial

standard as high-speed interface the implemented transmitter can be employed in communication devices. In addition to the improvements in circuit and system-level, the technology can be shifted to a smaller node to significantly boost the data rate and reduce the power consumption of the complete transceiver benefiting from the technology scaling.
As a final step, the FDADC-based receiver, as presented in Chapter 3, shall be investigated thoroughly in order to implement a completely new transceiver type. Thereby, a complete solution for immense high data rate wireless communication with low power consumption can be offered.
The proposed and demonstrated revolutionary data conversion technique is not limited to wireless communication systems. It has the potential to pave the way for the next generation of data communication infrastructure, wired, optical and wireless due to its high scalability and low cost. The FDDAC approach can be implemented in the optical domain, where each bin directly modulates light at different wavelengths at a significantly reduced sampling rate. The complete DSP and the electronic signal fed to the optical modulator can be generated by FDDACs as well which exponentiates the benefits of the introduced approach. Furthermore, the intrinsic spectral shaping feature allows to increase the spectral efficiency in the optical domain as well leading to a tremendous increase in the maximum achievable communication distances. Therefore, the presented data conversion technique will also have a huge impact on the capacity of optical data-transmission systems by making the information communication systems of tomorrow more sustainable and greener.

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Appendix A

Appendix

Curriculum Vitae

Name	Oner Hanay
Academic Degree	Master of Science (M.Sc.)
Date of Birth	26.03.1990
Place of Birth	Adana, Turkey
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Professional Experience

10/2015–today	High Frequency Electronics RWTH Aachen University Aachen, Germany Research Assistant
10/2014–4/2015	NXP Semiconductors Eindhoven, Netherlands CMOS circuit design Intern

Education

2013–2015	RWTH Aachen University Aachen, Germany Electrical and Information Engineering (M.Sc.), grade: 1.0
2010–2013	RWTH Aachen University Aachen, Germany Electrical and Information Engineering (B.Sc.), grade: 2.4
2007–2010	Wirtschaftsschulen des Kreises Steinfurt Steinfurt, Germany Abitur, grade: 1.6

List of Publications

Patents

- **O. Hanay**. „(Ger. Patent) Verfahren zum Umsetzen eines digitalen, komplexen Basisbandsignal in ein HF-Ausgangssignal“. Pat. 2016. URL: https://publications.rwth-aachen.de/record/690825

- **O. Hanay**. „(Ger. Patent) Schaltungsanordnung und Verfahren zur Erzeugung eines hochfrequenten, analogen Sendesignals“. Pat. DE102016102005B4. 2016.

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- G. Wang, G. Ascheid, Y. Wang, **O. Hanay**, R. Negra, M. Herrmann, and N. Wehn. „Optimization of Wireless Transceivers under Processing Energy Constraints“. In: *Frequenz* 71.9-10 (1Sep. 2017), pp. 379 –388. DOI: https://doi.org/10.1515/freq-2017-0150. URL: https://www.degruyter.com/view/journals/freq/71/9-10/article-p379.xml.

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- **O. Hanay** and R. Negra. „Symbolic Top-down Design Methodology of a Quadrature Bandpass Delta Sigma Modulator“. In: *2019 16th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*. 2019, pp. 253–256. DOI:

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- E. Bayram, **O. Hanay**, M. Sayed, and R. Negra. „Fully digital-IF based RF-DAC Transmitter“. In: *2019 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. 2019, pp. 89–92. DOI: 10.1109/PRIME.2019.8787752.

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- L. Frager, **O. Hanay**, E. Bayram, and R. Negra. „13-Bit RF-DAC up to 14GS/s at 3.5 GHz introducing Smart-Switching“. In: *2016 IEEE Nordic Circuits and Systems Conference (NORCAS)*. 2016, pp. 1–4. DOI: 10.1109/NORCHIP.2016.7792899.

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