Tailored Smart Lighting Systems with Energy-Efficient Electronics

Von der Fakultät für Elektrotechnik und Informationstechnik
der Rheinisch-Westfälischen Technischen Hochschule Aachen
zur Erlangung des akademischen Grades eines Doktors
der Ingenieurwissenschaften genehmigte Dissertation

vorgelegt von

Diplom-Ingenieur

Lukas Josef Maria Lohaus

aus Gladbeck

Berichter: Universitätsprofessor Dr.-Ing. Stefan Heinen
Universitätsprofessor Dr.-Ing. Tobias Gemmeke

Tag der mündlichen Prüfung 23.04.2021

Diese Dissertation ist auf den Internetseiten der Universitätsbibliothek online verfügbar.

Es ist nicht genug zu wissen,
man muss auch anwenden.
Es ist nicht genug zu wollen,
man muss auch tun.

Johann Wolfgang von Goethe

Acknowledgment

The six years at the Integrated Analog Circuits and RF Systems (IAS) group of RWTH Aachen University have been a precious time for me – a time of learning and gaining novel scientific insights, but also a time of personal growth, collaboration in a fantastic team and strong relationship building. I would like to sincerely thank all people, who supported and accompanied me on the long journey to the completion of this thesis.

First of all, I thank my academic supervisor Prof. Dr.-Ing. Stefan Heinen for his continuous support and the personal advancement during my doctoral studies. He gave me the opportunity to work on an exciting research topic in an emerging field and promoted to combine scientific progress with practical applicability. Beyond sharing his technical expertise, Prof. Heinen fostered my talents in many ways, e.g. by entrusting me with lecturing as his substitute. I am also grateful for the experiences I gained in project management as well as in the acquisition of research projects. I am glad and proud being a member of his research team.

I would also like to thank Prof. Dr.-Ing. Tobias Gemmeke for his interest in my research and the co-examination of my thesis. He supported me with valuable comments and ideas improving my thesis. I appreciated the fruitful as well as the challenging discussions with him. Moreover, my best thanks go to Prof. Dr.-Ing. Bernhard Hill for the technical discourse on color quality of LED lighting systems. His kind support and sharing his laboratory equipment

enabled the spectral measurements on LED color accuracy presented in this work. Additionally, I would like to express many thanks to Prof. Dr. ir. Dr. h. c. (RTU) Rik W. De Doncker for his friendly assistance and for acting as chairman during my doctoral examination procedure.

A special acknowledgment goes to Dr.-Ing. Ralf Wunderlich, who accompanied me as the IAS' engineer-in-chief on my PhD journey from the very beginning and supported me in an outstanding manner. In particular, I would like to mention the fostering of the HQLED tape-out, which was a great and challenging experience for me. I thank him very much for the great collaboration, his thoughtful advice from time to time as well as for the fruitful discussions.

Many thanks go to the ENIAC Joint Undertaking and the German Federal Ministry of Education and Research (BMBF) for funding my research within the *"EnLight"* projects as well as to all associated project partners. I appreciated the collaboration and interesting exchange of ideas, in particular with Friedhelm Holtz from Insta Elektro GmbH, Lüdenscheid, Germany. I thank him for the close and cordial cooperation, his instructive perspectives that he shared with me as well as for his valuable feedback in the proofreading of this thesis.

I thank all of my former colleagues at the IAS. The time with them has been affected by a great atmosphere, good collaboration and intense knowledge sharing. Dirk Bormann, Niklas Zimmermann, Tobias Werth, Stefan Kählert, Yifan Wang, Markus Robens, Jan Henning Müller, Bastian Mohr, Aytac Atac and Lei Liao got me off to a good start, when I joined the institute. I enjoyed all the technical and social activities with them as well as the exchange of experience. Likewise, special thanks go to René Adams for his enduring support in technical and personal discussions as well as for many joyous moments during joint adventures. In addition I would like to thank my office colleagues in all these years, Sebastian Strache, Stefan Dietrich, Vahid Bonehi, Michael Hanhart and Leo Rolff, for the many interesting discussions, being ambitious and discerning dialog partners as well as for the collaborative working atmosphere. In the same manner, special thanks go to Eva Schulte Bocholt for sharing her clever ideas and pragmatic perspectives on difficult technical problems as well as in the proofreading of this thesis. I am very grateful for the fruitful personal conversations as well as for her exceptional commitment throughout my entire time at the IAS. Spending countless weekends and night shifts, Eva made an enormous contribution to the tape-out of the HQLED chip. She always managed to brighten the hard work up with her happy, cheerful attitude. It has been a great pleasure to work with her. Moreover, I am grateful to all colleagues, who supported me during the tape-out process of the HQLED ASIC. A special acknowledgment goes to Fabian Speicher and Soheil Aghaie for their

help in the digital verification of the HQLED chip. Fabian furthermore provided valuable comments in the proofreading of this thesis. Additionally, I would like to thank my colleagues Tobias Zekorn and Markus Scholl for their given feedback and insights in the proofreading of this work. I cordially thank Tobias Saalfeld for his outstanding personal support and dedication during the final completion of this thesis. I am grateful for his extensive LaTeX support, his shared experiences during long lasting phone calls as well as for the friendly reminders from time to time. Many thanks also go to our secretariat, the IT team and the mechanical workshop for their helpfulness and support in every situation. I would like to emphasize the keen commitment of Marion Efing, Rike Bosbach and Wladimir Oleschenko. In particular, I would like to thank Wladi for providing his extraordinary rescue skills on the data recovery of my faulty hard disks and Peter Bransch for the excellent mechanical manufactures used in our hardware demonstrators.

A huge *"Thank You!"* goes to the many students and assistants, who jointly worked together with me. This thesis would not have been possible without their diligence, dedication and team spirit! In particular, I would like to thank Emanuel Leicht, who substantially contributed for many years as a student assistant to the scientific results and development of the color control algorithm. Additionally, Colin de Vrieze and Florian Renneke spent endless hours on the hardware development and measurements of the different receiver concepts for DLT backmodulation. In the same manner, special thanks go to Arne Rossius, who worked for several years in an outstanding dedication on elaborate hardware design and laboratory work. I thank him for the many valuable discussions, for sharing his brilliant expertise with me as well as for his significant contribution to the joint papers. It has been a great pleasure to work with him.

I would also like to express my best thanks to all companions and friends, who sympathized with me, for their inspiring technical and personal discussions as well as their continuous motivation. In particular, I thank Johannes Hauck, Marco Stienecker and Nils Soltau for their technical reviews and great support in preparation of the oral examination. Johannes furthermore helped to improve the written thesis by giving deliberate feedback in the proofreading of this work. Additionally, I want to acknowledge the support of my current Infineon colleagues, especially of Uwe Schmidinghoff, who enabled very flexible working hours and a personal latitude for me in the final completion of this thesis. Special thanks go to Julia Badeda and my cousin Johannes Lohaus for their continuous support and positive encouragement during this thesis, for their friendship and the many insights broadening my horizon as well as for the wonderful joint time in Aachen.

Moreover, my best thanks go to Heiner Schmitz, Dörte Kaulard-Bayer and Akin Bayer, who accompanied and encouraged me in an extraordinary manner during different periods of my thesis writing. I thank all of them very much for fostering my personal advancement, for their dedicated commitment, their friendship and the great support, they granted me in every sense.

My family is my source of strength and energy in my life. I gratefully thank my parents Maria and Ludger Lohaus, who enabled my development with their continuous support and outstanding dedication as well as their strong faith in me. They always fostered my talents, kept me grounded and helped me to get clear thoughts in an exceptional and loving manner. My best thanks likewise go to my sisters Raphaela Hilz and Theresa Rösener with their families, who always gave me strong encouragement and caring assistance. I cherish our strong bond and am glad and proud to be part of this amazing family. Finally, I thank my wife Barbara for her enduring patience and endless love as well as her exceptional support giving me strength and confidence, with which this work was only possible. I am deeply grateful for her enormous dedication and distinguished commitment that she set in me and this thesis. Barbara has been my role model to continue and walk the extra mile whenever necessary.

"Thank you all for your great support!" I am honored and grateful to have so many trusting people, friends and family at my side.

To my family

Preface

This thesis encompasses many of my research activities during my time at the IAS group of RWTH Aachen University. The research topic on *"smart LED drivers"* providing high efficiency, outstanding color rendering and robust communication simultaneously, evolved out of my scientific work conducted within the framework of the *"EnLight"* project. This innovative EU project formed a consortium of 27 scientific and industrial partners from five European countries and comprised a total project cost of more than 40 Million Euro. Finally, the *"EnLight"* project achieved 45 % to 70 % energy savings, which was rewarded by the *"2014 Innovation Award"* of the ENIAC Joint Undertaking. In this regard, parts of my research have been funded within the *"EnLight – Energy efficient and intelligent lighting systems"* project by the ENIAC Joint Undertaking (project ID: 270707-2) and the German Federal Ministry of Education and Research (FKZ: 16N11438, Subproject: Erforschung von Elektronikbausteinen für energieeffiziente, intelligente Beleuchtungssysteme). In the course of this project, a close cooperation with the company Insta Elektro GmbH in person of Friedhelm Holtz was established. Thereby, parts of this thesis about the DLT methodology supported the transformation of DLT into an official IEC standard [106] continuously with several background activities.

At the IAS, various scientific publications emerged from my research activities in the course of the years. Several sections and parts of this thesis have therefore been previously published in scientific journals or on peer-reviewed conferences.

For that matter, the corresponding papers are briefly listed in the following paragraph according to their content that has been embedded in the larger context in this work. Regarding the DLT methodology, paper [235] presents a comparison of different DLT FW-RXs, whereas publications [238] and [241] highlight efficient dual-stage power supplies for DLT control devices (CDs). A fully functional CD with advanced features has been released in [240]. The general concept on bidirectional DLT communication was published in [243]. The publications [236] and [237] introduce a digital dynamic headroom control for LED driving stages. Moreover, the initial idea on the *"Current Replica"* sensing method was shown in [242]. Finally, the basic algorithm of the developed color control approach has first been published in paper [239].

The broad variety of topics studied in this thesis could also be successfully covered due to the reliable commitment of my colleagues and co-workers. Also the students, who wrote their Bachelor's and Master's theses under my guidance, contributed essentially to the main subjects of the presented research. Some of these works which I supervised as well as the associated accomplishments have also been integrated in this PhD thesis. I would like to give a concise overview on the individual contributions. In particular, I would like to mention the excellent works of Colin de Vrieze [97], who laid the groundwork for a bidirectional DLT communication, and of Andreas Sturm [331], who build the first dual-stage power supply for DLT CDs. To achieve meaningful measurement results, elaborate laboratory work was performed in an outstanding dedication by Arne Rossius [305]. Setting a special focus on DLT communication, power supplies and LED driving circuits he took care of versatile engineering tasks, e.g. circuit design, PCB layout or software programming. Florian Renneke contributed to the topic of bidirectional DLT communication by assembling PCBs and hardware setups, writing (measurement) software as well as recording measurements. Peter Bransch fabricated multiple useful mechanical tools and devices, e.g. the housings of three self-constructed LED spotlight demonstrators and four table lamps that were needed in measurement setups. Emanuel Leicht programmed the most part of the extensive MATLAB® GUI and had a significant contribution to the development of the color control algorithm. Maximilian Nitsch succeeded Emanuel and adapted the MATLAB® GUI for measurement purposes. Josua Arndt implemented a ZigBee stack onto the self-developed universal control board, whereas Maximilian Lorent engineered a WiFi infrastructure and an iPad App for the luminaire demonstrators.

Regarding the HQLED chip, several people have been involved in the tape-out process. Eva Schulte Bocholt contributed to a great extend to the HQLED ASIC. Beyond implementing and improving circuit designs conceived during her Master's Thesis [313], she did the entire chip layout. Some analog circuits

of the DLT FW-RXs were provided by Mario Su. Soheil Aghaie modified the HSD interface based on an original design from Jan Henning Müller and took care of its functional verification. Fabian Speicher facilitated functional verification of some digital circuits, particularly the serial UART interface [271], whose basic core also originates from a design of Jan Henning Müller. Bastian Mohr occasionally supported the setup of the digial design flow. Moreover, the HQLED ASIC contains some components and circuit blocks that have been previously developed by Stefan Dietrich and Sebastian Strache during another power electronics project called *"SIMO LED Driver"* [102]–[105], [329].

Aachen, April 23rd, 2021

Abstract

Energy efficiency is up to date still the key driver for future lighting systems. Beyond the vast deployment of light-emitting diodes (LEDs), smart control features using intelligent algorithms in combination with active sensor nodes have proven to enhance efficiency and reduce power consumption significantly. Applying both, centralized and decentralized control techniques, light sources are thus only turned on, where and when really needed. Combining the solid-state lighting (SSL) technology with smart control systems moreover enables completely new functionality that goes far beyond efficiency improvements. Artificial light sources can thereby be dynamically adapted throughout the course of a day to match the human circadian rhythm. Consequently, so-called *"human centric lighting"* (HCL) has recently risen as an emerging field in future lighting applications. Light quality turns out to play an important role in this context as it stimulates body functions like cognition or the wake/sleep cycle and affects human emotions as well as well-being and perception. Beyond that, multiple other applications require a high technical light quality, such as museum lighting, industrial processes or medical purposes.

This thesis focuses on three core components of an intelligent lighting system, which are the communication system, a color control and mixing algorithm as well as a multi-channel LED driving stage. Aiming to pave the way for HCL applications, this thesis proposes new control theories, circuit architectures and system concepts for each of these functional blocks. Typical limitations, such

as providing high efficiency at the expense of poor color rendering or vice versa shall be overcome with energy-efficient and flexibly deployable electronics. To optimize color precision, efficiency and tailored system intelligence at the same time, the three functional units are matched to one another. Providing easy interaction and assembly with other lighting systems, this thesis designs the core blocks in a flexible manner and develops improvements on both, component and system level.

After conducting a thorough literature review, this thesis evaluates the Digital Load-Side Transmission (DLT) approach as an attractive communication method to be further investigated in detail. Targeting minimum (standby) power consumption, robust receiver architectures are developed for this power line communication (PLC) technology at lowest possible circuit complexity. Special emphasis is set on being monolithically integrable for a system on chip (SoC). The proposed receiver circuits finally achieve very high robustness. 24 h long-term measurements show that failure rates in a two digit ppm range are realized.

Furthermore, this thesis seeks to overcome the unidirectional communication capability and strict power supply limitations of the DLT architecture. Two efficient dual-stage power supply concepts for DLT CDs are proposed, implemented and optimized for maximum output power. It is thereby possible to power a Wireless Fidelity (WiFi) module in the CD and thus enable wireless accessibility of the DLT system. This thesis thereby improves system intelligence of the DLT approach, while coping with its harsh power supply limitations. Additionally, a bidirectional communication approach is developed that extends the DLT methodology far beyond the existing standard. Modulating the current flow is used for realizing a reverse communication channel. Four different receiver architectures for this backward transmission are conceived, implemented and evaluated in real hardware measurements. The corresponding performance evaluation investigates again power consumption, robustness and sensitivity as well as circuit complexity of all proposed concepts. 24 h measurements yield error rates in a two to three digit ppm range, while maintaining low complexity and tolerable low power consumption. Balancing power consumption and system intelligence, the applied methods eventually realize a tailored DLT communication interface for smart lighting systems. Finally, this thesis assesses this improved DLT approach in contrast to other (low power) wireless communication systems and constitutes that DLT is an effective alternative for future lighting systems.

Achievable color quality regarding brightness accuracy, color deviation and spectral power distribution (SPD) is mainly determined by the underlying color control algorithm. State-of-the-art approaches mostly only use the minimal number of three LED primaries, which however creates adverse SPDs and decreased color quality. Existing solutions of a tetra- or penta-color system

on the contrary typically suffer from very high complexity. This thesis closes this scientific gap by developing a six-channel color control algorithm balancing measurable color quality with employed hardware demands. Due to this additional degree of freedom, the color control offers an optimization opportunity of the emitted SPD by selectable criteria, such as color rendering index (CRI) or luminous efficacy, while keeping minimal perceivable color shift. Simulation and measurement results prove that a high CRI > 90 is achieved over a large color temperature (CT) range ($2000\,\mathrm{K} < \mathrm{CT} < 7500\,\mathrm{K}$). Simultaneously, the color deviation is kept below the acceptable limits of $\Delta E < 3$ and $\Delta u'v' < 0.035$. Although accounting for the highly nonlinear relationships of human color and brightness perception, hardware complexity is kept low. The color control approach is in fact implemented on a simple microcontroller (μC) and could also be realized in dedicated hardware on an ASIC, for example (e.g.) by using the CORDIC algorithm for realizing the needed QR decomposition. Further improvement measures and handling of specific application cases are also briefly discussed and outlined.

In addition to the color control algorithm, the LED driving stage influences color accuracy significantly due to the linear relationship between average LED forward current and emitted luminance. Excessive current ripples must consequently be avoided to ensure good color stability. This thesis therefore improves a dynamic headroom control concept for a high efficiency and precise current regulation by introducing a digitally assisted control methodology. This approach gives maximum design flexibility and enhances control over regulation speed and stability by ensuring good decoupling between the interdepending control loops. The current deviation ΔI_{LED} is finally kept below 1.2 % from the nominal target value, while the transient waveform is ripple free and after a short settling phase nearly perfectly flat. An overall peak efficiency of $\eta_{peak} = 93.9\,\%$ is recorded in measurements of the prototype implementation. A very high efficiency is maintained even over a large dimming range down to 20 %.

Finally, the proposed concepts for DLT communication and LED driving stage are implemented in an ASIC solution to further improve overall system performance. Particularly energy efficiency and color precision benefit from the synergy effects of the integration because it is possible to realize faster switching speeds and more precise matching between the individual circuit components. This thesis discusses the improvement potential for a monolithic integration in detail and implements the corresponding concepts.

In conclusion, this thesis presents various novel circuit and control concepts for energy-efficient electronics to improve and tailor the quality of smart lighting systems. The improved core components thereby found the basis for further enhancements regarding human centric lighting (HCL) applications.

Contents

Acknowledgment **v**

Preface **xi**

Abstract **xv**

List of Figures **xxv**

List of Tables **xxxiii**

List of Abbreviations **xxxv**

1 Introduction **1**
1.1 Intelligent and Efficient Solid-State Lighting 2
1.2 Scope of this Thesis 5
1.3 Aim of this Work 7
1.3.1 Communication System: Digital Load-Side Transmission 9
1.3.2 Color Control Algorithm 10
1.3.3 LED Driving Stage 11
1.3.4 System Optimized ASIC Implementation 12
1.3.5 Definition of Specific Measurable Aims 12

2 System Considerations for a Smart LED Driver 15
2.1 Review of Communication Systems Suited for Intelligent Lighting Control . . . 16
2.1.1 Wireless Communication Systems . . . 18
2.1.2 Wire-Bound Communication Systems . . . 21
2.1.3 Assessment and Comparison of Communication Technologies Suited for Intelligent Lighting Control . . . 26
2.2 Fundamentals of Color Management and Control . . . 32
2.2.1 LED Fundamentals: Electrical and Optical Properties . 33
2.2.2 Human Perception, Colorimetry and Color Mixing . . . 36
2.2.3 Review of State-of-the-Art Color Control Approaches . 48
2.2.4 Human Centric Lighting (HCL) and Applications with High Technical Light Quality . . . 51
2.3 Theoretical Background on Energy-Efficient LED Driving . . . 57
2.3.1 Fundamentals of Current-Based LED Driving and Dimming Techniques . . . 58
2.3.2 Review of State-of-the-Art LED Driver Topologies . . . 67
2.3.3 Energy-Efficient LED Driver Topologies Using Dynamic Headroom Regulation . . . 72
2.4 Summary of System Requirements and Concept for a Smart LED Driver . . . 75

3 Intelligent Lighting Control with Digital Load-Side Transmission (DLT) 79
3.1 DLT Fundamentals and Specification . . . 81
3.1.1 Power Supply Boundary Conditions . . . 82
3.1.2 DLT Communication . . . 84
3.2 Development and Evaluation of Receiver Topologies for DLT Control Gears . . . 91
3.2.1 System Concept of an Effective DLT Receiver . . . 92
3.2.2 Architecture and Implementation of Different DLT Detector and Decoder Circuits . . . 99
3.2.3 Performance Evaluation and Comparison of Implemented DLT-Receiver Architectures . . . 111
3.3 Efficient DLT Power Supplies . . . 120
3.3.1 Power Budget, Supply Limitations and Efficiency Targets in DLT Control Devices . . . 122
3.3.2 Preliminary Investigations and Conceptual Idea of a Dual-Stage Power Supply Topology for DLT CDs . . . 127

3.3.3 Power Supply Concept A: Dual-Stage Topology with a Flyback- and a Buck-Converter . . . 130
3.3.4 Power Supply Concept B: Dual-Stage Topology with a Boost- and a Flyback-Converter . . . 135
3.3.5 Performance Evaluation and Comparison of Power Supply Concepts A and B . . . 142
3.4 Towards Bidirectional DLT Communication . . . 149
3.4.1 System Considerations for Bidirectional DLT . . . 151
3.4.2 Reverse Transmitter Concept and Implementation for Bidirectional DLT Communication . . . 158
3.4.3 Reverse Receiver Concepts and Implementation for Bidirectional DLT Communication . . . 160
3.4.4 Performance Evaluation and Comparison of REV-RXs for Bidirectional DLT Communication . . . 172
3.5 Assessment of the Developed DLT System . . . 183
3.6 Summary and Conclusion of the Improved DLT System Developments . . . 192

4 Color Mixing and Control for High Quality Lighting Systems 197
4.1 Color Computation Algorithm for Multi-Channel LED Lighting Systems . . . 198
4.2 Nonlinear Adaption to Human Color and Brightness Perception 206
4.3 Implementation of Color Control Algorithm . . . 212
4.4 Application Related Improvements and Optimization for Precise Color Control . . . 217
4.4.1 Handling of Color Temperature . . . 218
4.4.2 Mapping of Outside Gamut Points . . . 219
4.4.3 Handling of Negative Scaling Factors: Optimization with an Intelligent Elimination Routine . 219
4.4.4 Adaptive Optimization Vector . . . 221
4.4.5 Adaption of Color Control Algorithm to Other Dimming Techniques . . . 223
4.4.6 Enhanced Color Quality by Closed Loop Control . . . 224
4.5 Experimental Validation of the Optimized Color Control Strategy 225
4.5.1 Simulation Results of the Proposed Color Control Algorithm . . . 226
4.5.2 Measurement Results of the Proposed Color Control Algorithm . . . 234

5 Efficient LED Driving for High Quality Lighting Applications 255
5.1 System Concept of an Efficient LED Driver Topology 256
5.2 Digital Dynamic Headroom Regulation with RDAC Feedback Control 259
5.2.1 Sensitivity Analysis on the Impact of the RDAC Resolution 262
5.2.2 Digital Control Algorithm for Dynamic Headroom Regulation 267
5.2.3 Stability Considerations for Decoupling the Three Interacting Control Loops 270
5.3 Implementation of the Developed LED Driver 274
5.3.1 Buck-Boost Converter for LED Power Supply 274
5.3.2 PWM-controlled Linear Current Regulator for Precise Brightness Adjustment 277
5.3.3 Digital Dynamic Headroom Control with an RDAC . . 279
5.4 Performance Evaluation and Measurement Results of the Developed LED Driving Stage 282

6 Monolithic Integration of a Smart LED Driver 297
6.1 Optimized System-on-a-Chip Concept 298
6.2 Integrated Receivers for DLT Control Gears 302
6.3 Digital Dynamic Headroom Control for Integrated LED Drivers 308
6.3.1 Integrated Voltage Control Loops for Digitally Assisted Dynamic Headroom Regulation 311
6.3.2 Implementation Aspects for the Integrated Buck Converter and its Control Circuits 330
6.4 Efficient and Precise Current Sense and Control Approach for Integrated LED Drivers 336
6.4.1 System Concept and Implementation of the Current Replica Sense Approach 339
6.4.2 All Digital Current Controller 344
6.5 Summary & Efficiency Analysis of the HQLED ASIC Design . 349

7 Conclusion and Outlook 355
7.1 Summary and Conclusion 356
7.1.1 Enhanced DLT Communication 356
7.1.2 Advanced Color Control For High Quality Lighting Applications 359
7.1.3 Efficient LED Driving with Precise Current Control . . 361
7.1.4 Closing Remarks and Reflections on the Targeted Goals 362
7.2 Outlook 364

Bibliography **367**

A Additional Material on Digital Load-Side Transmission **399**
A.1 DLT Fundamentals 400
A.2 DLT FW-RX 400
A.3 DLT Control Device Implementation 406
A.4 Power Supply Calcuations for a DLT CD Enabling WLAN Access 408
A.5 REV-RX Concept B: TER measurements 409
A.6 Derivation of the Mean Power Consumption for the Presented DLT REV-TX 410

B Additional Material on Color Mixing & Control **413**
B.1 CIE 1976 (u'v') Chromaticity Diagram 414
B.2 Computation of CCT from Realized (x,y) – Color Coordinates 414
B.3 Photometric and radiometric quantities 416

C Luminaire Demonstrators **417**
C.1 Spotlight Demonstrator 418
C.2 Table Lamp Demonstrator 422

Curriculum Vitae **427**

List of Publications **429**

List of Figures

1.1 Strategic roadmap of the European lighting industry. 4
1.2 The scope of this thesis: A *"smart LED driver"* as part of an intelligent lighting system. 6
1.3 Outline and structure of this thesis. 8

2.1 I–V relationship for different LED colors. 34
2.2 LED current vs. Illuminance 34
2.3 Normalized LED spectra of different peak wavelengths λ_{peak}. . 35
2.4 CIE eye sensitivity functions $V(\lambda)$ in the visible spectral range for the photopic vision regime. 37
2.5 CIE 1931 color matching functions $\bar{x}(\lambda)$, $\bar{y}(\lambda)$ and $\bar{z}(\lambda)$. . . . 39
2.6 CIE 1931 (x, y)-chromaticity diagram showing different CTs on the planckian locus and several MacAdam ellipses. 41
2.7 Flicker risk limits as a function of flicker frequency $f_{Flicker}$. . . 57
2.8 Implementation examples of different LED driving circuits with AM dimming functionality. 60
2.9 Implementation example of a PWM-switched LED driving circuit and its corresponding transient waveform signals. 61
2.10 Illuminance modulation as a function of (average) LED forward current for different driving methods. 63

2.11 Exemplary solutions for AC-DC-based LED driver topologies in single-phase AC power grids. 69
2.12 Conceptual block diagram of dynamic headroom control with a DC-DC converter and a linear current regulator. 73
2.13 Target concept of a monolithically integrable *"smart LED driver"*. 76

3.1 Conceptual block diagram and typical wiring of a DLT system. 80
3.2 Classification of DLT timing periods and expected voltage waveforms at CD and CGs according to the official DLT standard [106]. 82
3.3 Maximum current and voltage ratings during DLT supply period. 84
3.4 Current and voltage signals during DLT data period. 85
3.5 Timing and voltage specifications for DLT data modulation. . . 86
3.6 All possible DLT frame sequences indicating transmitted data bits and state of the six corresponding half-bits. 87
3.7 Example of a single DLT brightness telegram. 88
3.8 Structure of DLT telegram types. 91
3.9 Internal setup of a DLT forward (FW)-receiver (RX). 93
3.10 Implementation of zero crossing detector (ZCD). 95
3.11 Implementation examples of different current sources suited as bypass circuits in a DLT control gear (CG). 97
3.12 Implementation of low current (LC) and high current (HC) bypass circuits for DLT FW-RXs. 98
3.13 Concept A: Active bandpass with Schmitt-Trigger. 101
3.14 Transfer functions of the active bandpass filter. 101
3.15 Measured waveform signals of detector concept A in a DLT FW-RX during DLT data period using $C_2 = 49\,\mathrm{pF}$. 102
3.16 Concept B: Resistive Divider with Digitial FIR Filter. 104
3.17 Measured waveform signals of FW-RX concept B. 104
3.18 Concept C: Differential Analog Subtraction Filter. 106
3.19 Measured waveform signals of FW-RX concept C. 106
3.20 Flowchart of the implemented DLT frame decoder. 108
3.21 Flowchart of the implemented DLT telegram reconstruction and evaluation. 109
3.22 Test board of a fully functional DLT FW-RX using filter concept A. 112
3.23 Recorded telegram errors per minute of different DLT FW-RX concepts under evaluation in 24 h longterm measurement. . . . 118
3.24 Current draw measurement of a WiFi module for different operation modes at a constant supply of $V_{DD} = 3.3\,\mathrm{V}$. 124
3.25 Conceptual topology of a conventional single-stage buck converter suited for powering a DLT CD. 128

3.26 Conceptual topology of a dual-stage power supply circuit suited for high power demands in DLT compliant CDs. 129
3.27 Schematic of implemented dual-stage supply concept A for powering WLAN-equipped DLT CDs. 131
3.28 Efficiencies of 1st and 2nd converter stage in supply concept A. 133
3.29 Measured overall efficiency of supply concept A at $V_{out} = 3.3\,\mathrm{V}$. 133
3.30 Schematic of implemented dual-stage supply concept B for powering WLAN-equipped DLT CDs. 136
3.31 Schematics of the boost converter's control circuit. 138
3.32 Influence of inductor size on drawable average input current of the boost converter in power supply concept B for DLT CDs. . 139
3.33 Measurement on the effects of switching frequency and input voltage on boost converter efficiency. 139
3.34 Measured output and switch pin voltages of the developed boost converter for a constant 100 mA load. 140
3.35 Measured efficiencies of the converter stages of supply concept B dependent on load current for different input voltages. 141
3.36 Photograph of the developed test board with both power supply concepts using the same current limiter and enable switch. . . . 143
3.37 Measured input characteristcs and voltage drop over the input current limiter of supply concept A and B at $I_{load} = 100\,\mathrm{mA}$. . 144
3.38 Overall efficiency of both concepts A and B at $V_{out} = 3.3\,\mathrm{V}$ over drawn load current. 146
3.39 System concept of bidirectional DLT communication highlighting internal setups of CD and CG. 152
3.40 Suitable modulation schemes for DLT backward transmission. . 155
3.41 Specified current limit for a DLT CG during data period for rated nominal power consumptions of 40 W and 60 W. 156
3.42 Modified LC bypass in a CG with digital controllable current modulation level $I_{mod,set}$ suited for DLT backward transmission. 159
3.43 Sense resistor in bypass path of implemented DLT CD. 161
3.44 Conceptual architectures for different REV-RX approaches. . . 162
3.45 Implementation of REV-RX concept A: Sense resistor with active analog bandpass filter and Schmitt-Trigger. 163
3.46 Internal hardware configuration of the μC for the digital bandpass and matched filters of REV-RX concept B. 165
3.47 Implementation of REV-RX concept C: Current sense transformer with burden resistor. 168
3.48 Flowchart of the implemented frame decoding software for all REV-RXs in DLT backward transmission. 171

3.49 Measurement setup of implemented CD and CGs for bidirectional DLT communication. 173
3.50 Measurement of V_{grid} and I_{byp} at the input of a DLT CG. . . . 174
3.51 Recorded telegram errors per minute of different DLT REV-RX concepts under evaluation in 24 h longterm measurement. . . . 177
3.52 Photograph of the implemented DLT CD with efficient power supplies enabling extended functionality and interoperability. . 191

4.1 Displayable color gamut of different LED configurations in the CIE 1931 chromaticity diagram. 200
4.2 Brightness B versus lightness and normalized luminance. 210
4.3 Flowchart of the implemented color control algorithm. 213
4.4 Flowchart of nonlinear brightness correction adjusting computed factors $d_{rel,i}$ to PWM duty cycles D_i. 214
4.5 Color gamut of an RGB-CAW configuration highlighting specific areas with removable LEDs for intelligent ellimination. 221
4.6 GUI of self-developed MATLAB® program for simulation and calculation of color synthesis with a set of LEDs. 225
4.7 Simulation of emitted optical spectrum for three different luminaire configuarions at CT=5500 K and max. lumiance L_v. 227
4.8 Simulation of CRI versus CT for three different luminaire realizations at maximum constant luminous flux. 228
4.9 Simulation of color difference ΔE versus CT for three different LED configurations at maximum constant luminous flux. . . . 230
4.10 Simulation of color distance $\Delta u'v'$ versus CT for three different LED configurations at constant luminous flux. 230
4.11 Simulation of color difference ΔE versus CT for three different LED configurations at 50 % brightness level. 231
4.12 Simulation of color difference ΔE versus CT for three different LED configurations at 20 % brightness level. 231
4.13 Simulation of ΔCCT versus CT for three different LED configurations at maximum constant luminous flux. 232
4.14 Simulation of color shift over the entire displayable gamut for an RGB-CAW configuration with intelligent elimination. 233
4.15 Measurement setup for spectral recordings of self-constructed spotlight luminaire under different viewing angles. 235
4.16 Internal configuration of LED spotlight luminaire demonstrator with color sensor and temperature measurement probes. 237
4.17 Comparison of measured LED spectra at $T_{measure} = 40\,°C$ with the datasheet based LED spectra used for simulation. 239

4.18 Comparison of measured LED spectra for two different ambient temperatures ($T_1 = 35\,°C$ and $T_2 = 60\,°C$). 240
4.19 Simulation versus measurement results of CRI over the entire CT range for three different luminaire realizations. 242
4.20 CIE 1931 chromaticity diagram with spanned color gamuts of measured and datasheet based chromaticities. 243
4.21 Simulation of CRI versus CT using measured calibration spectras except for the blue LED relying on the datasheet. . . . 244
4.22 Simulation vs. measurement results of color distance $\Delta u'v'$ over the entire CT range for three different LED configurations. . . 245
4.23 Measured color distance $\Delta u'v'$ versus CT for RGB-CAW luminaire setup at different brightness levels. 246
4.24 Measured ambient temperatures at LED spot over CT range for three different luminaire realizations. 247
4.25 Color quality measurements under different viewing angles for the RGB-CAW luminaire configuration. 248
4.26 Color shift measurements over the displayable gamut for an RGB-CAW configuration using $\boldsymbol{s_{opt}}$ ($a = 1$; $b = 2$). 250
4.27 Color shift measurements for different luminaire configurations without the intelligent elimination routine. 251

5.1 System concept of the proposed dimmable LED driver using digital feedback control for dynamic headroom regulation. . . . 256
5.2 Structure of an RDAC for digitally assisted headroom control. . 260
5.3 Principle of operation of the digital feedback control loop. . . . 261
5.4 Exemplified regulation behavior of drain potential V_D within minimum target window size. 263
5.5 Step size V_{step} and efficiency η as a function of RDAC resolution N_{RDAC}. 265
5.6 Flowchart of the digital dynamic headroom control. 268
5.7 Interacting control loops within the proposed digital dynamic headroom regulation concept. 271
5.8 Small-signal equivalent circuit diagrams for control loop I. . . . 272
5.9 Stability criteria for interaction of control loops II and III. . . . 273
5.10 Photographic image of the implemented LED driver with a digitally assisted dynamic headroom regulation. 275
5.11 Implementation of the switching pre-regulator as a buck-boost converter with an RDAC based dynamic headroom control. . . 276
5.12 Measured efficiency of the buck-boost converter versus output voltage. 277

5.13 Schematic of PWM-switched linear current regulator with compensation network. 279
5.14 Measurement of LED current flow I_{LED} for a minimum PWM on-time while operating five series-connected LEDs. 283
5.15 Measured Variations of I_{LED} and $V_{DD,LED}$. 284
5.16 Voltage dips on drain potential V_D at 50 % PWM duty cycle. . 285
5.17 Measured current accuracy of I_{LED} with respect ot its nominal value as a function of dimming level. 287
5.18 Measurements of $V_{DD,LED}$ showing the control behavior of the digital dynamic headroom approach for different scenarios. . . . 289
5.19 Measured control behavior of the digital dynamic headroom regulation for higher output voltages. 290
5.20 Measured efficiencies of the entire control system for several LED voltages over different dimming levels. 293
5.21 PCB assembly with eight instances of the proposed LED driving stage for a powerful spotlight luminaire. 295

6.1 System concept of the developed HQLED test chip. 299
6.2 Layout of the HQLED test chip, a 4-channel *"smart LED driver"* with external color control. 301
6.3 Auxiliary cirucits of the integrated DLT FW-RX. 304
6.4 Implementation of the programmable DLT bypass driver. . . . 307
6.5 Conceptual block diagram of the integrated LED driving stage with dynamic headroom regulation for one channel. 309
6.6 Flowchart of a hysteretic buck converter control providing additional protection features. 312
6.7 Realized concept of the floating input range ADC. 314
6.8 Flowchart of the improved buck converter control with a negative counteracting hysteresis and additional protection features. . . 316
6.9 Transient behavior of involved current and voltage signals during the voltage start-up. 321
6.10 Highlighted feedback paths of the dynamic headroom regulation for its two control variables b_{DAC} and *VFB_SET*. 324
6.11 Current flow and voltage definitions of the buck converter. . . . 326
6.12 Timing diagram of the current and voltage relationships at a switching event of the current regulator. 327
6.13 Layout view of the integrated LED driver with the CR concept and the RDAC based dynamic headroom control. 333
6.14 Implementation of the fully differential 4 bit floating input range SAR-ADC with a programmable dual gain stage. 335

6.15 Implementation of the 6 bit single slope ADC measuring the drain potential V_D over the current regulator. 335
6.16 CR sense and control concept for integrated LED drivers. . . . 337
6.17 Highlighted analog key components in CR sense and control concept. 340
6.18 Detailed schematics of the implemented CR sense and control concept. 342
6.19 Photograph of the produced HQLED ASIC. 354

7.1 LED driver with digital dynamic headroom regulation and thermo-electrical model for color shift compensation. 365

A.1 Internal setup and wiring of a DLT CG according to the official DLT standard [106]. 400
A.2 Photograph of the implemented UCB with a powerful ATxmega μC featuring multiple connectors and interfaces. 401
A.3 Flowchart of implemented DLT frame decoder for concepts B and C. 403
A.4 Schematics of benchmark design for DLT FW-RX concept A: Passive analog bandpass filter with Schmitt-Trigger. 404
A.5 Measured waveform signals of detector concept A in a DLT FW-RX using the passive analog bandpass filter configuration. 404
A.6 Schematics of benchmark design for DLT FW-RX concept A: An active analog BP with non-integrable component sizes. . . . 405
A.7 Measured waveform signals of detector concept A using an active analog BP filter setup with non-integrable component sizes. . . 405
A.8 Circuitry of the modulating 0 V bypass of a DLT CD. 406
A.9 Hardware setup of the power supply board for a DLT CD. . . . 406
A.10 Start-up supply circuit for a DLT CD. 407
A.11 System concept and board assembly of the proposed DLT CD. 407
A.12 24 h measurements of DLT REV-RX concept B for different $I_{mod,set}$. 409

B.1 CIE 1976 (u', v')-chromaticity diagram showing different CTs on the planckian locus. 414

C.1 Arrangement of self-developed luminaires and control devices. . 417
C.2 Example of 120 W spotlight demonstrator. 418
C.3 Board assembly & data distribution of spotlight demonstrator. 419
C.4 Power distribution of the spotlight luminaire. 419

C.5 Internal setup and PCB assembly of the spotlight luminaire . . 420
C.7 LED driver board with eight individual LED channels. 421
C.8 Aluminium case with RF antenna of a table lamp demonstrator. 422
C.9 Board assembly and data distribution of the table lamp demonstrator. 423
C.10 Power distribution of the table lamp demonstrator. 423
C.11 LV main control and LED driver board. 424
C.12 HV board with 25 W power supply and DLT circuitry. 425
C.13 LED board for table lamp with installed true color sensor. . . . 425

List of Tables

1.1 Summary of specific, measurable goals to be achieved within this work. 13

2.1 Power consumption for different chip sets of low-power wireless communication techniques. 30

3.1 Payload data in dependence of selected telegram type. 89
3.2 Circuit components and correlated functions in a DLT FW-RX. 93
3.3 Power Consumption of DLT FW detector concepts. 115
3.4 Evaluation of TERs recorded in 24 h measurements. 117
3.5 Summary and comparison of DLT-FW detector topologies. . . 119
3.6 Selected component values for power supply concept *A*. 134
3.7 Selected component values for power supply concept *B*. 142
3.8 Comparison of measurement results on efficiency and maximum available output power for both power supply topologies. 147
3.9 Measurement results on robustness for developed power supplies of DLT CDs. 148
3.10 Selected resistance values for the implemented 8 bit RDAC. . . 159
3.11 Selected component values for REV-RX concept *A*. 163
3.12 Selected component values for REV-RX concept *C*. 169

3.13 Measured robustness and sensitivity for each REV-RX concept under evaluation. 176
3.14 Measured current draw of the DLT CD and associated power consumption for each REV-RX concept. 180
3.15 Calculated power consumption for each REV-RX concept. . . . 182

4.1 Required memory space in dependency of employed LEDs for the proposed color control algorithm. 216
4.2 Settings used for an adaptive optimization vector in different luminaire configurations for high CRI over a large CT range. . 222
4.3 Weightings of fixed optimization vectors $\boldsymbol{s_{opt}}$ for three different luminaire configurations and optimization parameters. 227

5.1 Selected resistance values for the implemented 8 bit RDAC. . . 281
5.2 Efficiency Enhancement in % versus number of connected LEDs when reducing the drain potential V_D from 500 mV to 300 mV. 285
5.3 Performance comparison of different LED drivers. 294

6.1 Gain start-up settings of $A_{V,LED\text{-}ADC}$ in dependence of the range of the RDAC control word b_{DAC}. 323
6.2 Component sizes and specification of system performance for the developed switching pre-regulator. 331
6.3 Characteristics of the used power devices as implemented in the switching pre-regulator design. 332
6.4 Dimensioning of the implemented 9 bit RDAC. 332
6.5 Loss contributions for a single channel LED driver with digital dynamic headroom regulation and all digital current control. . 353

7.1 Summary of achieved performance in contrast to targeted benchmark. 363

A.1 Evaluation of DLT-FW detectors' TERs in 24 h measurements. 402

B.1 Coefficients used in equation B.1. 415
B.2 Coefficients used in equation B.2. 415
B.3 Summary of photometric and radiometric quantities. 416

List of Abbreviations

6LoWPAN	IPv6 over low power wireless personal area network (WPAN)
AC	alternating current
ACK	acknowledgement
ACL	asynchronous connectionless link
AC-DC	alternating current to direct current
ADC	analog-to-digital converter
ALU	arithmetic logic unit
AM	amplitude modulation
ARQ	automatic repeat request *also known as:* automatic repeat query
ASK	amplitude-shift keying
ASIC	application-specific integrated circuit
CCM	continuous conduction mode

BAN	building area network
BACnet	building automation and control network
BC	best case
BER	bit error rate
BL	bilevel
BLE	Bluetooth Low Energy
BOM	bill of materials
BP	bandpass
BR	basic rate
BSS	basic service set
BT	Bluetooth
CAN	Controller Area Network
CCR	continuous current reduction
CIE	International Commission on Illumination *from French: "Commission Internationale de l'Éclairage"*
CD	control device
CG	control gear
CFL	compact fluorescent lamp
CMF	color matching function
CMOS	complementary metal-oxide-semiconductor
COTS	commercially available off-the-shelf
CQS	color quality scale
CR	current replica
CRI	color rendering index
CSMA	carrier sense multiple access

CSMA/CA	carrier sense multiple access with collision avoidance
CSMA/CD	carrier sense multiple access with collision detection
CT	color temperature
CCT	correlated color temperature
DAC	digital-to-analog converter
DALI	Digital Adressable Lighting Interface
DC	direct current
DC-DC	direct current to direct current
DCM	discontinuous conduction mode
DLT	Digital Load-Side Transmission
DOE	Department of Energy
dSD	digitalSTROM™ device
dSM	digitalSTROM™ meter
DSP	digital signal processor
dSS	digitalSTROM™ server
DSSS	direct sequence spread spectrum
DUT	device under test
e-cap	electrolytic capacitor
EDR	enhanced data rate
e.g.	for example *(abbreviation of latin 'exempli gratia')*
EIB	European Installation Bus
EHS	European Home Systems
EoF	end-of-frame
ESR	equivalent series resistance

ESS	extended service set
etc.	et cetera
EMI	electromagnetic interference
ENOB	effective number of bits
EU	European Union
FB	feedback
FEC	forward error correction
FET	field-effect transistor
FFD	full function device
FIR	finite impulse response
FPGA	field-programmable gate array
FSK	frequency-shift keying
FHSS	frequency-hopping spread spectrum
FW	forward
GaAs	gallium arsenide
GAI	gamut area index
GaN	gallium nitride
GBW	gain-bandwidth product
GE	General Electric Company
Ge	germanium
GUI	graphical user interface
HAN	home area network
HC	high current
HCL	human centric lighting

HSD	high-speed debug
HQLED	high quality lighting efficient driving
HV	high voltage
HW	half-wave
I^2C	Inter-integrated Circuit
IAS	Integrated Analog Circuits and RF Systems
IC	integrated circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IES	Illuminating Engineering Society
I-MOD	current modulation
InGaN	indium gallium nitride
IoT	internet of things
IR	infrared
ISM	industrial, scientific and medical
KNX	Konnex
LAN	local area network
LC	low current
LCD	liquid crystal display
LDO	low-dropout regulator
LE	low energy
LED	light-emitting diode
LoRaWAN	(low power) long range wide area network
LSB	least significant bit

LUT	lookup table
LV	low voltage
MAC	medium access control
MACA	multiple access with collision avoidance
μC	microcontroller
MCU	microcontroller unit
MIM	metal-insulator-metal
MLE	maximum likelihood estimation
MOSFET	metal-oxide-semiconductor field-effect transistor
MSB	most significant bit
MV	medium voltage
NACK	negative-acknowledgement
NAN	neighborhood area network
OCP	overcurrent protection
OECD	Organisation for Economic Co-operation and Development
OFDM	othogonal frequency-division multiplexing
OLED	organic LED
OOK	on-off keying
OP	operational amplifier
opamp	operational amplifier
PC	personal computer
PC	phosphor-converted
PCB	printed circuit board
PD	power delivery

PDK	process development kit
PF	power factor
PFC	power factor correction
PHY	physical
PL	power line
PLC	power line communication
PMU	power management unit
PPD	proportional and proportional derivate
PSDU	PHY service data unit
PWM	pulse-width modulation+
RAM	random-access memory
RC	real case
RDAC	resistive DAC
RDAC	resistive digital-to-analog converter
REV	reverse
RF	radio frequency
RFD	reduced function device
RFID	radio frequency identification
RMS	root mean square
ROM	read-only memory
RWTH	Rheinisch-Westfälische Technische Hochschule
RX	receiver
SAR	successive approximation register
SC	switched-capacitor

SEPIC	single-ended primary inductance converter
S-FSK	spread-frequency-shift keying
Si	silicon
SIG	Bluetooth Special Interest Group
SIMO	single-inductor multiple-output
SMPS	switched-mode power supply
SMD	surface-mount device
SNR	signal-to-noise ratio
SoC	system on chip
SoF	start-of-frame
SoT	start-of-telegram
SPI	serial peripheral interface
SPD	spectral power distribution
SRD	short range device
SSL	solid-state lighting
SUN	smart utility network
TER	telegram error rate
THD	total harmonic distortion
TRIAC	triode for alternating current
TX	transmitter
TRX	transceiver
UART	Universal Asynchronous Receiver Transmitter
UCB	universal control board
USB	unversal serial bus

UWB	ultra-wideband
UI	user interface
U.S.	United States
USA	United States of America
USB	universal serial bus
UV	ultraviolet
VHDL	very high speed IC hardware description language
VLC	visible light communications
V-MOD	voltage modulation
WC	worst case
WirelessHART	wireless highway adressable remote transducer
WiFi	Wireless Fidelity
WLAN	wireless local area network
WPAN	wireless personal area network
ZCD	zero crossing detector
ZCD	zero crossing detection
ZVS	zero-voltage switching

Chapter 1

Introduction

One key challenge of today's society is the worldwide energy consumption and security of energy supplies, which is mainly driven by the trend of an increasing globalization and industrialization. Additionally, the energy consumption – especially in residential homes and offices – rises significantly, further intensifying this issue. Environmental concerns and sustainability have therefore risen great interest in today's society effecting science, politics and industry. Besides strongly promoting renewable energy sources, the European Union (EU) took certain measures to save energy and improve efficiency, for example (e.g.) by stepwise phasing-out inefficient light sources, such as incandescent lamps, since September 2009 [377]. Particularly, lighting has been identified to offer large energy saving potentials. Office and street lighting in fact made up for about one quarter of the tertiary electricity consumption in the EU-27 countries [27] at that time. By establishing the specific directive 2009/244/EC [377], the EU consequently targeted to reduce lighting related energy consumption until 2020 for about 20 %. The worldwide energy consumption in the lighting sector therefore became more and more a subject to mandatory efficiency policies.

Between the years from 2000 to 2015 the coverage of these standards and regulations for lighting experienced a tremendous increase from 2 % to 63 % [112]. Recently, the United States (U.S.) Department of Energy (DOE) forecasted potential energy savings from LED lighting of 5.1 quads ($\approx$ 1494 TWh) until 2035, which is a reduction of about 75 % from the total annual energy used in lighting [326]. Deployment and improvements of the solid-state lighting (SSL) technology thus plays a key role to meet these DOE targets.

1.1 Intelligent and Efficient Solid-State Lighting

Energy efficiency is indeed the main driver for future developments of artificial light sources. Light-emitting diodes (LEDs) as a type of SSL device are thus becoming the predominant lighting source in the near future. While compact fluorescent lamps (CFLs) were the most installed lighting source in U.S. homes in 2016 closely followed by halogen lamps, LEDs outsold all other types of bulbs for the first time in 2017 [298]. In contrast to CFLs, LEDs offer significant advantages, such as longer lifetime, higher robustness, better efficacy, smoother color rendering or the absence of toxic compounds [74], [265]. Because LEDs are *"current controlled"* devices that operate at a low voltage (LV) direct current (DC) supply, some kind of circuitry is however required to transform the alternating current (AC) grid voltage down into the LV domain. A concise overview on SSL including electrical circuitry is given in [40]. The corresponding LED driving circuits actually represent the bottleneck in the SSL reliability chain [6] due to the need of bulky electrolytic capacitors (e-caps). The issue of enhancing the life span of LED drivers has thus been discussed in [6], whereas Castro *et al.* [57] provide a comprehensive review on flicker-free AC-DC LED drivers for single- and three-phase AC power grids for the same reasoning. In order to effectively utilize the assets of the SSL technology, LEDs eventually require suitable driving circuits with matching outstanding performance. The quality of these LED drivers determines in the end possible achievements of the LED fixture regarding (electrical) efficiency, life span and even optical parameters like color precision or flickering.

The upcoming success of this so called *"LEDification"* is strengthened by the increasing trend of deploying smart home automation systems in households and offices that are also capable of intelligent lighting control. Due to a good ease of use these systems are meanwhile widely spread and accepted. Remote control access as well as a modular expandability thus provide much greater flexibility to end users. One key benefit of smart lighting systems is once more a higher energy efficiency, which can be reached on system level by automated light control.

Active sensor nodes, e.g. occupancy or presence detectors communicating with installed luminaires, thereby enable localized illumination of single spots or certain areas in a room [397]. Applying intelligent algorithms to the recorded sensor data [278], [287] consequently realizes a further optimization of energy consumption as light sources are only turned on where and when really needed. Additionally, light level sensors can be deployed to measure the light intensity at a workspace plane or even react on the daylight distribution [49], [50]. Magno *et al.* [257] achieve e.g. between 55 % to 69 % additional power savings measured over a six month period under realistic conditions in an office environment by combining adaptive daylight control with motion detectors. The sensing devices could of course also be directly integrated into an *"intelligent luminaire"*, which saves hardware effort and costs while yielding comparable results [50]. In literature both, centralized and decentralized, control techniques have been reported and successfully applied for such kind of applications and smart control systems [49], [285], [286], [388].

While artificial light is typically fixed in the course of a day, natural light adapts dynamically from sunrise to sunset [219]. Smart lighting systems can thus help to adapt the ambient light to the natural circadian rhythm and thereby achieve higher living comfort as well as enhanced life quality [119]. Combining SSL technology with smart control systems enables completely new features and functionality that go far beyond increasing energy efficiency or minimizing power consumption. As light is the most important timer for the internal human body clock, adaptive lighting systems may stimulate body functions like alertness, cognitive performance or the wake/sleep cycle [140], [400]. Additionally, human emotions, such as mood, energize and relaxation are affected [11], [36], [183]. So-called *"human centric lighting"* (HCL) has thus recently risen as an emerging field in future lighting applications. HCL addresses visual and non-visual as well as emotional and biological effects of emitted light in order to benefit human health and well-being. Fig. 1.1 illustrates the current strategic roadmap to 2025 of the European lighting industry, which defines HCL in conjunction with the aforementioned improvements in LED drivers and intelligent lighting systems as a major aim for the current decade.

The quality of light plays indeed a significant role in human well-being and perception. In this manner, Boyce [38] provides a comprehensive summary of human factors in lighting. In addition, multiple studies reveal that mood, alertness and cognition of human subjects are strongly related to the lighting conditions [140], [311], [433]. Emitted luminance and correlated color temperature (CCT) of a light source are identified as the dominating optical parameters in this context and shall hence be considered for optimizing artificial lighting. Bright light exposure and higher CCTs effectively improve alertness, fatigue

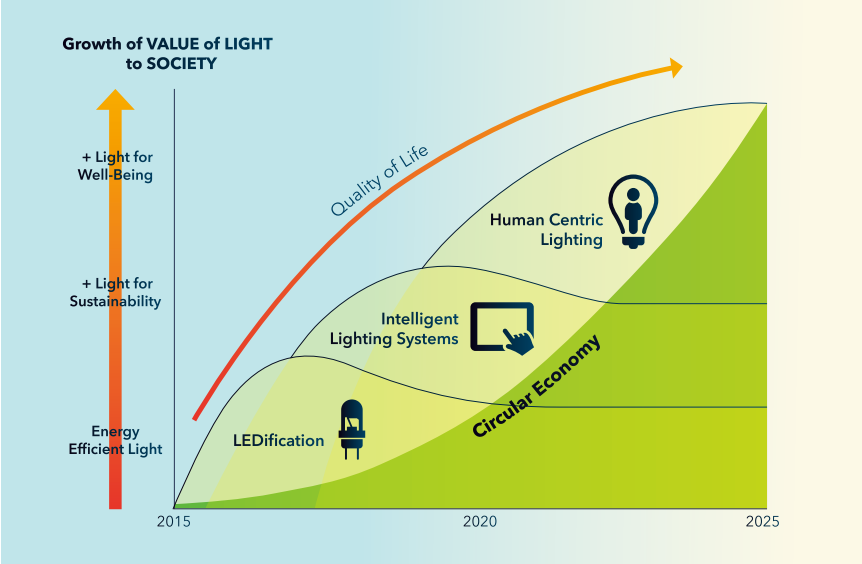


Figure 1.1: Strategic roadmap of the European lighting industry [220], [330].

and cognitive performance in offices and other workspaces [140], [266], [311]. Additionally, the spectral power distribution (SPD) of a light source influences the circadian response considerably regarding mood, performance and attention [20]. If the portion of emitted blue light is e.g. too intense, the human sleeping cycle might be affected, which could result in disruption of the circadian rhythm [23]. Beyond that, poorly designed LED drivers suffering from visible or non-visible flicker might induce possible health concerns [402]. Flickering is e.g. likely to cause headaches and migraines, may impair the performance of visual tasks and could potentially provoke seizures [210]. In summary, it is hence very important to ensure outstanding light quality in general lighting applications, such as residential, hospitality or office illumination.

The benefits of HCL are also applicable to many other scenarios, e.g. in hospitals [25], universities [20] or in the commercial sector for shop lighting. Especially industrial processes consider lighting as an important factor regarding job performance and safety [162] because severe accidents could be prevented by improving visual responses like detection, reaction time and recognition. Beyond that, various other applications also require a high technical light quality, e.g. optical imaging systems for medical purposes like endoscopes [31],

[334]. Particularly museum lighting represents a challenging task due to the demand for a high color rendering index (CRI) at low CCTs while maintaining good color uniformity [380]. If color precision, CRI or CCT specifications are not met, an illuminated object would look completely different, e.g. golden artifacts could appear rather silverish [59]. Also the automotive sector demands very good light quality in terms of uniformity, color precision and luminance control for the purpose of interior and ambient illumination of the cabin [29] or for new functions, such as display-like contour lighting [30]. In all these environments, adaptive lighting conditions have a significant impact and put strict requirements on the used light source. Summarizing the key challenges in future smart lighting finally leads to three major tasks that need to be solved simultaneously, namely

1. **Reduce energy consumption**
2. **Increase system intelligence**
3. **Enhance light quality.**

1.2 Scope of this Thesis

To enhance system performance of smart lighting systems, the three key challenges pointed out in section 1.1 should be considered in each step of new developments. Hence, this thesis focuses on the core component of a smart lighting system, the so-called *"smart LED driver"* in an intelligent luminaire. More precisely, the *"smart LED driver"* is composed of three main functional units that have been identified as crucial regarding the described key challenges. These central blocks are the communication system, the color control algorithm as well as the multi-channel LED driving stage. Fig. 1.2 highlights these blocks as a part of an intelligent lumianire and a smart lighting system. The communication interface is necessary to receive commands for dimming and color control as well as to enable intelligent features, such as automated light control, or sending status information, e.g. expected remaining lifetime, back to the user interface. Based on received commands and accessible information, the color control algorithm subsequently computes a relative intensity distribution and generates the corresponding control sequences for the individual LED channels. The multi-channel LED driving stages then translate their respective control sequences into action and regulate the associated current flow through the LEDs accordingly. In addition to these main components, integrated sensors may deliver relevant information that is worth of being transmitted back to a user interface or being processed in the applied control mechanisms of color adjustment and LED driving.

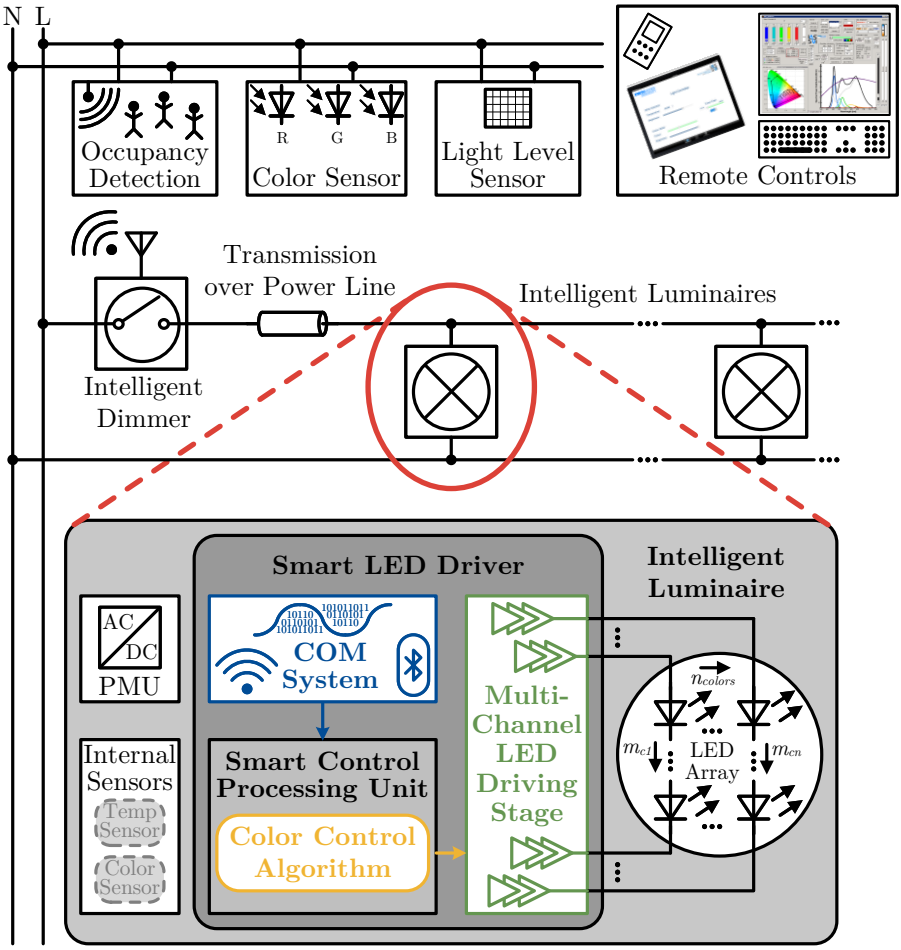


Figure 1.2: The scope of this thesis – A *"smart LED driver"* as part of an intelligent lighting system.

For each of the three mentioned functional units, single solutions and approaches exist addressing the key challenges of an effective *"smart LED driver"* as identified in section 1.1. Efficient concepts for LED driving stages realize efficiencies far beyond 90 % [122], [221], [289], while distinct color control approaches allow for full color flexibility [67], [338], [428] and bidirectional

communication systems offer intelligent features [101], [351], [352]. Very attractive single-inductor multiple-output (SIMO) LED driving stages have also been proposed by Dietrich *et al.* [102], by Hanhart *et al.* [138] as well as by Yang *et al.* [413]. These designs moreover optimize hardware demand, are fully monolithically integrated and achieve very high efficiencies of 96 %.

The main problem however is that great performance in one part typically comes at the cost of poor achievements in another functional unit, e.g. a high efficiency of the LED driving stage is bought for an imprecise color point stability and brightness control or even flickering of employed LEDs due to a large current ripple and limited switching speeds. In this context, a tailored system intelligence also plays an important role since most practical bidirectional wireless solutions suffer from high standby power consumption. Beyond that, conventional state-of-the-art color control approaches are extremely complex due to relying on additional hardware demands like color sensors [428] and (micro) spectrometers [72], [233] or because of employing very elaborate (thermal-electrical-luminous-chromatic) models while being limited to only three LED primaries at the same time [67], [338].

To the best of the author's knowledge, there is no balanced approach available addressing all three topics simultaneously giving an optimized system solution for an efficient *"smart LED driver"*. In addition to that, the performance of existing approaches can be further improved on two levels of profoundness. This thesis therefore tackles the described issues of *"smart LED drivers"* regarding power consumption, light quality and system intelligence on both, component and system level. The main idea driving this entire thesis is consequently attributed to the question,

Which measures can be taken to enhance, tailor and optimize *"smart LED drivers"* regarding

- **energy efficiency,**
- **light quality and**
- **system intelligence**

with energy-efficient electronics?

1.3 Aim of this Work

This thesis aims to pave the way for HCL applications by designing a tailored intelligent lighting system, which mainly founds on *"smart LED drivers"* according to Fig. 1.2. New control theories, circuit architectures and system concepts are consequently developed, studied and applied to the individual

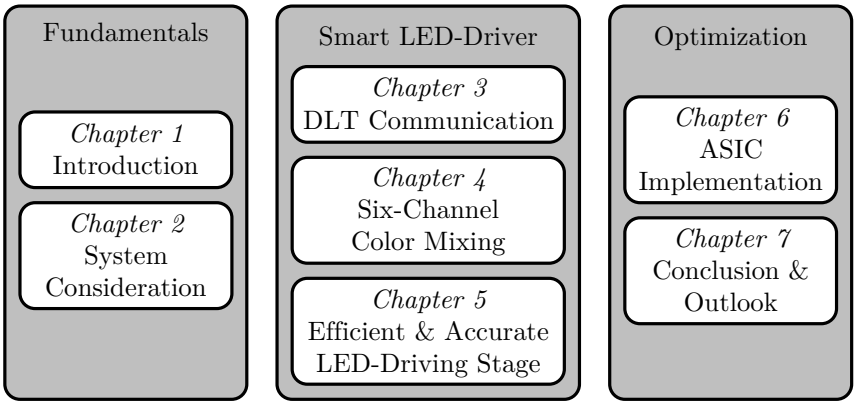


Figure 1.3: Outline and structure of this thesis.

building blocks of a *"smart LED driver"*. Thereby, current limitations, such as providing high energy efficiency at the expense of poor color rendering or vice versa, shall be overcome with energy-efficient and flexibly deployable electronics. The ultimate goal is to find an optimized approach solving the conflict of aims between high energy efficiency, precise color control and tailored system intelligence for future lighting systems creating excellent light quality and living comfort. Further important design aspects, such as robustness, complexity, size and costs are also considered in the proposed approaches and discussions.

Fig. 1.3 outlines content and structure of this thesis. Following a classic top-down approach, the system requirements of a *"smart LED driver"* derive the specifications for each block. Thereby, communication unit, color control algorithm and LED driving stage shall perfectly fit together. More details on the system considerations including fundamentals and a thorough literature research can be found in chapter 2. The central topic of this thesis is covered in chapters 3 to 5. Although the three main units are matched to one another, they shall be designed in a flexible manner. This approach targets easy interaction and assembly with other lighting systems, while keeping the outstanding performance of the individual blocks. The following paragraphs shortly introduce the three main blocks and highlight specific measurable aims for each of them. Further optimization could be reached on system level, which is exemplarily shown in chapter 6 on the basis of a monolithic integration. Chapter 7 finally concludes this work and provides an outlook to future research and possible improvements.

1.3.1 Communication System: Digital Load-Side Transmission (DLT)

Providing all kind of smart, energy saving and application dependent features an intelligent luminaire completely relies on its main communication system to translate user-specific or automatic control commands into action. In this context, Digital Load-Side Transmission (DLT) has been developed as a simple, unidirectional power line communication (PLC) technology with particular focus on intelligent lighting control [235]. Meeting the specific requirements of modern lighting systems, such as brightness, color and CCT control, DLT additionally provides low standby power consumption, high robustness as well as good compatibility with conventional wiring in existing installations [238], [243]. Thereby, it offers easy and efficient retrofit of standard switches, dimmers and lamps at low cost [106]. Consequently, the International Electrotechnical Commission (IEC) has recently promoted and established the DLT methodology as an official IEC standard [106]. Because of its favorable properties DLT is an interesting and attractive communication approach for intelligent lighting control that is worthy of being further investigated (chapter 3.1). Therefore, DLT has been selected amongst the huge variety of communication technologies as the employed lighting control system for the *"smart LED driver"* presented in this thesis. A detailed review of other communication techniques suited for intelligent lighting control is additionally provided in section 2.1.

Developing DLT compliant receivers for an intelligent luminaire is conducted with a special focus on being monolithically integrable in a system on chip (SoC) (chapter 3.2). This research part evaluates achievable performance of different DLT receivers regarding robustness, power consumption and circuit complexity. Beyond that, the further potential of the DLT approach is explored in detail. Thereby, corresponding challenges and weaknesses are identified, such as strict power supply limitations or the unidirectional communication capability. This thesis targets to develop effective concepts and solutions to overcome such limitations, which leads to improved efficiency and an increased system intelligence. Pursuing these aims this thesis proposes optimized circuit architectures for DLT power supplies delivering high output powers (chapter 3.3) to connect DLT to other communication systems like WiFi or ZigBee. Particularly, establishing a bidirectional communication (chapter 3.4), which extends the DLT methodology beyond the official standard, is valuable for realizing an integration into other smart home environments. By comparing functionality and performance with other potential communication techniques, this thesis seeks to find out, whether DLT can be an alternative to (low-power) wireless communication systems in future smart home automation.

1.3.2 Color Control Algorithm

Focusing on HCL applications, the achievable performance of an LED luminaire regarding brightness accuracy, color shift and other optical parameters mainly relates to two things: First, the electrical regulation of the LED current flow realized by a multi-channel driving stage as introduced in section 1.3.3, and second, the performance of the used color control algorithm. The color control approach determines the (theoretically) achievable brightness accuracy, color deviation and SPD by its computational resolution and the number of useable LED channels. State-of-the-art LED lighting systems however only use the minimal number of three LEDs required for full color control. In these systems, red (R), green (G) and blue (B) are typically taken as LED primaries to cover a large color gamut. In terms of generating white light this approach though creates adverse SPDs yielding low color rendering of illuminated objects. It is reported that adding supplemental LED primaries, particularly ones featuring a broadband spectra like white (W) or amber (A), significantly improves measurable light quality due to the additional degree of freedom [379]. Existing solutions of these tetra- and penta-color systems however suffer from high hardware complexity because relying on additional color sensors [427], [428], micro-spectrometers [72], [233] or elaborate models [67], [338].

This thesis targets at closing the identified scientific gap by developing a color mixing strategy that balances measurable color quality with employed hardware demand. CRI and color distances ΔE and $\Delta u'v'$ are chosen as performance metrics to quantify light quality. The acceptable limits of CRI > 90 [114], $\Delta E \leq 3$ [432] and $\Delta u'v' \leq 0.0035$ [99], [408] shall thus be maintained. To achieve minimum color shift and an optimization of the optical emission spectrum, the presented color control algorithm (chapter 4.1) must be capable of controlling more than four LED channels. It copes with different optimization criteria, such as maximum CRI, luminous output or efficacy, while keeping the perceivable color shift at a minimum. Additionally, the color control approach changes emitted luminance L_v independently of the color selection by applying PWM dimming and accounts for the highly nonlinear relationships of human brightness and color perception (chapter 4.2). Still, it is aimed to keep the color control strategy flexible for deployment in other systems using AM-, bilevel- or hybrid-dimming techniques. Although the color control algorithm includes these complex requirements and computations, it shall be implemented in a simple manner, e.g. on a tiny microcontroller (μC) (chapter 4.3). Beyond proposing an enhanced color control methodology, this thesis investigates further improvement methods (chapter 4.4). Functionality and achievable performance shall finally be proven by means of simulation and measurement results (chapter 4.5).

1.3.3 LED Driving Stage

The LED driving stage is a key component for both, optical performance and electrical efficiency. Due to the (nearly) linear relationship between emitted luminance and LED forward current, most LED drivers are typically designed to control the average current flow [251]. The regulation accuracy of the LED driving stage thereby directly impacts brightness variations and color point stability. Aiming to minimize any color shifts, this thesis targets to keep LED current flow variations below a tolerance of $\pm$ 3 % even under dimming operation. While dimming functionality is an essential feature of the LED driver, PWM control is preferred over amplitude modulation (AM) due to a more linear brightness profile in dependence of average forward current [245]. A pulse-width modulation (PWM) based LED driving stage requires fast turn-on and turn-off times because the switching behavior impacts dimming resolution and minimum adjustable brightness level. In total, the PWM switching must be fast enough to realize dimming levels well below 1 % in order to ensure high dynamic contrast ratios and hence precise color control. In addition, different studies reveal that the size of the LED current ripple as well as the current waveform can significantly impact the targeted color point [7], [68], [403]. Color variation can e.g. easily occur, if the ripple size changes [245]. In the end a (large) current ripple makes color accuracy hardly controllable and should consequently be as low as possible so that the average current can be controlled precisely [26], [62]. This matter implies a completely flat current waveform in an ideal case. Due to these stringent requirements on color and brightness accuracy, switching converter architectures, which typically provide very good efficiencies but feature comparatively high current ripples, may not be applied. Beyond that, these solutions suffer from a duty-cycle dependent current error, which further increases color shift deviations.

To find a suitable trade-off between the initial key challenges light quality and energy-efficiency, an LED driving stage with dynamic headroom regulation [74], [153], [230] is evaluated as most promising for the targeted application (chapter 2.3.3). This thesis therefore selects the adaptive voltage control approach as a system level solution and moreover focuses on further improvements of this concept (chapter 5). It is aimed to enhance electrical efficiency ($\eta > 90\,\%$) over a wide dimming range by introducing a digitally assisted control to the dynamic headroom regulation concept (chapters 5.1 and 5.2). As an additional constraint, this approach shall be implemented with maintainable hardware effort (chapter 5.3). The aforementioned objectives shall finally be met and proven by measurement results of the developed hardware implementation (chapter 5.4).

1.3.4 System Optimized ASIC Implementation

Monolithic integration of the proposed new concepts and ideas offers the potential to further improve performance of the *"smart LED driver"* (chapter 6.1). Beyond that, it features other advantages regarding industrial aspects, such as enabling small form factors and low cost solutions for a broad mass market. The color control algorithm may be realized either internally on the application-specific integrated circuit (ASIC) or on an external μC. In the latter case, the ASIC must yet provide a communication interface, such as UART or I^2C, to ensure proper alignment of the color control with the other two main functional blocks. The developed circuit architectures for DLT communication only need minor modifications (chapter 6.2), as they have already been designed for an IC implementation (chapter 3).

Regarding an improved ASIC solution, this thesis focuses on the LED driving stage. Especially, energy-efficiency is expected to increase by designing a tailored switching pre-regulator (chapter 6.3) as conducted in [313]. Additionally, the feedback network of the dynamic headroom regulation shall be integrated to enhance overall LED driver efficiency. Beyond that, an all digital current control using a sense-FET based approach is introduced to further boost efficiency, while maintaining a precise current regulation mechanism (chapter 6.4). Since its main control resides in the digital part, this solution aims to provide higher flexibility, e.g. by implementing AM as well as PWM dimming operation, which enables bilevel (BL) and hybrid dimming strategies.

1.3.5 Definition of Specific Measurable Aims

A *"smart LED driver"* suited for multicolor illumination systems needs to provide the following feature set:

- A high (system) efficiency with low standby power consumption.
- Dimming functionality with high contrast ratio.
- Full color control and CCT adaption with high accuracy.
- Accurate LED current flow regulation.

Approaching these objectives on both circuit and system level, Tab. 1.1 defines specific, measurable goals for each functional unit that shall be targeted within this thesis. The subsequent aims have thus been defined in compliance to the three key challenges based on a thorough literature review and derivation of system requirements (chapter 2).

Table 1.1: Summary of specific, measurable goals to be achieved within this work.

Goal		Goal Description	Indicator
Digital Load-Side Transmission	1	Propose integrable DLT CG concept with robust FW-RXs and low (standby) power consumption	$\text{TER}_{FW} \leq 1\,\%$ $P_{FW\text{-}RX} \leq 50\,\text{mW}$
	2	Enable wireless accessibility for DLT CDs with decent power efficiency	$\eta_{CD} \geq 50\,\%$
	3	Extend DLT towards bidirectional communication with robust REV-TX and REV-RX concepts at lowest possible power consumption	$\text{TER}_{REV} \leq 1\,\%$ $P_{REV,total} \leq 50\,\text{mW}$
Color Control	4	Develop multi-channel color control algorithm for more than four channels optimizing color quality with high CRI and low color shift deviation	$N_{LEDs} \geq 4$ $\text{CRI} \geq 90$ $\Delta E \leq 3$ $\Delta u'v' \leq 0.0035$
LED Driver	5	Conceptualize dimmable LED driving stage balancing efficiency and high current accuracy	$DIM_{min} \leq 1\,\%$ $\eta_{LED,DRV} \geq 90\,\%$ $\Delta I_{LED} \leq 3\,\%$
	6	Design an ASIC based *"smart LED driver"* with improved efficiency and similar current accuracy	$DIM_{min} \leq 1\,\%$ $\eta_{LED,DRV} \geq 95\,\%$ $\Delta I_{LED} \leq 3\,\%$

Chapter 2

System Considerations for a Smart LED Driver

Analyzing the main challenges in future lighting systems, the introduction chapter 1 identifies the *"smart LED driver"* as a key component, which is investigated in depth by means of this thesis. Communication system, color control approach and LED driving stage thereby represent the core building blocks to be enhanced and optimized applying novel control theories, circuit techniques and conceptual approaches. In order to capture the state-of-the-art for these individual building blocks, this chapter gives a résumé about the theoretical background, relevant fundamentals and existing solutions including a thorough literature research. In doing so, it exposes essential demands, impacts and inter-dependencies of the three functional units with respect to targeted system performance. Chapter 2.1 thereby looks into different communication systems, whereas chapter 2.2 outlines the fundamentals of color mixing and control. Beyond that, chapter 2.3 provides the theoretical background on LED driving circuits and studies existing concepts. Pursing the goal of achieving

high energy efficiency, excellent light quality and tailored system intelligence at the same time, a system analysis eventually summarizes identified performance criteria from these different areas and balances associated needs. By this means, the main functional units shall on the one hand perfectly fit together yielding an optimized *"smart LED driver"*, and remain on the other hand flexibly deployable to other lighting systems. Section 2.4 precises these findings and defines specific interfaces between the three core building blocks. Subsequently, clear target requirements and related boundary conditions are deducted for each functional block – also with respect to a monolithic integration. This method enables this thesis to seek for improvements on both, component and system level.

2.1 Review of State-of-the-Art Communication Methodologies for Intelligent Lighting Control

The idea of intelligent lighting control is to adopt brightness, color or color temperature (CT) of installed light sources according to user inputs, predefined events or surrounding conditions. A robust communication system is consequently required to transmit and receive the corresponding control commands and it furthermore offers the integration of distributed active sensor nodes. Applying adaptive algorithms an intelligent lighting control thereby realizes additional features using presence and occupancy detection as well as measuring light intensity levels and daylight distribution [49], [50], [278], [287]. Intensity, location and time of illumination can hence be controlled precisely in order to enable power savings on system level or to create higher user satisfaction and comfort [235], [332]. A proper communication system is thus not only inevitable for increasing energy efficiency but also helps to develop and optimize lighting towards HCL control strategies. In summary, the main task of a communication system for intelligent lighting control is to transmit and receive control commands for an intelligent luminaire as well as to send status or sensing information to a smart processing unit.

Intelligent lighting control may actually be seen as a subset of a smart home area network (HAN). The requirements on the respective communication technology thus resemble each other very much. From a general perspective the communication related demands can hence be deduced by pursuing a broader literature review. It might also be reasonable to look into other smart grid applications, like building area networks (BANs) or neighborhood area networks (NANs), which is however not the primary focus of this thesis. In depth studies and a broad overview on smart grid communication infrastructures and home automation are provided in [133], [169], [194]–[196], [412].

Generally, home automation control requires comparatively low data rates [53], which is hence not a critical constraint for smart lighting control. In fact, very simple control commands, which only need a few dozen bytes per second, can be used for brightness adaption, color adjustment or CT settings and are thus completely sufficient for the target application [97], [196]. In the context of intelligent lighting control, the most important requirements of a communication system are high robustness and low power consumption [196], [257]. Robustness or rather reliability is considered to be greater than 98 % in smart home and building communication systems [196], [199]. Also, ease of use and featuring a low latency play a substantial role to ensure high user acceptance. While latencies of up to 200 ms are not recognizable by human beings, delays of 300 ms to 400 ms might still be tolerable since human simple reaction time is in that range [1], [131]. For home automation systems latency is actually defined more relaxed in the range of several seconds [195], [196]. Considering commercialization, conceptual aspects like (hardware) effort, costs and complexity have to be taken into account as they might also affect robustness and power consumption of the used communication device.

In terms of power consumption it needs to be distinguished between active power consumption P_{TRX} for transmit and receive actions as well as standby power consumption P_{stdby}, when the system is switched off or in sleep mode, and to some extend power consumption during idle times P_{idle} with the communication system being powered but not communicating. Light sources might indeed be switched off for a comparatively long time during the day. Consequently, standby power consumption becomes an even more important topic, which is not limited to the communication device alone but affects the entire intelligent luminaire. The actual power-on time however depends strongly on application scenario and surrounding conditions. Workplace illuminations in offices or industrial environments might require much longer turn-on times than the cosy, low intensity ambient lighting of a living room. Additionally, intensity and CT of available sunlight, cloudy weather conditions or natural lighting in variation of the season cycle influence the need of different dimming levels or switch-on times. Typically lighting is indeed used between 7 h to 13.5 h in common use cases of homes and offices [14], [420]. Beyond that, brightness, color or CT changes do commonly not happen very often, once a user has set ambient and general lighting conditions according to his desires. This aspect, can indeed be used for further power optimization, particularly in regard to the communication system, e.g. by minimizing idle power consumption or even bringing the communication device into a low-power standby mode. Nevertheless, low latency and high robustness must of course be maintained.

In literature, different approaches from wireless systems like ZigBee [46], [125], [136], [155], [257], Bluetooth [78], [294] or Wireless Fidelity (WiFi) [165], [176], [414], [434] up to modern PLC methods, such as othogonal frequency-division multiplexing (OFDM) based systems [185], [254], P-BUS [214] or digitalSTROM™ [101], have been proposed as suitable solutions to home automation and intelligent lighting control [243]. Meanwhile, there are many different communication systems and flavors available in the market. A general overview and comparison of the different communication techniques in the context of smart home control is provided in [134], [196], [263]. Particularly wireless solutions are recently becoming predominant in intelligent lighting control because of featuring a good ease of use and compatibility to existing installations. On the other hand, wireless communication techniques are usually more complex than PLC methods or other wirebound systems [214] and thus might require additional hardware effort. The subsequent sections therefore expound different state-of-the-art communication systems that are suitable for intelligent lighting control, while section 2.1.3 compares these communication approaches and highlights individual assets and drawbacks, particularly regarding power consumption, robustness and complexity.

2.1.1 Wireless Communication Systems

Referring to wireless control systems in home automation and intelligent lighting, the most relevant communication techniques are ZigBee, Bluetooth and WiFi, which are all well described by the respective IEEE standards 802.15.1, 802.15.4 and 802.11, respectively [204]. While these IEEE protocol definitions only specify physical (PHY) and medium access control (MAC) layers for wireless communications over an action range around 10 m to 100 m [204], independent alliances may further rate additional network, security and application layers [97], [204]. Still, all wireless communication protocols under investigation operate in the 2.4 GHz industrial, scientific and medical (ISM) radio band, although featuring different frequency channels, modulation schemes, data rates and hopping patterns [24], [97]. Beyond that, IEEE 802.15.4 and IEEE 802.11 also specify other frequency ranges in different subsets of the respective standards.

Of course, there are also a lot of other communication standards and methods available, which are suitable for intelligent lighting control. These techniques might even use other transmission frequencies, e.g. LoRaWAN operating in the 433 MHz and 915 MHz ISM bands as well as in the 868 MHz short range device (SRD) band. Z-Wave, Enocean and Insteon are also well-known communication systems used in home and building automation or for industrial applications. Likewise, WirelessHART, SUN, 6LoWPAN and Thread, which all found on the

IEEE 802.15.4 communication standard, are applicable to home automation control and smart grid applications. Recently, a new wireless communication method called visible light communications (VLC) is penetrating the market for intelligent lighting control. It offers low-cost broadband communication while exhibiting a high degree of spatial reuse [167]. Reusing LED lighting fixtures as a communication device, VLC systems emerge many new and interesting applications [186] while reducing hardware effort by this dual function. Although IEEE 802.15.7 standardizes high data rate and flicker-free VLC, supporting of dimming functionality and flicker avoidance are still the main challenges for this communication technology [302].

Finally, Bluetooth, ZigBee and WiFi represent the most common and mostly deployed wireless protocols that are used in today's lighting control networks. The subsequent paragraphs therefore give a brief introduction to these three particular communication methods, which are considered as benchmark technologies in this thesis with respect to the utilized DLT approach.

Bluetooth

Bluetooth has been developed in the late 1990s by the Bluetooth Special Interest Group (SIG) for short range wireless transmission of voice data, images and data files [97], [115]. Thereby, it was initially meant to replace cables for computer peripherals and functions as a wireless personal area network (WPAN) at the vicinity of around 10 m [24], [204]. Ferro and Potorti [118] provide a concise overview and description of Bluetooth history, operation and protocol definition. A Bluetooth WPAN is called *"piconet"*, which operates in a star-connected master-slave structure. Within these small ad-hoc networks, one master may communicate with up to seven slaves. Synchronization is achieved by sharing the master's clock. Combination and overlapping of multiple piconets is not only possible but defines the second connectivity topology in Bluetooth called a "scatternet", which consequently enables multihop wireless networks. Thereby, a Bluetooth device may participate as a slave in several piconets at the same time, while it can be the master in only one of them [204].

Bluetooth subdivides the ISM radio band ranging from 2.4 GHz to 2.85 GHz into 79 designated channels, each featuring a bandwidth of 1 MHz. For robustness reasons, the IEEE 802.15.1 protocol uses frequency hopping, which changes the transimssion channel 1600 times per second. Bluetooth features an asynchronous connectionless link (ACL), which guarantees high reliability by means of an automatic repeat request (ARQ). Additionally, forward error correction (FEC) is applied to protect packets against bit errors. A packet is composed of a 72 bit access code for synchronization and identification, a 54 bit

header and a flexible payload of up to 2745 bit [33], [97]. Further information on Bluetooth can also be found in the current *"Bluetooth Core Specification"* [33], which describes different configurations, such as low energy (LE) or enhanced data rate (EDR), in addition to the above outlined basic rate (BR).

Particularly Bluetooth Low Energy (BLE) is interesting for smart lighting control as this subset reduces implementation cost and power consumption [97]. BLE thus limits the data rate to a possible maximum of 1 Mbit/s and shortens data packet size [97]. Consequently, the number of available channels is reduced to 43 in BLE each featuring a channel width of 2 MHz [321]. Low power consumption is achieved because master and slave devices sleep most of the time and data transmission is organized by so-called *"connection events"*. After discovery of a slave by the master scanning three designated advertisement channels, both devices wake up synchronously and exchange frames [321].

ZigBee

The 2002 formed *"ZigBee Alliance"* – a consortium of several industrial companies – developed the ZigBee communication technology based on the IEEE 802.15.4 standard and promotes it as a low cost, low power consumption alternative to Bluetooth [115]. The main target in ZigBee development was to address communication demands in home automation, remote monitoring and industrial control applications. Although the ZigBee architecture is similar to that of Bluetooth and WiFi, it shows lower complexity regarding protocol implementation, lower latency and a reduced data rate [115]. Operating in the 2.4 GHz ISM band, ZigBee achieves data rates of 250 kbit/s for distances of up to 75 m [24]. ZigBee defines 16 channels in the 2.4 GHz band of 5 MHz bandwidth each [417] and transmits data packets with a maximum payload of 127 byte called PHY service data unit (PSDU). Preceding the payload data, a 32 bit long preamble followed by a start-of-frame (SoF) delimiter byte and a second byte denoting the frame length completes the transmission packet [24].

For complexity, power consumption and cost reasons ZigBee defines two types of devices in its network topology, a full function device (FFD) and a reduced function device (RFD). The FFD implements the full protocol stack and all required ZigBee functions, whereas an RFD manages minimal functionality and supports only certain protocol parts [24], [97]. The low power ZigBee WPAN is structured in either a star or peer-to-peer topology with up to 254 participating nodes and one FFD serving as the network coordinator. More complicated topologies, such as a cluster-tree network, may be realized by combining one or more star configured networks with peer-to-peer groups, which guarantees high flexibility regarding network configuration.

Robustness against noise, distortions or interference is achieved on different levels. Applying direct sequence spread spectrum (DSSS) modulation technique protects transmission against narrowband interference, while carrier sense multiple access with collision avoidance (CSMA/CA) prevents two or more stations to transmit simultaneously [24], [97]. Beyond that, the ZigBee protocol accounts for a so-called frame check sequence, which is included in the PSDU and will in addition be independently calculated by the receiver. The receiving side only sends an acknowledgement (ACK) back, if these two frame checks match, which finally terminates the transmission. Otherwise, the transmitting side will continue to send its message until it receives the ACK.

Wireless Fidelity (WiFi)

Founding on the IEEE 802.11 standard, Wireless Fidelity (WiFi) represents the predominant industrial standard for wireless local area network (WLAN) equipped products and devices and is continuously being updated by IEEE working groups [24]. Meanwhile there are many different versions and supplements available, each providing various data rates and modulation schemes. WiFi is actually designed for very high data rates in local area networks (LANs) [97], which yields increased complexity and power consumption. While the original IEEE 802.11 standard achieved only about 2 Mbit/s, its predecessor IEEE 802.11*b* already enabled 11 Mbit/s. On the contrary, more recent supplements provide data rates of 54 Mbit/s (IEEE 802.11*g*) and 300 Mbit/s (IEEE 802.11*n*). Moving to the 5 GHz band, the most recent versions even enable data rates in the gigabit range.

In the 2.4 GHz band the IEEE 802.11 standard defines 13 overlapping 22 MHz frequency channels [417]. Channel access is also organized by CSMA/CA method, while different techniques like DSSS, frequency-hopping spread spectrum (FHSS) and infrared (IR) are used to deal with frequency-selective interference depending on the protocol supplement [97]. The network architecture of WiFi is very flexible and founds on the so-called basic service set (BSS) as its core building block [24]. A simple BSS achieves a top range of about 100 m [97]. Applying extended service set (ESS) more complicated network structures and wider transmission ranges can be realized using portals and access point connections [97]. More detailed information on WiFi, its specifications and implications may be found in [24], [159], [160].

2.1.2 Wire-Bound Communication Systems

Beyond wireless solutions, there is also a broad variety of wire-bound communication systems available that can be applied to lighting control and home

automation. Typical examples in this context are Digital Adressable Lighting Interface (DALI) [142], [191], [217], Controller Area Network (CAN) bus [100], [206], [381], Konnex (KNX) [264], [288] and (Power over) Ethernet [137], [184]. A brief overview of common communication approaches, systems and standards – including wireless solutions – is given in [96], [130], [196], [389]. Particularly, KNX and DALI are often used in wired smart homes and lighting controls due to their high robustness and flexibility. While KNX is a worldwide standard for building automation, DALI has been specifically developed for lighting control. Meanwhile, DALI is however adapted in many other applications, such as fan controllers or proximity alarms [21]. Several gateway solutions exist combining DALI with wireless (sensor) networks [21], [108] or KNX with ZigBee based systems [129], [209], [405] to create more powerful smart home environments and a better ease of use for end customers. Beyond that, also other popular wire-bound communications exist like BACnet and LonWorks® [264] used in home automation or DMX512 [166], [223] for stage lighting.

However, all of these systems require additional wiring for their data transmission. Considering compatibility to existing installations, this demand represents indeed a major drawback regarding ease of use because it involves elaborate and costly construction or replacement measures. The extra cabling itself already increases installation costs. Since luminaires have to be attached to mains voltage anyways, it is hence more favorable – particularly in terms of retrofit solutions – to utilize a PLC technology that transmits data over the supply voltage line. Besides briefly introducing DALI and KNX as well known wire-bound communication systems, the subsequent paragraphs highlight PLC methods with special emphasis on the digitalSTROM™ approach.

Digital Adressable Lighting Interface (DALI)

The DALI protocol has been developed as a specific standard for digital communication in smart lighting control aiming to create low cost systems that are easy to handle [87]. It is specified in IEC standard 60929 under Annex E [157]. Operating in a master-slave structure a DALI network can handle up to 64 devices due to the limited address range, while further extension is possible via gateway connections. Both, single-master and multi-master configurations, are possible in star-shaped, serial connection and mixed structure topologies [87]. Thereby, DALI realizes single device and group control mechanisms. Using Manchester coding for error detection, DALI transmits its data with a fixed rate of 1200 bit/s over a two wire bus [142]. A beneficial feature is the specified DALI dimming curve, which covers a range from 0.1 % to 100 %. DALI thereby defines a logarithmic dimming behavior to compensate for the human perception

as outlines later in section 2.2.2. Further information including hands-on and practical manual instructions can be found in [87], [142], [143].

Konnex (KNX)

The KNX technology founds on the former European Installation Bus (EIB) extended by protocol parts of BatiBus and European Home Systems (EHS). It has been developed as an industrial building control system realizing automated functions and processes. KNX employs the twisted pair cable configuration as selected transmission medium [264], which enables relatively low cost and high robustness. Meanwhile there are also other KNX variants available, which are e.g. for communication over PL, RF, Ethernet or fiber optics.

In twisted pair configuration the data is transferred as a differential voltage signal with a transmission rate of 9.6 kbit/s. KNX distinguishes two frame types, which are a data frame and an acknowledgment frame. The acknowledge message type is only one byte long and used to confirm, whether the data frame has been received correctly at the corresponding end device. Besides the payload data, a data frame contains several other bytes, such as source and destination addresses, priority, routing counter, data length and a checksum field. For error detection purposes KNX employs a double parity check, which is called *"block parity"*. Since error correction is not performed, the data needs to be resend in case an error occurs or a negative-acknowledgement (NACK) command is send back in the acknowledgment frame. To avoid channel access problems when multiple devices try to send data at the same time, KNX utilizes the CSMA/CA technique. More detailed information on frame structure and the way KNX transmission operates can be found in [264]. The KNX network topology conventionally follows as a tree structure, which distinguishes certain hierarchy levels. On the lowest level, up to 64 nodes can be connected to a line segment, of which a maximum of four form an entire line. A so-called main line connects up to sixteen entire lines forming an area. Multiple areas, more specifically a maximum of sixteen, may be linked with each other over the backbone line [264]. The KNX address range therefore provides 16 bit, which allows to attach $2^{16} = 65536$ nodes in total.

Power Line Communication (PLC) Systems

The key idea of PLC is to use existing cable infrastructure for dual purposes, which are transmission of energy on the one hand and data communication on the other hand [117], [303]. Arising in the beginning of the 20th century, PLC was developed with a primary focus on load management and meter reading from distance [117] but also for distribution automation and demand side

management [303]. Nowadays, many other applications, such as energy management in buildings [327], smart home automation [90] and high-speed power line LAN [226], have become very attractive for PLC networks due to recent advances in modulation methodologies, digital signal processing, error detection and error correction [226], [422]. Spread spectrum technology has e.g. been applied to the well-known X-10 PLC system for home automation in order to increase speed by a factor of 100-150 [320]. Using the OFDM modulation technique the initial version of *"HomePlug 1.0"* published in 2002 already realized data rates of 14 Mbit/s [207], [226]. More recent subsets, such as *"HomePlug AV"*, achieve transmission rates between 150 Mbit/s to 200 Mbit/s [421]. In terms of data rate broadband PLC systems are meanwhile comparable with WiFi and domestic Ethernet [54] as commercial PLC modems reach speeds of 500 Mbit/s [16]. PLC methods are distinguished between ultra-narroband (125 Hz-3 kHz), narrowband (3 kHz-500 kHz) and broadband (1.8 MHz-100 MHz) techniques [54]. Furthermore, the transmission medium, which is the power line itself, is classified into three major voltage domains, namely high voltage (HV) (>100 kV), medium voltage (MV) (1-100 kV) and LV (<1 kV) [117]. Smart home PLC systems obviously operate in the LV domain. A general overview on PLCs, its principles, challenges and applications is provided in [54], [117], [198], [422]. Yousuf, Rizvi, and El-Shafei [421] briefly list common PLC standards and systems while mainly focusing on the dominating *"HomePlug"* standard. More information on HomePlug 1.0 is also provided in [207]. Beyond that a requirement study for PLC in smart grid applications proposing different transmission concepts is published in [44].

Although providing distinct cost advantages due to using the existing wiring infrastructure, PLC faces some severe challenges because power lines were initially not designed for communication and hence represent a difficult environment with excessive noise levels [117]. Typical loads that are connected to the AC grid, such as SMPSs, generate e.g. high frequency distortions, which may actually interfere with PLC systems [90]. Moreover, PLC signals suffer from a frequency-dependent attenuation due to the non-shielded cabling, which increases at higher frequencies [422]. Additionally, impedance mismatch occurs in the electrical network so that PLC signals may experience a varying impedance, which leads to various reflections and complex echo scenarios for high frequency signals [128]. The resulting fading effect superimposes the aforementioned attenuation [128]. Thus, a low pass characteristic can be observed at all power line links, which becomes crucial for high frequency, high-speed systems or if cables exceed a length of about 300 m [128]. The main issues in PLCs are described and summarized in a very concise manner in [422]. To counteract on these harsh surrounding conditions and develop robust PLC

systems, various studies provide detailed modeling of the transmission channel and noise characteristics [117], [128], [164], [391].

Still, high data rate PLC approaches using OFDM suffer however from interference caused by LED luminaire power supplies [95] and might require circuitry of relatively high complexity. As figured out in the beginning of section 2.1, a low data rate is by far sufficient in intelligent lighting control. Therefore, employing a low frequency PLC approach is indeed more beneficial for LED lighting applications. In addition, LED power supplies emit less noise on lower frequencies [95]. Besides the Digital Load-Side Transmission (DLT) approach that is investigated in depth by this thesis, there are also other interesting and suitable solutions available, such as P-BUS [214] or digitalSTROM™ [101]. The P-BUS system is yet limited to operate on low voltage DC power only. digitalSTROM™ on the contrary operates to some extend similar to DLT and is therefore described more detailed in the following.

digitalSTROM™

The digitalSTROM™ topology is a centralized communication approach, which defines so-called digitalSTROM™ meters (dSMs) and digitalSTROM™ devices (dSDs) [101]. One dSM, which is situated behind the circuit breaker in the distribution board, connects to a maximum of 128 dSD nodes. Multiple dSMs, each controlling its own dSDs on a single phase, are connected via an RS-485 bus and may be accessed over a local server unit called digitalSTROM™ server (dSS). The system topology is outlined to minimize cross-talk between different phases and neighboring circuits [101].

The downstream communication from dSM to dSD is realized over two voltage pulses, one at the beginning and one at the end of the half-wave close to the zero crossing of mains. Employing a simple on-off keying (OOK), the system considers the absence of a pulse as logic zero (‘0’) and the presence of a pulse as logic one (‘1’) [101]. Considering the 50 Hz European Union utility grid digitalSTROM™ achieves transmission rates of 200 bit/s, which is claimed to be sufficient for home automation control because the total system throughput scales with the number of dSMs [101]. A (7,4)-Hamming code extended by an additional parity bit is used to detect or even correct isolated errors [101]. Upstream communication, which runs vice versa from dSD to dSM, employs a current source as its transmitter and uses spread-frequency-shift keying (S-FSK) with two sets of carrier frequencies. The transmit current of 35 mA is used, while the transmission timeslots are limited within the proximity of the mains zero crossing [101]. More detailed information on the digitalSTROM™ topology can be found in [101], [113] or on the webpage `https://www.digitalstrom.com/`.

2.1.3 Assessment and Comparison of Communication Technologies Suited for Intelligent Lighting Control

The previous sections introduced different communication techniques suitable for intelligent lighting control, each featuring individual performance metrics and degrees of complexity. The choice of communication technology indeed strongly depends on requirements of the targeted application regarding power consumption, robustness and latency, range, data rates, maintenance, ease of use or even security features. Summarizing the conducted literature review on wireless and wire-bound communication methods, four key systems are identified to serve as a benchmark for the Digital Load-Side Transmission (DLT) approach investigated in this thesis. These systems are Bluetooth, ZigBee, WiFi and digitalSTROM™. Conventional wire-bound systems like DALI or KNX are disregarded due to the high effort and costs associated with the extra wiring infrastructure. Still, it should be noted that these systems feature a high degree of reliability, almost unlimited extensibility and high data transfer speed [191], [264]. Beyond that, other OFDM-based PLC methods, such as the HomePlug standard, involve relative high complexity for circuit and hardware implementation. Because the associated high data rates are not needed for a simple lighting control system, the usage of a complex OFDM-based PLC would only unnecessarily increase the costs and also power consumption. Therefore, the evaluation conducted in this thesis does also not include these approaches.

Since the four mentioned communication methods were initially designed for different target applications, it appears difficult to compare them to one another and also later to the DLT approach. A current literature review however reveals that at least different comparisons among the mentioned wireless communication techniques have been carried out. A general comparison on low power wireless technologies is e.g. provided by Smith [325], whereas Ferro and Potorti [118] present a concise comparison of WiFi and Bluetooh on protocol level. A contrasting juxtaposition on a relatively high level between BLE and ZigBee can be found in [225]. Cordova *et al.* [80] even include the HomePlug standard in their high level comparison of ZigBee and WiFi. Lee, Su, and Shen [204] compare Bluetooth, UWB, ZigBee and WiFi regarding power consumption, transmission time, data coding efficiency and protocol complexity, while Lee, Dong, and Sun [203] analyze BLE and ZigBee with respect to transmission time, data coding efficiency, power consumption and delivery ratio. Regarding power consumption comparative measurements of BLE and ZigBee over IEEE 802.15.4 are presented in [321], while Thomas, Wilkie, and Irvine [378] contrast BLE with WiFi inbuilt internet of things (IoT) devices. Shahzad and Oelmann [314] even provide a detailed analysis of the

power consumption of BLE, ZigBee and WiFi in dependence of the transmitted payload data and Ferro and Potorti [118] compares Bluetooth and WiFi also in terms of power consumption. Other studies investigate the mentioned wireless communication methods regarding specific environments and target applications like home automation [88], indoor location [431] and indoor positioning [228], smart grid or industrial utilization [13]. Another interesting analysis and comparison with special emphasize on power consumption has been conducted in [190], which includes the digitalSTROM™ approach and several other wireless systems, like Z-Wave, HomeMatic, Delta Dore, Trådfri or TP-Link.

Finally, all techniques can be assessed with respect to the target specifications derived in the beginning of section 2.1. Complexity, robustness, latency and power consumption have thereby been identified as the most important criteria. Other demands, such as minimum required data rate, access range, low maintenance, good ease of use and security, are all evaluated as more than sufficient for the communication methods under test in regard to lighting control tasks.

Complexity

Simple PLC techniques typically feature lower circuit complexity than any low power wireless solution [97]. This circumstance also holds true for the digitalSTROM™ approach as it only uses simple OOK for data modulation on mains voltage in case of the downstream communication. Upstream communication is realized a little bit more complex employing Spread-frequency-shift keying (FSK) modulation on the AC current flow but remains still much simpler than the modulation techniques of ZigBee, WiFi and Bluetooth (Low Energy). Since the digitalSTROM™ topology provides the opportunity of realizing a complete home automation system, it comes with a certain degree of complexity and additional hardware effort regarding wiring and component usage on the distribution board. This is because every dSM requires a direct link to a dedicated server interface (dSS), which connects to the home LAN or the internet, over an RS-485 bus [101]. Out of the four evaluated communication techniques the digitalSTROM™ approach features lowest circuit and system complexity.

Although WiFi offers the highest coding efficiency [204], it is the most complicated technology to integrate into a system because it requires various drivers, a full protocol stack and needs to be designed with tight tolerances in order to meet the specified performance [325]. Furthermore, WiFi is somehow over-dimensioned for low data rate applications like lighting control as it comes with a minimum protocol overhead of at least 58 bytes [97], [204]. BLE and ZigBee show comparable complexity with a slight advantage for the ZigBee solution. For further details please refer to the above mentioned studies.

Robustness and Latency

As pointed out earlier, wire-bound communication systems generally offer higher reliability and range than wireless solutions at comparatively low complexity [97]. In terms of PLC approaches this is only partially true due to the harsh surrounding conditions and excessive noise levels as explained in the PLC systems paragraph. Typical distortions and interference may arise from switched electrical loads, which can be either asynchronous, like user-switched devices, or synchronous to mains voltage, such as switched-mode power supply (SMPS) devices [101]. Additionally, large inrush currents at the start-up of plugged devices and ripple control systems may also cause interference and noise on the power line. The digitalSTROM™ technique has been evaluated as very robust and reliable to these distortions, which is shown in the corresponding paper discussion providing one-shot measurements of typically disturber scenarios [101] and a worst-case condition measurement. It should however be noted that a long-term measurement evaluation is missing so that an effective bit error rate (BER) could not be determined. Expecting only very little amount of payload data for each command transmission due to a low complexity protocol for simple control commands, latency should not be major concern in a digitalSTROM™ system although the data rate is only about 200 bit/s.

Except for the Bluetooth BR configuration all low power wireless communication systems feature very low latencies, which are by far sufficient for the described lighting application. Considering an initially sleeping slave BLE achieves latencies around 6 ms, while ZigBee shows similar performance of about 15 ms [13], [97]. Latency in WiFi is evaluated as only about 1.5 ms [325]. Thus, latency is not a concern for the wireless approaches as it is by far lower than the targeted 300 ms to 400 ms. However, reliability on the other hand is a critical concern because all wireless communication protocols under investigation operate in the 2.4 GHz ISM radio band. Due to the widely spread use of this frequency range, robustness against noise, distortions or even discrete interferers is an important task and likewise a challenge for each of the mentioned wireless communication systems. Bluetooth, ZigBee and WiFi cope with this issue in different ways. While Bluetooth uses adaptive frequency hopping, ZigBee employs CSMA/CA and backs off the channel in case of interference [321]. Two main parameters significantly influence associated error rates when interference is present, which are first the distance between transmitter and receiver of the communicating system and second the proximity to the main interferer. Different studies actually reveal that Bluetooth (LE), ZigBee and WiFi interfere with each other, particularly if their used channels overlap or in case of occupying adjacent transmission channels [135], [319], [321]. Especially WiFi and Bluetooth strongly interfere with each other [319]. But also other devices may

distort the transmission of a wireless communication system significantly, e.g. a microwave oven in close proximity to the communication nodes [135]. Although Siekkinen *et al.* [321] demonstrate that a distance of 1 m to 1.5 m between interferer and receiver is sufficient to reach acceptable transmission rates, this represents an unrealistic application scenario considering the dense deployment of wireless devices in a smart home environment [97]. Considering an interferer distance of about 0.5 m, Guo, Healy, and Zhou [135] furthermore show packet error rates around several percent for all wireless communication systems under test. Recalling the reliability requirement of at least 98 %, this fact might become critical with respect to robustness but can probably be compensated by the comparatively high data rates of the wireless communication techniques with respect to the target application of lighting control. Nevertheless, interference remains a concerning problem that leads to reduced throughput, packet loss or increased transmit times [319], [321]. This circumstance will in the end provoke a higher power consumption due to extra energy needed for multiple clear channel analysis or necessary retransmissions [321]. The power consumption values stated in the subsequent paragraph might therefore become much worse as they only state a nominal case. Furthermore, latency might also be affected in a crucial manner. Further studies on coexistence of different wireless techniques and interference issues can also be found in [282], [322]. In summary, the well-established lower power wireless systems ZigBee, BLE and WiFi are obviously suitable for intelligent lighting control but are expected to perform significantly worse in terms of robustness compared to a PLC system like digitalSTROM™ and as we will see later DLT.

Power Consumption

A comparison concerning power consumption of WiFi, ZigBee and Bluetooth (LE) has been carried out in multiple studies as mentioned in the introducing paragraphs of section 2.1.3. Additionally, Blom *et al.* [32] present detailed energy characteristics of Bluetooth for low packet sizes, whereas Mulla *et al.* [273] examine different ZigBee chipsets [97]. Although featuring highest efficiency measured in power per bit, WiFi still shows much higher power consumption compared to BLE and ZigBee due to its high complexity [97]. BLE and ZigBee on the contrary consume very comparable amounts of energy for data transmission. An outstanding solution for a multi-standard digital baseband ASIC covering both Bluetooth Smart and ZigBee is e.g. presented in [12]. Tab. 2.1 therefore exemplarily depicts the power consumption of different chips for each wireless protocol under test according to references [97], [204], [273], [314], [321]. Mulla *et al.* [273] also provide data for other ZigBee chips, which

Table 2.1: Power consumption for different chip sets of low-power wireless communication techniques according to [97], [204], [273], [314], [321].

Protocol	Chipset	Supply	TX-Mode	RX-Mode	Data Rate
BT BR	Bluecore2 [349]	1.8 V	57 mA 102.6 mW	47 mA 84.6 mW	0.72 Mbit/s
BLE	BLE112 [348]	3 V	28 mA 84 mW	22 mA 66 mW	1 Mbit/s
	CC2540 [352]	3 V	21 mA 63 mW	15.8 mA 47.4 mW	1 Mbit/s
ZigBee	CC2430 [350]	3 V	24.7 mA 74.1 mW	27 mA 81 mW	0.25 Mbit/s
	CC2520 [351]	3 V	25.8 mA 77.4 mW	18.5 mA 55.5 mW	0.25 Mbit/s
WiFi	CX53111 [370] [97], [273]	3.3 V	219 mA 722.7 mW	215 mA 709.5 mW	54 Mbit/s
	CC3000 [373]	3.6 V	190 mA 684 mW	92 mA 331.2 mW	54 Mbit/s

however all suffer from a higher power consumption. The comparative values listed in Tab. 2.1 only represent nominal power consumptions for the different modes of operation. As mentioned in the previous robustness discussion, power consumption might also (signficiantly) increase due to interference and disturbances because retransmission of several data packets or channel access analysis become necessary in that case.

Generally, most of the wireless protocols aim to save power consumption by applying the concept of duty cycling or cyclic sleeping [97]. Waking up only every once in a while, the communication devices remain most of the time in a low-power standby mode or sleep state when using this concept. Varying duration and interval of the sleeping cycle consequently influences power consumption significantly [32]. Dementyev *et al.* [98] provide various measurements for different low power wireless communication techniques and show that current consumption drops exponentially with increasing sleep interval. However, a longer sleep interval results in higher latency. Dementyev *et al.* [98] suggest optimal sleep intervals of 10 s and 14.3 s for BLE and ZigBee, respectively. As

these sleeping times violate the specified latency requirement of maximum 400 ms for lighting control, much smaller sleeping intervals must be applied if duty cycling is used. The expected energy savings are hence limited.

Because PLC methods directly operate on mains voltage, the power consumption of the digitalSTROM™ approach appears comparatively high as indicated by Dickmann [101]. Due to the downstream data transmission link a minimum DC current needs to be flowing as calculated by equation 2.1,

$$I_{DC,dS,min} \geq \sqrt{2} \cdot I_{AC,dS,RMS} = \sqrt{2} \cdot 35\,\text{mA} \approx 49.5\,\text{mA}\,. \tag{2.1}$$

Considering the European grid voltage of $V_{grid,RMS} = 230\,\text{V}$ this results in a minimum transmitter consumption of $P_{TX,dS,min} \geq 11.4\,\text{W}$, when the current is constantly flowing. Dickmann [101] therefore suggest to restrict the transmission to timeslots within close proximity of the mains zero crossing. In doing so, power consumption can be reduced to about 10 % assuming $I_{DC,dS,min}$ flows only 0.5 ms before and after each zero crossing. Assigning 1 ms timeslots for data transmission before and after each zero crossing, at least diminishes transmission energy to about 20 %. These timeslots should be long enough for the targeted low data rate transmission. Applying this restriction leads to power consumptions between 114 mW and 228 mW by multiplying $I_{DC,dS,min}$ and $V_{grid,RMS}$ with the percental timing reduction. By this means, the digitalSTROM™ technology comes close to the power consumption values realized by low-power wireless communication techniques. Unfortunately, Dickmann [101] does not mentioned how much energy is needed for any receiver (RX) circuits. Due the low complexity of the digitalSTROM™ approach it is expected that similar results as those for the wireless techniques can be achieved.

Kruse [190] moreover measured the standby power consumption for different lighting systems that are available in the market. According to his study, dSDs typically consume around 400 mW to 500 mW in standby mode, whereas dSM and dSS need about 1.32 W and 1.54 W, respectively, in a digitalSTROM™ system. These power consumptions are in fact comparable to those of the wireless systems under test. Lowest power consumption in standby mode was achieved by *"TP-Link"* lamps, which use WiFi as communication technology, and ranges from about 330 mW to 360 mW. The also investigated IKEA system *"Trådfri"* employs ZigBee light link for communication and consumes about 450 mW in standby for luminaires and 1.36 W for its gateway. The other systems under test, Z-Wave, HomeMatic and Delta Dore, which all use proprietary protocols and transmit over the 868 MHz ISM band, consume much more power in standby, namely about 2.32 W for the bridging gateway and 600 mW to 900 mW for connected devices. It should however be noted that the measured

power consumptions include the entire luminaire or end device and not only the communication front-ends. Kruse [190] thus states that the used power supplies, sensors and microcontroller unit (MCU) are more crucial regarding power consumption. Still, it is shown that all these systems consume a significant amount during standby operation.

Beyond that, it needs to be considered that the wireless protocol chips additionally require some kind of alternating current to direct current (AC-DC) conversion for their power supply, which further increases the power budget, whereas DLT and digitalSTROM™ directly operate on mains voltage. Tab. 2.1 however only contains the consumption in relation to a low voltage DC supply. Aiming to access the home LAN or WLAN for a full integration into the smart home environment, ZigBee and Bluetooth devices furthermore need in addition a WiFi bridge or gateway, which typically consumes quite high power demands in the single digit watt range [190] as outlined above. digitalSTROM™ uses its dSS device for this purpose. Section 3.5 will eventually use shown rough ballpark figures of the different communication systems to assess the investigated DLT methodology and evaluate the improvements developed in this thesis.

2.2 Fundamentals of Color Management and Control for LED Based Luminaires

Although the origin of the LED development dates back to 1907 [312], [398], it took until 1962 until the first LED could emit visible red light [147], [398]. Nick Holonyak, an engineer working for General Electric Company (GE) at that time, built this device and is therefore referred to as the “father of LED” [398]. In the 1970s as well as in the early 1990s, SSL experienced a rapid growth phase because LEDs of various different light colors had been invented [82], [83], [110], [398]. The final breakthrough was however first achieved in 1994 by S. Nakamura, who developed high brightness blue LEDs based on indium gallium nitride (InGaN) [279], [398]. This innovative step enabled the generated of white light by mixing red, green and blue LEDs and was thus finally honored by the Nobel Prize in 2014 [77]. From there on, LEDs were no longer only used for low intensity status lights but advanced into various different applications, particularly interior lighting in homes, offices and hospitality environments, but also into street and traffic lighting or industrial and medical processes. Meanwhile, there are many kinds of LEDs commercially available that can be classified according to power level, application or colors [398]. LEDs offer significant advantages in a large quantity for these applications, such as a long lifetime, high robustness due to being insensitive to vibration and movement,

high efficacy and flux range, the absence of toxic compounds, smooth dimming over a large range, fast switching capability, compact optics design, high power conversion efficiency or full color control [74], [79], [265]. Recent hotspot topics with respect to LED based lighting are on the one hand organic LEDs (OLEDs) and on the other hand multi chip RGB LED modules [398].

2.2.1 LED Fundamentals: Electrical and Optical Properties

Like conventional silicon (Si)- or germanium (Ge)-diodes, LEDs are also constructed of a p-n junction and therefore inherit the same basic electrical characteristic. The resulting current-voltage relationship known as the Shockley equation is given in formula 2.2 for a diode with cross-sectional area A [312],

$$I = I_s \cdot \left(e^{\left(\frac{eV}{kT}\right)} - 1\right) \quad \text{with} \quad I_s = eA \cdot \left(\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A}\right), \quad (2.2)$$

where $N_{D,A}$, $D_{n,p}$ and $\tau_{n,p}$ represent the corresponding doping concentrations of donor and acceptor in the p-n junction, electron and hole diffusion constants as well as minority-carrier lifetimes, respectively [312]. Under typical forward-bias condition, the Shockley equation simplifies to

$$I = eA \cdot \left(\sqrt{\frac{D_p}{\tau_p}} \cdot N_A + \sqrt{\frac{D_n}{\tau_n}} \cdot N_D\right) \cdot \left(e^{\left(\frac{e\cdot(V-V_{th})}{kT}\right)}\right). \quad (2.3)$$

as $V \gg \frac{kT}{e}$ obtains. Once the voltage drop over the LED exceeds a certain threshold voltage V_{th}, which equals approximately to the diffusion voltage $V_{diff,LED}$ over the space charge region in the semiconductor, the current flow through the LED strongly increases according to an exponential behavior [312]. Fig. 2.1 exemplarily illustrates the I-V relationship for various LEDs of different color type or nominal forward voltage $V_{F,LED}$.

Under forward bias condition, electron and hole charge carriers diffuse into the regions of the opposite conductivity type where they will eventually recombine [312]. The difference between conventional diodes and LEDs can essentially be condensed to the predominate kind of recombination in each case. Conventional diodes typically consists of indirect bandgap materials like Si and Ge, in which the non-radiative recombination process prevails. This type of recombination generates phonons resulting in lattice vibration causing heat generation. LEDs on the other hand are built of direct bandgap materials, such as gallium arsenide (GaAs), gallium nitride (GaN) or other (III-V) and (II-VI)

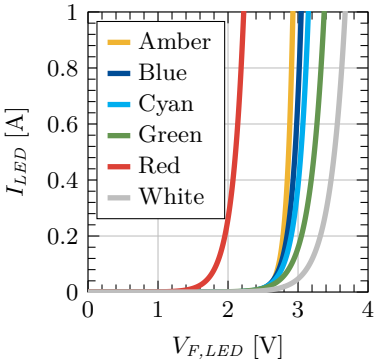


Figure 2.1: I–V relationship for different LED colors.

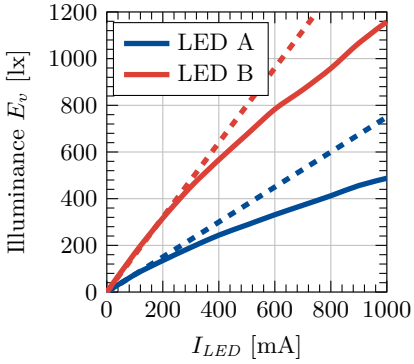


Figure 2.2: LED current vs. Illuminance according to [251].

compound semiconductors and hence experience radiative recombination with a spontaneous emission of photons. The working principle of an LED is hence derived from the phenomenon of *"injection electroluminescense"* [245] describing the above mentioned process of radiative recombination due to injected charge carriers. The amount of emitted photons thereby depends on the rate of injected charge carriers, which means that the produced light or rather the emitted luminous intensity shows a linear dependency on the LED current flow [245]. LEDs are consequently referred to as *"current controlled devices"*. Fig. 2.2 depicts this relationship between illuminance and LED forward current. As can be seen, the linear dependency is only valid for small currents because the emission intensity tends to saturate at high current flows [245], which is also widely reported in literature [3], [213], [272], [280], [281], [317]. More details on current based driving circuits for LEDs are provided in section 2.3.

The energy of a photon emitted during the radiative recombination process approximately equals to the bandgap energy $E_g = \frac{hc}{\lambda}$, which also defines the peak wavelength λ of the emitted narrow band spectrum [312], where h is the Planck constant and c is the speed of light in vacuum. Consequently, the semiconductor compound type determines in the end the emitted color of an LED's spectrum. Meanwhile there are multiple semiconductor compounds available, which results in LEDs of various colors as depicted in Fig. 2.3. The light emitted by an LED is perceived as monochromatic because its optical emission spectrum is indeed much narrower than the spectral width of a single color perceived by the human eye [312] as outlined later in section 2.2.2.

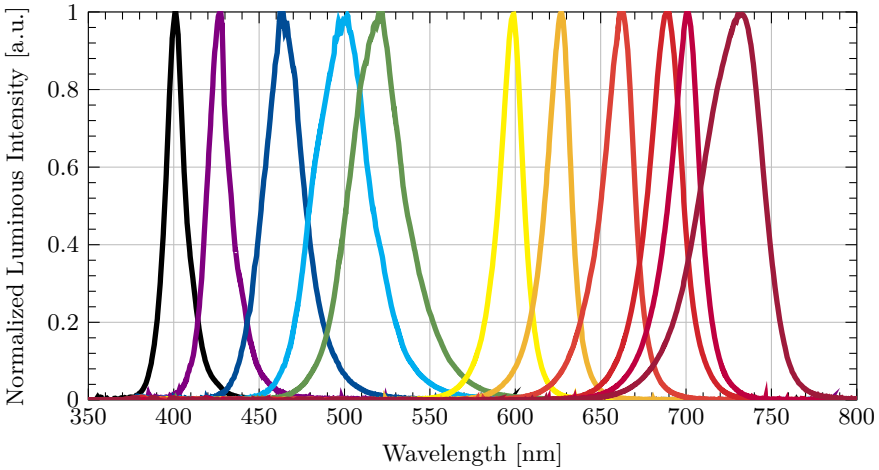


Figure 2.3: Normalized LED spectra of different peak wavelengths λ_{peak}.

The bandgap energy not only defines LED color and emitted photon energy but also approximates the diffusion voltage $V_{diff,LED}$ of the semiconductor material when being divided by the elementary charge $q_e = 1.602 \times 10^{-19}$ C. The diffusion voltage effectively represents the barrier free charge carriers must overcome to enter the neutral region of the opposite conductivity type [312]. Because a significant amount of current can only start flowing once this barrier is overcome, $V_{diff,LED}$ nearly equals the LED's threshold voltage V_{th} so that the relationship $V_{th} \approx V_{diff,LED} \approx \frac{E_g}{q_e}$ obtains [312]. The bandgap energy thereby indirectly affects LED forward voltage $V_{F,LED}$. As equation 2.3 reveals, $V_{F,LED}$ moreover depends on the (selected DC) LED current flow, junction temperature and process variations in the semiconductor material. Due the latter mentioned manufacturing tolerances LED forward voltage might vary significantly even among different LEDs of the same type [313], [376]. For the same reasoning the parasitic resistance of an LED changes and causes and an additional fluctuation in LED forward voltage [312]. The Luxeon Rebel LEDs, which are used in this work, can in fact show deviations of up to 1 V regarding their forward voltage under identical biasing conditions [342], [343], [376]. In the same manner, the optical emission spectrum of an LED is affected by visible peak wavelength shifts, which affects perceived color. These production uncertainties might thus indeed represent an issue, particularly for applications

demanding high light quality with reproducibly constant perceived optical parameters, such as luminous flux, color point stability, CCT, etc. In order to minimize such effects, LEDs are typically clustered after manufacturing by different aspects, such as peak wavelength, forward voltage, CCT or color coordinates. This clustering process is called *"binning"*.

Another effect that influences LED forward voltage and optical properties substantially, is the aforementioned temperature dependency. Since the energy of a semiconductor generally decreases with increasing temperature, LED forward voltage is impacted with a negative temperature coefficient of around $-2.3\,\mathrm{mV/K}$ [312]. Furthermore, threshold voltage and series resistance of the LED increase drastically when the device is cooled down, which leads to a different curve progression of the exponential I-V characteristic described by equation 2.3. This characteristic also makes voltage based LED driving circuits disadvantageous compared to current based approaches. Nevertheless, even current driven approaches suffer from certain visible effects due to temperature fluctuations or different current magnitudes as explained later in section 2.3.1. The temperature dependency of a semiconductor's energy gap additionally yields shifting of the peak emission wavelength and hence perceived color. Furthermore, the emission intensity of an LED decreases with increasing temperature [312]. Temperature fluctuations thus affect visible optical properties heavily, which is undesired in applications requiring high color precision and stability. Several approaches have consequently been developed to counteract on these temperature induced variations as outlined later in section 2.2.3. To understand, how these changes affect human perception, the subsequent section 2.2.2 explains relevant and important fundamentals for LED brightness and color control in more detail.

2.2.2 Human Perception, Colorimetry and Color Mixing

Light stimulation can be classified in different categories, which are actinometry, radiometry, photometry and colorimetry [114]. While actiometry and radiometry only relate to the physical nature of light in terms of particles and waves, respectively, photometry and colorimetry consider the interaction of light with the human visual system [114]. Therefore, it needs to be distinguished between radiometric parameters that can actually be measured as well-known physical quantities and photometric units, which characterize light and color sensation according to the human perception. Tab. B.3 in the appendix provides a brief overview of the most relevant photometric and radiometric quantities including a short description and how they relate to one another. The relation between radiometric and photometric units in the visible spectral range is given by

the luminosity function $V(\lambda)$, which has been introduced by the International Commission on Illumination (CIE) in 1924 [312]. Further information on radiometric, photometric and colorimetric relations can be found in common literature, such as, [17], [38], [114], [178], [249], [312], [408].

Human Visual Perception

Considering light as an electromagnetic wave, it has a certain range of electromagnetic radiation that is visible for the human eye [192]. The visible spectrum of light resides within a spectral range of 380 nm to 780 nm. Thereby, the human eye effectively uses about 51 % of the solar radiation for visual perception and has optimally adapted over the years in its evolutionary process to exploitation of daylight [17]. As the luminosity function $V(\lambda)$ converts radiometric quantities to the photometric domain as perceived by the human eye, it is also referred to as the eye sensitivity function. Fig. 2.4 shows two different versions of the $V(\lambda)$ curve for the photopic vision regime. Although

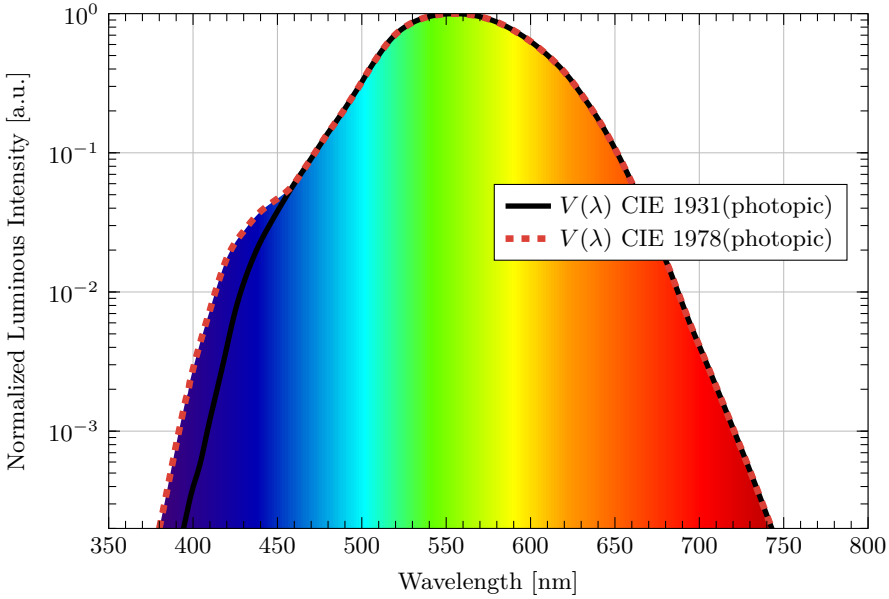


Figure 2.4: CIE eye sensitivity functions $V(\lambda)$ in the visible spectral range for the photopic vision regime.

CIE 1931 $V(\lambda)$ function is the current standard and consequently also used in this work, CIE 1978 $V(\lambda)$ function is more accurate as it accounts for the underestimated human eye sensitivity in the blue and violet spectral region [312].

According to the luminosity function depicted in Fig. 2.4, the human eye performs a wavelength selective brightness perception with a maximum sensitivity in the green spectral range at 555 nm. Generally, human brightness perception follows a strongly non-linear behavior. This non-linear relationship between emitted luminous intensity of a light source and human brightness perception has first been described by Stevens [328] with the famous *"power law"*. Stevens showed that there is an exponential behavior between the stimulus intensity of a physical property and the perceived psychological magnitude. Applying the power law to human brightness perception yields equation 2.4 [38],

$$B = k \cdot L_v^{n}\,, \tag{2.4}$$

with brightness magnitude B and emitted luminance L_v. It should be noted that k is a simple constant and n an exponent to be chosen. Since the exponent value deviates among different individuals and surrounding conditions, various selections of this parameter have been investigated and found suitable in a range from 0.23 to 0.31 [38]. More advanced models [34] also cover a range of background luminances based on the correlation established by Haubner [139]. The power law thereby nicely and precisely reflects the sensation of the human eye. In case of low luminance levels the human eye namely responses very sensitive to small changes in luminance, whereas it is rather insensitive to comparable variations at high luminance levels [290]. To correct for this non-linear perception of brightness, it is inevitable to change emitted luminance L_v of the LED light source also as a non-linear function but in highly controlled manner. One well-known technique that uses an exponential compensation mechanism is the so-called *"gamma correction"* applied in computer monitors [208]. Typical compensation exponents range from about 2.2 to 2.6 [208]. Further information on brightness perception and the non-linear correlation can be found in [38], [249]. It should be noted that perceived brightness is equal to the tristimulus value Y introduced in the subsequent paragraph about *"color spaces"*.

Besides brightness perception, also color sensation is an important aspect in LED lighting. To better understand human color vision the following paragraph provides a concise insight into the physical setup of the human eye. The human retina, which is the light sensitive part of the human eye, contains multiple visual light receptors that are so-called rod and cone cells [312]. While rods lack the possibility of color differentiation, they are able to sense the whole visible spectrum with higher sensitivity, which is beneficial for low light levels, and

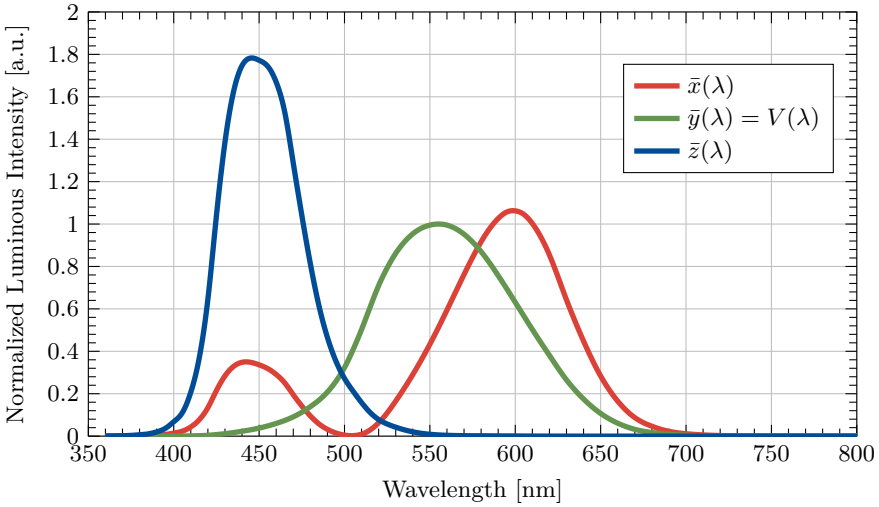


Figure 2.5: CIE 1931 color matching functions $\bar{x}(\lambda)$, $\bar{y}(\lambda)$ and $\bar{z}(\lambda)$.

are found more ubiquitously on the retina than cones [114]. Rods do therefore not contribute to color perception, which is rather accomplished by cone cells. Three different types of cone cells exist, which are sensitive in the red (L-cones), blue (S-cones) and green (M-cones) spectral range, respectively. It should be noted that the letters S, M and L stand for short, medium and long wavelength sensitive photoreceptors [192]. Rods consequently dominate the visual process under dimming conditions at low light intensities, whereas cones are the main contributors at high ambient light levels. The corresponding perception types are called the scotopic and the photopic vision regime, respectively. At medium light levels both rods and cones are actively contributing to the visual perception process, which is therefore called mesopic regime. For LED lighting and color mixing the photopic vision regime dominated by the three wavelength selective cone types thus represents the most important domain. Due to the three different cone types, human color vision possesses trichromacy, which means that the color of any light source can effectively be described by just three variables [312] namely the red, green and blue portions. The CIE has therefore developed three color-matching functions $\bar{x}(\lambda)$, $\bar{y}(\lambda)$ and $\bar{z}(\lambda)$, which reflect this fact and indicate the red, green and blue stimuli, respectively. Fig.2.5 illustrates the three color-matching functions $\bar{x}(\lambda)$, $\bar{y}(\lambda)$ and $\bar{z}(\lambda)$ versus the spectral

wavelength. It should be noted that the green color matching function $\bar{y}(\lambda)$ has been selected to equal the eye sensitivity function $V(\lambda)$. The intensities of the color-matching functions are therefore also relating to the V(λ) curve.

Color Spaces & Color Differences

Although the sensation of color is to some extent a subjective quantity and varies among different individuals, CIE uses the color-matching functions to standardize the measurement of color [312] by employing the so-called CIE 1931 (x, y)-chromaticity diagram depicted in Fig. 2.6. Therefore, the three color-matching functions define the tristimuls values X, Y and Z, which reflect the stimulation of the three primaries red, green and blue, respectively. In summation they match the color of a given spectral power density $P(\lambda)$. Equations 2.5 to 2.7 summarize the mathematical relationships. The ratios of these tristimulus values given in equation 2.8 then determine the chromaticity coordinates x and y, which denote a specific color point in the chromaticity diagram of Fig. 2.6. As monochromatic colors are in fact located on the perimeter, color saturation decreases towards the center so that white light is eventually located at the center of the diagram [312]. A constant spectral distribution over the visible optical spectrum is actually realized by the so-called *"equal-energy point"* E located at $(x, y, z) = (1/3, 1/3, 1/3)$, which moreover results in equal tristimulus values.

$$X = \int_{\lambda} \bar{x}(\lambda) \cdot P(\lambda)\, d\lambda \;=\; \int_{380\,\mathrm{nm}}^{780\,\mathrm{nm}} \bar{x}(\lambda) \cdot P(\lambda)\, d\lambda \tag{2.5}$$

$$Y = \int_{\lambda} \bar{y}(\lambda) \cdot P(\lambda)\, d\lambda \;=\; \int_{380\,\mathrm{nm}}^{780\,\mathrm{nm}} \bar{y}(\lambda) \cdot P(\lambda)\, d\lambda \tag{2.6}$$

$$Z = \int_{\lambda} \bar{z}(\lambda) \cdot P(\lambda)\, d\lambda \;=\; \int_{380\,\mathrm{nm}}^{780\,\mathrm{nm}} \bar{z}(\lambda) \cdot P(\lambda)\, d\lambda \tag{2.7}$$

$$x = \frac{X}{X+Y+Z} \quad , \qquad y = \frac{Y}{X+Y+Z} \tag{2.8}$$

$$z = \frac{Z}{X+Y+Z} = 1 - x - y \tag{2.9}$$

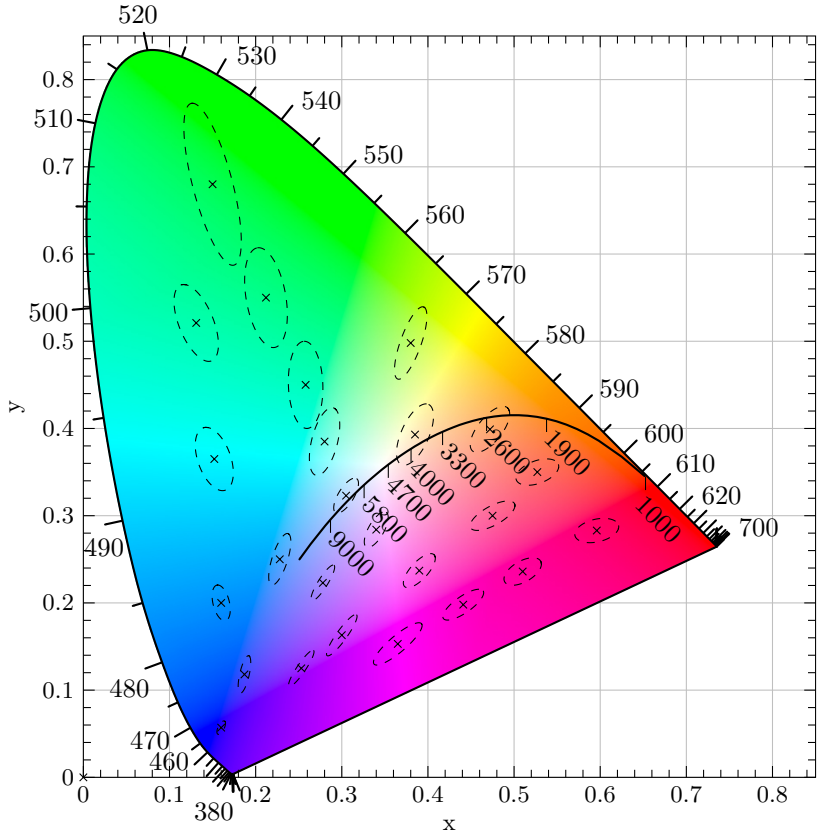


Figure 2.6: CIE 1931 (x, y)-chromaticity diagram showing different CTs on the planckian locus and several MacAdam ellipses.
The axis of the ellipses are ten times their actual lengths [256], [312].

The commonly used CIE 1931 (x, y)-chromaticity diagram however suffers from being nonuniform regarding the color distribution [114]. This means that the geometrical difference between two color points does not consistently correspond to the perceived color difference so that not proportional relationship can be found. This effect can be illustrated by drawing the so-called *"MacAdam ellipses"* as shown in Fig. 2.6. MacAdam [256] analyzed color differences in the

CIE 1931 (x, y)-chromaticity diagram and discovered that color points within a certain proximity to one another appear identical to human subjects [312]. The depicted ellipses represent these small regions of similar perceived color coordinates in the CIE 1931 (x, y)-chromaticity diagram. By means of the MacAdam ellipses it is calculated that the human eye can approximately distinguish between 50 000 distinct chromaticities [312]. If brightness variations are included in this considerations, the number of differentiable colors even increases to a value greater than 10^6 [312]. As can be seen from Fig. 2.6, the MacAdam ellipses are however very different in size, comparing e.g. ellipses in the blue and green region. Therefore, the geometric distance between two points does not scale linearly with the color difference [312]. To solve this issue different versions and various color spaces have been developed in literature, such as the CIE 1960 (u, v) and the CIE 1976 (u', v') chromaticity diagrams or the more advanced CIE $L^*a^*b^*$ and CIE $L^*u^*v^*$ color spaces. Further information on different color spaces is also provided in [114], [249], [312], [408]. A more linear color space is e.g. the uniform CIE 1976 (u', v')-chromaticity diagram, which calculates its color coordinates according to equation 2.10 and the nearly linear color distance by equation 2.11. A transformation of the respective coordinates to the CIE 1931 (x, y)-chromaticity diagram is easily possible using equation 2.12. The CIE 1976 (u', v')-chromaticity diagram is illustrated in appendix section B.1, in Fig. B.1.

$$u' = \frac{4X}{X + 15Y + 3Z} \quad , \qquad v' = \frac{9Y}{X + 15Y + 3Z} \tag{2.10}$$

$$\Delta u'v' = \sqrt{(u'_1 - u'_2)^2 + (v'_1 - v'_2)^2} \tag{2.11}$$

$$x = \frac{9u'}{6u' - 16v' + 12} \quad , \qquad y = \frac{2v'}{3u' - 8v' + 6} \tag{2.12}$$

Although the CIE 1976 (u', v')-chromaticity diagram vastly reduces the nonuniform color differences, it does not completely eliminate them [312]. Nevertheless, the distance between two color points $\Delta u'v'$ is often used as a measure for achievable color deviation and will also be applied within this thesis. A color distance below $\Delta u'v' \leq 0.002$ is not perceivable by the human eye, whereas a maximum limit of 0.0035 is still acceptable and considered to be a just noticeable difference [99], [392], [408]. A four-step MacAdam ellipse represents the perceivable threshold for light source standards [392]. Boyce [38] moreover mentions that lamps are only regarded as white light sources as long as the color distance from the planckian locus remains below a value of $\Delta u'v' \leq \pm 0.006$.

In LED lighting control, the CIE 1931 (x, y)-chromaticity diagram is however widely adopted as it is practical for hardware implementations because mainly linear computations have to be performed [239]. Furthermore, it is desired to adjust chromaticity and brightness independently from one another [239], which can also be easily realized by employing the CIE 1931 (x, y)-chromaticity diagram. Therefore, the smart LED driver developed in this thesis is designed for (x, y) inputs regarding the communication system and color control algorithm for compatibility reasons with this widely spread standard usage. Nevertheless, it should be considered that color is actually a three-dimensional quantity since it is also affected by the emitted luminance L_v. It should however be noted that the terms *"color"* and *"chromaticity"* may be used synonymously, if considering a light source to be restricted to a single brightness level [312]. If brightness changes are taken into account, a three-dimensional color space like the CIE $L^*a^*b^*$ would be more accurate to determine color difference, plus theses color spaces additionally solve the issue of non-uniformity completely. The color difference in these color spaces is named ΔE and can be computed by the Euclidean distance shown in equations 2.13 and 2.14 [145], [171]. A color difference value ΔE below 0.5 to 1 [145], [171] is not perceivable by the human eye, while a value of $\Delta E \leq 3$ might still be acceptable [239], [432]. A more detailed derivation and explanation of ΔE using the *"CIEDE2000 Color-Difference Formula"* according to equation 2.15 is provided in [316] and further information on color spaces and color difference formulas can also be found in [145], [171], [249], [408].

$$\Delta E_{ab} = \sqrt{\left(\Delta {L^*}^2 + \Delta {a^*}^2 + \Delta {b^*}^2\right)} \tag{2.13}$$

$$\Delta E_{uv} = \sqrt{\left(\Delta {L^*}^2 + \Delta {u^*}^2 + \Delta {v^*}^2\right)} \tag{2.14}$$

$$\Delta E = \sqrt{\left(\frac{\Delta L'}{k_L S_L}\right)^2 + \left(\frac{\Delta C'}{k_C S_C}\right)^2 + \left(\frac{\Delta H'}{k_H S_H}\right)^2 + R_T \cdot \frac{\Delta C'}{k_C S_C} \cdot \frac{\Delta H'}{k_H S_H}} \tag{2.15}$$

Color Rendering Index (CRI)

Besides computing the achievable color shift there is another important metric to determine quality and performance of a (white) light source, which is the capability to render the true colors of illuminated objects [114], [312]. While different approaches to quantify this property exist, the most adapted method is to compute the so-called color rendering index (CRI) based on spectral measurements [114]. Recently, complementary and to some extend

more accurate methods, such as color quality scale (CQS) [93], [94], gamut area index (GAI) [304] or TM-30-15 [92], [306] have been developed. Particularly, GAI supplements the CRI since light sources are evaluated as featuring excellent light quality, if both measures, CRI and GAI achieve values of higher than 80 [304]. This thesis still focuses mainly on CRI as the most adopted standard, while the other mentioned metrics would be interesting for evaluations in future work. The CRI method calculates the color differences ΔE_i that occur when 14 specific test colors are illuminated first by a reference illumination source and subsequently by the light source under test [312]. The CRI calculation has been discussed in detail by Wyszecki and Stiles [408] and additional information can also be found in [114], [312]. The CIE general CRI is an average calculated according to equation 2.16 using only eight of the 14 test color samples,

$$CRI = \frac{1}{8}\sum_{i=1}^{8} 100 - 4.6\Delta E_i^* \,. \tag{2.16}$$

While color differences can be computed for any set of color coordinates, CRI is only applicable to white light sources. The maximum achievable CRI is a value of 100, if there is no difference in color appearance between test source and reference source [312]. If low CRI is emitted by the light source, the illuminated object would look totally different regarding its color appearance, e.g. a wood plate might appear reddish. Hence, it should be aimed for high CRI ≥ 90 for descent color rendering. If in fact a CRI greater than 90 can be achieved, the light source is considered to successfully render the real color of objects [114].

Color Temperature (CT)

Another standard to describe white light sources is the color temperature (CT). The definition of a CT refers to the planckian black-body radiation spectrum that is characterized by only one parameter, the temperature of the body, as shown in equation 2.17 [312],

$$I(\lambda) = \frac{2 \cdot h \cdot c^2}{\lambda^5 \cdot \left(\exp\left(\frac{h \cdot c}{\lambda \cdot k \cdot T}\right) - 1\right)} \,, \tag{2.17}$$

where h is the Planck constant, c the speed of light in vacuum, λ the spectral wavelength and k the Boltzman constant. A black-body radiator thereby represents an ideal thermal radiator emitting electromagnetic radiation of intensity $I(\lambda)$ with a characteristic spectral curve progression according to equation 2.17 [249]. The CT of a white light source is thus defined as the temperature, at which the ideal black-body radiator and the light source appear

with identical color and thus share the same color coordinates in the chromaticity diagram [312]. Black-body radiators are therefore considered as perfect color renderers and thus feature a CRI value of 100 [114]. A natural, well-known thermal radiator is the sun emitting a smooth continuous spectrum over the entire visible range, which is very convenient for the human eye. Consequently, thermal radiators have traditionally been selected as artificial light sources, such as the candle light or an incandescent lamp, also featuring a CRI value of 100 [114]. A typical incandescent lamp emits light at a CT of about 2800 K, whereas wax candles lie in the range between 1500 K to 2000 K. An overview of CTs from different light sources and at specific daylight conditions is provided in [312]. LEDs and likewise CFLs however suffer from certain spikes and peaks in their spectral radiation as these light sources are not a black-body radiator. This implicates that the color of the emitted light of these sources does not exactly match to the one of a black-body radiator. Considering the CIE 1931 (x, y)-chromaticity diagram, the location of the black-body radiation is called planckian locus. The chromaticity coordinates of LED and CFL based light sources hence do not fall exactly on this planckian locus. In this case, the so-called correlated color temperature (CCT) is used instead, which is defined as the temperature of a planckian black-body radiator whose color is closest to the color of the white light source [312]. Due to the non-uniformity of the CIE 1931 (x, y)-chromaticity diagram it is not possible to take the shortest distances in this domain to determine the CCT but the CIE 1976 (u', v')-chromaticity diagram is used instead. A conversion of CT into (x, y)-coordinates is provided in equations 4.30 and 4.31 in chapter 4.4.1 according to [181]. An analog transformation of (x, y)-coordinates into CCT is given by McCamy [260] and Hernández-Andrés, Lee, and Romero [144]. A bit confusing might be the fact that low CTs and CCTs, e.g. around 2000 K to 3000 K, correlated to a *"warm"* perceived light, whereas higher temperatures, ace.g. above 5000 K, are considered as *"cold"* light. This CT paradox originates from low CTs having larger red content in the white light, which is perceived as warm, while higher CTs show a stronger bluish color tint of the white light [114].

Color Mixing with LEDs

Generally spoken, there are two fundamental methods for generating white light with LEDs. The first one is called the *"color conversion approach"*, which founds on the principle of photoluminescence using a fluorescent material. In this case an LED emitting light at a shorter wavelength excites the color-converting material by higher energy photons. This is why this concept is also called *"wavelength up-conversion"* or *"energy down-conversion"* [114]. Typically,

phosphorous materials are used for the color conversion as they possess a broad emission spectrum, while blue LEDs are being employed for the excitation process. To optimize the luminous efficacy of the optical radiation these phosphors are tuned, e.g. by controlling their ion concentration and composition, so that the overlap with the human eye sensitivity function is maximized as much as possible and luminous efficiencies of $> 100\,\mathrm{lm/W}$ can be realized [114]. Although this method is widely used in the commercial sector, which is mainly driven by cost reasons, there are certain issues associated with this method particularly regarding the visible optical performance. The ability of tuning the emission spectrum is very limited, which leads to decreased colorimetric and photometric performance [114]. Although this issue is (partially) addressed by the development of quantum dots [65], it remains a limiting constraint especially for high quality lighting applications which require a spectral tuning even during operation or when reacting on certain events and surrounding conditions. Furthermore, the number of available phosphor materials that can efficiently absorb in the blue or near ultraviolet (UV) spectral region and emit light efficiently in the visible domain is very limited because of the challenging requirements and operating conditions in LED lighting [177]. More information on the application of phosphorous based white LEDs is provided in [177], while Erdem and Demir [114] summarizes certain design considerations for high quality lighting in different applications.

The second method for generating white light with LEDs founds on the principle of *"additive color mixing"*, which uses two or more LEDs, and is hence called *"multi-chip approach"*. Conventional systems with full color control employ a combination of three LEDs, which are typically red, green and blue, in order to realize precise color synthesis. Combining various LED colors thereby allows to carefully optimize the emission spectrum regarding colorimetric and photometric quantities and features. By employing smart control strategies it is even possible to react on certain surrounding conditions, such as low daylight levels, or human physical demands like a high concentrativeness as outlined later in section 2.2.4 and tune the optical emission spectrum of the LED based light source accordingly. While this method enables precise spectral tuning, its main drawbacks are associated with a higher complexity and increased costs regarding the electrical driving circuitry and color control strategy. Beyond that, some practical aspects like different lifetimes and temperature dependencies of the individual LED chips and the so-called *"green gap problem"*, which addresses the lack of a semiconductor material enabling efficient green light emission, shall also be mentioned [177]. The research for novel materials and techniques to solve these issues is yet still ongoing [114]. Nevertheless, additive color mixing is the only way to ensure high light and color quality of an LED based light

source, while allowing for tuning the emission spectrum on demand. Therefore, this thesis aims at finding an efficient color control and mixing strategy based on this approach.

Recalling the CIE 1931 (x, y)-chromaticity diagram of Fig. 2.6 helps to better understand additive color mixing in the multi LED chip approach. The color point of an LED in the chromaticity diagram is commonly referred to as LED *"primary"* or *"primary valence"*. The bounded area that is spanned by the different primaries is called a *"color gamut"*. In case of using only two LED colors, the color gamut reduces to a single straight line interconnecting the corresponding two primaries. Thus, the chromaticity coordinates of the mixed color always lies exactly on the connection line, while the precise location on this line is determined by the mixing ratio of the two emitted LED spectra. A representative application example for a light source composed of only two LEDs is a tunable white luminaire, e.g. in a setup with a broadband white LED and an amber-colored LED. If three LEDs are being used, the connection lines of corresponding primaries even surround an entire area of displayable colors in the chromaticity diagram. In this case, every chromaticity coordinate that resides within this triangular-shaped gamut plane can be realized by mixing the emission spectra of the employed LEDs accordingly. Applying vector analysis helps to understand this fact, since the primary LEDs can be treated as vectors spanning a plain and a desired chromaticity pair (x, y) can be realized by any linear combination of these primaries. To enable full color control an LED luminaire actually hence at least three different LED primaires, which are typically red (R), green (G) and blue (B). The setup of an R-G-B LED configuration is e.g. commonly found in displays and computer monitors [75]. In this particular application the deployed LEDs are selected in a manner to maximize the gamut area since its size determines the amount of displayable colors. Other applications might require different performance criteria, e.g. interior lighting that is investigated in this thesis rather evaluates suitable LEDs according to their spectral properties or luminous efficacy. In case of using more than three LEDs, the color gamut changes its shape, if one or more of the additional LED primaries lie outside of the original triangle. Fig. 4.1 in chapter 4 illustrates this behavior for a color gamut created by six different LED primaries in the CIE 1931 (x, y)-chromaticity diagram. If however all of the additional colors lie inside the original triangular gamut, which is e.g. the case for the RGB-W configuration also depicted in Fig. 4.1, the amount of displayable colors remains the same. An RGB-W configuration makes still sense, as the fourth white primary provides an additional degree of freedom in optimizing the spectral emissions of the LED luminaire [114], which is described more detailed in section 2.2.3 and chapter 4.

2.2.3 Review of State-of-the-Art Color Control Approaches

In science and industry various approaches have been developed to control LED based luminaires regarding brightness, chromaticity coordinates and CCT in order to generate improved white light sources. A brief summary and overview of issues in control of RGB based LED light sources is described in [276], [277]. The main issues associated with LED based lighting that need to be solved are unwanted variations in luminous intensity and visible color shifts, which originate from temperature fluctuations, aging effects or changes in LED drive current as pointed out in section 2.2.1. A suitable color control approach must consequently be capable of controlling the color point or CCT precisely and change the luminous intensity independently from the corresponding chromaticity coordinates. Simple approaches trying to solve color control with independently changeable illuminace have been proposed in literature, e.g. in [179], [315].

Intensive research has therefore been accomplished on color, CCT and intensity control of RGB light sources [67], [99], [244], [300], [338], [392] as it is possible to synthesize an entire gamut of displayable colors with this setup. Deurenberg *et al.* [99] employ a complex system with various different control loops like a temperature feedforward, luminous flux measurement with a photosensor and a color sensor, to ensure color point stability, whereas Hoelen *et al.* [146] focuses on the realization of LED multi-chip spot modules that can be controlled for this purpose. Other approaches try a simple, low complexity control to compensate color shifts and brightness effects caused by temperature fluctuations [300]. Any drifts originating from the relatively slow aging process of the LEDs are ignored in this case as these variations can be solved by regularly calibrating [300]. The excellent research of Loo *et al.* [244] focuses on light source suffering from prolonged aging and maintains the white color point under accelerated aging conditions through repetitive current stress cycles. More complex approaches like the one of Wang, Tang, and Huang [392] propose a multivariable robust control technique to achieve luminous intensity and color consistency under junction temperature variations. This concept relies on a multi-variable thermal-electrical modeling and employs a look-up table as feedforward compensator for temperature and power variations. Tang, Huang, and Ying [338] further improve this concept by a novel control structure using a thermal-electrical-luminous-chromatic model to achieve outstanding results, such as a $\Delta u'v'$ range between 0.00297 and 0.00171. Beyond that, also non-linear control methods are being employed that even include coupling effects among different LED devices to predict and control color precisely [67]. Other

non-linear control approaches realize luminous intenstity and CCT control for tuneable white applications with good results using only a set of two LED primaries in a low complexity hardware implementation [66] or by means of a more complex closed-loop regulation [200]. A very interesting idea is proposed by Li *et al.* [216] suggesting to assign a dual function to the RGB LED lighting module, which are sensing the actual color and controlling the illumination. Even smartphone cameras have been tested in feedback control systems of an RGB luminaire achieving a $\Delta u'v'$ of 0.0225 with respect to selected color [339]. Of course, it is also possible to use other combinations of LEDs in a setup with three primary valences. Measuring the forward voltage drop of each LED, Buso and Spiazzi [45] compensate temperature induced effects with a feedforward controller for a system using red, green and white LEDs. Aiming at wide-range CCT and illuminance regulation with a simple open-loop control mechanism Malik, Ray, and Mazumdar [259] propose two-component color blending. This concept uses the light of a white LED mixed with the emissions of a blue or red LED to tune the CCT accordingly from 2500 K to 12 500 K. Chakrabarti *et al.* [59] on the contrary developed a tricolor control system based on white, cyan (C) and red LEDs to realize high color rendering at low CCTs, which is indeed very difficult to achieve. CRIs ranging from 80 to 98 are realized with this method, while $\Delta u'v'$ is kept below 0.003.

Although the mentioned solutions realize brilliant ideas and control strategies while achieving outstanding results, they are limited to a maximum of three LED primaries that can be controlled. This limitation however represents a significant drawback since it is reported that three color components are not sufficient to optimize photometric properties and realized high-quality lighting at the same time [114]. Thorseth [379] thus states that adding a fourth color gives an additional degree of freedom that allows for an optimization of the optical emission spectrum and hence light quality. Thereby, such tetracolor LED systems can realize a desired chromaticity (x, y)-pair with an infinite amount of possible linear combinations of the primary LED vectors [239]. Of course, the optimization of light quality does not come for free but has to be traded for higher system complexity and increased costs as mentioned earlier. In fact, color control becomes much more complicated because mathematically an underdetermined system of equations needs to be solved, which is explained in more detail in chapter 4. Still, several approaches have been accomplished realizing four color control systems with RGB-W [179], [315], [324], [337] or RGB-A [222], [428]. White (W) or amber (A) LEDs are commonly chosen as fourth primary because these LEDs provide a broadband spectra facilitating synthesis of optical spectra with a high CRI value [239]. But also other combinations are conceivable in a tetracolor approach. Dang *et al.* [89] e.g. employs four different types of

white LEDs aiming to protect paintings from damage and aging provoked by artificial illumination. The control system of Sisto and Gauvin [324] also employs a junction temperature feedback technique for realizing accurate chromatic control and color rendering optimization. For a CCT range between 5500 K and 8000 K luminaince and CCT error can be kept below 1 %, while ΔE^*_{ab} remains smaller than 1. Zhan, Wang, and Chung [428] achieves high CRIs over a large CCT range by approximating the spectral power distributions of black-bodies. The presented control strategy therefore suffers from very high complexity regarding hardware effort. Still, it is claimed that the control approach is applicable to all multi-color LED systems. Using trained neural networks [427] [427] achieves high CRIs > 90 over a wide range of CCTs for an exemplary setup with an RGB-A luminaire. While this approach does not rely on any thermo-electrical model, it still requires two different color sensors for feedback and shows in general high complexity.

While the tetracolor lamps represent the easiest setup for featuring improved optical performance, adding even more primary colors is expected to further enhance photometric as well as colorimetric properties since each additional primary provides an extra degree of freedom for tuning the emission spectrum. Generally spoken, the more LED channels a luminaire has, the larger its displayable color gamut is and the better the emitted light and color quality [427]. Chakrabarti *et al.* [58] thereby proposes a LED engine with five distinct colors to achieve a wide white gamut. This method evaluates user inputs according to a pre-calibrated look-up table and a rule-based optimization of the chromaticity distance. A calibrated color sensor is furthermore employed providing a feedback signal for correction and precise regulation, which yields color differences residing in a circle radius of 0.0013 around the desired chromaticity coordinate in the CIE 1976 (u', v') chromaticity diagram. Chew *et al.* [72] even employs up to eight LEDs, but also requires a spectral sensor in its feedback path, which makes the solution very costly and expensive. The same is valid for the solution of Llenas and Carreras [233] with 10 LED primaries, which uses a very complex spectral matching calculation on a PC. This approach is actually not easy to implement in a commercial system as it requires multiple micro spectrometers. Beyond that, Murdoch [275] shows different sets of luminaires employing five, seven and eleven colors, respectively, and explains the potential of such approaches in application but also states that simple control strategies and optimization of these more complex systems are still not available or rather under study.

In summary, various excellent color control approaches exist that can be applied for general illumination with LED based luminaires. However, these control algorithms are typically very complex to implement particularly when considering more than three LED primaries because they rely on expensive

and elaborate equipment like color sensors or even micro spectrometers in the feedback path. This complex setup is a distinct disadvantage compared to simpler approaches that only measure LED forward voltage and temperature in conjunction with applying a thermo-electrical model for color shift compensations. Most approaches also operate based on the tristimulus values, which is computationally intensive due to solving large integrals of the SPDs with the color matching functions in contrast to a one factor multiplication as shown later in this thesis in section 4.2. This thesis therefore seeks to find a color control approach that can precisely regulate CCT and chromaticity coordinates over a large gamut and independently from the user selected brightness, while employing more than three LEDs in order to provide the possibility of tuning the optical emission spectrum. The developed algorithm shall be designed to keep computational and hardware effort of the entire system to a practical minimum while maintaining excellent optical performance. Chapter 4 presents an appropriate solution in detail and explains mathematical, optical and electrical implications for the control approach and the corresponding system. Simulation and measurement data are provided as well to verify the functionality and evaluate performance according to standard metrics like CRI, ΔE, $\Delta u'v'$ and ΔCCT. The presented color control algorithm of this thesis can possibly be extended by several of the aforementioned (closed-loop) control approaches, e.g. by means of a feedforward temperature compensator or a full color sensor. In this context approaches, which compensate temperature induced color shifts but balance complexity and color accuracy, are very attractive.

2.2.4 Human Centric Lighting (HCL) and Applications with High Technical Light Quality

As outlined in section 2.2.2, the human eye has perfectly adopted in its evolutionary process to the sun as the predominant natural light source. During the daily cycle, the sun light experiences dynamic changes from sunrise to sunset regarding CT, intensity, timing and direction [219]. On top of that, the yearly season cycle modulates these parameters of the natural light. The human eye thereby links the corresponding light-dark-cycle within the daily 24 h rhythm to the human body and associated functions like alertness, cognitive performance as well as the wake/sleep cycle [11]. Light thus represents the most important timer for the internal human body clock and is besides also proven to affect human emotions, such as mood, energize and relaxation [11]. The influence of lighting – no matter if the source is a natural or an artificial one – therefore not only serves visual aspects of human sight but also causes certain non-visual effects in the human body on the so-called *"circadian rhythm"*. Compared

with the dynamic changes of natural light, artificial indoor lighting on the contrary is unfortunately mostly static throughout the day with a constant luminous intensity, direction and CCT. Beyond that, the luminous intensity of an artificial light source is effectively much lower compared to that of natural sunlight. Moeller *et al.* [268] therefore suggests to introduce lighting tuning luminance and CCT in different sequences and evaluate short-term as well as long-term effects. Because solid-state lighting (SSL) offers various optimization potential by applying novel techniques and approaches, the idea of human centric lighting (HCL) consequently aims to improve artificial light sources in order to positively affect human health, productivity and well-being. The big challenge in LED based lighting design is hence not limited to simple metrics like power efficiency or sustainability but includes moreover the different aspects of human perception and health.

Boyce [39] classifies health effects caused by (artificial) lighting into three different categories, which are first light as radiation, second light through the visible system and third light operating through the circadian system. UV, visible and IR radiation of light might cause damage of the eye and skin through thermal or photochemical mechanisms, which is rather rare for indoor lighting but may still potentially occur. The second issue caused by light through the visible system is typically associated with visual discomfort, eyestrain, headaches or even migraines. In this context, particularly flicker plays an important role for artificial indoor lighting but also other reasons like insufficient or too much illumination, glare, veiling reflections or shadows could lead to negative health effects caused by the visible system [39]. The third class of health effects relates to the circadian rhythm, which may influence several non-visual aspects like perception of feelings (e.g. mood), functioning (e.g. alertness and cognition), the wake-sleep-cycle [11] or other health effects. Especially the third class is often related to HCL and associated applications. Various reviews on health risks with artificial LED lighting [23], [382] or visual and non-visual biological effects of lighting [119], [148], [387], [400] can be found in literature. Besides changing sleep patterns, Boyce [39] as well as Motta [270] also mention an increased risk for breast cancer by excessive exposure to nighttime lighting, which is e.g. the case for night shift workers. The main reason for that is believed to originate from a suppression of melatonin, which has an anticancer effect [270].

In order to measure, quantify and evaluate human behavior as a function of the illumination source, manifold studies have been conducted. Hawes *et al.* [140] e.g. investigate the effect of workspace lighting on perception, cognition and affective state. They report an increased alertness and visual cognitive efficiency among workers when comparing LED and CFL based lighting. It is found that higher CTs lead to an increased arousel state and lower rated depression.

Also visual perception tasks like color recognition can be performed faster with increasing CTs, while reaction times for a verbal and a spatial cognition task actually go down. Testing different CRIs and CT combinations Knez [183] showed how to enhance long-term memory and to improve problem solving tasks, while investigating gender specific reactions on the stimuli. Similar studies on mood and cognition have been accomplished in office [36] and university classroom [20] environments. It is shown that not only intensity but also the SPDs influence the circadian response significantly regarding mood, performance and attention [20]. Beyond that also the impact of blue and red light as short and long wavelength spectral influencers plays a role on alertness, sleepiness and momentary mood [295]. Comparing conventional and daylight LED luminaires Cajochen *et al.* [52] discusses the effect on visual comfort, melatonin, mood, waking performance and sleep. Mills, Tomkins, and Schlangen [266] report substantial improvements regarding concentration, fatigue, daytime sleepiness, alertness and work performance by investigating the effects of high CCT office lighting. In order to reduce the discomfort glare from windows in offices and diminish the likelihood of users to turn-on the ceiling lights or to move the blinds, Amirkhani *et al.* [8] suggest to increase the light around windows, which improves human performance and well-being. Schlangen *et al.* [311] analyze acuity, cognitive performance and well-being in older (60 year old) and younger (30 year old) people as a result of workplace illumination in an office environment. Increasing illuminance from 500 lx to 1400 lx significantly improves visual acuity by about 8.8 %. Reducing the illuminance to about 300 lx is perceived as an uncomfortable dim, whereas 2700 lx are considered as slightly to bright by both age groups [311]. Zhu *et al.* [433] present effects of illuminance and CCT on daytime cognitive performance, subjective mood and alertness in healthy adults. It is shown that bright light exposure reduces sleepiness of the participants, whereas low *"warm"* lighting leads to slowest responses in inhibition, working memory and recognition of facial expression tasks [433]. Illuminance levels and CCT should hence be considered for optimizing lighting during regular daytime hours. Tam, Kalavally, and Parkkinen [336] determine the melanopsin response, which affects shifting of the circadian rhythm, alertness and hormone production, for several times of the day as well as compare those among different seasons of the year. Based on these findings an LED engine is optimized for high melanopic-lux in addition to high CRI and luminous efficacy. Comparing daytime and nighttime exposure Rüger *et al.* [308] investigate the time-of-day dependent effects of bright light. At night this could e.g. lead to an increased heart rate and a higher core body temperature, while sleepiness and fatigue are independent of the exposure time. Analyzing the effect of LED lighting on sleep, sleepiness, mood and vigor, Curcio *et al.* [85] however state

that better sleep quality and quantity is achieved in individuals when being exposed to cold light during daily hours as it reduces the duration of night-time awakenings and increases total sleep time. It is found that visual fatigue under LED lighting based on reading tasks is affected in the same manner as more blue light suppresses the visual fatigue [395].

Meanwhile several control approaches are investigated that directly relate to HCL and influence circadian rhythm. Therefore Oh, Yang, and Do [284] introduces advanced figure of merits in addition to CRI, CCT, ΔE, $\Delta u'v'$ and ΔCCT and compares different artificial lighting sources and LED based luminaires. Quantum dots [418] and OLEDs [409] have likewise been applied in the context of HCL. The reasarch in [411] develops a color control algorithm to ensure comfortable lighting by counteracting human's negative feelings.

As can be seen, there are multiple application scenarios in the context of HCL for LED based luminaires featuring high CCT and color precision, exact luminance control and an optimization opportunity for tuning the spectral emissions. Besides homes and offices HCL is thus also very beneficial for the usage in hospitals [25] or in learning environments like schools [173] and universities [20]. Especially in industrial environments, such as the oil and gas sector, lighting has been evaluated as an important parameter regarding job performance and safety [162] as it helps to prevent accidents from happening by improving visual responses like detection, reaction time and recognition. Also the performance of day- and night-shift workers can significantly be improved by biorythm balancing [84]. The different applications obviously require different illumination conditions, spectral power distributions (SPDs), degrees of color accuracy and overall light quality, which makes a tuneable color control approach with certain optimization parameters very valuable. Apart from HCL, there are however also various other applications that require a high technical light quality. Particularly museum lighting represents a challenging task due to the demand for high CRI, color uniformity and minimizing damaging effects of both visible and invisible radiation [380]. Illumination of golden artefacts e.g. requires to synthesize low CCTs around 2200 K with very high CRIs [380]. This is indeed a complex and difficult task to be solved [59] as it is much easier to realize high CRIs for CTs in the range of 3000 K to 4000 K. In order to protect valuable paintings from physical damage caused by the light source, Dang *et al.* [89] proposes a method for spectral tuning of museum illumination. Zhai, Luo, and Liu [425] investigate optimal lighting conditions of paintings under illuminance and CCT influence regarding visual perceptions. A general overview on considerations for good lighting fixtures in museums, galleries and exhibitions is provided in [126] including different lighting types like diffuse lighting and directional lighting, lighting sources from luminous

ceilings over cove luminaires and wallwashers up to spot lamps and view positioning of visitors. Additionally, the article presents considerations for different applications related to museums, such as showcase lighting, audiovisual media rooms, lecture halls, foyers, corridors and staircases as well as cafeteria, museum shop and even workplace lighting. The suggested lighting management guidelines are hence also applicable to other HCL scenarios as mentioned above. Another field requiring high technical light quality are medical applications, e.g. optical imaging systems like endoscopes [31], [334] or lighting during surgical operations [318]. In endoscopic diagnostics the quality of light is particularly important, if the color of an object or the distribution on its surface shall be investigated in detail [31]. Tuning the spectral characteristics of emitted light by means of an LED based light source can hence improve color rendering while featuring smaller form factors [334]. For surgical operations color rendering of red (raw) flesh is very important in order to correctly illuminate and distinguish skin, blood (vessels), fat tissue or internal organs from one another [318]. Also the automotive sector demands very good light quality, particularly regarding uniformity, color precision and luminance control, for the purpose of interior and ambient illumination of the cabin [29]. Modern cars are expected to deploy more than 1000 RGB LEDs in the near future [30]. One reason for this is assisted and autonomous driving, which leads to a shift from monochrome to RGB full color control LEDs and a from single to multiple LEDs per lightpipe [161]. Thereby, completely new functions, such as a display-like contour lighting (direct-lit light guides), can be realized [30]. A pixel-wise control of the light guides consequently allows for generating synchronized lighting effects in the cabin of the automotive vehicle. By this means automotive lighting aims to create a cozy, living room like environment, while providing additional visual safety features and status indications for manual and semi-automated driving [29], e.g. flashing red or yellow lights indicating pedestrian presence or any other warning. In order to realize these pixelated contour lights Isele, Neumann, and Blankenbach [161] propose a *"smart* LED driver" that is embedded in the RGB LED housing. This smart LED driving system is equipped with a built-in LED driving stage, a data communication, temperature sensor and a pre-calibration [29]. Blankenbach, Hertlein, and Hoffmann [29] use a contrast sensitivity function to determine the performance of this system in several measurements. Beyond these elaborate vehicle illumination systems, it is furthermore suggested to adapt the ambient lighting conditions of the cabin to personal needs, e.g. for older people that might require higher luminance levels to increase their accuracy in vision [116]. Caberletti *et al.* [47] has thus investigated the influence of ambient lighting in a vehicle interior on the driver's perceptions. Therefore also studies on modeling of automotive interior illumination systems are found in literature [205]. Beyond

lighting the introduction of VLC systems in an automotive environment has meanwhile been discussed [423]. Due to their high luminous efficacy and long lifetime, LEDs are also attractive for the usage in airfield lighting [43], which also requires good light quality with respect to appearance of runway and taxiway lighting systems. Photometric, colorimetric and temporal characteristics of the employed LEDs might however affect human perception like color identification, brightness and glare, visibility in fog and haze, response to onset of flashing lights and stroboscopic effects such as the phantom array [43], which is hence reviewed in detail in [43]. The mentioned applications are only listed as illustrative examples but not limited to these since various other uses cases like shop lighting, event and stage lighting, etc. exist.

In addition to featuring excellent performance regarding photometric and colorimetric quantities in conjunction with HCL related effects, all of the aforementioned application cases require that flickering is avoided in any case. As mentioned earlier, visible and non-visible flicker might induce biological human responses leading to possible health concerns [402]. Flickering may thus cause increased headache incidence, trigger severe migraines, impair performance of visual tasks or even run the risk of provoking seizures [210]. Because flickering is in fact closely related to the employed LED driving stage and technique, Wilkins, Veitch, and Lehman [402] present the biological effects of flicker for power electronic designers in associated circuitry, whereas Cao *et al.* [55] discus flicker effects of different dimming control methods. Moreover, Lehman *et al.* [211] introduce new measures and definitions of lamp flicker in lighting. The most common measure of flicker is the so-called *"percent flicker"* $F_{percent}$, which represents the peak-to-peak to contrast of light source and is therefore sometimes referred to as *"modulation"* [210]. Equation 2.18 presents the corresponding mathematical computation formula,

$$F_{percent} = 100\,\% \cdot \frac{L_{v,max} - L_{v,min}}{L_{v,max} + L_{v,min}}\,. \tag{2.18}$$

To mitigate the biological effects of light flicker Lehman and Wilkins [210] suggest certain criteria that should be considered in the design of an LED driving stage. Using bilevel (BL) or pulse-width modulation (PWM) mode to enable dimming functionality, flicker can easily occur. Although flicker frequencies between 200 Hz to 500 Hz are typically not seen by the human eye, they become visible during rapid eye movement, which could e.g. be the case in car taillights. The *"stroboscopic effect"*, which describes a rapid object movement, while the observing eye is stable, causes similar perception. Lehman and Wilkins [210] define percent flicker requirements in dependence of the flicker

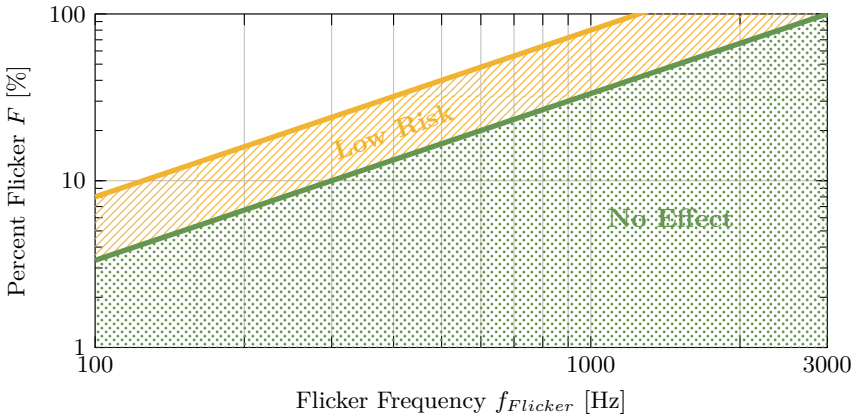


Figure 2.7: Flicker risk limits as a function of flicker frequency according to [210].

frequency $f_{Flicker}$. For PWM dimming, the flicker frequency $f_{Flicker}$ equals the modulation frequency f_{PWM}. If a frequency above 3 kHz is chosen, no effect will be visible at all, whereas a threshold of 1.25 kHz is associated with low risk of flickering minimizing visible distraction, such as phantom array effects [210]. These values are defined as the maximum thresholds at a percent flicker $F_{percent}$ of 100 % according to $F_{percent} \leq 0.08\,\% \cdot \frac{f_{Flicker}}{1\,\mathrm{Hz}}$ and $F_{percent} \leq 0.0333\,\% \cdot \frac{f_{Flicker}}{1\,\mathrm{Hz}}$ for low risk or no effect of flickering, respectively [210]. Using a lower percentaged flicker modulation value, the minimum required frequency limits decrease as well. Fig. 2.7 illustrates the corresponding curve progression for both boundary conditions. The flickering potential is consequently also associated with the employed driving circuit and dimming technique, which are both discussed in the subsequent section 2.3.

2.3 Theoretical Background on Energy-Efficient LED Driving Methodologies

Due to the nearly linear relationship between emitted luminous intensity and LED forward current flow, LEDs are generally referred to as *"current controlled"* or *"current driven"* devices as outlined in section 2.2.1. The linear dependency actually comes in handy when designing suitable drive and dimming circuits for different LED applications. Therefore, most of these driving concepts are

designed for regulating the (average) LED forward current flowing through the device [251]. Of course, it is generally conceivable to design voltage based LED drivers. These circuits however suffer from major drawbacks that are related to the exponential I-V relationship of an LED as described in equation 2.2 and depicted in Fig. 2.1. Small forward voltage deviations $\Delta V_{F,LED}$ and changes of LED threshold voltage V_{th}, which could both e.g. be induced by temperature changes, effectively result in large and excessive current variations. A voltage driven approach would hence lead to significant brightness changes and is consequently only very rarely used. When driving an LED with a constant voltage source, the temperature dependence of emitted luminous intensity can at least be reduced by applying a series resistor [312], which also helps to diminish the aforementioned voltage variations a little bit. After introducing fundamental current based driving and dimming techniques, section 2.3.1 also highlights and briefly discusses associated effects on human perception, such as visible color shifts or luminous intensity variations. Subsequently, section 2.3.2 presents a detailed overview about common architectures and recent developments in LED driver design for both, AC-DC and direct current to direct current (DC-DC) topologies, as well as for single-channel and multi-channel approaches. Particular focus is in the following section 2.3.3 then set on dynamic headroom control approaches, which regulate the supplying bus voltage adaptively.

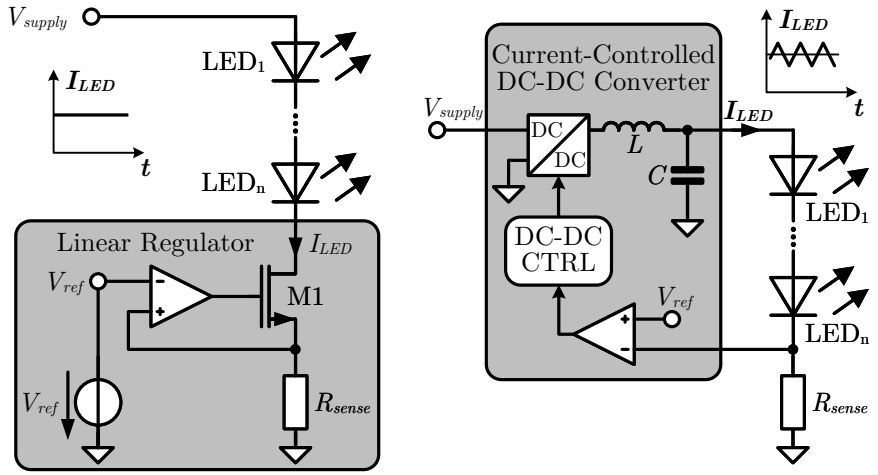
2.3.1 Fundamentals of Current-Based LED Driving and Dimming Techniques

Generally, two major driving techniques exist for regulating the LED current flow and controlling emitted luminance accordingly. These common methods are first the amplitude modulation (AM) technique, which is sometimes also referred to as continuous current reduction (CCR) method, and second the pulse-width modulation (PWM) technique. Lun *et al.* [251] as well as Loo *et al.* [245] also present a concise description of these two conventional methods in their research studies.

The simplest way to drive an LED at constant luminous output and stable color coordinates is the AM mode, which regulates the (average) DC current flow through the LEDs to a specific target value. Fig. 2.8 depicts two different ways to realize this method. While Fig. 2.8a shows the implementation with a linear current regulator, Fig. 2.8b illustrates a switched-mode power converter design. In Fig. 2.8a, an error amplifier compares the voltage dropping over a current sense resistor installed in the LED path with a fixed reference value and controls a power transistor accordingly, which then regulates LED current flow to the desired target value. Changing the reference voltage thereby allows

for enabling dimming functionality as the LED current settles to another DC value corresponding to the new reference voltage. The major drawback of this implementation method comes from a decreased efficiency due to the additional voltage drop over the current regulator. Accounting for certain fluctuations on the supply voltage V_{supply} or LED forward voltage $V_{F,LED}$, this voltage drop may indeed become comparatively large. Beyond that, a fast transient response of the regulator is required to eliminate any distortions or variations on the supply. Typically, this is however not a problem to be achieved because most operational amplifiers (opamps) used as error amplifiers in conjunction with the attached MOSFET in a simple common source configuration provide the necessary bandwidth. Aiming to operate at much higher efficiencies, switched-mode power converter designs can be employed instead as presented in Fig. 2.8b. Measuring the current flow in a similar manner by means of a sensing resistor and an error amplifier, the current-mode converter control switches its power transistor(s) accordingly to regulate the average current flow through attached LEDs. In this case, the LED current waveform is no longer a flat, constant line but follows a triangular shape rippling around the average target current. Both transient current waveforms are also conceptually sketched in Fig. 2.8a and Fig. 2.8b, respectively. Lun *et al.* [251] also explain the possibility to use a voltage controlled power converter in the same configuration as Fig. 2.8b. As this approach is however in fact a voltage based control method, it suffers from the aforementioned drawbacks explained in the introducing statements of section 2.3. In this case, the converter would consequently need to provide a very stable and accurate output voltage, while being capable to react extremely fast to load jumps or other dynamic changes [251]. Additionally, hysteretic control is claimed to be better than peak current control with respect to an enhanced current accuracy.

Because LEDs are semiconductor built devices, they inherit an extremely fast switching capability. This property enables LEDs to respond nearly instantaneously on time-varying currents and it can hence be used to operate them in pulsed mode [247] with the PWM methodology. Fig. 2.9a exemplarily shows a possible realization of the PWM mode in a linear current regulator design, whereas Fig. 2.9b depicts the corresponding control voltage and LED current waveforms. Of course, PWM dimming can generally also be applied to switched-mode power converter designs mentioned above. This requires however an extremely high dynamic response of the converter due to the fast periodic load switching [251]. Improvement strategies, such as constant on-time control [410] and proportional and proportional derivate (PPD) compensation control [150] have therefore been proposed in literature [251]. As can be seen from Fig. 2.9, the current flowing through the LEDs is switched between zero



(a) Linear LED current regulator.

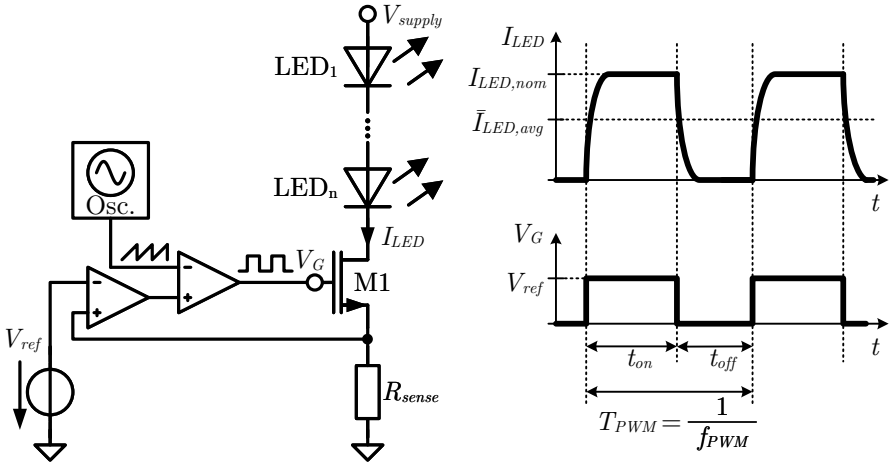
(b) Current-controlled DC-DC converter.

Figure 2.8: Implementation examples of different LED driving circuits with AM dimming functionality.

and the desired target level $I_{LED,nom}$ for a certain off- and on-time, respectively. The average current $\bar{I}_{LED,avg}$, which eventually determines the perceived luminosity, is thus given by the duty cycle $D = \frac{t_{on}}{T_{PWM}}$ of the switching pulses and the peak target current $I_{LED,nom}$ according to equation 2.19,

$$\bar{I}_{LED,avg} = D \cdot I_{LED,nom} = \frac{t_{on}}{T_{PWM}} I_{LED,nom} = \frac{t_{on}}{t_{on} + t_{off}} I_{LED,nom} \,. \quad (2.19)$$

Dimming functionality is therefore achieved by changing the effective on-time t_{on} of the LED driving circuit. If t_{on} equals to the complete duration of a PWM period T_{PWM}, the duty cycle D yields one or 100 %, which means that the LED current is continuously flowing so that $\bar{I}_{LED} = I_{LED,nom}$ obtains. This case is in fact identical to the AM mode with the same DC drive current and corresponds to the maximum achievable luminous output. Reducing the on-time and hence the duty cycle D also lowers the emitted luminous intensity and realizes dimming until $t_{on} = 0$ or a duty cycle D of 0 % is reached. In this condition, no current is any longer flowing and all LEDs are finally turned off. Due to the rapid switching behavior, flicker considerations mentioned in the end of section 2.2.4 need to be taken into account when using the PWM



(a) LED current control with a PWM-switched linear regulator.

(b) Control voltage and LED current waveforms in PWM-mode.

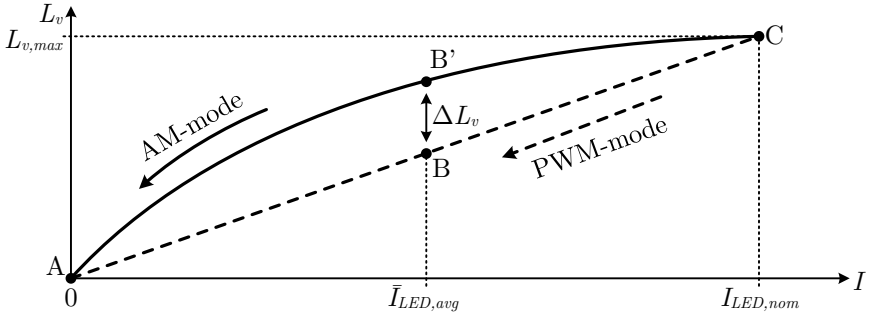
Figure 2.9: Implementation example of a PWM-switched LED driving circuit and its corresponding transient waveform signals.

mode. According to [210], the PWM should thus be selected higher than 3 kHz to avoid any visible effect or set at least above 1.25 kHz for low flickering risk at maximum duty cycle. Castro *et al.* [57] present a very thorough and extensive review on flicker-free AC-DC LED drivers that are suited for both single- and three-phase AC power grids. This comprehensive overview takes the latest trends, specific regulations and recommendations for AC-DC drivers into account providing designers with a concise summary of different categories, solutions, advantages and disadvantages. Beyond that, a converter-free LED driver featuring low flicker lighting is proposed in [48]. This approach represents a low cost and low size solution as elaborate AC-DC and DC-DC converters with bulky transformers/inductors are saved and driver as well as LEDs are integrated in a single package [48].

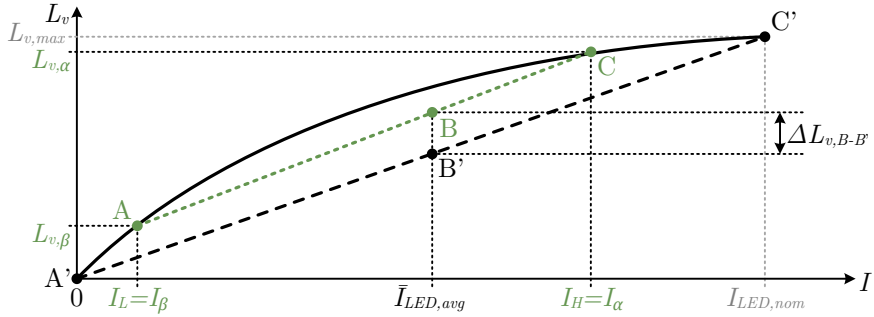
Beyond the AM and PWM driving methods, also other approaches exist, which use a combination of both techniques. Aiming to pave the way towards a generalized LED driving methodology, Loo *et al.* [245] thereby introduce the so-called *"bilevel"* driving and dimming technique. Instead of switching LED current between a maximum value and zero like in PWM mode, the bilevel (BL) method uses two (programmable) current levels, an upper one I_H and a lower

one I_L that can be chosen freely, and switches in between them. AM and PWM modes can hence be considered as special cases of this bilevel approach. For selecting AM mode, upper and lower boundarys are set to identical values equaling the chosen target DC current, e.g. with $I_H = I_L = I_{LED,nom}$, whereas PWM operates with $I_L = 0$ and $I_H = I_{LED,nom}$. By this means, Loo *et al.* [245] realize an additional degree of freedom in LED driving strategy that can be used for optimization of different target applications. In the same manner also other hybrid dimming schemes are conceivable, e.g. by defining distinct brightness sections of a dimming curve, in which AM, PWM and bilevel dimming modes are each used exclusively. Fig. 2.10 depicts generalized examples of the corresponding dimming curves for each of the four mentioned driving techniques, AM, PWM, BL and hybrid mode.

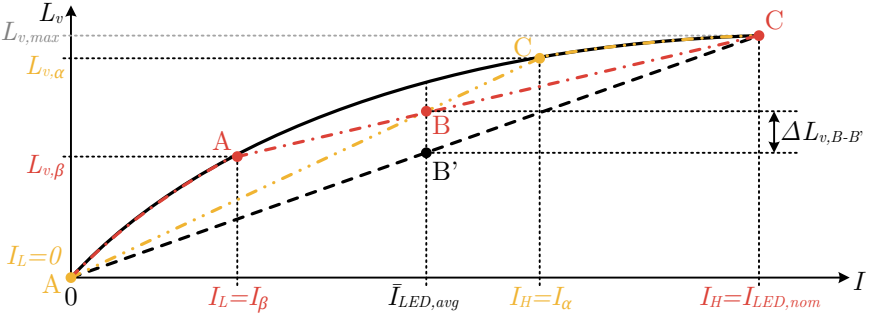
Each of the different driving methods has its specific advantages and drawbacks. Different studies have therefore evaluated AM, PWM and bilevel driving regarding photometric and colorimetric performances, namely perceivable illuminance variations [132], [245], [251], [283] and visible color shifts [19], [111], [246], [247], [250]. The luminous intensity of an LED is mainly influenced by two key factors, which are the forward current flow and the effective junction temperature of the LED [245]. As mentioned in section 2.2.1, the luminous output of an LED varies linear with the current as long as the temperature is kept constant and the current flow remains small. For higher currents the emission intensity tends to saturate and hence only follows a sublinear progression [245]. Although this non-linear saturation effect is generally weak considering constant junction temperature, it is clearly not negligible and leads to a non-linear dimming curve considering AM mode [245] as can be seen from Fig. 2.10a. In the PWM case on the contrary, there are no current variations contributing to the light output as the on-current is always kept at a fixed level (e.g. $I_H = I_{LED,nom}$). Only the linear duty-cycle function actually determines the average current flow and hence luminous intensity. Thus, a perfectly linear dimming curve progression can be achieved for fixed junction temperatures in the PWM mode. Fig. 2.10a taken from [245] exemplarily shows this behavior by plotting illuminance as a function of average forward current for AM and PWM dimming technique. Inspecting this graph, it further becomes evident that DC driven LEDs in AM mode emit higher illuminance than PWM driven ones for the same average current. This behavior is indeed intuitive because the PWM methodology drives attached LEDs at higher currents during its on-time so that the saturation effect of the luminous intensity comes to the fore. As a result of this behavior, the AM driving method operates at a higher luminous efficacy, which means that a brighter light output is generated for the same amount of electrical power. The BL method can in fact be applied to balance the advantages and disadvantages



(a) Illuminance vs. (average) LED current for AM- and PWM-mode [245].



(b) Bilevel BL dimming mode: Exemplified illuminance pathway in dependence of LED forward current with $I_H = I_\alpha < I_{LED,nom}$ and $I_L = I_\beta > 0$ [245].



(c) Exemplified illuminance pathways for hybrid (AM+BL) dimming operating.

Figure 2.10: Illuminance modulation as a function of (average) LED forward current for different driving methods, redrawn & inspired from [245].

of AM and PWM method [245]. Consequently, a linear dimming profile can be achieved at intermediate luminous intensities and efficacies as depicted in Fig. 2.10b. Due to the additional degree of freedom, any illuminance level in the area enclosed by the AM and PWM dimming progressions can be adjusted, while maintaining the linear dimming profile. In terms of efficacy Loo *et al.* [245] constitute that it is better to reduce the upper current level I_H than to increase the lower one I_L. However, the BL dimming achieves the improved illuminance compared to the PWM method at the expense of a reduced dynamic dimming range since the lower, non-zero boundary I_L determines the new minimum light output. The levels I_H and I_L therefore need to be selected carefully as a trade-off between the amount of illuminance/efficacy improvement and the dynamic range needed to ensure sufficient control headroom [251]. Fig. 2.10c illustrates the illuminance-current relationship for hybrid dimming operation, which is realized by combining the different driving methods, e.g. AM and BL mode or PWM and BL mode. Thereby, it is possible to achieve all of the aforementioned illuminance levels with sufficient dynamic range for the average current modulation. Of course, it has to be considered that the dimming profile might become non-linear in some regions, if AM dimming is applied. Furthermore, the dimming profile might become discontinuous in some cases or different current-illuminance slopes might cause a non-linear human perception of the dimming profile. For a final target application, the driving method hence needs to be selected carefully. In addition to the influence of LED forward current, also junction temperature variations have to be considered regarding emitted illuminance L_v. Recalling that luminosity decreases significantly with increasing junction temperature for a constant LED current flow [245], the driving current could be selected a little bit higher when the temperature rises in order to compensate for this effect [312]. However, when current and temperature variations become effective simultaneously, illuminance becomes a highly non-linear function of the forward current and saturates even faster [245]. This fact might lead to elaborate and complex control strategies, if the forward current is used to compensate for temperature changes and obviously requires some kind of closed-loop control employing a temperature sensor. Beyond modulating photometric quantities, forward current and junction temperature both also affect colorimetric performance, such as perceivable color shifts, as explained in the subsequent paragraph.

With respect to perceivable color variations the forward current level and the junction temperature actually show opposing effects for phosphor-converted (PC) white LEDs [247]. While an increase in current amplitude provokes a *"blue-shift"* towards shorter wavelengths, an increase in junction temperature yields a *"red-shift"* towards longer spectral wavelengths [247]. Keeping the temperature

constant AM dimming thus suffers from visible color variations, whereas PWM or BL dimming ideally experience no color shifts at all [245]. Lun *et al.* [251] proves this behavior by means of different experiments recording temperature stabilized measurements of illuminance and color shift under different dimming techniques. Minimum color shift $\Delta u'v' < 0.00075$ is indeed achieved for the PWM method. The slight color variations are attributed to peak current ripple changes, measurement accuracy and minimum temperature variations. In reality junction temperature caused effects are however present in every driving system and may hence not be neglected. Detailed mathematical deductions and derivations for color shifts of white LEDs due to junction temperature and drive currents are therefore provided in [246], [247]. Based on these mathematical relationships in conjunction with conducted measurements Loo *et al.* [246] prove the opposite shifting effects of junction temperature and LED forward current. Thereby, the authors model corresponding chromaticity paths for each of the three driving techniques (AM, PWM and BL) under test. As the respective color shifts of LED forward current and junction temperature counteract on each other, AM mode shows lowest overall color shift. PWM mode on the contrary inherits the largest color shift because the physical LED forward current is not changed over dimming and any junction temperature induced color shift can thus not be compensated at all. The bilevel method obviously lies again somewhere in between the other two techniques. It should however be noted that PC white LEDs experience wavelength shifts that depend on the temperature behavior of the phosphor coating. Similar results regarding compensation of opposing peak wavelength shift effects have also been report in [250], however only with respect to cold white LEDs. In warm white LEDs this is not the case because this LED type has a much higher phosphor concentration in its coating, which suppresses the blue spectrum more effectively. Hence, current induced blue shifts do not take effect and the temperature dependent red-shift dominates. For warm white LEDs the PWM therefore performs better with respect to color stability [250]. Beczkowski and Munk-Nielsen [19] also investigates PC white LEDs as well as InGaN LEDs under AM, PWM and hybrid driving methods. In this study, the opposite peak wavelength shift phenomenon was also used to compensate color shifts under dimming operation. Therefore, hybrid dimming is reported to be particularly useful for PC white LEDs in order to minimize color shifts due to having two independent control variables, current level and duty cycle, respectively, instead of just one compared to AM or PWM dimming methods. While best results are achieved for the hybrid approach, PWM mode yielded better results than the AM method. Dyble *et al.* [111] furthermore described strong chromaticity shifts under both AM and PWM dimming methods for RGB color mixing with a slight advantage

for PWM, whereas PC white LEDs only showed minor color shifts for both driving techniques in this study. A very attractive approach for color shift reductions in PC white based LED systems is presented by Loo *et al.* [247] including detailed mathematical derivations. Again the opposing wavelength shifting effects of forward current level and junction temperature are used in the bilevel dimming approach to realize color stabilization. The proposed method actually tweaks the difference $\Delta I_{HL} = I_H - I_L$ between high and low current level to counteract the thermally induced shifts. In order to assure a smooth transition between two dimming points, a new ΔI_{HL} is chosen in the way that the average current remains the same [247]. The result of current level, duty cycle and junction temperature are summarized in an optimization function $f(\Omega)$. While this approach appears very attractive and beneficial it also comes at the cost of high complexity for the control circuitry as well as the necessity of calibration for different ΔI_{HL} values, duty cycles D and dimming conditions [247]. Furthermore, a digital signal processor (DSP) is needed to store LED chromaticity information and to compute the upper and lower switching levels I_H and I_L based on the sensed LED voltage, current and case temperature [245]. Therefore, this approach is extremely elaborate in the way it is implemented, but its general idea remains very attractive, if a simpler hardware realization can be found.

Further studies about the effect of current waveform shapes including rippling on photometric as well as colorimetric performance for LEDs and OLEDs are presented in [5] and [22], respectively. The research of [5] obviously uses badly shaped PWM waveforms, which is unfortunate and thus represents not a meaningful result for the PWM mode, only in that sense that poor driver design and too slow switching behavior significantly decreases optical performance metrics. Although no significant photometric difference between DC current driven LEDs and those driven by a 20 % triangular shaped ripple current (like it is in a conventional buck converter design) were being measured in [5], it is however broadly reported in common literature that variations of a current ripple size can have visible effects on luminous intensity and perceived color [245], [251]. Even small fluctuations are not tolerable for high-end, high-performance applications, such as liquid crystal display (LCD) backlighting [251]. Thus, ripple-free converter topologies are more suitable for these cases, as they would reduce the chromaticity variations [62], but are also more costly. Targeting a $\Delta uv < 0.002$ (with respect to the CIE 1960 (u, v) chromaticity diagram), the current ripple should be as low as possible so that the average current can be controlled precisely [62]. This implies a perfectly flat current waveform in an ideal case. The implications of current ripple are however less severe for PWM based systems compared to AM driven approaches [251].

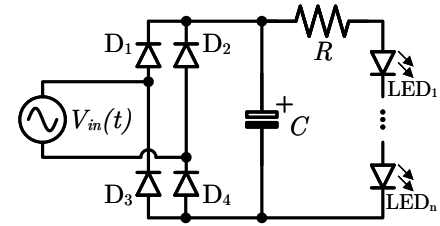
Because the purpose of this thesis is to establish a fundamental color control methodology for high quality lighting system in HCL applications, selective tuning of the optical spectrum, precise color mixing as well as a predictable linear dimming profile are very important. Therefore a multi-channel approach is considered in this thesis, which founds on the PWM driving method. The PWM mode provides greater dimming flexibility than AM [245] and has a perfectly linear dimming profile that allows for correctly matching the proportions of the individual LED primaries to enable precise color mixing. Beyond that, any color shift is solely susceptible to temperature fluctuations when the corresponding LEDs are being driven in PWM mode. In order to counteract on the visible deviations, these thermally induced color shifts can in fact be compensated by well-known feedforward techniques as introduced in section 2.2.3. Since it is rather difficult and very elaborate to determine the peak wavelength shift, e.g. by micro spectrometers, a simpler and more accurate method to monitor the temperature variations is to measure the actual LED forward voltage deviations [312]. Such an approach might indeed become helpful and may be added to a suitable LED driver design as the one designed in chapter 5 of this thesis. Of course, it needs to be considered that multi-string LED drivers should be improved with current-balancing strategies to ensure uniform luminous intensity and color produced by an LED array [73], [224], [406]. Bender *et al.* [22] deduce in summary that AM based approaches should be used for applications that require low cost realizations and high luminous efficacy, whereas PWM and BL based drivers are better suited for more sophisticated lighting systems, where accuracy and color are important. This thesis consequently focuses on the PWM driving method, which could potentially be extended to a BL dimming approach in future work.

2.3.2 Review of State-of-the-Art LED Driver Topologies

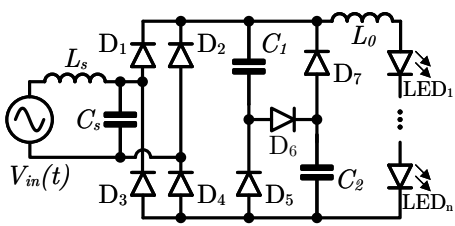
Since LEDs are meant to replace conventional light sources, such as incandescent lamps or CFLs, it is desirable to operate them in the same manner being directly connected to the AC grid. Due to the fast switching behavior and immediate current-to-light response of LEDs, a direct connection to mains voltage would however result in extensive flickering [57]. Because LEDs can only conduct a current flow into one direction due to their inherent diode behavior, their luminous output would pulsate at double the sinusoidal line frequency. Therefore, a suitable driving circuit is required, which performs an AC to DC power conversion while regulating LED current flow to a specified (DC) target current. All of the aforementioned AM, PWM and hybrid dimming techniques are then applicable to the regulated output current. In literature a broad variety

of LED driver designs ranging from simple passive solutions over single-stage power converters up to multi-stage topologies and modular concepts exist that could be applied for general lighting applications. Castro *et al.* [57] present a comprehensive and generalized overview of flicker-free AC-DC LED drivers considering not only single-phase systems but also approaches for three-phase power grids. Three-phase solutions are in fact particularly suited for driving high power (LED) loads (>300 W) in commercial and industrial installations. The excellent study of Castro *et al.* [57] classifies state-of-the-art AC-DC LED driver concepts into different categories and analyzes advantages as well as drawbacks of various approaches in depth including research results of more than 230 references. Performance metrics, like efficiency, power factor (PF) and total harmonic distortion (THD) are evaluated for each fundamental topology including specific feature sets, such as control approach, dimming functionality, universal voltage range or flicker-free condition [57]. Fig. 2.11 illustrates several examples of LED driver topologies for three different categories in single-phase AC power grids according to [57], which are passive drivers (Fig. 2.11b and Fig. 2.11a), single-stage systems (Fig. 2.11c and Fig. 2.11d) and multi-stage solutions (Fig. 2.11e). The depicted circuit diagrams have been redrawn from corresponding figures illustrated in [57].

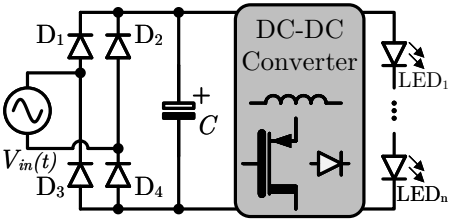
Because general lighting still contributes to a significant share of the world wide energy consumption, efficiency improvement remains to be the dominating key parameter in LED driver designs and developments up to date. Therefore, various approaches and topologies have been proposed focusing on minimizing losses and gaining maximum efficiency. An efficient and fully integrated solution for a single-stage, primary-side controlled LED driver with adaptive output current estimation is e.g. proposed in [76], whereas Hu, Huber, and Jovanović [151] develop a high-performance single-stage PFC flyback with variable boost inductance. Several single-stage designs also enable compatibility to the operation by TRIAC dimmers [201], [255], [269]. Beyond that, Castro *et al.* [57] also mentions that LED driver research focuses on reducing cost and enhancing life-time by removing limiting components as electrolytic capacitors (e-caps). Different studies therefore present single-stage [70], [253] and multi-stage [9], [141], [393] solutions for LED driving without employing an e-cap. It should be noted that single-stage designs are typically more cost effective than dual-stage designs because using lesser components and lower complexity circuits, whereas dual stages achieve higher efficiencies and reliability due to the better optimization of its tasks in its two different stages [57]. While passive and single-stage solutions are consequently more attractive for simple, low cost applications, only two- or multi-stage approaches are capable of fulfilling high performance requirements, such as dimming, high light quality, galvanic isolation, flicker-free



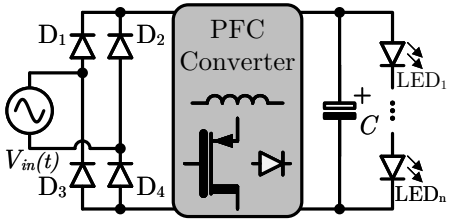
(a) Passive AC-DC conversion with capacitive input filter.



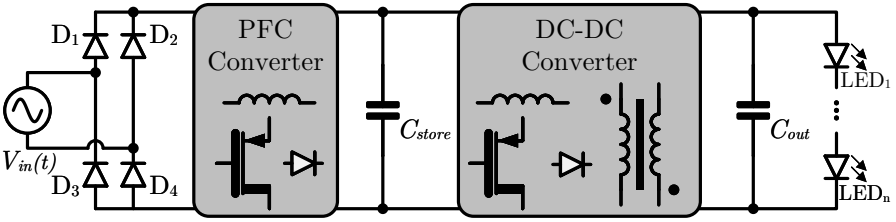
(b) Passive AC-DC conversion with valley-fill circuit.



(c) Single stage AC-DC converter based on capacitive input filter.



(d) Single stage AC-DC converter based on loss free resistor like PFC stage.



(e) Dual-stage (full cascade) AC-DC converter with active power factor correction (PFC) for high PFs.

Figure 2.11: Exemplary solutions for AC-DC-based LED driver topologies in single-phase AC power grids, all redrawn from [57].

operation and the removal of e-caps, all at once [57]. Single-stage systems on the contrary typically have to trade some of these benefits off due to physical limitations and constraints in their LED driver design.

Many studies therefore also focus on the output stage of a multi-stage AC-DC LED driver, as this one dominates the final LED driving performance. Wang, Alonso, and Ruan [398] presents a review on LED drivers and related technologies with a particular focus on DC-DC driving topologies, which are often used as

an output stage in a multi-stage driver design. It is shown that all kind of converters like buck, boost, buck-boost or flyback approaches can be employed. Advantages and disadvantages of these circuits are discussed in detail, while also highlighting other important aspects, such as current balancing circuits. Especially buck converter based approaches have proven to feature very high peak efficiencies and are hence exceedingly studied, improved and optimized. Garcia *et al.* [122] e.g. reaches 97 % efficiency, however at the dispense of a high current ripple of about 10 %. Lim *et al.* [221] even achieves 98.16 % efficiency while keeping the current error below 1.7 % by an integrated current control and realizing very wide input ranges between 110 V to 200 V. Even fully integrated designs, e.g. a floating-buck converter [289], achieve outstanding results with peak efficiencies of 93 %. Meanwhile also boost [71] as well as buck-boost [258] converters have recently proven to yield excellent results. However, the latter two examples suffer from an extremely low input voltage range up to 5.5 V only and are hence limited in their applicability. Another interesting idea is to use switched-capacitor (SC) converters, which also deliver high efficiency in high power LED driving [56], [415]. In automotive applications also CUK converters are reported to yield very good performance [81].

The aforementioned AC-DC and DC-DC LED driver topologies are all designed for one single LED color channel and therefore preferentially deployed for (cost-effective) driving of PC white LEDs. Due to the rapid evolution of multi-color and HCL applications, more and more LED driving concepts are recently developed that feature control of multiple high brightness LED channels for providing additive color mixing. A simple two-channel approach, which realizes cost-effective driving in tunable white applications, is e.g. proposed in [407], whereas a similar but a little bit more complex two-channel LED driver with automatic current balancing and zero-voltage switching (ZVS) is published in [156]. In fact, the topic of current balancing is very popular and important in multi-channel approaches because the current accuracy or rather the deviation between adjacent channels determines the quality of color mixing as outlined earlier in section 2.3.1. The technique of current balancing is well-known from high performance applications like LCD backlighting. Some innovative approaches on current balancing can be found in [75], [227], [416], [429], while Wang, Alonso, and Ruan [398] describes the fundamental techniques in their review.

Even though very elaborate multi-channel solutions like the one of Luo *et al.* [252] exist, the circuit complexity increases significantly for these approaches. Also, when a single-stage converter is added for each LED color channel, the hardware effort becomes huge. In this context, innovative approaches based on the SIMO technique have evolved as an advancement of step-down converter

architectures and outstanding solutions are explored for both AC [215] and DC [267] input voltage supplies. Very attractive SIMO LED drivers have also been proposed by Dietrich *et al.* [102], by Hanhart *et al.* [138] as well as by Yang *et al.* [413] because these designs moreover optimize hardware demand, are fully monolithically integrated and achieve very high efficiencies of 96 %. A fundamental study on N-channel SIMO LED drivers is furthermore provided in [426]. Compared to conventional SIMO topologies, the proposed design only requires N instead of $N + 1$ switches and allows all channels to be driving concurrently. Further interesting SIMO designs and respective background information can be found in [64], [103]–[105], [335]. For integrated LED driver solutions, there are also very interesting concepts that further enhance and optimize energy efficiency, e.g. digitally controllable and tunable gate driver circuits of the employed power switches [329] or accurate reference voltage circuits for high-side switching [424].

LED driver design and developments mainly focuses on efficiency improvements even though featuring multi-channel solutions for color mixing. Even in recently published research reports, optical parameters of employed LEDs, such as color stability or brightness fluctuations, are often neglected. The aforementioned approaches still represent excellent solutions with great efficiency achievements, cost reductions and even bill of materials (BOM) and hardware minimization. However, they also suffer from a degradation of optical performance with respect to photometric but more importantly colorimetric quantities. All switched mode controlled LED driving approaches inherit a comparatively large current ripple. As outlined in the previous section 2.3.1, large ripples in the transient LED current waveform may cause difficulties in color stability, lead to perceivable color shifts or provoke (slight) illuminance fluctuations. Additionally, most SIMO approaches are susceptible to flickering due to their sequential color mixing schemes in conjunction with duty cycle limitations. Talking about high quality lighting these properties are however crucial for a precise optical performance since even small differences in emitted luminance, CCT or color coordinate as well as low frequency flickering can easily be detected by the human eye. In terms of optical performance, it would therefore be more beneficial to provide linear current regulators that keep the LED current flow nearly perfectly flat. These driving circuits are however very inefficient due to dissipating a lot of (heat) power because of the additional voltage headroom required. LED driving topologies that aim to balance hardware needs, high efficiency, current precision and good optical performance are so-called *"dynamic headroom control"* approaches as explained in the subsequent section 2.3.3.

2.3.3 Energy-Efficient LED Driver Topologies Using Dynamic Headroom Regulation

Dynamic headroom regulation in an LED driving circuit typically means minimizing the voltage drop over a linear current regulator, which in consequence minimizes its corresponding losses. This is achieved by putting a switching voltage pre-regulator on top of a linear current controller [153]. While the linear current regulator settles LED current flow, the switching pre-regulator adjusts its output voltage to the desired minimum value according to a determined feedback control signal. Most implementations use either the gate-to-source voltage (V_{GS}) [152], [153] or the drain potential (V_D) [73], [74], [109], [149], [168], [230], [231], [365], [396] of the power MOSFET in the linear current regulator as its feedback control signal for the actual voltage regulation loop. The applied circuit topology of the switching pre-regulator may be freely chosen as it strongly depends on application scenario and specification parameters, such as employed LEDs per string or the desired input and output voltage range, etc. The converter topology may though consist of either an isolated or a non-isolated circuit architecture [153], be mains-fed like in [74], [231], [396] or just supplied with a constant DC input voltage as the concepts shown in [109], [153], [168], [230]. Fig. 2.12 illustrates this conceptual idea of adaptive voltage regulation in LED driving using a DC-DC converter as switching pre-regulator. Considering the discussion about different LED driving concepts in section 2.3.2, the sketched DC-DC converter could also be seen as the second stage of an AC-DC LED driver system.

The dynamic headroom regulation concept as depicted in Fig. 2.12 features three independent control loops competing against each other, which are the LED current flow settling in the linear current regulator, the inner DC-DC converter control loop and the outer voltage minimization process over the current regulator. If the system is not thoroughly designed, these control loops might interfere with each other leading to an instability in any of the control loops, which might cause a destruction of the hardware setup. Therefore, it is important to design all loops robustly at different regulation speeds. The current regulation loop obviously has to be the fastest loop in order to avoid any fluctuations and keep the current waveform nearly perfectly flat after the driver is turned on. The inner DC-DC converter control loop is also desired to be fast but may operate slower than current regulation loop. Typically switching frequencies in the switching pre-regulator of several hundred kHz up to some MHz can be achieved. The slowest control process is the voltage adaption, which minimizes the power loss over the linear current regulator. Nevertheless, it is still desired to realize comparatively fast settling times particularly when

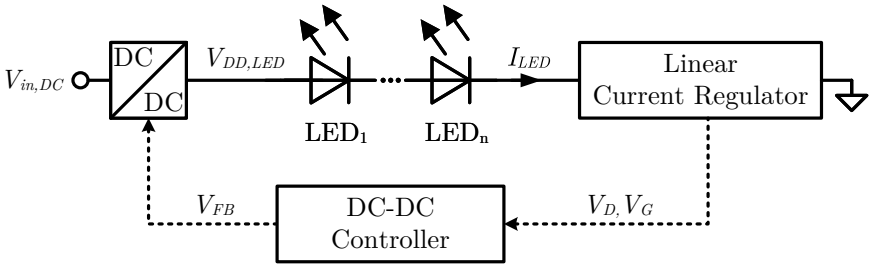


Figure 2.12: Conceptual block diagram of dynamic headroom control with a DC-DC converter and a linear current regulator.

using sequential color mixing schemes in order to operate the LED driving stages always at optimum efficiency. In order to achieve a good decoupling of the three independent regulation loops, corresponding control speeds shall be set with a difference in magnitude by at least a factor of ten.

Optimizing the dynamic headroom approach for maximum efficiency, demands keeping the power MOSFET of the linear current regulator in its ohmic region, in which $V_{DS} \leq V_{GS} - V_{th}$ obtains. To realize this behavior Hu and Jovanovic [153] suggest using V_{GS} as feedback control signal and a pulse-width modulator as the control element setting duty cycle D of the switching pre-regulator [153]. This excellent paper describes the interdependencies of high efficiency and (very) low modulator gain as well as their resulting impact on a hardware implementation and control performance. Hu and Jovanovic [153] define a specific range for the allowable modulator gain, which has to be maintained during all operating conditions to keep the MOSFET in the linear region. This may become difficult to achieve depending on the number of attached LEDs per string corresponding to the maximum bus voltage. It is shown that a high modulator gain is preferable to achieve a loop gain much greater than one and hence ensure good loop regulation performance. However, in the given configuration, the modulator gain has to become very low (≤ 0.2) to keep the MOSFET in the linear region and realize high efficiencies. Implementing a very low gain modulator with discrete components may though not be practical, while internal modulators can not be used at all [153], [236], [237]. Applying a level-shifter in front of the modulator as proposed by Hu and Jovanovic [153] reduces described limitations and widens the aforementioned allowable modulator gain range, but modulator gain still remains a challenging constraint putting high demands on the hardware implementation.

Similar as in [153], Chiu *et al.* [74] employ a single-ended primary inductance converter (SEPIC) for power supply and voltage control and several parallel current regulators with PWM dimming functionality, each for another LED string and hence color channel. This time, the developed LED driver is however capable of operating from AC mains directly and covers a large input voltage range from 90 V to 270 V. Furthermore, the minimum of the drain potentials in the parallel LED strings is used as control variable for the feedback loop. Chiu *et al.* [74] apply an analog feedback control consisting of two operational amplifiers (OPs) and several resistors for realizing the dynamic bus voltage regulation. However, external OPs within the feedback path of commercially available SMPS controllers can lead to instabilities in the control loop [305]. Especially, if a wide output voltage range should be covered, which is a key requirement according to [153], such instabilities may easily occur and become very critical. Another mains-fed approach using the drain potential as feedback control variable proposed by Liu and Peng [231] changes the feedback (FB) pin of a flyback SMPS controller integrated circuit (IC) to regulate the bus voltage dynamically. Changing of the FB pin causes the employed IC to tune the duty cycle of the switching pre-regulator accordingly. Besides developing an effective bus voltage regulation controller this concept also employs a novel energy recycling control scheme to improve efficiency [231]. A very similar approach to [74] using a PFC flyback converter as the switching pre-regulator is presented in [396]. V_{Drain} sensing is realized by means of several analog-to-digital converters (ADCs) in an MCU, which varies the potential of the converter's FB pin by a buffer stage according to an internal dynamic voltage regulation process. Another conventional alternative to realize adaptive voltage regulation is adjusting the reference of the SMPS controller's error amplifier. For realizing a large output voltage range this method is yet disadvantageous as the system would become very sensitive to offset voltages or noise distortions at small output voltages [237]. Even a few millivolts difference in the reference adjusting causes large variations of the output voltage. In fact, this would lead to reduced robustness and increased susceptibility to failure. Jung, Hong, and Kwon [168] introduce a fast transient controller in conjunction with an adaptive frequency controller to the dynamic headroom regulation LED driver aiming to shorten recovery time and reduce voltage fluctuations while maintaining a good peak efficiency of around 89.2 % [168].

Switching all LED channels at once would actually result in the input-output power to periodically face abrupt changes, which in turn brings certain performance degradation regarding electromagnetic interference (EMI) and operating efficiency as well as problems like large pulsating input/output currents or an increased voltage bus ripple [153]. Doshi and Zane [109] initially tackled this issue

and applied a digital phased-shifted PWM to achieve sequential shifting among a scalable number of parallel connected LED strings in a dynamic bus voltage regulation system. Thereby, load current variations are minimized resulting in reduced output capacitance, improved converter efficiency and diminished system EMI [109]. Combining and coordinating the control of power converter and current regulators consequently leads to a deterministic load behavior [109]. An advanced version of this approach is presented in [230]. The usage of phase-shifted PWM control is particularly beneficial at low dimming values because the linear current regulators would have less or even no overlapping on-times and each string could then be driven with a more optimized supply voltage [153]. For an LED driver with N LED strings, there are always overlapped turn-on times between different (color) channels, if the PWM duty cycle is greater than $1/N$ [153]. Although sequential PWM control provides advantages like a better load sharing for the supplying power converter, it might actually yield flickering effects regarding color mixing if not properly designed. This has to be avoided in any case considering high quality lighting applications, such as HCL.

In summary, dynamic headroom approaches have proven to provide a good trade-off between high efficiency, flat transient LED current waveform, accurate current precision and current balancing, dimming functionality, color mixing with N LED channels, wide output voltage range and circuit complexity. However, circuit complexity is indeed increased compared to simple switched-mode power supplies. Also, ensuring stable control behavior remains a challenging task, which might become impractical when it comes to conventional reference adjusting or analog feedback loops for SMPSs with active elements, such as external OPs. Nevertheless, realization of a wide output voltage range in combination with an adaptive voltage regulation is a desirable and valuable feature as it gives maximum design flexibility for various applications. Additionally, the system could safely continue to operate with similar efficiency in case of a short circuit failure of some LEDs in a string. Therefore, this approach is also selected for the LED driving concepts proposed in this thesis.

2.4 Summary of System Requirements and Concept for a Smart LED Driver

The previous sections have clearly identified specific performance criteria for each main functional unit of a *"smart LED driver"* and provided a comprehensive overview of existing state-of-the-art solutions in each field under investigation. This section summarizes these requirements in a concise manner and balances the individual demands, if needed. Additionally, distinct interfaces are defined

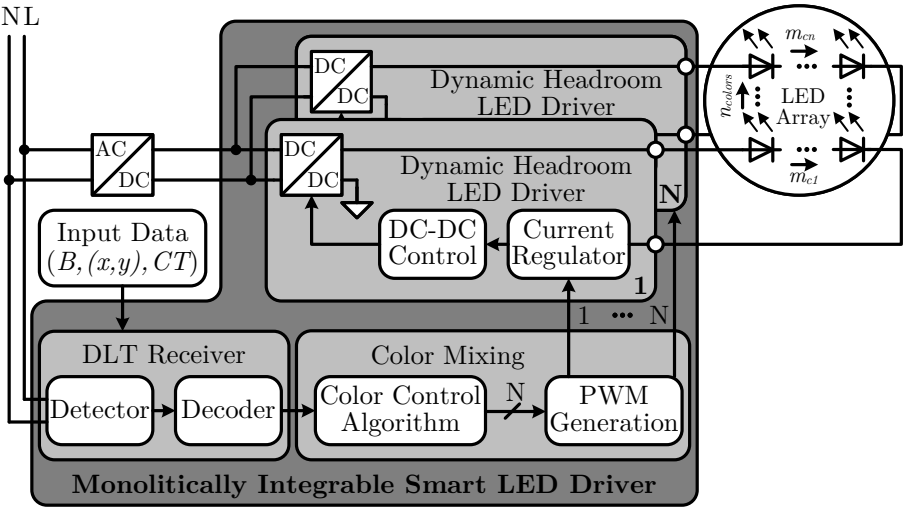


Figure 2.13: Target concept of a monolithically integrable *"smart LED driver"*.

between the three main building blocks, communication unit, color mixing algorithm and LED driving stage. Thereby, the ultimate goal of this thesis is pursued to achieve high energy efficiency, excellent light quality and tailored system intelligence at the same time. Fig. 2.13 finally embraces the findings of the conducted literature review and presents the targeted concept of a *"smart LED driver"*, which is completely monolithically integrable. As can be seen, the DLT approach is selected as communication interface, a multi-channel LED color control algorithm is incorporated and dynamic headroom controlled LED driving stages balance achievable efficiency and current accuracy.

The interface between communication system and color control algorithm is rather uncritical. User input data like brightness, color and CT selection have to be transferred with sufficient resolution. Since this thesis investigates the novel DLT approach, these resolutions are well defined by the corresponding standard [106] to 8 bit brightness levels, 24 bit (x, y) color coordinates (12 bit for each) and 8 bit CT selection. More details can be found in section 3.1 or the official DLT standard [106]. In order to assess whether DLT is competitive with low power wireless solutions, this thesis targets to develop monolithically integrable RX circuits that provide a reliability of more than 98 % as demanded by and for smart home automation systems [196], [199]. As stated in Tab. 1.1, this thesis sets the tolerance for erroneous transmission even more stringent

to a maximum acceptable error rate of only 1 %. Referring to the wireless benchmark systems listed in Tab. 2.1 and according to the literature review covered in section 2.1.3 the developed RX circuit need to consume less than 50 mW in standby and normal operation mode in order to achieve comparable performance to these communication systems in terms of power consumption. Additionally, it is aimed at further enhancements on system level to realize good integrability in other smart home systems and improve ease of use by providing a tailored system intelligence as described in chapter 1, e.g. by means of developing efficient power supplies for DLT control devices that enable accessibility of wireless communication systems. Moreover, DLT shall e.g. be extended towards a bidirectional communication methodology, which fulfills the same performance criteria as derived above, which are an error rate below 1 % and a power consumption of less than 50 mW.

The color control algorithm must be capable to handle the specified input data sizes of brightness, color and CT. The literature review on human brightness and color perception conducted in section 2.2.2 revealed that color distances below $\Delta E \leq 3$ [432] and $\Delta u'v' \leq 0.035$ [99], [408] are acceptable limits for the human eye, while a CRI > 90 [114] shall be maintained. The color control algorithm developed within this thesis therefore targets to achieve these high color quality requirements. In addition to that, the review on state-of-the-art color control techniques outlined in section 2.2.3 points out that using more than three LEDs yields better color quality regarding the metrics listed above and additionally allows for more flexibility [379], [427]. The color control algorithm proposed in this theses therefore aims to operate at least four individual LED channels ($N_{LEDs} \geq 4$) while keeping the computational effort to a reasonable limit. Eventually, it shall be able to control even up to six LED channels in total and thereby surpass other excellent tetra- and pentacolor approaches like [324], [428] and [58], respectively. As Zhao and Wang [432] state that a computational resolution of $M_{comp} \geq 14$ bit is needed to achieve good color metrics, this thesis aims for a color control algorithm that provides 16 bit computational resolution to account for a certain safety margin. Additionally, chromaticity and brightness must be independently adjustable [179], [239], [315]. Regarding an interface to the LED driving stage, the PWM mode dimming control defines smooth handover of the computed control sequences for each LED driving channel. At its end section 2.2.4 discusses the effect of flicker, describes common measures like the so-called *"percent flicker"* $F_{percent}$ that can be calculated according to equation 2.18 and finally highlights certain mitigation strategies for LED driver design as proposed by Lehman and Wilkins [210]. Based on these results of this literature review and the evaluation of different LED driving techniques in section 2.3.1, this thesis uses a PWM based driving approach, defines a

contrast ratio of at least 1:100 ($DIM < 1\,\%$) and a minimum PWM frequency of $f_{PWM} \geq 1\,\text{kHz}$ to balance hardware needs as well as optical performance, such as minimum adjustable brightness level, flicker avoidance, etc.. Thereby, the LED driver design can e.g. be kept in a low risk zone for flicker [210]. Achieving a higher contrast ratio would of course boost the achievable optical performance.

The computed PWM duty cycles D_i are finally received by the LED driving stage. The conducted comparison of state-of-the-art LED drivers in section 2.3 in fact reveals that very high efficiencies far over 90 % are only achieved by direct switching converters. Lim *et al.* [221] e.g. realize an excellent switching LED driver with 98.16 % efficiency while keeping the DC current error below 1.7 %. Other outstanding solutions of fully integrated designs as those proposed by Dietrich *et al.* [102], by Hanhart *et al.* [138] as well as by Yang *et al.* [413] moreover optimize the hardware demand an and provide peak efficiencies of up to 96 %. However, such high peak efficiencies come at the cost of an increased current ripple that can easily be in the order of 100 mA [221], [289]. The current ripple size can certainly cause visible effects on luminous intensity and perceived color [245], [251], which counteracts the above stated aims on minimum color shift and makes color point stability over all operating conditions and under different dimming profiles hardly possible. Balancing electrical efficiency and current accuracy, the concept of dynamic headroom regulation has been chosen for the PWM based LED driving stage of this thesis based on the literature review and evaluation of this approach in section 2.3.3. While an LED driver with dynamic headroom control enables precise current control and hence color stability, it trades these performance metrics off for a lower efficiency. State-of-the-art designs realize efficiencies slightly below 90 % [74], [152], [168]. This thesis therefore targets to realize efficiencies higher than $\eta_{LED,DRV} \geq 90\,\%$ while maintaining a maximum current deviation of $\Delta I_{LED} \leq 3\,\%$ in compliance with the above listed benchmark designs. For comparability reasons with these benchmark designs LED current flow as well as input and output voltages are defined in very similar ranges. The proposed LED driving stage shall provide LED current flows of up to 1 A, while the nominal current level is set to 700 mA. As many luminaires and LED drivers operate on 12 V or 24 V, the LED driver should cover these specifications in its input voltage range. Additionally, it is targeted to realize a wide output voltage range to drive at least one to five LEDs in series with one channel. The maximum output voltage shall hence be higher than approximately 15 V.

The here mentioned specifications finally extend the goal Tab. 1.1 from the introduction with some more specifics. This thesis therefore aims for achieving all stated specifications within this work.

Chapter 3

Intelligent Lighting Control with Digital Load-Side Transmission

Digital Load-Side Transmission (DLT) has specifically been developed for general lighting applications in residential homes and small offices focusing on compatibility to conventional wiring. Therefore, it copes with typical wiring issues in existing infrastructures, such as lacking a neutral wire connection at the light switch port. DLT has thus been designed as a simple, two-wire bound PLC technology operating on mains voltage at low data rate. In fact, using a PLC technology relying on mains voltage is quite favorable with respect to hardware effort because luminaires have to be connected to the AC grid voltage anyways for their power supply. Thus, no additional wiring would be required for any control lines compared to other wired lighting control systems or smart home automation approaches like DALI [191] or KNX [264].

Of course, the official DLT standard published by the IEC specifies ratings for different utility grids used worldwide [106]. This thesis on the contrary focuses particularly on the European utility grid and refers to its respective

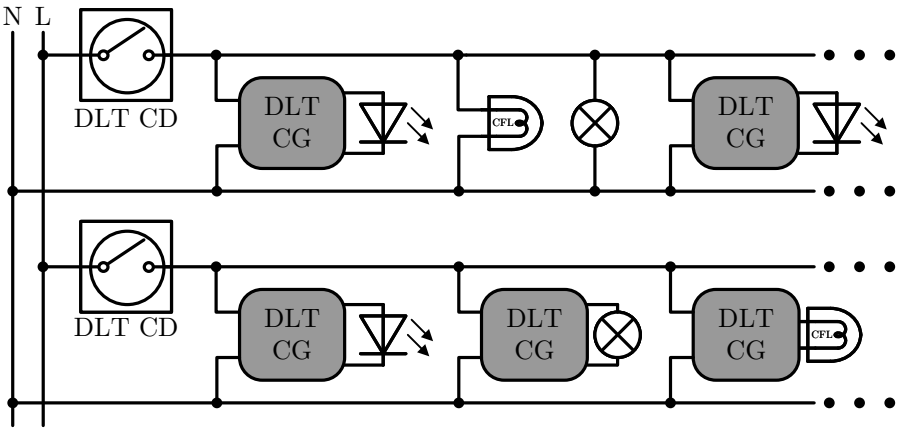


Figure 3.1: Conceptual block diagram and typical wiring of a DLT system.

ratings, such as an root mean square (RMS) voltage of $V_{grid,RMS} = 230\,\mathrm{V}$ and a nominal grid frequency of $f_{grid} = 50\,\mathrm{Hz}$. Nevertheless, the concepts, ideas and implementations proposed within the scope of this work can easily be adopted with minimum effort for any other supply grid.

Considering DLT as a retrofit technology it specifies so-called *"control devices (*CDs*)"* replacing conventional light switches or dimmers and defines *"control gears (*CGs*)"* as lamp or luminaire substitutes. To maintain the desired compatibility with existing wiring infrastructures, a single CD is thus connected in series with one or more parallel connected CGs. Fig. 3.1 highlights the typical setup and wiring of a DLT system. The number of CGs that can be operated at once by a single CD is only limited by the CD's capabilities [106], which denote a maximum permissible total power consumption of attached loads or a maximum wiring range.

DLT operates in a master-slave structure, where the CD always works in master mode while CGs on the contrary are only used as slaves [106], [188]. This operating structure thereby suggests the unidirectional communication scheme of DLT. A CD only transmits data to one or multiple attached CGs, which on the other side only receive this digitally transmitted information. Although the unidirectional communication capability represents a drawback in terms of system intelligence, it also comes along with certain advantages, which are highly reduced distortions on the grid voltage and simple hardware realization. Since a CD only influences the supply line on its load side – between CD and

CGs – it does not affect the incoming phase line when transmitting data. Thus, a bulky and expensive band elimination filter protecting the phase line from possible PLC originated distortions is not required in a DLT system. Moreover, it is possible to operate multiple DLT control devices – each with its own CGs – on a single phase without interference. Fig. 3.1 also illustrates this application scenario of multiple DLT systems operating on the same single phase line, which could e.g. represent independently controlled areas in a room.

As DLT has been specifically designed for controlling future lighting systems, it provides brightness, color and color temperature control. In this regard, the compatibility of DLT mentioned above is not only limited to existing wiring infrastructure but also extends to operating conventional light sources, such as incandescent lamps or CFLs. The DLT technology offers to connect these traditional lighting fixtures with intelligent DLT equipped luminaires in parallel while being operated together by a single CD. However, conventional light sources are not capable of using the full potential of the DLT technology as their physical structure cannot provide any color or color temperature control. Nevertheless, CFLs, if provided with a suited DLT receiving unit, can at least be dimmed, whereas incandescent lamps are only to be switched on or off.

3.1 DLT Fundamentals and Specification

DLT boundary conditions and specifications relate to half-waves of mains voltage [106]. The DLT standard [106] subdivides each half-wave of mains into three distinct periods, which are the *"supply period"*, the *"operating period"* and the *"data period"*. A transition from one period to another occurs when the grid voltage crosses over a predefined threshold level V_{SW}. In case of the European grid, this level is defined as $V_{SW} = 120\,\mathrm{V}(-0\,\mathrm{V}/+10\,\mathrm{V})$. Fig. 3.2 exemplarily depicts the described classification into different periods with respect to mains voltage. Additionally, the presented graph illustrates how mains voltage splits up into the voltage drops over the operating DLT control device V_{CD} and over attached control gears V_{CG}.

As can be seen, the traverses from one period to another happen at about 1.2 ms and 8.8 ms after zero crossing of mains voltage for the given European grid ratings. While supply and data period are situated at the edges of a mains half-wave, the operating period sits quite in its middle. Since this middle portion contains the highest possible voltage, it also provides maximum drawable power. Therefore, the operating period is used to *"operate"* all connected luminaires by supplying them with the desired amount of power. Consequently, the CD is in a low ohmic state during this time interval so that the entire grid voltage

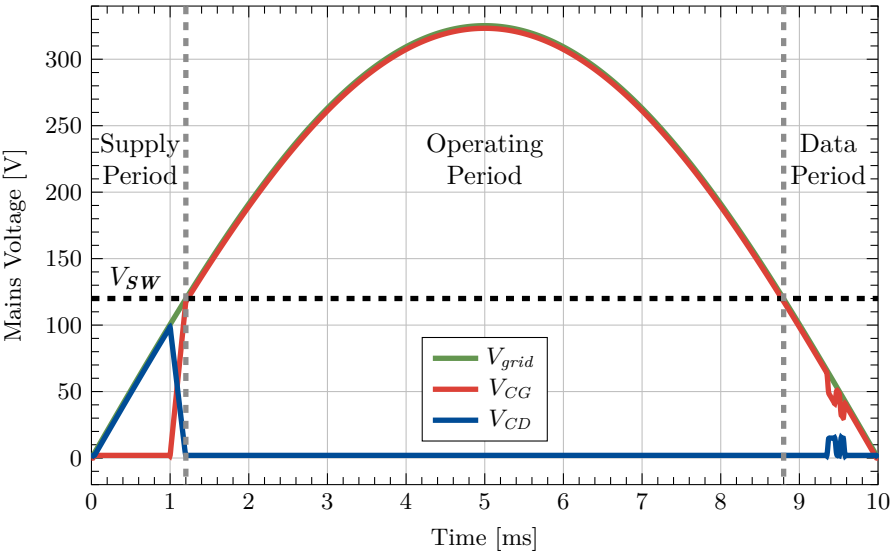


Figure 3.2: Classification of DLT timing periods and expected voltage waveforms at CD and CGs according to the official DLT standard [106].

drops over attached CGs. As the naming mentioned above indicates, the supply period is used to supply a CD with power, e.g. by charging an internal capacitor. During data period the CD modulates its digital control data on the load side of its power line. Since both of the last mentioned periods are quite essential for the DLT communication approach, they will be explained in more detail within the subsequent sections including all relevant specifications, boundary conditions and implications.

3.1.1 Power Supply Boundary Conditions

Typically, light switches or dimmers are connected in series with their light bulbs as shown above in Fig. 3.1. Existing wiring infrastructure – especially in old houses – therefore relies on this two-wire connection and does not provide a neutral wire line at a light switch lead-out. Because rewiring existing buildings is neither desirable nor possible without major efforts and costs, DLT copes with this issue and maintains compatibility by using a suitable bypass structure in series-connected luminaires and CGs. In order to minimize losses

and hence increase system efficiency, the DLT standard permits CDs to supply themselves with power only during the specified supply period and only within very restricted limits as explicated in the following.

The supply period starts at the initial zero crossing of a mains half-wave and lasts until the grid voltage exceeds the threshold V_{SW}. During this time interval nearly the entire voltage drops over the CD, while attached CGs are in a low ohmic state and conduct the desired supply current by means of a bypass structure. Investigating the supply period in more detail, it can further be subdivided into three phases, which are one high current (HC) surrounded by two low current (LC) intervals. The actual power supply of a CD happens during the HC phase, which lasts from $t_1 = 300\,\mu s$ to $t_2 = 700\,\mu s$ after the zero crossing of mains voltage [106], [241]. During this supply time of $t_{supply} = 400\,\mu s$ the DLT standard limits the maximum input current drawn by a CD to $I_{in,max} = I_{CD,HC,max} = 350\,mA$. The two LC intervals may indeed be neglected in terms of power supply but fulfill two other important functions. The first LC phase is needed for a reliable zero crossing detection in a CD ensuring synchronization to mains voltage. Attached CGs help to realize this by providing a low current flow during this time. The second LC phase allows a CD to reduce the voltage drop across its terminals with a defined slew rate [106]. In both LC intervals the maximum current flowing through the CD shall not exceed $I_{CD,LC,max} = 18\,mA$. While the operating CD limits the current flow during HC and LC intervals to the respective maximum values, attached CGs must provide a current bypass that is capable of carrying a current of at least $I_{CG,HC} \geq 400\,mA$ during the HC phase and $I_{CG,LC} \geq 18\,mA$ within the LC phases. However, during the LC phases CGs may not exceed a current draw according to equation,

$$I_{CG}(t) \leq \frac{V_{grid}(t) \cdot P_{CG}}{V_{grid,RMS}^2} + 25\,mA\,. \tag{3.1}$$

Fig. 3.3 shows the described timing, current and voltage relationships during the supply period. In order to realize the desired current paths, the DLT standard allows for a maximum voltage drop of $V_{CG,max} = 20\,V$ across a CG during the HC interval, which in turn diminishes V_{CD}. Fig. 3.3 depicts both scenarios, the ideal (no drop, solid line) and the worst-case (full 20 V drop, dashed line) voltages across the CD [238]. Time interval t_2 to t_3 determines a roll-off phase for CGs to reduce their current bypass from the aforementioned HC level of down to the LC limit. t_4 denotes the cross-over point of $V_{grid}(t) = V_{SW}$, whereas t_5 is specified to a fixed value of $t_5 = 1.2\,ms$ according to the DLT specification [106].

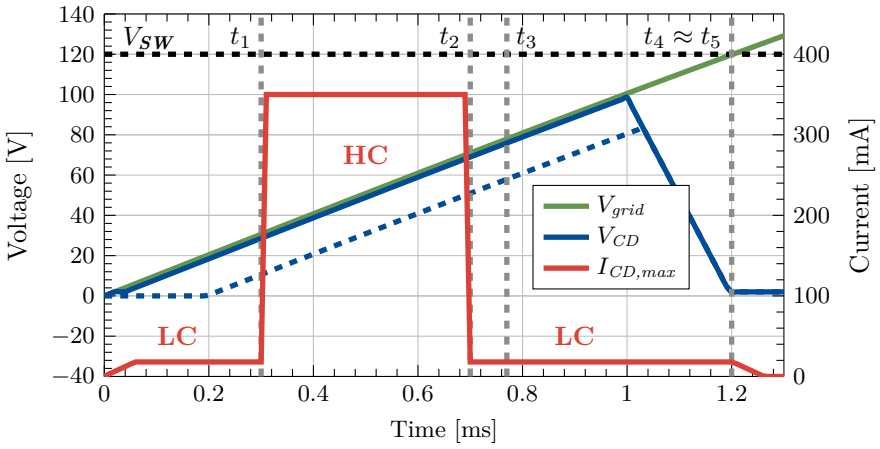


Figure 3.3: Maximum current and voltage ratings during DLT supply period.

3.1.2 DLT Communication

The entire DLT communication happens at the end of a half-wave in the so-called data period. During this period all denoted timings refer to the next projected zero crossing of mains voltage [106]. As mentioned above, the data period begins when the grid voltage passes over the switching level $V_{SW} = 120\,\text{V}$ for the second time. This happens at $t_6 \approx 1.2\,\text{ms}$. CD as well as CGs have to be ready for either data transmission or reception, respectively, until setup time $t_7 = 800\,\mu\text{s}$ is reached. DLT data transmission then happens during the time interval of $t_7 = 800\,\mu\text{s}$ and $t_8 = 250\,\mu\text{s}$. In order to correctly and robustly modulate its data onto the power line, a DLT CD requires a minimum current flow of $I_{CG,LC} \geq 18\,\text{mA}$, which needs to be realized in attached CGs, e.g. by means of a distinct bypass path. This minimum current flow has to be provided until mains voltage falls below a level of $V_{LC,min} = 6\,\text{V}$. Maximum current flow through a CG is again limited according to equation 3.1. During data period mains voltage mostly drops over attached CGs. Of course, the voltage drop over the operating CD is subtracted from it. Until t_7 is reached, the CD still resides in its low ohmic state and hence only features a minimum voltage drop of $V_{CD} = V_{CD,min}$. During data modulation from t_7 to t_8, the signal amplitude of the transmission signal V_{TS} additionally drops over the CD [106], which leads to a total voltage drop of $V_{CD} = V_{Data} = V_{CD,min} + V_{TS}$, with $V_{TS} = 15\,\text{V} \pm 1\,\text{V}$. Fig. 3.4 illustrates a close-up shot of the data period including the relevant

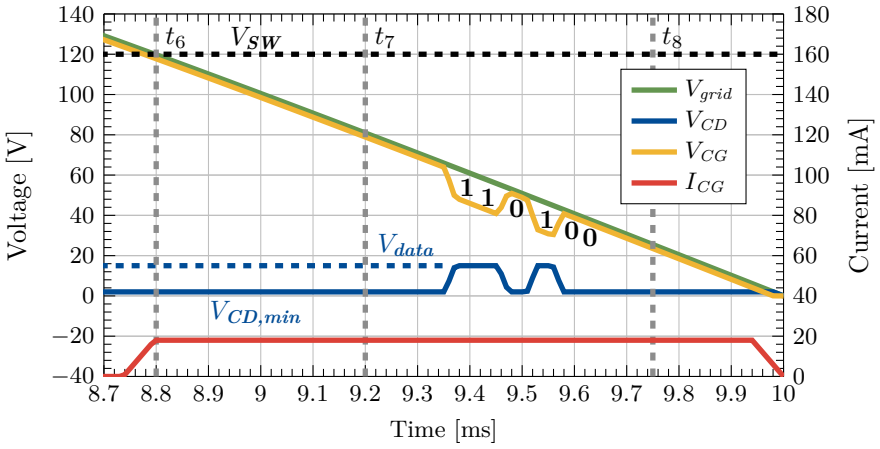


Figure 3.4: Current and voltage signals during DLT data period.

voltage and current waveforms. In addition to that, the graphs highlights the transmission of a single data frame as explained in the following.

In each data period the DLT communication scheme modulates two data bits and incorporates those in a single data frame. Control commands for brightness, color or color temperature adaption are hence transmitted in a telegram structure consisting of successive data frames sent over several half-waves of mains voltage. Considering the European grid frequency of 50 Hz a relatively low transmission rate of 200 bit/s is achieved, which is however good enough for simple control systems, such as intelligent lighting, and might even be enough for ordinary home automation control considering future extensibility of the DLT technology. The two information bits are encoded in a *"Manchester Code"* [106], which uses rising and falling edges to digitize logical ones ('1') and zeros ('0'), respectively. A changeover from high to low level therefore represents a logical zero, whereas a transition from low to high level constitutes a logical one. In this way four data combinations are generally feasible of being transmitted in a DLT frame per mains half-wave, namely '00', '01', '10' and '11'. Although Manchester coding suffers from an inefficient use of bandwidth, it is widely spread in low-cost short range data communication applications [309]. One of the main benefits is the simple timing recovery [86], [274], [309], which is also used in DLT receiver developments shown in chapters 3.2 and 3.4. Other advantages of Manchester coding are its level insensitivity, zero DC content, very fast start-up from no signal condition, self clocking, simple error detection or even signal absence

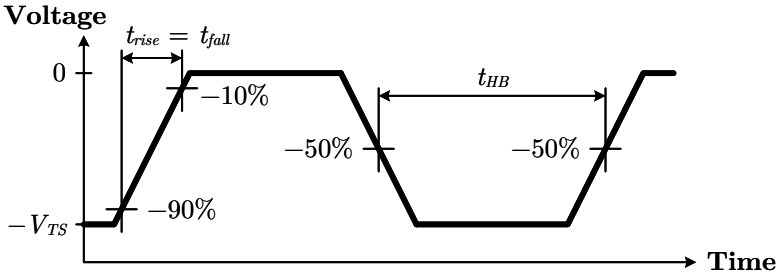
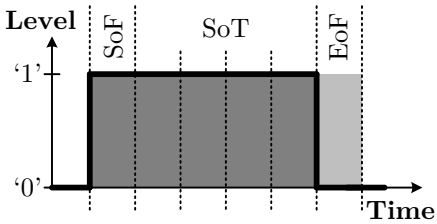


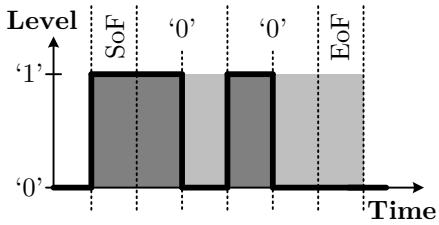
Figure 3.5: Timing and voltage specifications for DLT data modulation.

detection [86], [172], [274], [309]. Manchester coding is indeed also applied in very recent communication technologies, such as VLC [51] or in ambient backscatter systems like radio frequency identification (RFID) [340]. Further information on Manchester coding, possible implementations as well as application examples, may be found in common literature. Fig. 3.5 illustrates the correlation of timing and voltage specifications for DLT modulated signals. Avoiding harmful distortions on the power line, the DLT standard applies strictly defined slew rates that are rather slow. The nominal modulation depth of $V_{TS} = 15\,\mathrm{V}$ is realized at rise and fall times of $t_{rise} = t_{fall} = 22.5\,\mu\mathrm{s} \pm 7.5\,\mu\mathrm{s}$. High and low levels have to be hold for a nominal time interval of $t_{HB} = 50\,\mu\mathrm{s} \pm 7.5\,\mu\mathrm{s}$.

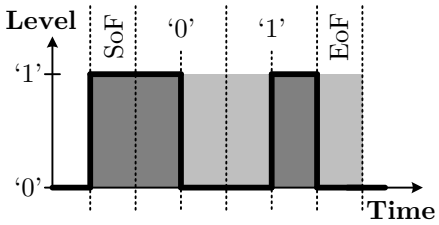
Although DLT applies the Manchester (bi-phase) coding scheme, it can more or less be seen as a simple OOK transmission methodology [97]. In this regard the DLT standard subdivides each data frame sent per mains half-wave by its high and low level regions into six so-called *"half-bits"*. The two Manchester coded information bits thus split into four consecutive half-bits, which are surrounded by one start-of-frame (SoF) and one stop half-bit. Since the SoF half-bit indicates the beginning of a new frame sequence, it is defined to be always set to a high level. This practice allows for a simple and easy detection of a beginning of a new frame. In the same manner and for the same reasoning the stop half-bit, which is also called end-of-frame (EoF) half-bit, consistently remains zero in all possible frame constellations determining the end of a frame sequence. The transmitted frame shown in Fig. 3.4 may serve as an example, as it highlights the high and low states of the individual half-bits. Thereby, it can be seen that the illustrated frame contains the data sequence '00'. In addition to four data containing frames a fifth frame exists, which is used to prefigure a new telegram sequence. Hence it is called the "start-of-telegram (SoT) frame" and builds up upon five consecutive half-bits all being at a high level and one



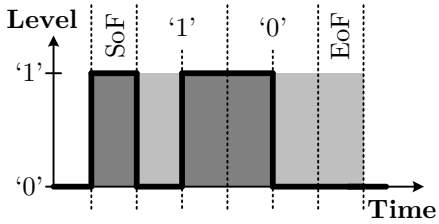
(a) DLT frame sequence ‘*start-of-telegram (*SoT)’.



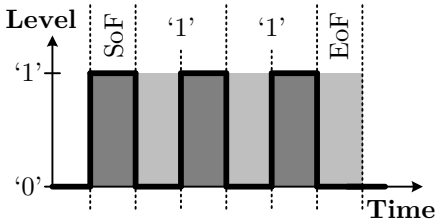
(b) DLT frame sequence ‘0 0’.



(c) DLT frame sequence ‘0 1’.



(d) DLT frame sequence ‘1 0’.



(e) DLT frame sequence ‘1 1’.

Figure 3.6: All possible DLT frame sequences indicating transmitted data bits in used Manchester coding and state of the six corresponding half-bits.

EoF bit, which is set to zero. Thereby, the rule of an SoF and an EoF half-bit being one and zero, respectively, is maintained. Fig. 3.6 consequently shows all feasible frame assemblies that are being transmitted in a DLT system.

As mentioned earlier, control commands are transmitted in a telegram structure by consecutive frames over several half-waves of mains and differ from one another by the so-called telegram type. The DLT methodology allows in total for eight possible telegram types, from which only five are specified so far by the

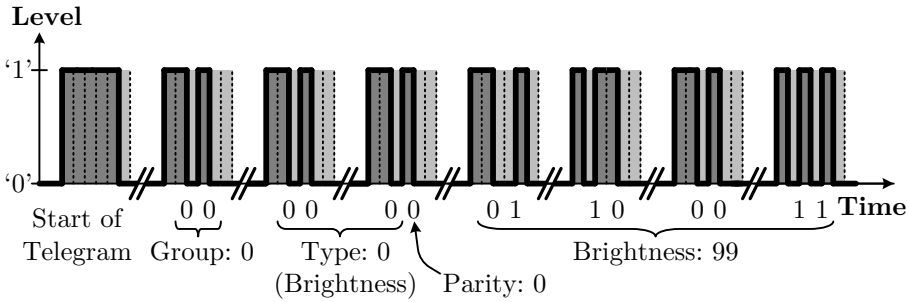


Figure 3.7: Example of a single DLT brightness telegram.

official DLT standard [106]. The other three types are reserved for future use and extensions. Besides the obvious control commands brightness, color and color temperature, the defined telegram types also include a commissioning and a manufacturer specific telegram. While the manufacturer specific telegram – as its name indicates – leaves some freedom to vendors for implementing individual control sequences, the commissioning telegram type is used for assigning one of three possible group numbers to attached CGs. The group commissioning and related group control used in other telegram types might be extremely useful in offices or larger residential rooms to separate different functional units or areas from each other. In this way it is possible to set different brightness levels, colors or color temperatures to luminaires in one part of a room, which could e.g. be a lounge area, than to such ones situated at a dining table in another part of the same room. By this means DLT already enables the possibility to increase energy efficiency on a system level, as unused areas of a single room can explicitly be turned off, while other ones are utilized at the same time.

All transmitted telegrams are assembled in the same manner and frame structure. Depending on the selected telegram type only the total length or moreover the amount of applied payload data varies. Thereby, the first four frames of each telegram type are structured identical as explicated in the subsequent paragraph. Fig. 3.7 exemplarily illustrates the structure of a typical DLT telegram for brightness adjustment. It should be noted that DLT communication always operates at MSB first transmission. This means that the most significant bit (MSB) is followed by bits with decreasing significance and ends with the least significant bit (LSB) [106]. This structure applies to every single frame as well as to any payload data, subparts and even an entire telegram sequence.

Table 3.1: Payload data in dependence of selected telegram type.

Telegram Type		**Payload Data**		**Details**
Code	Name	Bits	Frames	
'000'	Brightness	8	4	0 : telegram controlled off state $1-255$: adjustable brightness
'001'	Color Control	24	12	12 bit for x-coordinate +12 bit for y-coordinate
'010'	Color Temperature	8	4	8 bit integer representation of CCT used according to eq. 3.3
'011'	*Reserved*	–	–	
'100'	*Reserved*	–	–	
'101'	Group Commissioning	2	1	payload frame [m1,m2]=[0,0] other values res. for future use
'110'	Manufacturer Specific Telegram	12 +4 +120	6 +2 +60	12 bit manufacturer ID +4 bit number of payload bytes +up to 16 byte payload data
'111'	*Reserved for Ext. Telegrams*	– –	– –	

A new telegram always starts with an SoT frame indicating the beginning of a new control command sequence. After an SoT frame is being sent, a second frame succeeds, which determines the group number of addressed CGs. A CG only executes received control commands, if its assigned group number coincides with the transmitted one. The two bits used for group control hence offer to distinguish between three different group assignments (groups $1-3$) offering application scenarios as suggested above. Group number 0 is reserved for broadcast transmission. In this case all attached CGs – no matter which group number they are assigned to – must react on such broadcasted telegrams. This is particularly valid for CGs without any group number assignment. The next two frames determine the selected telegram type and a parity error detection. Thereby, their first three bits identify the applied telegram type out of the eight possibilities as explained above, whereas one additional bit is used for parity recognition. DLT employs *"even parity"* error recognition [106], which means that a correctly recorded telegram contains an even number of *"ones"* [120]. If a CG decodes a telegram with an odd number of ones, it must reject the

received telegram because it is erroneous. By applying the described parity method, only single bit errors can be detected [120] and it is not possible to correct those. For multi bit error detection or even any error correction, more sophisticated approaches need to be applied, e.g. those using multiple parity bits and performing forward error correction (FEC), such as *"Hamming code"* or *"Reed-Solomon code"* [120], [154]. These techniques are however not relevant for a simple DLT system but may come into play for a bidirectional communication approach as discussed later in section 3.4. In this context, it also needs to be considered whether it is more energy-efficient to apply FEC or retransmit a sent message [28]. Due to its high robustness the wirebound DLT connection is yet expected to show only little transmission errors, particularly those related to more than single bit flips. CGs not only reject telegrams exhibiting a parity error, but any defective telegram not complying with the specified DLT telegram or frame structure. Furthermore, DLT demands CDs to continuously sent a selected telegram type including the chosen payload data without interruption. This continuous transmission additionally ensures that any falsely detected telegrams would be overwritten automatically by the subsequent correctly received telegram coming shortly after. If the information to be transmitted changes, e.g. by a user-defined input, or if fast response times on a specific control commands are required, a CD may abort transmitting the current telegram and start with the new telegram sequence [106], [305].

After transmitting the four structural frames containing SoT frame, group number, telegram type and parity bit, a DLT CD modulates the corresponding payload data on its load-side of mains. As the length or amount of modulated payload data depends on the transmitted telegram type, table 3.1 denotes the payload data in terms of bit and frame size for each telegram type. Furthermore, this table also states the three bit digit code $[t_1\ t_2\ t_3]$ used in DLT communication for setting the selected telegram type. In addition to that, Fig. 3.8 illustrates the bitwise construction of the five most relevant telegram types according to the official DLT standard [106]. It should be noted that the payload data for both color and color temperature control, which are the (x,y)-coordinate pairs and the CCT, respectively, need to be converted to integer values according to equations 3.2 to 3.3 before transmitting,

$$x_{int} = int\left(\frac{x}{0.84} \cdot 4096\right), \qquad y_{int} = int\left(\frac{y}{0.84} \cdot 4096\right), \tag{3.2}$$

$$c_{int} = int\left(\frac{250000}{CCT} - 0.5\right). \tag{3.3}$$

SoT	Group	Type	Parity	Brightness Value		
All '1'	g1, g2	t1, t2	t3, p	b1, b2	•••	b7, b8

(a) Structure of a brightness telegram.

SoT	Group	Type	Parity	x-Coordinates		y-Coordinates	
All '1'	g1, g2	t1, t2	t3, p	x1, x2	••• x11, x12	y1, y2	••• y11, y12

(b) Structure of a color control telegram.

SoT	Group	Type	Parity	Color Temperature		
All '1'	g1, g2	t1, t2	t3, p	c1, c2	•••	c7, c8

(c) Structure of a color temperature telegram.

SoT	Group	Type	Parity	Commissioning
All '1'	g1, g2	t1, t2	t3, p	m1, m2

(d) Structure of a group assignment/commissioning telegram.

SoT	Group	Type	Parity	Manufacturer-ID	Length	Payload
All '1'	g1, g2	t1, t2	t3, p	m1,m2••• m11,m12	n1,n2•••n3,n4	k1••• k120

(e) Structure of a manufacturer specific telegram.

Figure 3.8: Structure of DLT telegram types.

3.2 Development and Evaluation of Receiver Topologies for DLT Control Gears

In order to establish intelligent lighting control based on DLT communication, the smart LED driver concept outlined in the introduction of this thesis needs to be equipped with a suitable receiver (RX) complying to the specifications listed in the previous section. In fact, it is essential to realize all functional communication features of a DLT CG and integrate these into the smart LED driver. According to the official DLT standard [106] the term *"control gear"* (CG) comprises in addition to communication relevant circuitry also other components between supply line and lamp, e.g. a power supply unit, a PFC block or a lamp controller with an LED driver. The internal setup of a CG in compliance with the DLT standard [106] is shown in the appendix (Fig. A.1). Hence, using DLT naming conventions the smart LED driver presented in Fig. 1.2 can thus be seen as a sophisticated, highly integrated CG.

This work summarizes those parts of a CG that are necessary to enable DLT communication as a subunit under the definition of a so-called "DLT forward

receiver" (FW-RX). Referring to the block diagram shown in Fig. 1.2 this FW-RX thus takes the position of the communication device in the smart LED driver. The differentiation between a DLT FW-RX and a so-called "DLT reverse receiver" (REV-RX) becomes inevitable, since this thesis extends the DLT methodology beyond the official standard towards bidirectional communication, which is explicated later in detail in chapter 3.4. The REV-RX is obviously needed for the return channel and thus situated as a second circuit on other end in a DLT CD [243].

3.2.1 System Concept of an Effective DLT Receiver

The main task of a DLT FW-RX is to retrieve the telegram information modulated by a DLT CD onto mains voltage and evaluate embedded control commands for further processing within the intelligent luminaire. The corresponding receiving procedure can in fact be separated into two individual steps. First, a transmitted data frame needs to be decoupled from mains voltage and its modulated two bit pattern is subsequently filtered to reconstruct the frame in a low voltage domain for further processing, e.g. on a μC. In a second step, the complete telegram is reassembled out of successively sent frame sequences and evaluated according to the selected telegram type. Received brightness values, color coordinates or color temperature may then be forwarded to a smart processing unit that puts the desired control command into action.

To comply with the official DLT standard [106] a DLT FW-RX additionally needs to take care of several other auxiliary functions, such as the synchronization to mains voltage, providing low and high current paths during the respective time intervals or detecting transitions between the different DLT periods within a mains half-wave. Fig. 3.9 reveals the internal structure and setup of the developed DLT FW-RX highlighting all relevant circuit components attributed to the mentioned main tasks. Additionally, table 3.2 summarizes these circuit blocks including their respective function.

Regarding performance of a DLT FW-RX the actual filter clearly represents the dominant key component, as its design directly determines general receive properties, such as signal-to-noise ratio (SNR), BER or overall robustness. Therefore, the main focus is set onto DLT filter design in the following sections and also to some extend onto corresponding decoder units as these two blocks closely cooperate together. It should be noted that the basic concepts of detector and decoder circuits in a DLT FW-RX presented in this chapter have been published and discussed in [235]. The other circuit components, ZCD, bypasses, rectifier and V_{SW}–Detector, only cope with functional tasks, which are indeed essential for ensuring DLT compliance and enabling its way of communication,

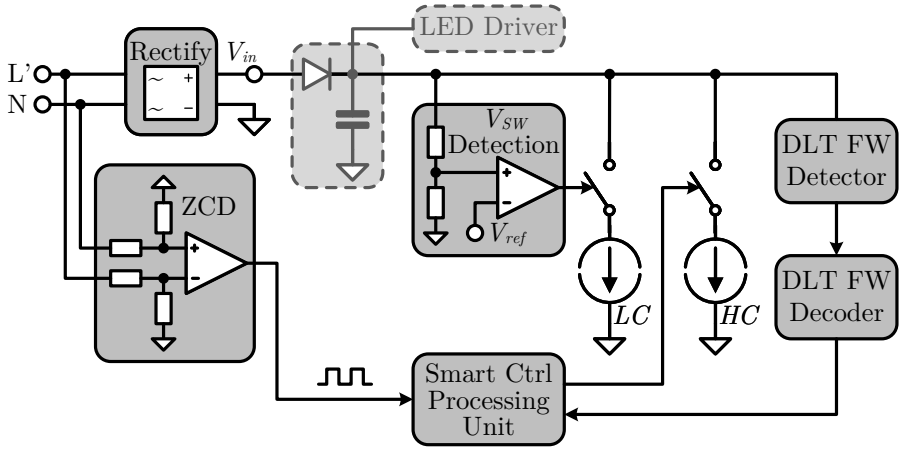


Figure 3.9: Internal setup of a DLT FW-RX.

Table 3.2: Circuit components and correlated functions in a DLT FW-RX.

Component	Functional Description
Zero Crossing Detection (ZCD)	Synchronization to mains voltage
V_{SW}–Detection Circuit	Detecting transitions between different DLT periods within a mains half-wave
Bypass Current Sources	Providing low and high current paths during the respective time intervals
Rectifier	Rectify mains voltage for easier handling of voltage detection and data reception
DLT Filter / DLT Detector	Decoupling, filtering and reconstructing the modulated two bit pattern of a frame sequence
DLT Decoder	Reassembling and decoding of complete telegrams for further processing

but have no significant impact on receiving performance. Nevertheless, the subsequent paragraphs briefly describe some details and practical design aspects for each of these common circuit blocks in the FW-RX with special emphasis on a final target implementation.

Rectifier

The rectifier is only needed for rectifying mains voltage enabling an easier handling of 120 V detection and DLT data reception. Thereby, all functions except for the ZCD can be referred to positive voltage levels with respect to the rectifier's negative output, which is the common ground connection for the entire FW-RX. For a hardware implementation the rectifier can be realized yb a commercially available off-the-shelf (COTS) component. It might also be possible to utilize the rectifier of a luminaire's main power supply as indicated in Fig. 3.9. The sketch exemplarily depicts a simplistic version of a power supply using only a diode and a smoothing storage capacitor powering an LED driver load. The diode is needed to prevent the internal capacitor of the power supply from being discharged.

Zero Crossing Detector

The main purpose of the ZCD is to ensure a proper synchronization to mains voltage. As depicted in Fig 3.9, the ZCD is a simple comparator connected in front of the rectifier to phase (*'L'*) and neutral (*'N'*) wire of the supply grid. It compares the voltage levels on these input lines to one another referencing the local circuit ground. Thus, the ZCD operates as a sign detector indicating a half-wave's polarity. The comparator output hence toggles at every zero crossing of mains between its local supply voltage V_{DD} and ground. A *"smart control processing unit"* as highlighted in Fig. 3.9, e.g. a μC, subsequently evaluates this output signal by triggering on both of its edges to provide the desired zero crossing function and control other circuit blocks in synchronization to mains. Galvanic isolation between ZCD and processing unit could e.g. be realized by employing an opto-coupler [358] or an inductive coupling IC [346].

Fig. 3.10 shows an implementation example of this ZCD concept. Since COTS comparators operate in a low voltage domain, e.g. $V_{DD,max} = 5V \pm 10\,\%$, the large resistive voltage dividers $\frac{R_1+R_2}{R_3}$ and $\frac{R_5+R_6}{R_7}$ are added reducing the input voltage at both terminals before feeding it to the comparator. Resistances R_4 and R_8 may optionally be installed in order to introduce a small offset lifting both inputs up accordingly. This measure could be taken to prevent any negative voltages on the comparator's input terminals. Considering the rectifier limiting any negative voltage on the input lines L' and N by its inherent diodes to a value of $-0.7\,\mathrm{V}$ with respect to circuit ground, negative voltages at the comparator's input terminals become negligible because this slightly negative input voltage is again attenuated by the large resistive dividers.

For an ASIC implementation, resistors R_1 and R_2 as well as R_5 and R_6 have to be placed externally on a printed circuit board (PCB) while the other

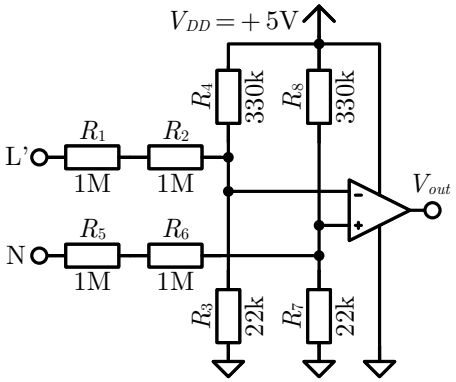


Figure 3.10: Implementation of zero crossing detector (ZCD).

resistances and the comparator can be integrated inside of the ASIC. In doing so, a galvanic isolation of the ASIC is obviously not feasible. This fact needs to be considered when designing the corresponding circuits of the DLT CG.

V_{SW}–Detection Circuit

The V_{SW}–detection circuit measures whether the rectified mains voltage exceeds or falls below the threshold level of $V_{SW} = 120\,\text{V}$. Thereby, its output signal can directly be taken to control the LC bypass, which needs to be enabled in a DLT CG during supply and data period according to the standard [106]. In conjunction with the ZCD, this so-called 120 V comparator additionally ensures that the correct period of operation with respect to the DLT standard [106] is recognized by the smart processing unit. Using an appropriate counter or timer this control unit can hence extract the timing information when to switch the HC bypass and when to prepare the FW-RX for incoming data in time.

The physical setup of the 120 V comparator, which is highlighted in the next paragraph in Fig. 3.12a, is quite similar to the one of the ZCD. A large resistive divider reduces the rectified mains voltage to a low voltage domain, while the second input terminal is connected to a fixed bandgap reference voltage. The ohmic resistance values of the voltage divider have to be chosen according to the selected reference voltage.

Low- and High-Current Bypasses

As explained in previous sections 3.1.1 and 3.1.2, the DLT specifications demand well defined current flows during specific time intervals of a mains half-

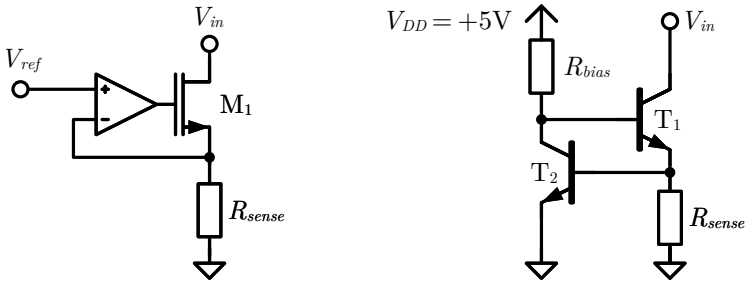
wave. A low current must flow when mains voltage resides below $V_{SW} = 120\,\mathrm{V}$ and a high current path shall be provided from $t_1 = 300\,\mu\mathrm{s}$ to $t_2 = 700\,\mu\mathrm{s}$ after the zero crossing of mains voltage [106], [241] to power the CD. Both current flows need to be realized by attached CGs using corresponding bypass circuits and are limited by the CD with a suitable current limiting circuitry.

Both, the HC and the LC bypass circuit of a CG, can be realized with simple current sources as depicted in Fig. 3.11. The illustrated concepts are advantageous in terms of BOM and circuit complexity while featuring precise accuracy and minimum cutoff voltage drop. Resistance R_{sense} and reference voltage V_{ref} finally determine the current flow, as indicted in equation 3.4,

$$I_{bypass} = \frac{V_{ref}}{R_{sense}} \quad . \tag{3.4}$$

For the concept shown in Fig. 3.11a, V_{ref} may generally be chosen arbitrarily. However, V_{ref} is typically referenced to an available bandgap voltage and is furthermore desired to be kept as low as possible since power dissipation in R_{sense} should be minimized. It should be noted that the bypass source presented in Fig. 3.11a is preferred for a monolithically integrated CG since most HV-CMOS technologies do not necessarily provide high power bipolar devices or only to such a limited extend that their usage would result in a huge area demand. Especially for an ASIC solution of the CG, it is beneficial to implement only one bypass structure for both current levels and simply switch the sensing resistance R_{sense} to another value by digital control, which saves hardware effort and chip area hence reducing costs. More details on the integrated version are presented later in chapter 6.2.

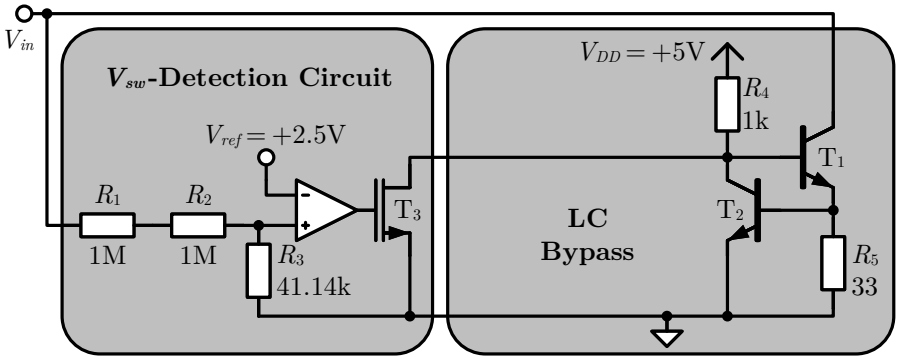
The two-transistor bypass current source shown in Fig. 3.11b is preferably deployed in discrete circuits as its BOM and complexity advantage is slightly better compared to the other concept. That is because of its inherent reference voltage generation by using the base-emitter voltage of transistor T_2. The circuit operates as follows as described in [305]. A current flowing from the auxiliary power supply V_{DD} through resistor R_{bias} into the base of T_1 enables this main transistor. Hence, T_1 conducts, which leads to a current flow through R_{sense}. Once the voltage drop over R_{sense} reaches $V_{ref} = V_{BE,\,T2} \approx 0.7\,\mathrm{V}$, the bipolar transistor T_2 starts conducting and pulls the base of T_1 down. Thereby, current through T_1 is limited according to equation 3.4 in direct dependency of sense resistor R_{sense}. The tolerances and variations of the sensing resistor thus directly impact current accuracy, which represents the main drawback of this circuit. Either a precise sense resistor needs to be used or, if allowing for larger tolerances, the target current has to be increased, which in turn yields a decreased overall efficiency. Investigating the minimum cutoff voltage, this



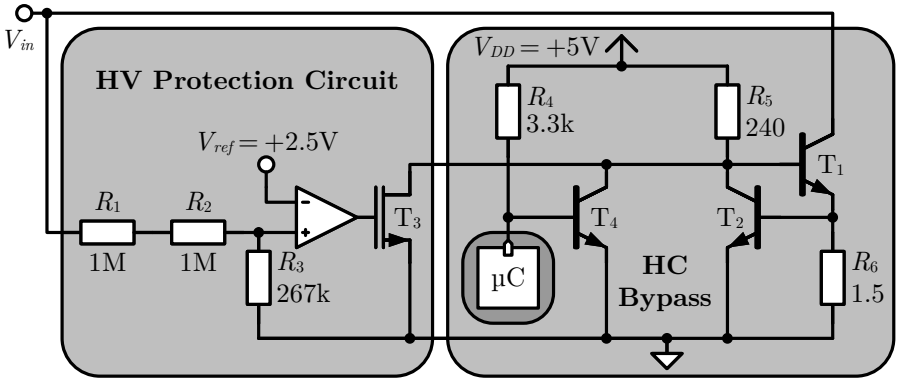
(a) MOSFET based current source. (b) Bipolar based current source.

Figure 3.11: Implementation examples of different current sources suited as bypass circuits in a DLT CG.

bypass circuit only requires one base-emitter junction and the saturation voltage of T_1 to conduct the desired current. Thus, it can operate even for input voltages lower than 1 V. Considering the voltage drop over the installed rectifier of two forward diode voltages of approximately $V_{rect} = 2 \cdot V_{diode} \approx 2 \cdot 0.7\,\mathrm{V} = 1.4\,\mathrm{V}$, the worst case voltage drop is about 2.4 V, which is well below the specified DLT limits. Thus, thee full current of the targeted set level is sustained down to mains voltages below 3 V. Although the bypass itself is fully DLT compliant, it relies on the auxiliary power supply voltage V_{DD} that needs to be provided somehow. A conventional SMPS or an AC-DC converter is however not suitable for an implementation of a DLT CG, since these circuits suffer from a significant start-up time. Therefore, an additional start-up circuit is required that can directly operate from mains voltage and supply the bypass current source immediately after power-on. Fig. 3.12 depicts the hardware implementation for LC and HC bypass circuits that is applied for evaluating DLT FW-RX performance of the different filter concepts introduced in the next chapter. The two-transistor bypass current source shown in Fig. 3.11b has been selected for the realized hardware setup because the receiver comparison founds on real measurements of a discrete CG implementation. The circuit schematics of the LC bypass also contain the V_{SW}–detection, which is used to directly turn the bypass current source off, once mains voltage passes over the threshold level V_{SW}. This is achieved by the opamp enabling transistor T_3, when the divided mains voltage is higher than the selected fixed reference. Consequently, T_3 conducts and pulls the base of the main transistor T_1 to ground disabling the bypass. For the presented implementation the switching level V_{SW} has been set to 124 V by dimensioning the resistive divider according to a reference voltage



(a) LC bypass with V_{SW}–detection circuit.



(b) HC bypass with HV protection circuit.

Figure 3.12: Implementation of LC and HC bypass circuits for DLT FW-RXs.

of $V_{ref} = 2.5\,\text{V}$. This slightly higher value compared to the ideal minimum of 120 V is chosen for two reasons. First, to account for any component variations and second, to particularly consider the turn-on delay of the bypass when entering the data period because the full current must be flowing when mains voltage falls below $V_{SW} = 120\,\text{V}$. The nominal value of the LC bypass current source is set to 18.2 mA according to equation 3.4 considering a base-emitter voltage of T_1 of 0.6 V [359]. The auxiliary supply is kept at a fixed level of 5 V.

While the LC bypass may be turned on and off automatically by the comparator output signal, the HC bypass requires a decided timing control of the central processing unit, e.g. from a μC. Therefore, transistor T_4, which can

be switched by such a digital control signal, is added to the circuit in contrast to the LC bypass setup. The digial processor disables transistor T_4 at 300 µs after zero crossing of mains, which consequently lets the base of T_1 settle to the desired target level of about two diode forward voltages. Thereupon, the HC bypass conducts and regulates for a target current level of 400 mA with respect to equation 3.4 and considering the V_{BE} - drop of T_2 of about 0.6 V. It should be noted that the auxiliary resistor R_1 is set to a much smaller resistance value compared to the LC case, which results in a higher quiescent cross current. This measure needs to be taken because of the low current amplification of T_1 at high collector currents. At the expense of a slightly higher cutoff voltage a Darlington transistor may be used instead of T_4 leading to reduced quiescent current consumption. The disable circuit on the left handed side in Fig. 3.12b is not the 120 V comparator, but a protection circuit, which disables the HC bypass for input voltages higher than 21 V. By this means the main transistor T_1 is protected against excessive power loss, if no CD is installed upfront connecting the bypass directly to mains or if the CD even suffers from a short circuit failure.

3.2.2 Architecture and Implementation of Different DLT Detector and Decoder Circuits

Clearly, the filtering DLT detector and a suited decoder unit form the most relevant circuit components in a DLT FW-RX since they directly determine overall receiver performance regarding sensitivity, error rate, robustness, complexity and power consumption. As stated in table 3.2, the detector unit copes with decoupling, filtering and reconstructing of any DLT modulated bit pattern of a single frame sequence, whereas the decoder records all received frames, reassembles those to a complete telegram and decodes the resulting telegram structure according to the DLT specification. The obtained control command can then be used for further processing translating it into action.

Enabling smart LED drivers with a small form factor [235] the detector design aims for providing simple but robust DLT receiver solutions that can easily be monolithically integrated in a SoC. This particular requirement therefore puts special restrictions on the detector design, e.g. limiting values and sizes of employed components or dictating maximum applicable voltage levels for a chosen complementary metal-oxide-semiconductor (CMOS) technology. This limiting factor becomes crucial when considering that the rectified mains frequency of 100 Hz is present in the actual signal spectrum because a DLT CD repetitively transmits DLT data on every half-wave of mains voltage. Depending on the modulated (payload) data the signal frequency of the wanted DLT pattern

is however only one to two decades higher than that. Thereby, filtering the complete DLT signal with a typical bandpass based approach, which might have been the most obvious solution, implies two major issues. First, a bandpass structure with very high attenuation would be required in order to suppress disturbing influences originating from grid frequency [235]. Such a concept hence demands bandpass filtering of higher order, which increases design complexity significantly. Second, and even more restrictive, a bandpass filter with a center frequency of about 5 kHz to 10 kHz requires relatively high component values of employed capacitors and resistors. Thereby, this classical approach becomes impractical for a monolithically integrated DLT FW receiver solution [235].

Considering the finite slew rate of the DLT modulated data pattern, a better suited solution can be found taking the concept of edge detection into account. Obviously, the edges of a data signal comprise higher frequency components [235], which consequently allows to design bandpass filters at higher center frequencies. Thus, building an edge detector also leads to using smaller component values of employed capacitors and resistors. All of the DLT FW-RX concepts presented in the following therefore rely on the edge detection principle.

3.2.2.1 Detector Concept A: Active Bandpass with Schmitt-Trigger

The first DLT detector concept is based on a typical active bandpass structure. It differentiates the incoming DLT data signal and thereby transforms the slew-rate defined signal edges into distinct positive or negative pulses with respect to the common mode voltage. Afterwards, a Schmitt-Trigger converts these pulses into a digital signal for further processing. Fig. 3.13 illustrates the proposed filter structure including dimensioning for an implementation with discrete, commercially available off-the-shelf (COTS) components. Component sizes and values are still well suited for a monolithically integrated solution of the proposed detector concept. A Zener diode D_1 is added to the circuit for protection from any overvoltage originating from mains. It clamps the voltage level at that point to maximum of about 5.1 V.

The high-pass filtering part of the bandpass based detector concept is used to remove most of the rectified high-voltage 100 Hz sine-wave of mains voltage. The low-pass filtering part of the applied bandpass structure lets high frequency components of the slew-rate defined edges pass while it filters higher frequency components of any grid disturbances out. Equation 3.5 shows the corresponding transfer function of the proposed bandpass filter,

$$H(j\omega) = \frac{-j\omega R_5 C_1}{(1 + j\omega(R_1 + R_2)C_1) \cdot (1 + j\omega R_5 C_2)} \quad . \tag{3.5}$$

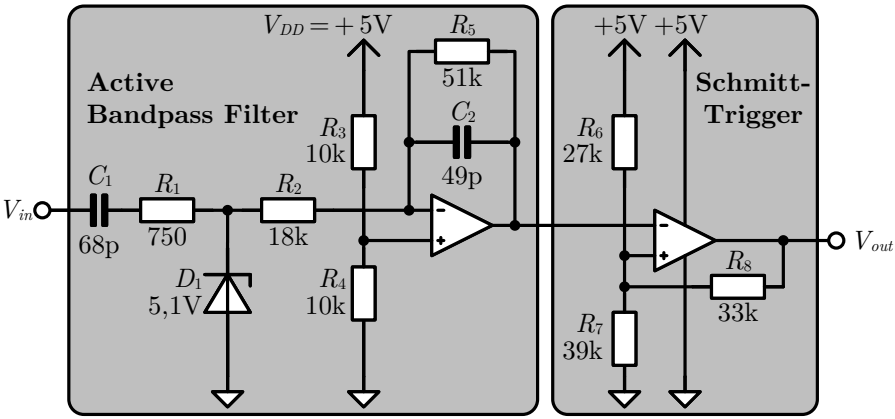
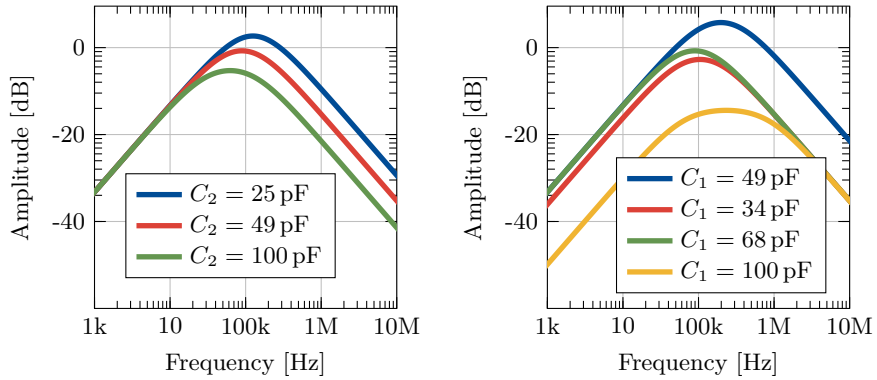


Figure 3.13: Concept *A*: Active bandpass with Schmitt-Trigger [235].

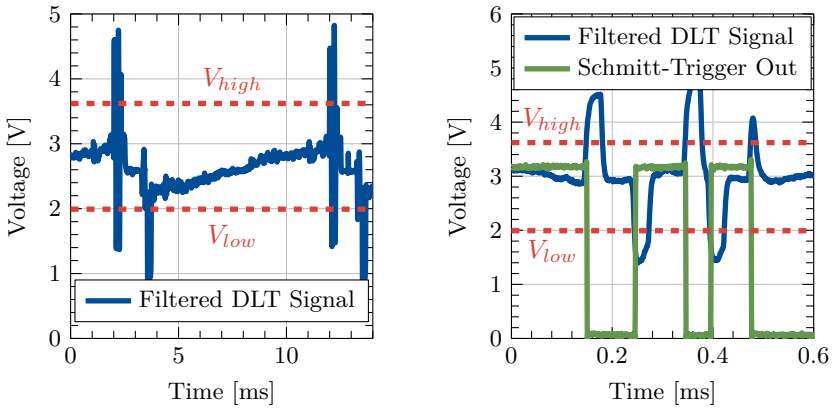


(a) Transfer function for $C_1 = 68\,\text{pF}$ and different C_2 values.

(b) Transfer function for $C_2 = 49\,\text{pF}$ and different C_1 values.

Figure 3.14: Transfer functions of the active bandpass filter for different variants.

The component values shown in Fig. 3.13 are chosen for realizing a bandpass center frequency around 88 kHz. Reducing capacitance C_2 enables tuning of the center frequency. This measure however increases the bandwidth of the active bandpass filter accordingly by shifting the cut-off frequency of the low pass filtering part to higher frequencies. Fig. 3.14 shows the effects on the transfer function of equation 3.5 when tuning capacitances C_1 and C_2 accordingly.



(a) Measured output signal of analog BP filter in DLT FW-RX concept A.

(b) Close-up shot of measured DLT signals in DLT FW-RX concept A.

Figure 3.15: Measured waveform signals of detector concept A in a DLT FW-RX during DLT data period using $C_2 = 49\,\text{pF}$.

For performance evaluation two variants of this detector concept have been implemented. Capacitor values of $C_{2,a} = 49\,\text{pF}$ and $C_{2,b} = 25\,\text{pF}$ have been used resulting in center frequencies of 88 kHz and 125 kHz, respectively. Fig. 3.15a and Fig. 3.15b show measurements of the bandpass filtered signal at the Schmitt-Trigger input for an implementation with $C_2 = 49\,\text{pF}$.

Apparently, the common mode voltage at the Schmitt-Trigger input resides around 3 V for the presented implementations. The hysteretic threshold values for high and low output level of the Schmitt-Trigger have been set to $V_{low} \approx 2\,\text{V}$ and $V_{high} \approx 3.6\,\text{V}$, respectively, as indicated in Fig. 3.15a and 3.15b. Comparing the filtered DLT data signal to these threshold levels, the Schmitt-Trigger performs already a signal digitalization because it operates as a 1 bit ADC [235]. Thereby, it inherently reconstructs the DLT data pattern as desired. This digital output signal is also shown in Fig. 3.15b and can directly be forwarded to a μC or any other digital processing unit. In case an isolation from mains voltage of the digital processing unit is needed, an optocoupler circuit can be inserted in between. Although galvanic isolation would not be feasible for a monolithically integrated approach, the presented DLT detector concept is attractive and favorable for an integrated design because it is easy to implement in the analog domain, automatically provides digitization for any further processing unit and features low circuit complexity.

3.2.2.2 Detector Concept B: Resistive Divider & Digital Filtering

The second DLT FW detector concept founds on a digital filtering approach, which is performed on a μC [345] in the presented implementation. In order to use a digitally based signal evaluation, it is essential to decouple the DLT modulated data signal from mains voltage and perform an appropriate digitization in a first step. Subsequently, the digitized signal can be filtered and reconstructed in the digital domain for further processing, such as the DLT telegram evaluation. Fig. 3.16 depicts the concept schematics of a digitally based DLT detector circuit including dimensioning for the analog resistive divider.

As can be seen, decoupling and digitalization is performed by a resistive divider in conjunction with an ADC. The resistive divider brings the amplitude of the grid voltage down into the 3.3 V domain of the employed μC [345]. For the presented setup with discrete COTS components the HV part of the resistive divider is built by two distinct (1206)–SMD resistors of the same value because each of them is only rated for a maximum voltage of 200 V. Since both resistors have the same value, they share the voltage equally between them. To account for a certain security margin, the resistor values have been selected so that the peak grid voltage $\hat{V}_{grid} = \sqrt{2} \cdot V_{grid,RMS} = \sqrt{2} \cdot 230\,\mathrm{V} \approx 325\,\mathrm{V}$, if showing an overshoot of about 10 %, stays well below the maximum of 3.3 V. Additionally, diode D_1 is added to protect the input of the μC from any harmful overvoltage. The resistive divider has been designed as a trade-off between quiescent current and input resistance to the ADC. Considering the selected resistor values a quiescent current through the resistive divider of about

$$I_q = \frac{V_{grid}}{R_1 + R_2 + R_3} \approx 114\,\mu\mathrm{A} \tag{3.6}$$

is expected to flow yielding a power consumption of at least

$$P_q = V_{grid} \cdot I_q \approx 26\,\mathrm{mW}\,. \tag{3.7}$$

The μC performs the analog to digital conversion by means of an 11 bit ADC for input voltages from 0 V to $\frac{V_{CC}}{1.6} = 2.0625\,\mathrm{V}$. Hence, grid voltages above 231 V are clipped in the digital domain. Since DLT modulates its data onto mains voltage only below a level of $V_{SW} = 120\,\mathrm{V}$ at the end of a half-wave, this clipping is not critical for data reception. In order to better use the ADC resolution to its full capacity, it can in fact be thought of an analog clipping by changing the dimensioning of the resistive divider. In this case, overvoltage protection for the MCU is regularly performed by diode D_1 in each half-wave of

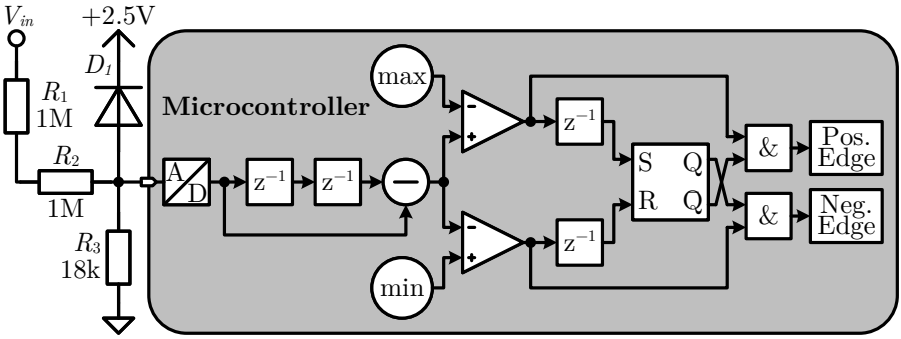
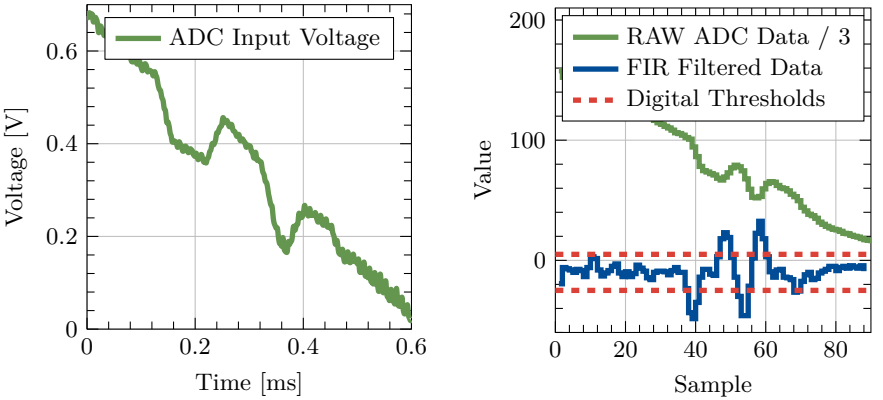


Figure 3.16: Concept B: Resistive Divider with Digitial FIR Filter [235].



(a) ADC input voltage measurement. (b) Digitized and processed DLT signal.

Figure 3.17: Measured waveform signals of FW-RX concept *B*.

mains. The effective usage of the ADC resolution is more crucial for an ASIC implementation and will hence be further discussed in chapter 6.2.

The sampled waveform is passed through the digital filter as depicted in Fig. 3.16. The delay elements form in conjunction with the sampled input signal and the subtraction element a third order finite impulse response (FIR) filter acting as a differentiator [235]. The resulting signal is fed into a window comparator, which detects rising and falling edges and passes the corresponding logical levels to the AND gates and delayed by one clock cycle to the flipflop

inputs. The SR-flipflop and the AND gates prevent detection of consecutive edges of the same polarity. Fig. 3.17a and 3.17b show the input signal to the ADC and the digitized signals including selected thresholds, respectively.

As can be seen from Fig. 3.17a, recurrent spikes are noticeable on the grid voltage during the data period for the presented implementation and dimensioning. These periodical spikes originate from the internal sample-and-hold circuit of the μC's ADC and are related to the relatively high ohmic input node of the resistive divider. However, the magnitude of these spikes hardly changes over the relevant voltage range and hence only causes a constant offset on the digitized signal. Since the digital differentiator operates as a high-pass filter, it completely removes this offset component of the input signal. Therefore, the periodical spikes generated by the internal sample-and-hold circuit do not affect robustness of the receiver significantly and are hence negligible for the presented implementation. Changing the resistive divider, e.g. by increasing the lower resistance R_3, might however aggravate this issue, which could consequently lead to problematic behavior, such as an increased failure rate of received telegrams. In this case adding a filtering capacitor to ground, connected in parallel to R_3, reduces the described issue. Yet, it needs to be taken care that this measure does not affect or distort the input signal of the ADC too much, since the additional capacitor forms a low-pass filter in conjunction with the resistive divider. If not properly designed, this low-pass filter could smoothen or even flatten the DLT modulated data on the scaled down input voltage so much that reliable detection is not possible anymore or only with decreased robustness and higher error rate.

3.2.2.3 Detector Concept C: Differential Analog Subtraction Filter

Aiming to directly generate the desired data signal at its output, the third DLT FW detector concept follows the idea of a subtraction in the analog domain. If an ideal 50 Hz sine-wave was subtracted from the DLT modulated mains voltage, the two 50 Hz signals would cancel out resulting in a DC voltage level with the DLT modulated data signal on top of it at the respective points of time. Fig. 3.18 illustrates the actual circuit implementation of this conceptual idea including dimensioning of analog components. The odd resistance values for R_4 and R_6 arise from connecting two regular E24 resistors in parallel.

The MCU generates the ideal sine-wave voltage by means of a lookup table (LUT) and an internal digital-to-analog converter (DAC) circuit. For the presented setup an inverse sine-wave is synthesized as the resulting analog signal as well as the divided mains voltage are added at the negative input of an opamp. This corresponds to a subtraction of an ideal, non-inverted sine-wave from mains.

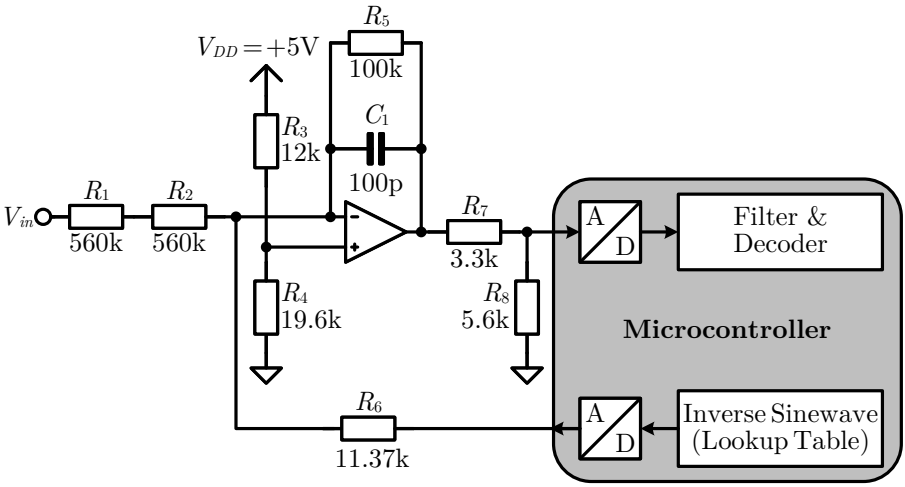
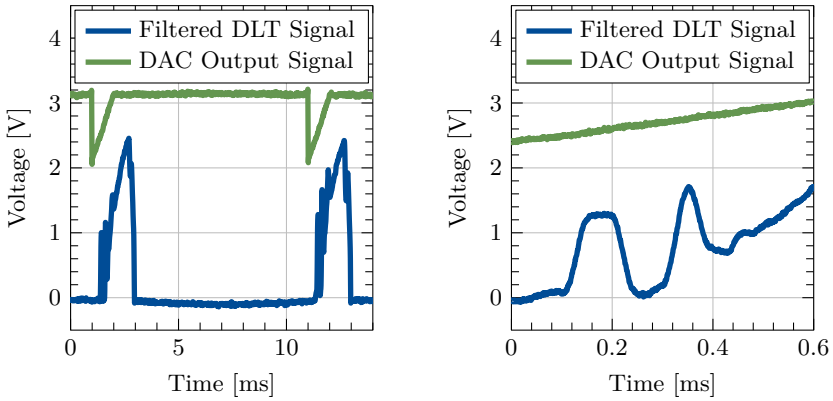


Figure 3.18: Concept C: Differential Analog Subtraction Filter [235].



(a) DAC output and filtered DLT signal in DLT FW-RX concept C.

(b) Close-up shot of measured DLT signals in DLT FW-RX concept C.

Figure 3.19: Measured waveform signals of FW-RX concept C.

The opamp does not only deal with the subtraction of the sine-wave signals but also provides a low-pass filtering of the resulting difference signal. Subsequently, the signal is sampled by an ADC of the employed μC. A resistive voltage

divider reduces the grid related input voltage to levels below 3.3 V. Fig. 3.19a and 3.19b depict the filtered difference signal as an input to the ADC as well as the DAC output waveform. In order to save memory in the μC, the DAC only operates during the DLT data period. The needed memory M_{store} for the LUT depends on the DAC resolution, the targeted sampling rate $f_{sample} = \frac{1}{t_{sample}}$ and the output time duration T_{out} as shown in equation 3.8,

$$M_{store} = \frac{M(N_{DAC}) \cdot T_{out}}{t_{sample}} \,. \tag{3.8}$$

The output time interval hence linearly increases the memory storage. As the DLT data period lasts 1.2 ms, it represents only a 12 % fraction of one 10 ms lasting mains half-wave. The limited output time duration therefore reduces the required memory storage of the LUT by 88 %. Considering a 12 bit DAC operating at a sampling rate of $f_{sample} = 100\,\text{kHz}$ and the μC storing a 12 bit DAC output data word in 2 byte of memory ($M(N_{DAC} = 12\,\text{bit}) = 2\,\text{byte}$), the LUT requires 240 byte instead of 2000 byte, which would be needed for an entire half-wave. If only a tiny μC shall be used, this represents already a considerable amount of memory, especially since the same calculation must be applied to the ADC sampling mains voltage. Hence, also the ADC is only operated during the short time interval of the DLT data period.

As can be seen from Fig. 3.19, the filtered difference signal shows a moving offset, which distorts the DLT modulated data. This deviation comes from differences in the actual mains voltage compared to an ideal sine-wave. Any irregularities of mains voltage from its ideal counterpart regarding voltage level, waveform shape or timing deviations directly result in additional changes because the two 50 Hz sine-waves do not cancel anymore in that case. Also, any offset or delay between the zero crossing and the DAC output of the DLT detector would hence cause moving offset deviations on the difference signal. Obviously, this behavior would thus decrease effective SNR and lead to diminished robustness. To enhance detection quality of this concept an additional high-pass filtering and edge detection of the sampled data is conducted in the digital domain on the MCU. In fact, the digital processing is identical to that of the fully digital approach presented in section 3.2.2.2. This measure however increases complexity in contrast to the other detection concepts.

3.2.2.4 DLT Decoder for Edge Detection based DLT FW Receivers

Once an employed DLT FW detector has decoupled, filtered and reconstructed the DLT data pattern from mains voltage, the DLT decoder unit resumes evaluation of the transmitted data. For that purpose the decoder only needs to

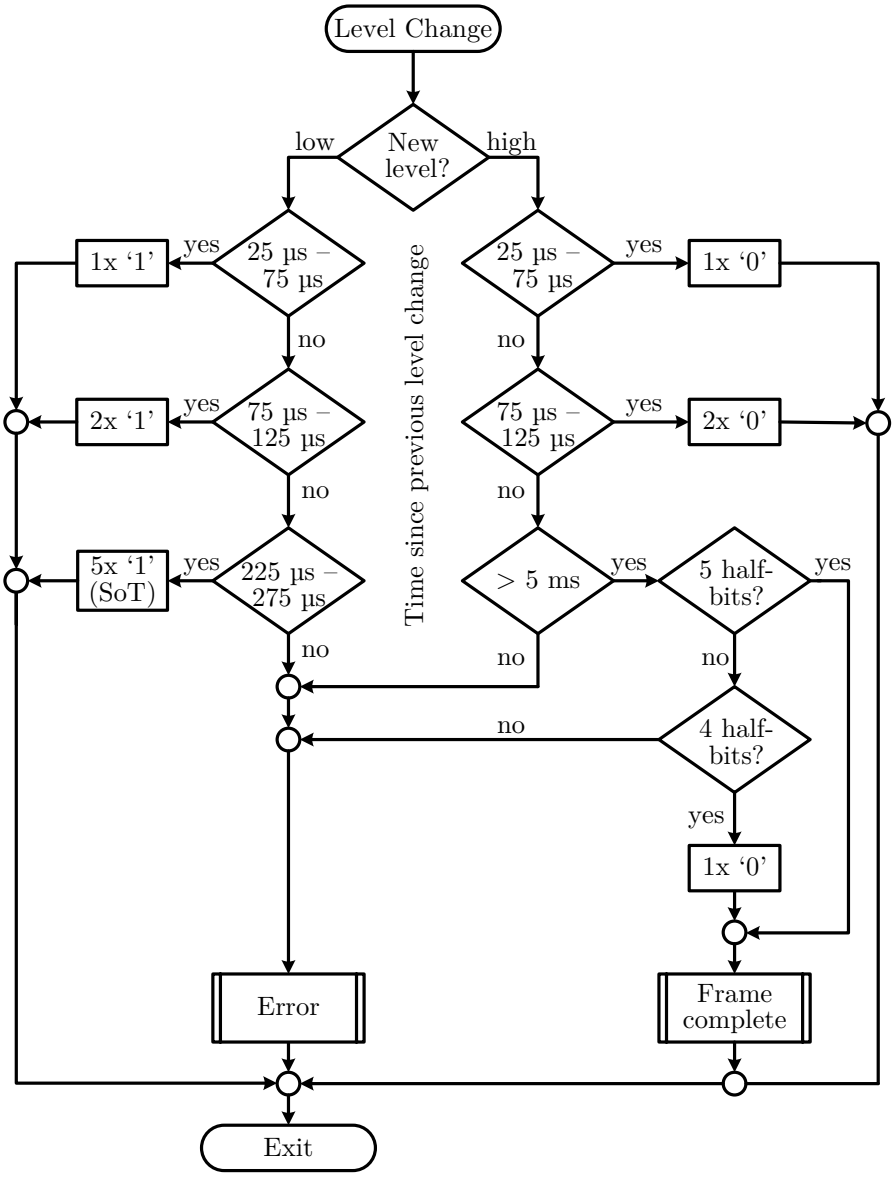


Figure 3.20: Flowchart of the DLT frame decoder for detector concept *A*.

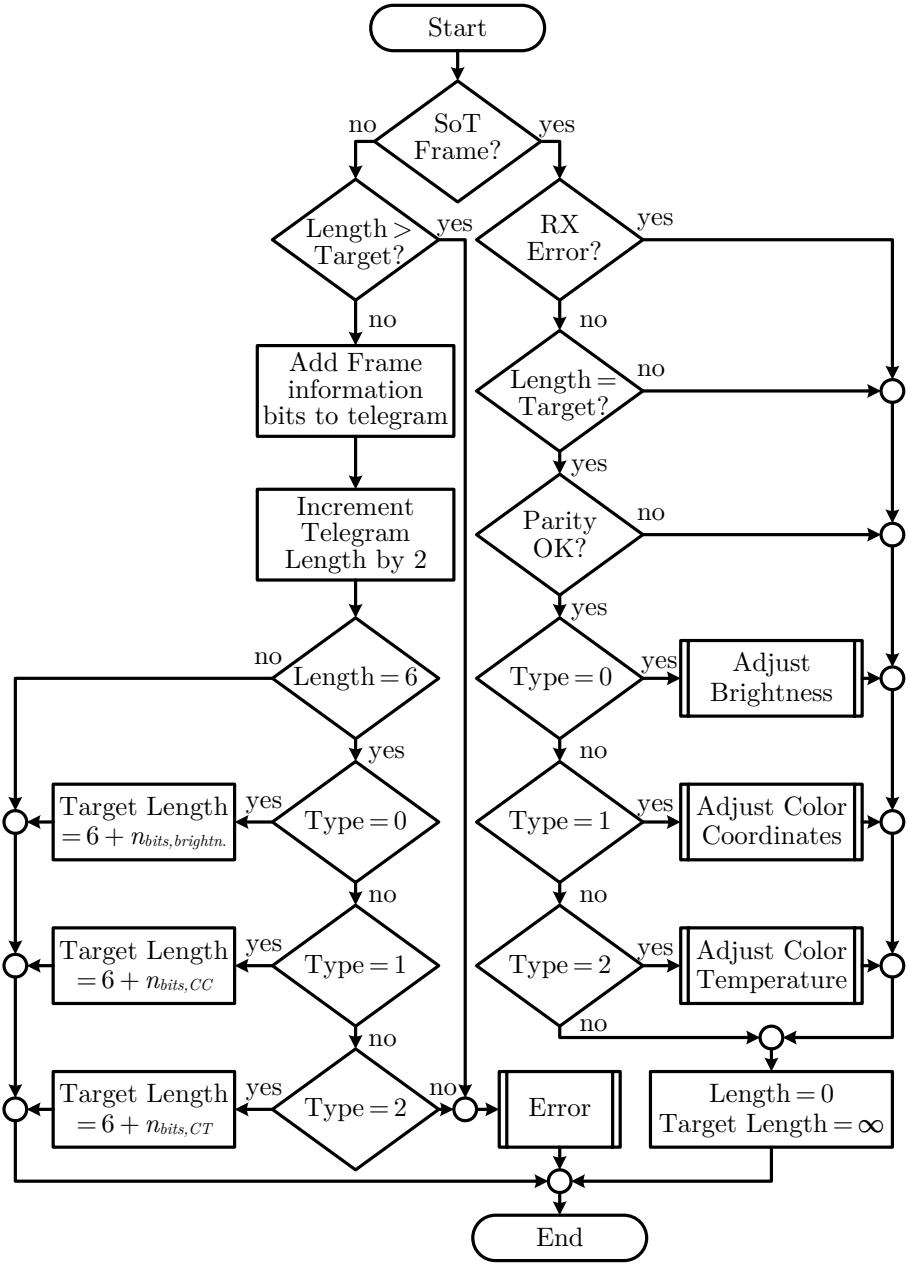


Figure 3.21: Flowchart of the DLT telegram reconstruction and evaluation.

evaluate received frames, reassemble them into complete telegrams and analyze received telegrams according to their type. In doing so the decoding procedure can be split into two separate processes, a frame decoding and a telegram evaluation. Both digital routines have been fully implemented on a μC for verification purposes and are explained individually in the following.

Since all presented DLT FW detector concepts rely on edge detection, the frame decoding process can simply apply a counter to decode the received frame bits. Measuring the time between two adjacent edges the decoding routine determines the time of logical *'low'* and *'high'* periods of the data signal. It thereby decodes the binary data of each half-bit and subsequently stores it in a register. The Manchester-coded information bit values have to be restored afterwards by a state-machine according to the five independent frame assemblies described in section 3.1.2. Fig. 3.20 exemplarily shows the flowchart of the decoder's half-bit evaluation for DLT FW detector concept *A*. The flowchart of the frame decoder would look slightly different for detector concepts *B* and *C* although the same measuring principle is applied. This is because their software procedure evaluates a frame sequence once it is completely sampled, while the decoding routine of detector concept *A* analyzes received edges continuously during a current frame reception. The corresponding flowchart of the frame decoding process for detector concepts *B* and *C* can be found in the appendix (Fig. A.3).

Every time an edge occurs, the depicted routine evaluates the current logic level. Depending on the time difference to the previous edge, the respective half-bit value(s) is (are) saved in a register. By this means it is possible to detect all five cases of frame assemblies as described in section 3.1.2. If the half-bits' timing relation of these predefined frame structures is not met, an error is detected. At the beginning of a new frame sequence the decision engine will always follow the path depicted on the right side since a SoF half-bit always causes a positive edge detection. To clearly identify the start of a new frame the software procedure then checks, whether a long time (*here:* 5 ms) has passed as the last data period has preceded the current one for almost 10 ms. After recognizing the start of a new frame, the state machine finalizes the previously recorded frame for further processing by the telegram evaluation routine. For this purpose, it checks whether four or five half-bits have been recorded in the previously recorded frame. In case of a four half-bit sequence an additional '0' has to be added because the EoF half-bit did not generate an edge as it equals zero. If less than four half-bits have been recorded, the frame detection procedure outputs an error. Subsequently, the evaluation subroutine is called, which converts the recorded half-bit sequences into the two transmitted information bits as illustrated in Fig. 3.6 and then performs the telegram

evaluation. The flowchart for this telegram reconstruction and evaluation is illustrated in Fig. 3.21 for the three most relevant telegrams, brightness, color and color temperature.

At first, it is checked whether the latest frame indicates the start of a new telegram. This step is performed for synchronization. Once an SoT-frame has been received, the previously recorded telegram is evaluated. In case no telegram has been detected yet (start-up), the examination of actual and target telegram length will yield a *'no'* because the actual telegram length is initially set to zero and the target length is initialized to be infinite. When receiving regular data frames, the decoder will follow the left-handed part of the flowchart. Within this path the two data bits of the current frame are added to the current telegram, unless the telegram length has exceeded its target limit. Afterwards the telegram length is increased by two. When a length of six is reached, the telegram type can already be determined. The target length for the current telegram is now set corresponding to the telegram type. The following information bits represent the payload data of the telegram and are simply added to the current telegram. When the next SoT-frame occurs, the previously received telegram is evaluated. The described algorithm has also been implemented on the μC.

It can be seen that error detection has been introduced on half-bit, frame and telegram level. Telegram length and parity bit represent a further security mechanism to prevent from decoding false signals. If an error is detected within any of these levels, the entire telegram is ignored.

3.2.3 Performance Evaluation and Comparison of Implemented DLT-Receiver Architectures

All receiver concepts have been implemented in hardware using an MCU [345] for digital signal processing, decoding and evaluation as described in chapter 3.2.2. Fig. 3.22 presents a photo of the employed test board. Due to providing galvanic isolation by means of distinct opto-couplers [358], the μC is situated on a second board – shown in the appendix (Fig. A.2) – and can therefore not be seen here. In the presented photo 3.22, filter concepts B and C have not been installed on the test board, as they have been mounted later on a similar board. Still, their corresponding place holders for the required SMDs are visible.

Evaluation and comparison of the different DLT FW-RX filter architectures mainly focuses on robustness, complexity and power consumption, while considering a later on-chip integration. Sensitivity and error rate analysis is included in the robustness discussion. Since these main aspects have to be reasonably balanced for a suitable trade-off in a final target SoC implementation, the sub-

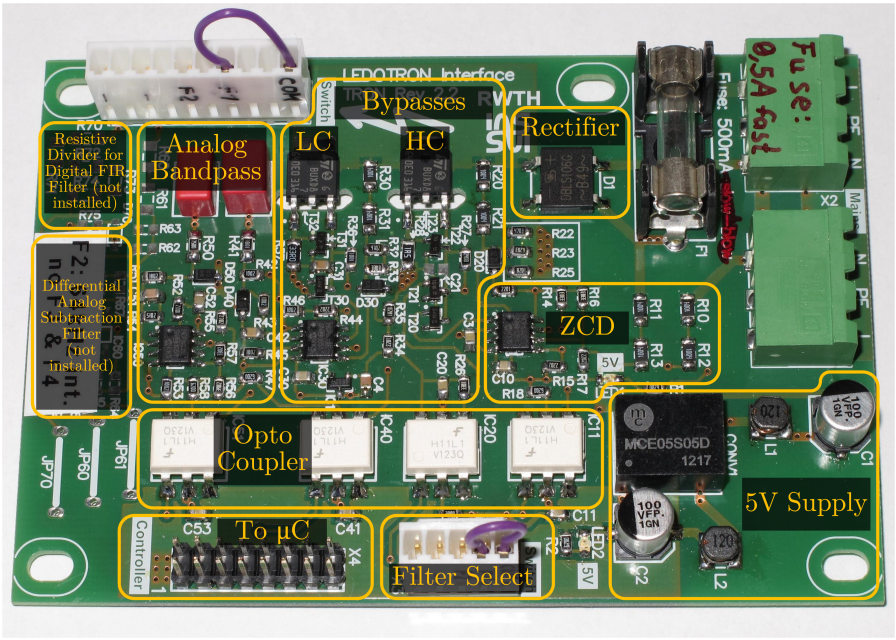


Figure 3.22: Test board of a fully functional DLT FW-RX using filter concept *A*.

sequent paragraphs summarize performance evaluation regarding the mentioned parameters for each receiver concept and provide a concise comparison.

Circuit Complexity

Circuit complexity can easily be compared among the presented receiver concepts by estimating number and prices of used COTS components as well as evaluating necessary implementation effort, particularly for a later ASIC solution. As stated in section 3.2.2.1, detector concept *A* features very low circuit complexity due to its simple analog structure, which only employs two opamps and several passive components. For an integrated design, the second opamp and resistors R_6 to R_8, which form the Schmitt-Trigger altogether, can simply be replaced by a few transistors making an ASIC implementation less elaborate. Different Schmitt-Trigger solutions with (programmable) hysteresis have been proposed and analyzed using only either four, six or eight transistors [107], [399] or standard CMOS inverters [293]. Beyond that, the inherent digitization of the

DLT data signal provided by concept A represents another beneficial advantage over the other DLT FW-RX architectures in terms of circuit complexity.

In the shown hardware implementation, the fully digital filter architecture of detector concept B clearly benefits from using a μC as the FW-RX's smart control processing unit because the MCU comes along with a high-resolution ADC [345]. Although detector concept B requires no additional COTS components besides a simple and cheap resistive divider, it is still evaluated to be of higher complexity than its analog counterpart of detector concept A due to two reasons. First, the effort of implementing an on-chip ADC is assumed higher than the design of an operational amplifier and a Schmitt-Trigger. Second, the corresponding area demand in an ASIC version is expected to be higher for the ADC based filter concept B. Nevertheless, the overall complexity of concept B can be evaluated as reasonably feasible and is hence attributed to a medium level. Amoungst this comparison, detector concept C obviously represents the filter architecture with the highest complexity as it requires an additional DAC circuit beyond using an ADC and an opamp. The implementation effort in an integrated design is hence very high.

In summary, circuit complexity ranges from low for concept A over medium for concept B up to high for concept C. Detector concept A is actually not only suitable but very attractive for an integrated design approach. Also detector concept B represents a reasonable approach for an ASIC solution. Hence, these two concepts – if yielding comparable performance regarding robustness and power consumption – shall be considered for the ASIC implementation as presented in chapter 6.2.

Power Consumption

Evaluation and comparison of power consumption for the different DLT FW detector concepts is fairly difficult. Because it was not possible to measure the overall current consumption of the presented implementation with discrete components, a meaningful statement can only be made based on SPICE simulations for this case [235]. The SPICE simulation based calculation includes the power consumption of voltage dividers, opamps and reference voltages as well as the power drawn from mains for each concept to compute the totally used power. However, the power consumption of the μC is not included in this calculation, which results in a distinct advantage for the digital approaches in this comparison. In reality detector concepts B and C will need some more power for supplying their ADCs, DAC and digital filtering. Taking the entire power consumption of the MCU is yet not fair and would lead to a value, which is by far too high, since a lot of auxiliary processes, such as the decoding procedure

or telegram evaluation, are also conducted on the μC. Aiming to equitably compare all topologies to each other, suitable assumptions are derived for the power consumption of each detector concept with respect to an ASIC implementation based on the concept schematics of Fig. 3.13, Fig. 3.16 and Fig. 3.18. For detector concept A, the main power consumers are the two opamps. Considering a 5 V supply voltage and a current draw of $I_{opamp} = 400\,\mu A$, yields a maximum consumption of about 2 mW for these kinds of amplifiers. Additionally, the resistive divider of the Schmitt-Trigger consumes on average around 0.5 mW according to the implementation shown in Fig. 3.13. The current consumption of the active bandpass filter's reference generation can be neglected since it can be realized at a much lower power consumption in an integrated version. However, an additional safety margin of around 2 mW shall be considered in the calculation. For comparability reasons, this safety margin is applied for each detector concept under evaluation. By this means the stated assumptions for detector concept A rather represent a worst-case approximation, especially when considering that the presented Schmitt-Trigger circuit using the second opamp can be replaced by a simple CMOS implementation with only a few transistors like the ones published in [107], [293], [399]. Detector concept A eventually consumes a power of less 6.5 mW as calculated by equation 3.9,

$$\begin{aligned} P_{Detector,A} &= 2 \cdot P_{Opamp} + P_{Rdiv,Schmitt} + P_{margin}\,, \\ &= 2 \cdot 2\,\mathrm{mW} + 0.5\,\mathrm{mW} + 2\,\mathrm{mW} \;= 6.5\,\mathrm{mW}\,. \end{aligned} \tag{3.9}$$

The main contributors of detector concept B are the big resistive voltage divider connected to mains and the ADC that is needed to digitize the DLT data signal. Considering an ASIC implementation, the resistive divider has been dimensioned to $(R_1 + R_2) = 20\,\mathrm{M\Omega}$ and $R_3 = 270\,\mathrm{k\Omega}$ leading to a power dissipation of approximately 2.6 mW considering a full-scale deflection of 1.8 V at 135 V input voltage. The power consumption of ADC and DAC can be estimated by equation 3.10 under the assumption of a total input capacitance of $C_{ADC,in} = 8\,\mathrm{pF}$, a sampling frequency of $f_s = 100\,\mathrm{kHz}$ and digital supply voltage of $V_{DD,dig} = 1.8\,\mathrm{V}$ to

$$\begin{aligned} P_{ADC} &= f_s \cdot C_{ADC,in} \cdot V_{DD,dig}^2 \\ &= 100\,\mathrm{kHz} \cdot 8\,\mathrm{pF} \cdot (1.8\,\mathrm{V})^2 \approx 2.6\,\mathrm{mW}\,. \end{aligned} \tag{3.10}$$

Table 3.3: Power Consumption of DLT FW detector concepts.

	Concept *A*	**Concept *B***	**Concept *C***
SPICE simulation	37.72 mW	25.73 mW	64.59 mW
ASIC estimation	$\leq$ 6.5 mW	$\leq$ 7.2 mW	$\leq$ 14.5 mW

The total power consumption of detector concept B thereby calculates to

$$P_{Detector,B} = P_{Rdiv,mains} + P_{ADC} + P_{margin}\,, \tag{3.11}$$

$$= 2.6\,\text{mW} + 2.6\,\text{mW} + 2\,\text{mW} = 7.2\,\text{mW}\,.$$

Detector C suffers from its relatively low input impedance of its mains fed input connection. The power directly drawn from mains hence represents its biggest power consumer. Reducing the input current flow by means of an increased impedance, would yield a correspondingly high resistance value for R_5. Thereby, an input impedance of $R_1 + R_2 = 20\,\text{M}\Omega$, as used for the estimation of the fully digital approach, should not be considered for realization in an ASIC solution because this measure might require a prohibitively large chip area. A resistive divider value of $R_1 + R_2 = 10\,\text{M}\Omega$ is used instead. The total power consumption of detector concept C finally computes to

$$P_{Detector,C} = P_{Rdiv,mains} + P_{ADC} + P_{DAC} + P_{Opamp} + P_{margin}\,, \tag{3.12}$$

$$= 5.3\,\text{mW} + 2.6\,\text{mW} + 2.6\,\text{mW} + 2\,\text{mW} + 2\,\text{mW} = 14.5\,\text{mW}\,.$$

Table 3.3 summarizes the calculation of consumed power for both cases, SPICE simulation based computation of the implementation with discrete components and an ASIC estimation. It is clearly noticeable that the SPICE simulated power consumption of all receivers appears relatively high. This is due to several reasons. First, discrete opamps are used, which consume much more current than necessary as they are not optimized for the desired application scenario. The same argument is valid for resistive dividers that have been utilized to generate required bias voltages. Secondly, all detectors operate with a non-optimized control. Since DLT data reception only occurs during the data period, the detectors can at least be partly switched off during DLT operating and supply period. Therefore, a more realistic view on expected power consumption is achieved by the estimations for an ASIC implementation.

Comparing all presented detector concepts in terms of power consumption, the architecture of detector C obviously performs worse in both cases, whereas detector concepts A and B are comparable with a slight advantage for the analog approach of detector A. For a complete evaluation of DLT FW-RX performance, the power consumption of bypass circuits and ZCD also has to be taken into account. As these parts are independent of the chosen detector and decoder concepts, this additional power consumption is expected to yield identical results in all cases and can hence be neglected at this point. The current draw of these auxiliary circuits still needs to be considered for computing overall RX and TX power consumptions of a DLT system in order to comparatively evaluate DLT system performance with respect to other smart home communication systems. Total power consumption calculations and relation to other communication techniques are provided at the end of this chapter in section 3.5, also including the results of sections 3.3 and 3.4 about efficient CDs and a bidirectional DLT communication approach, respectively.

Robustness

The key performance indicator of a communication system is its robustness or reliability. Typically, robustness and reliability of communication systems are tested by determining a BER in (long-term) measurement tests under various application scenarios in different noisy environments or with distinct patterns [41]. Due to the DLT communication structure it is however not possible to determine an exact BER because a single bit flip cannot be detected. If e.g. an error occurs in a single frame, which contains two information bit, it would simply not be possible to distinguish whether one or two bit have been falsely received or if the erroneous frame even was a faulty SoT-frame. As explained in section 3.2.2.4, the developed DLT frame decoder and telegram evaluation routines feature error detections on different levels, particularly on telegram level. Parity bit detection and checking of the expected telegram length or telegram type represent the most important error detection mechanisms. Additionally, an error detection on frame level has been introduced. In case an error occurs at any of these levels, the entire telegram is ignored. Instead of determining a BER it is thereby feasible to measure a so-called telegram error rate (TER) giving a significant indication of a receiver's robustness.

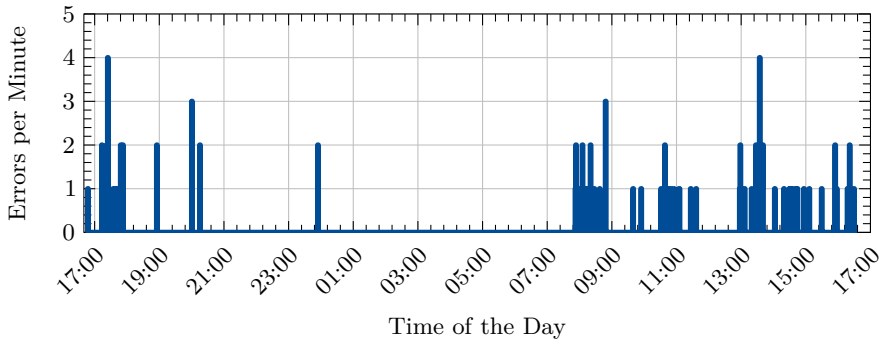
To evaluate the robustness of the three different detector topologies, a 24 h long term measurement has been taken for each concept. During all measurements the entire DLT system, which is built of a CD plus one fully operational CG inlcuding an LED driving stage, has been connected to regular 50 Hz mains in a noisy lab environment. Therefore, the DLT detector concepts were tested

Table 3.4: Evaluation of TERs recorded in 24 h measurements.

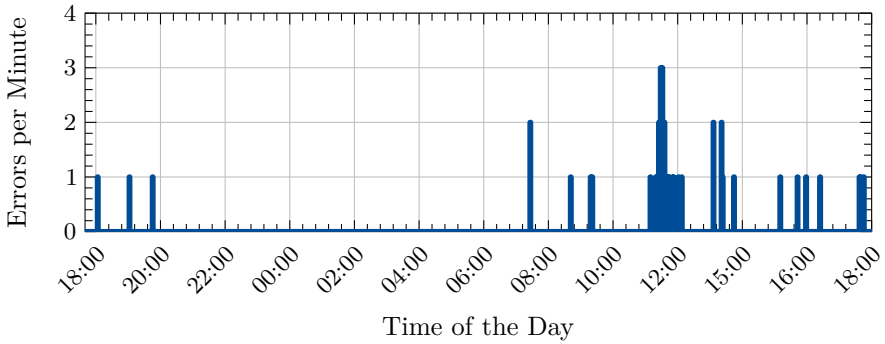
Detector Concepts	**Recorded Telegrams**	**Detected Errors**	**TER in ppm**
Concept *A*:			
Analog Bandpass ($C_2 = 49\,\mathrm{pF}$)	1083037	87	80
Analog Bandpass ($C_2 = 25\,\mathrm{pF}$)	1079471	61	57
Concept *B*:			
Digital Bandpass	1131627	50	44
Concept *C*:			
Mixed-Signal Subtraction Filter	1080507	1556	1440

under real operational conditions and exposed to typical distortions on the European utility grid. The amount of faulty as well as correctly decoded telegrams was recorded for the entire measurement time. In this way, a TER can be calculated for every receiver approach by simply dividing the measured erroneous telegrams by the total number of recorded telegrams. Table 3.4 gives an overview of the amount of recorded and faulty telegrams for all detectors as well as the correspondingly determined error rates.

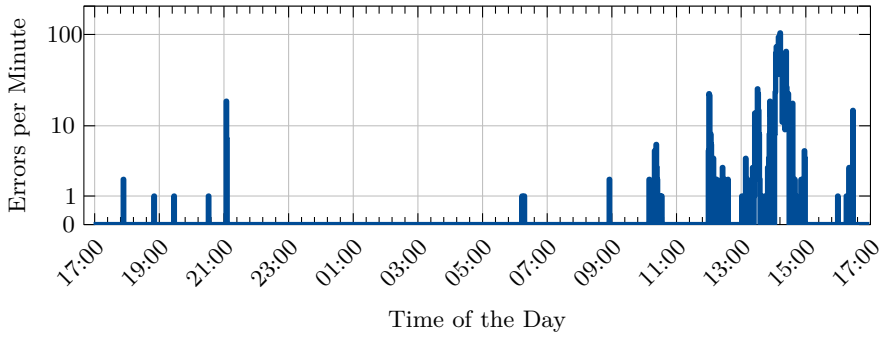
In addition to that, Fig. 3.23 depicts the measured number of errors per minute for all concepts. Considering only brightness telegrams being sent with a telegram length of eight consecutive half-waves, percental error rates per minute can be determined for all DLT FW detectors under evaluation. The peak error rate per minute was below 0.55 % for detectors A and B but almost 15 % for detector C. Furthermore, Fig. 3.23a to Fig. 3.23c indicate the robustness against reaction on environmental disturbances. While all concepts show nearly no erroneous behavior during night times, they reach their highest error rates during the afternoon, when the lab frequently visited for all kinds of works implying many disturbance sources. Still, the error rates for concepts A and B remain relatively low even during these busy times. Due to the used measurement setup it was however not possible to record error rates for all three concepts simultaneously, which might result in slightly different network noise applied to the particular device under test (DUT). In order to maintain at least similar network noise conditions, all concepts have been setup identically in the same laboratory and measured over a 24 h period on consecutive typical workdays. The long lasting measurement time in conjunction with the same laboratory environment thus ensures similar



(a) Recorded telegram errors of DLT FW-RX concept *A*.



(b) Recorded telegram errors of DLT FW-RX concept *B*.



(c) Recorded telegram errors of DLT FW-RX concept *C*.

Figure 3.23: Recorded telegram errors per minute of different DLT FW-RX concepts under evaluation in 24 h longterm measurement.

measurement conditions. In summary, a TER of 44 ppm and 87 ppm has been measured for receivers A and B, respectively, whereas the third detector concept C showed a TER of 1440 ppm. This correlation already clearly indicates that concepts A and B perform significantly better than concept C. In terms of sensitivity and robustness concept B is slightly advantageous compared to DLT FW detector A. All results have again been summarized in table 3.5.

In a second test setup the DLT CD and the receiver topologies under test were connected in series to a synthesized ideal AC voltage with $V_{RMS} = 230\,\text{V}$ and $f_{grid} = 50\,\text{Hz}$. By changing the grid frequency, reactions on grid frequency variations can be observed and deduced. The results are also listed in Table 3.5. Although allowable frequency variations seems quite limited for detector concepts B and C, these approaches could also be used for different utility grids, such as the one in the USA running at 60 Hz, by adapting the digital filtering correspondingly to the respective timings.

Summary and Conclusion of DLT FW-RX Evaluation

Summarizing the results of the conducted performance evaluation, it turns out that detector concepts A and B surpass the third approach of detector C in all tested categories. On the contrary, the performance of topologies A and B are very similar and well comparable in all fields under test. Table 3.5 sums up all relevant results of the performed DLT FW- comparison.

Detector concepts A and B are evaluated to be very well suitable for a monolithically integrated DLT CG solution. Due to their comparable performance, the decision, which implementation to choose, finally depends on the available IC technology and the best suited concept for the desired target application. If the digital detector can e.g. be used for additional functionality, such as zero

Table 3.5: Summary and comparison of proposed DLT-FW detector topologies.

	Detector *A*	**Detector *B***	**Detector *C***
Circuit Complexity	Low	Medium	High
$P_{sim,SPICE}$	37.72 mW	25.73 mW	64.59 mW
$P_{expect,ASIC}$	$\leq$ 6.5 mW	$\leq$ 7.2 mW	$\leq$ 14.5 mW
Measured TER (over 24 h)	57 ppm	44 ppm	1440 ppm
Max. Errors per Minute	4 errors	3 errors	104 errors
TER_{max} per Minute	0.53 %	0.4 %	13.9 %
f_{grid} Input Range	40-60 Hz	49.1-50.4 Hz	49.5-50.4 Hz

crossing detection or generation of the DLT timings for high- and low-current supply phases, the slightly higher power consumption and complexity might be justified. On the other hand, some IC technologies are not well suited for digital designs, e.g. because of lacking a process development kit (PDK) with digital standard cells so that the digital functionally would have to be designed manually in an analog design environment or because of featuring only a large minimum feature size in a given technology node, which would result in large chip area consumption. In these cases an analog detector solution would obviously be preferable. In conclusion, the first two concepts have proven functional with very good performance and robustness and are both suited for highly integrated, intelligent LED drivers. Therefore, the ASIC solution presented in this thesis embodies both detector concepts as laid out in chapter 6.

3.3 Efficient Power Supplies for an Increased System Intelligence of DLT Control Devices

Providing modern features of intelligent lighting control DLT typically operates as a stand-alone system in domestic homes and small offices. To increase overall system intelligence, it is favorable to integrate it as a subsystem into a smart home environment with an intelligent backbone infrastructure [241]. This measure enables interoperability with existing control systems and enhances DLT system intelligence by offering additional smart features, such as automated light adaption or remote control, and thereby improves living comfort.

An integration into other home automation systems can easily be achieved by providing a wireless uplink [238], [241], e.g. WiFi [165], [176], [414] or Bluetooth [78], [294], because mobile phones and tablet PCs may then be used as remote controls [10]. Also ZigBee represents a suitable communication technology for smart home applications as outlined in section 2.1. Employing wire-bound interfaces like LAN, DALI or KNX would not be reasonable in this setup as outlined in section 2.1.2 because they require additional wiring effort, which involves extensive construction measures, particularly in old housings.

In a common setup, the CD operates as the controlling *"master node"* of the DLT system and transmits provided user inputs, like brightness, color or color temperature adjustments, to attached CGs. Aiming to embed DLT into a smart home infrastructure, the main CD thus needs to be equipped with a suitable communication interface, e.g. a WLAN module, a Bluetooth transceiver (TRX) or a ZigBee communication IC. A detailed characterization and implementation of a DLT CD with extended functionality as used during the investigations of this thesis has been published by Lohaus *et al.* [240]. Appendix section A.3

provides additional material on relevant circuit schematics of this CD regarding DLT data modulation (Fig. A.8), power supply concept (Fig. A.9) and start-up supply (Fig. A.10). Additionally, Fig. 3.39 and Fig. 3.43 in section 3.4 give an insight into the developed CD's system concept and bypass structure with overcurrent protection circuitry. Since a DLT CD represents a fixed, wall-mounted console replacing conventional light switches or dimmers, it requires in addition to a (wireless) communication interface a suitable user interface (UI), such as an liquid crystal display (LCD) or touchscreen.

Especially LCD backlights and WLAN links can be very power hungry and may require up to several hundred milliwatts [354], [355], [357]. Even low power ZigBee frontends may consume an additional power of about 50 mW to 160 mW depending on the data transfer [347], [375]. This circumstance is in fact troublesome for a DLT CD because the conventional two-wire connection between dimmer and luminaire implies the nonavailability of a neutral wire at the light switch lead-out, especially in old houses. Therefore, existing AC-DC converter solutions [70], [127], [404], [430] that supply peripheral devices from mains with a constant DC output voltage of e.g. $V_{out,DC} = 3.3\,\mathrm{V}$ are unfortunately not applicable as they cannot be operated without a neutral wire at the light switch lead-out. A well-suited method overcoming the explained power supply issue is to make use of a current carrying bypass structure in attached luminaires, as proposed by the DLT approach. However, the DLT standard [106] specifies strict boundary conditions and power supply limitations as pointed out in section 3.1.1. The corresponding power supply hence needs to handle highly discontinuous input voltage conditions while providing high output power at a constant DC output voltage. Section 3.3.1 therefore describes associated limits and calculations as well as preliminary investigations in more detail as an initial starting point. Further information on DLT power supply limitations and theoretical calculations are provided in [106], [331].

Aiming to extend DLT system intelligence by providing a wireless link connection this chapter presents two different power supply topologies for DLT CDs that cope with the described issue and boundary conditions while maintaining the official DLT specification [106]. The proposed power supplies are designed to deliver sufficient energy powering a WiFi module and an LCD simultaneously in addition to the required control device circuitry. Because the power consumption of a WiFi link is much higher than that of a Bluetooth or ZigBee one, the same power supply units can also be used for those communication methods without change. Both supply concepts are fundamentally introduced in papers [238] and [241]. Several experimental investigations are additionally conducted in [331], which also describes a functional reference design of a suitable power supply concept that has been developed within this thesis.

3.3.1 Power Budget, Supply Limitations and Efficiency Targets in DLT Control Devices

As pointed out in section 3.1.1, a DLT CD may only power itself in a well-defined, 400 µs lasting HC supply interval shortly after every zero crossing of mains voltage with a maximum current draw of $I_{in,max} = 350\,\text{mA}$. Consequently, the available amount of energy per mains half-wave is very limited [241]. Based on initial considerations stated in [238], [241], this section summarizes effective supply limits and derives specific efficiency requirements to develop a DLT compliant power supply for CDs with a wireless link connection. Following the boundary conditions indicated in Fig. 3.3 and section 3.1.1, the maximum available energy per mains half-wave can theoretically be calculated for a best and a worst case scenario according to an associated voltage drop over a CG's current carrying bypass structure [238]. Considering the ideal case without any voltage drop over an attached CG, equation 3.13 computes the maximum available energy to

$$W_{CD,avail,max} = \int_{t_1}^{t_2} \hat{V}_{grid} \cdot \sin(2\pi \cdot f_{grid} \cdot t) \cdot I_{CD,max}\, dt \tag{3.13}$$

$$= \int_{300\,\mu\text{s}}^{700\,\mu\text{s}} \sqrt{2} \cdot 230\,\text{V} \cdot \sin(2\pi \cdot 50\,\text{Hz} \cdot t) \cdot 350\,\text{mA}\, dt = 7.12\,\text{mJ}\,.$$

Assuming a maximum possible voltage drop of $V_{drop,max} = 20\,\text{V}$ across a CG's bypass circuitry, equation 3.14 denotes the minimum available energy per mains half-wave in the same manner to

$$W_{CD,min} = \int_{t_1}^{t_2} (\hat{V}_{grid} \cdot \sin(2\pi \cdot f_{grid} \cdot t) - V_{drop}) \cdot I_{CD,max}\, dt = 4.32\,\text{mJ}. \tag{3.14}$$

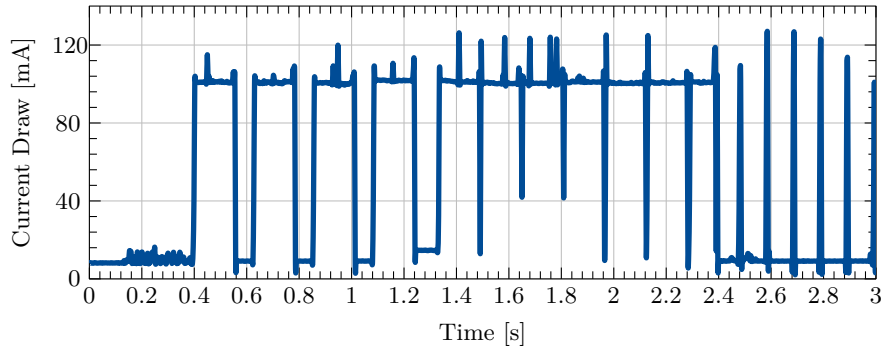
Since these computations indicate the available energy for one 10 ms long half-wave of mains, the calculated energy levels correspond to average output powers of $P_{CD,max} = 712\,\text{mW}$ and $P_{CD,min} = 432\,\text{mW}$, respectively [238]. Checking whether this amount of available average power is sufficient for supplying a DLT CD during the desired, power-hungry application scenario, it is necessary to pre-estimate the power consumption of a common WiFi-module and additional periphery, such as an LCD. Additionally, the conversion efficiency of an appropriate power supply circuit needs to be taken into account.

In a first step the way of operating the employed WiFi module [357] hence needs to defined and set, as it impacts the required power consumption significantly. Keeping the power consumption within manageable limits, it is therefore suggested to apply the concept of beaconing [248] and use the so-called power-save mode of the employed WiFi module [357]. In this mode of operation the WiFi frontend only wakes up, when a new beacon package is delivered by the hosting access point, which happens typically every 100 ms [238], [248], [357]. Once woken up, the WiFi module checks for incoming requests and data transfer during a comparatively short active time $t_{beacon,active}$ of about 10 ms to 15 ms. In comparison to an always-on mode, the power consumption in the power-save mode is hence reduced drastically as equation 3.15 indicates,

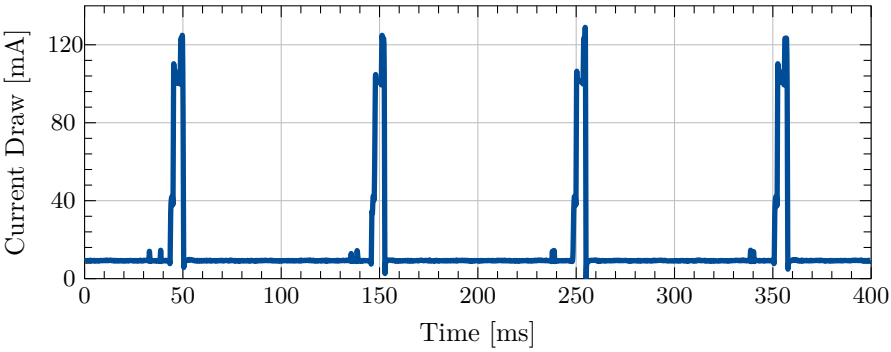
$$\begin{aligned} P_{WLAN,beacon} &= \frac{t_{beacon,active}}{T_{beaconing}} \cdot P_{WLAN,active} + \frac{t_{beacon,sleep}}{T_{beaconing}} \cdot P_{WLAN,sleep} \quad (3.15) \\ &= \frac{15\,\text{ms}}{100\,\text{ms}} \cdot P_{WLAN,active} + \frac{85\,\text{ms}}{100\,\text{ms}} \cdot P_{WLAN,sleep} \\ &= 0.15 \cdot P_{WLAN,active} + 0.85 \cdot P_{WLAN,sleep}\,. \end{aligned}$$

It is expected that communication events, which relate to lighting control, such as dimming, turning the light on and off or color adjustments, occur only rarely compared to the operating hours. Using this power-safe mode during continuous operation hence enables an enormous reduction of power consumption as the WiFi module is inactive most of the time. Furthermore, the overall system benefits from the low data volume that is needed for communication purposes of control commands in a typical interior lighting environment. This results in comparatively short active cycles of the employed communication device. In case of data transfer, the used WiFi module only requires transmit and receive times of $t_{WLAN,TRX,on} \approx 100\,\text{ms}$ for this kind of low data volume.

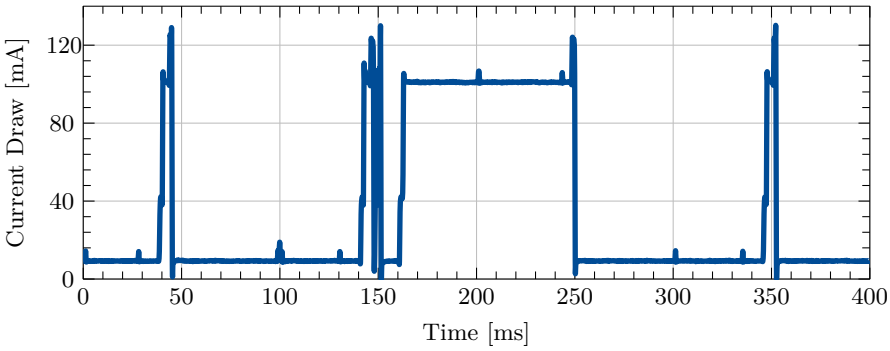
In order to pre-estimate the application related power consumption, the selected WiFi module [357] has been operated in its most relevant modes of operation. In addition to data transfer and power-save mode it also has to been accounted for the so-called association phase, when a connection to a WLAN is established through an access point or router. Typically, this association phase however happens only once after power-up [238]. For all three cases the actual current consumption has been measured while a constant DC supply voltage of $V_{supply} = 3.3\,\text{V}$ has been applied. These preliminary measurements have already been published in [238]. Fig. 3.24 reillustrates the recorded current consumption profiles for association phase, data transfer and power-save mode in its corresponding subplots, Fig. 3.24a to Fig. 3.24c, respectively.



(a) Current draw of the WiFi module during association phase.



(b) Current draw of the WiFi module during power-save mode.



(c) Current draw of the WiFi module during data transfer.

Figure 3.24: Current draw measurement of a WiFi module for different operation modes at a constant supply of $V_{DD} = 3.3\,\mathrm{V}$ [238].

Calculating the power demand from these measurements for data transfer and power-safe mode yields equations 3.16 to 3.19. In case of data transfer, it has been assumed that an active period occurs every $T_{COM,request} = 200\,\text{ms}$, which is a rather worst case approximation. Furthermore, an average current draw of $I_{WLAN,max} \approx 120\,\text{mA}$ is assumed to flow during the active phases in each mode, which is also worse than actually measured.

$$P_{WLAN,TRX} = \frac{t_{WLAN,TRX,on}}{T_{COM,request}} \cdot P_{active} \tag{3.16}$$

$$= \frac{t_{WLAN,TRX,on}}{T_{COM,request}} \cdot V_{supply} \cdot I_{WLAN,max} \tag{3.17}$$

$$= \frac{100\,\text{ms}}{200\,\text{ms}} \cdot 3.3\,\text{V} \cdot 120\,\text{mA} = 198\,\text{mW}\,,$$

$$P_{WLAN,beacon} = 0.15 \cdot P_{WLAN,active} + 0.85 \cdot P_{WLAN,sleep} \tag{3.18}$$

$$= 0.15 \cdot V_{supply} \cdot I_{WLAN,max} + 0.85 \cdot V_{supply} \cdot I_{WLAN,sleep} \tag{3.19}$$

$$= 0.15 \cdot 3.3\,\text{V} \cdot 120\,\text{mA} + 0.85 \cdot 3.3\,\text{V} \cdot 8\,\text{mA} = 81.8\,\text{mW}\,.$$

Still, due to the relatively short active phases in both modes (TRX and beaconing), the additional power demand is much smaller than the minimum available average power of $P_{CD,min} = 432\,\text{mW}$ in case of a 20 V voltage drop over connected CGs. Accounting for a conversion efficiency of approximately 65 %, which is ambitious to achieve due to the highly discontinuous input conditions but yet a quite realistic goal, the additional power demand lies within an acceptable range that can be provided by an appropriate supply circuitry. Hence, these computations clearly indicate that it is feasible to realize WLAN access and operation for a DLT CD.

Although general operation of a WiFi module in a DLT CD appears feasible when using the power-save mode, the CD's power supply circuit also needs to cope with higher power demands during association phase. Obviously, the association phase represents the worst case scenario in terms of power consumption, since a high average current flows for a relatively long time period $t_{WLAN,assoc,on}$ of about 2 s to 3 s. Investigating the current consumption measurements depicted in Fig. 3.24 in more detail, it is yet found that the WiFi module never exceeds an average current draw of about 110 mA in all cases [238]. To perform a worst case approximation a continuous current

draw of $I_{WLAN,assoc} = 110\,\text{mA}$ is hence assumed to flow during association phase. Considering a supply voltage of $V_{DD} = 3.3\,\text{V}$, equation 3.20 consequently computes the maximum power required to operate a common WiFi module to

$$P_{WLAN,max} = V_{DD} \cdot I_{WLAN,assoc} = 3.3\,\text{V} \cdot 110\,\text{mA} = 363\,\text{mW}\,. \quad (3.20)$$

Accounting for an additional current consumption of $I_{periphery} \approx 10\,\text{mA}$, which is used for supplying the DLT CD itself including other employed components, such as a main μC and an LCD, equation 3.21 determines the associated extra power budget to

$$P_{CD,periphery} = V_{out} \cdot I_{periphery} = 3.3\,\text{V} \cdot 10\,\text{mA} = 33\,\text{mW}\,. \quad (3.21)$$

In compliance with the published paper [238] the CD's power supply circuit needs to feature a high power supply efficiency to provide enough energy for a continuous current flow of the assumed worst case amount of $I_{WLAN,assoc} = 110\,\text{mA}$, particularly in case of a 20 V reduced mains input voltage. Equation 3.22 reckons this efficiency requirement accordingly to

$$\eta_{CD,supply,WC} = \frac{P_{WLAN,max} + P_{CD,periphery}}{P_{CD,min}} = 91.7\,\%\,. \quad (3.22)$$

Accounting on the contrary for the maximum available input energy in this application scenario, this efficiency requirement relaxes to

$$\eta_{CD,supply,BC} = \frac{P_{WLAN,max} + P_{CD,periphery}}{P_{CD,max}} = 55.6\,\%\,, \quad (3.23)$$

which is rather realistic to achieve. These simple calculations already show how strongly the effective efficiency requirement depends on applied boundary conditions. Hence, poorly designed lighting sources resulting in a voltage drop on the supplying AC mains voltage of up to 20 V are yet not only disadvantageous in terms of power consumption, but indeed pose a critical threat to the power supply of a DLT CD providing WLAN access, at least in regard to the power hungry association phase. Since the association phase typically happens only once after power-up [238], the CD's power supply circuit could provide the high energy demand during association – in case these precarious boundary condition actually occur – by an extra power source, e.g. from a big storage capacitor that has been precharged before enabling the WiFi module. Even in this worst case scenario it will therefore be possible to enable WLAN operation in conjunction with DLT, if a proper power supply concept for CDs can be designed.

Although the described absolute worst case scenario may theoretically occur, a 20 V voltage drop over an attached CG is neither desirable nor very realistic,

particularly if the entire lighting system in a household has been trimmed for high efficiency. Reconsidering the DLT CG design described in chapter 3.2.1, it is indeed possible to design efficient luminaires at reasonable cost that feature a voltage drop well below $V_{CG,drop} \leq 5\,\mathrm{V}$. In this case the efficiency requirement relaxes sufficiently to make an implementation of a DLT compatible power supply feasible enabling WLAN access and providing enough energy even during the association phase. Assuming $V_{drop} = 5\,\mathrm{V}$, equation 3.14 yields an available energy of $W_{CD,5Vdrop} = 6.42\,\mathrm{mJ}$ during the HC supply interval, which corresponds to an available average power of $P_{CD,5Vdrop} = 642\,\mathrm{mW}$. The efficiency requirement calculates accordingly to

$$\eta_{CD,supply,5Vdrop} = \frac{P_{WLAN,max} + P_{CD,periphery}}{P_{CD,5Vdrop}} = 61.7\,\%\,. \tag{3.24}$$

In summary, it is theoretically feasible to develop an efficient power supply for DLT CDs that is capable of providing a WLAN uplink even under worst case assumptions. Considering the described measures, such as operating the employed WiFi module in a power-save mode or using well designed DLT CGs connected in series to the CD, relax the worst case boundary conditions to a more realistic application scenario. The power supply topologies presented in the subsequent sections therefore rather aim to exploit the maximum possible energy yield out of the limited DLT supply period [238] in order to survive also the power-hungry association phase under realistic operating conditions.

3.3.2 Preliminary Investigations and Conceptual Idea of a Dual-Stage Power Supply Topology for DLT CDs

Searching for a simple, low complexity solution, a conventional single-stage power converter, as depicted in Fig. 3.25, appears suitable for realizing a DLT CD's power supply circuitry at first glance. While this topology might in general provide a sufficiently high conversion efficiency even for the presented worst case approximation, it additionally features low hardware effort. However, this straightforward approach implicates severe problems for a practical implementation in the desired application scenario [238]. Between two successive DLT supply periods the output capacitor C_{out} represents the only energy source for the entire load consisting of WiFi module, μC, LCD and other CD periphery because no input voltage from mains is applied in that time. Keeping the output voltage ripple within reasonable limits, C_{out} reaches very big values as shown in the following. Accounting for the WLAN association current draw from equation 3.20, a constant load current of $I_{load} = 110\,\mathrm{mA}$ is assumed. Allowing for a

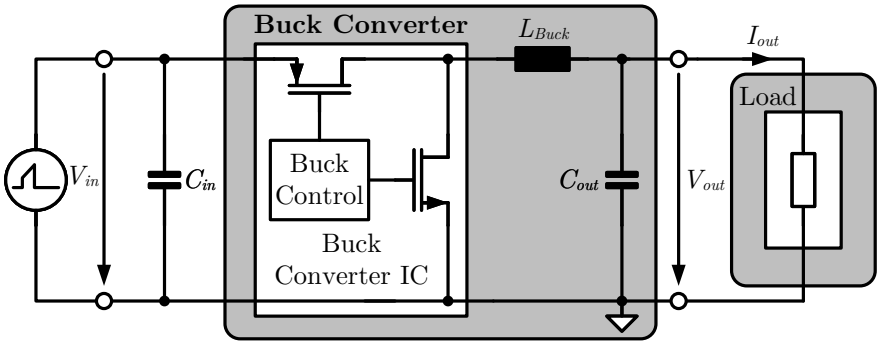


Figure 3.25: Conceptual topology of a conventional single-stage buck converter suited for powering a DLT CD in the described target application.

maximum variance on the provided output voltage of about $\Delta V_{out,max} = \pm 10\,\%$ at $V_{out} = 3.3\,\mathrm{V}$ yields a capacitance value of about

$$C_{out} = \frac{I_{load} \cdot \Delta t}{\Delta V_{out}} = \frac{110\,\mathrm{mA} \cdot (10\,\mathrm{ms} - 0.4\,\mathrm{ms})}{2 \cdot 330\,\mathrm{mV}} \approx 1.6\,\mathrm{mF}\,. \tag{3.25}$$

Although it might technically be feasible to employ such a huge capacitor, it is rather impractical due to area and lifetime reasons. Instead of using small ceramic capacitors, a single-stage concept would require to utilize a large e-cap resulting in larger footprint, slower start-up behavior and reduced lifetime [241]. Furthermore, Sturm [331] thoroughly analyzes with additional computations and experiments that using a single stage buck converter topology is not suitable for the targeted application. Due to the mentioned reasons a single-stage topology shall not be used. Instead, this thesis shows two practical solutions for DLT CDs based on a dual-stage power supply concept as illustrated in Fig. 3.26. Both implementations have been presented in [238] and [241].

The developed two-stage power supply architecture consists of four main functional blocks, which are an enable switch, a current limiter, the 1st and the 2nd converter stage. Enable switch and current limiter are required for conforming to the specified DLT characteristics of a maximum input current $I_{in,max} = 350\,\mathrm{mA}$ during a supply time of $t_{supply} = 400\,\mu\mathrm{s}$ starting shortly after the zero crossing of mains. The enable switch also protects the circuitry downstream of it from any occurring over-voltage, particularly outside of the DLT supply interval. Converter stages one and two can be built of conventional DC-DC converters since the input voltage from mains increases nearly linearly

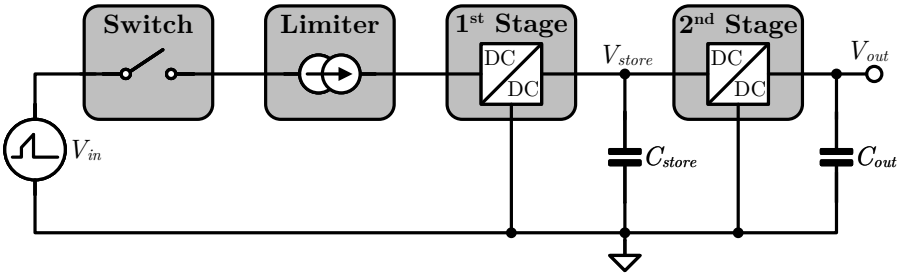


Figure 3.26: Conceptual topology of a dual-stage power supply circuit suited for high power demands in DLT compliant CDs.

during the HC supply interval and stays in the end below approximately 70 V. The first converter stage is only active during the 400 µs lasting supply interval trying to bring as much charge as possible onto a storage capacitor C_{store} by optimally exploiting defined DLT limits. The second stage operates continuously from a nearly constant DC voltage V_{store} resulting from the gained charge stored on C_{store}. The general idea of using this two-stage power supply concept is to decouple the highly discontinuous charging procedure of C_{store} from the continuous power supply of the CD and its components.

Furthermore, the dual-stage power supply concept features another degree of freedom, which leaves room for improvement, namely optimizing the aim of conflict between selected intermediate voltage level V_{store}, the actual size of the chosen storage capacitor C_{store} and the achievable efficiency of the second power converter stage. Investigating equation 3.26,

$$W_{store} = \frac{1}{2} \cdot C_{store} \cdot V_{store}^2 \,, \tag{3.26}$$

it appears that the amount of stored energy depends quadratically on the storage voltage, whereas it only shows a linear relationship regarding the capacitive influence [238], [241], [331]. Hence, using an increased intermediate storage voltage, e.g. of about one decade higher than the planned output voltage, allows for employing much smaller capacitors while keeping the conversion efficiency of the second stage within reasonable limits. Still, the storage voltage V_{store} should not be selected too high, as it impairs not only efficiency but also limits available COTS controller ICs and high voltage capacitors on hand at an acceptable price range [238].

While it is impractical to achieve the high conversion efficiency calculated in equation 3.22 with a dual-stage approach, the additional optimization opportunity of trading capacitor size for storage voltage level allows for balancing two important things regarding the described application scenario. First, the CD's power supply can be designed for delivering maximum continuous output power. Using this design criterion aims to provide enough energy to the power supply's load in order to survive the power hungry WLAN association phase under the assumed realistic operating conditions stated in section 3.3.1 and summarized in equation 3.24. Secondly, storage voltage V_{store} and capacitor C_{store} can be selected by this means within reasonable limits while buffering enough energy for surviving association phase in case of absolutely worst case conditions. Thereby, this concept accounts for all kinds of application scenarios and boundary conditions while using only ceramic storage capacitors. This approach is hence expected to yield a functional WLAN equipped DLT CD with reasonable hardware effort.

3.3.3 Power Supply Concept A: Dual-Stage Topology using Flyback- & Buck-Converter

The first dual-stage power supply concept that is proposed to fit demanded application needs consists of a flyback converter as the first power stage and a buck converter forming the second converter stage. In fact, this implementation can be considered an extension to the simple single-stage topology of Fig. 3.25 mentioned in section 3.3.2 by applying the idea of a two-stage approach [241]. Fig. 3.27 presents the corresponding circuit schematic implemented in this work.

As mentioned earlier in section 3.3.2, enable switch and current limiter are required for DLT compliance reasons. When the protection switch is activated by the main μC during the supply interval, the available input energy is stored in capacitor C_{in}. Since the inrush current into this capacitor is only limited by the upstream connected current regulator, it is possible to draw the maximum allowable current nearly without ripple during the entire supply interval. From this fact it also becomes clear that the requirement for a current limiter is inevitable as there are no other means to limit inrush current into capacitor C_{in} to a maximum of $I_{in,max} = 350\,\text{mA}$. Despite of reaching nearly maximum input current, it is not possible to conclude, whether also maximum input energy is harvested in this case, because the voltage drop over the limiter is yet unknown. Taking this as a design criterion, it might however be possible to boost the available output energy for a known load in a certain operating point.

During the supply interval the input voltage rises approximately linearly from around 30 V to 70 V [106], [238], [241]. To achieve an optimum energy yield,

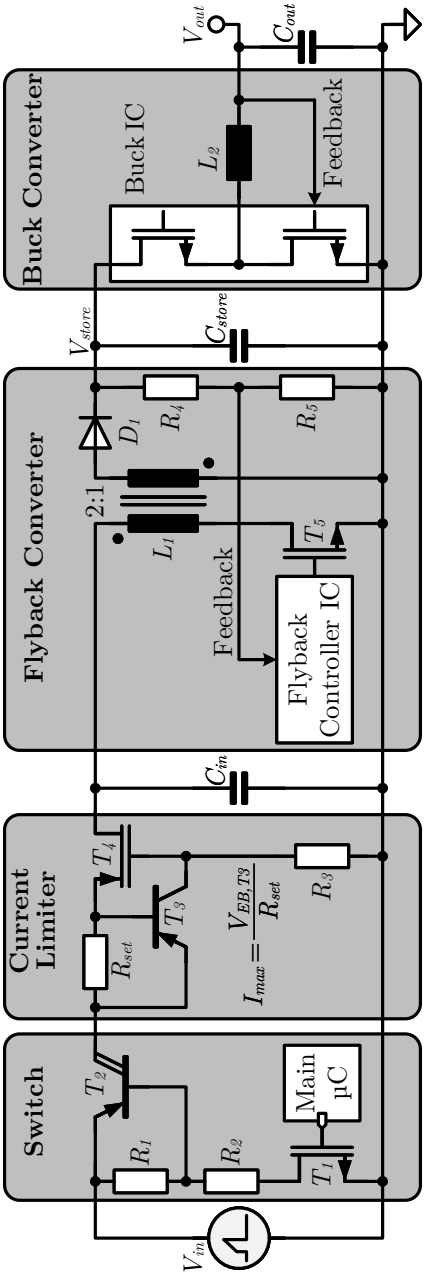


Figure 3.27: Schematic of implemented dual-stage supply concept *A* for powering WLAN-equipped DLT CDs.

the voltage over C_{in} has to follow mains voltage as closely as possible avoiding a voltage drop over the current limiter. Hence, the flyback converter has to ensure that the voltage across C_{in} never drops below 30 V, which is realized by turning the controller IC off using its *'RUN'* pin [241], [363]. The linear rise condition of V_{in} thus determines dimensioning of C_{in},

$$C_{in} = \frac{I_{in,max} \cdot t_{supply}}{V_{in}(t_2) - V_{in}(t_1)} = \frac{350\,\text{mA} \cdot 400\,\mu\text{s}}{70.96\,\text{V} - 30.6\,\text{V}} \approx 3.5\,\mu\text{F}\,, \tag{3.27}$$

$$\text{with:} \quad t_2 = t_1 + t_{supply} = 300\,\mu\text{s} + 400\,\mu\text{s} = 700\,\mu\text{s}\,.$$

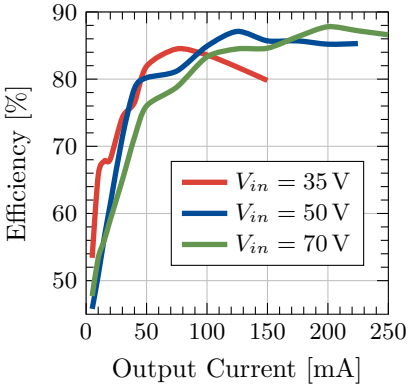
Operating in a highly discontinuous manner the flyback converter is only active during the DLT supply interval. As the first converter stage it charges storage capacitor C_{store} to an intermediate voltage V_{store} in this time. As explained in section 3.3.2, storage capacitor C_{store} accordingly buffers the energy taken from the utility grid between supply intervals and thereby ensures continuous operation of the second stage, which is the buck converter in this case. This measure not only reduces the required output capacitance C_{out} of the second converter stage substantially, but furthermore also enables both converters to operate in the voltage domains they are optimized for [241]. The challenging constraints coming from the huge input to output voltage ratio is thus reduced for both converters increasing overall efficiency. The capacitance of C_{store} and the chosen intermediate voltage $V_{store,max}$ determine the amount of energy that can be stored applying equation 3.26 as follows,

$$W_{C_{store}}(t) = \frac{1}{2} \cdot C_{store} \cdot (V_{store}(t))^2 + W_{C_{store}}(t_0) \tag{3.28}$$

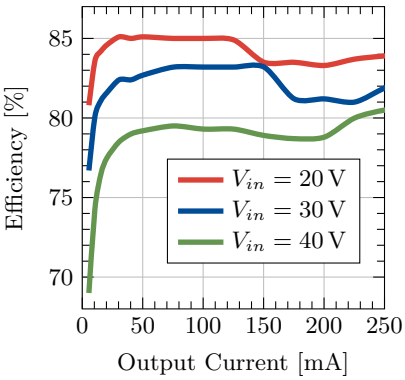
$$\Rightarrow W_{C_{store},max} = \frac{1}{2} \cdot C_{store} \cdot (V_{store,max})^2 \tag{3.29}$$

$$= \frac{1}{2} \cdot 50\,\mu\text{F} \cdot (40\,\text{V})^2 = 40\,\text{mJ}\,.$$

Aiming to optimize the trade-off between capacitor size of C_{store}, intermediate storage voltage V_{store} and achieved converter efficiency η_A, this implementation exploits the quadratic voltage dependency of the stored energy and thereby selects an intermediate voltage of $V_{store,max} = 40\,\text{V}$. In this way storage capacitance C_{store} is kept small, which enables the use of ceramic capacitors and hence reduces footprint area [241]. In the presented implementation C_{store} has been set to 50 µF for good robustness. If a few supply intervals are missing

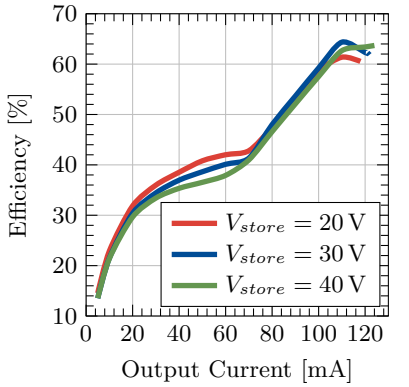


(a) Efficiency of the flyback converter at $V_{out,flyback} = 40\,\mathrm{V}$.

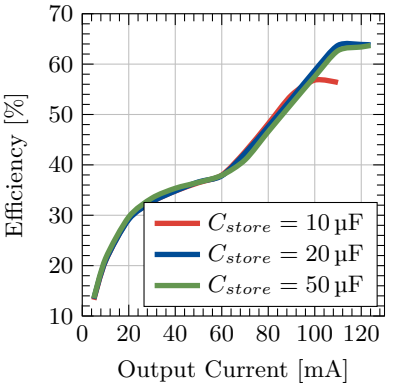


(b) Efficiency of the buck converter at $V_{out,buck} = 3.3\,\mathrm{V}$.

Figure 3.28: Efficiencies of 1st and 2nd converter stage in supply concept A.



(a) Efficiency of concept A with $C_{store} = 50\,\mu\mathrm{F}$ and sweeping V_{store}.



(b) Efficiency of concept A with $V_{store} = 40\,\mathrm{V}$ and sweeping C_{store}.

Figure 3.29: Measured overall efficiency of supply concept A at $V_{out} = 3.3\,\mathrm{V}$.

due to utility grid fluctuations, which is likely to happen, or if high peak currents are drawn by the second stage, the storage capacitor contains enough energy to

Table 3.6: Selected component values for power supply concept A.

Component	C_{in}	C_{store}	C_{out}	L_1	L_2	
Value	8 µF	50 µF	47 µF	350 µH	68 µH	
Resistor	R_1	R_2	R_3	R_4	R_5	R_{set}
Value	8.2 kΩ	68 kΩ	10 kΩ	390 kΩ	8 kΩ	2 Ω

continuously power the load. Furthermore, the voltage level of $V_{store} = 40\,\mathrm{V}$ remains in a voltage class that may safely be touched [158] assuming the flyback converter provides galvanic isolation from mains [241]. Table 3.6 depicts the selected component values, which have been used in the implementation referring to schematics of Fig. 3.27. It should be noted that only ceramic capacitors were used. The value of C_{in} was experimentally determined for highest possible output power, starting with a value of 3.5 µF from equation 3.27.

Fig. 3.28a and Fig. 3.28b show the achieved efficiencies for different supply voltages and load currents applied to the converter stages. Both converters ([362], [363]) have been measured with constant DC input voltages [241]. The output voltages have been regulated to constant DC levels of $V_{out,flyback} = 40\,\mathrm{V}$ and $V_{out,buck} = 3.3\,\mathrm{V}$ for flyback and buck converter, respectively, while output current draw of the attached current sink is swept from 5 mA to 250 mA. The flyback converter is designed for maximum output power since its efficiency is highest for high output currents. The buck converter efficiency decreases as expected with a rising input to output voltage ratio. Thus, further optimization could potentially be achieved, if a better intermediate voltage level V_{store} can be found. However, this optimization has to be performed under the boundary condition of using ceramic capacitors. Lowering V_{store} leads to an increased capacitance value for C_{store}, which limits the number of available ceramic capacitors. The chosen values of $C_{store} = 50\,\mu\mathrm{F}$ and $V_{store} = 40\,\mathrm{V}$ have been determined in various experimental tests aiming for delivering maximum possible output power. Also, different controller ICs for flyback and buck converter as well as diverse transmission ratios of the used transformer have been installed and investigated. Fig. 3.29a and Fig. 3.29b show the result of the conducted optimization procedure by measuring the overall efficiency of power supply concept A for different storage voltages V_{store} and capacitors C_{store}. Although the selected values for intermediate voltage and buffer capacitance have been determined through various experiments and by extensive testing, they might still not represent the optimal voltage level and capacitor size, respectively, which would be interesting to further investigate in future work [241].

3.3.4 Power Supply Concept B: Dual-Stage Topology using Boost- & Flyback-Converter

A different implementation to realize the dual-stage power supply concept for WLAN enabling DLT CDs uses a boost- and a flyback converter for first and second stage, respectively. This topology implementation has been presented in detail in [238]. Again, protection switch and current limiter are installed upstream of the two power converters for the same DLT compliance reasons mentioned earlier. The enable switch protects the circuit from input voltages above 100 V, which can occur outside of the HC supply phase. The current limiter is required to limit the inrush current during the initial charging of C_{store} after power-on because the boost converter topology has no means of controlling the input current in this case. This ensures that the DLT specifications are maintained as no current higher than $I_{CD,max}$ can be drawn and that only during $t_{supply} = 400\,\mu s$ within the HC supply interval. An identical implementation for these two blocks as presented in section 3.3.3 can be realized here as well. Fig. 3.30 presents the corresponding circuit schematic.

Similar to concept A presented in section 3.3.3, concept B also requires to draw the maximum possible current and follow mains voltage as closely as possible in order to achieve the maximum possible energy yield out of the limited DLT supply period, which has been calculated in equations 3.13 and 3.14 for best and worst case operating conditions, respectively. However, a voltage jump at the input of the power supply must not result in excessive input current. A boost converter has thus been chosen as the first stage of the power supply for the two following reasons. First, the voltage across the inductance L_1 may rise abruptly at the turn-on time t_1 while the input current ramps up from zero. Second, the inductor L_1 ensures a continuous input current flow, which is regulated by the boost converter's control circuitry. Both features ensure the following of mains voltage and a continuous current draw close to the specified DLT limit at the same time. Therefore, an optimum energy yield can be achieved depending on both the dimensioning of L_1 and the converter efficiency.

Boosting the input voltage to a higher level enables storing of large energy portions using relatively small (ceramic) capacitors. Due to the higher storage voltage the storage capacitor can be even much smaller in contrast to the implementation of concept A. This is because concept B exploits the quadratic voltage dependency of the stored energy in C_{store} even further recalling equations 3.26 and 3.28. However, the storage voltage cannot be selected too high since it impairs the efficiency of the second stage and limits the number of COTS controller ICs. Therefore, C_{store} must be dimensioned accordingly. If several half-waves of mains voltage are missing, the capacitor has to supply the

Figure 3.30: Schematic of implemented dual-stage supply concept B for powering WLAN-equipped DLT CDs.

second stage with energy without being recharged. To determine a reasonable value for the capacitance of C_{store} a trade-off between physical size and start-up time on the one hand and available energy during blackouts on the other hand has to be considered. In the current approach, the storage capacitance is chosen to equal $C_{store} = 5\,\mu\text{F}$ and V_{store} is limited to $V_{store,max} = 91.7\,\text{V}$.

For the second stage a commercially available flyback converter IC that can handle input voltages of up to 100 V is used [361]. This IC is optimized for applications with load currents around some hundreds of mA. In the presented implementation, the converter regulates its output to the desired 3.3 V employing a transformer L_2 with a primary inductance of $L_2 = 300\,\mu\text{H}$ and a (4:1) turns ratio. Generally, the flyback converter offers the opportunity to provide galvanic isolation, if needed. This is a good feature for a later commercialization. However, in the realized implementation no galvanic isolation is utilized for simplicity. Since the flyback converter already has a diode on the output, no additional measures are required to prevent current from flowing into the disabled converter's output during start-up.

In the presented implementation two μCs are used. One is the main μC for the entire DLT CD, which takes care of precise timing and controls the enable switch, just like the one used for concept *A*. The second μC is part of the boost converter's control circuitry providing the PWM frequency as well as taking care of the overvoltage protection in the boost converter stage. It is inevitable to use two dedicated μCs since both tasks are timing critical. It should be noted that a small start-up circuit is necessary to start the operation of these μCs. In consequence, the enable switch remains disabled during this start-up phase. After the start-up has finished, the power supply, which has been fully realized with COTS components, can supply itself.

The purpose-designed boost converter control circuitry is depicted in Fig. 3.31. It allows for switching frequencies of up to 1 MHz, while an inductor size of $L_1 = 1\,\text{mH}$ has been chosen for the presented implementation. The converter control uses a very simple PWM control methodology implemented with a discrete flip-flop. The input current is measured with a sense resistor R_{sense} and whenever it reaches the limit of $I_{CD,max} = 350\,\text{mA}$, the flip-flop turns transistor T_5 off. It should be noted that the value of R_{sense} has to be selected very carefully. If the current limit of the boost converter stage is higher than the activation level of the current limiter, which is determined by means of R_{set}, a large voltage drop across the limiter will occur resulting in massive losses and severely impacting the available output power. In this case, the transistor T_5 would continuously be conducting because the current sense level V_{sense} never reaches its limit $V_{I_{max}}$ and no more energy is transferred onto C_{store}. Hence, when selecting the values of R_{sense} and R_{set}, component tolerances have to

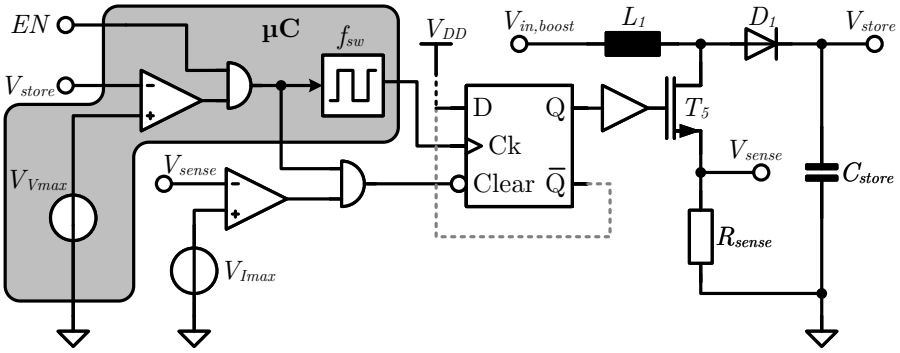


Figure 3.31: Schematics of the boost converter's control circuit.

be considered in order to account for a certain security margin. To avoid this deadlock situation, the circuit can be modified to limit the MOSFET's on-time as illustrated in Fig. 3.31. This is done by connecting the flip-flop's *'D'* input to its inverted output (gray dashed line) instead of tying it to V_{DD} (black dashed line) directly. This way, if the current limit has not been reached by the end of a PWM period, the MOSFET turns off for the next PWM period. In all other cases, the behavior of the two variants is identical.

Additionally, the converter can be switched off completely by stopping the PWM frequency $f_{sw,boost}$ and asserting the *"Clear"* input to the flip-flop. This happens in the two following cases: First, when the *"Enable"* (EN) pin is pulled low, which is done by the main μC outside of the specified HC supply phase, and second, when the maximum storage voltage $V_{store,max}$ is exceeded, which occurs regularly at light load conditions. When the enable signal is low, the μC additionally enters sleep mode to reduce power consumption. It wakes up again, when the enable input is brought high. Since a high level of the enable signal only happens during the very short DLT supply interval, low power consumption in disabled state is important giving the entire CD more margin for additional periphery like the WiFi module.

The circuit schematics depicted in Fig. 3.30 and Fig. 3.31 reveal that no input capacitance has been used because a large capacitor would cause excessive inrush currents, which could not be regulated in that case. In order to avoid any oscillations a very small capacitance, which does not affect the current regulation, has however been inserted at the input of the circuit. Since the boost converter cannot control the input current when the voltage on C_{store} is larger than its input voltage, care must be taken to avoid this situation. For

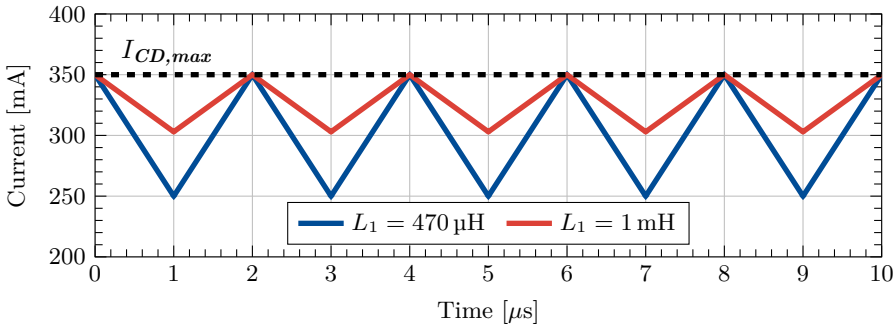


Figure 3.32: Influence of inductor size on drawable average input current of the boost converter in power supply concept B for DLT CDs.

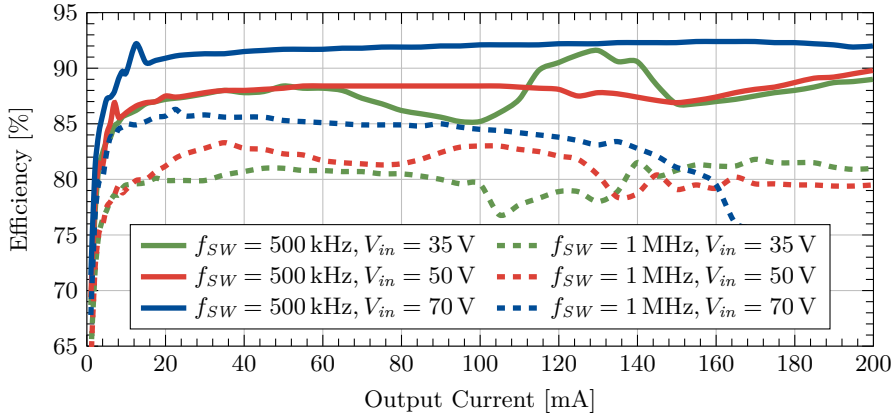


Figure 3.33: Measurement on the effects of switching frequency and input voltage on boost converter efficiency.

this reason, the flyback converter only turns on, when V_{store} has reached 80 V. This allows the boost converter to build up some initial charge on C_{store} before any significant power is drawn by the second converter stage.

Fig. 3.32 shows the influence of the inductor size on the input current of the boost converter. Because the maximum current limit $I_{CD,max} = 350\,mA$ must not be exceeded, the size of input current ripple determines the maximum available energy. A lower current ripple hence yields a higher average input

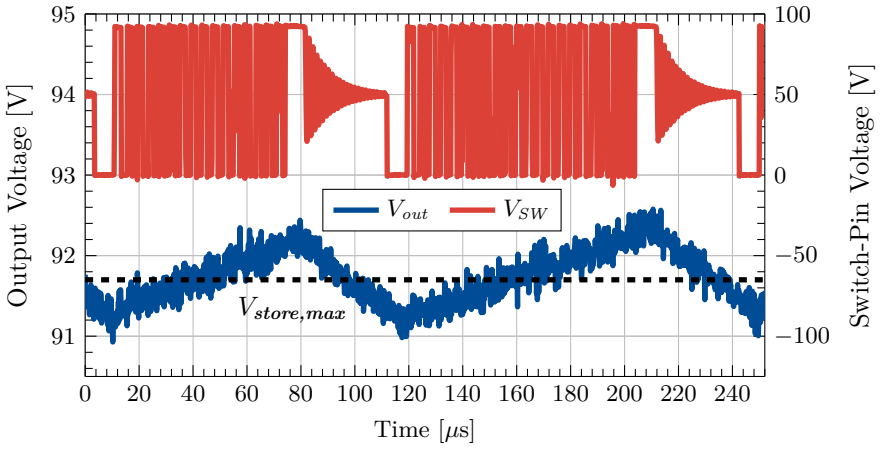
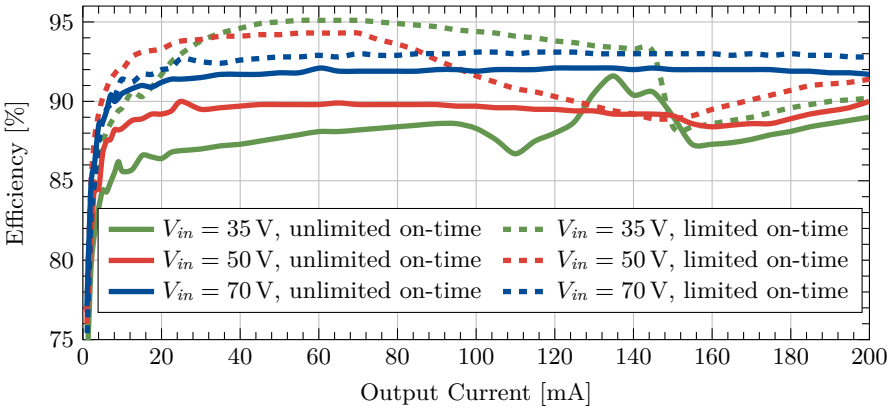


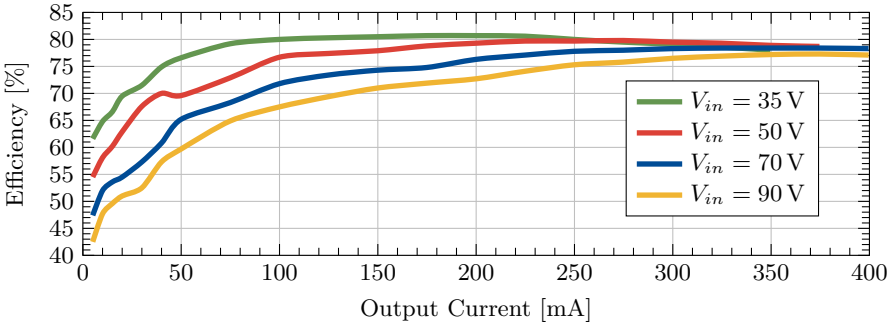
Figure 3.34: Measured output and switch pin voltages of the developed boost converter for a constant 100 mA load.

current as it is possible to move closer to the DLT limit. As can be seen from Fig. 3.32, the dimensioning of L_1 is hence critical. A higher inductance value obviously yields a lower current ripple, hence increasing the possible average current draw. However, a higher inductance goes along with a bigger footprint, a longer ramp-up time at turn-on and higher ohmic losses due to a bigger parasitic resistance. The current ripple can also be decreased by selecting a higher switching frequency $f_{sw,boost}$, which in turn increases the dynamic losses of the converter. Therefore, the trade-off between inductor size, switching frequency and the amount of available energy needs be to be optimized.

Fig. 3.33 shows the efficiency of the boost converter versus load current for different constant input voltages and switching frequencies. Although the switching frequency should be as high as possible to minimize the input current ripple, the dynamic power losses have to be considered. Fig. 3.33 depicts the significant impact of these dynamic losses. With a switching frequency of $f_{sw,boost} = 1\,\text{MHz}$ the converter efficiency is between 5 % to 10 % lower compared to identical scenarios with $f_{sw,boost} = 500\,\text{kHz}$. For the presented implementation a switching frequency of $f_{sw,boost} = 500\,\text{kHz}$ has thus been selected. Using this lower frequency actually leaves some headroom for optimization as the μC can run at a lower clock frequency, reducing its power consumption. Consequently, the μC clock frequency has been lowered from 8 MHz to 1 MHz.



(a) Measured boost converter efficiency.



(b) Measured flyback converter efficiency at $V_{out} = 3.3\,\mathrm{V}$.

Figure 3.35: Measured efficiencies of the converter stages of supply concept *B* dependent on load current for different input voltages.

Fig. 3.34 presents output and switch pin voltage of the developed boost converter for a constant current load of 100 mA. It is clearly shown that the storage voltage ripples around its target value $V_{store,max} = 91.7\,\mathrm{V}$. This waveform originates from the overvoltage protection circuit. The converter stops operating when the output voltage exceeds $V_{store,max}$ and starts operating again when it has dropped below this threshold. The large ripple is caused by the hysteresis of the comparator and the delays introduced by the software running on the μC.

Table 3.7: Selected component values for power supply concept B.

Component	C_{store}	C_{out}	L_1	L_2	R_{sense}	
Value	5 µF	10 µF	1 mH	300 µH	0.33 Ω	
Resistor	R_1	R_2	R_3	R_4	R_5	R_{set}
Value	8.2 kΩ	68 kΩ	10 kΩ	180 kΩ	7.5 kΩ	2 Ω

Fig. 3.35a and Fig. 3.35b show the measured efficiencies of the individual converters with constant supply voltages applied to their inputs. The boost converter's efficiency was measured with the μC running at 1 MHz for both variants shown in Fig. 3.31. It can be seen that the variant with limited MOSFET on-time has significantly higher efficiency especially at light loads. Fig. 3.35a shows also an improvement compared to the efficiency measured with the controller running at 8 MHz from Fig. 3.33. For all different input voltages the boost converter provides a quite good efficiency. The efficiency of the flyback converter on the contrary is rather poor. Especially for high input voltages and under light load conditions the flyback efficiency drops significantly. One reason for this might be that the applied IC uses an internal transistor with a relatively high on-resistance. Choosing a different COTS flyback IC or developing a custom-designed switching power supply for the second stage might be possible solutions to further increase efficiency and hence boost the available output power.

Summarizing all implementation considerations finally yields Table 3.7, which depicts the selected component values that have been applied in the final hardware implementation. Again, only ceramic capacitors were used.

3.3.5 Performance Evaluation and Comparison of Power Supply Concepts A and B

The performance evaluation and comparison of the two topology implementations mainly founds on measuring the maximum available output power, conversion efficiency and robustness on missing utility grid half-waves (HWs) as these parameters determine the actual capability and qualification of the developed supply concepts regarding the desired power hungry application scenario. Fig. 3.36 shows the realized measurement board, on which both power supply topologies have been implemented according to the given descriptions in sections 3.3.3 and 3.3.4 using dimensioning listed in tables 3.6 and 3.7, respectively. In order to draw a fair comparison in the end, both power supply

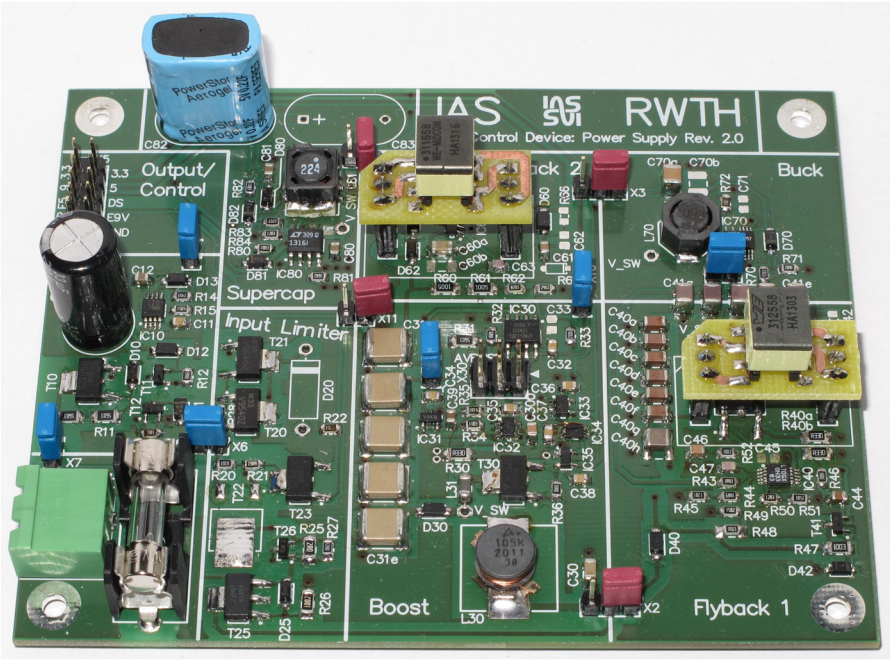
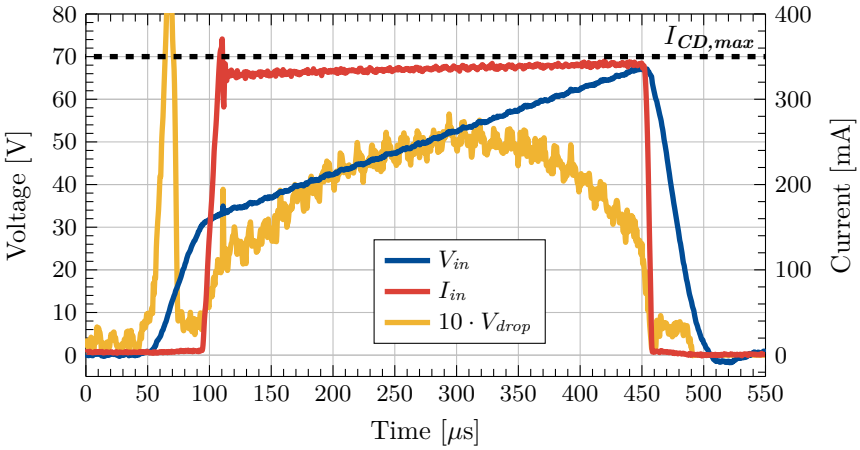


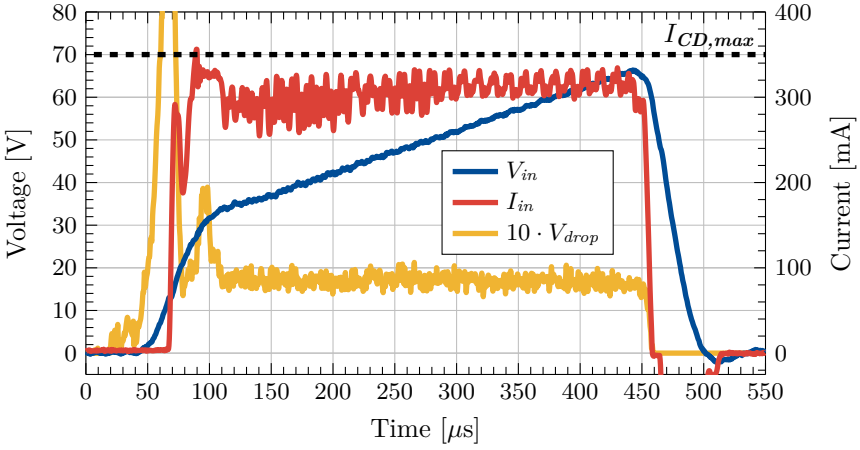
Figure 3.36: Photograph of the developed test board with both power supply concepts using the same current limiter and enable switch.

circuits share the same current limiter and enable switch at the input, thus ensuring an identical measurement setup for concept A and B in all cases. For the presented measurements an output voltage of 3.3 V, a typical supply voltage for a microcontroller and its periphery, has been selected for both topology implementations. Both power supply concepts are evaluated while complying to the official DLT standard [106] and were realized with commercially available off-the-shelf (COTS) components as presented in publications [238], [241].

Fig. 3.37a and Fig. 3.37b show the measured input waveforms of power supply concept A and B, respectively, at a load current of 100 mA each. As shown, both concepts fully comply with the DLT standard [106] depicted in Fig. 3.3 except for a very short negligible overshoot at the beginning of the supply interval. Although both concept implementations are measured with the same applied input voltage waveform and at identical measurement conditions, the input current waveforms differ significantly as those depend on the power supply



(a) Current limiter voltage drop measurement of concept A during DLT supply period.



(b) Current limiter voltage drop measurement of concept B during DLT supply period.

Figure 3.37: Measured input characteristcs and voltage drop over the input current limiter of power supply concept A and B at $I_{load} = 100\,\text{mA}$.

topology used. Due to the architecture of concept A having a comparatively large capacitor at the input, its ripple on the input current is much lower

compared to that of concept B. Hence, from the theoretical point of view, it is expected to achieve a higher output power with concept A because a higher average input current can be drawn. However, this only holds true, if the voltage drop over the current limiter is not significantly higher than that of concept B as already mentioned in section 3.3.3. Fig 3.37a and Fig. 3.37b therefore also display the measured voltage drop over the limiter for each power supply topology. It can be seen that the voltage drop over the limiter is nearly double in case of concept A compared to concept B, which is consequently expected to result in a corresponding efficiency or drawable output power decrease as discussed in the subsequent paragraphs.

Achievable Efficiency and Output Power

Fig. 3.38 depicts the overall efficiency for both power supply topologies measured under discontinuous input conditions compliant to the DLT standard [106] and with an output voltage of 3.3 V. In terms of efficiency and maximum output power concept B is in fact superior to concept A, which can be seen from Fig. 3.38 and Table 3.8. The peak efficiencies have been measured at maximum load conditions, which was determined to be a load current of $I_{load,max,A} = 105\,\text{mA}$ for concept A and $I_{load,max,B} = 119\,\text{mA}$ for concept B. Concept A achieves a peak efficiency of $\eta_{peak,A} = 63.7\,\%$, whereas concept B has a slightly higher peak efficiency of $\eta_{peak,B} = 66.3\,\%$. Comparing both concepts at an output current of $I_{load} = 100\,\text{mA}$, which is a typical case for an active WLAN module, efficiencies of $\eta_A = 60.9\,\%$ and $\eta_B = 62.8\,\%$ were recorded for concepts A and B, respectively. It can be seen that the overall peak efficiencies are close to the maximum considering the individual converter efficiencies measured at continuous input conditions as shown in Fig. 3.28a, Fig. 3.28b, Fig. 3.29a, Fig. 3.29b, Fig. 3.33, Fig. 3.35a and Fig. 3.35b. With regard to the very limited input power and the discontinuous conversion operation, this represents a very good result. For smaller output powers the respective efficiency drops significantly. This is because both concepts have been optimized for maximum energy yield at the output with regard to the input power restrictions. In fact, it is difficult to achieve efficiencies higher than 80 % as the individual converter efficiencies of first and second stage multiply and the discontinuous input voltage conditions reduce efficiency even further. Moreover, the enable switch and the current limiter also contribute to the power losses. Furthermore, the high voltage ratio between V_{store} and V_{out}, particularly for concept B, limits the achievable efficiency. Although the efficiency drops drastically for lower load cases, the available power from both supply concepts is still sufficient to functionally operate the CD. Hence, this efficiency drop is

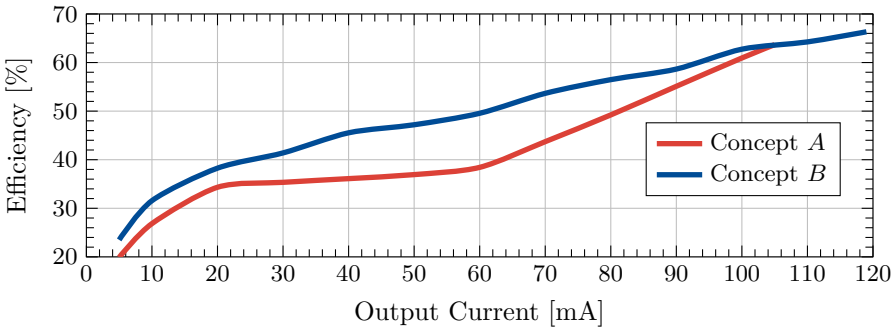


Figure 3.38: Overall efficiency of both concepts A and B at $V_{out} = 3.3\,\mathrm{V}$ over drawn load current.

not relevant for the described application scenario. The power dissipation due to this low efficiency is moreover insignificant compared to the power draw of a typical LED luminaire. Nevertheless, the proposed power supplies are not suited for operating during standby mode or the so-called "power controlled off state" of the DLT standard [106] because completely different boundary conditions apply. In this case nearly the entire mains voltage drops over the CD and the protection switch is turned off to prevent the proposed power supplies from being connected to too high input voltages. For standby mode operation an additional small power supply must hence be used that can be optimized for high efficiency at low current draws. In addition to the measured efficiencies, table 3.8 shows the maximum available output power. The proposed concepts yield maximum continuous output powers of $P_{out,max,A} = 353\,\mathrm{mW}$ and $P_{out,max,B} = 389\,\mathrm{mW}$ for concepts A and B, respectively. Thus, concept B outperforms concept A by an additional output power of almost 36 mW. The achieved output power of concept B nearly reaches the worst case approximation in power demand during WLAN association phase calculated by adding the results of equations 3.20 and 3.21. The slight difference is expected to be covered by stored charge in buffering capacitors C_{out} and C_{store} or if the power demand of the CD's periphery can be reduced by about 2 mA. For the same reason the achievable output power of concept A might even be high enough for enabling WiFi operation and surviving the association phase as proven in the following by functionality and robustness tests.

One reason for the worse performance regarding efficiency and maximum output power of concept A may be found in the voltage drop across the current

Table 3.8: Comparison of measurement results on efficiency and maximum available output power for both power supply topologies.

	Concept *A*	**Concept *B***
Measured efficiency at $V_{out} \approx 3.3\,\mathrm{V}$ and at drawn load current $I_{load} = 100\,\mathrm{mA}$	60.9 %	62.8 %
Measured efficiency at $V_{out} \approx 3.3\,\mathrm{V}$ and at drawn load current $I_{load,max} =$	63.7 % 105 mA	66.3 % 119 mA
Maximum available output power $P_{out,max}$ at regulated output voltage $V_{out} =$	353 mW 3.36 V	389 mW 3.27 V

limiter as mentioned earlier. A comparable or even higher output power of concept A versus concept B could only be achieved, if the voltage drop over the limiter is nearly identical in both cases. Furthermore, efficiency and maximum output power of concept A are also reduced due to the poor performance of the buck converter stage, which leaves some room for improvement. As the buck converter efficiency is quite low for the chosen intermediate voltage of $V_{store,max} = 40\,\mathrm{V}$, overall efficiency is expected to increase by either selecting a better suited buck converter IC or by tweaking $V_{store,max}$ and C_{store} as explained earlier in section 3.3.3. The trade-off between the amount of stored energy and the overall efficiency can be further optimized for specific applications with these measures. The efficiency of concept A could also be increased, if the buck controller was supplied with power from the output voltage. Although this measure would require an additional start-up circuit, it is not a major drawback since the start-up circuit is already required for a DLT CD anyway.

Circuit Complexity

Circuit complexity, another good reference criterion for comparison of two concepts, is evaluated to be nearly identical for both investigated power supply topologies. Of course, circuit and board design require more effort for concept B at first glance because it uses a custom-made SMPS controller for the boost converter stage, whereas concept A just applies COTS ICs [241]. The additional effort for the boost converter's control circuitry of concept B is basically attributed to the nonavailability of suitable boost controller ICs. Building an appropriate ASIC solves this discrepancy making the slightly higher hardware effort of the presented implementation with COTS components completely negligible. It might even be beneficial for both concepts to built a single

Table 3.9: Measurement results on robustness for power supplies of DLT CDs.

	I_{load}	Concept *A*	Concept *B*
Time without applied V_{in}, until	10 mA	450 ms	228 ms
V_{out} drops significantly (> 10 %)	50 mA	98 ms	59 ms
for specified load currents I_{load}	100 mA	46 ms	32 ms
Number of missing half-waves that	10 mA	43 HW	21 HW
can be compensated for	50 mA	8 HW	4 HW
(no drop in output voltage)	100 mA	3 HW	1 HW

controller ASIC for the two converter stages in order to achieve a distinct cost advantage for high volume productions. In this way, implementation and control of the second converter stage can be further optimized in each of the presented supply concepts as explained above. Since the trade-off between storage capacitance C_{store} and voltage V_{store} is not maxed out, particularly for concept *A*, it is expected to improve overall efficiency and available output power for each topology by developing an ASIC solution.

While both power supply concepts are generally capable of providing galvanic isolation, a single die solution is particularly interesting for concept *B* because the decoupling is realized at the output of the second converter stage. A monolithic integration of the two controller circuits for both converter stages is thus easily feasible in that case. Because power supply concept *A* on the contrary provides the option of electrical isolation between first and second converter stage, a monolithic integration of both controller circuits becomes impractical. If galvanic isolation must be ensured by the electrical circuitry, it would only be possible to realize concept *A* with two separate die islands inside of a single package, which appears from the outside as a single IC. In this case power supply concept *B* features a clearly noticeable cost advantage over concept *A* due to the lower effort regarding packaging and die production. Otherwise, it can be thought of building two individual ASICs for first and second converter stage of each concept that are optimized for the respective topologies. In terms of safety considering protection against electric shock concept *A* is easier to handle because its second converter stage operates in a voltage domain, which can safely be touched [158], [241]. This is a complexity advantage over concept *B*, which operates both converters in high voltage domains, especially when using COTS components.

Functionality and Robustness Tests

Both power supplies were tested with a load of a WiFi module [357] in a real setup with a DLT compatible luminaire and have proved to work reliably over a long period of time. Each concept was able to power the WiFi module continuously, such that data for lighting control could be received by the frontend. The provided output powers of both concepts are also high enough to supply an LCD [355] and a ZigBee interface [347] simultaneously. It would moreover be possible to use different output voltages, e.g. 5 V or 12 V, for other applications, which would yet lead to efficiency changes.

Table 3.9 presents measurement results on robustness of the investigated power supply architectures. It is checked, how long the power supplies under test can power the load when no input voltage is applied. By these means the concepts are tested for robustness against blackouts of the utility grid. It is likely to happen that several half-waves (HWs) of mains are missing during normal operation. The recorded data clearly shows that the topology of concept A is more robust against these blackouts of the utility grid compared to concept B. In case of missing HWs concept A can supply its load without a drop in output voltage about twice as long as concept B under the same conditions. The reason for this discrepancy in robustness arises from the difference of stored energy in C_{store}, as it depends on capacitor size and selected intermediate voltage V_{store}. Due to the higher storage voltage in case of concept B available capacitors and sizes are limited and much more expensive. Therefore, comparable robustness could only be achieved, if high voltage capacitors featuring bigger capacitance are available and a significant cost increase can be tolerated for concept B.

In summary, both power supply topologies are applicable to wall mounted CDs and smart dimmers, if series-connected luminaires or CGs provide the required current bypass [241]. Thereby, they are also compatible to and work with conventional incandescent bulbs and CFLs. The presented concepts for power supplies in DLT CDs proved functional to operate a CD with a wireless uplink, such as WLAN or ZigBee, in addition to a user interface like an LCD.

3.4 Towards Bidirectional DLT Communication

While the DLT approach provides beneficial features, such as low standby power consumption, high robustness or compatibility to existing infrastructure and light sources, it is however limited to its unidirectional communication capabilities [235]. Thereby, CGs lack the ability of sending information back to the CD [243]. Although a bulky and expensive band elimination filter for getting rid of any PLC originated distortions is saved in this way, it might still

be useful to provide a return channel for several reasons. A bidirectional DLT communication would e.g. enable a better system integration of DLT sub-systems into a smart home environment or other intelligent control systems. In this way, DLT would be able to facilitate all kind of smart features, which consequently increases system intelligence significantly. Beyond that, bidirectional DLT offers distinct advantages that are highlighted in the following.

First, CGs would have the possibility to transmit status information of installed luminaires, such as remaining lifetime or failure and fault detection for maintenance purposes [243]. Considering public, office, hospitality or industrial applications this feature could substantially reduce (maintenance) costs [292], e.g. by predicting estimated failure time of employed LEDs and replacing weak illuminants all at once. Second, and maybe even more important, the backward transmission could be used to save energy on system level in a smart home environment [97], [243] by employing presence detection, occupancy and light level sensors. Instead of always illuminating an entire room at a constant light level, the main control system can adapt light intensity to specific needs and surrounding conditions by applying intelligent control strategies based on this sensor data [257], [287], [323]. Using occupancy and presence detectors e.g. enables localized illumination of certain areas and spots of a single room [197], [278], [397], [434], whereas light level sensors can help to adjust light intensity in dependency of the actual daylight by measuring the ambient illuminance [257], [401]. Taking the described measures, the energy demand in office buildings can approximately be halved, which has been experimentally validated [307]. Integrating sensors directly into an intelligent luminaire saves additional effort and space [97], while yielding comparable results to sensors directly located at the workspace plane [50]. Also in terms of power supply and communication interface such a high integration is beneficial as these components can be reused for embedded sensors. In literature both, centralized and decentralized, control techniques have been reported and proven functional for such kind of applications and smart control systems [49], [285], [286], [388], [394].

Additionally, a reverse communication channel could be used to reduce power consumption of the acDLT communication. Currently, a DLT CD continuously sends a selected telegram over and over again because it cannot guarantee that all CGs have received the corresponding data [243]. Using a proper automatic repeat request (ARQ) protocol, bidirectional DLT communication could minimize active transmission times [97]. If attached CGs transmit an acknowledge command back to the CD by this means, the CD could stop transmitting once all CGs have received the sent telegram. As in a typical lighting scenario parameters like brightness, color or color temperature would not change that often, a bidirectional DLT communication may lead to significant

savings regarding power consumption of the total system. Since only one CG needs to provide the high- and low current carrying paths for the operating CD, an intelligent bypass structure could be applied for attached DLT CGs. Using a backward channel with an ARQ protocol would hence allow to turn off other bypasses in additionally connected CGs or limit at least the overall sum of flowing bypass currents to the specified minimum by a proper control mechanism in each CG. This method would further reduce power consumption of a DLT communication system and increase system efficiency.

Thus, realizing a bidirectional DLT communication interface enables a broad variety of new possibilities and advantages, which makes it worth to be further investigated. Therefore, this chapter presents a suitable method and concept for backward transmission in an existing DLT system and develops transmitter (TX) as well as different receiver (RX) circuits for the reverse (REV) channel in CG and CD, respectively. As mentioned in chapter 3.2, it needs to be distinguished between the existing forward transmission and the novel backward modulation. Correspondingly, RX and TX circuits for DLT backward transmission are in the following referred to as REV-RX and REV-TX, respectively. Obviously, the REV-TX must be situated in attached DLT CGs while the REV-RX is installed in the operating DLT CD. Fig. 3.39 illustrates the DLT system concept and wiring as a modified version of Fig. 3.1 (and Fig.A.1 in the appendix) while highlighting particular aspects for a DLT backward transmission. The main ideas and findings of this bidirectional DLT communication that are shown here have been introduced, presented and investigated in [97] and [243]. In addition to the investigations of these previous works, this thesis proposes further refinements of the different REV-RX concepts, develops an improved digital reverse detector relying on a matched filter and subsequently evaluates all REV-RXs regarding robustness and possible perturbations by recording the corresponding TERs in long-term measurements. For comparability to other communication techniques, power consumption and complexity are also considered and investigated in the following study.

3.4.1 System Considerations for Bidirectional DLT

As the voltage signal is already used for DLT forward (FW) modulation, it is impractical to transmit the backward modulation on the same channel [243]. Both time and frequency multiplexing could not be realized without major efforts in compliance to the existing standard due to synchronization and interference issues, respectively, as explained in the following. Although time multiplexing appears rather simple at first glance, it requires precise synchronization to ensure non-overlapping of the corresponding signals of forward and backward

Figure 3.39: System concept of bidirectional DLT communication highlighting internal setups of CD and CG.

transmission [97]. The DLT standard [106] however allows the FW modulation to vary its actual transmit time within a certain window in the data period, namely between t_7 and t_8 before the next zero crossing according to Fig. 3.4. Accounting for typical grid fluctuations, the starting point of time for transmitting with respect to a half-wave might moreover change between consecutive half-waves. Using a fixed synchronization scheme hence becomes impractical and would also violate the current DLT standard [97], [106]. Synchronizing on a transmitted FW modulation frame would also not work because of two reasons. First, dynamic frame synchronization is difficult for a frame sequence of only six (half-)bits [97]. Second, even if this issue could be solved, this type of synchronization would result in a timing violation with respect to the current DLT standard [106]. Assuming identical modulation of forward and reverse channel regarding half-bit time and frame structure, two consecutive frames would last

$$T_{2frames,synched} = 2 \cdot T_{frame} = 2 \cdot 300\,\mu s = 600\,\mu s\,, \tag{3.30}$$

since each frame consists of six 50 µs lasting half-bits. Calculating the time difference for the transmit interval in the DLT data period [106] yet only delivers

$$\Delta t_{transmit} = t_7 - t_8 = 800\,\mu s - 250\,\mu s = 550\,\mu s\,, \tag{3.31}$$

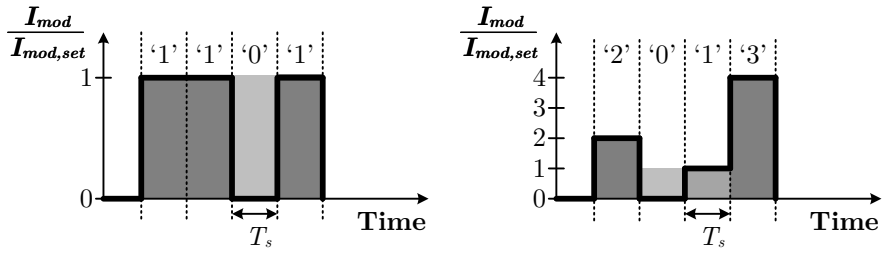
which is smaller than $T_{2frames,synched}$. It is thus not possible to ensure synchronization of FW and REV channel in compliance with the current DLT standard. While frequency multiplexing – as it is e.g. used in OFDM – does not require synchronization due its inherent orthogonality, it demands non-overlapping frequency spectra [97]. Due to the limited slew rates in the OOK modulation of DLT FW transmission the resulting spectra is rather wide, which makes it difficult to define a frequency margin for non-interference of FW and REV modulation. Using a much higher frequency for a proper decoupling causes spurious emissions in RF bands due to the non-shielded power line, whereas a considerably lower transmission frequency would not provide the required time resolution [97]. Frequency multiplexing is in consequence of these interference issues also not suitable for a robust backmodulation in a DLT system.

Therefore, the basic idea for implementing DLT backward transmission is to modulate the load current and use it as a communication channel for sending data from a CG back to the CD. The DLT backward transmission generated by the REV-TX in a DLT CG is hence called current modulation (I-MOD), whereas DLT FW transmission caused by the FW-TX situated in a DLT CD is referred to as voltage modulation (V-MOD) in the following. Still, different disturbance sources, which could cause an interference of FW and REV channel, also need to be considered in case of employing the I-MOD technique for DLT

backward transmission. The main reason for interference essentially originates from the current-to-voltage relationship of mains in this context. Creating current pulses on the power line for establishing the backward transmission obviously affects the voltage waveform as a function of connected load and wiring resistances [97]. In addition to theses disturbances, which relate to the communication channel itself, other connected devices may introduce critical perturbations, e.g. by distinct peak current draws or using an active PFC in their power supplies. Thereby, these perturbation effects are considered in the investigated test setup for bidirectional DLT as explained in section 3.4.4.

A similar approach for bidirectional power line communication employing voltage and current modulation for FW and REV channel, respectively, is already used in industry by a smart home system called *"digitalSTROM™"* [101]. In fact, this system has been developed in parallel and independently from the DLT approach. While digitalSTROM™ is only a proprietary system, DLT on the contrary operates as an official IEC standard [106]. It might still be helpful and interesting to investigate a digitalSTROM™ system for further learnings and study of critical effects. Such an investigation however exceeds the scope of this thesis and is therefore attributed to future work.

Using a modulated load current as the REV channel, DLT backward transmission may apply different modulation schemes in realizing this. The most common ones are on-off keying (OOK), amplitude-shift keying (ASK) and (binary) frequency-shift keying (FSK). Although FSK represents the most sophisticated technique, which is rather resistant against amplitude degradation caused by noise, it requires higher carrier frequencies that would lead to undesired emissions due to the weak shielding of the power line [97]. Hence, FSK is not suitable for DLT backward transmission and would beyond that implicate the highest complexity and hardware effort. For simplicity reasons an ordinary on-off keying is thus being used for DLT backward transmission switching the amplitude of the modulation current I_{mod} only between two levels, $I_{mod,low} = 0\,\mathrm{mA}$ and $I_{mod,high} = I_{mod,set}$. In this way hardware effort and complexity for both, REV-TX and REV-RX, are minimized because only one bit per symbol is being transmitted [97]. The ASK can rather be seen as an enhancement of OOK because it increases the data rate by mapping n bit on 2^n symbols, which correlate to different current amplitude levels in this case. The number of used current modulation levels is however bound to the REV-RX's sensitivity and channel SNR [97]. Due to its increased complexity compared to OOK, ASK shall hence be left open as a possible extension to the DLT backmodulation concept presented in this thesis. Still, ASK might be quite useful for the described application scenario of a DLT return channel. Fig. 3.40 exemplarily depicts the modulation scheme for a simple OOK and an



(a) On-off keying (OOK) scheme. (b) Amplitude-shift keying (ASK) scheme.

Figure 3.40: Suitable modulation schemes for DLT backward transmission.

ASK with $n = 2\,\text{bit/symbol}$, which results in four effective current levels. As can be seen, a selected current amplitude stays constant for the symbol time T_s, which is equal to modulation frequency $f_{mod} = T_s^{-1}$ [97].

To enable robust but energy efficient data transmission the amplitude of the modulation current I_{mod} in the employed OOK needs to be selected carefully. On the one hand, a higher modulation amplitude ensures more robust data transmission for the REV channel, on the other hand it directly determines the power consumption for DLT backward transmission, which is desirable to be kept as low as possible. A higher current modulation amplitude is also more likely to interfere with the V-MOD of the DLT FW-TX due to load and wiring dependent current-to-voltage relationship of mains. Therefore, the minimum value for $I_{mod,set}$ needs to be found, for which a reliable detection is still feasible, which obviously strongly depends on the developed REV-RX concepts and associated sensitivity. Tuning architecture and implementation of the chosen REV-RX concepts consequently optimizes the trade-off between required SNR and power consumption for DLT backward transmission.

Furthermore, when selecting the modulation current level $I_{mod,set}$ one needs to recall the maximum current limit $I_{CG,max}$ specified in the DLT standard for current draws during DLT data period. Equation 3.1 in section 3.1.2 denotes the corresponding formula of this time variant current limit $I_{CG}(t)$ in dependence of the instantaneous mains voltage value $V_{grid}(t)$. The calculated current limit conforms to the current draw of conventional incandescent lamps and thus depends on its rated nominal power or rather on that of a DLT CG. Fig. 3.41 illustrates the time variant current limit for a 40 W and 60 W load case.

If full compliance to the existing DLT standard is desired, the modulation amplitude is hence bound to the respective moving current limit. Due to the

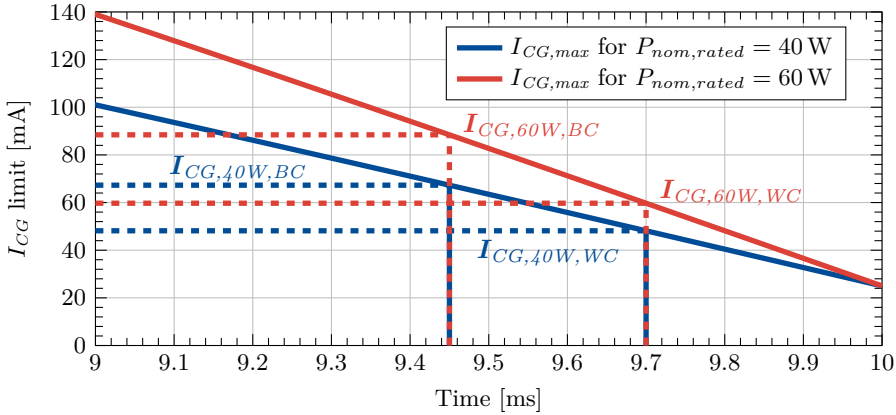


Figure 3.41: Specified current limit for a DLT CG during data period for rated nominal power consumptions of 40 W and 60 W.

descending curve progression, the latest point of time, when a high level is transmitted back, determines maximum possible modulation depth $I_{mod,set}$ considering a constant modulation current. Assuming an identical modulation scheme for I-MOD as it is used for V-MOD in DLT forward transmission, this point of time is reached, when the fifth half-bit of a frame sequence turns low because half-bit six always equals zero by specification. Fig. 3.41 consequently labels minimum and maximum timing as well as the corresponding current limit for best case (BC) and worst case (WC) with respect to the varying starting point of transmission within the data period defined by the DLT standard. For a 40 W load condition these current flow limits are determined to 67.79 mA and 48.15 mA, respectively. The current margin available for DLT backward modulation is however much smaller. At first, it necessarily needs to be accounted for the LC bypass flow of at least 18 mA. Secondly, an active PFC circuit, which could possibly be installed in a DLT CG, would also contribute to a certain current draw at the same time. Both effects however limit the available margin for the current modulation depth $I_{mod,set}$ to a minimum as they need to be subtracted from the computed current flow limits. The present DLT standard does obviously not account for a return channel using current modulation. The restrictive current draw limitation is therefore being ignored during the development process for a reliable DLT backward transmission. However, section 3.4.4 finally evaluates different REV-RX circuits regarding

the required modulation depth $I_{mod,set}$ and thereby determines the available margin with respect to the specified DLT current limit during data period.

For the communication protocol of the backward transmission using I-MOD an identical structure to the V-MOD of DLT forward transmission has been chosen. A DLT backward telegram is also sent over several half-waves of mains with two Manchester-coded information bits per half-wave. Each frame starts with a leading start-of-frame (SoF) half-bit set to *'1'* and ends with an end-of-frame (EoF) half-bit equaling *'0'*. A telegram always starts with a new start-of-telegram (SoT) frame and uses MSB first transmission on all hierarchy levels following the structure of the V-MOD as shown in Fig. 3.7 and described in section 3.1.2. Further details on the DLT communication protocol can be found in [106], [235] and have also been explained in chapter 3.1.

Beyond the mentioned considerations about available transmission channel, modulation depth and timing, used protocol as well as the specific DLT limits, another aspect needs to be deliberated for establishing bidirectional DLT communication, which is channel access collision problems. Since conventional DLT systems operate in a master-slave configuration for FW transmission, they do not suffer from this problem as only one CD continuously sends data on the voltage channel to multiple CGs. In case of bidirectional DLT, it may however occur that two or even more CGs try to simultaneously transmit data packages on the shared current channel back to the operating CD [97]. If that happens, a REV-RX situated in the operating CD might consequently not be able to distinguish between the multiple messages of the different CGs or might not be able to detect the I-MOD at all, which would thus lead to loss of information [97]. In order to prevent this undesired effect from happening, it is inevitable to employ a proper protocol managing the REV channel access.

As explained by de Vrieze [97], standard techniques like CSMA [182] would not be applicable due to the parallel connected CGs experiencing the *"hidden node problem"* [37], [180], [189], [232], [301], [383]. Instead, MACA represents a possible solution [174], [202], [291], [419], which effectively allows slaves (*here:* CGs) to request channel access that is subsequently granted by the master (*here:* CD). de Vrieze[97] outlines the transferability and applicability of the MACA protocol to a DLT system as shortly summarized in the following. Initially, a CG inquires channel access of the CD by sending a proper request message. Broadcasting an acknowledge command, the CD informs the requesting CG to start transmitting and all other attached CGs to stay idle for a certain time. If the telegram length of the desired REV transmission is included in request and acknowledge command, this idle time could exactly be predicted. After a successful REV transmission, the requesting CG becomes idle again and other CGs may start an inquery for DLT backmodulation [97]. Additionally, a similar

scheme like classic *"ALOHA"* [2] is applied to avoid many successive REV transmissions. To protect the request messages from interference, when two or more CGs ask simultaneously for channel access, de Vrieze [97] suggests that the CD sends a NACK, which informs attached CGs about the collision. The requesting ones hence back off for a random timing before starting over as in classic ALOHA [97], while the CGs, which did not initate a transmission, remain silent until a successful REV transmission is positively acknowledged by the CD. Furthermore, the probability of request collisions can be vastly reduced by selecting a minimum telegram length for request commands.

This work however focuses on the basic functionality and physical hardware for establishing a robust bidirectional DLT communication. Protocol refinements and solutions for solving channel access collision problems hence goes beyond the scope of this thesis and are consequently attributed to future work.

3.4.2 Reverse Transmitter Concept and Implementation for Bidirectional DLT Communication

The REV-TX circuit is rather simple to realize, particularly when recalling the implementation of the LC bypass in a DLT CG as explained in section 3.2.1. In fact, the LC bypasss already provides a defined current path, just as it would be needed for DLT backtransmission. Hence, modifying this circuit enables the desired functionality, while saving hardware effort due to a high reuse factor. Since the bypass current depends linearly on the employed sense resistor R_{sense}, as determined by equation 3.4, a current modulation can easily be implemented by tuning R_{sense} accordingly. For the investigations conducted in this research the LC bypass has therefore been extended by a binary weighted resistive digital-to-analog converter (RDAC) that is controlled via an 8 bit shift register as can be seen from Fig. 3.42. In this way the modulation current I_{mod} can be adjusted linearly by a digital control word b_{RDAC}.

Recalling equation 3.4 and considering the binary resistor weighting with

$$R_0 = 2 \cdot R_1 = ... = 2^{N_{RDAC}-1} \cdot R_{N_{RDAC}-1} \tag{3.32}$$

$$\Rightarrow R_n = \frac{R_0}{2^n}\,, \tag{3.33}$$

the current modulation amplitude is calculated by

$$I_{mod} = \frac{V_{BE}}{R_{mod}} = \frac{V_{BE}}{R_0} \cdot b_{RDAC} = \frac{V_{BE}}{2^7 \cdot R_7} \cdot b_{RDAC}\,, \tag{3.34}$$

where b_{RDAC} is the digital control word ranging from 0 to 255.

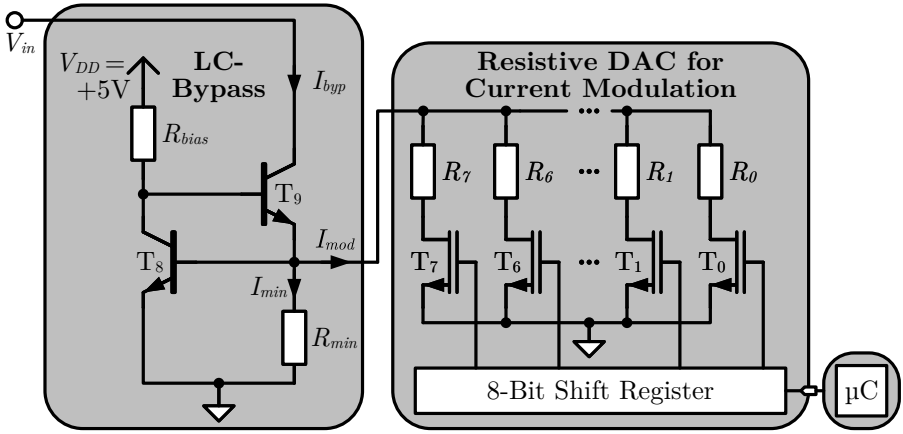


Figure 3.42: Modified LC bypass in a CG with digital controllable current modulation level $I_{mod,set}$ suited for DLT backward transmission.

Changing the modulation amplitude $I_{mod,set}$ in the applied OOK data transmission allows for testing different modulation depths during experimental validation. Thereby, the optimum trade-off between power consumption and robustness can be found in dependence of the chosen REV-RX circuit.

The resistances for the hardware implementation have been chosen according to the values listed in Table 3.10. In conjunction with the selected resolution of the resistive DAC of $N_{RDAC} = 8$, the modulation current I_{mod} can thus be set in steps of $\Delta I_{mod} = 1.37\,\text{mA}$. The minimum current level is determined by R_{min}, which is the low current level required by the DLT standard for forward modulation. In this case I_{mod} equals zero. With the selected component values the modulation current can be tuned to a maximum of $I_{mod,max} \approx 350\,\text{mA}$. The value for R_{bias} has to be reduced to $510\,\Omega$ in contrast to the original current sink shown in Fig. 3.12a in order to reach this maximum value. Otherwise the modulation current would be limited to a value of about $I_{mod,limit} \approx 180\,\text{mA}$ because R_{bias} limits the current flow into the base of T_9.

Table 3.10: Selected resistance values for the implemented 8 bit RDAC.

Resistance	R_{bias}	R_{min}	R_0	R_7
Value	$1\,\text{k}\Omega$ ($510\,\Omega$)	$33\,\Omega$	$512\,\Omega$	$4\,\Omega$

3.4.3 Reverse Receiver Concepts and Implementation for Bidirectional DLT Communication

Architecture and implementation of the REV-RX circuit determine in the end the required SNR of the backward transmission by the receiver's sensitivity. Hence, the REV-RX defines the necessary current level of modulation amplitude $I_{mod,set}$ for reliable and robust data transmission on the reverse DLT communication channel. Therefore, different REV-RX concepts have been developed and are later on compared regarding robustness (required SNR or modulation amplitude $I_{mod,set}$, respectively), current consumption and hardware complexity in section 3.4.4. Considering the REV-RX to be situated in the operating DLT CD, it would be beneficial to reuse components and circuits of the CD for a REV-RX implementation, particularly in terms of saving hardware effort. The employed DLT CD, which is designed according to the implementation presented in [240], already incorporates a small sense resistor in its bypasses, which are needed for DLT FW modulation. Fig. 3.43 shows this configuration in the used setup of the operating DLT CD.

To enable DLT forward modulation the implemented CD features three different bypasses: A 0 V bypass passing mains voltage to the CGs, a modulating bypass generating the 15 V voltage drop for DLT V-MOD and a resistive bypass ensuring reliable zero crossing detection (ZCD). Since attached DLT CGs might draw high currents during start up to charge the input capacitors of their power supplies, an overcurrent protection (OCP) circuit in the CD is necessary to protect the bypass MOSFETs from excessive inrush currents. As shown in Fig. 3.43, the overcurrent sensing is realized by the small sense resistance $R_{sense} = 90\,\mathrm{m\Omega}$. The voltage over R_{sense} is directly fed to the input of an analog-to-digital converter (ADC) of a μC, which disables all bypasses in case of an overcurrent detection event preventing the CD from blowing up.

Using the installed sensing resistor to convert the modulated current pulses of DLT backtransmission into proportionally voltage signals enables comparatively easy setup of suitable REV-RX circuits. In this way a similar RX principle as used for DLT forward transmission relying on edge detection of a voltage signal can be applied. The sensed voltage signals needs to be filtered to suppress unwanted distortions and interfering signals. Additionally, an amplification is required due to the small sensing resistor of only 90 mΩ and a 1 bit quantizer like a window comparator or Schmitt-Trigger must be applied for proper signal reconstruction. Thereby, two different filter architectures based on this concept are developed in analog and digital domain providing the desired RX functionality. Fig. 3.44a and Fig. 3.44b illustrate the basic concepts for these two REV-RX approaches highlighting the digital domain in a light gray box.

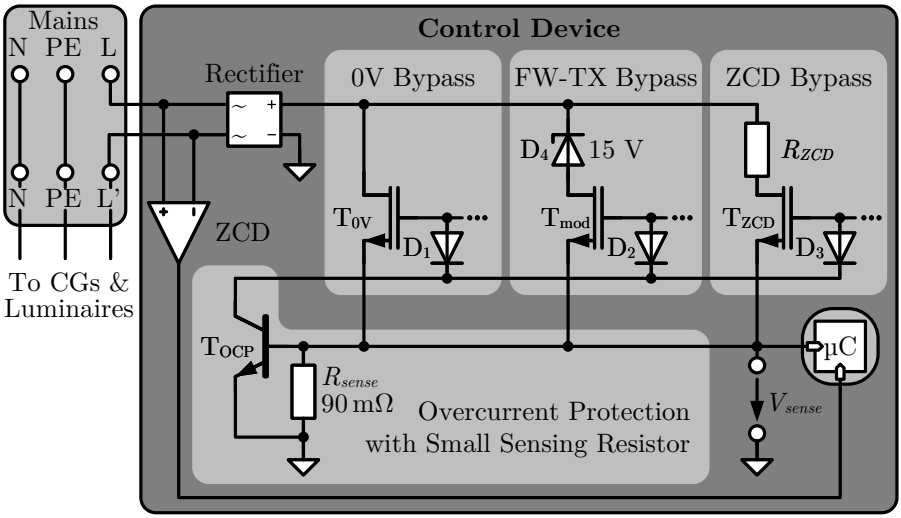
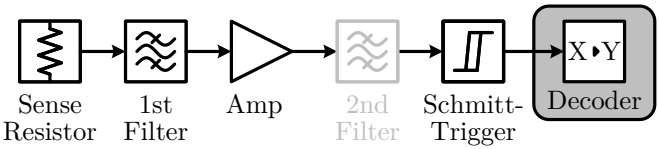
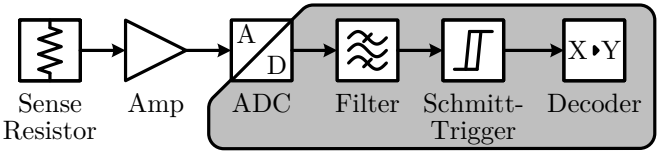


Figure 3.43: Sense resistor in bypass path of implemented DLT CD.

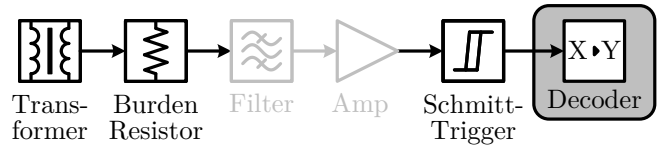
It is not demanded to utilize the sense resistor R_{sense} when developing a suitable REV-RX circuit sitting in the DLT CD. Tolerating an increased hardware effort, also other measurement principles like inductive coupling or induction by magnetic flux may hence be considered. Thereby, Fig. 3.44c shows a third approach, which is further investigated in this thesis. This concept uses a current sense transformer and its burden resistor, thereby providing galvanic isolation, which is a distinct advantage over the other two approaches justifying additional hardware effort. It is expected to achieve lower modulation amplitudes $I_{mod,set}$ and hence lower current consumption due to the passive filtering structure of the employed transformer. This concept is solely susceptible to current noise, which is typically less critical than voltage noise across a shunt resistor or from an active power supply circuit [97]. Hall effect sensors represent another suitable approach for measuring the pulsating currents of DLT backmodulation, while providing electrical isolation from mains voltage. This kind of sensors measures the magnetic field induced by the primary current and translates it into a proportional voltage [69], [296], [297], for which a separate power supply is required [97]. Different COTS Hall sensor ICs have been tested in [97] and were evaluated to suffer from poor performance compared to the other three approaches. Thus, a Hall effect sensor based concept is not considered in this thesis. However, it might be interesting to study this approach in future



(a) REV-RX concept A: Sense resistor with analog filtering.



(b) REV-RX concept B: Sense resistor with digital filtering.



(c) REV-RX concept C: Current sense transformer with burden resistor.

Figure 3.44: Conceptual architectures for different REV-RX approaches.

work building a customized Hall effect sensor tailored to the requirements for the described application scenario. In the following the three REV-RX circuits conceptually illustrated in Fig. 3.44 are described in more detail.

3.4.3.1 REV-RX Concept A: Shunt Resistor with Analog Filter

REV-RX concept *A* operates in the analog domain and relies on measuring the voltage drop over the sense resistor $R_{sense} = 90\,\text{m}\Omega$ in the CD. Applying an active bandpass filter structure this topologies combines suppressing of undesired distortions and amplification of the wanted signal in a single step. Because the modulation frequency f_{mod} of the I-MOD signal resides close to the 50 Hz grid frequency of mains, the active bandpass filter needs to provide a large gain roll-off in order to realize sufficient interference suppression of these two signals. While a typical wide-band filter is not capable of ensuring such steep gain roll-off decreasing effective SNR, a simple narrow-band filter with a center frequency f_c designed around $f_{mod} \approx 10\,\text{kHz}$ might cause inter-symbol interference due to its slow reaction time [97]. Hence, the same principle as used

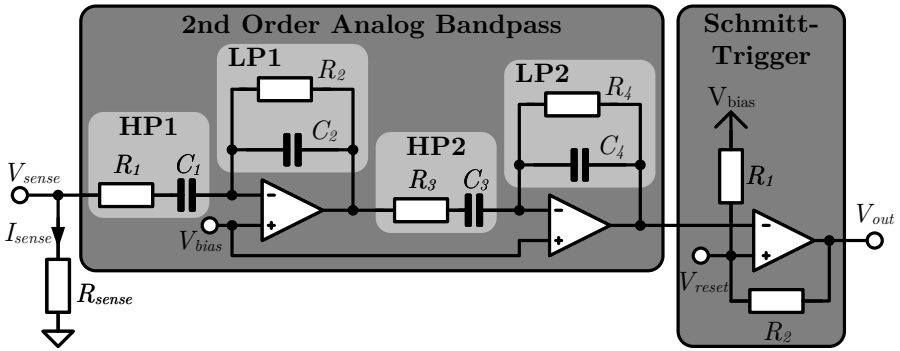


Figure 3.45: Implementation of REV-RX concept *A*: Sense resistor with active analog bandpass filter and Schmitt-Trigger.

for V-MOD in the DLT FW transmission is applied here, which is performing an edge detection by selecting a higher center frequency f_c of the analog bandpass filter than the modulation frequency f_{mod} and using a narrow-band filter setup. Fig. 3.45 shows the corresponding circuit schematics, while table 3.11 denotes a possible implementation as used during the performance evaluation presented in section 3.4.4. Compared to the implementation presented in [97] the component values have been slightly fine-tuned and hence only show minimum differences. The biasing voltage V_{bias} is generated from the 2.5 V reference voltage by means of an additional resisitve divider and set to $V_{bias} \approx 2.45\,\mathrm{V}$.

Due to the edge detection based principle, the presented narrow-band filter implementation hence yields positive and negative pulses with respect to the chosen DC biasing voltage level like a differentiator circuit. The detected pulses thereby correspond to symbol transitions of the rectangular REV-TX current waveform using a simple OOK modulation scheme. A Schmitt-Trigger circuit as highlighted in Fig. 3.45 is thus inevitable in order to subsequently transform

Table 3.11: Selected component values for the implemented REV-RX concept *A*.

Resistance	R_1	R_2	R_3	R_4	R_5	R_6
Value	1.6 kΩ	16 kΩ	1.1 kΩ	16 kΩ	39 kΩ	620 kΩ + 56 kΩ
Capacitor	C_1	C_2	C_3	C_4		
Value	1.5 nF	150 pF	100 nF	150 pF		

measured pulses according to their orientation into high and low digital voltage levels. Thereby, it operates as a simple 1 bit quantizer, while simultaneously taking care of reconstructing the original transmitted signal. The presented dimensioning results in a 180 mV ($\pm$ 90 mV) hysteresis window of the deciding Schmitt-Trigger circuit, which is thus relatively robust against distortions as it needs a large signal amplitude to toggle the Schmitt-Trigger output.

3.4.3.2 REV-RX Concept B: Shunt Resistor with Digital Filter

REV-RX concept *B* also measures the voltage drop over the sense resistor $R_{sense} = 90\,\text{m}\Omega$, which is directly connected to an ADC input pin of the main MCU, thus saving hardware effort and costs. As its name indicates, concept *B* accordingly performs filtering and evaluation of the I-MOD signal in the digital domain in contrast to concept *A*, which operates in the analog domain. Due to the small voltage drop over R_{sense} the sensing voltage is amplified in a first step to minimize quantization noise and is subsequently sampled by a 12 bit ADC of the MCU. Fig. 3.46 shows the internal hardware configuration of the μC for the digital filter implementation. The differential ADC operates in signed mode and uses an internal 1 V bandgap reference voltage [97].

Performing signal filtering in the digital domain is quite beneficial as it allows for a certain degree of freedom and flexibility. In this way, the filter can easily be adapted and even more advanced filtering approaches, which would simply not be feasible in the analog domain due to extremely increased hardware expenses, could be realized with minimal effort [97]. However, a higher complexity of the digital filter has to be traded versus computation time, which is of course limited and should therefore be kept as low as possible. Additionally, the filter capability also depends on the sampling time of the ADC and hence the number of available sample points. The presented concept thus operates the ADC in a pipeline staged design, which allows for simultaneous sampling at the input and other ongoing ADC conversions [97]. While it is desirable to keep the filter resolution as high as possible for achieving high robustness of the digital filter on the one hand, it must be feasible to process the recorded data within the limited available computation time on the other hand. Both, ADC sampling and computation time of the digital filter, are related to the system clock of the main μC and hence effect overall power consumption, particularly if a higher clock frequency should be used. Therefore, a sweet spot between power consumption, filter resolution, filter complexity and computation time needs to be found. Due to tight limitations in terms of power consumption [238], [241], [243] as described in sections 3.1.1 and 3.3.1, the main μC in the DLT CD only operates with a system clock of 2 MHz to save energy. The ADC samples

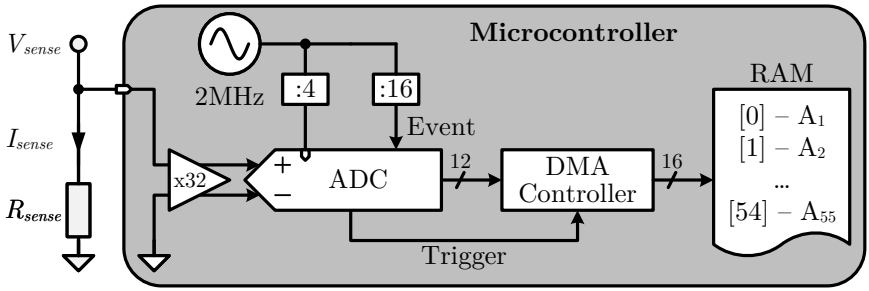


Figure 3.46: Internal hardware configuration of the μC for the digital bandpass and matched filters of REV-RX concept *B*.

the voltage drop over R_{sense} with a resolution of 12 bit every 8 µs and stores the values in the random-access memory (RAM) of the controller. In this way, the computation of the digital filtering can be processed asynchronously at a different point of time. This feature is necessary as the CD is busy with timing critical tasks during the supply and data periods. Therefore, the digital filtering is done during the operating period, when the CD is mostly idle.

Digital Bandpass Filter

Similar to the FW-RXs used for V-MOD detection [235] shown in chapter 3.2.2 the digital filter for backward transmission also relies on edge detection. A second order FIR filter realized as a difference filter has been used to achieve this. Subsequently, the filtered signal is passed through a second order moving average filter to smooth the signal and reduce the noise floor. Digital difference and moving average filter hence correspond to high and low pass, respectively, as their analog counterparts. Considering theory of true FIR filters the corresponding transfer functions can be converted from inverse z-transformation to time discrete domain according to [97], [299] by,

$$H(z) = \frac{Y(z)}{X(z)} = a_0 + a_1 z^{-1} + \cdots + a_q z^{-q} \tag{3.35}$$

$$\overset{z}{\longleftrightarrow} \; y[n] = a_0 x[n] + a_1 x[n-1] + \cdots + a_q [n-q] \,.$$

Thereby, difference and moving average filter form the digital bandpass filter with a filter coefficient vector in the time-discrete domain selected to

$$a_{bp} = a_{mov,avg} * a_{diff} = [0.5\, 0.5] * [1 \;\; -1] = [0.5 \quad 0 \;\; -0.5] \,. \tag{3.36}$$

The filter sizes have been chosen in accordance to the total computation time of the digital filter implementation since it may not exceed around 5 ms to be fully processed during the operation period. Section 3.4.3.4 describes the subsequent software evaluation and edge detection in more detail. Further details on the implementation of the digital bandpass filter can be found in [97], [243].

Digital Matched Filter

Since DLT backward modulation contains only five well-known frame sequences, the concept of a matched filter may be applied as suggested by [97]. This filter type is also known as an *"optimal (linear) filter"* or *"(auto-)correlation filter"* because it correlates the received signal with an expected transmission pattern and thereby maximizes effective SNR in the presence of additive stochastic noise [42], [170]. The matched filter may also be considered as a special case of the *"least squares approximation"* and hence represents an application of the *"maximum likelihood estimation (MLE) method"* [163], [384].

Mathematically, the correlation of two signals is realized by their convolution. Equation 3.37 presents the convolution of filter function $h(t)$ and received signal $x(t)$ in the discrete time domain. The matched filter function $h[n]$ herein represents the mirrored or time-inverse sequence of the expected transmission pattern. Instead of evaluating the actual signal waveform at its input, a matched filter therefore effectively calculates the (auto-)correlation by multiplying the sampled input signal x with the filter function h and subsequently integrating the corresponding result.

$$y[n] = \sum_{k=-\infty}^{\infty} h[n-k] \cdot x[k] \tag{3.37}$$

For the REV-RX implementation the complete correlation function may thus be realized in the digital domain on the MCU, which uses the same internal hardware setup as the digital bandpass filter depicted in Fig. 3.46. To avoid computationally intensive multiplications due to the limited computation time of the μC, calculating the correlation function of measured and expected signal sequence is performed slightly differently. The binary pattern of each expected frame sequence is bitwise tested against a high signal level. If the respective digital *'AND'* operation for the selected bit of the known signal sequence delivers a *'true'* statement, the corresponding measured ADC sample of the received signal is summed up in a temporary variable. Shifting through all available bits of the expected frame pattern and simultaneously through the corresponding sampled ADC values, the evaluation routine thereby determines a correlation of the recorded frame to the expected sequence, which is stored as an accumulated

integer number in the associated temporary variable. This kind of evaluation is performed for each frame structure, which consequently yields a distinct variable for each specific frame sequence. The variable with the biggest integer number obviously shows the highest correlation and is hence evaluated as the transmitted frame sequence of the recorded REV-TX's signal. Unfortunately, the SoT frame cannot be detected in this way as it would always feature the highest correlation. Hence the routine only checks for the four data containing bit patterns. In addition, a specific threshold is defined, which needs to be exceeded in order to recognize an SoT frame. This threshold value may be found either manually for a test setup or via an automated calibration routine in a later product. It should be noted that the μC only operates on half of the available ADC samples due to the limited computation time.

In future studies it might be interesting to investigate, whether the *"Viterbi"* algorithm can be applied for decoding DLT frames, especially in an ASIC solution. Excellent concepts and implementations of the Viterbi algorithm can be found in [123], [175].

3.4.3.3 REV-RX Concept C: Current Sense Transformer

Instead of using a small sense resistor for measuring the current pulses generated by the REV-TX, a current sense transformer can be applied, which beneficially provides the advantage of electrical isolation from mains. Exploiting the inductive coupling of its primary and secondary windings, the transformer induces a proportional current flow on its secondary side as a reaction on the current pulses on the primary side. In fact, the turns ratio of primary and secondary winding, which are coiled around a shared ferrite or iron core, determines this transformation ratio according to equation 3.38,

$$I_{sec} = \frac{N_{prim}}{N_{sec}} \cdot I_{prim} = \frac{V_{burden}}{R_{burden}}\,, \tag{3.38}$$

$$\Leftrightarrow V_{burden} = R_{burden} \cdot \frac{N_{prim}}{N_{sec}} \cdot I_{prim}\,. \tag{3.39}$$

A current sense transformer thereby scales the primary current down into a designed measurement range, while a burden resistor R_{burden} on the secondary side converts this lower current into a measurable voltage. Turns ratio and burden resistor hence determine together the overall scaling factor and must be selected in concert with one another. However, it must be taken care that the voltage drop over R_{burden} remains below the knee-point of the transformer. Otherwise the transformer core would be saturated and equation 3.38 no longer

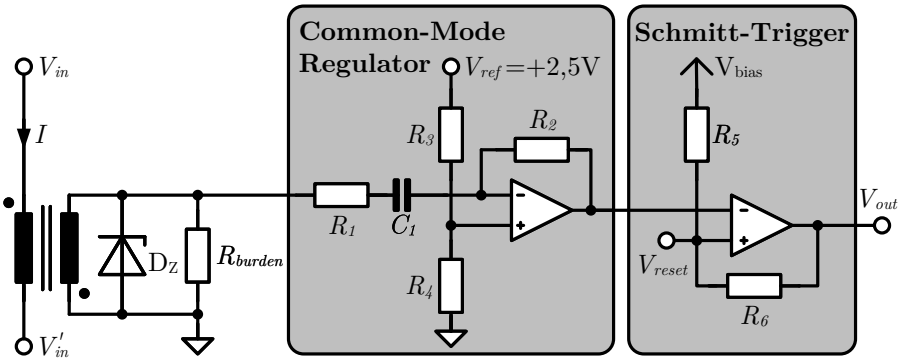


Figure 3.47: Implementation of REV-RX concept C: Current sense transformer with burden resistor.

holds true. Since high currents are expected on the primary side, which is also the case for the described DLT target application, the primary side typically features a low winding number, commonly even $N_{prim} = 1$ is used [61], [91]. This is also the case for the presented setup since a toroidal core transformer has been applied [344]. The main conductor wire of the primary side is simply fed through its hole and serves by that as the primary winding.

The current sense transformer inherently provides a bandpass filtering characteristic, which depends on structure and material of the employed transformer core, thereby setting upper as well as lower cutoff frequency. Utilizing this intrinsic bandpass property an edge detection based filter concept can be developed with minimal effort. Due to the filtering effect of the transformer, the REV modulated current pulses on the primary side correspondingly generate positive and negative current spikes on the secondary side. Similar as in the other concepts, a downstream installed Schmitt-Trigger takes care of signal reconstruction and serves again as a 1 bit quantizer for further digital processing. A Zener diode has been added in parallel to the burden resistor for protection reasons in case large current spikes occur on the primary side, which are e.g. caused by excessive inrush currents of connected loads. The realized circuit implementation is shown in Fig. 3.47, while Table 3.12 denotes the selected dimensioning of all components as used during the performance evaluation.

Although additional active filtering circuits are not necessarily required in this concept, they could still be applied to further improve signal quality or minimize inter-symbol interference [97]. Operating without extra filters would save hardware effort and in case of active circuits being applied furthermore

Table 3.12: Selected component values for the implemented REV-RX concept C.

Resistance	R_1	R_2	R_3	R_4	R_5	R_6
Value	10 kΩ	29 kΩ	62 kΩ	150 kΩ +7.5 kΩ	39 kΩ	100 kΩ +75 kΩ
Component	C_1	R_{burden}	Toroidal Transformer T_1			
Value	150 pF	1 kΩ	$N_2 = 50 \quad I_{max} = 10\,\text{A}$ $f_{trafo} = 20\,\text{kHz} - 200\,\text{kHz}$			

reduce power consumption. However, a simple amplifier regulating the DC common mode voltage to a desired offset value V_{bias} is still demanded. As a trade-off solution, the implementation used during performance evaluation of this concept combines an analog highpass filtering with the needed common mode opamp as illustrated in Fig. 3.47. The common mode voltage is selected to about $V_{bias} \approx 1.8\,\text{V}$. The burden resistor R_{burden} effectively converts the positive and negative current pulses to positive and negative voltage transitions with respect to the chosen common mode voltage V_{bias} that can be evaluated by the downstream connected Schmitt-Trigger. As can be seen from equation 3.39, the burden resistor in fact defines the actual gain of the sensing voltage in a linear manner, which allows to realize much higher measurement voltages compared to concepts A and B. The sensing voltage can thereby be fine tuned to optimally fit the Schmitt-Trigger evaluation. Due to the passive structure of the transformer the sensing signal is to the greatest extend only susceptible to current noise, which is typically less critical than voltage noise across a shunt resistor as used in concepts A and B [97]. Of course, in the presented setup some voltage noise is added on the sensing signal due to the scaling of the burden resistor and because of the active power supply on the common mode regulator. Still, the impact of theses error sources are comparatively low as they are only added with small margin on the already filtered and amplified signal of the transformer. It is therefore expected to achieve superior performance in contrast to concepts A and B, like a better sensitivity of the REV-RX implying an increased SNR and thus lower required modulation amplitude I_{mod}. Since the current implementation is of course limited to COTS current sense transformers, it is hence expected to achieve improved performance by manually building and tweaking a suited transformer optimized for the target application. Particularly, adapting the bandpass characteristic of a transformer core as well as coiling up the number of secondary windings in conjunction with selecting a suited burden

resistor will be the required actions in that case. Since this effort is evaluated as too high for the scope of this thesis, it is attributed to future work. Table 3.12 also summarizes the characteristics of the selected transformer [344]. A different current sense transformer with smaller footprint in an SMD housing [374] has been investigated in [97], which also shows suitable characteristics with a turn ratio of $\frac{N_2}{N_1} = 20$ and a frequency range of $f_{trafo} = 50\,\text{kHz} - 1\,\text{MHz}$. In experimental tests however, it turned out that this SMD transformer is not capable of keeping up with the performance achieved by the toroidal one, particularly in terms of robustness [97].

In terms of power consumption different aspects have to be considered for the current sense transformer based REV-RX concept. While the power loss on the primary side caused by the series resistance of the coil is more or less negligible due to the low turns ratio (*here:* $N_{prim} = 1$), a high burden resistor will contribute significantly even though the measurement current has been scaled down by the turns-ratio [97]. Additionally, the power consumption of the common mode voltage regulator and the Schmitt-Trigger have to be considered and if applied any additional filtering circuits. Still, the current sense transformer based concept mostly relies on passive components and thereby beneficially saves a higher power demand.

Besides expecting an improved sensing performance and lower power consumption, this concepts also features galvanic isolation from mains voltage, which is a distinct advantage over the other REV-RX concepts justifying higher hardware effort like a bigger footprint area and increased costs. Additional information on current sense transformers including design challenges, bandwidth considerations, error assessments and experimental validation of transformer modeling are provided in common literature, such as [61], [91], [187], [261].

3.4.3.4 REV-RX Decoding Software

As the DLT backward transmission concept has been developed in the same style as the existing FW transmission, its evaluating frame decoder routine appears similar to the ones presented in Fig. 3.20 of section 3.2.2.4 and in publication [235]. Assigning detected edges of a received REV modulation signal to consecutive half-bit sequences, the frame decoder evaluates the recorded frame to one of the five pre-defined structures shown in Fig. 3.6. Fig. 3.48 illustrates the corresponding flowchart of the implemented software for frame decoding of the REV-RXs, which has already been introduced in [243].

If an edge occurs, the time difference to the previous edge is computed. Therefore, the first edge of a new frame always has to be ignored. By different window comparators the decoder distinguishes between an SoT frame and the

other possible bit sequences [106], [235], [243]. If the last half-bit is *"zero"*, it is not followed by another edge and thus cannot be detected by the receiver. For this reason, it is automatically attached to the decoded frame in the end, if the received data is one half-bit short. The decoder software includes an error detection, e.g. if none of the specified time intervals are met.

Except for the digital matched filter all REV-RX circuits share the same software decoder as depicted in Fig. 3.48 because all of them rely on edge detection and reconstruct the data signal of a single frame in the same manner. The digital matched filter on the contrary operates completely different. It directly determines the transmitted frame sequence by its correlation function without distinctively reconstructing the original data signal or measuring any

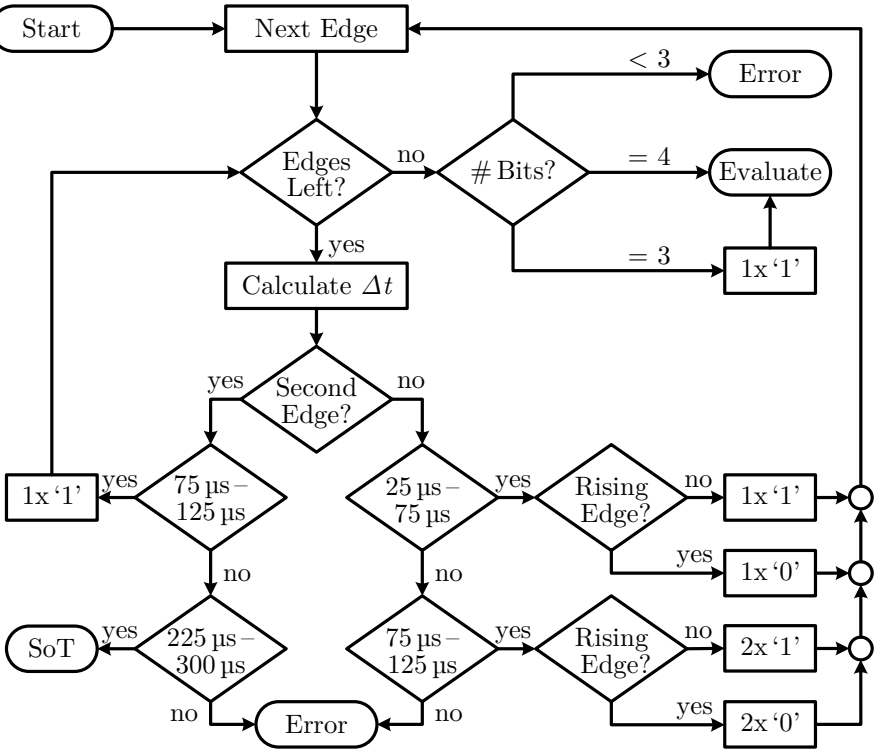


Figure 3.48: Flowchart of the implemented frame decoding software for all REV-RXs in DLT backward transmission.

time differences between occurring edges. Thereby, a dedicated frame decoder is not required for this particular concept. Nevertheless, all REV-RX concepts subsequently use the same telegram evaluation routine, which is identical to the one of the DLT FW modulation shown in Fig. 3.21 as no additional telegram types have been defined for DLT REV transmission yet. Due to the limited processing power of the main MCU, which operates only at 2 MHz clock frequency for power saving reasons, the telegram evaluation cannot directly be conducted because the DLT CD is already busy with timing critical tasks during the data period. Still, it is possible to run the simple frame decoder routine as illustrated in Fig. 3.48, which is hence done for the two analog concepts A and C. Because of their intensive computation demands, the two digitally based concepts are executed at a later point of time, namely during the DLT operating period in the next half-wave of mains. Since the main μC is mostly idle during this phase, it has enough time and resources to perform the digital filtering. Thus, also the telegram evaluation processing previously recorded frames according to the flowchart depicted in Fig. 3.21 is carried out during that period. In every case, the data processing needs to be finished in about 5 ms after the operating period has begun, as the transition to a new data period then happens, which includes again timing sensitive functions. While this distinct timing limit is not a major problem for concept A and C, which only rely on the telegram evaluation in that time period, it may however become rather precarious for the digital filters due to their high computation effort. Both digital filters have therefore been designed in a way to fit this boundary condition as a hard requirement.

3.4.4 Performance Evaluation and Comparison of REV-RXs for Bidirectional DLT Communication

The REV-RXs handling DLT I-MOD can be compared and evaluated in a similar manner as the FW-RX circuits for DLT V-MOD. Circuit complexity, power consumption and achieved robustness hence are again the most relevant performance criteria. Particularly, the determined minimum modulation depth $I_{mod,set}$ as well as the recorded TER in 24 h longterm measurements thereby represent crucial performance metrics for the backward transmission. Fig. 3.49 illustrates the hardware setup that is used for validation and performance evaluation of these conducted tests. FW-RXs and REV-RXs are highlighted within CG and CD, respectively.

CD and CGs are connected according to the wiring depicted in Fig. 3.1. To verify the described REV-RX concepts in a typical lighting environment including noisy distortions emitted by other devices, such as power supply units,

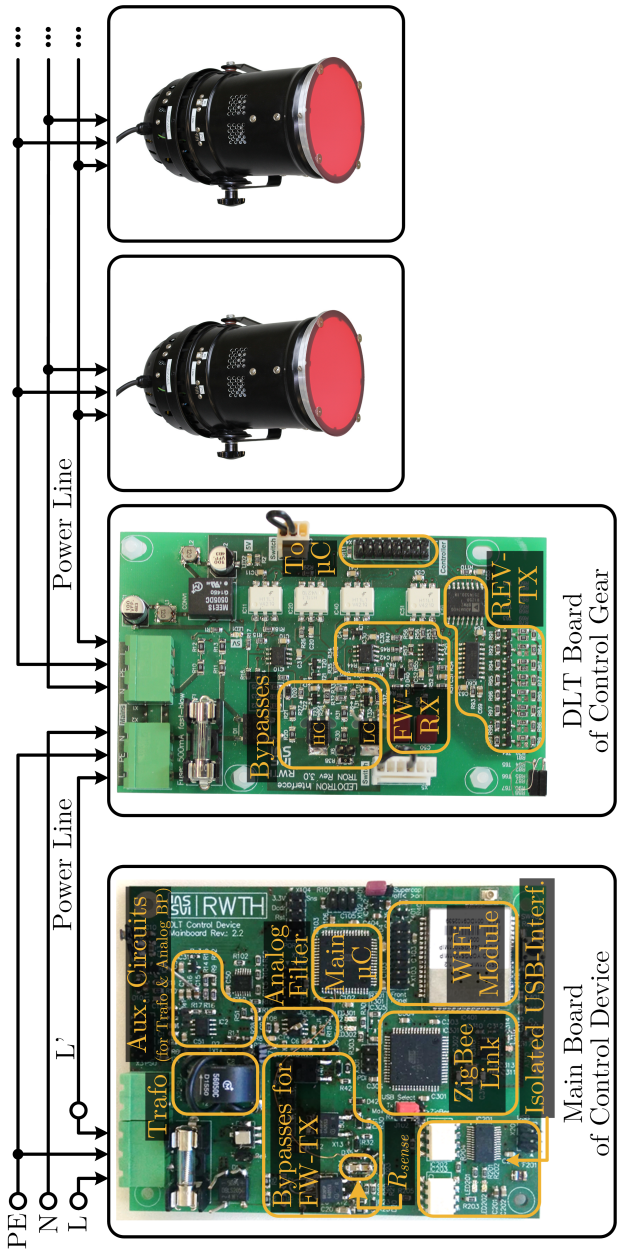


Figure 3.49: Measurement setup of implemented CD and CGs for bidirectional DLT communication.

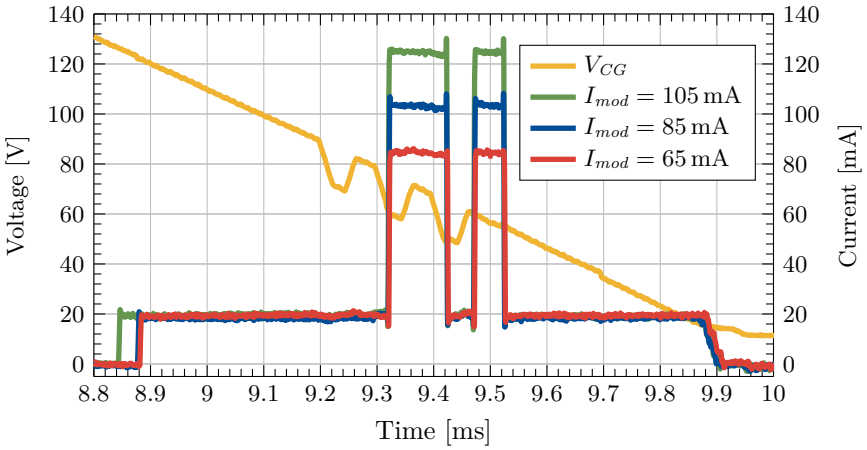


Figure 3.50: Measurement of V_{grid} and I_{byp} at the input of a DLT CG.

the DLT board of the CG depicted in Fig. 3.49 is connected in parallel to two fully functional DLT luminaires, which only contain a FW-RX each on its DLT board. Each of these self-constructed spotlight demonstrators employs an active PFC circuitry and is capable of drawing a power consumption of up to 120 W for supplying the LED driving circuitry. Hence, the demonstrators are a strong distortion to the parallel-connected DLT REV-TX. All measurements have been conducted with the devices under test being connected to real mains voltage of the European utility grid with $V_{grid,RMS} = 230\,\text{V}$ and $f_{grid} = 50\,\text{Hz}$ in a noisy laboratory environment. The CD has been powered by supply concept *A* presented in section 3.3.3 to generate the 3.3 V power supply. Additionally, a 9 V boost converter has been installed, which provides the gate drive voltage for the bypass MOSFETs in the CD. More information on the 9 V power supply is presented in [97], whereas the complete DLT CD implementation including bypass MOSFETs and start-up circuits is explained in [240].

Fig. 3.50 shows the voltage generated by the FW-TX and several frames of the backward transmission for different current modulation amplitudes $I_{mod,set}$. The REV-TX works very well and generates sharp current pulses as desired. The selected levels of $I_{mod,set} = 65\,\text{mA}$, 85 mA and 105 mA are clearly recognizable. If I_{mod} equals zero, the REV-TX still provides the low current flow I_{min} needed for DLT FW transmission. The current modulations depicted in Fig. 3.50 have been adjusted to appear at the same point of time. However, in the measurements the frames from different half-waves do not (need to) sync and

hence occur at different timing positions with reference to mains within the data period. This is identical to the DLT FW modulation because the start point of modulation is not explicitly specified by the DLT standard.

Robustness

The robustness of the REV transmission is evaluated in a similar manner as for DLT FW modulation by determining the respective TER in 24 h longterm measurements for each of the proposed REV-RX concepts. In the presented setup, the FW-TX transmits brightness data continuously to the CG, which uses a passive analog bandpass (BP) filter as its FW-RX. Circuit schematics and component dimensioning of this FW-RX are provided in the appendix (Fig. A.4). The passive analog BP was used as a benchmark concept for the DLT FW-RX evaluation conducted in section 3.2.3. However, the used component sizes would be too big for an ASIC integration. The corresponding FW-RX concept of the passive analog BP also founds an edge detection and utilizes the identical evaluation routine as the active one of FW-RX concept *A*. In case of using the passive analog BP, an additional inversion compared to the active BP filter is however first required, which can easily be performed by the μC [305].

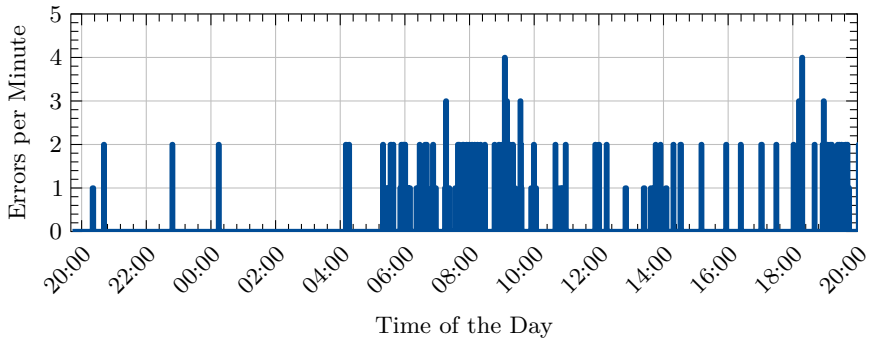
Once the passive FW-RX in the CG obtained the DLT brightness data, the REV-TX continuously sends the detected brightness values back to the CD using identical structure as the FW transmission. In compliance to the FW-RX evaluation presented in section 3.2.3 the TER is determined this time for both FW and REV transmission recorded by the FW-RX and REV-RX circuits, respectively. In both cases, the respective μCs measure again the number of recorded and valid telegrams to evaluate the corresponding TER. Beyond that, the μCs simultaneously meter the elapsed time from the start point of the 24 h longterm measurement. Knowing the length of a typical brightness telegram, which lasts about $t_{Tel,B} = 80\,\text{ms}$ for the investigated European utility grid, it is thereby possible to approximate the number of telegrams that are additionally lost during transmission. Compared to the DLT FW-RX evaluation, this provides a more detailed evaluation of both transmission directions. The constant brightness value $B = 228$ has been chosen for continuous transmission since it contains all five possible frame sequences according to Fig. 3.6 in chapter 3.1.2. For the same reasoning, $B = 147$ represents another suitable brightness value for the robustness tests as used in [243] and [97]. In this work, $B = 228$ has been selected because it accounts for a higher power draw of attached CGs, which results in noisier distortions that are furthermore more likely to happen more often. Hence, the higher brightness value provides a more worst-case scenario for the conducted robustness measurements.

Table 3.13: Measured robustness and sensitivity for each REV-RX concept under evaluation.

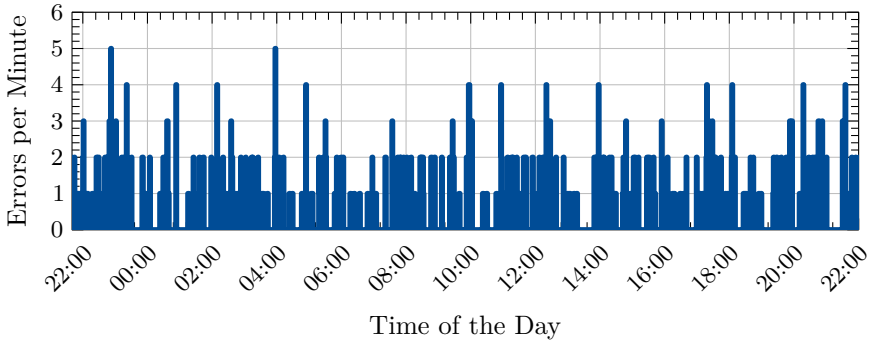
	Concept *A*: Analog BP	**Concept *B*: Matched Filter**	**Concept *C*: Transformer**
$I_{mod,set}$	45 mA	28 mA	10 mA
TER of I-MOD	114 ppm	322 ppm	5 ppm
TER_{Losts} of I-MOD	298 ppm	532 ppm	10 ppm
TER of V-MOD	120 ppm	158 ppm	146 ppm
TER_{Losts} of V-MOD	427 ppm	531 ppm	878 ppm

As outlined in section 3.4.1, the employed modulation depths $I_{mod,set}$ directly influences achievable TER for each REV-RX concept, while it also influences overall power consumption associated with the I-MOD for DLT REV transmission. Balancing both performance indicators, this thesis assumes a maximum acceptable error rate for DLT REV transmission of less then 1 %. This value should still provide decent comfort and user acceptance in a final target implementation. Furthermore, it represents a challenging low level for the REV-RX concepts, which results in different needs of the minimum used modulation depth $I_{mod,set}$. Thereby, the determined modulation depth $I_{mod,set}$ somehow indicates the sensitivity of the respective REV-RX and additionally provides the measured current level for power consumption calculations presented in the subsequent section.

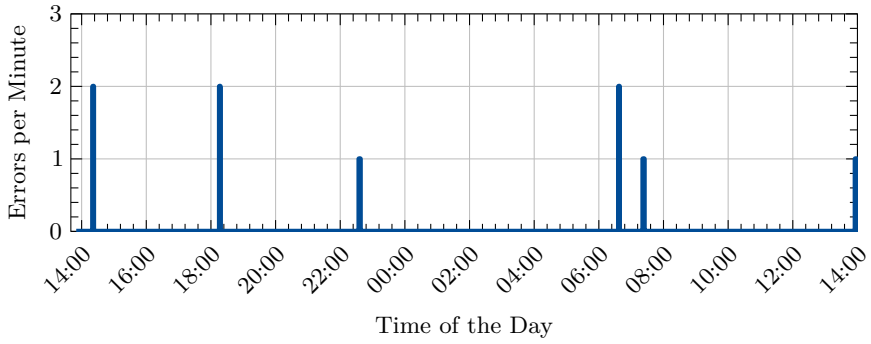
Table 3.13 thus lists the achieved modulation depths $I_{mod,set}$ that have been determined during the robustness experiments in addition to the measured TERs. As mentioned earlier, Table 3.13 additionally computes TERs including the estimated number of lost telegrams. Since some time is required for assembling and evaluating the received telegrams, this value might yet be estimated as too high. Beyond that, Fig. 3.51 illustrates the measured number of errors per minute for each REV-RX concept, which allows to deduct a maximum instantaneous error rate correspondingly, which is below $TER_{inst,max} < 0.67\,\%/\text{min}$ in all cases. It should be noted that the digital BP of REV-RX concept *B* has not been evaluated in the robustness measurements because it showed a much worse performance compared to the digital matched filter of REV-RX concept *B*, while both implementations feature comparable hardware effort and power consumption as can be seen in the subsequent sections. The robustness and sensitivity for the digital BP based approach may however be evaluated by



(a) Recorded telegram errors of DLT REV-RX concept *A*.



(b) Recorded telegram errors of DLT REV-RX concept *B*.



(c) Recorded telegram errors of DLT REV-RX concept *C*.

Figure 3.51: Recorded telegram errors per minute of different DLT REV-RX concepts under evaluation in 24 h longterm measurement.

taking the results from [97] and [243] into account. In these studies, a modulation depth $I_{mod,set}$ of 65 mA was used to achieve TERs of about 0.45 % and 0.52 %, respectively. According to the acceptable 1 % limit, the achieved error rates would be sufficient but still are more than one decade higher compared to the other concepts evaluated in this work as can be seen from Table 3.13. It is further shown in [243] that a significantly higher modulation depth of at least $I_{mod,set} = 105$ mA would be required to achieve comparable TER results in a lower three digit ppm range. This value is however not acceptable in terms of power consumption, while the original 65 mA are already way beyond the modulation depths used for the other REV-RX concepts.

Evaluating the results from the 24 h longterm measurements, it is found that the transformer based concept performs best in terms of sensitivity and robustness since it features the lowest possible modulation depth $I_{mod,set}$ of only 10 mA and simultaneously records nearly zero errors over the entire measurement time. REV-RX concept *A* also shows a low TER of about 114 ppm, which is comparable to that of DLT FW modulation. However, this analog BP based circuit requires a modulation depth of at least $I_{mod,set} = 45$ mA and hence shows worse sensitivity. Increasing the modulation depth to higher values did not yield better TER results, while lowering $I_{mod,set}$ yields much higher error rates exceeding the acceptable 1 % limit. The digital matched filter employed as REV-RX concept *B* achieved acceptable results in terms of TER using a modulation amplitude of $I_{mod,set} = 28$ mA. Investigating the instantaneous error rates depicted in Fig. 3.13, it strikes however that this concept suffers from a constant error occurrence over the entire measurement time, while the other two concepts show (nearly) no errors during the night time. Several further 24 h longterm measurements were therefore taken employing the digital matched filter based concept and using modulation depths of 25 mA and 30 mA. The corresponding error rate plots can be found in appendix A.5 of this work (Fig. A.12). In case of setting $I_{mod,set}$ to 25 mA a TER of 0.30 % is achieved, which is similar to the digital bandpass implementation of concept *B*. Using a higher modulation depth of $I_{mod,set} = 30$ mA TER goes down to 282 ppm. The transisent behavior of the corresponding instantaneous error rates remains however similar in both cases compared to the one demonstrated in Fig. 3.51b.

Considering the current draw limitation depicted in Fig. 3.41 according to the DLT standard [106] only REV-RX concept *C* and the digital matched filter of concept *B* are capable of staying below these specified limits for the 40 W load case if no active PFC is applied in attached CGs. Adding the DLT LC flow of $I_{LC} = 18$ mA to the respective modulation amplitudes of $I_{mod,set} = 10$ mA and $I_{mod,set} = 28$ mA yields a value less than the worst case approximation of $I_{CG,40W,WC} = 48.15$ mA. The analog and digital bandpass

REV-RX architectures consequently exceed this limited with their modulation amplitudes of $I_{mod,set} = 45\,\text{mA}$ and $I_{mod,set} = 65\,\text{mA}$, respectively.

The measured TERs for DLT FW transmission of the V-MOD are similar to each other for all REV-RX concepts under evaluation using different modulation depths. Compared to the results in section 3.2.3 the TER has slightly gone up but still remains in a low ppm range. The increase in faulty telegrams is probably more attributed to the higher power draw and associated noise floor of the additionally connected spotlight luminaire and higher brightness value than to the DLT REV transmission. Nevertheless, the presence of the distinct current pulses might apparently also effect the FW transmission slightly. In conclusion, the TER of the employed FW-RX still remains in a more than acceptable range featuring results of about 100 ppm to 160 ppm. This proves robustness and feasibility of the proposed bidirectional DLT communication.

Power Consumption

Enabling bidirectional DLT communication obviously comes at the cost of an increased overall power consumption. In fact, two main contributions have been identified for each REV-RX concept, which are first the power consumption of the REV-RX circuit itself and second the REV transmission energy that depends on the required minimum value of the backward modulation amplitude I_{mod}.

The additional power consumption for each REV-RX concept is determined by measuring the current draw of the entire CD with and without the respective REV-RX circuit being connected. In order to individually disconnect the different concepts, the implemented test board foresees several jumpers that can be closed or left open. During these tests a constant 3.3 V DC supply [368] is used to power the DLT CD, while an ideal AC source [386], which provides galvanic isolation, synthesizes mains voltage. Thereby, precise current draw measurements can be conducted with the applied DC supply source [368]. The CD continuously operates in its active mode providing the V-MOD for DLT FW transmission to two spotlight luminaires with a rated nominal power of 120 W connected as the main load as depicted in Fig. 3.49. Table 3.14 summarizes the measured current draw of each REV-RX concept as well as the power consumption calculations with respect to the applied 3.3 V supply. $P_{REV\text{-}RX}$ herein denotes the difference to the case, when no REV-RX circuit is installed in the CD. Thereby, this column effectively computes the additional amount of power that is needed for running the respective REV-RX concept.

The additional transmission energy caused by the current flow I_{mod} of the REV-TX circuits represents the second main impact on power consumption of the presented DLT backward transmission concept. In fact, this portion can

Table 3.14: Measured current draw of the DLT CD and associated power consumption for each REV-RX concept.

REV-RX concept		$I_{CD,active}$	$P_{CD,active}$	$P_{REV\text{-}RX}$
	No REV-RX	2.52 mA	8.32 mW	
Concept A:	Analog BP Filter	11.815 mA	38.99 mW	30.67 mW
Concept B_1:	Digital BP Filter	7.99 mA	26.37 mW	18.05 mW
Concept B_2:	Digital Matched Filter	8.435 mA	27.84 mW	19.52 mW
Concept C:	Transformer	7.51 mA	24.78 mW	16.47 mW

simply be calculated by considering the maximum modulation depth $I_{mod,set}$ required for each REV-RX concept as well as the corresponding voltage level of mains being present during the time of the REV transmission. The power consumption of the REV-TX circuit itself is actually negligible because it uses the existing LC-bypass and the energy for switching the additional modulation transistors is rather low. In order to perform a worst-case consideration, the earliest possible point of time for DLT backward transmission is taken into account as mains voltage shows the highest voltage level at this moment during DLT data period. Following the DLT specification [106], this timing is the beginning of the data modulation $t_7 = 800\,\mu s$ before the next zero crossing of mains. The additional power consumption resulting from the modulating REV-TX hence computes to

$$P_{REV\text{-}TX} = \frac{1}{T_{grid}} \int_{t_7}^{t_7+T_{frame}} \left| \widehat{V}_{grid} \cdot \sin(2\pi \cdot f_{grid} \cdot t) \cdot I_{mod} \right| dt \qquad (3.40)$$

$$= \frac{1}{T_{grid}} \int_{9.2\,\mathrm{ms}}^{9.45\,\mathrm{ms}} \left| \widehat{V}_{grid} \cdot \sin(2\pi \cdot f_{grid} \cdot t) \cdot I_{mod} \right| dt, \qquad (3.41)$$

in dependence of the transient behavior of the I-MOD. To compute the average power consumption, the respective current-voltage product needs to be integrated in the specified time period and is subsequently divided by one period of mains (*here:* $T_{grid} = \frac{1}{f_{grid}} = 10\,\mathrm{ms}$). The additional power consumption computed by equation 3.40 therefore strongly relates to the chosen modulation depth $I_{mod,set}$ as well as the transmitted payload data. Amongst the five possible frame assemblies, the SoT-frame features highest conceivable power

consumption. The modulation current I_{mod} is set to its high level $I_{mod,set}$ during the entire transmission time in this case, whereas it always shows a low current level for the length of two half-bits in the other four frame constellations. Considering only transmissions of SoT-frames in combination with the earliest transmission point of time hence gives an absolute worst-case approximation of the additional power consumption needed for DLT backward transmission. Because the SoT-frame is only send once per DLT telegram, more detailed calculations taking the distribution probability of the five different frame sequences into account would hence give a more realistic approximation. Table 3.15 therefore calculates the power consumption for both scenarios, a worst-case approximation and a realistic frame distribution probability. A best-case scenario for the latest possible transmission at $t_{REV\text{-}TX,start} = 550\,\mu s$ before the next zero crossing is also being considered. The detailed computations for the realistic scenario found on equation 3.40 and are provided in appendix A.6 of this work (equation A.16). Still, the transmission energy needed for an SoT-frame is an indirect measure for the power efficiency of the respective REV-RX concept and is thus also shown in Table 3.15 for all cases.

As mentioned earlier, the chosen modulation depth $I_{mod,set}$ strongly depends on the REV-RX under evaluation as it needs to be selected as a trade-off between power consumption and achievable TER for good robustness. Assuming a maximum acceptable error rate of 1 %, the conducted robustness experiments presented in the previous section determined the respective modulation depths that are taken into account for the power consumption calculations. If a better SNR and hence lower TER is desired, the power consumption of the proposed concepts would go up accordingly. It is still expected that the differences among the REV-RXs will remain in a similar relative range. Additionally, Table 3.15 computes the total power consumption that is needed for DLT REV transmission in a realistic case by including the results presented in Table 3.14.

The computed SoT transmission energies of the different REV-RX concepts obviously scale with the respective modulations depths due to the linear relationship denoted in equation 3.40. The digital BP filter therefore shows the highest energy demand, followed by the analog BP and the digital matched filter, whereas the transformer based approach of concept *C* yields the lowest SoT energy of $E_{REV\text{-}TX,SoT,real} \approx 139.8\,\mu W\,s$. The average power consumption needed for the backward transmission consequently follows the same order. Investigating the measured power consumptions of the individual RX circuits in the DLT CD draw a slightly different picture. The analog RX concept features by far the highest consumption, which is nearly double the amount of the transformer concept. The two digital filters consume very comparable amounts of power with a slight advantage for the BP-based approach and the

Table 3.15: Calculated power consumption for each REV-RX concept.

	Concept A: Analog BP	Concept B_1: Digital BP	Concept B_2: Matched Filter	Concept C Transformer
$\boldsymbol{I_{mod,set}}$	45 mA	65 mA	28 mA	10 mA
$\boldsymbol{E}_{REV\text{-}TX,SoT,WC}$	770.0 µW s	1.11 mW s	479.1 µW s	171.1 µW s
$\boldsymbol{E}_{REV\text{-}TX,SoT,BC}$	487.0 µW s	703.4 µW s	303.0 µW s	108.2 µW s
$\boldsymbol{E}_{REV\text{-}TX,SoT,real}$	629.0 µW s	908.5 µW s	391.4 µW s	139.8 µW s
$\boldsymbol{P}_{REV\text{-}TX,WC,max}$	77.0 mW	111.2 mW	47.9 mW	17.1 mW
$\boldsymbol{P}_{REV\text{-}TX,WC,mean}$	51.0 mW	73.7 mW	31.8 mW	11.3 mW
$\boldsymbol{P}_{REV\text{-}TX,BC,max}$	48.7 mW	70.3 mW	30.3 mW	10.8 mW
$\boldsymbol{P}_{REV\text{-}TX,BC,mean}$	32.7 mW	47.2 mW	20.3 mW	7.3 mW
$\boldsymbol{P}_{REV\text{-}RX}$	30.67 mW	18.05 mW	19.52 mW	16.47 mW
$\boldsymbol{P}_{REV\text{-}TX,real,mean}$	41.9 mW	60.5 mW	26.1 mW	9.3 mW
$\boldsymbol{P}_{REV,total,real}$	72.57 mW	78.55 mW	45.62 mW	25.77 mW

transformer based concept C is again the most economical Evaluating the total power consumptions, concepts A and B_1 provide comparable results, which are both however greater than 72 mW and hence higher than the targeted value of 50 mW. The digital matched filter and the transformer based RX show on the contrary lower power consumptions compared to this target value and are hence well suited for application in bidirectional DLT communication systems. Particularly concept C is interesting in this regard as it not only performs best but also consumes only about half of the energy needed for concept B_2, which represents the second best approach.

Circuit Complexity

Comparing circuit complexity for the different REV-RXs concepts can be performed similarly to the evaluation of DLT FW modulation by taking used COTS components, necessary implementation effort (also with respect to an ASIC solution) and costs into account. Although an ASIC realization of a DLT CD has not been specified as a major aim, it might still represent an interesting idea considering the amount of functionality that could be included in such a design. Besides the investigated REV-RX circuits this includes the relevant parts necessary for DLT V-MOD as well as proper power supply controllers like the ones outlined in section 3.3.

The two digital solutions summarized as concept B represent the most advantageous approaches in terms of hardware effort, since they only rely on components that would be needed anyway for a DLT CD implementation. These circuits components are a small sensing resistor and an ADC including an internal gain stage for adaption of the sensing voltage to its full-scale range. The internal comparator needed for the overcurrent protection of the CD and the ADC share the same pin on the MCU, which supersedes any rewiring of the CD's PCB. Other digital filter concepts with an improved filtering performance and characteristics can easily be applied within this setup because they would only require a suitable firmware or software update.However, in regard to an ASIC solution, the circuit complexity increases to a medium level similar to the digital DLT FW-RX concepts because of the design effort associated with implementing the ADC and a suitable analog gain stage.

The analog REV-RX proposed as concept A in section 3.4.3.1 features a medium complexity for an implementation with COTS components. The hardware effort can be estimated based on the given schematics to two opamps, a couple of resistors and capacitors as well as a downstream connected Schmitt-Trigger. The circuit complexity of the analog REV-RX concept A consequently behaves inversely compared to the digital approaches of concept B. Considering an ASIC implementation for the entire DLT CD its design effort may actually be evaluated as low level complexity. Comparing concepts A and B a slight advantage for the digital solutions remains due to the inherent flexibility coming from their adaptability by simple software or firmware updates.

The transformer based approach of REV-RX concept C features highest circuit complexity due to using a bulky current sense transformer. Beyond that, the bias voltage generation and possible further analog filtering require additional opamps and passive components. Although the available ADC of the MCU could be used instead of the common voltage regulator as it is capable of sensing negative input voltages, overall complexity of REV-RX concept C stays at a (very) high level. This high implementation efforts are only acceptable, if the transformer based concept proves significant better robustness in terms of recorded TER and required modulation depth $I_{mod,set}$ or if galvanic isolation is a demanded requirement, e.g. for a possible ASIC solution.

3.5 Assessment of the Developed DLT System in Relation to Other Communication Techniques

The detailed studies, in-depth analysis and thorough investigations that have been conducted throughout chapter 3 proved that the DLT communication

methodology is more than suitable for intelligent lighting control applications. Moreover, the proposed improvements generate additional value in terms of flexibility, energy-efficiency and system intelligence. While featuring many beneficial advantages, DLT also suffers from two distinct drawbacks, which are first a comparatively low data rate and second the unidirectional communication capability. Concerning data rate, the literature review on different communication approaches in section 2.1 revealed that only a few dozen of bytes per second are required for lighting controls and smart home automation systems [97], [196]. Furthermore, digitalSTROM™ [101] has already proven the applicability of a low data rate communication method for effective usage in a smart home automation environment by employing transmission speeds of 200 bit/s. Besides lighting, DLT may consequently be applied to controlling other low data rate applications in a smart home, such as heating and cooling, roller blinds, fire alarms, light guidance or presence and occupancy detection. On the contrary, high data rate services, such as audio and video feeds, can obviously not be supported by DLT and will require the installation of another (sub)system. The low data rate is in conclusion a weakness regarding high data rate services, which is yet not the primary task of a home automation system. Due to the excellent robustness of the DLT approach, the low data rate is not expected to affect latency in a crucial manner. The limitation of a unidirectional communication on the other hand is indeed a major deficiency, if DLT is targeted for deployment as a full home automation system like digitalSTROM™. This issue has been overcome by the proposed concepts in [97], [243] and those in section 3.4 of this thesis. Although these solutions leave some room for further enhancements in future studies, the gained insights and measured system performance are a sound basis for evaluating the improved DLT system in reference to other communication methods.

As mentioned earlier, a direct comparison of the DLT methodology to other communication systems is difficult or moreover not really possible because DLT operates for example completely different than wireless techniques. Beyond that, versatile boundary conditions are applied for the diverse communication methods in various application scenarios and use cases. Nevertheless, the literature review in section 2.1 identified four specific benchmark systems to asses and evaluate the DLT methodology by rough ballpark figures in terms of power consumption, robustness and complexity. These benchmark technologies are the resembling digitalSTROM™ approach as well as the three wireless techniques WiFi, ZigBee and Bluetooth (LE). Further interesting performance metrics, like coverable range, maintenance, ease of use and security, have been evaluated as sufficient for lighting control among the systems under test and are thus not considered in following discussions.

Circuit and System Complexity

Circuit and system complexity of the DLT technology are relatively low due to its simple modulation scheme, the unidirectional communication capability and its PLC origin. Even when using the extension of a bidirectional communication approach, overall complexity remains low. In fact, digitalSTROM™ shows a very similar complexity level except for its upstream communication, which employs the more advanced Spread-FSK modulation technique compared to a simple OOK. Because the digitalSTROM™ methodology provides certain additional features due to its network topology, such as the connection to the internet via a backbone server structure or the interconnection of several dSMs over an RS-485 line on the distribution board, complexity is a bit higher and evaluated to a medium level. If DLT is aimed to operate in the same manner and topology, the complexity degree would of course result in a similar range. Although it is generally conceivable to apply a similar network topology to DLT, with multiple CDs installed on the distribution board, the original installation method is meant to substitute conventional switches, dimmers and lamps in a retrofit manner. DLT thereby avoids elaborate setups and wiring effort on the distribution board and minimizes overall complexity. Moreover, the novel power supply concepts for DLT CDs developed in chapter 3.3 of this thesis provide the opportunity to connect each individual DLT controlled entity (one CD with multiple CGs attached) over a wireless uplink, such as ZigBee, Bluetooth or WiFi, to any server backbone structure or directly to the internet. This setup consequently requires to use DLT as a subsystem in combination with another smart home automation system. All of the wireless communication techniques suffer indeed from a higher degree of complexity as they use sophisticated protocol stacks, more advanced modulation schemes and have to employ corresponding circuits and chip sets. Furthermore, wireless communications have to use costly noise cancellation techniques and appropriate circuits with tight tolerances as already outlined in detail in section 2.1.3. Amongst the wireless methods, WiFi requires the highest complexity, whereas BLE and ZigBee are comparable to one another with respect to this measure.

Robustness

Robustness behaves indeed quite similar to complexity among the different systems under test. Due to being a wire-bound PLC method, DLT is – likewise as digitalSTROM™ – very robust. It is capable of coping with strong distortions emitted by discrete interferers, such as SMPS loads. Robustness has thus been evaluated as excellent in several 24 h long-term measurements. The measured telegram error rates (TERs) determined in this thesis showed maximum error

rates below 88 ppm and 322 ppm for forward and reverse communication direction, respectively. Depending on the used detector concept these values could be even much lower, e.g. 44 ppm for forward transmission and only 5 ppm for the reverse channel. The achieved error rates are hence far below the targeted 1 % limit. These outstanding achievements originate from the simplicity of the modulation schemes in conjunction with sufficiently high modulation amplitudes and the well-designed receiver circuits providing good sensitivity.

For digitalSTROM™ there are unfortunately no exact numbers available but Dickmann [101] reports very high reliability of this system with zero detected errors in short term observations and measurements. Wireless communication techniques are however affected from interference among each other. Chapter 2.1.3 described the involved implications in detail and lists corresponding research studies. Robustness of the wireless communication techniques may hence be decreased, particularly if two different communication methods use adjacent transmission channels or even experience a channel overlap. Also, if any interferer is present in close proximity (≤ 0.5 m) of the used wireless device, reliability may be affected significantly. Due to the wide deployment of WiFi, ZigBee and Bluetooth, interference between these systems or other discrete interferers is likely to happen. As a result, latency and power consumption might be increased and the coverage range could be reduced. This kind of behavior was exemplarily observed, when testing the self-developed luminaires, which are presented in appendix section C. of this thesis, with direct control over DLT, WiFi and ZigBee communication in a lecture hall as a presentation to an audience of many students. While the DLT approach showed strong robustness and good functional performance, the aforementioned related effects were perceivable for the wireless communications. It could e.g. be seen that the range of the wireless systems decreased significantly, whereas its latency increased simultaneously to perceivable levels, probably because of multiple interfering devices, such as the smart phones of the students. Nevertheless, the high data rates of the wireless communication systems are expected to compensate for latency effects in most use cases so that an end user will not be able to notice when controlling luminaires or the home automation system. Some critical application scenarios might still exist, in which the reliability target of 98 % may not be achieved, especially for the wireless communication approaches. These use cases are however rare, only represent a minority and are hence irrelevant. The robustness target is thus achievable within all systems under test for most use cases that are relevant in a smart home environment. Good robustness in conjunction with ease of use is actually the reason, why wireless communication systems like Bluetooth, WiFi and ZigBee have found a broad acceptance and deployment in the market. In conclusion, WiFi, ZigBee

and Bluetooth achieve good robustness fulfilling the demanded requirements but perform a little bit worse compared to DLT or digitalSTROM™.

Power Consumption

Although the robustness and complexity evaluations highlight the superiority of DLT and digitalSTROM™ in both categories compared to WiFi, ZigBee and Bluetooth, a very important performance metric remains to be investigated, which is the power consumption of the entire system. The power consumption figures of the benchmark systems are taken from the thorough evaluation presented in section 2.1.3. At first glance, it appears that DLT also achieves the lowest power consumption when comparing TX and RX consumptions for FW- and REV-communication listed in tables 3.5 and 3.15, respectively, with the benchmark values stated in table 2.1. The best DLT FW-RX needs between 6.5 mW to 37.72 mW, which is lower than all wireless benchmark ICs itemized in table 2.1. For the REV transmission this figure of merit looks even better, as the best concept only consumes 25.77 mW combined for RX and TX actions together. However, the wireless transceivers feature much higher data rates of about 0.25 Mbit/s to 1 Mbit/s compared to 200 bit/s of the DLT methodology. In addition to that, the different communication methods require further consumptions on system level that are related to overall TX and RX performance. Certainly, several measures can be taken to reduce the average system power consumption for all communication methodologies under test and also required standby power is an important aspect, which needs to be considered. Therefore, some further analysis on system level is conducted in the following, with emphasis on the DLT approach.

The official DLT standard [106] demands a compulsory current flow during supply and data period of at least $I_{CG,LC,min} = 18\,\mathrm{mA}$. In order to perform a worst-case approximation of the V-MOD for DLT FW-RX and FW-TX, the full voltage drop of mains is assumed to be present at the CG, although some portion is dropping over the CD depending on its on-resistance and transmitted payload data. By this means, the computed total power contains both parts of required transmission and receiving energy as shown in the subsequent equation,

$$P_{FW\text{-}TRX} = \frac{1}{T_{grid}} \int_{t_6}^{t_9 = T_{grid}} \left| \widehat{V}_{grid} \cdot \sin(2\pi \cdot f_{grid} \cdot t) \cdot I_{CG,LC} \right| dt\,, \tag{3.42}$$

$$= \frac{1}{10\,\mathrm{ms}} \int_{8.8\,\mathrm{ms}}^{10\,\mathrm{ms}} \left| \sqrt{2} \cdot 230\,\mathrm{V} \cdot \sin(2\pi \cdot 50\,\mathrm{Hz} \cdot t) \cdot 18\,\mathrm{mA} \right| dt \approx 130.9\,\mathrm{mW}.$$

Since the DLT standard [106] only demands the required minimum current flow for one entire subsystem (one CD plus attached CGs), it can be thought of an intelligent bypass structure to save power consumption on system level and keep it at this minimum level. It is e.g. possible that only one main CG enables the necessary bypass circuits, while other connected CGs only use their DLT FW detector and decoder circuits as well as the required auxiliary circuits like ZCD, V_{SW}–detector and the common rectifier. This conceivable application scenario could be realized by either equipping CGs with different hardware setups and differentiate between a full function CG and reduced function CGs or it could also be implemented by using the proposed bidirectional communication approach. In the latter case it might even be possible to precisely regulate the overall drawn bypass current needed for DLT communication since connected CGs and the CD may negotiate, how much power draw is demanded or who is conducting how much current similar to recent developments in universal serial bus (USB) 3.0 power delivery (PD) [385]. Thereby, it might even be possible to optimize connected loads regarding aging effects by applying current balancing and hence increase lifetime. Using an appropriate supply circuit, it is considered that the demanded current flow of $I_{CG,LC,min} = 18\,\text{mA}$ is by far sufficient for powering any auxiliary circuitry in a DLT FW-RX and for covering switching losses for the modulation, which is both proven by the hardware implementations presented in this thesis. To account for a certain safety margin, the total bypass current draw is still assumed to be a little bit higher. Taking $I_{CG,LC} = 21\,\text{mA}$ into account, the worst-case approximation yields a a total average power consumption of $P_{FW\text{-}TRX} \approx 152.7\,\text{mW}$ applying equation 3.42. Additionally, the power for DLT backward transmission as well as the consumption of FW-RXs in dependence of the number of attached CGs has to be taken into account. Equation 3.43 finally sums up the total DLT system consumption needed for communication,

$$P_{DLT,TRX} = P_{FW\text{-}TRX} + P_{REV\text{-}RX} + (n_{CG} - 1) \cdot P_{FW\text{-}RX} + n_{CG} \cdot P_{REV\text{-}TX}\,, \tag{3.43}$$

with n_{CG} being the number of attached DLT CGs. Using equation 3.43 it becomes clear that if only one CG is connected and REV-RX concept C with the transformer is used, the total power consumption would yield $P_{DLT,total} = 152.7\,\text{mW} + 16.47\,\text{mW} + 9.3\,\text{mW} \approx 178.47\,\text{mW}$. This value lies actually in between the approximated minimum consumption range for the basic power consumption of a digitalSTROM™ system of (114 mW to 228 mW). For a complete evaluation of digitalSTROM™, the power consumption of any TX

and RX circuits have to be added but are unfortunately not specified by Dickmann [101]. digitalSTROM™is therefore expected to have in the end a higher power consumption than 228 mW. In addition to the power consumption stated above, the DLT system also requires the LC flow during the supply period, which gives an extra 130.9 mW power consumption on system level yielding a total sum of 309.37 mW for a system with one connected CG. This value is still evaluated in a similar range compared to the digitalSTROM™ approach considering the unknown consumption parts for this system. Because the initial system power demand in a DLT system is comparatively high due to the required current flow during supply and data period, it is very beneficial if multiple CGs are installed. The additional power consumption for each further connected device would indeed be relatively small. The same actually holds true for the digitalSTROM™ approach. In an extended DLT system as developed by this thesis full-duplex mode is supported, which means that CD as well as CG may simultaneously transmit and receive data on FW and REV channel. The same obviously holds true for the digitalSTROM™ system.

A comparison to the wireless communication systems is rather difficult. While it becomes obvious that the entire DLT system consumes less than one WiFi module already needs for its RX action alone, the consumption of ZigBee and BLE on system level strongly depends on the amount of employed nodes in the wireless network. Furthermore, the latter two systems might require an additional WiFi bridge for connection to the internet or a server station. These bridges are typically very power hungry and might consume even several watts [190]. Additionally, and even more important, the DLT computations include all auxiliary circuits and consider that the current is drawn directly from mains voltage. The wireless communication technologies, like WiFi, Bluetooh or ZigBee, on the contrary would always need an additional AC-DC conversion providing the low voltage, which is used in the measured computations stated in table 2.1 from section 2.1.3. This will indeed increase the overall system power consumption depending on the achievable efficiency of the employed AC-DC converter, which needs to be embedded in each wireless node.

If the wireless systems are enabled and do not employ cyclic sleeping, each node in the network consumes at least the denoted RX power consumption plus a certain amount of TX power depending on the amount of data transmissions happening. Therefore power consumption increases significantly with the number of employed network nodes. Considering typical uses cases with five to ten luminaires per room, already very similar power consumption values may be achieved compared to DLT, maybe with a slight advantage for the low power wireless techniques, ZigBee and BLE. Meanwhile the number of used network nodes has however risen significantly due to employing further

distributed sensors, such as light level detectors, occupancy or color sensors. Some power saving options of course exist, such as the aforementioned cyclic sleeping for wireless network nodes. If this technique is applied, it must however be ensured that other requirements, such as latency, are not violated. For the DLT system it can also be thought of a similar power saving method. So far the recent DLT standard [106] requires the low current (LC) to always flow during supply and data period. If the bidirectional communication scheme is applied with some kind of ACK or NACK messages, data does not need to be resend continuously but only when really needed. Thereby, not only the power consumption for transmission can be saved but also the current flow during data period could be reduced or even be turned off completely.

Another important aspect is the power consumed during standby operation, as intelligent luminaires reside most of the time during a day within this state. A detailed study on standby power consumption of different lighting systems has been carried out by Kruse [190], who analyzed the digitalSTROM™ approach as well as several systems based on wireless communication. Section briefly 2.1.3 describes the findings on standby power consumption. Please refer to this paragraph or to the original work [190] for further details. In summary, Kruse [190] measured that power consumption of a single luminaire in standby mode typically lies in the range of several hundred mW (300 mW to 600 mW), whereas gateways even dissipate powers between 1.3 W to 2.3 W. Since DLT CGs are completely disconnected from mains voltage during standby mode, they consume zero power consumption in this case, not only for the communication but at all. Even if the CD resides within *"power controlled off state"* and thus might enable a little current flow from time to time to power itself, the voltage drop over attached CGs is minimal in these times and nearly zero. The CD is consequently the only power consumer when the system is powered down or in standby. For measurement purposes and to determine standby power consumption, a complete DLT system has hence been setup according to the conceptual designs described within this thesis. The corresponding results as well as fundamentals of the CD implementation have been published in [240]. Some circuit schematics are also added in the appendix section A.3 for the sake of completeness. Fig. 3.52 illustrates a photograph of the resulting DLT control device (CD) featuring the improved power supply circuits to provide extended functionality, such as the interoperability with other communication systems and lighting controls via ZigBee or WiFi. The standby power consumption of this advanced CD has been measured during power controlled off state to approximately $P_{CD,stdby} \approx 745\,\text{mW}$ ($S_{CD,stdby} \approx 804\,\text{mV A}$) [240]. This is an excellent result, which outperforms commercially available wireless system as measured by Kruse [190] as well as the digitalSTROM™ approach. Two to three

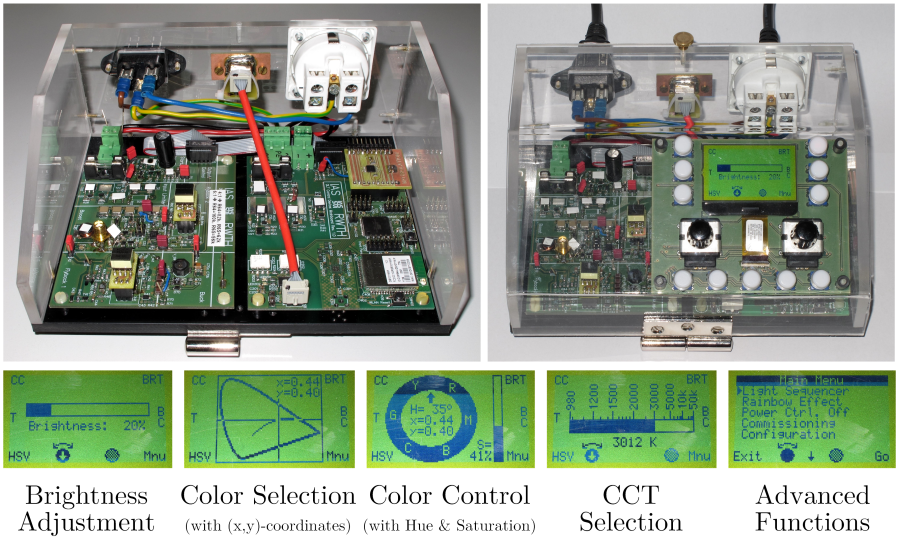


Figure 3.52: Photograph of the implemented DLT CD with efficient power supplies enabling extended functionality and interoperability.

wireless controlled luminaires consume as much power as the entire DLT system during standby mode, which demonstrates the advantages of the DLT method. The additional power dissipation of the CD during DLT modulation equals only $P_{CD,on,mod} \approx 8.3\,\mathrm{mW}$, whereas the loss power in CD and CGs strongly depend on load conditions, particularly the current draw of the intelligent LED luminaires [240]. The DLT system consequently achieves outstanding results and is capable of competing with other lighting control systems.

In conclusion, DLT has been evaluated as a suitable system for lighting control in smart homes, which provides beneficial and attractive features, such as high compatibility to existing installations, easy retrofitting and low complexity, while maintaining high robustness and reliability for an acceptable power consumption. DLT thus represents a good alternative to other (wireless) communication systems. Additionally, several aspects have been highlighted, which leave further room for improvements in future work, such as the protocol stack for bidirectional DLT communication with an optimization on system level or the extensibility to other functions covering tasks of a complete home automation system. Due to the improved system intelligence developed in this thesis, it is possible to combine wireless systems with DLT to use the strength

of the respective communication methods, where exactly needed. The improved DLT system suggested by this thesis is thus assessed as a reliable control system for lighting applications with great performance regarding robustness, complexity and (standby) power consumption.

3.6 Summary and Conclusion of the Improved DLT System Developments

The existing state-of-the-art DLT approach provides very beneficial features for controlling intelligent lighting loads, such as easy retrofitting at low complexity and costs while offering high robustness and low standby power consumption. These advantageous properties make DLT interesting for being further investigated, which has been conducted throughout chapter 3 according to two of the three major objectives listed in chapter 1, which are improved energy efficiency and tailored system intelligence of smart LED drivers. The third key task of delivering high light quality is inherently ensured by the DLT communication approach as it provides all relevant control commands for modern lighting systems, such as brightness adaption, color control and CCT adjustment, with sufficient resolution. Beyond that, the DLT approach including the improved system developments of this thesis, which enable extended functionality, have been assessed in relation to other communication methodologies, particularly concerning power consumption, robustness and complexity. The following paragraphs therefore briefly summarize the gained insights and achievements.

Focusing on energy-efficiency and system intelligence, chapter 3 has studied the existing DLT methodology regarding three major enhancement aspects, which are consistent with the specific goals 1 to 3 outlined in the introduction chapter 1. The corresponding key investigations consequently concentrate on the development of

1. robust DLT FW-RXs with low power consumption that are suitable for monolithic integration,
2. energy-efficient power supplies for DLT CDs enabling WiFi operation to improve interoperability with other smart home systems and
3. a bidirectional DLT communication approach yielding a tailored system intelligence at reasonable power consumption.

Pursuing the first research topic, section 3.2 consequently establishes a system concept for monolithically integrable DLT CGs and compares three different DLT FW-RX topologies with one another based on simulation and

measurement results. For this purpose, the developed FW-RX circuits are finally implemented in hardware using commercially available off-the-shelf (COTS) components. The comprehensive investigation thoroughly evaluates circuit complexity, power consumption and robustness of the three DLT detector and decoder approaches. Detailed results are presented in section 3.2.3, in which table 3.5 summarizes the achieved performance metrics. In conclusion, the conducted analysis evaluates two favorable DLT detector concepts as suitable for monolithic integration and hence optimized smart LED driver platforms. These RX circuits are first, an active analog bandpass filter with a downstream connected Schmitt-Trigger (concept A) and second, a differentiating digital FIR filter with a window comparator (concept B) that uses a resistive divider to scale mains voltage down into the digital voltage domain. Both architectures achieve comparable performance results regarding complexity, power consumption and reliability with a slight advantage for the digital detector approach (concept B). While complexity and power consumption are rather simple to determine, robustness evaluation requires very elaborate measurements under real operating conditions with discrete interferers and random grid distortions. Therefore longterm measurements, which lasted 24 h for each of the proposed detector concepts, recorded corresponding error rates in a noisy lab environment and achieved outstanding results with telegram error rates (TERs) in a two digit ppm range. The achievable RX power consumption is low, even for the implemented hardware solutions with COTS components, and also circuit complexity remains rather simple in both cases. In standby mode, DLT CGs do not consume any power due to being disconnected from mains by the CD. The achieved results not only fulfill the first goal set in the introduction of this thesis but even outperform targeted performance and thereby also pave the way for high-volume production of monolithically integrable DLT CGs as shown later in chapter 6.

The second investigation on energy-efficient power supplies for DLT CDs has been carried out in section 3.3 aiming to enhance embedding of DLT subsystems into a smart home environment, e.g. by means of a WiFi or Zigbee connection. However, this target is rather challenging to achieve because of the very restricting supply limitations specified in the official DLT standard [106] regarding timing interval ($t_{supply} \leq 400\,\mu s$ shortly after mains zero crossing) and amount of maximum allowable current draw ($I_{CD,in} \leq 350\,mA$). To overcome this issue two different supply circuits have been developed based on a dual-stage power converter approach with a storage capacitor in between. Concept A uses a flyback-converter and a buck-converter, whereas concept B combines a boost-converter with a flyback converter as first and second stage, respectively. While both designs provide galvanic isolation, concept B is more beneficial regarding a monolithic integration as the decoupling from mains voltage is realized at the

output of the second converter stage. Concept A on the contrary is easier to handle concerning protection against electric shock, since the second converter stage operates completely in a low voltage domain that may safely be touched. Considering the discontinuous input conditions and the limited input power restrictions, both converters achieved very good results in terms of efficiency and maximum energy yield. Supply concepts A and B provide a maximum continuous output power of 353 mW and 389 mW, respectively, at $V_{out} \approx 3.3\,\mathrm{V}$. Drawn peak power may indeed be much higher for both approaches due to the stored energy on the buffering capacitor C_{store}. The stored energy furthermore ensures high reliability even when half-waves of mains voltage are missing during normal operation, which is likely to happen [241]. It is shown in several experiments that robustness of concept A against these blackouts is nearly twice as good as those of concept B. Detailed performance metrics are presented in tables 3.8 and 3.9. The choice of power supply topology eventually depends on the desired use case or application scenario, whether output power and efficiency or robustness and reliability is more important. The developed power supplies are in fact applicable to all kinds of wall-mounted dimmers or control devices and are also compatible to retrofit technologies, such as incandescent lamps or CFLs. In summary, both investigated power supply concepts have proven in several measurements under realistic operating conditions that provided output power is high enough to continuously supply a ZigBee link [347] and an LCD backlight [355] simultaneously or a WiFi module [357] in different modes of operation, even during the power-hungry association phase, while fully complying with the DLT specification [106]. Thereby, system intelligence of the DLT approach is significantly improved as it is now possible to embed DLT as a sub-system into other lighting control systems or smart home environments and consequently achieve a tailored systems intelligence. Goal 2 targeted in the introduction chapter 1 is thus considered to be completely achieved.

The third investigation objective focuses on one major drawback of the DLT technology, which is the unidirectional communication capability. Section 3.4 therefore identifies the current flow as a suitable reverse transmission channel and consequently developed a suitable reverse (REV)-TX as well as different REV-RX circuits to extend the DLT approach towards bidirectional communication. The REV-TX uses the existing LC bypass hardware in a DLT CG and additionally applies a programmable resistive DAC (RDAC) to modulate the current flow for backward transmission of the desired data in a simple OOK modulation scheme. In order receive this data in the DLT CD, three fundamental RX circuits were developed and compared in this thesis, which are first an active analog bandpass (BP), second a digital matched filter and third a transformer based sensing approach. Another digital bandpass filter topology

as proposed in [243] has also been investigated but delivers worse performance in terms of robustness and power consumption compared to the digital matched filter while featuring comparable hardware effort. The different receiver circuits have indeed been trimmed for high reliability while minimizing the required modulation current amplitude and hence power consumption at the same time. Detailed results of measured robustness and sensitivity levels are denoted in table 3.13, whereas tables 3.14 and 3.15 depict measured power consumption as well as calculations for different scenarios and operating conditions for RX and TX mode. The transformer based approach yields outstanding results regarding sensitivity and robustness as it requires a modulation current of only $I_{mod,set} = 10\,\text{mA}$ and achieves a TER of less than 5 ppm. This excellent performance comes at the cost of an increased hardware effort, footprint area on the PCB and thus higher costs. Due to employing the current sense transformer this REV-RX is the only concept that offers the possibility of galvanic isolation. The digital matched filter represents in fact a good trade-off between hardware demand, power consumption and robustness. With a modulation depth of $I_{mod,set} = 28\,\text{mA}$ a TER of 322 ppm is achieved, which is far below the 1 % limit defined by goal 3 in the introduction chapter. The hardware effort is indeed minimal since this approach only uses components that are anyways needed in the control device. The analog BP realizes a slightly better TER of 114 ppm but requires higher power consumption and circuit complexity. In summary, a fully functional, bidirectional DLT communication system has been established, which further improves overall system intelligence and consequently even surpasses the target goal 3 set in chapter 1. The digital matched filter and the transformer based REV-RX approaches are more than suitable for bidirectional DLT communication while featuring very good performance characteristics.

Of course, several further research questions have resulted from the conducted investigations aiming to further improve the DLT methodology, e.g. to use another modulation scheme for reverse transmission that is more preferable in terms of EMI or the idea of expansing DLT to a full home automation system similar to the digitalSTROM™ approach presented in [101]. In conclusion, this thesis has fulfilled and partially even exceeded the ambitious goals 1, 2 and 3 defined in the introduction chapter 1. The proposed improvement measures may be applied to further enhance DLT and consequently push market acceptance.

Chapter 4

Color Mixing and Control for High Quality Lighting Systems

The employed color control strategy significantly impacts achievable light quality because it determines the number of usable LED primaries as well as the adjustable brightness resolution per LED channel. As outlined in section 2.2.3, more than three primary LEDs actually yields better performance in terms of light quality and color mixing, e.g. a higher CRI. Targeting a flexible deployment in HCL lighting applications with excellent optical properties, the color control approach presented in this thesis thus aims at handling up to six different LED primaries. Its flexible design shall thereby also enable operating systems with less LED channels, e.g. in tunable white applications, which only requires at least two LED primaries. The key idea on the presented color control approach has been published in [239].

Due to the linear relationship between PWM duty cycle of the LED current I_{LED} and emitted luminance L_v of attached LEDs the presented color control strategy is designed for PWM based LED driving stages. It is assumed

that all LED channels are individually and independently controllable. The number of series-connected LEDs per channel however only depends on the chosen topology of the LED driving stage and its deliverable output voltage. It is hence independent of the actual color control algorithm. More details on the LED driving stage including a concept proposal and implementation for a suitable topology with high flexibility is provided in chapter 5.

Although the color control strategy is in principle independent of the used communication system or interface, it still needs to be capable of handling certain input data, such as desired brightness values B, color coordinates (x, y) or color temperatures (CTs). As explicated in section 2.2, it is essential to control emitted luminance L_v independently from the desired color point $\boldsymbol{p} = (x_P, y_P)^T$ or selected CCT. Hence, the general idea of the color control approach presented here is to compute a relative intensity distribution for the used LED channels, which is subsequently scaled by the selected brightness value B. The relative intensity distribution is calculated in dependence on physical parameters, such as the luminous flux of the individual LEDs and their color coordinates, as well as in terms of received user inputs, like desired color point $\boldsymbol{p}$ or CCT. Additionally, the main control logic maps the computed intensity distribution onto distinct PWM duty cycles for the respective LED driving stages regulating and adjusting LED current flow accordingly. The proposed color control algorithm can hence be split into two individual parts, which are first the color computation as a relative intensity distribution and second the independent brightness adjustment including adaption to the nonlinear perception of the human eye as well as a PWM mapping procedure. Both processes forming together the color mixing and control strategy are explained in detail in the following sections.

4.1 Color Computation Algorithm for Multi-Channel LED Lighting Systems

The color computation algorithm aims to synthesize an arbitrarily chosen color point $\boldsymbol{p} = (x_P, y_P)^T$ by driving employed LEDs in a given luminaire setup according to their relative mixing properties. Therefore, the relative intensity distribution, which needs to be found, shall indicate the relative proportion or share of each LED to realize the desired color point. By applying vector analysis techniques, the LED primaries or moreover their (x, y) coordinate pairs – regarding the CIE 1931 (x, y) chromaticity diagram – can be treated as position vectors spanning the gamut plane of displayable color points. Only colors inside this gamut, which is bordered by the connecting lines of adjacent LEDs, can be synthesized due to physical constraints. Nevertheless, scaling and

adding LED primary vectors in fact enables the synthesis of all color points within the spanned gamut. Fig. 4.1 shows the displayable color gamut spanned by six different LEDs in the CIE 1931 (x, y) chromaticity diagram. In the presented setup these six LED primaries are blue (B), cyan (C), green (G), amber (A), red (R) and white (W). Any color within this RGB-CAW gamut can be rendered by the developed six channel light source. Removing LED primaires, e.g. cyan and amber or cyan and white, reduces the size of the gamut and hence the amount of displayable colors. Fig. 4.1 exemplarily illustrates this fact for two four-channel configurations, namely RGB-W and RGB-A, in contrast to the six channel RGB-CAW setup.

In order to render a desired color point inside the displayable gamut, the scaling and adding up of LED primary vectors has to meet certain conditions and rules. This fact becomes clear when investigating a simple example, which is a light source built of just two LEDs as introduced in the *"color mixing"* paragraph at end of section 2.2.2. In this case it is only possible to synthesize color points on the connecting line between these two LED coordinates. Consequently, the scaling factor for each LED may not exceed a value of one, while the sum of both scaling coefficients has to equal one. Negative scaling coefficients are not realizable and would thus not yield any valid solution. These conditions and rules can simply be transfered to more complex systems like the one presented in this work. Hence, summing up the scaling factors of all used LEDs has to result in a value of one. This condition also includes LEDs lying inside the spanned gamut, which is in the presented case the white (W) one. In more complex LED systems negative scaling factors are also forbidden due to the physical constraints. To find an analytical expression, which can mathematically be solved, all LED scaling coefficients are gathered in a common vector of prefactors $\boldsymbol{f}$. Expressing a desired color point $\boldsymbol{p} = (x_P, y_P)^T$ as a linear combination of scaled LED primary vectors $f_i \cdot (x_i, y_i)^T$ and considering this color point $\boldsymbol{p}$ to be inside the displayable gamut leads consequently to the subsequent system of equations 4.1,

$$\underbrace{\begin{pmatrix} x_B & x_C & x_G & x_A & x_R & x_W \\ y_B & y_C & y_G & y_A & y_R & y_W \\ 1 & 1 & 1 & 1 & 1 & 1 \end{pmatrix}}_{=\boldsymbol{C}} \cdot \underbrace{\begin{pmatrix} f_B \\ f_C \\ f_G \\ f_A \\ f_R \\ f_W \end{pmatrix}}_{=\boldsymbol{f}} = \underbrace{\begin{pmatrix} x_P \\ y_P \\ 1 \end{pmatrix}}_{=\boldsymbol{P}}, \tag{4.1}$$

where the indices B, C, G, A, R and W represent the six LED primary colors as denoted above. The third line in this system of equations implies the summation

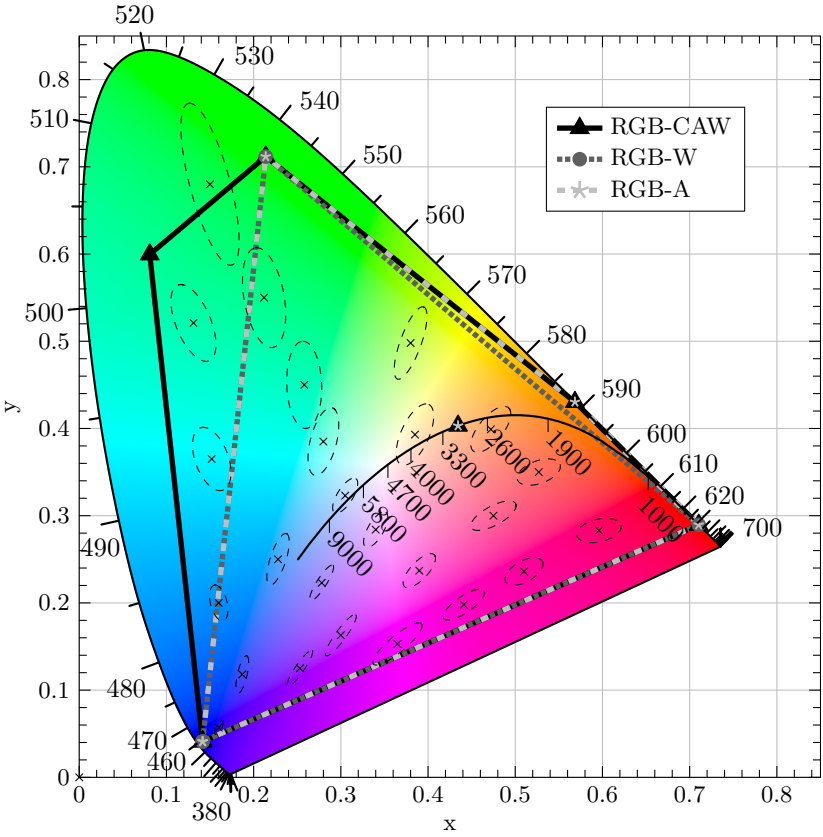


Figure 4.1: Displayable color gamut of different LED configurations in the CIE 1931 chromaticity diagram.

condition, which equals one when adding up all scaling factors. Additionally, this line also represents a normalization to maximum emitted luminance enabling scalability to selected brightness values B, which is required in a later step as explained in section 4.2. As a matter of fact, the scaling coefficients f_i correlate with the relative lengths of the LED primary vectors. Hence, solving the system of equations 4.1 directly yields the sought-after relative intensity distribution of the employed LEDs.

The color matrix $\boldsymbol{C}$ containing all LED primary vectors and the summation condition is of dimension $m \times n$, with $m = 3$ rows and $n = 6$ columns. Investigating the formula given in equation 4.1 reveals that an under-determined system of equations has to be solved as $m < n$ holds [18]. Therefore, an infinite amount of solutions exists solving this under-determined system of equations. Obviously, the three rows of the given system of equations in 4.1 are independent of each other because all of the LED coordinates neither form a straight line nor have identical x- or y-values at the same time. The rank of matrix $\boldsymbol{C}$ hence equals $rank(\boldsymbol{C}) = 3$, which directly gives matrix $\boldsymbol{C}$'s kernel dimension of $n - rank(\boldsymbol{C}) = 6 - 3 = 3$. Therefore, three independent basis vectors exist spanning the nullspace of matrix $\boldsymbol{C}$ [239]. All computable solutions of the under-determined system of equations in 4.1 can thus be expressed as a linear combination of three homogeneous solution vectors $\boldsymbol{l_{h,i}}$, with $i = 1...3$, plus an arbitrary inhomogeneous solution vector $\boldsymbol{l_{inh}}$. Equation 4.2 shows the corresponding mathematical relationship,

$$
\begin{aligned}
& \boldsymbol{f} = \quad \lambda \cdot \boldsymbol{l_{h1}} + \mu \cdot \boldsymbol{l_{h2}} + \sigma \cdot \boldsymbol{l_{h3}} + \boldsymbol{l_{inh}} \quad , \\
\Leftrightarrow \quad & \boldsymbol{f} = \underbrace{\begin{pmatrix} l_{h1,B} & l_{h2,B} & l_{h3,B} \\ l_{h1,C} & l_{h2,C} & l_{h3,C} \\ l_{h1,G} & l_{h2,G} & l_{h3,G} \\ l_{h1,A} & l_{h2,A} & l_{h3,A} \\ l_{h1,R} & l_{h2,R} & l_{h3,R} \\ l_{h1,W} & l_{h2,W} & l_{h3,W} \end{pmatrix}}_{=\boldsymbol{L_{hom}}} \cdot \underbrace{\begin{pmatrix} \lambda \\ \mu \\ \sigma \end{pmatrix}}_{=\boldsymbol{\zeta}} + \underbrace{\begin{pmatrix} l_{inh,B} \\ l_{inh,C} \\ l_{inh,G} \\ l_{inh,A} \\ l_{inh,R} \\ l_{inh,W} \end{pmatrix}}_{=\boldsymbol{l_{inh}}} , \qquad (4.2) \\
\Leftrightarrow \quad & \boldsymbol{f} = \quad \boldsymbol{L_{hom}} \cdot \boldsymbol{\zeta} \quad + \quad \boldsymbol{l_{inh}} \quad .
\end{aligned}
$$

Each row of this second system of equations 4.2 represents a solution to the scaling factors f_B, f_C, f_G, f_A, f_R and f_W, respectively. The unknown coefficients λ, μ and σ may be chosen arbitrarily. Any combination of these three variables will yield a valid solution to synthesize the desired color point $\boldsymbol{p}$.

At first, it is hence crucial to find the homogeneous and inhomogeneous solution vectors as used in equation 4.2. An efficient way to numerically solve under-determined systems of equations, as the one given in 4.1, is using a typical QR factorization. The QR decomposition splits matrix $\boldsymbol{C}$ into an orthogonal matrix $\boldsymbol{Q}$, with $\boldsymbol{QQ^T = E}$, and an upper triangular matrix $\boldsymbol{R}$. Applying such a QR decomposition on given matrix $\boldsymbol{C}$ in the system of equations 4.1, leads to

the subsequent equations and mathematical relationships,

$$\boldsymbol{C}\cdot\boldsymbol{f} = \boldsymbol{Q}\cdot\boldsymbol{R}\cdot\boldsymbol{f} = \boldsymbol{p} \tag{4.3}$$

$$\Leftrightarrow \quad \boldsymbol{R}\cdot\boldsymbol{f} = \boldsymbol{Q^T p} = \boldsymbol{p^*} \tag{4.4}$$

$$\Leftrightarrow \quad \boldsymbol{f} = \boldsymbol{R^{-1}}\cdot\boldsymbol{p^*}. \tag{4.5}$$

Having a closer look into equation 4.4 reveals that the same considerations are valid as the ones made for equation 4.1. Equation 4.4 also represents an under-determined system of equations with an infinite amount of possible solutions that are realizable by any combination of the same three homogeneous basis vectors plus an arbitrary inhomogeneous solution. In order to find these three homogeneous solution vectors, the nullspace of matrix $\boldsymbol{R}$ needs to be found. Therefore, solving equation 4.6,

$$\boldsymbol{R}\cdot\boldsymbol{f} = \begin{pmatrix}0\\0\\0\end{pmatrix}, \tag{4.6}$$

where the upper triangular matrix $\boldsymbol{R}$ follows a given structure of

$$R = \begin{pmatrix} r_{11} & r_{12} & r_{13} & r_{14} & r_{15} & r_{16} \\ 0 & r_{22} & r_{23} & r_{24} & r_{25} & r_{26} \\ 0 & 0 & r_{33} & r_{34} & r_{35} & r_{36} \end{pmatrix},$$

yields the sought-after solution. The three vectors $\boldsymbol{f_i}$, with $i = 1...3$, which solve equation 4.6, are identical to the predefined homogeneous solution vectors, $\boldsymbol{l_{h1}}$, $\boldsymbol{l_{h2}}$, and $\boldsymbol{l_{h3}}$, respectively. Since the given system of equations is under-determined, only three scaling factors depend on the other ones, which leaves the remaining three variables to be freely chosen. The presented algorithm uses these degrees of freedom to (arbitrarily) set the variables to $f_W = \lambda$, $f_R = \mu$ and $f_A = \sigma$. The homogeneous solution vectors are hence identified as follows.

$$\boldsymbol{l_{h1}} = \begin{pmatrix} l_{h11}\\ l_{h12}\\ l_{h13}\\ l_{h14}\\ l_{h15}\\ l_{h16}\end{pmatrix} = \begin{pmatrix} l_{h11}\\ l_{h12}\\ l_{h13}\\ 0\\ 0\\ 1\end{pmatrix}; \; \boldsymbol{l_{h2}} = \begin{pmatrix} l_{h21}\\ l_{h22}\\ l_{h23}\\ l_{h24}\\ l_{h25}\\ l_{h26}\end{pmatrix} = \begin{pmatrix} l_{h21}\\ l_{h22}\\ l_{h23}\\ 0\\ 1\\ 0\end{pmatrix}; \; \boldsymbol{l_{h3}} = \begin{pmatrix} l_{h31}\\ l_{h32}\\ l_{h33}\\ l_{h34}\\ l_{h35}\\ l_{h36}\end{pmatrix} = \begin{pmatrix} l_{h31}\\ l_{h32}\\ l_{h33}\\ 1\\ 0\\ 0\end{pmatrix}$$

The upper three entries of each homogeneous solution vector are computed iteratively by solving the system of equations 4.6 with the made choices for the three freely selectable variables. Equations 4.7 to 4.9 exemplarily illustrate this iterative solution procedure for the first homogeneous solution vector $\boldsymbol{l_{h1}}$. The same scheme is applied for finding the other two homogeneous solution vectors.

$$l_{h16} = 1; \qquad l_{h15} = l_{h14} = 0$$

$$l_{h13} = -\frac{r_{36}}{r_{33}} \tag{4.7}$$

$$l_{h12} = -\frac{r_{26} - l_{h13} \cdot r_{23}}{r_{22}} \tag{4.8}$$

$$l_{h11} = -\frac{r_{16} - l_{h13} \cdot r_{13} - l_{h12} \cdot r_{12}}{r_{11}} \tag{4.9}$$

The inhomogeneous solution vector is a direct result of the QR decomposition. It is found by back substitution of $\boldsymbol{R}$ on $\boldsymbol{p^*}$ following the calculation rule of

$$l_{inh,k} = r_{kk} \cdot \left(p_k^* - \sum_{i=k+1}^{n} r_{ki} \cdot l_{inh,i} \right). \tag{4.10}$$

Instead of inserting the number of columns for n in equation 4.10, the color computation algorithm uses the minimum of rows or columns, $\min_{\forall n,m \in \mathbb{N}}(m,n)$. In this way, the same algorithm can also be used for over-determined systems of equations, which is needed later for the conducted optimization routine. Coming from equation 4.4 vector $\boldsymbol{f}$ is in this case again identical to $\boldsymbol{l_{inh}}$. Within a threefold under-determined system of equations the inhomogeneous solution vector therefore always follows a structure of

$$\boldsymbol{l_{inh}} = \begin{pmatrix} l_{inh,1} \\ l_{inh,2} \\ l_{inh,3} \\ 0 \\ 0 \\ 0 \end{pmatrix} = \begin{pmatrix} f_1 \\ f_2 \\ f_3 \\ 0 \\ 0 \\ 0 \end{pmatrix}. \tag{4.11}$$

Once the homogeneous and inhomogeneous solution vectors have been found, any possible combination of the three variables λ, μ and σ delivers a valid solution for the scaling factors $\boldsymbol{f}$. In the end, all these solutions will yield

the same desired color point $\boldsymbol{p}$, however with a different spectral distribution regarding the emitted optical spectrum of employed LEDs. Hence, it is desirable to find an optimum in the computation and synthesis process for the selected color point $\boldsymbol{p}$ with respect to certain criteria. A potential optimization criterion is a maximum CRI in case of "white light" or colors close to the planckian locus like selected CCTs. Other possible constraints could e.g. be a maximum optical or electrical efficiency, a maximum emitted luminance, a minimum perceivable color shift (ΔE or $\Delta u'v'$) or a preferably continuous emitted optical spectra. Using numerical calculations, various methods exist to determine a result within the infinite diversity of the general solution space, which minimizes the deviation to a predefined vector. Hence, a so-called optimization vector $\boldsymbol{s_{opt}}$ is introduced to the system of equations 4.2 aiming to find a relative distribution of the scaling factors $\boldsymbol{f}$ that meets one or more of the mentioned criteria. This optimization vector $\boldsymbol{s_{opt}}$ does not describe a specific color, but indicates in fact a weighting of the respective LED channels according to the specified optimization criteria. Different scenarios therefore require different optimization criteria and hence also different optimization vectors. Equalizing $\boldsymbol{s_{opt}}$ to the sought-after scaling factors $\boldsymbol{f}$ thus modifies equation 4.2 to the following subset of equations,

$$\boldsymbol{f} = \boldsymbol{L_{hom}} \cdot \boldsymbol{\zeta} + \boldsymbol{l_{inh}} = \boldsymbol{s_{opt}}\,,$$

$$\Leftrightarrow \begin{pmatrix} l_{h1,B} & l_{h2,B} & l_{h3,B} \\ l_{h1,C} & l_{h2,C} & l_{h3,C} \\ l_{h1,G} & l_{h2,G} & l_{h3,G} \\ l_{h1,A} & l_{h2,A} & l_{h3,A} \\ l_{h1,R} & l_{h2,R} & l_{h3,R} \\ l_{h1,W} & l_{h2,W} & l_{h3,W} \end{pmatrix} \cdot \begin{pmatrix} \lambda \\ \mu \\ \sigma \end{pmatrix} = \begin{pmatrix} s_{opt,B} \\ s_{opt,C} \\ s_{opt,G} \\ s_{opt,A} \\ s_{opt,R} \\ s_{opt,W} \end{pmatrix} - \begin{pmatrix} l_{inh,B} \\ l_{inh,C} \\ l_{inh,G} \\ l_{inh,A} \\ l_{inh,R} \\ l_{inh,W} \end{pmatrix}, \quad (4.12)$$

which represents an over-determined system of equations. Generally, these types of linear problems provide neither a distinct nor an exact solution. For the given case it is however not necessary to find an exact solution of equation 4.12. Moreover, the Euclidean distance between the general solution and the optimization vector $\|(\boldsymbol{f} - \boldsymbol{s_{opt}})\|_2$ shall be minimized as shown in equation 4.13,

$$\min_{\forall \boldsymbol{\zeta} \in \mathbb{R}^n} \|\boldsymbol{L_{hom}} \cdot \boldsymbol{\zeta} - (\boldsymbol{s_{opt}} - \boldsymbol{l_{inh}})\|_2 = \min_{\forall \boldsymbol{\zeta} \in \mathbb{R}^n} \|\boldsymbol{L_{hom}} \cdot \boldsymbol{\zeta} - \boldsymbol{k}\|_2 \,, \quad (4.13)$$

$$\text{with} \quad \boldsymbol{s_{opt}} - \boldsymbol{l_{inh}} := \boldsymbol{k}\,. \quad (4.14)$$

A well-known method to numerically determine the best approximation of a solution vector for an over-determined system of equations is again using a QR

decomposition. In consideration of an implementation this fact becomes quite beneficial as the same QR decomposition algorithm can be used for solving both, under- and over-determined system of equations, resulting in a lower hardware and implementation effort or rather relaxed demands on the computing DSP or MCU. When utilizing the same QR decomposition algorithm in both cases, column and row length have to be passed invertedly for the over-determined system of equations 4.12. Additionally, some minor modifications as shown in the subsequent equations have to be considered. The QR decomposition is defined by

$$\boldsymbol{Q^T} \cdot \boldsymbol{L_{hom}} = \begin{pmatrix} \tilde{\boldsymbol{R}} \\ - \end{pmatrix} \quad \text{with} \quad \tilde{\boldsymbol{R}} \in \mathbb{R}^{n \times n} \tag{4.15}$$

$$\Leftrightarrow \boldsymbol{Q^T} \cdot (\boldsymbol{s_{opt}} - \boldsymbol{l_{inh}}) \;=\; \boldsymbol{Q^T} \cdot \boldsymbol{k} \;=\; \begin{pmatrix} \boldsymbol{k_{upper}} \\ \boldsymbol{k_{lower}} \end{pmatrix}, \tag{4.16}$$

$$\Leftrightarrow \qquad \tilde{\boldsymbol{R}} \cdot \boldsymbol{\zeta} \;=\; \boldsymbol{k_{upper}}\,. \tag{4.17}$$

Applying forward substitution on equation 4.17 directly yields vector $\boldsymbol{\zeta}$, which automatically solves the minimization problem. In conjunction with the homogeneous and inhomogeneous solution vectors, $\boldsymbol{L_{hom}}$ and $\boldsymbol{l_{inh}}$, vector $\boldsymbol{\zeta}$ defines the sought-after vector $\boldsymbol{f}$ giving the relative intensity distribution for controlling the individual LED channels synthesizing the desired color point $\boldsymbol{p}$.

As mentioned above, the color computation algorithm also works for less than six LED channels and any other combination of LED primary sets. Replacing any of the LED colors by another one, e.g. removing cyan and using mint or lime instead, the algorithm just requires the corresponding (x, y) coordinates and – in a later step – the luminous flux of the new LEDs as inputs to its memory storage. The influence of luminous flux on the color control is explained in detail in section 4.2. In case of employing less than six LEDs, the linear system denoted in equation 4.1 yields according to the rules of linear algebra either infinitely many solutions ($n = 4$ or $n = 5$), one single unique solution ($n = 3$) or no general solution at all ($n = 2$) because the number of independent rows ($m = 3$) never changes. Using three LEDs for color synthesis ($n = 3$) is in fact the simplest case as the linear system of equations 4.1 has only one distinct and unique solution. In fact, the QR decomposition of matrix $\boldsymbol{C}$ already solves the linear system 4.1 by computing the inhomogeneous solution vector $\boldsymbol{l_{inh}}$ via back substitution. Obviously, an optimization is neither possible nor necessary, which supersedes the introduced optimization vector $\boldsymbol{s_{opt}}$ in this case. On the contrary employing a light source with just two LEDs ($n = 2$) leads to the linear system

of equations 4.1 being over-determined. Although it is generally not possible to find an exact solution to this problem, QR decomposition fortunately helps again to determine the best – or in this case closest – approximation as shown by equations 4.15 to 4.17. The color computation algorithm hence outputs a relative intensity distribution for the color point sitting on the connection line between the two LEDs with closest distance to the chosen color point $\boldsymbol{p}$. A typical application scenario for using this setup is building a tuneable white light source. In an implemenation of the color computation algorithm, the homogenous solution matrix $\boldsymbol{L_{hom}}$ as well as the multiplication vector $\boldsymbol{\zeta}$ are set to zero in these both cases ($n = 2$ and $n = 3$). Thereby, the algorithm can be applied without any changes still yielding the correct solution for or the closest approximation to the chosen color point. If four or five LED primaries were used, the amount of valid solutions remains infinitely. RGB-W or RGB-A are widely-spread setups in case of employing four LED channels and are typically used in high-end lighting systems featuring enhanced light quality as outlined in section 2.2.3. Due to the remaining degree(s) of freedom the proposed color computation algorithm yields in both cases similar solution sets as the one described for six colors. Equation 4.18 shows a typical one for an RGB-W setup. The homogeneous solution is hence composed by a single vector.

$$\boldsymbol{f} = \quad \boldsymbol{l_{hom}} \quad \cdot \boldsymbol{\zeta} \; + \quad \boldsymbol{l_{inh}} \quad = \quad \boldsymbol{s_{opt}} \quad ,$$

$$\Leftrightarrow \boldsymbol{f} = \begin{pmatrix} l_{hom,B} \\ l_{hom,G} \\ l_{hom,R} \\ l_{hom,W} \end{pmatrix} \cdot \lambda + \begin{pmatrix} l_{inh,B} \\ l_{inh,G} \\ l_{inh,R} \\ l_{inh,W} \end{pmatrix} = \begin{pmatrix} s_{opt,B} \\ s_{opt,G} \\ s_{opt,R} \\ s_{opt,W} \end{pmatrix}, \tag{4.18}$$

Since choosing number and type of employed LEDs remains completely free, the proposed color computation algorithm provides maximum flexibility in various application scenarios and use cases.

4.2 Nonlinear Adaption to Human Color and Brightness Perception

To realize an optimized color mixing, the individual channels of an employed LED driver shall be controlled according to the relative intensity distribution $\boldsymbol{f}$ that has been determined by the color computation algorithm shown in chapter 4.1. So far it has been assumed that all LED colors or moreover their (x, y) coordinate pairs are equally weighted to compute the desired color point. This

is obviously correct in terms of a pure mathematically vector analysis. However, the employed LEDs differ in their emitted radiometric power, which depends on the physical properties and characteristics of the respective LED, such as used bandgap material or luminous efficacy [239], [312], as explained in section 2.2. Additionally, light and color sensation of the human eye follow a nonlinear perception curve according to the eye sensitivity function $V(\lambda)$ mentioned also in section 2.2. All LEDs hence feature a different luminous intensity I_v, luminous flux ϕ_v and emitted luminance L_v. Therefore, the computed relative intensity distribution $\boldsymbol{f}$, which is meant to indicate the weighting of each LED channel for controlling its respective electrical driving stage, needs to be adapted according to the human color and intensity perception. This control mechanism thus requires a suitable mapping function – in the presented case to distinct PWM duty cycles – accounting for the nonlinear perception characteristics of the human eye. Consequently, this brightness adaption of the computed relative intensity distribution involves several steps, which are

1. a nonlinear adaption of the relative intensity distribution to human color perception,

2. a nonlinear brightness scaling of the synthesized color and finally

3. a PWM mapping procedure combining the results of these first two steps.

Nonlinear Adaption of the Relative Intensity distribution $\boldsymbol{f}$

Recalling that the tristimulus values X_i, Y_i and Z_i describe the color impression sensed by the human eye based on their corresponding color matching functions [312], they can be used to realize the desired nonlinear adaption mechanism. Dividing each scaling factor f_i by the sum of the corresponding LED's tristimulus values X_i, Y_i and Z_i hence compensates for this nonlinear perception effect [239] as the scaling factors are adopted to the relative color impression of their respective LED by this means. Applying equation 2.8 this division can also be expressed as a multiplication by y_i/Y_i. Additionally, a normalization to the maximum of these corrected relative scaling factors is required in order to keep the relative distribution among employed LEDs and scale it in a later step with the user-defined selected brightness value B. Applying these considerations leads to an adoption of the relative scaling factors f_i according to equation 4.19. The final relative intensity distribution is expressed by the factors $d_{rel,i}$, with

$$d_{rel,i} = \frac{f_i}{d_{rel,max}} \cdot \frac{1}{X_i + Y_i + Z_i} = \frac{f_i}{d_{rel,max}} \cdot \frac{y_i}{Y_i} \,. \tag{4.19}$$

The tristimulus value Y represents per definition by the CIE the emitted luminance L_v of the respective light source. Fortunately, this luminance factor of each LED can in fact directly be taken from the associated data sheet by the indicated luminous flux $\phi_{lum,i}$, as equation 4.20 obtains [239], [312],

$$\phi_{lum,i} = 683.002 \frac{\text{lm}}{\text{watt}} \int_0^\infty P(\lambda) \cdot \bar{y}(\lambda) \, \text{d}\lambda = 683.002 \frac{\text{lm}}{\text{watt}} \cdot Y_i \,. \qquad (4.20)$$

This is a distinct advantage over other approaches, like the ones presented in [179] and [315], because the proposed color control algorithm does not need to handle the relative intensities of each LED within all computations, but justs adopts them in a final step. In fact, the algorithm just scales the computed factors f_i linearly with a constant value, which relaxes hardware demands in a later target implementation. The intensity correction values $\frac{y_i}{Y_i}$ only need to be calculated once by the luminous flux taken from the LED data sheet and can be stored in the memory of the intelligent luminaire [239].

Nonlinear Brightness Scaling

Once the final relative intensity distribution $\boldsymbol{d_{rel}}$ is found for a selected color point $\boldsymbol{p} = (x_P, y_P)^T$, it is desired to independently scale emitted luminance L_v of the light source in order to achieve different illuminance levels for the chosen color coordinates. The brightness adjustment hence aims to transfer a user defined input value of a linear brightness scale $B \in \{0, 1, 2, ..., b\}$ into a luminous output, which is linearly perceived by the human eye. Unfortunately, the human eye also features a highly nonlinear relationship between brightness perception and emitted luminance L_v [38], [328] as outlined in section 2.2.2. In case of low luminance levels the human eye responses very sensitive to small changes in luminance, whereas it is rather insensitive to comparable variations at high luminance levels [290]. Indeed human brightness sensation strongly depends on the surrounding and observation conditions [408]. It is thus more useful to consider a relative brightness magnitude of related visual stimuli, which is the so-called lightness L. Lightness is defined as the proportion of two related visual stimuli, of which one is perceived as "white" by the human eye [408].

In this work perceived lightness L is defined slightly different in contrast to the original definition listed in [408] but still considered as a "relative brightness". In order to express perceived brightness on a measurable relative scale, lightness L is therefore in the following referred to as the brightness user input value B normalized on its maximum b. The exact function mapping the digital brightness values B with $\{B \in \mathbb{N}_{\nvDash} | 0 \leq B \leq b\}$ onto the perceived lightness scale L with

$\{L \in \mathbb{R},\ 0 \leq L \leq 1\}$ is given by the subsequent equation 4.21. Because of the normalization to its maximum, lightness L only takes values between 0 % and 100 % or 0 and 1, respectively. In case of a DLT system the brightness scale B is specified as an 8 bit range resulting in a maximum possible user input value of $b = 2^8 - 1 = 255$, which is the equivalent for a 100 % lightness. If another communication system is to be used, the brightness control can be easily adapted by simply changing the range of B to the desired value.

$$L(B) = \begin{cases} 0 & \text{, if } B = 0 \\ \dfrac{B-1}{b-1} \cdot (1 - L_{min}) + L_{min} & \text{, else} \end{cases} \tag{4.21}$$

The value L_{min} denotes the minimum adjustable lightness level. It accounts for the physical limitation of the LED driving stage, which is the minimum possible on-time $t_{PWM,min}$ for the LED current to flow. This minimum on-time obviously strongly depends on circuit design and architecture of the LED driving stage as explained later in chapter 5 and is thereby related to minimum achievable PWM duty cycle.

In order to determine the nonlinear relationship between perceived lightness L and emitted luminance L_v, various different kinds of mapping functions have been developed in the past. In fact, it turns out that all of them describe somehow a logarithmic correlation between perceived lightness and emitted luminance. A well-known technique to compensate for this nonlinear effect is the so-called gamma correction, which is widely applied in computer monitors using a γ value of about 2.2 [333]. Another famous compensation formula for linear brightness perception over dimming is the DALI dimming curve [341]. Both methodologies actually compensate the logarithmic brightness perception of the human eye by applying an exponential mapping function. The algorithm for nonlinear brightness adaption developed in this work also founds on gamma correction to realize a linear perceivable lightness with respect to the linearly selected user input word B. Normalizing luminance L_v to its achievable maximum $L_{v,max}$ in a given set of luminaire and LED driver yields normalized luminance $L_{v,nom}$, which is equivalent to the normalized tristimulus value Y_{nom} with $\{Y_{nom} \in \mathbb{R},\ 0 \leq Y \leq 1\}$. Both normalized quantities thus scale between 0 % and 100 %. In the following, it is always referred to normalized luminance as Y_{nom} in order to easier distinguish between lightness L and emitted luminance L_v sharing a similar notation. Applying gamma correction using equation 2.4 with $k = 1$, normalized luminance can consequently be expressed in terms lightness following equation 4.22,

$$Y_{nom} = L^{\gamma}\,. \tag{4.22}$$

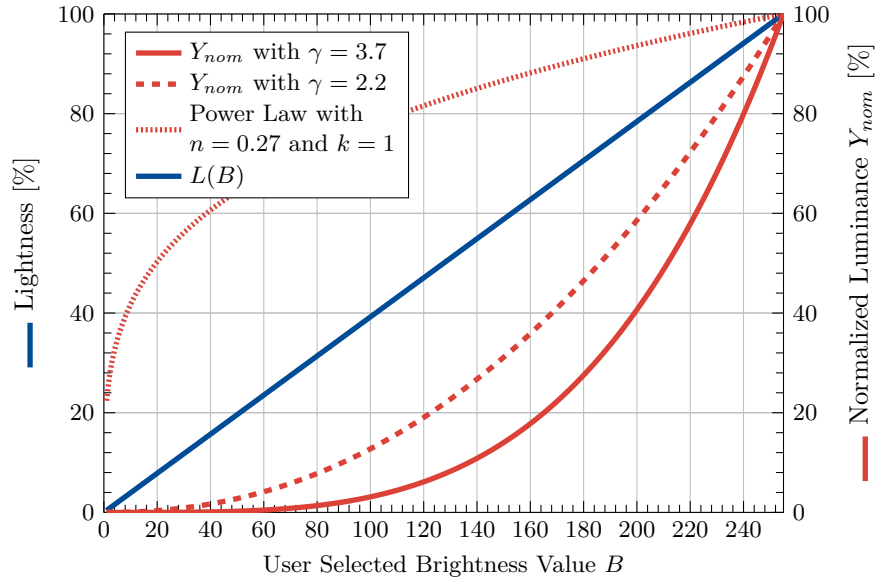


Figure 4.2: Brightness B versus lightness and normalized emitted luminance.

Inserting equation 4.21 thereby gives:

$$Y_{nom}(B) = \begin{cases} 0 & \text{, if } B = 0 \\ \left(\dfrac{B-1}{b-1} \cdot (1 - L_{min}) + L_{min} \right)^{\gamma} & \text{, else } (0 < B \leq b) \end{cases} \tag{4.23}$$

To get a visual impression on the relationship between brightness scale B, lightness L and normalized emitted luminance Y_{nom}, Fig. 4.2 illustrates the corresponding relationships of equations 4.21 and 4.22, respectively. For the sake of completeness Stevens' power law [328] stated in equation 2.4 in section 2.2.2 is also included in the graph using parameters $n = 0.27$ and $k = 1$ to illustrate the compensation effect of human perception by the nonlinear brightness adaption.

PWM mapping procedure

Obviously, the effective (normalized) luminance Y_{nom} is directly proportional to the LED current as described in chapter 2.2 and 2.3. Since a PWM based LED driving stage is employed within the presented work, emitted luminance therefore relates to a certain on-time $t_{on,PWM}$ with respect to one entire PWM time

period T_{PWM}. Pulse width $t_{on,PWM}$ and cycle duration T_{PWM} can obviously be expressed by their digital counterparts, n_{PWM} and N_{PWM}, respectively, when considering a digital control mechanism that generates the final PWM duty cycles D_i. Theoretically, the minimum possible on-time from the digital perspective is therefore only limited by the applied resolution $M_{PWM} = log_2(N_{PWM})$. In reality, the effective minimum on-time is however limited by physical constraints and applied architecture of the LED driving state determining rising and falling times with respect to the target LED current. The digital resolution should consequently be selected much higher avoiding any performance degradation due to quantization effects. Zhao and Wang [432] therefore recommends a resolution of at least $M = 14\,\text{bit}$ to ensure $\Delta E \leq 3$. The control algorithm developed within this thesis uses in fact a resolution of $M_{PWM} = 16\,\text{bit}$ accounting for a certain safety margin. In conclusion, emitted luminance can be expressed by PWM on-time $t_{on,PWM}$ and cycle duration T_{PWM} since the proportional relationship between these measures obtains as explained above. Equations 4.24 and 4.25 summarize the corresponding mathematical relationships,

$$L_v \propto Y_{nom} \propto t_{PWM} \propto n_{PWM}\,, \tag{4.24}$$

$$\Rightarrow Y_{nom} = \frac{t_{PWM}}{T_{PWM}} = \frac{n_{PWM}}{N_{PWM}}\,. \tag{4.25}$$

Based on this knowledge an algorithm can be established, which translates the linear digital brightness input $B \in \{0, 1, 2, ..., b\}$ into distinct PWM duty cycles D_i in dependence of the employed digital resolution. Inserting equation 4.23 into equation 4.25 results in the sought-after relationship depicted in equation 4.26 for $B \neq 0$,

$$n_{PWM} = N_{PWM} \cdot L(B)^{\gamma} = N_{PWM} \cdot \left(\frac{B-1}{b-1} \cdot (1 - L_{min}) + L_{min} \right)^{\gamma}. \tag{4.26}$$

If B equals 0, the intelligent luminaire or moreover its LED driving stage will be set into a controlled off state. So far, equation 4.26 only accounts for the nonlinear brightness adaption mechanism. To get the final PWM duty cycles D_i that can be committed to the used LED driver, the relative intensity distribution $\boldsymbol{d_{rel}}$ from equation 4.19 also needs to be considered. Combining the results from the nonlinear relative intensity distribution $\boldsymbol{d_{rel}}$ from equation 4.19 and the nonlinear brightness adaption calculated in equation 4.26 finally leads to the desired PWM mapping function of a linear brightness input into distinct PWM duty cycles for each employed LED. Equation 4.27 shows the final computation of duty cycles D_i by multiplying the relative intensity factor $d_{rel,i}$

with the selected and nonlinearly adopted brightness B,

$$D_i = n_{PWM} \cdot d_{rel,i} = d_{rel,i} \cdot L(B)^{\gamma} \cdot N_{PWM}$$

$$= d_{rel,i} \cdot \left(\frac{B-1}{b-1} \cdot (1 - L_{min}) + L_{min} \right)^{\gamma} \cdot N_{PWM} \,. \tag{4.27}$$

Considering a DLT CD sending brightness values B of a linear 8 bit scale, it should be noted that this mapping function is on the one hand perfectly suitable for the DLT methodology, but can on the other hand be very flexibly deployed to other communication systems by adapting the digital scale range.

4.3 Implementation of Color Control Algorithm

The proposed color control algorithm has been implemented within the framework of a self-developed MATLAB® software program as well as an explicit C-code on a μC. While the MATLAB® software enables simulation of all relevant color metrics, like CRI or ΔE, and provides in addition graphical illustration of different CIE chromaticity diagrams, the C-code on the μC allows for hardware testing and measurements in conjunction with a DLT system and a multi-channel LED driver like the ones presented in chapters 3 and 5, respectively. Fig.4.3 illustrates the flowchart of the implemented color control algorithm in detail.

As mentioned in section 4.1, the color matrix $\boldsymbol{C}$ contains the chromaticity coordinates x_i and y_i of each primary LED, which have to be stored in the memory of the μC or within the MATLAB® workspace, respectively [239]. The (x, y)-pairs of the employed LEDs can in fact be extracted from the corresponding data sheets, calibrated via spectral measurements or computed over the associated tristimulus values, X, Y and Z by the given spectral intensity distribution [312] according to equations 2.5 to 2.8. Investigating the flowchart in Fig. 4.3 clearly reveals that the color control algorithm is mainly based on a typical QR decomposition. Within the proposed implementation the method of *"Gram-Schmidt"* has been applied [60], [262]. Other very well known implementations are the procedures of *"Householder"* [121], [193] and *"Givens"* [63], [218]. Considering an ASIC implementation the algorithms of *"Householder"* and *"Givens"* might be more favorable as they can be realized more efficiently [193]. The *"Givens"* algorithm can e.g. be implemented in a very hardware-friendly and area-efficient manner by the *"CORDIC"* algortihm [60], [63], [218], [390]. Assuming that an arithmetic logic unit (ALU) is available, e.g. on an MCU, the procedure by *"Householder"* is in principle the most efficient

way to calculate the QR decomposition. Chang *et al.* [60] moreover propose an efficient implementation of the *"Gram-Schmidt"* method in hardware.

Solving the system of equations 4.1, the color control algorithm determines $\boldsymbol{L_{hom}}$ and $\boldsymbol{l_{inh}}$ by applying the QR decomposition [239]. As this yields an infinite amount of solutions, the flowchart follows the optimization path, which directly leads to the over-determined system of equations 4.12. The color algorithm thereby releases a combination of κ, μ, and σ that minimizes the Euclidean distance between optimization vector $\boldsymbol{s_{opt}}$ and the general solution set consisting of $\boldsymbol{L_{hom}}$ and $\boldsymbol{l_{inh}}$. Solving the system of equations 4.12, is performed with the same QR decomposition based algorithm except that column and row length, m and n, respectively, are passed invertedly. This also reduces complexity and thus hardware demand [239].

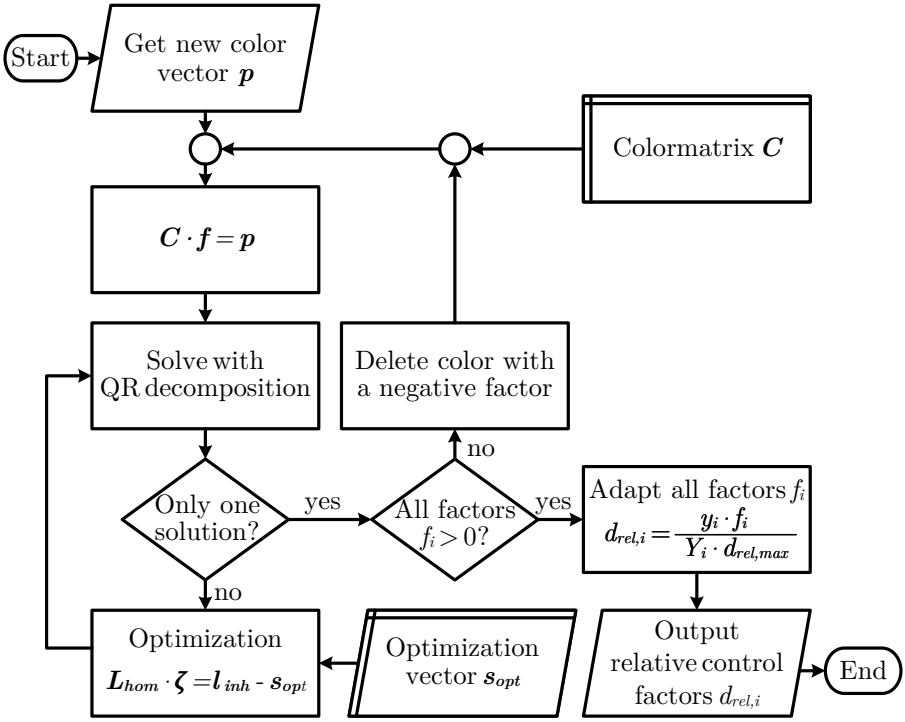


Figure 4.3: Flowchart of the implemented color control algorithm.

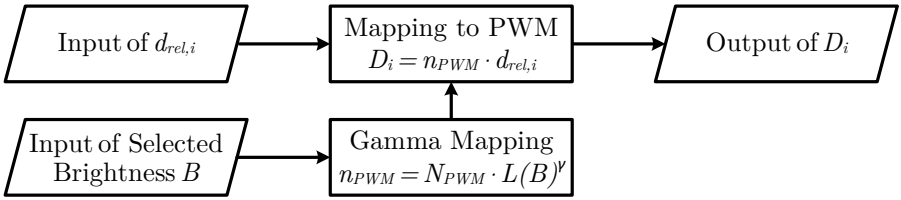


Figure 4.4: Flowchart of nonlinear brightness correction adjusting computed factors $d_{rel,i}$ to PWM duty cycles D_i.

Before the determined solution is passed to the output, it has to be checked whether all factors are greater than zero. This is because not all colors are displayable with a given optimization vector for all LEDs being switched on as explained again later in more detail in section 4.4.3. Hence, if negative factors occur, the algorithm applies either the *"intelligent elimination routine"* based on the area request presented in section 4.4.3 or simply eliminates the first color with a negative factor following a clockwise order of the CIE 1931 chromaticity diagram from blue to white (B-C-G-A-R-W). Subsequently, it starts all over for the reduced system of equations. Obviously, this case scales the gamut down, as one LED will be switched off for the new solution. If the desired color is then no longer within the new gamut, no solution can be found at all. In fact, this problem is automatically solved applying the intelligent elimination routine with a simple area request mentioned above and outlined in section 4.4.3. The algorithm thereby eliminates an LED, which is not limiting the gamut in such a way that no solution will be possible.

Before the calculated prefactors f_i can be committed to the PWM for adjusting its duty cycles D_i accordingly, the nonlinear adaption to human color perception explained in chapter 4.2 is executed. Taking the emitted luminous flux of each LED into account, this nonlinear adaption mechanism scales and normalizes the calculated prefactors f_i by applying equation 4.19. Due to the simple multiplicative scaling this step relaxes hardware demands compared to other solutions [179], [315]. At last, the resulting relative factors $d_{rel,i}$ are mapped with a nonlinear brightness correction mechanism onto distinct PWM duty cycles D_i. The presented implementation employs gamma factor correction [333], which leads to the mapping function of equation 4.27. Fig. 4.4 shows the corresponding implemented block diagram in a flowchart style for the nonlinear PWM adjustment routine of computed factors $d_{rel,i}$ including gamma factor correction for a linear input brightness scale B.

The digital resolution of the applied PWM finally determines in conjunction with the minimum on-time of the LED driving stage the achievable color and brightness accuracy. A high PWM resolution therefore features a significant advantage regarding color point stability. Especially for lower light intensities the inherited color shift is thereby minimized, as PWM duty cycles can be adjusted more precisely in this region. Thus, it is expected that an object appears nearly in the same color for low intensities as it does in bright light. For the current implementation a PWM resolution of $M_{PWM} = 16\,\text{bit}$ has been chosen for each channel, which enables a maximum step count of $N_{PWM} = 65536$. For some practical reasons, like using a clock divider with the power of two, the maximum step count in the μC is however limited to $N_{PWM} = 64000$. Since the LED driver cannot switch infinitely fast, a minimum on-time of $t_{on,min} = 4\,\mu\text{s}$ is assumed for the LED driving stage operating at a PWM switching frequency of $f_{PWM} = 1\,\text{kHz}$. In fact, these metrics represent the achievable performance of the LED driver developed in chapter 5, which confirms the validity of this assumption. While $t_{on,min}$ and f_{PWM} hence define a contrast ratio of $(1:250)$ for each LED channel, the minimum lightness can be calculated by taking the clock frequency of the digital step counter of $f_{counter} = 64\,\text{MHz}$ into account, which runs at the maximum possible frequency of the employed μC in the given implementation. Equation 4.28 shows the associated computation,

$$L_{min} = \frac{n_{PWM,min,on}}{N_{PWM}} = \frac{t_{on,min} \cdot f_{counter}}{N_{PWM}} = \frac{256}{64000}\,. \tag{4.28}$$

If an LED driving stage – just like the one proposed in chapter 5 – is employed that can more or less switch the current flow through the LEDs off instantaneously, it is possible to enable very precise color and brightness control of $\frac{1}{64000}$ starting from the L_{min} level calculated above with the shown implementation. In summary, considering a 16 bit PWM resolution for a number of 8 bit brightness levels, enables high quality gamma correction and precision for color point stability at low light intensities while maintaining manageable hardware demands. Of course, the digital resolution can also be traded for clock frequency to limit hardware demands and power consumption. Another practical implementation was hence realized by using a 15 bit resolution on a μC running with only $f_{\mu C} = 32\,\text{MHz}$.

The hardware demand of the proposed color computation algorithm can be approximated in terms of required storage memory M_{store} and the minimal computational bit resolution r_{comp}. M_{store} obviously also depends on the number of employed LEDs N_{LEDs}. Table 4.1 illustrates the required memory space for each computational parameter. Besides the ones used during derivation in chapter 4.1, Table 4.1 also lists several additional variables, which were

Table 4.1: Required memory space in dependency of employed LEDs for the proposed color control algorithm.

Variable	$\boldsymbol{C}$	$\boldsymbol{f}$	$\boldsymbol{p}$	$\boldsymbol{Q}$	$\boldsymbol{R}$	$\boldsymbol{L_{hom}}$	$\boldsymbol{l_{inh}}$	$\boldsymbol{\zeta}$	$\boldsymbol{k}$	$\boldsymbol{s_{opt}}$
Memory	$2N$	N	2	N^2	N^2	N^2-3N	N	$N-3$	N	N

Variable	$\boldsymbol{sum_{factors}}$	$\boldsymbol{sum_{weights}}$ (16 bit only)	$\boldsymbol{weights}$ (16 bit only)
Memory	1	1	N

Variable	$\boldsymbol{color_{pos}}$ (8 bit only)	$\boldsymbol{color_{remain}}$ (8 bit only)
Memory	N	1

needed in the final hardware implementation on a μC. Based on this summary of Table 4.1, the required memory storage M_{store} is computable as a function of the number of employed LEDs N_{LEDs} using the subsequent equation,

$$M_{store} = (3 \cdot N_{LEDs}^2 + 4 \cdot N_{LEDs}) \cdot r_{comp} + (3 \cdot N_{LEDs} + 3) \cdot 8\,\text{bit}\,. \quad (4.29)$$

In extensive simulation tests and evaluating temporary results using MATLAB® it was found that a minimum binary resolution of 7 bit in front of and 21 bit behind the decimal point are needed to achieve sufficiently accurate computations. One additional bit is necessary to consider the sign. Hence, a computation precision of $r_{comp} = 29\,\text{bit}$ is sufficient for all cases assuming fixed-point data [239]. The actual implementation on the μC however uses 32 bit floating-point computations. The nonlinear brightness adaption employing gamma correction also manages on these restricted binary resolutions achieving sufficient accuracy in both cases. Due to the limited computational effort, the color control algorithm is also suitable for implementations in very high speed IC hardware description language (VHDL) on a SoC. Thus, it is accounted for both kind of realizations on ASICs or a μC. For the largest case, which is the RGB-CAW luminaire, a memory demand of $M = 500\,\text{Byte}$ for $r_{comp} = 29\,\text{bit}$ and $M = 549\,\text{Byte}$ for $r_{comp} = 32\,\text{bit}$ is approximated, respectively. It should be noted that the calculated numbers of required memory space published in [239] are indeed a little bit higher. This deviation arises from a different assumption for the memory size of $\boldsymbol{L_{hom}}$. The issued paper [239] actually considers a memory allocation of N_{LEDs}^2 for $\boldsymbol{L_{hom}}$, which is however a too worst-case supposition because $\boldsymbol{L_{hom}}$ only describes the nullspace of matrix $\boldsymbol{C}$. While the associated memory demand is zero for three or less LEDs, it needs an additional factor

of N_{LEDs} for every further LED primary. The formula for the allocated memory space of $\boldsymbol{L_{hom}}$ denoted in Table 4.1 is hence only valid for $N_{LEDs} > 3$, otherwise it is zero. Even if the overestimated memory allocation of $M = 565\,\text{Byte}$ for $r_{comp} = 29\,\text{bit}$ and $M = 621\,\text{Byte}$ for $r_{comp} = 32\,\text{bit}$ according to [239] is taken, it is still a reasonable and manageable amount for a hardware implementation. Of course, additional effort is needed for the computation process itself including buffer registers. It is reported in literature about low power MCUs [310] that should be able to handle the proposed color control algorithm. Applying smart design methodologies like the one presented by Gemmeke *et al.* [124], powerful DSP building blocks can e.g. be realized at low power consumption in SoCs. Though, this is a matter of how the implementation is finally conducted and shall therefore not be considered in more detail here. In conclusion, it was possible to realize the proposed color control on a μC, which is the base for the simulation and measurements presented in section 4.5.

4.4 Application Related Improvements and Optimization for Precise Color Control

Chapters 4.1 and 4.2 introduced the basic idea and concept of the proposed color control algorithm as originally shown in [239]. Although the color control algorithm would already perform quite good in a real implementation like the one presented in chapter 4.3, it should be capable of handling certain boundary conditions and special application cases, which have not been considered yet. These application related conditions include e.g. the handling of transmitted CTs or the synthesis of color coordinates, which are situated outside of the displayable color gamut. Beyond that, certain improvement measures can be found aiming to further enhance color accuracy on both, component and system level. Considering the initial algorithm and its implementation the color control can be advanced by two means, which are first the way of handling negative scaling factors and second using multiple or a flexible, non-fixed optimization vector. On system level, more sophisticated approaches, which require higher hardware and software effort like a closed loop color control, can be introduced to improve color quality and precision. Although the presented color control algorithm is designed for PWM based LED drivers, it can easily be adapted for usage in lighting systems that employ amplitude modulation (AM), bilevel (BL) or hybrid dimming techniques. This section therefore briefly presents the mentioned application scenarios and improvements in the subsequent paragraphs. Most of these essential features, namely the ones described in sections 4.4.1 to 4.4.4, are directly implemented in the presented color control algorithm and

can hence be evaluated later in various simulations and measurements shown in chapter 4.5. The optional and more sophisticated methods, such as the adaption to other LED driving stages featuring AM, BL or hybrid dimming (4.4.5) or the employment of a closed loop control (4.4.6), are only theoretically discussed in a concise manner. Nevertheless it is briefly shown, how the latter two improvement approaches could be applied to the developed color control algorithm.

4.4.1 Handling of Color Temperature

Since color temperatures (CTs) or correlated color temperatures (CCTs) represent the temperature of an ideal black-body radiator, they reside on or close to the planckian locus (within any applied CIE chromaticity diagram) and thereby correlate to different hues of white light. This means that every CT or CCT can be reduced to a distinct set of (x, y)-coordinates within the CIE 1931 chromaticity diagram. Because the synthesis of distinct color coordinates is already completely realized by the proposed color control algorithm, CTs and CCTs can be handled identically, once they have been converted into a corresponding (x, y)-coordinate pair. The *"Smart Control Processing Unit"* consequently computes associated color coordinates according to the subsequent equations published by [181],

$$x_{CT} = \begin{cases} -0.2661239\dfrac{10^9}{CT^3} - 0.2343580\dfrac{10^6}{CT^2} \\ \quad +0.8776956\dfrac{10^3}{CT} + 0.179910 \end{cases} \text{, if } 1650\,\text{K} \leq CT \leq 4000\,\text{K}$$

$$\begin{cases} -3.0258469\dfrac{10^9}{CT^3} - 2.1070379\dfrac{10^6}{CT^2} \\ \quad +0.2226347\dfrac{10^3}{CT} + 0.240390 \end{cases} \text{, if } 4000\,\text{K} \leq CT \leq 25\,000\,\text{K} \tag{4.30}$$

$$y_{CT} = \begin{cases} -1.1063814x_{CT}^3 - 1.34811020x_{CT}^2 \\ \quad +2.18555832x_{CT} - 0.20219683 \end{cases} \text{, if } 1650\,\text{K} \leq CT \leq 2222\,\text{K}$$

$$\begin{cases} -0.9549476x_{CT}^3 - 1.37418593x_{CT}^2 \\ \quad +2.09137015x_{CT} - 0.16748867 \end{cases} \text{, if } 2222\,\text{K} \leq CT \leq 4000\,\text{K} \tag{4.31}$$

$$\begin{cases} +3.0817580x_{CT}^3 - 5.87338670x_{CT}^2 \\ \quad +3.75112997x_{CT} - 0.37001483 \end{cases} \text{, if } 4000\,\text{K} \leq CT \leq 25\,000\,\text{K}\ .$$

The actual implementation on the μC is therefore limited to the specified ranges of CTs. Considering daylight synthesis this is however more than enough. For this work, a CT range from 2000 K to 7500 K is assumed to be sufficient for proper daylight synthesis. The calculation rules declared in equations 4.30 and 4.31 are obviously also valid for the same specific CCT regions.

4.4.2 Mapping of Outside Gamut Points

A practical issue that might occur, particularly if employed luminaires are of a different lighting system or brand than the installed smart home system, is that transmitted color coordinates cannot be realized by the smart LED driver because they reside outside of the displayable gamut. While it can be thought of different ways to handle such a condition, this algorithm optionally provides two solutions in its hardware implementation. First, the color point is mapped towards the white point $E = (1/3, 1/3, 1/3)$. The intersection between this connection line and the color gamut boundary is taken as the point of synthesis. The second method computes the shortest distance between selected color point and the gammut border. In any case, the achieved deviation from the selected color point will be quite high. It is therefore more important to functionally handle this case somehow in the hardware implementation than to realize best color precision for this condition, which is indeed not really possible.

4.4.3 Handling of Negative Scaling Factors: Optimization with an Intelligent Elimination Routine

Depending on the employed LED configuration the color control algorithm may compute negative factors $\boldsymbol{f}$ for one or more LEDs in certain areas of the gamut after a first run. Negative scaling factors are a mathematical but not a practical solution in LED color synthesis since these coefficients represent the emitted (non-negative) intensity of their corresponding LED. Therefore, they cannot be realized due to these physical constraints and are consequently forbidden as explained in the beginning of chapter 4.1.

There are different ways of handling a situation with negative scaling coefficients. While it is possible to influence the computed factors by choosing specific optimization vectors, this measure is not always constructive since it might produce results with bad or reduced color quality. Another alternative is to run the color control algorithm with a reduced set of LEDs for these particular cases. Again, different optimization strategies are possible here. The implementation presented in section 4.3 simply eliminates the first color with a negative factor following a clockwise order in the CIE 1931 chromaticity diagram from blue to

white (B-C-G-A-R-W). A more robust technique, which has consequently been selected as the default option of this color control algorithm, is to delete the LED, which features the biggest negative scaling factor according to

$$f_{neg,max} = max\left(|f_{<0}| \cdot \frac{y_i}{Y_i}\right). \tag{4.32}$$

Since both choices are however somehow arbitrary and might yield to conflicts, such as a limited gamut that is not capable of synthesizing the desired color points $\boldsymbol{p}$ anymore, it might be more beneficial to take an LED away, which is not restricting the displayable gamut regarding the desired color coordinates to be synthesized. To deal with negative scaling coefficients in a more suitable way, a so-called area request is conducted, which removes an LED for the subsequent run regarding a specialized instruction. Consequently, a simple intelligent elimination routine is developed for three possible configurations of LED sets, which are RGB-CAW, RGB-W and RGB-A. All elimination rules basically rely on an area request of the displayable gamut. It is thereby checked, where the desired color point is situated. The displayable color gamut is in fact subdivided into different regions, each containing a list, of which LED is deleted first for the next run. Fig. 4.5 shows the specified regions for an RGB-CAW luminaire. The small letters indicate color and descending order of LEDs to be removed for the next synthesizing run. If a new color point is being transmitted, the control algorithm obviously starts all over with the complete set of equations containing all available LEDs installed in the system.

The area request for an RGB-W luminaire is much simpler. Based on the white LED, which is situated more or less in the center of the gamut, three connection lines can be drawn to the red, green and blue LED, respectively. This results in three triangles that are spanned by the corresponding LEDs situated in the corners. In case negative scaling factors occur, it is checked in a first step, whether the chosen color point is located in a radius smaller than 0.02 around an LED primary valence. In this case, the white LED is eliminated. Otherwise, the algorithm eliminates in case of occurring negative scaling coefficients the LED, which is not belonging to the respective triangle but lies on its opposite side. For RGB-A it is found that only color points in the bluish area show negative factors in some cases. If the selected color point features coordinates with $x \leq 0.4$ and $y \leq 0.2$, amber (A) is removed at first.

All area requests can be further optimized, particularly if considering that the RGB-CAW case handles quite small elimination regions. In addition to an intelligent elimination routine, it might e.g. be desirable to change the optimization vector $\boldsymbol{s_{opt}}$ adaptively or in dependence of the respective (x, y)-region to further improve light quality as outlined in the next paragraph.

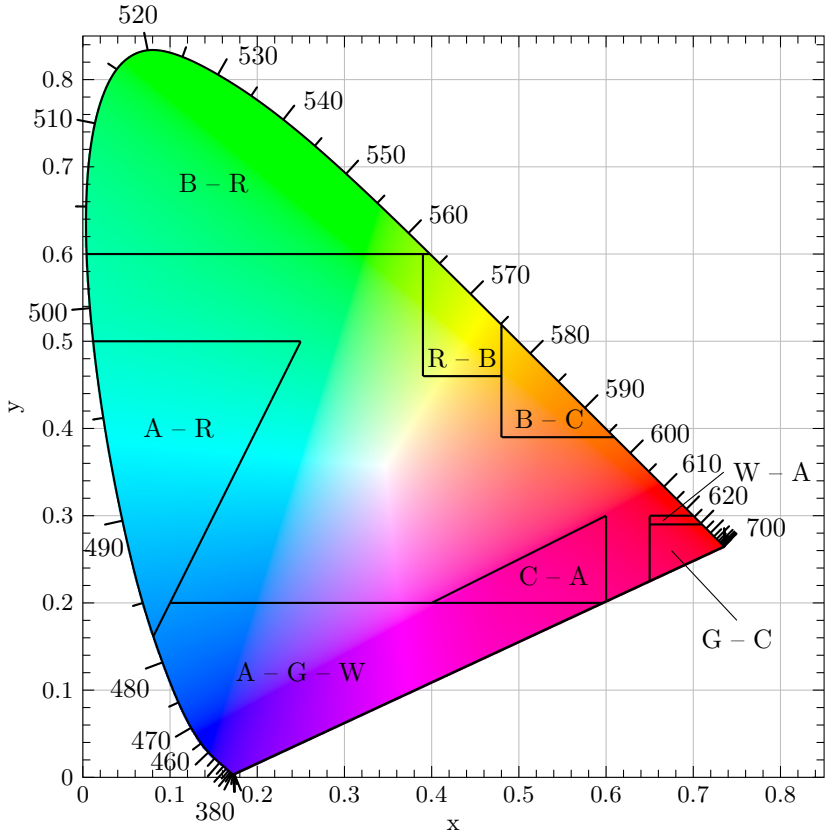


Figure 4.5: Color gamut of an RGB-CAW configuration highlighting specific areas with removable LEDs in descending order.

4.4.4 Adaptive Optimization Vector

As explained in section 4.1, the optimization vector $\boldsymbol{s_{opt}}$ significantly impacts the determined solution for the color synthesis of a chosen color point $\boldsymbol{p} = (x_P, y_P)^T$. Hence, it represents a suitable measure to influence the color control algorithm selectably towards improved color precision, better spectral distribution, higher CRI and so forth. One general improvement that can be thought of in this context is to shape the optimization vector $\boldsymbol{s_{opt}}$ in dependence of the selected

color point and the optical properties of employed LEDs. The key idea therefore is to cleverly set the LED weightings of the optimization vector in a flexible manner according to two main properties, which are

1. the distance $dist_i$ between each LED and the selected color point $\boldsymbol{p}$ and
2. the corresponding spectral intensity distribution of the respective LED.

Combining both parameters and scaling each in a proportional and exponential manner results in the final weighting factor for each LED according to equation

$$s_{opt,i} = k \cdot \left(\frac{1}{dist_i}\right)^a \cdot (X_i + Yi + Z_i)^b = k \cdot \left(\frac{1}{dist_i}\right)^a \cdot \left(\frac{Y_i}{y_i}\right)^b . \quad (4.33)$$

The exponents a and b as well as the proportional constant k can be freely chosen. Hence, also negative values are allowed to be selected. Best matching for CT synthesis with an adaptive optimization vector was achieved by using the settings listed in Table 4.2, while the proportional constant was always set to a value of $k = 1$.

Table 4.2: Settings used for an adaptive optimization vector in different luminaire configurations aiming for high CRI over a large CT range.

LED configuration	Exponent a	Exponent b
RGB-CAW	1	2
RGB-W	2	2
RGB-A	1.8	0.8

Of course, also other mathematical combinations of the mentioned parameters, color point distance and spectral distribution, are conceivable that could be applied to find an improved solution with respect to certain optimization criteria. In the end, the use of an adaptive optimization vector implies an additional computational effort. Every time a new color coordinate is selected, the distance to each LED primary needs to be calculated and subsequently equation 4.33 (or another calculation rule) needs to be evaluated for selected settings like the exponents a and b. While this procedure is rather uncritical for a μC implementation, it might cause a large area impact in an ASIC realization. Depending on the desired application, it needs to evaluated, if the considerable effort is worth to be taken. In this work, an adaptive optimization vector is implemented and may be used for the evaluation in chapter 4.5.

4.4.5 Adaption of Color Control Algorithm to Other Dimming Techniques

The presented color computation algorithm may also be applied to AM, BL or hybrid dimming approaches. However, a different mapping procedure for the individual channel brightnesses has to be found as the color coordinates of employed LED primaries vary in dependence of the selected LED forward current and emitted luminance might deviate from the approximated linear behavior. These effects can be taken care of by a proper calibration and storing the corresponding information in one or more specific LUTs. Beyond storing calibration and configurations of color coordinates and dimming profiles for different LED forward current levels, these LUTs may also provide information on temperature dependent behavior.

Because BL dimming operates similar to the PWM-mode except for a non zero current level during the off time, the developed color control algorithm could indeed be used without any change. The LUT only needs to specify corresponding (x, y)-coordinates for selectable sets of current amplitudes. When using BL dimming, it has to be considered that the actual dynamic dimming range is reduced in contrast to the PWM-mode as outlined in detail in section 2.3.1. In case of using AM or hybrid dimming techniques, the control algorithm needs to take care of the nonlinear dimming profile with respect to the selected LED forward current by a calibrated LUT as mentioned above. Additionally, a translation unit, e.g. a resistive DAC (RDAC), is needed to convert the digitally computed relative intensity distribution into different analog amplitudes of LED forward current I_{LED}. Applying an LED driving stage like the solution presented in chapter 5, an RDAC could be used to either trim the current sensing resistor or the programmable reference voltage. Considering an ASIC implementation, it is easier to change the reference voltage because the sensing resistor is often placed outside of the chip on the PCB by means of a high precision device. The same is valid for many other LED driver architectures, e.g. hysteretic buck converters using a simple RS flip-flop to regulate the converter's output current in dependence of sensing and reference voltages. Tuning the hysteretic threshold levels by a digitally controlled translation unit, such as an RDAC, hence does the job. Systems relying on PWM control but suffering from a duty cycle limitation, like the ones presented in [102], [109], may still use the basic functions of the proposed color computation algorithm as they are. However, these solutions would require minor adoptions in the final PWM mapping procedure to account for their respective physical limitation. The duty cycle limitation consequently implies a decreased dimming range and might in dependence of the actual switching frequency lead to perceivable flicker as

explained in section 2.3.2. The flickering is only attributed to the deployed LED driving circuitry and accompanied limitations. Beyond that, these systems might also require sequential color shifting due to the duty cycle limitation. The smart control processing unit hence needs to take care to output the correct PWM duty cycles for the respective color at the demanded point of time.

In conclusion, the proposed color control algorithm is suitable for a large variety of LED lighting systems and driving stages. Due to its good flexibility the proposed color mixing strategy can be utilized in all of these approaches with only some minor modifications.

4.4.6 Enhanced Color Quality by Closed Loop Control

A very nice, but complex method to enhance color precision and light quality in terms of $\Delta u'v'$, ΔE or CRI is to employ a closed loop control with an accurate color sensor or a (micro) spectrometer. In this way it is possible to measure the emitted tristimulus values X, Y and Z of the synthesized color point. Consequently, the realized color coordinates can be calculated and a compensation mechanism may be applied. Different approaches have been presented in scientific work using color sensors [58], [99], [200], [428] or spectral measurements [72], [233] for the feedback control as described in section 2.2.3. A suitable product for such a color sensor, which has been installed in the self-developed luminaires highlighted in Fig. 4.16 as well as in appendix section C, is one of the company MAZeT [366]. Such a color sensor could be situated inside of a luminaire or in an external sensor node. In any case, the closed loop control would require a complex regulation mechanism that is capable to compensate visual effects with sufficient accuracy. In addition to that, the color control algorithm must be calibrated from time to time according to the (x, y)-coordinates of each employed LED primary. The closed-loop control method with a color sensor or micro specrometer is indeed beneficial as it would compensate for different parasitic inductions, such as changes of ambient temperature, variations on flowing LED current, inaccuraccies in circuit designs like bandgap references and so on. Beyond that, it could also be combined with other sensors, e.g. with those performing current or temperature measurements, to ensure more precise color regulation. For further details please refer to the literature review provided in sections 2.2.3, which names several research studies employing these complex regulation routines. Due to the extensive amount of optimization strategies, this field of color science is left open for future work. Nevertheless, the developed color control algorithm could operate in such a closed loop control system, if provided with the compensated (x, y) coordinate pair that is meant to be realized.

4.5 Experimental Validation of the Optimized Color Control Strategy

The color control algorithm has been implemented in an extensive MATLAB® program as well as on a μC for different hardware implementations of an intelligent luminaire. Thereby, the algorithm can be validated with both simulation and measurement results for different LED configurations. Luminaires with six (RGB-CAW) and four (RGB-A, RGB-W) primary valences have been investigated in simulation and experimental test setups. For all investigations the Luxeon Rebel LEDs of Phillips (now Lumileds) have been employed in the respective colors [342], [376]. Their optical spectra including intensity levels have been transfered from the technical data sheets [342], [376] into the MATLAB® program and also on the μC for all computations. CRI, ΔE and $\Delta u'v'$ are computed to the standard formulas mentioned in section 2.2.2

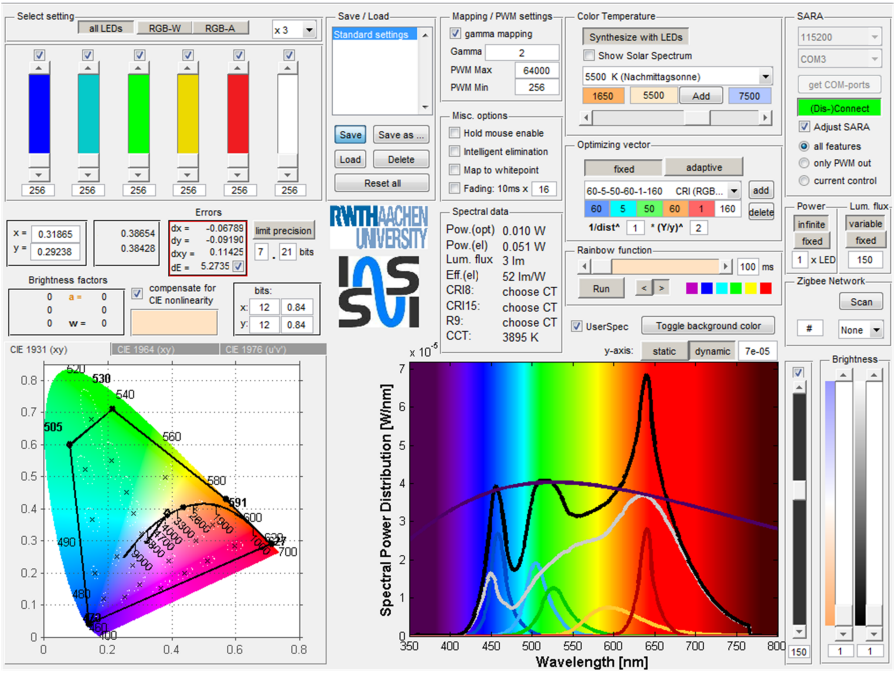


Figure 4.6: GUI of self-developed MATLAB® program for simulation and calculation of color synthesis with a selected set of LEDs.

according to equations 2.16, 2.15 and 2.11, respectively. The CRI calculations thereby use eight reference spectra as listed in [312]. It should be noted that the MATLAB® program, which is shown in Fig. 4.6, already accounts for physical constraints of the realized hardware implementation, such as a limited binary resolution of $r_{comp} = 29\,\text{bit}$ for any computation. From the computational perspective, the simulation results thereby represent close approximation to real measurement results. If perceptible deviations of the synthesized color coordinates or CTs between simulation and measurement occur, it is expected that they mainly originate from process variations or other non-ideal effects related to the utilized hardware, such as LED current accuracy, varying ambient temperature or optical properties of the employed LEDs [239]. These causes and contributions can however be compensated by a proper calibration of x_i, y_i, and Y_i from the measured curves to the data sheet information for different temperatures and LED current amplitudes.

4.5.1 Simulation Results of the Proposed Color Control Algorithm

For HCL application it is essential to synthesize sunlight or daylight with an LED based luminaire in order to adopt the indoor artifical lighting to the natural circadian rhythm as described in section 2.2.4. Therefore, the realization of different CTs in the range from about 2000 K(sunrise/sunset) over 3500 K(golden hour) and 5500 K(midday) to 7500 K(foggy sky) is very important. Also, the adaption to other thermal radiators like an incandescent lamp (40 W: $CT \approx 2600\,\text{K}$) is of high interest. When synthesizing these white light sources or moreover their respective CTs, the proposed color control algorithm aims for optimum light quality, which demands a very good color rendering ($\text{CRI} \geq 90$) and minimum color shift ($\Delta E \leq 3$ or $\Delta u'v' \leq 0.035$) at the same time. In doing so, it is furthermore desired to realize a nice continuous spectrum emitted by the LED based luminaires under test like that of an ideal black-body radiator according to equation 2.17. Fig. 4.7 shows the emitted optical summation spectrum simulated for all three luminaire realizations at a CT of 5500 K and maximum luminous output. Although the different spectra still contain certain bumps, it is clearly noticeable that adding additional LED primaries helps to create a smoother spectral progression of the emitted intensity. All luminaire configurations realize indeed very high CRI values that are greater than 90, while maintaining a non-perceivable color shift of $\Delta E < 1$ as noted in the legend of Fig. 4.7.

Using a fixed optimization vector, the proposed color control algorithm yields similar results of a very high light quality for all three luminaire configurations

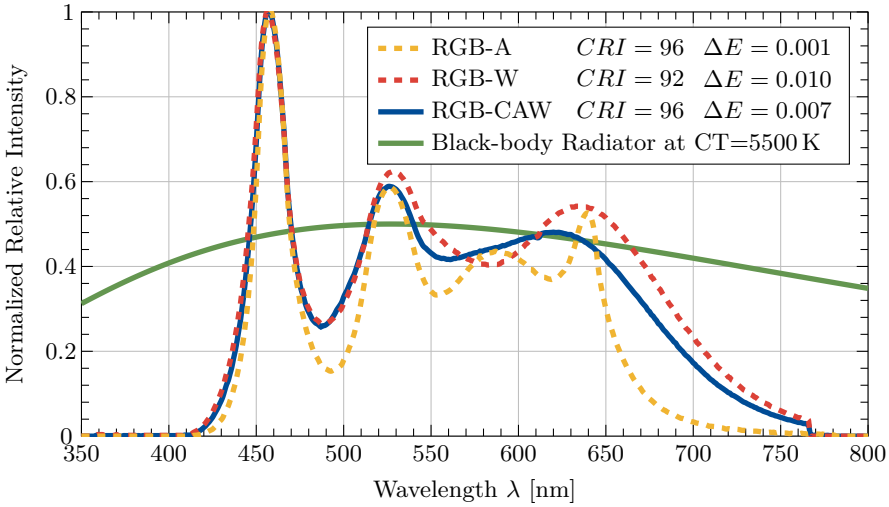


Figure 4.7: Simulation of emitted optical spectrum for three different luminaire configuarions at CT=5500 K and maximum lumiance L_v.

over the entire CT range as illustrated in Fig. 4.8 to Fig. 4.12. Besides optimizing the optical spectrum for high CRI values and minimizing perceivable color deviations, the presented control approach also enables trimming towards other optimization criteria, such as maximum luminous output (lm) or efficiency ($\frac{\text{lm}}{\text{W}}$), by applying different optimization vectors $\boldsymbol{s_{opt}}$. Table 4.3 summarizes the used weightings of the fixed optimization vectors $\boldsymbol{s_{opt}}$ for each luminaire configuration and desired optimization parameter.

Fig. 4.8 depicts the simulation results of achieved CRI versus selected CT. For drawing a fair comparison among the different CTs, the emitted luminance

Table 4.3: Weightings of fixed optimization vectors $\boldsymbol{s_{opt}}$ for three different luminaire configurations and optimization parameters.

Optimization Criterion	**R-G-B-C-A-W**	**R-G-B-W**	**R-G-B-A**
Max. Lumen	10-18-35-40-25-30	100-79-1-95	10-25-50-25
Max. Efficiency	1-1-1-1-1-1000	1-1-1-1000	1-1-10-1
Max. CRI	60-5-50-90-1-160	60-60-1-850	1-8-100-70

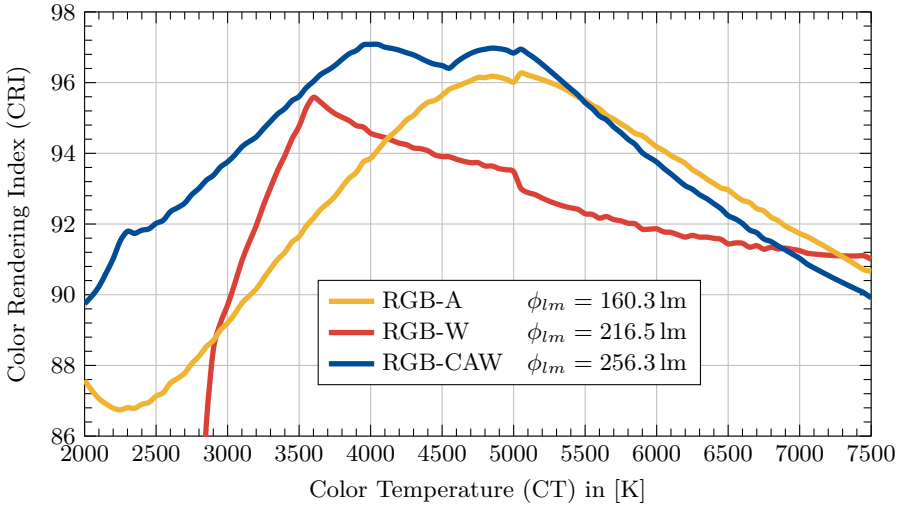


Figure 4.8: Simulation of CRI versus CT for three different luminaire realizations at maximum constant luminous flux.

is kept constant over the entire CT range at the highest possible level for each luminare configuration. The realized constant luminous flux ϕ_{lm} is listed in the corresponding legend of Fig. 4.8 for each LED configuration. Further simulations however showed that the impact of keeping ϕ_{lm} constant versus a varying luminous output is not very strong. In all cases, the CRI remains greater than 90 for a very wide color temperature range lasting from 3200 K to 7500 K. For low CTs ($< 3000\,\mathrm{K}$), CRI behaves very differently among the three luminaire realizations. While the CRI of the RGB-W implementation decreases drastically in this range, the other two configurations maintain good to very good results featuring CRI values that are more than acceptable. This matter exemplifies the difficulty of achieving high light quality in a low CT region as stated by Chakrabarti *et al.* [59]. The results for RGB-A actually drop slightly below the target value of CRI = 90, whereas the RGB-CAW realization features a CRI that always exceeds this desired minimum boundary. If optimizing for high CRI values, using additional LED primaries hence becomes particularly beneficial in the low CT range indicating "warm white light". Especially using an amber LED boosts CRI significantly compared to adding a standard white LED. It was furthermore observed that CRI remains nearly identical over a wide dimming range and is mostly independent of the selected brightness value.

Thus, very good color rendering is also achieved for low light intensities. Still, CRI becomes worse at very low brightness levels due to the physical limitations considered for an actual LED driver implementation.

Besides featuring high CRI values, the color control algorithm simultaneously minimizes the color distance over the entire CT range. Fig. 4.9 illustrates the color difference ΔE versus selected CT, while identical settings, such as optimization vector and emitted luminance, have been maintained. It can be seen that ΔE remains lower than 0.28 for all luminaire realizations over the entire CT range. This is an excellent result because color shift just becomes distinguishable by the human eye for $\Delta E > 1$ and $\Delta E < 3$ is still classified to be acceptable for most lighting applications [432]. The visible peaks occur due to the considered minimum on-time $t_{on,min} = 4\,\mu s$ of the PWM, which corresponds to a minimum number of 256 steps of the 16 bit resolution. If shorter on-times are realized, the minimum step number could be decreased accordingly, thus allowing for higher precision in the LED duty cycle control minimizing such peaks in ΔE. In addition to investigating ΔE, color distance $\Delta u'v'$ has been simulated for the same CT range and identical settings. The corresponding results appear very similar, as shown in Fig. 4.10, and thus confirm the observed and stated conclusions. As mentioned earlier, this behavior is actually expected considering the maximum brightness level to which ΔE is referred to. At maximum brightness ΔE and $\Delta u'v'$ should thus yield identical results.

Typically, color distance ΔE strongly grows with decreasing luminance. Investigating Fig. 4.11 yields the insight that the proposed color control algorithm also minimizes color distance for lower light intensities. Even at a brightness level of 50 %, ΔE remains mostly within tolerable limits over the entire CT range. Only the RGB-W configuration slightly exceeds the $\Delta E = 1$ boundary around CT $\approx 3050\,K$ but still remains far below the acceptable $\Delta E < 3$ limit. Decreasing the brightness level even further down to 20 % leads to a noticeable effect on ΔE. Only the RGB-CAW configurations remains below the tolerable limit of $\Delta E < 3$ and is in most cases still below the non-visible $\Delta E < 1$ boundary. Again, the performance of the RGB-A setup is quite remarkable as it resides also below $\Delta E < 1$ for nearly the entire CT range. Only in the very low CT region its ΔE performance becomes slightly worse and experiences a peak up to a maximum of $\Delta E = 3.2$. RGB-W again shows the worst results as its ΔE peaks above a value of 3 in the interesting region between 3000 K to 4000 K. In all cases and different brightness values, the visible peaks result again from the minimum duty cycle considering a hardware realization with a finite minimum on-times of the employed LED driver. Regarding perceivable color difference, the RGB-A realization finally performs best, whereas RGB-CAW and RGB-W yield comparable results with a slight advantage for the implementation

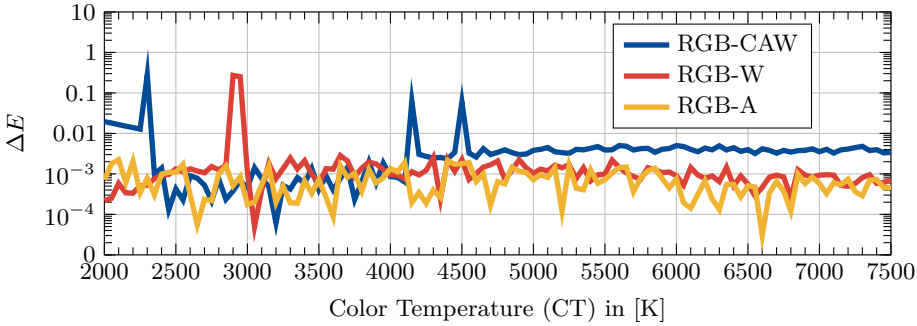


Figure 4.9: Simulation of color difference ΔE versus CT for three different LED configurations at maximum constant luminous flux.

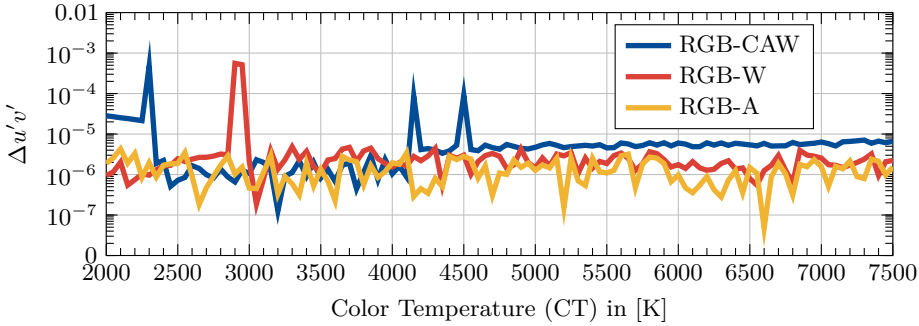


Figure 4.10: Simulation of color distance $\Delta u'v'$ versus CT for three different LED configurations at constant luminous flux.

with six distinct LED primaries. Including the CRI performance, RGB-A thus represents a good trade-off between achievable light quality and hardware effort. Still, it should be noted that luminous efficacy is slightly worse compared to the RGB-W case.

Finally, the absolute deviation between desired CT and realized CCT is investigated. Realized CCT is computed according to the selected (x, y)-chromaticity coordinates using equations B.1 and B.2 from appendix section B.2 as derived in [144] and [260]. Fig. 4.13 shows that a very small deviation of less than $\pm 50\,\mathrm{K}$ is achieved for all luminaires under test. Even for a dimming level of 70 %, the deviation ΔCCT remains smaller than $\pm 50\,\mathrm{K}$. Thus, a superior performance

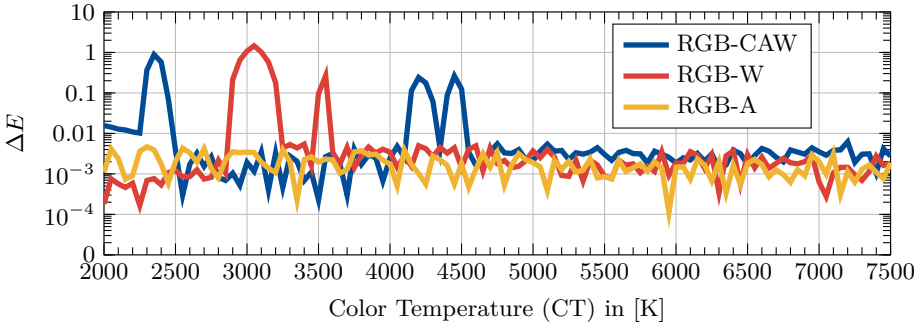


Figure 4.11: Simulation of color difference ΔE versus CT for three different LED configurations at 50 % brightness level.

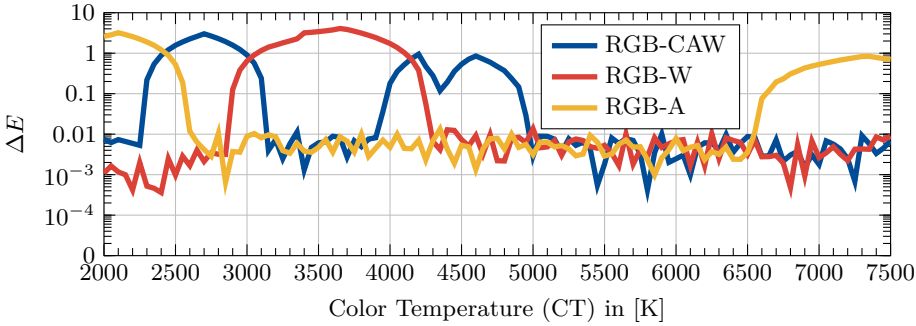


Figure 4.12: Simulation of color difference ΔE versus CT for three different LED configurations at 20 % brightness level.

compared to [315] is achieved. This performance is kept up until a dimming level of 43 % is reached. At a dimming level of 40 %, a ΔCCT of around ± 50 K can be maintained for the RGB-A and RGB-CAW luminaire. The RGB-W luminaire becomes slightly worse, but still features a ΔCCT of less than ± 100 K. With decreasing brightness level the performance obviously becomes worse due to the physical limitations of a finite computational resolution and a required minimum on-time considered for a real LED driver as the one presented in chapter 5. Nevertheless, the ΔCCT error remains below ± 50 K at 31 % dimming for the RGB-A case, whereas the RGB-CAW setup features a $\Delta CCT < \pm 100$ K and the RGB-W configuration still shows a $\Delta CCT < \pm 150$ K.

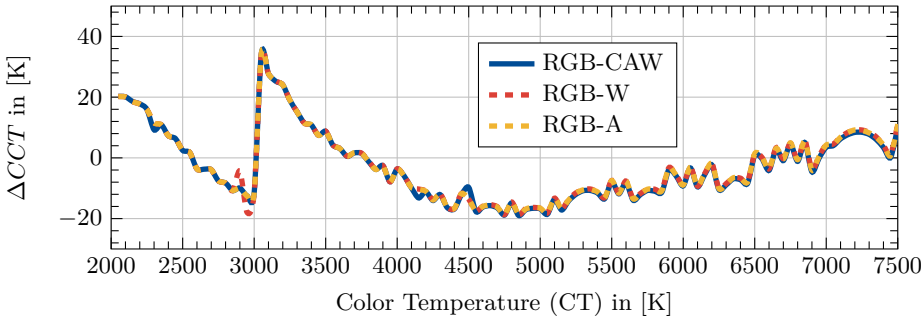
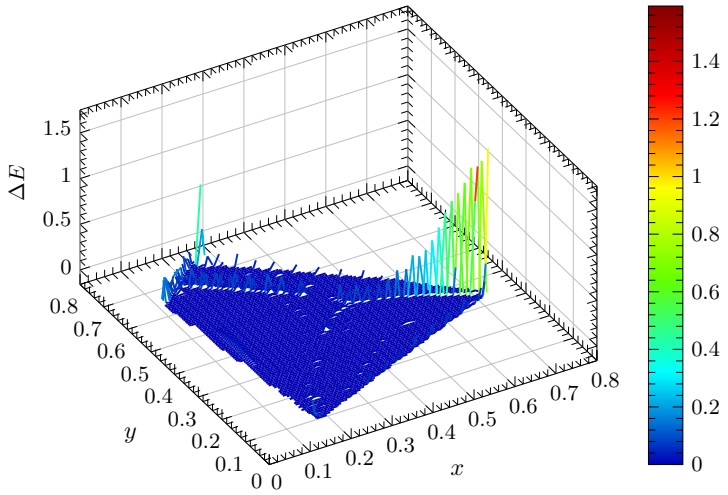
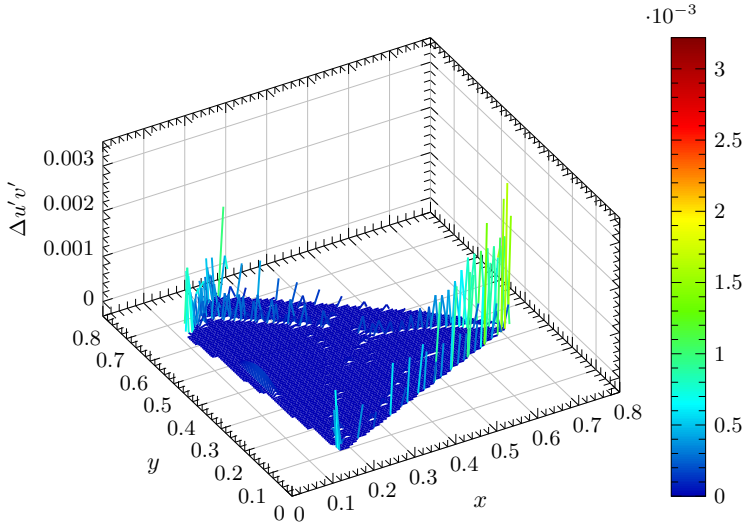


Figure 4.13: Simulation of ΔCCT versus CT for three different LED configurations at maximum constant luminous flux.

In order to illustrate the superior performance of the proposed algorithm, color distance ΔE and color shift $\Delta u'v'$ have been plotted over the entire displayable gamut for the RGB-CAW configuration at maximum luminance with an adaptive optimization vector using exponents $a = 1$ and $b = 2$ and employing the intelligent elimination routine proposed in section 4.4.3. Fig. 4.14a and Fig. 4.14b present the corresponding three-dimensional graphs. It can be seen that ΔE and $\Delta u'v'$ remain below their tolerable limits of $\Delta E < 3$ and $\Delta u'v' < 0.0035$, respectively, over the entire gamut. In fact, for most of the displayable gamut area the color control algorithm maintains even the non perceivable tolerances as ΔE and $\Delta u'v'$ reside below 1 and 0.002, respectively. Just in close proximity to the LED primaries, certain spikes in the color deviation metrics are observable. While this is not a major issue for most of the gamut area, this effect is particularly noticeable in the very deep reddish region. It is thus expected to improve performance in this matter by fine tuning the area request or finding more suitable optimization vectors. In conclusion, the achieved performance represent excellent results in terms of color accuracy and outperforms other scientific research work [59], [315], [324], [428]. It is therefore interesting to see, if this performance can be kept up within real measurements shown in the subsequent section 4.5.2.



(a) Simulation of ΔE at maximum brightness with an adaptive $\boldsymbol{s_{opt}}$ ($a = 1$; $b = 2$).



(b) Simulation of $\Delta u'v'$ at maximum brightness with an adaptive $\boldsymbol{s_{opt}}$ ($a = 1$; $b = 2$).

Figure 4.14: Simulation of color shift over the entire displayable gamut for an RGB-CAW configuration using the intelligent elimination routine.

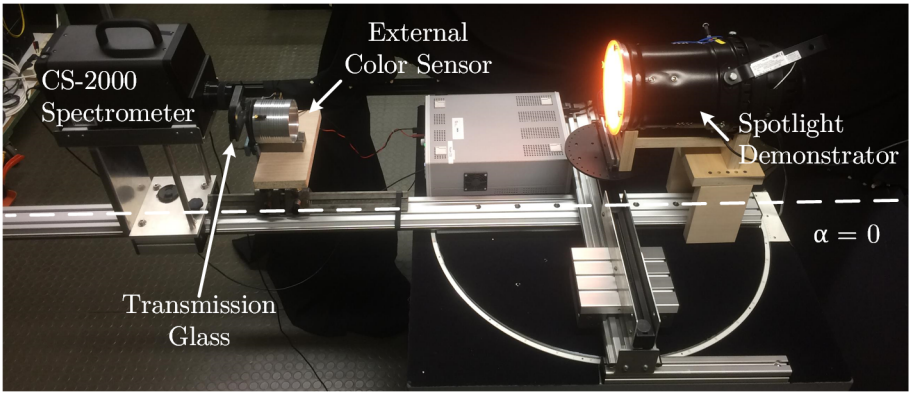
4.5.2 Measurement Results of the Proposed Color Control Algorithm

Validating achieved color quality in real measurements is considerably harder than proofing functionality and performance in various simulations. The main issue in this context is that the emitted optical spectrum of each LED may vary significantly in dependence of external conditions that are difficult to control or monitor. LED junction temperature, LED forward voltage variations or the precision of the analog current flowing through employed LEDs represent the key parameters in this context as explained in sections 2.2.2 and 2.3.1. These metrics might consequently be affected and may influence the optical performance of achievable color quality in a critical manner. Hence, it is important to install a proper measurement setup and conduct a precise calibration of the LEDs' (x, y)-coordinates used in the proposed color control algorithm.

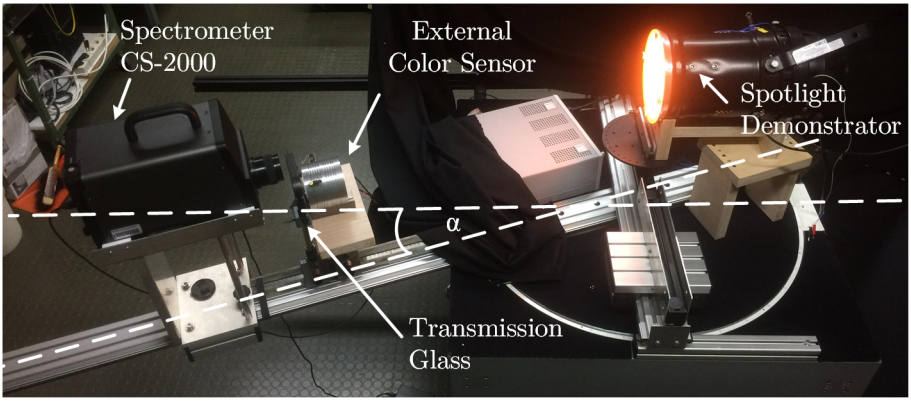
Measurement Setup

Fig. 4.15 shows the used measurement setup of the self-constructed spotlight luminaire, which has also been used for DLT verification in chapter 3. This light source realizes the RGB-CAW LED configuration, while it provides two additional white LED channels for increasing the luminous output, if desired. Each of these eight LED channels contains six series-connected LEDs of the same color type. The physical layout and distribution on the PCB arranges all LEDs in six cluster sets of the desired RGB-CAW structure plus an additional inner and outer circle of white light LEDs. Fig. 4.16 shows the corresponding setup inside of the spotlight luminaire. The LED current flow in each of these eight LED channels is regulated by a discrete implementation of the LED driver presented in chapter 5. In this way, the current deviation of each channel is aimed to be kept within 1 % to 2 % [236], [237]. A deeper insight into the physical setup, PCB layouts and construction of the spotlight demonstrator is provided in appendix C.1.

All spectral data have been obtained using the *"Konica Minolta Spectroradiometer CS-2000"* [35], which enables accurate measurements of the visible spectrum in the range from 380 nm up to 780 nm featuring a precision of 0.3 nm. The CS-2000 calculates (x, y)-coordinates from the obtained spectrum with an accuracy of $\Delta x = \pm 0.0015$ and $\Delta y = \pm 0.001$. Spectrometer and luminaire are precisely positioned vis-à-vis from one another, in a 0° angle and with the spectrometer's object lens being centered to the middle of the luminaire. Fig.4.15a illustrates a photograph of this measurement configuration. The CS-2000 spectrometer is mounted on a fixed axis that can be rotated with an angle accuracy of 0.1° with respect to the measurement table, on which the



(a) Measurement setup for a straight viewing angle ($\alpha = 0°$).



(b) Measurement setup for a tilt viewing angle ($\alpha > 0°$).

Figure 4.15: Measurement setup for spectral recordings of self-constructed spotlight luminaire under different viewing angles.

luminaire under test is situated. In this way angle dependent measurements of the emitted optical spectrum are conducted to check, whether the optical performance is also met under different viewing angles. A high quality light source should maintain its optical performance (regarding CRI, ΔE, $\Delta u'v'$, etc.) also under different viewing angles, which is indeed a challenge. Fig.4.15b exemplifies the measurement setup for a non-zero rotation angle α.

Because the emitted luminance of the RGB-CAW spotlight luminaire saturates the spectrometer at higher brightness levels in the presented setup, a transmission glass has been inserted in front of the shutter of the CS-2000 to attenuate light intensity accordingly. This transmission glass is hence kept installed for all conducted measurements in order to maintain the same optical measurement path. However, it is essential to compensate for its inherent transmission characteristic, which may deviate in dependence of the optical wavelength. Prior to the color quality measurements of the RGB-CAW light source, a proper calibration of the transmission glass is therefore recorded using a conventional incandescent lamp as the light source since it operates as a thermal radiator. These calibration measurements finally yield computation of a compensation factor curve in dependence of the wavelength, which is later used to correct recorded measurement spectra accordingly.

A measurement PC controls the spotlight luminaire by using the self-developed MATLAB® program and transmits the desired CTs, color coordinates (x, y) and brightness information to the luminaire. Furthermore, it also connects the CS-2000 spectrometer and a temperature sensor with four measurement probes via USB to record all relevant measurement information at once and feed those back to the MATLAB® program. Additionally, an external color sensor node, which is positioned directly below of the spectrometer is also attached to the measurement PC, although it was not used in the end for the final recordings.

Because optical characteristics of each LED may vary significantly in accordance to the junction temperature, monitoring the ambient temperature turns out to be very important and performance critical as it is proportional to emitted luminous intensity. In order to gain reproducible results, continuous temperature measurements are therefore taken establishing an automated calibration and measurement routine as outlined in the following paragraph. For this reason, the four independent measurement probes (T_1-T_4) are mounted at different positions on one of the six RGB-CAW LED spots monitoring the current temperature present at this LED spot. Fig. 4.16 also illustrates the corresponding setup and positioning. The measurement PC continuously reads the temperature information out and computes the average value of all four probes. This mean temperature is subsequently used as the main control variable for the automated measurement routine.

Automated Measurement Routine

The adjustment of different CTs and (x, y)-coordinates results in different junction temperatures of the employed LEDs because a warm white ($\approx 2700\,\mathrm{K}$) color synthesis requires e.g. higher shares of red and amber LEDs, whereas

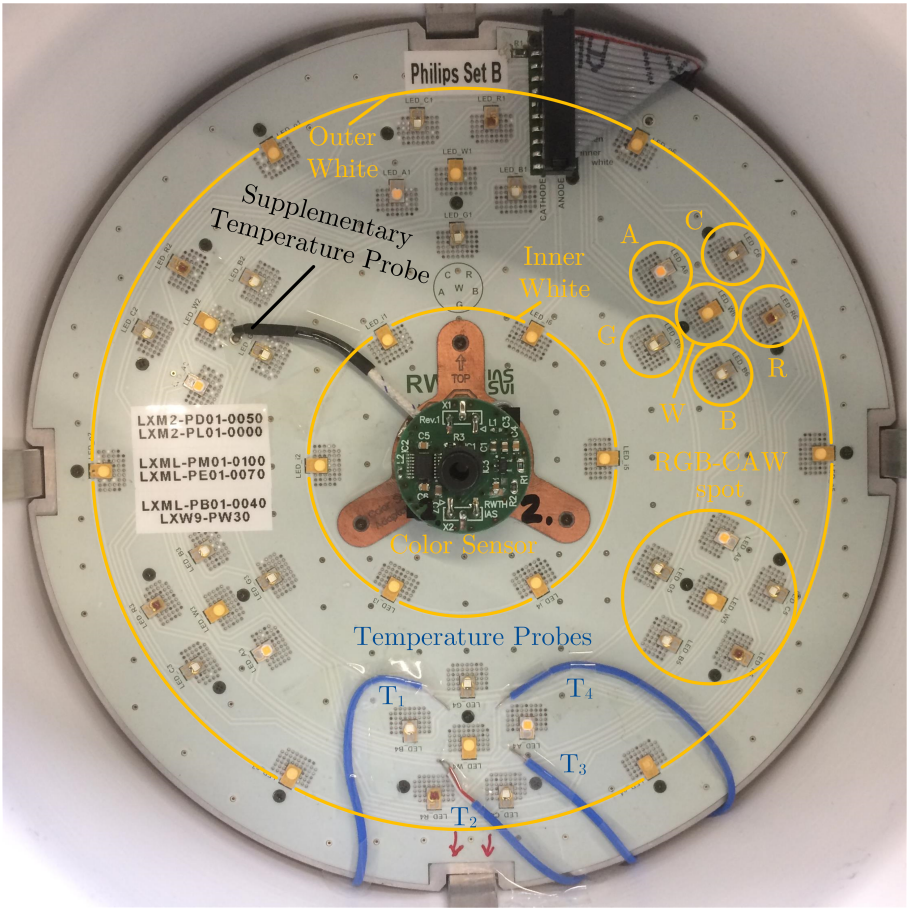


Figure 4.16: Internal configuration of LED spotlight luminaire demonstrator with color sensor and temperature measurement probes.

colder CTs ($\approx 5500\,\mathrm{K}$) imply stronger portions of the blue LED. The difference in junction temperature among employed LEDs leads in fact to strong deviations in the optical performance, which has been assessed during several initial tests for the investigations conducted in this thesis. Particularly at room temperature it was difficult to maintain stable surrounding conditions. Once the luminaire is switched on, it heats its heat sink up very quickly, and once it is switched off,

temperature degrades relatively fast again. Although temperature deviations typically happen comparatively slowly, the underlying temperature variation process of these experiments was fast and strong enough to influence the results significantly, especially for lower ambient temperatures. The automated measurement routine therefore aims to keep the average temperature at the LED spot more or less constant to maintain comparable measurement conditions for all conducted experiments. This matter is important for two reasons. First, the spectral measurement of a select (x, y)-coordinate may take some time. Keeping the ambient temperature more or less constant, thus yields good reproducibility between different measurements of the same color coordinate. Second, color accuracy of synthesized color coordinates shall be recorded over the entire CT range or even an entire color gamut area. Besides reproducibility, constant temperature conditions thereby allow for comparing the achieved color precision among the broad variety of realized (x, y)-coordinates.

Using the measured average temperature at the LED spot, the automated measurement routine operates as follows. In a first step, the control routine enables all LED channels at maximum brightness until a defined pre-heating temperature T_{pre} is reached. For the conducted experiments T_{pre} was set to 47 °C. Subsequently, the control routine waits until the average temperature has dropped back down to a desired measurement temperature $T_{measure}$, which is chosen to 40 °C in this work. While this decreasing process progresses fast in the beginning, it slows more and more down approaching $T_{measure}$ until it takes more than half a minute for the last decimal places to settle. Hence, this method ensures relatively stable temperature conditions, when turning the luminaire on. This procedure is also the reason for the relatively long measurement time of a single color point. Once $T_{measure}$ is reached, the luminaire turns on immediately and adjusts to the targeted color point. Waiting for a minimum delay time, the controlling PC then starts the spectrometer measurement, which actually happens within less then several seconds. The measurement routine pushes the CS-2000 to take three spectra for each measurement point, stores the three spectral curves on the PC's harddisk, evaluates optical paramteters of interest, such as CRI or $\Delta u'v'$, from the recordings and finally averages the computed parameters over all three samples. In this manner, the automated measurement routine performs both, the initial LED calibration as well as the subsequent color quality measurements of the luminaire under test.

LED Calibration

In an initial step, before the actual CT and color point measurements of the gamut can be started, the individual LED primaries have to be calibrated

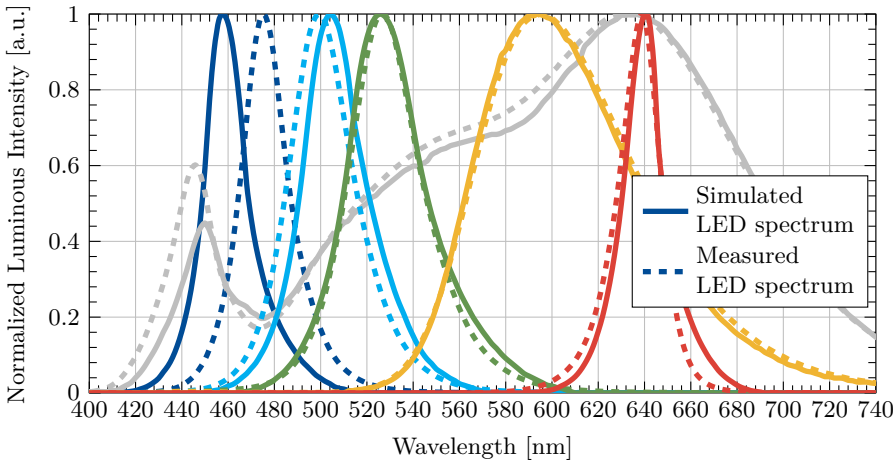


Figure 4.17: Comparison of measured LED spectra at $T_{measure} = 40\,°C$ with the datasheet based LED spectra used for simulation.

according to their actual (x, y)-coordinates in the CIE 1931 chromaticity diagram and emitted luminance L_v or luminous flux ϕ_{lm}. This step is inevitable for two reasons. First, the spectra of the employed LEDs might actually deviate from the datasheet information. This effect is demonstrated in Fig. 4.17 by plotting LED spectra measured at $T_{measure} = 40\,°C$ (dashed lines) and datasheet based LED spectra (solid lines), which have been used for simulation. Inspecting the normalized spectra for both cases reveals a distinct wavelength shift that is e.g. clearly noticeable for blue and cyan LEDs. The second reason has already been outlined in the previous paragraph – a strong temperature dependency of emitted intensity and peak wavelength. Fig. 4.18 thus exemplarily illustrates measured spectra for two different ambient temperatures at $T_1 = 35\,°C$ (solid lines) and $T_2 = 60\,°C$ (dashed lines). It is clearly observable that the peak emission wavelength of the LEDs shifts towards higher wavelengths with increasing ambient temperatures, while the emitted intensity decreases simultaneously. Both effects are well described in literature [312] as introduced in section 2.2.

While the respective (x, y)-coordinates of the six LED primaries are easily determined by the recorded optical emission spectra, luminous flux is unlike harder to measure. In fact, the luminous flux could only be quantified by integration over the entire dihedral angle, which would experimentally be conducted by using an integrating (*"Ulbricht"*) sphere. Since an Ulbricht sphere

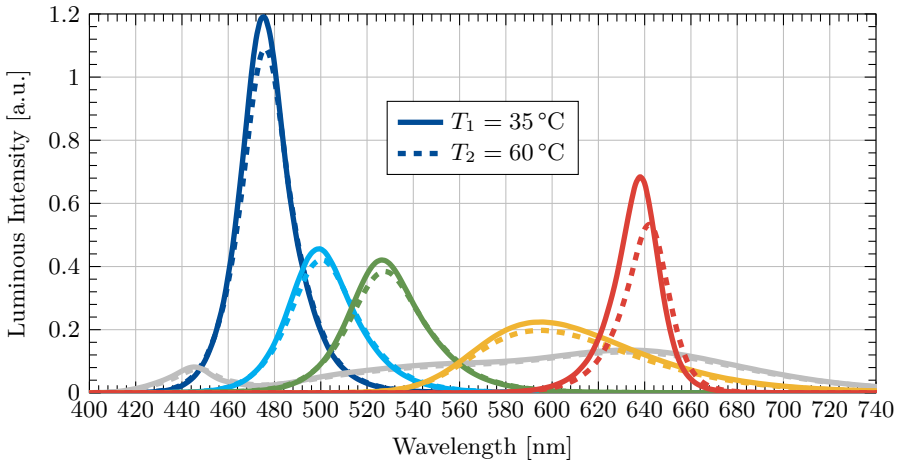


Figure 4.18: Comparison of measured LED spectra for two different ambient temperatures ($T_1 = 35\,°C$ and $T_2 = 60\,°C$).

has not been available for the experiments presented in this work, luminous flux could not be measured directly. Fortunately, the color control algorithm only needs the tristimulus value Y_i of each LED as its brightness information, which could simply computed by the recorded optical emission spectra. Additionally, the relative relation between emitted intensities from employed LEDs must be maintained. To obtain the tristimulus values Y_i as brightness information, these relative intensities are subsequently processed by the $V(\lambda)$ curve for human perception according to equation 2.6.

Employing the automated measurement routine explained above, the x_i, y_i and Y_i parameters are determined for each LED at maximum brightness level ($n_{PWM} = 64000$). As explained earlier, LED calibration finally turns out to be the key for achieving precise results matching to prior simulations. Hence, it can be thought of different calibration techniques to improve achievable performance, which is yet left open for future work. Nevertheless, some main aspects to be considered shall shortly be mentioned in the following. First, all LED primaries should be characterized and calibrated according to LED current flow, forward voltage and temperature. These data sets can then be stored in RAM or read-only memory (ROM) of the digital controller unit, e.g. an MCU. Using all of these data however requires some storage space as well as corresponding current, voltage and temperature sensors. Of course, these hardware demands cause

some effort in implementation but can eventually be realized easily in an ASIC solution. The LED driver concept and implementation presented in chapter 5 exemplarily incorporates all needed sensing circuits. Second, a simple current characterizing method for the presented PWM based approach would be to measure x_i, y_i and Y_i for different brightness levels or moreover PWM duty cycles and store these values in the RAM or ROM on the μC. Once the color control algorithm has found the relative intensity distribution for the desired color point based on the initial calibration values, it knows the actual range of the PWM duty cycles D_i for each LED channel. Recalculating the relative intensity distribution using the respective x_i, y_i and Y_i values for the targeted PWM duty cycles is then expected to increase accuracy and hence performance accordingly.

Color Temperature Measurements

After calibrating the LED primaries according to their optical properties, the MATLAB® program starts the automated measurements over the entire CT range. It is targeted to verify the simulated performance by evaluating CRI and achieved color distance ΔE or $\Delta u'v'$ with recorded spectrometer measurements using the Konica Minolta CS-2000 [35].

Fig. 4.19 shows the CRI for the measured as well as for simulated spectra, both using the calibrated LED color coordinates and luminance. As can be seen, simulated and measured data fit very well to one another. In the lower CT region, the simulation results yield a little bit higher CRIs, whereas the measured CRI performance is slightly better for higher CTs. The aim of achieving a CRI higher than 90, is however only realized by the RGB-CAW configuration in case of CT $\leq$ 4200 K and for the RGB-W setup in a middle CT region ranging from about 3100 K to 4700 K. This represents still a very good result, since the region between 2500 K up to 4000 K is the most important one for indoor lighting. Beyond that, the literature review already revealed that it is rather difficult to achieve high CRIs for very low CTs in the region of about 2200 K [59], which is yet realized with the proposed color control algorithm for the RGB-CAW LED configuration. This is an excellent result. Comparing the measured results to the original simulation depicted in Fig.4.8, which uses the LEDs' data sheet information, it strikes that the measured performance is quite comparable in the lower CT region up to 4000 K-4500 K, while there are very strong deviations for "colder" CTs above 5000 K. Two main reasons have been found explaining the observed behavior as outlined in the following.

First, the fixed optimization vectors, for which the performance in Fig.4.8 was simulated and extracted, could not be used for the measurements because

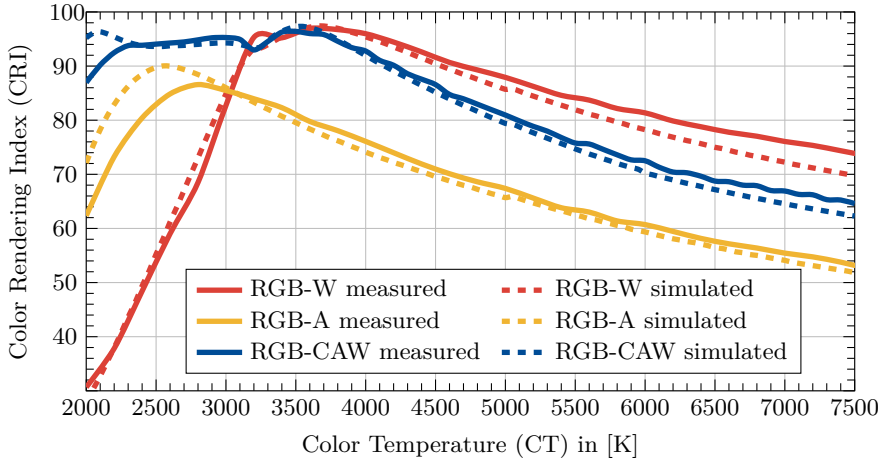


Figure 4.19: Simulation versus measurement results of CRI over the entire CT range for three different luminaire realizations.

the LEDs employed in the actual measurement setup differ regarding their optical properties from the initially assumed simulation values. Using the fixed optimization vectors $\boldsymbol{s_{opt}}$ denoted in table 4.3 would hence lead to significantly reduced CRI performance. An adaptive optimization vector, with $a = 1$ and $b = 2$, was thus chosen instead for all luminaire configurations. Various simulations, also the ones using the initially assumed LED data sheet properties, showed that the adaptive optimization vector has the tendency to provide high CRIs for "warm" CTs up to about 4000 K-4500 K and reduced performance for "colder" CTs in the higher kelvin region. Tuning of the optimization vector $\boldsymbol{s_{opt}}$ is hence expected to further improve CRI performance for higher CTs and in particular for the RGB-A case. In this context, it should also be noted that RGB-A and RGB-W setups should perform better utilizing other a and b parameter values for the adaptive optimization vector referring for instance to table 4.2, which was unfortunately not tested in the conducted experiments due to limited time capabilities.

Second, and even more important, it was found that the optical properties of the blue LED significantly impact CRI results. Fig. 4.17 therefore compares the spectra taken from the datasheets [342], [376] with the actual measured ones for each employed LED primary. Especially, the blue LED showed a strong deviation of its spectral distribution. It is observed that the recorded spectrum

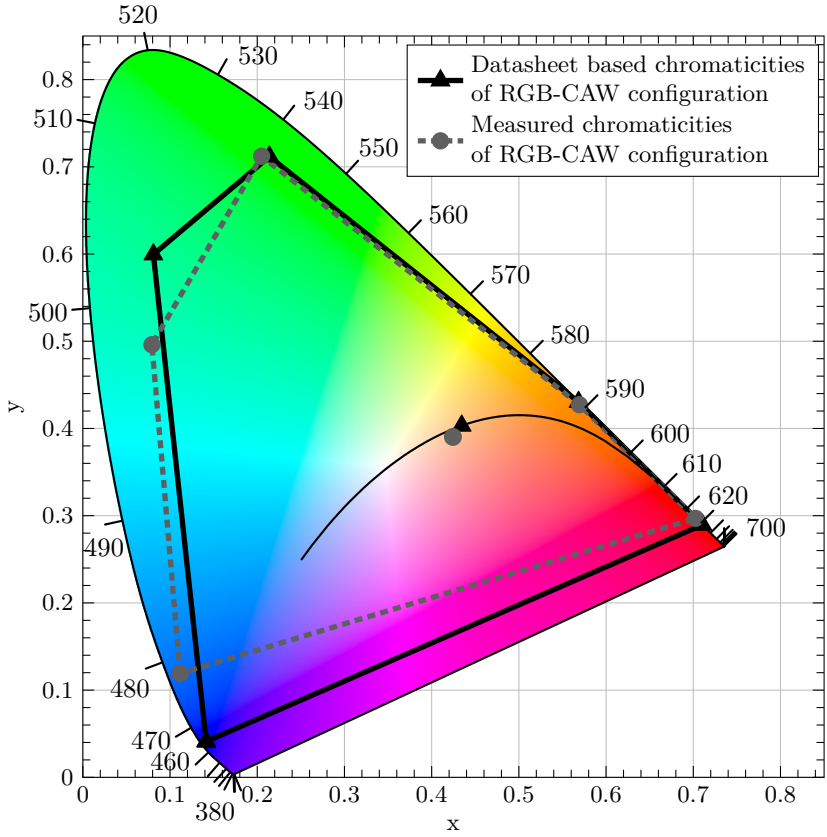


Figure 4.20: CIE 1931 chromaticity diagram with spanned color gamuts of measured and datasheet based chromaticities.

of the blue LED shifted strongly towards higher wavelengths of more than 10 nm in contrast to the datasheet curve. This is a huge deviation, which is clearly visible and also affects the corresponding (x, y) coordinates. Fig. 4.20 thus illustrates the measured (x, y)-coordinates in the CIE 1931 chromaticity diagram for all LED primaries in contrast to the corresponding datasheet set. It becomes clearly noticeable how the spanned gamut shifts and shrinks, which makes the realization of fully saturated blue colors impossible. The strong shift of the blue LED is consequently the reason for degraded CRI performance. In

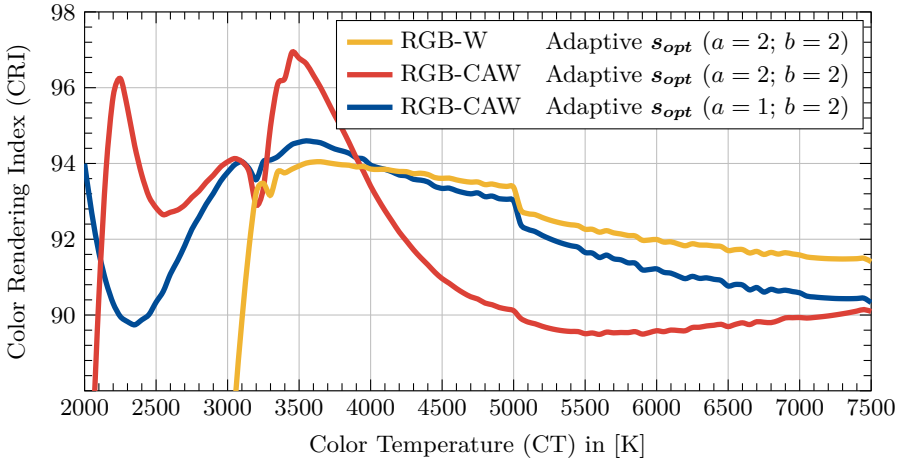


Figure 4.21: Simulation of CRI versus CT using measured calibration spectras except for the blue LED, which relies on datasheet information.

further simulations it could moreover be shown that very good CRI results were obtained, if only the blue LED was exchanged for its initial simulation data set. The other LED primaries relied on the measured spectra recorded during the calibration phase. Fig. 4.21 exemplarily presents several results for an RGB-CAW and RGB-W configuration using different adaptive optimization vectors $\boldsymbol{s_{opt}}$. It can be seen that a CRI higher than 90 is achieved nearly over the entire CT range for the RGB-CAW configuration. It is expected that CRI can be further optimized, especially for the other luminaire configurations or specific CT regions, if the optimization vector is further fine tuned. Beyond that, also other studies reveal that better CRI performance is achieved, if a deep royal blue LED is being used [15]. For building a high performance lighting system, it is therefore very important to utilize a (royal) blue LED with a short peak wavelength in the near UV range, which is yet still visible for the human eye. In case of synthesizing lower CTs in the yellow, orange or reddish region, the effect on a decreased CRI is strongly reduced because the blue LED is barely turned on or moreover at merely very low PWM duty cycles. In summary, the CRI measurements show great performance also in a real hardware system and prove the previously presented simulation results. The proposed color control algorithm can hence be employed in high quality lighting system optimizing for outstanding CRI performance.

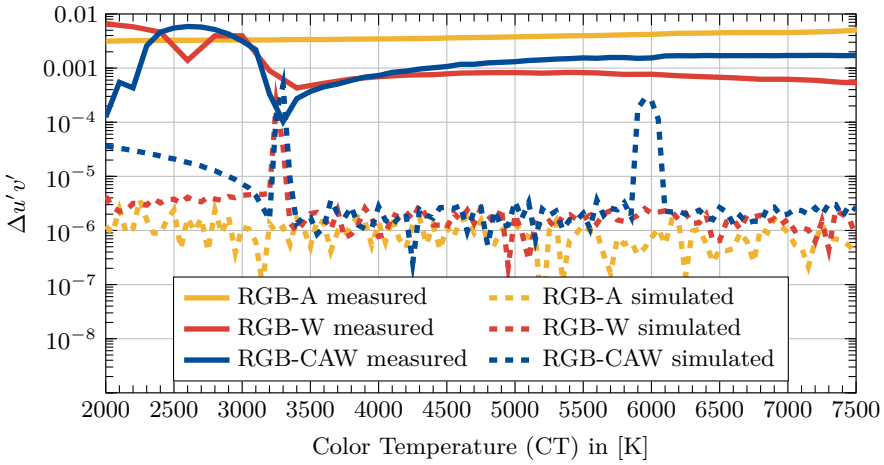


Figure 4.22: Simulation versus measurement results of color distance $\Delta u'v'$ over the entire CT range for three different LED configurations.

Fig. 4.22 illustrates the measured color distances $\Delta u'v'$ in comparison to the corresponding simulation results for all three LED configurations. The color difference had to be plotted on a logarithmic scale as the measured values deviate from their simulated counterparts for more than two decades. Although the measured color distances are comparatively high, they reside mostly below the non-perceivable limit of $\Delta u'v' \leq 0.002$ or the acceptable limit of $\Delta u'v' \leq 0.0035$. However, these boundaries are exceed in the range between 2300 K and 3000 K. In this region $\Delta u'v'$ stays below a max. deviation of 0.006, which is still an excellent result compared to other works [99], [146], [338]. For the most interesting luminaire configuration, which is the RGB-CAW case, the color shift was additionally observed at different brightness levels. Fig. 4.23 presents the corresponding measurement results, which show a very similar behavior than those of Fig. 4.22. Except for the 20 % dimming case, the color shift $\Delta u'v'$ stays within the acceptable tolerance of $\Delta u'v' \leq 0.0035$ for CT $\geq$ 3000 K and mostly remains even below the non-visible threshold of $\Delta u'v' \leq 0.002$. For lower CTs this limit is however exceeded for all dimming cases. This particular region also shows the expected behavior of an increased color shift for lower brightness levels. This tendency is however not clearly recognizable throughout the entire measurement range. The reason for the unexpected deviations and increased color shift levels most likely relate to a bundle of measurement uncertainties,

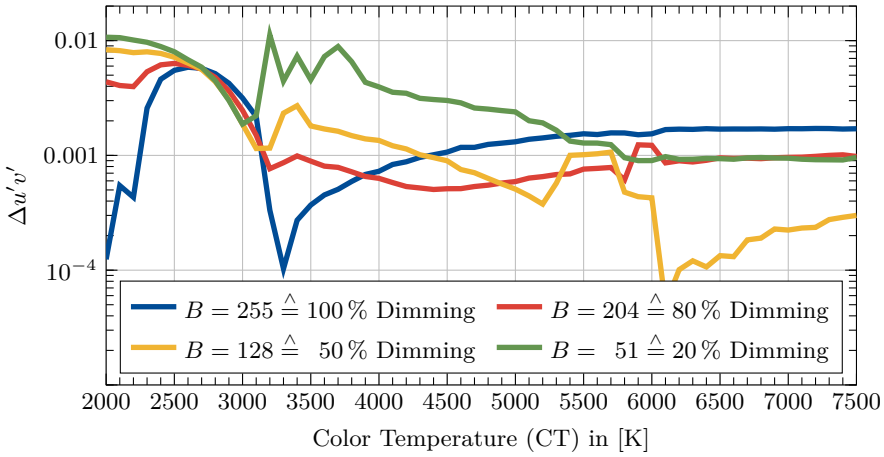
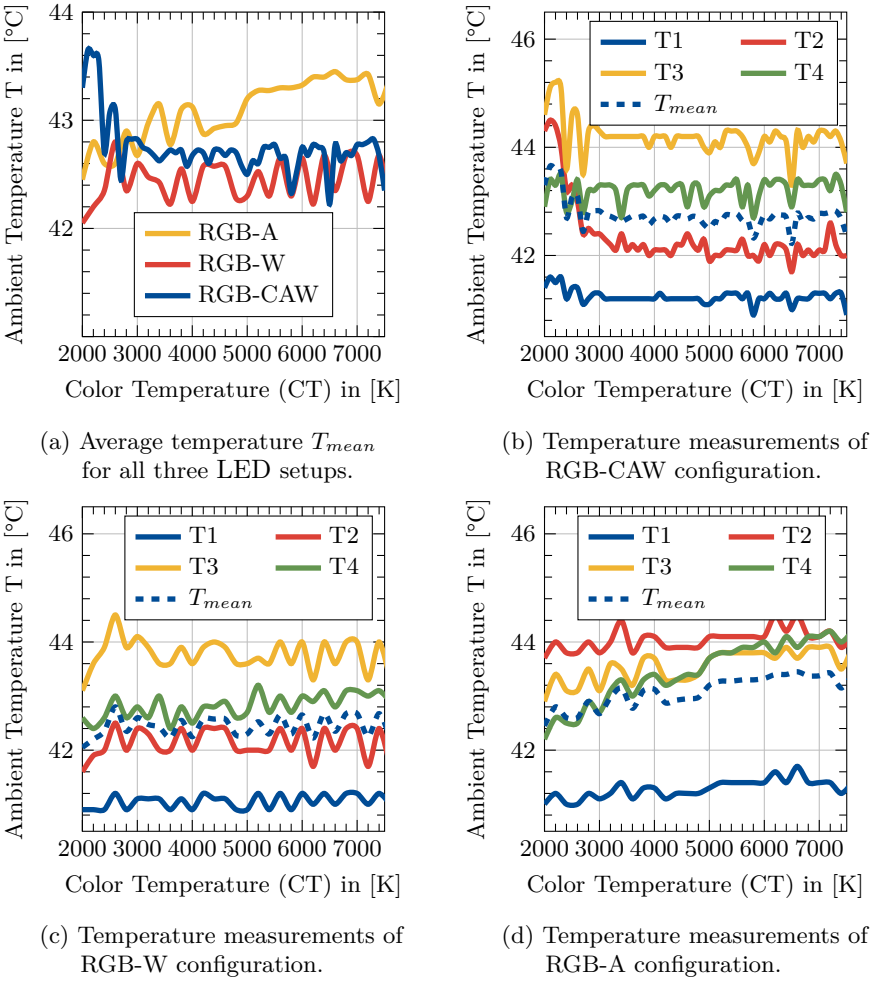


Figure 4.23: Measured color distance $\Delta u'v'$ versus CT for RGB-CAW luminaire setup at different brightness levels.

which have not or could not be considered when conducting the experiments, as explained in the following paragraph.

In the used experimental setup, various measurement uncertainties can actually be found that directly influence color shift performance. It was e.g. not possible to measure the LED current flow deviations caused by temperature effects or mismatch between the different LED channels. Although the LED current of the employed driving circuit proposed in chapter 5 is kept within 1 % to 2 % over dimming, it may deviate further between the different channels due to mismatch errors and varying component tolerances of used resistors, reference and sensing voltages, etc. Additionally, temperature effects in the LED driver have not been considered at all. Non-stable temperature conditions may however lead to differences in reference and sensing voltages, which alter the actual LED current flow in the end. Different temperatures of the LED driver may yet e.g. easily occur for longer measurement times or when a large number of measurement points are taken because the driving circuits heats up over time accordingly. This is e.g. the case when recording measurements over the entire CT range and particularly for measurements recording the entire displayable color gamut. Using little fans providing active ventilation, it was at least targeted to minimize the issue of temperature effects and realize constant conditions, which was however only possible to realize to some extent. Beyond LED current flow variations, also temperature uncertainties and forward voltage



(a) Average temperature T_{mean} for all three LED setups.

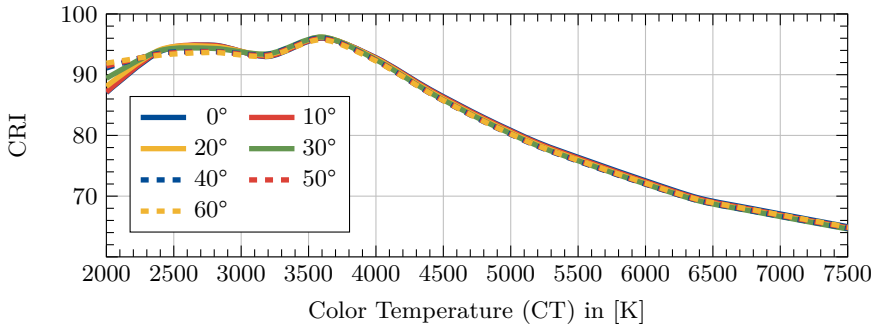
(b) Temperature measurements of RGB-CAW configuration.

(c) Temperature measurements of RGB-W configuration.

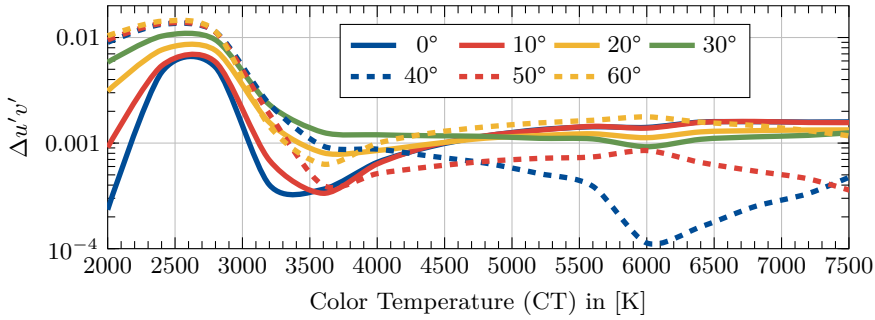
(d) Temperature measurements of RGB-A configuration.

Figure 4.24: Measured ambient temperatures at LED spot over CT range for three different luminaire realizations.

variations in the LEDs themselves may contribute an additional error as these effects shift the (x, y)-coordinates significantly. Thus, Fig. 4.24 exemplarily depicts the recorded temperatures of the four measurement probes T_1 to T_4



(a) CRI measurements.



(b) Color distance $\Delta u'v'$ measurements.

Figure 4.25: Color quality measurements under different viewing angles for the RGB-CAW luminaire configuration.

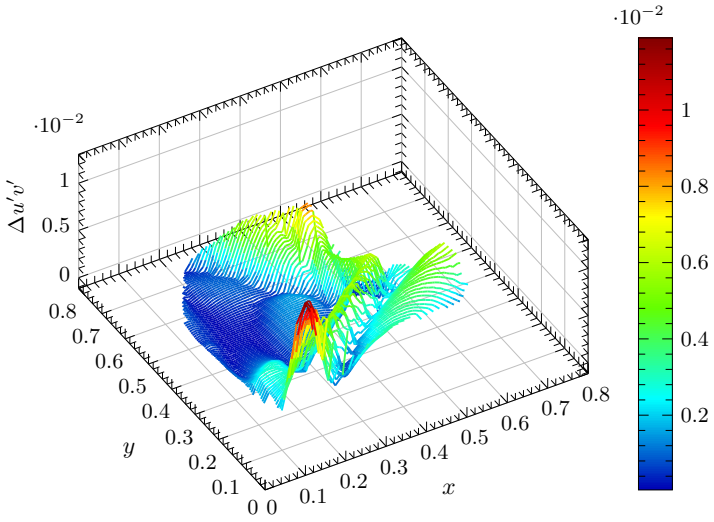
and the overall mean temperature that was used for LED calibration for all LED configurations. As can be seen, LEDs close to temperature probe T_4 experience much higher ambient temperatures than those, which are close to T_1. The deviations may easily lie in the range of 1 °C to 2 °C, which is quite a lot. If LED forward voltage were measured for each individual LED channel by the respective driving stage, the color control algorithm could conclude to the actual junction temperature in each LED string by means of a pre-determined LUT. This LUT must contain precise data of the relationship between LED forward voltage and junction temperature in dependence of selected or rather measured LED forward current. It is expected to drastically reduce the temperature related effects and correct the realized (x, y)-coordinates, if such a

compensation mechanism could be applied. The temperautre gradient among the employed LED channels actually becomes relevant when investigating the LEDs' on-times during the CT measurements. For low CTs the blue LED is nearly not used, whereas for high CTs the PWM duty cycles of red and amber LEDs are much less. Furthermore, the ambient temperature at the LED spot may additionally deviate between the conducted color point measurements and the initial LED calibration because only one LED is turned-on at maximum brightness in the latter case instead of four to six LEDs being pulsed all at different PWM duty cycles in the first mentioned case. Although the automated measurement routine aimed to minimize such temperature gradients, it can obviously not fully compensate for them. It is supposed that this effect could also be eliminated by the forward voltage based measurement compensation technique described above.

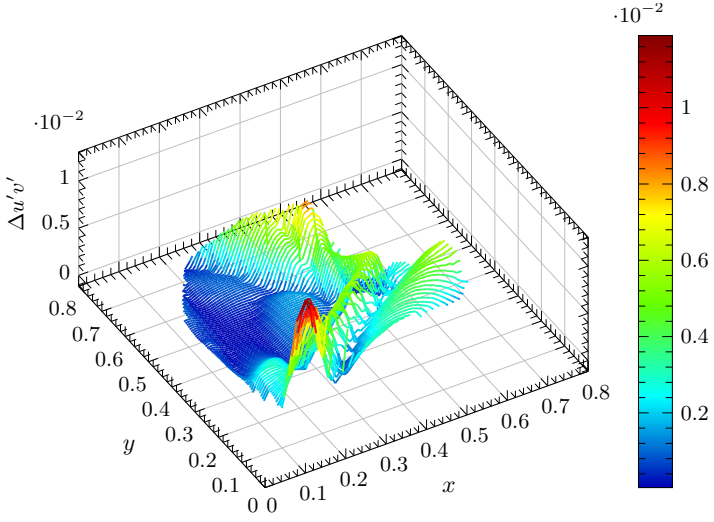
Finally, color quality is evaluated under different viewing angles in order to check, whether the performance can be kept constant. Fig. 4.25 depicts the achieved measurement results. While CRI is not affected at all, color distance $\Delta u'v'$ increases with advancing viewing angle, particularly for lower CTs. In case of higher CTs $\geq 4500\,\mathrm{K}$, the color distance $\Delta u'v'$ is nearly unaffected for viewing angles up to 30°, while it remains below the perceivable threshold of $\Delta u'v' \leq 0.002$. The differences in $\Delta u'v'$ are of course also affected by the aforementioned measurement uncertainties, which becomes obvious looking at the 40° and 50° measurment curves. Although there is some deviation visible, it is kept within relatively small limits and hence a very good result for the self constructed luminaire.

Gamut Measurements

Beyond evaluating color quality for a large CT range, the performance of the proposed color control algorithm is also measured in terms of $\Delta u'v'$ over the entire displayable gamut of three different LED configurations. Due to the comparatively long pre-heating and cooling cylces during the automated measurement routine, the recording time of a single color coordinate took about 3.5 min to 4 min. Thus, the amount of measurement points had to be limited to a reasonable amount, which is still high enough to yield a sufficiently precise coverage of the displayable gamut. The step sizes in x- and y-direction have therefore been selected to $dx = 0.03$ and $dx = 0.03$, respectively. The measurement time for recording an entire gamut of a single LED configuration consequently lasted about 40 h to 44 h. Fig. 4.26 and Fig. 4.27 illustrate the corresponding results of color distance $\Delta u'v'$. All measurement setups used an adaptive optimization vector $\boldsymbol{s_{opt}}$ with exponent values of $a = 1$ and

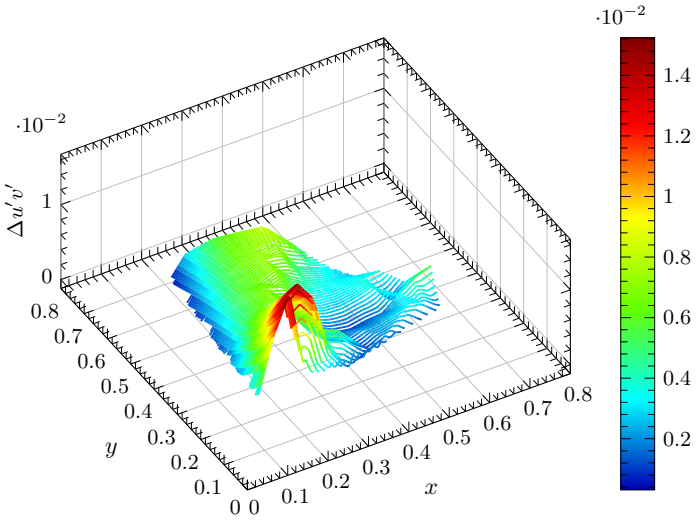


(a) Measurement of $\Delta u'v'$ using the color control algorithm without an area request.

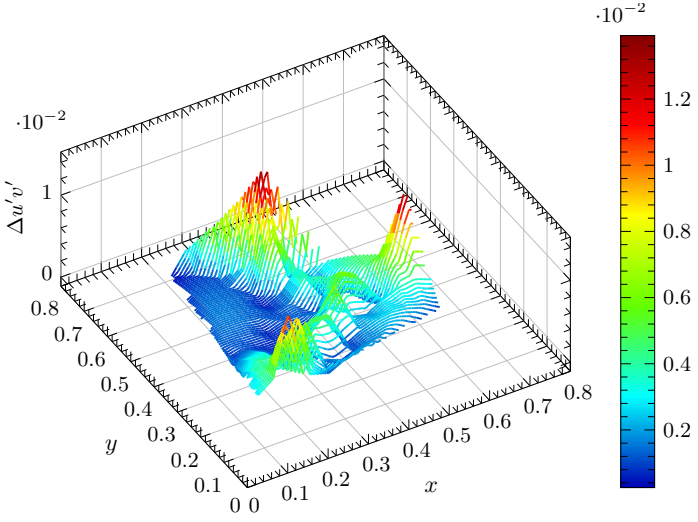


(b) Measurement of $\Delta u'v'$ using the intelligent ellimination routine.

Figure 4.26: Color shift measurements over the displayable gamut for an RGB-CAW configuration using $\boldsymbol{s_{opt}}$ ($a = 1$; $b = 2$).



(a) Measurement of $\Delta u'v'$ for RGB-A LED configuration.



(b) Measurement of $\Delta u'v'$ for RGB-W LED configuration.

Figure 4.27: Color shift measurements for different luminaire configurations using $\boldsymbol{s_{opt}}$ ($a = 1$; $b = 2$) without intelligent elimination.

$b = 2$, while the proportional constant k is always chosen to equal one. The intelligent elimination was disabled for all LED configurations, which are RGB-CAW, RGB-W and RGB-A. In addition to that, one gamut measurement of the RGB-CAW setup was performed with the elimination routine enabled. Fig. 4.26b contrasts this case to the one without this refinement depicted in Fig. 4.26a. The implemented area request does actually not show a visible effect in the recordings so that both graphs appear nearly identical. This is because of the aforementioned measurement uncertainties of temperature variations, current accuracy and mismatch between the LED channels, which all affect and superpose achievable color precision. Hence, the same reasoning and also the same counter measures, which have been outlined and described in detail in the previous paragraphs about the CT range measurements, also apply here. Additionally, the employed blue LED featuring an adverse spectrum further degrades color quality as described earlier. This effect comes especially to the fore when color precision is targeted in particular regions of the gamut.

The RGB-CAW setup eventually yields the best performance of all three luminaire realizations. Inspecting Fig. 4.27, it might appear at first glance that RGB-A and RGB-W perform better but the different scale of the color bar has to be considered. The gamut measurement of the RGB-W configuration in Fig. 4.27b additionally visualizes another interesting effect that is also noticeable for the other LED setups. Approaching the locations of the outer LED primaries, the measured color distance $\Delta u'v'$ strongly increases. This bigger deviation directly relates to the PWM duty cycles of employed LEDs. The duty cycles of far distant LED primaries with respect to the synthesized color point become very small and eventually reach a critical level considering the minimum on-time of the respective LED driving stage. This effect was also observed in subsequent simulations using the measured, calibrated coordinates of the employed LED primaries, especially in close proximity of the (strongly shifted) blue LED. To allow for a more precise adjustment it is hence desirable to realize even faster switching and settling times in the LED driving stages, particularly at turn-on. This aspect is thus considered in the ASIC implementation presented in chapter 6. In summary, the gamut measurements show good color precision considering the rough measurement uncertainties, limited switching speed of the employed LED driver and the averted spectrum of the blue LED. It is expected that the proposed color control algorithm is hence capable of achieving acceptable and maybe even non-visible color distances over the entire gamut, if certain enhancements are applied as described before. Besides choosing a blue LED with better optical properties, these methods involve improvements in the LED driving stage regarding shorter minimum on-times and a diminished current mismatch (over temperature and component tolerances) between independent

LED color channels. Junction temperature related effects must be minimized with a proper (closed-loop) compensation technique. Measuring the forward voltage of employed LEDs and thereby determining the temperature indirectly by means of a lookup table (LUT) appears to be a very attractive and suitable method. For this approach, very precise and accurate calibration of each LED's x_i, y_i and Y_i properties are required for certain ranges of current, ambient temperature and forward voltage conditions. In conclusion, the proposed color control algorithm achieves excellent results in simulation and maintains very good color precision and outstanding CRI even under realistic measurement conditions. The developed color control technqiue consequently founds the basis for precise color rendering in high quality lighting systems.

Chapter 5

Efficient LED Driving for High Quality Lighting Applications

LED driving for high quality lighting applications aims to balance high energy efficiency with precise LED current regulation to achieve excellent optical properties of the emitted visual spectrum at minimum possible power consumption. As outlined in chapter 2.3, dynamic headroom regulation has proven to be a suitable LED driving method with respect to the desired target application because it provides a good trade-off between energy efficiency and a flat transient LED current waveform. Consequently, this type of topology is chosen for the LED driving concept presented in this thesis.

However, chapter 2.3.3 also revealed that current solutions founding on dynamic headroom regulation [74], [153], [305] suffer from several limitations related to their analog feedback control implementations, such as low pulse-width modulator gain, possible instabilities in one of the three control loops, power-hungry opamps or increased hardware effort and complexity. To overcome these major drawbacks, the LED driver design presented in this thesis tackles

such disadvantages by introducing a simple but efficient digital control strategy. This digital control approach, which has been published in [236], [237], targets to feature high flexibility and programmable regulation speeds while providing good decoupling of the individual control loops from each other. Beyond that, the proposed LED driver aims at satisfying other important requirements mentioned in sections 2.3 and 2.4 like providing a wide output voltage swing, dimming functionality as well as good robustness for enabling a flexible deployment in all kinds of high quality lighting applications. Thus, the presented concept optimizes the conflict of aims between high efficiency, precise current accuracy, good flexibility, robustness and stability, as shown in the following.

5.1 System Concept of an Efficient LED Driver Using Digital Dynamic Headroom Regulation

In compliance with the three independent control loops described in section 2.3.3, the presented LED driver using a digital dynamic headroom control consists of three main functional blocks. These three elements are first a switching voltage pre-regulator for power supply, second a PWM-switched linear current regulator for LED current and brightness control and third an MCU with a resistive digital-to-analog converter (RDAC) for the digital control methodology of the adaptive voltage regulation loop. The developed approach uses the drain potential V_D of the power transistor M1 as feedback control signal for the

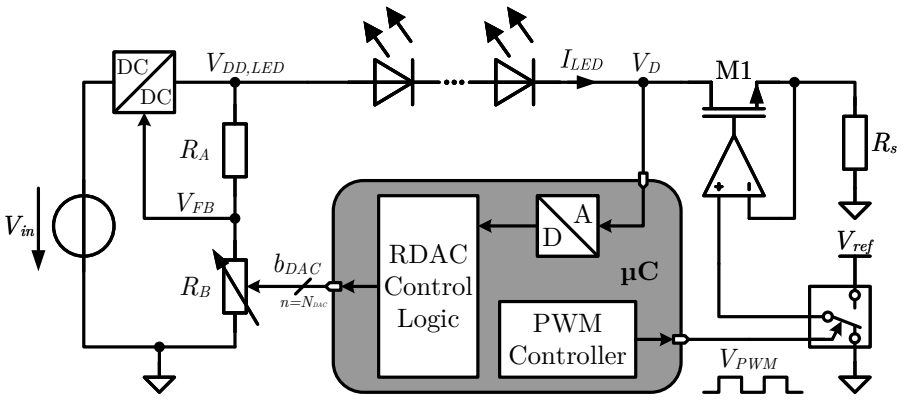


Figure 5.1: System concept of the proposed dimmable LED driver topology using digital feedback control for dynamic headroom regulation.

voltage minimization process over the linear current regulator. Fig. 5.1 shows the corresponding system concept for an efficient implementation with discrete components. In contrast to the research published in [74], [109], [152], [230], [231], this work focuses on a single-channel LED driver design. Nevertheless, it is possible to extend the system concept presented in this thesis with some minor modifications to operate similarly on multiple LED channels. In that case, several parallel-connected linear regulators would perform a (sequential) phase-shifted color mixing while being supplied by only one switching pre-regulator. For further details of this method please refer to section 2.3.3 and publications [74], [109], [152], [230], [231]. Proper color mixing can also be achieved by using the presented single-channel LED driver design and employing multiple instances of it, one for each channel or rather LED primary. Based on this second approach, a spotlight demonstrator featuring eight independently controllable LED channels has been designed and built as shown in appendix C.1. This demonstrator design has indeed been used for evaluating the developed color control algorithm by spectral measurements with respect to CRI and color precision ($\Delta u'v'$ and ΔE) in dependence on the chosen CCT or chromaticity coordinates (x, y) as presented in chapter 4.

A buck-boost converter topology has been chosen as switching pre-regulator since this architecture provides a very large input and output voltage swing, thus giving the desired flexibility. This great amount of flexibility is however bought by decreased efficiency and increased circuit complexity. Depending on the final target implementation this trade-off can be further optimized. Using e.g. a buck converter instead, might provide a higher efficiency while reducing the number of (external) components from four power-switching transistors to two. Though, this approach is only practical, if the available input voltage is higher than the target output voltage level in a final application. A buck-converter based approach with good flexibility but improved efficiency is therefore presented later in this thesis within chapter 6 by means of developing a custom tailored, monolithically integrated solution. In the presented concept, the power converter operates from a fixed DC input voltage and directly supplies its DC output voltage to attached LEDs. Nevertheless, the digital control methodology shown here can easily be transferred to mains fed systems as the ones published in [74], [231], [396]. Assuming a fixed input voltage and a defined output voltage range, the available output power that can be supplied to the LED load is only determined and hence limited by the size of inductance L and by the converter's power switches since these elements set the provided maximum output current. Switching frequency of the power converter needs to be selected as a balance of output voltage ripple and achievable efficiency, while regulation speed and stability requirements have to be obeyed.

Minimization of brightness fluctuations or color shifts is assured by precise current control with a linear current regulator realized in a conventional circuit architecture. The regulator needs to act very fast in order to compensate for variations on LED supply voltage $V_{DD,LED}$ and keep the LED current level I_{LED} flat. Additionally, it is crucial to realize fast turn-on and turn-off times for combining a high PWM switching frequency with a large resolution in dimming range. Therefore, it is necessary to use a high-speed opamp in conjunction with a power MOSFET featuring very low gate capacity C_{GS}. Fast changes on LED supply voltage may on the one hand be caused by load transients due to the fast PWM switching of the linear current regulator and may on the other hand originate from the continuous output voltage ripple of the switching voltage pre-regulator. In fact, the fast PWM switching of transistor M1 may result in severe voltage dips on LED supply voltage $V_{DD,LED}$, which therefore requires a certain safety margin of the voltage drop V_D over the LED current regulator. Optimizing overall LED driver efficiency hence demands accounting for this additional headroom in the design considerations. Achieving a low output voltage ripple of the converter and small dips at load transitions are thus essential design specifications and requirements for the presented driver concept. Realizing a small voltage ripple on $V_{DD,LED}$ the switching pre-regulator also requires a relatively fast control loop for setting its output voltage. However, the speed of this inner control loop of the power converter, which is equivalent to its switching frequency, may not be chosen too fast ensuring thorough decoupling of the LED current control process. This demands a difference in control speeds of at least one decade, where the current control loop is the faster process. The voltage minimization of the dynamic headroom regulation can be much slower than the other two loops as it is not timing critical and only relevant for minimizing static DC losses in the current regulator. A digital control methodology as the one presented in this thesis allows for stepwise adapting the control speed of the dynamic headroom regulation in multiples of a digital clock frequency. Therefore, the dynamic headroom regulation process can easily be optimized for the perfect trade-off between regulation speed and stability.

Many COTS converter ICs feature a voltage feedback pin V_{FB} for setting the static DC output voltage. Likewise the switching pre-regulator settles its output voltage $V_{DD,LED}$ according to the feedback voltage signal V_{FB} provided by the resistive divider of R_A and R_B as shown in Fig. 5.1. V_{FB} thereby is a representation of the scaled down output voltage $V_{DD,LED}$ and follows the transfer function of the resistive divider according to

$$H_{FB}(s) = \frac{V_{FB}}{V_{DD,LED}} = \frac{R_B}{R_A + R_B}\,. \tag{5.1}$$

The developed digital control methodology tackles the voltage regulation process by modifying this feedback transfer function from output voltage $V_{DD,LED}$ to feedback voltage V_{FB} by changing the ratio of the resistive divider. The systematic key idea of this control strategy has been presented in [236], [237] and is outlined in more detail in the following section 5.2.

5.2 Digital Dynamic Headroom Regulation with Resistive DAC Feedback Control

As indicated in Fig. 5.1 and just mentioned in the last paragraphs of section 5.1 the switching pre-regulator used in the presented LED driver topology regulates its output voltage according to the voltage V_{FB} applied at the feedback pin. The ASIC compares the feedback voltage V_{FB} internally with a fixed reference $V_{FB,ref,int}$. Aiming to minimize the difference between these two values, the inner converter control loop adjusts the output voltage $V_{DD,LED}$ of the switching pre-regulator accordingly. Thereby, the static DC value of $V_{DD,LED}$ can be calculated by replacing the external feedback voltage V_{FB} in transfer function 5.1 with the given internal reference value of the used ASIC leading to

$$V_{DD,LED} = V_{FB,ref,int} \cdot \frac{R_A + R_B}{R_B} \,. \tag{5.2}$$

Dimensioning the resistive divider of R_A and R_B hence directly sets the desired LED supply voltage $V_{DD,LED}$. Therefore, adjusting the ratio of the resistive divider represents a good measure for introducing dynamic headroom regulation into an LED driver with a circuit topology identical or similar to the one presented in this thesis. In fact, the key idea of the developed digitally assisted control technique founds on tuning only the lower resistance R_B while the upper resistance R_A is set to a fixed value. In order to realize the desired functionality resistance R_B needs to be programmable by means of a digital control word b_{DAC}. Fig. 5.2 shows the physical structure of a suitable concept. This system employs a fixed resistance R_{max} indicating the maximum possible value of resistor R_B and several switchable resistors R_1 to $R_{N_{DAC}}$ in parallel. Due to the parallel connection of all resistors it is only possible to lower R_{max} by turning one or more of the digitally controlled resistances R_1 to $R_{N_{DAC}}$ on.

As already mentioned in section 5.1, the presented digital control strategy uses the drain potential V_D of the power transistor M1 as its feedback signal in the control loop. Considering the given physical structure of the RDAC as indicated in Fig. 5.2, the general principle of operation for the digital control methodology can be outlined as follows. If the voltage drop of V_D is too high

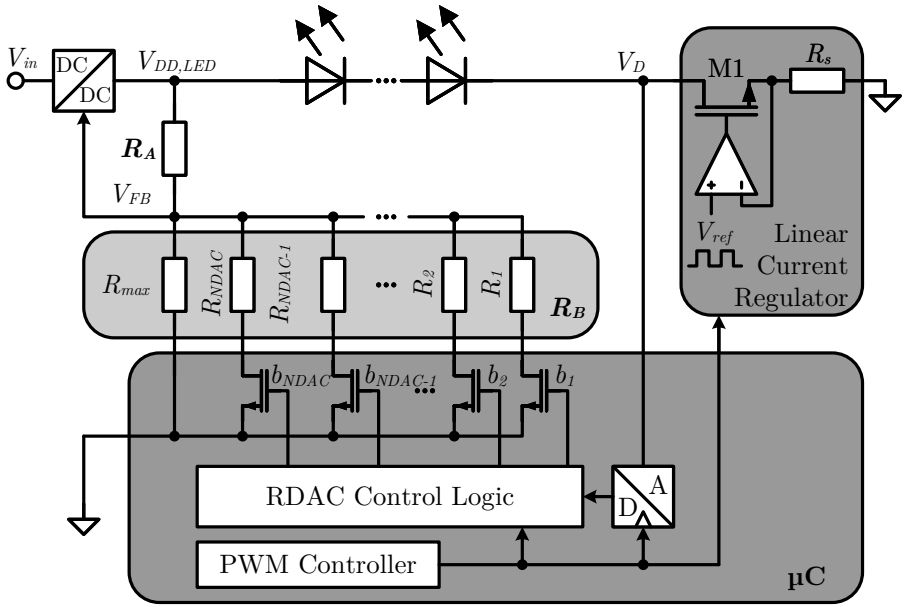


Figure 5.2: Structure of an RDAC for digitally assisted headroom control.

in reference to a desired target value, the digital control algorithm lowers its control word b_{DAC}. This results in a higher effective resistance of R_B leading to an increased feedback voltage V_{FB}. The converter control IC thus reduces the output voltage $V_{DD,LED}$ yielding a decreased drain potential V_D. If the measured drain potential is smaller than the set target value, the control loop acts exactly the other way around. The digital control logic then increases its control word b_{DAC}, which consequently lowers resistance R_B such that V_{FB} goes down. Hence, $V_{DD,LED}$ and V_D will rise again until the target value is reached. For stability reasons the digital control mechanism employs a certain hysteresis window that can be adjusted in the control logic. Fig.5.3 illustrates this principle of operation for the developed digitally assisted control mechanism in a simplified block diagram.

Based on this conceptual idea the mathematical relationships can be evolved. Since resistance R_B can only be decreased by means of the digital control, the value of the (additional) non-switchable resistor R_{max} determines in combination with a chosen fixed value for resistance R_A the minimum achievable LED supply voltage $V_{DD,LED}$ in compliance with equation 5.2. Maximum selectable output

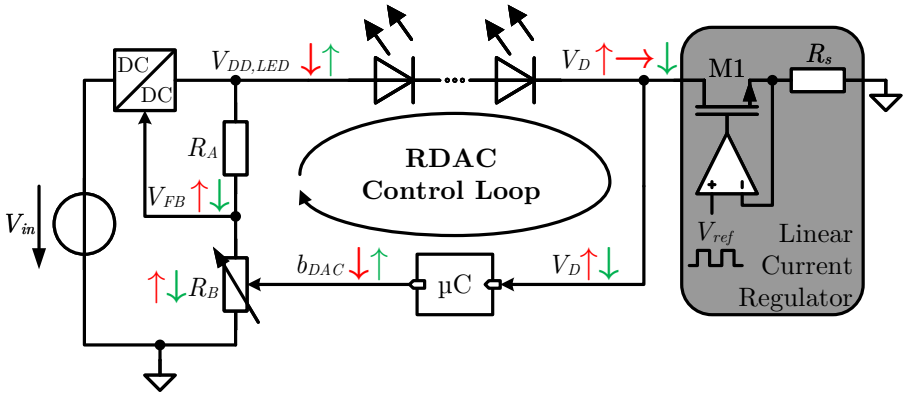


Figure 5.3: Principle of operation of the digital feedback control loop.

voltage of the switching pre-regulator on the other side depends on the number of digitally switchable resistors N_{DAC} in R_B, which is in fact the resolution of this so-called resistive DAC,

$$\frac{1}{R_B} = \frac{1}{R_{max}} + \frac{1}{R_1} + \frac{1}{R_2} + ... + \frac{1}{R_{N_{DAC}}},$$

$$\Leftrightarrow R_B = \frac{1}{\frac{1}{R_{max}} + \sum_{n=1}^{N_{DAC}} \frac{1}{R_n}}. \tag{5.3}$$

Aiming to achieve a linear tuning range of the RDAC, its resistances R_n must have binary weighted values with a finite bit resolution of N_{DAC}. Computing the individual resistor values inside of the RDAC hence follows subsequent formulas,

$$R_1 = 2 \cdot R_2 = ... = 2^{N_{DAC}-1} \cdot R_{N_{DAC}}, \tag{5.4}$$

$$\Rightarrow R_n = \frac{R_1}{2^{n-1}}. \tag{5.5}$$

Combining equations 5.3 and 5.5 leads to the calculation rule of total resistance R_B, the lower part of the feedback resistive divider,

$$R_B = \frac{1}{\frac{b_{DAC}}{R_1} + \frac{1}{R_{max}}}\,, \tag{5.6}$$

$$\Leftrightarrow R_B = \frac{R_1 \cdot R_{max}}{R_1 + b_{DAC} \cdot R_{max}}\,, \tag{5.7}$$

where b_{DAC} denotes the binary input control setting for the RDAC given as an integer value in the range of 0 to $2^{N_{DAC}} - 1$. In compliance with equation 5.2 this calculation rule determines the static output voltage of the switching pre-regulator $V_{DD,LED}$ in dependency of the binary control word b_{DAC} resulting in equation

$$V_{DD,LED}(b_{DAC}) = V_{FB} \cdot \left(R_A \cdot \left(\frac{b_{DAC}}{R_1} + \frac{1}{R_{max}} \right) + 1 \right). \tag{5.8}$$

Thereby, output voltage $V_{DD,LED}$ is adjustable in discrete steps by the digital control word b_{DAC}, where a higher value of b_{DAC} yields a proportionally higher LED supply voltage $V_{DD,LED}$. The step size between two possible LED supply voltages is set by the actual resolution of the RDAC N_{DAC} according to equations

$$\Delta V_{DD,LED}(N_{DAC}) = V_{step}(N_{DAC}) = \frac{V_{DD,LED,max} - V_{DD,LED,min}}{2^{N_{DAC}} - 1}\,, \tag{5.9}$$

$$\Leftrightarrow V_{step}(N_{DAC}) = \frac{V_{DD,LED}(2^{N_{DAC}} - 1) - V_{DD,LED}(0)}{2^{N_{DAC}} - 1}\,. \tag{5.10}$$

5.2.1 Sensitivity Analysis on the Impact of the RDAC Resolution

As can be seen from equations 5.8 and 5.9, LED supply voltage can only be adjusted in discrete voltage steps due to the applied digital control mechanism. Obviously, the inherent quantization error thus also affects the voltage drop V_D over the linear current regulator. The choice of the RDAC's resolution N_{DAC} hence directly influences efficiency of the LED driver as explained in the following. Occurring fluctuations on LED supply voltage $V_{DD,LED}$ or even large dips due to load jumps require a distinct safety margin of voltage drop over the linear current regulator in the presented concept. Otherwise, if this voltage drop becomes to small, the linear current regulator can no longer assure a precise and

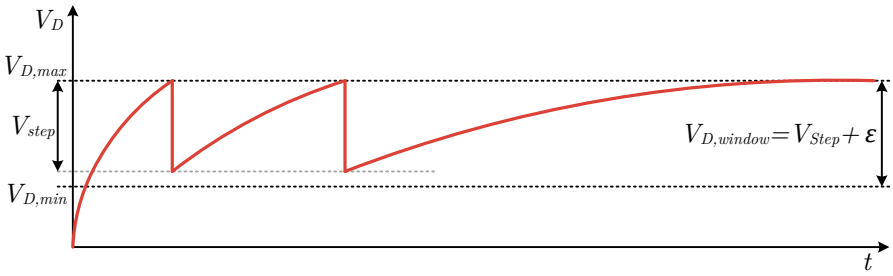


Figure 5.4: Exemplified regulation behavior of drain potential V_D within minimum target window size.

accurate regulation of the LED current flow. To account for these variations the drain potential V_D may only be lowered until a certain limit $V_{D,min}$ is reached. This value $V_{D,min}$ therefore represents the absolute minimum, which can be regulated to by the digital control logic. Due to the quantization error of the RDAC an additional voltage drop $\Delta V_{D,overhead}$ over the linear current regulator on top of $V_{D,min}$ may occur. Since the dynamic headroom control aims to keep the drain potential as low as possible in order to avoid additional power losses, it defines a tolerable target window range $V_{D,window}$, which is spanned by the lower and upper limits $V_{D,min}$ and $V_{D,max}$, respectively. For efficiency reasons, this window size and hence the limit of $V_{D,max}$ shall consequently be selected as small as possible. Due to the quantization error of the RDAC the specified window must however feature a minimum size of at least one V_{step} plus an additional tiny safety margin to ensure a stable regulation performance. Fig. 5.4 illustrates an exemplified regulation behavior within the described target window size in case of thermal heating, while equations 5.11 to 5.14 show the corresponding mathematical relationships for the voltage drop V_D over the linear current regulator as

$$V_{D,max} \geq V_{D,regulated} \geq V_{D,min}\,, \tag{5.11}$$

$$V_{D,regulated} = V_{D,min} + \Delta V_{D,overhead}\,, \tag{5.12}$$

$$V_{D,window} = V_{D,max} - V_{D,min}\,, \tag{5.13}$$

$$V_{D,max} > V_{D,min} + V_{step}\,. \tag{5.14}$$

This unavoidable additional voltage drop $\Delta V_{D,overhead}$ directly results in extra (static) losses and hence a decreased LED driver efficiency. Therefore, it is desirable to keep these losses as small as possible. A higher resolution of the RDAC would of course minimize the additional voltage drop by reducing the adjustable step size V_{step} and would thereby yield a higher average efficiency of the LED driver. However, the adjustable step size V_{step} cannot be selected too small due to an increasing hardware effort in the RDAC and a limited resolution of the ADC sensing the drain potential V_D. In order to better understand both limitations of RDAC resolution and V_D-sensing ADC, it is helpful to perform a sensitivity analysis for a given application scenario. The impact of the RDAC resolution on the minimum adjustable step size V_{step} can easily be calculated by equation 5.10, which shows an inverse exponential behavior of $\propto \frac{1}{2^x}$. Assuming a maximum LED supply voltage of $V_{DD,LED,max} = 40\,\mathrm{V}$ and a minimum adjustable LED supply of $V_{DD,LED,min} = 3.5\,\mathrm{V}$, the step size V_{step} reduces from 143 mV to around 8.9 mV by increasing the RDAC resolution from 8 bit to 12 bit, as shown in equations 5.15 and 5.16,

$$V_{step}(8) = \frac{40\,\mathrm{V} - 3.5\,\mathrm{V}}{2^8 - 1} \approx 143\,\mathrm{mV}, \tag{5.15}$$

$$V_{step}(12) = \frac{40\,\mathrm{V} - 3.5\,\mathrm{V}}{2^{12} - 1} \approx 8.9\,\mathrm{mV}. \tag{5.16}$$

Likewise, the resulting impact of V_{step} on the average efficiency can be approximated by equation 5.19,

$$\eta = \frac{P_{used}}{P_{total}} = \frac{P_{total} - P_{loss,Ireg}}{P_{total}} = \frac{I_{LED} \cdot (V_{DD,LED} - V_D)}{I_{LED} \cdot V_{DD,LED}}, \tag{5.17}$$

$$= \frac{I_{LED} \cdot N_{LED} \cdot V_{F,LED}}{I_{LED} \cdot (N_{LED} \cdot V_{F,LED} + V_D)}, \tag{5.18}$$

$$\Leftrightarrow \eta(V_{step}) \approx \frac{I_{LED} \cdot N_{LED} \cdot V_{F,LED}}{I_{LED} \cdot (N_{LED} \cdot V_{F,LED} + V_{D,min} + V_{step})}. \tag{5.19}$$

Dividing equation 5.19 by the factor of $I_{LED} \cdot N_{LED} \cdot V_{F,LED}$ helps to illustrate the dependency of the efficiency on V_{step} and the number of employed LEDs N_{LED} and their forward voltage $V_{F,LED}$ as shown in equation 5.20,

$$\eta(V_{step}) = \frac{1}{1 + \dfrac{V_{D,min} + V_{step}}{N_{LED} \cdot V_{F,LED}}}. \tag{5.20}$$

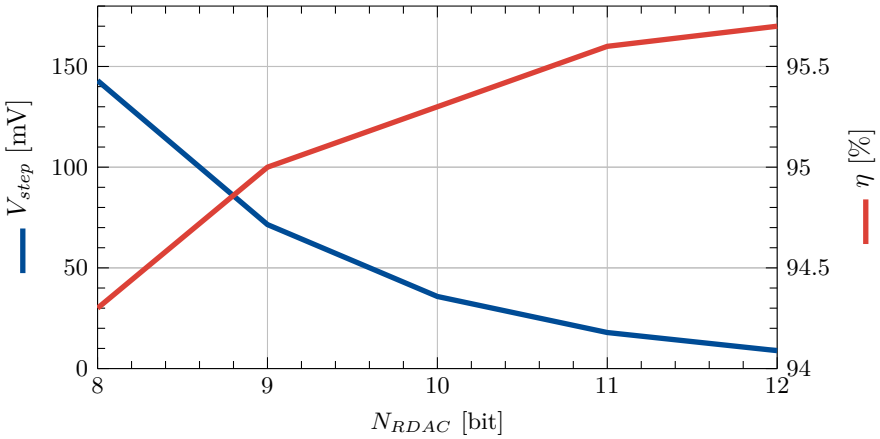


Figure 5.5: Step size V_{step} and efficiency η as a function of the RDAC resolution N_{RDAC}.

Consequently, the magnitude of the impact of V_{step} on the LED driver efficiency strongly depends on the minimum required voltage drop $V_{D,min}$ over the current regulator as well as on the number of employed LEDs and their forward voltage. Using more series-connected LEDs with a higher forward voltage results in a higher used power and hence obviously reduce the corresponding efficiency impact. Nevertheless, the effect of a higher RDAC resolution is still clearly visible as shown by the following application example. Considering a use case of three series-connected LEDs each having a forward voltage of $V_{F,LED} = 3.0\,\mathrm{V}$ at a current flow of $I_{LED} = 700\,\mathrm{mA}$ and minimum required voltage drop of $V_{D,min} = 400\,\mathrm{mV}$, yields the subsequent efficiencies for an 8 bit and 12 bit RDAC resolution,

$$\eta(V_{step}(8)) = \frac{700\,\mathrm{mA} \cdot 3 \cdot 3.0\,\mathrm{V}}{700\,\mathrm{mA} \cdot 3 \cdot 3.0\,\mathrm{V} + 400\,\mathrm{mV} + 143\,\mathrm{mV}} = 94.30\,\%\,, \quad (5.21)$$

$$\eta(V_{step}(12)) = \frac{700\,\mathrm{mA} \cdot 3 \cdot 3.0\,\mathrm{V}}{700\,\mathrm{mA} \cdot 3 \cdot 3.0\,\mathrm{V} + 400\,\mathrm{mV} + 8.9\,\mathrm{mV}} = 95.65\,\%\,. \quad (5.22)$$

Figure 5.5 shows the dependency of the step size V_{step} as a function of the RDAC resolution for the described exemplified application case. As can be seen, the shown V_{step}-curve follows an inverse exponential descent as expected referring to the mathematical relationship stated in equation 5.10. The efficiency on the

contrary improves with a curve progression reciprocal to V_{step} approaching a maximum efficiency limit asymptotically. It should be noted that the calculated efficiency values represent worst-case efficiencies as a complete V_{step} voltage drops additionally over the current regulator. The digital dynamic headroom control is hence only one ϵ away from switching to the next lower (RDAC) level. The hardware effort of the RDAC however increases linearly with each additional bit, while the requirement on its component tolerances rise exponentially with an increasing resolution. Obviously, the RDAC resolution can therefore only be increased up to a certain point, at which the deviations of the used resistors due to manufacturing tolerances become larger than an LSB. This point depends of course strongly on the component tolerances of the employed resistors. A further increase in resolution would thus not have any effect at this point. Too large component tolerances could moreover lead to a non-monotonic behavior of the RDAC control. It should be noted that even in this case of a non-monotonic behavior, the proposed control mechanism remains stable and is thus designed in a very robust manner as explained later.

Furthermore, a higher RDAC resolution also requires a more accurate sensing of the drain potential V_D at first glance. The minimum resolution requirement of the sensing ADC can be calculated according to equations 5.23 and 5.24 for a ground referenced and a $V_{D,min}$ referenced ADC, respectively,

$$N_{ADC,gnd} = \left\lceil log_2 \left(\frac{V_{D,max}}{V_{step}} \right) \right\rceil , \tag{5.23}$$

$$N_{ADC,Vmin} = \left\lceil log_2 \left(\frac{\Delta V_{ADC}}{V_{step}} \right) \right\rceil . \tag{5.24}$$

In order to keep the window size of additional losses over the current regulator as close as possible to only one V_{step}, it is however necessary to sense the drain potential V_D much more accurately. Referring to the dimensioning used in this thesis, the upper and lower window limits have been selected to $V_{D,max} = 550\,\text{mV}$ and $V_{D,min} = 400\,\text{mV}$, respectively, which yields a window size of $V_{D,window} = 150\,\text{mV}$. Considering a V_{step} of 143 mV for an 8 bit RDAC, this would yield only a 7 mV difference between $V_{D,window}$ and V_{step}. For efficiency reasons, ϵ, which is the difference between $V_{D,window}$ and V_{step}, must be as small as possible. The resolution of the drain ADC is hence required to be smaller than one ϵ. In order to account for a certain safety margin, it is therefore fair to demand a quantization in steps of 5 mV for the V_D-sensing ADC in the given application case, while covering a 600 mV input voltage range using a ground referenced ADC. Consequently, a minimum resolution of at least 7 bit as shown

in equation 5.25 would be required,

$$N_{ADC,gnd} = \left\lceil log_2 \left(\frac{\Delta V_{in,ADC}}{V_{LSB}} \right) \right\rceil = \left\lceil log_2 \left(\frac{600\,\text{mV}}{5\,\text{mV}} \right) \right\rceil = 7\,\text{bit}. \quad (5.25)$$

The same ADC could indeed be used for an RDAC with a resolution of 12 bit as $V_{step}(12) = 8.9\,\text{mV}$ is still bigger than one $V_{LSB} = 5\,\text{mV}$ of the ADC. Moreover, the input voltage range of the ADC could be reduced due to a smaller window size of e.g. $V_{D,window} = 20\,\text{mV}$ instead of $V_{D,window} = 150\,\text{mV}$, which even gives a smaller V_{LSB} for the considered 7 bit resolution. It is therefore fair to say that the impact of the RDAC resolution on the drain sensing ADC is negligible.

Instead of using a complex ADC, it would also be possible to realize the drain sensing functionality with a simple window comparator, whose thresholds compare levels are directly set to the respective voltages of $V_{D,min}$ and $V_{D,max}$. In this case the same method approach as just shown for the ADC consideration applies. Similar to the LSB voltage in the ADC the RDAC resolution now only impacts the requirements of the comparators' input offset voltage. The input offset voltage must however also reside in the range of several millivolts for a lower RDAC resolution in order to keep the window size of voltage overhead over the current regulator as small as possible. The impact of the RDAC resolution is thus also negligable up to a point where the added input offset voltages of the two comparators become bigger than one V_{step}.

By means of a sensitivity analysis, it is finally possible to determine an optimum RDAC size balancing these needs and demands of hardware effort and efficiency in a final target implementation in order to realize an optimal performance. Based on the calculations shown above, it is hence expected that an RDAC featuring a resolution of up to 12 bit is reasonably feasible in terms of circuit complexity and hardware costs, while limiting $\Delta V_{D,window}$ to a maximum value slightly above the corresponding step size V_{step} of several millivolts depending on the desired output voltage range.

5.2.2 Digital Control Algorithm for Dynamic Headroom Regulation

Fig. 5.6 shows the flowchart of the proposed digital control algorithm for dynamic headroom regulation with an RDAC. In each PWM period the control algorithm measures the current drain potential V_D and stores it in a (volatile) memory. After a certain number of PWM cycles m have passed, the digital control logic computes the mean value $V_{D,mean}$ of the recorded drain potentials V_D and evaluates it according to predefined voltage levels $V_{D,min}$,

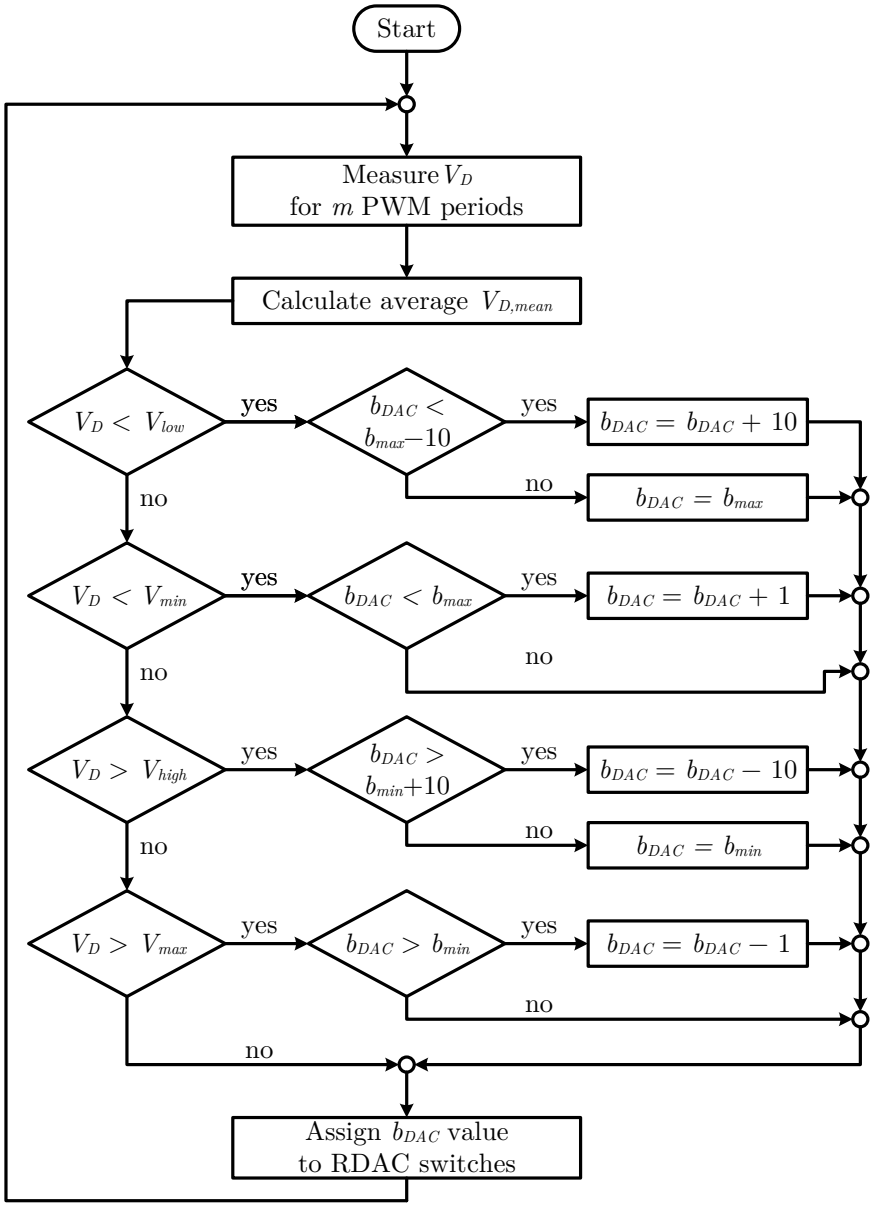


Figure 5.6: Flowchart of the digital dynamic headroom control.

$V_{D,max}$, $V_{D,low}$ and $V_{D,high}$. The digital control aims to keep $V_{D,mean}$ within the window of $V_{D,min}$ and $V_{D,max}$ according to equation 5.11. This window size is programmable and depends on the targeted application or implementation. If the measured mean value $V_{D,mean}$ lies outside of this predefined window, the digital control changes the RDAC control word b_{DAC} in steps of one in the respective direction. The voltage levels $V_{D,low}$ and $V_{D,high}$ specify thresholds for larger deviations of $V_{D,mean}$ and are also user-programmable. In theses cases, if the measured averaged drain potential is far away from the target value, the digital control increases the step size of b_{DAC} to ten. By this means settling time for larger voltage deviations is significantly reduced and thereby enhanced regulation speeds can be realized, especially at power-on with a large number of LEDs [236]. The control routine follows the first path, whose condition is true. Once the corresponding statement is evaluated, it assigns the new value for b_{DAC} to the RDAC's switches setting the resistive value of R_B [237] accordingly.

Sensing V_D is an essential and hence crucial task because the digital control logic completely relies on V_D as its main feedback control variable and its correct measurement. Therefore, an ADC with decent precision samples the drain potential V_D at a fixed timing with respect to the PWM period and at steady state conditions, once the LED current has settled to its target value. The sampling point of time, at which the voltage measurement of V_D is taken, needs to be selected carefully in order to ensure reliable sensing that is applicable to all possible PWM duty cycles. Certainly, the voltage sensing of V_D thus has to happen before the minimum on-time $t_{PWM,on,min}$ of a PWM period has passed but still after LED current has stabilized after turn-on. Therefore, the subsequent equation,

$$t_{stable,I_{LED}} < t_{sense,V_D} < t_{PWM,on,min}\,, \tag{5.26}$$

has to be maintained. It should be noted that the minimum on-time $t_{PWM,on,min}$ of the linear current regulator determines the lowest brightness level and in conjunction with the applied PWM frequency f_{PWM} sets the dimming contrast ratio accordingly.

Averaging of V_D over m periods provides two main benefits in terms of control. First, computing an average of V_D provides a more accurate voltage level to be regulated to since voltage spikes or any other distortions will be leveled out. Secondly, control speed of the dynamic headroom regulation is influenced by the number of averaging cycles m. In fact, adjusting the number of averaging cycles varies the delay introduced into the control loop [237] and inherently ensures precise timing control of regulation speed. This property is very useful in decoupling the three independent control loops of the proposed LED driving

system. While current regulation and internal control of the switching pre-regulator have to run at a relatively high speed, the adaptive dynamic headroom control can be rather slow. Therefore, it is possible to find an optimum trade-off between accuracy, regulation speed and loop stability.

As depicted in Fig. 5.6 the digital control logic also features high flexibility for deployment in different hardware implementations because LED supply voltage can also be limited in software by specifying minimum and maximum values for b_{DAC}. Besides good flexibility, an adaptable regulation speed for control loop decoupling and an optimized trade-off between efficiency and circuit complexity, the presented concept offers another significant advantage as explicated in the following. Typically, mismatch or offset errors arising from component tolerances have to be considered or may even decrease performance in a real hardware implementation. For the presented LED driver this mainly affects the RDAC's resistances. Occurring differences from the nominal values may introduce an offset at the feedback pin V_{FB} or even worse lead to a non-monotonic behavior of the RDAC. The presented digital control strategy copes with any of these possible distortions. Because V_D is measured continuously the control automatically compensates for any offsets or mismatches. Even if the RDAC becomes non-monotonic, the loop remains stable and regulates V_D to the desired target value.

5.2.3 Stability Considerations for Decoupling the Three Interacting Control Loops

As pointed out at the end of section 5.1, the proposed digital dynamic headroom regulation method features three independent control loops that interact with one another. Fig. 5.7 highlights these control loops as part of the proposed system concept. Control loop I describes the current regulation process within the linear current regulator, whose performance is dominated by the gain-bandwidth product (GBW) of the employed opamp acting as an error amplifier. The second control loop, which is named loop II, represents the inner control loop of the power converter, which determines the LED supply voltage $V_{DD,LED}$. The regulation speed of this loop is set by the switching frequency f_{sw} of the power converter. Control loop III is the digital dynamic headroom regulation sensing the drain potential V_D and steering the RDAC situated at the feedback pin of the power converter. Its control speed can be adjusted digitally, e.g. by the applied sampling rate of the V_D-sensing ADC or the used number of averaging cycles.

As outlined in section 5.1 it becomes obvious from a system point of view that loop I must be the fastest control process in order to avoid any ripple on the LED

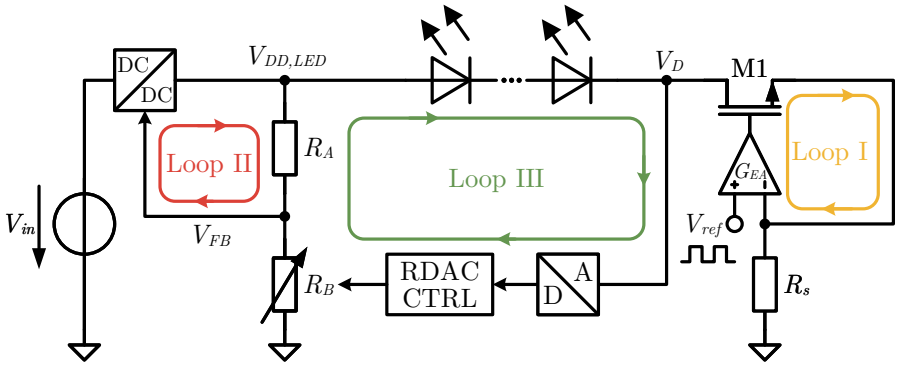
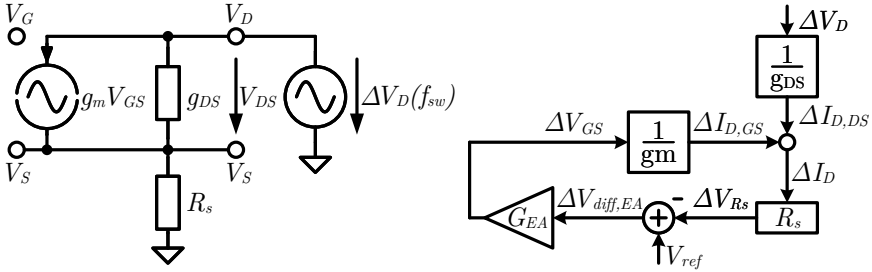


Figure 5.7: Interacting control loops within the proposed digital dynamic headroom regulation concept.

current flow despite the present voltage ripple on ΔV_D induced by the switching pre-regulator. From this perspective, control loop II of the power converter hence needs to feature the second fastest regulation speed because it determines the size of voltage ripple ΔV_D over the linear current regulator, which shall be kept as small as possible for efficiency reasons. Control loop III remains as the slowest of the three loops. Its control speed can indeed be much slower than the regulation speeds of loops I and II because the voltage minimization process of the dynamic headroom control is only relevant regarding minimizing static DC losses over the linear current regulator caused e.g. by temperature or aging effects and is hence not timing critical. To avoid interference between all control loops two main cases thus need to be investigated regarding stability considerations, namely the inference between loop I and loop II as well as the interference between loop II and loop III.

Stability Criterion for Interference Between Loop I and Loop II

The coupling between control loop I and control loop II happens at the drain connection of the linear current regulator. The switching of the DC-DC converter introduces a voltage ripple at V_D with its switching frequency f_{sw}. This voltage ripple represents an external distortion to the current regulator, who aims to counteract this unwanted distortion. For a stability analysis it is therefore helpful to examine the small-signal behavior of the proposed circuit concept. Fig. 5.8 consequently shows the small-signal representation of the



(a) Small-signal equivalent circuit diagram for MOSFET M1.

(b) Small-signal block diagram for control loop I.

Figure 5.8: Small-signal equivalent circuit diagrams for control loop I.

current steering MOSFET M1 as well as a small-signal block diagram for loop I. Based on these small-signal representations the transfer function of control loop I is found to be equal to

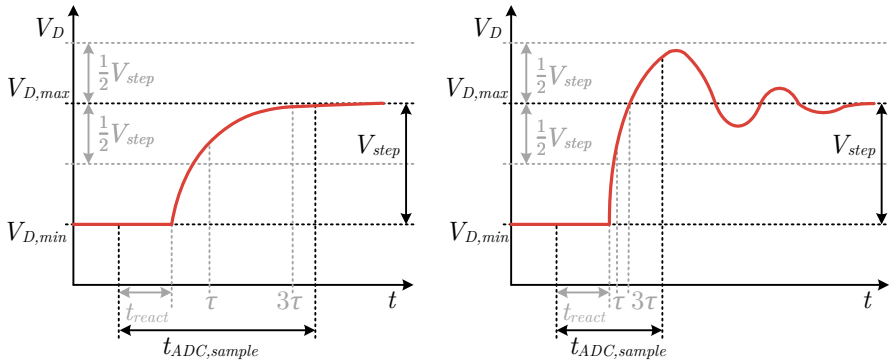
$$\frac{i_D}{v_D} = \frac{g_{DS}}{1 + R_S \cdot g_{DS} + R_S \cdot g_m \cdot (1 + G_{EA})} \,. \tag{5.27}$$

According to equation 5.27 the gain $G_{EA}\ (f)$ of the error amplifier, which is a function of frequency, finally determines the performance for a precise LED current regulation. Since the transistor M1 is meant to operate as a current sink, it needs to feature a high output resistance r_{out} even in the frequency range of the power converter's switching frequency. Therefore the stability criterion for avoiding interference between control loops I and II can be derived to

$$G_{EA}(f_{sw}) \gg 1 \Rightarrow\ r_{out} = \frac{v_D}{i_D} \rightarrow \infty, \tag{5.28}$$

$$G_{EA}(f_{sw}) \approx 1 \Rightarrow\ r_{out} = \frac{v_D}{i_D} \rightarrow \text{low ohmic}. \tag{5.29}$$

If $G_{EA}(f_{sw}) \gg 1$ is fulfilled, a good regulation performance of the LED current can thus be realized, whereas the regulation is not working anymore once $G_{EA}(f_{sw})$ reaches a value of approximately one. This means that the switching frequency f_{sw} of the power converter cannot be selected too high, but has to be chosen in dependence of the used error amplifier's gain $G_{EA}\ (f)$ or rather GBW. This demands a minimum error amplifier gain G_{EA} of at least 10 at the power converter's switching frequency to ensure high output impedance of the current regulator.



(a) Stability criteria for a step response of loop II with 90° phase margin.

(b) Stability criteria for a step response of loop II with 60° phase margin.

Figure 5.9: Stability criteria for interaction of control loops II and III.

Stability Criterion for Interference Between Loop II and Loop III

The coupling between control loops II and III happens at two places in the circuit concept, which are first the feedback pin of the power converter and second the drain connection of the linear current regulator. Since the RDAC control changes the programmable lower resistance value R_B by a hard switching mechanism, it causes a distinct voltage jump on the feedback voltage V_{FB} when assigning a new control word b_{DAC} to the RDAC. To ensure a stable operation of the proposed system, the digital dynamic headroom controller of loop III has to wait until the step response of the inner DC-DC control from loop II has settled. Not till then, when control loop II has settled for the new LED supply voltage $V_{DD,LED}$, control loop III may continue to sample the drain potential V_D. By this means, it is guaranteed that control loop III records a valid new sample for V_D with the corresponding ADC. Considering the DC-DC control loop II to hold a time constant τ_{DCDC} for its step response, it reaches close proximity of around 95 % to the target value of $V_{DD,LED}$ within a time of $3 \cdot \tau_{DCDC}$. Deriving a stability criterion for stable interaction of control loops II and III, equation 5.30 must thus be maintained,

$$\frac{1}{f_{ADC,sample}} = t_{ADC,sample} > 3 \cdot \tau_{DCDC}\,. \tag{5.30}$$

In addition to that, an overshoot to the step response may not exceed a value of $0.5 \cdot V_{step}$ since this represents half an LSB of the RDAC and would hence trigger a change in the RDAC control word thus leading to instability. Control

loop II must therefore ensure that its phase margin is large enough (e.g. $> 60°$) in any case so this boundary condition is satisfied as stated in equation 5.31,

$$V_{D,overshoot} < 0.5 \cdot V_{step} \,. \tag{5.31}$$

The stability criterion for a stable interaction of control loops II and III is hence described by equations 5.30 and 5.31 as both conditions must be fulfilled. Fig. 5.9 exemplarily illustrates these two stability conditions for different phase margins of control loop II, which are approximately 90° and 60°.

5.3 Implementation of the Developed LED Driver

As a proof of concept and for a thorough performance evaluation regarding efficiency, current accuracy, loop stability and circuit complexity the proposed LED driver concept has been implemented in a real hardware setup. Thereby, this work focuses on performance optimization of a one-channel LED driver, as mentioned earlier. According to the specifications derived in sections 2.4, the system operates from a fixed DC input voltage of $V_{in} = 24\,\text{V}$ while it regulates LED current to a nominal value of $I_{LED,nom} = 700\,\text{mA}$. Dimming resolution N_{PWM} of the PWM control is set to 16 bit applied to a PWM dimming frequency of 1 kHz. The proposed dynamic headroom regulation concept is realized with commercially available off-the-shelf (COTS) components. Fig. 5.10 shows the assembled PCB highlighting each main block with its relevant circuit parts. In completion to the design considerations emphasized in conceptual chapters 5.1 and 5.2 the subsequent sections 5.3.1 to 5.3.3 will give a deeper insight in implementation aspects for each of the three main blocks of the developed LED driver.

5.3.1 Buck-Boost Converter for LED Power Supply

A buck-boost converter has been chosen as switching pre-regulator to provide the desired high output voltage swing for enhanced flexibility. The chosen SMPS controller IC [364] features an input voltage range between 4 V to 38 V and provides the desired feedback voltage pin V_{FB} needed for the digitally assisted dynamic headroom control. Furthermore, the buck-boost controller IC is capable of realizing output voltages in the range of 0.8 V to 38 V. The relatively wide input and output voltage ranges already indicate the high flexibility of the proposed concept implementation. In case of white LEDs with a typical forward voltage of $V_F \approx 3.6\,\text{V}$ the LED driver could e.g. drive up to ten LEDs in series. Fig. 5.11 shows the physical implementation of the

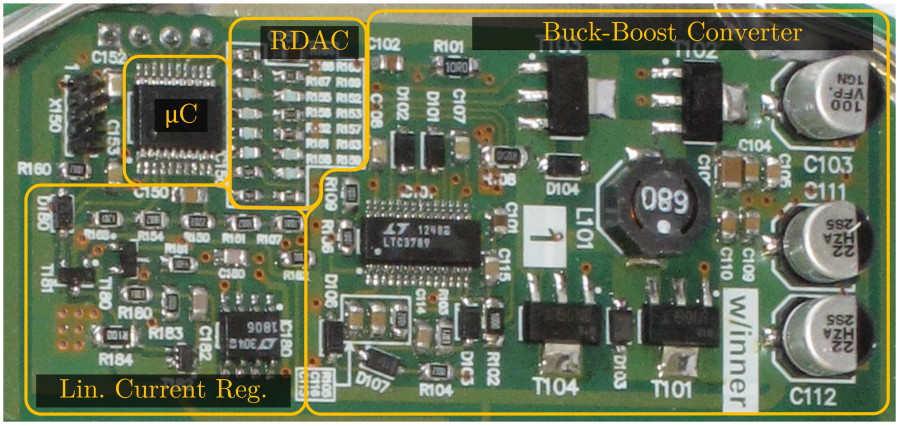


Figure 5.10: Photographic image of the implemented LED driver with a digitally assisted dynamic headroom regulation.

buck-boost converter in conjunction with the RDAC based dynamic headroom control and the linear current regulator.

Depending on the chosen LED load and with regard to the selected fixed DC input voltage the converter may hence operate in different modes, which are buck, buck-boost and boost operation [364]. Of course, this degree of flexibility impacts efficiency to some extend. Fig. 5.12 illustrates this effect by showing the efficiency dependency versus output voltage for two different fixed DC input voltages of $V_{in,DC1} = 12\,\mathrm{V}$ and $V_{in,DC2} = 24\,\mathrm{V}$. Output current was kept at a constant level of $I_{out} = 700\,\mathrm{mA}$ in both cases to ensure a fair comparison. As can be seen, the applied buck-boost converter features very high efficiencies of more than 90 % over nearly the entire output voltage range. For safety reasons the curves were only measured up to $V_{out} = 32.3\,\mathrm{V}$. This limitation results from the maximum value of b_{DAC} set to $b_{max} = 200$. The full output voltage is yet not reached for $V_{in} = 12\,\mathrm{V}$ because the input current is limited by $R_{s,1}$ (see Fig. 5.11), which has been chosen for 24 V operation. For the following measurements V_{in} is kept at a fixed level of 24 V.

Although the buck boost converter's controller IC would be capable of directly operating from the fixed DC input voltage of $V_{in} = 24\,\mathrm{V}$ alone, it is powered by an additional 5 V supply. Thereby, efficiency of the controller IC is boosted significantly [236], [237], [364]. A final target implementation of the LED driver would hence require the usage of an additional step-down converter to provide this 5 V supply. Since some other auxiliary circuitry like the MCU for the digital

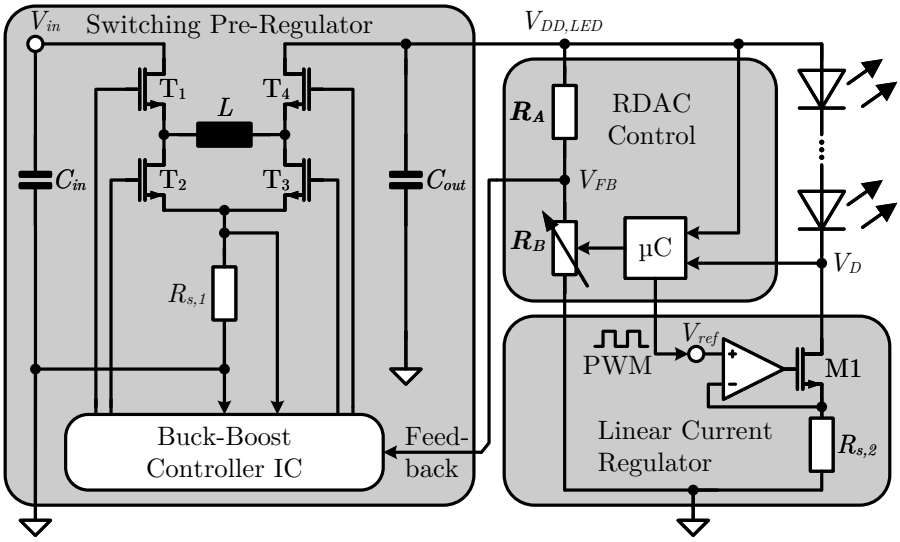


Figure 5.11: Implementation of the switching pre-regulator as a buck-boost converter with an RDAC based dynamic headroom control.

control or the bandgap reference of the linear current regulator would require this 5 V supply anyways, it does not represent a major drawback. In fact, if multiples of the proposed LED driver are used in a color mixing luminaire, all these drivers could be supplied by one single 5 V supply.

The implemented buck-boost converter operates at a fixed frequency of $f_{buck\text{-}boost} = 400\,\text{kHz}$, which has been chosen as a good trade-off between efficiency and output voltage ripple [236], [237]. Since the number of series-connected LEDs per string defines the regulated output voltage of the converter, maximum available output power depends on the provided LED current that can be drawn. External components like the power switches and the main inductance of the buck-boost converter have to be selected accordingly and limit available output current to the extend of their physical properties. In compliance to the specified nominal LED current of $I_{LED,nom} = 700\,\text{mA}$ all external components of the buck-boost converter, namely the power switches $T_1 - T_4$ [367], the inductor $L = 68\,\mu\text{H}$ [372] and the sense resistor $R_{s,1}$ [353] are selected to withstand a current flow in excess of 900 mA including a certain safety margin [237].

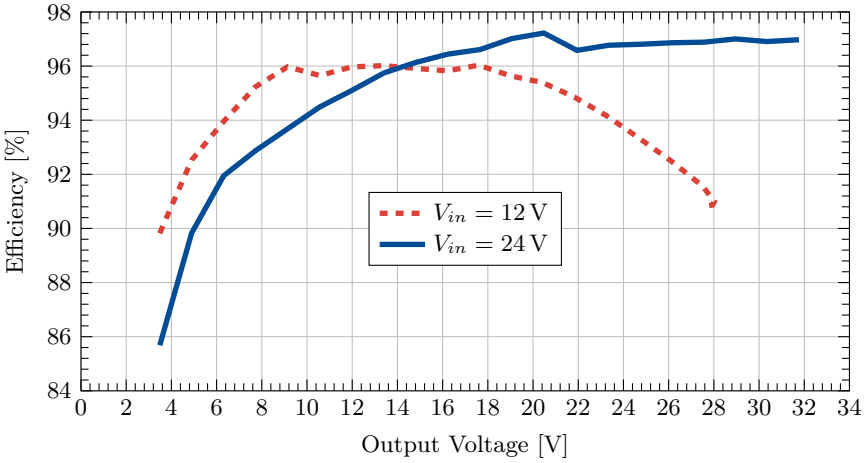


Figure 5.12: Measured efficiency of the buck-boost converter versus output voltage for a constant current load of $I_out = 700\,\mathrm{mA}$.

5.3.2 PWM-controlled Linear Current Regulator for Precise Brightness Adjustment

Precise current control is a key performance parameter in LED driver design since current accuracy impacts brightness and color perception of the human eye as highlighted in section 2.3.1. In order to minimize any color shifts or perceivable brightness fluctuations, the LED current control loop has to be designed for a very fast regulation speed while maintaining good accuracy, which keeps the LED current level nearly perfectly flat. A second major requirement for achieving exceptional optical performance is a high contrast dimming ratio while realizing highest possible PWM dimming frequency. This demand consequently requires very fast switching and hence short turn-on and turn-off times of the PWM controlled linear current regulator. Aiming for a precise target current with minimal deviations the linear current regulator has to cope in fact with all kinds of variations on the LED supply voltage. This requirement yet involves an additional voltage headroom over the regulator itself, which has to be included as a safety margin in the design considerations. Clearly, this headroom voltage critically effects electrical efficiency because it represents an additional power loss consumed in the main power MOSFET of the linear current regulator. It

is hence desirable to keep the required safety margin of the voltage drop over the regulator as small as possible.

In the proposed conceptual design two major contributors determine the amount of headroom voltage needed. This is on the one hand the output voltage ripple of the buck-boost converter and on the other hand distinct voltage dips of the LED supply voltage occurring at fast load transients due to the PWM switching of the linear regulator in dimming operation mode. Minimizing the output voltage ripple of the DC-DC converter while achieving small dips at load transients thus brings the desired efficiency increase. Both, output voltage ripple and transient voltage dips, depend on the performance of the switching pre-regulator, namely converter accuracy, selected output capacitance and applied regulation speed of the converter control. Additionally, the fast turn-on behavior of the current regulator also affects the magnitude of the transient voltage dips. As a result, the design of the buck-boost converter has to be matched to the one of the linear current regulator in order to find the aspired sweet spot for outstanding optical performance in conjunction with high energy efficiency. The fixed buck-boost converter frequency of 400 kHz is found by this optimum trade-off balancing output voltage ripple and converter efficiency while matching to the transient behavior of the linear current regulator. Designing the proposed LED driver concept requires to solve the conflict of aims between contrast dimming ratio, LED current precision, regulation speed, output voltage ripple and converter efficiency under pre-defined conditions leading to an optimized trade-off solution.

Fig. 5.13 shows the designed hardware implementation of the linear current regulator including its compensation network and PWM control circuit. As can be seen, a conventional architecture of a linear current regulator has been applied. Fast regulation speeds as well as short turn-on and turn-off times are realized by a high-speed opamp [360] and a power MOSFET [371] featuring relatively low gate capacitance C_G. By these means a minimum on-time of $t_{PWM,on,min} = 4\,\mu s$ was achieved, which determines the lowest possible light level in the given setup. To avoid any overshoots or oscillating behavior capacitors $C_{comp,1}$ and $C_{comp,2}$ have been inserted in the proposed circuit implementation as depicted in Fig. 5.13 [237]. PWM dimming is performed by pulsing the bandgap reference voltage V_{ref} with a digital control signal. In the on-phase (V_{PWM} ='1') transistor $\mathrm{T_{PWM}}$ conducts and passes V_{ref} over a resistive divider to the positive input pin of the high-speed opamp. The ratio of this resistive divider formed by resistors $R_{set,1}$ and $R_{set,2}$ defines the desired target current for a given reference voltage V_{ref}. In the PWM off-phase (V_{PWM} ='0') transistor $\mathrm{T_{PWM}}$ is not conducting. Resistor $R_{set,2}$ then pulls the positive opamp input port down to ground, which sets the target current to zero. To

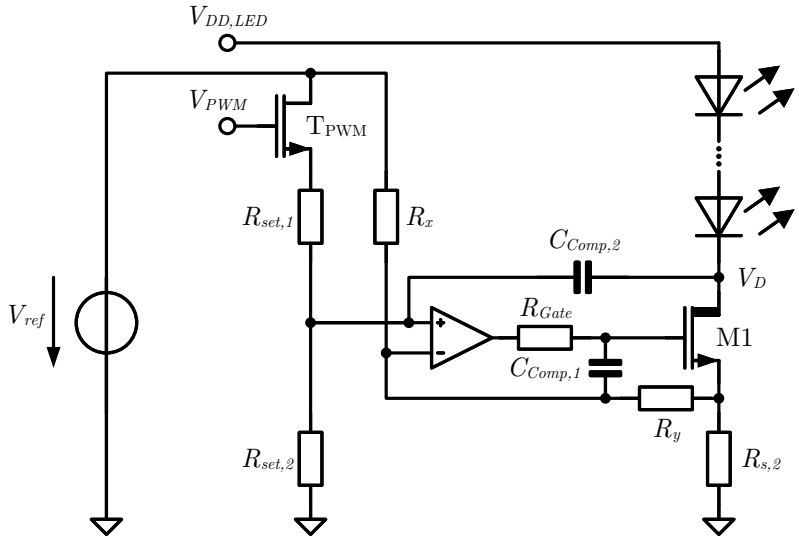


Figure 5.13: Schematic of PWM-switched linear current regulator with compensation network.

ensure transistor M1 is in fact disabled it has to be accounted for a certain input offset voltage of the high-speed opamp. Therefore, a small resistance R_y inserted in the feedback path and a large pull-up resistance R_x lifting the negative opamp input by a few millivolts have been added [237]. PWM dimming is implemented with a fixed target frequency off_{PWM}= 1 kHz while using 16 bit of resolution in the digital domain for precise brightness adjustment and – if using multiple channels – precise color control. In conjunction with the minimum possible on-time of $t_{PWM,on,min} = 4\,\mu s$, the 1 kHz PWM frequency determines a dimming contrast ratio of 250 : 1, which results in a minimum duty cycle of 0.4 %.

5.3.3 Digital Dynamic Headroom Control with an RDAC

The digital RDAC feedback control has to cover the pre-defined wide output voltage range from $V_{out,min} = 4\,V$ to $V_{out,max} = 38\,V$ with an optimized resolution balancing the trade-off between minimum adjustable step size V_{step} and lowest circuit complexity. On the one hand, a higher RDAC resolution reduces the additional voltage drop over the current regulator by diminishing the adjustable step size and hence boosts efficiency. On the other hand, the

circuit complexity and hardware effort increases with each additional bit of the RDAC needed. As a fair trade-off between step size and circuit complexity, the resolution of the RDAC has been chosen to 8 bit for the presented implementation with discrete components. Furthermore, the used μC only provides 8 ports for the RDAC control. Of course, even higher values of up to 12 bit are indeed expected to be reasonably feasible for the RDAC as mentioned earlier in section 5.2, but these high resolutions are preferably, if not only, achieved in monolithically integrated ASIC solutions.

Accounting for certain tolerances and variations in the real hardware setup, the voltage range covered by the RDAC has been slightly increased to $V_{out,min} = 3.5\,\mathrm{V}$ and $V_{out,max} = 40\,\mathrm{V}$. In doing so the highest possible output voltage that can be adjusted could however exceed the buck-boost controller's maximum of 38 V [364]. This circumstance is in fact critical in the final application as it might even lead to device destruction. Here comes the flexibility of the digital control algorithm into play, which enables an output voltage limitation of $V_{DD,LED}$ by software programming as shown in the flowchart, Fig. 5.6. The control algorithm thereby ensures an *"always safe"* operation by selecting appropriate minimum and maximum levels for b_{DAC}. The b_{max} limitation consequently must be selected in a manner that the corresponding output voltage is lower than the maximum rating of the used buck-boost controller IC [364]. In the proposed implementation b_{min} is chosen to be zero and b_{max} is set to 200 corresponding to a maximum voltage $V_{DD,LED}$ of 32.3 V [236], [237].

Following the design procedure and relationships explained in section 5.2 the RDAC resistances can consequently be dimensioned according to equations 5.2 to 5.8. The internal feedback voltage of the used buck-boost converter, which is regulated to $V_{FB} = 0.8\,\mathrm{V}$, in conjunction with the transfer function stated in equation 5.2 denotes the relationship of R_A and R_B. Applying certain boundary conditions to this equation or even to the modified, digitally controlled transfer function of equation 5.8 directly delivers a dimensioning instruction. If the output voltage $V_{DD,LED}$ reaches its minimum of 3.5 V, the lower resistance R_B is at its maximum, which is in fact R_{max}, and b_{DAC} equals zero. Both equations 5.2 or 5.8 thus lead to the subsequent relationship

$$R_A = \frac{V_{DD,LED,min}}{V_{FB,ref,int}} \cdot R_{max} - R_{max}\,, \tag{5.32}$$

$$= \frac{3.5\,\mathrm{V}}{0.8\,\mathrm{V}} \cdot R_{max} - R_{max} = 3.375 \cdot R_{max}\,. \tag{5.33}$$

In case of the maximum possible output voltage of $V_{DD,LED} = 40\,\mathrm{V}$, the lower resistance R_B reaches its minimum value, which means that b_{DAC} is also set to

its highest value of $b_{DAC} = 2^{N_{DAC}} - 1 = 2^8 - 1 = 255$. Applying this boundary condition again to equation 5.8 yields the relationship for R_1 as follows,

$$R_1 = \frac{b_{DAC} \cdot R_A \cdot R_{max}}{\left(\frac{V_{DD,LED,min}}{V_{FB,ref,int}} - 1\right) \cdot R_{max} - R_A} \,. \tag{5.34}$$

Inserting equation 5.33 into 5.34 yields the dimensioning of the highest DAC resistance R_1,

$$R_1 = \frac{3.375 \cdot b_{DAC} \cdot R_{max}}{\left(\frac{V_{DD,LED,min}}{V_{FB,ref,int}} - 1\right) - 3.375} \,, \tag{5.35}$$

$$= \frac{3.375 \cdot 255}{50 - 4.375} \cdot R_{max} = 18.86 \cdot R_{max} \,. \tag{5.36}$$

Once the highest resistance R_1 in the RDAC chain is found, all the other ones, R_2 to R_8, can easily be computed by equation 5.5. In the current implementation R_{max} is chosen to equal 68 kΩ. Following equations 5.32 to 5.36 all resistance sizes are computed to the values stated in table 5.1. Applying equation 5.10 the output voltage of the buck-boost converter $V_{DD,LED}$ can be adjusted in steps of approximately 143 mV for the given dimensioning according to

$$V_{step} = \frac{40\,\text{V} - 3.5\,\text{V}}{255} \quad = \quad 143\,\text{mV} \,. \tag{5.37}$$

Based on the computation of V_{step} it is possible to select the window size of $V_{D,min}$ and $V_{D,max}$ for the digital control algorithm according to the flowchart depicted in Fig. 5.6. Since the current regulator requires at least a voltage headroom of about 400 mV to compensate for fluctuations on the LED supply voltage $V_{DD,LED}$ and in compliance with equation 5.11, the regulated drain potential should reside within a range of $V_{D,min} = 400\,\text{mV}$ and $V_{D,max} = 550\,\text{mV}$. Choosing $V_{D,min}$ and $V_{D,max}$ in this manner, equation 5.14 still persists considering $V_{step} \approx 143\,\text{mV}$. In case the measured drain potential falls outside

Table 5.1: Selected resistance values for the implemented 8 bit RDAC.

Resistance	R_A	R_{max}	R_1	R_8
Value	230 kΩ	68 kΩ	1.28 MΩ	10 kΩ

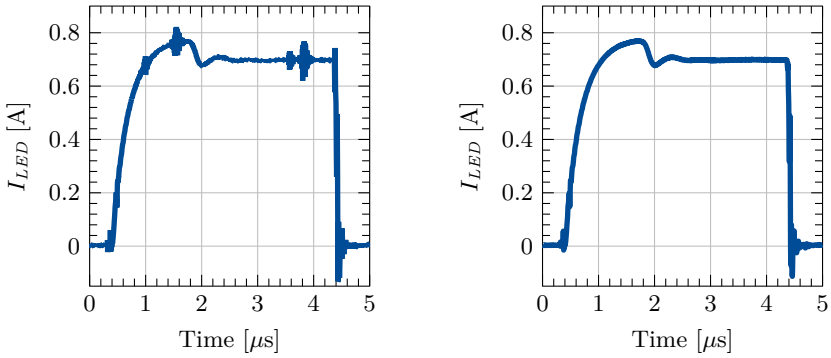
this predefined window, the user-programmable thresholds $V_{D,low} = 0.1\,\mathrm{V}$ and $V_{D,high} = 2\,\mathrm{V}$ speed up the settling time of the regulation process by increasing the step size from 1 V_{step} to 10 V_{step}, as explained earlier and shown in Fig. 5.6.

To ensure reliable measurements of the drain potential $V_{D,sense}$ the measurement point of time t_{sense,V_D} has to be chosen properly according to equation 5.26. In the presented setup t_{sense,V_D} has been set to 3 µs as the LED current settles for a stable flat line at around $t_{stable,I_{LED}} = 2.5\,\mu\mathrm{s}$, which is shown in the subsequent performance evaluation chapter.

5.4 Performance Evaluation and Measurement Results of the Developed LED Driving Stage

The two main key features for an excellent LED driver performance are first providing very high efficiency and second achieving outstanding optical properties, such as linear dimming range, precise brightness level control, good color point stability, high dimming contrast ratio or preventing any kind of flicker. The discussion in section 2.3.1 emphasized that these optical properties are mainly related to waveform and accuracy of the LED current flow, which particularly depend on the performance of the PWM-switched linear current regulator. Therefore, this chapter evaluates the proposed LED driver concept based on measurement results of the presented hardware implementation with particular regard to its timing behavior, achieved LED current accuracy and overall electrical efficiency. Furthermore, other important criteria, such as hardware complexity, flexibility, robustness and loop stability are assessed. All results are in the end compared to other state-of-the-art solutions.

At first, the PWM-switched linear current regulator shall be investigated in detail since its performance determines not only accuracy and timing behavior of the LED current but also affects efficiency by its needed overhead voltage. Fig. 5.14 shows two measurements of the regulated LED current I_{LED} recorded for the shortest possible PWM duty cycle of $D_{PWM,min} = 0.04\,\%$ when the LED driver operates a load of five series-connected LEDs. The first plot Fig. 5.14a illustrates a one-shot measurement, while the second graph Fig. 5.14b depicts an averaged curve of the recorded LED current. Both measurements indicate that a minimum on-time of $t_{PWM,on,min} = 4\,\mu\mathrm{s}$ is realized, while fast turn-on and turn-off times are achieved. The LED current settles to its desired target value of $I_{LED} = 700\,\mathrm{mA}$ at around 2 µs after turn-on, whereas switching off happens nearly instantaneously. The steep transient at turn-off though causes a minor ringing effect on the LED current, which may be neglected, since it does not affect any visible property nor impacts electrical characteristics significantly.



(a) One-shot measurement of I_{LED}.

(b) Averaged measurement of I_{LED}.

Figure 5.14: Measurement of LED current I_{LED} for a min. PWM on-time of $t_{min,on} = 4\,\mu s$ while operating five series-connected LEDs.

Both subplots appear almost identical, but still differ in a high frequency noise visible in the one-shot measurement. These distortions occur at four distinct points of time during the minimum PWM interval and originate from the buck-boost converter switching its four power MOSFETs. The switching frequency of the power converter of $f_{DC\text{-}DC} = 400\,kHz$ can be observed in the graph between two associated spikes. The other two switching events happen within a much shorter time interval and are hence correlated to a non-overlapping control of the buck-boost controller IC [364]. It has been found that these noisy injections of the DC-DC converter appear at a random timing with regard to the PWM dimming frequency of $f_{PWM} = 1\,kHz$. Hence, they have no effect on the optical performance. First, the human eye averages perceived brightness and cannot detect such (high-frequency) fluctuations in the LED current. And second, the switching frequency of the buck-boost converter is by far too high to cause any (visible) flicker or other comparable effects affecting optical light output of the LED driver.

Although these high frequency distortions may be neglected, the switching pre-regualtor impacts the performance of the linear current regulator. As mentioned in section 5.1 two main contributors have been identified, which are the inherent voltage ripple of the supply voltage $V_{DD,LED}$ and voltage dips induced at hard switching load transients occurring at turn-on of each PWM cycle. In order to investigate the effect of output voltage ripple on actual LED current the deviations of both, LED supply voltage $V_{DD,LED}$ and

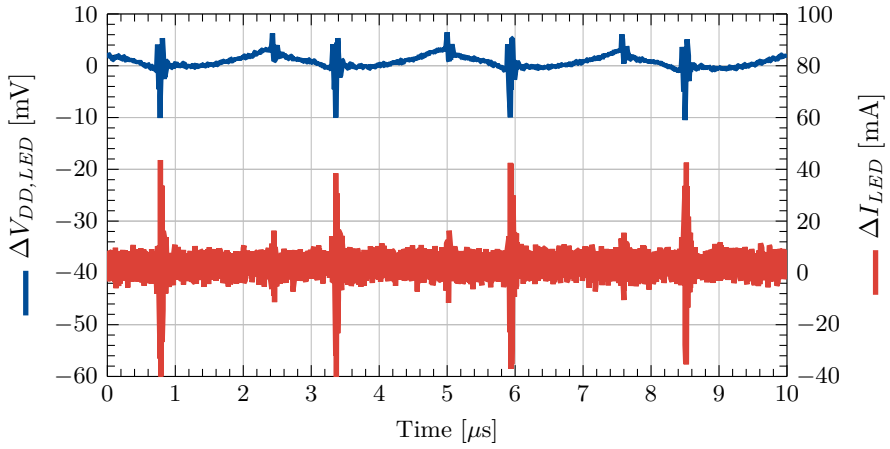


Figure 5.15: Measured Variations of I_{LED} and $V_{DD,LED}$.

LED current I_{LED}, to their nominal values have been measured simultaneously. Fig. 5.15 shows the corresponding measurement curves. The output voltage ripple $\Delta V_{DD,LED}$ is much less than 10 mV and thus has no influence on the LED current deviations. On the contrary, the high frequency spikes originating from the SMPS switching its four power MOSFETs clearly provoke a measurable deviation in the regulated LED current as just outlined in the subsequent paragraph. Peak current deviations of up to $\Delta I_{LED} \approx 50$ mA have been recorded for ultra short time intervals as highlighted in Fig. 5.15. The switching events caused by the buck-boost converter also result in sharp transient distortions on LED supply voltage of about $\Delta V_{DD,LED} \approx 10$ mV at the same time. These deviations on both, supply voltage and LED current, are yet negligible in terms of optical and electrical performance of the linear current regulator as already explained above. Whether these sharp short transients have any effect on EMI, has not been investigated yet and might hence be subject to future work. Fig. 5.16 shows the voltage dip on the drain potential V_D of the linear current regulator at turn-on of a PWM period for a load of five series-connected LEDs. The voltage dip is about 150 mV to 200 mV large, but has no impact on the LED current and its accuracy since it has been accounted for this additional voltage headroom over the linear current regulator. However, decreasing the size of these voltage dips would boost efficiency of the LED driver significantly as the additional voltage headroom could be reduced by the same amount saving the corresponding static losses.

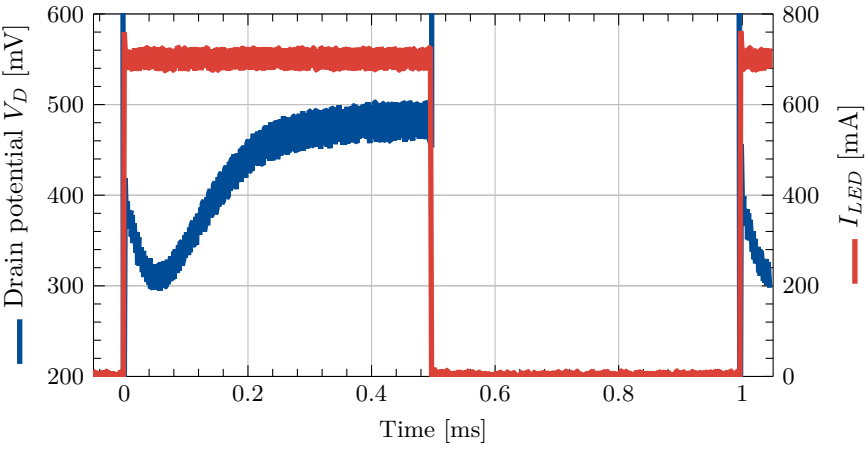


Figure 5.16: Voltage dips on drain potential V_D at 50 % PWM duty cycle.

Assuming a forward voltage for a single power LED of $V_{F,LED} \approx 3\,\text{V}$ while a current of $I_{LED} = 700\,\text{mA}$ is flowing, the minimization of these voltage dips may even lead to efficiency improvements of up to 5.2 % depending on the load connected to the LED driver. Table 5.2 shows the associated efficiency improvements versus the number of LEDs connected in series for a voltage headroom reduction of the drain potential V_D from 500 mV to 300 mV. Obviously, the efficiency enhancement decreases with increasing output power because the amount of saved losses remains constant in all cases. For a typical scenario in interior lighting it is hence fair to assume an efficiency boost of approximately 1 %. However, the voltage headroom savings are not achievable with the presented discrete hardware implementation because of using an off-the-shelf SMPS as the switching pre-regulator. Building a monolithically integrated solution of the proposed concept on the contrary might actually yield the calculated energy savings since it is possible to directly influence the control of the pre-regulator

Table 5.2: Efficiency Enhancement $\Delta\eta$ in % versus number of LEDs N_{LED} connected as load when reducing V_D from 500 mV to 300 mV.

N_{LED}	1	2	3	4	5	6	7	8	9	10
$\Delta\eta$ in %	5.19	2.93	2.04	1.56	1.27	1.06	0.92	0.81	0.72	0.65

and adjust it precisely to system needs as well as to the timing behavior of the linear current regulator. A more detailed description on this idea is given in the subsequent chapter 6, in which a monolithically integrated solution is introduced. In this context, section 6.3 discusses efficiency improvements due to a synchronized control of the three independent regulation loops, which relies on the work presented in [313].

The main parameter that is influenced by the performance of the linear current regulator is in fact LED current accuracy. Under steady-state conditions a constant LED current of $I_{LED} \approx 708\,\text{mA}$ is measured. In comparison to the desired nominal current level of $I_{LED,nom} = 700\,\text{mA}$ this results in a static deviation of less than 1.2 %. This high degree of accuracy is in fact maintained over the entire dimming range, as presented in Fig. 5.17. Above a dimming level of 5 % a current accuracy of at least 98.8 % is thus achieved resulting from a deviation smaller than 1.2 %. Investigating the graph in detail reveals two error mechanisms influencing LED current accuracy, namely first a static deviation under steady-state conditions and second a dynamic contribution dominating at lower dimming levels. Corresponding to these error mechanisms two main contributors have been identified, which are on the one hand certain component tolerances and on the other hand the transient behavior of the linear current regulator at turn-on, respectively. The static deviation from the nominal LED current results from an offset voltage present at any of the opamp inputs and may hence be introduced by both sensing and reference voltage. $R_{set,1}$ and $R_{set,2}$ in conjunction with the band gap voltage reference $V_{BG,ref}$ determine the accuracy of the reference input, whereas variations on the sensing resistance $R_{s,2}$ directly influence the voltage at the sense pin. In the presented hardware setup resistances with an accuracy of 1 % have been used. The employed band gap IC [369] reference voltage of $V_{BG,ref} = 1.2\,\text{V}$ with a precision of 2 %. The dynamic contribution arises from the transient turn-on behavior of the linear current regulator and becomes predominate at lower dimming levels. This fact becomes obvious when recalling the transient LED current waveform for the minimum on-time from Fig. 5.14. During settling time the LED current is by far off of its desired target level. Since the settling phase becomes relatively speaking bigger when decreasing the PWM duty cycle, the erroneous deviation from the nominal LED current level also increases. For higher PWM duty cycles the short turn-on phases is leveled out due to averaging over the entire on-time [237]. Fig. 5.17 illustrates this fact since the current deviation remains nearly constant for light levels higher than 20 % dimming. For the presented implementations the measurements show an opposite effect of both error mechanisms. Static and dynamic contribution cancel each other at around 4 % PWM duty cycle. While the dynamic error will always lead to a negative

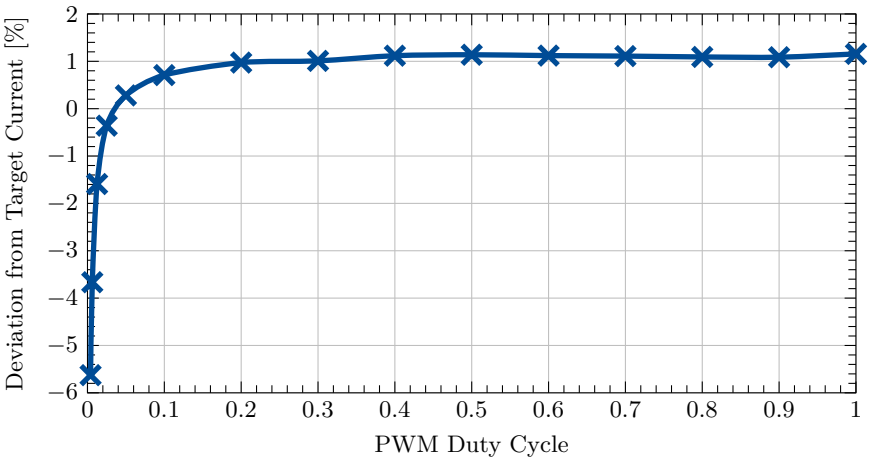


Figure 5.17: Measured current accuracy of I_{LED} with respect ot its nominal value as a function of dimming level.

deviation from the desired LED target current, the static error might change its sign depending on the component tolerances of resistors and band gab IC. Therefore, both erroneous contributions might even add up for another band gap IC and a different set of resistances resulting in an increased deviation. Particularly for an integrated solution implemented on an ASIC it is expected to eliminate the static offset error by proper calibration, e.g. trimming of the bandgap reference voltage $V_{BG,ref}$. Since $R_{set,1}$ and $R_{set,2}$ can be matched to each other, only minimal contribution is expected to originate from these two resistors. Additionally, it is expected to achieve even faster turn-on times with an ASIC implementation, which would also minimize the dynamic error contribution and limit it to very low dimming cycles. Besides featuring a very good current accuracy, the presented approach nearly eliminates any ripple on the LED current. Fig. 5.15 and Fig. 5.16 mostly show noise coupled into the measurement probe and not an effective current ripple as that ripple is much lower. A variance of $4.08 \cdot 10^{-8}$ and a standard deviation of $2.02 \cdot 10^{-4}$ from recorded current towards its DC value have been determined from another measurement [237].

Evaluating the control behavior of the presented dynamic headroom approach founds on measuring LED supply voltage $V_{DD,LED}$ over time and observing

its regulation process under steady-state load conditions. In order to ensure stable load conditions, the dimming option is disabled for this test setup and a constant current flows continuously through attached LEDs. Consequently, the developed LED driving concept regulates its output current to a constant level of $I_{LED} = 700\,\text{mA}$ at 100 % PWM duty cycle. Due to the relatively small step size of $V_{step} \approx 143\,\text{mV}$ realized by the chosen RDAC values in the developed hardware implementation, the control behavior can be monitored more precisely for lower LED supply voltages. Hence, a smaller number of LEDs is connected in series to the output of the buck-boost converter for observation purposes and chosen to a value of three for the subsequent measurements. The dynamic headroom control approach is tested and evaluated in three different application scenarios, which are the initial start-up behavior, an LED short circuit failure and thermal heating. Fig. 5.18 shows the respective voltage measurements of $V_{DD,LED}$ over time. For the sake of completeness, Fig. 5.19 additionally illustrates the same application scenarios in a single measurement for higher output voltages resulting from five to six attached LEDs.

The initial start-up of the implemented LED driver shown in Fig. 5.18a clearly illustrates a precise, fast and stable regulation behavior of the output voltage control loop. The fast regulation speed is achieved by adapting the incremental step size of b_{DAC} in the digital control algorithm depending on the difference between measured and target drain potential V_D. As explained in section 5.2 the step size decreases from ten to one, once the measured drain potential falls inside the window of

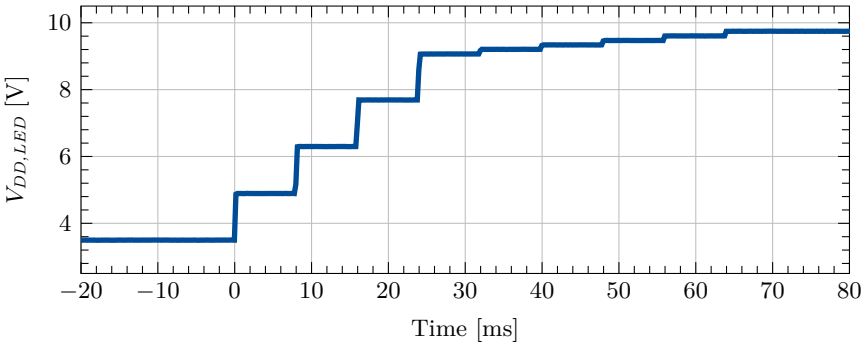
$$V_{low} \geq V_{D,measured} \geq V_{high}\,. \tag{5.38}$$

This behavior can exactly be observed in 5.18a. Directly at turn-on a step size of $b_{DAC} = 10$ is used resulting in voltage increments of

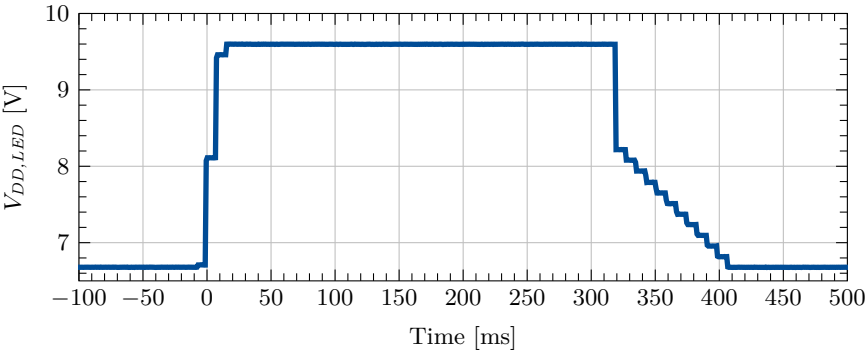
$$V_{step,big} = 10 \cdot V_{step} = 10 \cdot 143\,\text{mV} = 1.43\,\text{V}\,. \tag{5.39}$$

Approaching the final target value, the digital control algorithm reduces the increment of its control variable b_{DAC} after around 24 ms to one resulting in a smaller voltage increase of one single $V_{step} = 143\,\text{mV}$. The desired target value is finally reached at about 64 ms after turn-on. Stable operation is achieved by properly decoupling the three independent control loops from each other and setting their regulation speeds accordingly. For the presented measurements the feedback control loop of the dynamic headroom regulation operates at a comparably low speed. Its loop delay between two regulation steps is

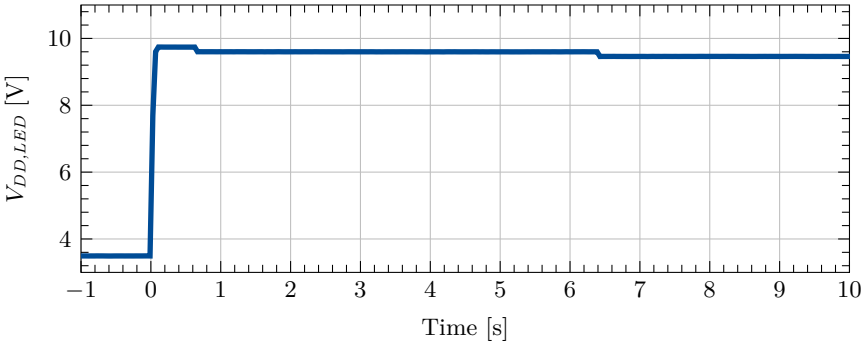
$$t_{V_D,ctrl} = 2 \cdot m \cdot T_{PWM} = 8\,\text{ms}\,, \tag{5.40}$$



(a) Measured start-up behavior of $V_{DD,LED}$ with digital dynamic headroom control.



(b) Measured dynamic headroom regulation of $V_{DD,LED}$ compensating a voltage jump.



(c) Measured dynamic headroom control compensating thermal heating of used LEDs.

Figure 5.18: Measurements of $V_{DD,LED}$ showing the control behavior of the digital dynamic headroom approach for different application scenarios.

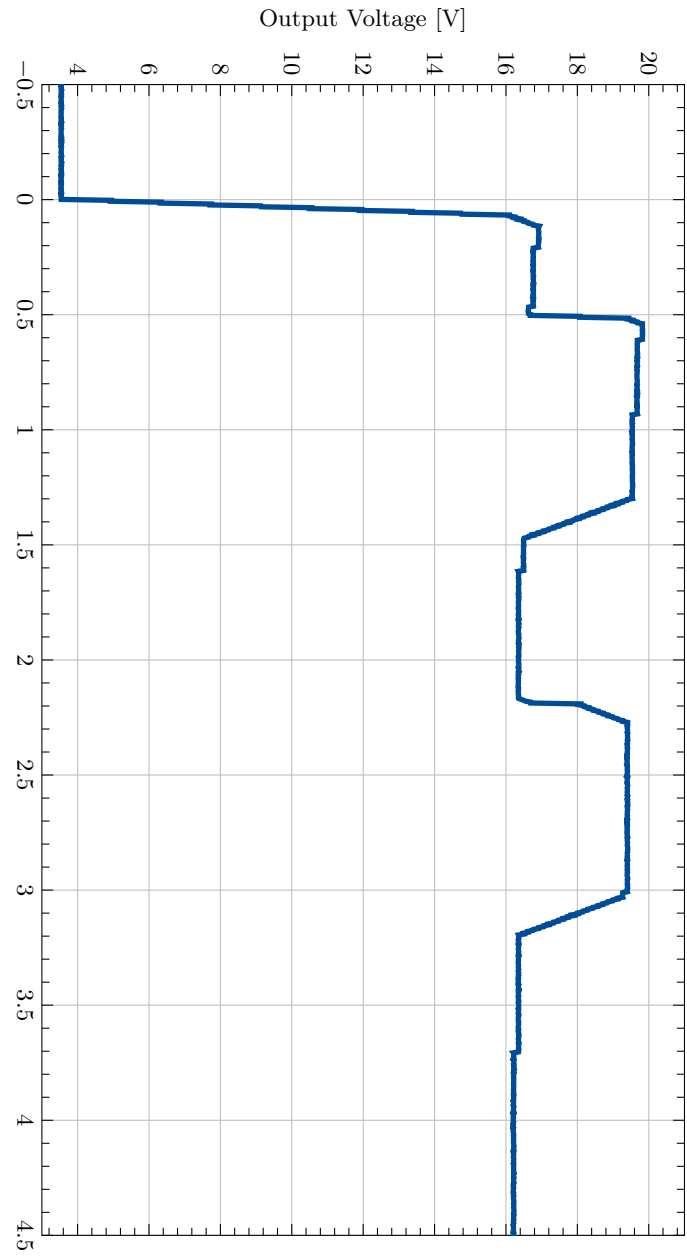


Figure 5.19: Measured control behavior of the digital dynamic headroom regulation for higher output voltages.

for the measured LED driver operating at a 1 kHz PWM frequency. The averaging factor m has been chosen to $m = 4$ referring to the closed-loop control diagram illustrated in 5.6. Due to the well designed stability of the control loop according to the derived criteria outlined in section 5.2.3 any overshoot on the LED supply voltage is avoided.

Although the dynamic voltage control loop has been designed much slower than current regulation and (inner) control of the buck-boost IC, its fast and stable control behavior can be observed in case of emulating a short-circuit failure of an LED. Fig. 5.18b depicts this emulated scenario, which would lead to a voltage jump of one LED forward voltage V_F on LED supply voltage. In this test setup, one of the three employed load LEDs is bypassed by an additional switch connected in parallel. The LED current hence only flows through two series-connected LEDs and the bypass switch. At a certain point of time – indicated as 0 ms in Fig. 5.18b – the bypass switch is opened for several hundred milli seconds. The LED reacts with a fast increase in LED supply voltage $V_{DD,LED}$ so that the LED current may flow through all three LEDs as desired during this period. Once the bypass switch is closed again. The digital control approach regulates the supply voltage back to its lower level within only some tens of milli seconds. This experiment proves the very fast and stable performance of the voltage control loop. In case of an LED (short-circuit) failure, the presented control approach hence protects the linear current regulator by this means from any additional heating or thermal stress, which could have lead to lifetime reductions or other possible malfunctioning.

Thermal heating is in fact a common problem in designing LED-based luminaires since it impacts both electrical efficiency and emitted light quality as outlined in chapters 2.2, 2.3 and 4.5. High currents flowing through the LEDs in conjunction with a (possible) limited heat removal or minor cooling capability of the LED driver housing might even intensify thermal heating. Actually, there are various primary and secondary effects on the LED driver itself and employed LEDs associated with thermal stress, e.g. an increased $R_{DS,on}$ of the power FETs, a deferred LED current level or forward voltage deviations of the used LEDs including peak wavelength shifts and color divergence. With an increasing temperature, LED forward voltage is known to decrease [312], which leads to a higher voltage drop over the linear current regulator. As a result, the static losses consumed in the PWM-switched current regulator would linearly increase by the same amount and even intensify the overall thermal situation in an intelligent luminaire, if not compensated for. Because of its adaptive supply voltage regulation mechanism the proposed LED driver inherently takes care of these thermally induced forward voltage changes in the LED load. To observe the corresponding reaction on thermal heating, Fig. 5.18c pictures the

LED supply voltage $V_{DD,LED}$ recorded for a longer period of time. As can be seen, the dynamic headroom control lowers LED supply voltage $V_{DD,LED}$ once thermal heating occurs after some time. Besides relaxing the overall thermal situation in an intelligent luminaire this feature also yields a significant efficiency improvement due to saving the additional power losses in the linear current regulator. Considering the supply voltage reduction of two V_{step} as indicated in Fig. 5.18c after around 6.5 s, implies power savings of about

$$P_{loss,saved} = 2 \cdot V_{step} \cdot I_{LED} = 2 \cdot 143\,\text{mV} \cdot 700\,\text{mA} \approx 200\,\text{mW}\,. \quad (5.41)$$

In comparison to a classic approach with constant LED supply voltage the measured case already yields an efficiency improvement of approximately

$$\Delta\eta = \frac{P_{loss,saved}}{P_{total}} = \frac{P_{loss,saved}}{I_{LED} \cdot V_{DD,LED}} = \frac{200\,\text{mW}}{700\,\text{mA} \cdot 9.8\,\text{V}} \approx 3\,\%\,. \quad (5.42)$$

This exemplary calculation for the measured case clearly demonstrates a big advantage of the proposed concept in terms of efficiency, especially since applicative situations are conceivable that might even lead to much worse conditions regarding ambient temperature or thermal heating. However, it should be noted that the limited RDAC resolution as mentioned earlier in sections 5.2 and 5.3.3 also impacts precision of the dynamic headroom approach in this case. Therefore, the proposed LED driver only improves overall efficiency to the extend of its RDAC resolution, which might result in one V_{step} for the worst case. In conclusion, the dynamic headroom approach nevertheless improves efficiency significantly in case of thermal heating.

Finally, efficiency measurements of the proposed LED driving concept are conducted to evaluate this second key performance indicator. The efficiency measurements consider power consumption of all involved components depicted in Fig. 5.10 and Fig. 5.11 including current regulator, SMPS and even the μC, all with their entire circuitry around. LED driver efficiency is recorded similarly to the measurements of LED current accuracy as a function of PWM duty cycle but in addition also for different load conditions. While LED current is kept at its nominal level of $I_{LED} = 700\,\text{mA}$, the number of connected LEDs is swept from one to six in order to cover a wide output voltage range. Fig. 5.20 presents the corresponding measurement curves for all recorded LED configurations. Very high efficiencies are achieved over a wide spread dimming range and for different LED assemblies [236], [237]. The proposed concept reaches its peak efficiency of $\eta = 93.9\,\%$ when driving six series-connected LEDs at 92 % PWM duty cycle.

Comparing the performance of the proposed concept to other solutions for LED driving from literature yields Table 5.3 as partially published in [236], [237].

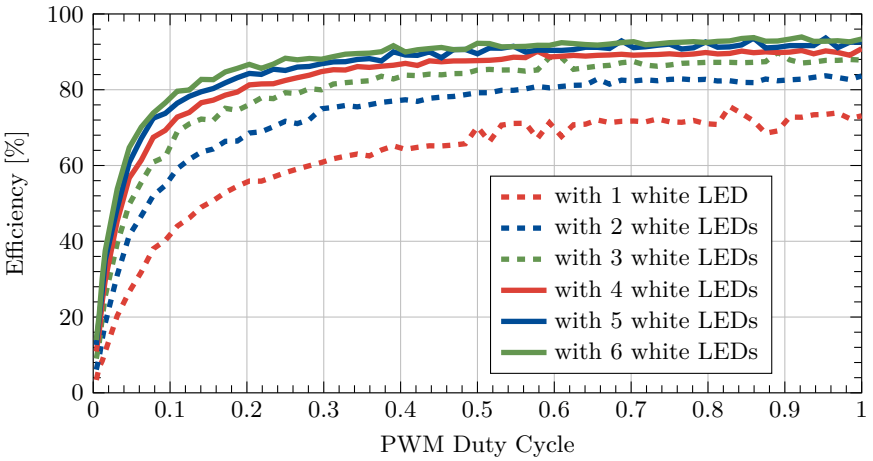


Figure 5.20: Measured efficiencies of the entire control system for several LED voltages over different dimming levels.

While the first two approaches [74] and [152] also employ a dynamic headroom regulation mechanism, the other referenced LED drivers only rely on a single DC-DC converter including the aforementioned drawbacks regarding current ripple and accuracy affecting optical properties like color point stability of attached LEDs. Still, these single stage systems represent a very good benchmark, since such designs typically feature higher efficiencies than a dynamic headroom regulation approach and it is sought to achieve highest possible efficiency for the proposed concept as well. Investigating Table 5.3, it is evident that the LED driver presented in this thesis achieves comparable performance with respect to efficiency and current accuracy. From this point, it also becomes clear that these two performance indicators are traded against each other depending on the final target application. To be fair, it has to be mentioned that the concept of [74] operates at higher alternating current (AC) input voltages. Although similar performance metrics are achieved in these three LED drivers using dynamic headroom regulation, the digital control methodology introduced in this work provides additional benefits, such as a higher design flexibility regarding control speed, precision, stability and output voltage range [236], [237]. The benchmark reference designs depicted in Table 5.3 obviously provide higher efficiencies, as expected, because they are operating as conventional DC-DC converters.

Table 5.3: Performance comparison of different LED drivers.

	Research Work	V_{in} [V]	V_{out} [V]	η_{peak} [%]	I_{LED} [mA] ($\Delta I_{LED,DC}$)
Dynamic Headroom Control	[152]	20 - 30	–	89.27 @24 V	350 ($\leq 0.4\,\%$)
	[74]	90 - 270 (AC)	43	93.5 @110 V	350 (–)
	This Work	24 (5 - 38)	3.5 - 38	93.9	700 ($\leq 1.2\,\%$)
Benchmark Designs	[122]	63.8 - 70.9	33.6	97	1000 ($\leq 10\,\%$)
	[229]	8 - 40	–	94.3	720 ($\leq 2\,\%$)

The performance of [229] is indeed very close and hence comparable to the one of this work while similar voltage and current ratings are achieved, which makes it a good benchmark [237]. Although efficiency is slightly better in the research work of [229], the average DC current accuracy is almost 1 % worse compared to the presented system in this work. Additionally, the LED driver of [229] suffers from a very high AC current ripple, which is unfortunately not quantified in the corresponding publication. However, current accuracy and ripple are important quality measures in an LED lighting system as they determine optical performance and thus perceived light quality. Furthermore, it is expected to increase system efficiency of the proposed concept in a monolithic integration using a high voltage analog-mixed-signal technology due to reaching several synergy effects as outlined in chapter 6. The μC can e.g. be replaced by digital logic and the RDAC control can directly be embedded into the DC-DC converter control.

Fig. 5.21 illustrates the final assembly of eight LED driving stages as proposed by this thesis for the spotlight luminaire presented in appendix section C.1. An additional auxiliary 5 V power supply is installed on the PCB, which supplies the controller ICs of all eight LED channels.

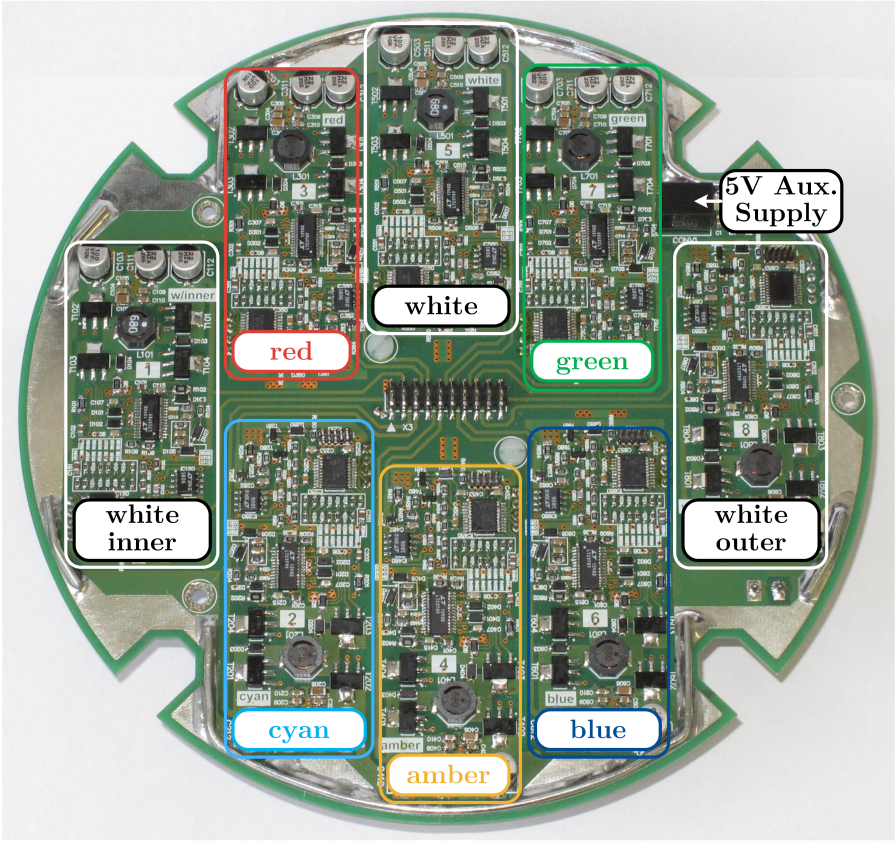


Figure 5.21: PCB assembly with eight instances of the proposed LED driving stage for a powerful spotlight luminaire.

Chapter 6

Monolithic Integration of a Smart LED Driver

The previous chapters have introduced new concepts and ideas for robust DLT communication, accurate color synthesis and efficient LED drivers, which have all been verified in hardware measurements achieving excellent results. While these approaches have demonstrably proven to enhance *"smart LED drivers"* regarding the key challenges in intelligent lighting applications, as highlighted in chapter 1.1, it would in addition be quite beneficial to combine and implement the achieved solutions inss a single ASIC design. A monolithic integration offers the potential to achieve optimal system performance since all components can be perfectly matched to one another. Applying typical techniques and methodologies that are only feasible in an integrated design, it might even be possible to realize higher flexibility and further improve certain performance metrics, particularly energy efficiency. Besides, an ASIC solution features several other advantages, such as being very cost effective, while providing minimal footprint area on a PCB, which enables small form factors of LED

based luminaires for a cheap price. It would thereby be feasible to built high quality lighting products for a broad mass market and consequently boost HCL applications significantly. In summary, monolithic integration provides a great benefit in terms of yielding an optimized system solution for *"smart LED drivers"* creating high quality color mixing with efficient LED driving stages and an intelligent communication interface from one source as a single die.

6.1 Optimized System-on-a-Chip Concept for Intelligent and Efficient LED Driving

In order to achieve optimized performance for a *"smart LED driver"*, a monolithically integrated ASIC solution should combine a DLT communication interface, multiple efficiently dimmable LED driving stages and a color control algorithm. The number of employed LED channels obviously depends on the final application with respect to targeted color rendering performance. While simple tunable white luminaires already get by with two distinct LED channels, more sophisticated approaches require at least four different LED colors and hence the same amount of driving stages. Certain semiconductor technologies also provide digital signal processors (DSPs) in their PDK, which enables an easy implementation of the color control on an ASIC. In this case, any changes in the color control algorithm would require a new firmware update, if no RAM is accessible. This might entail new chip fabrication or at least an updated metal mask in a final production, if modifications to the color control algorithm shall be applied. Of course, the color control algorithm can also be run on an external μC, if a suited interface like UART or I^2C is realized on chip. This measure relaxes complexity and hardware effort for the ASIC implementation, while giving more flexibility to later adoptions in the color control.

To balance hardware demand and innovative features, the engineered test chip, called "High Quality Lighting Efficient Driving" HQLED ASIC, realizes a DLT FW-RX and four individually controllable LED driving stages based on the digital dynamic headroom control concept presented in chapter 5. The color control algorithm on the contrary is sourced out for complexity reasons and is thus implemented externally on a μC. The integrated DLT FW-RX contains two concept designs for its detection filter, which are first the analog bandpass and second the digital FIR approach, both evaluated in chapter 3.2. In compliance with the monolithically integrable system concept of a *"smart LED driver"* derived in section 2.4, Fig. 6.1 illustrates a conceptual block diagram of the implemented ASIC solution. Apart from the color control algorithm, also some other components and functional units, which are relevant for a final

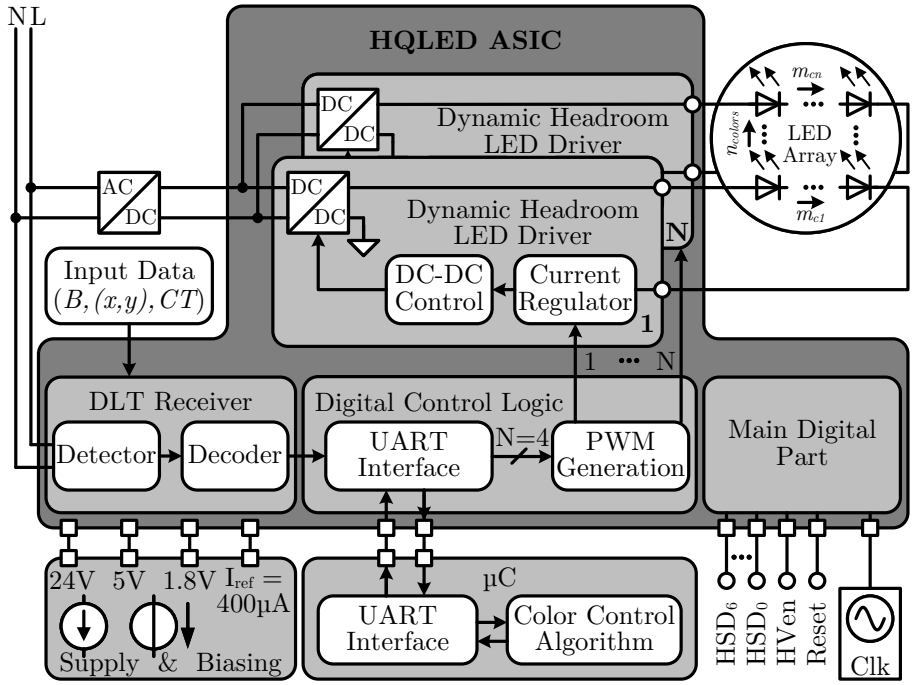


Figure 6.1: System concept of the developed HQLED test chip.

product implementation, have not been included on the HQLED test chip. In particular, this involves circuit blocks coping with housekeeping functions, like a high frequency clock generation by an internal oscillator, bandgap references for accurate, temperature stabilized reference currents and voltages as well as a PMU with internal LDOs providing the power supply on different voltage domains. These components represent conventional circuits that are of no relevance from a scientific point of view in this context. The respective currents and voltages as well as the main clock for the digital part are thus provided by external references and supplies over distinct pins as shown in Fig. 6.1. All in all, the engineered HQLED test chip handles three power domains, which are $DVDD = 1.8\,\mathrm{V}$ for the digital part and low voltage circuitry, a calm analog supply voltage $AVDD = 5\,\mathrm{V}$ as well as a high power domain $HVDD = 24\,\mathrm{V}$. The digital domain $DVDD$ is split up into a calm supply domain used for references in ADCs, sensing circuits, etc. and a noisy domain coping with the main digital

part and any hard switching circuitry. Besides the supply voltage network, a digital clock with a frequency of $f_{clk} = 200\,\text{MHz}$ and a reference current of $I_{ref} = 400\,\mu\text{A}$ are provided from external sources via distinct pads. For power consumption reasons the relatively high but accurate reference current is directly scaled down to $I_{ref,int} = 100\,\mu\text{A}$. It is internally distributed with a biasing network to the DLT circuitry and the four LED driver channels.

A serial UART interface according to [271] is implemented to ensure communication between the external μC and the HQLED test chip. This gateway is needed to transfer relevant data, such as brightness values, color coordinates and CTs, from the DLT FW-RX of the ASIC to the computing μC running the color control algorithm and subsequently to send calculated PWM duty cycles D_i back to the LED driving stages in the ASIC. Additionally, the UART interface allows to set certain configuration registers of the chip, e.g. to adjust the analog dimming level of the LED current or to tune a gain and offset correction in the current sensing approach, which is explained later in section 6.4. Beyond that, a high-speed debug (HSD) interface has been installed for test purposes, which allows to directly control the integrated power switches and readout measured ADC values at high speed. It is thereby possible to bypass the digital control of the LED driver and run a (modified) control on an external FPGA. As can be seen from Fig. 6.1, the HQLED chip provides seven pins for this bidirectional HSD interface. While one pin is needed for a synchronizing 100 MHz clock, all other six pins can be used for data transfer. Beyond the mentioned interfaces, the HQLED chip provides a distinct reset pin and another one enabling HV control circuitry.

The major aim of the proposed monolithic integration is to further boost the performance of the developed concepts and topologies, particularly that of the LED driving stage. Special emphasis is consequently put on achieving a higher energy efficiency of more than 95 % while maintaining precise current regulation with $I_{LED} \leq 3\,\%$ and improving the dimming contrast ratio to $DIM \leq 0.4\,\%$. In order to achieve this, certain measures are taken in the switching pre-regulator, the digital dynamic headroom control as well as in the low-side current regulator of the LED driving stage. Briefly summarized these changes can be condensed to the following aspects, which are

- using a buck converter topology with reduced output voltage range,
- increasing the RDAC resolution to 9 bit,
- matching the regulation mechanisms of the control loops to one another,
- dispensing with the sense resistor in the linear current regulator,
- employing an all-digital current control and
- increasing switching speed of the PWM and the power MOSFET(s).

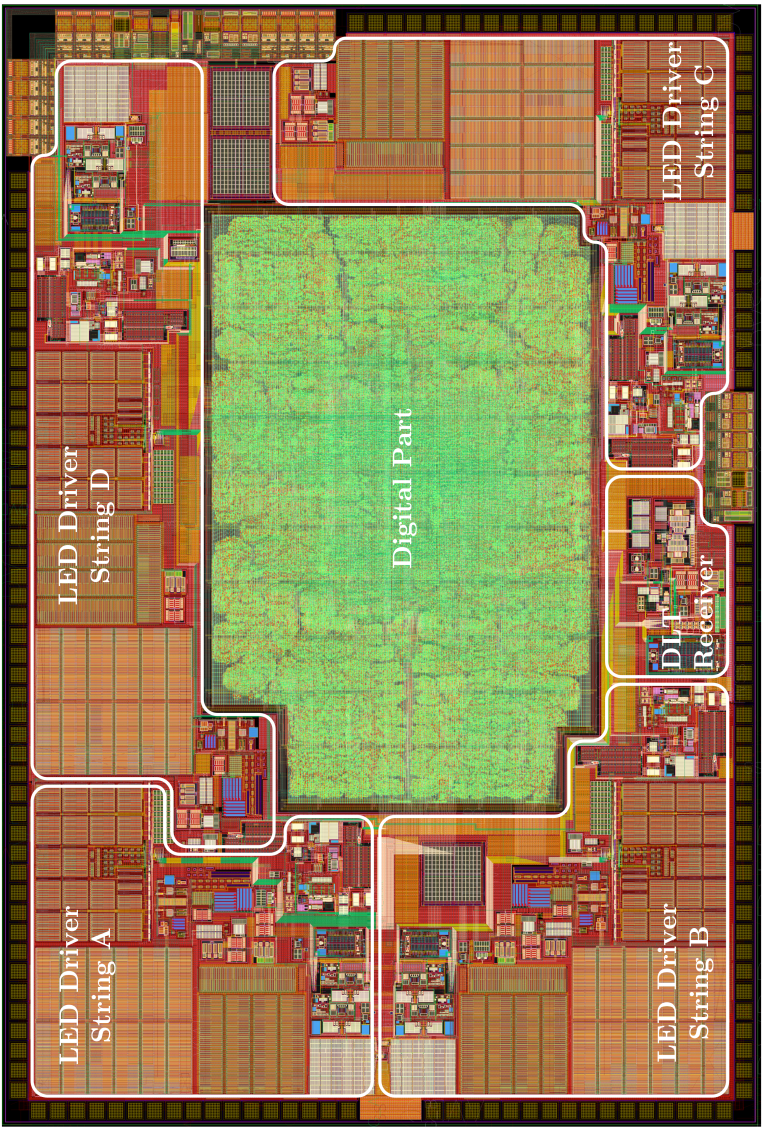


Figure 6.2: Layout of the HQLED test chip, a 4-channel *"smart LED driver"* with external color control.

A monolithic integration of the proposed LED driving concept thus provides a broad variety of additional improvements and optimization opportunities in terms of achievable performance. Beyond that, this chapter highlights several design aspects and modifications in comparison to the discrete prototype implementations presented in chapters 3.2 and 5, respectively. The subsequent sections hence give a short overview on particular specialties in the HQLED ASIC implementation. For that matter, section 6.2 covers all differences in the DLT FW-RX circuits. While these changes are rather small, the main emphasis is set on the above stated enhancements in the LED driving stage. Section 6.3 thereby focuses on improvements regarding the switching pre-regulator and its associated control loops, which covers the first three listed aspects. Proposing the innovative *"Current Replica"* (CR) sense and control concept, section 6.4 copes with the latter three mentioned enhancements in the current regulator part. Finally, section 6.5 evaluates achievable system efficiency and summarizes the gained insights. As a forecast, Fig. 6.2 illustrates the final layout of the realized HQLED test chip containing all circuit components described above.

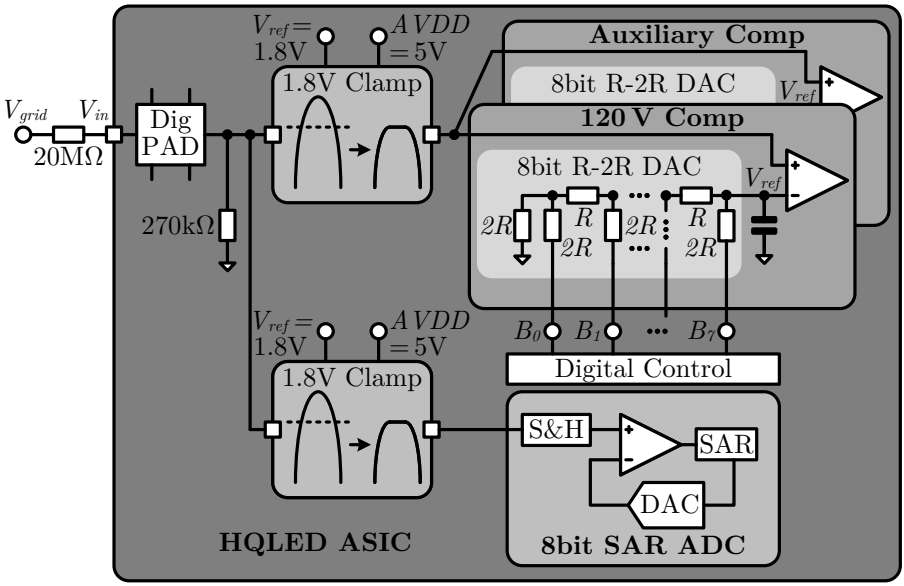
6.2 Integrated Receivers for DLT Control Gears

The investigation on different DLT FW-RX topologies conducted in chapter 3.2.3 yielded two comparable detector concepts that are suited for a monolithic integration. These concepts are an active analog bandpass filter and a digital FIR filter. Both architectures rely on edge detection of the transmitted DLT data signal and feature robust performance with respect to TER, low power consumption and reasonable circuit complexity. The HQLED test chip consequently implements both solutions, which could thereby be compared to one another in an experimental performance evaluation. Beyond the two detector concepts, the ASIC implementation contains a fully functional DLT FW-RX including a ZCD, the V_{SW} comparator and HC as well as LC bypass paths for the required auxiliary functions. The digital evaluation routines for frame and telegram decoding have been hard coded in the digital part of the HQLED chip. By means of the embedded UART interface, received and decoded telegrams are subsequently committed to the external μC for further processing in the color mixing algorithm. Since the hardware realizations with COTS components presented in chapter 3.2 were meant to serve as functional concept verifications for the ASIC design, the DLT FW-RX integrated on the test chip is more or less identical to its discrete counterpart. Some differences regarding effective implementation are however briefly highlighted and summarized in the following paragraphs.

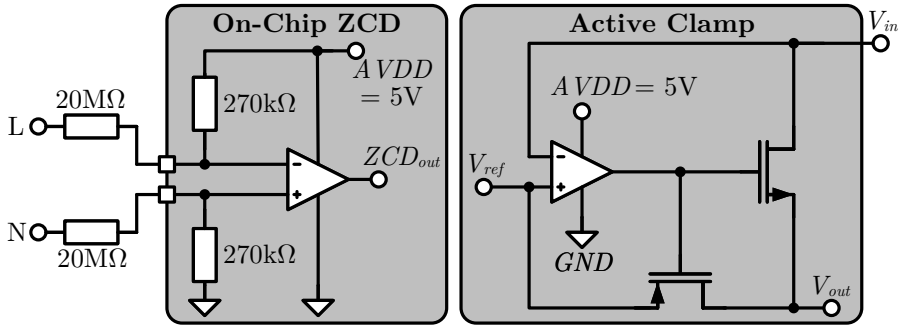
Auxiliary Circuits

The auxiliary circuits, particularly the ZCD and the 120 V comparator, have been realized in the same manner as with discrete components. To optimize both comparators with respect to power consumption, a basic structure consisting of a differential input stage, active load and buffering output inverters has been applied. Still, the two comparators are dimensioned and designed slightly different from one another. Aiming to save power consumption even further, the upstream connected resistive dividers, which scale the mains fed input voltage down to a measurable dimension, have been increased compared to the discrete solutions presented in chapter 3.2. The internal pull-down resistors have been set to 270 kΩ, which demands an external resistance of 20 MΩ to scale the grid voltage $V_{grid}(t)$ down into the analog *AVDD* domain of 5 V. Consequently, the crosscurrent flowing through these resistive dividers is lowered into the one digit µA range compared to the realization with COTS components. If this current flow should however be too low in the end for ensuring a reliable zero crossing detection or accurate measurement of the $V_{SW} = 120$ V cross-over point, the resistive divider can be adopted and resized by external circuitry. Connecting a discrete pull-down resistor in parallel to the internal one actually lowers the overall resistance and hence increases the crosscurrent accordingly. Fig. 6.3 depicts the realized auxiliary circuitry inside of the HQLED test chip, with a special emphasis on ZCD and 120 V comparators.

Additional clamping circuits protect any downstream connected circuit blocks from possible over-voltage conditions. Fig. 6.3 also highlights an 8 bit SAR-ADC, which is required for the digital DLT detector as an converting input stage. The SAR-ADC shares the same pad connection as the 120 V comparator. Beyond that, a second comparator has been installed in parallel, which also features a digitally programmable reference voltage. This auxiliary comparator is built as a test feature to check for an alternative way of realizing the ZCD function. Measuring the cross-over point of a low, one-digit voltage, e.g. 3 V, on the rectified mains voltage, this comparator will toggle twice when a zero crossing event occurs because the low voltage level is passed on the falling as well as on the rising edge of mains. The actual zero crossing is then expected to sit directly in the middle between the two detected time stamps. Thus, the digital part can subsequently interpolate between these two successive crossings and calculate the effective zero crossing point by averaging. To some extent, this method would obviously suffer from a time dependent uncertainty, particularly because of the internal processing time of the digital core and the quantization error associated with the digital clock frequency. Also, propagation delay for rising and falling edges as well as the offset voltage of the ZCD comparator may affect the timing variance leading to a miscalculated zero crossing point.



(a) V_{SW} comparators and 8 bit SAR-ADC.



(b) Integrated ZCD circuit.

(c) Active 1.8 V clamping circuit.

Figure 6.3: Auxiliary cirucits of the integrated DLT FW-RX.

The comparator's influences are however expected to be rather negligible with respect to the resulting timing error, if the design is properly matched. In the end, an experimental validation must be conducted to investigate, whether the

accuracy of this alternative ZCD approach is sufficient in realistic application scenarios. All comparators are equipped with programmable reference voltages, which is used for test purposes as well as for trimming functionality.

DLT Detectors

The DLT detector circuits have been realized identically to their discrete counterparts. Hence, the analog filter uses the same structure and equal component sizes regarding the implementation indicated in Fig. 3.13. Again low power opamps have been used realizing the analog filter and Schmitt-Trigger. The Schmitt-Trigger could of course also be implemented with a simplistic either four, six or eight transistor approach in the ASIC as described in [107], [399]. Except for C_1, which is rated for withstanding mains voltage, the entire analog detector referring to Fig. 3.13 is integrated on the ASIC. Optionally, resistor R_1 and protection diode D_1 can also be placed externally on the PCB. By means of selecting different values for C_1 and R_1, it is also possible to tune the high pass cut-off frequency of the analog bandpass, hence shifting its center frequency and modifying the corresponding bandwidth. Additionally, internal resistor R_2 and capacitor C_2 are programmable in steps of a 9.3 kΩ unit resistor and a 12.5 pF capacitance, respectively, to fine-tune center frequency and bandwidth by changing the low pass cut-off frequency.

The digital filter according to Fig. 3.16 has been hard coded in the ASIC as well as the frame and telegram detection routines explained in section 3.2.2.4 and the published paper [235]. Fig. 3.20 and 3.21 illustrate flowcharts of frame and telegram evaluation, respectively, whereas Fig. A.3 in appendix section A.2 depicts the frame decoder for the digital filter. Referring to Fig. 3.16, the simple, high ohmic resistive divider is only partially integrated on the ASIC due to the applied high mains voltage of $V_{grid,RMS} = 230\,\text{V}$. While the HV domain resistances $R_1 + R_2 = 20\,\text{M}\Omega$ thus have to be attached externally, the pull-down resistor $R_3 = 270\,\text{k}\Omega$ sits inside of the ASIC. The dimensioning accounts for over-voltages of the grid voltage of up to 10 %, which reflects official tolerances. The analog-to-digital conversion is subsequently performed by the 8 bit SAR-ADC depicted in Fig. 6.3 with a maximum input capacitance of 8 pF. The SAR-ADC has been implemented in a low power variant according to the proposed concept and structure of Aghaie *et al.* [4]. Although the very large resistive divider with $R_1 + R_2 = 20\,\text{M}\Omega$ and $R_3 = 270\,\text{k}\Omega$ is used, the input capacitance is not flattening the modulated DLT FW signal too much ensuring reliable detection. Several simulations have shown that capacitance values up to 10 pF are easily tolerable. While input capacitances of up to 25 pF might even be possible, a 50 pF capacitor already smoothens the modulated DLT

voltage waveform so much that a negative impact on measured TER is expected. Therefore, the PCB design has to be outlined thoroughly. In case of measuring an increased TER, it is also possible to lower the resistive divider by external circuitry. As already described above for the ZCD, this measure is realized by connecting a lower ohmic pull-down resistance in parallel to the internal one and choosing a suited HV resistance accordingly. Of course, the increased power consumption due to the higher crosscurrent has to be considered.

Because mains voltage is only brought to the 5 V domain by the large resistive divider, an additional clamping circuit, which is also installed inside of the IC, is required for any circuitry operating at the digital supply of $DVDD = 1.8\,\mathrm{V}$ and sharing the same pin connection as the 120 V comparator. This $DVDD$ clamping as circuit pictured in Fig. 6.3 does not only serve as a simple protection measure for any downstream connected circuitry but also fulfills an important task with respect to the digital DLT detector. Due to clamping the downscaled mains voltage, the internal 8 bit ADC of the HQLED ASIC maps its 1.8 V full scale range only to approximately 135 V instead of resolving the entire peak voltage of mains. Since the voltage level during DLT data period never exceeds 130 V by definition, the clamping does not even affect the DLT FW-RX. Consequently, the effective resolution of the employed SAR-ADC is increased significantly, which is quite beneficial with respect to sensitivity and robustness of DLT FW modulation. Furthermore, it might be possible to reduce hardware effort a little bit more in a final target implementation since an effective number of bits (ENOB) of 5 bit to 6 bit might hence already be enough for robust and reliable reception of DLT FW modulated messages.

HC and LC Bypass

Due to the high mains potential of several hundreds of volts, the actual bypass transistors conducting the respective low- and high-currents cannot be integrated in the HQLED chip for the chosen technology. Thus, they have to be placed externally on the PCB but still need to be controlled via the ASIC. In order to save pin count and hardware efforts, LC and HC bypasses are implemented with a single transistor device and controlled by an integrated driver circuit accordingly. Fig. 6.4 illustrates the designed driver and current regulation structure. Changing either the reference voltage of the regulating opamp or modifying the employed internal sense resistor allows for setting different current amplitudes and thereby distinguishing between LC and HC phases. To program the reference voltage a simple R-2R resistor latter with a full scale deflection of 1.8 V and an 8 bit control structure is installed. The reference voltage can thereby be set in very precise steps of approximately 7 mV.

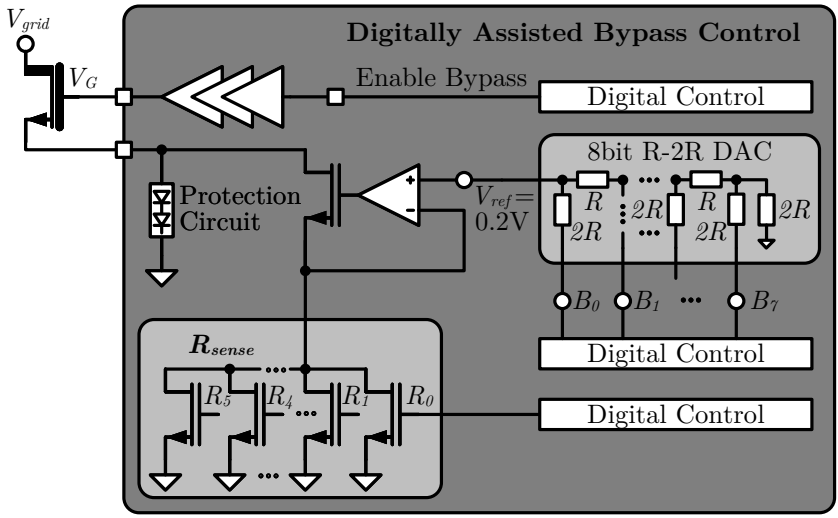


Figure 6.4: Implementation of the programmable DLT bypass driver.

Since a very low ohmic connection for the HC bypass is required, the effective sensing resistance is realized by on-resistances of current carrying transistors. If all transistors are enabled, a minimum resistance of about 0.3 Ω is achieved. The layout is however very critical for this part as parasitic resistances may diminish the effective current flow. In order to reach a 400 mA current carrying capability of the bypass, a minimum resistance of only 0.5 Ω is demanded referring to a typical reference voltage of 200 mV. Furthermore, it is desired to keep the sensing resistance as low as possible because the associated losses during the HC phase will heat up the chip and hence limit the thermal budget. Considering metal and wiring resistances, extracted simulation showed that about 0.5 Ω are finally realized in the lowest R_{sense} case, which enables the targeted HC flow of 400 mA. The lowest resistance is provided by transistor $R_0 \approx 0.5\,\Omega$. R_1 and R_2 are dimensioned to approximately 2 Ω each, whereas R_3 and R_4 yield 4 Ω each. A maximum resistor value of $R_5 = 8\,\Omega$ can be set by the digital control. In normal operation – when switching between LC and HC phase and vice versa – the sense resistance is stepwise reduced or increased by switching more and more parallel connected transistor stages on or off, respectively. Hence, a smooth transition between both intervals is assured. Additionally, some kind of protection circuit is required at the source pin of the external power field-effect transistor (FET) in order to protect the ASIC, if mains voltage is applied but

the chip itself is not powered yet. In this case, leakage currents could increase the source potential of the FET to a higher value than tolerable by internal devices. Suitable measures are hence a high ohmic bleeding resistance that may conduct several µA at a potential of 2 V to 3 V. Another possibility is to insert protection diodes, which act as a clamping circuit and dissipate the current in case of too high applied potentials. The advantage of the latter opportunity is that this circuit also protects against capacitive coupling induced overcharging of the rectified mains voltage. The entire structure is controlled by the digital part of the ASIC, which hence requires a precise synchronization to mains by means of the aforementioned ZCD circuit. Since the current amplitudes can be chosen and set freely by the digital control, it would also be possible to realize a DLT REV-TX for a subset of distinct current amplitudes by this means. So far, this feature of a fully functional REV-TX is however not implemented in the HQLED test chip. It would still be possible to set different resistor values and reference voltages over a UART command and test, if the modulated amplitude is sufficient for DLT REV communication.

6.3 Digital Dynamic Headroom Control for Integrated LED Drivers

Each of the four LED driving stages embedded in the HQLED ASIC is designed in the same manner. Based on the discrete prototype implementation, which has been demonstrated in chapter 5 and published in [236], [237], the integrated LED driver realizes the aforementioned system level enhancements. Focusing on the switching pre-regulator and the associated control loops, this section discusses the design specialties of the monolithic solution and highlights relevant differences in contrast to the discrete prototype implementation. For that matter, the subsequent paragraphs introduce the taken measures for the first three system level improvements listed in the end of section 6.1 in more detail. In addition, Fig. 6.5 illustrates the implemented block level concept for a single LED channel of the integrated dynamic headroom based LED driver.

Switching Pre-Regulator Converter Type & Output Voltage Range

At first, the topology of the switching pre-regulator is changed from a buck-boost type to a voltage mode, hysteretic controlled buck converter. The buck converter topology is generally known as the most efficient DC-DC converter type [313], which has been confirmed by several experimental results of the discrete prototype implementation under various application conditions. Fig. 5.12 in chapter 5 allusively depicts this effect as an example by showing the measured

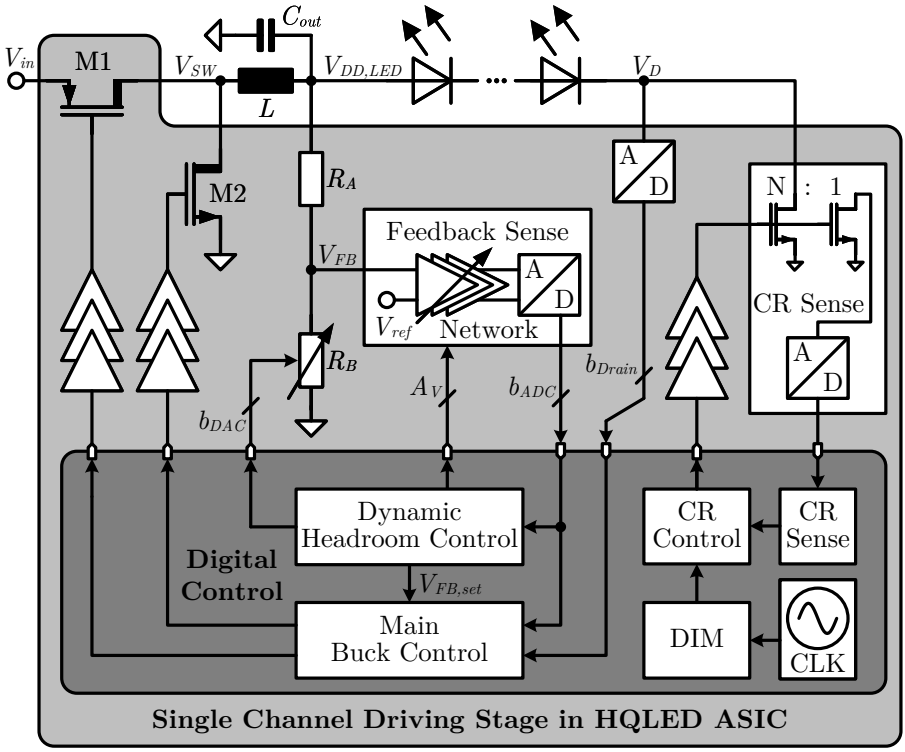


Figure 6.5: Conceptual block diagram of the integrated LED driving stage with dynamic headroom regulation for one channel.

efficiency versus input voltage at a constant current load. The used converter IC achieved highest peak efficiency when operating in buck-mode, whereas buck-boost and boost operation both yielded slightly lower peak efficiencies. The change from a buck-boost type to a buck converter moreover reduces the number of power switches and hence the required hardware effort. However, this modification comes at the cost of a limited flexibility, such as a smaller output voltage range that is bounded to the maximum applicable input voltage. Considering the final target application to be well-known, the power converter of an ASIC implementation can be optimized for a distinct set of input/output voltage ranges for further efficiency improvements. The current implementation also integrates the main power switches and effectively handles input voltages

of up to 23 V accounting for a small safety margin [313]. 24 V as specified by the *HVDD* voltage domain may generally be applied without damaging the chip, however this might become critical during several operating conditions. Assuming a maximum duty cycle of 80 %, output voltages of up to 18.4 V can eventually be realized. While lowering the output voltage range, the switching pre-regulator must maintain a small output voltage ripple of maximum $\Delta V_{out} \leq \pm 20\,\text{mV}$ in order to keep the voltage overhead over the linear current regulator with reasonable limits. Since the integrated buck converter is custom designed, it is moreover possible to optimize its ohmic and switching losses with respect to the targeted application scenario. By this means, the efficiency of the LED driver is boosted even further, which has therefore been conducted by Schulte Bocholt in an outstanding Master's thesis [313].

Increased RDAC Resolution

Beyond modifying the switching pre-regulator, it is aspired to minimize the additional voltage headroom dropping over the current regulator. Recalling the digital dynamic headroom regulation concept presented in chapter 5, the resolution of the RDAC is enlarged by an additional bit to a 9 bit full scale range. In conjunction with the reduced output voltage range from 38 V to approximately 18.4 V the augmented RDAC resolution diminishes the minimum step width from about 143 mV to $V_{step} \approx 42\,\text{mV}$. This value is obtained by applying equations 5.8 and 5.10 for the dimensioning given in table 6.4 from [313] as described later in section 6.3.2. Thereby, it is possible to control the drain potential more accurately and further reduce the overhead over the current regulator. In particular, this measure decreases the additional voltage window $\Delta V_{D,window}$ on top of the current regulator that is caused by the quantization error. Of course, it would be possible to increase the RDAC resolution even further, e.g. to about 12 bit as suggested in chapter 5.2 and [237]. Due to the increased circuit complexity and hardware effort, this measure would however be more reasonable for implementations providing a higher maximum output voltage, such as the solutions presented in chapter 5 and in [237]. Accounting for the small ripple on the LED supply voltage of $\Delta V_{DD,LED} \leq \pm 20\,\text{mV}$, the realized minimum step width is already close to the achievable optimum, which would hence not justify any additional hardware effort.

Enhanced Matching of the Control Loops

In an integrated design it is much easier to coordinate, fine-tune and match the digital control mechanisms to one another since all relevant (control) signals,

such as the used PWM duty cycle or the gate driving signals of the power stage, are well-known and internally available for the individual control loops. Fast load transients, which happen regularly due to the applied PWM dimming when switching the current regulator circuit on and off, can thus be predicted reliably and precisely. Balancing the different digital control loops hence allows to minimize large voltage dips at turn-on as described in chapter 5.4, which will consequently increase achievable peak efficiency. Also, overcharging at the end of a PWM dimming phase is kept within reasonable limits since the turn-off point can be easily approximated. Nevertheless, a small overcharging and slight undershoot will finally remain, but vastly reduced [313] compared to the implementation with discrete COTS components.

6.3.1 Integrated Voltage Control Loops for Digitally Assisted Dynamic Headroom Regulation

While the adoptions of converter type, output voltage range and RDAC resolution are rather ordinary measures, the main difference in the integrated approach of a dynamic headroom regulation is the way the various control loops work and how they are adjusted to one another. In the following, special emphasis shall therefore be set on the inner voltage control loop of the buck converter as well as on the dynamic headroom regulation minimizing the voltage drop over the current regulator. The control loop for LED current regulation is subsequently proposed and discussed in section 6.4.

Inner Control Loop of the Buck Converter

The integrated buck converter operates in voltage-mode control and employs a hysteretic regulation mechanism for its main control loop. Sensing the LED supply voltage $V_{DD,LED}$, the inner control loop switches power MOSFETs M1 and M2 according to the predefined (and adjustable) hysteresis. An additional timing control ensures non-overlapping switching events of M1 and M2 to prevent excessive current flows through both devices that could lead to shoot-trough and hence destruction of the entire circuitry. This protection feature leads to a short time period, in which neither of the two power transistors are conducting. The resulting dead-time t_{dead} obviously affects efficiency, which is rather small, if designed properly. The control mechanism also provides a maximum on-time limitation as an additional safety feature to avoid a permanent increase of the inductor current and hence thermal stress of the power MOSFETs. To prevent unnecessary often switching events, the converter control enables both power devices at least for a minimum on-time $t_{on,min}$. Fig. 6.6 illustrates a

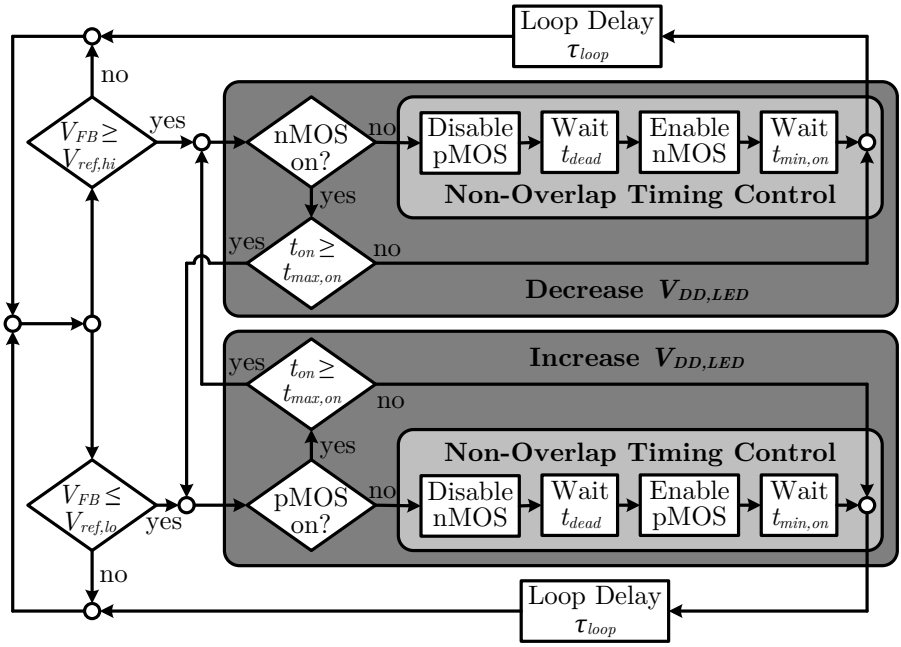


Figure 6.6: Flowchart of a hysteretic buck converter control providing additional protection features.

conceptual flowchart of the hysteretic converter control with minimum and maximum on-time limitations as well as a non-overlap switching protection. For more detailed information please refer to [313].

Aiming to minimize the output voltage ripple $\Delta V_{DD,LED}$, the converter control needs to operate at a high switching frequency f_{sw}. It is therefore essential to keep the (internal) loop delay as small as possible. The loop delay τ_{loop} is composed of the conversion time of the feedback sense network t_{conv}, the digital processing time t_{proc} needed for evaluation, the dead-time t_{dead} of the non-overlapping switching protection, the gate driver delay t_{drv} and the group delay t_{LC} of the LC low pass filter at the output to

$$\tau_{loop} = t_{conv} + t_{proc} + t_{dead} + t_{drv} + t_{LC}\,. \tag{6.1}$$

Since most of these timings are fixed due to system dimensioning and realized design, only t_{conv} remains as a tunable parameter in dependence of the architecture for the feedback sense network. In terms of implementation effort

and speed, a fast comparator connected to the feedback pin would thus be the perfect choice for the feedback sense network as it provides a minimum conversion time t_{conv}. The aforementioned hysteresis could thereby be realized in different ways, e.g. directly within the window comparator itself by means of a suitable Schmitt-Trigger circuit or by using two distinct instances of a fast comparator with different adjustable threshold voltages. The latter implementation possibility is indeed the preferred choice as it allows for precise adjusting of the hysteresis window by selecting the two threshold voltages $V_{ref,hi}$ and $V_{ref,lo}$ via digital settings. In any case, the offset voltage of the used comparator(s) as well as deviations in the reference voltage(s) are crucial for the performance of the dynamic headroom regulation as these variations would cause a systematic offset error at the drain potential and hence compromise the second major control loop. How critically this effect impacts overall system performance becomes clear when calculating the possible forfeit in terms of effective RDAC resolution as shown in the following. The reference compare voltage has been selected in the center of the *DVDD* supply to $V_{ref} = 0.9\,\mathrm{V}$. The hysteresis compare voltages $V_{ref,hi}$ and $V_{ref,lo}$ are set symmetrically around V_{ref}, with

$$V_{ref,hi} = V_{ref} + \Delta V_{set} \qquad \text{and} \qquad V_{ref,lo} = V_{ref} - \Delta V_{set}\,. \tag{6.2}$$

Considering the 9 bit resolution of the RDAC, one LSB changes the feedback voltage by approximately $\Delta V_{FB} \approx 1.76\,\mathrm{mV}$ under steady state conditions. Since the comparator's offset voltage and reference voltage variations may easily add up to voltage levels in the range between 10 mV to 20 mV, these deviations would effectively cost about 3 bit to 4 bit in terms of RDAC resolution. If not accounted for, this part of the RDAC resolution would unwillingly be spend on compensating the offset error and reference deviations instead of regulating the drain potential. This behavior is unacceptable because the headroom of the drain potential could not be controlled sufficiently in that case leading to increased power losses. Trimming the respective reference voltage(s) in accurate steps of about 1 mV would compensate for this offset induced error and represents a suitable solution to the described issue. Though, the compensation by reference trimming requires calibration and test time during production, which leads to increased costs for the manufacturer.

For scientific purposes the presented HQLED ASIC employs a tiny 4 bit SAR-ADC with an upstream connected programmable gain stage instead of an analog window comparator to realize the feedback sense network of the integrated buck converter. The ADC operates at a floating input range and effectively only resolves the present output voltage ripple of the converter, whereas the gain stage is used to adjust the input range accordingly. Fig. 6.7 illustrates a functional block diagram of this approach. At first glance, this solution appears

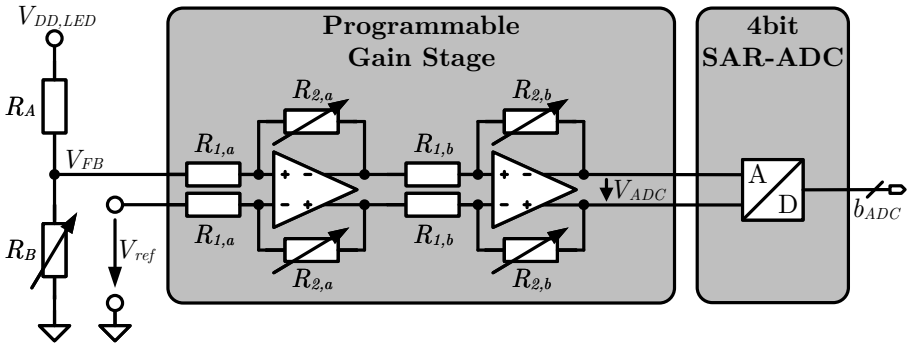


Figure 6.7: Realized concept of the floating input range ADC.

disadvantageous as the problem regarding offset and reference voltage deviations remains, plus the ADC conversion time increases the loop delay noticeably. On the other hand, the additional bits of the ADC can be used to enhance the effective RDAC resolution of the dynamic headroom control. Thereby, it might e.g. be possible to avoid the necessity for trimming offset and reference voltages, which could be beneficial for mass market productions. In this case, extra costs for the bigger chip area as well as the additional power dissipation have to be evaluated against the required test and calibration time. If a trimming is applied to the reference input of the gain stage, the additional ADC bits could even be utilized to extend the (9 bit) RDAC resolution to the aspired range of 12 bit to 13 bit. This would be particularly advantageous for implementations with higher LED supply voltages since the hardware and matching requirements to both, RDAC and SAR-ADC, are kept within reasonable limits. Moreover, it might be possible to conclude to the real voltage drop over attached LEDs from the state of the adjusted gain stage and the measured ADC values. Although this feature requires a more sophisticated computational approach, it could e.g. enable a color shift compensation method as discussed in chapter 4. Due to the higher loop delay it must be ensured under any circumstance that the floating input range ADC approach does not slow down the switching frequency f_{sw} too much because that would result in an increased output voltage ripple, which in turn requires a higher voltage headroom over the current regulator. This thesis thereby seeks to find out whether the conversion time is even fast enough for the main buck converter control, hence additionally dispensing the window comparator. Running at a 50 MHz clock, the 4 bit ADC achieves conversion times of around $t_{conv} \approx 160$ ns, which represents a reasonable increment of the

overall loop delay in contrast to the window comparator solution. This approach thereby aims to balance additional resolution with efficiency losses due to an increased loop delay. From a scientific point of view the floating input range ADC is an interesting solution, as this approach tackles multiple purposes. Due to offering these various interesting examination possibilities, it has finally been selected for implementation in the HQLED ASIC. The floating input range ADC is described in more detail in the subsequent paragraph. In general, it is also conceivable to employ a combination of a fast window comparator for the main buck control and the floating range ADC providing the aforementioned additional functionality.

In contrast to the analog window comparator, which realizes the hysteresis by its two independently selectable reference voltages, the floating range ADC approach already comes with an inherent non-adjustable hysteresis induced by the higher loop delay due to the finite conversion time t_{conv} of the 4 bit SAR-ADC. Hence, no additional hysteresis in the digital domain would be necessary and the control approach could directly regulate to a single reference compare level $V_{FB,set}$ instead of using the two thresholds $V_{ref,hi}$ and $V_{ref,lo}$. In this case, the digital control approach presented in Fig. 6.6 simplifies a little bit as the two queries of the feedback voltage V_{FB} regarding the upper and lower thresholds are merged to only one request. If V_{FB} is greater than the compare level $V_{FB,set}$, $V_{DD,LED}$ needs to be decreased. Otherwise, the LED supply voltage is increased and the flowchart follows the corresponding paths. Since the entire control happens in the digital part, it compares obviously the digital representations of the analog voltages to one another, which are called *VFB* and *VFB_SET*, respectively. It should be noted that the digital feedback value *VFB* is in the following used synonymously to the measured ADC output value b_{ADC}. The simplistic basic control approach conforming Fig. 6.6 but using only the single request regarding *VFB* as described above is used during the start-up of the LED driving stage, which is outlined later in this section. If this conventional control method is however employed during normal operation, it would lead to comparatively high output voltage ripples due to a lower switching frequency and thus reducing overall efficiency as explained earlier. Because the voltage ripple might actually increase more than one LSB of the floating input range ADC during a conversion cycle, an advanced control mechanism as proposed by Schulte Bocholt [313] is applied instead. It aims to switch somewhat earlier in order to compensate for some part of the increased loop delay. The developed control approach therefore introduces a "negative counteracting hysteresis" employing two digital levels of $VFB_SET \pm 1$. This hysteresis thus equates to a symmetrical distance of $\pm$ one LSB voltage of the floating input range ADC from the defined set value $V_{FB,set}$. Thereby,

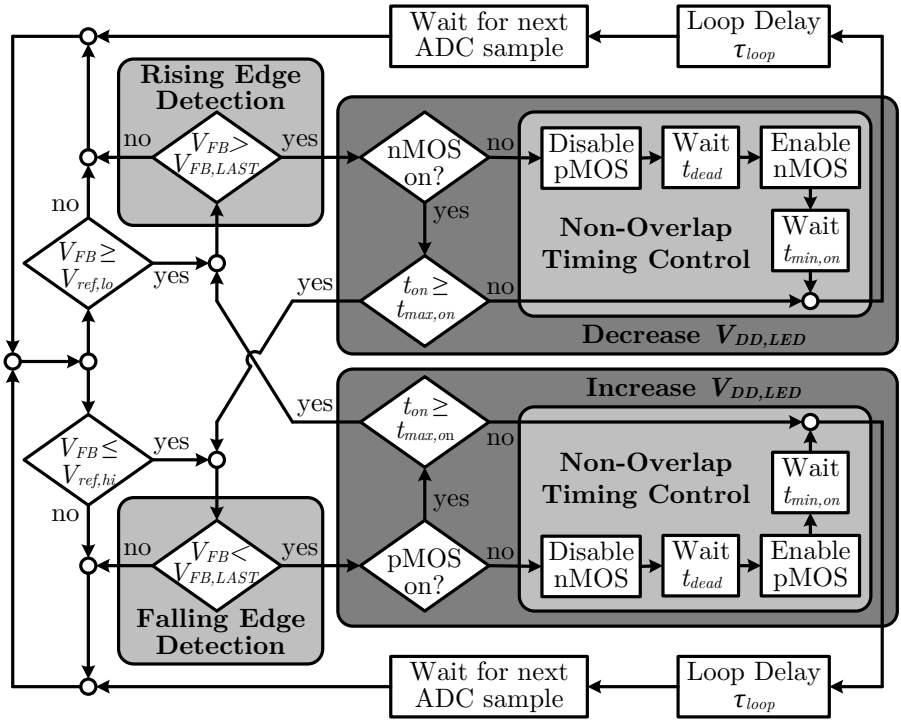


Figure 6.8: Flowchart of the improved buck converter control with a negative counteracting hysteresis and additional protection features.

the upper and lower thresholds of the advanced control are thus defined as $V_{ref,hi} = V_{FB,set} + \Delta V_{FB,LSB}$ and $V_{ref,lo} = V_{FB,set} - \Delta V_{FB,LSB}$, respectively. Fig. 6.8 shows the corresponding flowchart as implemented. Inspecting this advanced control method, two major differences strike in comparison to the basic control algorithm shown in Fig. 6.6. First, the improved control swaps the comparing threshold levels $V_{ref,hi}$ and $V_{ref,lo}$ in their respective queries to introduce the negative counteracting hysteresis. Second, the sign of the output voltage slope is detected and included in the decision paths of the flowchart. The sign of the output voltage is measured by storing the last recorded digital value *VFB_LAST* and comparing it with the currently sampled one of *VFB*. Thereby, the control mechanism extracts, whether the output voltage is rising or falling. Additionally, also the sign of the inductor current slope is determined, which is

easily done by using the internal control states of the two power transistors. If the p-channel MOSFET is turned on, the inductor current rises as charge is introduced from the input voltage supply *HVDD*. In case the nMOS transistor is enabled, the inductor current obviously declines. The sign detection of the inductor current slope has also been included in the basic control approach. If the output voltage ripple remains smaller than one LSB of the ADC, the control still ensures rippling around the target value *VFB_SET*.

Floating Input Range ADC

As outlined in the preceding paragraph, it would be desirable to employ a high resolution ADC recording the LED supply voltage in order to enable multiple valuable features, such as color shift compensation or real-time power monitoring. A conventional high resolution ADC however comes at the cost of a relatively high hardware effort in conjunction with either long conversion times or high power consumption depending on the used ADC architecture. The key idea of the floating input range ADC is thus to balance hardware effort and conversion time with the effective achievable resolution. This optimization is realized by employing an adjustable gain stage in front of the actual ADC circuit as conceptually depicted earlier in Fig. 6.7. Increasing the effective voltage gain eventually limits the resolvable input voltage range because of the opamp's bounded output voltage. Thereby, the opamp performs a clipping of voltages outside the resolvable input voltage range and improves sensitivity accordingly. The proposed concept eventually targets to only resolve a limited range around the output voltage ripple of the switching pre-regulator for a given operating condition. The floating input range ADC thus only handles relative values around the regulated LED supply voltage level. A relation to the absolute potential of the converter's output voltage is at first glance not deducible and also not necessary for the hysteretic regulation mechanism of the main converter control. The limited input voltage range thus implies two main consequences that need to be considered at all times. First, it is compulsory to ensure that the ADC is always capable of resolving the entire output voltage ripple and that it is never saturated by its input signal. The programmable gain of the amplifying OP hence needs to be chosen carefully in compliance with the actual LED supply voltage. In addition to choosing a suitable gain adjustment, the digital control fulfills the demand of ensuring an appropriate input voltage range by tuning the RDAC accordingly. Secondly, the proposed concept requires an appropriate start-up procedure in order to ramp up the LED supply voltage in a given setup, settle for the applied operating conditions and subsequently shrink the input voltage range of the ADC increasing the effective resolution. The

start-up routine thereby involves both leverages, the RDAC tuning and the gain adjustment of the opamp. The number of employed LEDs and the targeted LED current level mainly determine the final absolute potential of the converter's output voltage and hence affect startup time and behavior. Of course, also other operating conditions, such as temperature fluctuations, have an impact on the LED supply voltage. All these influences are inherently considered in the start-up routine, which is described and discussed in more detail in the subsequent paragraph. Once the start-up is finished, the proposed concept still tunes the RDAC in every dimming cycle during the off-time ($DIM = 0$) so that the measured ADC value is adjusted to reside in the middle of its resolvable range. Thereby, also slow temperature induced variations of the power converter's output voltage and hence of the ADC's input voltage can be compensated for in every dimming cycle. By this means, the system automatically eliminates the offset or error voltage between V_{FB} and V_{ref}. Considering the finite resolution of the RDAC a small offset of one RDAC LSB still remains, which is however not critical for system performance and can never lead to a saturation of the ADC as long as the gain is set correctly. This RDAC tuning routine can indeed be seen as an online auto-calibration technique. The absolute potentials of V_{FB} and V_{ref} must stay within a region from 0.8 V to 1 V, as this is the input common mode range of the downstream connected opamp.

Although the floating input range ADC handles only relative voltage levels, it is possible to calculate the absolute value of the LED supply voltage. The sought-after relationship is found by following the feedback path according to equations 6.3 to 6.8,

$$V_{DD,LED} = V_{FB} \cdot \frac{R_A + R_B}{R_B} \,, \tag{6.3}$$

$$V_{ADC} = A_{V,a} \cdot A_{V,b} \cdot (V_{FB} - V_{ref}) \,, \tag{6.4}$$

$$= -\frac{R_{2,a}}{R_{1,a}} \cdot \left(-\frac{R_{2,b}}{R_{1,b}}\right) (V_{FB} - V_{ref}) \,, \tag{6.5}$$

$$= |A_{V,LED\text{-}ADC}| \cdot (V_{FB} - V_{ref}) \,, \tag{6.6}$$

$$\Leftrightarrow \qquad V_{FB} = \frac{V_{ADC}}{|A_{V,LED\text{-}ADC}|} + V_{ref}, \tag{6.7}$$

$$V_{ADC} = \frac{\Delta V_{OP,out}}{2^{n_{ADC}} - 1} \cdot b_{ADC} \,. \tag{6.8}$$

Equation 6.10 eventually denotes an expression for the LED supply voltage in dependence of the digitally recorded ADC output b_{ADC},

$$V_{DD,LED}\left(b_{ADC}\right) = \left(\frac{V_{ADC}}{|A_{V,LED\text{-}ADC}|} + V_{ref}\right) \cdot \frac{V_{DD,LED}}{V_{FB}}\,, \tag{6.9}$$

$$V_{DD,LED}\left(b_{ADC}\right) = \left(\frac{\Delta V_{OP,out} \cdot b_{ADC}}{(2^{n_{ADC}} - 1) \cdot |A_{V,LED\text{-}ADC}|} + V_{ref}\right) \cdot \frac{R_A + R_B}{R_B}\,. \tag{6.10}$$

While this relationship appears rather complex at first glance, it can be reduced to a relatively low or at least well manageable complexity level. Once designed, the output range of the opamp ($\Delta V_{OP,out} = 1.4\,\mathrm{V}$) as well as the ADC resolution ($n_{ADC} = 4\,\mathrm{bit}$) and the reference voltage ($V_{ref} = 0.9\,\mathrm{V}$) are all not going to change and hence only represent a constant factor. For the presented implementation, the programmable gain $A_{V,LED\text{-}ADC}$ is only selectable in the powers of two, which results in simple shift operations for the computation. And last but not least, the changing factor of the resistive divider $\frac{R_A+R_B}{R_B}$ can be stored in a LUT in dependence of the control word b_{DAC} and thus also reduces to a constant factor for a given RDAC control word b_{DAC}. Thus the LED supply voltage can easily be calculated by the digital part without major effort. The computational effort is effectively reduced to a minimum of two multiplications, one shift operation and one subtraction of a constant.

In order to deduce the resolution of the floating input range ADC in terms of the LED supply voltage, it is helpful to calculate the LSB voltage in the HV domain. Equations 6.11 and 6.12 taken from [313] provide the corresponding relationship,

$$\Delta V_{DD,LED,LSB} = \frac{V_{OP,out,max} - V_{OP,out,min}}{(2^{n_{ADC}} - 1) \cdot |A_{V,LED\text{-}ADC}|} \cdot \frac{V_{DD,LED}}{V_{FB}}\,, \tag{6.11}$$

$$\Leftrightarrow \Delta V_{DD,LED,LSB} = \frac{1}{2^{n_{ADC}} - 1} \cdot \frac{\Delta V_{OP,out}}{|A_{V,LED\text{-}ADC}|} \cdot \frac{R_A + R_B}{R_B}\,, \tag{6.12}$$

Considering the used components in the feedback path leads to equation 6.12, whereas inserting the chosen $n_{ADC} = 4\,\mathrm{bit}$ ENOB resolution of the floating input range ADC in conjunction with the limited output range of the opamp of $\Delta V_{OP,out} = 1.4\,\mathrm{V}$ and a maximum programmable gain of $|A_{V,LED\text{-}ADC}| = 128$ gives equation 6.13. Considering a maximum output voltage of the switching pre-regulator of around 18 V, the LED supply voltage is resolved with an LSB value of less than 20 mV,

$$\Rightarrow \Delta V_{DD,LED,LSB} = \frac{1.4\,\mathrm{V} \cdot V_{DD,LED}}{15 \cdot 128 \cdot V_{FB}} = \frac{1.4\,\mathrm{V} \cdot 18\,\mathrm{V}}{15 \cdot 128 \cdot 0.9\,\mathrm{V}} \approx 14.6\,\mathrm{mV}. \tag{6.13}$$

Start-up Sequence of the Power Converter

At initial power turn-on the integrated buck converter has to ramp up the LED supply voltage to its final target value starting from 0 V. Because this final target value varies approximately between 2.5 V and 18.4 V depending on the number of connected LEDs, the implemented converter realizes a step-by-step start-up procedure in order to guarantee a secure and safe operation under all loading conditions [313]. Schulte Bocholt provides a detailed description of this start-up routine in her Master's thesis [313] as summarized in the following. The corresponding transient behavior, which has already been sketched in [313], is depicted in Fig. 6.9.

Preventing an overcharging condition, the power converter applies only certain charge packets $\Delta Q_{sup,x}$ to the output capacitor slowly increasing the LED supply voltage $V_{DD,LED}$. The start-up control of the converter forms a single charge packet $\Delta Q_{sup,x}$ by enabling the pMOS transistor for a fixed on-time $t_{on,sup}$ and subsequently activating the n-channel power MOSFET until the inductor current reaches zero ampere. The condition $I_L = 0$ is detected by a comparator at the switch pin as V_{SW} crosses the 0 V threshold in that case. The charge packets are continuously transferred to the output capacitor until the floating range ADC detects that the converter's output voltage $V_{DD,LED}$ has risen above its predefined internal target value. For this reason, the digital output word b_{ADC} of the floating input range ADC, which represents the analog feedback voltage V_{FB}, is internally compared to the digital reference value VFB_SET+1. This means that the start-up control triggers for measured voltages that are one LSB above the analog reference voltage of $V_{FB,set} = V_{ref} = 0.9\,\text{V}$ as VFB_SET resides exactly in the middle of the resolvable range of the floating input range ADC. Since the opamp gain is fixed to unity gain during the startup, one LSB corresponds to almost 100 mV in the V_{FB} voltage domain. Thereby, the entire input range of the upstream connected error amplifier is fully utilized. Once the internal set value is exceeded, the start-up control waits for a fixed settling time t_{settle} in order to avoid any distortions caused by switching the inductor current [313]. Subsequently, it enables the current regulator for a specific time duration t_{hold} letting the LED current jump to its aspired nominal level $I_{LED,nom}$. If the LED supply voltage $V_{DD,LED}$ is high enough, the drain potential V_D of the current regulator will rise to a certain voltage level according to the additional voltage headroom of the supply so that the LED current can actually flow. This condition is checked at the end of t_{hold} by a tiny comparator at the drain of the current regulator by assessing $V_D \geq V_{comp} = 600\,\text{mV}$. If the drain potential has exceeded the comparators threshold, the voltage start-up is finished since the LED supply voltage $V_{DD,LED}$ has reached a suitable value high enough to power all connected LEDs in compliance with the targeted current

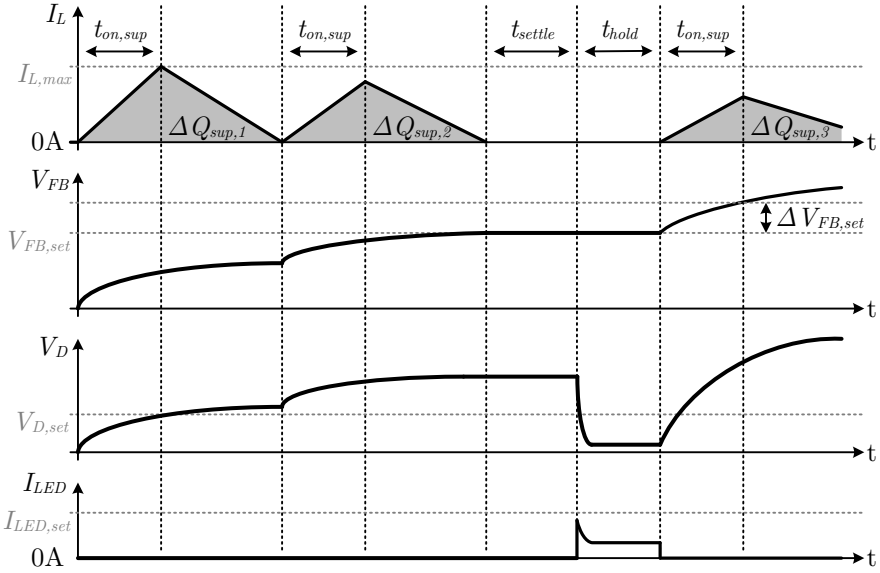


Figure 6.9: Transient behavior of involved current and voltage signals during the voltage start-up, redrawn from [313].

flow. Otherwise, the start-up control needs to continue and thus increments the RDAC's digital control word b_{DAC} according to a predefined value from a LUT. The b_{DAC} settings stored in that LUT are chosen to result in an increase of the output voltage $V_{DD,LED}$ between 0.7 V and 1.7 V as shown in [313], thus always assuring safe operating conditions and preventing a destructive overcharging. The start-up routine then repeats its procedure as described above for the new RDAC setting and continues to store charge packets on top of the output capacitor until the drain potential is finally high enough to finish the voltage startup. It should be noted that the programmable gain of the opamp in the feedback sense network is always fixed to 1 during the voltage start-up. Thereby, the floating input range ADC resolves the entire output voltage range with an LSB voltage $\Delta V_{DD,LED,LSB}$ of less than 2 V depending on the actual output voltage level according to equation 6.13. The step-by-step voltage start-up routine finally ensures that the LED supply voltage $V_{DD,LED}$ is charged with a maximum overhead of only 2 V for all possible operating conditions.

Once the voltage start-up of the switching pre-regulator is finished, an unknown overhead of up to 2 V still remains on top of the LED supply voltage.

While the dynamic headroom regulation process, which is explained later in more detail, obviously aims to minimize any additional overhead over the current regulator, it must however account for the size of the actual output voltage ripple $\Delta V_{DD,LED}$ of the buck converter. This ripple size is yet correlated to the effective LSB resolution of the floating input range ADC because the main converter control toggles around its internal digital target value *VFB_SET* with ±1 LSB. For efficiency reasons, it is therefore essential to enhance the effective ADC resolution to its maximum by increasing the gain of the upstream connected opamp before the converter can run in its normal operating mode. The gain adjustment needs to be performed again in a step-by-step manner in conjunction with a successive decrease of the drain potential because otherwise the floating input range ADC threatens to saturate to its rails under several operating conditions, which must be prevented in any case because of leading to an unstable control behavior. At the beginning of this gain start-up procedure the gain of the feedback sense opamp is still set to one as used during the voltage start-up routine. As a first step, the drain potential V_D over the current regulator circuit is decreased to a value smaller than its overall target level $V_{D,target}$ of 200 mV plus one LSB of the LED supply voltage according to equations 6.14 and 6.15,

$$V_{D,set} \geq V_D \geq V_{D,target}\,, \tag{6.14}$$

$$\begin{aligned} V_{D,set} &= V_{D,target} + \Delta V_{DD,LED,LSB}\,, \\ &= 200\,\text{mV} + \Delta V_{DD,LED,LSB}\,. \end{aligned} \tag{6.15}$$

In order to perform this action, the HQLED ASIC measures the drain potential by means of a 6 bit single-slope ADC and applies the dynamic headroom regulation procedure described later in the subsequent paragraph. Within this process the digital control regulates the measured and digitized drain potential to its internal given set value VD_SET that corresponds to the aforementioned analog voltage level of $V_{D,set}$. The digital control must therefore be aware of the correlation between an resolved LSB of the LED supply voltage and an LSB of the drain potential. According to Schulte Bocholt [313], equation 6.16 denotes the corresponding relationship, which results in a factor of approximately two for the given implementation,

$$\frac{\Delta V_{DD,LED,LSB}}{\Delta V_{D,LSB}} = \frac{\Delta V_{DD,LED,max}}{\Delta V_{D,max}} \cdot \frac{A_{V,Drain\text{-}ADC}}{A_{V,LED\text{-}ADC}} \cdot \frac{2^{n_{Drain\text{-}ADC}}}{2^{n_{LED\text{-}ADC}}}\,, \tag{6.16}$$

with $V_{D,max} = 600\,\text{mV}$ and $A_{V,Drain\text{-}ADC} = 2$. By design it must be ensured that the drain potential is resolved in terms of absolute voltage values at least

Table 6.1: Gain start-up settings of $A_{V,LED\text{-}ADC}$ in dependence of the range of the RDAC control word b_{DAC}.

b_{DAC}	Gain settings for incremental steps during start-up						
Range	$\mathbf{1}^{st}$	$\mathbf{2}^{nd}$	$\mathbf{3}^{rd}$	$\mathbf{4}^{th}$	$\mathbf{5}^{th}$	$\mathbf{6}^{th}$	**step**
$0 - 100$	1	2	4	8	16	32	
$101 - 200$	2	4	8	16	32	64	
$201 - 511$	4	8	16	32	64	128	

with the same, better a higher (digital) resolution than the LED supply voltage. Once the digital control has regulated the drain potential to a value that fulfills the condition of equation 6.14, it is save to increase the gain and hence the effective resolution of the floating input range ADC. Because the voltage overhead of the drain potential is limited to only one LSB of the LED supply voltage, an increase of the gain will never be able to saturate the feedback sense ADC. The opamp gain is thus increased in the next dimming cycle, typically by a factor of two. In the subsequent dimming period the entire process repeats for the increased resolution using the updated (and now smaller) value of $\Delta V_{DD,LED,LSB}$. The gain start-up is only then finished, when the control reaches the maximum possible amplification factor for the feedback sense opamp. Assuming a PWM dimming frequency of $f_{PWM} = 20\,\text{kHz}$, the gain start-up thus takes an additional 300 µs until the LED driving stage is ready for operation. It should be noted that the gain increment as well as the maximum programmable gain differ in dependence of the final LED supply voltage. For smaller output voltages the system cannot cope with very high gains as it would not be possible to resolve the entire output voltage ripple anymore in these cases. In order to prevent any undesired operating conditions, the digital control thus limits the maximum applicable gain and defines the gain increment levels in dependence of the RDAC control word b_{DAC}, which is an indirect indicator of the converter's output voltage $V_{DD,LED}$. Table 6.1 denotes the corresponding settings for the gain $A_{V,LED\text{-}ADC}$ of the feedback sense opamp.

Dynamic Headroom Adjustment Procedure

The dynamic headroom regulation for the integrated LED driving stage operates in principle like the initial idea presented in section 5.2 of chapter 5 for the discrete counterpart. The control routine measures the drain potential V_D by

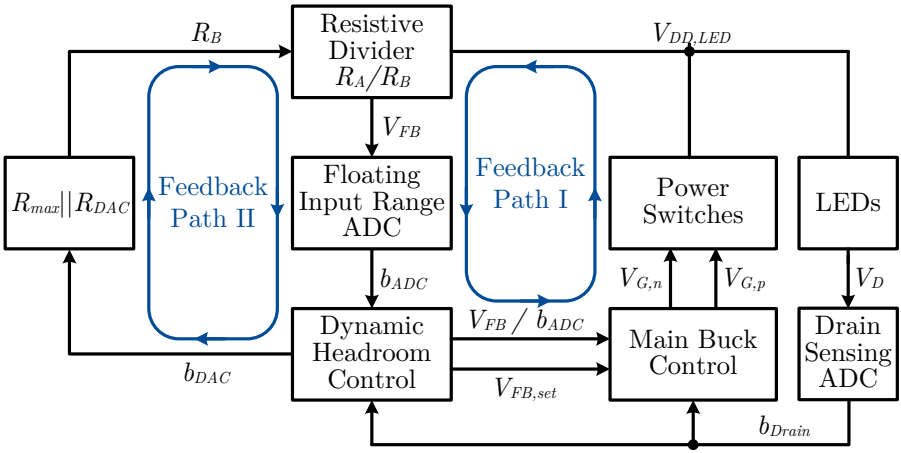


Figure 6.10: Highlighted feedback paths of the dynamic headroom regulation for its two control variables b_{DAC} and *VFB_SET*.

means of an ADC, subsequently averages the recorded values – typically over four consecutive samples – and compares the calculated mean drain potential $V_{D,mean}$ to its internal set value of the analog reference voltage $V_{D,set}$. By introducing an average mechanism over a programmable number of samples, the control speed is again kept intentionally slow. The drain potential V_D is moreover only sampled during the on-time of the current regulator ($DIM = 1$). Depending on the evaluation result of a too high or too low measured drain potential, the dynamic headroom regulation influences the main buck converter control to diminish or increase the LED supply voltage accordingly. In contrast to the solution presented in chapter 5, the integrated mechanism of the dynamic headroom control however possesses two control variables to affect the switching pre-regulator as desired. In addition to tuning the RDAC control word b_{DAC} it can also adjust the internal digital set value *VFB_SET* of the floating input range ADC, which serves as a reference level for the hysteretic main converter control. The conceptual block diagram of the dynamic headroom control mechanism as depicted in Fig. 6.10 shows both feedback paths that can be used to influence the converter's behavior adapting the LED supply voltage. Because the ADC resolution is designed to be more accurate than one LSB step of the RDAC, the digital reference level *VFB_SET* is always changed as first instance during the dynamic headroom regulation process and only in steps of ± one LSB. The control mechanism therefore follows feedback path I

as highlighted in Fig. 6.10 at first. In case $V_{D,mean}$ was determined to be too high, *VFB_SET* is lowered by one LSB, whereas it is increased by one LSB for a too low level of $V_{D,mean}$. The relatively small adaption steps of only one LSB are made in order to ensure that the floating input range ADC never saturates and is always capable of completely resolving the LED supply voltage including rippling effects. Considering large voltage overheads and a precise resolution/gain setting of the floating input range ADC, it may thus take a longer time to reach the aspired optimum value of the drain potential. A speed-up option like in the discrete implementation is so far not foreseen here. If the digital set value approaches the upper or lower limiting rail of its resolvable (4 bit) range during the regulation process, the RDAC control word b_{DAC} is adjusted instead. *VFB_SET* is then reset to the middle of its resolvable range in this case. As mentioned earlier, the RDAC is additionally tuned during the LED off-time ($DIM = 0$) so that the measured feedback voltage sits perfectly in the middle of the ADC's common mode input range. This measure in fact achieves full flexibility for changes of *VFB_SET* in the upcoming dimming cycle [313]. Beyond that, the entire dynamic headroom regulation is only executed, if the system resides in a so-called *"settled state"* [313], which is determined by an oscillation of the measured feedback voltage V_{FB} around its corresponding reference level *VFB_SET*.

Matching of the Main Control Loops

The PWM dimming control causes a hard and fast switching behavior of the LED current regulator at turn-on and turn-off. Thereby, sharp current pulses are generated, which appear as strong load jumps to the supplying power converter. Due to suffering from a limited response time the switching pre-regulator cannot readjust its output voltage fast enough. As a result the LED supply voltage experiences large voltage dips at turn-on that translate to the drain potential of the current regulator circuit as illustrated before in Fig. 5.16 and explained in chapter 5. Because these voltage drops require an additional headroom over the current regulator, the investigations conducted in chapter 5 moreover revealed possible efficiency improvements around 1 % to 3 % under realistic operating conditions, if these voltage drops can be vastly reduced.

In order to find a solution for diminishing the voltage drop over the current regulator it is helpful to investigate the current and voltage relationships of the regulating buck converter more precisely as illustrated in Fig. 6.11. The major reason for the voltage drop issue is the comparatively slow ramp-up time of the inductor current I_L. While I_L rises continuously with a slope of

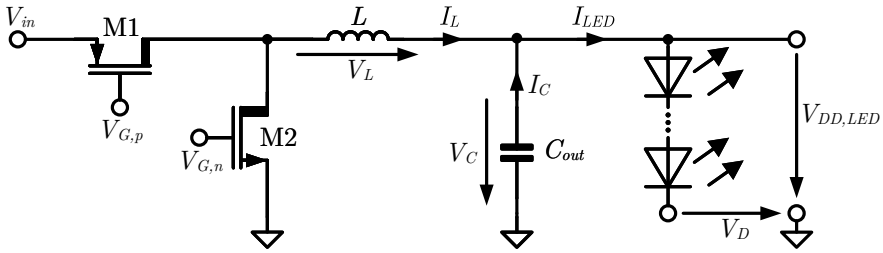


Figure 6.11: Current flow and voltage definitions of the buck converter.

$\frac{V_L}{L} = \frac{HVDD - V_{DD,LED}}{L}$ to its target value, the LED current I_{LED} through the current regulator jumps more or less instantaneously to its final level. As long as $I_{LED} > I_L$ prevails, the output capacitor is discharged with current I_C according to equation 6.17, which results in the aforementioned voltage drop. Fig. 6.12a qualitatively sketches the corresponding transient waveforms of the involved currents and voltages.

$$I_C(t) = I_{LED}(t) - \frac{I_{LED,nom}}{t_{drop}} \cdot t = I_{LED,nom} - \frac{V_L}{L} \cdot t \,, \text{ if } I_{LED} \geq I_L \quad (6.17)$$

$$t_{drop} = I_{LED,nom} \cdot \frac{L}{V_L} = I_{LED,nom} \cdot \frac{L}{HVDD - V_{DD,LED}} \,. \quad (6.18)$$

Calculating the charge taken from the buffering output capacitor directly delivers the height of the voltage drop according to the subsequent equations,

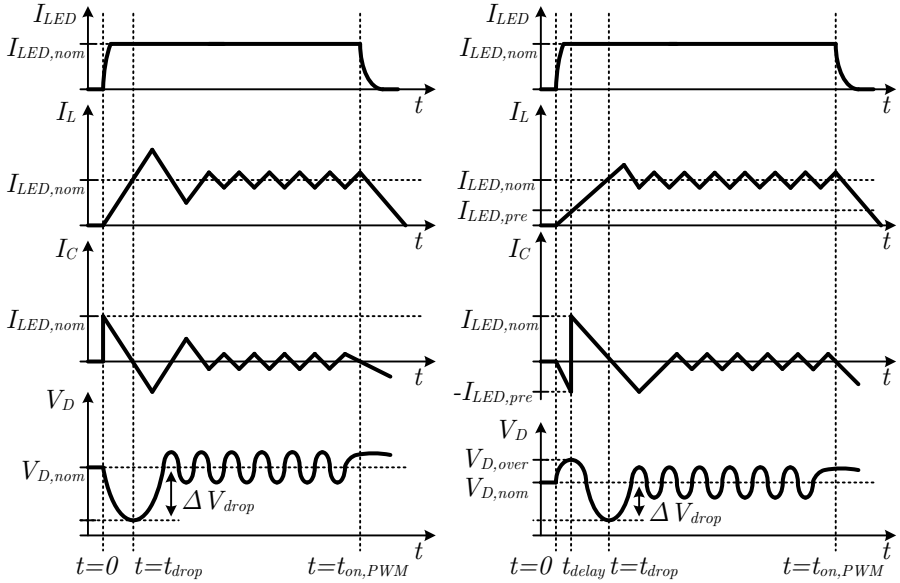
$$Q_{drop} = \int_0^{t_{drop}} I_C(t)\, dt = \frac{1}{2} \cdot I_{LED,nom} \cdot t_{drop} \,, \quad (6.19)$$

$$\Delta V_{drop} = \frac{Q_{drop}}{C_{out}} \,. \quad (6.20)$$

Inserting equation 6.18 and 6.19 into equation 6.20 finally yields an analytic expression for the voltage drop ΔV_{drop} in dependence of the selected system components, LED current flow and inductor voltage as shown in [313],

$$\Delta V_{drop} = \frac{1}{2} \cdot I_{LED,nom}^2 \cdot \frac{L}{C_{out}} \cdot \frac{1}{HVDD - V_{DD,LED}} \,. \quad (6.21)$$

Since the power converter cannot be designed to respond infinitely fast to such load transients and the system parameters L, C_{out}, I_{LED}, V_{in} and V_{out} on the



(a) Synchronous turn-on of the buck converter and current regulator.

(b) Delayed turn-on of the current regulator circuit.

Figure 6.12: Timing diagram of the current and voltage relationships at a switching event of the current regulator.

other hand are fixed for the given setup, a simpler and better way for reducing the voltage drop is to match the inner converter control loop to the current regulation loop. The implemented LED driving stage uses the PWM dimming signal for this purpose and applies it to both control loops as an enable indicator. In this context, the PWM signal effectively serves as a synchronization method of the two control instances.

The digital control is thus capable of introducing a specific delay t_{delay} to the current regulation loop as displayed in Fig. 6.12b. This delay allows for the inductor current to ramp up to a certain level $I_{LED,pre}$ before the full LED current is instantaneously turned on. As a consequence, the LED supply voltage rises by an amount ΔV_{over} according to the additional charge stored on the buffering output capacitor C_{out}, whereas the discharge period of C_{out} is reduced proportionately. The amount of overcharging according to Fig. 6.12b

is calculated by equation 6.22,

$$\Delta V_{over} = \frac{1}{C_{out}} \cdot Q_{over}\,, \qquad \text{with} \quad Q_{over} = \int_0^{t_{delay}} I_C(t)\,dt \tag{6.22}$$

$$\Rightarrow Q_{over} = \int_0^{t_{delay}} -I_L(t)\,dt = \int_0^{t_{delay}} -\frac{I_{LED,nom}}{t_{drop}} \cdot t\,dt\,, \tag{6.23}$$

$$\Leftrightarrow Q_{over} = -\frac{1}{2} \cdot I_{LED,nom} \cdot \frac{t_{delay}^2}{t_{drop}}\,. \tag{6.24}$$

In the same manner, the charge that is taken from the buffering output capacitor C_{out} can be computed in compliance with Fig. 6.12b following equation 6.25,

$$Q_{dis} = \int_{t_{delay}}^{t_{drop}} I_C(t)\,dt = \int_{t_{delay}}^{t_{drop}} I_{LED,nom} - I_L(t)\,dt\,, \tag{6.25}$$

$$= \int_{t_{delay}}^{t_{drop}} I_{LED,nom}\left(1 - \frac{t}{t_{drop}}\right) dt = I_{LED,nom}\left(t - \frac{t^2}{2 \cdot t_{drop}}\right)\Bigg|_{t_{delay}}^{t_{drop}}, \tag{6.26}$$

$$= I_{LED,nom} \cdot \left(\frac{1}{2} \cdot t_{drop} - t_{delay} + \frac{t_{delay}^2}{2 \cdot t_{drop}}\right). \tag{6.27}$$

The effective voltage drop can then be calculated by using equation 6.20, with a drop charge Q_{drop} that results from subtracting the absolute value of the overcharging (Q_{over}) from the total discharge charge (Q_{dis}) to

$$\Delta V_{drop} = \frac{Q_{drop}}{C_{out}} = \frac{1}{C} \cdot \left(|Q_{C,dis}| - |Q_{over}|\right), \tag{6.28}$$

$$\Leftrightarrow \Delta V_{drop} = \frac{I_{LED,nom}}{C_{out}} \cdot \left(\frac{1}{2} t_{drop} - t_{delay} + \frac{t_{delay}^2}{2 \cdot t_{drop}} - \frac{1}{2} \cdot \frac{t_{delay}^2}{t_{drop}}\right), \tag{6.29}$$

$$\Leftrightarrow \Delta V_{drop} = \frac{I_{LED,nom}}{C_{out}} \cdot \left(\frac{1}{2} t_{drop} - t_{delay}\right). \tag{6.30}$$

From the found expression of equation 6.30 a suitable delay can be derived in dependence of a tolerable voltage drop ΔV_{drop} and the previously specified system parameters as shown in equation 6.32,

$$\Delta t_{delay} = \frac{1}{2} t_{drop} - \frac{Q_{drop}}{I_{LED,nom}} = \frac{1}{2} I_{LED,nom} \cdot \frac{L}{V_L} - \frac{\Delta V_{drop} \cdot C_{out}}{I_{LED,nom}}, \quad (6.31)$$

$$= \frac{1}{2} I_{LED,nom} \cdot \frac{L}{HVDD - V_{DD,LED}} - \frac{\Delta V_{drop} \cdot C_{out}}{I_{LED,nom}}. \quad (6.32)$$

Different delay values can be stored in dependence of known input and output voltages (or for other application scenarios also in dependence of L and C_{out}) in a LUT. Alternatively, the corresponding delay can be programmed via the UART interface.

At the end of a PWM dimming cycle a similar issue occurs that could in fact be utilized to at least partially counteract the aforementioned voltage drop at turn-on. While the LED current is switched off nearly instantaneously, the inductor current decreases continuously and slowly. Because there is no more load current present for the switching pre-regulator, the entire inductor energy flows completely into the output capacitor C_{out} hence overcharging the LED supply voltage $V_{DD,LED}$. Fig. 6.12 illustrates also the transient behavior in this case. The resulting overcharging could on the hand be utilized for compensating the voltage drop at turn-on but might on the other hand lead to severe efficiency losses for application scenarios with a low LED supply voltage [313]. In such cases, the overcharging at turn-off can indeed become relatively large due to long discharge times of the inductor current [313]. Generally, it can be thought of two ways to handle this situation. First, the inductor current is switched-off a little bit earlier than the LED current regulator. This delay or rather associated *"advancing time"* is obviously different from the delay introduced at turn-on because the inductor current slope differs in both cases. A suitable advancing time could however be calculated in a similar manner as done for the turn-on case considering the charge stored on the output capacitor for a given inductor current $I_{LED,nom}$ and component sizes L and C_{out} as well as for different sets of output voltages. A second way to take care of this issue (especially for low LED supply voltages) is to measure the amount of overcharging by the floating input range ADC and compensate for it during the re-calibration phase of the RDAC during the LED off-time ($DIM = 0$). For this purpose, the digital control stores two values of the LED supply voltage and computes their difference to one another. The first value is the last measured one, when the LED current is still flowing ($DIM = 1$) and the second one is captured at a triggering event

of the switch pin comparator, which detects that the inductor current has fully decreased to zero. Since the difference of overcharging is well-known, the digital control can adjust the control word of the RDAC in a manner that the measured ADC voltage sits not exactly in the middle of its resolvable range but shifted by the amount of the measured overcharging difference. Therefore, the overcharging is more or less compensated for, while the turn-on delay for the current regulator remains suitable and unchanged to minimize the unwanted voltage dips at turn-on.

6.3.2 Implementation Aspects for the Integrated Buck Converter and its Control Circuits

Design, dimensioning and implementation of the employed switching pre-regulator and the corresponding control circuits have been carried out in the aforementioned Master's thesis [313],which describes concept and realization of the adopted converter stage in detail. Increasing the RDAC resolution as well as modifying converter type and output voltage range are rather straightforward procedures to be taken. These measures thereby employ conventional design methods realized in a simplistic manner as summarized in the following. Additionally, this section highlights the ADC implementations of the 4 bit SAR-ADC and the single slope ADC that are used for sensing the LED supply voltage $V_{DD,LED}$ and the drain potential V_D over the current regulator, respectively.

System Considerations

Considering the described digital control approaches for the main buck converter and the dynamic headroom regulation mechanism, Schulte Bocholt [313] provides detailed calculations and simulations of the system behavior in multiple application scenarios using different (worst-case) assumptions. This investigation includes various switching frequencies f_{sw}, inductor sizes L, output capacitors C_{out} and digital clock frequencies $f_{clk,buck}$. Based on the findings of the system analysis from [313], table 6.2 presents the dimensioning of system components and buck converter specifications that have been used for the final implementation in this work realizing the LED driving stage of the HQLED ASIC. The buck control operates at a clock frequency of $f_{clk,buck} = 100\,\text{MHz}$, while the main digital clock is set to $f_{clk,main} = 200\,\text{MHz}$. The high frequency main clock is needed for the current regulation process presented later in chapter 6.4. It should be noted that inductance L and buffering capacitor C_{out} are off-chip components that could easily be exchanged. This would however result

in different performance metrics, such as switching frequency, output voltage ripple, associated losses, etc. The switching frequency f_{sw} and the output voltage ripple $\Delta V_{DD,LED}$ define specifications that are eventually realized with the proposed system components and the implemented converter stage. The final layout of a single LED driving stage including all relevant integrated system blocks is presented in Fig 6.13. Besides highlighting the buck converter with its RDAC, floating input range SAR-ADC and single slope drain ADC, the graph also illustrates the CR based current regulator, which forms the PWM switched FET as proposed in the next section 6.4.

Dimensioning of the Power Stage in the Switching Pre-Regulator

The used 180 nm semiconductor technology provides different kinds of power devices that can withstand drain-to-source voltages of up to 20 V, 25 V and even 50 V, respectively. For the presented implementation, the medium devices that handle a $V_{DS,max}$ of 25 V have been selected as a compromise between electrical strength and area consumption. Accounting for a certain safety margin, the high voltage input supply *HVDD* is thus recommended to be kept below 23 V at maximum. nMOS and pMOS devices are both driven by a 5 V gate signal and must be capable of carrying currents up to 1.5 A [313]. Considering a nominal LED current flow of $I_{LED} = 700\,\text{mA}$ the switches are thereby capable to provide continuous conduction mode (CCM) as well as discontinuous conduction mode (DCM) operation. In terms of switching losses, the 20 V and 50 V power transistors appear indeed more attractive than the 25 V devices as these power MOSFETs could be driven by a relatively low 1.8 V gate signal. However, a maximum V_{DS} of only 20 V would restrict the number of attachable LEDs too much, whereas the 50 V devices consume an enormous amount of area.

In order to achieve the efficiency target of $\eta_{total} \geq 95\,\%$, it is moreover essential to keep the on-resistances of the power switches as low as possible. As a trade-off between area and overall efficiency, the power stage is dimensioned

Table 6.2: Component sizes and specification of system performance for the developed switching pre-regulator [313].

Component	L	C_{out}	$\Delta V_{DD,LED}$
Value	15 µH	4.7 µF	±10 mV
Frequency	$f_{clk,buck}$	$f_{clk,main}$	f_{sw}
Value	100 MHz	200 MHz	200 kHz − 1 MHz

Table 6.3: Characteristics of the used power devices as implemented in the switching pre-regulator design [313].

	Dimensions		**On-Resistance**	**Capacitances**	
	W	L	$T = 70\,°C$; $I_{LED} = 0.7\,A$	C_{GS}	C_{DS}
n-MOS	$5 \cdot 10\,mm$	400 nm	$R_{on,nMOS} \approx 240\,m\Omega$	316 pF	87 pF
p-MOS	$12 \cdot 10\,mm$	600 nm	$R_{on,pMOS} \approx 210\,m\Omega$	374 pF	72 pF

to yield an $R_{DS,on}$ around 200 mΩ for a nominal case with a load current of 700 mA. Table 6.3 finally shows the realized dimensions and characteristics of the power devices according to the implementation of [313].

RDAC Implementation

The RDAC is integrated on the HQLED ASIC with a 9 bit resolution and the values stated in table 6.4. As can be seen, the selected resistor values are quite similar to those of the discrete implementation from previous chapter 5, listed in table 5.1. Because the integrated version uses one bit more in contrast to its discrete counterpart, the LSB resistance $R_{B,1}$ is about double the size than its equivalent in the implementation with discrete COTS components. Because the RDAC concept as well as the resistive divider composed of R_A and R_B found on relative resistor ratios, absolute resistance tolerances are of no importance. The proposed implementation of the dynamic headroom regulation is therefore robust against temperature fluctuations and global process variations of the used semiconductor technology. This behavior is indeed very beneficial for a mass market production as it avoids the necessity of calibration for the proposed concept and thereby reduces die cost and test time. Nevertheless, very good matching between the individual resistances is indispensably required. A monolithic integration is thus quite advantageous as long as the total area consumption of the resistors is not becoming too big because the matching properties decrease with increasing implementation size. The employed resistor sizes as well as the digital resolution of the RDAC hence need to be chosen

Table 6.4: Dimensioning of the implemented 9 bit RDAC.

Resistor	R_A	R_{max}	$R_{B,1}$	$R_{B,9}$
Value	138 kΩ	69 kΩ	2.944 MΩ	11.5 kΩ

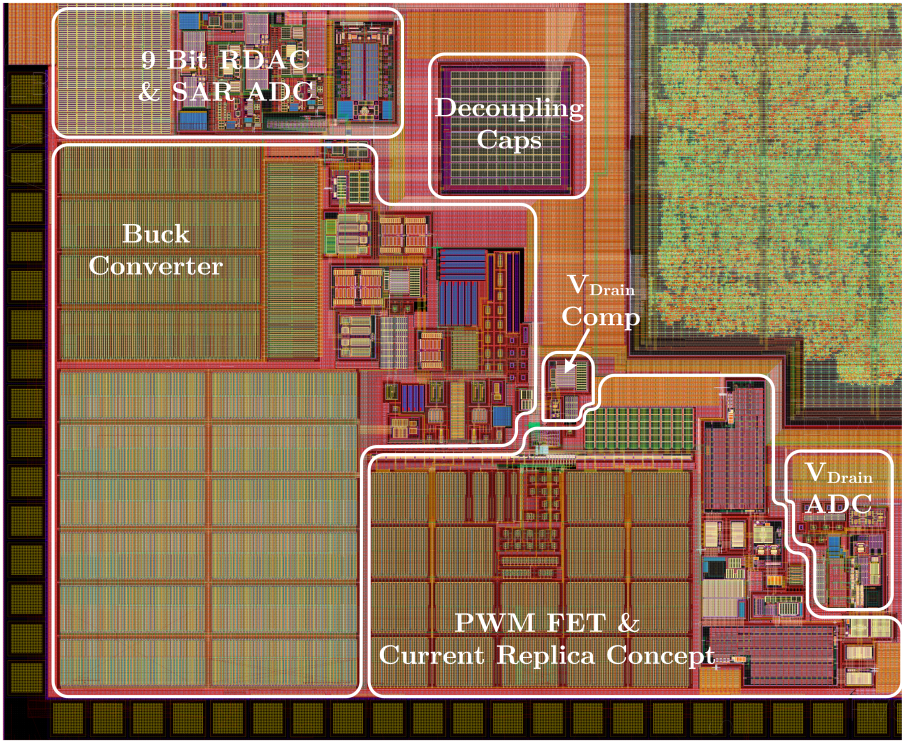


Figure 6.13: Layout view of the integrated LED driver with the CR concept and the RDAC based dynamic headroom control.

carefully. The resistances R_A, R_{max} and $R_{B,1}$ to $R_{B,9}$ are all realized by means of a unit resistor cell with a total value of 46 kΩ. This value is on the one hand large enough to keep the absolute number of instances low, while it is on the other hand small enough to allow for assembling of lower resistances by parallel connection at reasonable area consumption [313]. The layout of this unit resistor cell consists of five serial bars forming a square, which enables an increased electrical strength as the voltage drop is distributed equally among the series connected resistor bars [313]. Of course, the large resistors generate thermal noise, which has to be considered in the system evaluation, particularly with respect to the sensing ADC measuring the LED supply voltage. Further details on layout and implementation of the RDAC can be found in [313]. Due to its simplicity, high robustness and stability over temperature and process

variations, the RDAC based dynamic headroom control is in conclusion well suited for a monolithic integration.

Implementation of the Floating Input Range ADC

Fig. 6.7 illustrated not only the concept of the floating input range ADC but also the actual implementation. As can be seen, the programmable gain stage consists of two series connected opamps each featuring a linear amplification with a gain factor of $-\frac{R_{2,x}}{R_{1,x}}$. Both opamps are realized identically with the same switchable resistances $R_{2,x} = R_{2,a} = R_{2,b}$, which are dimensioned as a multiples of $R_{1,x} = R_{1,a} = R_{1,b}$ to ensure linear amplification by good matching properties. The resistance $R_{1,x}$ is chosen to equal about 16 kΩ, whereas the switchable resistances $R_{2,x}$ can be selected by the digital part in multiples of 1,2,4,8 and 16 of $R_{1,x}$. The gain stage or moreover the employed opamp is designed to feature an input common mode range spanning from 0.8 V to 1.0 V. Feedback and reference voltage, V_{FB} and V_{ref}, must always reside within this range. Since the reference voltage is chosen to equal $V_{ref} = 0.9\,\text{V}$, it sits perfectly in the middle of the input common mode range of the amplifier. After the LED supply voltage is downscaled by the resistive divider composed of R_A and R_B and has been amplified by the dual opamp stage according to the programmed gain setting, the 4 bit SAR-ADC converts the resulting analog voltage into the digital domain. The SAR-ADC – as well as some other circuit parts in the buck-converter like gate drivers, rising edge detection, etc. – has in fact been used from another project conducted at the chair of *"Integrated Analog Circuits and RF Systems"* at *"RWTH Aachen University"*. The ADC is designed in a fully differential manner according to the calibratable charge-redistribution architecture proposed by Aghaie *et al.* [4]. It uses a unit cell for the switchable capacitor array of $C_U = 16.3\,\text{fF}$. In order to keep the loop delay small, the ADC operates based on a 50 MHz clock and achieves conversion times of about 160 ns for the full 4 bit resolution. Further details on concept and implementation of this SAR-ADC can be found in [4]. Fig. 6.14 illustrates the implemented SAR-ADC embedded in the floating input range ADC concept in detail. The dummy capacitances C_{PD} and C_{ND} have been chosen to be equal to the unit capacitance $C_U = 16.3\,\text{fF}$.

Realization of the Single Slope ADC

The drain potential over the current regulator is sensed by a 6 bit single slope ADC. Following a conventional design topology, Fig. 6.15 illustrates the realized implementation. The input voltage is integrated over capacitance C_{trim}, while the time until the integrated voltage reaches the reference voltage level is

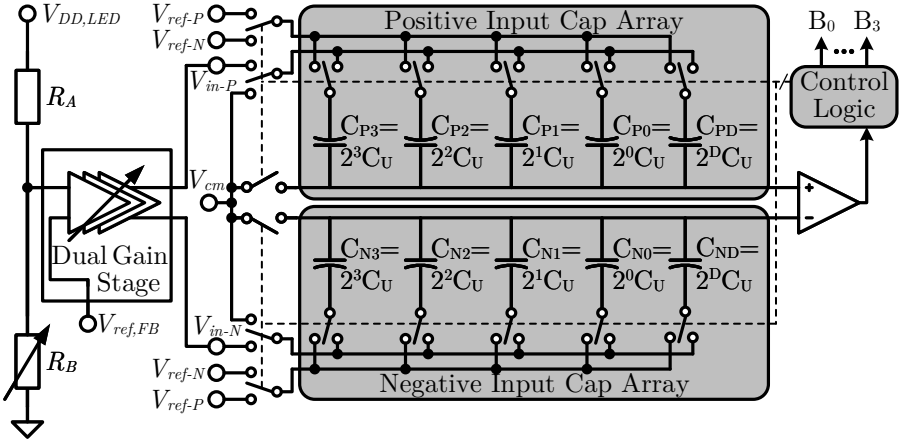


Figure 6.14: Implementation of the fully differential 4 bit floating input range SAR-ADC with a programmable dual gain stage.

measured by a digital counter. The capacitance C_{trim} is dimensioned with a fixed value of 5 pF that can be increased in steps of 1.25 pF up to 8.75 pF in total. Additionally, a minor 2 bit trimming mechanism is included to compensate for parasitic effects. The upstream connected resistor consists of a 210 kΩ resistance, which is moreover made trimmable. Three resistances of 10 kΩ, 20 kΩ and 40 kΩ that are all bypassed by default can be connected in series to the 210 kΩ if desired. If it is targeted to lower the 210 kΩ resistance, a 300 kΩ can be connected in parallel to the main input resistance.

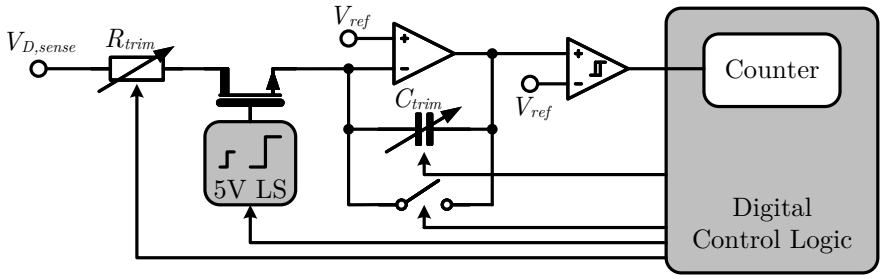


Figure 6.15: Implementation of the 6 bit single slope ADC measuring V_D.

6.4 Efficient and Precise Current Sense and Control Approach for Integrated LED Drivers

Particularly the current regulator circuit offers several optimization opportunities and improvement possibilities in a monolithically integrated design aiming to further boost energy efficiency as a key performance metric. For that matter, this section introduces the taken measures for the latter three system level enhancements listed in the end of section 6.1 in more detail. For example the drain potential of the current regulator can obviously be vastly reduced considering the 500 mV drop of the discrete implementation with COTS components as presented earlier in chapter 5. Besides optimizing the dynamic voltage adaption for this purpose, which has been explained in the previous section 6.3, it is suggested to eliminate the current sense resistor by applying the sense FET based *"Current Replica (*CR)" approach as initially proposed in [242]. Fig. 6.16 illustrates the conceptual idea and a possible realization of generating a current copy in a low voltage (LV) domain. Two well-matched power MOSFETs M_{ctrl} and M_{sense} are controlled with identical gate-to-source voltages, while a suitable control circuit like a high-speed opamp ensures that the drain-to-source voltages equal to each other under any operating conditions. Thereby, the generated sense current I_{sense} represents a precise replica of the LED current flow I_{LED} in dependence on the transistors' ratio, even if M_{ctrl} and M_{sense} reside in the very low ohmic region, which is necessary to achieve in order to ensure a high system power efficiency. Targeting to reduce the power consumption in the sensing path, transistors M_{ctrl} and M_{sense} must furthermore feature a high area ratio to one another, e.g. one of $(1000:1)$ or higher.

The published paper [242] already provides a concept feasibility as a matter of principle as well as a rough approximation for possible power savings in the sensing path. Assuming a 100 mΩ sense resistor R_{sense} in the main LED current path as used in the discrete implementation outlined in Fig. 5.1 of chapter 5 and publications [236], [237], the current sensing alone already consumes

$$P_{sense} = R_{sense} \cdot I_{LED}^2 = 0.1\,\Omega \cdot 0.7\,\mathrm{A}^2 = 49\,\mathrm{mW}\,. \tag{6.33}$$

While this number appears quite low at first glance, it already constitutes about 0.38 % of the total power consumption in a typical application scenario, which is the highest possible output power ($V_{DD,LED} = 18.4\,\mathrm{V}$; $I_{LED} = 700\,\mathrm{mA}$). For lower output voltages (or less series-connected LEDs) the percental share would even increase. Considering the fact that it is generally very difficult to improve already high efficiencies much further, a share of 0.38 % represents quite a large saving potential. The proposed CR concept on the contrary is expected

to consume less than 5 mW in its entire sensing path [242], which is only one tenth of the conventional sensing method. Applying the CR sensing method, it is expected to diminish the drain potential of the main current regulator M_{ctrl} to about 200 mV [242]. The CR concept is introduced in more detail in section 6.4.1 including particulars on the implemented circuit realization.

Beyond the sensing structure, also the current controller driving the main power transistor(s) consumes a significant amount of energy. In the discrete version referring to Fig. 5.13 this power consumption is mainly attributed to the regulating opamp as well as to the switching losses of MOSFET M_{ctrl}, when the PWM signal is turned on and off, respectively. Because this current control method is supposed to be very fast and accurate, it puts stringent demands on the design of the regulating opamp, particularly with respect to gain, bandwidth and loop stability. Applying the CR sense approach somehow intensifies this issue as a second high-speed opamp needs to be employed for the V_{DS} regulation of M_{ctrl} and M_{sense}. Because the two opamps regulate two different control loops, which may not interfere with one another, it is compulsory to thoroughly decouple them to ensure stable operation. Consequently, the CR OP needs to react at least ten times faster than the OP steering transistor M_{ctrl} to guarantee a settled I_{sense} for the acting current controller. The achievable trade-off between gain, speed and stability finally influences or moreover determines the reachable accuracy of I_{LED}. These extreme requirements might result in a very high

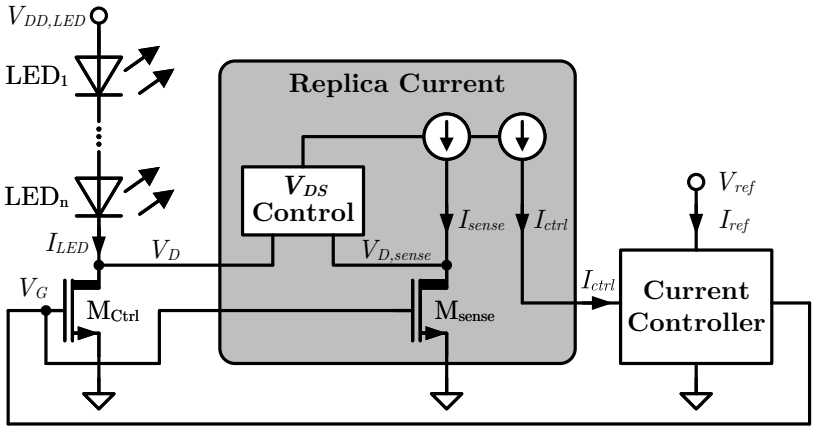


Figure 6.16: Current Replica (CR) sense and control concept for integrated LED drivers.

power consumption of the main opamp controlling MOSFET M_{ctrl}, while they even threaten to reach the physical limitations of the employed semiconductor technology. Implementing the proposed CR concept, different solutions for the current controller are yet conceivable. Besides the just described (and disadvantageous) fully analog solution, it is possible to develop either a mixed-signal approach, which regulates only a small portion of the analog current, whereas the main current contribution is provided by several digitally turned on power switches, or a complete digital regulation procedure. Both methods relax the specification of the main current regulating OP. For the mixed signal concept, a suitable segmentation between analogously regulated and digitally set portions has to be selected with respect to the desired target application. Assuming that the analog portion is capable of regulating approximately $I_{LED,ana,max} = 100\,\text{mA}$, the digitally portion needs to be set close enough to the desired target current but may not exceed it because the analog part can only add current to the system. For currents lower than $I_{LED,ana,max}$ the analog regulation would operate stand alone. Although the mixed-signal approach relaxes the specification of the main OP regarding its drive capability, the major issues of a high gain, bandwidth and stability requirement still remain. This work thus focuses on an all digital approach, which is explained in depth in the subsequent section 6.4.2. Of course, the speed and accuracy requirements are only shifted or rather distributed to a suitable ADC and the digital part, but it might still be easier to ensure stable decoupling of the interfering control loops in this case.

Dispensing with the sense resistor, the CR approach thus yields not only lower losses due to the smaller required voltage headroom over the current regulator and an efficient sensing circuit, but also offers the potential to realize an all digital current control. By this means, additional flexibility is introduced into the LED driving stage because the current control is e.g. capable of applying AM as well as PWM dimming to the effective LED current by simple digital re-programming. Hence, also bilevel (BL) and hybrid dimming techniques can be easily realized without any additional effort. Still, the dynamic headroom control needs to account for the different dimming methods and might require suitable adoptions in its digital control.

Beyond that, the switching behavior of the current regulator is optimized to realize faster turn-on and and turn-off transitions. The presented approach indeed targets to implement a minimum on-time of about 200 ns. Keeping the original contrast ratio of 1:250 or $DIM = 0.4\,\%$, this enhancement even enables very fast PWM dimming frequencies of up to 20 kHz. Increasing the employed PWM switching frequency of the LED current regulator to about 20 kHz is very beneficial as it diminishes audible noise while preventing any visible and non-visible flickering. Moreover, this feature offers another degree of freedom for

optimizing light quality with respect to contrast ratio and dimming capability. If a lower PWM frequency than the 20 kHz is chosen, it is possible to realize higher contrast ratios as the absolute minimum on-time of 200 ns remains. The simulation and measurement results of the color control algorithm's experimental validation in chapter 4.5 suggest that a higher contrast ratio may significantly improve the achievable color shift $\Delta u'v'$, particularly if the selected chromaticity coordinate is in close proximity to a LED primary. Therefore, lowering PWM frequency in the integrated design from 20 kHz to e.g. 5 kHz is a good measure to improve color precision. However in this case, it has to be taken care that the PWM frequency is not decreased too much. In order to minimize the risk of flickering f_{PWM} should remain greater than the critical flicker frequencies of $f_{flicker,lowrisk} = 1.25\,\text{kHz}$ and $f_{flicker,noeffect} = 3\,\text{kHz}$, respectively, as outlined in chapter 2.2.4. The CR sense and control approach hence offers various advantages and has thus been implemented in the HQLED ASIC as described in the following.

6.4.1 System Concept and Implementation of the Current Replica Sense Approach

The main idea of the proposed CR sense approach is to generate an accurate copy of the LED current in a LV domain, scaled down by a high ratio factor $b_{CR,ratio}$. Using a LV supply in conjunction with a high ratio factor $b_{CR,ratio}$ enables the targeted large power savings due a to small sensing current. Two key components in the CR sense module eventually determine the performance of the entire circuit regarding accuracy and speed. These dominating blocks are on the one hand the opamp regulating the drain potentials of M_{ctrl} and M_{sense} and on the other hand the (charge-based) ADC. Fig. 6.17 highlights these components as a part of the CR sense concept.

The opamp needs to be fast enough to follow the voltage ripple at the drain induced by the buck converter so that the resulting current flowing through the segmented power switch M_{ctrl} always equals precisely the copied sense current with respect to the applied ratio factor $b_{CR,ratio}$. Therefore, the regulating opamp OP1 demands a very high gain-bandwidth product (GBW). Considering a maximum switching frequency of the power converter for the dynamic headroom regulation of $f_{sw,max} = 1\,\text{MHz}$, a GBW of around 60 MHz to 100 MHz is aspired. In addition to the high speed operation this requirement also calls for an exact accuracy, which reflects in the opamp's DC gain, low noise and low offset voltage. A DC gain level of 80 dB to 100 dB shall therefore be reached to account for the high accuracy specification. It is thus advisable to use a folded-cascode architecture as the input stage of the opamp. To relax

the requirements on the DC gain a little bit, it can moreover be thought of applying an auto-zeroing technique to cancel the offset voltage of the opamp. Introducing a small time frame at the end of a PWM dimming period might provide the required time slot for applying this method and re-calibrating the offset error. Since the proposed LED driving system features a PWM signal (*DIM*) for enabling dimming functionality anyways, the correspondingly short calibration time, in which the PWM FET is always turned off, can easily be added at the end of the PWM period. In fact, this approach comes in handy for the voltage adaption loop of the previously described dynamic headroom control because the RDAC may always re-calibrate during that phase as well so the floating input range ADC is set to the middle of its evaluation range. It should be noted that the precise high-speed opamp requires some kind of HV protection circuit at its positive input to safeguard itself against the high voltages during the PWM off phase. With respect to offset voltage, it must thus

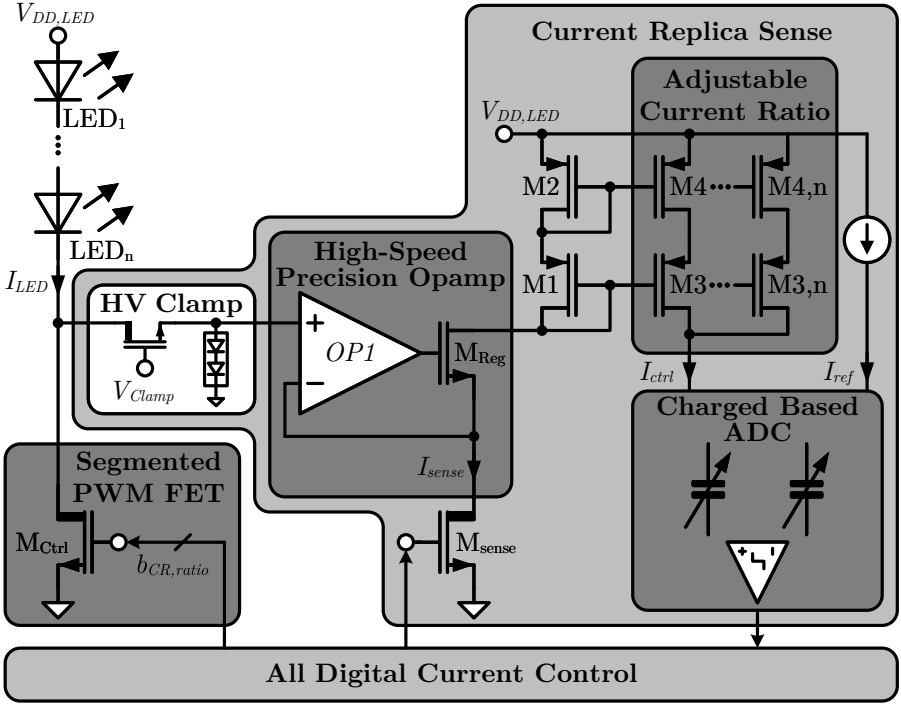


Figure 6.17: Highlighted analog key components in CR sense & control concept.

be ensured that the protection circuit does not impose a noticeable discrepancy between the drain potentials of power and sensing FET. In order to keep the power consumption of the CR sensing module to a minimum, the developed circuits operate on a relatively low supply voltage of $V_{DD,CR} = DVDD = 1.8\,\mathrm{V}$. This results in a limited operating range of the CR concept with respect to applied drain potential because transistor M_{Reg} suffers from a constricted V_{DS} headroom due to the bounded supply and the on top connected cascode current mirror. For the proposed design, precise current copies could consequently only be reached for $V_D < 600\,\mathrm{mV}$. Applying the dynamic headroom regulation proposed in section 6.3, this range is however more than sufficient because the drain potential is typically regulated to about 200 mV, which leaves enough room for any deviations. In addition to the opamp performance, also very good matching of the used components is required, particularly regarding the current mirrors that feed the sense (and also the reference) current, into the downstream connected ADC. To achieve high-speed current copies with precise accuracy, the proposed concept applies the cascode structure as well as good matching properties to all relevant current mirrors. Beyond that, a high precision of the reference current I_{ref} in the ADC must be ensured. The proposed implementation of the CR concept features a programmable current mirror copying the sense current I_{sense} to the input of the charged-based CR ADC. While the copying ratio $b_{CR,mirror}$ is typically set to one, it offers the possibility to introduce a gain boost to the sense current in gain steps 0.25 up to a factor of two. The relation between the actual sense current I_{sense} and the input current of the ADC I_{ctrl} is given by equation 6.34,

$$I_{ctrl} = b_{CR,mirror} \cdot I_{sense}\,. \tag{6.34}$$

The second important component in the CR sense path is the ADC converting the copied sense current I_{ctrl} into the digital domain. The developed ADC is designed as a charge-based architecture, while operating in a SAR structure. Fig. 6.18 illustrates the realized circuit schematics as part of the CR sense concept in detail. To allow for fast conversion times in conjunction with sufficient accuracy, a resolution of 8 bit has been chosen, while the ADC is driven by a main clock frequency of $f_{clk,main} = 200\,\mathrm{MHz}$. The unit capacitance of the 8 bit capacitor array is selected to approximately $C_{CR,U} = 111\,\mathrm{fF}$ using a metal-insulator-metal (MIM) structure, whereas the current I_{ctrl} that needs to be sampled varies between 50 µA to 200 µA depending on the actual drain potential V_D and the adjusted gain factor $b_{CR,mirror}$ of the copying current mirror. The nominal current level in the sense path equals about 125 µA for $V_D \approx 200\,\mathrm{mV}$. The operation of the charge-based CR ADC proceeds during a conversion cycle as described in the following. In an initial step, the ADC

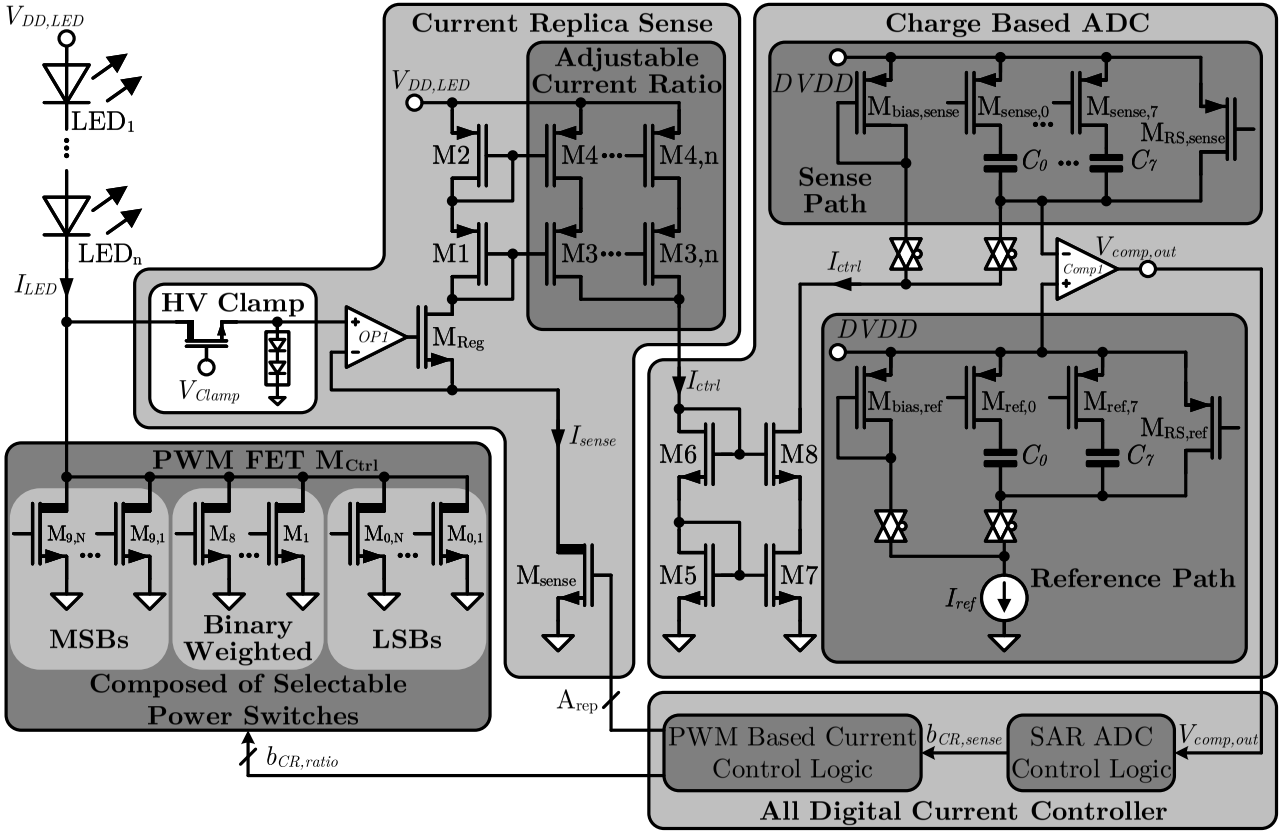


Figure 6.18: Detailed circuit schematics of the implemented CR sense and control concept.

control logic resets both inputs of the evaluating comparator as well as the entire capacitance array to the LV supply *DVDD* for a minimum time period of at least two 200 MHz clock cycles. The duration of this reset time $t_{CR,reset}$ is yet designed programmable, thus allowing for longer reset phases if desired, which might be necessary or beneficial in certain cases. After the entire circuitry has been reset, the actual sampling period begins. The length of this sampling period $t_{CR,sample}$ is once more adjustable by the digital part and typically set to five clock cycles of 5 ns each. During this time frame the ADC control logic enables the respective bit under evaluation as well as any previously evaluated bits according to their state and thereby connects the respective capacitances to the input of the evaluating comparator. Thus, the sensing current I_{ctrl} effectively discharges the selected ADC capacitors until the predefined time slot $t_{CR,sample}$ of the sampling period has elapsed. Subsequently, the digital part enables the analog comparator for evaluation and checks its output state in the successive clock cycle. If the ADC input current I_{ctrl} has discharged the connected capacitances more than the reference voltage, the comparator's output state yields a digital low level ('0'). Thereby, the control knows that the applied capacitances were in total still too small. The bit under evaluation thus needs to stay enabled and remain set to a digital high level ('1') for the next bit evaluation cycle. Otherwise, if the voltage at the comparator's sense pin remains above the comparing reference level and the output state of the comparator returns a high value ('1'), the selected bit is finally evaluated to zero ('0') and the corresponding capacitor is not turn-on in the next conversion cycle. Starting with the MSB the charged-based CR SAR ADC successively evaluates all 8 bit, each with a conversion time $t_{CR,conv}$ of typically 45 ns. Tuning the sampling time $t_{CR,sample}$ it is also possible to achieve faster conversion times down to 30 ns per bit while maintaining decent accuracy. The way of operation also explains the relatively high value of the unit capacitance $C_{CR,U}$, which is necessary to enable a certain minimum discharging time to feature a good accuracy. As can be seen from Fig. 6.18, sense and reference path of the charge-based ADC are built symmetrically. Instead of using a constant reference voltage V_{ref} at the positive input pin of the comparator, the proposed concept applies the same sensing technique to the reference path. In this way, the reference current I_{ref} is transformed into a reference voltage in the same manner as the sensing current I_{ctrl} translates to a sensing voltage at the comparators' inputs. The reasoning for this approach arises from distortions and deviations introduced into the sensing path by the switching activity of the SAR-ADC's capacitances. By applying the same switching technique to the reference path, the reference current I_{ref} experiences more or less the same deviations. As a consequence of this pseudo-differential configuration, the introduced distortions cancel each

other out, which facilitates in the end a very precise measurement of the copied sense current I_{ctrl}. The advantage of a charge-based ADC lies indeed in an additional tuning component, which is the sampling time $t_{CR,sample}$ that can be utilized to optimize accuracy. Equation 6.35 denotes the relationship for the amount of charge that is taken from the ADC capacitances, which results in equation 6.36 giving an expression for the measured current I_{ctrl} in dependence of the selected control word $b_{CR,sense}$ and the sampling time $t_{CR,sample}$,

$$\Delta Q_{sense} = C_{CR,sense,total} \cdot \Delta V_{sense} = I_{ctrl} \cdot t_{CR,sample}\,, \tag{6.35}$$

$$\Leftrightarrow I_{ctrl} = \frac{C_{CR,sense,total} \cdot \Delta V_{sense}}{t_{CR,sample}} = \frac{b_{CR,sense} \cdot C_{CR,U} \cdot \Delta V_{sense}}{t_{CR,sample}}\,. \tag{6.36}$$

Considering the I_{ref} being measured in the same way, equation 6.37 obtains,

$$\Rightarrow I_{ref} = \frac{C_{CR,ref,total} \cdot \Delta V_{ref}}{t_{CR,ref,sample}} = \frac{b_{CR,ref} \cdot C_{CR,U} \cdot \Delta V_{ref}}{t_{CR,ref,sample}}\,. \tag{6.37}$$

Assuming that the voltage differences ΔV_{sense} and ΔV_{ref} across the respective capacitors are nearly equal after evaluating all 8 bit, equations 6.36 and 6.37 finally yield an analytic expression of the measured current copy I_{ctrl} in dependence of evaluated control word $b_{CR,sense}$, the reference current I_{ref} and the corresponding adjusted digital settings as denoted in equation 6.38,

$$\Rightarrow I_{ctrl} = \frac{t_{CR,ref,sample}}{t_{CR,sample}} \cdot \frac{b_{CR,sense}}{b_{CR,ref}} \cdot I_{ref}\,. \tag{6.38}$$

This developed relationship is very useful, when it comes to the all digital current controller, as described in the subsequent section 6.4.2.

6.4.2 All Digital Current Controller

The current regulation mechanism has been designed to operate completely in the digital domain. Like its analog counterpart, the all digital current controller also targets to adjust the PWM-switched power MOSFET M_{ctrl} in dependence of available sensing and reference information so that the desired LED current actually flows. Due to its digital nature, the control mechanism is however not able to regulate the analog gate-to-source voltage of M_{ctrl} precisely. Instead of using a power-hungry high-speed opamp to drive the PWM FET, the proposed current controller therefore segments M_{ctrl} into small, well-defined portions that can be turned on- or off individually by digital control signals. Thereby, it is possible to realize extremely fast switching speeds for the single segments. The

used semiconductor technology is indeed quite beneficial for a digital control approach because it provides HV MOSFETs with breakdown voltages of 20 V and 50 V that are controlled via a comparatively small gate signal of only 1.8 V. Due to the segmentation of M_{ctrl}, the all digital current controller can regulate the analog LED current only in digitally selectable steps according to the segmented partitions. The conceptual idea of the MOSFET's fragmentation has already been indicated in Fig. 6.18.

In order to function and perform an accurate regulation of the overall LED current, the all digital current controller must be capable of relating the measured sensing information on I_{ctrl} to the total LED current flow as well as to the current flowing through the segmented partitions of M_{ctrl}. The smallest unit of the PWM FET M_{ctrl} is hence sized exactly like the sensing device M_{sense} and thus referred to as an LSB in the following. For the same reasoning, the largest fragment of M_{ctrl} is called an MSB. This dimensioning implies that the LSB current is identical to the sense current I_{sense} under ideal conditions, whereas the current flowing through the other parallel-connected transistor bits all the way up to the MSB relate to the sensing current in a fixed ratio according to their sizing. Besides keeping the gate-to-source voltages (V_{GS}) and the drain-to-source voltages (V_{DS}) of the replica sense transistor M_{sense} and the PWM FET M_{ctrl} identical to each other, very good matching between both devices must therefore be guaranteed at all times. Good matching among all segments is targeted to be achieved by using unit cells in the physical layout of the transistor devices. As can be seen from Fig. 6.18, the main power transistor M_{ctrl} contains multiple LSB switches. These have been added for trimming purposes, if needed. The major partitions of M_{ctrl} are yet binary weighted based on the LSB cell size in order to facilitate a simple digital control mechanism later on. The binary weighted design was however only realized to some extend because the MSB segment still needs to match very well to the LSB cell and hence the sense transistor M_{sense}. Therefore, multiple equally sized MSB cells have been integrated in the power MOSFET. In consequence of its physical structure, this part of M_{ctrl} requires a linear thermometer code control, which is also straightforward to implement. The span from LSB to MSB comprises 9 bit in total, while 17 equally sized MSBs have been integrated in the power transistor M_{ctrl}. While the lower binary weighted partitions are expected to match very well to the LSB cell, the higher segments, particularly the MSB, might yet deviate a little bit. The current control algorithm therefore foresees several trimming and calibration possibilities for each of the selectable power stages in the digital part, e.g. the ratio of a particular segment with respect to the LSB cell is made programmable in LSB steps. This means that in a addition to the binary weighting several single LSB steps can be added or subtracted in

dependence of the matching properties. Using the matched, digitally selectable transistor segments the all digital current controller correlates the recorded sense current to the actual LED current flow. The relation between sense and LED current is basically given by the ratio factor of transistors M_{ctrl} and M_{sense}, as denoted in the subsequent equation,

$$I_{LED} = b_{CR,ratio} \cdot I_{sense} \,. \tag{6.39}$$

It should be noted that the ratio factor $b_{CR,ratio}$ is composed of the individual segment weightings, which refer to sensing LSB cell of M_{sense}. Thus, the turned on bits of M_{ctrl} eventually determine the ratio factor $b_{CR,ratio}$. Since the digital control algorithm however only measures the copied sense current I_{ctrl}, it needs to correlate the recorded current copy to the sense current I_{sense} and thereby also to the LED current path. Inserting equation 6.34 into equation 6.38 yields the sought-after expression for the sense current,

$$I_{sense} = \frac{1}{b_{CR,mirror}} \cdot \frac{t_{CR,ref,sample}}{t_{CR,sample}} \cdot \frac{b_{CR,sense}}{b_{CR,ref}} \cdot I_{ref} \,, \tag{6.40}$$

whereas the resulting formula 6.40 can be passed to equation 6.39 for a correlation to the LED current,

$$I_{LED} = \frac{b_{CR,ratio}}{b_{CR,mirror}} \cdot \frac{t_{CR,ref,sample}}{t_{CR,sample}} \cdot \frac{b_{CR,sense}}{b_{CR,ref}} \cdot I_{ref} \,. \tag{6.41}$$

The analytic expressions highlighted in equations 6.40 and 6.41 finally show the sense and the LED current as a function of well-known digital settings, specified parameters and the measured digital representation of the copied sense current $b_{CR,sense}$. To achieve a high accuracy in the end, the reference current must be calibrated in advance of the measurement and the corresponding digital value needs to be transfered to the all digital current control via the UART interface. Also the digital setting $b_{CR,ref}$ for the capacitive switching matrix in the reference path has to be selected carefully in advance. Nevertheless, all elements in equations 6.40 and 6.41 are well-established so that the digital part can compute the actual current flow in LED and sense path based on the measured ADC word $b_{CR,sense}$ and in dependence of the actual current ratio $b_{CR,ratio}$. Since the sampling times of reference and sensing path as well as the current mirror ratio of the CR sense path and the information on the reference current I_{ref} and its capacitive bit selection value $b_{CR,ref}$ are typically not meant to be changed once the current measurement is running, they can be summarized to a constant pre-scaling factor $f_{prescale,sense}$, which can be computed in advance. Thereby, equation 6.40 simplifies to a linear function

of $b_{CR,sense}$, which is only multiplied with a constant factor. Formula 6.41 relaxes likewise to one additional multiplication of the updated current ratio $b_{CR,ratio}$. The subsequent equations depict the simplified relationships,

$$I_{sense} = f_{prescale,sense} \cdot b_{CR,sense}\,, \tag{6.42}$$

$$I_{LED} = b_{CR,ratio} \cdot f_{prescale,sense} \cdot b_{CR,sense}\,. \tag{6.43}$$

Recognizing the physical layout of the segmented PWM FET M_{ctrl} as well as recalling the algebraic equations eventually helps to better understand the developed digital control methodology. The key idea of the all digital current controller is to perform an online computation of the LED current flow and determine the difference in respect to a predefined target value, as denoted in equation 6.44,

$$I_{LED,diff} = I_{LED,target} - I_{LED}\,. \tag{6.44}$$

Consequently, the digital control methodology aims to minimize this current difference $I_{LED,diff}$ to a value below one LSB. After the ASIC is powered on and the start-up procedure described in section 6.3 is finished, the all digital current control enables a predefined number of segment switches as an initial step. Based on their known weightings the applied ratio factor $b_{CR,ratio}$ is found immediately. Once the selected bits have turned on the corresponding segments of the power MOSFET M_{ctrl}, a short wait phase elapses in order to let the LED current settle from its switching activity to the chosen init value. The length of this wait period is again programmable via the UART interface in steps of 5 ns according to a number of subset clock cycles of the main 200 MHz system clock. Subsequently, the current controller sends a conversion start command ($CS = \text{'1'}$) to the ADC control logic, which senses I_{ctrl} by means of the charge-based SAR-ADC according to the previously described measurement routine. Because the entire current regulation mechanism is timing critical, the digital controller already starts calculating the actual current levels in LED and sense path during the on-going ADC conversion as described in the following. Since it takes several clock cycles, until the charge-based SAR ADC has evaluated the first bit of the sense current, the digital control uses this time for several pre-computations. Recalling equations 6.40 and 6.42 the digital control algorithm computes at first the pre-scaling factor $f_{prescale,sense}$ based on predetermined digital settings and parameters. Beyond that, the digital control algorithm possesses an offset- as well as a gain-correction mechanism, which are both executed afterwards as a second and third pre-computational step. Both correction schemes represent another method of the aforementioned

trimming measures to improve overall accuracy. By this means, it is possible to account for any offset and gain errors of the charge-based SAR ADC and thus receive an exact result of the measured sense current. This step requires a thorough pre-calibration of the used HQLED chip. The specified offset and gain correction values can subsequently be passed to the digital control again via a sequence of UART programming. After the pre-computations are completed, the digital control waits for the ADC logic to indicate a successful evaluation of a new valid bit value. Every time the charge-based SAR ADC control has determined a single bit, it reports the found value, either '0' or '1', in conjunction with the respective bit position to the current controller. Using the pres-caling factor $f_{prescale,sense}$ the sense current (and likewise the LED current) is computed by simple shift and add operations depending if the evaluated bit is one or zero. This procedure allows for relaxed computational effort, while it saves computation time as it does not have to wait until the ADC conversion of all bits is completely finish. Once the LSB of the charge-based SAR-ADC is found, sense and LED current are thus readily calculated after only one additional clock cycle as well as the current level for each of the weighted MOSFET portions. Because of the binary weighting the segment current levels can be computed by a simple shift operation. If a correction for matching reasons is applied as discussed earlier, the respective current levels are modified according to the additional weighting. The specified correction hence requires one more step as a subtraction or addition of the respective LSB correction value has to be conducted. In parallel, the all digital current controller already determines the actual value of the difference current $I_{LED,diff}$ by executing equation 6.44. Subsequently, it detects the sign of the difference current and according to a case selection that is similarly organized to a binary search algorithm it finds the numbers of LSBs and MSBs to be switched on or off, respectively, until $I_{LED,diff}$ is smaller than an LSB. Thus, the all digital current controller finally outputs a new digital control word $b_{CR,ratio}$ for the segmented power transistor M_{ctrl} and regulates the LED current flow as desired. Because of simplifying the complex calculations to simple shift and add operations as well as using a straightforward case selection method, the all digital current controller can output a new control value within five to nine clock cycles after the ADC conversion is complete depending on the size of the difference current. Under steady state conditions it is expected that the all digital current controller only requires five clock cylces as the difference current $I_{LED,diff}$ is rather small.

In order to improve the regulation performance of the all digital current controller regarding speed and accuracy, certain enhancement techniques have additionally been implemented in the control algorithm. However, these additional features could unfortunately not be developed until a resilient maturity

level was reached due to project related timing reasons. Nevertheless, the developed control methodology comes e.g. with a *"tracking mechanism"* so that the ADC does not need to evaluate all of its eight bits, but only the last few ones. This feature speeds up the current regulation time significantly as a large part of the ADC conversion time can be saved. Additionally, the digital control incorporates an auto-selection for the current mirror ratio in the CR sense path as well as a D-controller taking the last differences between the current changes into account. Including a rising and a falling slope detection, the latter feature might be useful to predict the current flow and counter compensate for an increased or decreased current level, respectively, which results from the switching pre-regulator's output voltage ripple.

6.5 Summary & Efficiency Analysis of the Proposed HQLED ASIC Design

This chapter showed improvement strategies and concepts that can be taken in a monolithically integrated design of a *"smart LED driver"*, while focusing particularly on the LED driving stage. Several enhancements are also presented for the DLT approach regarding the integrated FW-RX architectures. In conducted simulations the DLT CG has proven to functionally and robustly work in the same manner as its discrete counterpart. A lower power consumption is expected for the DLT FW-RXs due to employing power optimized components like the filtering opamp or a slow SAR-ADC. Some innovate ideas, like new ZCD concepts are only theoretically discussed and need to be verified in real hardware measurements, which is attributed to future work.

Regarding the LED driving stage, it was found that especially design and matching of the individual control loops feature the capability of boosting the LED driver's performance significantly. In consequence of adjusting the different control loops more precisely to one another, the large voltage dips at turn-on can be diminished from about 150 mV in the discrete implementation with COTS components to less than 50 mV in the integrated design. Thus, the dynamic headroom regulation is improved significantly as the voltage over the current regulator can be lowered accordingly. In substantial simulations the proposed system concept was proven to be functionally and operate robustly under various application conditions and scenarios. Some of the results have already been published in a very good Master's thesis [313]. In the end, the proposed enhancements lead to a higher (system) efficiency compared to the implementation shown in chapter 5, while the output voltage is kept within reasonable limits of $\Delta V_{DD,LED} \leq \pm 20\,\text{mV}$. The system efficiency is eventually

boosted to more than 95 % as shown later in this section. Beyond that, an innovative concept for sensing the LED output voltage has been introduced, which is based on a floating input range ADC. By this means it is possible to measure the LED voltage with high precision so that it is conceivable to apply additional performance features like a color shift compensation method via forward voltage measurements as suggested in chapter 4. The floating input range ADC was also investigated regarding its possible control performance of the buck converter. Although the developed concept was found to functionally work in a robust manner, it must however be constituted that the increased loop delay yields a worse performance in contrast to a simple window comparator with trimmable threshold voltages. In fact a combination of both approaches would be the perfect choice to merge all beneficial features. Nevertheless, it should be noted that the offset voltage of the window comparator (as well as of the opamp for the floating range ADC) must be gauged to achieve good precision of the main converter control.

Additionally an all digital current control method based on the CR sensing technique has been introduced to further lower the drain potential of the current regulator. Extensive Monte Carlo simulations were conducted for the analog sensing frontend, which featured an overall accuracy for the measured sense current I_{sense} with respect to an LSB current in the main power transistor M_{ctrl} of around 1 µA. Applying the described calibration and trimming techniques in the digital domain this accuracy is kept up for the final performance analysis. Considering a nominal current flow of 125 µA, a deviation of 1 µA is in fact less than 1 %, which is clearly within the aspired target range of less than 3 %. The all digital current controller proved to work very well, fast and stable. A large set of simulations showed that the regulation was working with high accuracy as targeted. Nevertheless, the applied SAR-ADC topology was found to be the speed bottleneck. It operates effectively too slow in order to keep the LED current perfectly flat so that a ripple of several mA was still present at the LED current waveform. Therefore, it is suggested to apply another ADC architecture instead, which is capable of sensing the current much faster. A promising approach has been tested in several simulations, which is a 4 bit pipeline staged flash ADC. Applying three different reference currents and subtracting evaluated bits with a current DAC from the input current flow finally yields approximately 10 bit ENOB, which is more than sufficient. This concept is however not taped out on the HQLED test chip and still under development. Nevertheless, it is expected to yield the targeted speed up, while keeping the power consumption within reasonable limits. The all digital current controller itself was found to operate very fast based on a 200 MHz clock frequency. Also regarding the current controller there are still several improvement aspects open

that would be interesting to invest in future research. It might in fact turn out that a mixed signal solution or an analog regulation based on the CR approach are also well applicable, while balancing power consumption.

To evaluate the HQLED ASIC regarding overall power consumption and perform a suitable efficiency analysis, all circuit components need to be taken into account. Beyond presenting a detailed design procedure and comprehensive system investigations, Schulte Bocholt [313] has indeed already conducted an elaborate analysis on associated power losses of the complete system and for the employed components. The losses of the power stage in the switching pre-regulator can be calculated based on the dimensioning presented in Tab. 6.3. Accounting for a mean die temperature of approximately 70 °C and an average inductor current flow of $\bar{I}_{L,avg} = 700\,\mathrm{mA}$, the resistive losses are computed based on the applied duty cycle D,

$$P_{Ron,buck} = \bar{I}^2_{L,avg} \cdot (D \cdot R_{on,pMOS} + (1 - D) \cdot R_{on,nMOS}) \,, \tag{6.45}$$

whereas the capacitive losses for n- and pMOS are calculated in dependence of the switching frequency,

$$P_{sw,xMOS} = C_{GS} \cdot f_{sw} \cdot V^2_{GS} + C_{DS} \cdot f_{sw} \cdot V^2_{DS} \,, \tag{6.46}$$

$$P_{sw,\ buck} = P_{sw,nMOS} + P_{sw,pMOS} \,, \tag{6.47}$$

with $V_{GS} = 5.5\,\mathrm{V}$, $V_{DS} = HVDD = 23\,\mathrm{V}$ and the capacitance values of Tab. 6.3. Duty cycles from 20 % to 80 % have been assumed, while an average switching frequency of $f_{sw} = 550\,\mathrm{kHz}$ has been used as a typical and realistic application case. Besides taking the obvious loss contributions, such as resistive and switching losses of the buck converter's power stage, into account, this analysis of Schulte Bocholt [313] also includes other relevant lossy elements, like high contact resistances of pin and pad connections as well as parasitic resistances of used components. The overall parasitic resistance of pin and pad connections in the high power path as well as the inductor's equivalent series resistance (ESR) sum up to approximately $R_{para} \approx 300\,\mathrm{m\Omega}$, which yields a loss contribution of 147 mW for an average load current of $I_{LED} = 700\,\mathrm{mA}$. The resistive losses in the output capacitor are approximated to roughly 12.5 mW for an assumed ESR of the output capacitor of 50 mΩ [313]. It turns out that the losses in the feedback sense network of the buck converter are comparatively small. Accounting for associated losses in the RDAC based resistive divider, the amplifying gain stage and the 4 bit floating input range SAR ADC, Schulte Bocholt [313] concludes the overall losses in the feedback sense path to 7 mW at maximum. The comparator at the switch pin consumes an additional 0.07 mW, which is more or less

negligible. Besides the power converter used for dynamic headroom regulation, also the current regulator consumes a certain amount of energy. The resistive losses are evaluated to a contribution of $P_{Ron,Mctrl} = 140\,\text{mW}$, which assumes a 200 mV voltage drop for $I_{LED} = 700\,\text{mA}$. The driving losses for the power transistor M_{ctrl} are mainly associated with switching losses as several segments of M_{ctrl} are continuously turned on and off, respectively, when using the all digital current controller in conjunction with the CR sensing concept. Since the drain potential is comparatively low during these times, the gate switching losses are expected to dominate. For a worst case approximation the total gate capacitance of the entire M_{ctrl} transistor is measured to be $C_{GS} \approx 660\,\text{pF}$, while a switching frequency of 10 MHz is assumed. Equation 6.46 can be utilized to determine the switching losses during the online current regulation as well as for the turn-on and off phase caused by the dimming signal. For the all digital regulation it is assumed that half of the total capacitance is switched with a speed of 10 MHz. This is by far a worst case approximation and yields total losses of approximately 10.82 mW. The switching associated with dimming is conducted at a much lower frequency of maximum $f_{PWM} = 20\,\text{kHz}$ but this time the higher V_{DS} voltage, which equals the LED supply voltage in this case, leads to the drain associated switching losses being dominant, whereas the gate switching losses with a contribution of only 42.8 µW are nearly negligible. Applying again equation 6.46 for this case, the switching losses for dimming M_{ctrl} are found to be approximately 0.84 mW using $C_{DS} \approx 100\,\text{pF}$ and $V_{DS} = 20\,\text{V}$. The losses in the CR sense path sum up in total to 5.85 mW. While the high-speed opamp consumes about 0.5 mW, an average sensing current of 125 µA flows in three paths from the $DVDD = 1.8\,\text{V}$ supply to ground, which gives an average consumption of 675 µW. The same average current is flowing through the reference path, thus consuming an additional 675 µW. The charge-based ADC switches both reference and sense path with an average time period of $T_{sw,CR\text{-}ADC} = 45\,\text{ns}$. Considering the 8 bit resolution with a unit capacitance of $C_{CR,U} = 111\,\text{fF}$ equation 6.48 denotes a power consumption in both, reference and sense path of roughly 2 mW,

$$P_{CR,ADC} = \frac{V_{supply}^2 \cdot 2^{N_{CR,ADC}} \cdot C_{CR,U}}{T_{sw,CR\text{-}ADC}}\,. \tag{6.48}$$

Although the single slope ADC at the drain consumes much less, it is assessed in this efficiency calculation also by 2 mW for a worst case assumptions. Of course, also the digital part consumes some amount of power, which is estimated to roughly 50 mW. Tab. 6.5 summarizes all losses on component level according to [313] and the above stated assumptions and computations. As can be seen, the total loss power including parasitics and all mentioned circuits only adds

Table 6.5: Loss contributions for a single channel LED driver with digital dynamic headroom regulation and an all digital current controller.

Loss Contributor	**Symbol**	**Losses**
On-resistances of the power stage based	$P_{Ron,buck}$	106 mW to 115 mW
Capacitive switching losses of the power stage	$P_{sw,buck}$	57.7 mW
Parasitic pin, pad & routing resistances	P_{Rpara}	147 mW
Feedback sense network	P_{FB}	7 mW
Parasitic ESR of C_{out}	P_{RCout}	12.5 mW
Single slope ADC at Drain (V_D) of M_{ctrl}	$P_{Drain\text{-}ADC}$	2 mW
On-resistance of M_{ctrl}	$P_{Ron,Mctrl}$	140 mW
Switching losses of M_{ctrl} due to dimming	$P_{sw,Mctrl,Dim}$	0.84 mW
Switching losses of M_{ctrl} due to regulation	$P_{sw,Mctrl,Reg}$	10.82 mW
Power consumption in CR sense path	$P_{CR,sense}$	5.85 mW
Power consumption of digital part	$P_{digital}$	50 mW
Total power dissipation of LED driver	$\boldsymbol{P_{LED,drv}}$	**548.7 mW**

up to an overall value of 548.7 mW. This is an excellent result, as the targeted aim of a peak efficiency higher than 95 % can be fulfilled. The derived power consumption value even leaves some room (of about 80 mW) with respect to this set target, if unaccounted or slightly higher consumptions in the individual blocks occur. Considering the typical application scenario of five series connected LEDs with a forward voltage of 3.6 V at $I_{LED} = 700\,\text{mA}$, the useful power output yields 12.6 W. Based on these findings the overall efficiency of the proposed monolithically integrated LED driving stage is computed to

$$\eta_{HQLED,string} = \frac{P_{used}}{P_{loss} + P_{used}} = \frac{12.6\,\text{W}}{548.7\,\text{mW} + 12.6\,\text{W}} = 95.8\,\%\,. \quad (6.49)$$

Finally, it was possible to produce the HQLED ASIC in a 180 nm HV CMOS process including all of the proposed and described features and functionality. Fig. 6.19 illustrates a photograph of the produced testchip. In several test measurements, the all digital current controller was found to be operationally functional, but precise performance analysis including reliable measurements of the entire chip were so far not conducted and are assigned to future work.

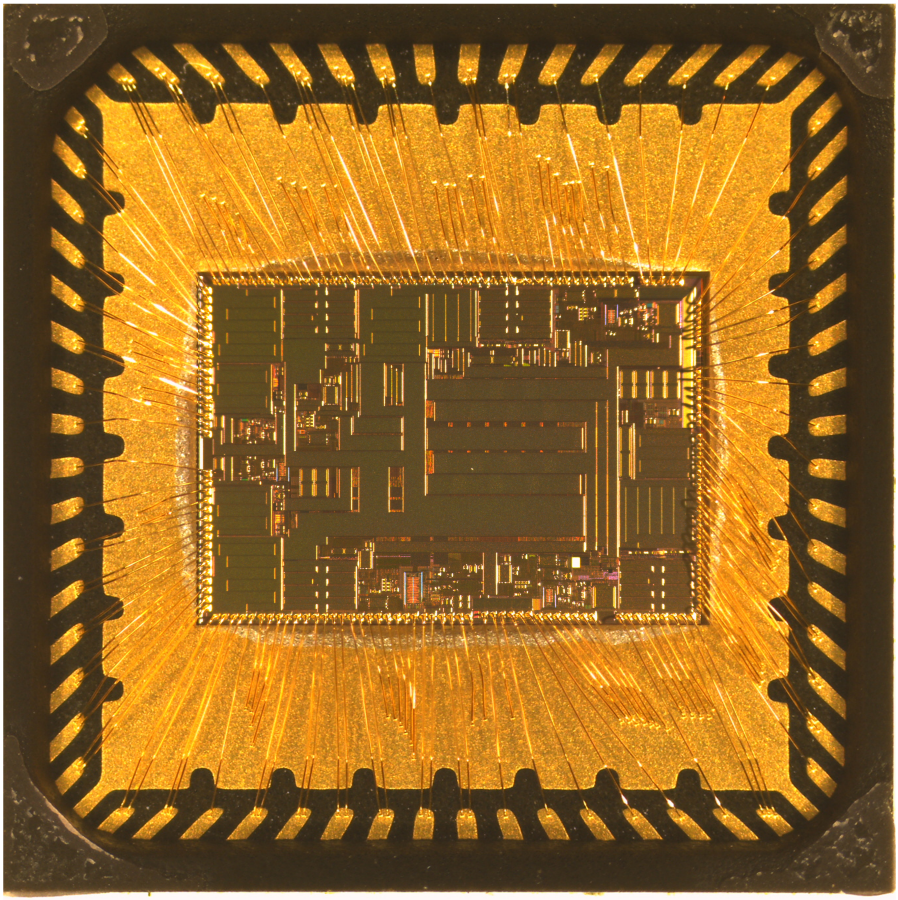


Figure 6.19: Photograph of the produced HQLED ASIC.

Chapter 7

Conclusion and Outlook

Future lighting systems face three major challenges that need to be addressed simultaneously by prospective concepts and developments. These key aspects can be summarized to first, *"reduce energy consumption and achieve high (system) efficiency"*, second, *"improve applied system intelligence of installed lighting fixtures"* and third, *"realize excellent light quality to enhance living comfort and well-being of human beings"*. In this context, human centric lighting (HCL) has recently evolved into an emerging research field in science and industry. Aiming to pave the way for HCL applications in the near future, this thesis focused on the core component of an automated lighting system, which is the *"smart LED driver"* inside of an intelligent luminaire. As its primary objective, the conducted research thus targeted to answer, how *"smart LED drivers"* can be tailored and improved regarding the aforementioned key challenges with energy-efficient and flexibly deployable electronics. In consequence of this guiding research question, the main building blocks, communication system, color control algorithm and multi-channel LED driving stage, have been investigated in depth on circuit, component and system level. Balancing the individual

requirements this thesis seeks to solve the conflict of aims between high energy efficiency and precise color control in conjunction with a substantial system intelligence. Taking additional design aspects into account, such as robustness, complexity, size and costs, it pursued to achieve the specific measurable goals for each of the three main functional units as summarized in Tab. 1.1.

7.1 Summary and Conclusion

The specific measurable goals denoted in Tab. 1.1 in fact originate from a sound literature review that was carried out throughout **chapter 2**. Aiming to establish an optimized solution for tailored smart lighting systems, this thesis therefore thoroughly analyzed and derived the corresponding system specifications in compliance with the three key challenges from a top-down perspective. Starting with a brief overview of smart home area networks (HANs) chapter 2 elucidated the fundamental physical relationships, requirements and bottlenecks for communication system, color control algorithm and multi-channel LED driving stage. Thereby, possible interdependencies between these main building blocks were identified and revealed. The selected LED current level and waveform as well as the applied dimming scheme influence e.g. optical performance of the color mixing algorithm like color accuracy or human perception parameters, such as flicker. Consequently, it was finally possible to define quantifiable performance metrics for each of the main building blocks, which basically reflect in the targeted goals stated in Tab. 1.1. In addition to that, the comprehensive literature survey comprises a compendium on state-of-the-art solutions for each of the main building blocks. By this means, it was later on possible to compare existing approaches in science and industry to the novel system concepts, control theories and circuit architectures developed within this thesis. Based on the found insights a monolithically integrable system concept was proposed that unites communication system, color control algorithm and multi-channel LED driving stage to a compact and flexibly deployable *"smart LED driver"*. In this manner, the main building blocks were well matched to one another and precisely specified in compliance with the key challenges. This general idea of a fully integrated *"smart LED driver"* and the resulting specifications finally propel the enhancements in each building block forward through the course of this work.

7.1.1 Goals 1-3: Enhanced DLT Communication

The first three goals that have been defined in the introductive part of this work cope with the communication system as part of a *"smart LED driver"*.

Pursuing these objectives **chapter 3** studies different enhancement measures for the Digital Load-Side Transmission (DLT) approach regarding increased system intelligence and better efficiency, while maintaining low power consumption, high robustness and minimum circuit complexity. Thereby, this thesis conceived various receiver (RX) architectures in compliance with the existing DLT standard [106]. The performance analysis of the developed concepts finally evaluated two designs, an active analog bandpass filter with a downstream connected Schmitt-Trigger (concept A) and a differentiating digital FIR filter with a window comparator (concept B), as being favorable for a monolithic integration of a DLT control gear (CG). Both architectures achieved comparable performance results regarding minimum circuit complexity, low power consumption and high reliability with a slight advantage for the digital detector approach. Power consumption was well below the targeted 50 mW for both RX circuits during active operation. In standby mode, the DLT system basically disconnects attached CGs, which leads to zero power dissipation in the RX circuits. Error rates were measured for each concept by means of a hardware test setup under real operation conditions over a longterm period of 24 h. Although the measurement setup was connected to real mains of the European utility grid in a noisy lab environment with many discrete interferers and random grid distortions, both RX architectures achieved excellent results, which is reflected in the low error rates of only 57 ppm and 44 ppm for concept A and B, respectively. Thus, goal 1 was in summary fully accomplished. The developed concepts and circuit architectures moreover pave the way for high-volume productions of monolithically integrated DLT CGs as part of a *"smart LED driver"*.

The second goal targets to improve system intelligence of the DLT communication methodology by enabling wireless accessibility of DLT control devices (CDs). Despite the strict power supply limitations of the DLT standard [106], this thesis devised two power supply topologies that can cope with the discontinuous input conditions and the low current draw during the DLT supply period. Both power supplies were based on a dual-stage converter design providing galvanic isolation. Realizing the corresponding circuits with commercially available off-the-shelf components, reliable measurements of the hardware setups were conducted yielding maximum continuous output powers of 353 mW and 389 mW at $V_{out} = 3.3\,\mathrm{V}$ with overall efficiencies of 63.7 % and 66.3 %, respectively. It was furthermore proven that the developed power supply topologies were resilient against blackouts of the utility grid, as they are capable of compensating for several missing half-waves of mains in dependence of the drawn load current. Both supply concepts enabled the continuous operation of a ZigBee or WiFi module in conjunction with an LCD backlight. It is thereby possible to embed DLT as a sub-system into other lighting control systems or smart home envi-

ronments. Because system intelligence of the DLT approach is substantially improved in that matter, goal 2 was also completely achieved. In addition to being compliant with the official DLT standard [106], the developed power supplies are compatible with existing installations and other retrofit technologies so that they could be applied to all kind of wall mounted dimmers.

Since DLT is limited due to its unidirectional communication capability, the third major objective of this work aimed at establishing a bidirectional communication method to further improve and tailor system intelligence of the DLT approach. In the course of its research, this thesis identified the load current as a suited reverse (REV) communication channel and applied a simple OOK scheme. In this way, the backward transmission closely relates to the existing DLT standard and its modulation patterns [106]. After conceiving a transmitter (TX) circuit that can be integrated in the structure of a DLT CG's FW-RX, this thesis investigated four different RX architectures situated in the CD for the reverse channel. These four approaches were all realized in hardware and examined in extensive measurements regarding power consumption, circuit complexity and robustness. During the investigations all REV-RX circuits were trimmed to comply with the reliability requirement ($\mathrm{TER}_{REV} \leq 1\,\%$) of goal 3, while minimizing the modulation current amplitude $I_{mod,set}$ and hence power consumption at the same time. In this procedure, robustness of the REV-RXs was evaluated by measuring error rates over a long transmission period of 24 h. Recording more than one million telegrams, these elaborate 24 h longterm measurements proved to be a reliable indicator for the REV-RX circuits's robustness. Finally, only two concepts, a transformer based sensing approach and a digital matched filter, were capable to satisfy both, the power consumption and the robustness targets of goal 3. The transformer based sensing yielded a TER of only 5 ppm at a total power consumption of $P_{REV,total} = 25.77\,\mathrm{mW}$, whereas the digital matched filter consumed $P_{REV,total} = 45.62\,\mathrm{mW}$ for achieving a TER of 322 ppm. Although the performance metrics clearly suggest the deployment of the transformer based approach, it needs to be considered that this performance boost is bought for an increased hardware effort, higher circuit complexity and a raised cost position. The digital matched filter on the contrary can be integrated on the operating main μC without any additional effort. If the power consumption requirement can be slightly relaxed, an active analog BP also represents a promising approach as it achieves a TER of only 114 ppm at $P_{REV,total} = 72.57\,\mathrm{mW}$. By developing a fully functional reverse transmission this thesis extended the DLT communication methodology far beyond the existing standard [106].

Summarizing the proposed improvement measures, chapter 3 finally investigated, whether the enhanced DLT technique is a competitive alternative in con-

trast to other well established communication methods. WiFi, Bluetooth (LE), ZigBee and digitalSTROM™ were referenced as suitable benchmark systems. Finally, this thesis assess the enhanced DLT approach as particularly suitable for tailored lighting systems in the near future. Satisfying the first three goals completely, the enhanced DLT methodology is more than capable of competing with existing communication methods due to providing multiple beneficial features, such as low (standby) power consumption, high robustness as well as easy retrofitting at low cost.

7.1.2 Goal 4: Color Control For High Quality Lighting

An essential key feature in HCL applications is to achieve excellent color precision, which is mainly determined by the underlying color control algorithm in conjunction with the analog regulation of the LED current. **Chapter 4** thus pursued the forth goal and focused on developing a multi-channel color control algorithm. Investigating the mathematical relationships of LED color computation, this thesis finally came up with a control strategy that comprises up to six LED primaries and can be flexibly deployed for any number between two to six LEDs. Being based on a QR decomposition the developed control approach accounts for the human nonlinear color and brightness perception and maps its computed relative intensity distribution onto PWM duty cycles of the corresponding LED channels. Due to handling more than three LEDs the color control approach features an additional degree of freedom for every extra LED primary. This work hence explored a parametric optimization and embedded it into the control algorithm by means of an optimization vector. This vector contains (fixed) weightings for each LED according to a chosen optimization criterion like CRI, luminous output or maximum efficiency. Beyond that, several additional features were implemented, such as an adaptive optimization vector, an intelligent elimination routine for non-used primaries or an outside gamut mapping. Even though the proposed control algorithm supports this large set of functionalities, overall hardware complexity and computational effort were kept low. The color control approach was in fact implemented on a simple μC and could potentially also be realized in dedicated hardware on an ASIC, e.g. by using the CORDIC algorithm realizing the QR decomposition.

This thesis eventually examined the developed color control algorithm in various simulation and measurement cycles for three different LED configurations, which are RGB-A, RGB-W and RGB-CAW. The simulations showed excellent performance results regarding CRI, ΔE and $\Delta u'v'$. The targeted specifications were met over the entire CT range from 2000 K to 7500 K, while a ΔCCT of less than ± 50 K was maintained. Only for CCTs below 3200 K

RGB-A and RGB-W did not achieve the aspired high CRI > 90. A simulation of the entire displayable gamut revealed that the color shift stayed well below the non-noticeable limits of $\Delta E < 1$ and $\Delta u'v' < 0.002$. In case of dimming, the investigations detected an expected worse performance, but the color shift remained mostly within acceptable tolerances of $\Delta E < 3$ and $\Delta u'v' < 0.0035$. The measurement results however showed a strong temperature dependence of emitted light color. Aiming to keep the LEDs at a quasi constant junction temperature, this thesis developed and applied an automated measurement routine. The measured color deviation resided mostly below the non-perceivable limit of $\Delta u'v' \leq 0.002$ or the acceptable limit of $\Delta u'v' \leq 0.0035$ for all LED configurations. Only for CCTs smaller than 3000 K higher deviations have been recorded. Similar results were obtained for angle dependent measurements and cases, in which dimming is applied. Regarding CRI, excellent results were measured in the CCT range from 2200 K to 3000 K. The RGB-CAW configuration realized measured CRI values between 92 and 96 in this region. This is an outstanding result considering that it is rather difficult to reach high CRIs in this CCT range, which is of high interest for (golden artefacts in) museum lighting applications. The measurement results further proved a strong influence of the blue LED on achievable CRI. This thesis substantiated that the deployment of a deep blue LED near the UV spectrum is demanded, if good color rendering with a CRI > 90 shall be realized for higher CCT values. In addition to that, extensive measurements over the entire displayable gamut were conducted. It was thereby observed that the measured color distance $\Delta u'v'$ strongly increased in close proximity to the LED primaries. To some extend this effect could be reproduced in simulations and is found to be correlated with the minimum on-time of the LED driving stage as well as with the settling time of the LED current flow. In conclusion, the proposed color control algorithm achieves excellent results in simulation and maintains very good color precision and outstanding CRI even under realistic measurement conditions. As expected, the six color RGB-CAW LED setup showed a superior performance regarding CRI and color shift $\Delta u'v'$. Due to the strong temperature dependency of the LEDs' emitted SPDs, this thesis confirms that a precise calibration of each LED primary in dependence of temperature, forward voltage and LED current is absolutely necessary to achieve high quality color rendering with minimum perceivable color shift. Therefore, it is suggested to employ some kind of closed loop mechanism regularly updating the x_i, y_i and Y_i parameters of each LED as a function of measurable quantities like LED forward voltage. Nevertheless, goal 4 has been fully accomplished and the developed color control technique is consequently found to be the basis for precise color rendering in high quality lighting systems.

7.1.3 Goal 5 & 6: Efficient and Precise LED Driving

To finally arrive at a tailored *"smart LED driver"*, goals 5 and 6 balance the efficiency requirements of the LED driving stage with achievable color quality determined by the minimum dimming level and LED current accuracy. Due to the linear relationship between average LED forward current and emitted luminance, excessive current ripples must be avoided under any circumstance to ensure good color stability. For this purpose, **chapter 5** applied a linear regulator adjusting LED current flow and improved its efficiency by introducing a digitally controlled dynamic headroom regulation based on an RDAC structure. It was ascertained that a digital control methodology applied to the dynamic headroom regulation process ensures better stability for the interdepending control loops, while increasing design flexibility regarding regulation speed and accuracy. To investigate the transient regulation behavior of the digital control approach, a suitable prototype implementation was realized using discrete components. This thesis thereby examined typical operational events of an LED driving stage, such as start-up behavior or long-term temperature induced effects. It was verified that the proposed concept reacts very precise, fast and stable, even under heavy load jumps caused by LED short circuit failures. This leads to significant efficiency improvements of the LED driving stage. The experimental investigations also discovered an undesired effect, which are large voltage dips of the LED supply voltage provoked by the rapid turn-on of the current regulator at the beginning of a PWM dimming sequence. In consequence of these voltage dips, the drain potential cannot be diminished any further, which leads to increased static losses in the linear current regulator. Finally, an overall peak efficiency of $\eta_{peak} = 93.9\,\%$ was measured for the entire LED driving stage including the consumption of a tiny μC, while the LED current flow deviation ΔI_{LED} is kept below 1.2 % with respect to its nominal target value. High efficiency and precise current regulation were maintained even over a large dimming range down to 20 %.

Although the achieved performance metrics represent an excellent result in contrast to existing solutions [237], it is expected to enhance efficiency even further by means of an ASIC implementation. **Chapter 6** therefore performed a conceptual study on a fully integrated *"smart LED driver"* and finally proved its feasibility in a 180 nm CMOS technology. After some minor modifications on the integrated DLT FW-RXs were briefly discussed, the major focus was set on innovative circuit concepts and control approaches improving the dynamic headroom controlled LED driving stage. A floating input range ADC as originally proposed by Schulte Bocholt [313] was realized to sense the LED supply voltage at relaxed hardware demands and lower circuit complexity.

The shown concept was identified to be applicable for the main converter control and proved to be useful for LED forward voltage measurements as needed in the color shift compensation techniques. The conducted study furthermore constituted a tremendous reduction of the voltage dips at turn-on, which is achieved by a better coordination of the dynamic headroom control and the LED current regulation. Aiming to further reduce overall power losses, this work conceived the so-called *"Current Replica (CR)"* sensing concept to dispense with the sense resistor in the LED current path and proposed an all-digital current controller in addition. While the concept was functionally working very well, its regulation speed was however determined to be too slow in order to keep the LED current ripple to a minimum. Employing a faster ADC circuit, e.g. a 4 bit flash ADC in a (three stage) pipeline structure with a subtracting current DAC in the CR sensing path, could be a promising solution balancing current consumption, speed and accuracy requirements. Finally, this thesis substantiated that the monolithic integration enables much faster switching speeds of the current regulator, which enhances the dimming ratio, increases the PWM frequency (avoiding flicker) and leads to a more precise turn-on and turn-off behavior. This measure is expected to improve perceivable color shift significantly and will likewise impact the quality of synthesized light. In the end, this thesis evaluates the power consumption of an ASIC solution and assesses overall peak efficiency of an integrated LED driver to 95.8 % taking parasitic contributions into account. All in all, chapter 6 highlights the enormous improvement and optimization potential of a fully integrated *"smart LED driver"* for tailored smart lighting systems.

7.1.4 Closing Remarks and Reflections on the Targeted Goals

Driven by its guiding research question this thesis tackled the major challenges of future lighting systems regarding energy efficiency, system intelligence and color quality. This work thus investigated, enhanced and optimized the core building blocks of a *"smart LED driver"* and thereby showed, how to tailor a lighting system with respect to specific needs. In this context, the major objective was to derive a balanced approach that achieves high energy-efficiency and accurate color control simultaneously, while providing substantial system intelligence. It is demonstrated, by which means and with what procedure the described conflict of aims can be overcome and thereby prepare a solid basis for HCL applications. Communication system, color control algorithm and LED driving stage were hence improved on circuit, component and system level. Furthermore, these core building blocks were designed in a flexible

Table 7.1: Summary of achieved performance in contrast to targeted benchmark.

Goal	Benchmark		Achieved Performance Metrics	
1	TER_{FW}	$\leq 1\,\%$	Analog BP filter	57 ppm
			Digital FIR filter	44 ppm
	$P_{FW\text{-}RX}$	$\leq 50\,\text{mW}$	Analog BP filter	37.72 mW ($\leq 6.5\,\text{mW}$)
			Digital FIR filter	25.73 mW ($\leq 7.2\,\text{mW}$)
2	η_{CD}	$\geq 50\,\%$	Flyback & Buck	63.7 % ($@P_{max} = 353\,\text{mW}$)
			Boost & Flyback	66.3 % ($@P_{max} = 389\,\text{mW}$)
3	TER_{REV}	$\leq 1\,\%$	Analog BP	114 ppm ($@I_{mod} = 45\,\text{mA}$)
			Matched Filter	322 ppm ($@I_{mod} = 28\,\text{mA}$)
			Transformer	5 ppm ($@I_{mod} = 10\,\text{mA}$)
	$P_{REV,total}$	$\leq 50\,\text{mW}$	Analog BP	72.57 mW
			Matched Filter	45.62 mW
			Transformer	25.77 mW
4	N_{LEDs}	≥ 4	flexibly deployable to all systems with 2-6 LEDs	
	CRI	≥ 90	RGB-CAW	always ≥ 90 in sim. and meas.
			RGB-A/W	≥ 90 for $CT \geq 3200\,\text{K}$ in sim. and meas.
	ΔE	≤ 3	All configuartions	≤ 1 in sim.
	$\Delta u'v'$	≤ 0.0035	All configuartions	$\ll 0.002$ in sim.
			All configuartions	≤ 0.0035 in meas. (mostly even ≤ 0.002)
5	DIM_{min}	$\leq 1\,\%$	$\leq 0.4\,\%$ with $t_{min,on} = 4\,\mu\text{s}$ and $f_{PWM} = 1\,\text{kHz}$	
	$\eta_{LED,DRV}$	$\geq 90\,\%$	$\geq 90\,\%$ down to $DIM = 30\,\%$ $\eta_{LED,DRV,max} = 93.9\,\%$	
	ΔI_{LED}	$\leq 3\,\%$	$\leq 1.2\,\%$ down to $DIM = 2\,\%$	
6	DIM_{min}	$\leq 1\,\%$	$0.02 - 0.4\,\%$ with $t_{min,on} = 200\,\text{ns}$ and $f_{PWM} = 1 - 20\,\text{kHz}$	
	$\eta_{LED,DRV}$	$\geq 95\,\%$	$\eta_{LED,DRV,max} = 95.8\,\%$ (calculated)	
	ΔI_{LED}	$\leq 3\,\%$	–	

manner so that they can be easily applied to other lighting systems. The gained insights, proposed control strategies, derived system concepts and developed circuit architectures thereby form the basis for future developments in HCL applications and other uses cases that require a high technical light quality, such as museum lighting. The set goals 1 to 6 served as a guideline during the optimization process and specified clear performance metrics that needed to be fulfilled. Tab. 7.1 eventually summarizes these targets in comparison to the realized achievements. Since all objectives were basically accomplished within this thesis, this work finally comes to a tailored system architecture for *"smart LED drivers"* in intelligent lighting systems.

7.2 Outlook

Since the outcome of this thesis can be applied to all kinds of lighting systems and applications, the developed approaches might become relevant and very useful in other scientific studies or industrial developments. Groundbreaking research, like investigations on the psychological and physiological effects of LED lighting on human behavior or the circadian rhythm, require reliable LED light sources with accurate color precision that are flexibly deployable. Moreover, the developed approaches for efficient and flexibly deployable electronics as well as the optimized system concept for an ASIC solution can be the starting point for an industrial exploitation and economic optimization of tailored *"smart LED drivers"*. In the course of the investigations conducted in this thesis, several other interesting aspects and new research questions emerged for each of the core building blocks. The following paragraphs therefore provide a brief outlook to possible future examinations and improvement measures.

Future Perspectives on Enhanced DLT Communication

While the FW modulation of DLT is now elaborately analyzed, the enhancements on tailored system intelligence leave further room for optimization and comparative studies. The proposed power supply topologies for DLT CDs could e.g. be monolithically integrated, which may enable further efficiency improvements, as the converters can be custom designed in this manner. If any RX circuit for bidirectional DLT is integrated as well onto the same die, further system optimizations can be realized regarding power consumption, robustness or costs. In addition to that, the proposed bidirectional communication approach may further lead to significant power savings on system level for the DLT methodology because a CD could send control commands in future implementations only once in a while instead of transmitting continuously

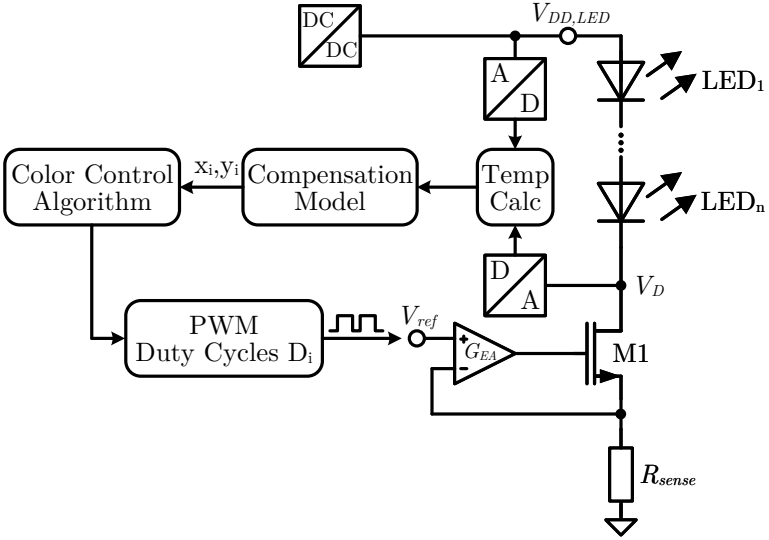


Figure 7.1: LED driver with digital dynamic headroom regulation and thermo-electrical model for color shift compensation.

by using a proper ARQ protocol. Of course, further optimization actions on circuit, component and system level are still conceivable, such as applying other modulation schemes or further tweaking the REV-RX circuits. Moreover, future research must define a suitable protocol stack in order to avoid channel access collision problems of attached CGs. Because the parallel connected CGs experience the *"hidden node problem"*, standard techniques like CSMA are not applicable to bidirectional DLT. Instead, it was briefly discussed, how the MACA protocol can be applied in combination with a similar scheme like classic *"ALOHA"* as originally proposed by de Vrieze [97].

Further Improvement Measures for Color Control Algorithm

The developed color control approach is a basic algorithm that can be deployed in any multi-color LED lighting system. The conceivable extensions, improvements and research opportunities are rather endless. Because the color of an LED varies strongly in dependence of the temperature, it would be very interesting to combine the developed color control strategy with a thermal-electrical modeling of employed LEDs as proposed in [338], [392]. Fig. 7.1 illustrates a possible implementation of this concept for the developed

LED driver with digital dynamic headroom regulation presented in chapter 5. Measuring the LED current flow as well as the LED forward voltage, a controller can conclude to the actual junction temperature and apply different x_i, y_i and Y_i parameters to the acting color computation algorithm. In this context, the monolithically integrated LED driving stage as presented in chapter 6 becomes very attractive as it measures and digitizes LED current flow and LED supply voltage anyways. Beyond that, it would be crucial to see how well the algorithm can handle other dimming schemes. While the developed approach maps its computed relative intensity distribution onto PWM duty cycles, it is generally conceivable to use other mapping routines for different dimming techniques. Thereby, it would be possible to apply the developed control algorithm also to amplitude modulation (AM), bilevel (BL) and hybrid based dimming systems with only minor adjustments.

Prospective Reflections on LED Driver and System Performance

Looking from a system perspective a monolithic ASIC implementation of a complete *"smart LED driver"* would be very beneficial as this realizes small form factors for intelligent luminaires, while maintaining high efficiency and precise color rendering. This guarantees a flexible deployment at low costs. For this purpose, the proposed concept of the HQLED chip can be further enhanced, particularly regarding the LED driving stage. It is thus suggested to use only one, maybe two switching pre-regulators for multiple LED strings. Although this measure decreases slightly the efficiency, it leads to huge savings in terms of die area. Beyond that, the CR sensing approach has not yet reached a sufficient maturity level. Further modifications are conceivable in terms of applying an analog or a mixed-signal control approach or improve the all-digital current controller with a faster ADC circuit as outlined earlier. Additionally, another aspect appears promising from a system point of view. Since the ASIC embeds a DLT FW-RX, it must be connected to mains voltage. Hence, the 50 Hz utility grid could be used as a reference input to generate a high frequency clock for the chip. Initial studies have already proven the feasibility of different concepts for this approach [188], [212], which is also compatible with the DLT communication methodology [188], [212].

In conclusion, this thesis proposed a tailored system architecture for *"smart LED drivers"* that is versatilely applicable to various use cases, application scenarios and intelligent lighting systems. The future perspectives on a vast deployment or further research studies on circuit, component and system level are hence promising.

Bibliography

[1] R. Abbasi-Kesbi, H. Memarzadeh-Tehran, and M. Deen, "Technique to estimate human reaction time based on visual perception", *Healthcare Techonolgy Letters*, May 2017. DOI: 10.1049/htl.2016.0106.

[2] N. Abramson, "The ALOHA system: another alternative for computer communications", in *Proceedings of the November 17-19, 1970, Fall Joint Computer Conference*, ser. AFIPS'70 (Fall), Houston, Texas: Association for Computing Machinery, Apr. 1970, pp. 281–285, ISBN: 9781450379045. DOI: 10.1145/1478462.1478502. Available online: https://doi.org/10.1145/1478462.1478502.

[3] V. Adivarahan *et al.*, "Ultraviolet light-emitting diodes at 340 nm using quaternary AlInGaN multiple quantum wells", *Applied Physics Letters*, vol. 79, no. 25, pp. 4240–4242, Dec. 2001. DOI: 10.1063/1.1425453. eprint: https://doi.org/10.1063/1.1425453. Available online: https://doi.org/10.1063/1.1425453.

[4] S. Aghaie *et al.*, "Design of a low-power calibratable charge-redistribution SAR ADC", in 10th *Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Jun. 2014, pp. 1–4. DOI: 10.1109/PRIME.2014.6872684.

[5] P. Almeida *et al.*, "An experimental study on the photometrical impacts of several current waveforms on power white LEDs", in 11th *Brazilian Power Electronics Conference*, Sep. 2011, pp. 728–733. DOI: 10.1109/COBEP.2011.6085242.

[6] P. Almeida *et al.*, "Matching LED and driver life spans: A review of different techniques", *IEEE Industrial Electronics Magazine*, vol. 9, no. 2, pp. 36–47, Jun. 2015, ISSN: 1941-0115. DOI: 10.1109/MIE.2014.2352861.

[7] P. Almeida *et al.*, "Static and dynamic photoelectrothermal modeling of LED lamps including low-frequency current ripple effects", *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3841–3851, Jul. 2015, ISSN: 1941-0107. DOI: 10.1109/TPEL.2014.2340352.

[8] M. Amirkhani *et al.*, "An energy efficient lighting design strategy to enhance visual comfort in offices with windows", *Energies*, vol. 10, p. 1126, Aug. 2017. DOI: 10.3390/en10081126.

[9] M. Arias *et al.*, "High-efficiency LED driver without electrolytic capacitor for street lighting", *IEEE Trans. Ind. Appl.*, vol. 49, no. 1, pp. 127–137, Jan. 2013, ISSN: 1939-9367. DOI: 10.1109/TIA.2012.2227644.

[10] M. Asadullah and A. Raza, "An overview of home automation systems", in 2th *International Conference on Robotics and Artificial Intelligence (ICRAI)*, Nov. 2016, pp. 27–31. DOI: 10.1109/ICRAI.2016.7791223.

[11] ATKearney and ZVEI and Lighting Europe, "Quantified benefits of human centric lighting", Apr. 2015, presentation slides. Available online: http://www.lightingeurope.org/.

[12] C. Bachmann *et al.*, "A 0.74V 200μW multi-standard transceiver digital baseband in 40nm LP-CMOS for 2.4GHz bluetooth smart / ZigBee / IEEE 802.15.6 personal area networks", in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2014, pp. 186–187. DOI: 10.1109/ISSCC.2014.6757393.

[13] N. Baker, "ZigBee and Bluetooth: Strengths and weaknesses for industrial applications", *Computing and Control Engineering*, vol. 16, pp. 20–25, Apr. 2005, ISSN: 0956-3385. Available online: https://digital-library.theiet.org/content/journals/10.1049/cce_20050204.

[14] S. Bannamas and P. Jirapong, "An intelligent lighting energy management system for commercial and residential buildings", in 5th *IEEE Innovative Smart Grid Technologies - Asia (ISGT ASIA)*, Nov. 2015, pp. 1–6. DOI: 10.1109/ISGT-Asia.2015.7386986.

[15] M. Barfuß and M. Kirsten, "Konzept und Aufbau einer 6-Kanal-Leuchte für die Produktbeleuchtung", in *6. Elektronik Lighting Congress*, Conference Presentation, in German, Jul. 2016.

[16] S. Barmada, M. Raugi, and M. Tucci, "Power line communication integrated in a wireless power transfer system: A feasibility study", in 18th *IEEE International Symposium on Power Line Communications and Its Applications (ISPLC 2014)*, Mar. 2014, pp. 116–120. DOI: 10.1109/ISPLC.2014.6812357.

[17] W. Bartenbach Christian und Witting, *Handbuch für Lichtgestaltung – Lichttechnische und wahrnehmungspsychologische Grundlagen*. Springer Verlag Wien New York, 2009, in German, ISBN: 978-3-211-75779-6.

[18] M. Bebendorf, *Einführung in die Numerische Mathematik*. University of Bonn, Sep. 2010, lecture manuscript fall 2010/2011, in German.

[19] S. Beczkowski and S. Munk-Nielsen, "LED spectral and power characteristics under hybrid PWM/AM dimming strategy", in 3rd *IEEE Energy Conversion Congress and Exposition (ECCE 2010)*, Oct. 2010, pp. 731–735. DOI: 10.1109/ECCE.2010.5617930.

[20] L. Bellia, A. Pedace, and G. Barbato, "Lighting in educational environments: An example of a complete analysis of the effects of daylight and electric light on occupants", *Building and Environment*, vol. 68, pp. 50–65, Apr. 2013, ISSN: 0360-1323. DOI: https://doi.org/10.1016/j.buildenv.2013.04.005. Available online: http://www.sciencedirect.com/science/article/pii/S0360132313001078.

[21] F. Bellido-Outeirino *et al.*, "Building lighting automation through the integration of DALI with wireless sensor networks", *IEEE Transactions on Consumer Electronics*, vol. 58, no. 1, pp. 47–52, Feb. 2012, ISSN: 1558-4127. DOI: 10.1109/TCE.2012.6170054.

[22] V. Bender *et al.*, "Experimental evaluation of current waveform on OLED photometric performance", in 51th *IEEE Industry Applications Society Annual Meeting*, Oct. 2016, pp. 1–8. DOI: 10.1109/IAS.2016.7731897.

[23] K. Benke and K. Benke, "Uncertainty in health risks from artificial lighting due to disruption of circadian rhythm and melatonin secretion: A review", *Human and Ecological Risk Assessment: An International Journal*, vol. 19, no. 4, pp. 916–929, Feb. 2013. DOI: 10.1080/10807039.2012.702608. Available online: https://doi.org/10.1080/10807039.2012.702608.

[24] A. Bensky, *Short-range Wireless Communication - Fundamentals of RF System Design and Application*, 2nd Edition. Newnes, Elsevier Inc., 2004.

[25] E. Bernhofer *et al.*, "Hospital lighting and its association with sleep, mood and pain in medical inpatients", *Journal of advanced nursing*, vol. 70, Oct. 2013. DOI: 10.1111/jan.12282.

[26] F. Bernitz, O. Schallmoser, and W. Sowa, "Advanced electronic driver for power LEDs with integrated colour management", in *Conference Record of the 2006 IEEE Industry Applications Conference,* 41th *IAS Annual Meeting*, vol. 5, Oct. 2006, pp. 2604–2607. DOI: 10.1109/IAS.2006.256906.

[27] P. Bertoldi, B. Hirl, and N. Labanca, *Energy Efficiency Status Report 2012 – Electricity Consumption and Efficiency Trends in the EU-27*. JRC Scientific and Policy Reports, 2012. DOI: 10.2788/37564. Available online: https://setis.ec.europa.eu/sites/default/files/reports/energy-efficiency-status-report-2012.pdf.

[28] D. Bertozzi, L. Benini, and G. De Micheli, "Error control schemes for on-chip communication links: the energy-reliability tradeoff", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 6, pp. 818–831, Jun. 2005, ISSN: 1937-4151. DOI: 10.1109/TCAD.2005.847907.

[29] K. Blankenbach, F. Hertlein, and S. Hoffmann, "Advances in automotive interior lighting", *Symposium Digest of Technical Papers SID*, vol. 50, pp. 176–179, Jun. 2019. DOI: 10.1002/sdtp.12884.

[30] K. Blankenbach and R. Isele, "Automotive interior lighting – Challenges and solutions for uniformity", *Symposium Digest of Technical Papers SID*, vol. 50, pp. 618–621, Jul. 2019. DOI: 10.1002/sdtp.13589.

[31] U. Blaszczak *et al.*, "Color mixing in LED illuminating system for endoscopic purposes", Sep. 2016, pp. 1–6. DOI: 10.1109/LUMENV.2016.7745522.

[32] M. Blom *et al.*, "Bluetooth energy characteristics in wireless sensor networks", in 3rd *International Symposium on Wireless Pervasive Computing*, May 2008, pp. 198–202. DOI: 10.1109/ISWPC.2008.4556196.

[33] *Bluetooth core specification – version 5.1*, pp. 1-2985, Bluetooth SIG, Jan. 2019. Available online: https://www.bluetooth.com/specifications/.

[34] H. Bodmann and M. La Toison, "Predicted brightness-luminance phenomena", *International Journal of Lighting Research and Technology*, vol. 26, no. 3, pp. 135–143, Jun. 1994. DOI: 10.1177/096032719402600302. Available online: https://doi.org/10.1177/096032719402600302.

[35] *Booklet of CS-20000 spectroradiometer – High-End spectroradiometer with high accuracy and high stability*, 9242-AOE3-41, Konica Minolata, 2007. Available online: https:/konicaminolta.com/instruments/network.

[36] A. Borisuit *et al.*, "Effects of realistic office daylighting and electric lighting conditions on visual comfort, alertness and mood", *Lighting Research and Technology*, vol. 47, pp. 192–209, Mar. 2014. DOI: 10.1177/1477153514531518.

[37] L. Boroumand *et al.*, "A review of technique to resolve the hidden node problem in wireless networks", *Smart Computing Review*, vol. 2, no. 2, Apr. 2012.

[38] P. Boyce, *Human Factors in Lighting*, 3rd Edition. CRC Press, Tylor & Francis Group, 2014, ISBN: 978-1-4398-7489-9.

[39] P. Boyce, "Review: The impact of light in buildings on human health", *Indoor and Built Environment*, vol. 19, no. 1, pp. 8–20, Sep. 2010. DOI: 10.1177/1420326X09358028. Available online: https://doi.org/10.1177/1420326X09358028.

[40] C. Branas, F. Azcondo, and J. Alonso, "Solid-state lighting: A system review", *IEEE Industrial Electronics Magazine*, vol. 7, no. 4, pp. 6–14, Dec. 2013, ISSN: 1941-0115. DOI: 10.1109/MIE.2013.2280038.

[41] G. Breed, "Bit error rate: fundamental concepts and measurement issues", *High Frequency Electronics*, vol. 2, no. 1, pp. 46–48, Jan. 2003.

[42] R. Bucy, "Optimal filtering for correlated noise", *Journal of Mathematical Analysis and Applications*, vol. 20, no. 1, pp. 1–8, Oct. 1967, ISSN: 0022-247X. DOI: https://doi.org/10.1016/0022-247X(67)90101-1. Available online: http://www.sciencedirect.com/science/article/pii/0022247X67901011.

[43] J. Bullough, "Human factors impacts of light-emitting diode airfield lighting", *Transportation Research Record*, vol. 2626, no. 1, pp. 51–57, Jan. 2017. DOI: 10.3141/2626-07. eprint: https://doi.org/10.3141/2626-07. Available online: https://doi.org/10.3141/2626-07.

[44] G. Bumiller, L. Lampe, and H. Hrasnica, "Power line communication networks for large-scale control and automation systems", *IEEE Communications Magazine*, vol. 48, no. 4, pp. 106–113, Apr. 2010, ISSN: 1558-1896. DOI: 10.1109/MCOM.2010.5439083.

[45] S. Buso and G. Spiazzi, "White light solid state lamp with luminance and color temperature control", in 11th *Brazilian Power Electronics Conference*, Sep. 2011, pp. 837–843. DOI: 10.1109/COBEP.2011.6085167.

[46] J. Byun *et al.*, "An intelligent self-adjusting sensor for smart home services based on ZigBee communications", *IEEE Transactions on Consumer Electronics*, vol. 58, no. 3, pp. 794–802, Aug. 2012, ISSN: 1558-4127. DOI: 10.1109/TCE.2012.6311320.

[47] L. Caberletti *et al.*, "Influence of ambient lighting in a vehicle interior on the driver's perceptions", *Lighting Research & Technology*, vol. 42, no. 3, pp. 297–311, Jan. 2010. DOI: 10.1177/1477153510370554. Available online: https://doi.org/10.1177/1477153510370554.

[48] Y. Cai *et al.*, "Low-flicker lighting from high-voltage LEDs driven by a single converter-free driver", *IEEE Photonics Technology Letters*, vol. 29, no. 19, pp. 1675–1678, Oct. 2017, ISSN: 1941-0174. DOI: 10.1109/LPT.2017.2742861.

[49] D. Caicedo and A. Pandharipande, "Distributed illumination control with local sensing and actuation in networked lighting systems", *IEEE Sensors Journal*, vol. 13, no. 3, pp. 1092–1104, Mar. 2013, ISSN: 2379-9153. DOI: 10.1109/JSEN.2012.2228850.

[50] D. Caicedo, A. Pandharipande, and F. Willems, "Daylight-adaptive lighting control using light sensor calibration prior-information", *Energy and Buildings*, vol. 73, pp. 105–114, Apr. 2014, ISSN: 0378-7788. DOI: https://doi.org/10.1016/j.enbuild.2014.01.022. Available online: http://www.sciencedirect.com/science/article/pii/S0378778814000607.

[51] A. Cailean *et al.*, "Evaluation of the noise effects on visible light communications using Manchester and Miller coding", in 12th *International Conference on Development and Application Systems (DAS)*, May 2014, pp. 85–89. DOI: 10.1109/DAAS.2014.6842433.

[52] C. Cajochen *et al.*, "Effect of daylight LED on visual comfort, melatonin, mood, waking performance and sleep", *Lighting Research & Technology*, vol. 51, no. 7, pp. 1044–1062, Jan. 2019. DOI: 10.1177/1477153519828419. Available online: https://doi.org/10.1177/1477153519828419.

[53] E. Callaway *et al.*, "Home networking with IEEE 802.15.4: a developing standard for low-rate wireless personal area networks", *IEEE Communications Magazine*, vol. 40, no. 8, pp. 70–77, Aug. 2002, ISSN: 1558-1896. DOI: 10.1109/MCOM.2002.1024418.

[54] C. Cano *et al.*, "State of the art in power line communications: From the applications to the medium", *IEEE Journal on Selected Areas in Communications*, vol. 34, no. 7, pp. 1935–1952, Jul. 2016, ISSN: 1558-0008. DOI: 10.1109/JSAC.2016.2566018.

[55] F. Cao *et al.*, "Effects of flicker on vision in LED light source dimming control process", in 32th *IET International Conference on Communication Technology and Application (ICCTA 2011)*, vol. 2011, Jan. 2011, pp. 930–933. DOI: 10.1049/cp.2011.0806.

[56] J. Castellanos, M. Turhan, and E. Cantatore, "A 93.3% peak-efficiency self-resonant hybrid-switched-capacitor LED driver in 0.18 μm CMOS technology", *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 1924–1935, Jul. 2018, ISSN: 1558-173X. DOI: 10.1109/JSSC.2018.2828097.

[57] I. Castro *et al.*, "A review on flicker-free AC–DC LED drivers for single-phase and three-phase AC power grids", *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 10 035–10 057, Oct. 2019, ISSN: 1941-0107. DOI: 10.1109/TPEL.2018.2890716.

[58] M. Chakrabarti *et al.*, "A color management system for multi-colored LED lighting", in 14th *International Conference on Solid State Lighting and LED-based Illumination Systems*, M. H. Kane *et al.*, Eds., International Society for Optics and Photonics, vol. 9571, SPIE, Aug. 2015, pp. 43–51. DOI: 10.1117/12.2188427. Available online: https://doi.org/10.1117/12.2188427.

[59] M. Chakrabarti *et al.*, "A white-cyan-red LED lighting system for low correlated color temperature", *Lighting Research and Technology*, Aug. 2015. DOI: 10.1177/1477153515608416.

[60] R. Chang *et al.*, "Iterative QR decomposition architecture using the modified gram-schmidt algorithm for MIMO systems", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 5, pp. 1095–1102, May 2010, ISSN: 1558-0806. DOI: 10.1109/TCSI.2010.2047744.

[61] G. Chau *et al.*, "Experimental verification of the linear current transformer model", in 18th *Australasian Universities Power Engineering Conference (AUPEC 2008)*, Dec. 2008, pp. 1–6.

[62] C. Chen *et al.*, "Sequential color LED backlight driving system for LCD panels", *IEEE Transactions on Power Electronics*, vol. 22, no. 3, pp. 919–925, May 2007, ISSN: 1941-0107. DOI: 10.1109/TPEL.2007.897001.

[63] D. Chen and M. Sima, "Fixed-point CORDIC-based QR decomposition by Givens rotations on FPGA", in *International Conference on Reconfigurable Computing and FPGAs (ReConFig 2011)*, Nov. 2011, pp. 327–332. DOI: 10.1109/ReConFig.2011.38.

[64] H. Chen, Y. Zhang, and D. Ma, "A SIMO parallel-string driver IC for dimmable LED backlighting with local bus voltage optimization and single time-shared regulation loop", *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 452–462, Jan. 2012, ISSN: 1941-0107. DOI: 10.1109/TPEL.2011.2160404.

[65] H. Chen, C. Hsu, and H. Hong, "InGaN-CdSe-ZnSe quantum dots white LEDs", *IEEE Photonics Technology Letters*, vol. 18, no. 1, pp. 193–195, Jan. 2006, ISSN: 1941-0174. DOI: 10.1109/LPT.2005.859540.

[66] H. Chen, S. Tan, and S. Hui, "Nonlinear dimming and correlated color temperature control of bicolor white LED systems", *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6934–6947, Dec. 2015, ISSN: 1941-0107. DOI: 10.1109/TPEL.2014.2384199.

[67] H. Chen *et al.*, "Precise color control of red-green-blue light-emitting diode systems", *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3063–3074, Apr. 2017, ISSN: 1941-0107. DOI: 10.1109/TPEL.2016.2581828.

[68] H. Chen and S. Hui, "Dynamic prediction of correlated color temperature and color rendering index of phosphor-coated white light-emitting diodes", *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 784–797, Feb. 2014, ISSN: 1557-9948. DOI: 10.1109/TIE.2013.2251736.

[69] K. Chen and N. Chen, "A new method for power current measurement using a coreless Hall effect current transformer", *IEEE Transactions on Instrumentation and Measurement*, vol. 60, no. 1, pp. 158–169, Jan. 2011, ISSN: 1557-9662. DOI: 10.1109/TIM.2010.2049234.

[70] W. Chen and S. Hui, "Elimination of an electrolytic capacitor in AC/DC light-emitting diode (LED) driver with high input power factor and constant output current", *Power Electronics, IEEE Transactions on*, vol. 27, no. 3, pp. 1598–1607, Mar. 2012, ISSN: 0885-8993. DOI: 10.1109/TPEL.2010.2103959.

[71] L. Cheng *et al.*, "On-chip compensated wide output range boost converter with fixed-frequency adaptive off-time control for LED driver applications", *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2096–2107, Apr. 2015, ISSN: 1941-0107. DOI: 10.1109/TPEL.2014.2326257.

[72] I. Chew *et al.*, "A spectrally tunable smart LED lighting system with closed-loop control", *IEEE Sensors Journal*, vol. 16, no. 11, pp. 4452–4459, Jun. 2016, ISSN: 2379-9153. DOI: 10.1109/JSEN.2016.2542265.

[73] C. Chiu and K. Chen, "A high accuracy current-balanced control technique for LED backlight", in 39th *IEEE Power Electronics Specialists Conference*, Jun. 2008, pp. 4202–4206. DOI: 10.1109/PESC.2008.4592615.

[74] H. Chiu *et al.*, "A high-efficiency dimmable LED driver for low-power lighting applications", *IEEE Transactions on Industrial Electronics*, vol. 57, no. 2, pp. 735–743, Feb. 2010, ISSN: 1557-9948. DOI: 10.1109/TIE.2009.2027251.

[75] S. Choi and T. Kim, "Symmetric current-balancing circuit for LED backlight with dimming", *IEEE Transactions on Industrial Electronics*, vol. 59, no. 4, pp. 1698–1707, Apr. 2012, ISSN: 1557-9948. DOI: 10.1109/TIE.2011.2138112.

[76] H. Chou, Y. Hwang, and J. Chen, "An adaptive output current estimation circuit for a primary-side controlled LED driver", *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4811–4819, Oct. 2013, ISSN: 1941-0107. DOI: 10.1109/TPEL.2012.2236581.

[77] Class for Physics, Royal Swedish Academy of Sciences, "Efficient blue light emitting diodes leading to bright and energy-saving white light sources", *Scientific Background on the Nobel Prize in Physics 2014*, pp. 1–9, Oct. 2014. Available online: http://kva.se.

[78] M. Collotta and G. Pau, "A novel energy management approach for smart homes using Bluetooth Low Energy", *IEEE Journal on Selected Areas in Communications*, vol. 33, no. 12, pp. 2988–2996, Dec. 2015, ISSN: 1558-0008. DOI: 10.1109/JSAC.2015.2481203.

[79] B. Cook, "New developments and future trends in high-efficiency lighting", *Engineering Science and Education Journal*, vol. 9, no. 5, pp. 207–217, Oct. 2000, ISSN: 0963-7346. DOI: 10.1049/esej:20000504.

[80] C. Cordova *et al.*, "Overview and comparison of leading communication standard technologies for smart home area networks enabling energy management systems", in 46th *International Universities' Power Engineering Conference (UPEC)*, Sep. 2011, pp. 1–6.

[81] L. Corradini and G. Spiazzi, "A high-frequency digitally controlled LED driver for automotive applications with fast dimming capabilities", *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6648–6659, Dec. 2014, ISSN: 1941-0107. DOI: 10.1109/TPEL.2014.2304776.

[82] M. Craford *et al.*, "Radiative recombination mechanisms in GaAsP diodes with and without nitrogen doping", *Journal of Applied Physics*, vol. 43, no. 10, pp. 4075–4083, May 1972. DOI: 10.1063/1.1660876. Available online: https://doi.org/10.1063/1.1660876.

[83] M. Crawford, "LEDs for solid-state lighting: performance challenges and recent advances", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 15, no. 4, pp. 1028–1040, Jul. 2009, ISSN: 1558-4542. DOI: 10.1109/JSTQE.2009.2013476.

[84] D. Cupkova *et al.*, "Intelligent human-centric lighting for mental wellbeing improvement", *International Journal of Distributed Sensor Networks*, vol. 15, no. 9, Sep. 2019. DOI: 10.1177/1550147719875878. Available online: https://doi.org/10.1177/1550147719875878.

[85] G. Curcio *et al.*, "LED lighting effect on sleep, sleepiness, mood and vigor", in 16th *International Conference on Environment and Electrical Engineering (EEEIC)*, Jun. 2016, pp. 1–5. DOI: 10.1109/EEEIC.2016.7555791.

[86] B. Dai *et al.*, "All-optical modulation format conversion from NRZ-OOK to PSK-Manchester using SOA-MZI", *Electronics Letters*, vol. 48, no. 19, pp. 1221–1222, Sep. 2012, ISSN: 0013-5194. DOI: 10.1049/el.2012.2095.

[87] DALI AG, *Dali manual*, ZVEI-Division Luminaires, 2001.

[88] S. Danbatta and A. Varol, "Comparison of Zigbee, Z-Wave, Wi-Fi, and Bluetooth wireless technologies used in home automation", in 7th *International Symposium on Digital Forensics and Security (ISDFS)*, Jun. 2019, pp. 1–5. DOI: 10.1109/ISDFS.2019.8757472.

[89] R. Dang *et al.*, "Illumination in museums: four-primary white LEDs to optimize the protective effect and color quality", *IEEE Photonics Journal*, vol. 11, no. 1, pp. 1–15, Feb. 2019, ISSN: 1943-0647. DOI: 10.1109/JPHOT.2019.2893822.

[90] H. Dange and V. Gondi, "Powerline communication based home automation and electricity distribution system", in *International Conference on Process Automation, Control and Computing (PACC 2011)*, Jul. 2011, pp. 1–6. DOI: 10.1109/PACC.2011.5978900.

[91] N. Das and M. Kazimierczuk, "An overview of technical challenges in the design of current transformers", in *Proceedings Electrical Insulation Conference and Electrical Manufacturing Expo, 2005.*, Oct. 2005, pp. 369–377. DOI: 10.1109/EEIC.2005.1566323.

[92] A. David *et al.*, "Development of the IES method for evaluating the color rendition of light sources", *Opt. Express*, vol. 23, no. 12, pp. 15 888–15 906, Jun. 2015. DOI: 10.1364/OE.23.015888. Available online: http://www.opticsexpress.org/abstract.cfm?URI=oe-23-12-15888.

[93] W. Davis, "Measuring color quality of light sources", in 6th *International Conference on Solid State Lighting*, I. T. Ferguson *et al.*, Eds., International Society for Optics and Photonics, vol. 6337, SPIE, Sep. 2006, pp. 89–98. DOI: 10.1117/12.685187. Available online: https://doi.org/10.1117/12.685187.

[94] W. Davis and Y. Ohno, "Development of a color quality scale", *Proc.* 6th *International LRO Lighting Research Symposium*, Feb. 2006.

[95] A. de Beer *et al.*, "Effects of LED lamps on the power-line communications channel", in 17th *IEEE International Symposium on Power Line Communications and Its Applications (ISPLC 2013)*, 2013, pp. 209–213.

[96] K. de Craemer and G. Deconinck, "Analysis of state-of-the-art smart metering communication standards", eng, 2010.

[97] C. de Vrieze, "Design and implementation of a bidirectional power line communication system for intelligent illumination systems", Supervisor: Lukas Lohaus, Bachelor's Thesis, Integrated Analog Circuits and RF Systems, RWTH Aachen University, Sep. 2015.

[98] A. Dementyev *et al.*, "Power consumption analysis of Bluetooth Low Energy, ZigBee and ANT sensor nodes in a cyclic sleep scenario", in 1st *IEEE International Wireless Symposium (IWS 2013)*, Apr. 2013, pp. 1–4. DOI: 10.1109/IEEE-IWS.2013.6616827.

[99] P. Deurenberg *et al.*, "Achieving color point stability in RGB multi-chip LED modules using various color control loops", *Proceedings of SPIE - The International Society for Optical Engineering*, vol. 5941, Aug. 2005. DOI: 10.1117/12.623020.

[100] J. Diaz *et al.*, "CAN bus embedded system for lighting network applications", in 51st *Midwest Symposium on Circuits and Systems*, Aug. 2008, pp. 531–534. DOI: 10.1109/MWSCAS.2008.4616853.

[101] G. Dickmann, "Digitalstrom™: a centralized PLC topology for home automation and energy management", in 15th *IEEE International Symposium on Power Line Communications and Its Applications (ISPLC 2011)*, Apr. 2011, pp. 352–357. DOI: 10.1109/ISPLC.2011.5764421.

[102] S. Dietrich *et al.*, "12.4 A 7.5W-output-power 96%-efficiency capacitor-free single-inductor 4-channel all-digital integrated DC-DC LED driver in a 0.18μm technology", in *IEEE International Solid-State Circuits Conference - (ISSCC 2015) Digest of Technical Papers*, Feb. 2015, pp. 1–3. DOI: 10.1109/ISSCC.2015.7063005.

[103] S. Dietrich *et al.*, "A low power high-side current sense SAR ADC for automotive applications", in 40th *Annual Conference of the IEEE Industrial Electronics Society (IECON 2014)*, Oct. 2014, pp. 2921–2926. DOI: 10.1109/IECON.2014.7048924.

[104] S. Dietrich *et al.*, "An innovative integration technique of a capacitor-free single-inductor, multiple-output LED driver", *IEEE Industrial Electronics Magazine*, vol. 9, no. 2, pp. 50–53, May 2015, ISSN: 1941-0115. DOI: 10.1109/MIE.2014.2382251.

[105] S. Dietrich *et al.*, "Get the LED out: Experimental validation of a capacitor-free single-inductor, multiple-output LED driver topology", *IEEE Industrial Electronics Magazine*, vol. 9, no. 2, pp. 24–35, May 2015, ISSN: 1941-0115. DOI: 10.1109/MIE.2014.2357091.

[106] *Digital load side transmission lighting control (DLT) – part 1: basic requirements*, 62756-1, International Standard, International Electrotechnical Commission (IEC), May 2015.

[107] B. Dokic, "CMOS schmitt triggers", *IEEE Proceedings G - Electronic Circuits and Systems*, vol. 131, no. 5, pp. 197–202, Oct. 1984, ISSN: 0143-7089. DOI: 10.1049/ip-g-1.1984.0037.

[108] F. Domingo-Perez *et al.*, "Lighting control system based on DALI and wireless sensor networks", in 3rd *IEEE PES Innovative Smart Grid Technologies (ISGT)*, Jan. 2012, pp. 1–6. DOI: 10.1109/ISGT.2012.6175666.

[109] M. Doshi and R. Zane, "Digital architecture for driving large LED arrays with dynamic bus voltage regulation and phase shifted PWM", in 22nd *Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2007)*, Feb. 2007, pp. 287–293. DOI: 10.1109/APEX.2007.357528.

[110] C. Duke and N. Holonyak, "Advances in light-emitting diodes", *Phys. Today*, vol. 26, pp. 23–31, 1973.

[111] M. Dyble *et al.*, "Impact of dimming white LEDs: Chromaticity shifts due to different dimming methods", *Proceedings of SPIE - The International Society for Optical Engineering*, vol. 5941, pp. 291–299, Aug. 2005. DOI: 10.1117/12.625924.

[112] *Energy efficiency market report 2016*, International Energy Agency (IEA), 2016. Available online: www.iea.org.

[113] R. Englert, "digitalSTROM. So funktioniert's. – Die nachrüstbare, zukunftsweisende Vernetzungstechnologie.", de – das elektrohandwerk, Tech. Rep., Sep. 2014, in German. Available online: https://www.digitalstrom.com/out/media/document/2014_9_digitalSTROM_Sonderdruck_DE_Version_Schweiz.pdf.

[114] T. Erdem and H. Demir, *Color Science and Photometry for Lighting with LEDs and Semiconductor Nanocrystals*, 1st Edition, H. V. Demir and A. O. Govorov, Eds. SpringerBriefs in Applied Sciences, Technology – Nanoscience, and Nanotechnology, 2019. DOI: 10.1007/978-981-13-5886-9.

[115] C. Evans-Pughe, "Bzzzz zzz [zigbee wireless standard]", *IEE Review*, vol. 49, no. 3, pp. 28–31, Mar. 2003, ISSN: 0953-5683. DOI: 10.1049/ir:20030303.

[116] S. Fernandes, J. Esteves, and R. Simoes, "Characteristics and human factors of older drivers: Improvement opportunities in automotive interior design", *International Journal of Vehicle Design*, vol. 74, p. 167, Jan. 2017. DOI: 10.1504/IJVD.2017.086418.

[117] H. Ferreira *et al.*, "Power line communications: An overview", in *Proceedings of IEEE. AFRICON 1996*, vol. 2, Sep. 1996, pp. 558–563. DOI: 10.1109/AFRCON.1996.562949.

[118] E. Ferro and F. Potorti, "Bluetooth and Wi-Fi wireless protocols: A survey and a comparison", *IEEE Wireless Communications*, vol. 12, no. 1, pp. 12–26, Feb. 2005, ISSN: 1558-0687. DOI: 10.1109/MWC.2005.1404569.

[119] M. Figueiro, R. Nagare, and L. Price, "Non-visual effects of light: How to use light to promote circadian entrainment and elicit alertness", *Lighting Research & Technology*, vol. 50, no. 1, pp. 38–62, Jan. 2018. DOI: 10.1177/1477153517721598. Available online: https://doi.org/10.1177/1477153517721598.

[120] L. Frenzel Jr., *Principles of Electronic Communication Systems*, 4th Edition. Mc Graw Hill Education, 2016.

[121] T. Fukaya, Y. Yamamoto, and S. Zhang, "A dynamic programming approach to optimizing the blocking strategy for the Householder QR decomposition", in *2008 IEEE International Conference on Cluster Computing*, Sep. 2008, pp. 402–410. DOI: 10.1109/CLUSTR.2008.4663801.

[122] J. Garcia *et al.*, "Interleaved buck converter for fast PWM dimming of high-brightness LEDs", *IEEE Transactions on Power Electronics*, vol. 26, no. 9, pp. 2627–2636, Sep. 2011, ISSN: 1941-0107. DOI: 10.1109/TPEL.2011.2121922.

[123] T. Gemmeke, M. Gansen, and T. Noll, "Implementation of scalable power and area efficient high-throughput Viterbi decoders", *IEEE Journal of Solid-State Circuits*, vol. 37, no. 7, pp. 941–948, Jul. 2002, ISSN: 1558-173X. DOI: 10.1109/JSSC.2002.1015694.

[124] T. Gemmeke *et al.*, "Design optimization of low-power high-performance DSP building blocks", *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1131–1139, Jul. 2004, ISSN: 1558-173X. DOI: 10.1109/JSSC.2004.829395.

[125] K. Gill *et al.*, "A ZigBee-based home automation system", *IEEE Transactions on Consumer Electronics*, vol. 55, no. 2, pp. 422–430, May 2009, ISSN: 1558-4127. DOI: 10.1109/TCE.2009.5174403.

[126] *Good lighting for museums, galleries and exhibitions*, Fördergemeinschaft Gutes Licht, 2016.

[127] P. Goravanchi, R. Wunderlich, and S. Heinen, "Capacitively divided an on-chip AC/DC converter with no-load over-voltage protection", in 8th *Conference on Ph.D. Research in Microelectronics & Electronics (PRIME)*, Jun. 2012, pp. 71–74.

[128] M. Götz, M. Rapp, and K. Dostert, "Power line channel characteristics and their effect on communication system design", *IEEE Communications Magazine*, vol. 42, no. 4, pp. 78–86, Apr. 2004, ISSN: 1558-1896. DOI: 10.1109/MCOM.2004.1284933.

[129] W. Granzer, W. Kastner, and C. Reinisch, "Gateway-free integration of BACnet and KNX using multi-protocol devices", in 6th *IEEE International Conference on Industrial Informatics*, Jul. 2008, pp. 973–978. DOI: 10.1109/INDIN.2008.4618243.

[130] F. Greenfeld and K. Shum, "Control of LED luminaires - An overview of competing wired and wireless standards", in 13th *China International Forum on Solid State Lighting (SSLChina 2016)*, Nov. 2016, pp. 83–89. DOI: 10.1109/SSLCHINA.2016.7804357.

[131] G. Grice, R. Nullmeyer, and J. Schnizlein, "Variable criterion analysis of brightness eeffect in simple reaction time", *Journal of Experimental Psychology: Human Perception and Performance*, vol. 5, no. 2, pp. 303–314, Jun. 1979.

[132] Y. Gu *et al.*, "Spectral and luminous efficacy change of high-power LEDs under different dimming methods", in 6th *International Conference on Solid State Lighting*, I. T. Ferguson *et al.*, Eds., International Society for Optics and Photonics, vol. 6337, SPIE, Sep. 2006, pp. 78–84. DOI: 10.1117/12.680531. Available online: https://doi.org/10.1117/12.680531.

[133] V. Gungor *et al.*, "A survey on smart grid potential applications and communication requirements", *IEEE Transactions on Industrial Informatics*, vol. 9, no. 1, pp. 28–42, Feb. 2013, ISSN: 1941-0050. DOI: 10.1109/TII.2012.2218253.

[134] V. Gungor *et al.*, "Smart grid technologies: Communication technologies and standards", *IEEE Transactions on Industrial Informatics*, vol. 7, no. 4, pp. 529–539, Nov. 2011, ISSN: 1941-0050. DOI: 10.1109/TII.2011.2166794.

[135] W. Guo, W. Healy, and M. Zhou, "An experimental study of interference impacts on ZigBee-based wireless communication inside buildings", in 2nd *IEEE International Conference on Mechatronics and Automation (ICMA 2010)*, Aug. 2010, pp. 1982–1987. DOI: 10.1109/ICMA.2010.5589256.

[136] D. Han and J. Lim, "Design and implementation of smart home energy management systems based on ZigBee", *IEEE Transactions on Consumer Electronics*, vol. 56, no. 3, pp. 1417–1425, Aug. 2010, ISSN: 1558-4127. DOI: 10.1109/TCE.2010.5606278.

[137] I. Han *et al.*, "An integrated home server for communication, broadcast reception, and home automation", *IEEE Transactions on Consumer Electronics*, vol. 52, no. 1, pp. 104–109, Feb. 2006, ISSN: 1558-4127. DOI: 10.1109/TCE.2006.1605033.

[138] M. Hanhart *et al.*, "A 16.5 W single-inductor 4-channel multi-color output DC-DC buck LED driver with digital control and 96% efficiency", in 44th *IEEE European Solid State Circuits Conference (ESSCIRC 2018)*, Sep. 2018, pp. 118–121. DOI: 10.1109/ESSCIRC.2018.8494324.

[139] P. Haubner, *Zur Helligkeitsbewertung quasi-achromatischer Reize*. Schadel, 1977, in German.

[140] B. Hawes *et al.*, "Effects of four workplace lighting technologies on perception, cognition and affective state", *International Journal of Industrial Ergonomics*, vol. 42, no. 1, pp. 122–128, Jan. 2012, ISSN: 0169-8141. DOI: https://doi.org/10.1016/j.ergon.2011.09.004. Available online: http://www.sciencedirect.com/science/article/pii/S0169814111001193.

[141] J. He, X. Ruan, and L. Zhang, "Adaptive voltage control for bidirectional converter in flicker-free electrolytic capacitor-less AC-DC LED driver", *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 320–324, Jan. 2017, ISSN: 1557-9948. DOI: 10.1109/TIE.2016.2608767.

[142] P. Hein, "DALI - A digital addressable lighting interface for lighting electronics", in *Conference Record of the 2001 IEEE Industry Applications Conference.* 36th *IAS Annual Meeting (Cat. No.01CH37248)*, vol. 2, Sep. 2001, pp. 901–905. DOI: 10.1109/IAS.2001.955559.

[143] S. Heinle, *Heimautomation mit KNX, DALI 1-Wire und Co. - Das umfassende Handbuch*. Rheinwerk Verlag, Nov. 2015, in German.

[144] J. Hernández-Andrés, R. Lee, and J. Romero, "Calculating correlated color temperatures – Across the entire gamut of daylight and skylight chromaticities", *Applied optics*, vol. 38, Oct. 1999. DOI: 10.1364/AO.38.005703.

[145] J. Hiltunen, "Accurate color measurement", Phd Thesis, University of Jensuu, Department of Physics Väisälä Laboratory, Feb. 2002, ISBN: 952-458-077-2.

[146] C. Hoelen *et al.*, "Multi-chip color variable LED spot modules", in 5th *International Conference on Solid State Lighting*, I. T. Ferguson *et al.*, Eds., International Society for Optics and Photonics, vol. 5941, SPIE, Sep. 2005, pp. 51–62. DOI: 10.1117/12.623010. Available online: https://doi.org/10.1117/12.623010.

[147] N. Holonyak and S. Bevacqua, "Coherent (visible) light emission from Ga (As1-x Px) junctions", *Applied Physics Letters*, vol. 1, no. 4, pp. 82–83, 1962. DOI: 10.1063/1.1753706. Available online: https://doi.org/10.1063/1.1753706.

[148] D. Holzman, "What's in a color? The unique human health effects of blue light", *Environmental health perspectives*, vol. 118, A22–7, Jan. 2010. DOI: 10.1289/ehp.118-a22.

[149] C. Hsieh *et al.*, "Efficienct LED driver with an adaptive reference tracking technique", in 16th *IEEE International Conference on Electronics, Circuits and Systems - (ICECS 2009)*, Dec. 2009, pp. 291–294, ISBN: 978-1-4244-5090-9. DOI: 10.1109/ICECS.2009.5410997.

[150] C. Hsieh *et al.*, "LED drivers with PPD compensation for achieving fast transient response", in *IEEE International Symposium on Circuits and Systems (ISCAS 2008)*, May 2008, pp. 2202–2205. DOI: 10.1109/ISCAS.2008.4541889.

[151] Y. Hu, L. Huber, and M. Jovanović, "Single-stage, universal-input AC/DC LED driver with current-controlled variable PFC boost inductor", *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1579–1588, Mar. 2012, ISSN: 1941-0107. DOI: 10.1109/TPEL.2010.2082564.

[152] Y. Hu and M. Jovanovic, "A novel LED driver with adaptive drive voltage", in 23rd *IEEE Applied Power Electronics Conference and Exposition (APEC 2008)*, Feb. 2008, pp. 565–571. DOI: 10.1109/APEC.2008.4522777.

[153] Y. Hu and M. Jovanovic, "LED driver with self-adaptive drive voltage", *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 3116–3125, Sep. 2008, ISSN: 0885-8993. DOI: 10.1109/TPEL.2008.2004558. Available online: http://ieeexplore.ieee.org/abstract/document/4696044/.

[154] W. Huffman and V. Pless, *Fundamentals of Error-Correcting Codes*. Cambridge University Press, 2003. DOI: 10.1017/CBO9780511807077.

[155] K. Hwang, B. Choi, and S. Kang, "Enhanced self-configuration scheme for a robust ZigBee-based home automation", *IEEE Transactions on Consumer Electronics*, vol. 56, no. 2, pp. 583–590, May 2010, ISSN: 1558-4127. DOI: 10.1109/TCE.2010.5505974.

[156] K. Hwu and W. Jiang, "Nonisolated two-channel LED driver with automatic current balance and zero-voltage switching", *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8359–8370, Dec. 2016, ISSN: 1941-0107. DOI: 10.1109/TPEL.2016.2515088.

[157] *IEC 60929: AC-supplied electronic ballasts for tubular fluorescent lamps - Performance requirements*, International Electrotechnical Commission (IEC), Jan. 2006.

[158] *IEC 61140:2001(E): protection against electric shock – common aspects for installation and equipment*, International Electrotechnical Commission (IEC), Oct. 2001.

[159] "IEEE draft standard for information technology–telecommunications and information exchange between systems local and metropolitan area networks–specific requirements part 11: Wireless LAN medium access control (MAC) and physical layer (PHY) specifications", *IEEE P802.11-REVmc/D3.0, June 2014*, pp. 1–3701, Feb. 2015.

[160] "IEEE standard for information technology - telecommunications and information exchange between systems - local and metropolitan area networks - specific requirements - part 11: Wireless LAN medium access control (MAC) and physical layer (PHY) specifications", *IEEE Std 802.11-2007*, pp. 1–1076, Jun. 2007. DOI: 10.1109/IEEESTD.2007.373646.

[161] R. Isele, R. Neumann, and K. Blankenbach, "Automotive interior lighting redefined", *SID Symposium Digest of Technical Papers*, vol. 48, no. 1, pp. 687–690, May 2017. DOI: 10.1002/sdtp.11731. Available online: https://onlinelibrary.wiley.com/doi/abs/10.1002/sdtp.11731.

[162] A. Jayawardena, D. Duffy, and J. Manahan, "Lighting matters in industrial environments: A framework linking workplace safety to lighting quality metrics", *IEEE Industry Applications Magazine*, vol. 23, no. 3, pp. 54–63, May 2017, ISSN: 1558-0598. DOI: 10.1109/MIAS.2016.2600697.

[163] A. Jazwinski, "Limited memory optimal filtering", *IEEE Transactions on Automatic Control*, vol. 13, no. 5, pp. 558–563, Oct. 1968, ISSN: 2334-3303. DOI: 10.1109/TAC.1968.1098981.

[164] B. Jensen and S. Kjaersgaard, "Benchmarking and QoS of in-house powerline equipment for AV streaming applications", in 10th *IEEE International Symposium on Power Line Communications and Its Applications (ISPLC 2006)*, Mar. 2006, pp. 160–165. DOI: 10.1109/ISPLC.2006.247454.

[165] H. Jiang *et al.*, "Smart home based on WiFi sensing: a survey", *IEEE Access*, vol. 6, pp. 13 317–13 325, Mar. 2018, ISSN: 2169-3536. DOI: 10.1109/ACCESS.2018.2812887.

[166] W. Jiang, Y. Jiang, and H. Ren, "Analysis and prospect of control system for stage lighting", in 3rd *International Congress on Image and Signal Processing (ICSIP 2010)*, vol. 8, Oct. 2010, pp. 3923–3929. DOI: 10.1109/CISP.2010.5647570.

[167] A. Jovicic, J. Li, and T. Richardson, "Visible light communication: Opportunities, challenges and the path to market", *IEEE Communications Magazine*, vol. 51, no. 12, pp. 26–32, Dec. 2013, ISSN: 1558-1896. DOI: 10.1109/MCOM.2013.6685754.

[168] Y. Jung, S. Hong, and O. Kwon, "A fast transient LED driver with adaptive frequency control according to load variation for large-sized LCD backlights", *Journal of the Society for Information Display*, vol. 25, no. 12, pp. 712–724, Jan. 2018. DOI: 10.1002/jsid.619. Available online: https://onlinelibrary.wiley.com/doi/abs/10.1002/jsid.619.

[169] A. Kailas, V. Cecchi, and A. Mukherjee, "A survey of communications and networking technologies for energy management in buildings and home automation", *Journal of Computer Networks and Communications*, vol. 2012, no. ID 932181, pp. 1–12, Mar. 2012. DOI: https://doi.org/10.1155/2012/932181.

[170] R. E. Kalman and R. S. Bucy, "New Results in Linear Filtering and Prediction Theory", *Journal of Basic Engineering*, vol. 83, no. 1, pp. 95–108, Mar. 1961, ISSN: 0021-9223. DOI: 10.1115/1.3658902. Available online: https://doi.org/10.1115/1.3658902.

[171] H. Kang, *Computational Color Technology*. SPIE—The International Society for Optical Engineering, 2006, ISBN: 0-8194-6119-9.

[172] A. Karagounis *et al.*, "A 90nm Manchester code generator with CMOS switches running at 2.4GHz and 5GHz", in 16th *International Conference on Systems, Signals and Image Processing (IWSSIP 2009)*, Jun. 2009, pp. 1–4. DOI: 10.1109/IWSSIP.2009.5367739.

[173] T. Karlsson, "Human centric school lighting – Evidence based design of light characters and automatic light variation, for a classroom in malmö", Master's Thesis, Lighting Laboratory, KTH Royal Institute of Technology, Dec. 2015.

[174] P. Karn, "MACA – a new channel access method for packet radio", in *ARRL/CRRL Amateur radio 9th computer networking conference*, vol. 140, Sep. 1990, pp. 134–140.

[175] M. Kermani, V. Singh, and R. Azarderakhsh, "Reliable low-latency Viterbi algorithm architectures benchmarked on ASIC and FPGA", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 1, pp. 208–216, Jan. 2017, ISSN: 1558-0806. DOI: 10.1109/TCSI.2016.2610187.

[176] A. Khan *et al.*, "Design of an IoT smart home system", in 15th *Learning and Technology Conference (L& T 2008)*, Feb. 2018, pp. 1–5. DOI: 10.1109/LT.2018.8368484.

[177] T. Q. Khanh *et al.*, *LED Lighting – Technology and Perception*, T. Khanh *et al.*, Eds. John Wiley & Sons, Ltd, 2015, ISBN: 9783527670147. DOI: 10.1002/9783527670147.fmatter. Available online: https://onlinelibrary.wiley.com/doi/abs/10.1002/9783527670147.fmatter.

[178] V. Khanna, *Fundamentals of Solid-State Lighting: LEDs, OLEDs, and Their Applications in Illumination and Displays*. CRC Press, Tylor & Francis Group, Mar. 2014, ISBN: 9781466561090.

[179] H. Kim *et al.*, "An LED color control system with independently changeable illuminance", in 31st *International Telecommunications Energy Conference (INTELEC 2009)*, Oct. 2009, pp. 1–5. DOI: 10.1109/INTLEC.2009.5351875.

[180] M. Kim and C. Choi, "Hidden-node detection in IEEE 802.11n wireless LANs", *IEEE Transactions on Vehicular Technology*, vol. 62, no. 6, pp. 2724–2734, Jul. 2013, ISSN: 1939-9359. DOI: 10.1109/TVT.2013.2246594.

[181] Y. Kim *et al.*, "Color temperature conversion system and method using the same", 10/270,390, May 2003.

[182] L. Kleinrock and F. Tobagi, "Packet switching in radio channels: part I - carrier sense multiple-access modes and their throughput-delay characteristics", *IEEE Transactions on Communications*, vol. 23, no. 12, pp. 1400–1416, Dec. 1975, ISSN: 1558-0857. DOI: 10.1109/TCOM.1975.1092768.

[183] I. Knez, "Effects of indoor lighting on mood and cognition", *Journal of Environmental Psychology*, vol. 15, no. 1, pp. 39–51, 1995, ISSN: 0272-4944. DOI: https://doi.org/10.1016/0272-4944(95)90013-6. Available online: http://www.sciencedirect.com/science/article/pii/0272494495900136.

[184] L. H. Koh *et al.*, "DC renewable connected building grid for intelligent LED lighting system", in 26th *IEEE International Symposium on Industrial Electronics (ISIE 2017)*, Jun. 2017, pp. 970–974. DOI: 10.1109/ISIE.2017.8001377.

[185] T. Komine, S. Haruyama, and M. Nakagawa, "Performance evaluation of narrowband OFDM on integrated system of power line communication and visible light wireless communication", in 1st *International Symposium on Wireless Pervasive Computing*, Nov. 2006, p. 6.

[186] T. Komine and M. Nakagawa, "Fundamental analysis for visible-light communication system using LED lights", *IEEE Transactions on Consumer Electronics*, vol. 50, no. 1, pp. 100–107, Feb. 2004, ISSN: 1558-4127. DOI: 10.1109/TCE.2004.1277847.

[187] N. Kondrath and M. K. Kazimierczuk, "Bandwidth of current transformers", *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 6, pp. 2008–2016, Jun. 2009, ISSN: 1557-9662. DOI: 10.1109/TIM.2008.2006134.

[188] K. Kossakowski, "High frequency clock synthesis from mains voltage", Supervisor: Lukas Lohaus, Master's Thesis, Integrated Analog Circuits and RF Systems, RWTH Aachen University, Jan. 2017.

[189] A. Koubaa *et al.*, "Improving quality-of-service in wireless sensor networks by mitigating "hidden-node collisions"", *IEEE Transactions on Industrial Informatics*, vol. 5, no. 3, pp. 299–313, Aug. 2009, ISSN: 1941-0050. DOI: 10.1109/TII.2009.2026643.

[190] M. Kruse, "Investigation and comparison of smart lighting solutions", in German, Supervisor: Michael Hanhart, Bachelor's Thesis, Integrated Analog Circuits and RF Systems, RWTH Aachen University, Nov. 2017.

[191] A. V. Kudryashov, E. S. Galishheva, and A. S. Kalinina, "Lighting control using DALI interface", in *International Conference on Industrial Engineering, Applications and Manufacturing (ICIEAM 2018)*, May 2018, pp. 1–5. DOI: 10.1109/ICIEAM.2018.8728728.

[192] R. Kuehni, *Color – An Introduction to Practice and Principles*, 3rd ed. John Wiley & Sons, 2013, ISBN: 978-1-118-17384-8.

[193] I. H. Kurniawan, J. Yoon, and J. Park, "Multidimensional Householder based high-speed QR decomposition architecture for MIMO receivers", in *IEEE International Symposium on Circuits and Systems (ISCAS 2013)*, May 2013, pp. 2159–2162. DOI: 10.1109/ISCAS.2013.6572302.

[194] M. Kuzlu and M. Pipattanasomporn, "Assessment of communication technologies and network requirements for different smart grid applications", in *IEEE PES Innovative Smart Grid Technologies Conference (ISGT 2013)*, Feb. 2013, pp. 1–6. DOI: 10.1109/ISGT.2013.6497873.

[195] M. Kuzlu, M. Pipattanasomporn, and S. Rahman, "Communication network requirements for major smart grid applications in HAN, NAN and WAN", *Computer Networks*, vol. 67, pp. 74–88, Jul. 2014, ISSN: 1389-1286. DOI: https://doi.org/10.1016/j.comnet.2014.03.029. Available online: http://www.sciencedirect.com/science/article/pii/S1389128614001431.

[196] M. Kuzlu, M. Pipattanasomporn, and S. Rahman, "Review of communication technologies for smart homes/building applications", in *IEEE Innovative Smart Grid Technologies - Asia (ISGT ASIA 2015)*, Nov. 2015, pp. 1–6. DOI: 10.1109/ISGT-Asia.2015.7437036.

[197] T. Labeodan *et al.*, "Experimental evaluation of the performance of chair sensors in an office space for occupancy detection and occupancy-driven control", *Energy and Buildings*, vol. 111, pp. 195–206, Nov. 2016, ISSN: 0378-7788. DOI: https://doi.org/10.1016/j.enbuild.2015.11.054. Available online: http://www.sciencedirect.com/science/article/pii/S0378778815304187.

[198] L. Lampe *et al.*, *Power Line Communications: Principles, Standards and Applications from Multimedia to Smart Grid*, 2nd Edition, T. G. Lutz Lampe Andrea M. Tonello, Ed. John Wiley & Sons, Ltd., 2016.

[199] N. Langhammer and R. Kays, "Performance evaluation of wireless home automation networks in indoor scenarios", *IEEE Transactions on Smart Grid*, vol. 3, no. 4, pp. 2252–2261, Dec. 2012, ISSN: 1949-3061. DOI: 10.1109/TSG.2012.2208770.

[200] A. Lee *et al.*, "Precise dimming and color control of LED systems based on color mixing", *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 65–80, Jan. 2016, ISSN: 1941-0107. DOI: 10.1109/TPEL.2015.2448641.

[201] E. S. Lee *et al.*, "A novel TRIAC dimming LED driver by variable switched capacitance for power regulation", in 4th *IEEE Energy Conversion Congress and Exposition (ECCE 2014)*, Sep. 2014, pp. 2600–2605. DOI: 10.1109/ECCE.2014.6953749.

[202] K. Lee and D. Cho, "A multiple access collision avoidance protocol for multicast services in mobile ad hoc networks", *IEEE Communications Letters*, vol. 7, no. 10, pp. 508–510, Oct. 2003, ISSN: 2373-7891. DOI: 10.1109/LCOMM.2003.817316.

[203] J. Lee, M. Dong, and Y. Sun, "A preliminary study of low power wireless technologies: ZigBee and Bluetooth Low Energy", in 10th *IEEE Conference on Industrial Electronics and Applications (ICIEA 2015)*, Jun. 2015, pp. 135–139. DOI: 10.1109/ICIEA.2015.7334098.

[204] J. Lee, Y. Su, and C. Shen, "A comparative study of wireless protocols: Bluetooth, UWB, ZigBee, and Wi-Fi", in 33rd *Annual Conference of the IEEE Industrial Electronics Society (IECON 2007)*, Nov. 2007, pp. 46–51. DOI: 10.1109/IECON.2007.4460126.

[205] J. Lee and J. Greivenkamp, "Modeling of automotive interior illumination system", *Optical Engineering - OPT ENG*, vol. 43, pp. 1537–1544, Jul. 2004. DOI: 10.1117/1.1748235.

[206] K. Lee and H. Lee, "Network-based fire-detection system via controller area network for smart home automation", *IEEE Transactions on Consumer Electronics*, vol. 50, no. 4, pp. 1093–1100, Nov. 2004, ISSN: 1558-4127. DOI: 10.1109/TCE.2004.1362504.

[207] M. K. Lee *et al.*, "HomePlug 1.0 powerline communication LANs – Protocol description and performance results", *International Journal of Communication Systems*, vol. 16, no. 5, pp. 447–473, Jun. 2003. DOI: 10.1002/dac.601. Available online: https://onlinelibrary.wiley.com/doi/abs/10.1002/dac.601.

[208] P. Lee and H. Chen, "Adjustable gamma correction circuit for TFT LCD", in *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, vol. 1, May 2005, pp. 780–783. DOI: 10.1109/ISCAS.2005.1464704.

[209] W. Lee and S. Hong, "KNX - ZigBee gateway for home automation", in *IEEE International Conference on Automation Science and Engineering*, Aug. 2008, pp. 750–755. DOI: 10.1109/COASE.2008.4626433.

[210] B. Lehman and A. Wilkins, "Designing to mitigate effects of flicker in LED lighting: Reducing risks to health and safety", *Power Electronics Magazine, IEEE*, vol. 1, pp. 18–26, Sep. 2014. DOI: 10.1109/MPEL.2014.2330442.

[211] B. Lehman *et al.*, "Proposing measures of flicker in the low frequencies for lighting applications", *LEUKOS*, vol. 7, Sep. 2011. DOI: 10.1109/ECCE.2011.6064154.

[212] E. T. Leicht, "Generation of a high frequency clock using utility grid frequency for integrated power control systems", Supervisor: Lukas Lohaus, Ye Zhang, Master's Thesis, Integrated Analog Circuits and RF Systems, RWTH Aachen University, Aachen, Germany, Jan. 2013.

[213] S. D. Lester *et al.*, "High-efficiency InGaN MQW blue and green LEDs", *Journal of Crystal Growth*, vol. 189-190, pp. 786–789, Jun. 1998, ISSN: 0022-0248. DOI: https://doi.org/10.1016/S0022-0248(98)00294-2. Available online: http://www.sciencedirect.com/science/article/pii/S0022024898002942.

[214] C. Li, J. Wu, and X. He, "Realization of a general LED lighting system based on a novel power line communication technology", in 25th *IEEE Applied Power Electronics Conference and Exposition (APEC 2010)*, Mar. 2010, pp. 2300–2304.

[215] S. Li *et al.*, "An off-line single-inductor multiple-output LED driver with high dimming precision and full dimming range", *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4716–4727, Jun. 2017, ISSN: 1941-0107. DOI: 10.1109/TPEL.2016.2597237.

[216] Y. Li *et al.*, "Study of healthy light-color parameters for LED lighting", *Optik*, vol. 126, no. 24, pp. 4887–4889, Dec. 2015, ISSN: 0030-4026. DOI: https://doi.org/10.1016/j.ijleo.2015.09.212. Available online: http://www.sciencedirect.com/science/article/pii/S0030402615012930.

[217] T. J. Liang, J. F. Huang, and P. K. Yadav, "Design and implementation of dimmable LED control circuit with DALI protocol", in 1st *IEEE International Conference on Power and Energy*, Nov. 2016, pp. 121–126. DOI: 10.1109/PECON.2016.7951545.

[218] G. Lightbody, R. Woods, and R. Walke, "Design of a parameterizable silicon intellectual property core for QR-based RLS filtering", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 4, pp. 659–678, Aug. 2003, ISSN: 1557-9999. DOI: 10.1109/TVLSI.2003.816142.

[219] Lighting Europe – The Voice of the Lighting Industry, "Human centric lighting – Lighting designed to benefit human health an wellbeing", 2016, presentation slides. Available online: http://www.lightingeurope.org/.

[220] Lighting Europe – The Voice of the Lighting Industry, "LightingEurope defines growth drivers for the European lighting market and will increase the value of light to society", *Press release in Frankfurt/Brussels, 15th March, 2016*, Mar. 2016.

[221] B. Lim *et al.*, "A 200-V 98.16%-efficiency buck LED driver using integrated current control to improve current accuracy for large-scale single-string LED backlighting applications", *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6416–6427, Sep. 2016, ISSN: 1941-0107. DOI: 10.1109/TPEL.2015.2499540.

[222] K. Lim *et al.*, "Illumination and color management in solid state lighting", in *Conference Record of the 2006 IEEE Industry Applications Conference 41st IAS Annual Meeting*, vol. 5, Oct. 2006, pp. 2616–2620. DOI: 10.1109/IAS.2006.256908.

[223] S. Lim *et al.*, "Entertainment lighting control network standardization to support VLC services", *IEEE Communications Magazine*, vol. 51, no. 12, pp. 42–48, Dec. 2013, ISSN: 1558-1896. DOI: 10.1109/MCOM.2013.6685756.

[224] C. Lin *et al.*, "A balancing strategy and implementation of current equalizer for high power LED backlighting", in *7th International Conference on Power Electronics and Drive Systems (ICEPDS 2007)*, Nov. 2007, pp. 1613–1617. DOI: 10.1109/PEDS.2007.4487925.

[225] J. Lin, T. Talty, and O. K. Tonguz, "On the potential of Bluetooth Low Energy technology for vehicular applications", *IEEE Communications Magazine*, vol. 53, no. 1, pp. 267–275, Jan. 2015, ISSN: 1558-1896. DOI: 10.1109/MCOM.2015.7010544.

[226] Y. Lin *et al.*, "A power line communication network infrastructure for the smart home", *IEEE Wireless Communications*, vol. 9, no. 6, pp. 104–111, Dec. 2002, ISSN: 1558-0687. DOI: 10.1109/MWC.2002.1160088.

[227] Y. Lin *et al.*, "LED backlight driver circuit with dual-mode dimming control and current-balancing design", *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4632–4639, Sep. 2014, ISSN: 1557-9948. DOI: 10.1109/TIE.2013.2288234.

[228] A. Lindemann *et al.*, "Indoor positioning: A comparison of WiFi and Bluetooth Low Energy for region monitoring", in *9th International Join Conference on Biomdeical Engineering Systems and Technologies (BIOSTEC 2016)*, ser. HEALTHINF, Department of Computer Science, vol. 5, Jan. 2016, pp. 314–321. DOI: 10.5220/0005704603140321.

[229] C. Liu *et al.*, "SAR-controlled adaptive off-time technique without sensing resistor for achieving high efficiency and accuracy LED lighting system", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 6, pp. 1384–1394, Jun. 2010, ISSN: 1549-8328.

[230] P. Liu, Y. Hsu, and S. Hsu, "Drain-voltage balance and phase-shifted PWM control schemes for high-efficiency parallel-string dimmable LED drivers", *IEEE Transactions on Industrial Electronics*, vol. 65, no. 8, pp. 6168–6176, Aug. 2018, ISSN: 1557-9948. DOI: 10.1109/TIE.2018.2793220.

[231] P. Liu and K. Peng, "Adaptive driving bus voltage and energy recycling control schemes for low-power AC–DC RGB-LED drivers", *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 7741–7748, Oct. 2017, ISSN: 1557-9948. DOI: 10.1109/TIE.2017.2688977.

[232] S. Liu, L. Fu, and W. Xie, "Hidden-node problem in full-duplex enabled CSMA networks", *IEEE Transactions on Mobile Computing*, vol. 19, no. 2, pp. 347–361, Feb. 2020, ISSN: 2161-9875. DOI: 10.1109/TMC.2019.2895034.

[233] A. Llenas and J. Carreras, "Arbitrary spectral matching using multi-LED lighting systems", *Optical Engineering*, vol. 58, no. 3, pp. 1–9, Mar. 2019. DOI: 10.1117/1.0E.58.3.035105. Available online: https://doi.org/10.1117/1.0E.58.3.035105.

[234] L. Lohaus, T. Bautze, and K. Dieopold, "Evaluation of optical sensors for laser welding in a technical cognitive environment", 29th *International Congress on Applications of Lasers and Electro-Optics (ICALEO 2010)*, vol. 103, pp. 1541–1546, Sep. 2010.

[235] L. Lohaus *et al.*, "A comparison of receiver topologies for Digital Load-Side Transmission in general LED lighting", in 18th *IEEE International Symposium on Power Line Communications and its Applications (ISPLC 2014)*, Mar. 2014, pp. 249–254. DOI: 10.1109/ISPLC.2014.6812336.

[236] L. Lohaus *et al.*, "A dimmable LED driver using resistive DAC feedback control for adaptive voltage regulation", in 5th *IEEE Energy Conversion Congress and Exposition (ECCE 2013)*, Sep. 2013, pp. 3126–3133. DOI: 10.1109/ECCE.2013.6647109.

[237] L. Lohaus *et al.*, "A dimmable LED driver with resistive DAC feedback control for adaptive voltage regulation", *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3254–3262, Jul. 2015. DOI: 10.1109/TIA.2014.2387486.

[238] L. Lohaus *et al.*, "A power supply topology operating at highly discontinuous input voltages for two-wire connected control devices in Digital Load-Side Transmission (DLT) systems for intelligent lighting", in 30th *IEEE Applied Power Electronics Conference and Exposition (APEC 2015)*, Mar. 2015, pp. 1897–1904. DOI: 10.1109/APEC.2015.7104605.

[239] L. Lohaus *et al.*, "Advanced color control for multicolor LED illumination systems with parametric optimization", in 39th *Annual Conference of the IEEE Industrial Electronics Society (IECON 2013)*, Nov. 2013, pp. 3305–3310. DOI: 10.1109/IECON.2013.6699658.

[240] L. Lohaus *et al.*, "An advanced control device for intelligent lighting in DLT-systems", in 18th *European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sep. 2016, pp. 1–10. DOI: 10.1109/EPE.2016.7695506.

[241] L. Lohaus *et al.*, "An efficient dual-stage power supply topology for series connected control devices in intelligent lighting systems", in 7th *IEEE Energie Conversion Congress and Exposition (ECCE 2015)*, Sep. 2015, pp. 2453–2460. DOI: 10.1109/ECCE.2015.7310005.

[242] L. Lohaus *et al.*, "Energy efficient current control technique for driving high power LEDs", in 8th *Conference on Ph.D. Research in Microelectronics and Electronics (PRIME 2012)*, Jun. 2012, pp. 1–4.

[243] L. Lohaus *et al.*, "Towards bidirectional power line communication with Digital Load-Side Transmission", in 20th *International Symposium on Power Line Communications and its Applications (ISPLC 2016)*, Mar. 2016, pp. 179–184. DOI: 10.1109/ISPLC.2016.7476283.

[244] K. H. Loo *et al.*, "Color control system for RGB LED with application to light sources suffering from prolonged aging", *IEEE Transactions on Industrial Electronics*, vol. 61, no. 4, pp. 1788–1798, Apr. 2014, ISSN: 1557-9948. DOI: 10.1109/TIE.2013.2267696.

[245] K. H. Loo *et al.*, "On driving techniques for LEDs: Toward a generalized methodology", *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2967–2976, Dec. 2009, ISSN: 1941-0107. DOI: 10.1109/TPEL.2009.2021183.

[246] K. H. Loo *et al.*, "On the color stability of phosphor-converted white LEDs under DC, PWM, and bilevel drive", *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 974–984, Feb. 2012, ISSN: 1941-0107. DOI: 10.1109/TPEL.2010.2086080.

[247] K. H. Loo *et al.*, "Stationary and adaptive color-shift reduction methods based on the bilevel driving technique for phosphor-converted white LEDs", *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1943–1953, Dec. 2011, ISSN: 1941-0107. DOI: 10.1109/TPEL.2010.2097610.

[248] M. Lorent, "System design and implementation of a wireless control infrastructure for intelligent led luminaires", in German, Supervisor: Lukas Lohaus, Bachelor's Thesis, Integrated Analog Circuits and RF Systems, RWTH Aachen University, Sep. 2012.

[249] E. Lübbe, *Farbempfindung, Farbbeschreibung und Farbmessung. Eine Formel für die Farbsättigung*, 1st. Springer Vieweg, 2013, in German, ISBN: 978-3-8348-1801-0. DOI: 10.1007/978-3-8348-2228-4.

[250] B. Ludwiczak and W. Jantsch, "Color deviations in phosphor converted high power light emitting diodes under different dimming schemes", *Journal of Luminescence*, vol. 158, Jan. 2015. DOI: 10.1016/j.jlumin.2014.10.037.

[251] W. Lun *et al.*, "Bilevel current driving technique for LEDs", *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2920–2932, Dec. 2009, ISSN: 1941-0107. DOI: 10.1109/TPEL.2009.2021687.

[252] Q. Luo *et al.*, "An LED driver with dynamic high-frequency sinusoidal bus voltage regulation for multistring applications", *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 491–500, Jan. 2014, ISSN: 1941-0107. DOI: 10.1109/TPEL.2013.2253335.

[253] H. Ma *et al.*, "A novel valley-fill SEPIC-derived power supply without electrolytic capacitor for LED lighting application", *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 3057–3071, Jun. 2012, ISSN: 1941-0107. DOI: 10.1109/TPEL.2011.2174446.

[254] H. Ma, L. Lampe, and S. Hranilovic, "Integration of indoor visible light and power line communication systems", in 17th *IEEE International Symposium on Power Line Communications and Its Applications (ISPLC 2013)*, Mar. 2013, pp. 291–296.

[255] W. Ma *et al.*, "Control scheme for TRIAC dimming high PF single-stage LED driver with adaptive bleeder circuit and non-linear current reference", in 31th *IEEE Applied Power Electronics Conference and Exposition (APEC 2016)*, Mar. 2016, pp. 816–821. DOI: 10.1109/APEC.2016.7467965.

[256] D. MacAdam, "Specification of small chromaticity differences", *Journal of the Optical Society of America*, vol. 33, no. 1, pp. 18–26, Jan. 1943. DOI: 10.1364/JOSA.33.000018. Available online: http://www.osapublishing.org/abstract.cfm?URI=josa-33-1-18.

[257] M. Magno *et al.*, "A low cost, highly scalable wireless sensor network solution to achieve smart LED light control for green buildings", *IEEE Sensors Journal*, vol. 15, no. 5, pp. 2963–2973, May 2015, ISSN: 2379-9153. DOI: 10.1109/JSEN.2014.2383996.

[258] P. Malcovati *et al.*, "A 0.18-μm CMOS, 91%-efficiency, 2-A scalable buck-boost DC-DC converter for LED drivers", *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5392–5398, Oct. 2014, ISSN: 1941-0107. DOI: 10.1109/TPEL.2013.2294189.

[259] R. Malik, K. K. Ray, and S. Mazumdar, "Wide-range, open-loop, CCT and illuminance control of an LED lamp using two-component color blending", *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9803–9818, Nov. 2018, ISSN: 1941-0107. DOI: 10.1109/TPEL.2017.2785684.

[260] C. S. McCamy, "Correlated color temperature as an explicit function of chromaticity coordinates", *Color Research & Application*, vol. 17, no. 2, pp. 142–144, Apr. 1992. DOI: 10.1002/col.5080170211. Available online: https://onlinelibrary.wiley.com/doi/abs/10.1002/col.5080170211.

[261] N. Mcneill and N. K. Gupta, "Assessment of the error in the average current sensed by the unidirectional current pulse transformer", *IET Circuits, Devices Systems*, vol. 2, no. 2, pp. 265–276, Apr. 2008, ISSN: 1751-8598. DOI: 10.1049/iet-cds:20070226.

[262] A. Meister, *Numerik linearer Gleichungssysteme*, 4. Edition. Vieweg+Teubner Verlag, Springer Fachmedien Wiesbaden GmbH, 2011, in German, ISBN: 978-3-8348-1550-7.

[263] T. Mendes *et al.*, "Smart home communication technologies and applications: Wireless protocol assessment for home area network resources", *Energies*, vol. 8, no. 7, pp. 7279–7311, Jul. 2015, ISSN: 1996-1073. DOI: 10.3390/en8077279. Available online: https://www.mdpi.com/1996-1073/8/7/7279.

[264] H. Merz, T. Hansemann, and C. Hübner, *Building Automation – Communication Systems with EIB/KNX, LON and BACnet*. Springer-Verlag Berlin Heidelberg, 2009. DOI: 10.1007/978-3-540-88829-1.

[265] A. Mills, "Lighting: The progress & promise of LEDs", *III-Vs Review*, vol. 17, no. 4, pp. 39–41, May 2004, ISSN: 0961-1290. DOI: https://doi.org/10.1016/S0961-1290(04)00466-1. Available online: http://www.sciencedirect.com/science/article/pii/S0961129004004661.

[266] P. Mills, S. Tomkins, and L. Schlangen, "The effect of high correlated colour temperature office lighting on employee wellbeing and work performance", *Journal of circadian rhythms*, vol. 5, p. 2, Jan. 2007. DOI: 10.1186/1740-3391-5-2.

[267] K. Modepalli and L. Parsa, "A scalable N-color LED driver using single inductor multiple current output topology", *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3773–3783, May 2016, ISSN: 1941-0107. DOI: 10.1109/TPEL.2015.2444853.

[268] K. Moeller *et al.*, "Led office lighting to promote performance and well-being", in *Ergonomics and Health Aspects of Work with Computers*, M. M. Robertson, Ed., Springer Berlin Heidelberg, Jul. 2011, pp. 68–77, ISBN: 978-3-642-21716-6.

[269] S. Moon, G. Koo, and G. Moon, "Dimming-feedback control method for TRIAC dimmable LED drivers", *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 960–965, Feb. 2015, ISSN: 1557-9948. DOI: 10.1109/TIE.2014.2349871.

[270] M. Motta, "Adverse Health Effects of Nighttime Lighting", *Journal of the American Association of Variable Star Observers (JAAVSO)*, vol. 40, no. 1, p. 380, Jun. 2012.

[271] J. H. Mueller *et al.*, "An adaptable UART based configuration and read-out interface for IC prototypes", in 8th *Conference on Ph.D. Research in Microelectronics Electronics (PRIME 2012)*, Jun. 2012, pp. 1–4.

[272] T. Mukai, M. Yamada, and S. Nakamura, "Characteristics of InGaN-based UV/blue/-green/amber/red light-emitting diodes", *Japanese Journal of Applied Physics*, vol. 38, no. Part 1, No. 7A, pp. 3976–3981, Jul. 1999. DOI: 10.1143/jjap.38.3976. Available online: https://doi.org/10.1143%2Fjjap.38.3976.

[273] A. Y. Mulla *et al.*, "Implementation of ZigBee/802.15.4 in smart grid communication and analysis of power consumption: A case study", in 11th *Annual IEEE India Conference (INDICON 2014)*, Dec. 2014, pp. 1–7. DOI: 10.1109/INDICON.2014.7030564.

[274] T. Muoi, "Receiver design for digital fiber optic transmission systems using Manchester (biphase) coding", *IEEE Transactions on Communications*, vol. 31, no. 5, pp. 608–619, May 1983, ISSN: 1558-0857. DOI: 10.1109/TCOM.1983.1095872.

[275] M. Murdoch, "Dynamic color control in multiprimary tunable LED lighting systems", *Journal of the Society for Information Display*, vol. 27, no. 9, pp. 570–580, Apr. 2019. DOI: 10.1002/jsid.779. Available online: https://onlinelibrary.wiley.com/doi/abs/10.1002/jsid.779.

[276] S. Muthu and J. Gaines, "Red, green and blue LED-based white light source: implementation challenges and control design", in 38th *IAS Annual Meeting on Conference Record of the Industry Applications Conference*, vol. 1, Oct. 2003, pp. 515–522. DOI: 10.1109/IAS.2003.1257549.

[277] S. Muthu, F. J. Schuurmans, and M. D. Pashley, "Red, green, and blue LED based white light generation: issues and control", in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, vol. 1, Oct. 2002, pp. 327–333. DOI: 10.1109/IAS.2002.1044108.

[278] Z. Nagy *et al.*, "Occupant centered lighting control for comfort and energy efficient building operation", *Energy and Buildings*, vol. 94, pp. 100–108, Mar. 2015, ISSN: 0378-7788. DOI: https://doi.org/10.1016/j.enbuild.2015.02.053. Available online: http://www.sciencedirect.com/science/article/pii/S0378778815001759.

[279] S. Nakamura and M. R. Krames, "History of gallium–nitride-based light-emitting diodes for illumination", *Proceedings of the IEEE*, vol. 101, no. 10, pp. 2211–2220, Oct. 2013, ISSN: 1558-2256. DOI: 10.1109/JPROC.2013.2274929.

[280] S. Nakamura, "InGaN/AlGaN blue-light-emitting diodes", *Journal of Vacuum Science & Technology A*, vol. 13, no. 3, pp. 705–710, May 1995. DOI: 10.1116/1.579811. Available online: https://doi.org/10.1116/1.579811.

[281] S. Nakamura, T. Mukai, and M. Senoh, "Candela-class high-brightness InGaN/AlGaN double-heterostructure blue-light-emitting diodes", *Applied Physics Letters*, vol. 64, no. 13, pp. 1687–1689, Mar. 1994. DOI: 10.1063/1.111832. Available online: https://doi.org/10.1063/1.111832.

[282] P. S. Neelakanta and H. Dighe, "Robust factory wireless communications: A performance appraisal of the Bluetooth™ and the ZigBee™ colocated on an industrial floor", in 29th *Annual Conference of the IEEE Industrial Electronics Society (IECON 2003)*, vol. 3, Nov. 2003, pp. 2381–2386. DOI: 10.1109/IECON.2003.1280617.

[283] S. K. Ng *et al.*, "Sequential variable bilevel driving approach suitable for use in high-color-precision LED display panels", *IEEE Transactions on Industrial Electronics*, vol. 59, no. 12, pp. 4637–4645, Dec. 2012, ISSN: 1557-9948. DOI: 10.1109/TIE.2011.2180490.

[284] J. Oh, S. Yang, and Y. Do, "Healthy, natural, efficient and tunable lighting: Four-Package white LEDs for optimizing the circadian effect, color quality and vision performance", *Light: Science & Applications*, vol. 3, Feb. 2014. DOI: 10.1038/lsa.2014.22.

[285] A. Pandharipande and D. Caicedo, "Daylight integrated illumination control of LED systems based on enhanced presence sensing", *Energy and Buildings*, vol. 43, no. 4, pp. 944–950, Apr. 2011, ISSN: 0378-7788. DOI: https://doi.org/10.1016/j.enbuild.2010.12.018. Available online: http://www.sciencedirect.com/science/article/pii/S0378778810004597.

[286] A. Pandharipande and D. Caicedo, "Smart indoor lighting systems with luminaire-based sensing: a review of lighting control approaches", *Energy and Buildings*, vol. 104, pp. 369–377, Oct. 2015, ISSN: 0378-7788. DOI: https://doi.org/10.1016/j.enbuild.2015.07.035. Available online: http://www.sciencedirect.com/science/article/pii/S0378778815301511.

[287] A. Pandharipande, D. Caicedo, and X. Wang, "Sensor-driven wireless lighting control: system solutions and services for intelligent buildings", *IEEE Sensors Journal*, vol. 14, no. 12, pp. 4207–4215, Dec. 2014, ISSN: 2379-9153. DOI: 10.1109/JSEN.2014.2351775.

[288] D. Pang, S. Lu, and Q. Zhu, "Design of intelligent home control system based on KNX/EIB bus network", in 10th *International Conference on Wireless Communication and Sensor Network*, Dec. 2014, pp. 330–333. DOI: 10.1109/WCSN.2014.74.

[289] D. Park, Z. Liu, and H. Lee, "A 40 V 10 W 93%-efficiency current-accuracy-enhanced dimmable LED driver with adaptive timing difference compensation for solid-state lighting applications", *IEEE Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1848–1860, Aug. 2014, ISSN: 1558-173X. DOI: 10.1109/JSSC.2014.2320951.

[290] D. Pascale, "A review of RGB color spaces", The BabelColor Company, Tech. Rep., 2003. Available online: http://www.babelcolor.com/index_htm_files/A%20review%20of%20RGB%20color%20spaces.pdf.

[291] J. Peng and L. Cheng, "Revisiting carrier sense multiple access with collision avoidance (CSMA/CA)", in 40th *Annual Conference on Information Sciences and Systems (CISS 2006)*, Mar. 2006, pp. 1236–1241. DOI: 10.1109/CISS.2006.286654.

[292] Z. Perko, D. Topic, and J. Perko, "Standardized system for monitoring and control of public lighting networks", in 2nd *International Conference on Smart Systems and Technologies (SST 2017)*, Oct. 2017, pp. 45–50. DOI: 10.1109/SST.2017.8188668.

[293] C. Pham, "CMOS schmitt trigger circuit with controllable hysteresis using logical threshold voltage control circuit", in 6th *IEEE/ACIS International Conference on Computer and Information Science (ICIS 2007)*, Jul. 2007, pp. 48–53. DOI: 10.1109/ICIS.2007.76.

[294] R. Piyare and M. Tazil, "Bluetooth based home automation system using cell phone", in 15th *IEEE International Symposium on Consumer Electronics (ISCE 2011)*, Jun. 2011, pp. 192–195. DOI: 10.1109/ISCE.2011.5973811.

[295] B. Plitnick *et al.*, "The effects of red and blue light on alertness and mood at night", *Lighting Research & Technology*, vol. 42, no. 4, pp. 449–458, Dec. 2010. DOI: 10.1177/1477153509360887. Available online: https://doi.org/10.1177/1477153509360887.

[296] R. S. Popovic, *Hall Effect Devices*, 2nd Edition, B. E. Jones and W. D. Spillman Jr., Eds., ser. Series in Sensors. Institue of Physics Publishing, 2003.

[297] R. S. Popovic, Z. Randjelovic, and D. Manic, "Integrated hall-effect magnetic sensors", *Sensors and Actuators A Physical*, vol. 91, no. 1, pp. 46–50, Jun. 2001, 3rd European Conference on Magnetic Sensors & Actuators., ISSN: 0924-4247. DOI: https://doi.org/10.1016/S0924-4247(01)00478-2. Available online: http://www.sciencedirect.com/science/article/pii/S0924424701004782.

[298] N. Popovich, "America's light bulb revolution", *The New York Times*, Mar. 2019. Available online: https://www.nytimes.com/interactive/2019/03/08/climate/light-bulb-efficiency.html.

[299] J. Proakis and D. Manolakis, *Digital Signal Processing – Principles, Algorithms and Applications*, 4th Edition. Pearson Prentice Hall, 2007, ISBN: 9780132287319. Available online: https://books.google.de/books?id=twtGPwAACAAJ.

[300] X. Qu, S. C. Wong, and C. K. Tse, "Color control system for RGB LED light sources using junction temperature measurement", in 33rd *Annual Conference of the IEEE Industrial Electronics Society 8IECON 2007)*, Nov. 2007, pp. 1363–1368. DOI: 10.1109/IECON.2007.4459976.

[301] A. Rahman and P. Gburzynski, "Hidden problems with the hidden node problem", in 23rd *Biennial Symposium on Communications (BSC 2006)*, May 2006, pp. 270–273. DOI: 10.1109/BSC.2006.1644620.

[302] S. Rajagopal, R. D. Roberts, and S. Lim, "IEEE 802.15.7 visible light communication: Modulation schemes and dimming support", *IEEE Communications Magazine*, vol. 50, no. 3, pp. 72–82, Mar. 2012, ISSN: 1558-1896. DOI: 10.1109/MCOM.2012.6163585.

[303] S. Ramseier, M. Arzberger, and A. Hauser, "MV and LV powerline communications: New proposed IEC standards", in *IEEE Transmission and Distribution Conference*, vol. 1, Apr. 1999, pp. 235–239. DOI: 10.1109/TDC.1999.755350.

[304] M. Rea and J. Freyssinier-Nova, "Color rendering: A tale of two metrics", *Color Research & Application*, vol. 33, no. 3, pp. 192–202, Aug. 2008. DOI: 10.1002/col.20399. Available online: https://onlinelibrary.wiley.com/doi/abs/10.1002/col.20399.

[305] A. Rossius, "Design and implementation of a powerline receiver for controlling high power LEDs", in German, Supervisors: Lukas Lohaus, Stefan Dietrich, Diploma Thesis, Integrated Analog Circuits and RF Systems, RWTH Aachen University, Aug. 2012.

[306] M. Royer, "What is the reference? An examination of alternatives to the reference sources used in IES TM-30-15", *LEUKOS*, vol. 13, no. 2, pp. 71–89, Dec. 2016. DOI: 10.1080/15502724.2016.1255146. Available online: https://doi.org/10.1080/15502724.2016.1255146.

[307] F. Rubinstein, M. Siminovitch, and Verderber, R., "Fifty percent energy savings with automatic lighting controls", *IEEE Transactions on Industry Applications*, vol. 29, no. 4, pp. 768–773, Jul. 1993, ISSN: 0093-9994. DOI: 10.1109/28.231992.

[308] M. Rüger *et al.*, "Time-of-day-dependent effects of bright light exposure on human psychophysiology: Comparison of daytime and nighttime exposure", *American journal of physiology. Regulatory, integrative and comparative physiology*, vol. 290, Jun. 2006. DOI: 10.1152/ajpregu.00121.2005.

[309] B. R. Saltzberg, "An improved Manchester code receiver", in *IEEE International Conference on Communications, Including Supercomm Technical Sessions*, vol. 2, Apr. 1990, pp. 698–702. DOI: 10.1109/ICC.1990.117167.

[310] R. Salvador *et al.*, "A Cortex-M3 based MCU featuring AVS with 34nW static power, 15.3pJ/inst. active energy, and 16% power variation across process and temperature", in 44th *European Solid State Circuits Conference (ESSCIRC 2018)*, Sep. 2018, pp. 278–281. DOI: 10.1109/ESSCIRC.2018.8494312.

[311] L. Schlangen *et al.*, "Workplace illumination effects on acuity, cognitive performance and well-being in older and young people", Jun. 2015.

[312] E. Schubert, *Light-Emitting Diodes*, 2nd Edition. Cambridge University Press, 2006. DOI: 10.1017/CBO9780511790546.

[313] E. Schulte Bocholt, "Integrated DC-DC converter control for adaptive voltage regulation of high power LEDs", Supervisor: Lukas Lohaus, Master's Thesis, Integrated Analog Circuits and RF Systems, RWTH Aachen University, Oct. 2013.

[314] K. Shahzad and B. Oelmann, "A comparative study of in-sensor processing vs. raw data transmission using ZigBee, BLE and Wi-Fi for data intensive monitoring applications", in 11th *International Symposium on Wireless Communications Systems (ISWCS 2014)*, Aug. 2014, pp. 519–524. DOI: 10.1109/ISWCS.2014.6933409.

[315] K. Shailesh and S. Tanuja, "Novel technique for implementation of color algorithm for LED used for general illumination.", Mar. 2009.

[316] G. Sharma, W. Wu, and E. Dalal, "The CIEDE2000 color-difference formula: Implementation notes, supplementary test data, and mathematical observations", *Color Research & Application*, vol. 30, no. 1, pp. 21–30, Feb. 2005. DOI: 10.1002/col.20070. Available online: https://onlinelibrary.wiley.com/doi/abs/10.1002/col.20070.

[317] M. Shatalov *et al.*, "Band-edge luminescence in quaternary AlInGaN light-emitting diodes", *Applied Physics Letters*, vol. 78, pp. 817–819, Feb. 2001. DOI: 10.1063/1.1343493.

[318] J. Shimada, Y. Kawakami, and S. Fujita, "Surgical operation using lighting goggle composed of white LED arrays", in *Solid State Lighting and Displays*, I. T. Ferguson *et al.*, Eds., International Society for Optics and Photonics, vol. 4445, SPIE, Dec. 2001, pp. 13–22. DOI: 10.1117/12.450042. Available online: https://doi.org/10.1117/12.450042.

[319] K. Shuaib *et al.*, "Co-existence of Zigbee and WLAN, a performance study", in *Wireless Telecommunications Symposium*, Apr. 2006, pp. 1–6. DOI: 10.1109/WTS.2006.334532.

[320] M. H. Shwehdi and A. Z. Khan, "A power line data communication interface using spread spectrum technology in home automation", *IEEE Transactions on Power Delivery*, vol. 11, no. 3, pp. 1232–1237, Jul. 1996, ISSN: 1937-4208. DOI: 10.1109/61.517476.

[321] M. Siekkinen *et al.*, "How low energy is bluetooth low energy? – comparative measurements with ZigBee/802.15.4", in *IEEE Wireless Communications and Networking Conference Workshops (WCNCW 2012)*, Apr. 2012, pp. 232–237. DOI: 10.1109/WCNCW.2012.6215496.

[322] A. Sikora and V. F. Groza, "Coexistence of IEEE 802.15.4 with other systems in the 2.4 GHz-ISM-band", in 20th *IEEE Instrumentationand Measurement Technology Conference Proceedings*, vol. 3, May 2005, pp. 1786–1791. DOI: 10.1109/IMTC.2005.1604479.

[323] V. Singhvi *et al.*, "Intelligent light control using sensor networks", in *Proceedings of the* 3rd *International Conference on Embedded Networked Sensor Systems*, ser. SenSys'05, San Diego, California, USA: Association for Computing Machinery, Nov. 2005, pp. 218–229, ISBN: 159593054X. DOI: 10.1145/1098918.1098942. Available online: https://doi.org/10.1145/1098918.1098942.

[324] M. Sisto and J. Gauvin, "Accurate chromatic control and color rendering optimization in LED lighting systems using junction temperature feedback", vol. 9190, Sep. 2014, p. 919 002. DOI: 10.1117/12.2060391.

[325] P. Smith, "Comparison between low power wireless technologies – Bluetooth Low Energy, ANT, ANT+, RF4CE, ZigBee, Wi-Fi, Nike+, IrDA and NFC", *CSR plc Whitepaper*, no. 1, May 2011.

[326] *Solid-state lighting – LED efficacy: What america stands to gain*, DOE/EE-1689, U.S. Department of Energy – Energy Effi, Oct. 2017.

[327] Y. Son *et al.*, "Home energy management system based on power line communication", *IEEE Transactions on Consumer Electronics*, vol. 56, no. 3, pp. 1380–1386, Aug. 2010, ISSN: 1558-4127. DOI: 10.1109/TCE.2010.5606273.

[328] S. S. Stevens, "The psychophysics of sensory function", *American Scientist*, vol. 48, no. 2, pp. 226–253, Jun. 1960. Available online: http://www.jstor.org/stable/27827540.

[329] S. Strache *et al.*, "A digital pulse width modulation closed loop control LDMOS gate driver for LED drivers implemented in a 0.18 μm HV CMOS technology", in *IEEE Custom Integrated Circuits Conference (CICC 2017)*, Apr. 2017, pp. 1–4. DOI: 10.1109/CICC.2017.7993618.

[330] *Strategic Roadmap 2025 of the European Lighting Industry*. Lighting Europe – The Voice of the Lighting Industry, 2016.

[331] A. Sturm, "Design and implementation of an energy-efficient power supply for control devices in intelligent illumination systems", in German, Supervisor: Lukas Lohaus, Bachelor's Thesis, Integrated Analog Circuits and RF Systems, RWTH Aachen University, Mar. 2013.

[332] A. Suzdalenko and I. Galkin, "Choice of power and control hardware for smart LED luminary", in 12th *Biennial Baltic Electronics Conference (BEC 2010)*, Nov. 2010, pp. 331–334.

[333] L. Svilainis, "LED PWM dimming linearity investigation", *Displays*, vol. 29, no. 3, pp. 243–249, Jul. 2008, ISSN: 0141-9382. DOI: 10.1016/j.displa.2007.08.006. Available online: http://www.sciencedirect.com/science/article/pii/S0141938207000777.

[334] T. Taguchi, Y. Uchida, and K. Kobashi, "Efficient white LED lighting and its application to medical fields", *physica status solidi (a)*, vol. 201, pp. 2730–2735, Sep. 2004. DOI: 10.1002/pssa.200405101.

[335] M. Tahan and T. Hu, "Multiple string LED driver with flexible and high-performance PWM dimming control", *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9293–9306, Dec. 2017, ISSN: 1941-0107. DOI: 10.1109/TPEL.2017.2655884.

[336] Y. Tam, V. Kalavally, and J. Parkkinen, "Mixed-color LED lighting with circadian benefits", Jan. 2014.

[337] M. Tanaka, T. Horiuchi, and S. Tominaga, "Color control of a lighting system using RGBW LEDs", *Proceedings of SPIE - The International Society for Optical Engineering*, Jan. 2011. DOI: 10.1117/12.872374.

[338] C. Tang, B. Huang, and S. Ying, "Illumination and color control in red-green-blue light-emitting diode", *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4921–4937, Sep. 2014, ISSN: 1941-0107. DOI: 10.1109/TPEL.2013.2251428.

[339] S. J. W. Tang *et al.*, "Closed-loop color control of an RGB luminaire using sensors onboard a mobile computing system", in *IEEE Student Conference on Research and Development (SCOReD 2016)*, Dec. 2016, pp. 1–5. DOI: 10.1109/SCORED.2016.7810062.

[340] Q. Tao *et al.*, "Symbol detection of ambient backscatter systems with Manchester coding", *IEEE Transactions on Wireless Communications*, vol. 17, no. 6, pp. 4028–4038, Jun. 2018, ISSN: 1558-2248. DOI: 10.1109/TWC.2018.2819188.

[341] *Technical application note – 2x36W digital dimmable ballast with L6574 and ST7FDALI*, Rev. 1, Application note – AN2708, ST Microelectronics, Mar. 2008.

[342] *Technical datasheed of DS61 – LUXEON rebel es – leading efficacy and light output, maximum designflexibility*, Philips Lumileds Lighting Company, 2013. Available online: www.philipslumileds.com.

[343] *Technical datasheed of DS64 – LUXEON rebel – general purpose white*, Lumileds Holding B.V., 2016. Available online: lumileds.com.

[344] *Technical datasheet of 56050c 10 A current sensing transformer in 5600 series*, KMP_5600c_C01, Murata Power Solutions, Inc., 2012. Available online: www.murata-ps.com/support.

[345] *Technical datasheet of 8/16-bit Atmel XMEGA A3U microcontroller*, Atmel Corp., Sep. 2014.

[346] *Technical datasheet of ADuM3400, ADuM3401, ADuM3402 – Quad-channel digital isolators with enhaned system-level ESD reliability performance*, Rev. E, Analog Devices Inc., Jul. 2016. Available online: www.analog.com.

[347] *Technical datasheet of AT86RF231 – Low-power 2.4 GHz transceiver for ZigBee, IEEE 802.15.4, 6LoWPAN, RF4CE, SP100, WirelessHART, and ISM applications*, Rev. 8111C, Atmel Corp., Sep. 2009. Available online: www.microchip.com.

[348] *Technical datasheet of BLE112 – Bluetooth Low Energy single mode module*, Version 1.48, Silicon Laboratories Inc., Dec. 2015. Available online: http://www.silabs.com.

[349] *Technical datasheet of BlueCore™ 2 – External: Single chip Bluetooth® system*, BC212015-ds-001Pj, Cambridge Silicon Radio (CSR) Ltd., Aug. 2006.

[350] *Technical datasheet of CC2430 – a true system-on-chip solution for 2.4GHz IEEE 802.15.4/ZigBee*, Rev. 2.1, Chipcon Products from Texas Instruments, May 2007.

[351] *Technical datasheet of CC2520 – 2.4GHz IEEE 802.15.4/ZigBee® RF transceiver*, SWRS068 – Initial Release, Texas Instruments, Dec. 2007.

[352] *Technical datasheet of CC2540F128 and CC2540F256 – 2.4GHz Bluetooth Low Energy system-on-chip*, SWRS084F – Revision F, Texas Instruments, Jun. 2013.

[353] *Technical datasheet of CRM0805 – high power current sense chip resistors*, Rev 5/15, Bourns, May 2015.

[354] *Technical datasheet of DT024CTFT – 2.4"TFT display module*, Rev. 1.0, Displaytech Ltd., Dec. 2012.

[355] *Technical datasheet of EA DOGL128-6 – High-contrast LCD supertwist display*, Electronic Assembly GmbH, Zeppelinstraße 19, 82205 Gilching, Germany, May 2014.

[356] *Technical datasheet of FT232R USB to UART converter IC*, Ver. 2.10, FT_000053, FTDI #38, Future Technology Devices International Ltd., Mar. 2012. Available online: http://www.ftdichip.com/FTProducts.htm.

[357] *Technical datasheet of gain span GS1011M – Low-power wireless system-on-chip WiFi module*, Rev. 1.6 (2013-03-01), GainSpan Corp., Mar. 2013.

[358] *Technical datasheet of H11L1M, H11L2M, H11L3M – 6-pin DIP schmitt trigger output optocoupler*, Rev. 1.0.7, Fairchild Semiconductor Corporation, Sep. 2014. Available online: www.fairchildsemi.com.

[359] *Technical datasheet of high voltage NPN power transistor BUXD87*, ST Microelectronics, Apr. 1999.

[360] *Technical datasheet of LT1806/1807 – 325MHz, single/dual,rail-to-rail input and output, low distortion, low noise precision op amps*, Linear Technology Corporation, 2000. Available online: www.linear-tech.com.

[361] *Technical datasheet of LT8300 – 100 V_{in} micropower isolated flyback converter with 150V / 260mA switch*, Rev. F, Linear Technology Corporation, Aug. 2012.

[362] *Technical datasheet of LTC 3630 – High efficiency, 65v 500ma synchronous step-down converter*, Rev. C, Linear Technology Corporation, Jul. 2012. Available online: http://www.linear.com/docs/41557.

[363] *Technical datasheet of LTC 3805-5 – Adjustable frequency current mode flyback/-boost/sepic DC/DC controller*, Rev. E, Linear Technology Corporation, May 2011. Available online: http://www.linear.com/docs/26143.

[364] *Technical datasheet of LTC3789 – High efficiency, synchronous, 4-switch buck-boost controller*, Rev. A, Linear Technology Corporation, Sep. 2011. Available online: www.linear.com.

[365] *Technical datasheet of MSL2021 – 2-string LED driver with built-in color temperature compensation and adaptive headroom control for high CRI LED luminaires*, Rev. 42062A-LED-02/2013, Atmel Corporation, Feb. 2013.

[366] *Technical datasheet of MTCSiCS – Integral true color sensor – LCC*, Version 5.0, MAZeT GmbH, Feb. 2008.

[367] *Technical datasheet of PHT8N06LT – TrenchMOS™ transistor logic level FET*, Rev. 1.1, Philips Semiconductors Electronics N.V., Jan. 1998.

[368] *Technical datasheet of R6243/6244 – high accuracy DC voltage and current source/-monitor with wide ranges of generation and measurement*, Rev. 2E, Advantest Corporation, Mar. 2003. Available online: www.advantest.com.

[369] *Technical datasheet of REF2925 – 2.5V high accuracy CMOS voltage reference*, SBVS033C – Revised June 2016, Texas Instruments, Jun. 2002.

[370] *Technical datasheet of single-chip WLAN radio CX53111*, Conexant, 2006.

[371] *Technical datasheet of SQ1420EEH – Automotive N-channel 60 V MOSFET*, Rev. D, Vishay Siliconix, Oct. 2011. Available online: www.vishay.com.

[372] *Technical datasheet of SRU8043 – shielded SMD power inductors*, Rev. 01/06, Bourns, Jan. 2006.

[373] *Technical datasheet of TI SimpleLink™ CC3000 module – Wi-Fi 802.11 b/g network processor*, SWRS126, Texas Instruments, Nov. 2012.

[374] *Technical datasheet of WE-CST current sense transformer*, Wuerth Elektronik eiSos GmbH & Co. KG, EMC & Inductive Solutions, Mar. 2014. Available online: www.we-online.com.

[375] *Technical datasheet of XBee multipoint RF modules*, Rev. B1/308, Digi International, 2008.

[376] *Technichal datasheed of DS68 – LUXEON Rebel and LUXEON Rebel ES – color protfolio*, Philips Lumileds Lighting Company, 2012. Available online: www.philipslumileds.com.

[377] The European Parliament and the Council of the European Union, "Directive 2009/244/EC of the european parliament and of the council", *Official Journal L 076*, pp. 3–16, Mar. 2009. Available online: http://eur-lex.europa.eu/LexUriServ/LexUriServ.do?uri=OJ:L:2009:076:0003:0016:EN:PDF.

[378] D. Thomas, E. Wilkie, and J. Irvine, "Comparison of power consumption of WiFi inbuilt internet of things device with Bluetooth Low Energy", in *International Journal of Computer and Information Engineering*, vol. 10, 2016.

[379] A. Thorseth, "Optimization of light quality from color mixing light-emitting diode systems for general lighting", vol. 8278, Feb. 2012. DOI: 10.1117/12.909429.

[380] A. Thorseth *et al.*, "Museum lighting for golden artifacts, with low correlated color temperature, high color uniformity and high color rendering index, using diffusing color mixing of red, cyan, and white-light-emitting diodes", *Proceedings of SPIE - The International Society for Optical Engineering*, vol. 8278, Feb. 2012. DOI: 10.1117/12.908293.

[381] F. Tian, X. Wu, and J. Liu, "Research and realization of LED display system based on combining CAN bus with DMX512 standard", in *International Conference on Audio, Language and Image Processing*, Jul. 2008, pp. 813–818. DOI: 10.1109/ICALIP.2008.4589986.

[382] C. Ticleanu and P. Littlefair, "A summary of LED lighting impacts on health", *International Journal of Sustainable Lighting*, vol. 17, pp. 5–11, Jun. 2015. DOI: 10.26607/ijsl.v17i0.11.

[383] F. Tobagi and L. Kleinrock, "Packet switching in radio channels: part ii - the hidden terminal problem in carrier sense multiple-access and the busy-tone solution", *IEEE Transactions on Communications*, vol. 23, no. 12, pp. 1417–1433, Dec. 1975, ISSN: 1558-0857. DOI: 10.1109/TCOM.1975.1092767.

[384] G. Ungerboeck, "Adaptive Maximum-Likelihood receiver for carrier-modulated data-transmission systems", *IEEE Transactions on Communications*, vol. 22, no. 5, pp. 624–636, May 1974, ISSN: 1558-0857. DOI: 10.1109/TCOM.1974.1092267.

[385] *Universal serial bus power delivery specification*, Version 2.0 + ECNs, Revision 3.0, Feb. 2020.

[386] *User's guide AC power solutions agilent model 6813A – AC power source/analyser*, Edition 4, Update2, Agilent Technologies, Inc., Sep. 2004.

[387] W. van Bommel and G. van den Beld, "Lighting for work: a review of visual and biological effects", *Lighting Research & Technology*, vol. 36, no. 4, pp. 255–266, Dec. 2004. DOI: 10.1191/1365782804li122oa. Available online: https://doi.org/10.1191/1365782804li122oa.

[388] N. van de Meugheuvel *et al.*, "Distributed lighting control with daylight and occupancy adaptation", *Energy and Buildings*, vol. 75, pp. 321–329, Jun. 2014, ISSN: 0378-7788. DOI: https://doi.org/10.1016/j.enbuild.2014.02.016. Available online: http://www.sciencedirect.com/science/article/pii/S0378778814001273.

[389] S. G. Varghese, C. P. Kurian, and V. I. George, "A study of communication protocols and wireless networking systems for lighting control application", in *International Conference on Renewable Energy Research and Applications (ICRERA 2005)*, Nov. 2015, pp. 1301–1306. DOI: 10.1109/ICRERA.2015.7418618.

[390] U. Vishnoi and T. Noll, "Quantitative optimization of highly efficient dedicated CORDIC macros for SoCs in deep-submicron CMOS technologies", *Journal of Electrical & Electronic Systems*, vol. 6, no. 3, pp. 1–6, Sep. 2017.

[391] T. N. Vo *et al.*, "Influence of interference in MIMO power line communication systems", in 18th *IEEE International Symposium on Power Line Communications and Its Applications (ISPLC 2014)*, Mar. 2014, pp. 255–260. DOI: 10.1109/ISPLC.2014.6812320.

[392] F. Wang, C. Tang, and B. Huang, "Multivariable robust control for a red–green–blue LED lighting system", *IEEE Transactions on Power Electronics*, vol. 25, no. 2, pp. 417–428, Feb. 2010, ISSN: 1941-0107. DOI: 10.1109/TPEL.2009.2026476.

[393] F. Wang *et al.*, "Flyback-based three-port topologies for electrolytic capacitor-less LED drivers", *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 5818–5827, Jul. 2017, ISSN: 1557-9948. DOI: 10.1109/TIE.2017.2677303.

[394] H. Wang *et al.*, "Distributed lighting control of locally intelligent luminaire systems", in *IEEE International Conference on Systems, Man, and Cybernetics (SMC 2012)*, Oct. 2012, pp. 3167–3172. DOI: 10.1109/ICSMC.2012.6378278.

[395] Q. Wang *et al.*, "Investigation of visual fatigue under LED lighting based on reading task", *Optik*, vol. 126, no. 15, pp. 1433–1438, Aug. 2015, ISSN: 0030-4026. DOI: https://doi.org/10.1016/j.ijleo.2015.04.033. Available online: http://www.sciencedirect.com/science/article/pii/S0030402615002430.

[396] S. Wang *et al.*, "Design and implementation of a single-stage high-efficacy LED driver with dynamic voltage regulation", in *IEEE International Conference on Systems, Man, and Cybernetics*, Oct. 2013, pp. 1438–1443. DOI: 10.1109/SMC.2013.248.

[397] X. Wang, T. Tjalkens, and J. Linnartz, "Smart office lighting control using occupancy sensors", in 14th *IEEE International Conference on Networking, Sensing and Control (ICNSC 2017)*, May 2017, pp. 453–458. DOI: 10.1109/ICNSC.2017.8000135.

[398] Y. Wang, J. M. Alonso, and X. Ruan, "A review of LED drivers and related technologies", *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 5754–5765, Jul. 2017, ISSN: 1557-9948. DOI: 10.1109/TIE.2017.2677335.

[399] Z. Wang, "CMOS adjustable schmitt triggers", *IEEE Transactions on Instrumentation and Measurement*, vol. 40, no. 3, pp. 601–605, Jun. 1991, ISSN: 1557-9662. DOI: 10.1109/19.87026.

[400] A. Webb, "Considerations for lighting in the built environment: Non-visual effects of light", *Energy and Buildings*, vol. 38, no. 7, pp. 721–727, Aug. 2006, Special Issue on Daylighting Buildings, ISSN: 0378-7788. DOI: https://doi.org/10.1016/j.enbuild.2006.03.004. Available online: http://www.sciencedirect.com/science/article/pii/S0378778806000648.

[401] Y. Wen, J. Granderson, and A. Agogino, "Towards embedded wireless-networked intelligent daylighting systems for commercial buildings", in *IEEE International Conference on Sensor Networks, Ubiquitous, and Trustworthy Computing (SUTC 20006)*, vol. 1, Jun. 2006. DOI: 10.1109/SUTC.2006.1636196.

[402] A. Wilkins, J. Veitch, and B. Lehman, "LED lighting flicker and potential health concerns: IEEE standard PAR1789 update", Oct. 2010, pp. 171–178. DOI: 10.1109/ECCE.2010.5618050.

[403] C. S. Wong *et al.*, "An alternative approach to LED driver design based on high-voltage driving", *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2465–2475, Mar. 2016, ISSN: 1941-0107. DOI: 10.1109/TPEL.2015.2434496.

[404] S. Wong, "High voltage AC to low-voltage DC converter", US Patent 5,818,708, Oct. 1998. Available online: http://www.google.com/patents/US5818708.

[405] Woo Suk Lee and S. H. Hong, "Implementation of a KNX-ZigBee gateway for home automation", in 13th *International Symposium on Consumer Electronics*, May 2009, pp. 545–549. DOI: 10.1109/ISCE.2009.5156866.

[406] C. Wu *et al.*, "Multistring LED backlight driving system for LCD panels with color sequential display and area control", *IEEE Transactions on Industrial Electronics*, vol. 55, no. 10, pp. 3791–3800, Oct. 2008, ISSN: 1557-9948. DOI: 10.1109/TIE.2008.921206.

[407] X. Wu, J. Zhang, and Z. Qian, "A simple two-channel LED driver with automatic precise current sharing", *IEEE Transactions on Industrial Electronics*, vol. 58, no. 10, pp. 4783–4788, Oct. 2011, ISSN: 1557-9948. DOI: 10.1109/TIE.2011.2109339.

[408] G. Wyszecki and W. Stiles, *Color Science: Concepts and Methods, Quantitive Data and Formulae*, 2nd Edition. John Wiley & Sons, Aug. 2000.

[409] Y. Xia, O. Wan, and K. Cheah, "OLED for human centric lighting", *Opt. Mater. Express*, vol. 6, no. 6, pp. 1905–1913, Jun. 2016. DOI: 10.1364/OME.6.001905. Available online: http://www.osapublishing.org/ome/abstract.cfm?URI=ome-6-6-1905.

[410] X. Xu and X. Wu, "High dimming ratio LED driver with fast transient boost converter", in 39*th IEEE Power Electronics Specialists Conference*, Jun. 2008, pp. 4192–4195. DOI: 10.1109/PESC.2008.4592613.

[411] Y. Yamagishi and A. Mita, "Control algorithm of lighting color for LED considering human's negative feeling", Mar. 2014. DOI: 10.1117/12.2041655.

[412] Y. Yan *et al.*, "A survey on smart grid communication infrastructures: motivations, requirements and challenges", *IEEE Communications Surveys Tutorials*, vol. 15, no. 1, pp. 5–20, Jan. 2013, ISSN: 2373-745X. DOI: 10.1109/SURV.2012.021312.00034.

[413] H. Yang *et al.*, "12.7A 96%-efficiency and 0.5%-current-cross-regulation single-inductor multiple floating-output LED driver with 24b color resolution", in *IEEE International Solid-State Circuits Conference (ISSCC 2016)*, Jan. 2016, pp. 230–231. DOI: 10.1109/ISSCC.2016.7417991.

[414] J. Yang *et al.*, "Device-free occupant activity sensing using WiFi-enabled IoT devices for smart homes", *IEEE Internet of Things Journal*, vol. 5, no. 5, pp. 3991–4002, Oct. 2018, ISSN: 2372-2541. DOI: 10.1109/JIOT.2018.2849655.

[415] L. Yang, W. Yu, and J. Zhang, "Variable frequency constant current control method for switched-capacitor converter based automotive LED driver", *IEEE Access*, vol. 7, pp. 42 094–42 106, Mar. 2019, ISSN: 2169-3536. DOI: 10.1109/ACCESS.2019.2907983.

[416] Y. Ye *et al.*, "Single-switch multichannel current-balancing LED drive circuits based on optimized SC techniques", *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4761–4768, Aug. 2015, ISSN: 1557-9948. DOI: 10.1109/TIE.2015.2408813.

[417] P. Yi, A. Iwayemi, and C. Zhou, "Developing ZigBee deployment guideline under WiFi interference for smart grid applications", *IEEE Transactions on Smart Grid*, vol. 2, no. 1, pp. 110–120, Mar. 2011, ISSN: 1949-3061. DOI: 10.1109/TSG.2010.2091655.

[418] H. Yoon *et al.*, "Circadian-tunable perovskite quantum dot-based down-converted multi-package white LED with a color fidelity index over 90", *Scientific Reports*, vol. 7, Jun. 2017. DOI: 10.1038/s41598-017-03063-7.

[419] S. Yoon, D. Kang, and S. Bahk, "Multichannel CSMA/CA protocol for OFDMA-based broadband power-line communications", *IEEE Transactions on Power Delivery*, vol. 28, no. 4, pp. 2491–2499, Oct. 2013, ISSN: 1937-4208. DOI: 10.1109/TPWRD.2013.2271316.

[420] G. Young Yun *et al.*, "A field survey of visual comfort and lighting energy consumption in open plan offices", *Energy and Buildings*, vol. 46, pp. 146–151, Mar. 2012, Sustainable and healthy buildings, ISSN: 0378-7788. DOI: https://doi.org/10.1016/j.enbuild.2011.10.035. Available online: http://www.sciencedirect.com/science/article/pii/S0378778811004981.

[421] M. S. Yousuf, S. Z. Rizvi, and M. El-Shafei, "Power line communications: An overview – Part II", in 3rd *International Conference on Information and Communication Technologies: From Theory to Applications*, Apr. 2008, pp. 1–6. DOI: 10.1109/ICTTA.2008.4530268.

[422] M. S. Yousuf and M. El-Shafei, "Power line communications: An overview – Part I", in *Innovations in Information Technologies (IIT 2007)*, Nov. 2007, pp. 218–222. DOI: 10.1109/IIT.2007.4430363.

[423] S. Yu *et al.*, "Smart automotive lighting for vehicle safety", *IEEE Communications Magazine*, vol. 51, no. 12, pp. 50–59, Dec. 2013, ISSN: 1558-1896. DOI: 10.1109/MCOM.2013.6685757.

[424] T. Zekorn *et al.*, "An accurate high-voltage supply-referred low-impedance reference-voltage for efficiency enhancement of the high-side switching process", in 26th *IEEE International Conference on Electronics, Circuits and Systems (ICECS 2019)*, Dec. 2019, pp. 390–393. DOI: 10.1109/ICECS46596.2019.8964643.

[425] Q. Zhai, M. Luo, and X. Liu, "The impact of illuminance and colour temperature on viewing fine art paintings under LED lighting", *Lighting Research and Technology*, vol. 47, Jul. 2015. DOI: 10.1177/1477153514541832.

[426] X. Zhan, H. Chung, and R. Zhang, "Investigation into the use of single inductor for driving multiple series-connected LED channels", *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3034–3050, Apr. 2017, ISSN: 1941-0107. DOI: 10.1109/TPEL.2016.2576279.

[427] X. Zhan, W. Wang, and H. Chung, "A neural-network-based color control method for multi-color LED systems", *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7900–7913, Aug. 2019, ISSN: 1941-0107. DOI: 10.1109/TPEL.2018.2880876.

[428] X. Zhan, W. Wang, and H. S. Chung, "A novel color control method for multicolor LED systems to achieve high color rendering indexes", *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8246–8258, Oct. 2018, ISSN: 1941-0107. DOI: 10.1109/TPEL.2017.2785307.

[429] J. Zhang, J. Wang, and X. Wu, "A capacitor-isolated LED driver with inherent current balance capability", *IEEE Transactions on Industrial Electronics*, vol. 59, no. 4, pp. 1708–1716, Apr. 2012, ISSN: 1557-9948. DOI: 10.1109/TIE.2011.2138111.

[430] J. Zhang, F. Lee, and M. Jovanovic, "An improved CCM single-stage PFC converter with a low frequency auxiliary switch", *Power Electronics, IEEE Transactions on*, vol. 18, no. 1, pp. 44–50, Feb. 2003, ISSN: 0885-8993.

[431] X. Zhao *et al.*, "Does BTLE measure up against WiFi? A comparison of indoor location performance", in 20th *European Wireless Conference*, May 2014, pp. 1–6.

[432] Z. Zhao and R. Wang, "An accuracy requirement analysis for LED brightness and color correction system", in *Proceedings International Conference on Transportation, Mechanical, and Electrical Engineering TMEE 2011*, Dec. 2011, pp. 962–965. DOI: 10.1109/TMEE.2011.6199363.

[433] Y. Zhu *et al.*, "Effects of illuminance and correlated color temperature on daytime cognitive performance, subjective mood, and alertness in healthy adults", *Environment and Behavior*, vol. 51, no. 2, pp. 199–230, Oct. 2017. DOI: 10.1177/0013916517738077. Available online: https://doi.org/10.1177/0013916517738077.

[434] H. Zou *et al.*, "WinLight: a WiFi-based occupancy-driven lighting control system for smart building", *Energy and Buildings*, vol. 158, pp. 924–938, Jan. 2018, ISSN: 0378-7788. DOI: https://doi.org/10.1016/j.enbuild.2017.09.001. Available online: http://www.sciencedirect.com/science/article/pii/S0378778817313907.

Appendix A

Additional Material on Digital Load-Side Transmission

A.1 DLT Fundamentals

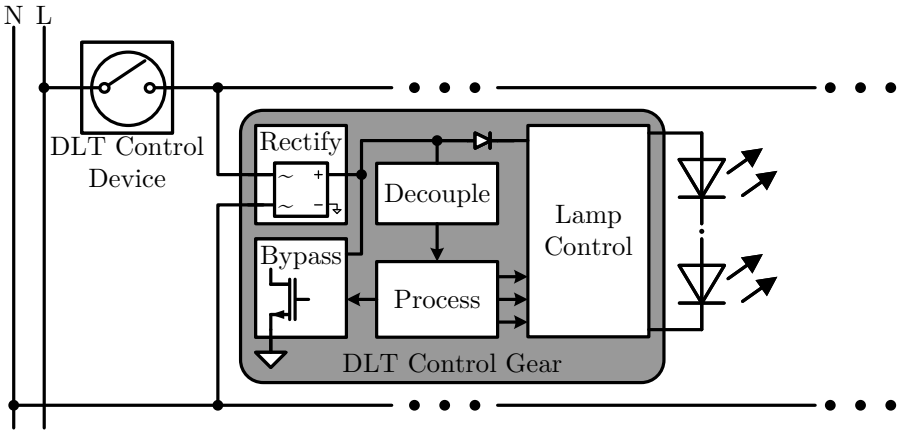


Figure A.1: Internal setup and wiring of a DLT CG according to the official DLT standard [106].

Fig. A.1 depicts the wiring of DLT CG and a generalized block diagram of its internal setup according to the official DLT standard [106].

A.2 DLT FW-RX

All of the presented DLT FW-RXs rely on the control of a μC acting as the smart processing unit. It provides specific timing control for the HC bypass circuit, runs the decoding routines and processes received commands. For several practical reasons, the smart processing unit has been setup on a separated PCB. Fig. A.2 depicts a photo of the hardware implementation for this so-called universal control board (UCB). The UCB has been developed for the use in multiple hardware implementations fulfilling various purposes. Besides handling different DLT FW-RXs, it is also capable of steering a DLT REV-TX, copes with different communication interfaces, computes precise brightness and color adjustments and even controls PWM based LED drivers. Consequently, this board has also been used in different versions within many other works and thesis at the *"Integrated Analog Circuits and RF System Laboratory"* at RWTH Aachen University [97], [235], [243], [305]. The board contains a powerful μC [345], a low-power WiFi-module [357], a 2.4 GHz RF-IC [347] enabling

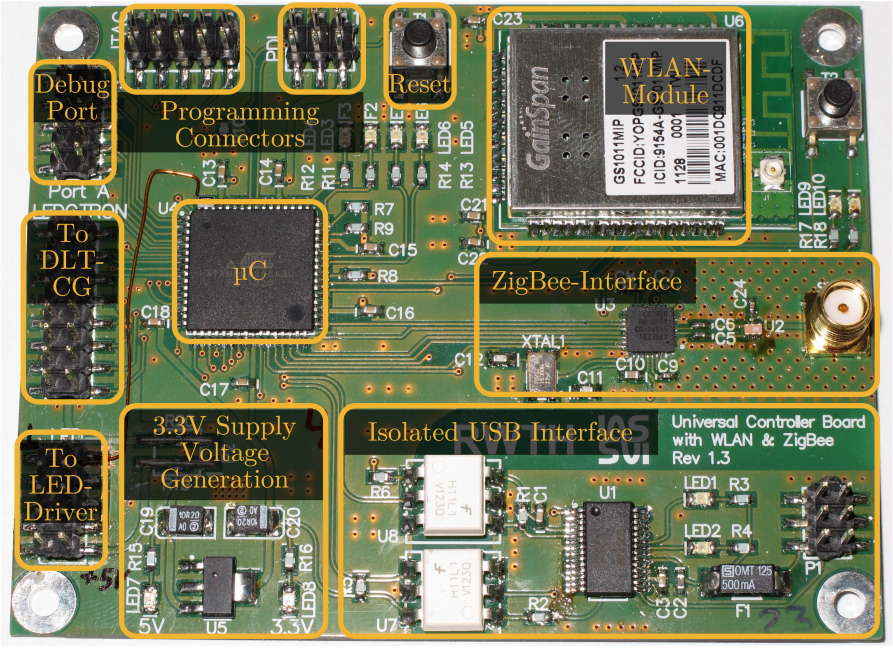


Figure A.2: Photograph of the implemented UCB with a powerful ATxmega μC [345] featuring multiple connectors and interfaces.

ZigBee communication and an isolated USB-interface [356], [358] for connecting a PC while operating on mains voltage. Furthermore, multiple frame connectors offer the possibility to attach other boards, such as a DLT FW-RX or LED driving stages featuring multiple color channels.

Fig. A.3 illustrates the flowchart of the alternative DLT frame decoder that is needed for evaluating detector concepts B and C in the a DLT FW-RX. This decoding routine has also been implemented on the MCU of the aforementioned UCB.

Fig. A.4 illustrates implementation and dimensioning of a passive analog bandpass filter suited for application in a DLT FW-RX. The presented design is in fact used as a benchmark design. It should however be noted that the component values – in particular the capacitance – are to big for a monolithically integrated design of a DLT CG. Fig. A.5a and Fig. A.5b show measurements

Table A.1: Evaluation of DLT-FW detectors' TERs in 24 h measurements.

Detector Concepts	**Recorded Telegrams**	**Detected Errors**	**TER in ppm**
Concept *A*:			
Analog Bandpass ($C_2 = 49\,\text{pF}$)	1083037	87	80
Analog Bandpass ($C_2 = 25\,\text{pF}$)	1079471	61	57
Concept *B*:			
Digital Bandpass	1131627	50	44
Concept *C*:			
Mixed-Signal Subtraction Filter	1080507	1556	1440
Benchmarks built of Concept *A*:			
Passive Bandpass	1083037	32	30
Active Bandpass (not integrable)	1079471	28	26

of the filtered signal after the passive analog BP at the Schmitt-Trigger input for the presented implementation.

Fig. A.6 shows an active analog bandpass filter with different component sizes. Particularly capacitance C_1 is increased significantly compared to the version presented in chapter 3.2.2 of this thesis, which makes it unsuitable for a monolithic integration. If it is however acceptable to place the large input capacitor C_1 as an external component, this concept implementation could also be realized in an ASIC. The bigger capacitance and different dimensioning in fact enhance overall robustness slightly. Fig. A.7a and Fig. A.7b show measurements of the filtered signal after the active bandpass filter at the Schmitt-Trigger input for an implementation with $C_2 = 470\,\text{pF}$ and $C_2 = 1\,\text{pF}$.

During the 24 h longterm robustness measurements outlined in table 3.4 in section 3.2.3 a TER of 30 ppm has been measured for the passive analog benchmark design, while the active bandpass with non-integrable component sizes realized a comparable value of 26 ppm. Table A.1 illustrates the detailed results in conjunction with the already shown measurement performance of table 3.4.

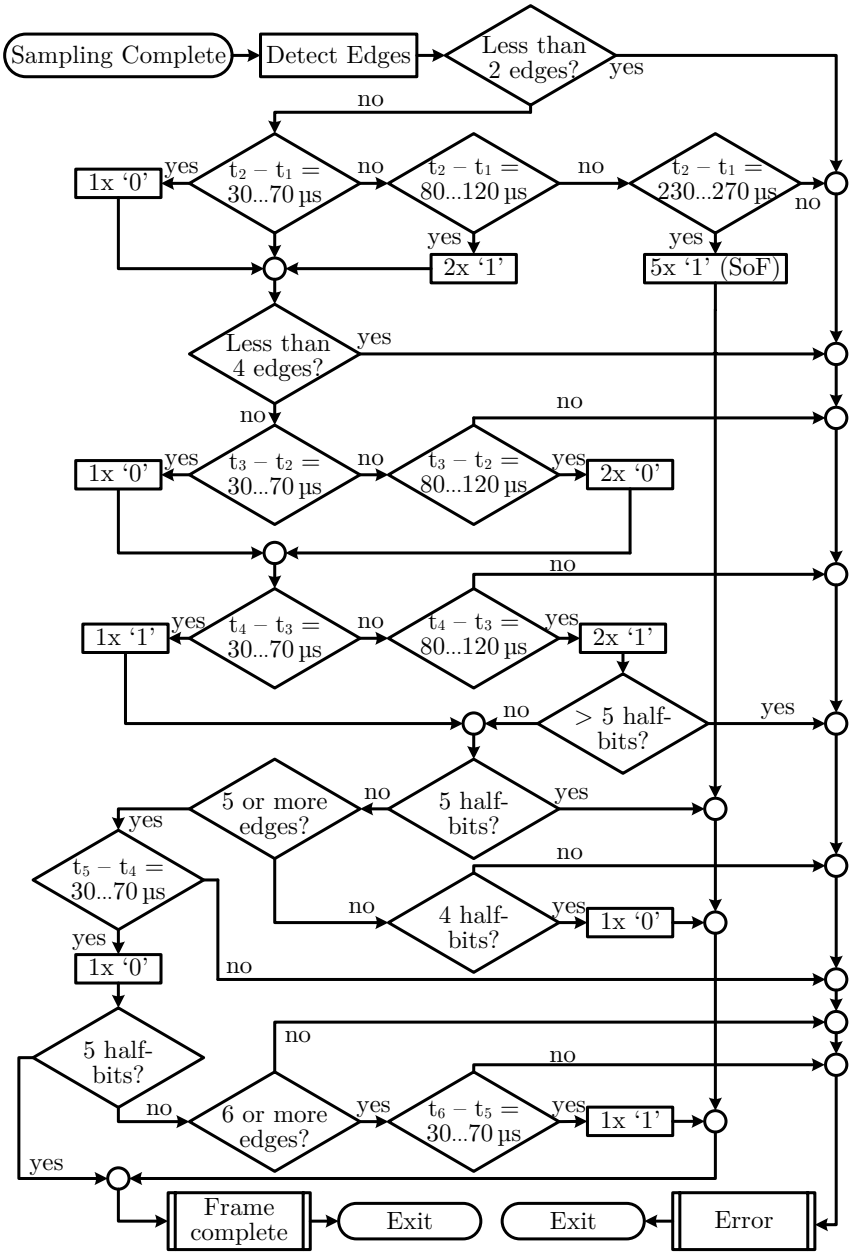


Figure A.3: Flowchart of implemented DLT frame decoder for concepts B and C.

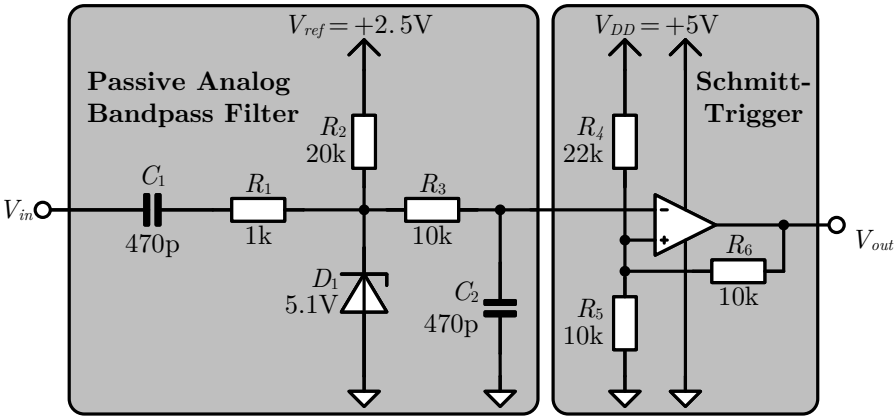
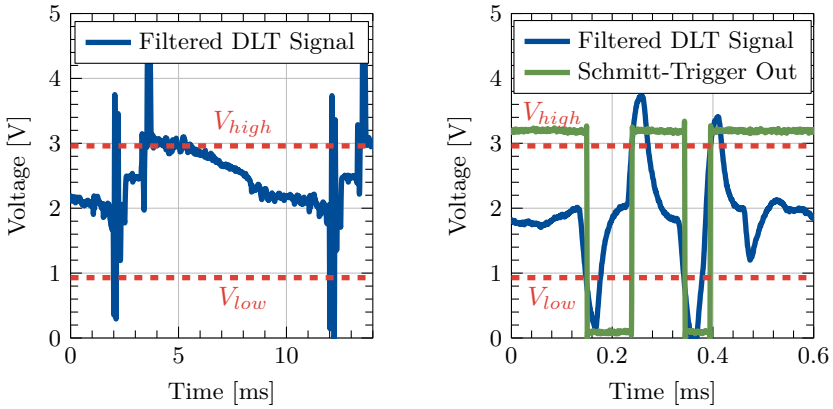


Figure A.4: Schematics of benchmark design for DLT FW-RX concept *A*: Passive analog bandpass filter with Schmitt-Trigger.



(a) Measured output signal of passive analog bandpass filter.

(b) Close-up shot of measured FW-RX signals for passive analog BP filter.

Figure A.5: Measured waveform signals of detector concept *A* in a DLT FW-RX using the passive analog bandpass filter configuration.

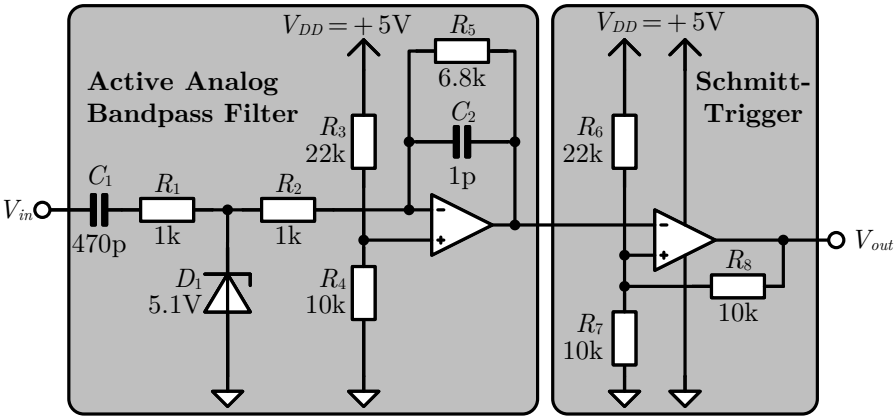
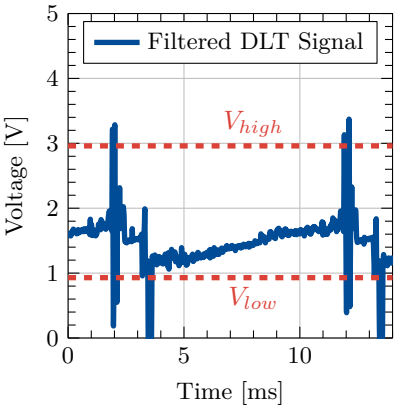
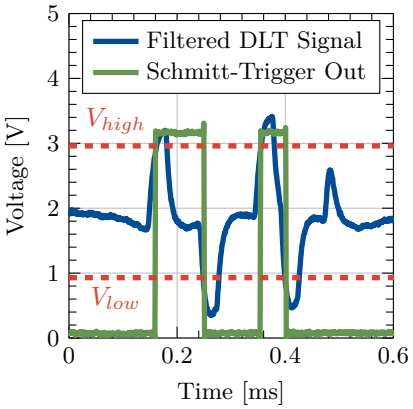


Figure A.6: Schematics of benchmark design for DLT FW-RX concept *A*: An active analog BP with non-integrable component sizes.



(a) Measured output signal of active analog bandpass filter.



(b) Close-up shot of measured FW-RX signals for active analog BP filter.

Figure A.7: Measured waveform signals of detector concept *A* using an active analog bandpass with non-integrable component sizes.

A.3 DLT Control Device Implementation

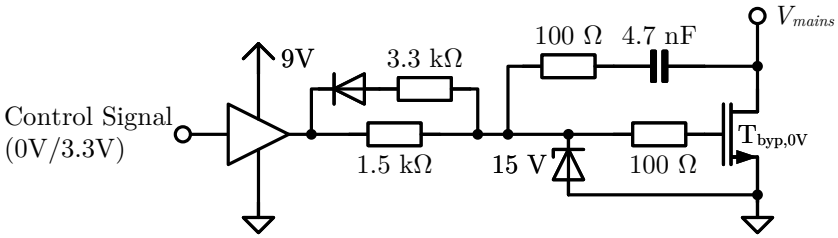


Figure A.8: Circuitry of the modulating 0 V bypass of a DLT CD from [240].

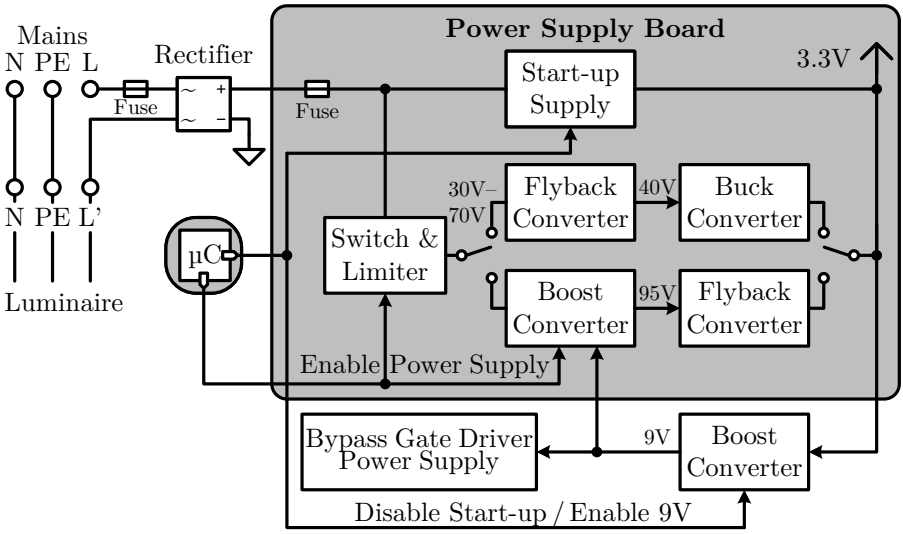


Figure A.9: Hardware setup of the power supply board for a DLT CD from [240].

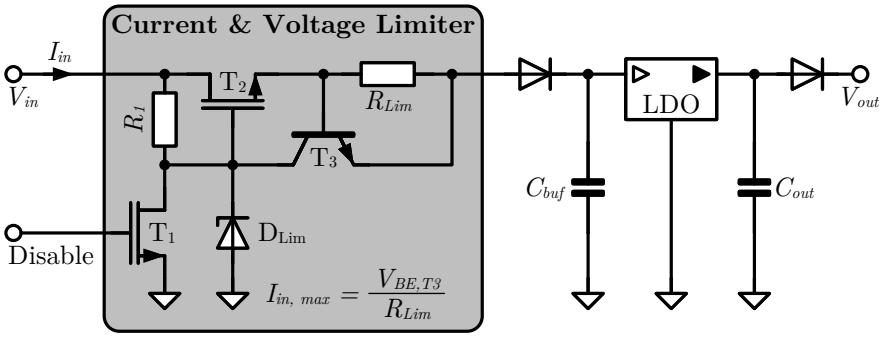


Figure A.10: Start-up supply circuit for a DLT CD from [240].

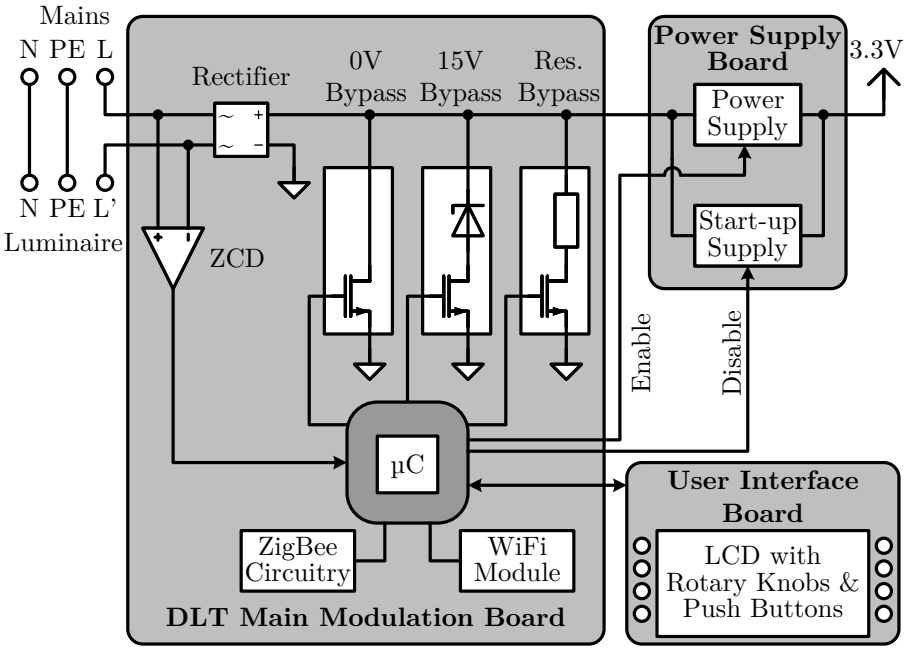


Figure A.11: System concept & board assembly of proposed DLT CD from [240].

A.4 Power Supply Calcuations for a DLT CD Enabling WLAN Access

In case of a voltage drop of $V_{drop} = 5\,\mathrm{V}$ across attached CGs, the available energy during the HC phase of the DLT supply period calculates to

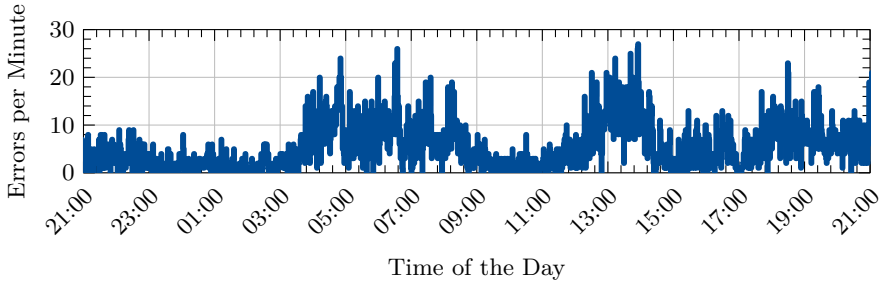
$$W_{CD,5Vdrop} = \int_{t_1}^{t_2} (\hat{V}_{grid} \cdot \sin(2\pi \cdot f_{grid} \cdot t) - V_{drop}) \cdot I_{CD,max}\, dt \quad \text{(A.1)}$$

$$= 6.42\,\mathrm{mJ}\,,$$

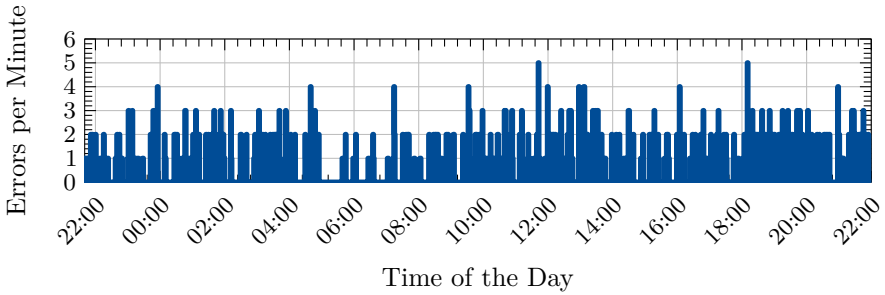
$$\Rightarrow P_{CD,5Vdrop} = 642\,\mathrm{mW}\,. \quad \text{(A.2)}$$

The actual energy demand or moreover power consumption of a CD's WiFi module strongly depends on the communication amount, like occurrence of a data transmission and size of the transmitted data. Furthermore the selected beaconing period can be tuned to influence power consumption, but of course also affects latency. Based on equations 3.15 to 3.19 the required power demand can be calculated for different assumptions of transmission occurrence $T_{COM,request}$, beaconing period $T_{beaconing}$ and current draw of the WiFi module I_{WLAN}. The actual transmission and active times should be kept at their original limits of $t_{WLAN,TRX,on} \approx 100\,\mathrm{ms}$ $t_{beacon,active} \leq 15\,\mathrm{ms}$, respectively, as these values represent good approximations of the described application scenario. The sleep time during a beaconing phase $t_{beacon,sleep}$ needs of course to be adapted to the selected beaconing period $T_{beaconing}$. In dependence of transmission occurrence $T_{COM,request}$, beaconing period $T_{beaconing}$ and current draw of the WiFi module I_{WLAN}, the final efficiency requirement can thus be computed as function of the considered use cases taking a realistic voltage drop across attached CGs into account. The power demand of the association phase is left out of these considerations. It is in fact assumed that association power demand is provided by an external power supply, e.g. by a start-up supply or a big storage capacitor, or that a realistic scenario like the one described in section 3.3.1 applies.

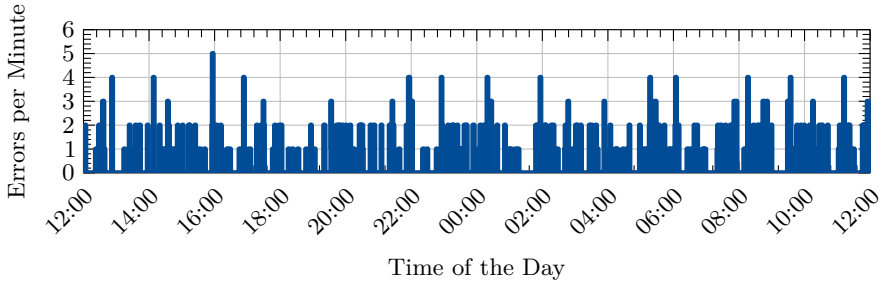
A.5 REV-RX Concept B: TER measurements



(a) Recorded telegram errors of DLT REV-RX concept B with $I_{mod,set} = 25\,\mathrm{mA}$.



(b) Recorded telegram errors of DLT REV-RX concept B with $I_{mod,set} = 28\,\mathrm{mA}$.



(c) Recorded telegram errors of DLT REV-RX concept B with $I_{mod,set} = 30\,\mathrm{mA}$.

Figure A.12: 24 h measurements of DLT REV-RX B for different $I_{mod,set}$.

A.6 Derivation of the Mean Power Consumption for the Presented DLT REV-TX

Using equation 3.40, a more generalized expression can be stated as follows,

$$P_{REV\text{-}TX} = \frac{1}{T_{grid}} \int_{t_{REV\text{-}TX,start}}^{t_{REV\text{-}TX,start}+T_{frame}} \left| \widehat{V}_{grid} \cdot \sin(2\pi \cdot f_{grid} \cdot t) \cdot I_{mod}(t) \right| dt\,. \quad \text{(A.3)}$$

Equation A.3 yields equation 3.40 by choosing a constant modulation depth for the transient reverse transmission with $I_{mod}(t) = I_{mod,set}$ and setting the beginning of the modulation to the earliest possible point in time with $t_{REV\text{-}TX,start} = t_7$. Assuming a constant modulation depth $I_{mod,set}$ is valid for the presented case of an OOK. If a digital '1' is transmitted, the selected $I_{mod,set}$ level is used as a constant in the calculations. For a digital '0' $I_{mod,set}$ equals zero and hence no contribution is added to the transmission power. Thus it needs to be distinguished between the respective cases. The constant amplitude can be extracted from the integral of equation A.3. A high level is transmitted for the length of one half-bit with $t_{HB} = 50\,\mu s$ yielding the subsequent formula,

$$\Rightarrow P_{REV\text{-}TX,HB} = \frac{\widehat{V}_{grid} \cdot I_{mod,set}}{T_{grid}} \int_{t_{REV\text{-}TX,start}}^{t_{REV\text{-}TX,start}+t_{HB}} |\sin(2\pi \cdot f_{grid} \cdot t)|\, dt\,. \quad \text{(A.4)}$$

$$\text{with:} \quad A = \frac{\widehat{V}_{grid} \cdot I_{mod,set}}{T_{grid}} \quad \text{(A.5)}$$

The starting point of the DLT backward transmission can be at any time within the data period after t_7 has passed considering that transmission of a single frame ($T_{frame} = 300\,\mu s$) is completed before t_8 is reached. The latest possible starting point with respect to a mains half-wave is thus $t_{REV\text{-}TX,start,latest} = 550\,\mu s$ before the next zero crossing. In oder to calculate an averaged power consumption for a realistic case, $t_{REV\text{-}TX,start,real}$ is thus selected to be in the middle of t_7 and $t_{REV\text{-}TX,start,latest}$, which gives $t_{REV\text{-}TX,start,real} = 675\,\mu s$ before the next zero crossing. With respect to the 50 Hz European utility grid one half-wave lasts exactly 10 ms. The corresponding starting points for worst case (WC), real case (RC) and best case (BC) are thus selected to $t_{REV\text{-}TX,WC,start} = 9.2\,ms$, $t_{REV\text{-}TX,RC,start} = 9.325\,ms$ and $t_{REV\text{-}TX,BC,start} = 9.45\,ms$, respectively.

In order to calculate the average transmission energy of a typical DLT sequence for the backward modulation, it is assumed that a DLT brightness

telegram consists of eight frames and hence 16 bit are transferred. To account for transmission energy and not power consumption, the division by T_{grid} is left out in the following computations and a (constant) pre-factor $B = I_{mod,set} \cdot \widehat{V}_{grid}$ is considered instead of A. It should be noted that a similar and consistent calculation has been provided in [97]. The assumed telegram consists of a SoT frame followed by seven other frames, which incorporate all a SoF sequence and then one out of the four possible symbols '00', '10', '01' or '11' as depicted in Fig. 3.6. The energy for a SoT and for a SoF is calculated as follows,

$$B = \widehat{V}_{grid} \cdot I_{mod,set} = \sqrt{2} \cdot 230\,\mathrm{V} \cdot I_{mod,set}\,, \tag{A.6}$$

$$E_{SoT} = B \cdot \int_{t_{REV\text{-}TX,start}}^{t_{REV\text{-}TX,start}+T_{frame}-t_{HB}} |\sin(2\pi \cdot f_{grid} \cdot t)|\,dt\,, \tag{A.7}$$

$$E_{SoF} = B \cdot \int_{t_{REV\text{-}TX,start}}^{t_{REV\text{-}TX,start}+t_{HB}} |\sin(2\pi \cdot f_{grid} \cdot t)|\,dt\,, \tag{A.8}$$

Based on equation A.8, the energy of a symbol can be determined. For simplicity reasons $t_{REV\text{-}TX,start}$ is referred to as t_{start} in the following. The subsequent formulas summarize the transmission energy for each of the four symbols '00', '10', '01' and '11',

$$E_{00} = B \cdot \int_{t_{start}+t_{HB}}^{t_{start}+2t_{HB}} |\sin(2\pi \cdot f_{grid} \cdot t)|\,dt + \int_{t_{start}+3t_{HB}}^{t_{start}+4t_{HB}} |\sin(2\pi \cdot f_{grid} \cdot t)|\,dt\,, \tag{A.9}$$

$$E_{01} = B \cdot \int_{t_{start}+t_{HB}}^{t_{start}+2t_{HB}} |\sin(2\pi \cdot f_{grid} \cdot t)|\,dt + \int_{t_{start}+4t_{HB}}^{t_{start}+5t_{HB}} |\sin(2\pi \cdot f_{grid} \cdot t)|\,dt\,, \tag{A.10}$$

$$E_{10} = B \cdot \int_{t_{start}+2t_{HB}}^{t_{start}+3t_{HB}} |\sin(2\pi \cdot f_{grid} \cdot t)|\,dt + \int_{t_{start}+3t_{HB}}^{t_{start}+4t_{HB}} |\sin(2\pi \cdot f_{grid} \cdot t)|\,dt\,, \tag{A.11}$$

$$E_{11} = B \cdot \int_{t_{start}+2t_{HB}}^{t_{start}+3t_{HB}} |\sin(2\pi \cdot f_{grid} \cdot t)|\,dt + \int_{t_{start}+4t_{HB}}^{t_{start}+5t_{HB}} |\sin(2\pi \cdot f_{grid} \cdot t)|\,dt\,, \tag{A.12}$$

Assuming each symbol occurs with the same probability, the summation of all (four) symbol energies divided by their quantity (which is four) gives the mean symbol energy. Adding E_{SoF} thus results in the average frame energy for one of the seven data frames,

$$E_{frame,avg} = E_{SoF} + \frac{1}{4}\left(E_{00} + E_{01} + E_{10} + E_{11}\right) . \tag{A.13}$$

Additionally, the SoT energy has to be added to seven times the average frame energy and it needs to be divided by the total number of frames. These considerations finally yield the total averaged energy of a mean telegram.

$$E_{telegram,avg} = \frac{1}{8} \cdot E_{SoT} + \frac{7}{8} \cdot E_{frame,avg} . \tag{A.14}$$

Consequently, the total mean power consumption of a reverse transmission can be calculated to

$$P_{REV\text{-}TX,mean} = \frac{1}{T_{grid}} \cdot E_{telegram,avg} , \tag{A.15}$$

$$= \frac{1}{T_{grid}} \cdot \left(\frac{1}{8} E_{SoT} + \frac{7}{8}\left(E_{SoF} + \frac{1}{4}\left(E_{00} + E_{01} + E_{10} + E_{11}\right)\right)\right) . \tag{A.16}$$

Appendix B

Additional Material on Color Mixing & Control

B.1 CIE 1976 (u'v') Chromaticity Diagram

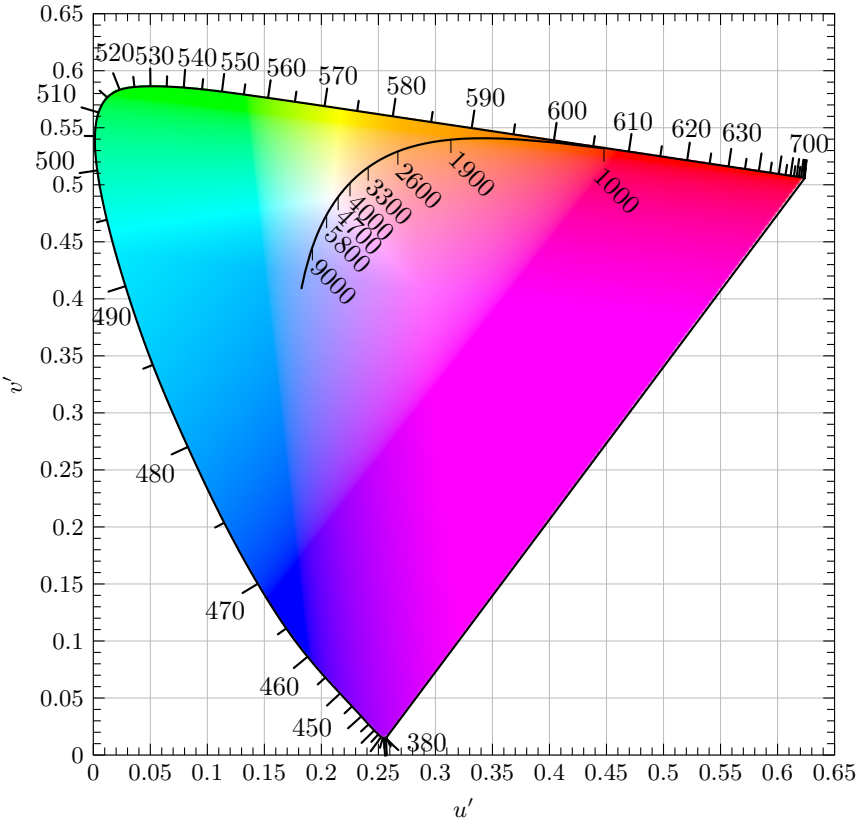


Figure B.1: CIE 1976 (u', v')-chromaticity diagram showing different CTs on the planckian locus.

B.2 Computation of CCT from Realized (x,y) – Color Coordinates

To deduce the achieved CCT from the realized (x, y)-coordinates, the calculation rules from McCamy [260] (equation B.1) and from Hernández-Andrés, Lee,

and Romero [144] (equation B.2) have been applied in this thesis. While equation B.1 derived by McCamy [260] gives good results for CCTs in the range from 2000 K to 12 500 K, it has only been used for CCTs below 3000 K because the computation by equation B.2 [144] yields more accurate and better results for CCTs above 3000 K. If much higher CCTs than the specified upper limit of 50 000 K are targeted, Hernández-Andrés, Lee, and Romero [144] provide also other fitting curves for CCTs up to 800 000 K in their paper.

Consequently, this thesis applies equation B.1, if $2000\,\mathrm{K} \leq CCT \leq 3000\,\mathrm{K}$,

$$CCT(x,y) = a \cdot n_1^3 + b \cdot n_1^2 + c \cdot n_1 + d\,, \tag{B.1}$$

$$\text{with} \quad n_1 = \frac{x - 0.3320}{y - 0.1858}\,,$$

and using the coefficients denoted in table B.1.

Table B.1: Coefficients used in equation B.1 from [260].

Coefficient	a	b	c	d
Applied Values	449	3525	6823.3	5520.33

If $3000\,\mathrm{K} \leq CT \leq 50\,000\,\mathrm{K}$ obtains, equation B.2 is used instead,

$$A_0 + A_1 \cdot \exp\left(\frac{-n_2}{t_1}\right) + A_2 \cdot \exp\left(\frac{-n_2}{t_2}\right) + A_3 \cdot \exp\left(\frac{-n_2}{t_3}\right)\,, \tag{B.2}$$

$$\text{with} \quad n_2 = \frac{x - 0.3366}{y - 0.1735}\,,$$

and using the coefficients denoted in table B.2.

Table B.2: Coefficients used in equation B.2 from [144].

Coefficient	A_0	A_1	A_2	A_3
Value	-949.86315	6253.80338	28.70599	0.00004
Coefficient	t_1	t_2	t_3	
Value	0.92159	0.20039	0.07125	

B.3 Photometric and radiometric quantities

Table B.3: Summary of photometric and radiometric quantities.

Photometric Quantities			
Quantity	**Symbol**	**Unit**	**Explanation**
Luminous Flux	Φ_v	$\mathrm{lm} = \mathrm{cd} \cdot \mathrm{sr}$	Luminous energy per unit time.
Luminous Intensity	I_v	$\mathrm{cd} = \mathrm{lm/sr}$	Luminous flux per unit solid angle.
Illuminance	E_v	$\mathrm{lx} = \mathrm{lm/m^2}$	Luminous flux incident on a surface.
Luminance	L_v	$\mathrm{cd/m^2}$	Luminous flux per unit solid angle per unit projected source area.
Luminous Efficiency	η_v	lm/W	Luminous flux divided by the dissipated (electrical) power.
Luminous Efficacy	K_v	lm/W	Ratio of luminous to radiant flux.
Radiometric Quantities			
Quantity	**Symbol**	**Unit**	**Explanation**
Radiant Flux	Φ_e	W	Radiant energy per unit time. Also called *"radiant power"*.
Radiant Intensity	I_e	W/sr	Radiant flux per unit solid angle.
Irradiance	E_e	$\mathrm{W/m^2}$	Radiant flux received by a surface per unit area.
Radiance	L_e	$\mathrm{W/(m^2\,sr)}$	Radiant flux per unit solid angle per unit projected area.
Radiant Efficiency	η_v	1	Radiant flux normalized by the dissipated (electrical) power.

Appendix C

Luminaire Demonstrators



Figure C.1: Arrangement of self-developed luminaires and control devices.

The photograph C.1 shows the self-developed luminaires, which are three spotlight demonstrators and one out of the four constructed table lamps. Suitable control devices are a tablet with self-programmed control software [248], a PC with the MATLAB® GUI and the DLT CD with extended functionality.

C.1 Spotlight Demonstrator

The three spotlight demonstrators are each equipped with a 120 W power supply, a DLT FW-RX and REV-TX, an 8-channel LED driver and a UCB handling the color mixing algorithm and all digital control functions. This self-developed luminaire incorporates six independently adjustable LED primaries and two additional white channels for higher luminous output, if desired. Additionally, a small color sensor is integrated on the LED board (LeBo).



Figure C.2: Example of 120 W spotlight demonstrator.

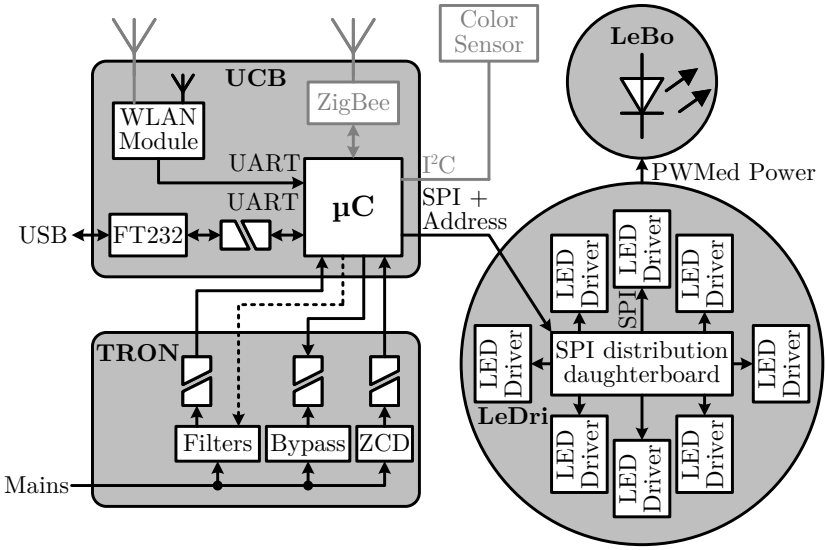


Figure C.3: Board assembly and data distribution of spotlight demonstrator.

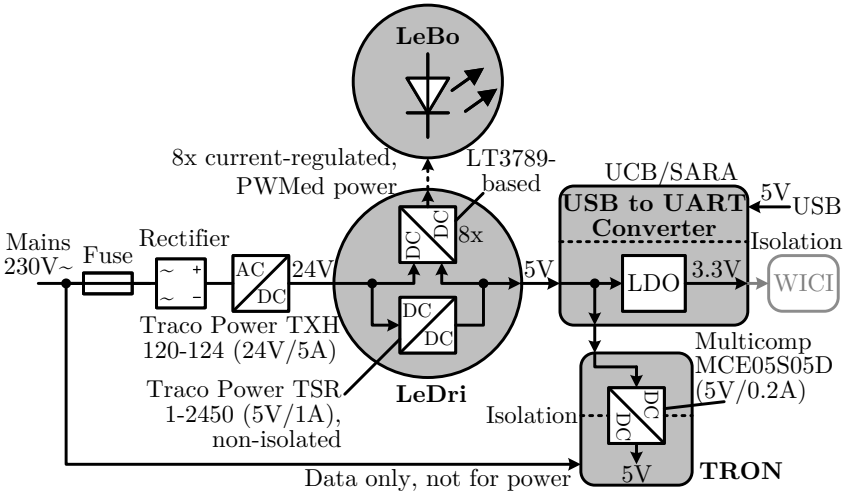
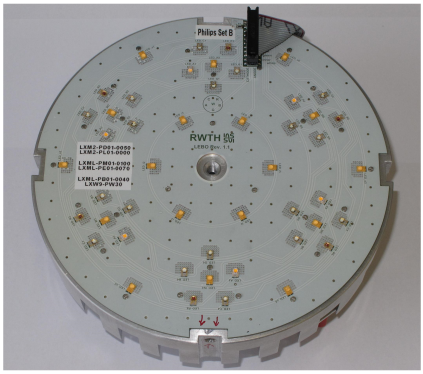


Figure C.4: Power distribution of the spotlight luminaire.



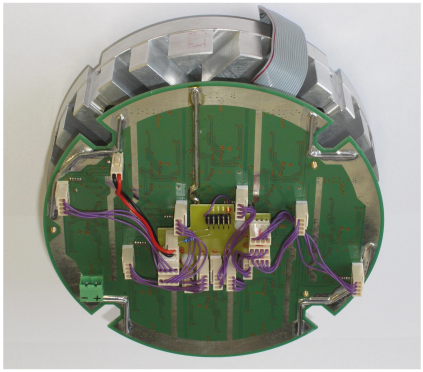
(a) Top view with spotlight on.



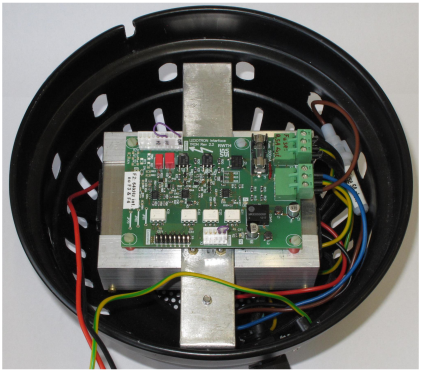
(b) LED board on top of the heatsink.



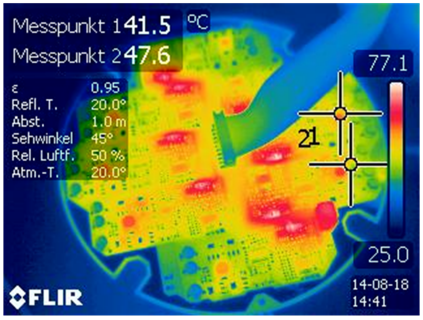
(c) Heatsink, driver board and UCB.



(d) SPI distribution daughterboard.

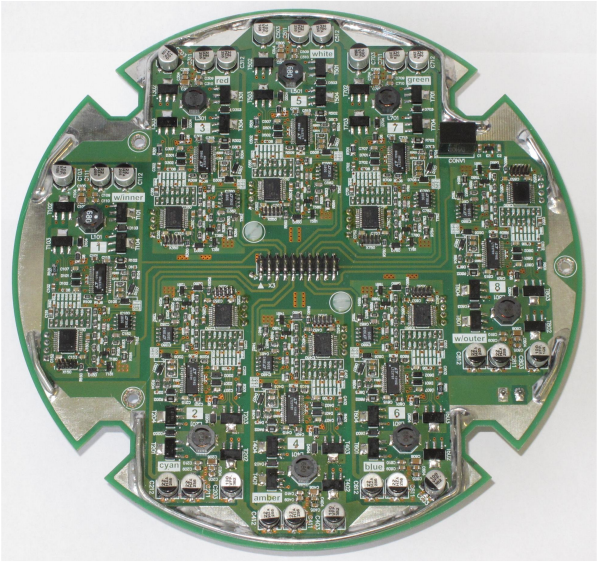


(e) 120 W supply and DLT FW-RX.

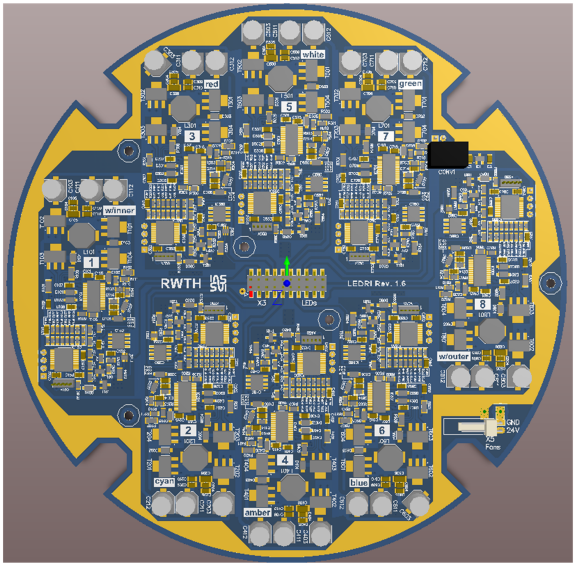


(f) Infrared view of the LED driver board.

Figure C.5: Internal setup and PCB assembly of the spotlight luminaire



(a) Manufactured PCB with eight LED driving stages.



(b) 3D view of LED driver PCB layout.

Figure C.7: LED driver board with eight individual LED channels.

C.2 Table Lamp Demonstrator



Figure C.8: Aluminium case with RF antenna of the table lamp demonstrator.

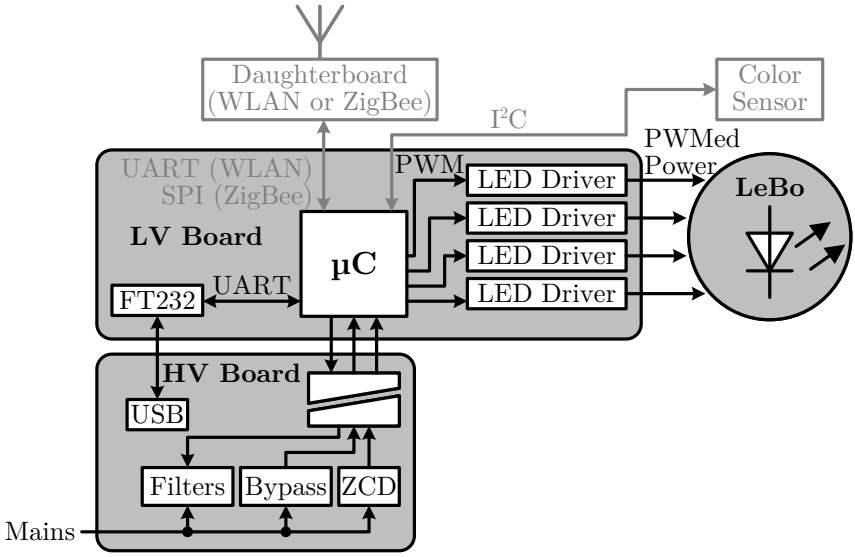


Figure C.9: Board assembly & data distribution of the table lamp demonstrator.

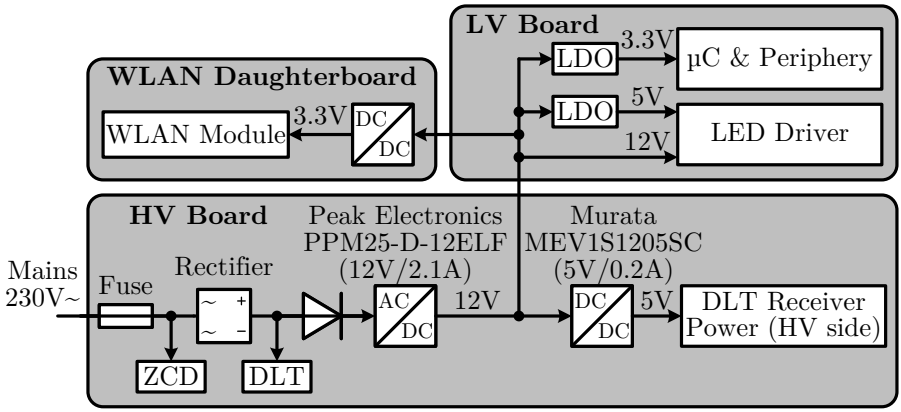
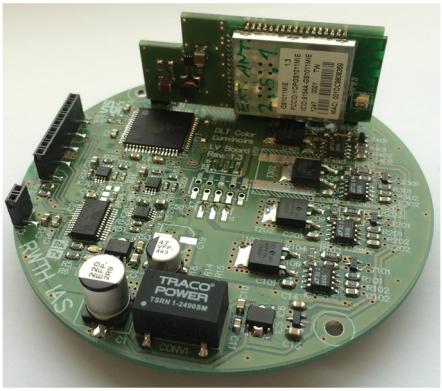
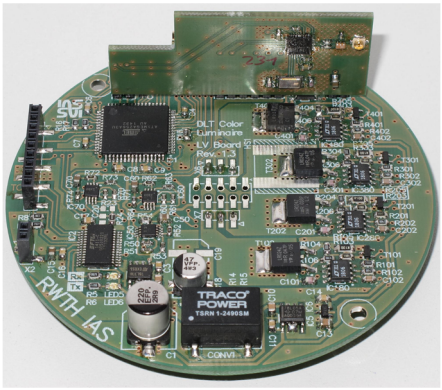


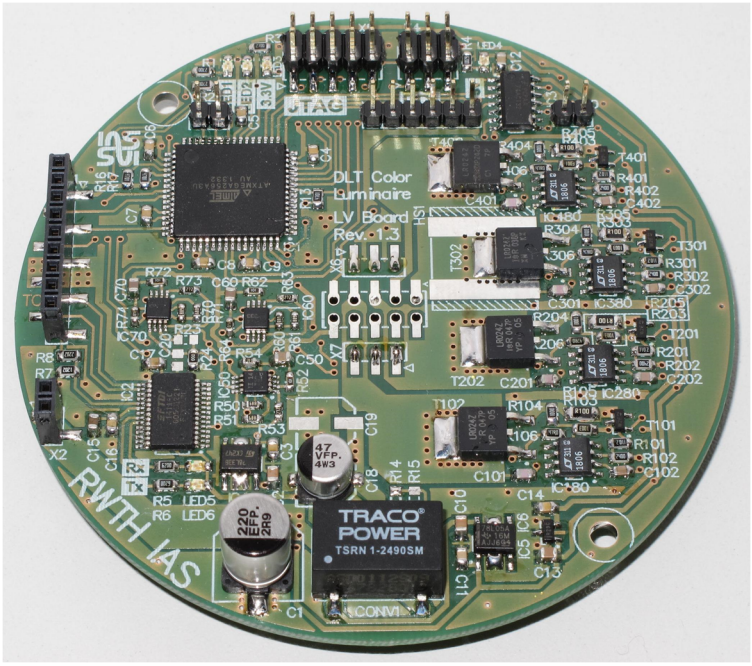
Figure C.10: Power distribution of the table lamp demonstrator.



(a) Main board with WLAN adapter.



(b) Main board with ZigBee adapter.



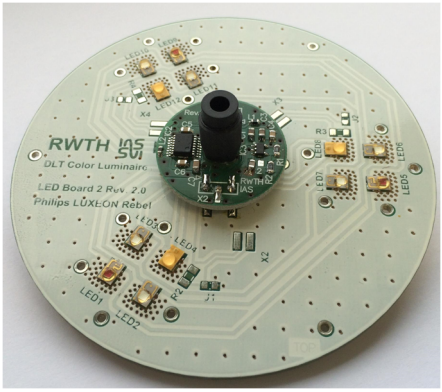
(c) Main control board with four LED driving stages, UART interface & LDO supply.

Figure C.11: LV main control and LED driver board.



(a) Top view of the HV Board. (b) Bottom view of the HV Board.

Figure C.12: HV board with 25 W power supply and DLT circuitry.



(a) 4 single LED colors. (b) 4 color multichip LEDs.

Figure C.13: LED board for table lamp with installed true color sensor.

Curriculum Vitae

Name	Lukas Lohaus
Academic Degree	Diplom-Ingenieur (Dipl.-Ing.)
Date of Birth	March 23rd, 1984
Place of Birth	Gladbeck, Germany

Professional Experience

since 07/2017	Mixed-Signal Design Engineer Infineon Technologies AG, Duisburg, Germany
03/2011–02/2017	Research Assistant and Ph.D. Student Integrated Analog Circuits and RF Systems RWTH Aachen University, Aachen, Germany
05/2009–07/2009	Intern in the R&D Department of Opticon Sensors Europe BV, Hoofddorp, Netherlands
07/2008–04/2009	Student Assistant Institue for Electronic Materials and Nanoelectronics Ruhr-University Bochum, Bochum, Germany
10/2005–06/2007	Student Assistant Institute for Electrical Engineering & Plasma Technology Ruhr-University Bochum, Bochum, Germany

Education

10/2004–11/2010	Studies on Electrical Engineering & Information Sciences Micro- & Nanoelectronics Ruhr-University Bochum, Bochum, Germany
08/2007–05/2008	Studies on Electrical Engineering Graduate School of Electrical Engineering Purdue University, West Lafayette, Indiana, USA
06/2003–04/2004	Civil Service, Social Services in Retirement Home Eduard-Michelis-Haus, Gladbeck, Germany
2001–2003	General Qualification for University Entrance St. Ursula Schule, Hannover, Germany
1994–2001	Städt. Ratsgymnasium Gladbeck Gladbeck, Germany

List of Publications

Peer Reviewed Journal Articles

1. L. Lohaus, A. Rossius, S. Dietrich, R. Wunderlich, and S. Heinen, "A dimmable LED driver with resistive DAC feedback control for adaptive voltage regulation", *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3254–3262, Jul. 2015. DOI: 10.1109/TIA.2014.2387486.

Peer Reviewed Conference Papers

Published as First Author

1. L. Lohaus, C. de Vrieze, A. Rossius, R. Wunderlich, and S. Heinen, "Towards bidirectional power line communication with Digital Load-Side Transmission", in 20th *International Symposium on Power Line Communications and its Applications (ISPLC 2016)*, Mar. 2016, pp. 179–184. DOI: 10.1109/ISPLC.2016.7476283.

2. L. Lohaus, A. Rossius, C. de Vrieze, R. Wunderlich, and S. Heinen, "An advanced control device for intelligent lighting in DLT-systems", in 18th *European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sep. 2016, pp. 1–10. DOI: 10.1109/EPE.2016.7695506.

3. L. Lohaus, A. Rossius, A. Sturm, R. Wunderlich, and S. Heinen, "An efficient dual-stage power supply topology for series connected control devices in intelligent lighting systems", in 7th *IEEE Energie Conversion Congress and Exposition (ECCE 2015)*, Sep. 2015, pp. 2453–2460. DOI: 10.1109/ECCE.2015.7310005.

4. L. Lohaus, A. Rossius, R. Wunderlich, and S. Heinen, "A power supply topology operating at highly discontinuous input voltages for two-wire connected control devices in Digital Load-Side Transmission (DLT) systems for intelligent lighting", in 30th *IEEE Applied Power Electronics Conference and Exposition (APEC 2015)*, Mar. 2015, pp. 1897–1904. DOI: 10.1109/APEC.2015.7104605.

5. L. Lohaus, A. Rossius, R. Wunderlich, and S. Heinen, "A comparison of receiver topologies for Digital Load-Side Transmission in general LED lighting", in 18th *IEEE International Symposium on Power Line Communications and its Applications (ISPLC 2014)*, Mar. 2014, pp. 249–254. DOI: 10.1109/ISPLC.2014.6812336.

6. L. Lohaus, E. Leicht, S. Dietrich, R. Wunderlich, and S. Heinen, "Advanced color control for multicolor LED illumination systems with parametric optimization", in 39th *Annual Conference of the IEEE Industrial Electronics Society (IECON 2013)*, Nov. 2013, pp. 3305–3310. DOI: 10.1109/IECON.2013.6699658.

7. L. Lohaus, A. Rossius, S. Dietrich, R. Wunderlich, and S. Heinen, "A dimmable LED driver using resistive DAC feedback control for adaptive voltage regulation", in 5th *IEEE Energy Conversion Congress and Exposition (ECCE 2013)*, Sep. 2013, pp. 3126–3133. DOI: 10.1109/ECCE.2013.6647109.

8. L. Lohaus, L. Liao, S. Strache, R. Wunderlich, and S. Heinen, "Energy efficient current control technique for driving high power LEDs", in 8th *Conference on Ph.D. Research in Microelectronics and Electronics (PRIME 2012)*, Jun. 2012, pp. 1–4.

9. L. Lohaus, T. Bautze, and K. Dieopold, "Evaluation of optical sensors for laser welding in a technical cognitive environment", 29th *International Congress on Applications of Lasers and Electro-Optics (ICALEO 2010)*, vol. 103, pp. 1541–1546, Sep. 2010.

Published as Co-Author

1. L. Rolff, E. Schulte Bocholt, L. Lohaus, R. Wunderlich, and S. Heinen, "Multiple input, single output, single inductor DC-DC converter architecture providing charge reuse by an efficient high voltage current sink", in 18th *European Conference on Power Electronics and Applications (EPE 2016 ECCE Europe)*, Sep. 2016, pp. 1–9. DOI: 10.1109/EPE.2016.7695489.

2. S. Dietrich, S. Strache, J. Mueller, L. Lohaus, R. Wunderlich, and S. Heinen, "A low power high-side current sense SAR ADC for automotive applications", in 40th *Annual Conference of the IEEE Industrial Electronics Society (IECON 2014)*, Oct. 2014, pp. 2921–2926. DOI: 10.1109/IECON.2014.7048924.

3. S. Dietrich, S. Strache, L. Lohaus, R. Wunderlich, and S. Heinen, "A capacitor-free single-inductor multiple-output LED driver", in 39th *Annual Conference of the IEEE Industrial Electronics Society (IECON 2013)*, Nov. 2013, pp. 6034–6039. DOI: 10.1109/IECON.2013.6700126.

4. L. Liao, L. Lohaus, A. Atac, S. Strache, R. Wunderlich, and S. Heinen, "A low power bandgap voltage reference circuit with PSRR enhancement", in 8th *Conference on Ph.D. Research in Microelectronics Electronics (PRIME 2012)*, Jun. 2012, pp. 1–4.

Presentations

1. L. Lohaus, H. Halfmann, N. Bibinov, and P. Awakowicz, "Bestimmung der Gastemperatur mittels optischer Emissionsspektroskopie zur Sterilisation in einem Niederdruckplasma", in *13. Fachtagung Plasmatechnologie (PT 13)*, Posterpresentation, in German, Mar. 2007.

2. L. Lohaus, H. Halfmann, N. Bibinov, and P. Awakowicz, "Bestimmung der Gastemperatur mittels optischer Emissionsspektroskopie zur Sterilisation in einem Niederdruckplasma", in *13. Tag der biomedizinischen Technik*, Posterpresentation, in German, Dec. 2006.

Monographs

1. L. Lohaus, “Monitoring of laser beam welding with optical coherence tomography (OCT) sensors in comparison to other optical sensors”, Diploma Thesis, Institue for Photonics and Terahertz Technology, Ruhr-Unversity Bochum, Nov. 2010.

2. L. Lohaus, “Simultation on analysis of contact effects in nanowire transistors under the assumption of ideal Schottky barriers”, Study Thesis, Institue for Electronic Materials and Nanoelectronics, Ruhr-University Bochum, 2008.