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Contact Resistance Study of "Edge-Contacted" Metal-Graphene Interfaces

V. Passi [a]*, **A. Gahoi** [a]*, J. Ruhkopf [a], S. Kataria [a], F. Vaurette [b], E. Pallecchi [b], H. Happy [b], M. C. Lemme [a]

[a] University of Siegen, School of Science and Technology, Hölderlinstr.3, 57076 Siegen, Germany

[b] Institut d'Electronique, de Microélectronique et de Nanotechnologie (IEMN,) 59652 Villeneuve d'Ascq, France

Corresponding author: max.lemme@uni-siegen.de

***Abstract*— The contact resistance R_C of "edge-contacted" metal-graphene interfaces is systematically studied. Our experiments demonstrate a reduction of contact resistance by intentional patterning of graphene to create "edge contacts". The parameter space for different hole patterns in graphene is explored. The contact resistance is reduced from 1518 Ωµm for structures without holes to 456 Ωµm in structures with holes of 500 nm diameter everywhere under the contact. These values were achieved at the Dirac point, i.e. at the point of minimum carrier density in graphene and they correspond to a reduction of 70%. These results provide a clear path towards higher performance in graphene based electronic devices, which are often limited by unreliable and high R_C.**

Keywords— contact resistance; edge contact; graphene; TLM

I. Introduction

Graphene has been heralded to lead the nanoelectronics revolution of two-dimensional materials due to its exceptional intrinsic properties [1]. A range of potential applications has been proposed and experimentally demonstrated, such as radio frequency (RF) analog transistors with cut-off frequencies in the hundreds-of-gigahertz range [2] [3] [4], photodetectors [5], [6] [7], nanoelectromechanical systems [8], [9] or terahertz modulators [10]. Large scale graphene synthesis is available today through chemical vapor deposition (CVD) [11]. However, the grown graphene must still be transferred to the desired substrates [12], [13], which introduces defects and contamination and restricts industrial uptake at the moment. Another major road block towards high performance nanoelectronics graphene devices is the high metal - graphene contact resistance (R_C) [14]–[17]. The contact resistivity requirement for state-of-the-art silicon metal oxide field effect transistors (MOSFETs) is 80 Ωµm per contact according to the International Technology Roadmap for Semiconductors (ITRS, [18]). Reported R_C values for metal graphene contacts vary greatly from ITRS compatible values of 69 Ωµm [19] to unacceptable 10^9 Ωµm [14]. This large variation is attributed to fabrication procedures, measurement conditions and graphene carrier density variations. We recently demonstrated that R_C can be tuned by changing the carrier density in graphene from several kΩµm at the Dirac voltage (V_D) down to 90 Ωµm far away from V_D [20].

Current injection at the metal-graphene interface takes place at the edge of the contact, and thus can be classified as a line contact instead of an areal contact. This limits current injection [21] and ultimately the performance of graphene devices. Various studies have been conducted to reduce R_C at the metal - graphene interface, including work function engineering [14], [22], reduction of the contamination at the lithography defined source/drain contact regions prior to metallization [23]–[25], double contact formation [26]–[28], contact area patterning [29], carbide formation [30], graphitic contact formation [31] and edge contact formation [31]–[33]. Theoretical studies further suggest that graphene contacted at its edges with the metal electrode results in reduced R_C [35].

In this work, transmission line method (TLM) structures were fabricated with conventional and lithographically defined "edge" contacts. The edge contacts consist of well-defined holes of various dimensions in graphene in the contact region in an effort to enhance the bonding with the contact metal. Electrical characterization was carried out on TLM devices to evaluate the effectiveness and repeatability of this approach in reducing R_C.

II. Experimental

Boron doped silicon wafers (1-20 Ωµm) were used as starting substrates. The silicon wafers were thermally oxidized to achieve a thickness of 85 nm and further diced into samples of 2 cm x 2 cm. Large area graphene was grown on copper (Cu) foil in a NanoCVD (Moorfield ,UK) rapid thermal processing tool by the CVD method [12]. Graphene growth was performed in a three-step process. Copper foil is annealed at 950°C in argon (80%) and hydrogen (20%) atmosphere, then argon (80%), methane (5%) and hydrogen (15%) gas is passed into the heated chamber at a temperature around 950°C where the methane dissociates leading to graphene growth, and finally the copper foil is cooled to room temperature before removing the sample from the chamber. Graphene films were transferred onto the SiO_2/Si substrates using an electrochemical delamination technique with PMMA as supporting material [12], [36].

After graphene transfer a negative tone electron beam resist (HSQ) was spin coated onto the sample. Rectangular graphene structures were first exposed in HSQ based on electron beam lithography using a RAITH EPBG-5000 plus system at 100 keV. The unexposed resist was developed with a suitable developer and the unprotected graphene was etched by oxygen

*these authors contributed equally to this work

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plasma, thereby resulting in the formation of channels. Finally, contact areas were structured with a bilayer poly-meta-methacrylate (PMMA) resist, and 250 nm of gold was deposited by evaporation. Gold was chosen as the contact material due to the fact that gold contacted to graphene provides low R_C due to the attractive interaction of 4-d orbitals of gold atoms to the π-orbitals of the sp^2 hybridized carbon [22]. Excessive metal was then removed by lift-off in acetone. Silicon-oxide at the wafer back side was removed by a buffered-oxide etch step followed by metal deposition (while the front was protected). This backside metal acted as a back-gate in all the measurements. A 3D schematic of the device and the fabrication steps are shown in Figure 1.

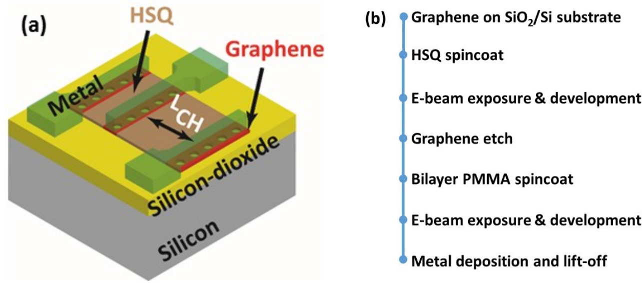

Figure 1: (a) 3D schematic of device showing various layers and holes everywhere under the contact, (b) Process steps of fabrication.

TLM structures without holes (hereafter termed as conventional contacts) and with holes (hereafter termed as edge contacts) of different diameter under the contact region were patterned.
Figure 2 shows the scanning electron micrograph of an entire device. The image shown in the inset was taken before the metal deposition step and illustrates the graphene channel (dark in color). TLM structures with channel width of 12 μm and length of 1 μm, 2 μm, 4 μm, 6 μm, 8 μm were fabricated.

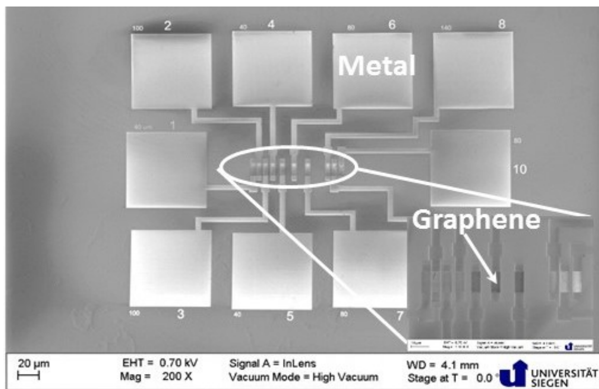

Figure 2: TLM device structure after fabrication. The inset shows the graphene region below the contact. The image shown in the inset was taken before the deposition of the metal.

III. Results & Discussion

The graphene under the contact metal was intentionally etched to create holes with varying diameters of 50 nm, 100 nm, 500 nm and 1000 nm. Two arrays of holes were fabricated, i.e. holes arranged only under the edge of the contact and holes spread all under the contact area as shown in
Figure 3.

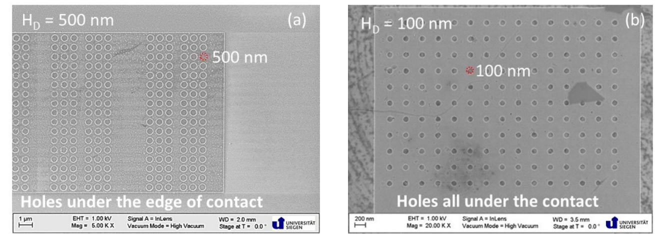

Figure 3: Scanning electron micrograph of patterned graphene (a) holes arranged only under the edge of the contact (b) holes arranged all under the contact area.

Electrical characterization commenced by measuring back-gated FETs with either conventional or edge contacts. All measurements were carried out in ambient air using a Keithley SCS4200 parameter analyzer. **Fehler! Verweisquelle konnte nicht gefunden werden.**a-d show the transfer characteristics (I_{SD}-V_G) of TLM structures with conventional contacts and with edge contacts consisting of devices with holes arranged only under the edge of the contact. The source drain currents (I_{SD}) increase for structures with edge-contacts as compared to conventional contacts. The current level for 1 μm channel length is 0.4 mA, 0.6 mA, 0.48 mA, 0.54 mA for conventional contacts and edge contacts with holes of 50 nm, 100 nm and 500 nm diameter, at -40 V_G back-gate bias, respectively.

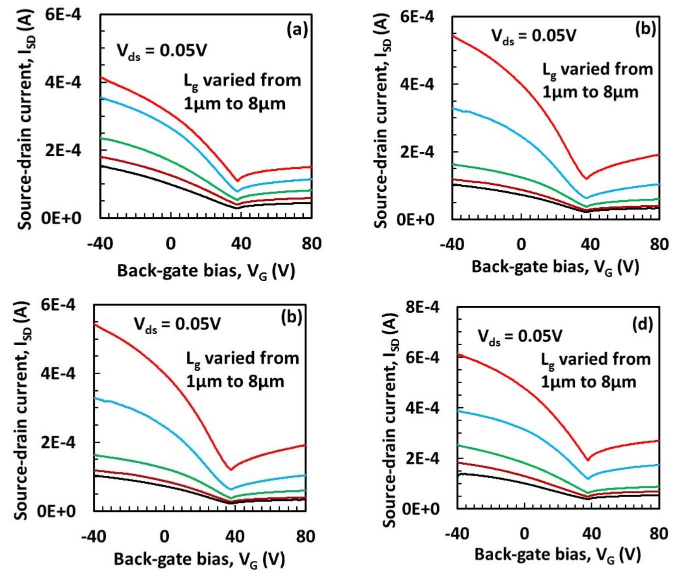

Figure 4: Transfer characteristics I_{SD} –V_G for (a) conventionally contacted graphene and edge contacted graphene with holes arranged only under the edge of the contact with hole dimensions of (b) 500 nm (b) 100 nm (c) 50 nm, respectively.

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Figure 5 summarizes the total device resistances with different contact configurations for varying gate lengths. All these measurements were taken close to the Dirac point (V_D = 38.2 V). The Dirac voltage for all the measured devices varied between 37.6 V to 38.9 V. These data include conventional and edge contacts with holes arranged only under the edge of the contact. Linear fit with high fidelity was applied to extrapolate to the Y-axis, which corresponds to the value of $2R_C$. For graphene patterned with 50 nm holes, an R_C of 620 Ωμm was extracted at the Dirac point, compared to conventional contacts of approximately 1500 Ωμm, a substantial decrease of 59%. This can be attributed to an increased number of carbon sp^2 orbitals available for σ bonding (covalent bonds) [35], which increases carrier injection.

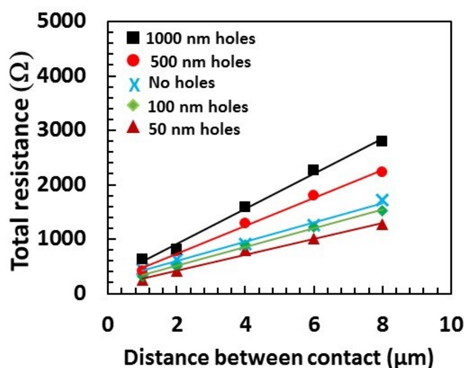

Figure 5: Extrapolation of the contact resistance at the Dirac point (38.2 V) for the surface contact and edge contact with holes arranged only under the edge of the contact.

Figure 6 shows the trend of the extracted R_C values at the Dirac voltage (38.2 V) as a function of the hole diameter in the graphene with holes arranged only under the edge of the contact. Low R_C is obtained as the dimensions of the holes are reduced, which increases effectively the edge perimeter and thus carrier injection. The increase in contact perimeter of the structure with holes of 50 nm is four times that of conventional contacted structure.

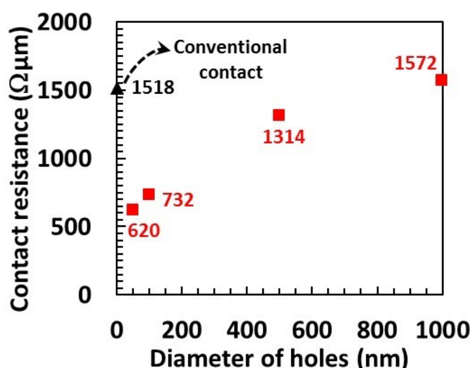

Figure 6: Contact resistance at the Dirac voltage for edge-contacted structure with holes of various dimensions (50 nm, 100 nm, 500 nm and 1000 nm); holes arranged only under the edge of the contact.

When the dimension of holes is increased to 1000 nm, R_C saturates and approaches the value of conventional contacts. In addition, the effective area of graphene under the contact is reduced, compared to edge-contacted graphene with 50 nm hole dimensions. The clear trend observed in Figure 6 suggests that smaller holes of higher density would further reduce R_C. Nevertheless, there would be an optimum hole to graphene ratio that needs to be established in the future to obtain ideal contacts.

We further compared two different TLM structures; holes arranged only under the edge of the contact with holes all under the contact area. Figure 7 shows $I_{SD} - V_G$ characteristics for contacts with 500 nm holes for both cases. The drain current is clearly increased when the graphene is patterned all under the contact area (Figure 7b). This supports the proposed mechanism of enhanced metal-graphene covalent bonding and increase in the perimeter of edge-contacted graphene.

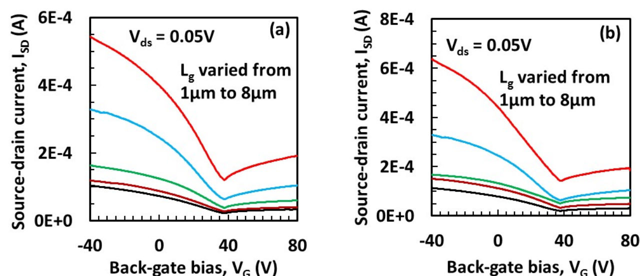

Figure 7: Transfer characteristics I_{SD}–V_{BG} for patterned graphene with hole dimensions of 500 nm (a) holes arranged only under the edge of the contact (b) all under the contact.

Figure 8 compares the TLM plots for both types of contacts with identical hole diameters of 500 nm. Again, the extrapolation of the high fidelity linear fits allowed the extraction of R_C (again at the Dirac point of V_D = 38.2 V). An R_C value of 456 Ωμm was achieved for holes under the entire contact area [red diamond] compared to R_C = 1314 Ωμm [black squares] for holes arranged only under the edge of the contact.

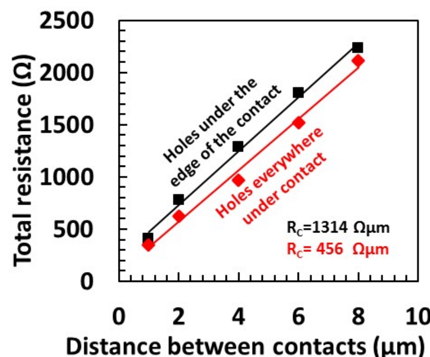

Figure 8: Extrapolation of the R_C at the Dirac point for the edge contacted configuration for patterned graphene only under the edge of the contact (black) and under the entire contact area (red).

Support from the European Commission through an ERC starting grant (InteGraDe, 307311) and an FP7 project (GRADE, 317839) as well as the German Research Foundation (DFG, LE 2440/1-1 and LE 2440/2-1) and the German BMBF (Nanogram, 03XP0006C) is gratefully acknowledged. This work is partly supported by the French RENATECH network. V. Passi would like to acknowledge the clean room staff at IEMN.

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IV. CONCLUSIONS

We investigated systematically the influence of graphene edges on the current injection at the metal-graphene interface. We compared contact resistances of conventional and edge contact configurations with patterned holes in graphene with diameters of 50 nm, 100 nm, 500 nm and 1000 nm. Low R_C of 620 Ωµm at the Dirac point ($V_D = 38.2$ V) is obtained with patterned graphene with holes of 50 nm diameter arranged only under the edge of the contact. Very low R_C of 456 Ωµm is obtained for patterned graphene with holes of 500 nm diameters when the holes are evenly distributed under the entire contact area (taken at the Dirac point as well). This is attributed to the high covalent bonding between the metal and the graphene at the perimeter of the holes [35]. The results demonstrate that an edge contact configuration is superior to conventional contacts. The systematic study further showed a clear dependence on hole diameter, i.e. graphene edge perimeter. The results point out a clear path towards achieving low R_C in a systematic manner, which is urgently required for potential future high performance graphene device applications.

REFERENCES

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, 2004.

[2] M. C. Lemme, L.-J. Li, T. Palacios, and F. Schwierz, "Two-dimensional materials for electronic applications," *MRS Bull.*, vol. 39, no. 08, pp. 711–718, 2014.

[3] J. S. Moon, D. Curtis, M. Hu, D. Wong, C. McGuire, P. M. Campbell, G. Jernigan, J. L. Tedesco, B. VanMil, and R. Myers-Ward, "Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates," *Electron Device Lett. IEEE*, vol. 30, no. 6, pp. 650–652, 2009.

[4] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, "100-GHz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, no. 5966, pp. 662–662, 2010.

[5] M. C. Lemme, F. H. Koppens, A. L. Falk, M. S. Rudner, H. Park, L. S. Levitov, and C. M. Marcus, "Gate-activated photoresponse in a graphene p–n junction," *Nano Lett.*, vol. 11, no. 10, pp. 4134–4137, 2011.

[6] F. Xia, T. Mueller, Y. Lin, A. Valdes-Garcia, and P. Avouris, "Ultrafast graphene photodetector," *Nat. Nanotechnol.*, vol. 4, no. 12, pp. 839–843, 2009.

[7] S. Riazimehr, A. Bablich, D. Schneider, S. Kataria, V. Passi, C. Yim, G. S. Duesberg, and M. C. Lemme, "Spectral sensitivity of graphene/silicon heterojunction photodetectors," *Solid-State Electron.*, vol. 115, pp. 207–212, 2016.

[8] A. D. Smith, F. Niklaus, A. Paussa, S. Vaziri, A. C. Fischer, M. Sterner, F. Forsberg, A. Delin, D. Esseni, P. Palestri, and others, "Electromechanical piezoresistive sensing in suspended graphene membranes," *Nano Lett.*, vol. 13, no. 7, pp. 3237–3242, 2013.

[9] A. D. Smith, K. Elgammal, F. Niklaus, A. Delin, A. C. Fischer, S. Vaziri, F. Forsberg, M. R\a asander, H. akan Hugosson, L. Bergqvist, and others, "Resistive graphene humidity sensors with rapid and direct electrical readout," *Nanoscale*, vol. 7, no. 45, pp. 19099–19109, 2015.

[10] B. Sensale-Rodriguez, R. Yan, M. M. Kelly, T. Fang, K. Tahy, W. S. Hwang, D. Jena, L. Liu, and H. G. Xing, "Broadband graphene terahertz modulators enabled by intraband transitions," *Nat. Commun.*, vol. 3, p. 780, 2012.

[11] S. Bae, S. J. Kim, D. Shin, J.-H. Ahn, and B. H. Hong, "Towards industrial applications of graphene electrodes," *Phys. Scr.*, vol. 2012, no. T146, p. 014024, 2012.

[12] S. Kataria, S. Wagner, J. Ruhkopf, A. Gahoi, H. Pandey, R. Bornemann, S. Vaziri, A. D. Smith, M. Ostling, and M. C. Lemme, "Chemical vapor deposited graphene: From synthesis to applications," *Phys. Status Solidi A*, vol. 211, no. 11, pp. 2439–2449, Nov. 2014.

[13] H. Zhou, W. J. Yu, L. Liu, R. Cheng, Y. Chen, X. Huang, Y. Liu, Y. Wang, Y. Huang, and X. Duan, "Chemical vapour deposition growth of large single crystals of monolayer and bilayer graphene," *Nat. Commun.*, vol. 4, 2013.

[14] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Metal/graphene contact as a performance killer of ultra-high mobility graphene analysis of intrinsic mobility and contact resistance," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1–4.

[15] F. Xia, V. Perebeinos, Y. Lin, Y. Wu, and P. Avouris, "The origins and limits of metal-graphene junction resistance," *Nat. Nanotechnol.*, vol. 6, no. 3, pp. 179–184, 2011.

[16] S. Russo, M. F. Craciun, M. Yamamoto, A. F. Morpurgo, and S. Tarucha, "Contact resistance in graphene-based devices," *Phys. E Low-Dimens. Syst. Nanostructures*, vol. 42, no. 4, pp. 677–679, 2010.

[17] K. Nagashio and A. Toriumi, "Density-of-states limited contact resistance in graphene field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 50, no. 7, p. 0108, 2011.

[18] L. Wilson, "International Technology Roadmap for Semiconductors (ITRS)," *Semicond. Ind. Assoc.*, 2013.

[19] H. Zhong, Z. Zhang, B. Chen, H. Xu, D. Yu, L. Huang, and L. Peng, "Realization of low contact resistance close to theoretical limit in graphene transistors," *Nano Res.*, vol. 8, no. 5, pp. 1669–1679, 2015.

[20] A. Gahoi, S. Wagner, A. Bablich, S. Kataria, V. Passi, and M. C. Lemme, "Contact Resistance Study of Various Metal Electrodes with CVD Graphene," *Solid State Electron.*, 2016.

[21] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Contact resistivity and current flow path at metal/graphene contact," *Appl. Phys. Lett.*, vol. 97, no. 14, pp. 143514–143514, 2010.

[22] V. P. Gahoi, S. Kataria, S. Wagner, A. Bablich, and M. C. Lemme, "Systematic comparison of metal contacts on CVD graphene," in *Solid State Device Research Conference (ESSDERC), 2015 45th European*, 2015, pp. 184–187.

[23] W. Li, C. A. Hacker, G. Cheng, Y. Liang, B. Tian, A. H. Walker, C. A. Richter, D. J. Gundlach, X. Liang, and L. Peng, "Highly reproducible and reliable metal/graphene contact by ultraviolet-ozone treatment," *J. Appl. Phys.*, vol. 115, no. 11, p. 114304, 2014.

[24] J. A. Robinson, M. LaBella, M. Zhu, M. Hollander, R. Kasarda, Z. Hughes, K. Trumbull, R. Cavalero, and D. Snyder, "Contacting graphene," *Appl. Phys. Lett.*, vol. 98, no. 5, p. 053103, 2011.

[25] A. Hsu, H. Wang, K. K. Kim, J. Kong, and T. Palacios, "Impact of graphene interface quality on contact resistance and RF device performance," *Electron Device Lett. IEEE*, vol. 32, no. 8, pp. 1008–1010, 2011.

[26] A. D. Franklin, S.-J. Han, A. A. Bol, and V. Perebeinos, "Double contacts for improved performance of graphene transistors," *Electron Device Lett. IEEE*, vol. 33, no. 1, pp. 17–19, 2012.

[27] L. Adamska, Y. Lin, A. J. Ross, M. Batzill, and I. I. Oleynik, "Atomic and electronic structure of simple metal/graphene and complex metal/graphene/metal interfaces," *Phys. Rev. B*, vol. 85, no. 19, p. 195443, 2012.

[28] C. Gong, D. Hinojos, W. Wang, N. Nijem, B. Shan, R. M. Wallace, K. Cho, and Y. J. Chabal, "Metal–graphene–metal sandwich contacts for enhanced interface bonding and work function control," *ACS Nano*, vol. 6, no. 6, pp. 5381–5387, 2012.

[29] J. T. Smith, A. D. Franklin, D. B. Farmer, and C. D. Dimitrakopoulos, "Reducing Contact Resistance in Graphene Devices through Contact Area Patterning," *ACS Nano*, vol. 7, no. 4, pp. 3661–3667, 2013.

[30] V. K. Nagareddy, I. P. Nikitina, D. K. Gaskill, J. L. Tedesco, R. L. Myers-Ward, C. R. Eddy, J. P. Goss, N. G. Wright, and A. B. Horsfall, "High temperature measurements of metal contacts on epitaxial graphene," *Appl. Phys. Lett.*, vol. 99, no. 7, p. 073506, 2011.

[31] K. Nagashio, R. Ifuku, T. Moriyama, T. Nishimura, and A. Toriumi, "Intrinsic graphene/metal contact," in *2012 International Electron Devices Meeting*, 2012.

[32] D. W. Yue, C. H. Ra, X. C. Liu, D. Y. Lee, and W. J. Yoo, "Edge contacts of graphene formed by using a controlled plasma treatment," *Nanoscale*, vol. 7, no. 2, pp. 825–831, 2015.

[33] E. J. Lee, K. Balasubramanian, R. T. Weitz, M. Burghard, and K. Kern, "Contact and edge effects in graphene devices," *Nat. Nanotechnol.*, vol. 3, no. 8, pp. 486–490, 2008.

[34] L. ANZI, "Very low contact resistance for graphene high frequency devices," 2014.

[35] Y. Matsuda, W.-Q. Deng, and W. A. Goddard III, "Contact Resistance for 'End-Contacted' Metal- Graphene and Metal- Nanotube Interfaces from Quantum Mechanics," *J. Phys. Chem. C*, vol. 114, no. 41, pp. 17845–17850, 2010.

[36] Y. Wang, Y. Zheng, X. Xu, E. Dubuisson, Q. Bao, J. Lu, and K. P. Loh, "Electrochemical delamination of CVD-grown graphene film: toward the recyclable use of copper catalyst," *ACS Nano*, vol. 5, no. 12, pp. 9927–9933, 2011.

V. Passi, A. Gahoi, J. Ruhkopf, S. Kataria, F. Vaurette, E. Pallecchi, H. Happy, and M. C. Lemme, 'Contact resistance Study of "edge-contacted" metal-graphene interfaces', in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, Sep. 2016, pp. 236–239. doi: 10.1109/ESSDERC.2016.7599629.