Reconfigurable Field-Effect Transistors Based on Wet-Chemically Etched Silicon Nanostructures

Von der Fakultät für Elektrotechnik und Informationstechnik
der Rheinisch-Westfälischen Technischen Hochschule Aachen
zur Erlangung des akademischen Grades eines Doktors
der Naturwissenschaften genehmigte Dissertation

vorgelegt von

Bin Sun, M. Sc. RWTH
aus Jiangsu, China

Berichter: Univ.-Prof. Dr. rer. nat. Joachim Knoch
Univ.-Prof. Dr.-Ing. Thomas Mikolajick

Tag der mündlichen Prüfung: 14.07.2022

Publication List

[1] **B. Sun**, B. Richstein, P. Liebisch, T. Frahm, S. Scholz, J. Trommer, T. Mikolajick, J. Knoch*, ''On the Operation Modes of Dual-Gate Reconfigurable Nanowire Transistors,'' in IEEE Transactions on Electron Devices, vol. 68, no. 7, pp. 3684-3689, July 2021, DOI: 10.1109/TED.2021.3081527.

[2] **B. Sun**, T. Grap, T. Frahm, S. Scholz, J. Knoch*, ''Role of electron and ion irradiation in a reliable lift-off process with electron beam evaporation and a bilayer PMMA resist system,'' in Journal of Vacuum Science & Technology B, vol. 39, no. 5, pp. 052601, Sep. 2021, DOI: 10.1116/6.0001161.

[3] **B. Sun**†, S. Scholz†, A. Kemper, T. Grap, J. Knoch*, ''Modeling and prediction of hydrogen-assisted morphological evolution in silicon utilizing a level-set approach,'' in IEEE Journal of Microelectromechanical Systems, vol. 30, no. 6, pp. 950-957, Oct. 2021, DOI: 10.1109/JMEMS.2021.3115715. († equal contribution)

[4] J. Klos†, **B. Sun**†, J. Beyer, S. Kindel, L. Hellmich, J. Knoch, L. Schreiber*. ''Spin qubits confined to a silicon nano-ridge,'' in Applied Sciences vol. 9, no. 18, pp. 3823, 2019, DOI: 10.3390/app9183823. († equal contribution)

[5] F. Riederer, T. Grap, S. Fischer, M. Müller, D. Yamaoka, **B. Sun**, C. Gupta, K. Klaus, J. Knoch*, ''Alternatives for Doping in Nanoscale Field-Effect Transistors,'' in physica status solidi (a), vol. 215, no. 7, p. 1700969, Jan. 2018, DOI: 10.1002/pssa.201700969.

[6] J. Knoch*, **B. Sun**, ''Sub-Linear Current Voltage Characteristics of Schottky-Barrier Field-Effect Transistors,'' in IEEE Transactions on Electron Devices, vol. 69, no. 5, pp. 2243-2247, May 2022, DOI: 10.1109/TED.2022.3161245.

Abstract

In recent years, device scaling close to the physical limit has spurred the move from geometrical to equivalent scaling of conventional MOSFETs utilizing new device architectures, materials and integration schemes to continue delivering integrated circuits with higher density and improved performance (power, speed). However, conventional doping at the nanoscale often leads to issues such as dopant deactivation as well as device-to-device variability due to random dopant effects. Reconfigurable field-effect transistors are a variant of Schottky-barrier MOSFETs with metallic source and drain contacts that have been attracting a great deal of interest since replacing the doped source/drain regions with metals allows avoiding dopant-related issues. Furthermore, transistor devices based on novel 2D materials or carbon nanotubes are usually fabricated in a straightforward way by depositing metals on top of the material. However, in most cases Fermi level pinning at the metal-semiconductor interface occurs within the band gap giving rise to substantial Schottky-barriers (SB) at the contact channel interfaces that strongly impact the electrical characteristics of such SB-MOSFETs, leading to a deteriorated on-state performance and a degraded switching behavior. In addition, one of the most predominant features of SB-MOSFETs is a distinct sub-linear behavior in the triode operation regime of the $I_\mathrm{d} - V_\mathrm{ds}$ characteristics for small bias which is highly undesirable with respect to applying such devices in logic circuits.

In this work, reconfigurable field-effect transistors with two gates that can be utilized to tune the effective Schottky barrier height at the source and drain sides individually are fabricated and investigated. First, a top-down technique using a two-step wet-chemical etching of silicon for the fabrication of nanowires with triangular cross-section on a silicon-on-insulator substrate is presented. Such a self-limiting fabrication approach yields localized silicon nanowires with atomically flat surfaces and minimal plasma damage manufacturable with conventional h-line contact lithography. Next, a simulation tool based on the level set method that allows modeling and prediction of the shape transformation of silicon structures during hydrogen annealing with high accuracy is introduced. Additionally, a modified electron beam evaporation setup is demonstrated for the first time to obtain a reliable and reproducible lift-off process. The modified electron beam evaporation chamber with two permanent magnets and a hollow metallic cylinder installed turns out to be very effective in avoiding the irradiation of electrons and ions on PMMA, yielding near perfect deposition results for a large variety of different materials. After the fabrication of the device, the rather overlooked device operation mode with the program gate at source (PGAS) is investigated and compared with the program gate at drain (PGAD). As it turns out, the PGAS mode yields an almost ideal switching behavior similar to a conventional MOSFET while its output characteristics are deteriorated when compared to PGAD which exhibits improved output but deteriorated transfer characteristics. Furthermore, PGAD and PGAS show a distinctly different non-linearity in the output characteristics with a stronger effect in the PGAS mode. Simulation results reveal that the non-linearity in PGAS is due to a forward-biased Schottky barrier at drain whereas it is due to a charge-mediated impact of drain bias on the channel potential in PGAD. We thereby present with simulation to show that a linear $I_\mathrm{d} - V_\mathrm{ds}$ behavior can be achieved in PGAD by approaching the so-called quantum capacitance limit.

Contents

Acronyms

AFM	Atomic Force Microscopy
CGAD	Control Gate at Drain
CGAS	Control Gate at Source
CMOS	Complementary Metal-Oxide-Semiconductor
DIBL	Drain Induced Barrier Lowering
DMSO	Dimethyl Sulfoxide
DNQ	Diazonaphthoquinone
EBL	Electron Beam Lithography
EDP	Ethylenediamine Pyrocatechol
EHT	Electron High Tension
EUV	Extreme Ultraviolet
FinFET	Fin Field-Effect Transistor
GAA FET	Gate-All-Around Field-Effect Transistor
HF	Hydrofluoric Acid
IC	Integrated Circuit
IPA	Isopropyl Alcohol
LDD	Lightly-Doped Drain
MBE	Molecular Beam Epitaxy
MEMS	Micro-Electromechanical Systems
MIBK	Methyl Isobutyl Ketone
MIGS	Metal-Induced Gap States
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NEGF	Non-Equilibrium Green's Function
PGAD	Program Gate at Drain
PGAS	Program Gate at Source
PMMA	Polymethylmethacrylat
RCA	Radio Corporation of America
RF	Radio Frequency
RFET	Reconfigurable Field-Effect Transistor
RMS	Root Mean Square
SC	Standard Clean
SB	Schottky Barrier

SB-MOSFET	Schottky-Barrier Metal-Oxide-Semiconductor Field-Effect Transistor
SCE	Short Channel Effects
SEM	Scanning Electron Micrograph
SiNW	Silicon Nanowire
SM	Step Monohydride
SOI	Silicon On Insulator
WKB	Wentzel-Kramers-Brillouin
TMAH	Tetramethylammonium Hydroxide
TVD	Total Variation Diminishing
2DEG	2-Dimensional Electron Gas

List of Symbols

$C_{\text{inv}}^{\square}$	$[\text{F}/\text{cm}^2]$	inversion-layer capacitance
$C_{\text{it}}^{\square}$	$[\text{F}/\text{cm}^2]$	interface-states capacitance
$C_{\text{ox}}^{\square}$	$[\text{F}/\text{cm}^2]$	oxide capacitance per unit area
$C_{\text{q}}^{\square}$	$[\text{F}/\text{cm}^2]$	quantum capacitance
$C_{\text{s,d}}^{\square}$	$[\text{F}/\text{cm}^2]$	source and drain parasitic capacitance
$C_{\Sigma}^{\square}$	$[\text{F}/\text{cm}^2]$	total capacitance
χ	[eV]	electron affinity
χ_{SiO_2}	[eV]	electron affinity of $\text{SiO}_2 = 0.95\,\text{eV}$
d_{ch}	[1/m]	depth of the triangular potential well
$\Delta\,\Phi_{\text{ox}}$	[V]	potential drop at the oxide layer
$D(E)$	$[1/(\text{m}^2 \cdot \text{J})]$	density of states
D_{it}	$[1/(\text{m}^2 \cdot \text{J})]$	interface trap density
d_{nw}	[m]	diameter of a nanowire
d_{ox}	[m]	oxide thickness
d_{tunnel}	[m]	tunneling distance
e	[C]	the elementary charge $(= 1.602176634 \times 10^{-19}\,\text{C})$
E_{C}	[eV]	conduction band edge
E_{F}^{m}	[eV]	Fermi energy of metal
E_{F}^{i}	[eV]	intrinsic Fermi energy of silicon
E_{F}^{Si}	[eV]	Fermi energy of silicon
E_{g}	[eV]	energy gap of silicon
$\mathscr{E}_{\text{ox}}$	[V/m]	electric field strength in oxide
E_{V}	[eV]	valance band edge
E_{vac}	[eV]	vacuum energy level
$\mathscr{E}(x)$	[V/m]	electric field strength in $x-$direction
ε_0	[F/m]	vacuum permittivity
ε_{i}	[none]	relative permittivity of the interfacial layer
ε_{ox}	[none]	relative permittivity of oxide
ε_{nw}	[none]	relative permittivity of nanowire
$f_{\text{D}}(E)$	[none]	Fermi distribution function at drain
$f_{\text{S}}(E)$	[none]	Fermi distribution function at source
γ	$[\text{J}/\text{m}^2]$	surface free energy per uni area

g_{m}	[A/V]	transconductance
h	[J·s]	Planck's constant ($h = 6.626 \times 10^{-34}$)
$j(x)$	[A/m^2]	current density in $x-$direction
κ	[m^{-1}]	mean curvature of an implicit function
k_{B}	[eV/K]	the Boltzmann constant ($= 8.617343 \times 10^{-5}$ eV/K)
L	[m]	channel length of a MOSFET
λ	[m]	screening length
$m^\star$	[kg]	effective mass
$m^\star_{\mathrm{c,v}}$	[kg]	effective mass of charge carriers in conduction or valance band
m_e	[kg]	mass of electron
m^*_{e}	[kg]	effective mass of electron
μ_{n}	[m^2/(V·s)]	charge carrier mobility
N_{A}	[m^{-3}]	acceptor impurity density
N_{D}	[m^{-3}]	donor impurity density
N_{C}	[m^{-3}]	effective density of states of conduction band
$\mathbf{n}_{\mathrm{i}}$	[none]	surface outward normal vector of the i$^{\mathrm{th}}$ element
n_{i}	[m^{-3}]	intrinsic carrier density
n_{S}	[m^{-2}]	surface density of atoms
$n(x,z)$	[m^{-3}]	charge carrier density in $x-$ and $z-$direction
Ω	[m^3]	atomic volume
$\partial\Omega$	[none]	interface (propagation front)
p_0	[Pa]	equilibrium vapor pressure of a flat surface
$Q^{\square}$	[C/cm^2]	charge per unit area
Q	[eV]	activation energy
$\mathbf{r}_{\mathrm{i}}(t)$	[none]	vector of the i$^{\mathrm{th}}$ element
$R(T)$	[m/s]	etch rate dependence on temperature
S	[mV/dec]	inverse subthreshold slope
T	[K]	temperature
V_{ds}	[V]	drain-source voltage
V_{gs}	[V]	gate-source voltage
V_{n}	[m/s]	propagation speed along the surface outward normal
V_{th}	[V]	threshold voltage
$v(x)$	[m/s]	carrier velocity in $x-$direction
W	[m]	channel width of a MOSFET
Ψ_{m}	[eV]	work function of metal
Ψ_{Si}	[eV]	work function of silicon
Ψ_{NL}	[eV]	charge neutral level
Φ_{bi}	[V]	built-in potential
Φ_{fb}	[V]	flat-band voltage
Φ_{B}	[V]	difference between Fermi potential and intrinsic potential
Φ_{S}	[V]	surface potential at the silicon-oxide interface
$\Phi^{\mathrm{d}}_{\mathrm{SB}}$	[V]	Schottky barrier height at the drain-channel side
$\Phi^{\mathrm{n}}_{\mathrm{SB}}$	[V]	Schottky barrier height for electrons

$\Phi_{\mathrm{SB}}^{\mathrm{p}}$	[V]	Schottky barrier height for holes
$\Phi_{\mathrm{SB}}^{\mathrm{s}}$	[V]	Schottky barrier height at the source-channel side
$\Phi_f(x)$	[V]	potential at the oxide silicon interface
$\phi(\mathbf{r}, t)$	[none]	level set function

Chapter 1

Introduction

Being the second most abundant element in the earth's crust, silicon is the most widely used semiconductor material for the fabrication of integrated circuits (ICs). It features an appropriate band gap, a similar electron and hole mobility, and a flexible tuning of resistivity by a variety of dopants, etc. Among others, Si stands out most importantly due to the feasible acquisition of high-quality SiO_2/Si interface (i.e., low inteface states and an appropriate band offset) [1]. As a result, the physical realization of a metal-oxide-semiconductor field-effect transistor (MOSFET) was successfully demonstrated in 1960 [2]. Since then, the world has witnessed an unprecedented growth of the device and it soon became the most widely used semiconductor device especially after the employment of complementary metal-oxide-semiconductor (CMOS) technology [3] mainly due to its small size, low power, and low cost [4]. In 1965, the famous Moore's Law was proposed to describe such an exponential growth in computing power, which is reflected in the doubling of transistor density on a single chip approximately every 18-24 months [5]. Over the past decades, the IC industry has been continuously delivering chips with higher packing density and improved performance (power, speed) through the employment of new materials, device architectures, and integration schemes [6]. At the current 5 nm technology node, transistors have a physical gate length of less than 20 nm [7] and their principles of operation still remain the same as before. Further downscaling would push toward quantum mechanical limits and ultimately justify scattering-free carrier transport.

Apart from the employment of a completely different transport theory, there are also technological difficulties that limit the further downscaling of conventional MOSFETs. As device structures are being continuously minaturized into the deep nanoscale using state-of-the-art EUV lithography, traditional ion implantation techniques gradually become less suitable. The highly energetic implantation species could easily amorphize the entire fin (< 10 nm in width) and lead to increased parasitic resistances if there is no seed layer available to recover the crystal damage during an activation anneal [8, 9]. In addition, the finite solid solubility of dopants and their increased ionization energy [10, 11, 12] in nanoscale dimensions also lead to increased parasitic resistances and capacitances in the source and drain regions. Furthermore, the stochastic nature of ion implantation and dopant

diffusion during an activation anneal make it hard to implement well-defined potential profiles with sharp interface transitions within a small volume of semiconductor material. This leads to a variability in threshold voltage from device to device due to random dopant distribution effects [13, 14, 15]. Moreover, the potential landscape created by physical doping stays fixed after an implantation and dopant activation process, which only allows either n- or p-type unipolar operation of the fabricated device.

The aforementioned issues are best addressed if doping in source/drain and channel can be avoided altogether. Recently, electrostatic doping [16, 17, 18, 19] has been proposed to create virtual n- or p-type regions in an undoped semiconductor material with an external gate bias applied on a metal-oxide-semiconductor (MOS) capacitor. In particular, volume inversion or accumulation could be achieved if the thickness of semiconductor material is sufficiently small, leading to a uniform vertical distribution of charge carriers within the sheet of semiconductor material[18]. The concept of electrostatic doping opens up a door for emerging devices based on novel materials such as carbon nanotubes [20], graphene [21], and WSe_2 [22], etc. for which a conventional physical doping is fundamentally difficult. In addition, novel device architectures employing one or two additional gates – the so-called reconfigurable field-effect transistors (RFETs) [23, 24] – based on electrostatic doping have attracted an increasing attention due to a number of advantages:

- the employment of electrostatic doping avoids dopant related issues;
- a reconfigurable FET can be operated as either n- or p-type device, which is exploited from the ambipolar operation of a Schottky-barrier MOSFET;
- the reconfigurability allows changing the functionality of a circuit block dynamically at runtime [24];
- the reconfigurability further allows a reduction of circuit topologies despite the more complex device architecture [25];
- the reconfigurability could also strengthen the hardware security of circuits.

In this work, the fabrication and characterization of a dual-gate reconfigurable silicon nanowire transistor based on wet chemically etched silicon nanowires (SiNWs) and Ni silicidation are presented. First, two fundamental building blocks of a reconfigurable transistor, namely, the MOS system and metal-semiconductor contacts are revisited. Next, the working principles of conventional MOSFETs as well as Schottky-barrier MOSFETs are presented. Chapter 3 deals with key fabrication techniques including a comparison of etching behavior in TMAH and KOH based solutions. The hydrogen annealing process which could be used for improving surface roughness and shape transformation is also presented. In particular, a practical process simulation tool based on the level set method is designed to predict the topological evolution without the need for carrying out laborious experiments. In addition, a modified electron-beam evaporation setup is presented to obtain a reliable lift-off process. After that, fabrication and characterization of the dual-gate

reconfigurable nanowire FET including process development and comparison of two device operation modes are presented. Another key feature of the fabrication approach is the generation of localized SiNWs with atomically flat surfaces and minimal plasma damage manufacturable with conventional h-line contact lithography. Strengths and drawbacks of two device operation modes, namely, program gate at source (PGAS) and at drain (PGAD), for both n- and p-type configurations are presented and analyzed. Finally, strategies for performance improvement towards a linear $I_\mathrm{d} - V_\mathrm{ds}$ behavior of the device is presented.

Chapter 2

Device Fundamentals

This chapter first revisits the metal-oxide-semiconductor (MOS) system and the formation of a Schottky barrier, which are two fundamental building blocks of a reconfigurable field-effect transistor (RFET). Next, the MOS and Schottky barrier are combined to form a gated Schottky junction. Subsequently, the principles of operation for both a conventional MOSFET and a Schottky-barrier (SB) MOSFET will be introduced and compared. Finally, the reason how a nanowire geometry helps improving the device performance will be explained.

2.1 The MOS System

The MOS system is a fundamental building block of a MOSFET. It is a stack of three different materials covering a distinct range of electrical conductivity. The so-called ''field-effect'' is the ability to induce a 2-dimensional electron gas (2DEG) close to the oxide-semiconductor interface by applying an external voltage at the metal electrode. In this thesis, the MOS structure is both used for electrostatic doping and the creation of a conductive channel between the source and drain regions.

Figure 2.1 shows the band diagram of an ideal metal-SiO_2-silicon system in separate form where interface states (e.g., dangling bonds), mobile sodium/potassium ions, and fixed charge states are neglected. The MOS structure can be treated as a series connection of two capacitors formed by the oxide and the semiconductor where the latter could be tuned by the relative separation between energy bands of the semiconductor and the Fermi level of the adjacent electrode through the thin oxide layer. The work function of a metal Ψ_{m} (e.g. Al) is smaller than that of p-type silicon Ψ_{Si} as illustrated in Fig. 2.1. Silicon dioxide, the material of choice as a gate oxide, features a high-quality SiO_2/Si interface, a high crystallization temperature ($\sim$1200 °C), and a large band gap ($\sim$9 eV). Furthermore, an appropriate alignment of the energy bands with respect to that of silicon blocks the flow of both electrons and holes.

Since the work function of metal Ψ_{m} is smaller than that of p-type silicon Ψ_{Si}, the bands close to the silicon surface bend downwards after equilibrium is established (i.e., the Fermi level lines up). As a result, a depletion region is formed near the silicon surface. The charge of the immobile acceptor ions across the depletion layer $|Q^{\square}_{\mathrm{depl}}|$ is equal to that of positive charges induced at the metal surface $Q^{\square}_{\mathrm{metal}}$ (the square sign denotes charge per unit area):

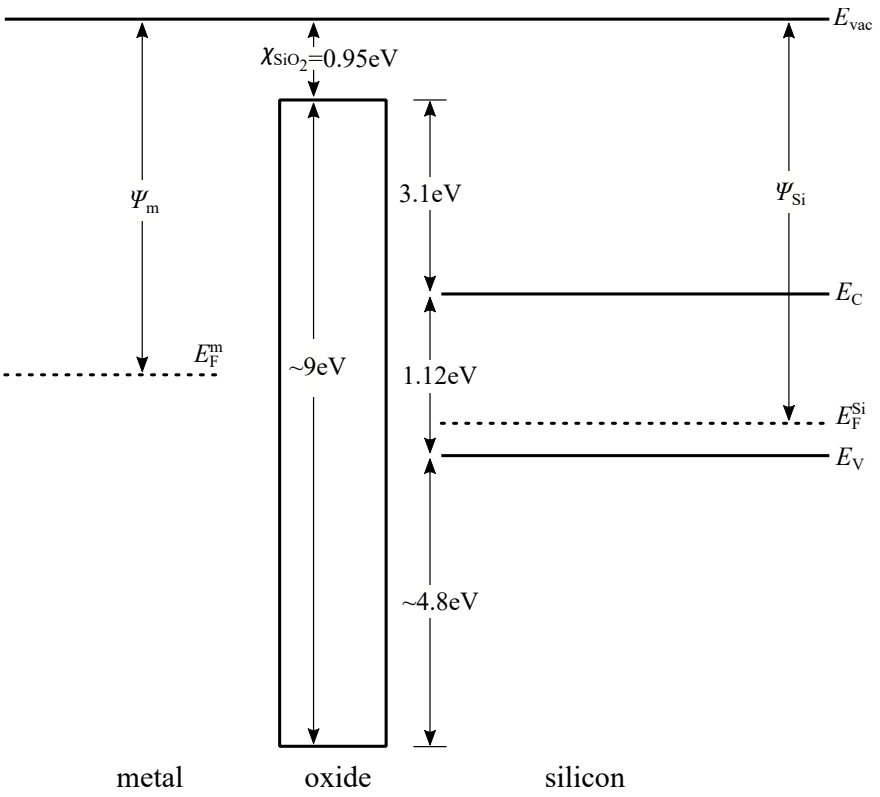


Figure 2.1: Band diagram of an ideal metal-SiO_2-silicon system in separate form. The work function of metal Ψ_{m} (e.g. Al) is smaller than that of a p-type silicon Ψ_{Si}. The alignment of the large band gap in SiO_2 ($\sim$9 eV) with respect to that in silicon ($\sim$1.12 eV) and the Fermi level of metal forms a large energy barrier between metal and silicon for both electrons and holes.

$$Q^{\square}_{\mathrm{metal}} = -Q^{\square}_{\mathrm{depl}}. \tag{2.1}$$

A flat band condition is obtained when the surface potential at the silicon surface becomes zero ($\Phi_{\mathrm{S}} = 0$):

$$-eV_{\mathrm{fb}} = \Psi_{\mathrm{fb}} = \Psi_{\mathrm{Si}} - \Psi_{\mathrm{m}}. \tag{2.2}$$

The energy bands bend downwards since $\Psi_{\mathrm{m}} < \Psi_{\mathrm{Si}}$ as depicted in Fig. 2.2. Weak inversion is obtained once the intrinsic Fermi level $E_{\mathrm{F}}^{\mathrm{i}}$ at the silicon surface meets the Fermi level $E_{\mathrm{F}}^{\mathrm{Si}}$ if a sufficiently large positive voltage is applied at the gate electrode, namely, $\Phi_{\mathrm{S}} = \Phi_{\mathrm{B}}$. Increasing the gate voltage further leads to additional band bending and strong inversion is

obtained when the surface electron density is equal to the bulk doping concentration [26] ($A = E_g/2 - e\Phi_B = E_g/2 - B$, hence $B = e\Phi_B$ and $\Phi_S = 2\Phi_B$) as depicted in Fig. 2.3. At this point, the threshold condition is obtained and the voltage applied at the gate electrode is calculated as

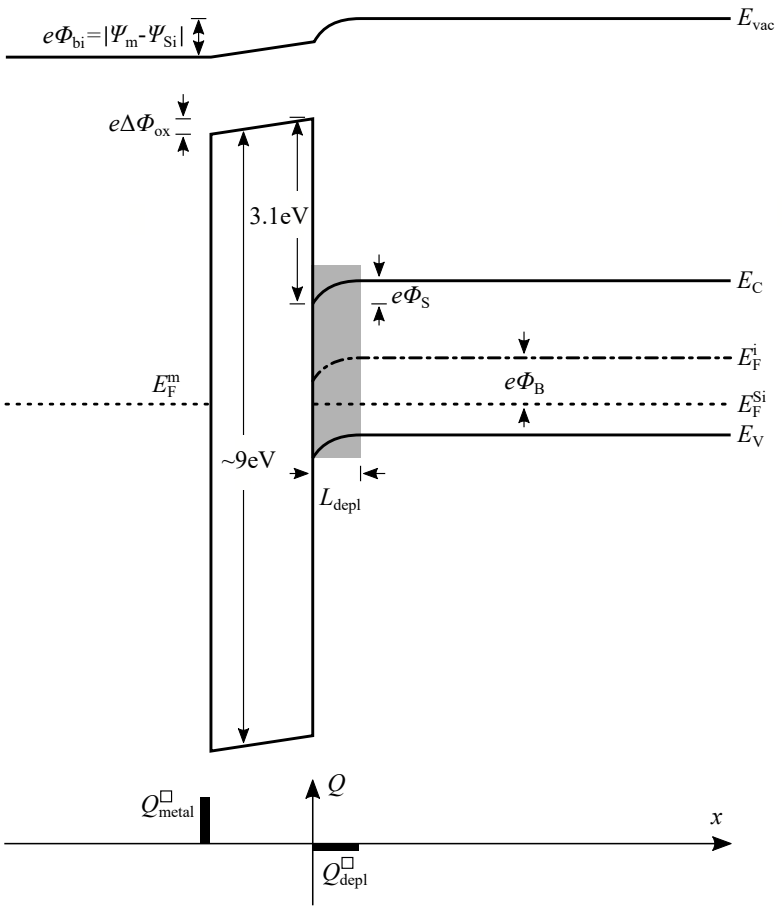


Figure 2.2: Band diagram of an ideal metal-SiO_2-silicon system in contact form. The conduction band edge E_C, valance band edge E_V, vacuum level E_{vac} and intrinsic Fermi level E_F^i of silicon bend downwards since $\Psi_m < \Psi_{Si}$. The Fermi level E_F^{Si} stays invariant of position as it is unaffected by the gate bias as a result of zero current flow ($I_g = 0$). A bias voltage $V_{fb} = (\Psi_m - \Psi_{Si})/e$ applied at the gate electrode is required to obtain a flat band condition.

$$V_g = \Phi_{fb} + \Phi_S + \Delta\Phi_{ox} = \Phi_{fb} + 2\Phi_B + \mathscr{E}_{ox} d_{ox}. \tag{2.3}$$

According to Poisson's equation ($\Delta\Phi = -\rho/(\varepsilon_0\varepsilon_{ox})$ where $\rho = 0$ in the ideal case), the electric field $\mathscr{E}_{ox}$ in the oxide layer is constant. Hence, $\mathscr{E}_{ox} d_{ox} = \varepsilon_0\varepsilon_{ox}\mathscr{E}_{ox} d_{ox}/\varepsilon_0\varepsilon_{ox} = Q^{\square}_{tot}/C^{\square}_{ox}$, where $Q^{\square}_{tot}$ is the total amount of charge per unit area stored in semiconductor and $C^{\square}_{ox}$ is the oxide sheet capacitance. $\varepsilon_{0,ox}$ are the vacuum and the relative permittivity

of oxide, respectively. Eqn. (2.3) can be rewritten as

$$V_{\mathrm{g}} = \Phi_{\mathrm{fb}} + 2\Phi_{\mathrm{B}} + \frac{Q^{\square}_{\mathrm{depl}} + Q^{\square}_{\mathrm{inv}}}{C^{\square}_{\mathrm{ox}}}. \tag{2.4}$$

For $\Phi_{\mathrm{S}} < 2\Phi_{\mathrm{B}}$, $Q^{\square}_{\mathrm{inv}} << Q^{\square}_{\mathrm{depl}}$, and hence the threshold voltage can be approximated as

$$V_{\mathrm{g}} \approx \Phi_{\mathrm{fb}} + 2\Phi_{\mathrm{B}} + \frac{Q^{\square}_{\mathrm{depl}}}{C^{\square}_{\mathrm{ox}}}. \tag{2.5}$$

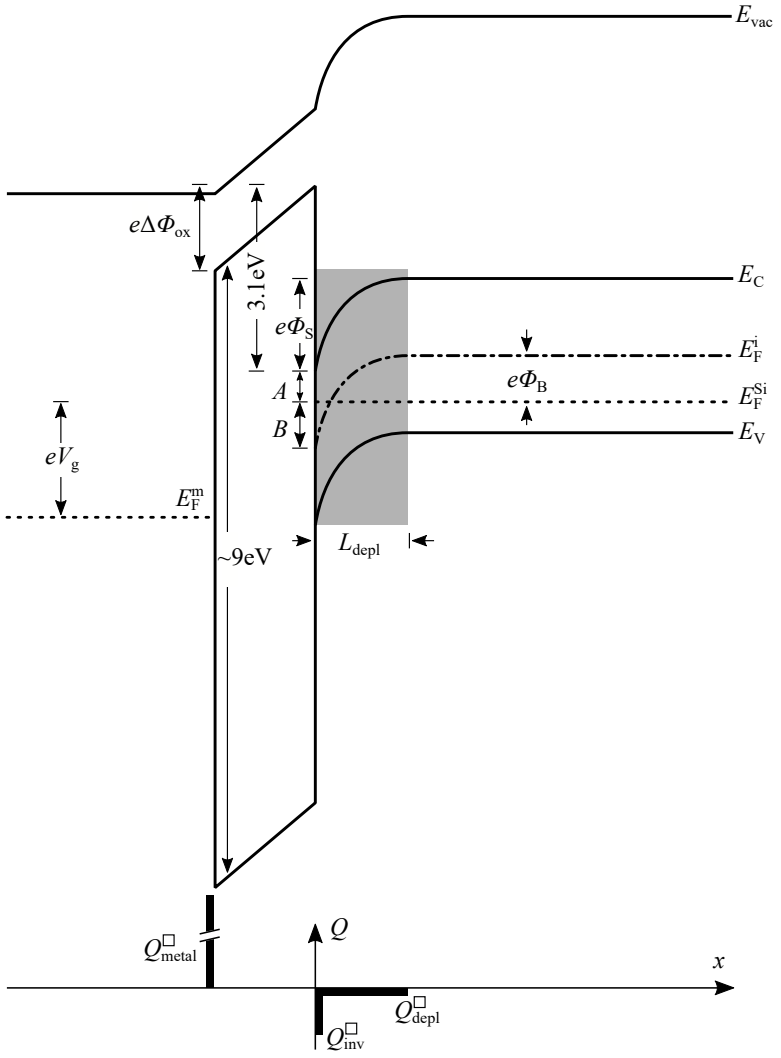


Figure 2.3: Band diagram of an ideal metal-SiO_2-silicon system in contact form with a voltage V_{g} applied to the gate electrode yielding a strong-inversion of the silicon channel.

Although $Q^{\square}_{\mathrm{inv}}$ can be neglected for calculating the threshold voltage, the band bending at the silicon-oxide interface allows a small amount of charge carriers to flow from source to

drain and hence is closely related to the transistor leakage current in the OFF-state [27]. The depletion depth L_{depl} can be derived with the Poisson's equation:

$$\Delta\,\Phi = \frac{d\mathscr{E}_{\mathrm{Si}}}{dx} = -\frac{\rho_{\mathrm{Si}}}{\varepsilon_0\varepsilon_{\mathrm{Si}}} = -\frac{-eN_{\mathrm{A}}}{\varepsilon_0\varepsilon_{\mathrm{Si}}}, \qquad \text{for } 0 \leq x \leq L_{\mathrm{depl}}. \tag{2.6}$$

Suppose the bulk Si substrate is grounded, the solution of Eqn. (2.6) should fulfill following boundary conditions: $\mathscr{E}_{\mathrm{Si}}\,(x = L_{\mathrm{depl}}) = 0$, and $\Phi\,(x = L_{\mathrm{depl}}) = 0$. Thus, the potential is then derived as

$$\Phi(x) = \frac{eN_{\mathrm{A}}}{2\varepsilon_0\varepsilon_{\mathrm{Si}}}\,(x - L_{\mathrm{depl}})^2\,. \tag{2.7}$$

With the surface potential at $\Phi(x = 0) = \Phi_{\mathrm{S}} = 2\,\Phi_{\mathrm{B}}$, the depletion length L_{depl} is calculated as

$$L_{\mathrm{depl}} = \sqrt{\frac{2\varepsilon_0\varepsilon_{\mathrm{Si}}\,\Phi_{\mathrm{S}}}{eN_{\mathrm{A}}}} = \sqrt{\frac{4\varepsilon_0\varepsilon_{\mathrm{Si}}\,\Phi_{\mathrm{B}}}{eN_{\mathrm{A}}}}. \tag{2.8}$$

Therefore, L_{depl} can be calculated by combining Eqn. (2.8) and $p = N_{\mathrm{A}} = n_{\mathrm{i}}\mathrm{exp}\left(\dfrac{E_{\mathrm{F}}^{\mathrm{i}} - E_{\mathrm{F}}^{\mathrm{Si}}}{k_{\mathrm{B}}T}\right)$ at room temperature where n_{i} is the intrinsic carrier density and $\Phi_{\mathrm{B}} = E_{\mathrm{F}}^{\mathrm{i}} - E_{\mathrm{F}}^{\mathrm{Si}}$.

For gate bias larger than the threshold voltage, the inversion charge layer shields the electric field in the semiconductor. Hence, the surface potential Φ_{S}, the depletion charge $Q_{\mathrm{depl}}^{\square}$, and the depletion layer width L_{depl} do not change too much further. In this case, Eqn. (2.4) can be written as

$$V_{\mathrm{g}} \approx \Phi_{\mathrm{fb}} + 2\,\Phi_{\mathrm{B}} + \frac{Q_{\mathrm{depl}}^{\square} + Q_{\mathrm{inv}}^{\square}}{C_{\mathrm{ox}}^{\square}} = V_{\mathrm{th}} + \frac{Q_{\mathrm{inv}}^{\square}}{C_{\mathrm{ox}}^{\square}}. \tag{2.9}$$

Eqn. (2.9) will be very important for deriving the transistor ON-state current using the gradual channel approximation. Volume inversion can be achieved if the bulk silicon substrate is replaced with a silicon-on-insulator (SOI) substrate where the top silicon layer is thinner than the depletion length L_{depl}.

2.2 Metal-Semiconductor Contacts

The metal-semiconductor contact is another fundamental building block of semiconductor devices whose rectifying property can be dated back to the early work of Braun in 1874 [28]. In a conventional MOSFET, the contact between a metal (e.g, silicide) and a heavily doped semiconductor exhibits a contact resistance, which is substantially smaller than the resistance of the channel when the device is switched on. Such low-resistive contacts are often referred to as Ohmic contacts and they serve as an important link between the device and the outside world. On the other hand, a high-resistive Schottky barrier is formed when a metal is brought in contact with a lightly-doped semiconductor, often regardless of the metal work function since the surface Fermi level of the semiconductor material tends

to be pinned at a certain level. The understanding of a Schottky-barrier formation is of vital importance as doping at the nanoscale becomes increasingly difficult due to the finite solubility of dopant species. In addition, the exploration of emerging devices based on, e.g., carbon nanotubes, graphene, MoS_2, etc., often incorporates Schottky-barrier contacts as physical doping is fundamentally difficult, if not impossible, for such novel materials.

The formation of a metal-semiconductor system can be treated by leaving out the oxide layer of a MOS capacitor as depicted in Fig. 2.1. Suppose there are no surface states present and the work function of metal Ψ_{m} is smaller than that of a lightly doped p-type silicon Ψ_{Si}, holes flow from silicon into the metal and the Fermi levels line up when these two materials are brought in contact. The positive charges on the surface of the metal is balanced by negative space charges in Si, which are provided by negative acceptor ions distributed in a space charge region with a depth of L_{depl}.

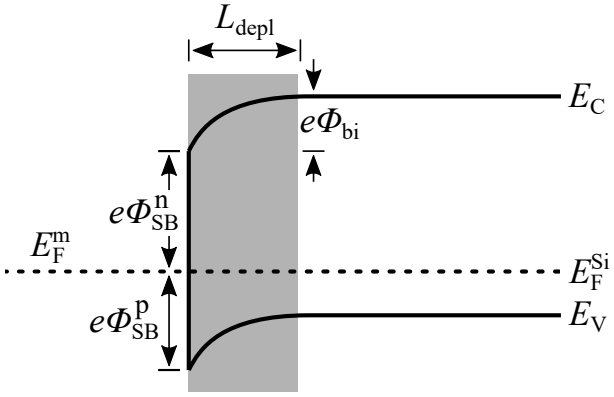


Figure 2.4: The formation of an ideal Schottky barrier when a metal is brought in contact with a lightly p-type doped silicon substrate ($\Psi_{\mathrm{m}} < \Psi_{\mathrm{Si}}$).

The bands in Si bend downwards and give rise to Schottky barriers for holes as well as for electrons:

$$e\,\Phi^{\mathrm{p}}_{\mathrm{SB}} = \Psi_{\mathrm{Si}} - \Psi_{\mathrm{m}} + E^{\mathrm{Si}}_{\mathrm{F}} - E_{\mathrm{V}} = \Psi_{\mathrm{Si}} - \Psi_{\mathrm{m}} + E^{\mathrm{Si}}_{\mathrm{F}} - (E_{\mathrm{C}} - E_{\mathrm{g}}). \tag{2.10}$$

Since the electron affinity χ_{s} is defined as

$$\chi_{\mathrm{Si}} = \Psi_{\mathrm{Si}} - (E_{\mathrm{C}} - E^{\mathrm{Si}}_{\mathrm{F}}), \tag{2.11}$$

the barrier height for holes can then be formulated as

$$e\,\Phi^{\mathrm{p}}_{\mathrm{SB}} = E_{\mathrm{g}} - (\Psi_{\mathrm{m}} - \chi_{\mathrm{Si}}). \tag{2.12}$$

Similarily, the Schottky barrier height for electrons can be derived as

$$e\,\Phi^{\mathrm{n}}_{\mathrm{SB}} = \Psi_{\mathrm{m}} - \chi_{\mathrm{Si}}. \tag{2.13}$$

Eqn. (2.12) and Eqn. (2.13) are called the Schottky-Mott approximation for the barrier height [29]. In reality, such Schottky-barrier heights are never achieved due to the presence

of interface states. Reasons for the existence of interface states are dangling bonds, lattice mismatch between metal and semiconductor, thin oxide formation at the interface during fabrication and metal-induced gap states (MIGS), which lead to a reduced impact of metal work function Ψ_{m} on the barrier height Φ_{SB} [30]. Suppose the density of interface traps is D_{it}, where $[D_{\mathrm{it}}] = \dfrac{1}{\mathrm{m}^2\ \mathrm{J}}$. According to the discussion given by Rhoderick [29], the barrier height for holes is given approximately by

$$e\,\Phi_{\mathrm{SB}}^{\mathrm{p}} = \gamma(E_{\mathrm{g}} - \Psi_{\mathrm{m}} + \chi_{\mathrm{Si}}) + (1-\gamma)\,\Psi_{\mathrm{NL}}, \tag{2.14}$$

where

$$\gamma = \frac{\varepsilon_0\varepsilon_{\mathrm{i}}}{\varepsilon_0\varepsilon_{\mathrm{i}} + e^2\delta D_{\mathrm{it}}}, \tag{2.15}$$

and Ψ_{NL} is called the ''neutral level'', an energy level defined as the position of the Fermi level in silicon that yields an equal occupation of donor-like and acceptor-like interface states [25]. Hence, a net negative surface charge is expected if Ψ_{NL} lies below $E_{\mathrm{F}}^{\mathrm{Si}}$ (i.e. $\Psi_{\mathrm{NL}} < E_{\mathrm{F}}^{\mathrm{Si}}$). δ and ε_{i} are the thickness and relative permittivity of the interfacial layer, respectively. If the density D_{it} approaches 0, the barrier height for holes can be simplified as

$$e\,\Phi_{\mathrm{SB}}^{\mathrm{p}} = E_{\mathrm{g}} - \Psi_{\mathrm{m}} + \chi_{\mathrm{Si}}. \tag{2.16}$$

On the other extreme, if the density D_{it} approaches ∞, then the barrier height for holes is no longer a function of Ψ_{m}, i.e.

$$e\,\Phi_{\mathrm{SB}}^{\mathrm{p}} = \Psi_{\mathrm{NL}}. \tag{2.17}$$

In this case the Fermi level at the interface is ''pinned'' by the surface states at the value Ψ_{NL}, because a small deviation from the neutral level Ψ_{NL} produces a large dipole moment at the interface, which will change the barrier height. This ''negative feedback'' stabilization is called the Fermi level pinning [29].

Although interface states are unavoidable, there are a couple of ways to reduce their impact on the barrier height. A straight-forward approach is to replace directly deposited metal contact with silicides. This avoids the interfacial native oxide layer which in turn provides a more intimate contact between the metal and semiconductor. In this case, however, so-called metal-induced gap states (MIGS) are not supressed and still could lead to Fermi level pinning. The depinning can be achieved by depositing an atomic-scale isolator layer (e.g. Si_3N_4) between the semiconductor and metal to form a potential barrier which supresses the lower energy states [31, 32, 33]. The appropriate band gap of Si_3N_4 reduces the influence of MIGS at the cost of a certain degradation in carrier injection due to the presence of an extra potential barrier.

Gated Metal-Semiconductor Contacts

As it was mentioned in the former section, metal-semiconductor contacts with a low contact resistance is often desired in a conventional MOSFET such that larger effective V_{ds} and V_{gs}

values can be obtained [25]. Such low-resistive Ohmic contacts are traditionally obtained by degenerate doping of silicon where the Fermi energy of the doped area is adjusted, leading to a narrowing of the Schottky junction as depicted in Fig. 2.5(b):

$$L_{\mathrm{depl}} \propto \sqrt{\frac{1}{N_{\mathrm{A}}}}. \tag{2.18}$$

Note that Eqn. (2.18) is derived analogous to Eqn. (2.8). As a result, L_{depl} decreases with a higher doping level and the current conduction becomes dominated by tunneling through the narrowed Schottky barrier (field emission and thermioic field emission). In this case, a large current can be achieved even at low voltages. In contrast, current transport is predominantly determined by thermionic emission for Schottky barriers formed on a lightly doped silicon substrate [30].

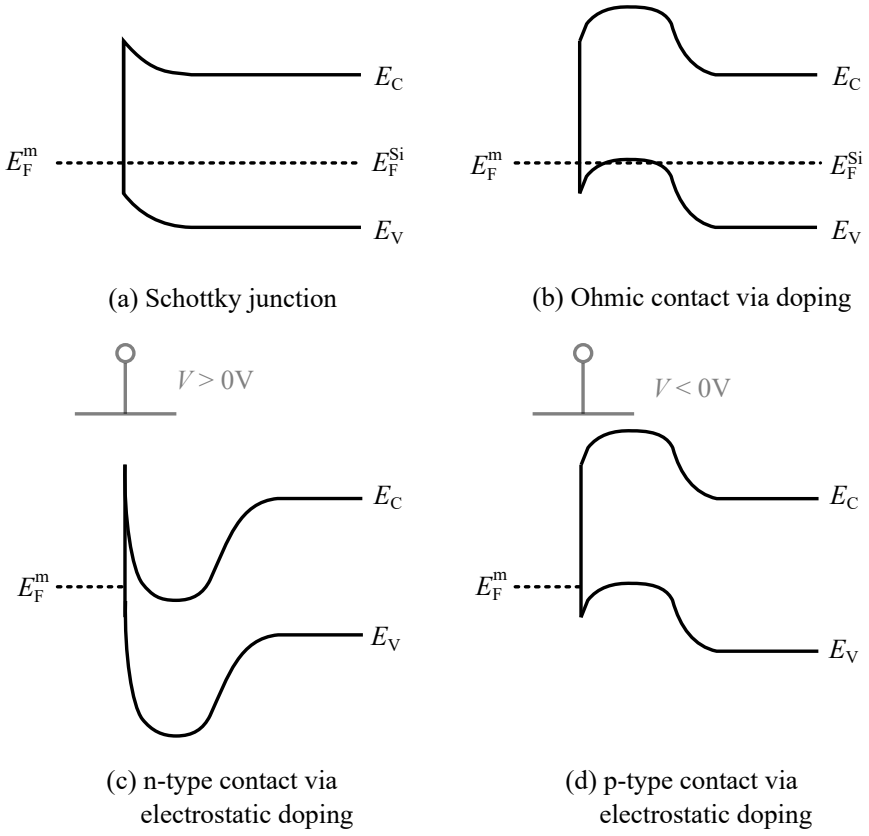


Figure 2.5: Band diagrams of metal-semiconductor contacts. The formation of a Schottky barrier between a metal and lightly p-type doped silicon where $\Psi_{\mathrm{m}} > \Psi_{\mathrm{Si}}$ (a). A p-type Ohmic contact is formed by degenerate doping of Si (b). Similar n-type (c) and p-type Ohmic contacts are obtained by using a gated Schottky barrier.

In this thesis, similar Ohmic behavior is realized by the so-called "programmable Schottky contacts" [34] where narrowing of the barrier width is achieved by applying an external gate bias as illustrated in Fig. 2.5(c) and (d). Such an electrostatic doping allows both n- and

p-type contact formation merely by choosing a different polarity of the external bias voltage. In addition, volume inversion could be achieved by reducing the size of the semiconductor material to avoid neutral regions and minority carriers, thus a stronger gate-channel coupling factor can be achieved, leading to a faster switching of the device. Furthermore, it is worthwhile to note that electrostatic doping allows a flexible tuning of charge carriers in a small volume of silicon even at cryo temperatures whereas dopants introduced via a conventional implantation/diffusion process into a lightly doped semiconductor gradually freeze-out as temperature decreases.

2.3 Conventional and Schottky-Barrier MOSFETs

Since the reconfigurable field-effect transistors to be discussed in this thesis are a type of SB-MOSFET with gated Schottky barriers, it is therfore important to first understand the operation principles of conventional MOSFETs as well as SB-MOSFETs. Fig. 2.6(a) shows a simplified schematic of a conventional, planar, long-channel, n-type MOSFET which is formed by degenerate n-type doping of source and drain regions in a lightly p-type doped silicon substrate. The conductivity of the channel can be controlled by an external bias voltage applied on the gate electrode which is separated from the channel area by a gate dielectric layer. A 2-dimensional electron gas will be formed near the oxide-Si interface if a positive voltage greater than the threshold voltage is applied at the gate electrode, i.e., $V_{\mathrm{gs}} > V_{\mathrm{th}}$. In this case, a conductive channel is formed under the gate oxide to connect source and drain regions. Electrons will flow from source to drain if a positive drain-source voltage is applied since electrons in the high-energy tail of the source Fermi distribution function could pass the energy barrier. In this case, current flowing through the device can be described by the gradual channel approximation [25]:

$$j(x) = en(x,z)v(x), \tag{2.19}$$

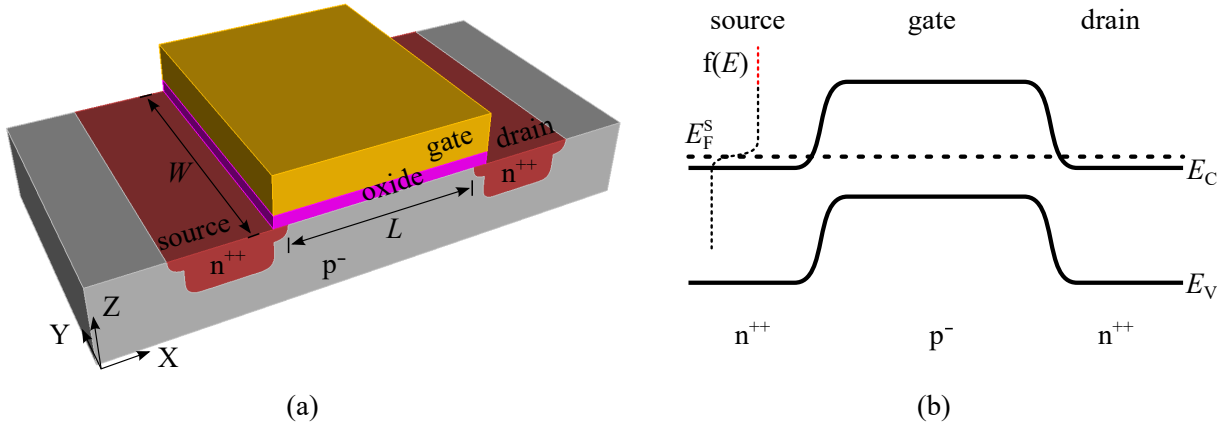


Figure 2.6: Schematic of a conventional n-type MOSFET (a). Band diagram of the device along the x-direction without applying gate and drain voltages (b).

where $j(x)$ is the current density, $v(x)$ is the carrier velocity along the x-direction and can be written as $v(x) = \mu_{\mathrm{n}}\mathscr{E}(x) = \mu_{\mathrm{n}}\dfrac{dV(x)}{dx}$ where μ_{n} is the electron mobility and $\mathscr{E}(x)$ is the electric field strength in x-direction. All parameters are independent of y due to a large transistor width W. The charge carrier density $n(x,z)$ depends on the z-coordinate as inversion charge carriers are confined in a triangular potential well [25] as illustrated in Fig. 2.3. Charges ($[Q^{\square}]$=C/m^2) that are stored in the MOS capacitor can be calculated from Eqn. (2.9) as

$$Q^{\square}(x) = C_{\mathrm{ox}}^{\square}\left(V_{\mathrm{gs}} - V_{\mathrm{th}} - V(x)\right), \quad \text{for } 0 \leq x \leq L, \tag{2.20}$$

where $C_{\mathrm{ox}}^{\square}$ is the sheet capacitance. The current flowing through the device can be calculated by integrating Eqn. (2.19) along the width W and over the z-coordinate:

$$I = \mu_{\mathrm{n}}\int_0^W dy\int_0^{d_{\mathrm{ch}}} en(x,z)dz\frac{dV(x)}{dx} = W\mu_{\mathrm{n}}Q^{\square}(x)\frac{dV(x)}{dx}, \quad \text{for } 0 \leq x \leq L, \tag{2.21}$$

where d_{ch} is the depth of the triangular potential well along the z-axis. Finally, Eqn. (2.21) is multiplied with dx at both sides and integrated along the x-axis yielding the current expression for the transistor in its ON-state:

$$I = \mu_{\mathrm{n}}C_{\mathrm{ox}}^{\square}\frac{W}{L}\left(V_{\mathrm{gs}} - V_{\mathrm{th}})V_{\mathrm{ds}} - \frac{V_{\mathrm{ds}}^2}{2}\right). \tag{2.22}$$

Depending on the drain-source voltages V_{ds} applied, Eqn. (2.22) can be used to describe the linear and saturation regimes of transistor operation when $V_{\mathrm{gs}} \geq V_{\mathrm{th}}$. Note that when $V_{\mathrm{ds}} \geq V_{\mathrm{gs}} - V_{\mathrm{th}}$, the transistor enters into the saturation regime and pinch-off of the channel occurs at the channel-drain junction, i.e., the channel disappears at the drain end. However, current still flows from drain to source since accelerated electrons still can pass the pinch-off area where the carrier density is low, yielding an almost constant current in the saturation regime. Increasing V_{ds} further will lead to an acceleration of electrons in the channel and eventually cause degradation of stability and performance of the transistor. Such hot electron effects can be mitigated by creating a shallow lightly-doped drain (LDD) region to increase the depletion width at the drain side, leading to a reduced electric field at the drain-channel p-n junction. The LDD region extends slightly into the channel as depicted in Fig. 2.6 and hence the gate-source and gate-drain parasitic capacitances are also increased. Such effects become more pronounced as the transistor dimensions are being continuously scaled down. Furthermore, the scaling gives rise to short-channel effects (SCEs) such as drain induced barrier lowering (DIBL) and an increased gate leakage current and OFF-state drain-source current.

The transistor is in the OFF-state if $V_{\mathrm{gs}} < V_{\mathrm{th}}$. In this regime, the inversion charge in the channel is negligibly small for the calculation of the threshold voltage but it allows a small amount of charge carriers to flow from source to drain. The inversion charge density can be calculated as

$$n = N_{\mathrm{C}}\exp\left(-\frac{E_{\mathrm{C}} - E_{\mathrm{F}}^{\mathrm{Si}}}{k_{\mathrm{B}}T}\right), \tag{2.23}$$

where $N_C = 2.8 \times 10^{19}\,\mathrm{cm}^{-3}$ is the effective density of states of the conduction band for silicon. Therefore, the conduction band bends towards the Fermi level and the inversion charge increases exponentially with increasing V_{gs}, leading to an exponential increase in drain-source current. Since a 2D transistor can be considered as consisting of independent 1-dimensional modes, the total current can be calculated by summing up contributions from individual subbands in the y-direction. As it turns out, the current of both a 2D and a 1D transistor has the same mathematical form of a constant prefactor multiplied with an exponential Boltzmann factor [25]. Therefore, it is possible to calculate the inverse subthreshold slope of a 2D MOSFET using a 1D transport model such that the current I_{ds}^{1D} can be computed using the Landauer formula as

$$I_{ds}^{1D} = \int \frac{2e}{h} T(E)\,[f_S(E) - f_D(E)]\,dE, \tag{2.24}$$

where h is the Planck's constant, and $T(E)$ is the transmission probability. It is assumed that $T(E) = 1$ above the barrier and $T(E) = 0$ below the barrier. Under a positive drain-source bias, $f_D(E)$ is substantially smaller than $f_S(E)$. Using the top-of-the-barrier model [25], Eqn. (2.24) can be re-written as:

$$I_{ds}^{1D} = \int_{\Psi_S^{max}}^{\infty} \frac{2e}{h} \exp\left(-\frac{E - E_F^S}{k_B T}\right) dE = \frac{2e k_B T}{h} \exp\left(\frac{E_F^S - \Psi_S^{max}}{k_B T}\right), \tag{2.25}$$

where Ψ_S^{max} is the maximum value of surface potential energy across the channel. The source Fermi distribution function $f_S(E) \approx \exp\left(-\frac{E - E_F^S}{k_B T}\right)$ in case $E - E_F^S \gg kT$ (which is indeed the case for a transistor in the OFF state). Thus, the inverse subthrehold slope S – a figure of merit to characterize the transition time between OFF (low current) and ON (high current) states – is then defined as [25, 35]:

$$S = \frac{\partial V_{gs}}{\partial\,(\log_{10} I_{ds}^{1D})} = \frac{\partial V_{gs}}{\partial \Psi_{gs}} \frac{\partial \Psi_{gs}}{\partial \Psi_S^{max}} \frac{\partial \Psi_S^{max}}{\partial\,(\log_{10} I_{ds}^{1D})} = \frac{1}{-e} \frac{C_\Sigma^\square}{C_{ox}^\square}\,(-k_B T \ln 10), \tag{2.26}$$

where $C_\Sigma^\square$ is the total capacitance seen at the gate electrode that comprise the oxide capacitance $C_{ox}^\square$, the capacitance of the depletion region $C_{depl}^\square$, the capacitance of the inversion layer $C_{inv}^\square$ (can also be denoted as the quantum capacitance $C_q^\square$ [25]), the interface capacitance $C_{it}^\square$, and parasitic capacitances such as $C_s^\square$ and $C_d^\square$, etc. Above all, the term $C_\Sigma^\square / C_{ox}^\square \geq 1$ and hence the inverse subthreshold slope has a theoretical minimum value of $S_{min} = \frac{k_B T}{e} \ln 10 \approx 60\,\mathrm{mV/dec}$ at room temperature.

Different than a conventional MOSFET where current flow is blocked by two reversely biased p-n junctions in the OFF state, two metallic electrodes are in direct contact with a moderately doped silicon channel for Schottky-barrier MOSFETs built on SOI as depicted in Fig. 2.7(a). As a result, two Schottky barriers are formed at the contact-channel interface as illustrated in the band diagram under equilibrium state displayed in Fig. 2.7(b). Recently, Schottky-barrier MOSFETs have attracted a great deal of interest since replacing the

doped source/drain regions with metals allows avoiding dopant-related issues prevalent in nanoscale conventional MOSFETs. However, different than a conventional MOSFET which is a unipolar device, the absence of a band gap in the metallic source/drain regions allows both electron and hole injection into the channel (thermionic emission part is indicated in the Boltzmann tail shown in Fig. 2.7(b) for both electrons and holes), leading to ambipolar operation of a Schottky-barrier MOSFET. This is rather undesired as an increase in OFF-state leakage current due to the injection of the other charge carrier type makes the Schottky-barrier MOSFET less ideal as a proper switch for logic circuit implementations.

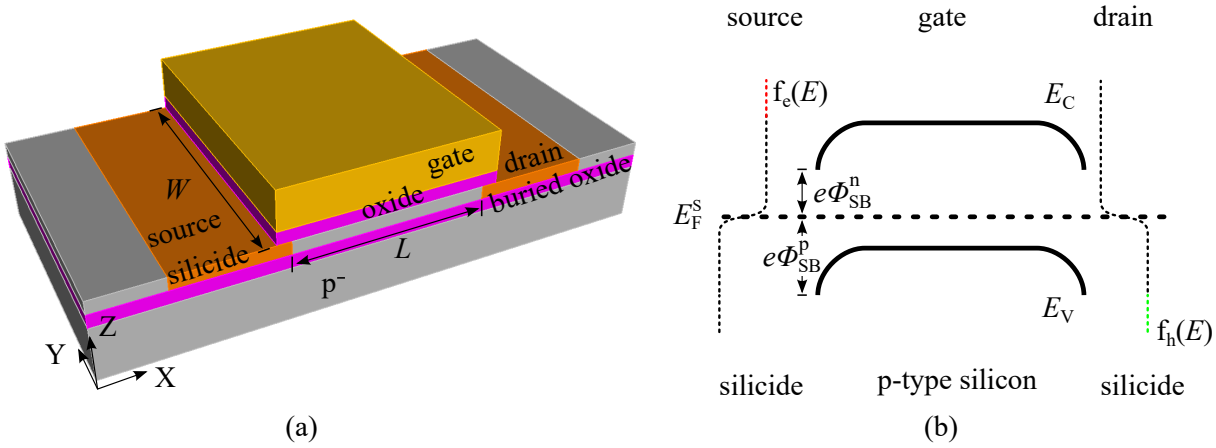


Figure 2.7: Schematic of a Schottky-barrier MOSFET built on a silicon-on-insulator substrate (a). Band diagram of the device along the x-direction without applying gate and drain voltages (b).

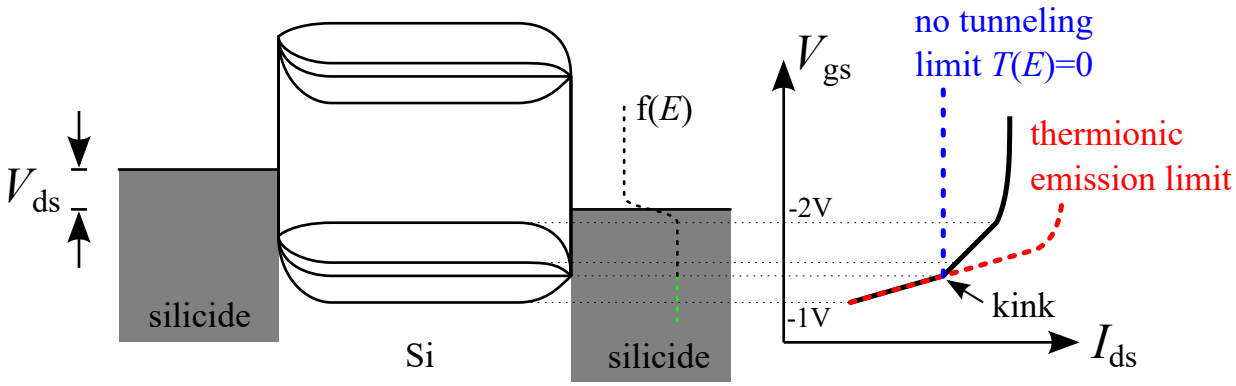


Figure 2.8: Band diagram and transfer characteristic of a Schottky-barrier MOSFET.

The operation of a Schottky-barrier MOSFET is explained with the band diagram under several gate voltages as depicted in the left panel of Fig. 2.8. At small gate voltages ($V_{gs} \approx -1\,V$), the potential maximum of the valence band lies below the Schottky barrier at the drain side. Hence, carrier injection is dominated by holes that belong to high-engergy tail of the Boltzmann distribution function (green dashed lines). In this regime, the

Schottky-barrier MOSFET behaves similar to a conventional p-type MOSFET in terms of a steep inverse subthreshold slope close to the thermionic emission limit ($S \approx 60\,\mathrm{mV/dec}$). As the gate voltage increases further ($V_{\mathrm{gs}} < -1.3\,V$), the potential maximum of the valence band drops below the Schottky barrier at the drain side. As a result, a further increase in drain current will then be determined by the thermionic emission current $I_{\mathrm{thermionic}}$ and the tunneling current I_{tunnel}. However, the thermonic emission current is relatively small for Schottky barriers defined by nickel silicide and silicon junction [36]. Therefore, the ON current is predominantly determined by the tunneling of holes through the Schottky barrier. The inverse subthreshold slope will be determined by the tunneling rate of charge carriers and hence will be substantially larger than the thermionic emssion limit of $60\,\mathrm{mV/dec}$. According to Ref. [25], the inverse subthreshold slope of a thin-body SB-MOSFET in the tunneling regime can be derived as

$$S = \frac{k_{\mathrm{B}}T}{e}\ln 10 \frac{1}{1 - \exp\left(\dfrac{-d_{\mathrm{tunnel}}}{\lambda}\right)}, \tag{2.27}$$

where d_{tunnel} is the tunneling distance, and λ is the screening length, a length scale for potential variations and reflects the particular device geometry under consideration [37, 38]. In practical cases, $d_{\mathrm{tunnel}} < \lambda$. Hence, Eqn. (2.27) can be approximated as

$$S \approx \frac{k_{\mathrm{B}}T}{e}\ln 10 \left(\frac{1}{2} + \frac{\lambda}{d_{\mathrm{tunnel}}}\right). \tag{2.28}$$

As a result, the inverse subthreshold slope of a Schottky-barrier MOSFET is often substantially larger than a conventional MOSFET.

2.4 Nanowire Field-Effect Transistors

The electrostatics in the channel region of a conventional MOSFET depicted in Fig. 2.6 can be computed using the 2-D Poisson's equation [25]:

$$\frac{\partial^2 \Phi(x,z)}{\partial x^2} + \frac{\partial^2 \Phi(x,z)}{\partial z^2} = -\frac{e(n(x,z) \pm N)}{\varepsilon_0 \varepsilon_{\mathrm{Si}}}, \tag{2.29}$$

where the potential $\Phi(x,z)$ is independent of y due to the assumption of a wide MOSFET. $n(x,z)$ is the density of the inversion charge. The background doping is assumed to be uniform and is denoted as N with either donors ($+N_{\mathrm{D}}$) or acceptors ($-N_{\mathrm{A}}$). In addition, $\varepsilon_{0,\mathrm{Si}}$ are the vacuum permittivity and the relative permittivity of silicon, respectively.

In the case of a silicon nanowire field-effect transistor depicted in Fig. 2.9, the electrostatics can be reduced from Eqn. (2.29) to a 1-D modified Poisson equation using a quadratic approximation of the potential distribution for a fully-depleted channel as [25, 39, 40, 41]:

$$\frac{\partial^2 \Phi_f(x)}{\partial x^2} - \frac{\Phi_f(x) - \Phi_{\mathrm{S}}^{\mathrm{max}}}{\lambda^2} = -\frac{en(x)}{\varepsilon_0 \varepsilon_{\mathrm{Si}}}, \tag{2.30}$$

where $\Phi_f(x)$ is the potential at the channel-dielectric interface. The geometric screening length λ is equal to [42]

$$\frac{\lambda}{\varepsilon_{\mathrm{Si}}} = \sqrt{\frac{L_{\mathrm{depl}}}{\varepsilon_{\mathrm{Si}}}\frac{d_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}}}, \tag{2.31}$$

where L_{depl} is the thickness of the depletion region. As a result, λ can be regarded as the geometric mean of the depletion region depth and the oxide thickness. Full depletion can be assumed due to the small cross-sectional size of a 1-D silicon nanowire. Hence, Eqn. (2.31) can be written as [38]

$$\lambda = \sqrt{\left(\frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}}\right) d_{\mathrm{nw}} d_{\mathrm{ox}}}. \tag{2.32}$$

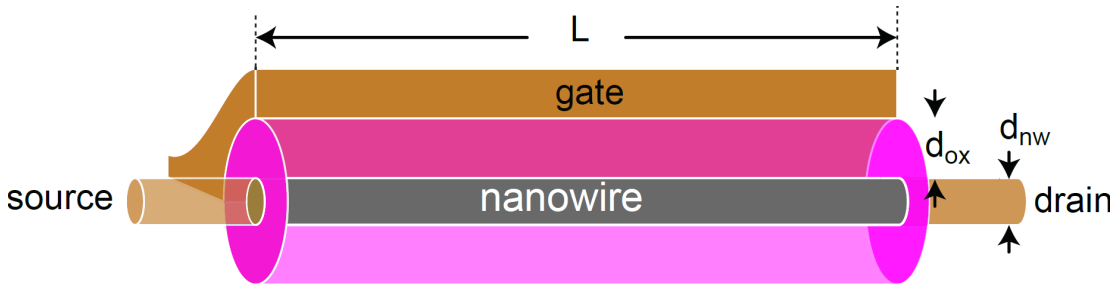


Figure 2.9: Schematic of a single-gate silicon nanowire MOSFET built on a silicon-on-insulator substrate with the gate oxide thickness d_{ox}, diameter of silicon nanowire d_{nw}, and channel length L.

Silicon nanowire transistors are less vulnerable to short-channel effects (SCEs) as the cross-sectional size (i.e. d_{nw}) can be made very small to ensure a substantially larger channel length than the screening length (i.e. $L \gg \lambda$)[1]. The maximum of surface potential $\Phi_{\mathrm{S}}^{\mathrm{max}}$ in a long-channel device can be calculated as [38]

$$\Phi_{\mathrm{S}}^{\mathrm{max}} \approx 2\sqrt{-(\Phi_{\mathrm{g}} + \Phi_{\mathrm{bi}})(\Phi_{\mathrm{d}} - (\Phi_{\mathrm{g}} + \Phi_{\mathrm{bi}}))}\exp(-L/2\lambda) + \Phi_{\mathrm{g}} + \Phi_{\mathrm{bi}} \approx \Phi_{\mathrm{g}} + \Phi_{\mathrm{bi}}, \tag{2.33}$$

[1]The screening length λ denotes the spatial extent of a channel-electrode junction. In a short-channel device, a channel length L on the same order of λ might lead to an overlapping of the source-channel and drain-channel junctions, leading to a reduction in potential maximum in the channel $\Phi_{\mathrm{S}}^{\mathrm{max}}$. This can be understood using a simple capacitor model of an ultra short channel MOSFET: the variation of channel potential can be written as $\delta\Phi_{\mathrm{S}}^{\mathrm{max}} \approx \frac{C_{\mathrm{ox}}^{\square}}{C_{\Sigma}^{\square}}\delta\Phi_{\mathrm{g}} + \frac{C_{\mathrm{d}}^{\square}}{C_{\Sigma}^{\square}}\delta\Phi_{\mathrm{d}}$ using the model of a capacitive potential divider. Whereas in a long-channel device, $C_{\mathrm{d}}^{\square}$ is negligibly smaller than $C_{\Sigma}^{\square}$ and hence $\Phi_{\mathrm{S}}^{\mathrm{max}}$ is solely dependent on the gate potential Φ_{g}. In an ultra-short channel MOSFET, the drain capacitor contributes a substantial fraction to the total capacitance, leading to a dependence of channel potential on the drain potential. It is worthwhile to note that the screening length can also be approximated using this model: in a short channel device $C_{\mathrm{d}} \approx \frac{\varepsilon_0\varepsilon_{\mathrm{Si}}W d_{\mathrm{Si}}}{L}$ which exhibits a value comparable to the gate oxide capacitance $C_{\mathrm{ox}} = \frac{\varepsilon_0\varepsilon_{\mathrm{ox}}WL}{d_{\mathrm{ox}}}$. Hence, a transistor with a channel length of $L \approx \sqrt{\left(\frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}}\right) d_{\mathrm{Si}} d_{\mathrm{ox}}}$ is expected to suffer from short channel effects.

where Φ_{d}, Φ_{g}, Φ_{bi} are the drain, gate and the built-in potentials, respectively. Note that the background doping $N_{\mathrm{A,D}}$ is not implemented in Eqn. (2.30). This is due to the fact that a 1D nanowire architecture can be considered to be fully-depleted within a broad range of of channel doping concentrations. Hence, the channel doping is taken into account by a shift of the built-in potential Φ_{bi}. Eqn. (2.33) indicates that a stronger gate-channel coupling factor $\partial\Phi_{\mathrm{gs}}/\partial\Phi_{\mathrm{S}}^{\mathrm{max}} \approx 1$ can be achieved since $\Phi_{\mathrm{S}}^{\mathrm{max}} = \Phi_{\mathrm{g}} + \Phi_{\mathrm{bi}}$ for a long-channel device that does not suffer from drain-induced barrier lowering (DIBL). As a result, the surface potential maximum $\Phi_{\mathrm{S}}^{\mathrm{max}}$ can well be controlled by an external gate voltage. As it will become clear below, this condition is approached by reaching the so-called quantum capacitance limit and thereby is the key to obtain a linear $I_{\mathrm{d}} - V_{\mathrm{ds}}$ behavior in the triode operation regime of a nanowire SB-MOSFET.

In this thesis, so-called reconfigurable field-effect transistors (RFETs) employing additional gate structures are built on silicon nanowires fabricated from a top-down approach, leading to an enhanced gate control and improved device performance. As it turns out, the RFETs demonstrate a significantly better performance compared with a single-gate SB-MOSFET: the ambipolar behavior is suppressed and exploited to operate the device either as unipolar *p*- or *n*-type. Furthermore, a steep inverse subthreshold slope comparable to a state-of-the-art conventional MOSFET could be achieved in certain operation modes.

The next chapter first deals with the key techniques used for the fabrication of RFETs based on SiNWs from a top-down approach and nickel silicidation process. In particular, a useful fabrication technique related to high temperature annealing in hydrogen ambient at reduced pressure is introduced for improving the surface roughness and transforming the cross-section from a triangle into a circle while maintaining its area. In addtion, a modified electron beam evaporation setup is presented to obtain a reliable lift-off process, which significantly improves the fabrication yield and device performance.

Chapter 3

Device Fabrication Techniques

Performance and characteristics of electronic devices are not only dependent on the material properties and physics behind, but they are also closely related to the device fabrication techniques. This chapter provides an overview of the key techniques used in the fabrication of reconfigurable devices to be discussed in later chapters. The key fabrication modules presented in this chapter are underpinned with a brief overview of the physical and chemical principles involved whereas some other standard fabrication techniques are supplemented in the appendix.

3.1 Silicon Wet Anisotropic Etching

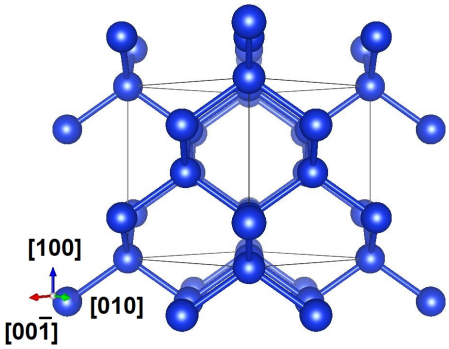


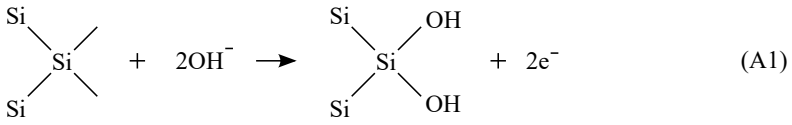
Figure 3.1: Crystalline structure of silicon. The paper lies in the $(01\bar{1})$ plane.

Anisotropic wet chemical etching of silicon is a convenient and economic fabrication technique to create high-quality micro- and nano-scale structures for the realization of microelectromechanical systems (MEMS) [43, 44], solar cells [45] and transistors [46, 47].

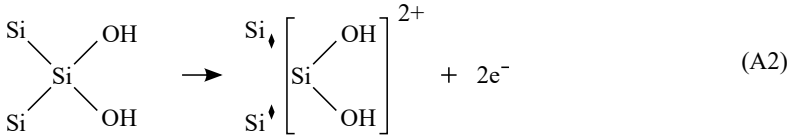
Part of the work in Chapter 3 is published in Applied Sciences (DOI: 10.3390/app9183823), in IEEE Journal of Microelectromechanical Systems (DOI: 10.1109/TED.2021.3081527), and in Journal of Vacuum Science and Technology B (DOI: 10.1116/6.0001161)

Silicon can be etched anisotropically in an aqueous alkaline solution due to its distinct etch rates of different crystalline planes. The {111} planes have the slowest etching speed, while {110} and {100} are the fast etching planes. A simple model to explain this is illustrated with the crystalline structure of silicon as depicted in Fig. 3.1: two interpenetrating face-centered cubic Bravais lattices, displaced along the body diagonal of the cubic unit cell by one quarter the length of the diagonal. The total number of chemical bonds exposed to an alkaline solution for each silicon atom on {111}, {100}, and {110} planes are 1, 2, and 3, respectively. For {110} planes these 3 chemical bonds comprise 1 dangling bond and 2 in-plane back bonds whereas all exposed bonds are dangling bonds for {111} and {100} planes. Furthermore, the density of surface atoms on the {111}, {100}, and {110} planes are 7.8×10^{14} atoms/cm^2, 6.8×10^{14} atoms/cm^2, and 9.6×10^{14} atoms/cm^2, respectively (see Appendix V for derivations). Therefore, {110} planes have the highest density of exposed chemical bonds whereas {111} planes possess the lowest density. All these exposed chemical bonds are the origin of hydroxylation, which is the main reason for dissolving silicon in an alkaline solution [48]. In other words, an alkaline etchant removes silicon atoms more rapidly, when they have fewer bonds holding to the lattice.

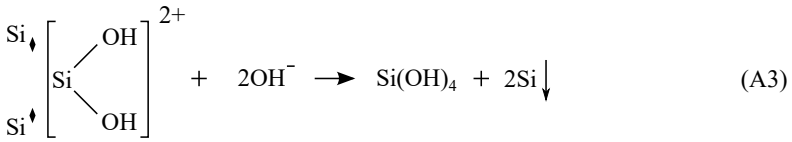
The potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) based solutions are used most commonly for the process of anisotropic etching of crystalline silicon. Other hydroxide alkaline solutions such as sodium hydroxide (NaOH), cesium hydroxide (CsOH), ammonium hydroxide (NH_4OH), hydrazine (H_2N-NH_2), and ethylenediamine pyrocatechol (EDP) are either rarely used or carcinogenic[2]. According to Refs. [48, 52, 53], silicon atoms on a (100) surface react with the OH^- groups in an alkaline solution under the following proposed reactions:



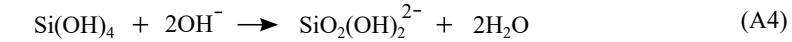
(A1)



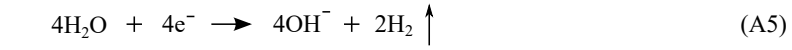
(A2)



(A3)



(A4)



(A5)

[2] Recent studies [49, 50, 51] reveal that TMAH is also an extremely hazardous chemical, protective clothing such as apron, chemical-resistant gloves, and face shield is mandatory when working with TMAH.

Each silicon atom on a (100) surface has two dangling bonds and two back bonds. First, these two dangling bonds are exposed after the removal of native oxide in a hydrofluoric acid (HF) solution and they become hydroxilated after immersion into a hydroxide alkaline solution and deliver two electrons that are considered to be confined to the silicon surface [53]. Next, the $Si_3[OH]_2$ complex ionizes and two more electrons are delivered (to the silicon surface) as illustrated in Eqn. (A2). Subsequently, the positive ion combines with two further OH^- ions from the solution to form $Si(OH)_4$. The fully hydroxylated silicon at the surface forms a water-soluble hydroxide ion as depicted in Eqn. (A4). Finally, the electrons at the silicon surface react with water molecules and hydrogen gas bubbles are generated as a by-product. All six equations listed above can be combined and reduced to Eqn. (A6) as displayed below:

$$Si + 2H_2O + 2OH^- \longrightarrow SiO_2(OH)_2^- + 2H_2 \uparrow \qquad \text{(A6)}$$

It has to be noted that the reaction scheme proposed above provides an explanation of heavily boron-doped silicon ($>10^{19}$ atoms/cm^3) as an etch stop layer [54]. Other etch stop or masking techniques include choosing materials that exhibit a low etching rate such as Cr, SiO_x, and SiN_x. Alternatively, this could also be achieved by changing the electrochemical potential of the substrate. Suppose an epitaxial *n*- type layer is grown on a *p*- type substrate and the resulting *pn* junction is reversely biased, the etching will stop at the *n*- type layer since an anodic oxide layer is generated by the positive potential [55]. In this dissertation, SiO_x, and SiN_x are used as the etch stop and masking material for the realization of nanostructures utilizing their material selectivity in different chemicals. In the next section, etching behavior of two commonly used alkaline solutions, namely, KOH and TMAH, will be investigated and discussed to develop an optimized etching recipe for the generation of nanostructures.

3.1.1 Etching behavior of KOH and TMAH based solutions

Anisotropic etching of silicon in an alkaline solution is predominantly determined by OH^- ions. Therefore, the concentration and temperature are supposed to play an important role. In addition, the etching behavior is also influenced by the weak adsorption of cations, e.g., K^+ and TMA^+, to the silicon surface [48]. Moreover, the addition of non-ionic surfactants such as isopropyl alcohol (IPA) also has an impact on the etching. In this section, the etching behavior of both KOH and TMAH based solutions will be investigated to develop a self-limiting etching recipe that is suitable for the generation of nanostructures with smooth etched surfaces.

As it was mentioned before, the etch rate of both KOH and TMAH are supposed to be correlated with the concentration and temperature of the solution. Indeed, it has been reported that the etch rate of (100) and (110) planes in a KOH solution reaches its maximum at a concentration of 25 % when the temperature is kept at 70 °C. Similarly, etch rate of the

(110) facet and some high-order planes in a TMAH solution (80 °C) shows a maximum at a concentration of 20 % [56]. This obvious since the chemical reaction consumes a substantial amount of water as displayed in the proposed reaction equation (A6), indicating stirring during etching is necessary to avoid concentration gradients. In addition, stirring is also beneficial to get rid of hydrogen bubbles and thus could ensure a homogeneous contact between the etchant solution and silicon surface. Furthermore, the etch rate increases with increasing temperature for both KOH and TMAH based solutions. The dependence of the etching rate $R(T)$ on temperature T ([T]=Kelvin) can be described with the equation shown below [48]:

$$R(T) = R_0 e^{-\frac{Q}{k_B T}}, \tag{3.1}$$

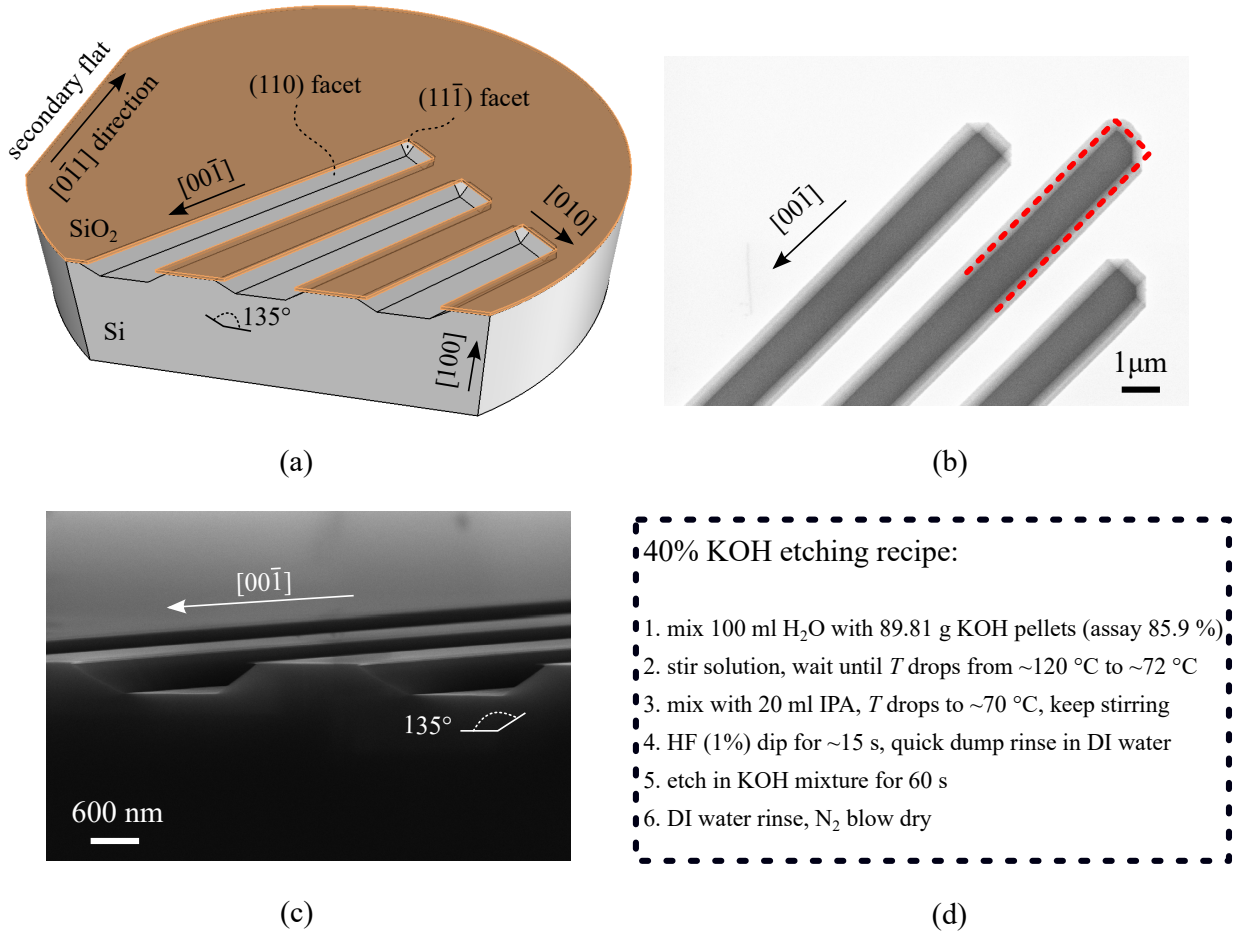


Figure 3.2: Etching of line structures patterned along <100> directions of a (100)-oriented silicon wafer in 40 % KOH solution with IPA additive at 70°C for 60 s. A schematic drawing of the hardmask patterning and etching result (a). A top-view scanning electron micrograph of the etched profile where the patterned hardmask is framed in red dashed lines (b). A cross-sectional scanning electron micrograph shows that the etched trapezoidal structure is bounded by two slanted {110} planes (c). KOH etching recipe with IPA additive (d).

where k_B is the Boltzmann constant and Q is the activation energy for different crystalline planes. The Arrhenius plot ($\ln R(T) - 1/T$) of Eqn. (3.1) gives a straight line:

$$\ln R(T) = \ln R_0 - \frac{Q}{k_B T}, \tag{3.2}$$

from which the activation energy Q can be extrapolated from the slope of the plotted curve.

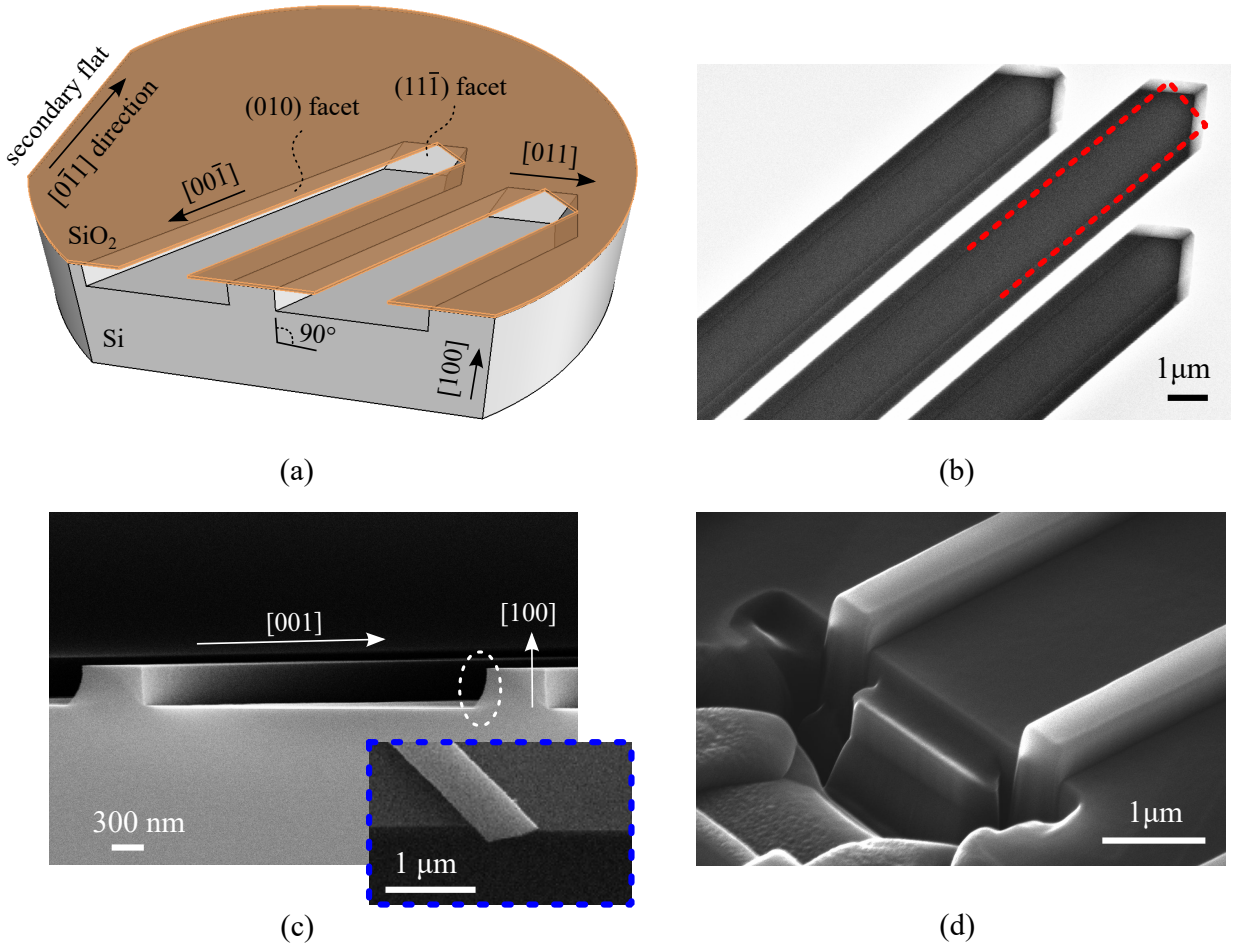


Figure 3.3: Etching of line structures patterned along <100> directions of a (100)-oriented silicon wafer in 40 % KOH solution without IPA additive at 70°C for 60 s. A schematic drawing of the hardmask patterning and etching result (a). A top-view scanning electron micrograph shows the two etched sidewalls are identical. The patterned hardmask is framed in red dashed lines (b). A cross-sectional scanning electron micrograph shows that the left sidewall after cleaving is not perpendicular to the (100) plane (c). The inset framed in blue shows that the arc shape is due to cleaving. The cross-section prepared by focused ion beam using Ga^+ ions reveals that both sidewalls are perpendicular to the (100) plane (d).

Apart from temperature and concentration considerations, it has been reported that the addition of surfactants such as isopropyl alcohol (IPA) also has an impact on the etching

speed. The reduction in etching speed is particularly pronounced for crystalline planes with step monohydride (SM) type of bonds such as {110} [57]. This could change the etching anisotropy of KOH since the etching speed for {110} planes drops below that for {100}. Fig. 3.2 shows the etching result in a 40 % KOH solution at 70 °C with IPA additive for 60 s (cf. recipe shown in Fig. 3.2(d)). The initial oxide hard mask is patterned into line structures along <100> directions of a (100)-oriented silicon wafer as illustrated with the brown top layer shown in Fig. 3.2(a) and red-dashed lines in Fig. 3.2(b). After the etching process, trapezoidal structures bounded by two tapered {110} facets reveal that the etching speed of {110} planes is slower than that of {100} planes in a KOH solution with the addition of IPA. On the other hand, the etched structure becomes bounded by two vertical {100} planes (cf. Fig. 3.3(a)) merely by removing IPA while keeping all other parameters unchanged (40 % KOH, 70 °C, 60 s). In this case, the etching speed for {110} planes is larger than that for {100}. Note that the cross-section displayed in Fig. 3.3(c) shows a vertical sidewall on one side and an arc-shaped structure on the other side (framed in a dashed white ellipse). The reason for this arc-shaped structure is likely due to cross-section preparation with a diamond scratch and cleaving method since the top-view depicted in the inset of Fig. 3.3(c) clearly shows an extra corner after cleaving. To avoid this, a cross-section is prepared by focused ion beam using Ga^+ ions as depicted in Fig. 3.3(d). It is clear that both sidewalls are perpendicular to the (100)-oriented substrate, further confirming the vertical {100} etched facets on both sides. Therefore, the addition of surfactants such as IPA could change the etching anisotropy of KOH due to a reversed etching speed for {110} and {100} planes.

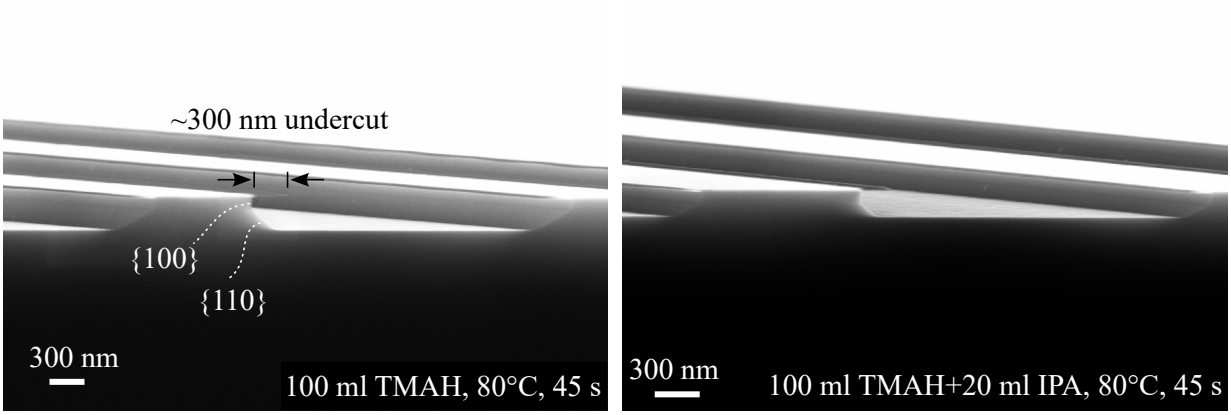
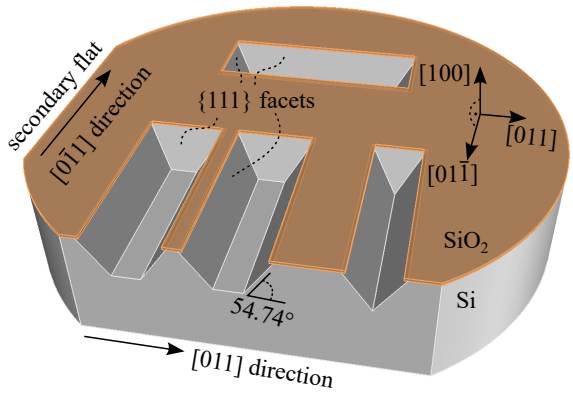


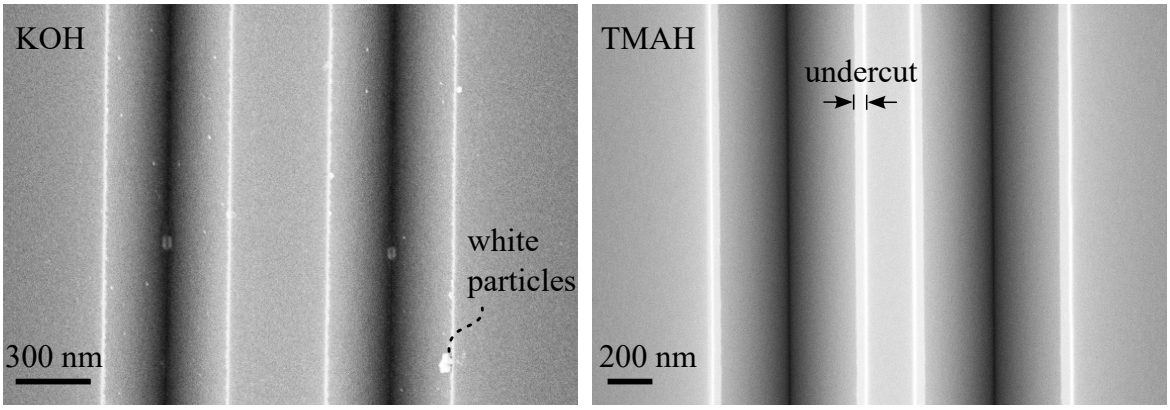
Figure 3.4: Etching of line structures patterned along <100> directions of a (100)-oriented silicon wafer in a 25 % TMAH solution at 80 °C for 45 s both for without adding IPA (a) and with the addition of 20 ml IPA (b).

Compared with KOH, the etching anisotropy stays mostly unchanged for TMAH based solutions for both with and without adding IPA as depicted in Fig. 3.4. The etched sidewalls comprise both vertical {100} and 45 °-inclined {110} facets using the same hardmask (brown

top layer) shown in Fig. 3.2(a) and Fig. 3.3(a). The presence of both {100} and {110} facets indicates a similar etching speed for both planes.



(a)



(a) (c)

Figure 3.5: Anisotropic wet etching of line structures patterned along <110> directions of a (100)-oriented silicon wafer. The etching leads to V-grooves bounded by {111} planes inclined at 54.74 ° with respect to the substrate surface (a). Top-view scanning electron micrographs show experimental results in a KOH based solution with almost no undercut of the hardmask (b) and a relatively larger undercut in a TMAH based solution (c).

Another difference between the etching behavior of KOH and TMAH based etchants lies in the etching speed for {111} facets as depicted in Fig. 3.5. The initial oxide hard mask is patterned into line structures along <110> directions of a (100)-oriented silicon wafer as illustrated in the brown top layer of Fig. 3.5(a). After the etching process, V-groove structures are formed by two inclined {111} facets. The {111} silicon planes are inclined at an angle of $\cos^{-1}(\frac{\begin{pmatrix}0\\0\\1\end{pmatrix}\cdot\begin{pmatrix}1\\1\\1\end{pmatrix}}{1\cdot\sqrt{3}}) = 54.74^\circ$ to the surface of a (100)-oriented silicon wafer. The relatively large undercut of the hardmask shown in Fig. 3.5(b) reveals a faster etching

speed of {111} facets in a TMAH based solution compared to that for KOH.

For the generation of nanostructures, a precise control of the etched dimensions is necessary. It is therefore desirable to develop a self-limiting process where the etching could terminate, e.g. at a slow etching plane or at an etch stop layer such as the buried oxide of a silicon-on-insulator substrate. On the other hand, a more reproducible etching result could be achieved by slowing down the etching speed. In the case of KOH, a highly concentrated solution ($> 40\,\%$) at low temperatures ($< 80\,^{\circ}\mathrm{C}$) saturated with IPA is desired as it demonstrates a very low etching speed for {111} planes and a relatively low speed for {110} planes (see the small undercut in Fig. 3.3(b)). Furthermore, the addition of IPA has also demonstrated an improvement in surface roughness of the etched facets [58].

However, the presence of potassium ions in a KOH based solution makes it less attractive for the fabrication of electronic devices, although a complete removal of K^+ ions seems to be possible with boiling water [48] or a modified SC-2 step ($HCl : H_2O_2 : H_2O = 1 : 1 : 1$) in a standard cleaning procedure [25]. In addition, it has been reported that 10 % KOH often leaves white-colored gel-like products such as oxyhydrates on an etched surface [48]. Highly concentrated KOH solutions (40 %) often generate white particles after the etching process as depicted in Fig. 3.5(a). Although these white particles could be removed with a standard cleaning procedure, KOH etching tied with a subsequent wafer cleaning leads to extra chemical consumption and hence an increased cost. Furthermore, KOH exhibits slightly lower etch selectvity of Si to SiO_2 ($\sim$150 : 1) compared with TMAH, which exerts requirements on oxide thickness especially for long etching durations.

TMAH based echants were first proposed by Schnakenberg [59] in 1991 as an attractive alternative to KOH. The replacement of potassium ions with TMA^+ leads to its full compatibility with the CMOS technolgy. In the following, TMAH etching parameters will be investigated to develop an etching recipe that delivers smooth etched surfaces and in the ideal case a reduced etching rate to enable a more controllable and reproducible process. In fact, it has been demonstrated that the etching rate for {100} planes reduces with increasing TMAH concentration and the surface roughness significantly improves for a concentration higher than 22 % [60]. Furthermore, the addition of surfactants (e.g., IPA) leads to a reduced etch rate and further improves the roughness of etched sufaces [61]. Figure 3.6 shows typical V-groove structures formed by etching line structures along <110> directions of a (100)-oriented wafer in a TMAH based solution with different parameters (cf. Fig. 3.5). The inititial Si_3N_4 hardmask is thermally grown in a rapid thermal processing chamber using ammonia (NH_3):

$$3\mathrm{Si} + 4\mathrm{NH_3} \rightarrow \mathrm{Si_3N_4} + 6\mathrm{H_2}. \tag{3.3}$$

The mechanism of thermal nitridation is similar to thermal oxidation [62]. However, Si_3N_4 is a very dense material and hence it demonstrates a strong impermeability that limits the thickness to less than 5 nm, even at very high temperatures [63]. Silicon nitride is an ideal candidate as the masking material for anisotropic wet etching of silicon since it features a

remarkably slow etching rate. In this work, the nitride layer is grown at 1050 °C for 250 s which yields a thickness of ∼3.2 nm. After the thermal nitridation process, line structures are patterned either with optical or electron beam lithography. In the former case, the sample is treated in oxygen plasma for 10 min to remove residual photoresist at trench corners, leading to an improved line edge roughness. Such a ‘‘descum’’ process is then followed by a subsequent baking step at 150 ° to induce reflow of photoresist. It can be seen in Appendix VII that a combination of both processes exhibits a substantial improvement in line edge roughness at the cost of certain loss in dimension control, i.e., the width of the line structure increases. In the latter case, electron beam lithography is used to pattern submicron structures using PMMA resist. A short treatment in oxygen plasma for 30 s is used to improve the line edge roughness. After patterning of resist mask, the uncovered silicon nitride layer is selectively etched away using CHF_3/O_2 plasma. Afterwards, the samples are treated in oxygen plasma to remove the resist layer.

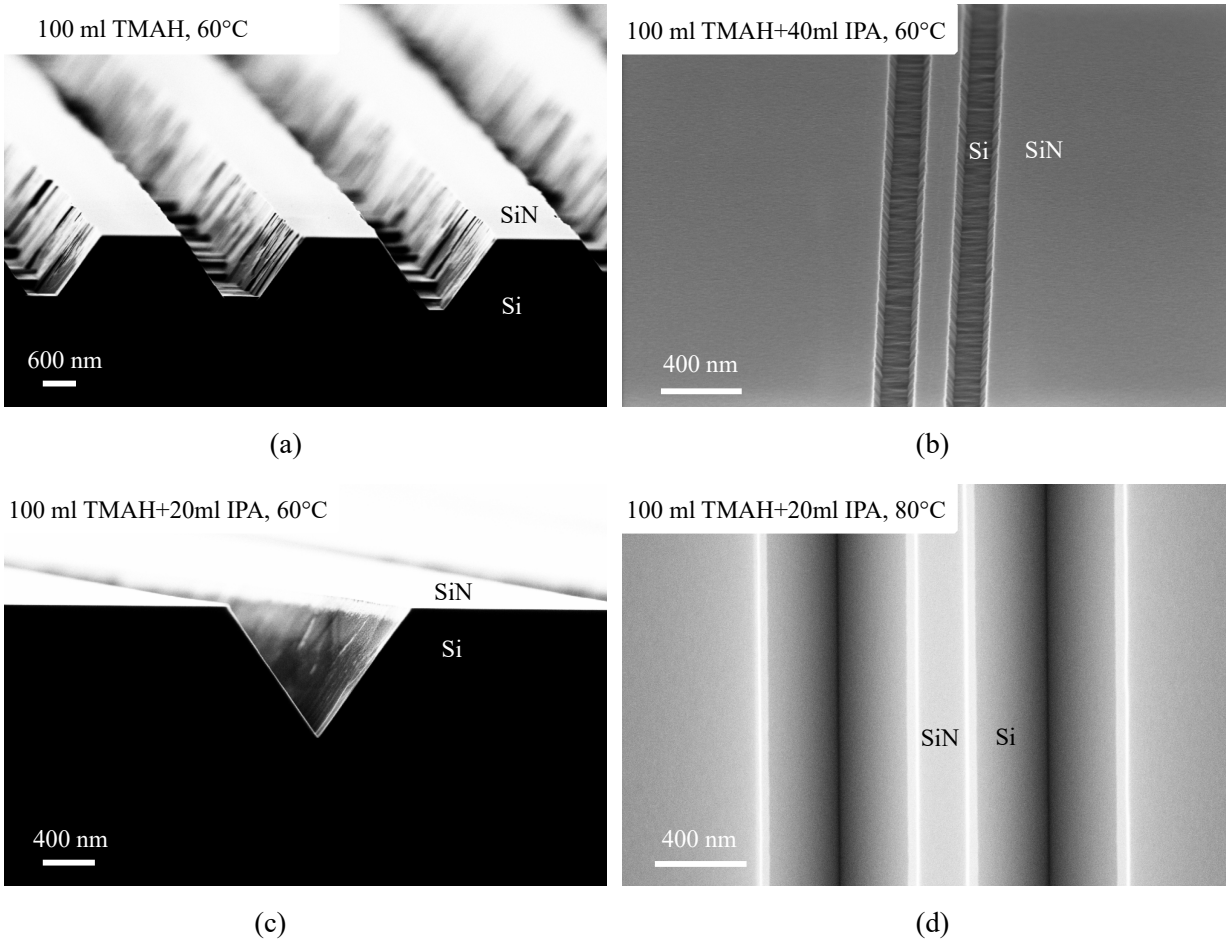


Figure 3.6: Cross-sectional scanning electron microscopy images of V-groove structures etched under various conditions. Etched in 100 ml 25 % TMAH at 60 °C (a), in a mixture of 100 ml 25 % TMAH and 40 ml IPA at 60 °C (b), in a mixture of 100 ml 25 % TMAH and 20 ml IPA at 60 °C (c), and in a mixture of 100 ml 25 % TMAH and 20 ml IPA at 80 °C (d).

Immediately prior to TMAH etching, the sample is treated in a hydrofluoric acid solution to remove the native oxide layer, which is extremely important as the oxide layer is hardly attacked by TMAH. Fig. 3.6 shows cross-sectional scanning electron micrographs of the V-groove structures after etching under various conditions. It is clear that an appropriate amount of IPA additive significantly improves the roughness of the etched {111} facets (compare (a), (b) and (c)). Furthermore, etching at a higher temperature of 80 °C leads to further improvement in surface roughness as depicted in Fig. 3.6(d).

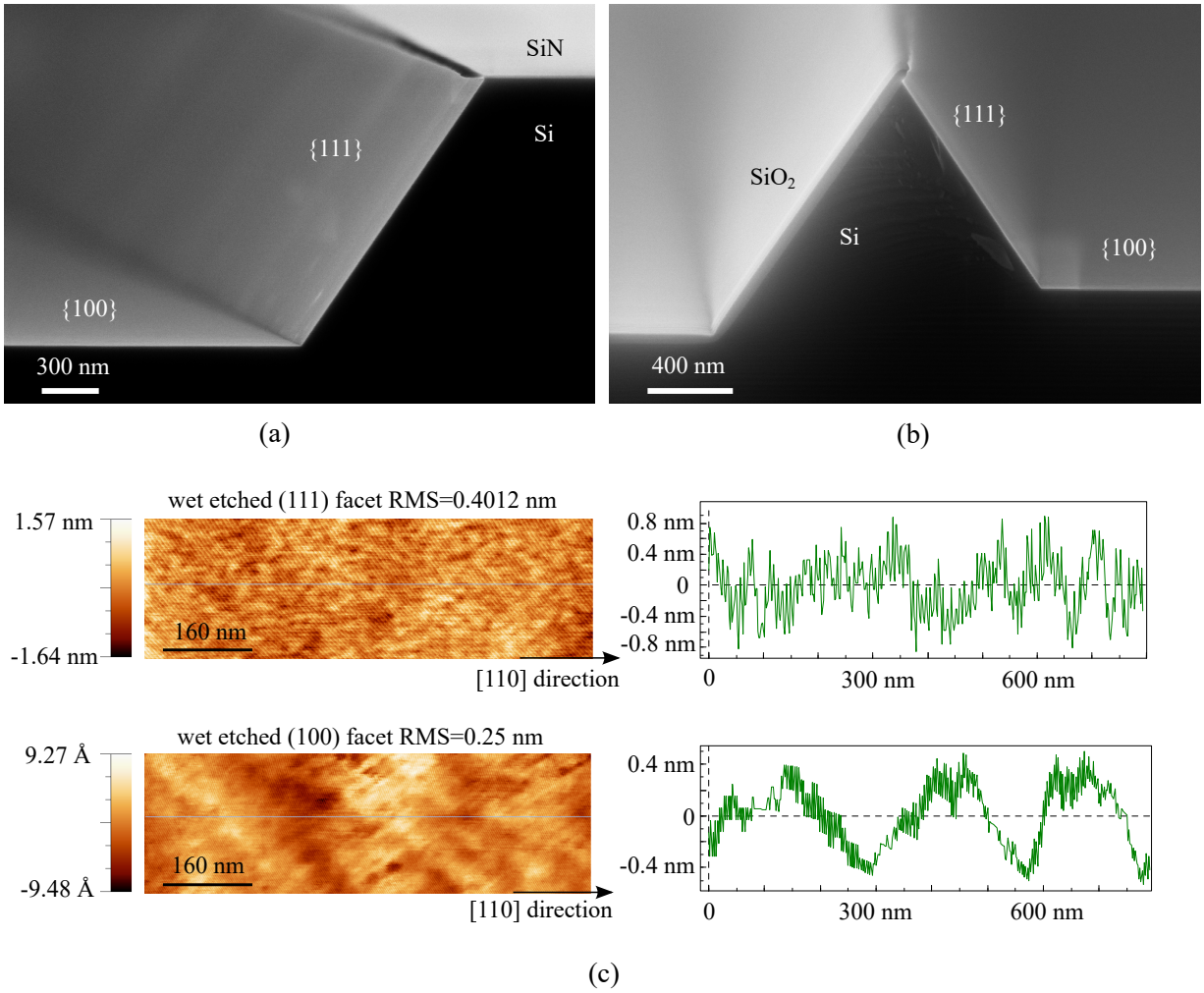


Figure 3.7: Anisotropic etching of a line structure in TMAH reveals a step formed by two {100} planes and a {111} plane (a). A triangle is formed after local oxidation of the the etched {111} facet followed with a second TMAH etching step (b). Atomic force microscopy is used to probe the surface roughness of the wet etched {111} and {100} planes.

In order to obtain a quantitative measure of the surface roughness of the wet-etched {111} facets, atomic force microscopy (AFM) is used. The measurement is performed on a large step structure as depicted in Fig. 3.7(a). A silicon cantilever (nominal tip radius = 10 nm,

cone angle = 40 °) is used to profile the tapered {111} surface in tapping mode (resonance frequency = 325 kHz, spring constant = 40 N/m). The tip axis is tilted by 15 ° with respect to the substrate normal in order to facilitate the imaging of the {111} facet. Fig. 3.7(c) shows AFM images and line-cuts of the wet etched {111} facet and the bottom {100} surface in a scanning area of 800 nm×250 nm. It is clear that the measured root-mean-square value for both the {111} and {100} facets ($RMS_{\{111\}}$=0.4012 nm, $RMS_{\{100\}}$=0.25 nm) are well within the range of a commercial prime-grade silicon wafer (RMS = 0.2-0.8 nm) [64].

After the formation of the step structure, a triangle can be formed by local oxidation of the wet etched surfaces followed with the removal of Si_3N_4 hardmask and a second TMAH etching step as depicted in Fig. 3.7(b). Here, distinct material selectivity of silicon dioxide and silicon nitride as well as the impermeability of Si_3N_4 to act as a diffusion barrier can be exploited to design a self-limiting process for the generation of triangular structures in silicon. It can be seen in Fig. 3.7(b) that the step height from the first and second TMAH etching are not identical. This is because a relatively high etching temperature (80 °C), which is necessary to achieve smooth etched facets, leads to a high etching rate for the {100} planes. However, if such a process is carried out on a silicon-on-insulator substrate where the buried oxide layer acts as an etch stop layer, this could lead to the generation of nanostructures beyond the capability of lithography tools and thus the size of the triangle will be predominantly determined by the thickness of the top silicon layer.

The fabrication process flow for triangular SiNWs on a silicon-on-insulator substrate mentioned above will be discussed in more detail in section 4.1 and Appendix I. In the next section, a high temperature anneal of the triangular SiNW in hydrogen ambient at a reduced pressure – the so-called hydrogen annealing process – will be introduced. The hydrogen annealing process has the potential to further improve the surface roughness of the wet-etched {111} facets and transform the cross-section of the SiNW from a triangle into a circle while maintaining its cross-sectional area. This is different than an oxidation process where the diffusion of oxygen atoms and strain at convex corners lead to a reduction in cross-sectional area and a change in oxidation behavior. Next, a simulation approach based on the level set method is employed to model such a shape transformation process.

3.2 Hydrogen Annealing

The cross-section of SiNWs fabricated with the two-step anisotropic wet etching discussed in the previous section can be transformed from triangular into circular shape with a high temperature (∼1050 °C) annealing step at a reduced pressure (∼65 mbar) in hydrogen ambient. In addtion, such a hydrogen annealing process allows for the smoothing of exposed surfaces which could allow a reduction in scattering to achieve a higher surface mobility of charge carriers [65, 66]. The mechanism of shape transformation and smoothing effect stems from surface diffusion of silicon atoms driven by a gradient in surface energy. Heated hydrogen facilitates such a migration of atoms at temperatures much lower than the melting

point of silicon [67]. Furthermore, the crystalline nature of SiNWs is maintained after the hydrogen annealing process [68, 69].

In this section, a simulation approach based on the level-set method will be presented to model the surface diffusion-assisted morphology evolution of silicon structures during hydrogen annealing. The level set method counts as one of the most effective approaches to compute motion driven by surface diffusion [70]. The study introduces a powerful tool that allows predicting the shape transformation of silicon structures without carrying out laborious and expensive processes.

3.2.1 A level-set method based simulation approach

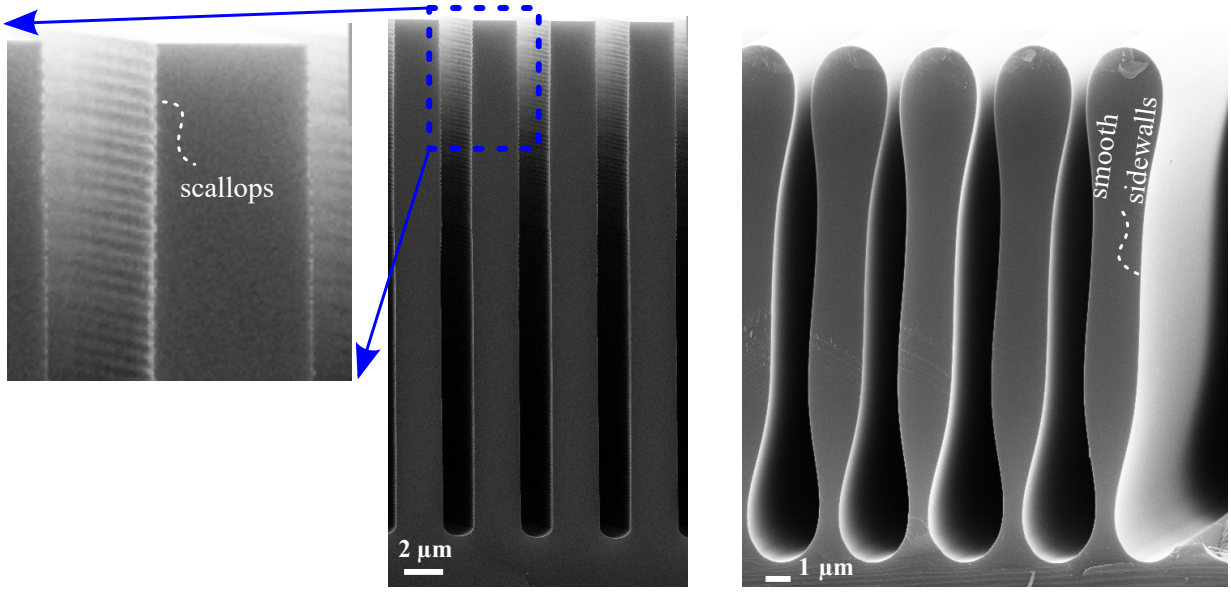


Figure 3.8: Surface smoothing and shape transformation of silicon. Grating structures etched with the Bosch™ process where the sidewall shows typical scallops (a). Annealing in hydrogen ambient at an elevated temperature of 1050 °C and a reduced pressure of 65 mbar for appoximately 550 min shows shape transformation of the initial grating structure as well as the smoothing effect of scallops (b).

Prior to a standard homoepitaxial growth process, silicon wafers are often in-situ annealed in a hydrogen ambient at a reduced pressure and high temperature to remove the wet-grown/native oxide. Such an annealing process also improves the flatness and crystal perfection of the silicon surface, thus providing an ideal seed layer for the subsequent growth of epitaxial silicon layers. The mechanism of surface flatness improvement lies in the diffusion of silicon atoms from energetically higher positions (sharp corners) to energetically

lower positions (flat areas) to obtain a favourable minimized ensemble surface energy, leading to rounded corners and eventually flattened surfaces as depicted in Fig. 3.8(b).

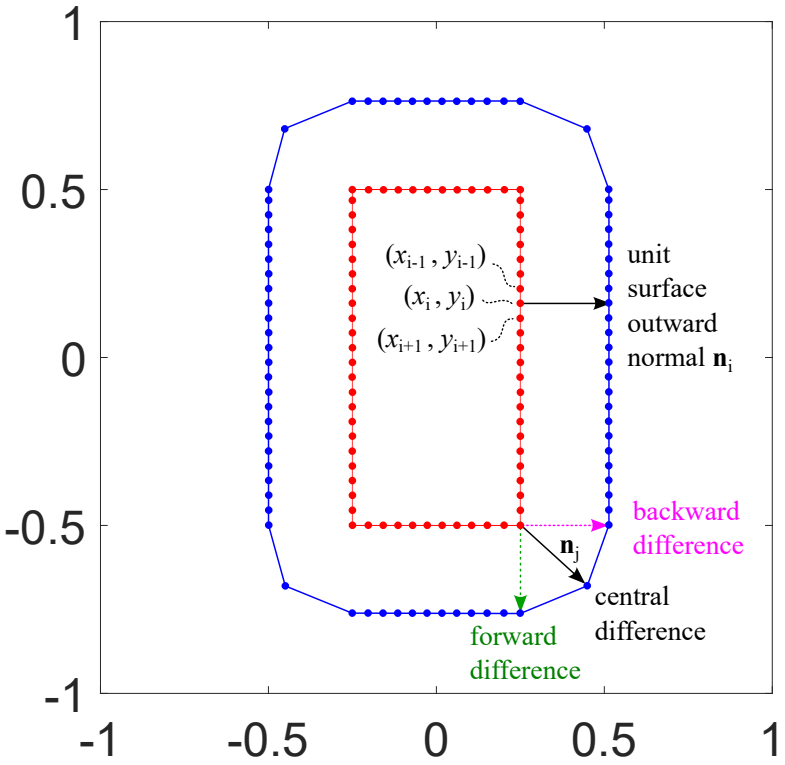


Figure 3.9: A rectangle expands with speed $V_n = 1$ along the surface outward normal $\mathbf{n}$.

Therefore, hydrogen annealing is a very useful technique and has been used as a step prior to epitaxial growth processes, for improving the surface roughness of silicon structures [71, 72], for transforming the cross-section of SiNWs from a rectangle into a circle [68], and also for MEMS applications such as pressure sensors fabricating an empty space in silicon [73]. Hence, there is the need for a simulation tool that could allow numerical modeling the outcome of the shape transformation without carrying out laborious and time-comsuming testing processes. The traditional and probabaly the most straight-forward simulation approach is to use a Lagrangian method that labels the propagating front with markers whose movement are tracked. A new propagation front is then formed by the interpolation of the markers at new positions. This could be explained with a rectangle (width $W = 0.5$, length $L = 1.0$) that is expanding with a velocity $V_n = 1$ along the surface outward normal $\mathbf{n}$ as depicted in Fig. 3.9. First, the initial rectangle (framed in red solid lines) is parameterized and markers (red solid circles) are placed along the parameterization. Next, the unit surface outward normal vector can be defined as

$$\mathbf{n}_i = (n_i^x, n_i^y) = \frac{(-y_{i+1} + y_{i-1}, x_{i+1} - x_{i-1})}{|\mathbf{r}_{i+1} - \mathbf{r}_{i-1}|}, \text{or } \mathbf{n}_i = \frac{(y_{i+1} - y_{i-1}, -x_{i+1} + x_{i-1})}{|\mathbf{r}_{i+1} - \mathbf{r}_{i-1}|} \tag{3.4}$$

depending on the position of the markers where the coordinates of the i^{th} marker point is $\mathbf{r}_{\text{i}}(t) = (x_{\text{i}}, y_{\text{i}})$. Note that a central difference is used in the calculation of the unit surface outward normal vector $\mathbf{n}_{\text{i}}$ since neither the forward nor the backward finite difference could give a wrong estimation, especially for marker points located at the corners of the rectangle. As an example, the forward finite difference method yields a unit surface normal vector pointing downwards (dashed green) whereas the vector points to the right (dashed pink) if calculated using the backward difference method.

The initial red markers shown in Fig. 3.9 are shifted to new positions (solid blue circles) after $t = 0.25$ following the evolvement rule defined by

$$\frac{d\mathbf{r}_{\text{i}}(t)}{dt} \approx \frac{\mathbf{r}_{\text{i}}(t + \Delta t) - \mathbf{r}_{\text{i}}(t)}{\Delta t} = V_{\text{n}}\mathbf{n}_{\text{i}}. \tag{3.5}$$

After the evolvement, a new interface (solid blue lines) is then formed by interpolating the blue marker points. It is clear that more marker points will lead to a more accurate new interpolated interface at the cost of longer computational time. Note that the expansion of such a rectangle under unit speed along the surface outward normal could be easily computed since the evolving interface is easily parameterized and the evolvement speed is constant. Since the marker points at the corners disperse during the evolvement, the new interface cannot be represented accurately by the limited number of marker points. On the other hand, the Lagrangian approach could run into difficulties, e.g., when the rectangle shrinks with a speed of $V_{\text{n}} = -1$ where the (j-1)$^{\text{th}}$ and (j+1)$^{\text{th}}$ marker points at the corner will evolve into the same position. In this case, a manual check of the updated marker positions becomes necessary and hence ad-hoc algorithms are needed to define the connectivity of the discretized marker points before interpolating a new interface.

Different than a Lagrangian formulation of interface evolution where evolvement is tracked by parameterized interface elements, the initial rectangle ($\partial\Omega$) shown in Fig. 3.9 can be represented as the ''zero-level set'' of a higher dimensional 3D implicit function $\phi(\mathbf{r}, t)$ without the need for parameterization as displayed in Fig. 3.10(a). A contour plot of the zero-level set in the $z = 0$ plane represents the initial rectangle (framed in red and filled in cyan) as depicted in Fig. 3.10(b).

The level set function $\phi(\mathbf{r}(t), t)$ is positive outside the rectangle, zero at the interface, and negative inside the rectangle:

- $\phi(\mathbf{r}(t), t) > 0$, outside
- $\partial\Omega = \{\mathbf{r}(t) \mid \phi(\mathbf{r}(t), t) = 0\}$, interface
- $\phi(\mathbf{r}(t), t) < 0$, inside

Such an implicit representation of interface as the isocontour of a function, which is one-dimension higher, does not require the determination of connectivity between discretized

points. Therefore, the extension from 2D to 3D is straight-forward whereas the connectivity of surface elements could become extemely complicated in a Lagrangian approach in particular for 3D cases when adjacent parts of the transforming interface start coalescing or splitting from each other. As a result, the level set method has been successfully used to model the the process of silicon reshaping [74, 75], glass reflow [76], etching [76, 77, 78], deposition and lithography development [77] in the field of semiconductor fabrication.

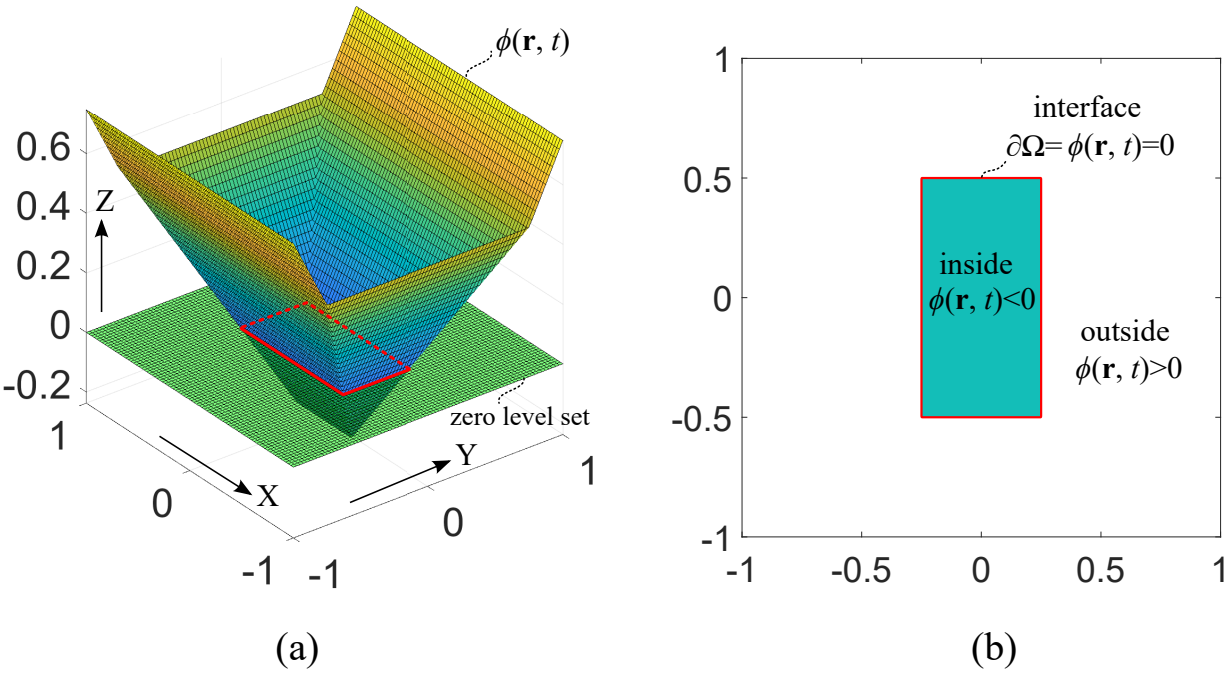


Figure 3.10: Initialization of the level set function for a 2D rectangle. The 2D rectangle (framed in solid and dashed red lines) is represented as the zero-level set of a 3D level set function (a). A contour plot of the zero-level set in the X-Y plane (b).

In a level set method, the evolvement of the interface is then tracked by the time derivative of the implicit zero-level set function. Applying the chain rule [79] to $\phi(\mathbf{r}(t), t)$ yields

$$\frac{d}{dt}\phi(\mathbf{r}(t), t) = \frac{\partial \phi}{\partial t} + \nabla\phi(\mathbf{r}(t), t)\frac{d\mathbf{r}(t)}{dt}, \tag{3.6}$$

with the surface outward normal $\mathbf{n} = \frac{\nabla\phi}{|\nabla\phi|}$ and speed $\frac{d\mathbf{r}(t)}{dt} = \mathbf{n}V_{\mathrm{n}}$. The gradient $\nabla\phi$ is perpendicular to the zero-isocontour of $\phi(\mathbf{r}(t), t)$ and it points in the direction of increasing $\phi(\mathbf{r}(t), t)$. The evolving surface remains the zero-level set of $\phi(\mathbf{r}(t), t) = 0$, hence the derivative of Eqn. (3.6) must always be zero and the level-set evolvement equation is derived as

$$\frac{d}{dt}\phi(\mathbf{r}(t), t) = \frac{\partial \phi}{\partial t} + V_{\mathrm{n}}|\nabla\phi| = 0. \tag{3.7}$$

Therefore, the initial rectangle displayed in Fig. 3.10(b) expanding at a speed of $V_{\mathrm{n}} = 1$ along the surface outward normal $\mathbf{n}$ can be described by the finite difference approximation

in time from Eqn. (3.7) as:

$$\frac{\phi(t+\Delta t)-\phi(t)}{\Delta t}+|\nabla\phi|=0. \tag{3.8}$$

The gradient of the implict function $\nabla\phi$ is defined as

$$\nabla\phi=\left(\frac{\partial\phi}{\partial x},\frac{\partial\phi}{\partial y}\right). \tag{3.9}$$

Hence, the term $|\nabla\phi|$ in Eqn. (3.8) can be written as

$$|\nabla\phi|=\sqrt{\left(\frac{\partial\phi}{\partial x}\right)^2+\left(\frac{\partial\phi}{\partial y}\right)^2}. \tag{3.10}$$

For numerical implementations, the partial derivatives in Eqn. (3.10) have to be approximated, e.g, using finite difference techniques. where Δx is a small increment step in x. As it was discussed before (cf. Fig. 3.9), neither the forward difference

$$\frac{\partial\phi}{\partial x}\approx\frac{\phi_{\mathrm{i}+1}-\phi_{\mathrm{i}}}{\Delta x} \tag{3.11}$$

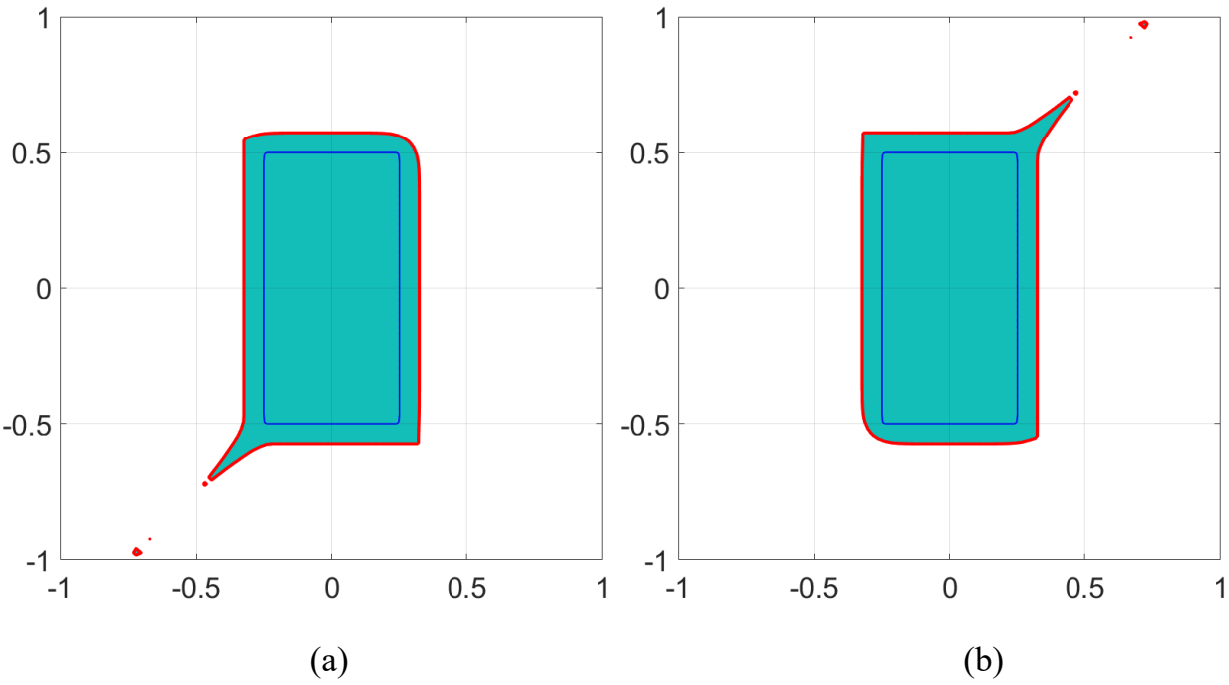


Figure 3.11: Evolvement of a rectangle expanding with speed $V_{\mathrm{n}}=1$ along the surface outward normal $\mathbf{n}$ using backward (a) and forward (b) difference approximations. The initial rectangle is framed in solid blue lines. The profile after evolvement after $t=0.15$ is filled in cyan and framed in solid red lines.

nor the backward difference

$$\frac{\partial \phi}{\partial x} \approx \frac{\phi_{\mathrm{i}} - \phi_{\mathrm{i\text{-}1}}}{\Delta x} \tag{3.12}$$

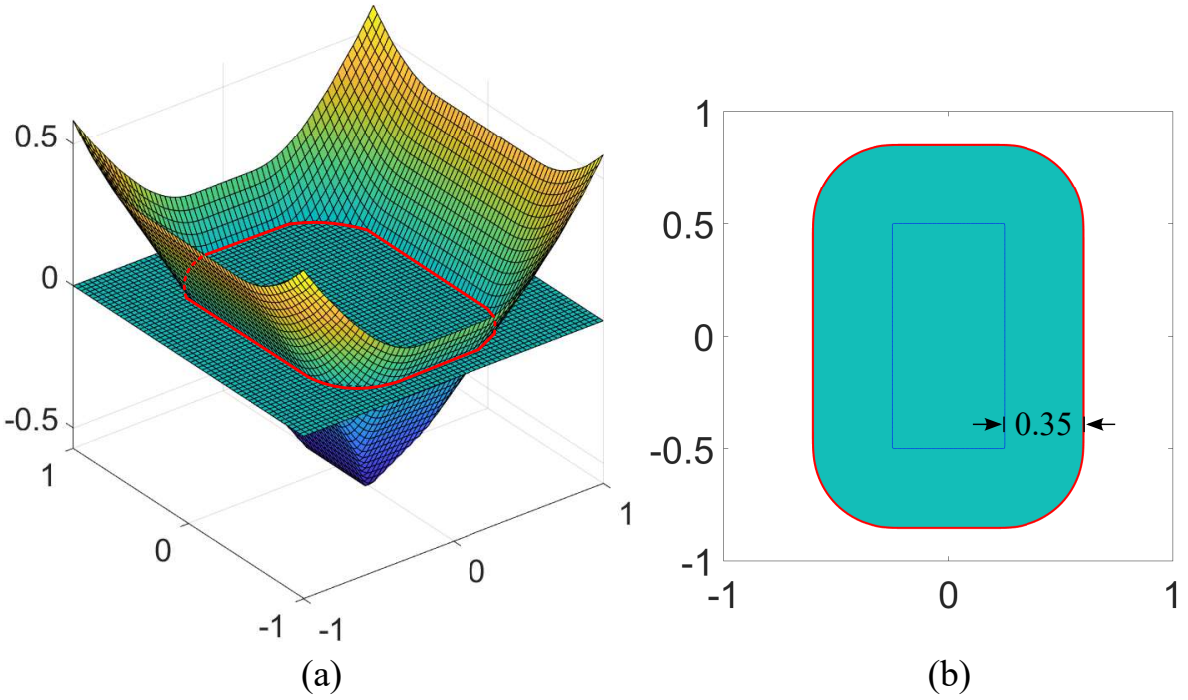


Figure 3.12: Evolution of the intial level set function after $t = 0.35\,\mathrm{s}$. The evolved rectangle is obtained by cutting the 3D level set function at $z = 0$ (a). A contour plot of the initial and the evolved rectangle (b). The initial rectangle is framed in solid blue lines. The profile after evolvement after $t = 0.15$ is filled in cyan and framed in solid/dashed red lines.

gives an accurate appoximation in particular for data points at corner positions as depicted in the evolvement result shown in Fig. 3.11. Therefore, a central difference which can be understood as the average of forward and backward difference is used for the calculation of $\frac{\partial \phi}{\partial x}$:

$$\frac{\partial \phi}{\partial x} \approx \frac{\frac{\phi_{\mathrm{i+1}} - \phi_{\mathrm{i}}}{\Delta x} + \frac{\phi_{\mathrm{i}} - \phi_{\mathrm{i\text{-}1}}}{\Delta x}}{2} = \frac{\phi_{\mathrm{i+1}} - \phi_{\mathrm{i\text{-}1}}}{2\Delta x}. \tag{3.13}$$

Figure 3.12(b) shows the evolution of the initial rectangle (solid blue lines) after $t = 0.35\,\mathrm{s}$

(solid/dashed red lines) using central difference approximations. A 3D plot of the evolved level set function after $t = 0.35$ is displayed in Fig. 3.12(a) where the evolved rectangle is obtained from the $\phi(\mathbf{r}(t), t)|_{t=0.35} = 0$ isocontour.

It is important to note that the initial implicit function can be realized with signed distance functions. A signed distance function is a subset of implicit function $\phi(\mathbf{r}(t), t)$ that $|\phi(\mathbf{r}(t), t)| = d(\mathbf{r}(t), t)$ for all $\mathbf{r}$(t), where $d(\mathbf{r}(t), t)$ is a distance function defined as

$$d(\mathbf{r}(t), t) = \min\left(|\mathbf{r}(t) - \mathbf{r}_{\mathrm{I}}(t)|\right), \quad \text{for all } \mathbf{r}_{\mathrm{I}}(t) \in \partial\Omega. \tag{3.14}$$

Similar to the property of implicit functions mentioned before, a signed distance function is positive in the exterior part, negative in the interior part, and zero at the interface:

- $\phi(\mathbf{r}(t), t) = d(\mathbf{r}(t), t)$, outside
- $\phi(\mathbf{r}(t), t) = 0$, interface
- $\phi(\mathbf{r}(t), t) = -d(\mathbf{r}(t), t)$, inside

An important property of a signed distance function is

$$|\nabla\phi| = 1. \tag{3.15}$$

Therefore, the evolvement equation for a rectangle expanding at speed $V_{\mathrm{n}} = 1$ depicted in Eqn. (3.8) can be reduced to

$$\frac{\phi(t + \Delta t) - \phi(t)}{\Delta t} + 1 = 0. \tag{3.16}$$

The major advantage of using a signed distance function is that they are monotonic across the interface ($\partial\Omega$) and hence can be differentiated at the zero-level set with significantly higher confidence than other implict functions [80]. Furthermore, computational cost can be reduced without the need for calculating $|\nabla\phi|$ at every cycle. However, the initial signed distance function property is not preserved during evolution, hence the level set function has to be regularly reinitialized [80].

3.2.2 Evaporation & condensation and surface diffusion

In the previous part, a simple example of an expanding rectangle is presented to compare the Lagrangian (i.e., the marker tracking method) and the Eulerian (i.e., the level set method) approaches of tracking morphological evolution. It has been demonstrated that the embedment of a 2D interface as the ‘‘zero-level set’’ of a higher dimensional 3D implicit function could track shape transformation without the need for parameterization at a cost of higher computational time. In addition, the level set method has the inherent ability to track a propagating front under coalescence or splitting where the connectivity of discretized

points does not have to be specified separately. Next, such an Eulerian approach will be employed to track the topological evolution of silicon structures during hydrogen annealing. In this case, the migration speed V_n along the surface outward normal $\mathbf{n}$ is defined either by the mean curvature κ or surface Laplacian of the mean curvature $\Delta_\mathrm{s}\kappa$ depending on different annealing conditions.

In a hydrogen annealing process, silicon atoms at sharp corners possess a higher surface energy as a result of a larger curvature value. They tend to diffuse into positions where the surface gradient of the curvature is constant (e.g., a sphere) and thus achieving a minimum ensemble energy. It has been reported that evaporation of silicon atoms at the surface becomes significant when the annealing temperature exceeds 1100 °C [81]. In this case, the mass transport under evaporation & condensation is described by V_n along the surface outward normal $\mathbf{n}$ as

$$V_\mathrm{n}^\mathrm{ec} = \theta_0 \Omega \left[1 - \exp\left(\frac{\gamma\Omega}{k_\mathrm{B}T}\kappa\right)\right], \tag{3.17}$$

where Ω is the atomic volume, γ is the surface-free energy per unit area, k_B is the Boltzmann constant, κ is the mean curvature of an implicit function ϕ, and θ_0 is defined by

$$\theta_0 = \frac{p_0}{\sqrt{2\pi m k_\mathrm{B} T}}, \tag{3.18}$$

where m is the mass of a silicon atom, p_0 is the equilibrium vapor pressure of a flat surface ($\kappa = 0$). The exponential term in Eqn. (3.17) can be expanded using the Taylor series as

$$V_\mathrm{n}^\mathrm{ec} = -\theta_0 \Omega \sum_{n=1}^{\infty} \frac{1}{n!} \left(\frac{\gamma\Omega}{k_\mathrm{B}T}\kappa\right)^n. \tag{3.19}$$

According to Ref. [82], $\dfrac{\gamma\Omega\kappa}{k_\mathrm{B}T} \ll 1$. Therefore, Eqn. (3.19) can be approximated by leaving out the high-order polynomials as

$$V_\mathrm{n}^\mathrm{ec} = -\frac{\theta_0\gamma\Omega^2}{k_\mathrm{B}T}\kappa = -A\kappa, \tag{3.20}$$

where $A = \dfrac{p_0\gamma\Omega^2}{(2\pi m)^{\frac{1}{2}}\,(k_\mathrm{B}T)^{\frac{3}{2}}}$. By inserting Eqn. (3.20) into Eqn. (3.7), the level set equation for mean curvature flow is derived as

$$\frac{\partial\phi}{\partial t} - A\kappa|\nabla\phi| = 0. \tag{3.21}$$

For simulation purposes, it is reasonable to assume $A = 1$. Note that Eqn. (3.21) is analogous to $\frac{\partial\phi}{\partial t} = \frac{\partial^2\phi}{\partial x^2}$; A stability condition $\Delta t < \Delta x^2$ is required for numerical implementation if explicit methods are used [83].

The mean curvature of an implicit function ϕ is defined as the gradient of the unit surface outward normal [80]:

$$\kappa = \nabla \cdot \left(\frac{\nabla \phi}{|\nabla \phi|} \right), \tag{3.22}$$

$$\kappa_{3D} = \frac{\phi_x^2 \phi_{yy} - 2\phi_x \phi_y \phi_{xy} + \phi_y^2 \phi_{xx} + \phi_x^2 \phi_{zz} - 2\phi_x \phi_z \phi_{xz} + \phi_z^2 \phi_{xx} + \phi_y^2 \phi_{zz} - 2\phi_y \phi_z \phi_{yz} + \phi_z^2 \phi_{yy}}{\left(\phi_x^2 + \phi_y^2 + \phi_z^2\right)^{3/2}}. \tag{3.23}$$

Eqn. (3.23) shows the mean curvature of a grid point on a 3D surface. The partial differences ϕ_x, ϕ_{xx} and ϕ_{xy} are discretized in a uniform Cartesian grid as central differences [80], namely

$$\phi_x = \frac{\partial \phi}{\partial x} \approx \frac{\phi_{i+1,\,j,\,k} - \phi_{i-1,\,j,\,k}}{2\Delta x}, \tag{3.24}$$

$$\phi_{xx} = \frac{\partial^2 \phi}{\partial x^2} \approx \frac{\phi_{i+1,\,j,\,k} - 2\phi_{i,\,j,\,k} + \phi_{i-1,\,j,\,k}}{\Delta x^2}, \tag{3.25}$$

$$\phi_{xy} = \frac{\partial^2 \phi}{\partial x \partial y} \approx \frac{\phi_{i-1,\,j-1,\,k} + \phi_{i+1,\,j+1,\,k} - \phi_{i-1,\,j+1,\,k} - \phi_{i+1,\,j-1,\,k}}{4\Delta x \Delta y}. \tag{3.26}$$

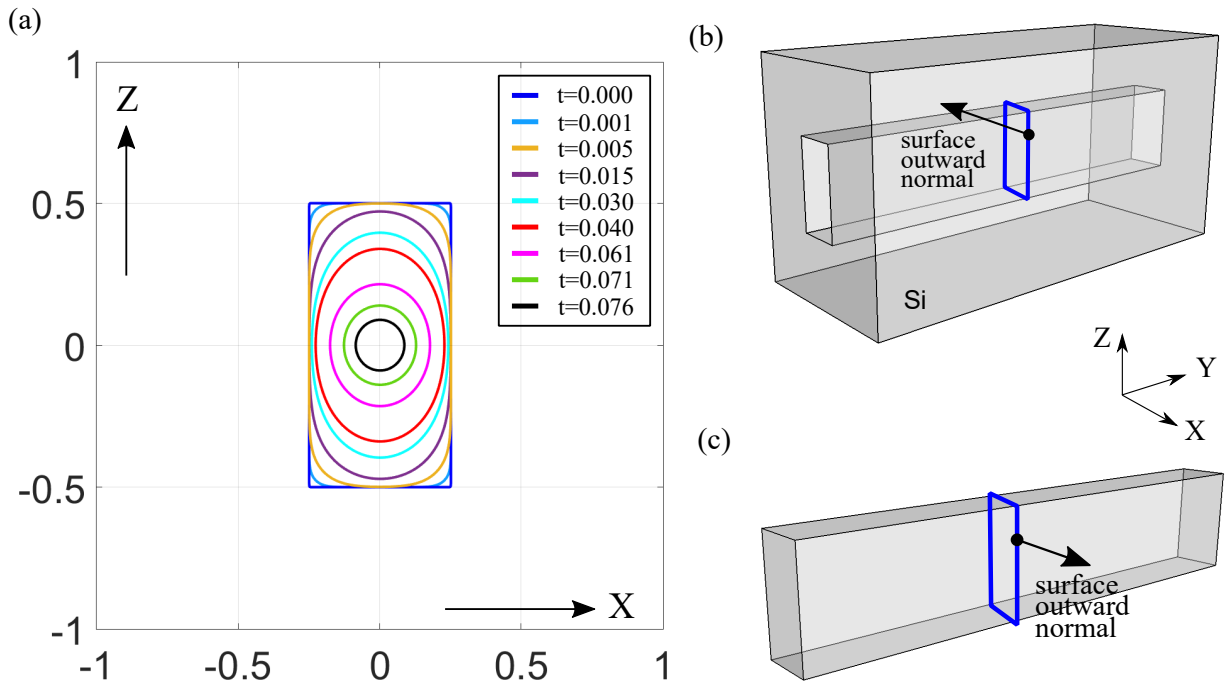
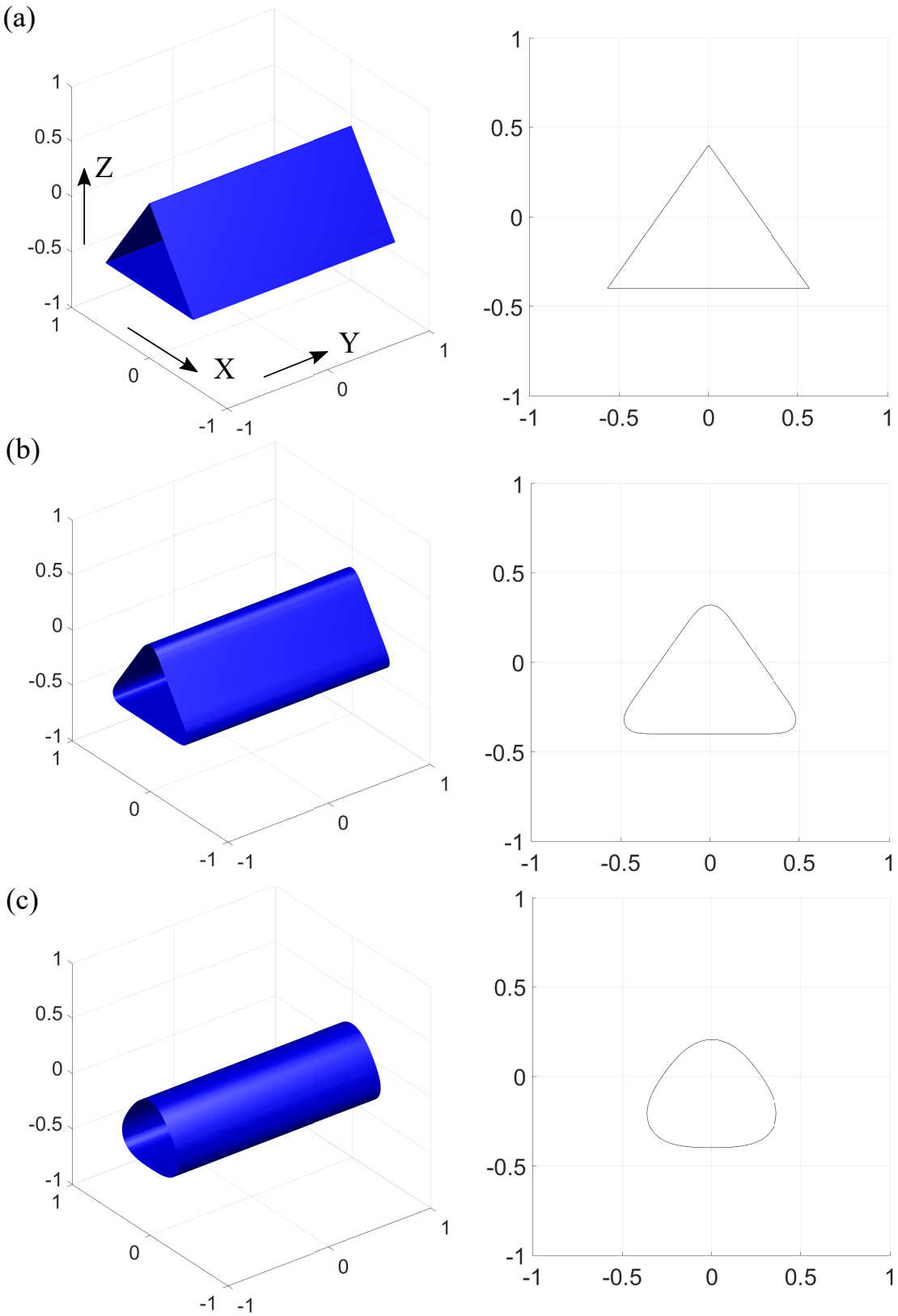


Figure 3.13: Evolution of a 2D rectangle under mean curvature flow. The corners become rounded and the rectangle shrinks into a small circle over time (a). The 2D rectangle represents either the cross-section of a deep rectangular hole (b) or a long solid rod with rectangular cross-section (c).


(a)
Z
X
Y
(b)
(c)

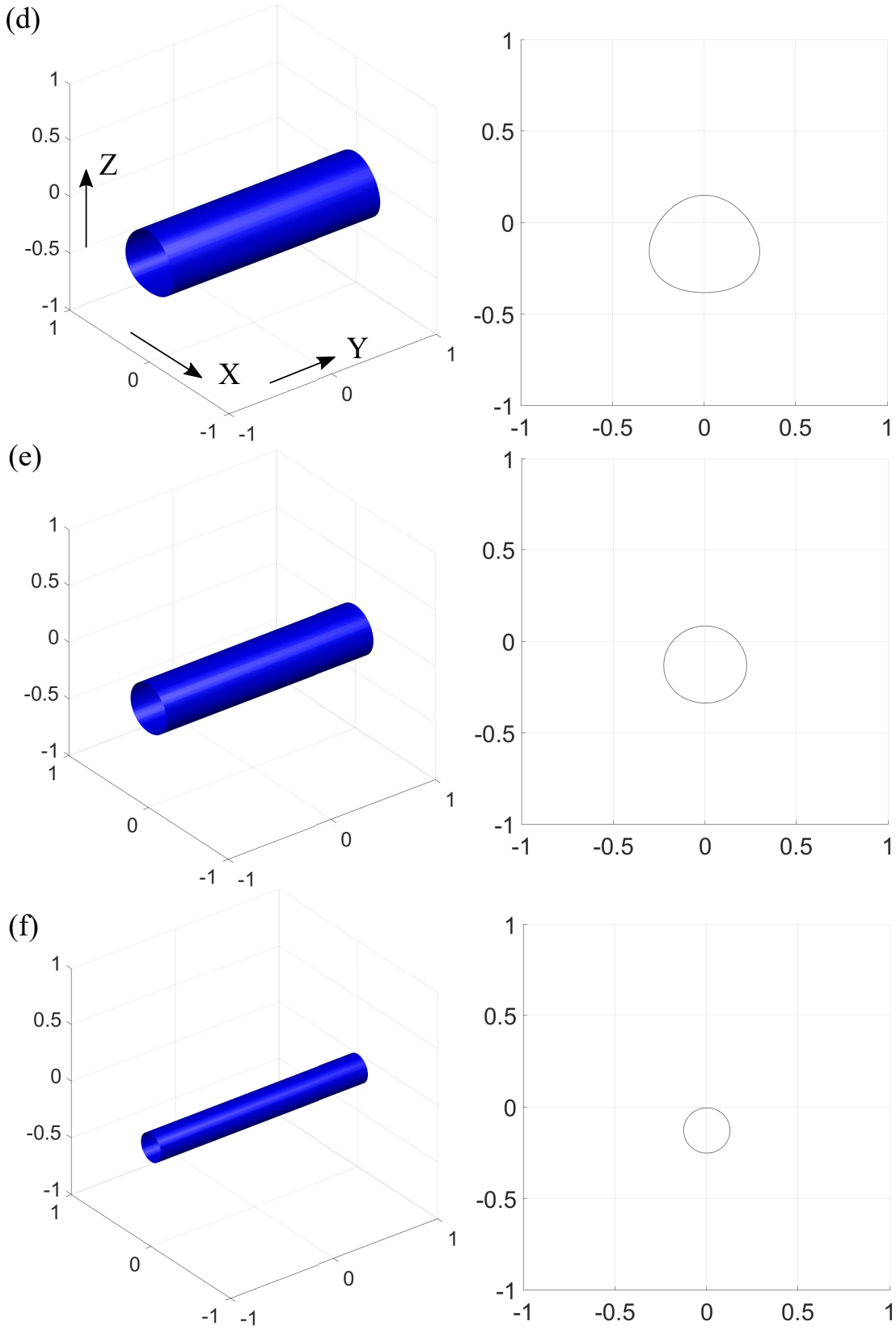


Figure 3.14: Evolution of a 3D rod with triangular cross-section under mean curvature flow. A cross-section of the 3D object at $y = 0$ is shown in the right panels.

Figure 3.13 shows the evolution of the same rectangle (width $W = 0.5$, length $L = 1$) under evaporation & condensation (i.e., mean curvature flow) over time. The 2D rectangle can be regarded as the cross-section of a deep rectangular hole or a long solid rod with rectangular cross-section. It can be seen that the mean curvature flow does not preserve the cross-sectional area during evolution and the initial rectangle gradually shrinks into a small circle.

Figure 3.14 shows the evolution of a 3D rod with triangular cross-section under mean curvature flow. Similar to the 2D rectangle example shown above, the evaporation & condensation shows a rounding effect of sharp corners and transforms the cross-section from a triangle into a circle with reduced cross-sectional area. Therefore, hydrogen annealing at a temperature $T > 1100\,^{\circ}\mathrm{C}$ could be employed to reduce the diameter of a SiNW and achieve a circular cross-section.

On the other hand, mass transport is dominated by surface diffusion if the annealing temperature is blow 1100 °C. The migration speed of silicon atoms along the surface outward normal is then described by the Mullins-Herring surface diffusion model [82]:

$$V_{\mathrm{n}}^{\mathrm{sd}} = \frac{D_{\mathrm{s}}\gamma\Omega^2\nu}{kT}\nabla_{\mathrm{s}}^2\kappa = B\nabla_{\mathrm{s}}^2\kappa, \tag{3.27}$$

where D_{s} is the surface diffusion constant, and ν is the number of atoms per unit area. The surface Laplacian of the mean curvature is denoted as $\nabla_{\mathrm{s}}^2\kappa$.

By inserting Eqn. (3.27) into Eqn. (3.7), the level set equation for motion by the surface Laplacian of the mean curvature is then derived as

$$\frac{\partial\phi}{\partial t} + B\Delta_{\mathrm{s}}\kappa|\nabla\phi| = 0. \tag{3.28}$$

For simulation purposes, it is reasonable to assume $B = 1$. Note that Eqn. (3.28) is analogous to $\frac{\partial\phi}{\partial t} = -\frac{\partial^4\phi}{\partial x^4}$; A stability condition $\Delta t < \Delta x^4$ is required for numerical implementation if explicit methods are used. Smereka [83] has derived the surface Laplacian of the mean curvature for the 2D case. Based on his method, the surface gradient of mean curvature κ can be written as:

$$\nabla_{\mathrm{s}}\kappa = \nabla\kappa - \mathbf{n}\partial_{\mathrm{n}}\kappa, \tag{3.29}$$

where for a 3D case $\partial_{\mathrm{n}}\kappa = n^{\mathrm{x}}\kappa_{\mathrm{x}} + n^{\mathrm{y}}\kappa_{\mathrm{y}} + n^{\mathrm{z}}\kappa_{\mathrm{z}}$. Note that n^{x} is the x-component of the normal vector $\mathbf{n}$ which can be written as:

$$n^{\mathrm{x}} = \frac{\phi_{\mathrm{x}}}{\sqrt{\phi_{\mathrm{x}}^2 + \phi_{\mathrm{y}}^2 + \phi_{\mathrm{z}}^2}}. \tag{3.30}$$

With the derived normal gradient of the mean curvature $\partial_{\mathrm{n}}\kappa$, the surface gradient of κ is then:

$$\nabla_{\mathrm{s}}\kappa = \kappa_{\mathrm{x}}\mathbf{x} + \kappa_{\mathrm{y}}\mathbf{y} + \kappa_{\mathrm{z}}\mathbf{z} - \left(n^{\mathrm{x}}\kappa_{\mathrm{x}} + n^{\mathrm{y}}\kappa_{\mathrm{y}} + n^{\mathrm{z}}\kappa_{\mathrm{z}}\right)\left(n^{\mathrm{x}}\mathbf{x}\right.$$

$$+n^{\mathrm{y}}\mathbf{y}+n^{z}\mathbf{z})=A\mathbf{x}+B\mathbf{y}+C\mathbf{z}, \tag{3.31}$$

where $\mathbf{x}$ is the unit vector in the x direction. Surface Laplacian of the mean curvature is then calculated as the following:

$$\begin{aligned}\Delta_{\mathrm{s}}\kappa=\nabla_{\mathrm{s}}\cdot\nabla_{\mathrm{s}}\kappa=(\nabla-\mathbf{n}\partial_{\mathrm{n}})\cdot(A\mathbf{x}+B\mathbf{y}+C\mathbf{z})=A_{\mathrm{x}}+B_{\mathrm{y}}+C_{\mathrm{z}}\\ -n^{\mathrm{x}}\left(n^{\mathrm{x}}A_{\mathrm{x}}+n^{\mathrm{y}}A_{\mathrm{y}}+n^{\mathrm{z}}A_{\mathrm{z}}\right)-n^{\mathrm{y}}\left(n^{\mathrm{x}}B_{\mathrm{x}}+n^{\mathrm{y}}B_{\mathrm{y}}+n^{\mathrm{z}}B_{\mathrm{z}}\right)\\ -n^{\mathrm{z}}\left(n^{\mathrm{x}}C_{\mathrm{x}}+n^{\mathrm{y}}C_{\mathrm{y}}+n^{\mathrm{z}}C_{\mathrm{z}}\right).\end{aligned} \tag{3.32}$$

Problems on numerically solving non-linear fourth-order partial differential equations are known to be very stiff. Stability is a big issue even though the level set method counts as one of the most effective approaches to compute motion by surface Laplacian of the mean curvature [79]. In this thesis, an explicit method is used to numerically solve the level set equation (3.28). Strategies used to improve the stability include:

- choosing a small time step ($\Delta t \ll \Delta x^4$),
- adding a small value of ε to the denominator in Eqn. (3.23) and Eqn. (3.30) which then becomes $\sqrt{\phi_{\mathrm{x}}^2+\phi_{\mathrm{y}}^2+\phi_{\mathrm{z}}^2+\varepsilon}$ allows smoothing the singularities caused by infinite mean curvature values,
- reinitialization of the level set function frequently to keep ϕ approximately equal to signed distance (chapter 7 of Ref. [80]).

In the present thesis, an algorithm using an explicit method is empolyed which is listed as follows:

1. grid discretization, choice of simulation time t_{tot} and time step Δt
2. initialization of the level-set function $\phi(\mathbf{r},t)$ as a signed distance function, set up periodic boundary conditions
3. compute the surface outward normal $\mathbf{n}$, surface gradient $\nabla\phi(t)$, mean curvature $\kappa(t)$ and surface Laplacian of the mean curvature $\Delta_{\mathrm{s}}\kappa(t)$ at time t
4. update ϕ with the third-order TVD Runge-Kutta scheme [84] (see Appendix IV) and re-initialize ϕ as a signed distance function every 10 iterations
5. update t and go to step 3 if $t < t_{\mathrm{tot}}$

Figure 3.15 shows simulation and experimental results of the smoothing effect in the inital phase of shape transformation. The level set method allows simulating arbitrarily shaped profiles including the initial smoothing effect of scallops generated from the iterative isotropic etching and passivation steps of the Bosch™ process as depicted in Fig. 3.15(b). Sidewall becomes smooth after a short annealing process as displayed in Fig. 3.15(c).

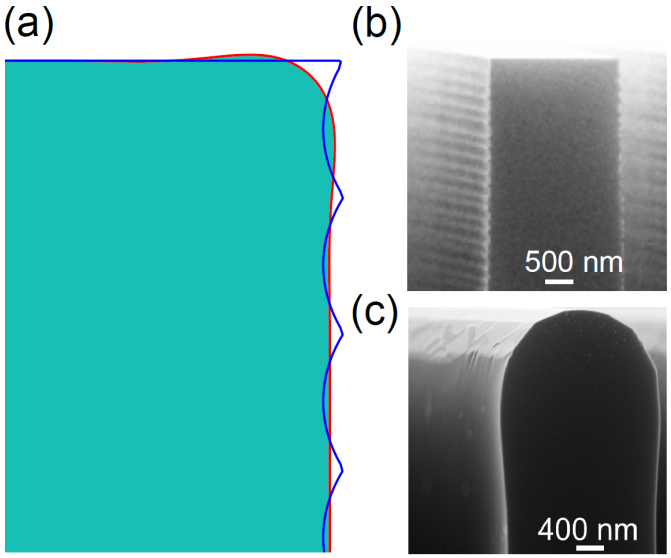


Figure 3.15: Simulation of the initial phase of hydrogen annealing showing the smoothing effect of scallops (b). Part of a silicon grating structure etched by the Bosch™ process with typical scallops on the sidewalls. Sidewall becomes smooth after a short hydrogen annealing process (c).

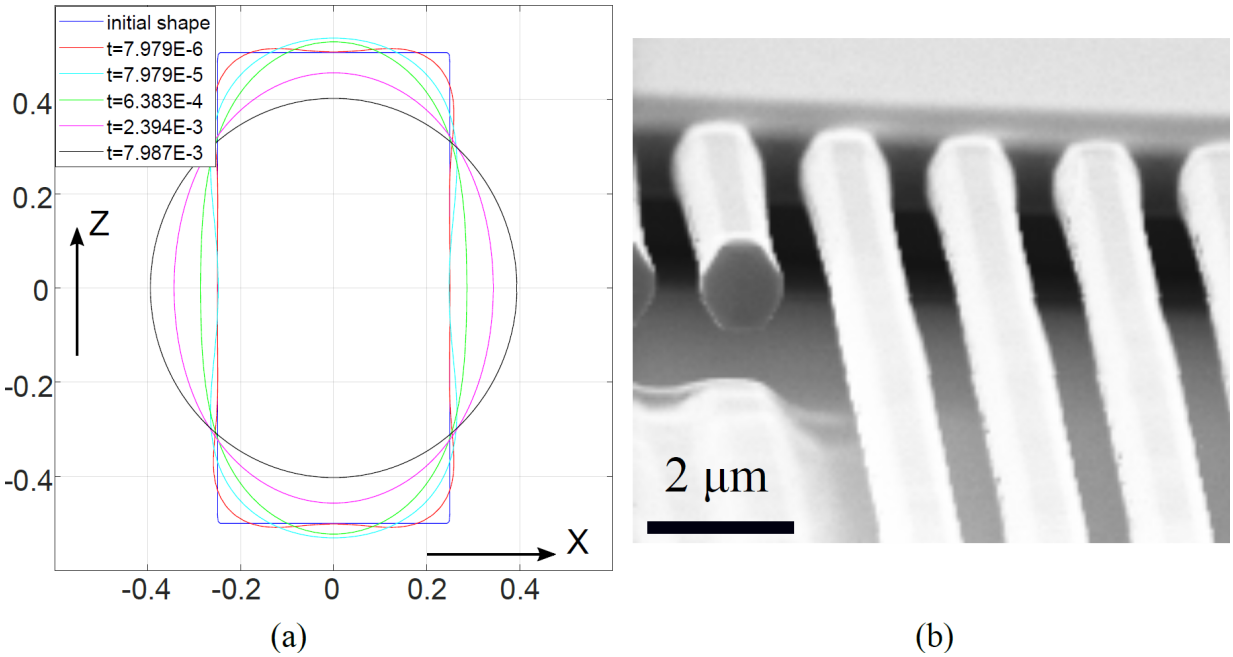
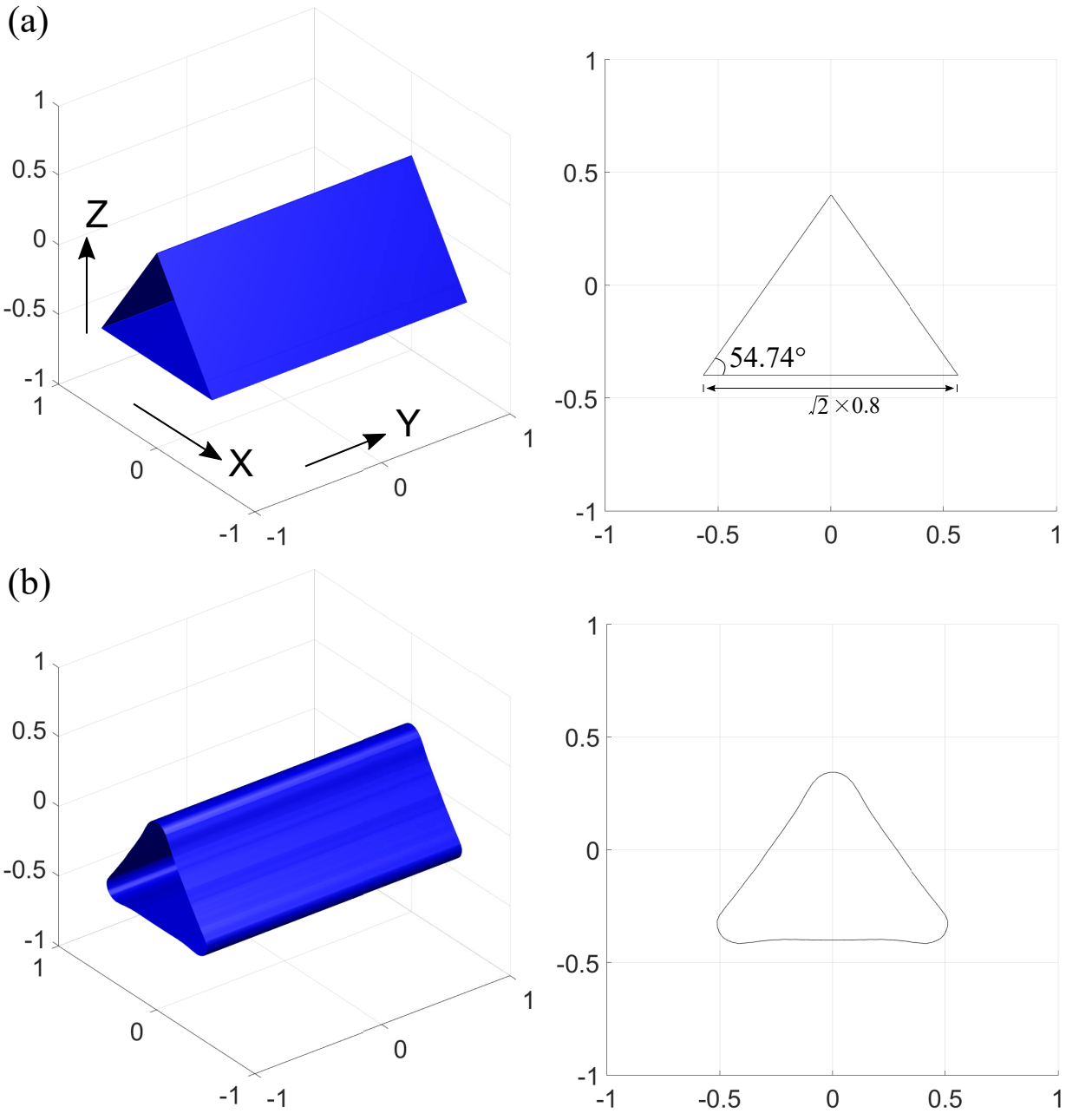


Figure 3.16: Evolution of a 2D rectangle under surface diffusion. The corners are rounded and the rectangle transforms into a circle while preserving its cross-sectional area over time (a). An experimental annealing result of rectangular rods etched on a silicon-on-insulator substrate reveals elliptical cross-section after the hydrogen annealing process.

Figure 3.16 shows simulation and experimental results of shape evolution of the same rectangle (width $W = 0.5$, length $L = 1$) under surface diffusion (i.e., surface Laplacian of the mean curvature) over time. It is clear that topological evolution mediated by surface diffusion rounds off sharp corners in the early stage and transforms the rectangle into a circle while preserving its cross-sectional area.



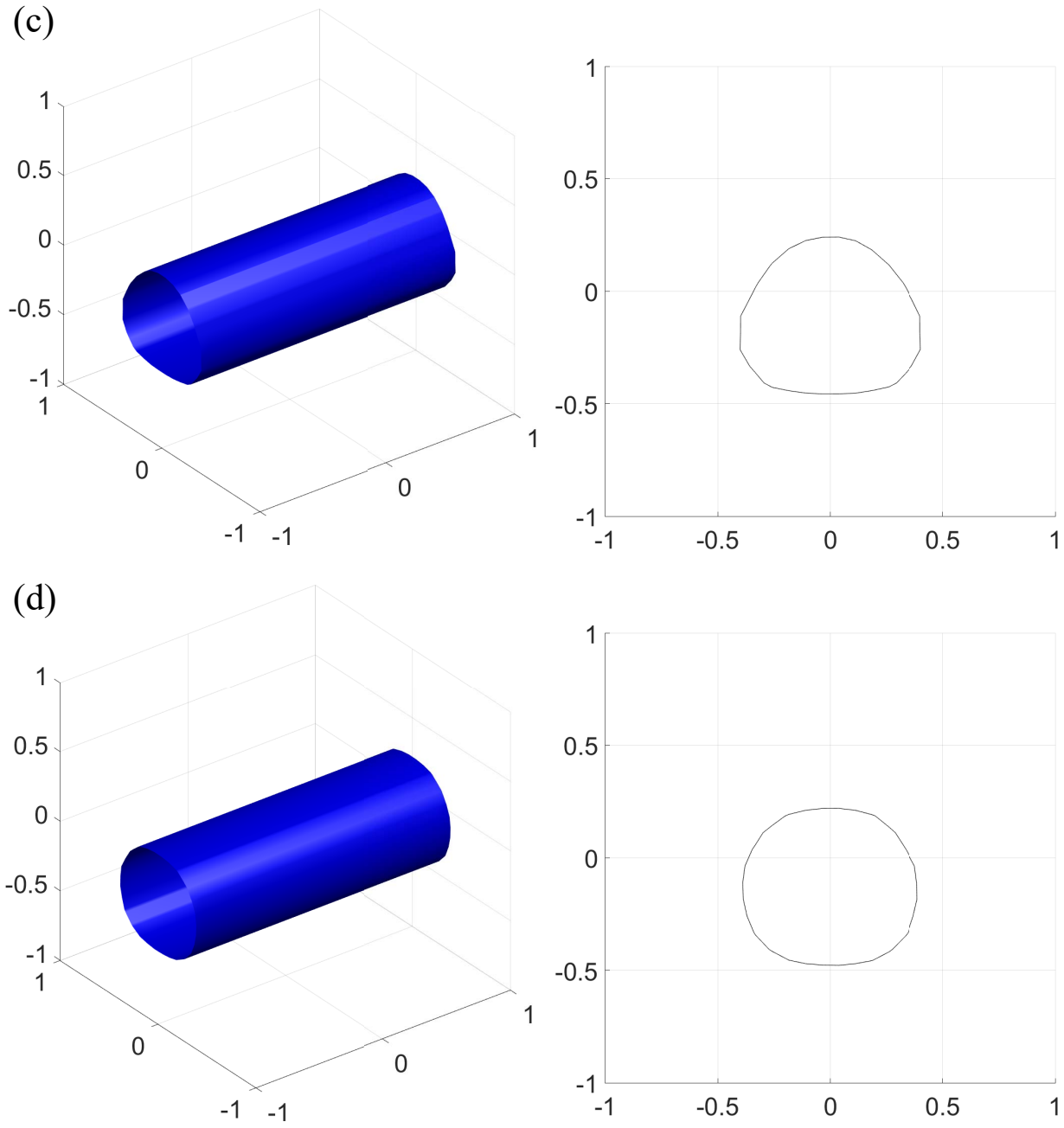


Figure 3.17: Evolution of a 3D rod with triangular cross-section under surface diffusion. A cross-section of the 3D object at $y = 0$ is shown in the right panels. The corners are rounded in the initial phase and the triangle eventually transforms into a circle with a radius of approximately 0.38 upon reaching equilibrium.

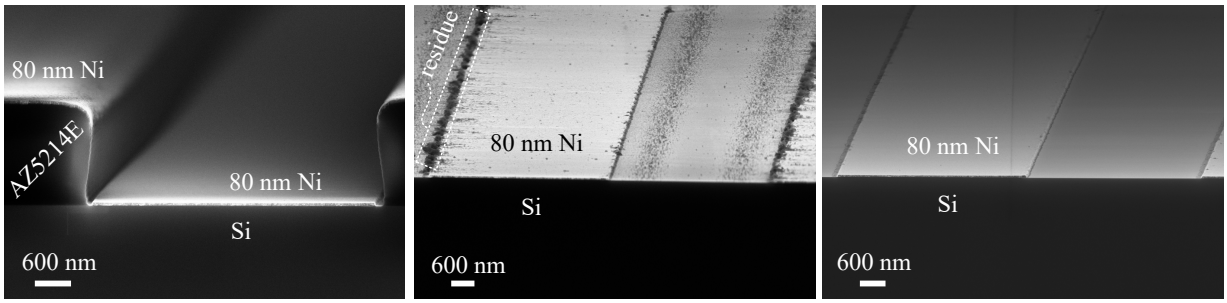
Figure 3.17 shows the shape evolution of a 3D rod with triangular cross-section driven by surface diffusion. It is clear that the topological evolution mediated by surface diffusion rounds off sharp corners of the triangle at the early stage and transforms the triangle into a circle while preserving the cross-sectional area upon reaching equilibrium.

As a short conclusion, the hydrogen annealing process is a very useful technique that can be used to improve the surface roughness and transform the shape of silicon structures. Annealing at a temperature higher than 1100 °C allows transforming the cross-sectional shape of a SiNW from a triangle into a circle while thinning down its cross-sectional size. The shape transformation becomes predominantly driven by surface diffusion at an annealing temperature below 1050 °C, yielding SiNWs with circular cross-sections while maintaining its area.

In the next section, a lift-off process utilizing e-beam evaporation in combination with a bilayer PMMA resist will be employed to create source/drain and gate electrodes on the fabricated SiNWs. The electron beam evaporation setup is modifed in a way that can avoid electron and ion bombardment on PMMA resist during the evaporation process, leading to a significant improvement in fabrication yield and device performance.

3.3 An Improved Electron Beam Evaporation Process

In this section, a modified electron beam evaporation chamber equipped with two passive measures − an appropriate magnetic field of two permanent magnets together with a self-charging, hollow cylindrical electrode − is presented to get rid of blistering and cracking of the deposited layer on a bilayer PMMA resist.



(a) (b) (c)

Figure 3.18: A nickel lift-off process with the unmodified evaporation setup and image-reversal photoresist AZ5214E™. Approximately 80 nm of nickel evaporated on a resist mask with inwardly tapered sidewalls (a). Incomplete resist removal after immersion in DMSO (60 °C) for 10 min (b). Resist residues are removed after an O_2 plasma ashing process (c).

The process of electron beam (e-beam) evaporation consists of placing the target material in a crucible and vaporizing the top surface in a vacuum chamber by supplying kinetic energy from an accelerated focused electron beam. The evaporated species travel at high speed in a line-of-sight manner by keeping the chamber at a high vacuum ($\sim 10^{-6}$ mbar) [85, 86] such that collisions between evaporant material and background gas molecules

are kept at a low level. Such a directional deposition nature of e-beam evaporation in combination with an inwardly tapered resist profile are well suited for lift-off processes. The lift-off process is a widespread and indispensable patterning technique for creating micro- and nano-structures of a target material on a substrate (e.g. silicon wafer) using a sacrificial layer (e.g. resist). The technique is particularly useful when there is no appropriate etching method that provides good selectivity between the target material and the substrate.

In practice, it is often observed that optical resist (e.g., AZ5214E™) becomes hardened after an e-beam evaporation process and hence organic residues are left over (cf. Fig. 3.18(b)) even after cooking in hot DMSO, which features a strong resist stripping ability. The surface becomes clean after an O_2 plasma treatment as depicted in Fig. 3.18(c). However, this is rather undesirable since the oxygen plasma process might oxidize the evaporated material and introduce plasma damage.

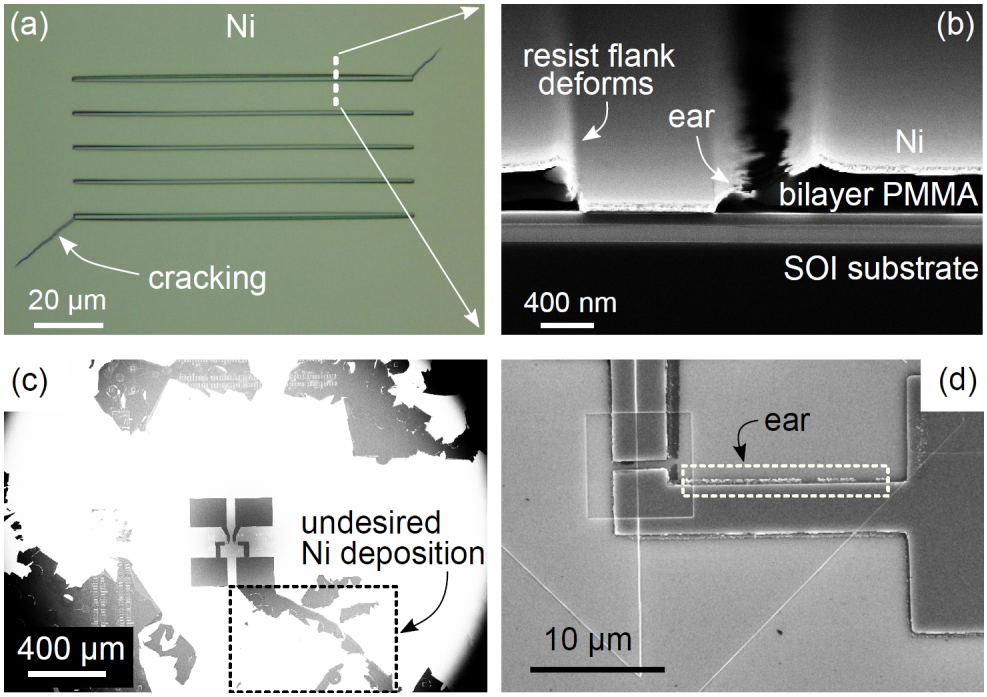


Figure 3.19: A nickel lift-off process with the unmodified evaporation setup and a bilayer PMMA resist. Top-view of 80 nm Ni evaporated on a bilayer PMMA resist showing undesired crackings (a). A scanning electron micrograph of the cross-section reveals resist flank deformation and ear formation (b). A top-view scanning electron micrograph of the sample after lift-off shows undesired Ni deposition as a result of peeling and cracking (c). A top-view scanning electron micrograph of the device area shows ear formation at the edge of contact lines (d).

In this work, polymethyl methacrylate (PMMA) is used in combination with e-beam evaporation to create high-resolution nickel contacts from a lift-off process. PMMA was one of the first materials developed for electron beam lithography [87] and it still remains as the

most commonly used positive-tone high-resolution e-beam resist. Moreover, an inwardly tapered resist profile can be easily realized by combining a more sensitive bottom layer (i.e., short polymer chain with lower molecular weight) and a less sensitive top layer (i.e., long polymer chain with higher molecular weight). Such an inwardly tapered resist profile is essential to facilitate solvent attack from uncovered resist sidewalls in order to obtain the best outcome in a lift-off process. However, one of the major drawbacks of such a process is associated with resist shrinkage and bubble formation that lead to cracking and blistering of the deposited layer. Fig. 3.19 displays typical results for nickel evaporation before and after the lift-off process. Fig. 3.19(a) depicts a top-view optical microscope image that clearly shows cracking, an electron micrograph cross-section along the dashed line in (a) is displayed in (b) revealing substantial shrinkage that leads to a strongly deformed resist pattern and hence to cracks and ear formation in the evaporated nickel film. Since ear structures are connected to the pattern, undesired nickel deposition is left over after the lift-off process as depicted in (c)-(d). Furthermore, more severe problems related to bubble formation that lead to blistering of the deposited film are observed for materials with a higher atomic number such as gold, hafnium, and platinum (cf. Fig. 3.24(a)).

Problems associated with resist shrinkage and blistering are due to a bombardment of the PMMA with charged particles (electrons and ions) [88, 89, 90, 91]. A series of complex mechanisms underlie the generation of these charged particles. According to Ref. [92], two major groups of electrons can be distinguished from the energy spectrum when a primary beam of electrons impinges on a specimen. The first group represents high energy electrons that are elastically scattered from the target material having nearly the same energy as the primary beam. The second group contains secondary electrons, electrons created through thermal ionization, thermionic emission, electron-impact ionization, and photoelectrons that feature an energy typically below 50 eV as depicted in Fig. 3.20 [90, 91, 93]. Apart from these high and low electrons, ions originating from thermal ionization and electron-impact ionization also play a role as will be disscussed below. These ions feature a low energy typically up to several electron volts [90].

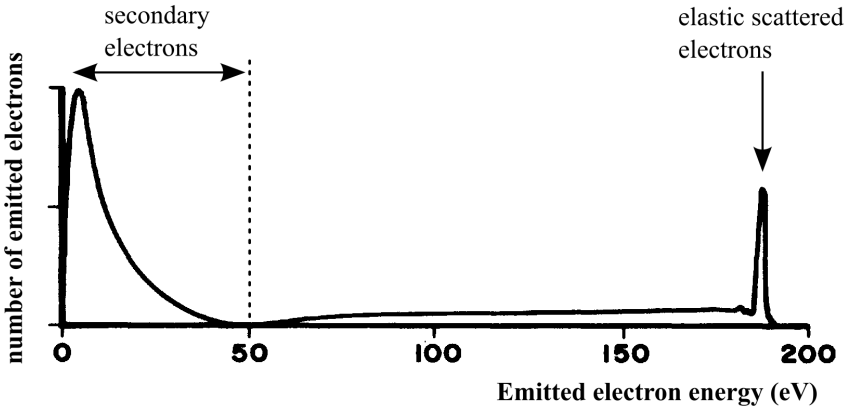


Figure 3.20: Energy distribution of emitted electrons when a primary electron beam of 180 eV impinges on a specimen. (From Ref. [92])

To study the impact of electrons and ions on resist shrinkage and blistering individually, the beam current is first ramped up to a value that is high enough to generate a sufficient amount of electrons yet still low enough to melt the material and induce any evaporation rate. A high-vacuum ($\sim 10^{-6}$ mbar) electron beam evaporation tool (Balzers™ PLS 500) is used to evaporate platinum, which tends to cause severe cracking and blistering issues with PMMA [88]. Bulk silicon substrates (p-type boron doped, 5-10 Ω·cm) are prepared with spin coating of bilayer PMMA films (see Appendix II). Structures are patterned with electron beam lithography and development in a mixture of methyl isobutyl ketone (MIBK) and isopropanol (IPA) (MIBK:IPA=1:3). The samples are mounted into the e-beam evaporation chamber and the emission current is increased up to 35 mA using a Pt target; note that at 35 mA beam current, no evaporation rate is detected with a quartz crystal microbalance, additionally the shutter remains closed. Thus, a direct irradiation of charged Pt ions, neutral Pt atoms and high energy electrons on PMMA film can be excluded.

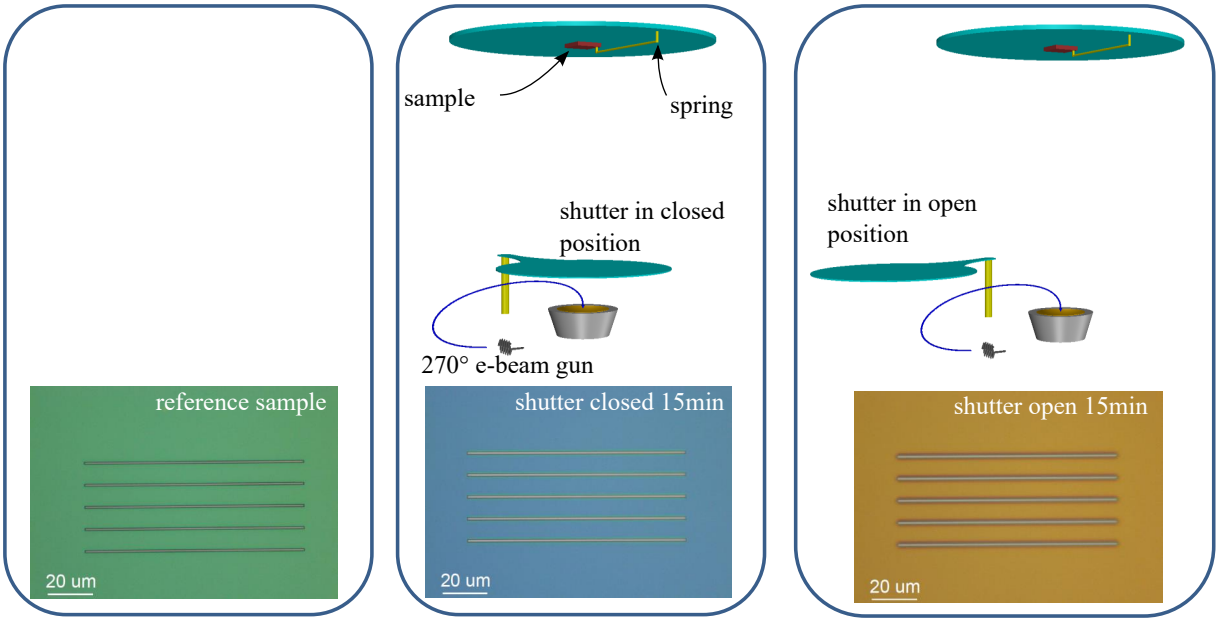


Figure 3.21: Comparison of bilayer PMMA film color for different evaporation conditions using platinum. All samples initially exhibit a green color after PMMA coating, electron beam lithography, and development like the reference sample (a). Film color changed to blue after ramping up power to 35 mA while keeping the shutter closed for 15 min (b). Film color changed to brown after ramping up current to 35 mA and opening shutter for 15 min (c). Note that the images are taken with the same settings of the microscope.

For a rapid initial study, optical microscopy of the PMMA film is employed using a Keyence™ digital microscope. All samples initially exhibit a green color as displayed Fig. 3.21(a). The PMMA film color changes into blue (see Fig. 3.21(b)) after ramping up the beam

current to 35 mA while keeping the shutter closed for 15 min (note that the shutter is also closed during the ramp up/down of beam current in a regular deposition process). This is unexpected and means that a substantial fraction of the electron beam incident on the target reaches the sample via multiple backscattering from the target and chamber walls. In addition, high energy electrons hitting the chamber walls may also lead to secondary electron emission that is incident on the sample. Next, when the shutter is opened for 15 min after reaching 35 mA beam current while keeping all other parameters the same, the PMMA film color changes into brown (as shown in Fig. 3.21(c)). Thus, we conclude that high energy electrons have a strong impact on PMMA even during the beam current ramp-up when the shutter is closed.

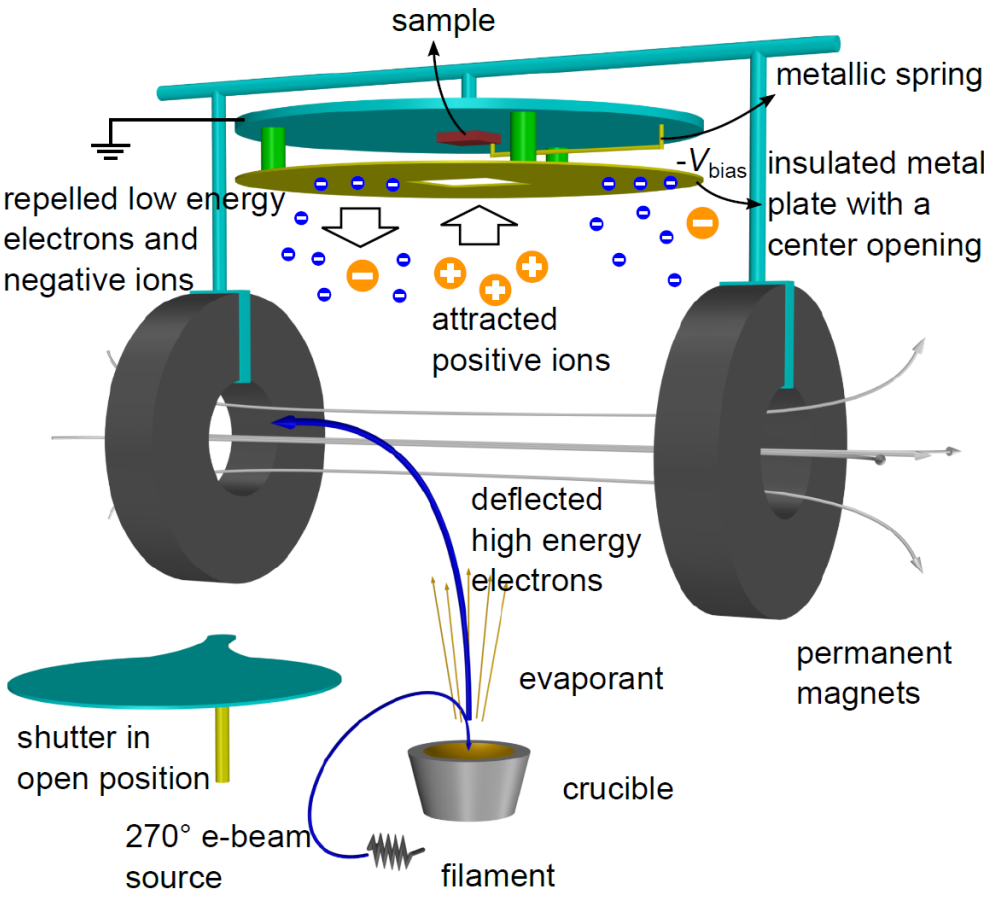


Figure 3.22: Schematic (dimension is not to scale) of a modified electron beam evaporation setup with permanent magnets and an electrically insulated metal plate installed to study the impact of electron and ion irradiation on sample surface.

Since charged particles can be manipulated with electric and magnetic fields, two ferrite ring magnets[3] together with the plate or the cylindrical electrode depicted in Fig. 3.22 and

[3]The inner diameter d_{inner}=60 mm, the outer diameter d_{outer}=100 mm, thickness 20 mm. The magnets are held with metal wires to an existing metallic rod which is designed by the manufacturer for mounting a

Fig. 3.23 are mounted in different configurations and their impact on the deposition result is studied. To this end, ∼80 nm of platinum is evaporated with a beam current of ∼81 mA (static spot ∼3 mm in diameter centered at the crucible) yielding a deposition rate of ∼1 Å/s. The initial evaporation setup yields a blistered and cracked surface as shown in Fig. 3.24(a). If only the magnets are installed, the surface depicted in Fig. 3.24(c) merely shows slight cracking compared to an evaporation process without magnets (cf. Fig. 3.24(a)). This means the magnets are very effective in deflecting the high energy backscattered electrons. However, despite the absence of blistering, the cross-sectional scanning electron micrograph shown in Fig. 3.24(d) reveals a bent Pt film (particularly on top of Si) and the layer starts to peel off the substrate. The reason for the peeling remains unclear but appears to be due to Pt ions and low energy electrons involved in the deposition process leading to reduced adhesion of the Pt film on the substrate.

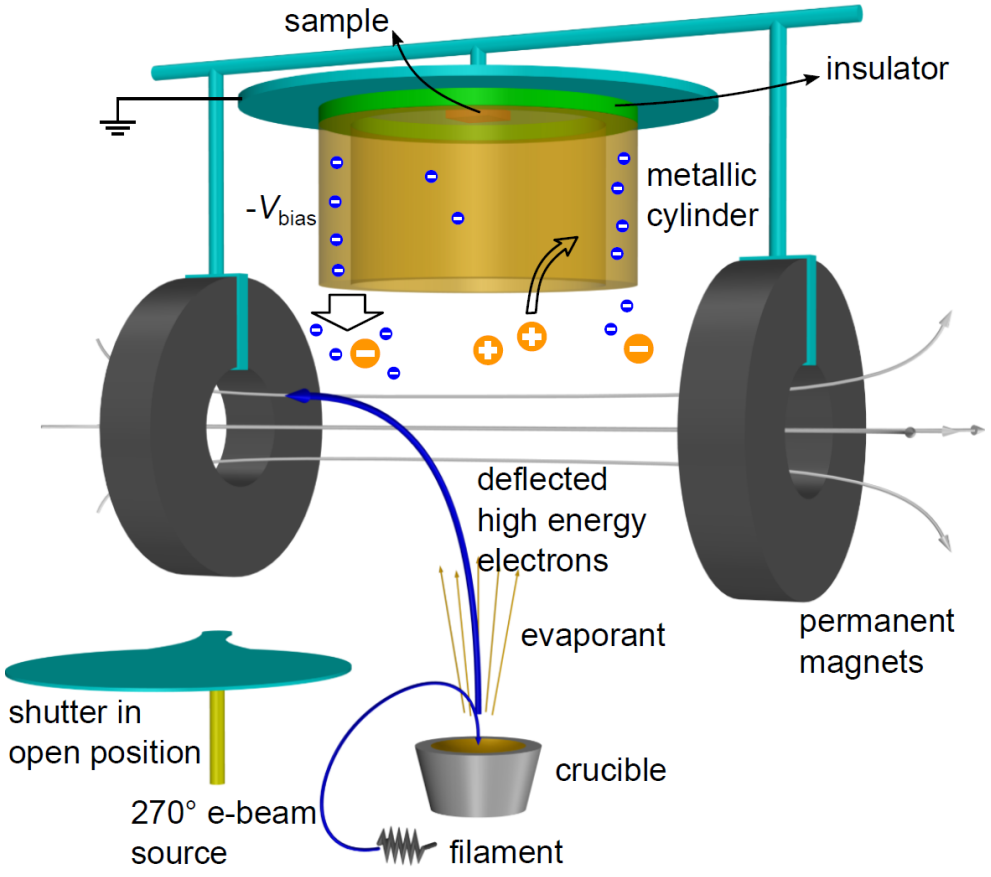


Figure 3.23: Schematic (dimension is not to scale) of the improved electron beam evaporation setup with permanent magnets and an electrically insulated metallic cylinder installed to avoid electron and ion irradiation on sample surface.

substrate holder. The magnets are installed relatively close to the substrate holder (bottom of the magnets to the substrate holder ∼125 mm) to reduce the disturbance on the 270 ° e-beam source. It is observed that there is no shift of the position where the electron beam hits the target within the crucible. The distance between the two magnets is ∼125 mm.

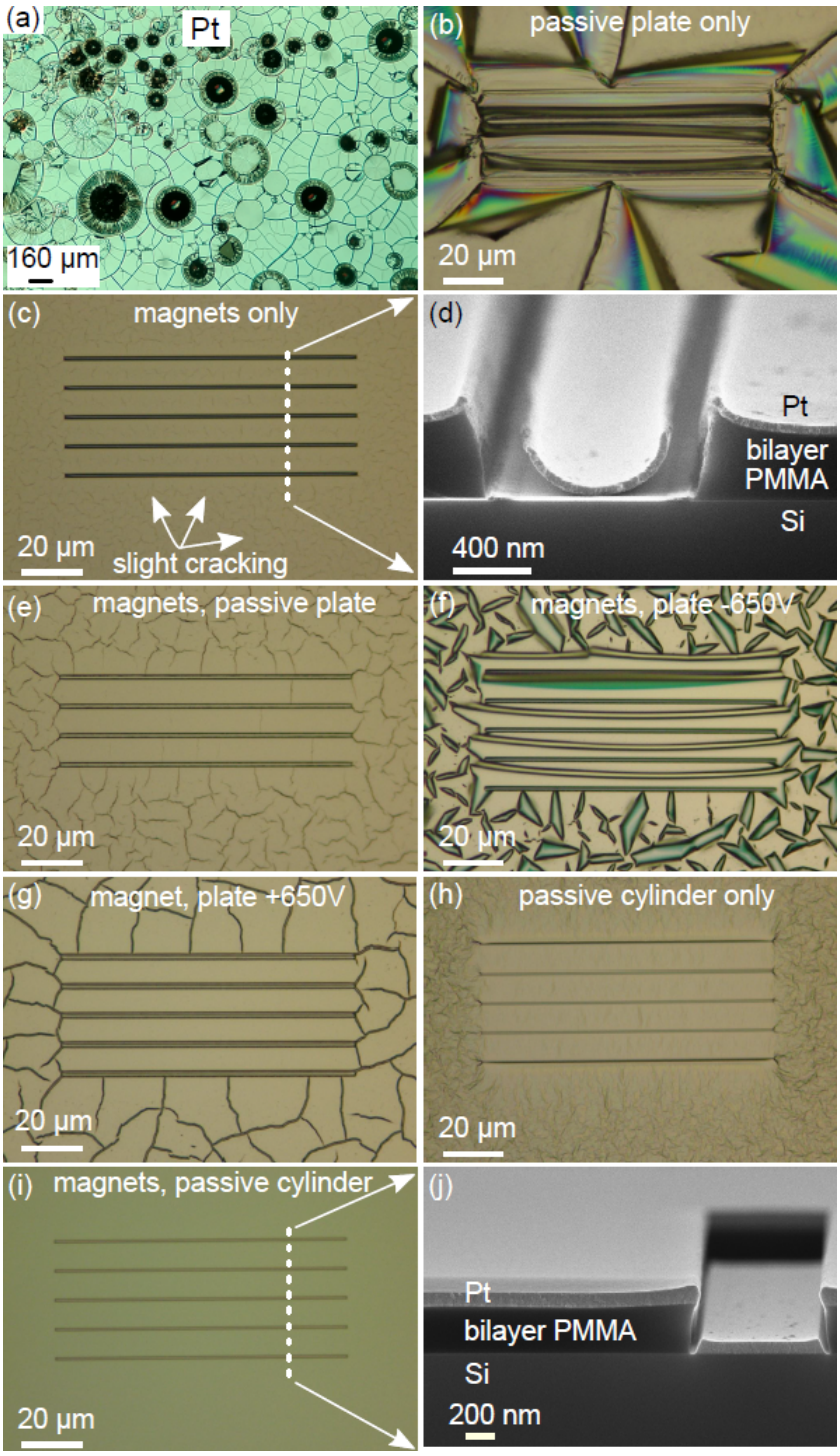


Figure 3.24: Evaporation result with different measures. Initial setup (a). Passive plate only (b). Magnets only (c). (d) is a scanning electron micrograph cross-section along the dashed line in (c). Magnets and passive plate (e). Magnets and the actively biased plate at $-650\,\mathrm{V}$ using an external voltage source (f). Magnets and the actively biased plate at $+650\,\mathrm{V}$ (g). Passive cylinder only (h). Magnets and passive cylinder using an evaporation rate of $1\,\mathrm{Å/s}$ (g) and a cross-sectional scanning electron micrograph along the dashed line in (i) is shown in (j).

Next, the magnets are removed and an electrically insulated plate electrode is installed. If it was only electron bombardment that yields blistering and resist shrinkage the plate should also be effective since it is expected that the plate negatively charges up (which is indeed the case as discussed further below) thus repelling at least the low energy part of the electrons. However, as depicted in Fig. 3.24(b), strong blistering is observed which is attributed to a significant bombardment of the sample with positively charged Pt ions that are accelerated by the negatively charged plate electrode. This is confirmed when mounting the magnets and the plate electrode showing slightly worse results compared to the case with magnets alone (compare Fig. 3.24(e) with (c)). Furthermore, applying a large negative bias of $-650\,\mathrm{V}$ at the plate electrode results in even stronger blistering due to accelerated positive Pt ions as shown in Fig. 3.24(f). In addition, a positive voltage ($+650\,\mathrm{V}$) applied at the plate electrode also leads to cracking which is mainly due to the acceleration of low energy electrons towards the sample as depicted in Fig. 3.24(g) (the impact of Pt^- ions is neglected since ions generated from the electron-impact ionization are almost exclusively Pt^+). The experiment continues by replacing the plate electrode with a cylindrical electrode as illustrated in Fig. 3.23 (however, no magnets are installed in the present case). As displayed in Fig. 3.24(h) a significant improvement compared to the plate electrode alone (cf. Fig. 3.24(b)) is obtained showing that the cylindrical geometry of the electrode shields the sample from a part of the Pt^+ ions. Finally, if the magnets and a floating cylindrical electrode are used, an ideal evaporation result could be achieved as depicted in Fig. 3.24(i) and (j): No blistering is observed and a cross-sectional scanning electron micrograph of the line structure shows no resist shrinkage and no bending of the deposited Pt film.

To further elaborate on this, the insulated hollow metallic cylinder is used to measure the potential of the electrode due to the charge accumulated during an electron beam deposition process. This potential together with the evaporation rate, deposited layer thickness and chamber pressure are plotted in Fig. 3.25 as a function of the electron beam current (note that the x-axis can also be interpreted as a time axis since the beam current is changed in steps of $\sim 5\,\mathrm{mA}$ during the beam ramp up/down with a stabilization time of $\sim 30\,\mathrm{s}$ - $45\,\mathrm{s}$.). First, the potential increases from A to B with an increasing beam current before the evaporation rate becomes non-zero reconfirming the observation shown in Fig. 3.21(b). When increasing the electron beam current from $\sim 55\,\mathrm{mA}$ to $\sim 81\,\mathrm{mA}$, the potential gradually drops while the evaporation rate increases (B to C). It is important to note that in this stage of the deposition process the shutter is still closed and hence the potential drop is likely caused by secondary electron emission due to a bombardment with high energy electrons reflected from the chamber walls. After the desired evaporation rate is reached, a sudden drop in plate potential is observed from C to D due to Pt^+ ions reaching the cylindrical electrode after opening the shutter (gray shaded area in Fig. 3.25). For platinum the measured potential drops to nearly zero at an evaporation rate of $\sim 3\,\text{Å/s}$. When the shutter is closed (D to E), Pt ions are prevented from reaching the electrode and the potential increases accordingly and reaches approximately -40 V again when the electron beam current is reduced (E to F); the potential is therefore 'M'-shaped.

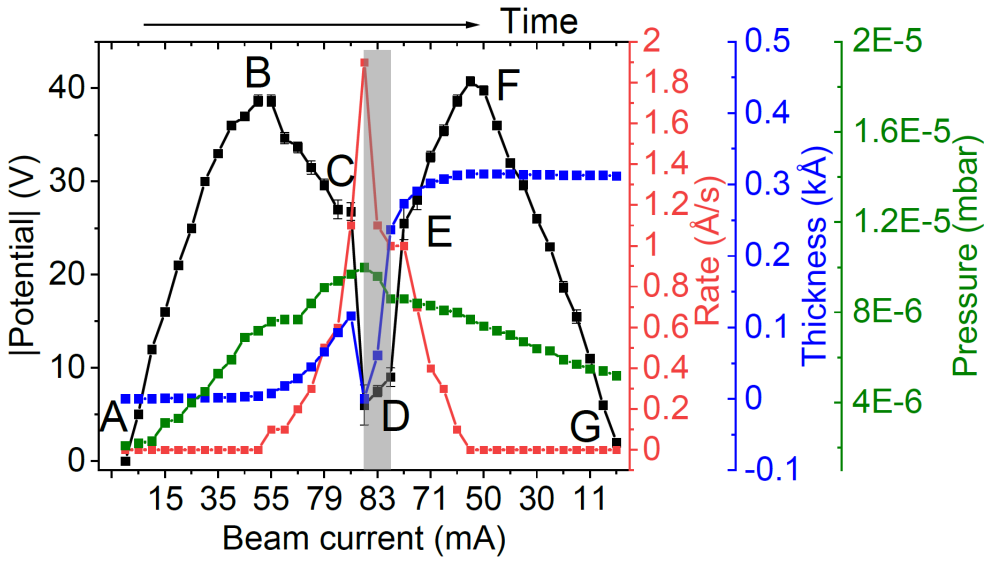


Figure 3.25: Potential at the cylindrical electrode, evaporation rate, film thickness (not corrected by tooling factor) and chamber pressure as a function of the electron beam current during Pt evaporation. The x-axis can also be interpreted as a time axis. Time window for an open shutter is indicated in the shaded area.

The investigations discussed above show that both electrons and ions play a predominant role on the blistering and cracking issues. Temperature has a lesser impact as the resist profile does not deform in an evaporation process using the modified evaporation setup (magnets and cylinder) to deposit a relatively thin layer of Pt (∼80 nm). In addition, the lift-off result shown in Fig. 3.26 obtained after cooking the sample in boiling acetone for 1 min without mechanical agitation also proves a non-crosslinked PMMA indirectly. Note that the deposited Pt film sticks well to the silicon surface without any adhesion layer (e.g., Ti) which is usually necessary.

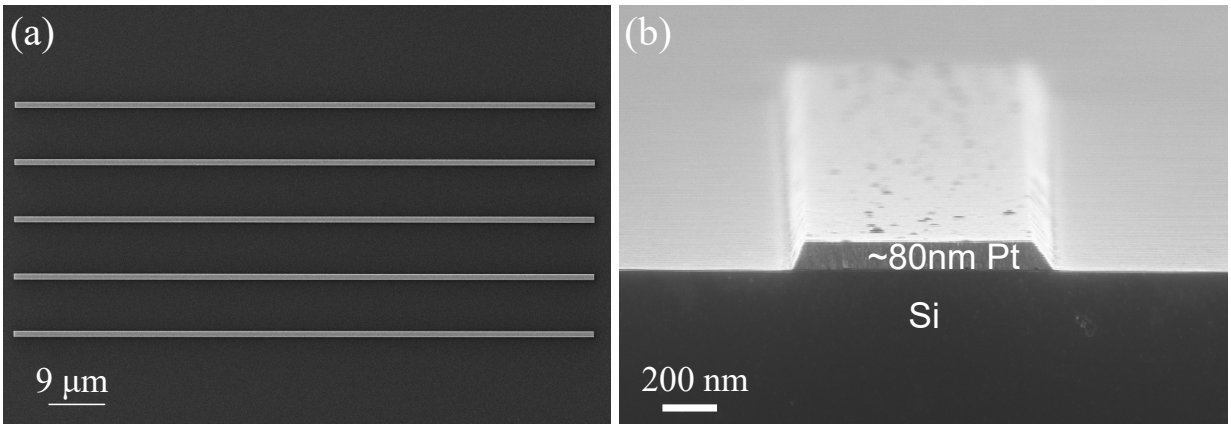


Figure 3.26: Top-view (a) and cross-sectional view (b) of the sample after cooking in hot acetone for ∼60 s without mechanical agitation.

3.3.1 Impact of temperature

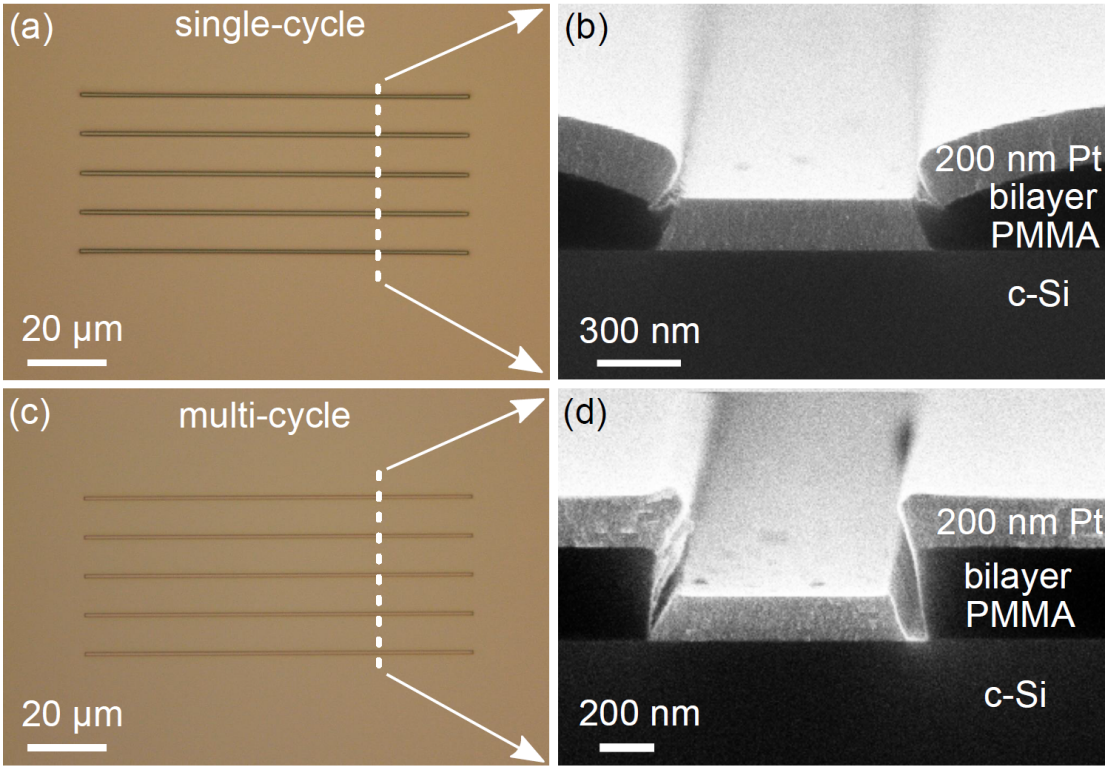


Figure 3.27: Impact of temperature on the PMMA resist profile. A thicker layer of 200 nm Pt using the proposed magnets/cylinder setup is deposited in a single-cycle evaporation process (a)-(b) and in a multi-cycle evaporation process (c)-(d). Approximately 50 nm of Pt is deposited in each cycle at a rate of 1 Å/s. The beam current is ramped down for substrate cooling (20 min) after each deposition cycle.

To further elaborate on the impact of temperature, irreversible temperature test strips (RS PRO™) are used to measure the highest temperature reached during the entire evaporation process through a color change of the sensing material. The test strips are mounted on a sample holder with the color change material facing towards the crucible. The test strips offer a measurement range between 40 °C and 260 °C.

The highest temperature measured in a Pt deposition process (80 nm @ 1 Å/s) is <116 °C. According to the manufacturer of PMMA resist, the glass temperature is in the range of 105 °C, and the polymers are thermostable up to a temperature of 230 °C. Furthermore, it is observed that the highest temperature reached throughout a single-cycle deposition process is still below 116 °C if a much thicker layer of 200 nm Pt is deposited. However, the PMMA resist profile deforms as depicted in Fig. 3.27(b) due to heat accumulation. One straight-forward approach to control the thermal budget is to split a single-cycle process into multiple deposition steps. Indeed, it turns out that a 4-cycle deposition process with

20 min of cooling interval is effective as depicted in in Fig. 3.27(d). Note that the 200 nm Pt layer still adheres well to the silicon substrate.

In conclusion, it is clear that temperature is absolutely not the root cause for blistering and cracking issues in a platinum e-beam evaporation process with a bilayer PMMA resist. However, temperature does have an impact on PMMA resist profile especially for thicker Pt layers due to heat accumulation. Therefore, it is recommended to water cool the substrate holder especially for thick layers or deep submicron structures. A multi-cycle deposition process is a straight-forward alternative that does not require any tool modification. Furthermore, permanent ferrite magnets do not lose magnetism throughout the evaporation process since the highest measured temperature is well below the Curie temperature of commercial ferrite magnets [94, 95].

3.3.2 Impact of X rays

It is observed that Pt deposition using the modified setup (magnets and cylinder) yields a quick and successful lift-off process in boiling acetone within 1 min as depicted in Fig. 3.26. This indicates that X-rays, which can not be manipulated by electric or magnetic fields, do not cause heavy cross-linking of PMMA throughout the evaporation process. In addition, this is separately confirmed by exposing a sample coated with a bilayer PMMA resist with the X-ray source from an X-ray diffractometer (Philips™ PANanalytical X'Pert PW3040/60). The PMMA is exposed to a Cu Kα line (8.0478 keV, $\lambda = 1.5406$ Å) X-ray source at an intensity of more than 10 million photons per second. The X-ray is generated by bombarding a copper electrode with an electron beam (40 mA at 40 kV acceleration voltage) and the resulting X-rays are filtered with a monochromator. After 60 hours of exposure, neither a change in film color nor bubble formation is observed. In addition, no heavy crosslinking is observed since the exposed PMMA film can still be dissolved in acetone.

Furthermore, it has been reported that the dose of X-ray is estimated to be on the order of $\sim$10 Mrad in a typical Al and Cr evaporation process [96]. According to Ref. [97], such a dose is far below the limit to induce crosslinking although a soft X-ray (317 eV) is used in this case.

3.3.3 Evaporation of nickel

In previous sections, a modified evaporation chamber equipped with ring magnets and a hollow metallic cylinder is proposed to deliver near perfect evaporation results for Pt. In fact, the modified evaporation setup has been demonstrated to be effective for a variety of materials commonly used in semiconductor fabrication, including metals, oxides, and semiconductor [98]. In particular, all these materials show an 'M'-shaped behavior of the potential (see Appendix III for details). The maximum potential measured is found to be strongly correlated with the atomic number of the material due to an increased

backscattering of the electron beam from the target material. For some of the materials, e.g. Si, Hf, TiO_2, and Al_2O_3, the measured potential further increases or reaches a plateau with increasing evaporation rate, which can be explained with different ionization degrees for different materials. In conclusion, despite the difference in material properties, the modified evaporation setup equipped with magnets and the passive cylinder using a moderate evaporation rate (∼1 Å/s) could deliver a blistering- and cracking-free deposition result for a variety of materials.

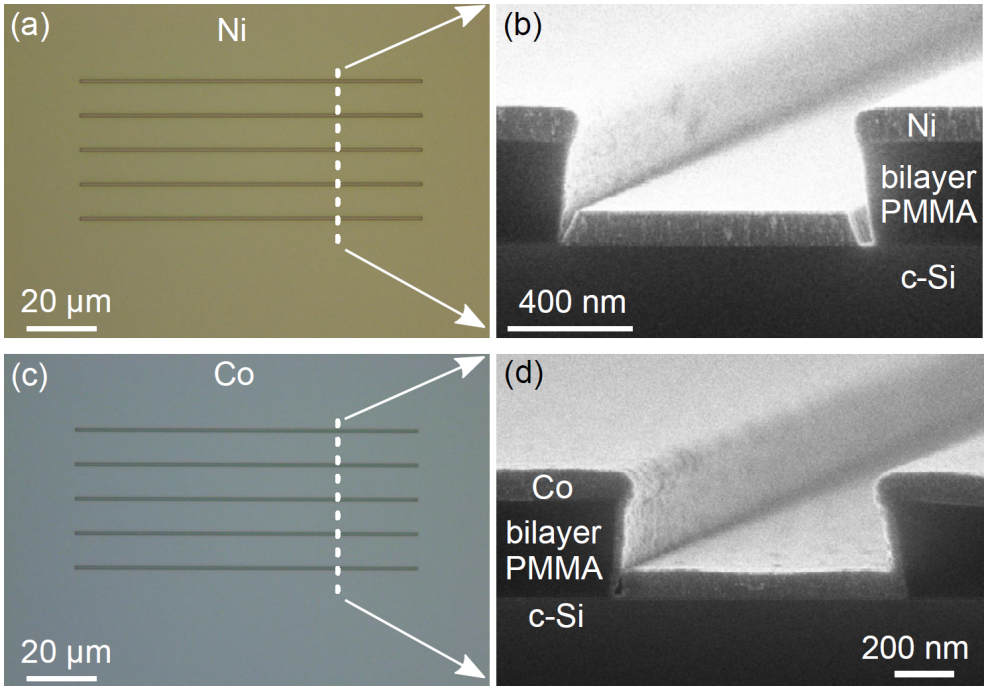


Figure 3.28: Evaporation of ∼80 nm Ni (a)-(b), and Co (c)-(d) using the modified setup with magnets and a passive hollow cylindrical electrode at an evaporation rate of 1 Å/s.

However, it is observed that despite the absence of blistering and cracking issues, the proposed evaporation setup yields deposition results where resist sidewalls are slightly covered with Ni as depicted in Fig. 3.28(b). Such sidewall coverage is even more pronounced in the case of Co as displayed in Fig. 3.28(d). It is speculated that such a behavior is due to the fact that both are ferromagnetic materials and the magnets are installed relatively close to the substrate holder. In addition, a more pronounced sidewall deposition is observed for Co since it features a higher Curie temperature ($T_{c,Ni} \approx 354\,°C$, $T_{c,Co} \approx 1130\,°C$). The issue is mitigated by increasing the distance between the two magnets (from ∼12.5 cm to ∼16 cm) as can be seen from the deposition results shown in Fig. 3.29. Note that the modified setup using a combination of magnets (∼16 cm) and cylinder is not tested since the atomic number of Ni is intermediate (no severe blistering is observed as shown in Fig. 3.19). Near perfect deposition results can already be achieved by using the magnets alone (cf. Fig. 3.29(a)) or even with the plate electrode also installed (cf. Fig. 3.29(b)), although a bent film (in particular on PMMA) is also observed similar to the case of Pt as

depicted in Fig. 3.24(d). Furthermore, it is worthwhile to mention that the lift-off of Ni can be accomplished in cold acetone without mechanical agitation within 15 s.

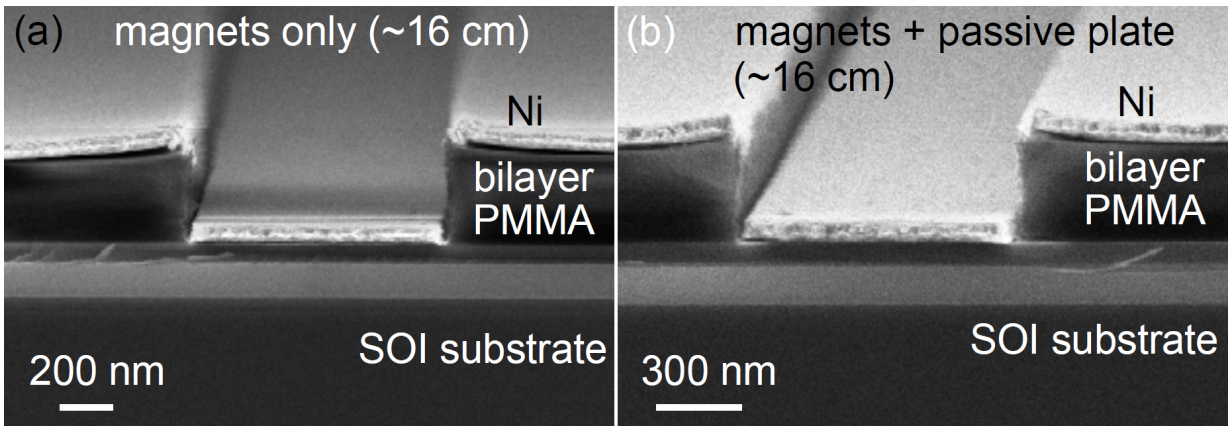


Figure 3.29: Evaporation results of Ni using different configurations. Cross-sectional scanning electron micrographs of the evaporation result using magnets only (separated wider from each other ∼16 cm) (b) and using both magnets (∼16 cm) and the passive plate (b).

3.4 Nickel Silicidation

Silicides fabricated by alloying silicon with metals such as Ti, Co, and Ni are essential ingredients of CMOS technology. They feature very low resistances and hence are widely used for the formation of polycide gate contact and Ohmic contacts in source/drain regions. Silicide is grown on a heavily doped semiconductor material for commercial integrated circuits as discussed in section 2.2 where low-resistive Ohmic contacts are formed as a result of the small depletion width (cf. Fig 2.5(b)), thus yielding a thin, and highly transmissive Schottky barrier. Compared with Ti and Co, the formation of nickel silicide offers an excellent control of thermal budget, less consumption of Si, better scalability (the ability to form uniform low-resistive silicide at a small gate length), and compatibility to SiGe [99]. Hence, nickel silicide has been extensively studied and integrated into CMOS technology since the 90 nm node and beyond [99].

Figure 3.30 shows cross-sectional scanning electron micrographs of as-deposited Ni films and silicidation results under different conditions. A two-layer material system is formed after thermal treatment in forming gas (10 % H_2 in N_2) ambient at 280 °C for 30 min as displayed in Fig. 3.30(c). According to Ref. [100], annealing at such a low temperature yields a nickel rich composition, i.e., Ni_2Si. Fig. 3.30(d) shows that full silicidation of the deposited layer is obtained after a two-step annealing process, namely, first at 280 °C for 15 min followed with a second annealing step at 380 °C for another 15 min. The thickness of the silicide film is approximately twice as much compared with the as-deposited layer. According to Ref. [101], the composition of the silicide is NiSi, which features the lowest

resistivity among all Ni_xSi_y phases [102]. In addition, the work function of nickel silicides ranges from 4.86 eV for Ni rich films to 4.3 eV for silicon rich films [103]. The work function of NiSi (∼4.5-4.7 eV) [104, 105] is closer to the midgap of silicon compared with other composites. Hence, NiSi could facilitate a more symmetric electron/hole injection into an ideal Schottky barrier which can be described by the Schottky-Mott model.

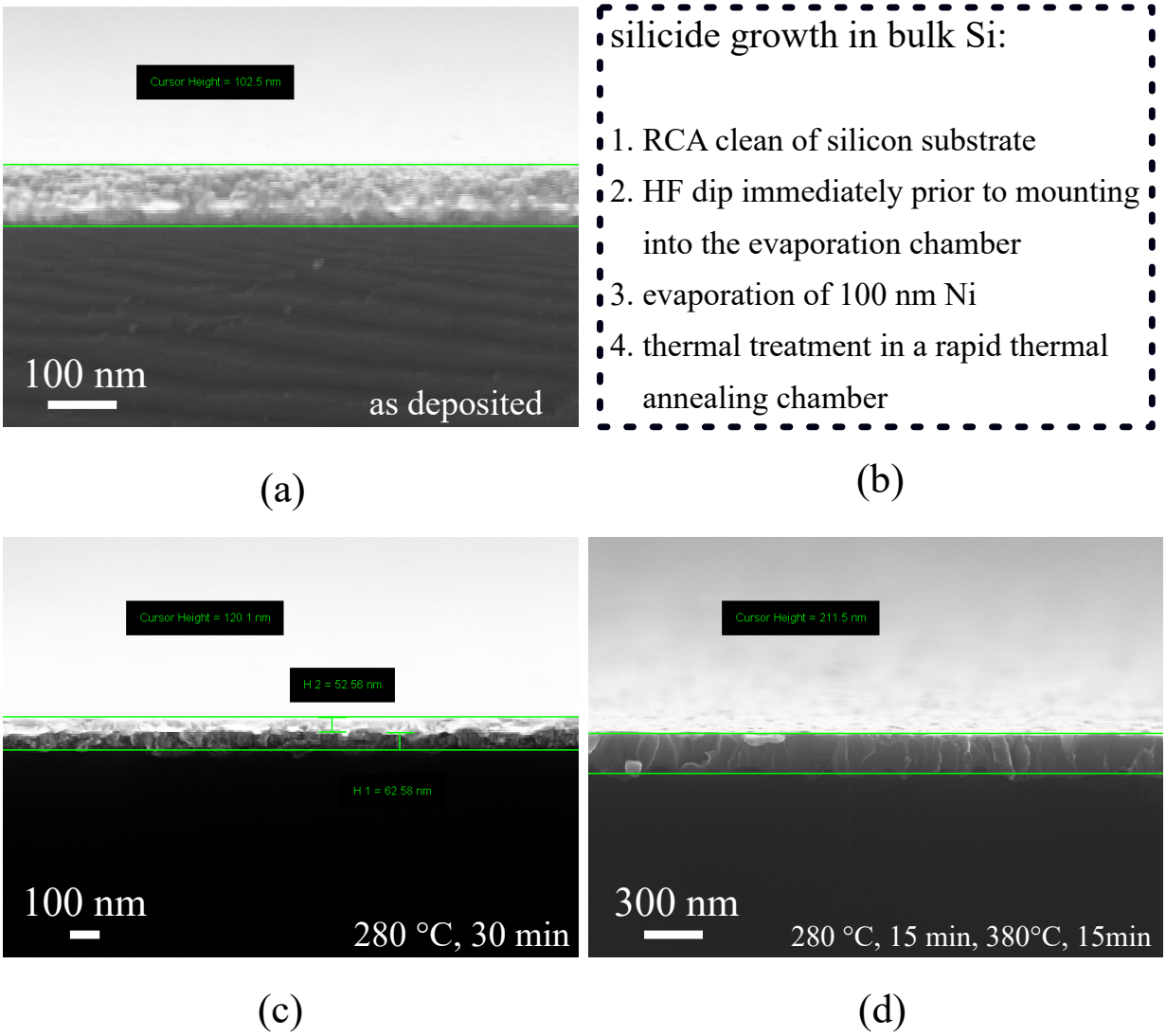


Figure 3.30: Nickel silicidation processes. A cross-sectional scanning electron micrograph of ∼100 nm Ni evaporated on a bulk silicon substrate (a). Recipe for silicide formation in bulk silicon substrate (b). Silicidation result after thermal treatment in forming gas at 280 °C for 30 min (c). Silicidation result after thermal treatment at 280 °C for 15 min followed with a second annealing step at 380 °C for another 15 min (d).

In addition, the phase formation of nickel silicide can be quite different in thin films than in silicon nanowires. It has been reported in Ref. [101] that the formation of the high-resistive

$NiSi_2$ could occur at a much lower temperature than 750 °C in SiNWs. To avoid this, the addition of 5 at% Pt to Ni has been demonstrated to raise the nucleation temperature of $NiSi_2$ and increase the thermal stability of the low-resistive NiSi composite [106].

Furthermore, the intrusion of nickel into a SiNW has been reported to cover a broad range of statistcal distribution[107] which could be mitigated by flash lamp anneal [108, 109] or a two-step annealing process, namely, create a finite source of Ni through selective removal of superficial Ni from the first annealing at low temperatures followed with a second anneal to form low-resistive NiSi [25]. The intrusion length is also dependent on the crystalline orientation where the silicide diffusion speed is faster in <100> compared to that in <110>-oriented SiNWs [107].

In the present thesis, nickel sicilide in direct contact with a moderately doped SiNW is used for the formation of a Schottky barrier. The intrusion of Ni into a SiNW for both with and without an oxide shell will be studied at different annealing temperatures. The resistivity of the nickel silicide will be evaluated with $I-V$ electrical measurements. Finally, an appropriate annealing time will be chosen to form silicide-SiNW junctions and create a gate overlap in order to achieve an excellent electrostatic control.

Chapter 4

Gated Schottky-Barrier MOSFETs

In this chapter, both single- and dual-gate SB-MOSFETs based on top-down fabricated silicon nanowires and nickel silicidation will be presented. Their principles of operation and device characteristics will be discussed in more detail to bring up strategies for performance improvement.

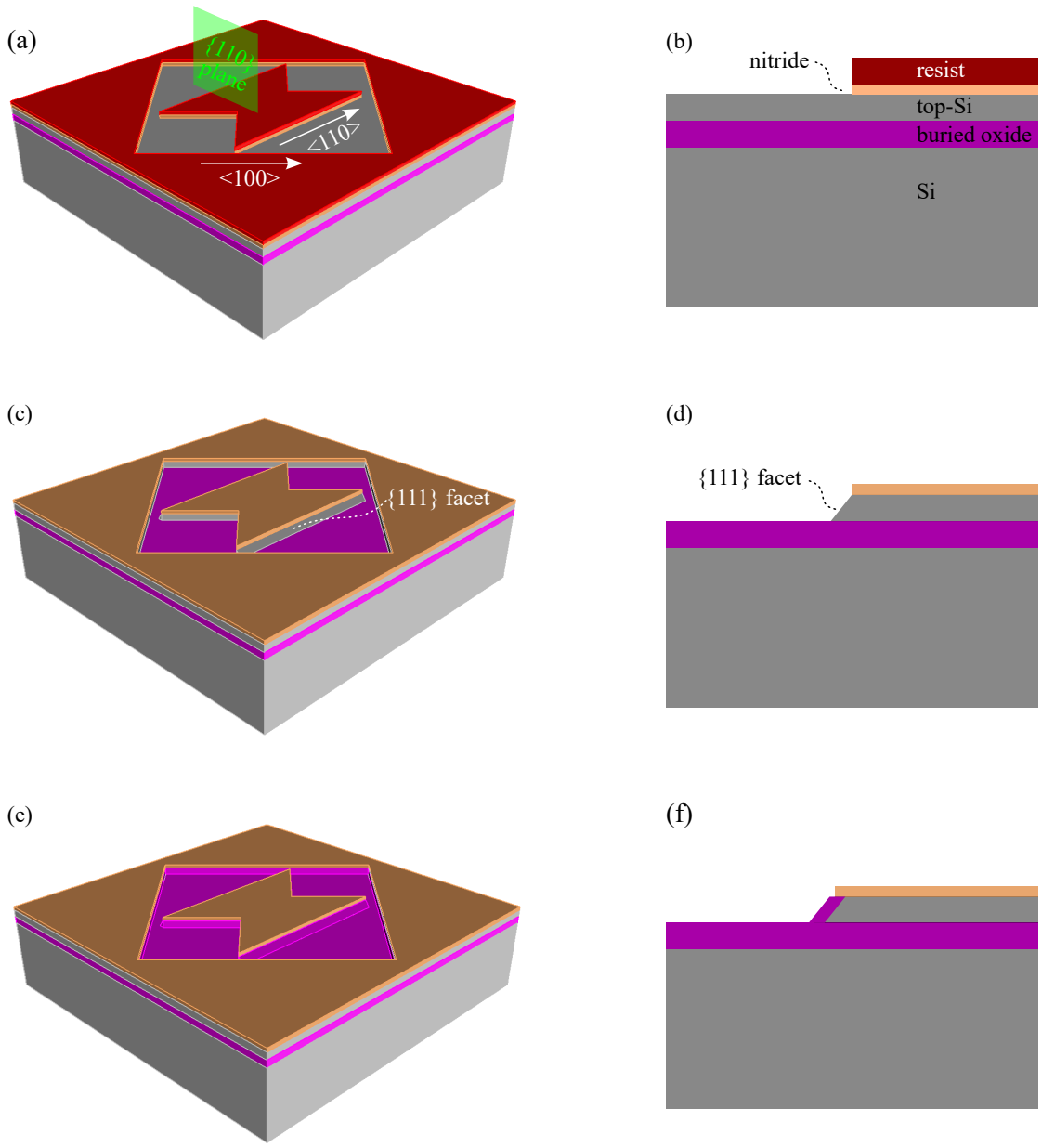
The next section first deals with the fabrication of triangular silicon nanowires from a two-step TMAH etching process. The self-limiting nature of this fabrication approach renders localized deep submicron silicon nanowires with atomically flat surfaces possible with conventional h-line contact lithography.

4.1 Silicon nanowire from a two-step TMAH etching

In recent years, silicon nanowires have attracted a great deal of interest for a variety of applications including gate-all-around field-effect transistors (GAA-FETs) [110, 111], tunnel FETs [112], junctionless FETs [113], biosensors [114, 115], and single electron transistors [116]. One-dimensional SiNWs intrinsically occupy less space and the small screening length makes nanowire FETs less susceptible to short-channel effects (see section 2.4), yielding a higher packing density of devices on a single chip. In addition, silicon nanowires facilitate the formation of gate structures that fully wrap a thin silicon body, yielding an excellent electrostatic control of the channel and full depletion of charge carriers. Moreover, silicon nanowires have a large surface-to-volume ratio and hence are attractive for highly sensitive biosensing applications. Furthermore, the confinement of charge carriers in a one-dimentional channel leads to a quantization of energy levels and hence SiNWs allow for the exploration of quantum mechanical effects.

Part of the work in Chapter 4 is published in IEEE Transactions on Electron Devices (DOI: 10.1109/TED.2021.3081527), and in IEEE Transactions on Electron Devices (DOI: 10.1109/TED.2022.3161245).

The devices mentioned above are often built on SiNWs that are fabricated from a bottom-up or top-down approach. The traditional vapor-liquid-solid method offers high-quality SiNWs yet the unavoidable transfer process is a key limiting factor for upscaling. Moreover, trace amount of non-CMOS-compatible material (i.e., Au), often unavoidable due to the growth method, can be detrimental to the device performance. On the other hand, conventional top-down fabrication techniques utilizing lithography and dry etching (see Appendix VII) often transfer line-edge-roughness from resist pattern to silicon feature via reactive-ion etching, which causes plasma damage and yields SiNWs with rough sidewalls, leading to a degradation in carrier mobility due to interface roughness scattering [42].



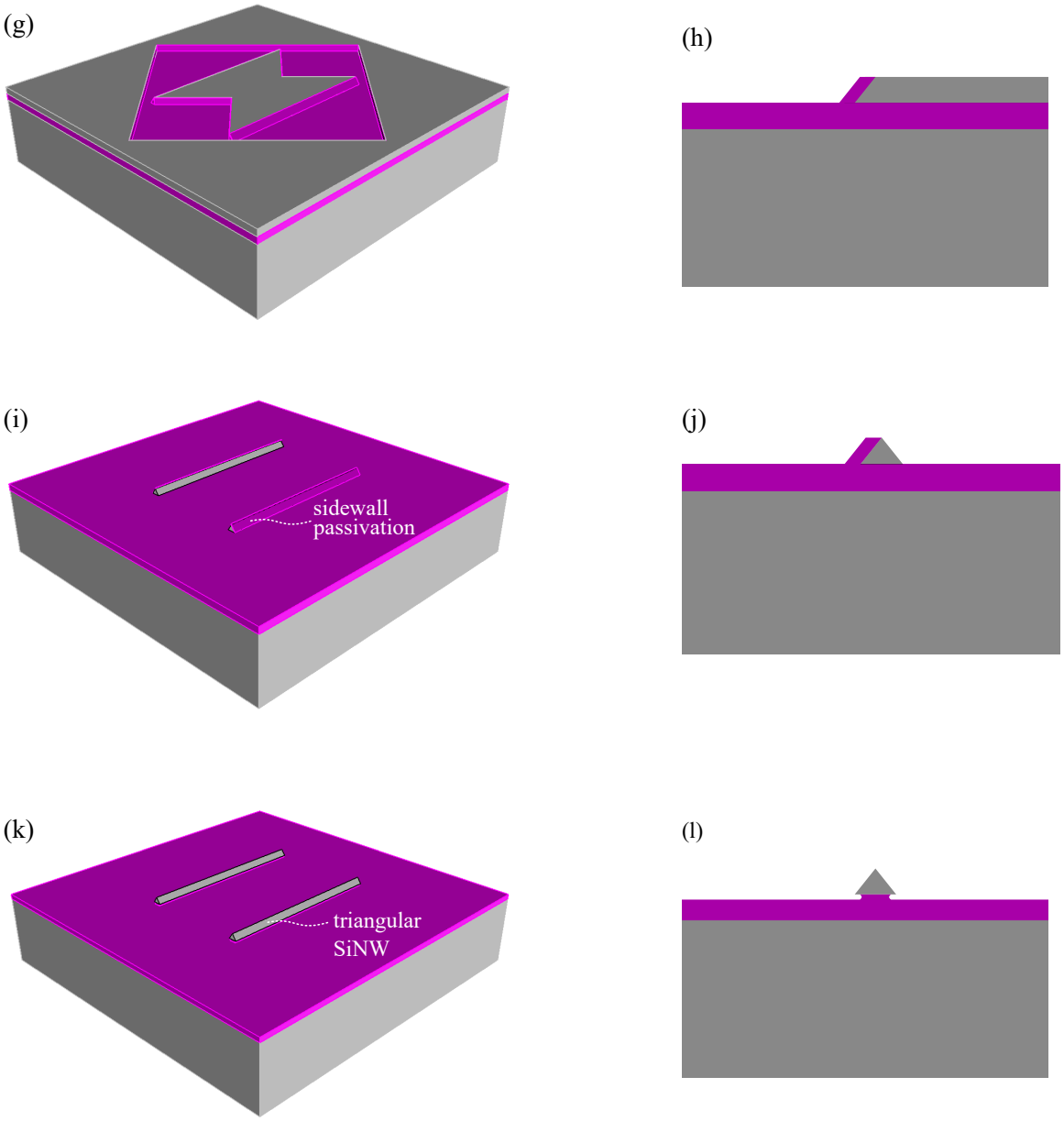


Figure 4.1: Mask design and fabrication process flow of silicon nanowires. Nitride hardmask patterning (a)-(b). A {111} facet is formed after resist removal and the first TMAH etching step (c)-(d). Local oxidation of the etched {111} facet (e)-(f). Removal of the Si_3N_4 hardmask (g)-(h). After the second TMAH etching step (i)-(j). A buffered oxide etch removes the local oxide (k)-(l).

In this work, silicon nanowires (SiNWs) are fabricated from a two-step wet chemical etching process as described in Ref. [117]. Tetramethylammonium hydroxide (TMAH) instead of potassium hydroxide (KOH) is used as the wet chemical etchant of silicon to ensure a fully CMOS-compatible fabrication process. The top-down fabrication approach yields localized

SiNWs with atomically flat surfaces and minimal plasma damage manufacturable with conventional h-line contact lithography. Fig. 4.1 shows the mask design and fabrication process flow of SiNWs with triangular cross-section. A {111} facet inclined at 54.74 ° with respect to the {100} facet is formed due to the distinct etch-rate anisotropy of different crystallographic planes [61] in an alkaline solution (i.e., TMAH) when a silicon nitride hardmask is defined in a line-pattern along the <110> direction of a (100)-oriented silicon substrate as depicted in Fig. 4.1(d). Fig. 4.1(f) shows a local oxidation of the etched {111} facet that exploits the ability of Si_3N_4 to act as an effective diffusion barrier. After selective removal of the Si_3N_4 (cf. Fig. 4.1(h)), a triangle bounded by two {111} facets is formed in a second TMAH etching as displayed in Fig. 4.1(j) since the {111} facet fabricated from the first TMAH etch step is protected by the grown, local oxide. Finally, a short dip in buffered oxide etch (BOE) removes the local oxide and creates an undercut in the buried oxide layer as depicted in Fig. 4.1(l). The complete run card including process parameters for the fabrication of SiNWs with triangular cross-section can be found in Appendix I.

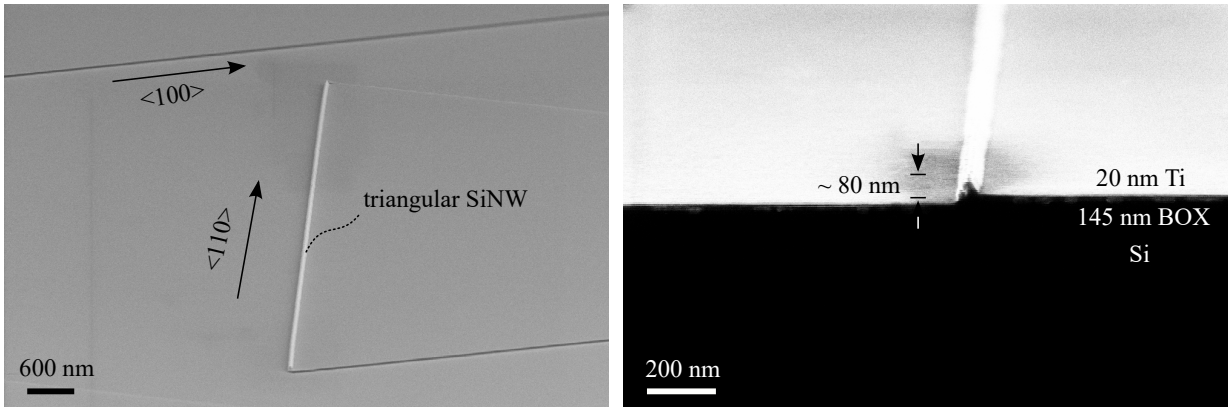


Figure 4.2: Scanning electron micrography images of the fabricated SiNWs. The SiNW in (a) reveals a triangular cross-section after cleaving (b). Length of the SiNW is 40 μm.

Figure 4.2 shows scanning electron micrographs of the fabricated SiNWs corresponding to the step shown in Fig. 4.1(i)-(j). The SiNW reveals a triangular cross-section (cf. Fig. 4.2(b)) after cleaving along the green {110} plane as depicted in Fig. 4.1(a). The buried oxide layer of a silicon-on-insulator substrate acts as an etch-stop layer. Hence, size of the triangle mainly depends on the thickness of the top-silicon layer and thus the nanowires are manufacturable with conventional h-line contact lithography. As it was discussed in section 3.1, the wet-etched {111} facets feature minimal plasma damage and exhibit a surface roughness comparable to that of a commercial prime-grade silicon wafer. It is worthwhile to mention that an optional treatment in 40 % NH_4F (see Appendix VIII) could further improve the surface roughness.

Next, the local oxide depicted in Fig. 4.1(j) is removed in a buffered oxide etch (BOE 7:1) for 15 s. Subsequently, a dry oxidation process is carried out to reduce the size of the SiNW

and form a gate oxide at the same time. To simplify the fabrication process as much as possible, a treatment in 40 % NH_4F and the hydrogen annealing process is not carried out. Finally, various electronic devices including resistors, single- and dual-gate Schottky barrier transistors are fabricated and characterized.

4.2 Back-gate Schottky-barrier devices

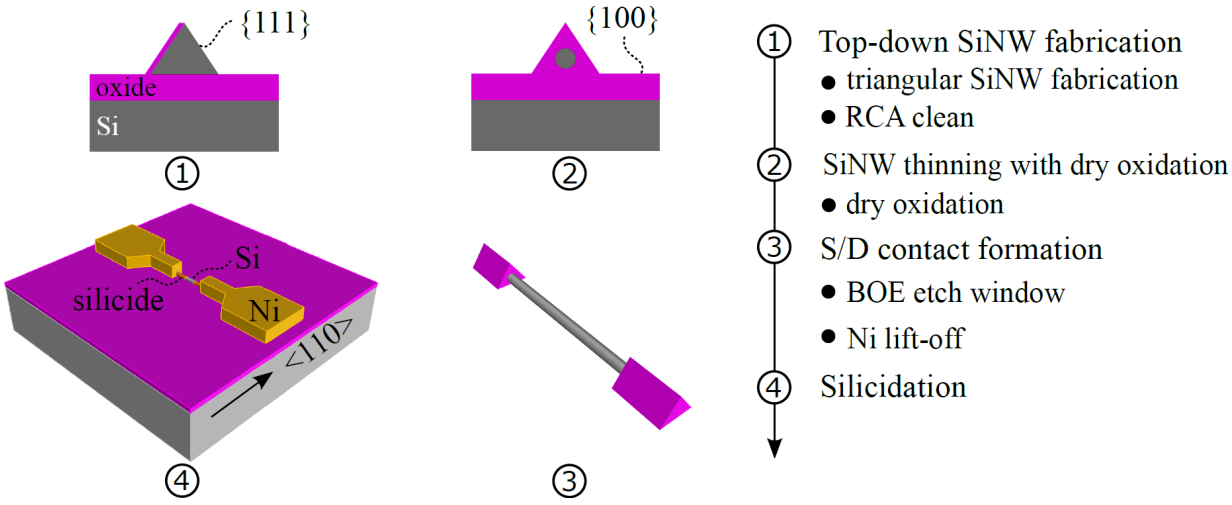


Figure 4.3: Schematics (dimension is not to scale) and key process steps for back-gate Schottky-barrier MOSFETs. The dimensions of the device are: oxide thickness $t_{ox} > 15\,nm$, diameter of SiNW $d_{SiNW} = \sim 25\,nm$, distance between source and drain $L_{S,D} = 900-1200\,nm$.

In this section, quality of the fabricated SiNWs and nickel silicide are preliminarily tested with back-gate Schottky barrier devices. First, the sample is cleaned with a standard cleaning procedure (i.e, RCA clean [118]) after removal of the local oxide as depicted in the first step of Fig. 4.3. Subsequently, a dry oxidation step is carried out to reduce the size of the SiNW. The dry oxidation is carried out for 3 min at a temperature of 1100 °C, i.e., higher than the viscous flow point. Although such a high temperature prevents a self-limiting oxidation [119], it allows transforming the cross-section of the SiNW from triangular to a circular shape as shown in the second step of Fig. 4.3(b) (also check Appendix VI for experimental results). In addition, it also minimizes the degradation of the Si-SiO_2 interface due to roughness induced by the oxidation process [120]. Next, etch windows are patterned and opened up by removing the oxide shell in a buffered oxide etch (BOE 7:1) step for 20 s (cf. the 3rd step in Fig. 4.3 and Fig. 4.4(a)). Afterwards, nickel contacts are fabricated with electron beam lithography using a bilayer PMMA resist, the modified electron beam evaporation (see section 3.3), and lift-off. Finally, the sample is annealed in forming gas (10 % H_2 in N_2) at various temperatures to grow the silicide and drive the silicide-SiNW junction towards the center of the SiNW as depicted in the fourth step of Fig. 4.3. An optical microscope image of two readily fabricated devices is shown in Fig. 4.4(b).

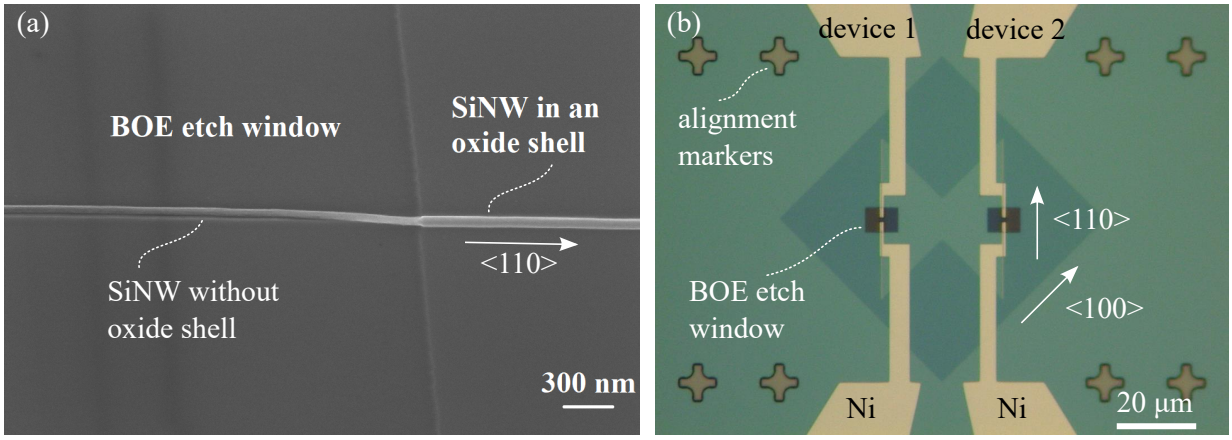


Figure 4.4: A scanning electron micrograph of the SiNW after removal of the oxide shell (a). An optical microscope image of two back-gate devices (b).

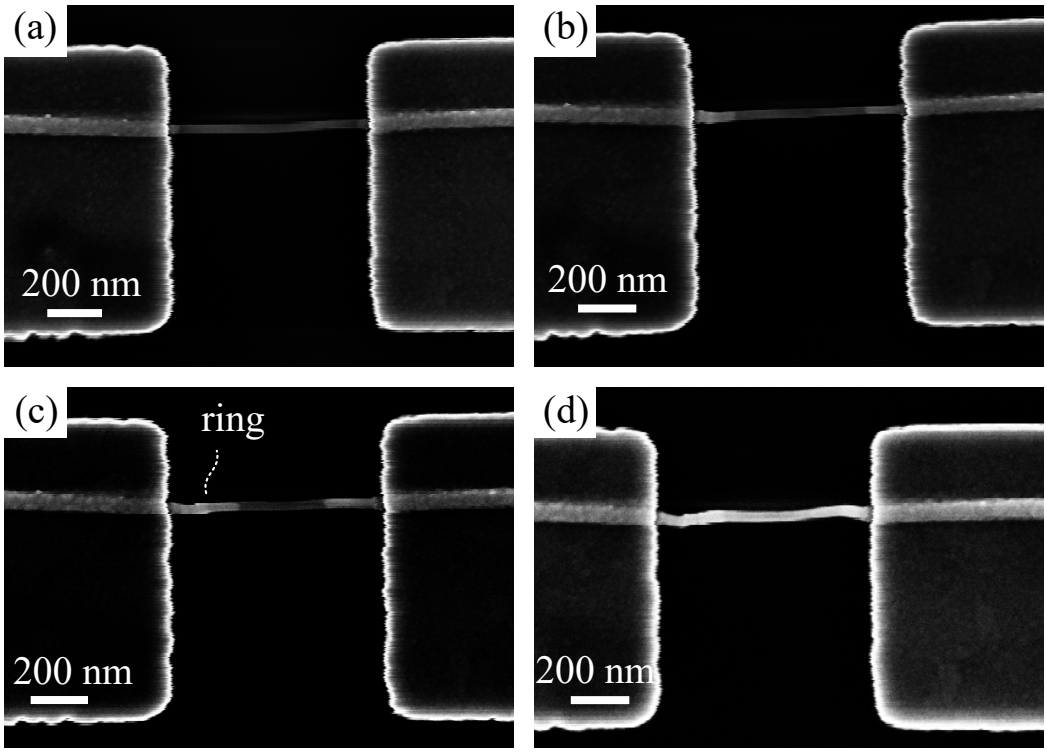


Figure 4.5: Axial diffusion of nickel along a SiNW after 4 cycles of thermal treatment. Almost no Ni intrusion is visible after the first annealing cycle (280 °C for 60 s, further ramp up to 380 °C and anneal for another 60 s) (a). Evident silicide growth is detected after the second annealing cycle (450 °C, 30 s) (b). Ni intrudes further after the third annealing cycle (450 °C, 30 s) (c). Silicide growth meets up from both ends after the fourth annealing cycle (450 °C, 60 s) (d).

Figure 4.5 shows the first type of back-gate devices where four cycles of thermal treatment

eventually lead to full silicidation of the nanowire. Fig. 4.5(a) shows that there is almost no Ni intrusion visible after the first annealing cycle at 280 °C for 60 s, and further ramp up to 380 °C and anneal for another 60 s. Evident silicide growth is detected after the second annealing cycle at a higher temperature of 450 °C for 30 s as displayed in Fig. 4.5(b). Further intrusion of Ni is facilitated by repeating the last process (450 °C, 30 s) as depicted in Fig. 4.5(c). Finally, a fourth annealing cycle at the same temperature (450 °C) for 60 s turns the SiNW into a silicide nanowire.

Figure 4.5(c) shows that the length of the silicide is longer at the left-hand side. Indeed, it is observed that the intrusion lengths from both sides are often not necessarily identical. Similar phenomena are also observed in Ref. [121]. Fig. 4.6 shows the length of axial Ni intrusion for 6 devices on the same chip after two cycles of thermal annealing at 450 °C for 30 s. It is clear that the silicide length covers a broad range from below 200 nm to above 300 nm. However, the mean intrusion lengths are almost the same for the left- and right-hand sides.

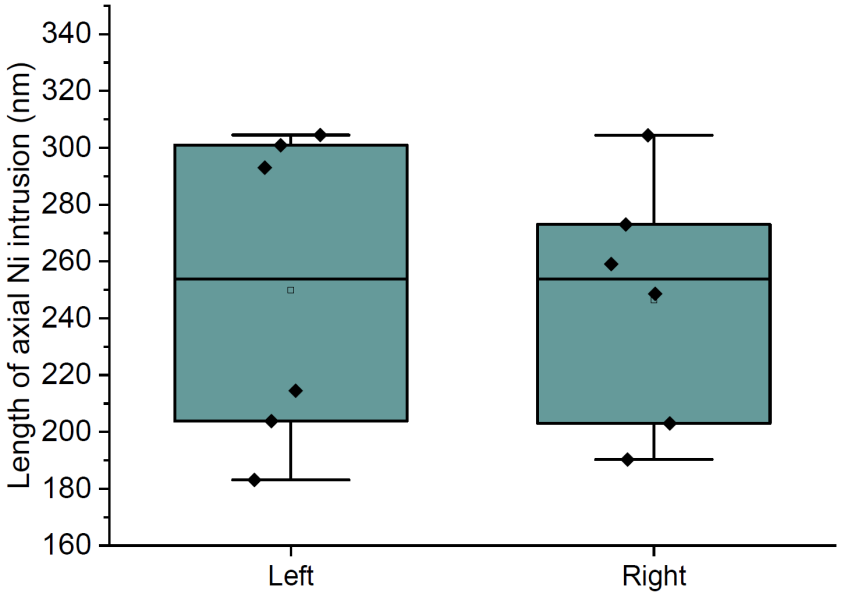


Figure 4.6: Axial diffusion of nickel along a SiNW after 2 cycles of thermal treatment (450 °C, 30 s). Silicide growth from left- and right-hand sides exhibits a broad range of intrusion length. The mean intrusion length is approximately 250 nm from both sides.

Figure 4.7 displays two more examples of full silicidation. It can be seen that the radius of the silicide nanowire is not homogeneous after the silicidation process. Similar phenomena are also observed, e.g., in Ref. [122]. Repeated annealing cycles often result in ring- and pea-like sections across the nanowire. These sections with substantially larger radii correspond to nickel-rich silicide whereas the homogeneous middle part in Fig. 4.7(b) represents the low-resistive monosilicide NiSi [122]. A homogeneous high-quaility monosilicide nanowire can be achieved by avoiding repeated thermal cycling of SiNWs [122], which is desirable

since the monosilicide exhibits a midgap work function and a lower resistivity than the nickel-rich silicides.

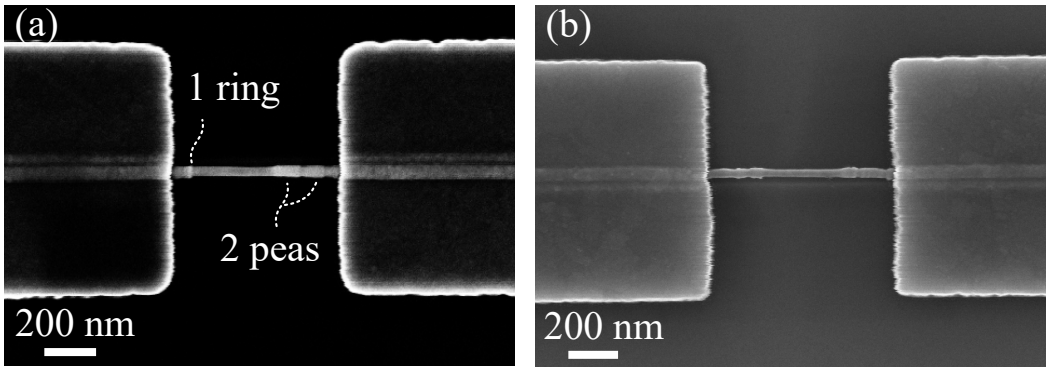


Figure 4.7: Two further examples of full silicidation. Repeated thermal cycling induces ring- and pea-like sections at both ends of the nanowire.

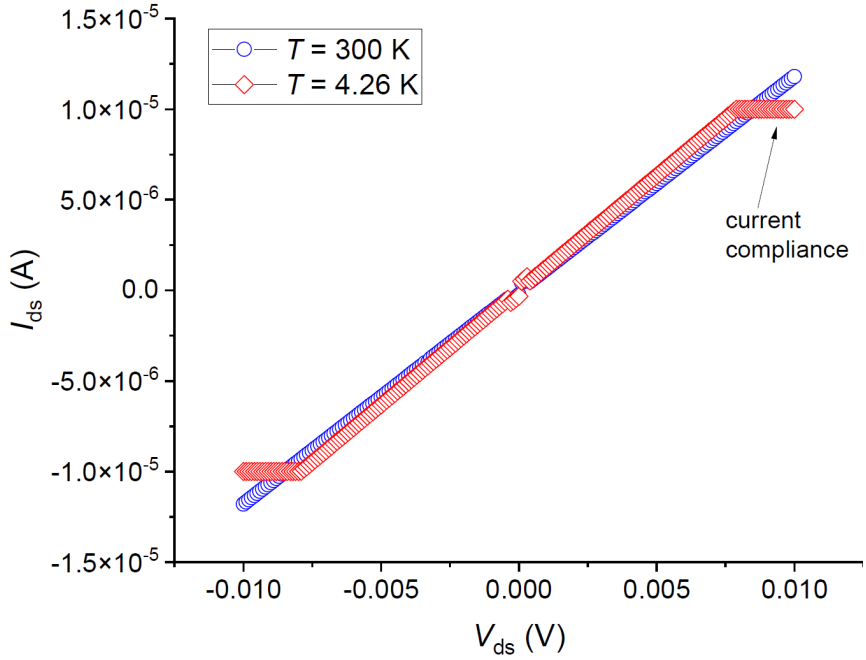


Figure 4.8: Two-point $I-V$ measurement of a nickel silicide nanowire at both room- and cyro- temperatures. Note that the device is bonded on a chip carrier with Al wires.

Electrical characterization of the silicide nanowires is carried out with simple two-point $I-V$ measurements. Lower resistivity of the silicide nanowire at liquid helium temperature ($R_{4.26\mathrm{K}} = 795.8\,\Omega$) compared to that at room temperature ($R_{300\mathrm{K}} = 829.9\,\Omega$) as depicted in Fig. 4.8 confirms the metallic behavior of the nickel silicide nanowire. In addition, the silicide nanowires do not turn superconducting at liquid helium temperature, which is consistent with Ref. [123]. Based on the room-temperature measurement results of 3 such

devices, the calculated resistivity is in the range of 37.2 $\mu\Omega$·cm−75.6 $\mu\Omega$·cm if the diameter of the silicide nanowire is 30 nm. Note that this value is slightly larger than the resistivity of monosilicide and rather corresponds to that of a nickel-rich silicide composition, although the resistances of aluminum bonding wires, cables, as well as contact resistances, etc. are not excluded in a two-point $I - V$ measurement.

Figure 4.9 depicts the second type of back-gate devices fabricated with the same annealing process mentioned above where the intrusion of Ni leaves an ultrasmall silicon island in the middle. Such a device can be used to realize extremely small single quantum dots defined by two Schottky tunnel barriers with silicide-SiNW junctions [124].

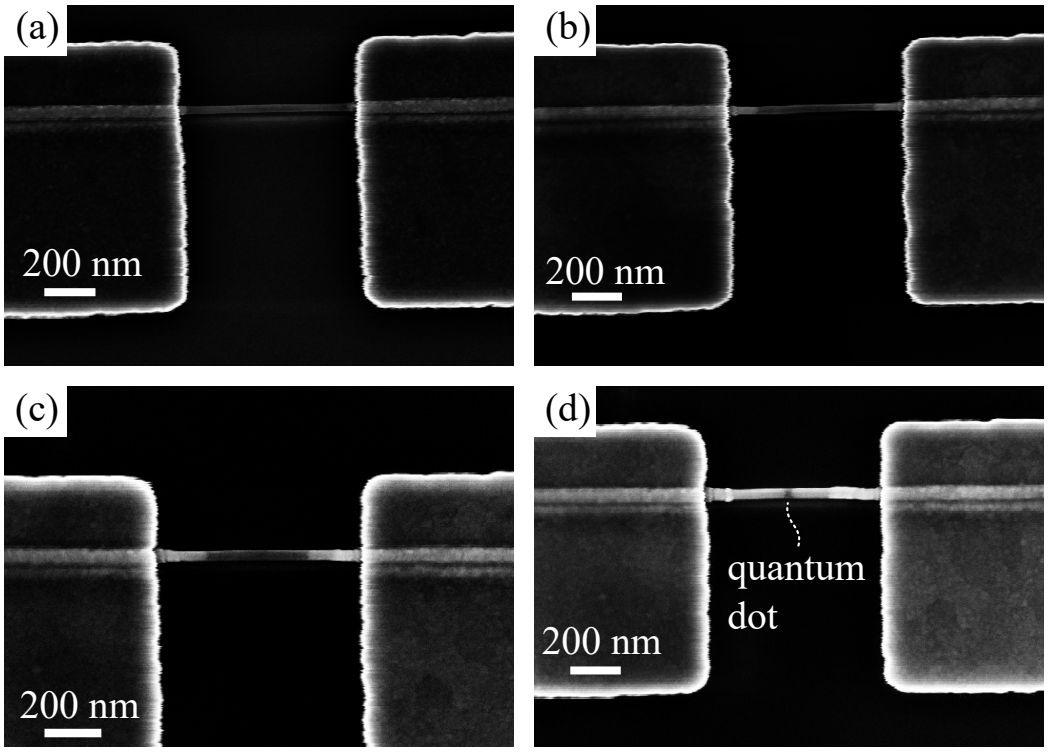


Figure 4.9: SiNW with nickel silicide source/drain contacts and an ultrashort channel length.

Similarly, Fig. 4.10(d) shows a longer silicon section (∼100 nm) achieved using the same annealing process merely by defining a larger distance between the source/drain contacts. The transfer characteristic curve displayed in Fig. 4.11 reveals typical ambipolar behavior of SB-MOSFETs due to the absence of a band gap in source and drain contacts [25]. Carriers can be injected into the conduction band and into the valance band depending on the V_{gs} voltages applied.

It has to be noted that the back-gate Schottky-barrier MOSFET is similar to the so-called Ψ-MOSFET [125], which can be employed for testing the quality of an SOI substrate.

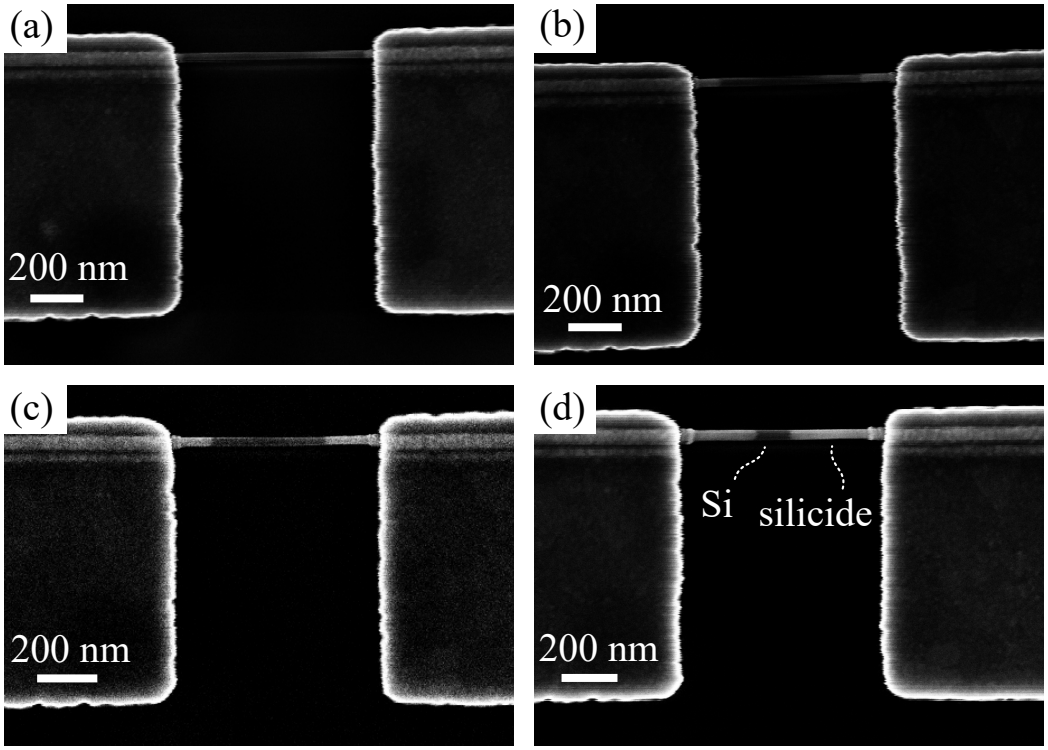


Figure 4.10: SiNW with nickel silicide source/drain contacts and a long channel length.

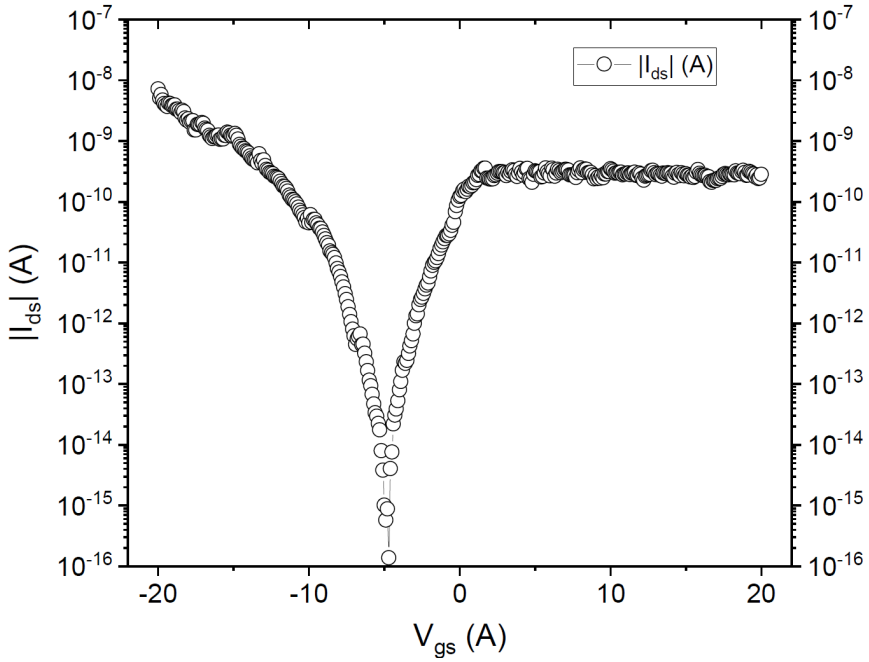


Figure 4.11: Transfer characteristic curve of a long-channel back-gate Schottky-barrier MOSFET. Note that V_{gs} covers a broad range from -20 V to 20 V due to a small gate coupling factor as a result of the thick buried-oxide layer ($\sim$ 145 nm).

A Ψ-MOSFET is formed by contacting the top-Si layer of an SOI substrate with two probe needles and the bulk-Si substrate acts as the back-gate electrode. A conduction channel can be formed at the interface of the buried oxide and top silicon layers by applying an appropriate back-gate voltage whereas the buried oxide layer acts as the gate oxide. Despite the simplicity of the device (no lithography needed), similar transistor characteristics (cf. Fig. 4.11) can be obtained and analyzed to evaluate the quality of an SOI material [126, 127].

4.3 Single top-gate Schottky-barrier devices

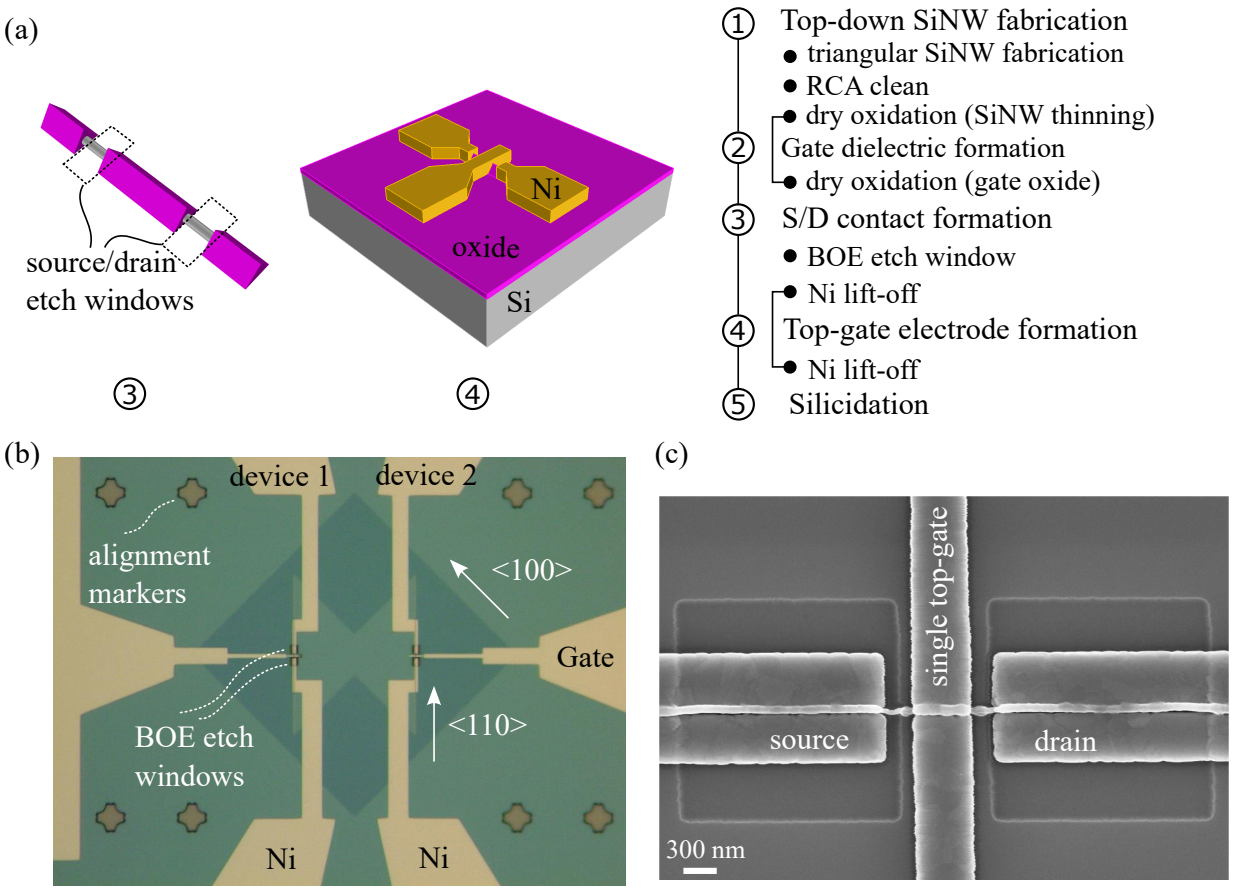


Figure 4.12: Schematics (dimension is not to scale) of the single top-gate Schottky-barrier MOSFET before and after metallization and the key steps in device fabrication (a). An optical microscopy image (b) and a scanning electron micrograph (c) of the readily fabricated single top-gate Schottky-barrier MOSFET.

In this section, silicide growth in an oxide shell will first be investigated. Next, a top-gate is then formed on top of the oxide shell to replace the back-gate electrode. Discussions

will be elaborated on the behavior of single top-gate Schottky-barrier MOSFETs and in particular to understand the kink formation in transfer characteristics.

The fabrication of single top-gate Schottky-barrier MOSFETs is similar to the back-gate device presented in the previous section. The back-gate devices utilize the buried oxide layer of SOI material as gate oxide whereas the oxide growth step depicted in Fig. 4.3 is employed both for nanowire thinning and gate oxide formation for the single top-gate devices. After the oxidation process, etch windows are patterned in source/drain contact areas and opened up by removing the oxide shell with buffered oxide etch (BOE) as displayed in the left panel of Fig. 4.14(a). Subsequently, source/drain contacts as well as the gate electrode are formed using the same method as discussed in section 4.2. Finally, silicidation is carried out at the same temperature (450 °C) in forming gas ambient (10 % H_2 in N_2) with reduced thermal cycling.

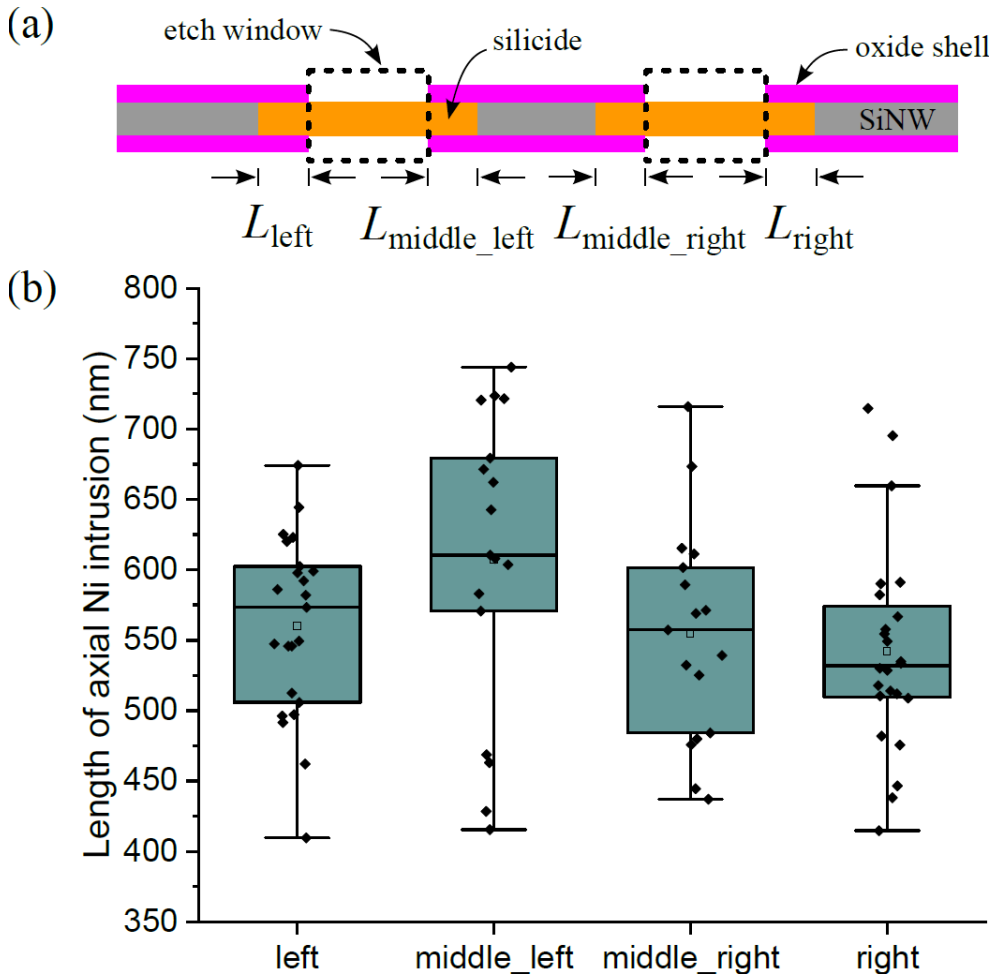


Figure 4.13: Axial diffusion of nickel along a SiNW in an oxide shell after thermal treatment at 450 °C for 300 s. Schematic of the device after selective removal of unreacted Ni (a). Silicide growth exhibits a broad distribution range of intrusion length (b). The mean intrusion length is approximately 550 nm.

To study the silicide growth behavior in an oxide shell, a test sample is deposited globally with Ni after opening source/drain contact windows as depicted in the left panel of Fig. 4.14(a). Note that the global deposition of Ni avoids alignment issues in an e-beam lithography process. After the silicidation process, unreacted Ni is selectively etched away in a Piranha solution ($H_2SO_4 : H_2O_2 = 4 : 1$). Similar to the growth behavior disscussed in the previous section and in Ref. [121], Ni diffusion in an oxide shell also exhibits a large statistical distribution of silicide length as depicted in Fig. 4.13. Fig. 4.14 shows three examples of Ni intrusion into a SiNW surrounded by an oxide shell. The mean intrusion length in a single-step annealing process at 450 °C for 300 s is approximately 550 nm and hence the growth speed is about half of that without an oxide shell (∼45 %).

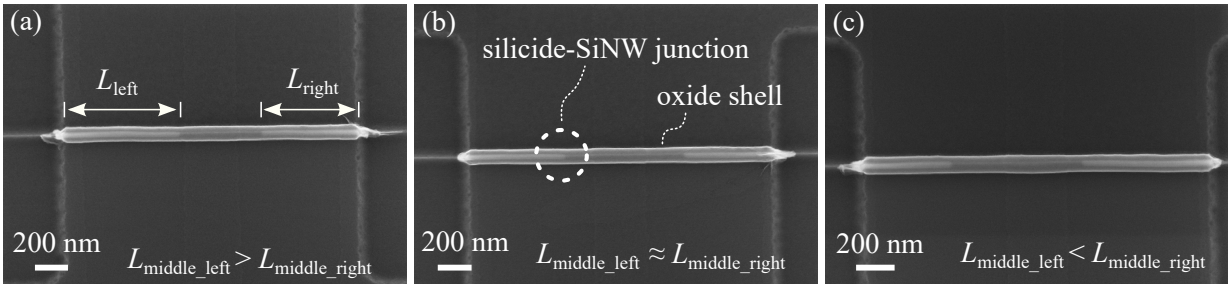


Figure 4.14: Scanning electron micrographs of three devices on the same chip after selective removal of unreacted Ni after the silicidation process at 450°C for 5 min. The Ni intrusion into a SiNW surrounded by an oxide shell in a single-step annealing process shows diverse silicide lengths, (a) $L_{middle\_left} > L_{middle\_right}$, (b) $L_{middle\_left} \approx L_{middle\_right}$, and (c) $L_{middle\_left} < L_{middle\_right}$.

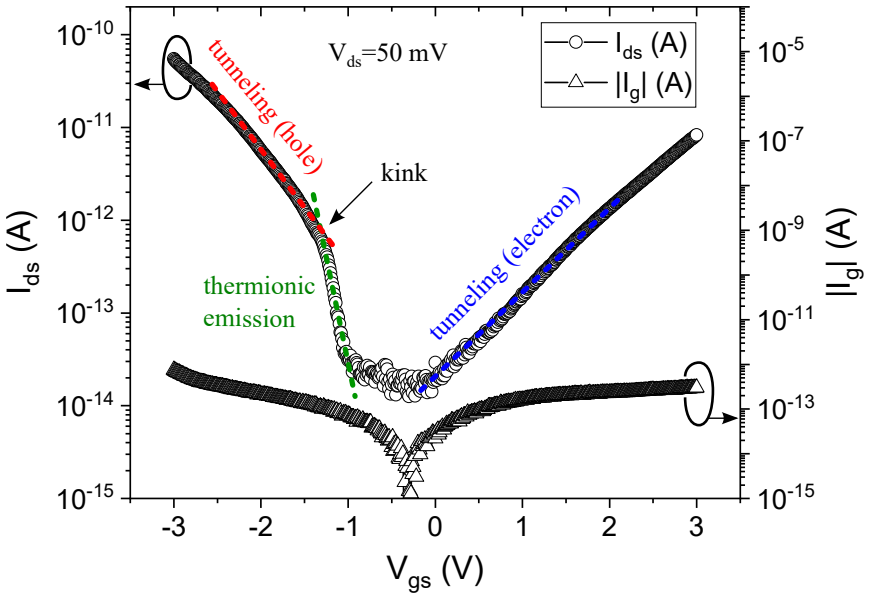


Figure 4.15: Transfer characteristic of a single top-gate Schottky-barrier MOSFET.

With the calculated mean intrusion length, the width of the single top-gate is designed to ensure a gate overlap and achieve a good electrostatic control of the channel as displayed in Fig. 4.12(b). Fig. 4.15 shows an experimental measurement result of such a single top-gate Schottky-barrier MOSFET. The transfer characteristic exhibits the typical ambipolar behavior and clearly the gate coupling factor is significantly improved compared to the back-gate device discussed in the previous section. Furthermore, a kink is clearly visible in the p- branch. Such a kink sets in when the carrier injection becomes dominated by tunneling through the Schottky-barrier as the gate voltage increases. Whereas such a kink is not visible for the n- branch, this means the Schottky barrier for hole injection is smaller than that for electron injection.

4.4 Dual-gate reconfigurable FETs

It has been discussed in the previous section that the typical ambipolar behavior of single top-gate Schottky-barrier MOSFETs leads to an increase in OFF-state leakage current. This is highly undesirable as the transistor can not function as a proper switch to turn the circuit ON/OFF in a logic circuit application. Recently, reconfigurable field-effect transistors (RFETs) have attracted an increasing attention because the ambipolar operation of a Schottky-barrier MOSFET can be suppressed by adding one or two additional gates to control the SBs at source/drain junctions electrostatically that allows substantial improvement in device performance [23, 24, 128, 129, 130]. In addition, the utilization of electrostatic doping for creating virtual n-/p- regions avoids dopant related issues. Moreover, RFETs can be switched to operate as unipolar n-type or unipolar p-type devices that allow more functionalities in a single circuit block and thus enabling a reduction of circuit topologies despite a more complex device architecture [25].

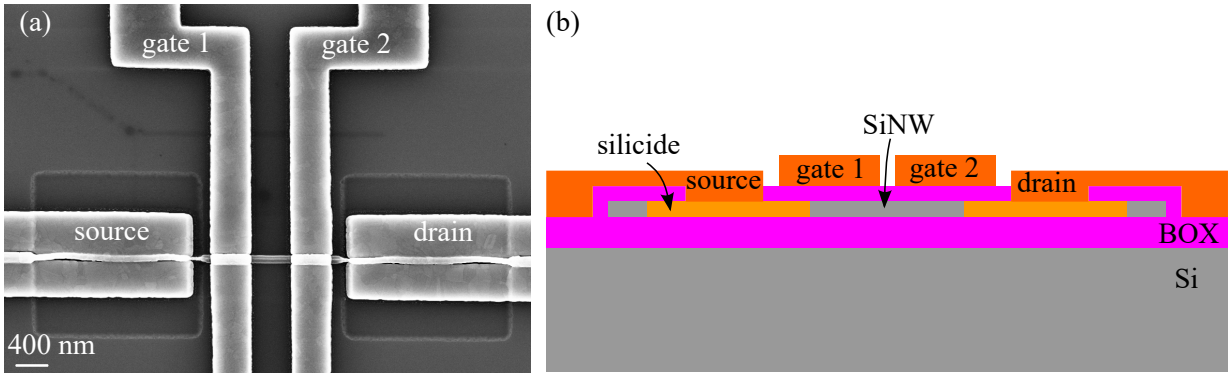


Figure 4.16: Scanning electron micrograph of a dual-gate reconfigurable FET (a). Cross-sectional schematic of the device along the nanowire.

It has been demonstrated that RFETs using triple gates, i.e., two gates for creating virtual source/drain regions and the third one for ON/OFF switching, could function as reconfigurable devices with high I_{ON}/I_{OFF} ratio and steep switching behavior [23, 128]. The

adoption of three gates will certainly need more space and might become a key limiting factor for downscaling. Hence, devices using only a dual-gate architecture have been investigated, too [24, 129, 130]. In these dual-gate devices, studies were focused on using the gate at the drain side for 'programming' the device either in n- or p- type configuration, while employing the gate at the source side to turn the device ON/OFF. Although unipolar device operation is obtained with this program gate at drain (PGAD) mode, the inverse subthreshold slope is significantly larger than the thermionic emission limit (i.e., $S > 60\,\mathrm{mV/dec}$). This is obvious since the RFET in PGAD mode is simply a Schottky-barrier MOSFET with suppressed ambipolar operation [37].

In this work, the rather overlooked device operation mode with the program gate at source (PGAS) is examined and compared with the PGAD. The fabrication process flow of dual-gate RFETs is similar to the single top-gate SB-MOSFETs discussed in the previous section. Fig. 4.16(a) shows a scanning electron micrograph of such a dual-gate RFET where the width of the two top-gates are designed to account for the statistical distribution of Ni intrusion in an oxide shell. Thus, excellent electrostatic control is achieved by creating an overlap of the Schottky-barriers at the drain and source sides as depicted in a cross-sectional schematic of the device shown in Fig. 4.16(b). It is worthwhile to note that only an estimation of the oxide thickness ($d_{\mathrm{ox}} > 15\,\mathrm{nm}$) and the diameter of SiNW ($d_{\mathrm{SiNW}} = \sim 25\,\mathrm{nm}$) is given mainly due to the different oxidation rates of the crystallographic planes of the initial triangular nanowire. In addition, the distance between two gates $L_{\mathrm{CG,PG}} = 450\,\mathrm{nm}$, distance between source and drain $L_{\mathrm{S,D}} = 2\,\mu\mathrm{m}$, width of each gate $L_{\mathrm{G}} = 500\,\mathrm{nm}$.

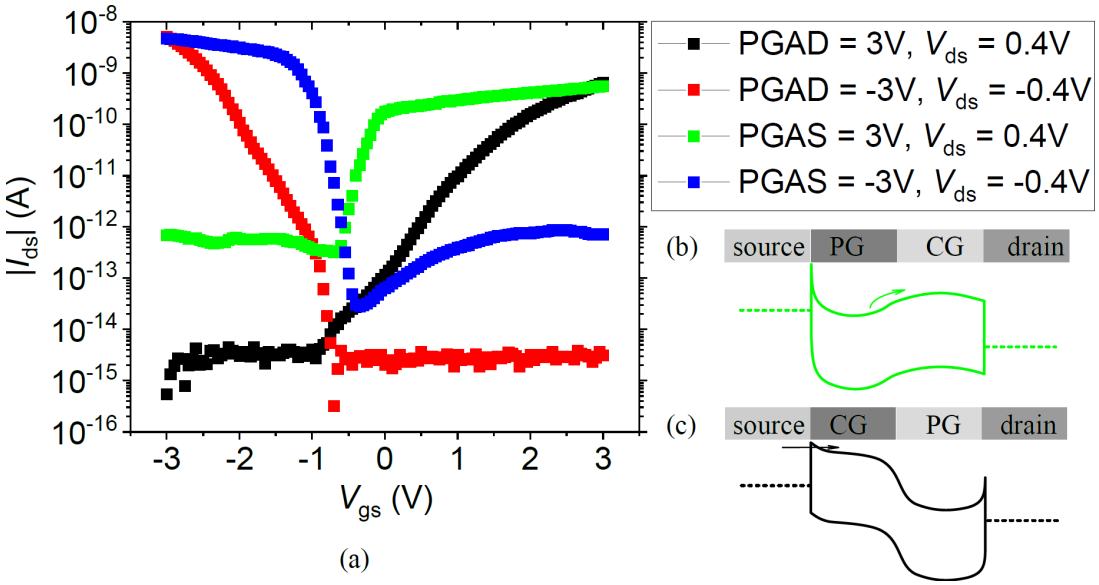


Figure 4.17: Transfer characteristics of the dual-gate RFET in PGAD and PGAS operation modes for both n- and p- type configuations (a). Band diagrams of the device in PGAS operation mode for n- type configuration (b) and in PGAD operation mode for n- type configuration (c). Gate leakage currents (I_{CG}, I_{PG}) are below $\sim 5{\times}10^{-15}\,\mathrm{A}$ and are not plotted for clarity.

Figure 4.17 shows transfer characteristics of the dual-gate RFET in PGAD and PGAS operation modes for both n- and p- type configuations with the same $|V_{\mathrm{PG}}|$ and $|V_{\mathrm{ds}}|$ values. Band diagrams in PGAS and PGAD operation modes for the n-type configuration are displayed in Fig. 4.17(b) and Fig. 4.17(c), respectively. It is observed that the OFF-state leakage current in PGAS is approximately two orders of magnitude higher than that for PGAD. In addition, the inverse subthreshold slope for the PGAS operation mode (n-type: green, p-type: blue) is substantially smaller than that for the PGAD (n-type: black, p-type: red). Furthermore, a kink in the p-branch of the PGAD operation mode (red curve) is observed similar to that of the single-top gate device shown in Fig. 4.15; the n-branch of the dual-gate RFET is, however, strongly suppressed due to the large negative voltage ($V_{\mathrm{PG}} = -3\,\mathrm{V}$) applied to the program gate at the drain side.

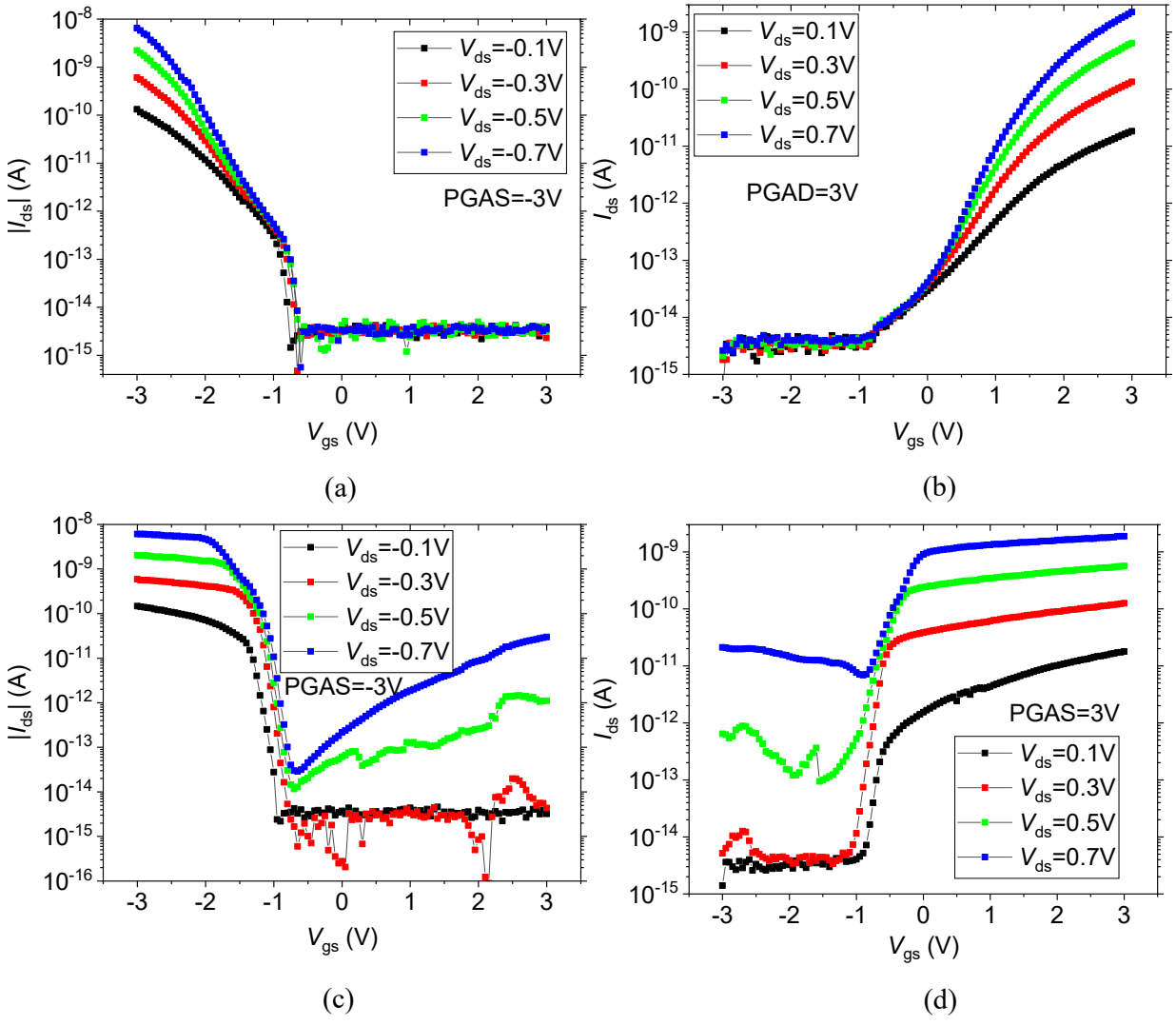


Figure 4.18: Transfer characteristics of an RFET for different drain source voltages in PGAD mode for p-type configuration (a), in PGAD mode for n-type configuration (b), in PGAS mode for p-type configuration (c), and in PGAD mode for n-type configuration (d).

In order to elaborate further on the difference in leakage current for these two operation modes, transfer curves are measured in PGAD and PGAS operation modes for both n- and p-type configurations with increasing V_{ds} values as depicted in Fig. 4.18. A current increase enabled by the modulation of the exit resistance at the drain side is observed for all cases. However, while in PGAD mode the leakage remains below the measurable threshold ($\sim 5 \times 10^{-15}$ A) due to the particular potential profile throughout the device, larger V_{ds} values lead to an exponential increase in leakage current in the PGAS mode as depicted in Fig. 4.18(c)-(d). The reason for this is that in PGAS mode, the ambipolar operation due to an increased carrier injection at the drain-side Schottky junction with increasing V_{ds} is not suppressed.

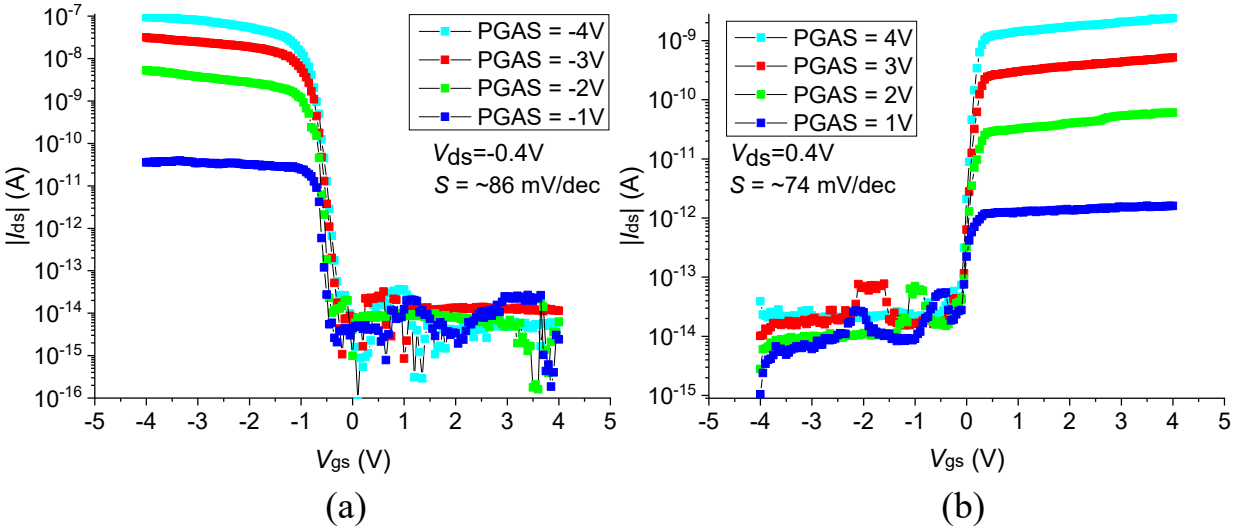


Figure 4.19: Transfer characteristics of an RFET for different program gate voltages in PGAS mode for p-type configuration (a), and in PGAS mode for n-type configuration (b).

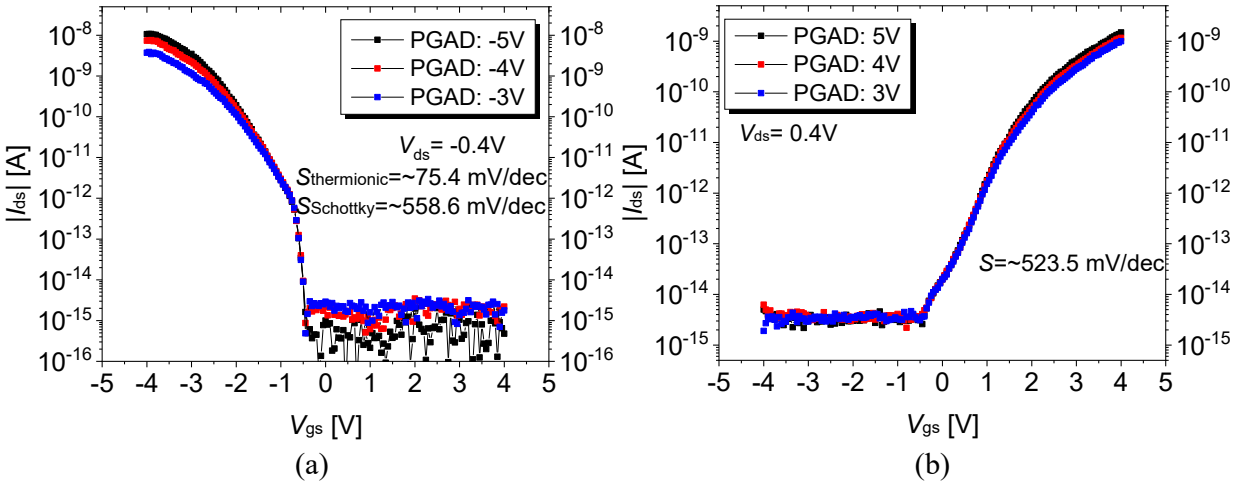


Figure 4.20: Transfer characteristics of an RFET for different program gate voltages in PGAD mode for p-type configuration (a), and in PGAS mode for n-type configuration (b).

Figure 4.19 shows transfer curves of an RFET in PGAS operation mode for both p-type (left panel) and n-type (right panel) configurations with increasing V_{PG} values. A virtual n-type source contact is created with a positive V_{PG} at the source side, and the behavior of the device is similar to a conventional n-type MOSFET in terms of a steep inverse subthreshold slope (i.e., close to 60 mV/dec). The ON-state current increases with a larger V_{PG} due to the increased carrier injection at the source-side Schottky junction.

Figure 4.20 shows transfer curves of an RFET in PGAD operation mode for both p-type (left panel) and n-type (right panel) configurations with increasing V_{PG} values. In this case, carrier injection through the source-side Schottky-barrier is modulated by different V_{CG} which makes the transistor behave similar to a conventional Schottky-barrier MOSFET. Therefore, the on-state current mainly remains constant even if a larger V_{PG} is applied at the drain side. The transition of carrier injection from thermionic emission to tunneling through the source-side Schottky-barrier is reflected in a kink in the transfer characteristic in Fig. 4.20(a). While such a kink is not visible for the n-type configuration in Fig. 4.20(b), it means that the Schottky-barrier for hole injection is smaller than that for electrons.

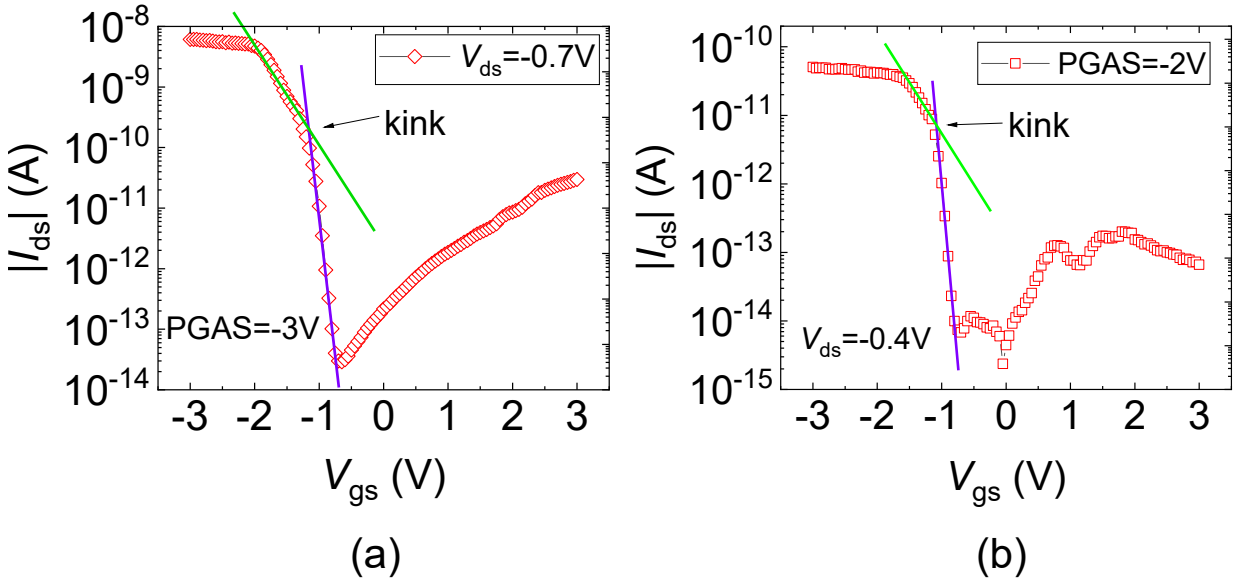


Figure 4.21: A kink in transfer characteristic of an RFET in PGAS operation mode may also appear for large V_{ds} (a) or small V_{PG} (b) values.

As it was mentioned before, a kink may appear in PGAD when carrier injection at source changes from thermionic emission to tunneling when increasing V_{CG} to more negative values (cf. Fig. 4.20(a)), a similar kink could also appear in the PGAS mode for large V_{ds} or small V_{PG} values as depicted in Fig. 4.21. The appearance of such a kink is due to the charge-mediated impact of V_{CG} on the potential distribution of the source-side Schottky-barrier: in the case of (a), an almost equilibrium distribution of holes is induced in the virtual p-type source contact if a large negative V_{PG} is applied at the source side. When the CG moves the valence band up, this gives rise to the steep switching of PGAS. However,

if the band under the drain-side CG is moved towards the source Fermi level, the carrier density within the virtual source contact is reduced due to the current flow into drain. As a result, the carrier density drops and the band in the virtual source can be moved further upwards giving rise to an increased tunneling through the source-side Schottky-barrier (see Ref. [25], chapter 7). Since this further increase of I_{ds} is due to tunneling, a kink occurs. A larger V_{ds} will lead to a larger V_{CG} range of the kink as is indeed observed experimentally (see e.g. Fig. 4.18(a)). However, it is important to mention that the kink only sets in, when the bands under drain-side CG are moved close to the Fermi level of source and hence a close to ideal inverse subthreshold slope is obtained over several orders of magnitude in the PGAS mode.

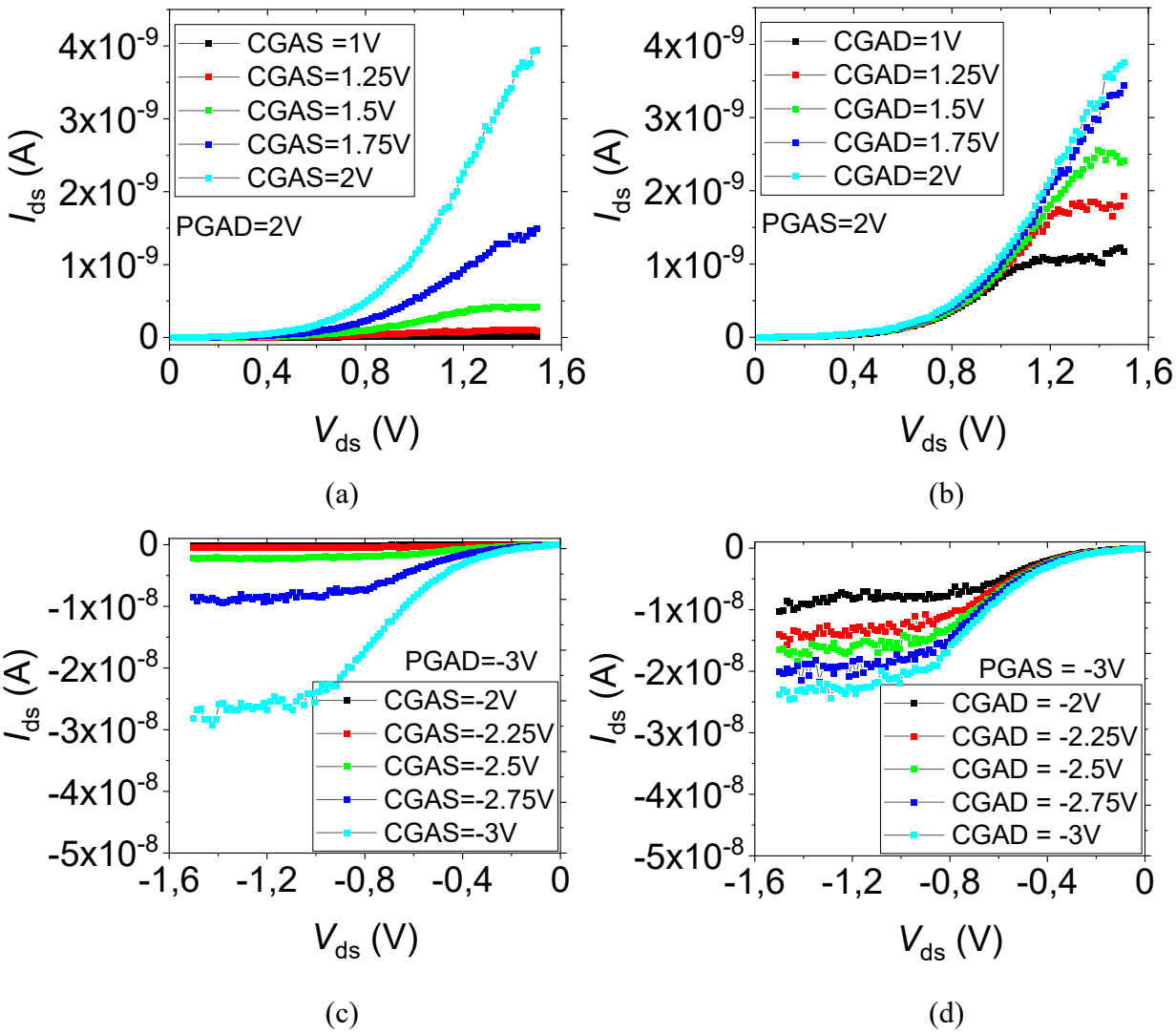


Figure 4.22: Output characteristics of an RFET for different control gate voltages in PGAD mode for n-type configuration (a), in PGAS mode for n-type configuration (b), in PGAD mode for p-type configuration (c), and in PGAS mode for p-type configuration (d).

Figure 4.22 shows output curves of an RFET in PGAD and PGAS operation modes for both n- and p-type configurations with increasing V_{CG} values. In the case of PGAD (left panels), a non-linear current increase in the triode regime is observed, typical of a Schottky-barrier MOSFET. In the PGAS mode, a non-linear current increase for small bias is also observed. However, in contrast to PGAD, an exponential increase is obtained that is almost the same for all CG voltages displayed in Fig. 4.22(b) and (d); a saturation of the current at different levels occurs only for V_{ds} larger than $\sim 1\,\mathrm{V}$. Both non-linearities, i.e. in PGAD and PGAS, might deteriorate the functionality of logic inverters built from those devices. This is particularly detrimental for the PGAS mode, leading to a complete loss of noise margin.

The different behavior of the output characteristics of the two device operation modes may at first be surprising since it is generally argued that the non-linearity of the I_d-V_{ds} curves stems from the forward biased drain-side Schottky junction [131, 132, 133]. But this is not the case as we will analyze below: while the non-linearity of the PGAS mode is indeed due to a forward-biased drain-side Schottky junction, the non-linearity of the PGAD mode is due to an increased tunneling through the source-side Schottky-barrier.

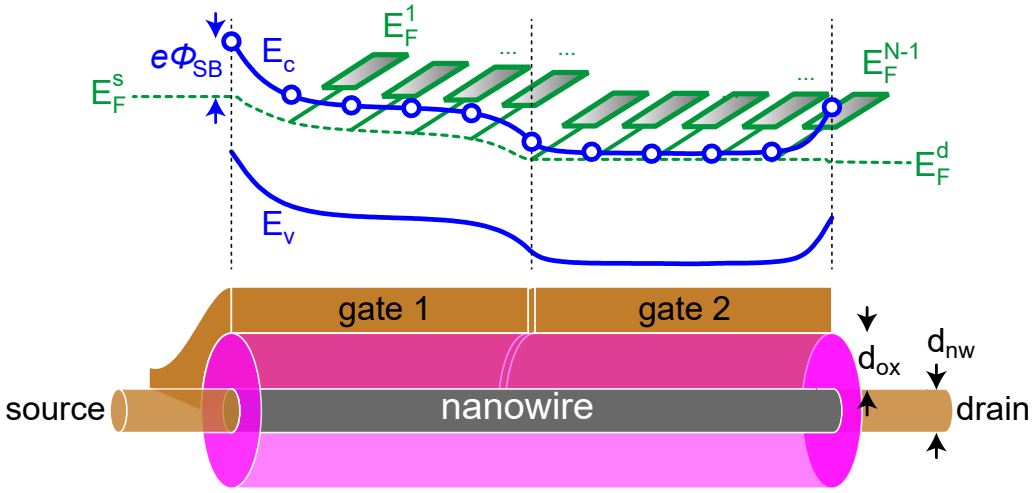


Figure 4.23: Schematic of the simulated dual-gate nanowire device (a). The top panel shows the conduction and valence bands (blue lines) on a finite difference grid. Buettiker probes are connected to each finite difference site with E_F^i representing the quasi Fermi level (green dashed line) through the device. For the simulation a device with $L = 100\,\mathrm{nm}$, $d_{nw} = 1\,\mathrm{nm}$, $d_{ox} = 10\,\mathrm{nm}$, $E_g = 1\,\mathrm{eV}$, $m^\star_{c,v}$=$0.1m_e$ and a scattering mean free path of 15 nm is assumed.

In order to elaborate further on the behavior of RFETs and in particular to understand the difference in the non-linear behavior of the PGAD and PGAS operation modes, self-consistent Poisson-Schrödinger simulations using the non-equilibrium Green's function formalism (NEGF) have been carried out[4] [25, 134]. An effective mass approximation with

[4]The NEGF simulations are carried out by Prof. Joachim Knoch

symmetric conduction and valence band is assumed; the complex band structure within the band gap is taken into account with Flietner's dispersion relation [135]. To reduce the computational burden, a nanowire FET with one-dimensional electronic transport with metallic contacts exhibiting a SB $\Phi_{\mathrm{SB}}^{\mathrm{s}}$ at the source and $\Phi_{\mathrm{SB}}^{\mathrm{d}}$ at the drain contact is considered as illustrated in Fig. 4.23. An undoped NW of diameter d_{nw} is assumed that is thin enough to justify one-dimensional (1D) electronic transport. The electrostatics of such a device can be described well by a 1D modified Poisson's equation (Eqn. (2.29)). The device architecture is accounted for with a proper choice of the screening length of $\lambda = \sqrt{\left(\frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}}\right) d_{\mathrm{nw}} d_{\mathrm{ox}}} = 1.83\,\mathrm{nm}$. Fermi level pinning with a midgap position of the source/drain Fermi level yielding a Schottky-barrier of $e\Phi_{\mathrm{SB}}^{\mathrm{n}} = e\Phi_{\mathrm{SB}}^{\mathrm{p}} = E_{\mathrm{g}}/2$ is assumed at the interface between source/drain and the channel; all other device parameters are stated in the caption of Fig. 4.23. Other simulation parameters are listed in the caption of Fig. 4.23. It is important to note that these assumptions will certainly not allow a quantitative comparison between experiment and simulation. However, qualitatively they replicate the experimental situation rather well and the approach has been used successfully to reproduce and explain the device behavior of conventional as well as Schottky-barrier field-effect transistors (see e.g. [136, 137]). An important ingredient here is the inclusion of Buettiker probes (cf. Fig 4.23), i.e. virtual contacts attached to the channel of the RFET that mimic inelastic scattering [138]; the Fermi levels of all Buettiker probes are determined to ensure a net zero current from/into each Buettiker probe thus representing the quasi Fermi level within the device (green dashed line). Note that the quasi-Fermi level is a reference energy level that reflects the charge carrier concentration in a nonequilibrium state [139].

Figure 4.24 shows simulated output characteristics in PGAD (upper panel) and PGAS (lower panel) operation modes for the n-type configuration, qualitatively reproducing the experimental results displayed in Fig. 4.22(a)-(b). It is observed that the non-linear current increase for small bias for the PGAS mode is more pronounced compared to that for PGAD. The reason for such a different behavior becomes obvious when comparing the quasi Fermi levels shown in the inset of Fig. 4.24(a) and (b): in PGAD, the quasi Fermi level at the drain end, i.e. underneath gate 2, drops substantially with increasing bias. This is due to a loss of carrier injection into the drain such that the conduction/valence bands are moved to lower energies because of the large V_{PG} at gate 2. As a result, the device does not behave like a forward biased Schottky junction. Opposed to this, the small non-linearity observed in PGAD (cf. Fig. 4.24(a)) stems from an increased tunneling through the source-side Schottky diode with increasing V_{ds} due to a significant reduction of the carrier density underneath the control gate. Note that the same is true in conventional, single-gate Schottky-barrier MOSFETs [25]. In contrast, in the case of PGAS (cf. Fig. 4.24(b)) the quasi Fermi level remains rather fixed by the source contact and increasing the bias yields a forward biased Schottky junction with an exponential increase of the current. This rather undesirable behavior strongly deteriorates, e.g., the performance of inverters made of RFETs operated in PGAS mode.

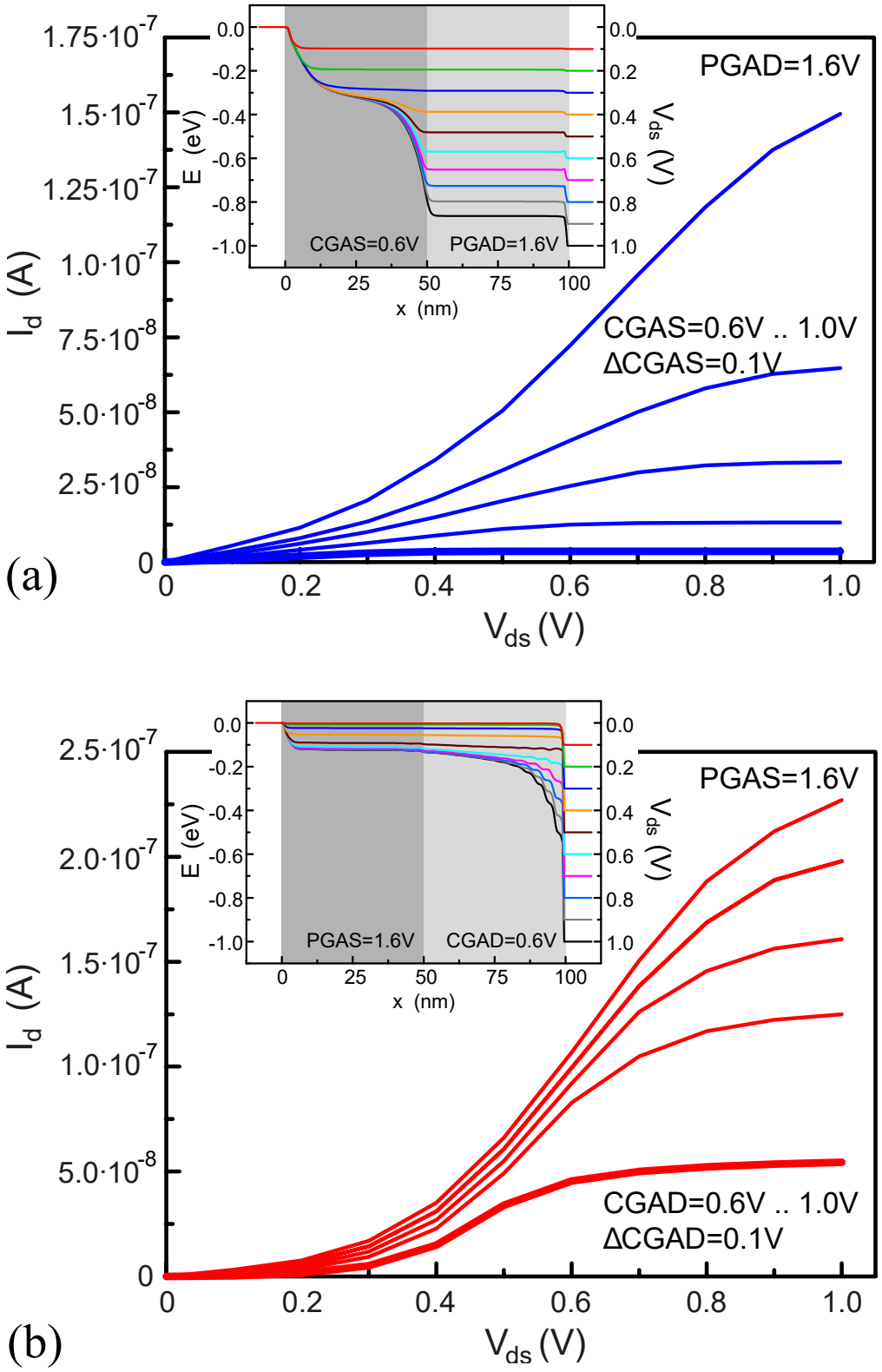


Figure 4.24: Simulated n-type output characteristics using NEGF approach for PGAD = 1.6 V, CGAS = 0.6-1.0 V (upper panel) and PGAS = 1.6 V, CGAD = 0.6-1.0 V (lower panel). The insets depict the quasi Fermi levels for $V_{ds} = 0.1, \ldots, 1.0$ V for both device operation modes.

It has been mentioned before that the kink formation in transfer characteristics of the PGAS operation mode is due to a feedback of carrier loss due to V_{CG} on the potential redistribution of the source-side Schottky barrier. While a similar feedback is also observed in the output characteristics of the PGAD operation mode, the sub-linear current increase in the triode operation regime of the dual-gate Schottky-barrier MOSFET is mainly due to a charge-mediated impact of increasing V_{ds}: an enhanced tunneling through the source-side Schottky barrier is enabled by a feedback where the bands are moved to lower energies due to a carrier loss in the channel with increasing drain-source bias.

Since each individual gate of the dual-gate Schottky-barrier MOSFET allows a flexible tuning of the effective Schottky barrier height at the drain-channel and the source-channel junctions, the behavior of the dual-gate Schottky barrier MOSFET could also be explained with simulation using a single top-gate architecture as depicted in Fig. 2.9 with varying Ψ^{s}_{SB} and Ψ^{d}_{SB} values.

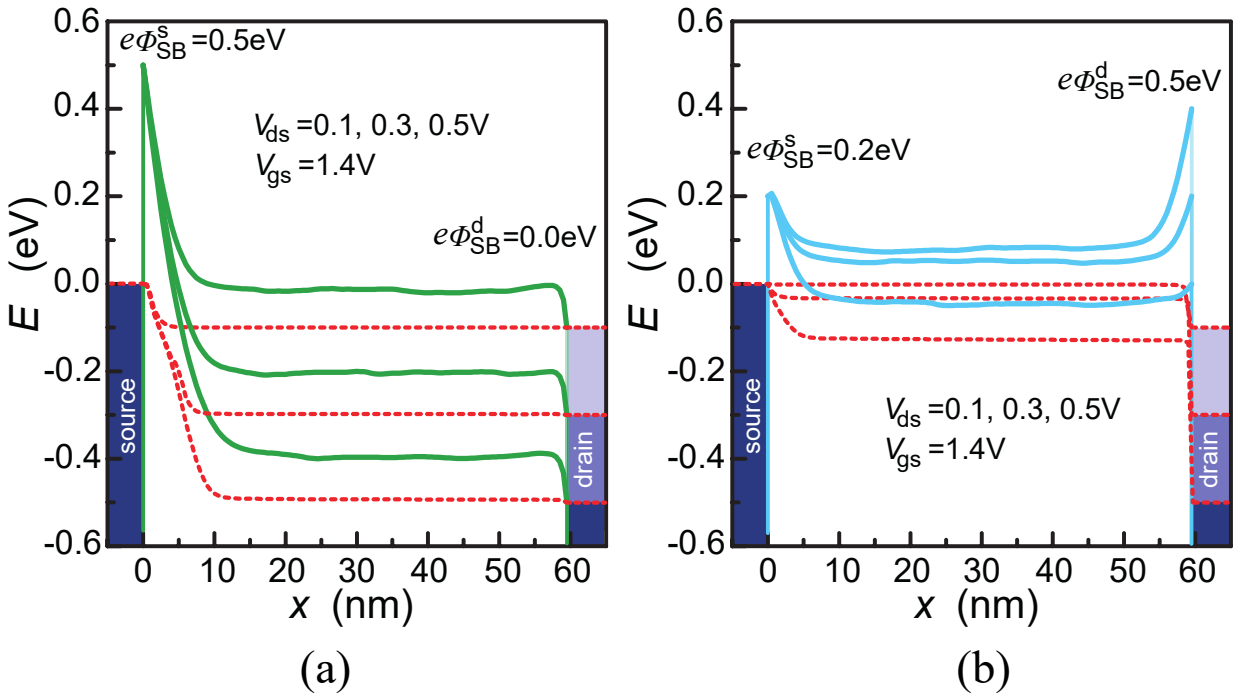


Figure 4.25: Band profiles (solid lines) and quasi Fermi level (dashed line) in the case of $\Psi^{s}_{SB} = 0.5\,\text{eV}$ and $\Psi^{d}_{SB} = 0\,\text{eV}$ (c), $\Psi^{s}_{SB} = 0.2\,\text{eV}$ and $\Psi^{d}_{SB} = 0.5\,\text{eV}$ (d) for varying V_{ds}.

Figure 4.25(a) shows conduction band profiles of a single top-gate SB-MOSFET under three V_{ds} values with $\Psi^{s}_{SB} = 0.5\,\text{eV}$ and $\Psi^{d}_{SB} = 0.0\,\text{eV}$, corresponding to the PGAD operation mode of the dual-gate SB-MOSFET. Note that only the n-type branch is presented here for simplicity purpose, although both electron and hole injection are considered in the simulation. A positve voltage applied at gate 2 ensures that the drain-side Schottky barrier is made rather thin and therefore the effective Schottky barrier height Ψ^{d}_{SB} is made smaller than Ψ^{s}_{SB}. It can be seen in Fig. 4.25(a) that the conduction band drops rather significantly

as V_ds increases. While such a behavior is often referred to as drain induced barrier lowering (DIBL) in conventional MOSFETs with a short channel length, the dependence of channel potential on V_ds in such a Schottky-barrier MOSFET is mediated by the charge within the channel in the device's ON state. As a result, this is not a consequence of short-channel effects (SCEs) and will also appear in long channel Schottky-barrier MOSFETs. In fact, the channel potential is both dependent on the gate bias V_gs and the drain-source bias V_ds even for a long-channel SB-MOSFET. Therefore, the impact of V_ds via channel charge on the potential distribution in the channel leads to a narrowing of the source-side Schottky barrier. As a consequence, the tunneling through the source-side Schottky barrier is increased and this gives rise to the sub-linear current increase in the triode operation regime of a dual-gate SB-MOSFET as depicted in Fig. 4.22(a) and the upper panel of Fig. 4.24.

On the other hand, Fig. 4.25(b) shows conduction band profiles of a single top-gate SB-MOSFET under three V_ds values with $\Psi_\mathrm{SB}^\mathrm{s} = 0.2\,\mathrm{eV}$ and $\Psi_\mathrm{SB}^\mathrm{d} = 0.5\,\mathrm{eV}$, corresponding to the PGAS operation mode of the dual-gate SB-MOSFET. A positve voltage applied at gate 1 makes the source-side Schottky barrier more transparent and therefore $\Psi_\mathrm{SB}^\mathrm{s} < \Psi_\mathrm{SB}^\mathrm{d}$. While the quasi-Fermi level is almost at the same level as the drain Fermi level in the case of PGAD (cf. Fig. 4.25(a)), the channel is almost in equilibrium with the source Fermi level in case of PGAS as depicted in Fig. 4.25(b). In this case, a substantial portion of the applied bias drops across the drain-side Schottky barrier. Hence, the device behaves more like a forward-biased Schottky diode at drain and this leads to the sub-linear behavior as depicted in Fig. 4.22(b) and the lower panel of Fig. 4.24.

4.5 Towards a linear $I_\mathrm{d} - V_\mathrm{ds}$ behavior of SB-MOSFETs

It has been shown in the previous section that the difference in output characteristics of the dual-gate Schottky-barrier MOSFET could also be well explained with the simulation of a single top-gate SB-MOSFET with varying $\Psi_\mathrm{SB}^\mathrm{s,d}$ values. Furthermore, in addition to the flexibility of choosing different $\Psi_\mathrm{SB}^\mathrm{s,d}$, the model allows changing various other simulation parameters to study their impact on device performance.

The sub-linear current increase in output characteristics of the triode operation regime is a rather undesirable behavior which leads to a loss in noise margin for inverters made of SB-MOSFETs. Up to now, it has been demonstrated that the two device operation modes of a dual-gate SB-MOSFET have their strengths and drawbacks. The PGAS operation mode yields an almost ideal switching behavior, however its output characteristics are deteriorated when compared to PGAD, which exhibits improved output but less ideal transfer characterisitics. Therefore, the PGAS operation mode is more favored for building an amplifier (due to a larger transconductance g_m) whereas the PGAD is more suitable for the implementation of an inverter (due to the less sub-linear $I_\mathrm{d} - V_\mathrm{ds}$ behavior). In the following, simulations are performed on a single top-gate nanowire transistor to find strategies for the optimization of SB-MOSFETs, in particular to achieve a linear $I_\mathrm{d} - V_\mathrm{ds}$

behavior.

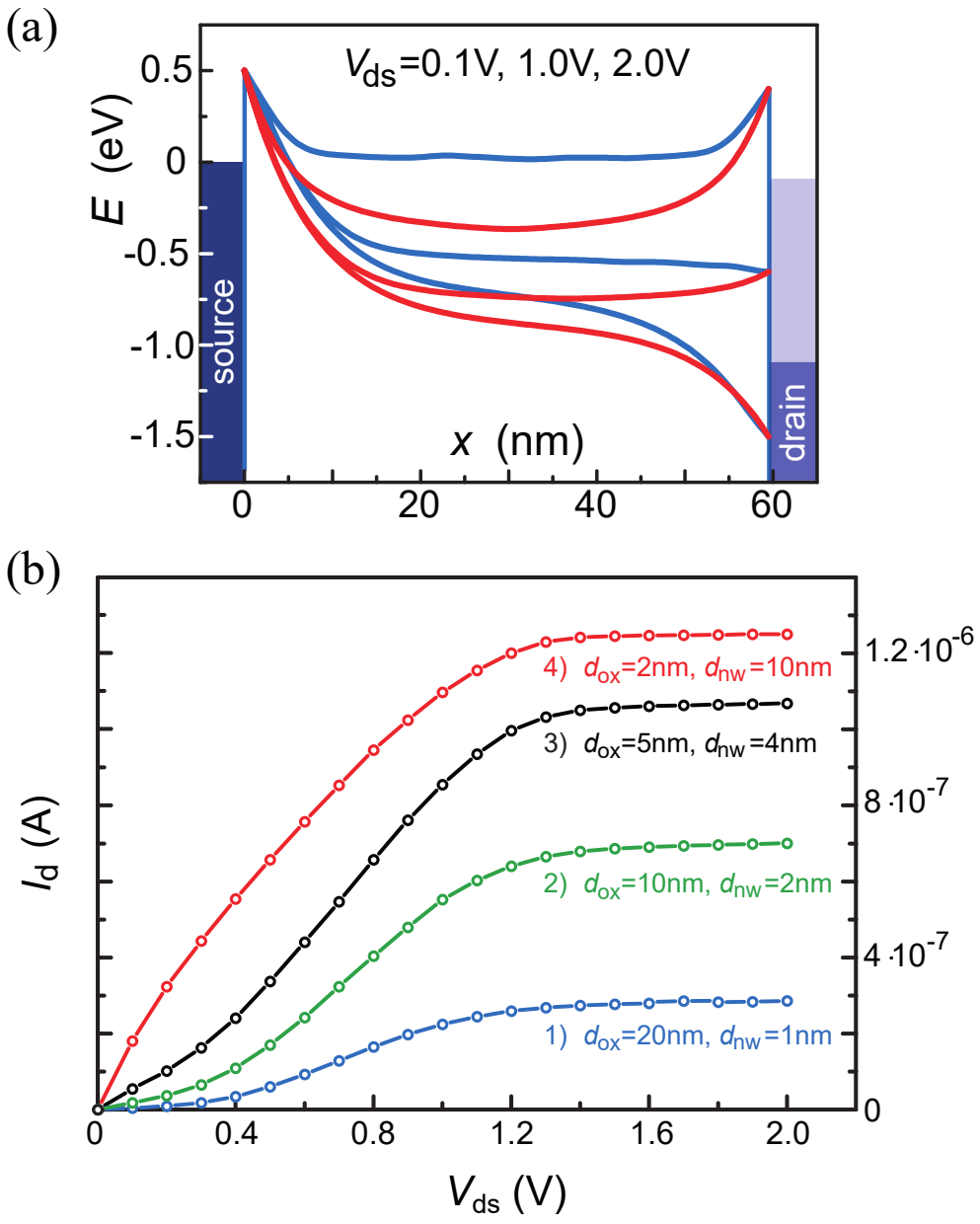


Figure 4.26: Simulation of a single top-gate nanowire SB-MOSFET with decreasing carrier density. Conduction band profiles with $d_{ox} = 20\,\text{nm}$, $d_{nw} = 1\,\text{nm}$ (blue) and $d_{ox} = 2\,\text{nm}$, $d_{nw} = 10\,\text{nm}$ (red) (a). Output characteristics of the SB-MOSFET with varying d_{nw}, d_{ox} resulting in the same screening length λ (b). Note that $V_{gs} = 1.4\,\text{V}$, $\Psi_{SB}^{s} = \Psi_{SB}^{d} = 0.5\,\text{eV}$, $m^{\star} = 0.05m_0$, $l_{mfp} = 50\,\text{nm}$, $V_{gs} = 1.4\,\text{V}$ and $L = 60\,\text{nm}$ are the parameters used for the simulation.

In the case of a single-gate nanowire FET as depicted in Fig. 2.9, 1D electronic transport is justified. An increase in d_{nw} yields a reduced carrier density if a constant charge

carrier density $n_{1\mathrm{D}}$ is assumed with carriers confined to the nanowire cross-section using a particle-in-a-box approximation. As a result, the wave function spreads across the nanowire cross-section leading to a reduction in carrier density ($n(x) \propto n^{1\mathrm{D}}/d_\mathrm{nw}^2$) for increasing d_nw if contributions from higher subbands of the nanowire are not taken into account. Furthermore, in order to rule out the impact of different device parameters [37] and to keep the transmission probability unchanged, d_ox and d_nw are changed leaving the screening length λ constant. To be specific, the following four devices are considered[5]: 1) $d_\mathrm{ox} = 20\,\mathrm{nm}$, $d_\mathrm{nw} = 1\,\mathrm{nm}$, 2) $d_\mathrm{ox} = 10\,\mathrm{nm}$, $d_\mathrm{nw} = 2\,\mathrm{nm}$, 3) $d_\mathrm{ox} = 5\,\mathrm{nm}$, $d_\mathrm{nw} = 4\,\mathrm{nm}$ and 4) $d_\mathrm{ox} = 2\,\mathrm{nm}$, $d_\mathrm{nw} = 10\,\mathrm{nm}$. Since a single-gate device architecture is considered, $\lambda = \sqrt{\frac{\varepsilon_\mathrm{nw}}{\varepsilon_\mathrm{ox}} d_\mathrm{ox} d_\mathrm{nw}} = 7.58\,\mathrm{nm}$ in all cases. In addition, since carrier density in the channel is proportional to the density of states which is proportional to $\sqrt{m^\star/E}$ for a 1D system, the effective mass is lowered from $m^\star = 0.2m_0$ to $m^\star = 0.05m_0$ in order to carve out the impact of the channel charge more clearly. Note that an increase of the effective band gap due to carrier confinement is neglected. The simulations are carried out for NW SB-MOSFETs with constant $\Psi_\mathrm{SB}^\mathrm{s} = \Psi_\mathrm{SB}^\mathrm{d} = 0.5\,\mathrm{eV}$. As it will be shown below, a linear $I_\mathrm{d} - V_\mathrm{ds}$ behavior can be achieved even if there is a substantial Schottky barrier present at the drain side.

Figure 4.26(b) shows output characteristics for the different d_nw and d_ox mentioned above. It is observed that an increasing sub-linear behavior develops if d_nw decreases. The reason for this is the increasing charge carrier density with decreasing d_nw, leading to a stronger charge-mediated impact of the potential distribution of the source-side SB with larger V_ds. In contrast, the carrier density becomes rather small in the case 4) and therefore, substantially less impact of the charge on the potential distribution is obtained which can also be observed in the conduction band profiles plotted in Fig. 4.26(a) by comparing the distances between neighbouring band profiles. As a result, in the case 4), the carrier density has become so small that linear output characteristics are obtained although a substantial Schottky barrier at the drain end exists. It is important to note that it is not an increased tunneling through the Schottky barrier (due to the low $m^\star$) that leads to the linear $I_d - V_\mathrm{ds}$ behavior, as evident from the sub-linearity of the device 1), but a strongly suppressed impact of the charge on the source-side Schottky diode. In fact, the device approaches from case 1) towards case 4) more and more the so-called quantum capacitance limit (QCL) [38, 25] which can be explained with the dependance of channel potential on the gate and

[5]It is observed in the 1-D modified Poisson's equation $\frac{\partial^2 \Phi_f(x)}{\partial x^2} - \frac{\Phi_f(x) - (\Phi_\mathrm{g} + \Phi_\mathrm{bi})}{\lambda^2} = -\frac{en(x)}{\varepsilon_0 \varepsilon_\mathrm{Si}}$ that the potential in the middle of the channel for a long-channel device where the curvature term $\frac{\partial^2 \Phi_f(x)}{\partial x^2}$ is approximately zero, the position of $\Phi_f(x)$ for a given Φ_g depends on the ratio of $\frac{d_\mathrm{ox}}{d_\mathrm{nw}}$ since $-(\Phi_f - (\Phi_g + \Phi_\mathrm{bi})) \approx -\frac{e^2 n^{1\mathrm{D}}/d_\mathrm{nw}^2}{\varepsilon_0 \varepsilon_\mathrm{nw}} \frac{\varepsilon_\mathrm{nw}}{\varepsilon_\mathrm{ox}} d_\mathrm{ox} d_\mathrm{nw} = -\frac{e^2 n^{1\mathrm{D}}}{\varepsilon_0 \varepsilon_\mathrm{ox}} \frac{d_\mathrm{ox}}{d_\mathrm{nw}}$. Furthermore, given the fact that the transmission probability T through a Schottky barrier calculated using the Wentzel-Kramers-Brillouin (WKB) approximation is proportional to $e^{-\lambda\sqrt{m^\star}}$ [25], parameters are designed in a way that d_ox is reduced while d_nw is increased while keeping the same $\sqrt{d_\mathrm{ox} d_\mathrm{nw}}$ (i.e. a constant λ to ensure the same transmission probability in all cases) in order to study the impact of the channel charge density on device behavior.

drain bias:

$$\delta\Phi_{\mathrm{S}}^{\max} = \frac{C_{\mathrm{ox}}^{\square}}{C_{\mathrm{ox}}^{\square} + C_{\mathrm{s,d}}^{\square} + C_{\mathrm{depl}}^{\square} + C_{\mathrm{it}}^{\square} + C_{\mathrm{q}}^{\square}}\delta\Phi_{\mathrm{g}} + \frac{C_{\mathrm{d}}^{\square}}{C_{\mathrm{ox}}^{\square} + C_{\mathrm{s,d}}^{\square} + C_{\mathrm{depl}}^{\square} + C_{\mathrm{it}}^{\square} + C_{\mathrm{q}}^{\square}}\delta\Phi_{\mathrm{d}}. \quad (4.1)$$

It is clear that the impact of drain bias is suppressed in a long-channel device where $C_{\mathrm{d}}^{\square}$ is significantly smaller than $C_{\mathrm{ox}}^{\square}$. The quantum capacitance $C_{\mathrm{q}}^{\square}$ (i.e. inversion layer capacitance) is defined as the change of the channel charge with changing surface potential [25]:

$$C_{\mathrm{q}}^{\square} = -e\frac{\partial Q_{\mathrm{inv}}^{\square}}{\partial\Psi_{\mathrm{S}}} = -e^2\int_{\Psi_{\mathrm{S}}}^{\infty} D(E)\frac{\partial f(E+\Psi_{\mathrm{S}}-E_{\mathrm{F}}^{\mathrm{S}})}{\partial\Psi_{\mathrm{S}}}dE \approx e^2 D_{\mathrm{eff}}(E_{\mathrm{F}}^{\mathrm{S}} - \Psi_{\mathrm{S}}). \quad (4.2)$$

Note that the derivative of the Fermi distribution function is a delta function. Eqn. (4.2) shows that the quantum capacitance $C_{\mathrm{q}}^{\square}$ is proportional to the density of states. In the case of a nanowire architecture, the density of states $D(E)$ decreases with increasing energy (i.e. $D(E) \propto \sqrt{m^{\star}/E}$ for a 1D system). As a result, the oxide capacitance $C_{\mathrm{ox}}^{\square}$ can be made significantly larger than $C_{\mathrm{q}}^{\square}$ by scaling down the oxide thickness d_{ox}. Therefore, the factor of the first term in Eqn. (4.1) approaches unity (i.e. $C_{\mathrm{ox}}^{\square}/C_{\Sigma}^{\square} \approx 1$) and therby a one-by-one dependence of channel potential on gate bias can be achieved. In this case, the so-called quantum capacitance limit is obtained where the position of the band is entirely determined by the gate potential while the impact of drain bias is suppressed.

In conclusion, the operation of the single top-gate nanowire SB-MOSFET is similar to that of the dual-gate RFET operated in PGAD (cf. Fig. 4.24(a)): First, an almost equilibrium distribution of charge carriers is induced in the channel when V_{ds} is close to 0. As V_{ds} increases, an increased tunneling through the source-side SB which is mediated by the impact of V_{ds} via carrier density on channel potential gives rise to a sub-linear behavior in output characteristics. In this case, the channel potential is both dependent on the gate bias V_{gs} and the drain-source bias V_{ds} even for a long-channel SB-MOSFET. The sub-linear behavior can be suppressed by scaling down the size of the nanowire and the oxide thickness to approach the quantum capacitance limit where the potential in the channel is fully dependent on the gate bias. Indeed, it has been demonstrated experimentally that a linear $I_d - V_{\mathrm{ds}}$ behavior can be achieved for highly scaled devices [130, 140, 141, 142]. For a large V_{ds}, charge carrier density in the channel has dropped significantly and hence the source-side SB stays mostly unchanged for a certain gate bias even if V_{ds} further increases, leading to a saturation of the current. Since the operation of the dual-gate reconfigurable transistor in PGAD mode is similar to that of a single top-gate device with a reduced Schottky barrier height at the drain side, approaching the quantum capacitance limit could lead to a performance improvement of the dual-gate RFET to obtain a linear $I_{\mathrm{d}} - V_{\mathrm{ds}}$ behavior.

Chapter 5

Summary and Outlook

In the present thesis, dual-gate reconfigurable FETs with wet chemically etched SiNWs and Ni silicidation are fabricated and characterized.

The top-down fabrication approach using a two-step TMAH etching yields localized silicon nanowires with atomically flat surfaces and minimal plasma damage manufacturable with conventional h-line contact lithography. After the fabrication of silicon nanowires with triangular cross-section, a wet chemical treatment in 40 % NH_4F could further develop the {111} facet into a clean and atomically ordered surface. The key of this process is to remove the dissolved oxygen in the solution which could reoxidize the surface and induce etch pits. Next, a hydrogen annealing step at a high temperature and reduced pressure can be optionally used to further improve the surface roughness and transform the cross-section of the silicon nanowire from a triangle into a circle while maintaining its cross-sectional area. In particular, a simulation tool based on the level-set method is designed to simulate such a shape transformation process. After the silicon nanowire fabrication, a dry oxidation step is carried out to grow gate oxide and reduce the cross-sectional size. After removing the oxide shell in source/drain areas, nickel contacts are fabricated using a bilayer PMMA resist, the modified e-beam evaporation setup, and lift-off. The modified evaporation setup equipped with two permanent magnets and a hollow, metallic cylinder allows avoiding the irradiation of electrons and ions on PMMA, yielding near perfect deposition results and hence significantly improved fabrication yield and device performance. In the end, a silicidation process is carried out to finalize the fabrication of dual-gate RFETs.

The dual-gate architecture allows operating the device in two different operation modes. In PGAD mode, the reconfigurable FET is a Schottky-barrier MOSFET with suppressed ambipolar behavior. The price paid for a lower off-state leakage current and more unipolar device behavior is a larger inverse subthreshold slope. Whereas in PGAS, the RFET demonstrates a steeper inverse subthreshold slope comparable to a state-of-the-art conventional MOSFET. However, V_{ds} should be kept low to prevent leakage increase induced by the other carrier type.

The kink observed in transfer characteristics of the PGAD mode for p-type configuration indicates that the silicide created from the one-step silicidation process at 450 °C exhibits a Fermi level close to the valance band of silicon. On the other hand, the kink in transfer characteristics of the PGAS operation mode is due to the charge-mediated impact of V_{CG} on the potential distribution of the source-side Schottky-barrier.

The charge-mediated impact also has an impact on the output characteristics of the PGAD operation mode. In this case, a sub-linear increase of the drain current as a function of V_{ds} in the PGAD operation mode is observed: When V_{ds} is increased, the charge in the channel is strongly reduced from the equilibrium value to a value proportional to the transmission probability through the source Schottky-barrier. In turn, the reduced charge yields an increased gate impact and hence a larger carrier injection from source. This results in the typical sub-linear output characteristics of SB-MOSFETs even if the drain Schottky-barrier is very small since the large V_{PG} applied at gate 2 ensures that the drain SB is made rather thin thereby increasing the tunneling probability through it (i.e., $\Psi_{\mathrm{SB}}^{\mathrm{d}}$ is reduced). On the other hand, the more pronounced sub-linearity in output characteristics for the PGAS operation mode is due to the forward-biased Schottky-diode at the drain side.

The dual-gate reconfigurable nanowire transistor operated in PGAS is more favored for building an amplifier due to its larger transconductance. In PGAD, it is more suitable for the implementation of logic circuits such as an inverter due to its less sub-linear $I_{\mathrm{d}} - V_{\mathrm{ds}}$ behavior compared with PGAS. The simulation using a non-equilibrium Green's function method reveals that a linear characteristic can be achieved in PGAD by approaching the so-called quantum capacitance limit even if there is a substantial Schottky barrier present at the drain side. In this limit, the charge in the channel is irrelevant and the channel potential is solely determined by the gate bias. The quantum capacitance limit can be reached by scaling down the oxide thickness (i.e. large $C_{\mathrm{ox}}^{\square}$) using a nanowire architecture (i.e. small $C_{\mathrm{q}}^{\square}$ due to $D(E) \propto \sqrt{m^{\star}/E}$ for 1D transport).

Future work might include:

- incorporate the NH_4F treatment and hydrogen annealing processes in device fabrication and compare device performance. To simplify the fabrication as much as possible, these two processes are not employed in the present thesis. In particular, the hydrogen annealing process could facilitate a wrap-gate or Ω-gate which features a smaller screening length, yielding an improved performance compared with the current Λ-shaped gate architecture;

- carry out cryogenic measurements of the dual-gate RFET to study the transistor behavior at low temperatures;

- carry out experiments and simulations for tri-gate RFETs;

- build simple logic circuits such as an inverter, NAND gate, etc.

Appendix

I. Process parameters for triangular SiNW fabrication

1. Starting material

Step	Description	Tool	Parameters
1	starting material		specifications of the silicon-on-insulator substrate: · diameter=12" · top-Si=∼80 nm · BOX=∼145 nm · (100)-oriented · ρ=13.5–22.5 Ω·cm · doping type: boron · doping concentration = 1×10^{15} atoms/cm^3
2	cleaving	diamond scriber	1/4 of the 12" wafer is prepared with a diamond scratch and cleaving method, the cleavage follows <110> directions
3	spin coating	HMDS oven/spin coater/hot plates	1. dehydration: 135 °C, 5 min 2. HMDS coating: 135 °C, N_2 bubbler, P<1 bar 3. sample cooling: cool on cold plate for 30 s 4. apply AZ5214E, 3000 rpm for 30 s 5. pre-bake @ 95 °C for 90 s
4	dicing	Disco DAD321	dice the 1/4 wafer along cleaved edges into 15 mm×15 mm sample pieces
5	strip resist	wet bench	1. boiling acetone: 10 min 2. boiling IPA: 5 min 3. DI water rinse 4. N_2 blow dry
		Oxford Plasmalab PRS90	O_2 plasma ashing · power=250 W, O_2 flow=40 %, duration=60 min

2. RCA-clean

Step	Description	Tool	Parameters
6	organics removal	RCA wet benches	1. piranha solution: H_2SO_4 : H_2O_2 = 4 : 1, 10 min 2. DI water rinse 10 min
7	wet oxide removal		1. 1 % HF till surface is hydrophobic 2. DI water rinse 10 min
8	organics and particle removal		1. SC-1: H_2O : NH_4OH : H_2O_2 = 5 : 1 : 1, 10 min 2. DI water rinse 10 min
9	wet oxide removal		1. 1 % HF till surface is hydrophobic 2. DI water rinse 10 min
10	metallic impurity removal		1. SC-2: H_2O : HCl : H_2O_2 = 6 : 1 : 1, 10 min 2. DI water rinse 10 min 3. N_2 blow dry

3. Marker definition

Step	Description	Tool	Parameters
11	spin coating	HMDS oven/spin coater/hot plates	1. dehydration: 135 °C, 5 min 2. HMDS coating: 135 °C, N_2 bubbler, P<1 bar 3. sample cooling: cool on cold plate for 30 s 4. apply AZ5214E, 3000 rpm for 30 s 5. pre-bake @ 95 °C for 90 s
12	exposure	MA/BA6 (SÜSS MicroTec)	1. exposure: vacuum contact mode, 15 mW/cm^2, h-line (405 nm), 2 s 2. image reversal bake @ 115 °C for 2 min 3. flood exposure for 10 s
13	development	wet bench	development: · AZ726MIF, 36 s · DI water rinse, 10 min · N_2 blow dry
14	dry etch	PlasmaPro 100 Cobra	SF_6=37.5 sccm, O_2=11 sccm, P=15 mTorr, RF power=20 W, t=10 min (target depth=2.4 μm)
15	strip resist	wet bench	1. boiling acetone: 10 min 2. boiling IPA: 5 min 3. DI water rinse 4. N_2 blow dry
		Oxford Plasmalab PRS90	O_2 plasma ashing · power=250 W, O_2 flow=40 %, duration=60 min

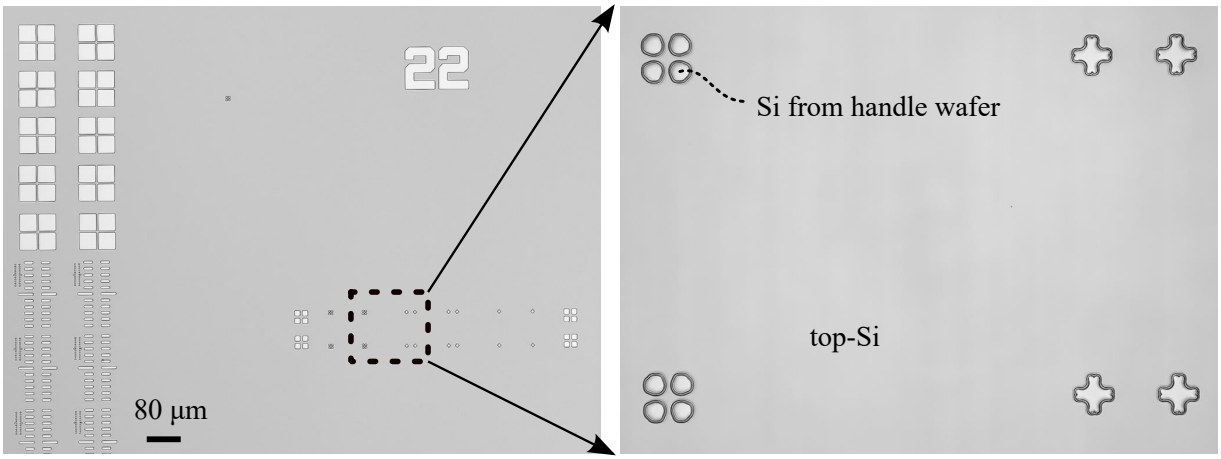


Figure 1: Laser microscope images of sample surface after resist removal. (b) is a zoom-in view of the area framed by dashed rectangle shown in (a).

4. Thermal nitridation

Step	Description	Tool	Parameters
16	organics removal	RCA wet benches	1. piranha solution: H_2SO_4 : H_2O_2 = 4 : 1, 10 min 2. DI water rinse 10 min
17	wet oxide removal		1. 1 % HF till surface is hydrophobic 2. DI water rinse 10 min
18	organics and particle removal		1. SC-1: H_2O : NH_4OH : H_2O_2 = 5 : 1 : 1, 10 min 2. DI water rinse 10 min
19	wet oxide removal		1. 1 % HF till surface is hydrophobic 2. DI water rinse 10 min
20	metallic impurity removal		1. SC-2: H_2O : HCl : H_2O_2 = 6 : 1 : 1, 10 min 2. DI water rinse 10 min 3. N_2 blow dry
21	wet oxide removal		1. 1 % HF till surface is hydrophobic 2. DI water rinse 10 min 3. N_2 blow dry
22	thermal nitridation	Annealsys AS-One 150	T=1050 °C, NH_3 flow=2000 sccm, P=1 bar, duration=250 s

5. Line structure patterning

Step	Description	Tool	Parameters
23	PMMA coating	spin coater/hot plates	1. dehydration: 150 °C, 5 min 3. sample cooling: cool on cold plate for 30 s 4. apply PMMA resist AR 679.02, 2000 rpm for 60 s 5. pre-bake @ 150 °C for 5 min
24	EBL	Raith 150-Two	e-beam exposure: · aperture 10 μm · acceleration voltage (EHT) 20 keV · beam current ca. 32 pA · area step size (U=V) 4 nm · beam speed ~5.4mm/s · area dose 150 μAs/cm^2 · dose factor 1.2
25	development	wet bench	development: · MIBK : IPA = 30 ml : 90 ml, 30 s · dip in IPA for 15 s · N_2 blow dry

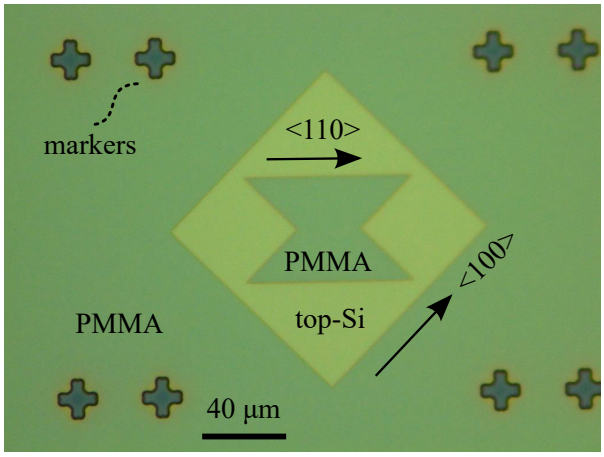


Figure 2: An optical microscope image of the sample surface after patterning PMMA resist.

6. Open hardmask and 1st TMAH etch

Step	Description	Tool	Parameters
26	dry etch	PlasmaPro 100 Cobra	CHF_3=19 sccm, O_2=2 sccm, P=10 mTorr, RF power=10 W, t=30 s
27	strip PMMA	Oxford Plasmalab PRS90	O_2 plasma ashing · power=250 W, O_2 flow=40 %, duration=60 min
28	1st TMAH etch	wet bench fume hood / hot plate	native oxide removal: · 1 % HF (∼15 s) · quick dump rinse in DI water
			etch in a TMAH/IPA mixture @ 80 °C for 25 s · TMAH (25 %) 100 ml, IPA 20 ml, 80 °C, magnetic stirrer 200 rpm · DI water rinse, 10 min · N_2 blow dry

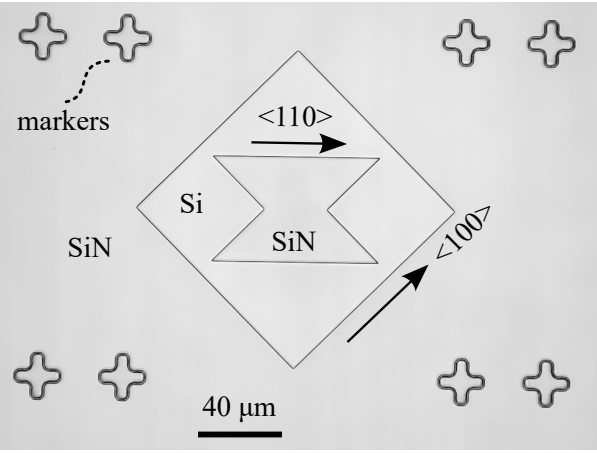


Figure 3: An laser microscope image of the sample surface after the first TMAH etch step.

7. Local oxidation (sidewall passivation)

Step	Description	Tool	Parameters
29	organics and particle removal	RCA wet benches	1. SC-1: $H_2O : NH_4OH : H_2O_2 = 5 : 1 : 1$, 10 min 2. DI water rinse 10 min
30	wet oxide removal		1. 1 % HF till surface is hydrophobic 2. DI water rinse 10 min
31	metallic impurity removal		1. SC-2: $H_2O : HCl : H_2O_2 = 6 : 1 : 1$, 10 min 2. DI water rinse 10 min 3. N_2 blow dry
32	dry oxidation	Annealsys AS-One 150	target thickness ∼20 nm · T=1100 °C, O_2 flow=2000 sccm, P=1 bar, duration=180 s

8. 2nd TMAH etch

Step	Description	Tool	Parameters
33	nitride hardmask removal	PlasmaPro 100 Cobra	oxynitride removal: · SF_6=40 sccm, O_2=10 sccm, P=10 mTorr, RF power=20 W, t=10 s
		wet bench	hot H_3PO_4 acid (85 %), 150 °C, duration=10 min
34	2nd TMAH etch	wet bench fume hood / hot plate	native oxide removal: · 1 % HF ∼10 s · quick dump rinse in DI water
			etch in a TMAH/IPA mixture @ 80 °C for 25 s · TMAH (25 %) 100 ml, IPA 20 ml, 80 °C, magnetic stirrer 200 rpm · DI water rinse, 10 min · N_2 blow dry
35	BOE etch	wet bench	local oxide removal: · BOE solution (7:1), ∼15 s

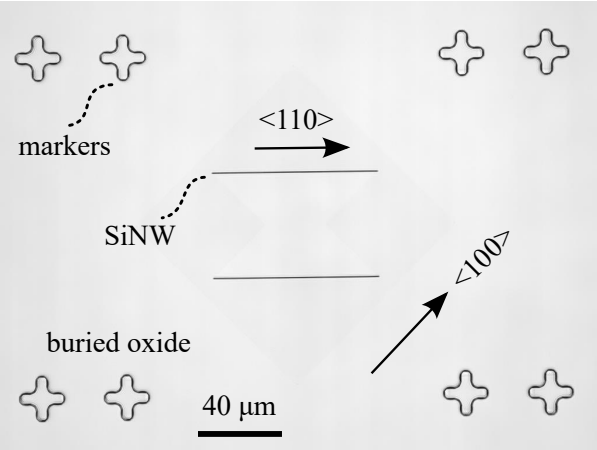


Figure 4: A laser microscope image of the sample surface after the second TMAH etch step.

II. Other process recipes

KOH etching recipe

Step	Description	Tool	Parameters
1	prepare KOH solution	wet bench (non-CMOS compatible) / hot plate	prepare 40 % KOH solution saturated with IPA: mix 89.81 g (assay 86.1 %) KOH pellets with 100 ml H_2O, temperature rises up to ∼120 °C right after mixing. Mix the solution with 20 ml IPA until temperature drops to ∼72 °C, temperature drops to ∼70 °C and keep stirring the mixture
2	KOH etching	wet bench (non-CMOS compatible) / hot plate	native oxide removal: · 1 % HF ∼10 s · quick dump rinse in DI water
			· etch in the prepared KOH solution @ 70 °C for 60 s · DI water rinse, N_2 blow dry

Bilayer PMMA patterning for lift-off

Step	Description	Tool	Parameters
1	PMMA coating	spin coater/hot plates	1. dehydration: 150 °C, 5 min 3. sample cooling: cool on cold plate for 30 s 4. apply PMMA resist AR 639.04, 4000 rpm for 60 s 5. pre-bake @ 150 °C for 5 min 6. sample cooling: cool on cold plate for 30 s 7. apply PMMA resist AR 679.04, 4000 rpm for 60 s 8. pre-bake @ 150 °C for 5 min
2	EBL	Raith 150-Two	**e-beam exposure for thin wires:** (7.5 μm aperture) · acceleration voltage (EHT) 20 keV · area dose 100 μAs/cm^2 · dose factor 1.8 · tune area step size to ensure beam speed < 10mm/s **e-beam exposure for thin wires:** (120 μm aperture) · aperture 120 μm · acceleration voltage (EHT) 20 keV · area dose 100 μAs/cm^2 · dose factor 2.8 · tune area step size to ensure beam speed < 10mm/s
3	development	wet bench	development: · MIBK : IPA = 30 ml : 90 ml, 42 s · dip in IPA for 15 s, N_2 blow dry

Image-reversal optical lithography process with AZ5214E™

Step	Description	Tool	Parameters
2	AZ5214E™ spin coating	HMDS oven/spin coater/hot plates	1. dehydration: 135 °C, 5 min 2. HMDS coating: 135 °C, N_2 bubbler, P<1 bar 3. sample cooling: cool on cold plate for 30 s 4. apply AZ5214E, 3000 rpm for 30 s 5. pre-bake @ 95 °C for 90 s
3	exposure	MA/BA6 (SÜSS MicroTec)	1. exposure: vacuum contact mode, 15 mW/cm^2, h-line (405 nm), t_1 s 2. image reversal bake @ 115 °C for 2 min 3. flood exposure for t_2 s
3	development	wet bench	development: · AZ726MIF, 36 s · DI water rinse, 10 min, N_2 blow dry

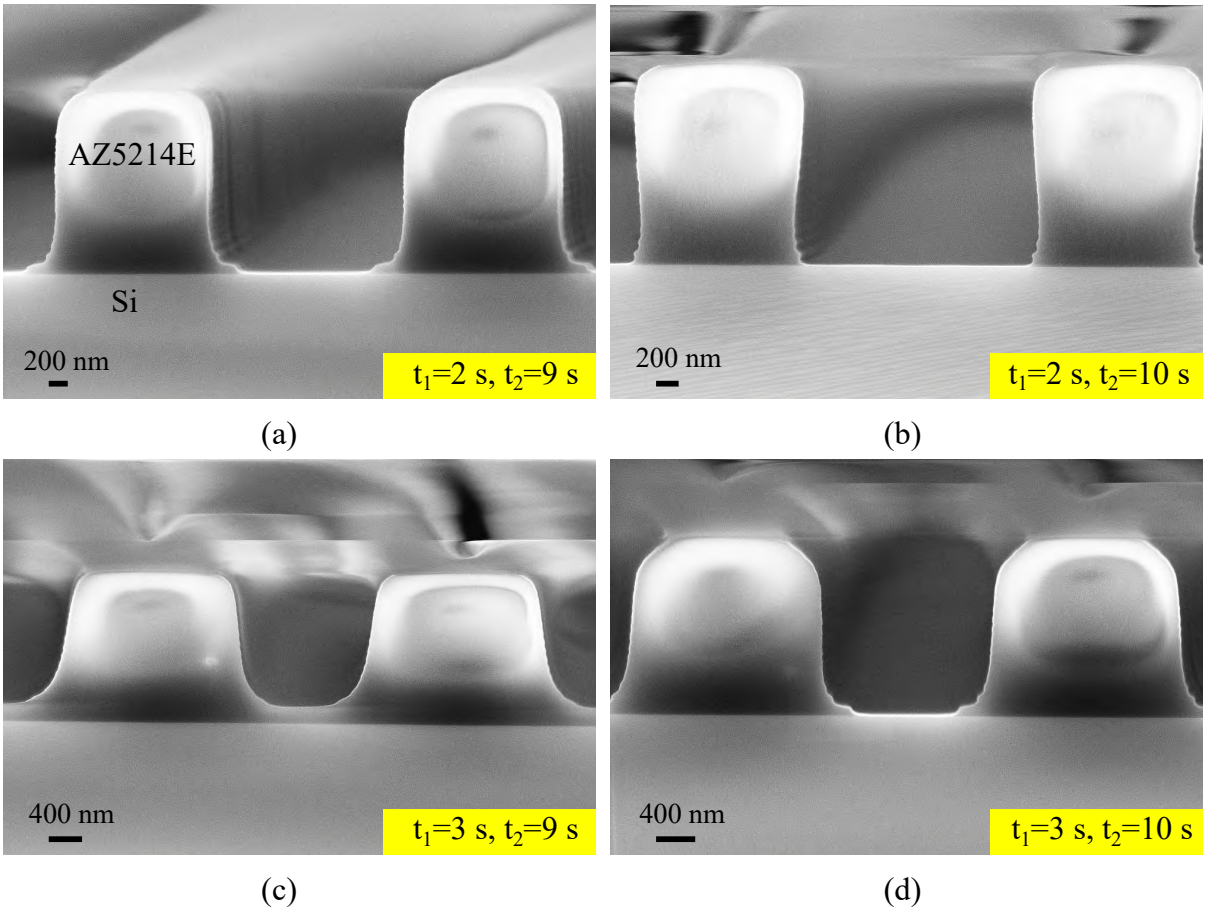


Figure 5: Image-reversal lithography process with AZ5214E™ using different exposure dose. Note that the UV lamp power is 15 mW/cm^2.

It is worthwhile to note that AZ5214E™ is a versatile photoresist that can change from positive-tone to image reversal by performing a so-called image-reversal bake and a subsequent flood exposure step. This versatility is enabled by adding a small amount of base additives, e.g. amine salts, to diazonaphthoquinone (DNQ) novolac based resists through the process of decarboxylation [143]. The amine salts decompose at an elevated temperature and neutralize the carboxylic acid produced during the first exposure. A flood exposure then follows to release carboxylic acid and hence increase its solubility in developer for the area which was covered by the mask during the first exposure. Resist patterns produced from the image-reversal lithography feature an inwardly sloped sidewall (cf. Fig. 5(b)) which is favored for a lift-off process.

Positive optical lithography process with AZ5214E™

Step	Description	Tool	Parameters
2	AZ5214E™ spin coating	HMDS oven/spin coater/hot plates	spin coating: 1. dehydration: 135 °C, 5 min 2. HMDS coating: 135 °C, N_2 bubbler, P<1 bar 3. sample cooling: cool on cold plate for 30 s 4. apply AZ5214E, 3000 rpm for 30 s 5. pre-bake @ 95 °C for 90 s
3	exposure	MA/BA6 (SÜSS MicroTec)	exposure: · 15 mW/cm^2 · h-line (405 nm) · vacuum contact mode · duration 6 s
3	development	wet bench	development: · AZ726MIF, 36 s · DI water rinse, 10 min, N_2 blow dry

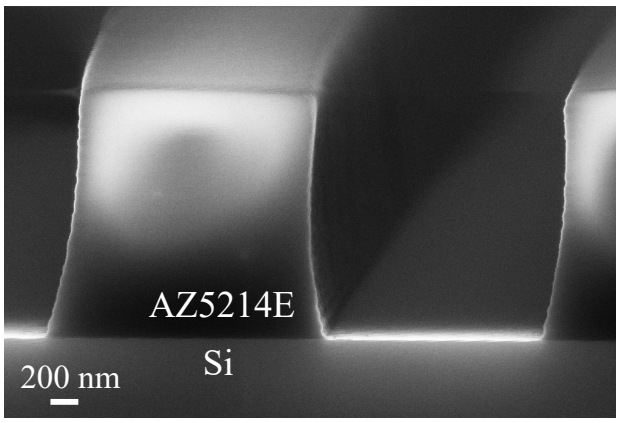


Figure 6: Positive lithography process with AZ5214E™.

Bosch™ high aspect ratio (HAR) etching process

The Bosch™ process is an alternating sequence of SF_6 and octafluoro cyclobutane (C_4F_8) etching and sidewall passivation steps to create high aspect ratio structures in silicon. The result shown in Fig. 7 is processed by two steps where the power and duration are increased in the etching cycle of step 2 to enhance the attack of passivation layer with increasing depth.

Step	Description	Tool	Parameters
1	Bosch™ HAR etching	Oxford ICP Etcher (PlasmaPro 100 Cobra)	50 iterations of: · deposition: 25 mTorr, 1500 W ICP, 5 W HF[6], -5 °C C_4F_8: 180 sccm, SF_6: 10 sccm, 2 s · etching: 40 mTorr, 1800 W ICP, 20 W HF, -5 °C C_4F_8: 10 sccm, SF_6: 200 sccm, 2200 ms
2			80 iterations of: · deposition: 25 mTorr, 1500 W ICP, 5 W HF, -5 °C C_4F_8: 180 sccm, SF_6: 10 sccm, 2 s · etching: 40 mTorr, 1800 W ICP, **25** W HF, -5 °C C_4F_8: 10 sccm, SF_6: 200 sccm, **2300** ms

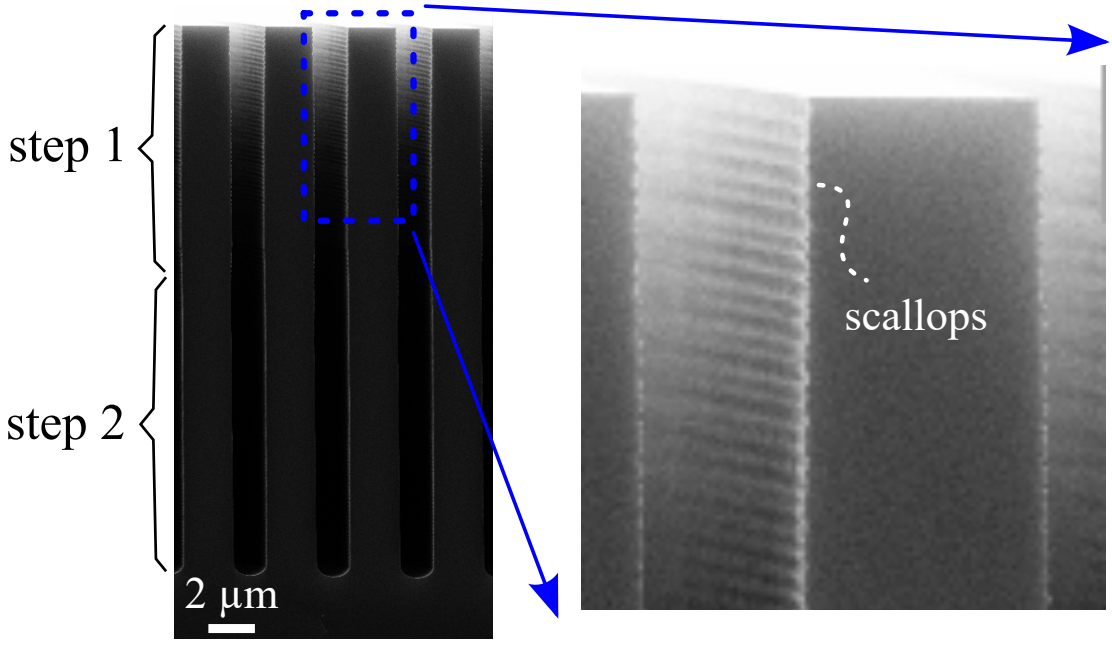


Figure 7: Cross-sectional scanning electron micrograph of a grating structure etched by the Bosch™ process. A close-up of the sidewall shows typical scallops of the Bosch™ etching process.

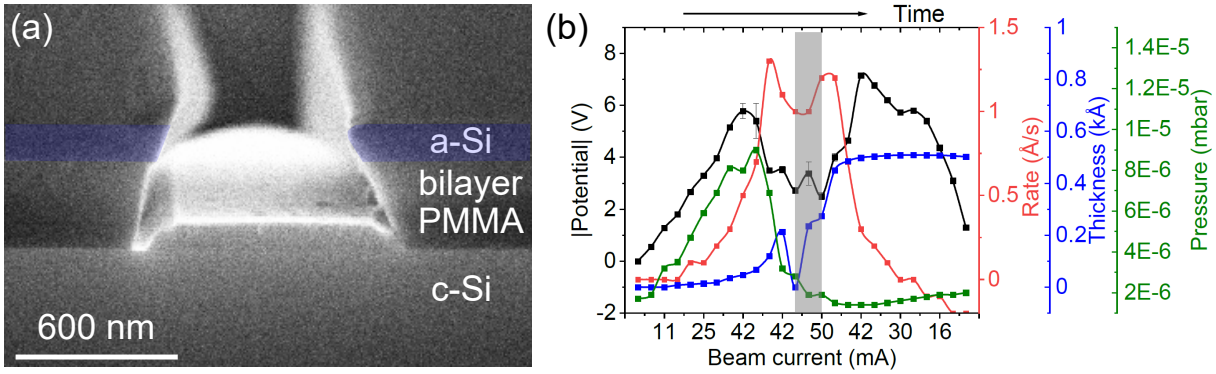
[6]Note that the 'HF' here differs from the abbreviation for "hydrofluoric acid", it refers to the radio frequency (13.56 MHz) power of an RF generator.

III. Evaporation of other materials

Evaporation and potential measurements are also carried out for a variety of other materials using the magnets/cylindrical electrode setup depicted in Fig. 3.23 at a moderate evaporation rate of ∼1 Å/s. Left panels in Fig. 8 show cross-sectional scanning electron micrographs of the evaporation results and the right panels show their corresponding potential measurements as well as other deposition parameters. It is clear that the resist profile remains intact after the evaporation, which facilitates solvent attack from the undeposited inwardly tapered sidewalls.

Potential measurements on a passive cylindrical electrode[7] reveal that almost all materials exhibit an 'M'-shaped potential profile like the case for Pt as depicted in Fig. 3.25. Moreover, the maximum potential measured is found to be strongly correlated with the atomic number of the material due to an increased backscattering of the electron beam from the target material. For some of the materials, e.g. Si, Hf, TiO_2, and Al_2O_3, the measured potential further increases or reaches a plateau with increasing evaporation rate. This can be explained with different ionization degrees for different materials. However, for most of the tested materials, a potential drop is observed during the switching of the shutter after reaching the desired evaporation rate.

In conclusion, despite the difference in material properties, the modified evaporation setup equipped with magnets and the passive cylindrical electrode using a moderate evaporation rate (∼1 Å/s) is very effective in avoiding any irradiation with charged particles, yielding an almost ideal evaporation scheme for a variety of materials commonly used in micro- and nanofabrication.



[7]Magnets are also used in this measurement setup as indicated in Fig. 3.23. Note that the beam current is changed in steps of ∼5 mA during the beam ramp up/down with a stabilization time of ∼30 s - 45 s. Therefore, the x-axis can also be interpreted as a time axis. It is observed that the measured potential value is dependent on the position of the beam spot and whether wobbling is used. Therefore, the potential measurements are carried out with a static spot centered at the crucible regardless of the material used.

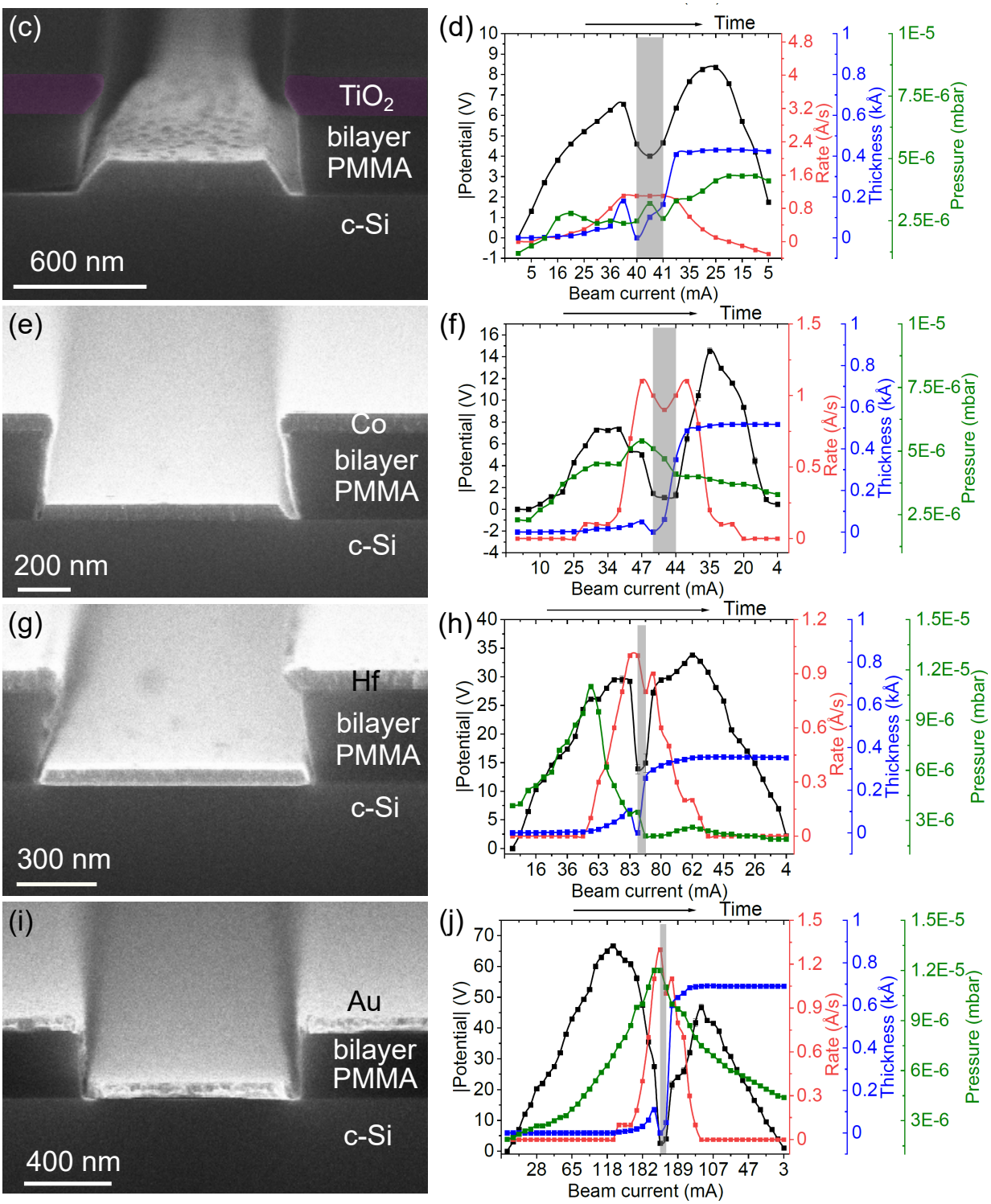


Figure 8: Evaporation results and potential measurements of some other commonly used materials in micro- and nanofabrication using the modified setup with magnets and a passive cylindrical electrode at an evaporation rate of 1 Å/s for amorphous Si (a)-(b), TiO_2 (c)-(d), Co (e)-(f), Hf (g)-(h), Au (i)-(j).

IV. Third-order TVD Runge-Kutta scheme

Instead of updating ϕ with the conventional first-order finite difference method, the application of the third-order total-variation-diminishing (TVD) Runge-Kutta time discretization scheme offers good shock transitions and a higher numerical approximation accuracy in smooth regions [84]. The level-set equation for surface diffusion is rewritten as:

$$\frac{\partial \phi}{\partial t} + \zeta \Delta_{\mathrm{s}} \kappa |\nabla \phi| = \frac{\partial \phi}{\partial t} + L(\phi) = 0. \tag{1}$$

The third-order TVD Runge-Kutta scheme approximates the level-set equation by surface diffusion Eqn. (1) as follows:

$$\begin{aligned} \phi^{(1)} &= \phi^{\mathrm{n}} + \Delta t L\left(\phi^{\mathrm{n}}\right), \\ \phi^{(2)} &= \phi^{\mathrm{n}} + \frac{1}{4}\Delta t \left[L\left(\phi^{\mathrm{n}}\right) + L\left(\phi^{(1)}\right)\right], \\ \phi^{\mathrm{n}+1} &= \phi^{\mathrm{n}} + \frac{1}{6}\Delta t \left[L\left(\phi^{\mathrm{n}}\right) + L\left(\phi^{(1)}\right) + 4L\left(\phi^{(2)}\right)\right]. \end{aligned} \tag{2}$$

V. Surface density of silicon atoms

Silicon belongs to group IV in the periodic table and it has a diamond crystal structure. The surface density of atoms is important, e.g., for determining how another material such as an insulator, will ''fit'' on the surface of a semiconductor material [144]. In addition, surface atoms provide the so-called ''dangling bonds'' that play an important role for the functionality of MOSFETs [25].

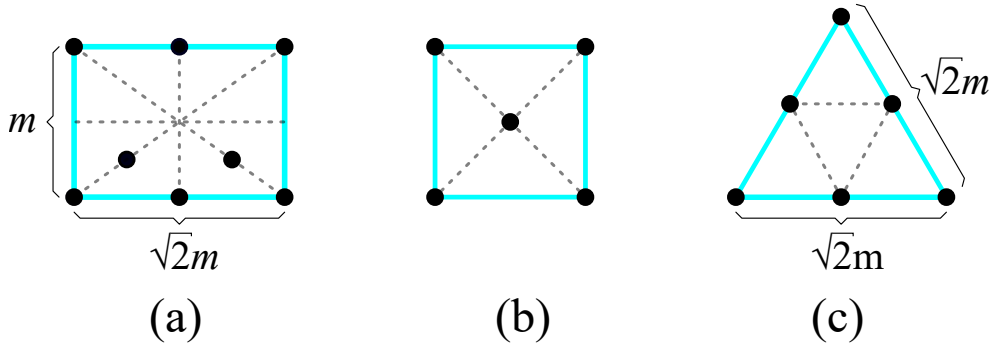


Figure 9: Silicon atoms in a unit cell of the diamond structure cut by the (110) plane (a), by the (100) plane (b), and by the (111) plane (c).

Figure 9 shows how the silicon atoms in a unit cell is cut by the (110), (100), and (111) planes, respectively. The lattice constant of the unit cell is m =5.43 Å. The surface density of silicon atoms on the (110) plane as depicted in Fig. 9(a) is calculated as follows: the atom at each corner of the rectangle (framed in cyan) is shared by four equivalent lattice planes. Therefore, each corner atom contributes 1/4 of its area to the (110) lattice plane. Similarily, each silicon atom at one side of the rectangle contributes 1/2 of its area and the remaining two silicon atoms inside the rectangle completely belong to the (110) lattice plane. The surface density of silicon atoms on the (110) lattice plane is then

$$n_{\mathrm{S}}^{(110)} = \frac{\text{number of atoms per lattice plane}}{\text{area of lattice plane}} = \frac{4\times\frac{1}{4}+2\times\frac{1}{2}+2}{\sqrt{2}m^2} \approx 9.6\times10^{14}\,\frac{\text{atoms}}{\text{cm}^2}. \quad (3)$$

The surface density of atoms for a (100) plane is calculated as

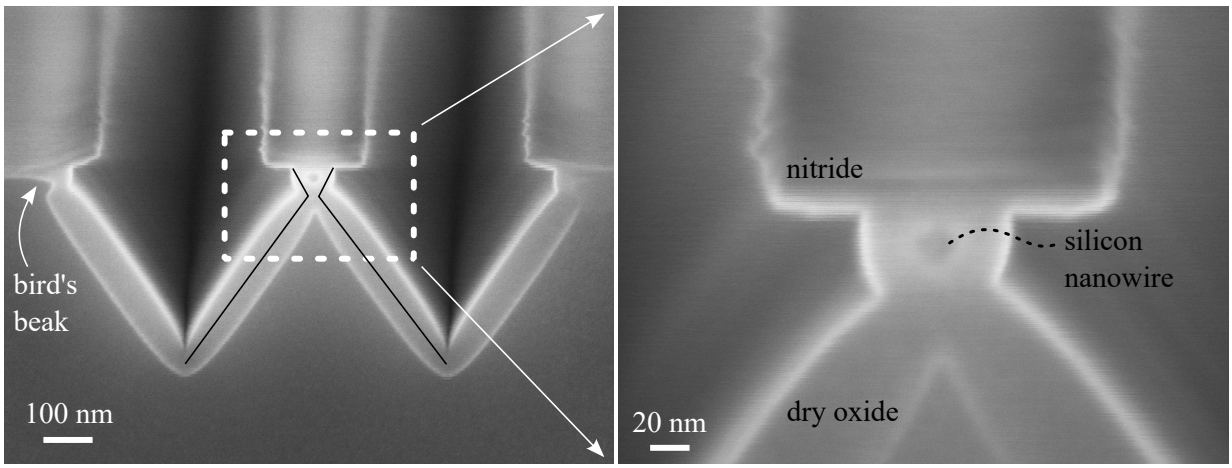
$$n_{\mathrm{S}}^{(100)} = \frac{4\times\frac{1}{4}+1}{m^2} \approx 6.8\times10^{14}\,\frac{\text{atoms}}{\text{cm}^2}. \quad (4)$$

Similarily, the surface density of atoms for a (111) plane is calculated as

$$n_{\mathrm{S}}^{(111)} = \frac{3\times\frac{1}{6}+3\times\frac{1}{2}}{\frac{\sqrt{3}}{4}\times(\sqrt{2}m)^2} \approx 7.8\times10^{14}\,\frac{\text{atoms}}{\text{cm}^2}. \quad (5)$$

VI. Oxidation of triangular silicon Nanowires

The cross-sectional scanning electron micrograph of the triangular silicon nanowire after oxidation is not shown in section 4.2. To further elaborate on the strain-induced oxidation behavior, V-groove structures are patterned with TMAH etching and a subsequent dry oxidation process is carried out at 1000 °C (800 mbar, 2000 sccm O_2 flow rate). The handstanding triangular silicon nanowire is formed due to slight over-etching of the SiN hardmask. Therefore, part of the silicon underneath the SiN hardmask is attacked and a sandglass-shaped structure bounded by four {111} planes is formed after the TMAH etching as indicated by the black solid lines depicted in Fig. 10(a). The left part of the V-groove displayed in Fig. 10(a) shows oxygen diffusion through the silicon-nitride interface, forming the so-called ''bird's beak'' and leading to an up-bending of the SiN hardmask. The close-up of silicon nanowire area (framed by white dashed rectangle) in Fig. 10(b) shows how compressive strain in concave corners in combination with oxygen diffusion through the silicon-nitride interface leads to the formation of a silicon nanowire with quasi-circular cross-section.



(a) (b)

Figure 10: Oxidation of a handstanding triangular silicon nanowire. The solid line in black color in (a) indicates the initial shape after TMAH etching and a close-up of the silicon nanowire area is shown in (b).

VII. Reduction of line edge roughness

The line edge roughness of resist patterns from a lithography process could be transferred to the layer beneath via subsequent etching steps. This is often undesirable since a rough surface could lead to deteriorated device performance. For example, charge carriers flow at the oxide/silicon interface in a field-effect transistor, a rough surface would hence lead to a degradation in charge carrier mobility. In the present thesis, a short treatment in O_2 plasma and a hardbake of resist pattern are carried out to reduce the line edge roughness prior to a subsequent SF_6/O_2 dry etching process as depicted in Fig. 11. It is clear that the etched surface still demonstrate certain roughness (see Fig. 11(a)-(b)) even after 10 min of O_2 plasma treatment. However, a smooth etched surface could be obtained as depicted in Fig. 11(c)-(d) if a hardbake of the resist pattern at 150 °C for 5 min is carried out in combination with a short O_2 plasma treatment.

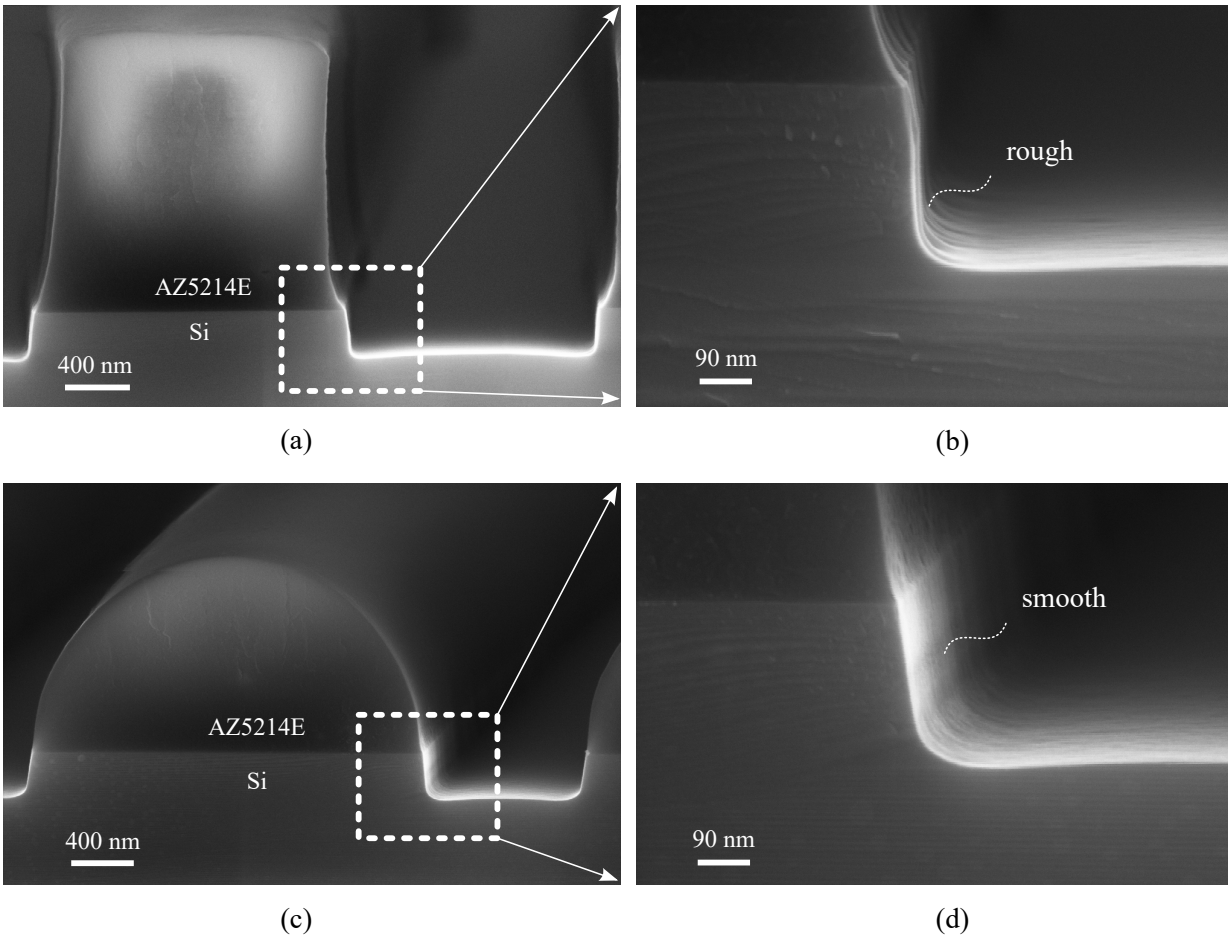
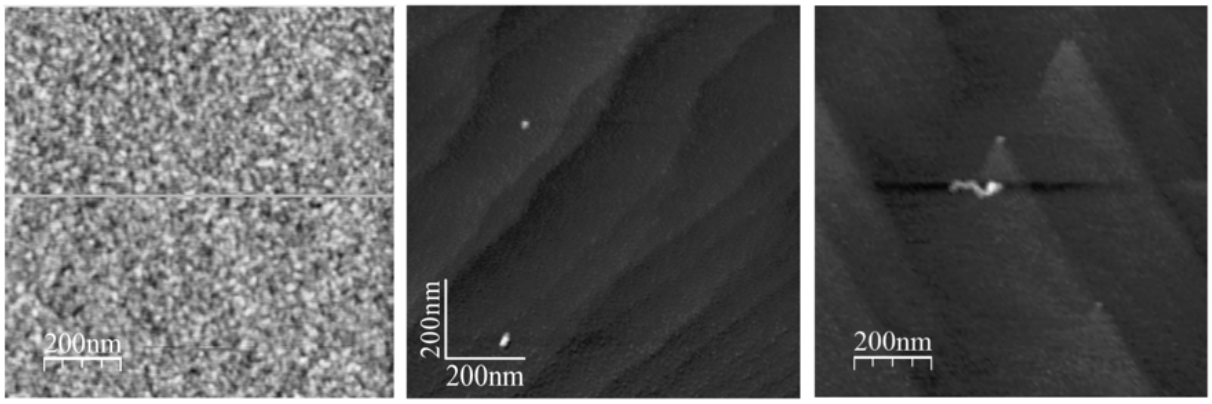


Figure 11: Plasma etching of line structures using SF_6/O_2 gas mixture. Etched sidewall exhibits a rough surface that is transferred from the resist mask even after 10 min of O_2 plasma treatment (a) and (b). A combination of O_2 plasma treatment and resist reflow bake prior to the silicon dry etching process leads to a very smooth etched sidewall (b).

VIII. NH_4F treatment of {111} surfaces

It has been mentioned in section 3.1 that both {111} and {100} surfaces after TMAH etching are atomically flat although the surface roughness of {111} facets is slightly larger than that for {100}. Since charge carriers flow at the oxide-silicon interface in a field-effect transistor, surface roughness plays an important role in device performance, in particular the surface mobility of charge carriers [65, 66]. In order to further improve the quality of {111} surfaces, an aqueous NH_4F etching process can be employed [145, 146, 147, 148, 149]. It is well known that Si{111} prepared by standard HF solutions are atomically rough [148]. Higashi *et al.* [148] found that increasing the pH value of an aqueous NH_4F solution could produce ideally terminated {111} silicon surfaces that are microscopically smooth. An established model for silicon etching in such a solution is presented in Ref. [150].



(a) Sample 1 (b) Sample 2 (c) Sample 3

Figure 12: Atomic force microscopy images of {111} oriented silicon substrate treated by different solutions. Standard 1 % HF solution delivers an atomically rough surface (a). Etch results in an oxygen free 40 % NH_4F solution for 15 min (b) and 30 min (c).

In the present thesis, similar experiments are carried out to confirm the effectiveness of this technique. To this end, <111>-oriented silicon substrates with a miscut of $\pm 0.5\,^\circ$ are used as starting material. After a standard cleaning procedure, etching in a NH_4F-based solution is carried out. the pH value of the solution is tuned to 9.45 (18.9 °C) by mixing NH_4F with ammonia solution. Furthermore, the oxygen dissolved in the solution is removed by adding $(NH_4)_2SO_3$. In addition, the beaker is kept in a nitrogen ambient to prevent further dissolution of oxygen. After the wet chemical treatment, samples are sealed in a bag filled with nitrogen and surface probing with AFM is carried out without delay.

Figure 12 shows atomic force microscopy images of three samples treated under different conditions as depicted in the table shown below. It is observed from the reference sample shown in Fig. 12(a) that the surface prepared using a 1 % HF solution is atomically rough. A treatment in oxygen-free solution with its pH value tuned to approximately 9.45 yields

an atomically flat surface with terraces (15 min) and hillocks (30 min) as depicted in (b) and (c), respectively. The atomic steps are formed to correct the misorientation of the {111}-oriented wafer from the {111} surface. The hillock growth is due to the retardation of flat terraces [149].

1	starting material	· <111>-oriented silicon substrate · miscut <111>±0.5 ° · prime grade, Czochralski-grown · $p-$type, boron doped, $\rho = 5 - 10\,\Omega$cm · single-side polished
2	RCA-clean	please refer to Appendix I for details (wet SC-2 oxide is not stripped)
3.1	sample 1	1. 1 % HF dip, until surface becomes hydrophobic 2. DI water rinse, N_2 blow dry
3.2	sample 2	1. $(NH_4)_2SO_3$:NH_4F:ammonia=5 ml:100 ml:10 ml, 15min 2. DI water rinse, N_2 blow dry
3.3	sample 3	1. $(NH_4)_2SO_3$:NH_4F:ammonia=5 ml:100 ml:10 ml, 30min 2. DI water rinse, N_2 blow dry

In conclusion, it has been demonstrated that an oxygen-free, pH-modified 40 % NH_4F solution could deliver an ultraclean and atomically ordered (111) surface in good agreement with literature results [149]. Compared with an hydrogen annealing process, which is an essential step prior to silicon epitaxy to remove native/wet oxide and deliver an atomically ordered seed layer for subsequent growth, NH_4F solution allows preparing such an ideal surface at room temperature. The key of this process is to remove the dissolved oxygen in the solution and to tune the pH value to 9-10 [149, 151, 152].

IX. Used chemicals

Chemical	Concentration	Manufacturer	Comments
BOE	7:1	Technic™ France	$HF : NH_4F = 12.5 : 87.5\,\%$ with surfactant
TMAH	25 %	Technic™ France	
KOH	86.9 %	VWR™	in pellet form
H_2SO_4	96 %	Technic™ France	
H_2O_2	30.5 %	Technic™ France	
HF	1 %	Technic™ France	VLSI grade
NH_4OH	28-30 %	Technic™ France	
HCl	37 %	Technic™ France	
H_3PO_4	86 %	Technic™ France	
AZ5214E™		Merck™	
AZ726MIF™	2.38 % TMAH	Merck™	with surfactant
DMSO		Technic™ France	TechniStrip™ Micro D350
AR-P 679™	4 %	Allresist™ GmbH	AR679.04, 950k
AR-P 639™	4 %	Allresist™ GmbH	AR639.04, 50k
AR-P 679™	2 %	Allresist™ GmbH	AR679.02, 950k
MIBK		Technic™ France	
acetone		Microchemicals™ GmbH	
isopropyl alcohol (IPA)		Microchemicals™ GmbH	
NH_4F	40 %	J.T. Baker™	
$(NH_4)_2SO_3$	35 %	Sigma-Aldrich™	ammonium sulphite

List of Figures

Bibliography

[1] E. H. Nicollian and J. R. Brews. *MOS (Metal Oxide Semiconductor) Physics and Technology*. Wiley-Interscience, Hoboken, NJ, 2003.

[2] D Kahng and M. M. Atalla. Silicon-silicon dioxide field induced surface devices. *IRE-AIEE Solid-State Device Res. Conf.*, 1960.

[3] F. Wanlass and C. T. Sah. Nanowatt Logic Using Field-Effect Metal-Oxide Semiconductor Triodes. In *1963 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, volume VI, pages 32--33, 1963.

[4] Kwok K. Ng. *Complete Guide to Semiconductor Devices*. J. Wiley & Sons, New York, 2002.

[5] G. E. Moore. Cramming more components onto integrated circuits. 38(8):4, 1965.

[6] IEEE-International Roadmap for Devices and Systems (IRDS) - More than Moore white paper, 2021.

[7] IEEE-International Roadmap for Devices and Systems (IRDS) - Lithography, 2021 Update.

[8] B. S. Wood, F. A. Khaja, B. P. Colombeau, S. Sun, A. Waite, M. Jin, H. Chen, O. Chan, T. Thanigaivelan, N. Pradhan, H. J. L. Gossmann, S. Sharma, V. R. Chavva, M. P. Cai, M. Okazaki, S. S. Munnangi, C. N. Ni, W. Suen, C. P. Chang, A. Mayur, N. Variam, and A. D. Brand. Fin Doping by Hot Implant for 14nm FinFET Technology and Beyond. *ECS Transactions*, 58(9):249--256, Aug. 2013.

[9] B. Colombeau, B. N. Guo, H.-J. Gossmann, F. Khaja, N. Pradhan, A. Waite, K. V. Rao, C. Thomidis, K.-H. Shim, T. Henry, and N. Variam. Advanced CMOS devices: Challenges and implant solutions: Advanced CMOS devices. *physica status solidi (a)*, 211(1):101--108, Jan. 2014.

[10] M. T. Björk, H. Schmid, J. Knoch, H. Riel, and W. Riess. Donor deactivation in silicon nanostructures. *Nature Nanotechnology*, 4(2):103--107, 2009.

[11] C. Blömers, J. G. Lu, L. Huang, C. Witte, D. Grützmacher, H. Lüth, and T. Schäpers. Electronic Transport with Dielectric Confinement in Degenerate InN Nanowires. *Nano Letters*, 12(6):2768--2772, 2012.

[12] D. Horwat, M. Jullien, F. Capon, J.F. Pierson, J. Andersson, and J. L. Endrino. On the deactivation of the dopant and electronic structure in reactively sputtered transparent Al-doped ZnO thin films. *Journal of Physics D: Applied Physics*, 43(13):132003, mar 2010.

[13] T. Mizuno, J. Okumtura, and A. Toriumi. Experimental Study of Threshold Voltage Fluctuation Due to Statistical Variation of Channel Dopant Number in MOSFET's. *IEEE Transactions on Electron Devices*, 41(11):2216--2221, 1994.

[14] P. Andrei and L. Oniciuc. Suppressing random dopant-induced fluctuations of threshold voltages in semiconductor devices. *Journal of Applied Physics*, 104(10):104508, 2008.

[15] T. Mikolajick, V. Häublein, and H. Ryssel. The effect of random dopant fluctuations on the minimum channel length of short-channel MOS transistors. *Applied Physics A: Materials Science & Processing*, 64(6), 1997.

[16] G. Gupta, B. Rajasekharan, and R. J. E. Hueting. Electrostatic Doping in Semiconductor Devices. *IEEE Transactions on Electron Devices*, 64(8):3044--3055, 2017.

[17] F. Riederer, T. Grap, S. Fischer, M. R. Mueller, D. Yamaoka, B. Sun, C. Gupta, K. T. Kallis, and J. Knoch. Alternatives for Doping in Nanoscale Field-Effect Transistors. *physica status solidi (a)*, 215(7):1700969, Apr. 2018.

[18] S. Cristoloveanu, K. H. Lee, H. Park, and M. S. Parihar. The concept of electrostatic doping and related devices. *Solid-State Electronics*, 155:32--43, May 2019.

[19] R. J. E. Hueting, B. Rajasekharan, C. Salm, and J. Schmitz. The Charge Plasma P-N Diode. *IEEE Electron Device Letters*, 29(12):1367--1369, 2008.

[20] R. D. Antonov and A. T. Johnson. Subband Population in a Single-Wall Carbon Nanotube Diode. *Phys. Rev. Lett.*, 83:3274--3276, Oct. 1999.

[21] J. R. Williams, L. DiCarlo, and C. M. Marcus. Quantum Hall Effect in a Gate-Controlled *p-n* Junction of Graphene. *Science*, 317(5838):638--641, Aug. 2007.

[22] M. R. Müller, R. Salazar, S. Fathipour, H. Xu, K. Kallis, U. Künzelmann, A. Seabaugh, J. Appenzeller, and J. Knoch. Gate-Controlled WSe2 Transistors Using a Buried Triple-Gate Structure. *Nanoscale Research Letters*, 11(1):512, Dec. 2016.

[23] M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P. . Gaillardon, Y. Leblebici, and G. De Micheli. Polarity Control in Double-Gate, Gate-All-Around Vertically Stacked Silicon Nanowire FETs. In *2012 International Electron Devices Meeting*, pages 8.4.1--8.4.4, 2012.

[24] M. Simon, B. Liang, D. Fischer, M. Knaut, A. Tahn, T. Mikolajick, and W. M. Weber. Top-Down Fabricated Reconfigurable FET With Two Symmetric and High-Current On-States. *IEEE Electron Device Letters*, 41(7):1110--1113, 2020.

[25] Joachim Knoch. *Nanoelectronics: Device Physics, Fabrication, Simulation*. DE GRUYTER, Berlin/Boston, 2020.

[26] Chenming Hu. *Modern Semiconductor Devices for Integrated Circuits*. Prentice Hall, Upper Saddle River, N.J, 2010. OCLC: ocn268789451.

[27] Yuan Taur and Tak H. Ning. *Fundamentals of Modern VLSI Devices*. Cambridge University Press, 2 edition, 2009.

[28] E H Rhoderick. The Physics of Schottky Barriers. *Journal of Physics D: Applied Physics*, 3(8):1153--1167, Aug. 1970.

[29] E. H. Rhoderick and R. H. Williams. *Metal-Semiconductor Contacts*. Number 19 in Monographs in electrical and electronic engineering. Oxford University Press, Oxford, New York, 2nd edition, 1988.

[30] S. M. Sze. *Physics of Semiconductor Devices*. Wiley, 2007.

[31] A. N. Daw. Metal-Semiconductor Contacts with Thin Interfacial Films. *IETE Journal of Research*, 26(2):118--122, 1980.

[32] S. Fischer, H. Ingolf Kremer, B. Berghoff, T. Maß, T. Taubner, and J. Knoch. Dopant-free complementary metal oxide silicon field effect transistors. *physica status solidi (a)*, 213(6):1494--1499, June 2016.

[33] B. Richstein, L. Hellmich, and J. Knoch. Silicon Nitride Interface Engineering for Fermi Level Depinning and Realization of Dopant-Free MOSFETs. *Micro*, 1(2):228--241, 2021.

[34] Sorin Cristoloveanu. *Fully Depleted Silicon-On-Insulator: Nanodevices, Mechanisms and Characterization*. 2021. OCLC: 1255811308.

[35] A. M. Ionescu and H. Riel. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature*, 479(7373):329--337, 2011.

[36] J. Knoch, M. Zhang, S. Mantl, and J. Appenzeller. On the Performance of Single-Gated Ultrathin-Body SOI Schottky-Barrier MOSFETs. *IEEE Transactions on Electron Devices*, 53(7):1669--1674, 2006.

[37] J. Knoch, M. Zhang, S. Mantl, and J. Appenzeller. On the Performance of Single-Gated Ultrathin-Body SOI Schottky-Barrier MOSFETs. *IEEE Transactions on Electron Devices*, 53(7):1669--1674, 2006.

[38] J. Appenzeller, J. Knoch, M. T. Bjork, H. Riel, H. Schmid, and W. Riess. Toward Nanowire Electronics. *IEEE Transactions on Electron Devices*, 55(11):2827--2845, 2008.

[39] C. P. Auth and J. D. Plummer. Scaling Theory for Cylindrical, Fully-Depleted, Surrounding-Gate MOSFET's. *IEEE Electron Device Letters*, 18(2):74--76, 1997.

[40] R.-H. Yan, A. Ourmazd, and K. F. Lee. Scaling the Si MOSFET: from bulk to SOI to bulk. *IEEE Transactions on Electron Devices*, 39(7):1704--1710, 1992.

[41] K. K. Young. Short-Channel Effect in Fully Depleted SOI MOSFET's. *IEEE Transactions on Electron Devices*, 36(2):399--402, 1989.

[42] Jesús A. del Alamo. *Integrated Microelectronic Devices: Physics and Modeling*. Pearson, New York, NY, 1st edition, 2018.

[43] J. Wei, P. M. Sarro, and T. C. Duc. A Piezoresistive Sensor for Pressure Monitoring at Inkjet Nozzle. In *SENSORS, 2010 IEEE*, pages 2093--2096, 2010.

[44] K. P. Rola, K. Ptasinski, A. Zakrzewski, and I. Zubel. Silicon 45 ° micromirrors fabricated by etching in alkaline solutions with organic additives. *Microsystem Technologies*, 20(2):221--226, Feb. 2014.

[45] S. Kwon, J. Yi, S. Yoon, J. S. Lee, and D. Kim. Effects of textured morphology on the short circuit current of single crystalline silicon solar cells: Evaluation of alkaline wet-texture processes. *Current Applied Physics*, 9(6):1310--1314, 2009.

[46] J. Appenzeller, R. Martel, P. Avouris, J. Knoch, J. Scholvin, J. A. del Alamo, P. Rice, and P. Solomon. Sub-40 nm SOI V-groove n-MOSFETs. *IEEE Electron Device Letters*, 23(2):100--102, 2002.

[47] J. Appenzeller, R. Martel, P. Avouris, J. Knoch, Y. Lu, K. L. Wang, J. Scholvin, J. A. del Alamo, P. Rice, and P. Solomon. Sub-40 nm V-groove MOSFETs. In *Device Research Conference. Conference Digest (Cat. No.01TH8561)*, pages 95--96, 2001.

[48] Kazuo Sato and Prem Pal. *Silicon Wet Bulk Micromachining for MEMS*. Pan Stanford Publishing Pte. Ltd., Singapore, 2017.

[49] C.-H. Lee, C.-L. Wang, H.-F. Lin, C.-Y. Chai, M.-Y. Hong, and C.-Kung Ho. Toxicity of tetramethylammonium hydroxide: Review of two fatal cases of dermal exposure and development of an animal model. *Toxicology and Industrial Health*, 27(6):497--503, July 2011.

[50] C.-C. Lin, C.-C. Yang, J. Ger, J.-F. Deng, and D.-Z. Hung. Tetramethylammonium hydroxide poisoning. *Clinical Toxicology*, 48(3):213--217, Mar. 2010.

[51] C.-L. Wu, S.-B. Su, J.-L. Chen, H.-J. Lin, and H.-R. Guo. Mortality from Dermal Exposure to Tetramethylammonium Hydroxide. *Journal of Occupational Health*, 50(2):99--102, Mar. 2008.

[52] H. Seidel, L. Csepregi, L. Heuberger, and H. Baumgärtel. Anisotropic Etching of Crystalline Silicon in Alkaline Solutions: I . Orientation Dependence and Behavior of Passivation Layers. *Journal of The Electrochemical Society*, 137(11):3612--3626, 1990.

[53] Miko Elwenspoek and Henri V. Jansen. *Silicon Micromachining*. Cambridge University Press, Cambridge, 1998.

[54] E. D. Palik, V. M. Bermudez, and O. J. Glembocki. Ellipsometric Study of the Etch-Stop Mechanism in Heavily Doped Silicon. *Journal of The Electrochemical Society*, 132(1):135--141, Jan. 1985.

[55] B. Kloeck, S. D. Collins, N. F. de Rooij, and R. L. Smith. Study of Electrochemical Etch-Stop for High-Precision Thickness Control of Silicon Membranes. *IEEE Transactions on Electron Devices*, 36(4):663--669, 1989.

[56] M. Shikida, K. Sato, K. Tokoro, and D. Uchikawa. Differences in anisotropic etching properties of KOH and TMAH solutions. *Sensors and Actuators A: Physical*, 80(2):179--188, 2000.

[57] Irena Zubel, Krzysztof Rola, and Malgorzata Kramkowska. The effect of isopropyl alcohol concentration on the etching process of Si-substrates in KOH solutions. *Sensors and Actuators A: Physical*, 171(2):436--445, 2011.

[58] I. Zubel and I. Kramkowska. Etch rates and morphology of silicon ($h\ k\ l$) surfaces etched in KOH and KOH saturated with isopropanol solutions. *Sensors and Actuators A: Physical*, 115(2):549--556, 2004. The 17th European Conference on Solid-State Transducers.

[59] U. Schnakenberg, W. Benecke, and P. Lange. TMAHW etchants for Silicon Micromachining. In *TRANSDUCERS '91: 1991 International Conference on Solid-State Sensors and Actuators. Digest of Technical Papers*, pages 815--818, 1991.

[60] O. Tabata, R. Asahi, H. Funabashi, K. Shimaoka, and S. Sugiyama. Anisotropic etching of silicon in TMAH solutions. *Sensors and Actuators A: Physical*, 34(1):51--57, July 1992.

[61] A. Merlos, M. Acero, M. H. Bao, J. Bausells, and J. Esteve. TMAH/IPA anisotropic etching characteristics. *Sensors and Actuators A: Physical*, 37-38:737 -- 743, 1993. Proceedings of Eurosensors VI.

[62] A. Izumi. Ultra thin silicon nitride prepared by direct nitridation using ammonia decomposed species. *Thin Solid Films*, 501(1-2):157--159, 2006.

[63] T. Ito, S. Hijiya, T. Nozaki, H. Arakawa, M. Shinoda, and Y. Fukukawa. Very Thin Silicon Nitride Films Grown by Direct Thermal Reaction with Nitrogen. 125(3):448--452, Mar. 1978.

[64] *Microoptics and Nanooptics Fabrication.* CRC Press, 2017. OCLC: 1008875755.

[65] T. Tezuka, E. Toyoda, S. Nakaharai, T. Irisawa, N. Hirashita, Y. Moriyama, N. Sugiyama, N. Taoka, Y. Yamashita, O. Kiso, M. Harada, T. Yamamoto, and S. Takagi. Observation of Mobility Enhancement in Strained Si and SiGe Tri-Gate MOSFETs with Multi-Nanowire Channels Trimmed by Hydrogen Thermal Etching. In *2007 IEEE International Electron Devices Meeting*, pages 887--890, 2007.

[66] Xiong W. Z., G. Gebara, J. Zaman, M. Gostkowski, B. Nguyen, G. Smith, D. Lewis, C. R. Cleavelin, R. Wise, S.F. Yu, M. Pas, T.-J. King, and J. P. Colinge. Improvement of FinFET Electrical Characteristics by Hydrogen Annealing. *IEEE Electron Device Letters*, 25(8):541--543, 2004.

[67] M.-C. M. Lee and M. C. Wu. 3D Silicon Transformation using Hydrogen Annealing. In *2004 Solid-State, Actuators, and Microsystems Workshop Technical Digest*, pages 19--22, Hilton Head, South Carolina, USA, June 2004. Transducer Research Foundation, Inc.

[68] M.-C. M. Lee and M. C. Wu. Thermal Annealing in Hydrogen for 3-D Profile Transformation on Silicon-on-Insulator and Sidewall Roughness Reduction. *Journal of Microelectromechanical Systems*, 15(2):338--343, 2006.

[69] E. Dornel, T. Ernst, J. C. Barbé, J. M. Hartmann, V. Delaye, F. Aussenac, C. Vizioz, S. Borel, V. Maffini-Alvaro, C. Isheden, and J. Foucher. Hydrogen annealing of arrays of planar and vertically stacked si nanowires. *Applied Physics Letters*, 91(23):233502, 2007.

[70] D. Chopp and J. Sethian. Motion by intrinsic Laplacian of curvature. *Interfaces and Free Boundaries*, pages 107--123, 1999.

[71] K. Kolari, T. Vehmas, O. Svensk, P. Törmä, and T. Aalto. Smoothing of microfabricated silicon features by thermal annealing in reducing or inert atmospheres. *Physica Scripta*, T141:014017, Nov. 2010.

[72] P. E. Acosta-Alba, O. Kononchuk, C. Gourdel, and A. Claverie. Surface self-diffusion of silicon during high temperature annealing. *Journal of Applied Physics*, 115(13):134903, 2014.

[73] X. C. Hao, S. Tanaka, A. Masuda, J. Nakamura, K. Sudoh, K. Maenaka, H. Takao, and K. Higuchi. Application of Silicon on Nothing Structure for Developing a Novel Capacitive Absolute Pressure Sensor. *IEEE Sensors Journal*, 14(3):808--815, 2014.

[74] R. Kant, M. Ziaei-Moayyed, and R. T. Howe. Suspended microstructures made using silicon migration. In *TRANSDUCERS 2009 - 2009 International Solid-State Sensors, Actuators and Microsystems Conference*, pages 1091--1094, 2009.

[75] R. Kant. Silicon migration as a process for micro/nanofabrication, 2009.

[76] M. Baranski, R. Kasztelanic, J. Albero, L. Nieradko, and C. Gorecki. Level set method for microfabrication simulations. *Micro-Optics 2010*, 7716:77161W, 2010.

[77] J. A. Sethian and D. Adalsteinsson. An Overview of Level Set Methods for Etching, Deposition, and Lithography Development. *IEEE Transactions on Semiconductor Manufacturing*, 10(1):167--184, 1997.

[78] N. Li, Z. F. Zhou, and Q. A. Huang. *An ICP Etching Simulation System Based on the Narrow Band Level Set Method*, pages 268--275.

[79] D. Chopp and J. Sethian. Motion by intrinsic Laplacian of curvature. *Interfaces and Free Boundaries*, pages 107--123, 1999.

[80] S. Osher and R. P. Fedkiw. *Level Set Methods and Dynamic Implicit Surfaces*. Springer, New York, 2003.

[81] K. Sudoh, H. Iwasaki, H. Kuribayashi, R. Hiruta, and R. Shimizu. Numerical Study on Shape Transformation of Silicon Trenches by High-Temperature Hydrogen Annealing. *Japanese Journal of Applied Physics*, 43(9A):5937--5941, sep 2004.

[82] W. W. Mullins. Theory of Thermal Grooving. 1956.

[83] P. Smereka. Semi-Implicit Level Set Methods for Curvature and Surface Diffusion Motion. *Journal of Scientific Computing*, 19(1):439--456, 2003.

[84] C.-W. Shu and S. Osher. Efficient Implementation of Essentially Non-oscillatory Shock-Capturing Schemes. *Journal of Computational Physics*, 77(2):439--471, 1988.

[85] Andrew Sarangan. *Nanofabrication: Principles to Laboratory Practice*. CRC Press, Boca Raton, 2019.

[86] A. Chambers, R. K. Fitch, and B. S. Halliday. *Basic Vacuum Technology*. Institute of Physics Pub, Bristol ; Philadelphia, 2nd ed edition, 1998.

[87] A. A. Tseng, K. Chen, C. D. Chen, and K. J. Ma. Electron Beam Lithography in Nanoscale Fabrication: Recent Development. *IEEE Transactions on Electronics Packaging Manufacturing*, 26(2):141--149, 2003.

[88] Y. C. Pao, K. Tran, C. Shih, and N. Hardy. Solution to the E-beam Gate Resist Blistering Problem of 0.15 micron PHEMTs, 1999. GaAs MANTECH.

[89] E. B. Graper. Charged Particle Flux Generated by an Electron-Beam Deposition Source. *Journal of Vacuum Science and Technology*, 7(1):282--285, 1970.

[90] R. Nishio, K. Tuchida, M. Tooma, and K. Suzuki. Origins of charged particles in vapor generated by electron-beam evaporation. *Journal of Applied Physics*, 72(10):4548--4555, 1992.

[91] F. Volmer, I. Seidler, T. Bisswanger, J.-S. Tu, L. R. Schreiber, C. Stampfer, and B. Beschoten. How to solve problems in micro- and nanofabrication caused by the emission of electrons and charged metal atoms during e-beam evaporation. *Journal of Physics D: Applied Physics*, 54(22):225304, 2021.

[92] J. I. Goldstein and H. Yakowitz. *Practical Scanning Electron Microscopy: Electron and Ion Microprobe Analysis*. Springer US, Boston, MA, 1975. OCLC: 840282729.

[93] H. Seiler. Secondary electron emission in the scanning electron microscope. *Journal of Applied Physics*, 54(11):R1--R18, 1983.

[94] B. W. Nuryadin and R. Rusman. Simple determination of Curie temperature using a smartphone magnetometer. *The Physics Teacher*, 57(6):422--423, 2019.

[95] Standard Specifications for Permanent Magnet Materials. Technical Report MMPA STANDARD No. 0100-00, Magnetic Materials Producers Association, ILLINOIS, USA.

[96] S. Mayo, K. F. Galloway, and T. F. Leedy. Radiation Dose Due to Electron-Gun Metallization Systems. *IEEE Transactions on Nuclear Science*, 23(6):1875--1880, 1976.

[97] X. Zhang, C. Jacobsen, S. Lindaas, and S. Williams. Exposure strategies for polymethyl methacrylate from in situ x-ray absorption near edge structure spectroscopy.

[98] B. Sun, T. Grap, T. Frahm, S. Scholz, and J. Knoch. Role of electron and ion irradiation in a reliable lift-off process with electron beam evaporation and a bilayer PMMA resist system. *Journal of Vacuum Science & Technology B*, 39(5):052601, 2021.

[99] J. P. Lu, D. S. Miles, J. DeLoach, D. F. Yue, P. J. Chen, T. Bonifield, S. Crank, S. F. Yu, F. Mehrad, Y. Obeng, D. A. Ramappa, D. Corum, R. L. Guldi, L. S. Robertson, X. Liu, L. H. Hall, Y. Q. Xu, B. Y. Lin, A. J. Griffin, F. S. Johnson, T. Grider, D. Mercer, and C. Montgomery. Nickel SALICIDE Process Technology for CMOS Devices of 90nm Node and Beyond. In *2006 International Workshop on Junction Technology*, pages 127--133, 2006.

[100] J. Appenzeller, J. Knoch, E. Tutuc, M. Reuter, and S. Guha. Dual-gate silicon nanowire transistors with nickel silicide contacts. In *2006 International Electron Devices Meeting*, pages 1--4, 2006.

[101] F. Fuchs, M. B. Khan, D. Deb, D. Pohl, J. Schuster, W. M. Weber, U. Mühle, M. LÃ¶ffler, Y. M. Georgiev, A. Erbe, and S. Gemming. Formation and crystallographic orientation of $NiSi_2$--Si interfaces. *Journal of Applied Physics*, 128(8):085301, 2020.

[102] L. J. Chen, editor. *Silicide Technology for Integrated Circuits*. Number no. 5 in Processing series. Institution of Electrical Engineers, London, 2004. OCLC: ocm57576829.

[103] N. Biswas, J. Gurganus, and V. Misra. Work function tuning of nickel silicide by co-sputtering nickel and silicon. *Applied Physics Letters*, 87(17):171908, 2005.

[104] K. Takahashi, K. Manabe, T. Ikarashi, N. Ikarashi, T. Hase, T. Yoshihara, H. Watanabe, T. Tatsumi, and Y. Mochizuki. Dual Workfunction Ni-Silicide/HfSiON Gate Stacks by Phase-Controlled Full-Silicidation (PC-FUSI) Technique for 45nm-node LSTP and LOP devices. In *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004.*, pages 91--94, 2004.

[105] J. Yuan, G. Z. Pan, Y.-L. Chao, and Jason C. S. Woo. Nickel Silicide Work Function Tuning Study In Metal-Gate CMOS Applications. *MRS Proceedings*, 829:B7.11, 2004.

[106] D. Mangelinck, J. Y. Dai, J. S. Pan, and S. K. Lahiri. Enhancement of thermal stability of NiSi films on (100)Si and (111)Si by Pt addition. *Applied Physics Letters*, 75(12):1736--1738, 1999.

[107] M. B. Khan, D. Deb, J. Kerbusch, F. Fuchs, M. Löffler, S. Banerjee, U. Mühle, W. M. Weber, S. Gemming, J. Schuster, A. Erbe, and Y. M. Georgiev. Towards Reconfigurable Electronics: Silicidation of Top-Down Fabricated Silicon Nanowires. *Applied Sciences*, 9(17), 2019.

[108] M. B. Khan, S. Ghosh, S. Prucnal, T. Mauersberger, R. Hübner, M. Simon, T. Mikolajick, A. Erbe, and Y. M. Georgiev. Towards Scalable Reconfigurable Field Effect Transistor using Flash Lamp Annealing. In *2020 Device Research Conference (DRC)*, pages 1--2, 2020.

[109] M. B. Khan, S. Prucnal, S. Ghosh, D. Deb, R. Hübner, D. Pohl, L. Rebohle, T. Mikolajick, A. Erbe, and Y. M. Georgiev. Controlled Silicidation of Silicon Nanowires Using Flash Lamp Annealing. *Langmuir*, page acs.langmuir.1c01862, Dec. 2021.

[110] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D.-L. Kwong. High-Performance Fully Depleted Silicon Nanowire (Diameter $\leq 5\,\mathrm{nm}$) gate-All-Around CMOS Devices. *IEEE Electron Device Letters*, 27(5):383--386, 2006.

[111] O. Shirak, O. Shtempluck, V. Kotchtakov, V. Bahir, and Y. E. Yaish. High performance horizontal gate-all-around silicon nanowire field-effect transistors. 23(39):395202, Sep. 2012.

[112] M. T. Björk, J. Knoch, H. Schmid, H. Riel, and W. Riess. Silicon nanowire tunneling field-effect transistors. *Applied Physics Letters*, 92(19):193504, 2008.

[113] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy. Nanowire transistors without junctions. *Nature Nanotechnology*, 5(3):225--229, Mar. 2010.

[114] Y. Cui, Q.-Q. Wei, H.-K Park, and C. M. Lieber. Nanowire Nanosensors for Highly Sensitive and Selective Detection of Biological and Chemical Species. *Science*, 293(5533):1289--1292, Aug. 2001.

[115] X. T. Vu, J. F. Eschermann, R. Stockmann, R. GhoshMoulick, A. Offenhäusser, and S. Ingebrandt. Top-down processed silicon nanowire transistor arrays for biosensing. *physica status solidi (a)*, 206(3):426--434, 2009.

[116] F. A. Zwanenburg, A. A. van Loon, G. A. Steele, C. E. W. M. van Rijmenam, T. Balder, Y. Fang, C. M. Lieber, and L. P. Kouwenhoven. Ultrasmall silicon quantum dots. *Journal of Applied Physics*, 105(12):124314, 2009.

[117] N. F. Za'bah, K. S. K. Kwa, L. Bowen, B. Mendis, and A. O'Neill. Top-down fabrication of single crystal silicon nanowire using optical lithography. *Journal of Applied Physics*, 112(2):024309, 2012.

[118] Werner K. The Evolution of Silicon Wafer Cleaning Technology. *Journal of The Electrochemical Society*, 137(6):1887--1892, 1990.

[119] D. Shir, B. Z. Liu, A. M. Mohammad, K. K. Lew, and S. E. Mohney. Oxidation of silicon nanowires. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, 24(3):1333--1336, 2006.

[120] S. J. Fang, W. Chen, T. Yamanaka, and C. R. Helms. The Evolution of (001) Si / SiO_2 Interface Roughness during Thermal Oxidation. *Journal of The Electrochemical Society*, 144(8):2886--2893, 1997.

[121] M. B. Khan, D. Deb, J. Kerbusch, F. Fuchs, M. Löffler, S. Banerjee, U. Mühle, W. M. Weber, S. Gemming, J. Schuster, A. Erbe, and Y. M. Georgiev. Towards Reconfigurable Electronics: Silicidation of Top-Down Fabricated Silicon Nanowires. *Applied Sciences*, 9(17):3462, Aug. 2019.

[122] A. Katsman, M. Beregovsky, and Y. E. Yaish. Formation and Evolution of Nickel Silicide in Silicon Nanowires. *IEEE Transactions on Electron Devices*, 61(10):3363--3371, 2014.

[123] E. M. Savitskii, V. V. Baron, Y. V. Efimov, Bychkova M. I., and Myzenkova L. F. *Superconducting Materials*. Plenum Press, New York, N.Y., 1973.

[124] F. A. Zwanenburg, A. A. van Loon, G. A. Steele, C. E. W. M. van Rijmenam, T. Balder, Y. Fang, C. M. Lieber, and L. P. Kouwenhoven. Ultrasmall silicon quantum dots. *Journal of Applied Physics*, 105(12):124314, 2009.

[125] S. Cristoloveanu and S. S. Li. Electrical Characterization of Silicon-on-Insulator Materials and Devices, 1995. ISBN: 9781461522454.

[126] S. Cristoloveanu and S. Williams. Point-Contact Pseudo-MOSFET for *In-Situ* Characterization of As-Grown Silicon-On-Insulator Wafers. *IEEE Electron Device Letters*, 13(2):102--104, 1992.

[127] S. Cristoloveanu and S. S. Li. *Electrical Characterization of Silicon-On-Insulator Materials and Devices*. Number SECS 305 in The Kluwer international series in engineering and computer science. Kluwer Academic, Boston, 1995.

[128] M.R. Müller, R. Salazar, S. Fathipour, H. Xu, K. Kallis, U. Künzelmann, A. Seabaugh, J. Appenzeller, and J. Knoch. Gate-Controlled WSe_2 Transistors Using a Buried Triple-Gate Structure. *Nanoscale Research Letters*, 11:512, 2016.

[129] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W. M. Weber. Reconfigurable Silicon Nanowire Transistors. *Nano Letters*, 12(1):119--124, 2012.

[130] M. Simon, A. Heinzig, J. Trommer, T. Baldauf, T. Mikolajick, and W. M. Weber. Top-Down Technology for Reconfigurable Nanowire FETs With Symmetric On-Currents. *IEEE Transactions on Nanotechnology*, 16(5):812--819, 2017.

[131] B. Winstead and U. Ravaioli. Simulation of Schottky Barrier MOSFET's with a Coupled Quantum Injection/Monte Carlo Technique. *IEEE Transactions on Electron Devices*, 47(6):1241--1246, 2000.

[132] A. Bolognesi, A. Di Carlo, and P. Lugli. Influence of carrier mobility and contact barrier height on the electrical characteristics of organic transistors. *Applied Physics Letters*, 81(24):4646--4648, 2002.

[133] R. Jhaveri, V. Nagavarapu, and Jason C. S. Woo. Asymmetric Schottky Tunneling Source SOI MOSFET Design for Mixed-Mode Applications. *IEEE Transactions on Electron Devices*, 56(1):93--99, 2009.

[134] D. Supriyo. Nanoscale device modeling: the Green's function method. *Superlattices and Microstructures*, 28(4):253--278, 2000.

[135] H. Flietner. The $E(k)$ Relation for a Two-Band Scheme of Semiconductors and the Application to the Metal-Semiconductor Contact. *physica status solidi (b)*, 54(1):201--208, 1972.

[136] J. Knoch, L. Lengeler, and J. Appenzeller. Quantum simulations of an ultrashort channel single-gated n-MOSFET on SOI. *IEEE Transactions on Electron Devices*, 49(7):1212--1218, 2002.

[137] J. Knoch, M. Zhang, J. Appenzeller, and S. Mantl. Physics of ultrathin-body silicon-on-insulator Schottky-barrier field-effect transistors. *Appl. Phys. A*, 87:351--357, 2007.

[138] R. Venugopal, M. Paulsson, S. Goasguen, S. Datta, and M. S. Lundstrom. A simple quantum mechanical treatment of scattering in nanoscale transistors. *Journal of Applied Physics*, 93(9):5613--5625, 2003.

[139] S. M. Sze. *Physics of Semiconductor Devices*. Wiley, New York, 2nd edition, 1981.

[140] W. M. Weber, A. Heinzig, J. Trommer, M. Grube, F. Kreupl, and T. Mikolajick. Reconfigurable Nanowire Electronics-Enabling a Single CMOS Circuit Technology. *IEEE Transactions on Nanotechnology*, 13(6):1020--1028, 2014.

[141] D.-Y. Jeon, S. Pregl, S. J. Park, L. Baraban, G. Cuniberti, T. Mikolajick, and W. M. Weber. Scaling and Graphical Transport-Map Analysis of Ambipolar Schottky-Barrier Thin-Film Transistors Based on a Parallel Array of Si Nanowires. *Nano Letters*, 15(7):4578--4584, July 2015.

[142] S. Pregl, A. Heinzig, L. Baraban, G. Cuniberti, T. Mikolajick, and W. M. Weber. Printable Parallel Arrays of Si Nanowire Schottky-Barrier-FETs With Tunable Polarity for Complementary Logic. *IEEE Transactions on Nanotechnology*, 15(3):549--556, 2016.

[143] E. Reichmanis, O. Nalamasu, and F. Houlihan. Polymers, Photoresponsive (in Electronic Applications). In *Encyclopedia of Physical Science and Technology*, pages 723--744. Elsevier, 2003.

[144] Donald A. Neamen. *Semiconductor Physics and Devices: Basic Principles*. McGraw-Hill, New York, NY, 4th edition, 2012. OCLC: ocn681739179.

[145] P. Allongue, C. Henry de Villeneuve, S. Morin, R. Boukherroub, and Danial D. M. Wayner. The preparation of flat H-Si(111) surfaces in 40% NH4F revisited. *Electrochimica Acta*, 45(28):4591--4598, Oct. 2000.

[146] Y. Sawada, K. Tsujino, and M. Matsumura. Hydrogen Evolution from Atomically Flat Si(111) Surfaces Exposed to 40% NH[sub 4]F, Oxygen-Free Water, or Wet Gas. *Journal of The Electrochemical Society*, 153(12):C854, 2006.

[147] P. Allongue, V. Kieling, and H. Gerischer. Etching mechanism and atomic structure of H-Si(111) surfaces prepared in NH_4F. *Electrochimica Acta*, 40(10):1353--1360, July 1995.

[148] G. S. Higashi, R. S. Becker, Y. J. Chabal, and A. J. Becker. Comparison of Si(111) surfaces prepared using aqueous solutions of NH_4F versus HF. *Applied Physics Letters*, 58(15):1656--1658, 1991.

[149] K. Hiroki, T. Takumi, N. Susumu, S. Gen, Y. Taro, C. Ryszard, W. Andrzej, N. Kazuo, K. Atsuo, and S. Shozo. Preparation of an Ultraclean and Atomically Controlled Hydrogen-Terminated Si(111)-(1× 1) Surface Revealed by High Resolution Electron Energy Loss Spectroscopy, Atomic Force Microscopy, and Scanning Tunneling Microscopy: Aqueous NH_4F Etching Process of Si(111). *Japanese Journal of Applied Physics*, 46(9A):5701--5705, Sep. 2007.

[150] M.L. Munford, R. Cortès, and P. Allongue. The Preparation of Ideally Ordered Flat H-Si(111) Surfaces. *Sensors and Materials*, 13(5):259--269, 2001.

[151] C. P. Wade and C. Chidsey. Etch-pit initiation by dissolved oxygen on terraces of H-Si(111). *Applied Physics Letters*, 71(12):1679--1681, 1997.

[152] B. S. Aldinger and M. A. Hines. Si(100) Etching in Aqueous Fluoride Solutions: Parallel Etching Reactions Lead to pH-Dependent Nanohillock Formation or Atomically Flat Surfaces. *The Journal of Physical Chemistry C*, 116(40):21499--21507, 2012.

[153] G. S. Higashi, Y. J. Chabal, G. W. Trucks, and K. Raghavachari. Ideal hydrogen termination of the Si (111) surface. *Applied Physics Letters*, 56(7):656--658, 1989.

[154] K. Sudoh, H. Iwasaki, H. Kuribayashi, R. Hiruta, and R. Shimizu. Numerical Study on Shape Transformation of Silicon Trenches by High-Temperature Hydrogen Annealing. *Japanese Journal of Applied Physics*, 43(9A):5937--5941, Sep. 2004.

[155] S. Osher and J. A. Sethian. Fronts Propagating with Curvature-Dependent Speed: Algorithms Based on Hamilton-Jacobi Formulations. *Journal of Computational Physics*, 79(1):12--49, 1988.

Acknowledgements

At this moment, I would like to thank all those people, with their invaluable knowledge, great technical expertise, and profound insight, that have supported me and made the years of my PhD studies at the RWTH Aachen University a wonderful and enjoyable period of my life.

First and foremost, I am deeply indebted to my thesis advisor Prof. Joachim Knoch for giving me the valuable opportunity to pursue my PhD degree in this fascinating field. It is an invaluable treasure to work as a student of such an admirable academic professional. He endeavors to spend time in the cleanroom with the students and has impressed me with his enthusiasm in teaching and research. Research on nanoelectronics requires a solid knowledge in physics, electrical engineering, and material science. In the beginning, I had only the smattering of semiconductor physics needed to explain the operation of a MOS transistor. The nanoelectronics book from Prof. Knoch is very intriguing which delivers a clear and incisive understanding of the most essential parts of quantum mechanics and solid state physics. Chapters on nanofabrication, device simulation, and state-of-the-art applications originating from his research experience in the past 25 years have made the book a companion of my daily work since he sent us the draft version. I wish he could have written it five years earlier.

Next, I would like to express my sincere gratitude to Prof. Thomas Mikolajick for agreeing to be the second reviewer of my thesis. In addition, I wish to thank Jens Trommer from NaMLab gGmbH for his insightful suggestions.

A special note of thanks goes to Prof. Uwe Schnakenberg, who showed great interest in my work and kindly offered to be the chair of my thesis examination committee.

I would also like to take this opportunity to thank Prof. Dirk Uwe Sauer for agreeing to be a member of the committee.

Many thanks to all people both inside and outside the institute who helped me with the experiments in the cleanroom. I would especially like to thank Dr. Stefan Scholz who leads me to the door of nanoelectronics and equipped me with basic lab knowledge and responsibilities when I started doing my master thesis. In addition, I gratefully acknowledge

the numerous wafer dicing, and deposition work kindly offered by my officemate Dipl. Horst Windgassen. His tireless hard work on processing and characterization striving towards an optimized recipe is indispensible for the success of my device. Furthermore, I feel lucky and happy to stay in our research group with very nice colleagues, just to name a few: Dr. Birger Berghoff, Dr. Thomas Grap, Dipl. Birgit Hadam, Noel Wilck, Patrick Libisch, Thorben Frahm, Benjamin Richstein, Lena Hellmich, Mattia Antonini, Raghutham Ramesha, Nazmus Sakib, Michail Michailow, and my officemates Daichi Yamaoka, Jochen Politze, etc. I want to thank all of you who have made our institute one of the most heartwarming places to work at.

For people outside the institute, I would like to thank Prof. Matthias Wuttig, Dr. Oana Cojocaru-Mirédin and Svitlana Taranenko (I. Institute of Physics A, RWTH Aachen University) for organizing and carrying out FIB cuts for my samples. Many thanks to Christian Teichrib (I. Institute of Physics A, RWTH Aachen University) for carrying out x-ray exposure experiments. I also thank Marcus Liebmann (II. Institute of Physics B, RWTH Aachen University) for carrying out dedicated AFM measurements on a tapered surface. I would also like to say thank you to Dr. Lars Schreiber and Jan Klos (Quantum Technology Group, RWTH Aachen University) for the collaboration work towards a silicon-based platform to host quantum bits. Special thanks to Jochen Heiss (Institute of Materials in Electrical Engineering 1, RWTH Aachen University) for his great help in tightening a vacuum tube fitting. It sounds indeed like a trivial task but without his support, the vacuum chamber might still be leaky.

I am very grateful to the China Scholarship Council for providing financial support for the first 4 years of my PhD studies. The follow-up fundings by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) under Germany's Excellence Strategy−Cluster of Excellence Matter and Light for Quantum Computing (ML4Q) EXC 2004/1-390534769 are gratefully acknowledged.

Finally, I would like to thank my dear wife, my closest friend, Hongyan, for her love, endurance, support, and constant encouragement during the ups and downs of PhD. Furthermore, I am greatly indebted to my parents, who always put my interests before theirs without any compromise.

Curriculum Vitae

Bin Sun, born on July 15th, 1988 in Jiangsu, China

10/1995 - 07/2001	Primary school
10/2004 - 06/2007	Junior & senior high school Changshu Foreign Language School, Jiangsu
09/2007 - 09/2009	B. Sc. Electrical Engineering and Automation China University of Mining and Technology
10/2009 - 01/2013	B. Sc. Electrical and Electronic Engineering University of Duisburg-Essen (*best graduation grade of the year*)
04/2013 - 02/2016	M. Sc. Electrical Engineering, Information Technology and Computer Engineering Field of study: Micro- und Nanoelectronics RWTH Aachen University
since 07/2016	Ph.D. student at the Institute of Semiconductor Electronics RWTH Aachen University