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Fabrication of Ultrasmall Si Encapsulated in Silicon Dioxide and Silicon Nitride as Alternative to Impurity Doping

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Further miniaturization of complementary metal oxide semiconductor devices based on impurity-doped semiconductors is limited due to statistical fluctuation of the impurity concentration in very small volumes and dopant deactivation, increasing the resistance and power consumption. Based on density functional theory calculations and backed by experimental data, the nanoscale electronic structure shift induced by anions at surfaces (NESSIAS) has been described recently. It explains the structure shift of low-doped single-crystalline Si nanowells (Si-NWs) with thicknesses ≤3 nm embedded in SiO_2 (Si_3N_4) toward n-type (p-type) behavior. The influence of the anions is on the scale of a few nanometers, allowing for very steep p–n junctions without the drawbacks of impurity doping. The process to fabricate crystalline silicon (c-Si) NWs embedded in SiO_2 and Si_3N_4, starting with silicon on insulator (SOI) across 15 × 15 mm^2 samples, is described. Four possible methods to fabricate Si-NWs by thinning down single-crystalline top-Si of an SOI substrate are evaluated in terms of reproducibility and surface roughness.

1. Introduction

The complementary metal oxide semiconductor (CMOS) technology is the foundation of our modern computers. Impurity doping is an essential technique for realizing CMOS devices, enabling many of their electronic key properties.[1] Hence, the type and density of impurity dopants is at the center of device design, allowing for the versatility and adaptability of CMOS technology to virtually every semiconductor technology, from analog design to very-large-scale integration (VLSI). By scaling down CMOS transistor dimensions, the influence of the applied gate potential on the channel current decreased. This phenomenon, known as short channel effects, gave rise to the introduction of silicon-on-insulator (SOI) substrates, the development of field-effect transistors (Fin-FET) technology, and the upcoming gate-all-around (GAA)–FET technology. With increasing surface to volume ratio, impurity doping on the nanoscale faces the problems of dopant inactivation, due to increased ionization energy as a consequence of dielectric mismatch,[2,3] the dopant out-diffusion being on the same length scale as the gate length,[4,5] and statistical fluctuations of the dopant concentration in nanoscale volume transistors,[4,6,7] leading to unpredictable device behavior. The deactivation of dopants near the surface in nanowires effectively increases the resistance of GAA–FETs. Besides the aforementioned issues, dopants can freeze out at low temperatures, leaving them electronically inactive and restricting their application in cryoelectronics. With these drawbacks it would be beneficial to avoid impurity doping altogether, enabling further downscaling of transistors below the dopant out-diffusion limit of drain and source regions.

Based on density functional theory (DFT) calculations, the effect of a nanoscale electronic structure shift induced by anions at surfaces (NESSIAS) was predicted[8,9] and would allow very steep p–n junctions on GAA–FETs with a diameter of a few nanometers.[10] Recently we demonstrated the NESSIAS effect on ultrathin Si-NWs as a function of Si thickness and embedding dielectric, with SiO_2 and Si_3N_4 yielding effective n- and p-type doping, respectively.[10–13] The conduction band edge of these samples was measured with grazing incidence X-ray absorption spectroscopy in total fluorescence yield (XAS–TFY) and the

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valence band edge with synchrotron UV photoelectron spectroscopy (UPS) measurements at Elettra Sincrotrone Trieste, Italy. The fabrication of appropriate samples combines etching down of the top-Si of SOI, digital etching, rapid thermal nitridation, chemical vapor deposition (CVD) of SiN_x and SiO_2, chemical mechanical polishing, direct bonding, and deep reactive ion etching (DRIE). The present work elucidates the fabrication details and parameters to arrive at high-quality crystalline silicon (c-Si) nanowells (NWs) embedded in SiO_2 and Si_3N_4 on samples of $15 \times 15\ mm^2$. Samples fabricated this way enable the measurement of the valence band fine structure of Si-NWs.[13] The fabrication of Si-NWs embedded in Si_3N_4 involves direct bonding, rendering the surface roughness of the samples during processing to be an important parameter. The Si-NWs for the XAS–TFY measurements had to be homogeneously thinned down over a lateral range of at least 4 mm to allow for the required grazing incidence angle with its associated beam width at the XAS–TFY setup (supporting information of[12]). Section 2 explains the methods used in sample fabrication and characterization. Section 3 presents results on the reliability of NW thickness determination by ellipsometry and high-resolution transmission electron microscopy (HRTEM) and a brief discussion of the XAS–TFY and UPS measurement results. Section 4 delivers the conclusion.

2. Experimental Section

Unless stated otherwise, all samples described here originate from a 12 inch SOI wafer with a p-doping concentration of $1 \times 10^{15}\ cm^{-3}$ in the top-Si. The initial SOI layer stack consists of 85 nm (100)-oriented Si (top-Si), 145 nm SiO_2 as the buried oxide (BOX), and 775 µm (100)-Si as substrate. The wafer was diced into square pieces with a side length of 15 mm. Regardless of whether the Si-NWs were embedded in SiO_2 or Si_3N_4, the top-Si was thinned down and served as the Si-NW. Although the bond interface was not the Si-NW itself, high initial roughness of the remaining Si layer could have been passed on to the upper layers. Therefore, it was imperative to keep the bond interface as smooth as possible to successfully fabricate Si_3N_4-embedded Si-NW samples. Four different approaches to the initial thinning down procedure were investigated. Using the best of these four methods determined, the SiO_2- and Si_3N_4-embedded NW samples were fabricated.

2.1. Thinning Down the Top-Si

For removing the bulk load of excessive top-Si, four methods were investigated and evaluated in terms of the achieved root mean square (RMS) roughness. After the rough initial thin-down, the desired Si thickness was achieved by digital etching in HNO_3 and hydrofluoric acid (HF). The impact of increasing cycle counts of digital etching on the roughest and smoothest method of the initial rough thin-down was investigated.

2.1.1. Initial Rough Thin-Down of the Top-Si

In order to roughly thin down the first 80 nm of top-Si, four different processes were explored. The first process was a two-step process and therefore not an obvious solution, while the other processes were established processes to etch Si. The tested processes were 1) dry thermal oxidation (TO) and subsequent wet etching in buffered oxide etch (BOE); 2) wet etching in tetramethylammoniumhydroxide (TMAH); 3) isotropic radical etching (IRE); and 4) inductively coupled plasma–reactive ion etching (ICP–RIE). The samples used for these tests originated from a 6 inch Si wafer, with p-type doping (B) corresponding to a resistivity of 1–100 Ωcm and a thickness of 675 µm. The wafer was diced into quadratic pieces with a side length of 15 mm. In order to grow a thermal oxide (I), a Centrotherm Centronix 1200 furnace was used at a temperature of 1200 °C. This temperature was above the threshold where SiO_2 begins to viscously flow,[14,15] so that the grown oxide and the BOX did not induce stress-related damages into the thin top-Si. From the molecular weight and density of SiO_2 and Si, the thickness of the consumed Si could be estimated to be 45% of the measured resulting thermal oxide thickness, [16, chapter 13.2]. The Deal-Grove model was used to estimate the required oxidation time to fully consume the top-Si layer.[17] The samples were oxidized shorter than this estimate to prevent a full oxidation and the resulting layer stack of thermal oxide, top-Si and BOX were measured with an Accurion nanofilm ep4 spectroscopic ellipsometer. Before performing atomic force microscopy (AFM), the samples, processed according to method (I), were immersed in BOE for 2 min to completely remove the thermal SiO_2. For the wet chemical etching (II), the native SiO_2 on the samples was removed with 1% HF prior to etching with TMAH. The etch rate and roughness of the remaining Si were strongly dependent on the choice of TMAH solution. In this work, a solution consisting of 25% TMAH and isopropyl alcohol (IPA), mixed in a 5:1 ratio, as described in ref., [18], was used. To increase the etch rate and smoothness of the resulting surface[18] further, the etching took place at 75 °C, instead of 60 °C. For the radical etching process (III), an Oxford Instruments Plasmalab PRS 90 barrel reactor was used with O_2 and SF_6 as reactive gases at a pressure of 810 mTorr and an high frequency power (P_{HF}) of 100 W. For the ICP–RIE process (IV), an Oxford Instruments PlasmaPro 100 Cobra ICP RIE system was used with a flow of 30 sccm O_2 and 15 sccm SF_6 at a pressure of 15 mTorr and only 20 W high frequency power.

The resulting surfaces were characterized by a DS95 AFM from DME in alternating current mode. Two samples per preparation method were measured in three areas each, with a size of $2 \times 2\ \mu m^2$. Measurement data was postprocessed with the software Gwyddion 2.56.[19]

The surface morphology after each thinning method is shown in **Figure 1**. The surface roughness appeared largely to be uniformly distributed as hills and valleys, being a few nanometers deep and wide. Method III shows an exception: there were larger hills of about 100 nm in diameter distributed across the entire surface.

Figure 2 illustrates that all methods resulted in a subnanometer RMS roughness, while the highest value for the IRE process was on the order of 0.55 nm and therefore slightly above the acceptable RMS roughness for bonding of 0.5 nm.[20] The lowest roughness was obtained by method (I) with around 0.14 nm. As the etching part is self-limited and stops at the Si layer, this method provided best overall results and process control for rough thinning of top-Si. The possible influence on the surface roughness by the BOE component in method I was investigated by comparing the etched Si to the sample state after TO, see

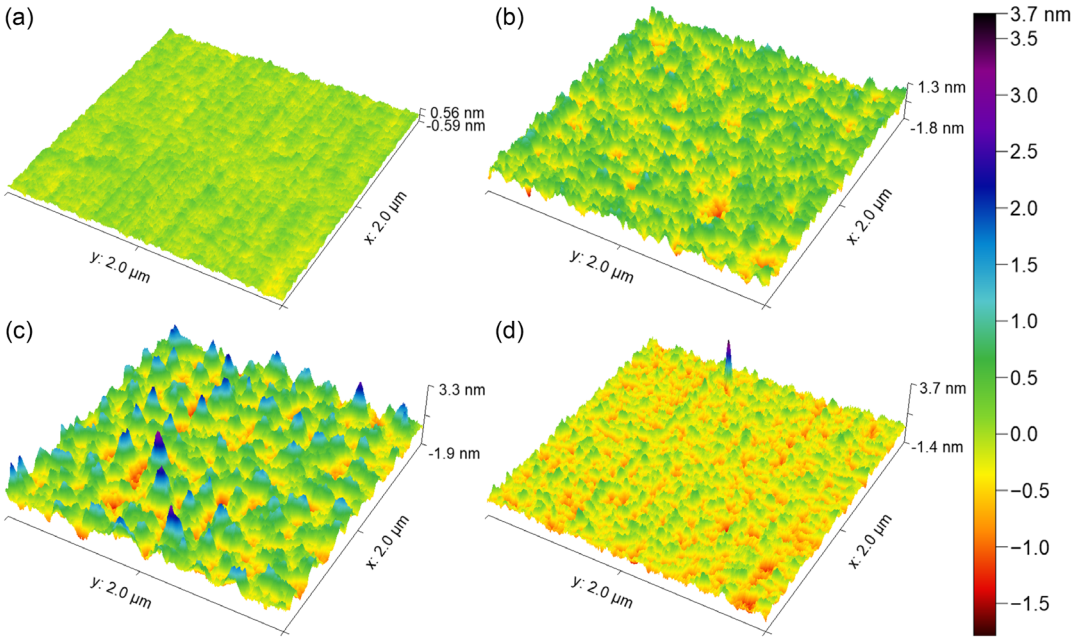

Figure 1. AFM measurements on bulk-Si samples prepared with the following methods. a) TO and removal of the SiO_2 with BOE. b) Wet etching in 25% TMAH and IPA, mixed in a ratio of 5:1, at 75 °C. c) IRE. d) ICP–RIE.

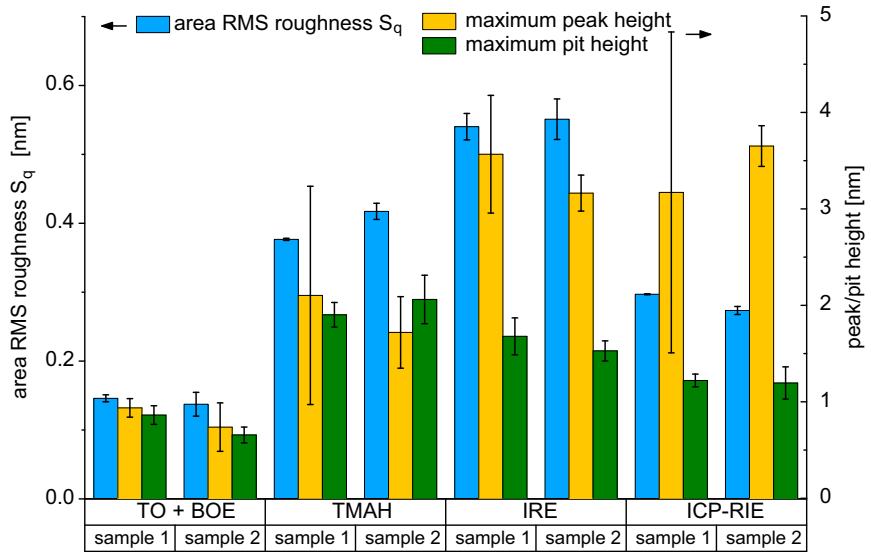

Figure 2. Area RMS S_q, maximum peak height, and maximum pit height for each of the Si thickness reduction methods. For each bar, an individual sample was fabricated. Error bars show standard deviations per variable and sample.

Figure 3. It was found that the RMS roughness reduced from 0.22 ± 0.02 nm prior to etching to 0.14 ± 0.01 nm after the BOE step. The AFM image in Figure 1 shows the occurrence of multiple particles with height up to 2 nm in the oxidized state. These were not detected after oxide removal.

2.1.2. Thinning Down to Required Thickness via Digital Etching

A cycle of digital etching starts with the removal of SiO_2 in BOE or HF and ends with oxidation of Si in HNO_3. The formation of SiO_2 in HNO_3 is described as a self-limiting process, making it the perfect choice for thinning down top-Si in a controlled way. In addition, the grown oxide was reported to be of comparable quality to thermally grown oxide.[21] The oxidizing solution consisted of 69.6% of HNO_3 and deionized water (DI-water) in a ratio of 59:41 and was heated up to 108 °C. Before immersing the samples in the oxidizing solution for 10 min, it was found that one oxidation cycle consumes 0.65 ± 0.1 nm of top-Si and grows 1.4 ± 0.2 nm of SiO_2 on top of the surface. Since the smoothest surfaces were observed with method I, the influence

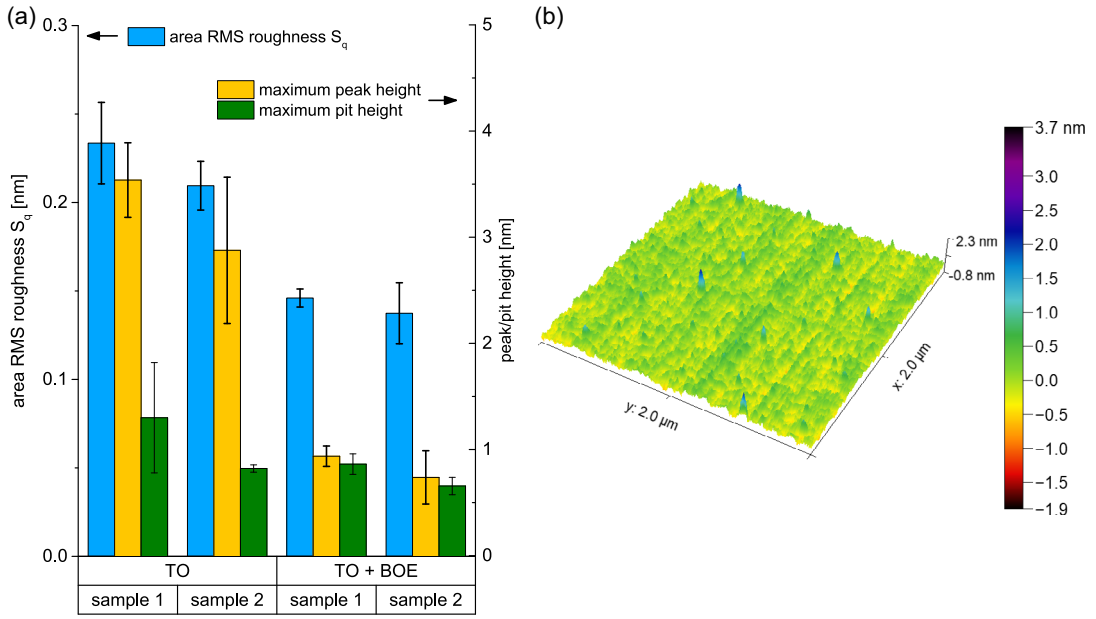

Figure 3. a) RMS roughness S_q, maximum peak height, and maximum pit height of TO before and after BOE etching and b) surface of TO before BOE etching. For each bar an individual sample was fabricated. Error bars show standard deviations per variable and sample.

of multiple digital etching cycles on samples etched by method I was investigated by fabricating six samples of bulk-Si. Out of these samples, two each were etched for one, four, and seven cycles; a selection of the resulting surfaces is shown in **Figure 4**. No negative impact could be seen for etching method I. On the contrary, already after the first cycle, the RMS roughness reduced to 0.11 ± 0.01 nm. In **Figure 5**a, the additional etching cycles performed showed no further RMS roughness reduction. The reduction from 0.14 ± 0.01 nm after the initial BOE etching of the SiO_2 to 0.11 ± 0.01 nm after the first oxidation in HNO_3 means an increase of smoothness of an already atomically flat surface. Since the SOI substrate was atomically flat at the beginning, it was therefore possible to maintain such an atomically flat surface using only chemical processes. This is of significant importance for the confined Si layer, as it is not possible to precisely predict how many digital etching cycles will be needed in order to achieve the required thickness. A variation in RMS roughness or a late saturation point of this value would not only prove difficult for fabrication, but also affect the synchrotron measurements. Furthermore, it is beneficial to perform at least one HNO_3/HF cycle when utilizing this method. Due to the high-quality surface achieved by digital etching, an investigation on its effect on the method III, which yielded the roughest Si surface, was performed. The Si surface etched by method III was measured after one, four, and seven cycles on six different samples (two samples per cycle count) of bulk-Si fabricated by method III. In **Figure 6**, large pinholes with up to 40 nm depth could be seen already after the first etching cycle. Although the application of at least a single HNO_3/HF cycle appeared to reduce the roughness (Figure 5b), it is important to note that different samples were first brought to the various etching stages and then were measured in sequence by AFM. This reduction in thickness, combined with the high variance between samples at the same etch state, suggested that deep impinging and surface damage or oxidation occurred during the IRE step. The random nature as well as severity of these defects rendered this method unviable, regardless of HNO3/HF etching, which even in most favorable cases did not significantly reduce the RMS roughness.

Overall the AFM measurements suggest that each digital etching step has the potential to reduce the RMS roughness. However, extending the number of etching cycles beyond the first one does not further decrease the surface roughness.

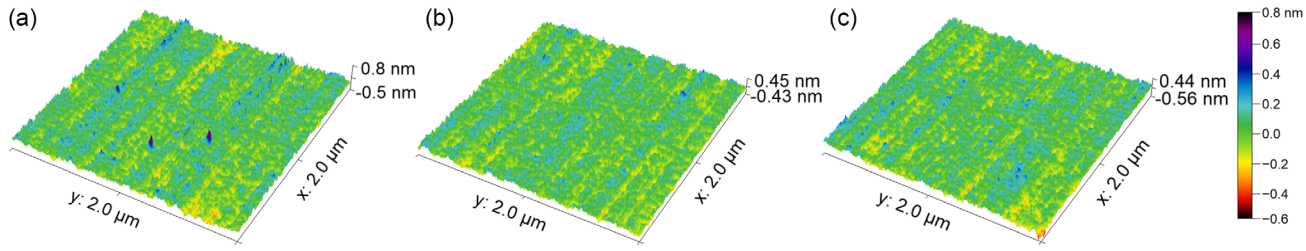

Figure 4. TO and BOE-etched Si samples, which were subsequently digitally etched by oxidizing in HNO_3 (69.6% HNO_3 and DI-water in a ratio 59:41) at 108 °C for 10 min and etching in 1% HF. Surface of samples etched for a) one cycle, b) four cycles, and c) seven cycles.

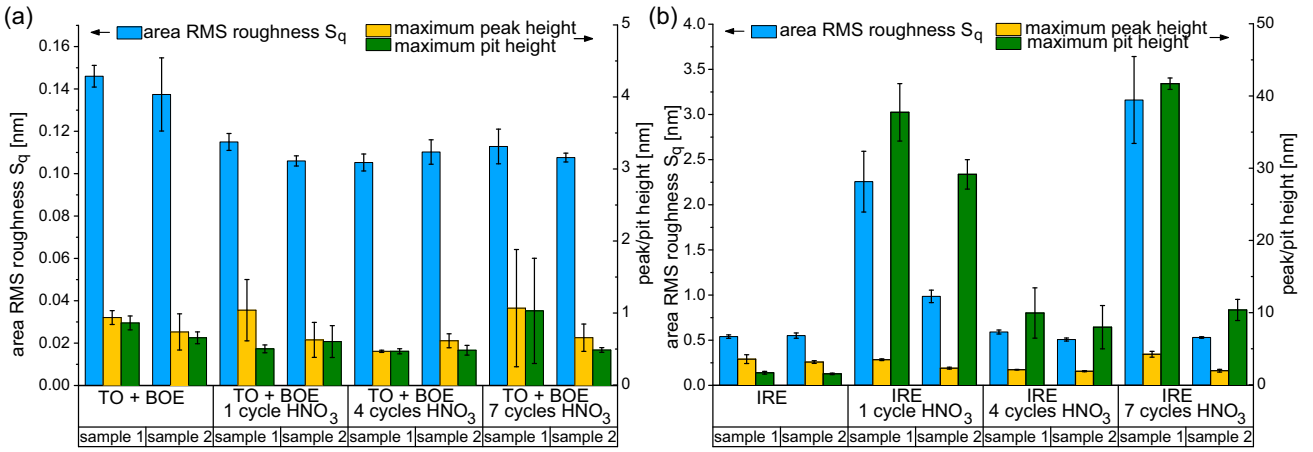

Figure 5. Comparison of the RMS roughness S_q, maximum peak height, and maximum pit height after thinning down Si by a) TO and BOE etching and b) IRE after thinning down and digital etching for one, four, and seven cycles. For each bar an individual sample was fabricated. Error bars show standard deviations per variable and sample.

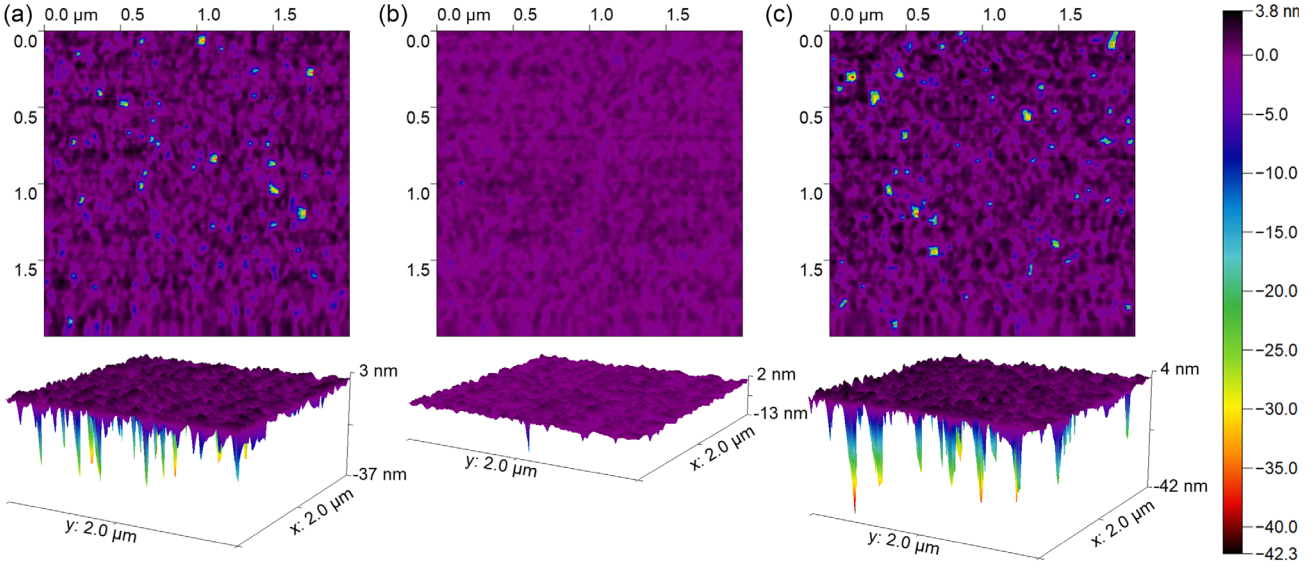

Figure 6. IRE-etched Si samples, which were subsequently digitally etched by oxidizing in HNO_3 (69.6% HNO_3 and DI water in a ratio 59:41) at 108 °C for 10 min and etching in 1% HF. Surface of samples etched for a) one cycle, b) four cycles, and c) seven cycles.

2.2. Sample Fabrication

Thinning down the top-Si by TO is the most controllable process and also yields the smoothest surface. Therefore, all Si-NWs were fabricated by initially thinning down the SOI by means of TO.

2.2.1. Si-NWs in SiO_2

In order to realize Si-NWs embedded in SiO_2, it was sufficient to thin down the Si and oxidize the top side of the remaining Si layer, since its rear side already was in contact with the BOX. The thermally grown oxide was removed with BOE, before digital etching in HNO_3 and HF was employed to reach the desired thickness.[21] SiO_2 was faster removed with BOE than with HF and yielded a slightly rougher surface, but as has been demonstrated in Section 2.1.2, the surface after removing the SiO_2 with BOE was already atomically flat and digital etching flattened the surface even more. The etching cycles of HF and HNO_3 were repeated until the thickness of the remaining Si-NW located below the SiO_2 grown in HNO_3 matched the required thickness. The oxide thickness was sufficient to protect the NWs from oxidation in air. For transportation to the synchrotron facility, the samples were coated with photoresist to prevent exposure of the Si-NW with its top SiO_2 to air. The fabrication of Si-NWs embedded in SiO_2 was concluded by the deposition of a 100 nm-thick Al frame, to prevent the sample from charging up during UPS measurements. After depositing the Al contacts, the samples were coated with photoresist to protect the wet chemical oxide from chemical or mechanical changes during the transport to the synchrotron.

2.2.2. Si-NW in Si_3N_4

In accordance with the Si-NWs embedded in SiO_2, the Si-NWs embedded in Si_3N_4 were fabricated across at least 4×4 mm^2 and to a thickness variation within one atomic layer. In contrast to Si-NWs embedded in SiO_2, Si_3N_4 was grown on the top and rear side of the NWs, since it was not possible to start with SOI, where the buried insulator was Si_3N_4 instead of SiO_2 and the top Si was single crystalline. Getting access to the rear side of the NW can be realized by bonding the sample directly onto another piece of Si (15×15 mm^2), followed by removing the substrate of the original SOI sample and the BOX after processing the top side.

Thinning Down and Rapid Thermal Nitridation: The initial thinning down of the SOI was realized by TO and subsequent digital etching. In contrast to Si-NWs in SiO_2, the thickness of the remaining top-Si had to be thicker than the final Si-NW thickness, because the consumption of Si during the fabrication had to be taken into account. Immediately before the thermal nitridation of the top-Si, the wet chemical SiO_2 was removed with 1% HF. The nitridation took place in an AnnealSys AS-ONE 150 RTP at atmospheric pressure in an atmosphere consisting of Ar and NH_3 achieved by a flow of 1000 sccm Ar and 300 sccm NH_3. The RTP was heated up to 1050 °C with 20 K s^{-1} and held there for 120 s. Benefits of thermally grown Si_3N_4 are a self-limiting growth process,[22] with a strong dependency of the resulting layer thickness on the processing temperature and good interface quality[23] and the possibility to grow layers of up to 3.7 nm with roughness of 0.32 nm as determined by X-ray reflectivity,[24] which is within limits for direct bonding. A schematic cross section of the sample after rapid thermal nitridation is shown in **Figure 7**a.

Deposition of CVD-SiN_x and -SiO_2: On top of the thermal Si_3N_4, about 24 nm of substoichiometric SiN_x were deposited using an Oxford Instruments PlasmaPro 100 ICP–plasma enhanced chemical vapor deposition (PECVD). This layer was used as a spacer between the thermal Si_3N_4 on top of the Si-NW and the CVD-SiO_2 and as a source of hydrogen for passivation of interface states. The tool was equipped with N_2, O_2, He, and a silane mixture of 10% SiH_4 and 90% He, which subsequently will be referred to as silane. The deposition of SiN_x was a cycled two-step process and took place at 350 °C; process parameters are listed in **Table 1**. The first step was the deposition of SiN_x itself, followed by pumping down the chamber for 20 s. The second part was a nitrogen plasma, which was used to reduce the amount of hydrogen in the deposited layer, since SiN_x deposited by PECVD is known to contain large amounts of hydrogen.[25–28] To further reduce the amount of H in the layer after deposition, the samples were annealed in the AS-One 150 °C in Ar at atmospheric pressure at 1050 °C. After the deposition and annealing of SiN_x, about 80 nm of SiO_2 were deposited by the same ICP-PECVD. This layer enabled hydrophilic direct bonding of SiO_2 and also acted as a source of hydrogen for annealing. Similar to the SiN_x process, the SiO_2 deposition was a cycled three-step process at 350 °C; the process parameters are listed in **Table 2**. The first half of the cycle was the deposition itself and was followed by pumping down the chamber for 1 min. In the second half of the cycle, it was attempted to reduce the amount of H using two oxygen plasmas, since PECVD-deposited SiO_2 is known to contain large amounts of hydrogen.[29–31] After the SiO_2 deposition in the ICP–PECVD, the samples were annealed in the RTP again, using the above-mentioned recipe. The ICP–PECVD was chosen for the deposition of SiN_x and SiO_2, since its processing temperature of 350 °C was closest to the temperature used for bonding and therefore reducing the strain of the layers in the latter process. Figure 7b schematically shows the layer sequence on the sample after the deposition of SiN_x and SiO_2.

Table 1. ICP–PECVD process for the deposition of SiN_x at 350 °C.

Step	t [s]	p [mTorr]	P_{RP} [W]	P_{ICP} [W]	N_2 [sccm]	O_2 [sccm]	He [sccm]	10% SiH_4 [sccm]
Deposition	30	10	10	300	200	0	50	25
H reduction	300	30	0	450	200	0	50	0

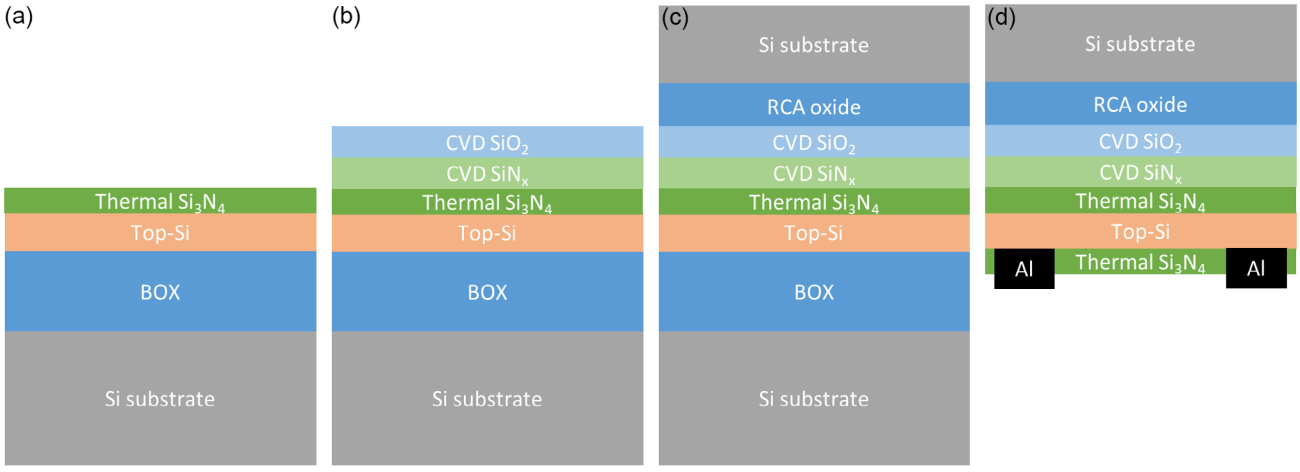

Figure 7. Schematic cross sections for selected processing steps during fabrication of Si-NWs embedded in Si_3N_4; The layers are not to scale. a) Sample after thinning down of the top-Si and with the first layer of thermal Si_3N_4. b) After the deposition of 24 nm SiN_x and 80 nm SiO_2 by ICP–PECVD. c) After polishing the CVD-deposited SiO_2 and RCA cleaning, the SOI sample was bonded to a piece of bulk-Si. d) After removing the SOI substrate by ICP–DRIE and the BOX with BOE, nitridation in an RTP, and deposition of contacts directly onto the Si-NW.

Table 2. ICP–PECVD process for the deposition of SiO_2 at 350 °C.

Step	t [s]	p [mTorr]	P_{Rf} [W]	P_{ICP} [W]	N_2 [sccm]	O_2 [sccm]	He [sccm]	10% SiH_4 [sccm]
Deposition	30	100	7	50	0	60	150	25
H reduction 1	180	30	0	600	0	100	100	0
H reduction 2	240	30	0	1000	0	100	100	0

Mechanical Polishing and Direct Bonding: The surface of the SiO_2 was mechanically polished with a silica slurry for three minutes, applying a pressure of 4.8 kPa in a Logitech PM5. This process reduced the RMS roughness below the required 0.5 nm to be able to directly bond the sample to a piece of bulk-Si.[20] Prior to direct bonding the sample and the piece, bulk-Si were RCA cleaned, named after the Radio Corporation of America, providing a thin wet chemical SiO_2 remaining on top of the bulk-Si for enabling hydrophilic bonding.[15,32] During RCA cleaning, two HF-dips were performed: one after the piranha clean and one after RCA 1 clean. The duration of the HF-dips was 10 s each, which was sufficient to remove the SiO_2 grown on the Si sample, while removing only a small amount of the thick SiO_2 on top of the SOI sample. The RCA clean did not include a third HF-dip to improve the bonding quality. Immediately after the RCA clean, the polished SiO_2 surface of the SOI sample was brought into contact with the polished side of the bulk-Si piece, holding the pieces in place via van der Waals forces and hydrogen bonds.[32] The sample was put into a SÜSS MicroTec SB6e Wafer Bonder. The tool was pumped down to 1×10^{-4} mbar, with the sample kept at 250 °C for 20 h. Following the initial bonding step, the samples were annealed for 10 h at 1100 °C at atmospheric pressure in a N_2 atmosphere with a flow of 5000 sccm N_2. This annealing step increased the strength of the bond interface due to two mechanisms. The first mechanism was the reaction of silanol groups of the opposing SiO_2 interfaces to SiO_2 releasing water, which diffused through the thin wet chemical SiO_2 layer and reacted at the Si interface to SiO_2 and H_2.[32] Some of the generated hydrogen diffused to the interface between the Si-NW and the thermal Si_3N_4 and passivated interface states.[33] The second mechanism was the viscous flow of SiO_2, reported to start between 1000 and 1100 °C, to close bubbles, which might have formed during the initial bonding step.[14,15] For a schematic cross section scheme of the bonded sample, we refer to Figure 7c.

Substrate and BOX Removal and Rapid Thermal Nitridation: After bonding the sample to bulk-Si, the original Si wafer from the SOI-sample was removed using a cycled three-step DRIE in a PlasmaPro 100 Cobra. A single cycle consists of three steps: a deposition step, a breakthrough and a main etching step; process parameters are listed in **Table 3**. In the first step, a polymer was formed and deposited onto the sides and on top of the sample. The deposited polymer protected the bonded interface from being etched along imperfections in the bond interface during the main etching step. During the breakthrough step, reactive ions were accelerated towards the surface of the sample and reacted with the polymer on the top of the sample, while such a reaction did not occur on the sides of the sample. The DRIE process removed 1.3 µm of Si per cycle with a selectivity of 1:1000 between SiO_2 and Si. Therefore, the initial BOX with a thickness of 145 nm was a reliable etch stop, giving a tolerance of almost 100 etching cycles. Following the etching of the SOI substrate, the sample was RCA cleaned, with very short HF dips to keep the BOX intact and protect the Si-NW from oxidation. Immediately before nitridation in the RTP AS-One 150, the BOX was removed with BOE. The sample fabrication of the Si-NW embedded in Si_3N_4 was concluded by locally removing the top Si_3N_4 and directly contacting the Si-NW with Al to prevent the sample from charging up during UPS measurements. For the transport to the synchrotron, the Si_3N_4-embedded samples were coated with resist as well. The finished sample is depicted in Figure 7d.

Table 3. Three steps of the ICP–DRIE process at −10 °C.

Step	t [s]	p [mTorr]	P_{HF} [W]	P_{ICP} [W]	SF_6 [sccm]	C_4F_8 [sccm]
Deposition	2	20	0	1750	5	100
Breakthrough	2	35	55	1750	250	5
Etching	4	50	0	2950	500	5

HRTEM Measurements: After measurement at the synchrotron, focused ion beam (FIB) lamellae were prepared by a FEI Strata400 system with a gallium (Ga) ion beam, and HRTEM images were recorded with a FEI Tecnai G2 F20 at 200 kV operation voltage. After leaving the UHV beamline environment, samples were enpackaged in transport containers which were flushed with N_2 for 5 min and subsequently evacuated to 1 mbar. All samples were then screened from light and transported by air to the TEM facility within 24 h, where they were submitted into HV (1×10^{-6} mbar) to await their processing within the next 14 days.

3. Results

In this section, the results of the fabrication of Si-NWs embedded in SiO_2 and Si_3N_4 will be described. A comparison between ellipsometric measurements and HRTEM images will be made and a brief overview of the results obtained by synchrotron measurements will be presented. A detailed discussion of the synchrotron measurements is beyond the scope of this work and is given in ref. [10–13].

3.1. Si-NWs in SiO_2

Si-NWs embedded in SiO_2 follow a simplified fabrication sequence as compared to the Si-NWs in Si_3N_4. The thickness of the remaining top-Si of every sample was measured by ellipsometry after every step of digital etching. Since the top-Si for Si-NWs embedded in Si_3N_4 had to be thicker after digital etching as compared to Si-NWs in SiO_2, samples with a remaining top-Si deemed too thin to be used for a Si-NW in Si_3N_4 were still be usable as a Si-NW in SiO_2. The thickness of the Si-NWs was measured by ellipsometry and confirmed by HRTEM.[10–12] The energy levels of the conduction and valence band with respect to the vacuum energy for Si-NWs between 1.1 and 5.0 nm thickness[10–13] are shown in **Figure 8** (magenta triangles). The NW thicknesses were determined by ellipsometry and an error of ± one monolayer along <100> Si or ±0.2 nm was

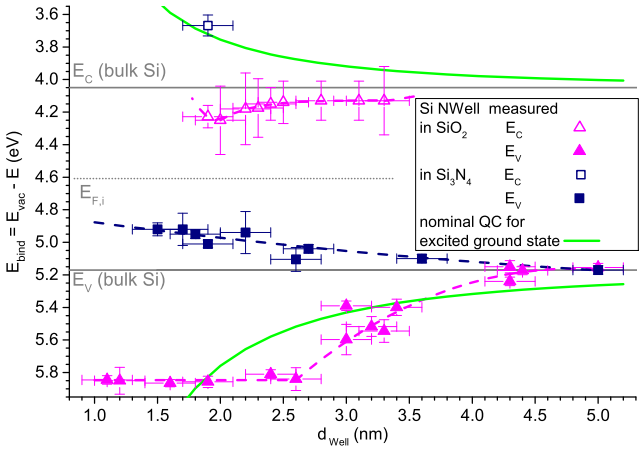

Figure 8. Electronic structure of the valence band edge (measured by UPS) and conduction band edge (measured by XAS–TFY) of Si-NWs thinner than 5 nm embedded in SiO_2 (magenta triangles) and the valence band edge for Si nanocrystals in Si_3N_4 (blue squares) with respect to the vacuum energy. The dashed lines only act as a guide to the eye. The measured energies are shifted with respect to the binding energies expected by only taking quantum confinement and the respective partition of the exciton binding energy (solid green line) into account. Binding energies for the valence and conduction band of Si-NWs in SiO_2 are higher than the energies of bulk-Si (solid grey lines), indicating n-type behavior, while the binding energy of the valence band edge of Si NWs in Si_3N_4 is lower than respective energies of bulk-Si, indicating p-type behavior. For more details refer to other studies.[10–13] The data was acquired during multiple beam times and originally published in ref. [11–13].

assumed. The binding energy for the conduction band edge was measured by grazing incidence XAS–TFY and the binding energy for the valence band edge by synchrotron UPS. Of particular interest is the fact that neither the conduction nor the valence band behave like predicted by conventional quantum confinement (solid green lines). The binding energy of the band edges is larger compared to bulk-Si (grey solid lines), indicating n-type behavior with respect to bulk-Si. The valence and conduction band edges of the NW of 1.9 ± 0.2 nm thickness were measured on the same sample, effectively removing errors due to sample variation.

3.2. Si-NWs in Si_3N_4

The sample fabrication of Si-NWs in Si_3N_4 starts from SOI, as described in Section 2.2.2, with the benefit of a single-crystalline NW having a known low-index orientation. **Figure 9**a shows a HRTEM cross-section image of Si-NW in Si_3N_4 along the <100> direction. The cyan area marks the Si-NW and its thickness is 3.5 ± 0.5 unit cells. With a lattice constant of $a = 0.54$ nm,[34] the thickness is determined to be 1.9 ± 0.3 nm from the HRTEM image and 1.7 ± 0.2 nm measured by ellipsometry. From the NW thickness of another sample (shown in ref. [13]) measured by HRTEM (1.5 ± 0.3 nm) and ellipsometry (1.3 ± 0.2 nm), it is concluded, that there is a constant offset of 0.2 nm between NW thicknesses determined by HRTEM and ellipsometry. This offset can be explained by inaccuracies in the dispersion relations, which have to be assumed for every layer in the ellipsometric model. The single-crystalline nature of the NWs eliminates any signal from amorphous Si in UPS measurements as was the case for earlier samples. As a consequence, the signal to noise ratio (SNR) and sensitivity regarding the detected valence band edge increase considerably. The earlier Si-NWs embedded in Si_3N_4 used for measurements of the valence band were fabricated by CVD of Si_3N_4, amorphous Si (a-Si) and Si_3N_4 on (111) Si and subsequent annealing in order to crystallize the amorphous silicon forming small Si crystallites.[10,11] Figure 9b shows the HR-TEM image of one of these samples with a nanocrystal highlighted in the cyan area. While it is not possible to determine the crystalline fraction of Si forming the NW, it is fair to say that the NW in ref. [10] is polycrystalline and thus significantly inferior to a monolithic Si-NW as formed by a thinned-down SOI layer of defined global orientation. The significant improvement in synchrotron UPS characterization was impressively demonstrated by resolving the valence band fine structure, using samples processed in accordance with our findings presented herein.[13] The measured valence band energies for Si NWs are shifted toward lower binding energies with respect to the energy of bulk-Si, as is shown in Figure 8 (blue squares), indicating p-type behavior.

In Figure 8, the binding energy of the valence band of Si_3N_4-embedded NWs of 1.5–5.0 nm is shown. In contrast to conventional quantum confinement, the binding energy of the valence band decreases along with NW thickness. It should be noted that for valence and conduction band measurements of the NW of 1.9 nm thickness, the same c-Si NW sample was used. The measured valence and conduction bands for SiO_2 and Si_3N_4 embedding indicate n- and p-type behavior enabling the fabrication of undoped FETs.

4. Conclusion

We demonstrated the fabrication of single-crystalline Si-NWs embedded in Si_3N_4 of homogeneous thickness across

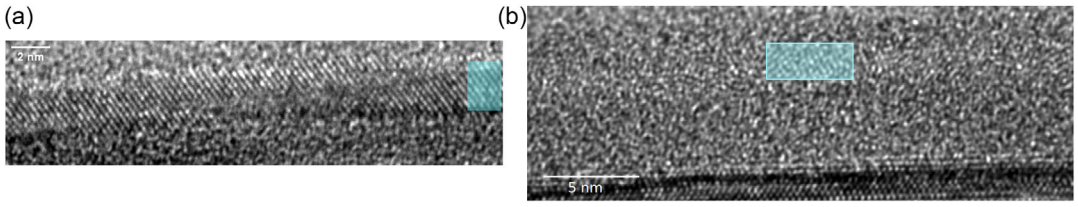

Figure 9. HRTEM cross section of Si-NW embedded in Si_3N_4. a) Fabricated across 15×15 mm^2 by direct bonding and etching through the Si-substrate and BOX with a thickness of 1.9 ± 0.3 nm, view along <100>. b) Crystallized amorphous Si deposited by PECVD embedded in PECVD-deposited Si_3N_4, resulting in polycrystalline Si and a notable fraction of amorphous Si (cyan area) [modified and adapted under common license from ref. [10]].

$15 \times 15\ mm^2$ SOI samples. The challenge of the fabrication of these samples is to grow high-quality thermal Si_3N_4 on the front and rear side of the NW. This was realized by polishing and directly bonding the samples after the front-side nitridation to a piece of Si, subsequently removing the original SOI substrate and the BOX before nitridation of the rear side was carried out. For Si-NWs in Si_3N_4, it was found that ellipsometry yields NW thicknesses which are 0.2 nm thinner as compared to values derived from HRTEM images. From comparison of ellipsometric measurements and HRTEM images, we conclude that the thickness of Si-NWs in SiO_2 measured by ellipsometry matches with HRTEM images. The NWs were fabricated by thinning down the top-Si of SOI. Since a rough surface after thinning down might be passed on to layers deposited on top of the NW, we investigated four different methods of thinning down Si, whereby we found that dry TO is the most controllable process, yielding the smoothest surfaces. The thinning down was concluded by digital etching, using BOE during the first cycle to remove the thermal oxide and to subsequently grow about 1.4 nm of wet chemical SiO_2 in HNO_3. For further cycles, HF instead of BOE is used to remove the wet chemical SiO_2. It was found that even one cycle of digital etching further improves the surface roughness of thinned-down top-Si. With a process established to fabricate Si-NWs in Si_3N_4 across $15 \times 15\ mm^2$ samples, measurements will be done to determine the valence and conductance band energies of different Si-NW thicknesses in Si_3N_4.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

deep reactive ion etching, direct bonding, nanoscale electronic structure shift induced by anions at surfaces, surface roughnesses, ultrasmall nanoscale Si wells

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