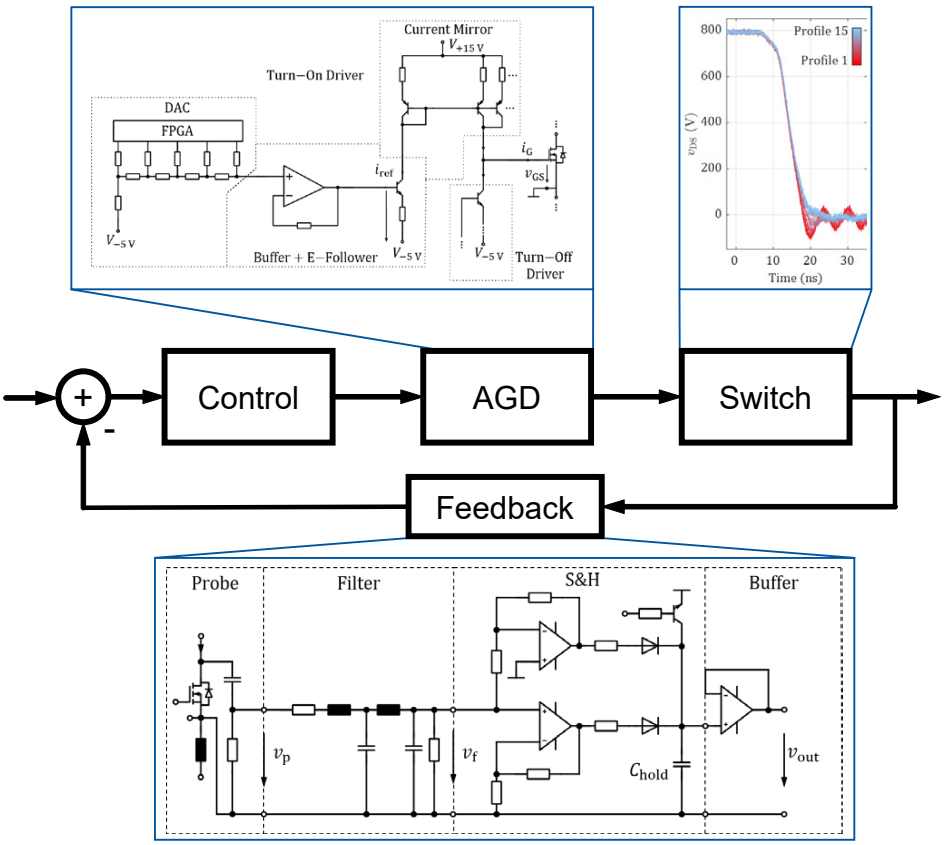
Jochen Henn

Gate Driver Integrated Closed-Loop Control for Electromagnetic Emissions and Switching Losses of Wide Bandgap Power Electronic Converters



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Gate Driver Integrated Closed-Loop Control for Electromagnetic Emissions and Switching Losses of Wide Bandgap Power Electronic Converters

Von der Fakultät für Elektrotechnik und Informationstechnik der Rheinisch-Westfälischen Technischen Hochschule Aachen zur Erlangung des akademischen Grades eines Doktors der Ingenieurwissenschaften genehmigte Dissertation

vorgelegt von
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Vorwort

Diese Dissertation entstand im Rahmen meiner Tätigkeit als wissenschaftlicher Mitarbeiter am Institut für Stromrichtertechnik und elektrische Antriebe (ISEA) der RWTH Aachen University.

Zuerst möchte ich mich bei meinem Doktorvater Herrn Professor Rik W. De Doncker für die Möglichkeit einer Promotion am ISEA bedanken. Das entgegengebrachte Vertrauen und die Freiheiten in der Forschung erlaubten die Anfertigung dieser Dissertation. Professor Stefan Heinen möchte ich herzlich für die Übernahme des Korreferts danken. Weiterhin danke ich dem Konsortium des BMBF Projekts RobKom für die gute Zusammenarbeit und fruchtbare Kooperation.

Außerdem möchte ich allen Mitarbeitenden des ISEA danken. Sowohl denjenigen, die in der Verwaltung und den Werkstätten viele Prozesse im Hintergrund handeln als auch allen wissenschaftlichen Mitarbeitenden, die ein kollegiales Miteinander ohne Konkurrenzdruck leben. Ganz besonders wird dies aber bei all den wissenschaftlichen und nichtwissenschaftlichen Projekten der LEA Gruppe deutlich.

Ob Olympiaden, B12-Runden, Kommunen-Sessions oder diverse Outdoor Meetings. Diese und ähnliche Veranstaltungen und die offene Zusammenarbeit sind nur möglich, wenn genug Menschen etwas mehr als Arbeit im Sinn haben. Deshalb danke ich allen, die Engagement zeigen und Verantwortung übernehmen. Für die Unterstützung bei der Finalisierung meiner Diss danke ich Laurids, Carsten, Vivien, Karl, Severin und Johannes für die vielen Verbesserungsvorschläge. Während meiner zeit am Institut habe ich insgesamt 16 Studenten als HiWis oder Abschlussarbeiter betreut. Ich hoffe, dass sie alle etwas gelernt haben und danke ihnen allen, besonders aber Leonard, Carsten und Laurids für die Unterstützung. Meine Bürokollegen Alex, Rafael und Severin haben sich durch das manchmal lautstarke aber ausdauernde Hand-Auge-Koordinations-Training ebenfalls eine extra Erwähnung verdient.

Wenn ich nicht am Institut oder unterwegs war, mussten mich meine Mitbewohner in der P9 ertragen. Die zehn Jahre dort haben mich vor allem die Menschen gehalten. Hier gilt zuletzt Marius, Lucy und besonders Lea mein Dank. Zum Schluss möchte ich meinen Eltern für die ausdauernde Unterstützung auf meinem langen Bildungsweg und in allen anderen Belangen danken.

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Abstract

With the adoption of wide-bandgap (WBG) semiconductor devices such as silicon carbide (SiC) MOSFETs into everyday applications such as dc-dc converters and traction inverters, new challenges are faced. The superior characteristics of SiC in terms of lower switching losses compared to silicon (Si) insulated-gate bipolar transistors (IGBTs) lead to increased power densities which are advantageous for mobile applications. However, this advantage comes at the cost of faster switching transitions which are disadvantageous in terms of electromagnetic emissions (EMEs). Additionally, the increased requirements for optimized switching cell designs lead to decreased parasitic elements. Therefore, the characteristics of the switching behavior are shifted into ranges of up to 110 MHz and can cause interference in communications or multi-media applications.

There are three major countermeasures against electromagnetic interference (EMI) caused by WBG converters. Firstly, apply filters to the output of the source of the emissions. Secondly, apply filters to the input of sensitive equipment to increase their resilience. Finally, change the switching behavior of the semiconductor devices, which are the main source of electrical disturbances, to account for their EMEs. Applying filters adds cost, weight and space requirements which decrease the advantages of WBG converters. Changing the switching behavior allows stopping the EMI at its source and opens additional degrees of freedom during the design phase. Today the switching behavior is adjusted during the design phase by increasing the gate resistance until all EME requirements are met in the worst-case scenario. Once the design is finalized, this static approach does not allow for more efficient operation during low EME operating conditions or to take changes in the switching behavior into account.

This work presents a gate driver integrated EME control loop which makes use of an adaptive gate driver and analyses and adjusts the switching characteristics to meet a given EME requirement. This way, the drawbacks of a static design choice are overcome and the gate drivers can adjust their output to changing conditions with little outside input. In comparison to a conventional gate driver the proposed method requires an adaptive gate driver (AGD), a way of sensing the switching behavior and control logic that is integrated into the driver. Each of these elements will be presented in detail and the control logic will be laid out in their respective chapters.

Finally, an evaluation of the control performance during continuous three phase inverter operation based on loss and emission measurements will be done. This allows to assess the dynamic compromise between EME and additional losses.

Contents

1 Introduction

In the sixth assessment report (AR6) of the intergovernmental panel on climate change (IPCC), 234 authors from 66 countries evaluate the changes in the earth's climate and provide an outlook on the consequences of the changing climate [1]. To summarize the report, three aspects are highlighted in the corresponding press release [2].

- Faster warming: Without immediate, rapid and large scale reduction in greenhouse gas emissions, limiting warming to close to 1.5 °C or even 2 °C will be beyond reach

- Every region faces increased changes: An increased temperature shifts weather towards its extreme variances. Heat waves, changing seasons, more intense rainfalls, rising sea levels and many more effects are expected to occur.

- Human influence: The last century of industrialization without considering greenhouse gas emissions, is a major reason for the climate change. However, AR6 shows that there is a potential for stopping or even reversing climate change if strong, rapid and sustained reductions in greenhouse gas emissions can be achieved.

One aspect of a possible reduction of greenhouse gas emissions is the mobility sector. By partially electrifying cars, trucks and buses, Germany aims to reduce the emissions in the mobility sector by 47.5 % from 181 Mt CO_2 equivalent in the year 2000 to 95 Mt CO_2 equivalent in the year 2030 [3]. This transition to electric vehicles is now ramping up. The number of battery electric vehicles registered in Germany increased elevenfold between Q2 of 2018 and Q2 of 2022 [4]. All of these vehicles are powered by an electric drivetrain, which includes a traction inverter.

Power density and efficiency are especially important for mobile power electronic applications. Lower weight and fewer losses increase the range of electric vehicles and decrease the transportation sector's energy need. Therefore, these aspects are in the focus of research for power electronic converters. In recent years, silicon carbide (SiC) replaced silicon (Si) as semiconductor material for traction inverters. The faster switching characteristics of SiC lead to a notable increase in efficiency. However, the gain in efficiency is counteracted by increased requirements in terms of electromagnetic interference (EMI) filtering and design of the power electronic converter.

Conventional approaches balance efficiency and electromagnetic emission (EME) for worst-case scenarios during the converters design phase. This way, potential of a higher uti-

lization, especially in dynamic load scenarios, is left unused. Switching characteristics of semiconductor devices can be influenced by their gate drivers [5]. Therefore, this work introduces a gate driver integrated closed-loop control of the EME and switching losses. With this, it is possible to dynamically adapt the EME according to a chosen set point.

1.1 Motivation and Background

An extensive review of gate driver related research shows the potential of intelligent gate drivers for future power electronic converters [6]. By enabling gate drivers to dynamically change the switching characteristics of the accompanying semiconductor devices, a new degree of freedom in converter design is enabled. Power electronics do not have to be designed purely for their worst case operating point, but the flexibility an intelligent gate driver provides, can be used to operate the converter in an optimized manner for many operating points.

An intelligent gate driver is characterized by its capability to adapt the gate driving characteristics based on the evaluation of feedback and the integrated control logic. Therefore, three components are needed for a gate driver integrated closed-loop control. Firstly, an adaptive gate driver (AGD), which provides the capability to change the switching characteristics of the semiconductor devices dynamically. Secondly, a means of measuring the switching characteristics, switching losses or EME. Finally, integrated logic to evaluate the feedback and adjust the switching characteristics according to a target.

1.2 Research Objectives

Recent research in the fields of AGDs, sensors and gate driver control reveals concepts for each aspect that lead to more intelligent drivers. For adaptive drivers, current source drivers [7]–[9], switched mode drivers [10] and adaptive resistive drivers are considered [11]–[17]. They all allow some form of adaption of the driving characteristics during the switching transitions. When the switching events are successfully adapted, an intelligent driver needs knowledge of the changes occurring to close the control loop. Therefore, sensing solutions like capacitive coupling [18], [19] of the voltage slopes or an evaluation of the current slope via a parasitic inductance [20] are proposed. After the feedback loop is closed, an evaluation of the switching behavior has to be done and the gate driving characteristics have to be adapted. This adaption is done by integrating a direct feedback path into the gate driver in [21], [22] and [23]. This way, closed-loop control over the voltage and current slopes is achieved for singular set points.

All presented closed-loop control approaches lack the flexibility of either changing the set points or adapting the control algorithm. Consequently, this work combines an adaptive current-source gate driver [24], a capacitive switching-voltage sensor [25] and a dynamic control algorithm [26] to form a driver integrated closed-loop controller that is able to control the EME of a traction inverter.

1.3 Outline of this Thesis

The structure of this thesis is adopted from the control circuit depicted in Fig. 1.1. This control loop is closed in between two switching events. Therefore, one switching event is evaluated and the gate driver adapts the next according to the control output. Firstly, the AGD, then the sensors and afterwards the control algorithm is presented. The final chapter evaluates the control performance based on its control capabilities in a three-phase inverter application.

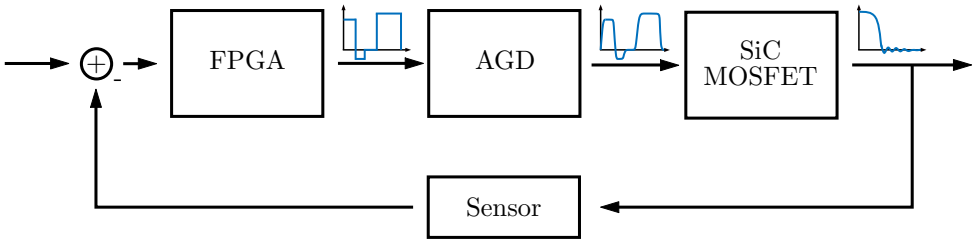


Figure 1.1: Control loop introduced in this thesis.

Chapter 2 - Adaptive Gate Drivers This chapter encompasses an extensive introduction to gate drivers. By analyzing the general switching behavior of metal-oxide semiconductor field-effect transistor (MOSFET) devices, a baseline for the introduction of fixed, adaptive and controlled gate drivers is given. Afterwards, the driver topology employed in this thesis is presented. Based on measurements with this driver and simulation results, a metric for the assessment of the EME is introduced.

Chapter 3 - Sensing the Switching Behavior In this chapter, the sensing elements providing the feedback for the controller are presented. Firstly, the bandwidth requirements for the sensors are derived from the switching characteristics of the SiC MOSFETs used in this work. Secondly, the sensor topology is introduced. A modular structure for the sensor is proposed, which allows to sense two different switching characteristics. Therefore, the probe, filter, amplification and Sample & Hold (S&H) stages are presented. Subsequently, the sensors are evaluated using synthesized test signals and measurements recorded on the testbench.

Chapter 4 - Closed-Loop EME Control Algorithm Chapter 4 gives an introduction into the control algorithm which is implemented on the field-programmable gate arrays (FPGAs) on the drivers. An overview over the sparse literature in this field is given and the modules of the control algorithm are presented. Two examples - dc and ac - showcase the controller's capabilities in terms of adapting the switching behavior dynamically.

Chapter 5 - Evaluation of Control in Three-Phase Converter Operation The fifth chapter evaluates the control performance in a three-phase converter application. An introduction into the measurement setup is given by presenting all measurement devices and methods. For every experiment, time and frequency domain measurements, the loss power information and switching characteristics are recorded. Afterwards, three sets of experiments are used to congregate measurement data. A variation of the set points allows an evaluation based on the metric introduced in chapter 2. Then, the operating voltage and load current are varied to test the controller's resilience against changes in the operating conditions.

Chapter 6 - Conclusions and Outlook The final chapter compiles the contributions of the previous chapters and emphasizes the findings of every topic. Additionally, an outlook towards future work is given.

2 Adaptive Gate Drivers

This chapter introduces the fundamental half-bridge topology and its parasitics and derives the switching behavior of MOSFETs. Furthermore, a brief introduction into state-of-the-art gate drivers, which are available for purchase and presented in research, is given. Afterwards, AGDs proposed in research are analyzed and an analysis of the dependency between switching characteristics and gate drivers is presented. Additionally, a detailed description of the current source gate driver developed for this thesis is given.

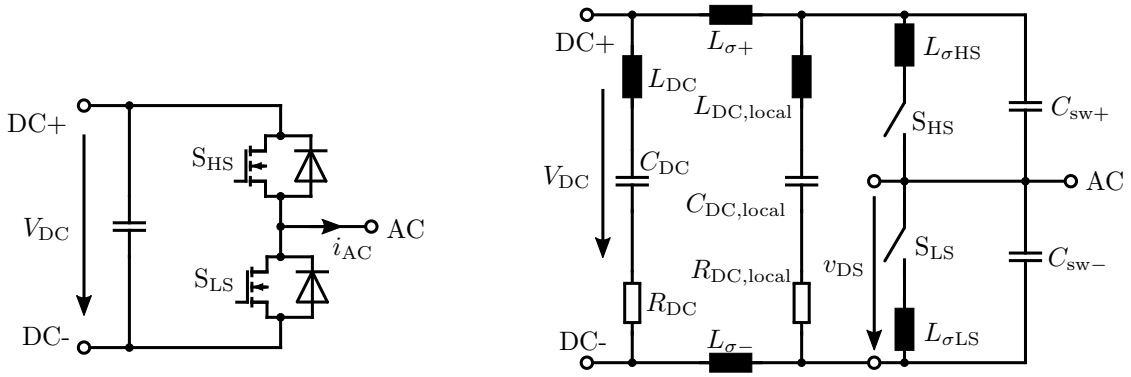
2.1 MOSFET Switching Behavior

This section discusses the parasitic elements and the general MOSFET switching behavior of MOSFETs in a half-bridge topology. The half-bridge topology and the parasitic elements of the dc-link layout, as well as the semiconductor devices are introduced first. Afterwards, generic switching events are presented to build an understanding for the following analyses.

2.1.1 Parasitic Elements in a Half-Bridge Setup

Figure 2.1a depicts a generic simplified half-bridge leg, which is the base component of most power electronic converters. For measurements of the EME behavior, the negative converter potential is not connected to ground. Instead, it is referred to as DC-, whereas the positive supply voltage is denominated as DC+. Both are fed through a line impedance stabilization network (LISN) which decouples them from the reference ground. The full measurement setup will be introduced in Section 5.1. For a three-phase traction inverter, three of these half-bridges, each containing a high- (S_{HS}) and low-side (S_{LS}) switch, are connected in parallel and share a global dc-link capacitance. The AC connection is the phase output and connected to the load.

To model the real switching behavior of the half-bridge, the equivalent circuit must be extended by the parasitic elements, as shown in Fig. 2.1b. A major difference is the extension of the dc-link capacitor C_{DC} by a local dc-link capacitor $C_{DC,local}$. Because the bulk capacitance is realized with foil or electrolytic capacitors which exhibit a high equivalent series inductance (ESL), referred to as L_{DC}, a smaller ceramic capacitor is



(a) Simplified half-bridge circuit.

(b) Half-bridge circuit with parasitic elements and simplified switches.

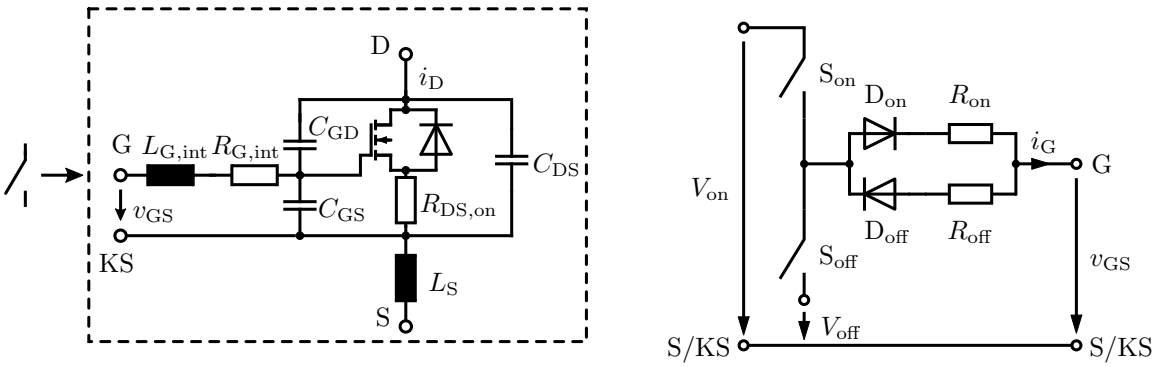
Figure 2.1: Two stages of simplification for a half-bridge circuit.

added in close proximity to each half-bridge. This local capacitance is represented by the string containing $C_{\mathrm{DC,local}}$. In between the capacitor stages $L_{\sigma+}$ and $L_{\sigma-}$ represent the parasitic inductance of the printed circuit board (PCB).

The switching cell itself comprises the two switches $\mathrm{S_{HS}}$ and $\mathrm{S_{LS}}$ and the parasitic inductances $L_{\sigma,\mathrm{HS}}$ and $L_{\sigma,\mathrm{LS}}$ of the PCB layout. In addition to the PCB parasitics, the semiconductor devices are modeled by including the capacitors shown in Fig. 2.2a. Furthermore, the parasitic capacitances between the output node AC and DC+ or DC-, $C_{\mathrm{sw+}}$ and $C_{\mathrm{sw,-}}$, are especially critical, because the voltage across them changes each switching cycle. This leads to an increase amount of disturbance currents throughout all of the setup.

The simplified switch model used in Fig. 2.1b is extended by the most important parasitics in Fig. 2.2a. For example, $R_{\mathrm{G,int}}$ is a resistance placed by the semiconductor manufacturer to limit the switching speed and provide a minimal amount of damping to the gate source voltage v_{GS}. Damping is necessary because the gate connection is inherently afflicted with an inductive behavior represented by $L_{\mathrm{G,int}}$. This inductance is caused by the combination of leg and bond wire length in a TO-247-4 package for example. Similarly, the source inductance L_{S} is located in the main current path to represent the ESL of the bond wires and packaging of the semiconductor device.

In parallel to the idealized MOSFET and diode, the output capacitance C_{DS} is located. MOSFET datasheets list C_{OSS} instead of C_{DS}, but both represent the same capacitance. This capacitance shows a high voltage dependency and has a major impact on the switching speed, because it has to be charged or discharged with every switching cycle. Going counterclockwise around the switch, the next capacitance C_{GD} is located between the gate and drain connections. This capacitance, also called feedback or miller capacitance, will force its charge into or pull it out of the gate when v_{DS} changes. Lastly, on the bottom left side the gate capacitance C_{GS} is connected between the gate and Kelvin-source (KS)



(a) Detailed equivalent circuit of a MOSFET.

(b) Push-pull driver stage.

Figure 2.2: Detailed replacement for the simplified switches in the previous figure and simplified equivalent circuit of a conventional push-pull driver stage.

pins. For MOSFETs it defines the on resistance $R_{DS,on}$ and therefore, turns the device on and off.

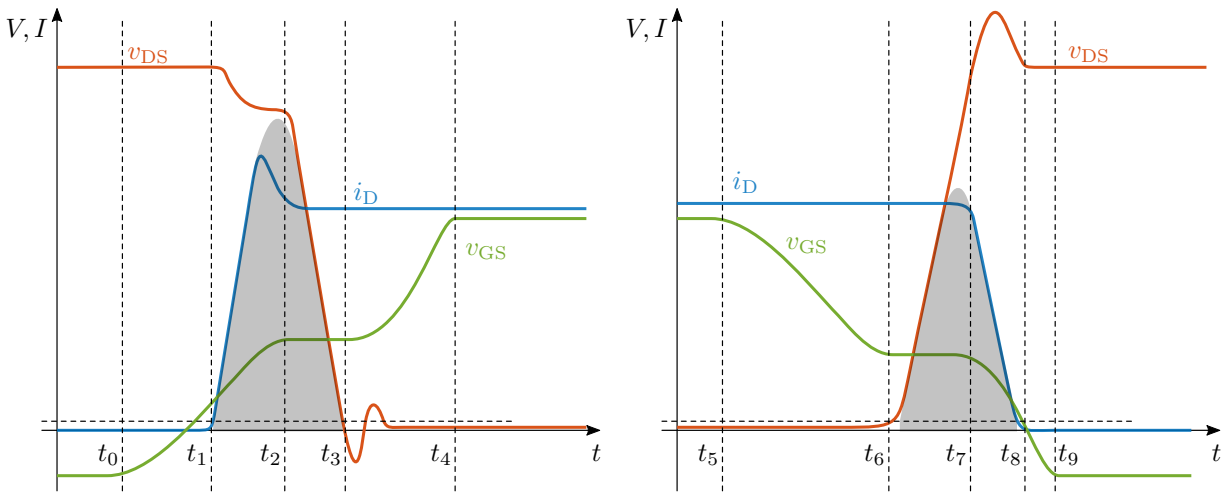
Figure 2.2b depicts a generic conventional push-pull voltage gate driver. Its simple structure utilizes two switches and a separate path for turn-on and turn-off are its main advantage. The outside circuitry decides which voltages are used for turn-on V_{on} and turn-off V_{off}. Both of them are referenced from the source (S) or kelvin source (KS) pin of the MOSFET, which is connected to the gate (G) terminal.

2.1.2 Generic MOSFET Switching Behavior

Figure 2.3 depicts both, the turn-on and turn-off switching processes of a voltage driven MOSFET. This behavior will be used as a reference in the simulation model and is close to the real driver module used in Section 5.2. The step-by-step behavior is described in Table 2.1. Additionally, the gray areas between t_1 to t_3 and t_6 to t_8 mark the shape of the instantaneous power loss. To calculate the switching losses, integration borders for the loss calculation have to be set. They are defined as 10 % of either the voltage or current waveforms for the start and end points.

Table 2.1: Step-by-step description of a pair of generic switching processes.

Time	Type
$t_0 < t < t_1$	The turn-on process starts by charging the gate up to the threshold voltage $V_{\mathrm{GS,th}}$.
$t_1 < t < t_2$	After crossing $v_{\mathrm{GS,th}}$ the current through the device increases and according to the $^{\mathrm{d}i}/_{\mathrm{d}t}$ and L_{S} the voltage across the device drops.
$t_2 < t < t_3$	At t_2, the current starts to settle into its dc value and v_{DS} decreases. During this time, C_{GD} is discharged towards drain and pulls current out of the gate. This causes what is known as the Miller plateau on the gate voltage v_{GS}.
$t_3 < t < t_4$	After v_{DS} declined, a negative overshoot occurs and the gate is charged to V_{on} to ensure the minimum $R_{\mathrm{ds,on}}$ and therefore lowest conduction losses. v_{DS} will settle to $v_{\mathrm{DS}} = i_{\mathrm{D}} \cdot R_{\mathrm{ds,on}}$.
$t_5 < t < t_6$	As a first step during the turn-off process, the gate voltage is lowered until v_{DS} starts to increase.
$t_6 < t < t_7$	Due to the further rise of $R_{\mathrm{ds,on}}$, v_{DS} increases to V_{DC}.
$t_7 < t < t_8$	At this point, the diode of the opposite switch can take over the current i_{D} and it decreases to zero. This $^{\mathrm{d}i}/_{\mathrm{d}t}$ causes a voltage overshoot and oscillation which is defined by L_{S}.
$t_8 < t < t_9$	After the voltage commutation the gate is further discharged down to V_{off} to ensure a safe off state of the device.



(a) Generic MOSFET turn-on event.

(b) Generic MOSFET turn-off event.

Figure 2.3: Generic turn-on and turn-off events of MOSFETs driven by a conventional voltage driver.

2.2 Overview of Gate Drivers

This section focuses on the actuator of the control loop proposed in this thesis. As highlighted in Fig. 2.4, the AGD is responsible for converting the logic-level gate signals into gate voltages, which in turn influence the switching characteristics of the semiconductor device.

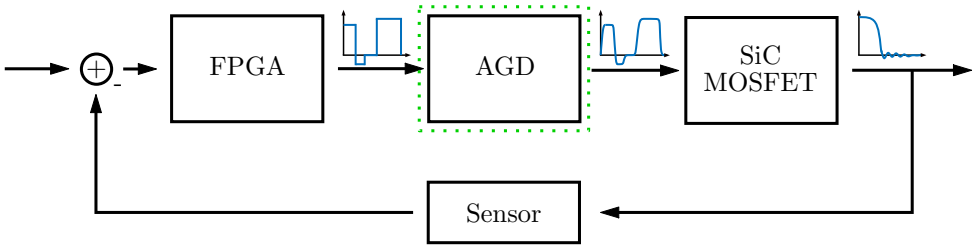


Figure 2.4: Control loop emphasizing the adaptive gate driver.

Non-adaptive gate drivers allow the adjustment of the otherwise static switching behavior, even after the design phase of the power electronic converter. Thus, the switching behavior can be influenced and adapted to the application requirements, even after the final hardware design. Since the research focus of traction inverters shifted away from new topologies and more towards improving the behavior and characteristics of existing converters, adaptive gate drivers were drawn into the light. Thus, increased integration efforts and the demand for highly utilized power electronic converters for mobile applications lead to an increased availability of features for conventional gate drivers. However, their behavior is still static over time and does only allow a very limited adaption to changing requirements.

A conventional gate driver fulfills several tasks. Firstly, it amplifies the logic level input to voltage levels, which set the semiconductor device in a safe on or off state. Secondly, in case it is driving a high-side switch in a half-bridge topology, the gate driver and its power supply have to provide galvanic isolation. Additionally, logic-level safety features such as glitch detection and various protection features can be implemented into gate drivers. Examples for protection features in commercially available drivers are:

- Overcurrent protection via desaturation detection
- Overvoltage protection or safe turn-off after a short circuit
- Signal-level resilience features

In general, gate drivers can be categorized into the three groups, non-adaptive gate drivers, adaptive gate drivers and controlled drivers, as listed in Fig. 2.5. In the following, these three categories are discussed in detail.

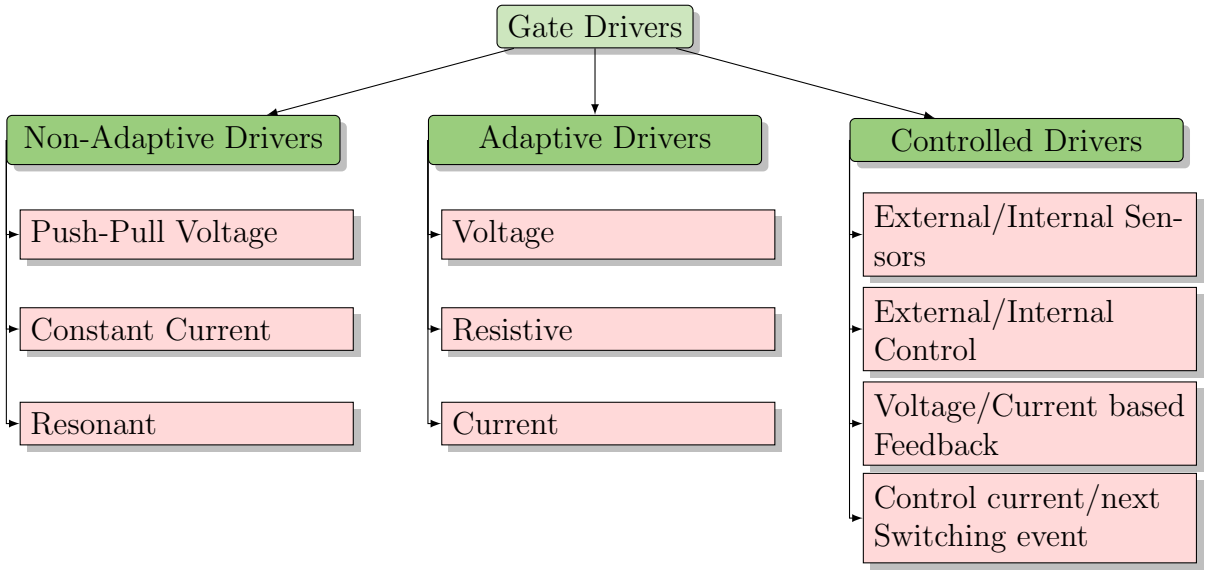


Figure 2.5: Categorization of gate driver topologies (green) and their most common permutations (red).

2.2.1 Non-Adaptive Gate Drivers

Commonly used voltage gate drivers are push-pull voltage drivers, as depicted in Fig. 2.2b. They allow easy design choices, which are limited to turn-on and turn-off voltages, turn-on and turn-off resistances, maximum gate currents and elementary protection features. Therefore, they provide an easy integration, low number of components and simple control. The advantages lead to one of the biggest disadvantages - their lack of adaptability. Once the choices are made, they are manifested into hardware and changing them afterwards requires a redesign or change of components.

Modern, commercial gate drivers include semi-adaptive features, such as safe turn-off after a short circuit current is detected. In this case, they include a short circuit detection and incorporate a secondary turn-off path which can be equipped with a higher gate resistance. This way, the device can turn-off the overcurrent safely without risking destruction by overvoltage. Several manufacturers offer drivers with this capability [27], [28]. Instead of only adapting the switching event during a fault, this next driver offers this capability at the cost of an additional input and a secondary set of output pins [29]. Additional control over the switching instance can be achieved by using a driver which allows setting the timing characteristics of a two step voltage output before operation [30]. The only commercially available current source driver which supports adjusting the gate current does so by using an analog input voltage and allows adjustment between constant 50 mA and 1 A for turn-on. However, this driver is rated for only 100 V operating voltage. Since traction inverters in the mobility sector require higher operating voltages and higher gate currents, this driver is not suitable.

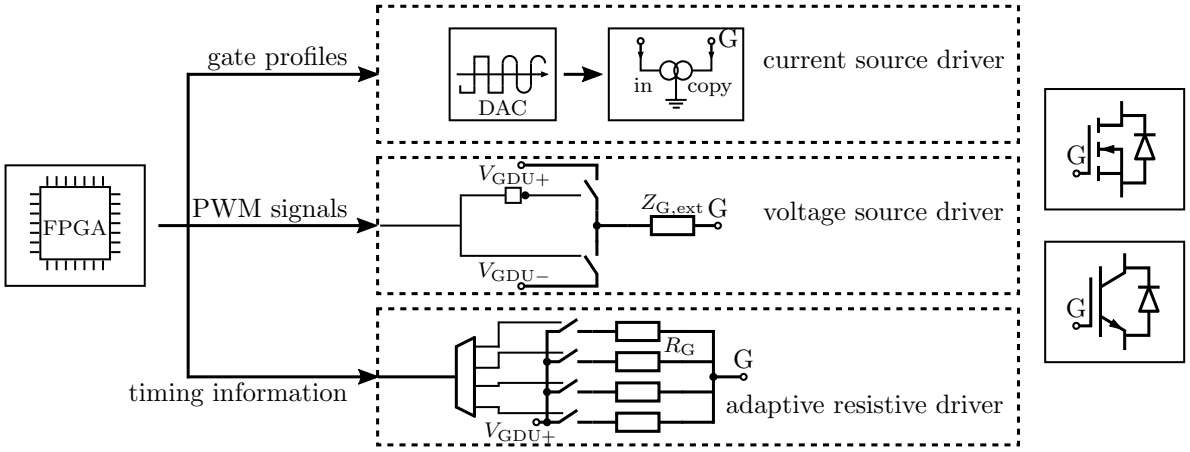


Figure 2.6: Different driver topologies allowing an adaption of the gate voltage during the switching instance [6].

2.2.2 Adaptive Gate Drivers

Adaptive drivers are often based on non-adaptive driver concepts such as a push-pull voltage driver, constant current driver or a resonant driver, as listed in Fig. 2.5. The three categories of AGDs mentioned in Fig. 2.5 are presented in the following. Figure 2.6 gives an overview over their general topologies. Current drivers often use current mirrors with adaptive set points [7]–[9], [24] or a combination of fixed amplitude current sources. Voltage source drivers can either have multiple push-pull stages connected to different turn-on or turn-off voltage levels [31] or use a pulse width modulation (PWM) based approach to modulate the gate voltage during the switching instance [10]. Adaptive resistive drivers employ several parallel push-pull stages, each connected to the gate using a different gate resistor [11]–[17]. This allows combining different resistor values throughout the switching event.

In all the given cases, the gate driver influences the switching behavior of the semiconductor device [32].Thus, the main advantage of AGDs is the capability to adjust the switching behavior of the semiconductor power devices and therefore, allowing an optimized adjustment depending on the operation point. Hence, the device stress can be reduced and switching losses decreased [33].

These improvements come at different costs in terms of control and hardware efforts. In comparison to a conventional gate driver, an AGD requires additional control parameters to adjust the gate driving characteristics. This can be realized by establishing communication to a central microcontroller (MCU) or providing local feedback, resulting in a closed-loop controlled driver. These closed-loop controlled drivers are investigated in more detail in the following section. In addition to the control, an increased amount of hardware components is required to employ AGDs. For adaptive resistive drivers as an example, the different gate resistances need to be external components and only the push-pull stages

can be integrated into an application-specific integrated circuit (ASIC). This is due to the power loss in the resistors, which has to be dissipated externally.

AGDs are most beneficial for applications with changing operating conditions and need for a high degree of optimization. In addition to the increased control and hardware effort, monetary cost increases with the number of features. In efficiency or size driven applications, the designer has to evaluate the balance between the advantages and disadvantages of the application of the adaptive gate drivers. Since mobile applications have a high need for power density and efficiency while the load is very volatile, the balance between EME and efficiency is important.

2.2.3 Controlled Gate Drivers

Controlled gate drivers exist in various permutations. In this section especially closed-loop controlled gate drivers are focused. Figure 2.7 depicts the concept of this closed-loop control including different variations. In the following, these variations are discussed.

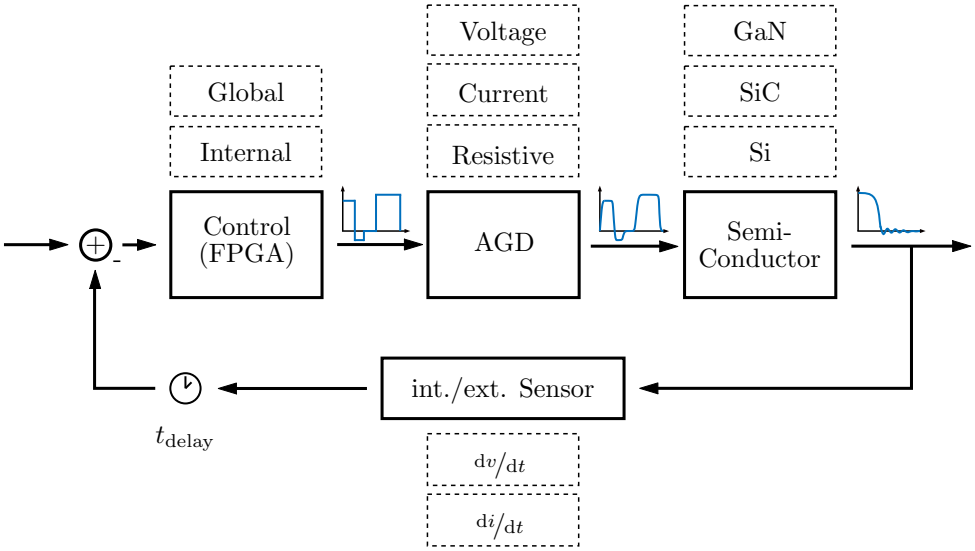


Figure 2.7: Overview over different permutations of control time scope, type of AGD, semiconductor device and type of feedback which are combined to closed-loop controlled gate drivers.

The first differentiation can be made in the time scope over which the control loop is closed. This is indicated by t_{delay} in Fig. 2.7. For very fast control loops, it is possible to adjust the switching transient during the switching event itself. This demands sub-nano second feedback delay t_{delay} for wide-bandgap (WBG) semiconductor devices [23]. Alternatively, the control loop can be closed in between switching events, as it is suggested in [26]. For

direct current (dc) or alternating current (ac) applications, the load current usually has a dynamic, which is an order of magnitude below the switching frequency. Therefore, the measurements done for one switching instance can be used to adjust the next switching event, because only minor changes in the current amplitude occur in between.

Another way of differentiating between different types of closed-loop controlled gate drivers, is to take the sensing element into account. In [34] an external measurement device is used to sense the switching characteristics. In contrast to this, [22] and [35] introduce the first examples of closed loop insulated-gate bipolar transistor (IGBT) drivers using analog circuitry integrated in the drivers. The switching characteristics are controlled using the $^{dv}/_{dt}$ across the semiconductor device as feedback. A common way to integrate a voltage feedback is to add a capacitor in parallel to the semiconductor device to derive the ac components of the voltage across the device [25]. The derivative of the voltage is a current, which is sensed by using a shunt resistor. Sensing the $^{di}/_{dt}$ is often achieved by using the inductance between the source and Kelvin-source pin, if available. A possible implementation is presented in [5]. Possible sensing solutions and the sensors used for this dissertation are discussed in more detail in Chapter 3.

As long as the semiconductor device has a capacitive gate characteristic, all presented gate drivers are capable of driving them. However, the use of gallium nitride (GaN) devices has higher requirements towards the bandwidth of the drivers and feedback sensors. Additionally, the high gate capacitance of a medium-voltage (MV) Si IGBT requires a higher gate current compared to a SiC MOSFET. Therefore, the output stage of the adaptive driver has to match the requirements of the semiconductor gate and the sensors bandwidth has to match the switching speeds.

In terms of control computation and implementation, two approaches are present in [36] or [22], [26]. The first is to use a central controller managing the adjustments to the reference gate signals [36]. The commercially available adaptive driver presented in [30] is employed in [36]. Alternatively, the controller can be integrated into a FPGA [26] or as an analog circuit, which is presented in [22]. The control algorithm employed in the prototype of this thesis is introduced in Chapter 4.

2.3 FPGA Enabled Current Source Gate Driver

The driver module designed for this thesis is an FPGA enabled adaptive current source driver. The driving stage was first presented in [24]. Its main characteristics are defined by the 5 bit resolution of turn-on and turn-off current amplitudes and the 400 MHz update rate for the reference input. The topology, driver control and dynamic characteristics are presented in the following sections.

2.3.1 Driver Topology

The driver topology can be separated into four main parts. The discrete 5 bit digital-to-analog converter (DAC), the buffer amplifier A_{buf}, the translation and the output stage consisting of M_1 and M_2 as well as M_3 to M_7. However, the number of output transistor can be adopted to the requirements of the maximum gate current needed for a specific application. Figure 2.8 depicts all stages of the AGD topology are introduced one by one in the following sections.

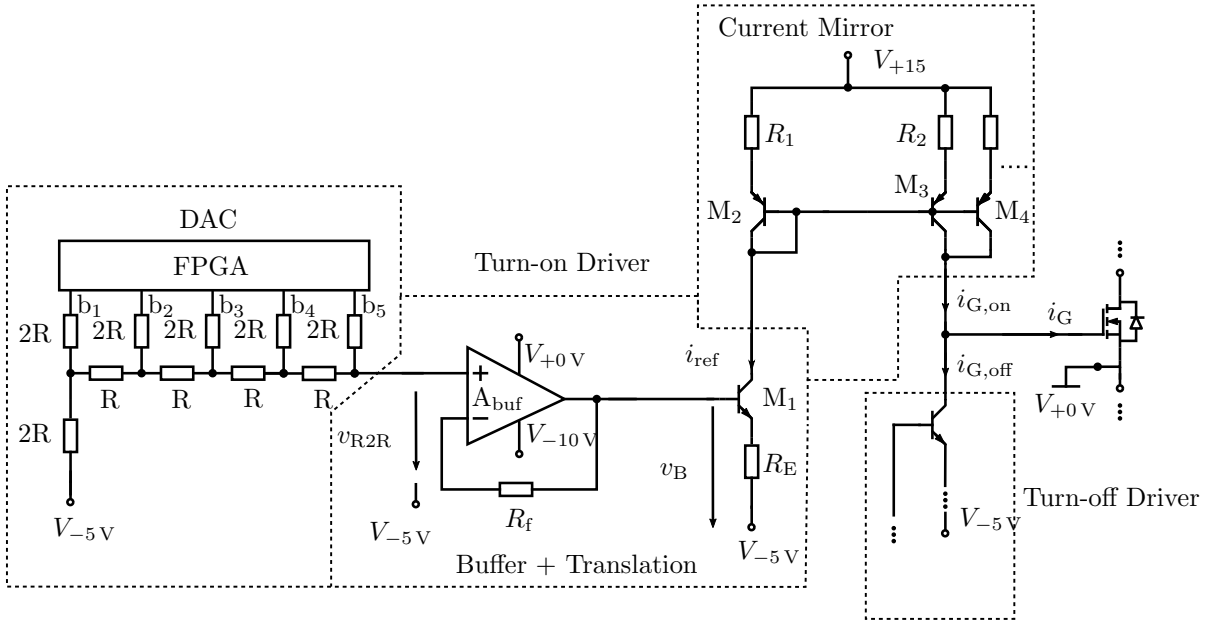


Figure 2.8: Topology of implemented current source driver.

Because the driver modules comprises many components, seven voltage rails have to be provided. The rails connected to the driving stage are visible in Fig. 2.8. They are listed in Table 2.2 to give an overview of the interconnections and relationships between the various supply rails.

Discrete DAC

Instead of using an integrated DAC, a discrete variant was designed to be the interface between the FPGA and output stage. By using an R2R ladder, the vertical resolution is easily adjustable by adding another ladder step and occupying another FPGA output pin. Because it is connected directly to the FPGA, the parasitics are negligible and the output bandwidth is only limited by the FPGA. A maximum internal clock frequency of 400 MHz is achieved and yields an update rate of the reference output of $\Delta t_{R2R} = 2.5\,\text{ns}$. The vertical resolution can be calculated to $\Delta v_{R2R} = 3.3\,\text{V} \cdot 1/2^5 = 103\,\text{mV}$. In comparison

Table 2.2: List of voltage rails used on the driver module.

Voltage	Source	Connections
$V_{+15\,\mathrm{V}}$	Isolated power supply	Upper driver supply V_{on}
$V_{+0\,\mathrm{V}}$	Isolated power supply	Kelvin-Source (KS)
$V_{-1.7\,\mathrm{V}}$	Integrated Buck Converter	3.3 V rail referenced from $V_{-5\,\mathrm{V}}$ for FPGA output logic banks
$V_{-3.2\,\mathrm{V}}$	Integrated Buck Converter	1.8 V rail referenced from $V_{-5\,\mathrm{V}}$ for internal FPGA supply and ADC usage
$V_{-4\,\mathrm{V}}$	Integrated Buck Converter	1.0 V rail referenced from $V_{-5\,\mathrm{V}}$ for internal FPGA supply
$V_{-5\,\mathrm{V}}$	Isolated power supply	Lower driver supply V_{off}
$V_{-10\,\mathrm{V}}$	Isolated power supply	Upper driver supply V_{on}

to a high performance integrated DAC, the advantages of this discrete solution are listed here.

- Low Cost: Cheap SMD resistors
- Low Complexity: No extra communication layer or parallel bus is needed
- High Bandwidth: Only limited by output bandwidth of FPGA and parasitics of the PCB

The major disadvantage is the high output impedance of the R2R ladder of 200 Ω. To compensate this, a buffer stage is inserted, which is introduced in the next section.

Buffer and Translation Stage

The buffer stage, depicted in the section labeled with 'Buffer + Translation' in Fig. 2.8, is responsible for providing a low impedance output of the analog voltage v_{B}, which is provided by the R2R ladder. Here, a current feedback operational amplifier (OP) AD8009 is used with a unity gain design as buffer amplifier. This way, the AD8009 can provide up to 175 mA at up to 1 GHz bandwidth. Therefore, the translation of v_{R2R} to v_{B} can be considered almost ideal.

To create a reference current i_{ref}, which is used as input current for the current mirror, an emitter follower, built by M_1 and R_{E}, is used. The ratio between v_{B} and i_{ref} is defined by the resistor R_{E} and the base-emitter voltage $V_{\mathrm{BE,M1}}$ of M_1 as is described in (2.1).

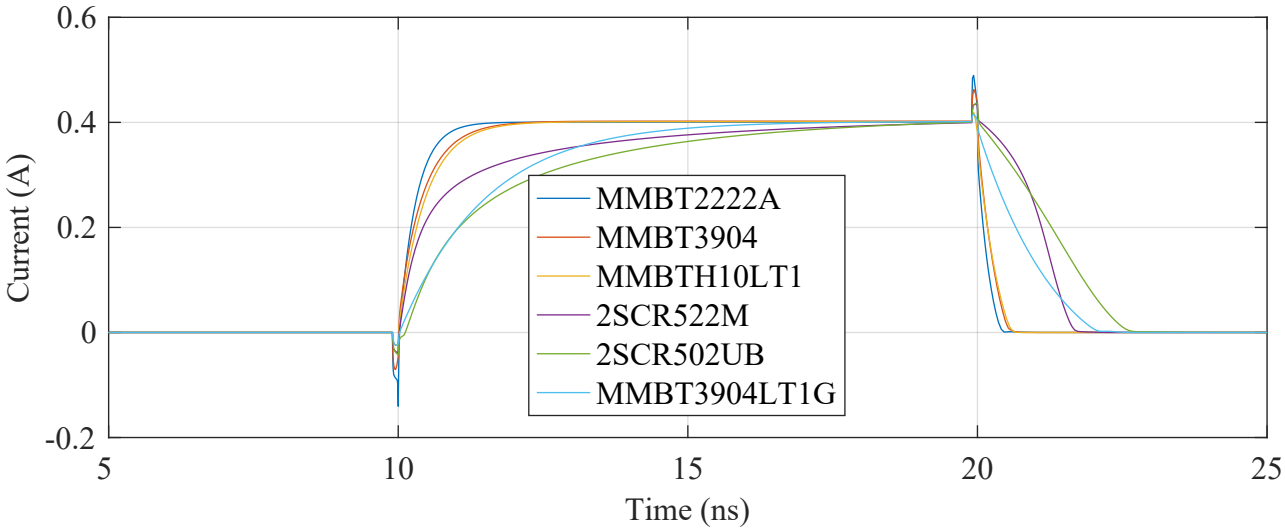


Figure 2.9: Comparison of similar BJT models in a spice simulation [24].

$$i_{\text{ref}} = \frac{v_{\text{B}} - V_{\text{BE,M1}}}{R_{\text{E}}} \tag{2.1}$$

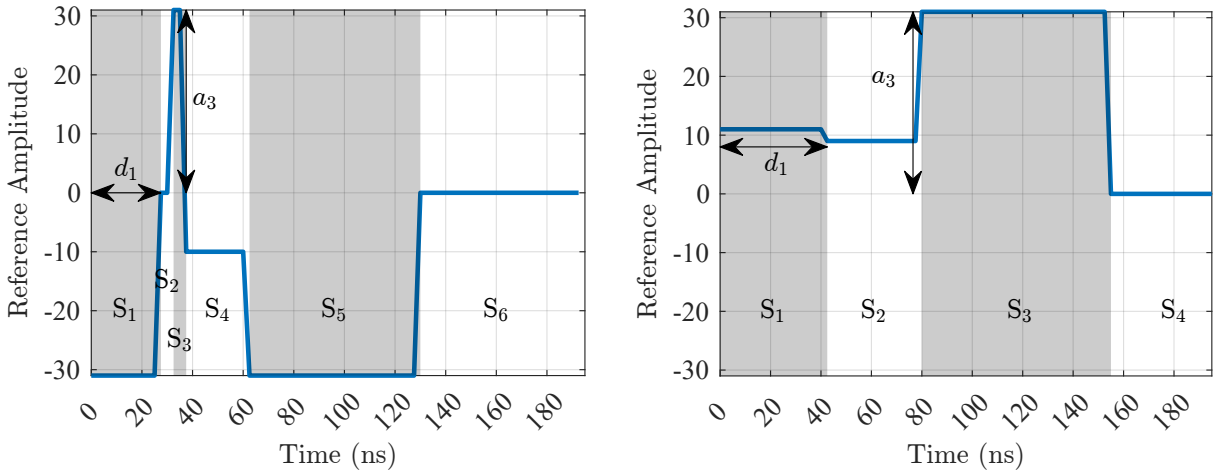
Output Stage

The output stage is a scalable discrete current mirror created from M_2 and the opposite output bipolar junction transistors (BJTs). While the turn-on driver is composed of PNP BJTs, the turn-off driver utilizes BJTs of complementary polarity in a very similar topology. The scalability is provided by the possibility to extend or decrease the number of output transistors such as M_3 and M_4. To allow a fast charging of C_{GS}, five output BJTs are used. The selection of BJTs is done after a characterization using a spice simulation and testing of the SOT-23 devices, as shown in Fig. 2.9 on a prototype PCB. Here, the MMBT2222A variant shows the best performance in bandwidth and is used for every NPN BJT. Using the same methods, the 50A02CH PNP BJT exhibits the best performance and is used for every PNP BJT in the driver topology.

2.3.2 Driver Control

In comparison to conventional drivers, which only require a binary input, the switching behavior of AGDs depends heavily on the reference profile they are supplied with. The reference profile describes how the driver output changes during the switching event. For the presented AGD, the gate current is controlled by setting the output state of the FPGA according to a reference profile. The 5 bit output can be changed with every internal clock cycle of 2.5 ns. During these states, the turn-on and turn-off driver stages

can be controlled independently by setting a reference amplitude between 0 and 31. To simplify profile storage and changes of profile states, each state is defined by a triplet. This triplet contains the on- and off reference amplitudes combined to $a_i = a_{i,\mathrm{on}} - a_{i,\mathrm{off}}$, as well as the duration d_i in FPGA clock cycles. The index i indicates the state the parameters correspond to. Finally, the complete profile contains several states, which are indicated by the alternating gray and white patches in Fig. 2.10. From the triplets and states, the profile waveforms can be composed and plotted. Additionally, Table 2.3 lists the triplets and assigns them to the corresponding states.



(a) Exemplary turn-off profile.

(b) Exemplary turn-on profile.

Figure 2.10: Turn-on and turn-off profiles highlighting the parameters for duration and amplitude variations as well as indicating the states with alternating gray and white patches.

Table 2.3: Turn-on profile depicted in Fig. 2.10b converted into a table.

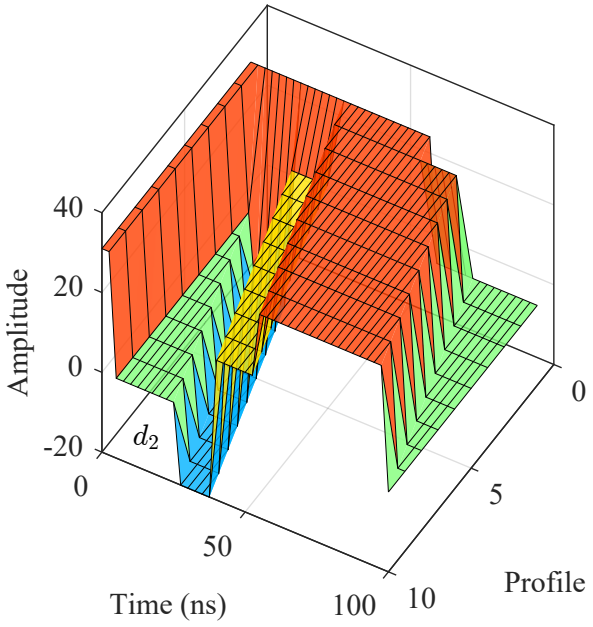
# State	S_1			S_2			S_3			S_4		
Parameter	on	off	dur	on	off	dur	on	off	dur	on	off	dur
test	11	0	17	9	0	15	31	0	30	0	0	0

2.3.3 Measurement Results for Profile Variations

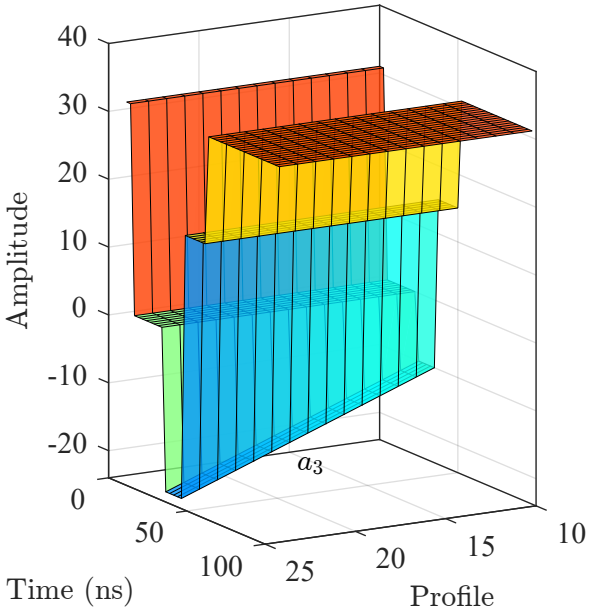
To evaluate the principles of the previously introduced driver, a simplified test setup is used. Two C3M0075120K, manufactured by Wolfspeed, are set up in a half-bridge topology with no load connected to the output [37]. They are 1200 V SiC MOSFETs with 75 mΩ $R_{\mathrm{DS,on}}$. This load configuration results in very fast switching instances with no influence of the load current amplitude on the switching characteristics. Additionally, there is a clear indication of the driver control on the device voltages v_{DS} and also on v_{GS}.

In the following sections, the effects of varying a duration and amplitude parameter of the gate profile are presented.

Figure 2.11 depicts overviews of the gate profile settings for both variations. The time and reference amplitude are equal to those in Fig. 2.10 and the third dimension introduces the profile index, which allows a visualization of the changes in between the profiles. Here, Fig. 2.11a contains a set of profiles, which only differ in the duration of state S_2. This is the duration between the first positive pulse and when the turn-off driver starts to slow down the turn-on transition during a turn-on event. It changes from 2.5 ns up to 22.5 ns in nine steps. A similar effect can be achieved by changing the amplitude of this state. Figure 2.11b shows the variation in the negative amplitude of state S_3. The variation of the amplitude a_3 ranges from -10 to -24.



(a) Sweep of the duration d_2 between the first positive and negative pulse with a variation range from 2.5 ns to 22.5 ns in 2.5 ns steps.

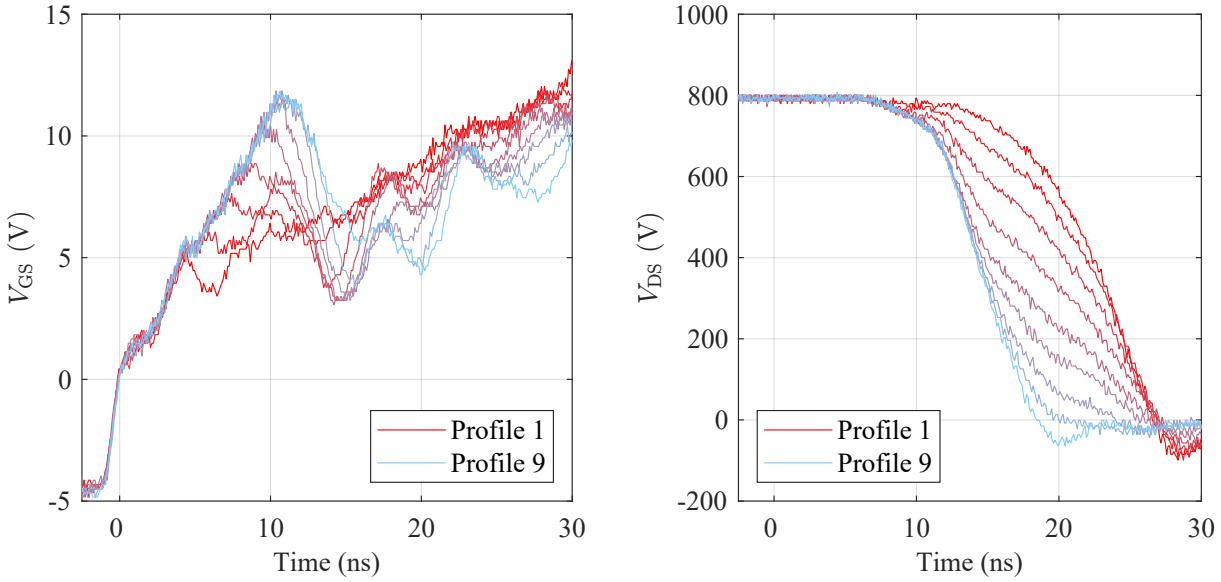


(b) Sweep of the amplitude a_3 during the negative pulse of the gate profile with a variation range of the amplitude from -10 to -24 in steps of 1.

Figure 2.11: Overview of the sweeps in the gate profiles during the following tests.

The resulting changes in the switching transitions are visible in Fig. 2.12 and Fig. 2.13 and are described in this paragraph. The variation of the timing setting for this profile results in different amounts of charge pushed into the gate during the first phase, as is visible in Fig. 2.12a. For v_{DS}, this results in a wide range of voltage slopes, as is visible in Fig. 2.12b. Additionally, the non-linearity of the influence of the gate driver on the switching behavior is visible. The voltage transition in Fig. 2.12b caused by profile 1 starts slow, but the voltage slope increases and a moderate negative overshoot and slope are the result of this gate profile. While the change in the profile is linear, the slope and negative overshoot first decrease, but increase for the last profiles again. This non-linearity is caused by the

lack of time v_{DS} has to end the transition before v_{GS} increases towards its final value. Therefore, if the gate profile adapts several parameters and gives the voltage transition enough time, the dependency can be linearized. This indicates the need for complex profiles or limited degrees of freedom in the profile choice, if a linear dependency between the changes in the profiles and their effect on the switching characteristic is desired.

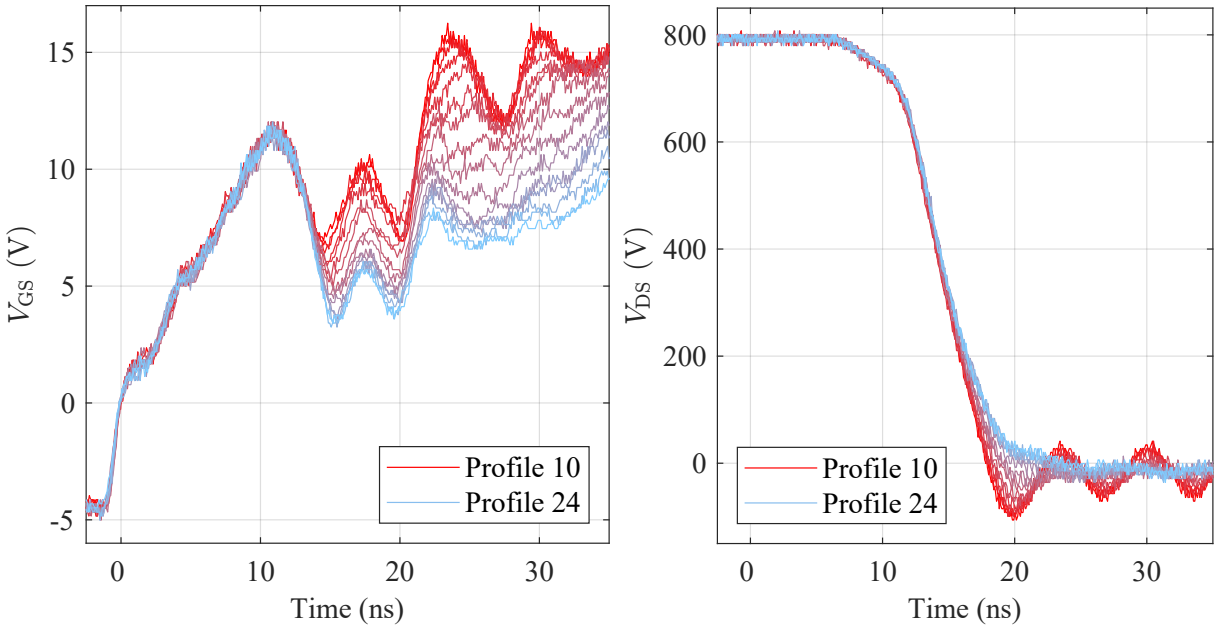


(a) v_{GS} for profiles 1 to 9.

(b) v_{DS} for profiles 1 to 9.

Figure 2.12: Effects on v_{GS} and v_{DS} while varying the duration of state two (d_2)in the gate profiles in between measurements.

In comparison to the changes in the timing setting, the adjustment of the amplitude during the negative pulse shows a lower impact on the gate voltage. This is depicted in Fig. 2.13a, where a gradual change between profile 10 and 24 is observed. These changes in the gate profiles cause an adaption of the overshoot and oscillation amplitude on v_{DS}, as is visible in Fig. 2.13b. Furthermore, the influence of the change in amplitude does not alter the effect of the gate profile on the switching behavior, which indicates a monotone control behavior for this parameter range. Generally, the ratio between the duration and amplitude of a state will give an indication of which parameter leads to a coarse or fine adjustment of the gate voltage. For short states with high amplitudes and a short duration similar to S_3 in Fig. 2.10a, the amplitude is the fine control setting. Profiles with an inverse ratio between the parameters behave the opposite way.



(a) v_{GS} for profiles 10 to 24.

(b) v_{DS} for profiles 10 to 2.4

Figure 2.13: Effects on v_{GS} and v_{DS} while varying the amplitude of state 3 (a_3) in the gate profiles in between measurements.

2.4 Analysis of Switching Behavior

After introducing the topology and functionality of the AGD, an analysis of the effects of the gate driver on the switching characteristics and their frequency components is performed. Firstly, a brief introduction into the frequency characteristics of switching waveforms is presented. Then, based on the half-bridge model introduced in Fig. 2.1b, a simulation model is created and the influence of the gate resistance on the emissions and switching losses is analyzed. Afterwards, a metric for the compromise between switching losses and EMEs is introduced.

2.4.1 Frequency Analysis

For the following analysis, the simulation model depicted in Fig. A.1 is used to recreate the switching behavior of the semiconductor devices in a half-bridge topology. It is based on the detailed equivalent circuit shown in Fig. 2.1b. Wolfspeed, the manufacturer of the semiconductor devices used in this thesis, provides simulation models for their SiC MOSFETs to be used in simulation program with integrated circuit emphasis (SPICE) tools like SIMetrix. This model includes the voltage dependency of the capacitances C_{GD} and C_{DS}. The models are included in a double pulse simulation testbench, which provide flexible operating point choices without the need for long simulation times.

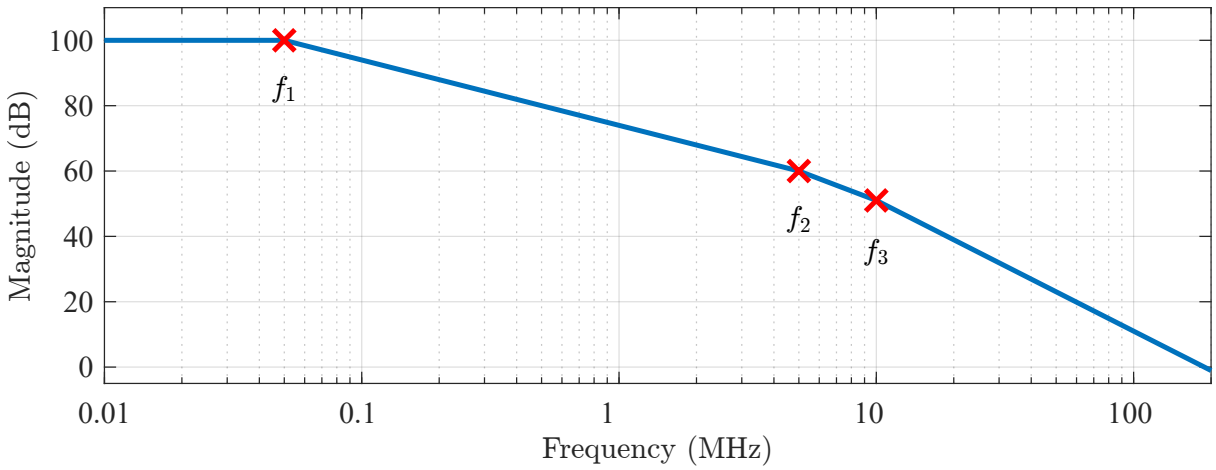


Figure 2.14: Exemplary spectral components of a trapezoidal voltage waveform with the respective cut-off frequencies.

The general purpose of a half-bridge is to create rectangular voltage waveforms across the load connected to the output node. With finite rise and fall times, the rectangular waveform is represented by a trapezoidal shape. As described in [38], this trapezoidal voltage shape results in a series of pulses repeating at multiples of the switching frequency when a fast Fourier transform (FFT) is performed. Therefore, it is considered a broadband emission source. Figure 2.14 depicts the upper envelope of exemplary spectral components of such a trapezoidal voltage waveform. The spectral components show a declining amplitude of −20 dB/decade after the first cut-off frequency f_1. After the next cut-off frequency, which is defined by the rise and fall times, they decline with −40 dB/decade. For cases with different rise and fall times, two cut-off frequencies are present and a gradual change from −20 dB/decade to −40 dB/decade is present in between. When describing the behavior of spectral components, the dB scale allows to describe ratios of values without using a reference unit. Therefore, in the descriptions regarding the general behavior the unit is reduced to dB instead of using dBµV, as is done for disturbance voltage measurements. Equation (2.2) describes the relationship of the cut-off frequencies and the rise and fall times.

$$
\begin{aligned}
f_1 &= \frac{f_{\mathrm{sw}}}{sin(\pi d)} \quad \text{with} \quad d = \text{duty cycle} \\
f_2 &= \frac{1}{\alpha\pi} \quad \text{with} \quad \alpha = \begin{cases} t_\mathrm{r} & \text{for } t_\mathrm{r}{<}t_\mathrm{f} \\ t_\mathrm{f} & \text{for } t_\mathrm{f}{<}t_\mathrm{r} \end{cases} \\
f_3 &= \frac{1}{\beta\pi} \quad \text{with} \quad \beta = \begin{cases} t_\mathrm{f} & \text{for } t_\mathrm{r}{<}t_\mathrm{f} \\ t_\mathrm{r} & \text{for } t_\mathrm{f}{<}t_\mathrm{r} \end{cases}
\end{aligned}
\tag{2.2}
$$

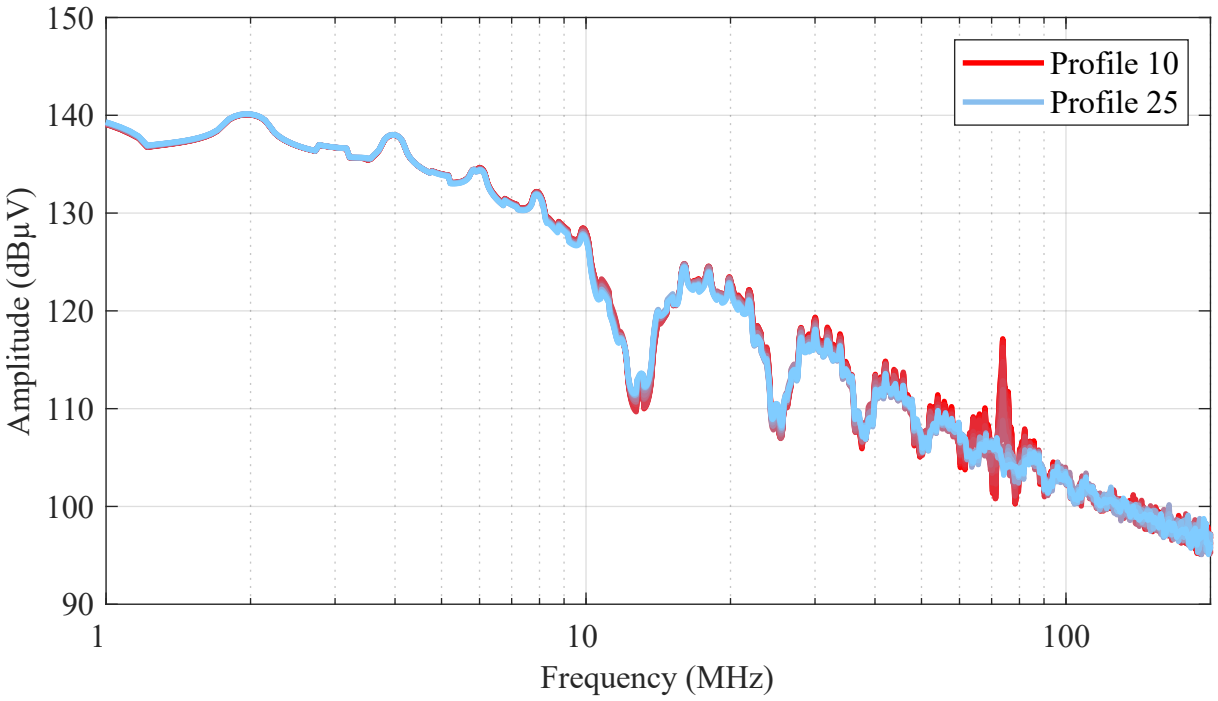


Figure 2.15: FFT of the voltage measurements in the amplitude variation experiment (Fig. 2.13b). The data has been filtered by an envelope filter to show the upper boundary of a noisy signal.

When there are overshoots or ringing on the voltages or currents waveforms, as indicated in Fig. 2.3 or in the measurements in Fig. 2.13b, a narrowband frequency component at the fundamental frequency of the overshoot or oscillation appears. Figure 2.15 depicts the FFT of the voltage waveform in Fig. 2.13b and exhibits this behavior. At 73 MHz, the narrowband component of the oscillation after the negative overshoot is visible. Similar to the time domain measurement, the amplitude of the resonance decreases. The voltage rise and fall times for this measurement are between 13.8 ns and 15 ns, which leads to cut-off frequencies in the range of 23 MHz and 21.2 MHz. As is visible in Fig. 2.15, the overall slope of the frequency components is very similar. It is measured to be −25 dB/decade. This indicates that the spectral components are in the transition region between −20 dB/decade to −40 dB/decade. Due to the limited measurement time and noise on the time domain measurement, a further decrease of the frequency slope is not present.

2.4.2 Metric for Switching Evaluation

The evaluation of the switching characteristics in a single metric is a complex topic. Voltage slopes, overshoots and oscillation amplitudes can be extracted from time domain measurements. Using these values results in a multi-dimensional evaluation, which can be simplified if the switching event is analyzed in the frequency domain. In the frequency domain the influence of slopes and switching oscillations are separated into different regions.

Therefore, the analysis of switching characteristics can be achieved by just choosing the frequency region corresponding to the desired metric.

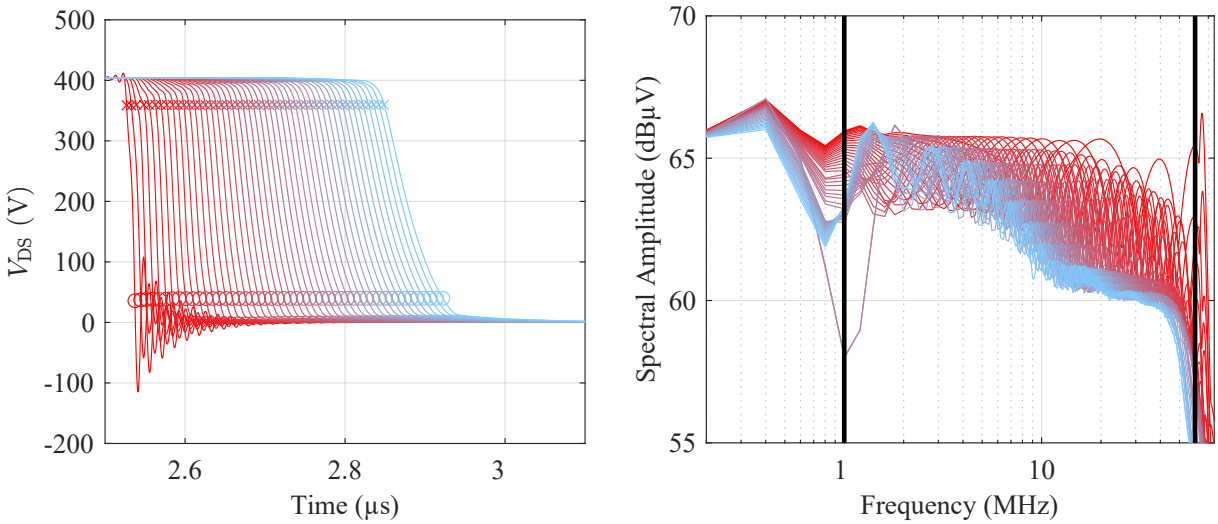
Representing the switching characteristics of a single switching event in relation to the spectral components of the frequency domain in one quantity has been first proposed in [39]. The goal is to define a metric for the influence of the gate resistance on the switching behavior in order to relate it to the switching losses. The spectrum in [39] is imposed with a +60 dB/decade factor above 30 MHz to increase the weight of the area influenced by the gate driver. Then the power spectrum is calculated and added up between 30 MHz and 100 MHz. This leads to a representation of the regions influenced by the gate driver in a single value.

In this thesis, a different approach is taken. Firstly, the characteristics of a single or a series of switching instances of one phase measured in time domain are considered. Instead of amplifying just the higher frequency spectrum, the transfer function of the sensors is multiplied with the spectrum. By imposing the transfer function of the voltage probe $G_{\text{probe}}(f)$ and the filters $G_{\text{filter}}(f)$ onto the FFT of the voltage measurement, a weighted spectrum is produced. The transfer function of the filter can either have a low-pass or band-pass behavior. Therefore, a differentiation between the voltage slope and overshoot/oscillation amplitude can be achieved. The sensor design and characteristics is presented in Chapter 3.

To calculate the power spectrum the peak disturbance voltage values $A_{\text{FFT,v}_{\text{DS}}}$ contained in the spectrum are transformed into their root mean square (RMS) values and used to calculate the power dissipated in a 50 Ω resistor. Equation (2.3) summarizes this procedure.

$$P_{\text{single}} = \sum_{f_{\text{low}}}^{f_{\text{up}}} \frac{\left(A_{\text{FFT,v}_{\text{DS}}}(f)/\sqrt{2} \cdot G_{\text{probe·filter}}(f)\right)^2}{50\,\Omega} \tag{2.3}$$

If instead of a single phase or switch, the full converter is considered, the FFT of the disturbance voltage v_{dist} measured at the LISNs using a measurement receiver can be used to calculate the metric. This yields the frequency components $A_{\text{FFT,v}_{\text{dist}}}$ which describe the frequency dependent behavior of the converter. The advantages of this proceeding are the extended measurement bandwidth of the measurement receiver and the possibility of analyzing the behavior of the complete converter. However, an additional measurement device is required and a comparison to simulations is not feasible because they would require long simulation times in order to represent the behavior over a full sine period of a traction inverter. Therefore, (2.3) is modified to disregard the combined transfer function $G_{\text{probe·filter}}(f)$ of the probe and filter. Instead, the boundaries of the sum can be used to analyze different characteristics of the switching behavior. Equation (2.4) describes how to obtain this metric. In addition to the boundaries for the sum, the spectral components



(a) Time domain simulation results.

(b) Frequency domain simulation results.

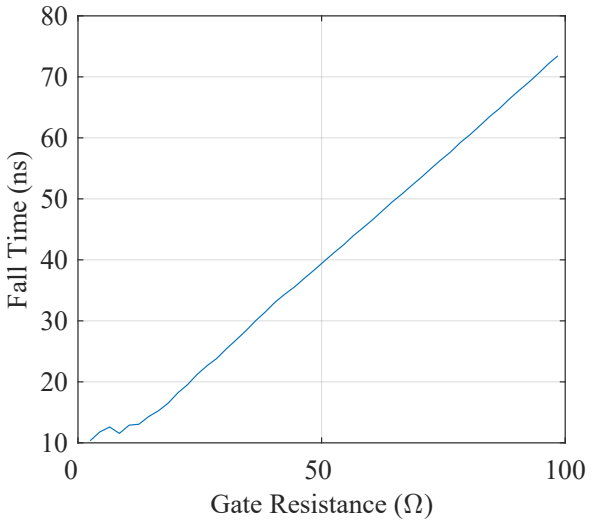
Figure 2.16: Sweep of the gate resistance and its effect on time and frequency domain simulation results. The simulations with 64.5 Ω and 66.5 Ω as R_G show a singularity in the FFT at 1 MHz which can not be explained from the time domain data.

have to be evaluated at the same sample frequencies for a valid comparison of different FFTs. If they do not match, the signal with the lower sample rate has to be resampled.

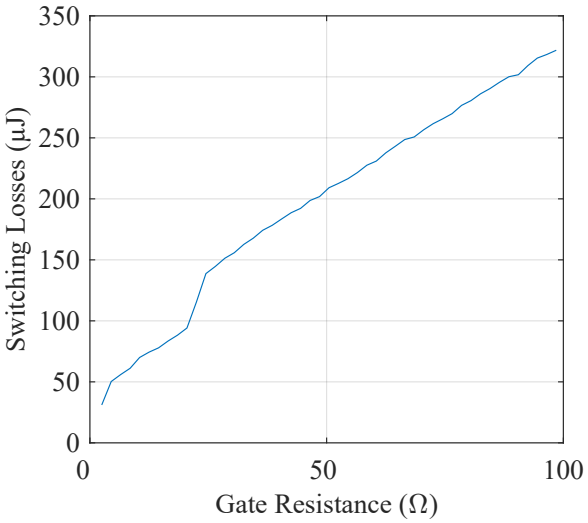
$$P_{\text{total}} = \sum_{f_{\text{low}}}^{f_{\text{up}}} \frac{\left(A_{\text{FFT,v}_{\text{dist}}}(f)/\sqrt{2}\right)^2}{50\,\Omega} \tag{2.4}$$

The basis for the following analyses are a set of simulation results obtained from SIMetrix. The model is depicted in Fig. A.1 and allows parameter sweeps for a multitude of variables. It uses a semiconductor model provided by the manufacturer Wolfspeed and the parasitics of the switching cell are close to the final prototype. A major difference compared to the prototype is the gate driver, which is modeled as simple resistive gate driver. This allows short simulation times and a simple parametrization. Figures 2.16a and 2.16b show the time and frequency domain simulation results of changing the gate resistance from 2.5 Ω (light red) to 100 Ω (light blue) in steps of 2 Ω, respectively. The 10 % and 90 % values in Fig. 2.16a of V_{DC} are marked with "x"and "o"respectively.

The variation of the gate resistance corresponds to the change in the plot color of Fig. 2.16a. Light red uses the lowest gate resistance and light blue the highest. As expected, the MOSFET model shows a linear dependency of the voltage slope to the gate resistance, as can be seen in Fig. 2.17a. Accordingly, the losses behave similarly as is visible in Fig. 2.17b. Both plots show a linear behavior for higher gate resistances. The datasheet of the semiconductor device lists switching characteristics up to gate resistances of 25 Ω



(a) Simulated fall times over gate resistance.



(b) Calculated switching losses over geate resistance.

Figure 2.17: Sweep of the gate resistance and its effect on the fall time and switching losses.

[37]. Therefore, the assumption is drawn, that the simulation model is simplified for high gate resistances.

Figure 2.18 depicts the emission representation $P_{\text{single,slope}}$ and the peak steepness of the voltage transition over the gate resistance. They show a close correlation in the overall shape, which depends on the vertical scaling. If the x-axis in Fig. 2.19a is limited to the resistor values listed in the datasheet, the correlation is higher. This indicates a valid representation of the switching behavior with respect to the voltage slope by the metric introduced here.

Finally, the emission representation can be plotted over the switching losses to analyze and asses the balance between switching losses and EME. Figure 2.19b depicts the resulting relationship between emission representation and switching losses for the simulation model. This indicates that the effects of different gate resistances saturate towards both ends of the graph.

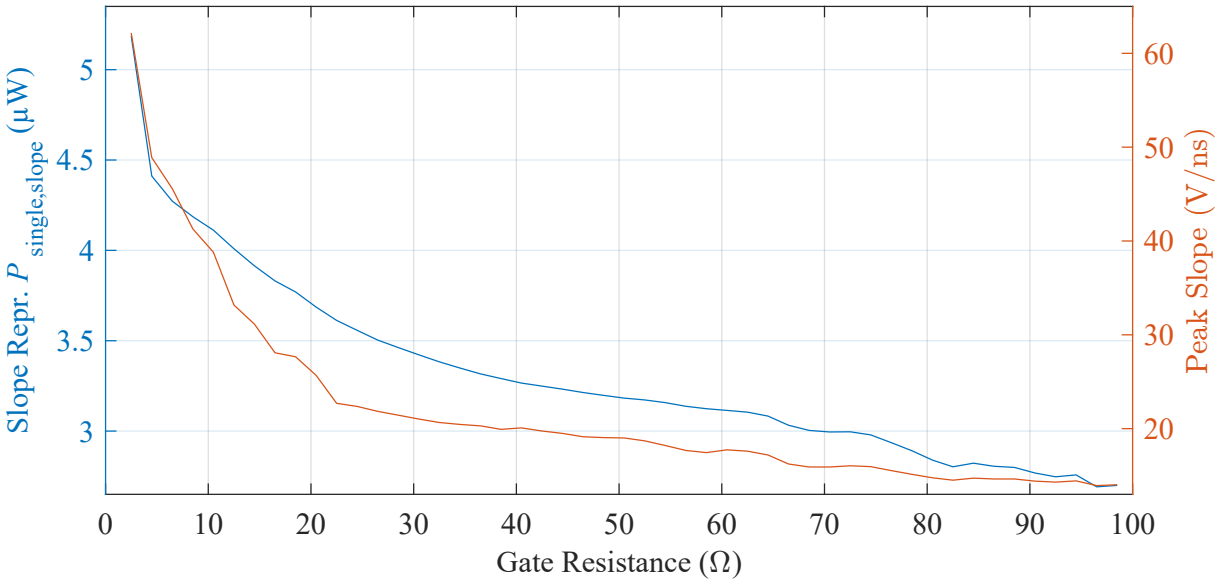
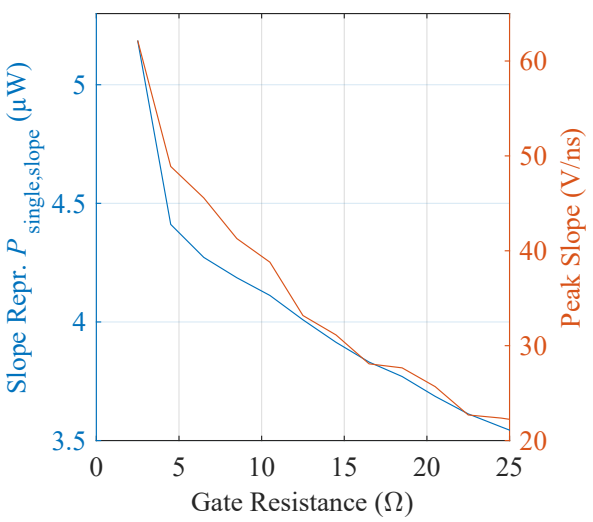
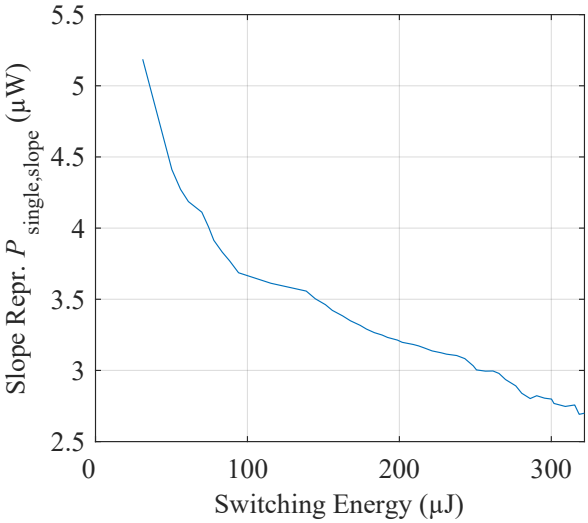


Figure 2.18: Emission representation and the peak slope of V_{DS} while varying the gate resistance.



(a) Emission representation and the peak slope of v_{DS} while varying the gate resistance.



(b) Emission representation plotted over the switching losses.

Figure 2.19: Changing the gate resistance and its effect on switching losses.

2.5 Summary

Recap

In this chapter, an introduction into the switching behavior of MOSFETs was done. Afterwards, a research overview of three categories of gate drivers was given. Commercially available drivers and their limited adaptive features were evaluated first. Secondly, adaptive drivers, which have been presented in research, were analyzed and their capabilities compared. Subsequently, control approaches, which include some form of feedback for the adaptive drivers, were presented. Based on the existing driver concepts, an adaptive gate driver, which is able to dynamically change the gate current during a switching event, was developed. From the measurements used to characterize the switching behavior, a metric for the representation of the frequency characteristics of switching waveforms was derived.

Conclusion

The flexibility in terms of maximum output current amplitude and scalability of vertical resolution in the signal path are clear advantages of the current-source gate driver topology. Furthermore, the driver is capable of influencing the switching characteristics in time and frequency domain by precise adjustments to the gate current during the switching events. These precise adjustments allow adaptions to either the voltage slope or overshoot independently. The aforementioned metric indicates different characteristics such as the voltage slope or oscillation amplitude, depending on the desired insight into the switching events. Therefore, the performance of an AGD or the complete EME control can be evaluated using this metric.

3 Sensing the Switching Behavior

Measuring the switching characteristics is conventionally done during the design and evaluation of a converter. Afterwards, the gate resistance is set to meet the design requirements. However, recent developments in AGD topologies allow an adaption of the switching characteristics during operation. Therefore, a basis for the decision on how to adapt the switching behavior has to be established. It can be based on fixed look up tables (LUTs) filled during the design phase, which are read according to the operating point or based on feedback provided during operation. Besides oscilloscopes, the source of this feedback can be a sensor connected to a central controller or the driver itself. Figure 3.1 depicts the position of the sensor in the closed control loop. This chapter will provide an overview of existing sensor topologies and technologies, as well as an in depth analysis of the sensor developed for the control loop presented in this thesis. Additionally, a characterization of the sensing circuits and evaluation of their performance against oscilloscope measurements is presented.

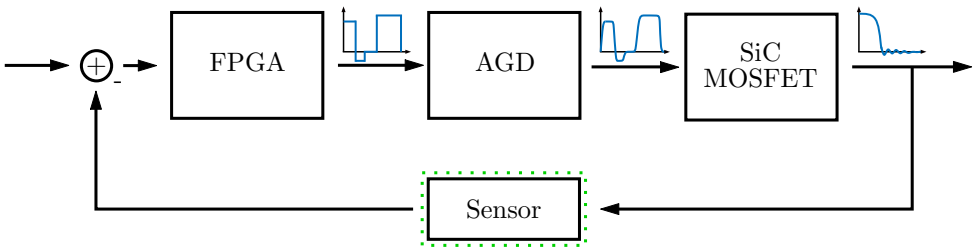


Figure 3.1: Control loop emphasizing the sensor providing feedback.

3.1 Introduction to Sensing Switching Characteristics

As mentioned before, the use of AGDs demands knowledge about the switching characteristics in order to adapt the behavior of the gate driver. This is especially important if the driver is meant to react dynamically to changes in the operating point or switching behavior.

To characterize the switching behavior of semiconductor devices two parameters are most valuable. The drain-source voltage v_{DS} and the drain current i_{D} during the switching instance. Measurements such as the gate-source voltage's shape or the gate current can be used to characterize the switching behavior too, but the objective of this thesis is to control

EME. Therefore, the behavior of the semiconductor devices towards their environment is in the focus of this thesis. The relevant characteristics for this behavior are the slope and overshoot or oscillation amplitude of v_{DS} and i_{D}.

For both, voltage and current, the amplitude of the switching slope provides valuable information on the switching characteristics. Firstly, it indicates the fall and rise times of the switching instances. These are relevant for the choice of the blanking time between a turn-off and the next turn-on instance of the opposite device in a half-bridge. Secondly, switching losses are closely correlated to the slopes of v_{DS} and i_{D}, because the overlapping area increases with slow switching speeds. This is depicted in Fig. 2.3. Lastly, the switching dynamics influence EME over a wide range of frequencies as described in Section 2.4.1.

In addition to the slope, a measurement of the overshoot and oscillation amplitude allows protecting the semiconductor device from overvoltages and enables the driver to reduce EME in a narrow band around the resonance frequency of the switching cell. Furthermore, for a turn-off transition the overshoot amplitude is a suitable indicator for the $^{\mathrm{d}i}/_{\mathrm{d}t}$, as is described in Section 2.1.

The following sections will give an overview over recent research into sensing switching characteristics and the bandwidth requirements for the sensor developed for this thesis.

3.1.1 Research Overview

In the past, sensors have been integrated into drivers for Si IGBTs [21], [22]. Their feedback is evaluated in an analog manner and the response characteristic is set during the design phase. In relation to the switching speeds of IGBTs the group and propagation delays of these sensor networks are acceptable. More recent research uses ASICs with integrated ADCs and direct evaluation to adapt the switching characteristics of WBG devices during the switching events.

For example, in [23] a 1 pF integrated capacitor to couple v_{DS} into the ASIC, which is developed for their research, is used. The ASIC achieves a sub-nanosecond feedback time with a fixed feedback gain and no further adaptability of the gate control. The authors of [20] present a $^{\mathrm{d}i}/_{\mathrm{d}t}$ feedback path by using the voltage across the inductance L_{S} between the source and Kelvin-source connections of a 1200 V 300 A SiC power module. This voltage is fed into an analog PD controller, which influences the behavior of the gate driver directly. Because the amplifiers and setting resistors are not integrated, this approach is more flexible, but the direct connection between controller and driver limits its adaptability.

Bendicks et. al. present sensor and evaluation circuits which make use of external measurement devices or external evaluation and computational devices in [40]. In this case,

they use the information about the switching behavior to control an active filter, which aims to cancel noise on the dc-link.

[19] presents an approach which uses a sensor to adaptively prevent crosstalk between the two switches in a half-bridge. A p-channel MOSFET is connected to the sensor and actively clamps the gate voltage in case a high voltage slope across the semiconductor device is detected.

In this thesis, a set of sensors presented in [25] is used. They are capable of providing information about the voltage slopes and overshoot amplitudes shortly after each switching instance. Separating the slope and overshoot amplitude information is done by using a low-pass filter for the slope and band-pass filter for the oscillation amplitude. This way, the low-pass filter can pick up the broadband characteristic of the slope and the oscillation sensor captures the narrowband behavior of the oscillation. The filter's group delay and the amplifier's propagation delay and evaluation calculations in the FPGA add up to about 330 ns. A major contribution to this delay is the time the driver needs to prepare a new profile inside the FPGA. Therefore, it can only be used to adjust the next switching instance, which is acceptable in case of dc-dc converters or traction inverters with high switching- to fundamental sine-frequency ratio.

3.1.2 Sensor Bandwidth Requirements

EME can be influenced by the switching characteristics in two frequency bands. Firstly, a wide range of frequencies is influenced by the broadband behavior of the voltage and current slopes. Secondly, a narrow but high frequency range is dominated by the overshoot and oscillation amplitude. Therefore, not only the gate driver as introduced in Chapter 2 is responsible for the switching behavior and emissions, but also the characteristics of the switching cell as introduced in Fig. 2.1b.

The relevant range for the slope sensor is defined by the cut-off frequencies in (2.2). For the MOSFET used in this thesis - the C3M0021120k manufactured by Wolfspeed - the datasheet states turn-on and turn-off times as listed in Table 3.1.

Table 3.1: Datasheet values for the timing characteristics of turn-on and turn-off instances of the C3M0021120K SiC MOSFET [41].

Parameter	Value
$t_{\mathrm{d,on}}$	29 ns
$t_{\mathrm{rise,on}}$	33 ns
$t_{\mathrm{d,off}}$	57 ns
$t_{\mathrm{fall,off}}$	14 ns

However, measurements at 600 V presented in Chapter 5 will show voltage slopes of up to 50 $^{\mathrm{V}}/_{\mathrm{ns}}$ which are caused by rise times $t_{\mathrm{rise,on}}$ of below 10 ns. Therefore, smaller rise and fall times compared to the datasheet values have to be considered for the bandwidth requirements of the sensors. This leads to cut-off frequencies according to (2.2) of up to 45 MHz.

The parasitic elements of the semiconductor device and the connections on the PCB form an LC resonant tank, which is excited by the switching instances. It is composed of the parasitic inductances in the power loop and the capacitances in parallel to the semiconductor device being in its off-state. Figure 2.1b and 2.2a depict the parasitic elements. These parasitics present the relevant elements to define the bandwidth of the oscillation sensor.

The dominant capacitive element in the resonant tank is C_{oss} of the semiconductor device. With a capacitance of 220 pF at 400 V it is bigger than the parasitic load capacitances $C_{\mathrm{sw},-/+}$ estimated to be 4 pF. However, it decreases with increasing dc-link voltage. Above 600 V C_{oss} converges to an asymptotic value of 180 pF. Because this driver gathers the feedback by capacitively coupling the $^{\mathrm{d}v}/_{\mathrm{d}t}$, an additional capacitance is connected in parallel to the semiconductor device. As this chapter will reveal, two 10 pF probe capacitors are used. The power loop inductance L_σ is defined by the layout of the cell and the parasitics of the semiconductor device. For the consideration of the resonance, the dc-link capacitors are not relevant because they are several magnitudes of capacitance bigger than the parasitics. Together, they define the resonance frequency, which dominates the oscillation after fast switching instances.

$$f_{\mathrm{res}} = \frac{1}{2\pi \cdot \sqrt{C_{\mathrm{par}} L_\sigma}} \tag{3.1}$$

where

$$L_\sigma = 2 \cdot L_{\mathrm{S}} + L_{\sigma,\mathrm{HS}} + L_{\sigma,\mathrm{LS}} + \left(L_{\mathrm{DC,local}} \| \left(L_{\sigma+} + L_{\sigma-} + L_{\mathrm{DC}}\right)\right) \tag{3.2}$$

and

$$C_{\mathrm{par}} = C_{\mathrm{oss}} + 2 \cdot C_{\mathrm{probe}} \tag{3.3}$$

From measurements at 400 V a resonance frequency of 63 MHz can be extracted. With (3.1) an effective parasitic inductance L_σ of 26.6 nH is calculated. Therefore, a resonance frequency of 69 MHz is to be expected at 800 V.

After the requirements for the bandwidths are defined here, the design limits for the filters in the sensor are deducted from them. The passband of the overshoot amplitude sensor has to be designed to match the resonance frequency including the changes caused by variations of the dc-link voltages. Therefore, the band-pass is defined between 60 MHz and 90 MHz. The cut-off frequency of the low-pass filter for the slope sensor is set to 65 MHz to include a wide range of switching speeds. Additionally, if part of the resonance band

is not attenuated by the slope filter, the influence of the voltage slope is still dominant. Therefore, a cut-off frequency so close to the resonance is suitable.

3.2 Sensor Topology

The sensors comprise a multi-stage topology. The differentiation between oscillation amplitude and slope requires a modular structure, which is divided into three stages. Firstly, the probing stage. This stage is identical for both sensors. Secondly, the filter stage and finally, the amplification and S&H stage. These two are individually designed for the slope and oscillation sensors. All three will be described in detail in the following sections. The choices of parameters for all sensor stages depend on each other. Therefore, design considerations were made iteratively, but only the final choices are presented here. An additional advantage of the modular stage design is the flexibility it offers. For changes of the semiconductor device or the desired filter types, only the impedances and signal amplitudes have to be matched. The stages and their overall structure is summarized in Fig. 3.2, which indicates the signal chain from the semiconductor device to the ADC input.

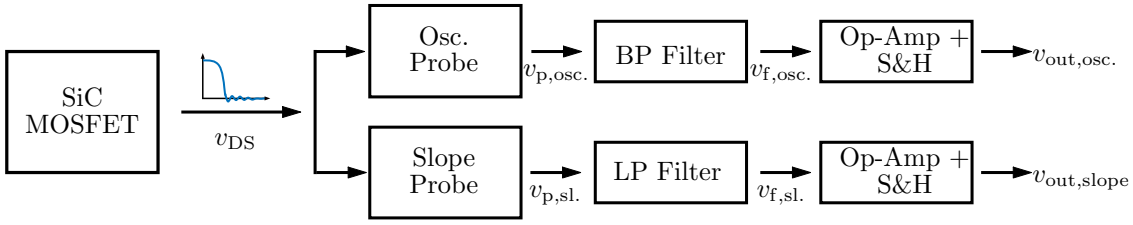
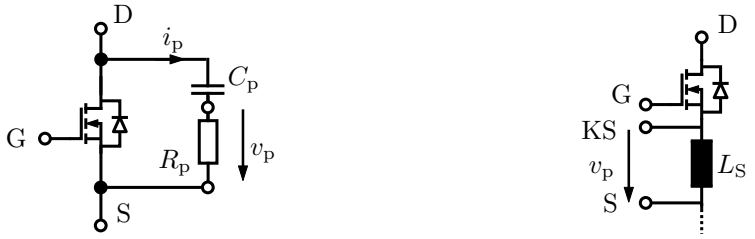


Figure 3.2: Dual sensor structure depicting the stages of each sensor and the signal path.

3.2.1 Probe Design

The probe is the interface between the sensor and the high voltage semiconductor devices. Two topologies are presented to sense both characteristics quantities v_{DS} and i_D. Figure 3.3 depicts the possible probe topologies. Both scale down the low frequency but high amplitude voltages and currents and protect the sensors and following logic devices.

For a $^{di}/_{dt}$ probe, the voltage across the stray inductance of a Kelvin-source equipped device can be used. This is depicted in Fig. 3.3b. In case of a $^{dv}/_{dt}$ probe, v_{DS} is derived by a capacitor C_p. The resulting current is fed through a small resistor, which acts as a current shunt. This probe circuits is shown in Fig. 3.3a.



(a) $^{\mathrm{d}v}/_{\mathrm{d}t}$ Probe (b) $^{\mathrm{d}i}/_{\mathrm{d}t}$ Probe

Figure 3.3: Overview of probe topologies for current or voltage sensors. The output v_p of the respective probe is connected to the corresponding filter inputs, according to the sensor type.

A key aspect in designing the probe is not to influence the switching characteristics of the semiconductor device. Therefore, the impedance of the probes should be higher than the series connection of $R_{\mathrm{DS,on}}$ and C_DS at the respective frequencies. In the following, the $^{\mathrm{d}v}/_{\mathrm{d}t}$ probe will be focused on.

The major design choices for the $^{\mathrm{d}v}/_{\mathrm{d}t}$ probe are the capacitance C_p and the shunt resistance R_p. For the capacitance, the choice of available small footprint, high voltage, C0G/NP0 capacitors is very limited. Suitably sized 0805 capacitors are available in values of 4.3 pF, 10 pF and 18 pF with a voltage rating of 1000 V. Choosing a small capacitance will influence the switching behavior less, but less current will be induced into the shunt resistor R_p. Therefore, its resistance would need to be higher in order to yield the same output amplitude. However, this will also increase the impedance of the probe's output, which degrades its performance. For a higher capacitance, the probe's output impedance decreases, but the negative effect on the semiconductor device's switching characteristics increases. Therefore, its capacitance is chosen to be 10 pF. In comparison to the output capacitance of the C3M0021120K, which is given as 180 pF at 800 V, this is suitably small [41].

The second degree of freedom in designing the probe, is the resistance of the shunt R_p. To not influence the probes output voltage v_p by overloading it, the input impedance of the filter has to be much greater than the shunt. Because the input impedance of the following filters is just R_S at their resonance points, this is the relevant impedance to consider. The design choices for the following filter will be presented in Section 3.2.2. Finally, R_p has to be chosen according to the following equation.

$$R_\mathrm{p} \ll R_\mathrm{S} \tag{3.4}$$

Figure 3.4 depicts the transfer function of the $^{\mathrm{d}v}/_{\mathrm{d}t}$ probe. For the following considerations of the probes transfer functions, a parasitic inductance of 1.5 nH is added in series to C_p and R_p. This parasitic inductance consists of 0.5 nH per 0603 element and an estimated stray inductance of 0.5 nH of the PCB trace between them. The characteristic

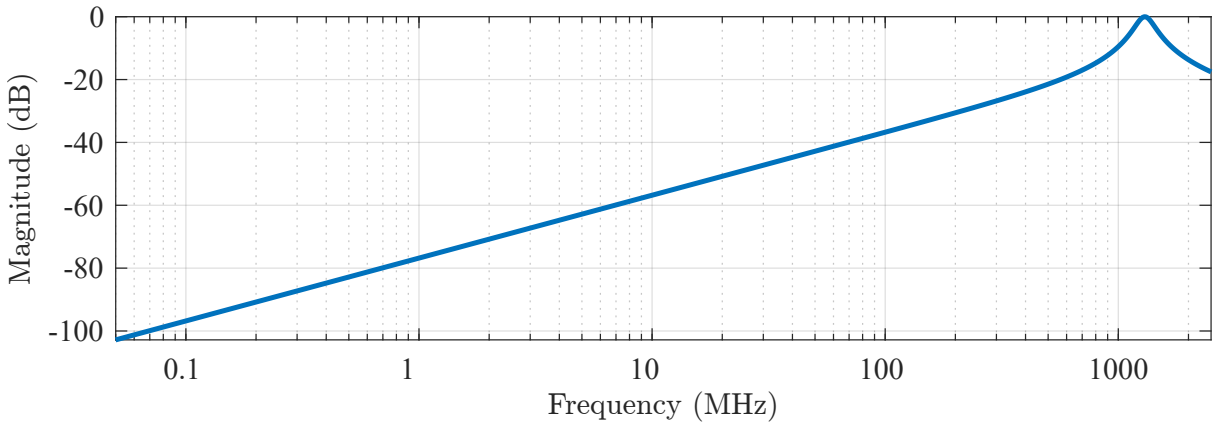


Figure 3.4: Attenuation of the $^{dv}/_{dt}$ probe including a parasitic inductance of 1.5 nH.

20 dB/decade slope of the attenuation continues up to the corner frequency of 1.29 GHz. This perfectly counteracts the negative 20 dB/decade slope of the frequency components of the trapezoidal voltage waveform as described in Section 2.4.1. Therefore, the filter input should receive a signal with a steady amplitude up to the second cut-off frequency caused by the rise or fall times of the switching instances.

3.2.2 Filter Design

After the $^{dv}/_{dt}$ probe provides a signal representing the derivation of the voltage waveform during the switching instance, a filter can be used to gain insight into different aspects of the switching characteristics. The frequency analysis in Section 2.4 shows different areas of interest, which are close together. Therefore, both filters need steep attenuation skirts after the cut-off points in their frequency responses. At the same time, the filter should stay as simple as possible to save PCB area close to the switching cell. Therefore, Chebyshev Type I filters of 4th order are selected for both filters. Their design is done analytically according to [42]. Figure 3.5 and 3.8 depict the low-pass and band-pass filter topologies, which will be presented in the following sections.

Slope Filter

The range of voltage slopes to be considered is 100 $^{V}/_{ns}$ down to 10 $^{V}/_{ns}$. While it is possible to create lower slew rates, the increase in losses will diminish the advantages of using WBG semiconductor devices at very slow switching transitions. According to the analysis in Section 3.1.2, frequencies up to the highest cut off frequency are of interest. Therefore, a low-pass filter is suitable to capture a wide frequency spectrum up to its cut-off frequency. To ensure a successful probing of the signal a margin of 20 MHz is added to the expected cut-off frequency of the voltage slope.

Consequently, a low-pass filter with a cut-off frequency of 65 MHz is selected for the slope filter. Its structure is depicted in Fig. 3.5. The ladder topology forms a fourth order low-pass filter and includes a series resistance R_S to ensure an input impedance much greater than the output impedance of the probe. In this case, R_S is chosen to be 50 Ω. This values sets an upper boundary for the choice of R_p in the probe according to (3.4).

The resulting magnitude of the probe and slope filter combination is depicted in Fig. 3.6. The magnitude of the probe circuit and the low-pass filter are shown in red and blue. Adding both magnitudes yields the combined transfer function between the semiconductor device and the S&H stage. The resulting magnitude is shown in yellow. As mentioned before, the declining nature of the frequency components of the switching waveforms is canceled by the increasing magnitude of the filter. Therefore, applying this filter to Fig. 2.15 results in the overall transfer function of the system and visualizes which frequency components are used to evaluate the slope. The corresponding frequency behavior is depicted in Fig. 3.7.

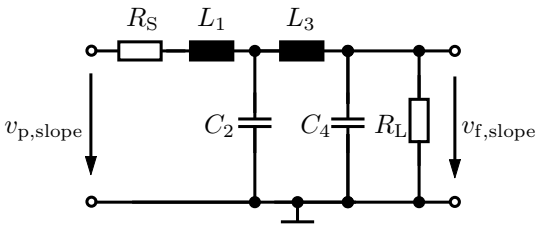


Figure 3.5: Structure of the low-pass filter used to separate the influence of the oscillation from the voltage slope.

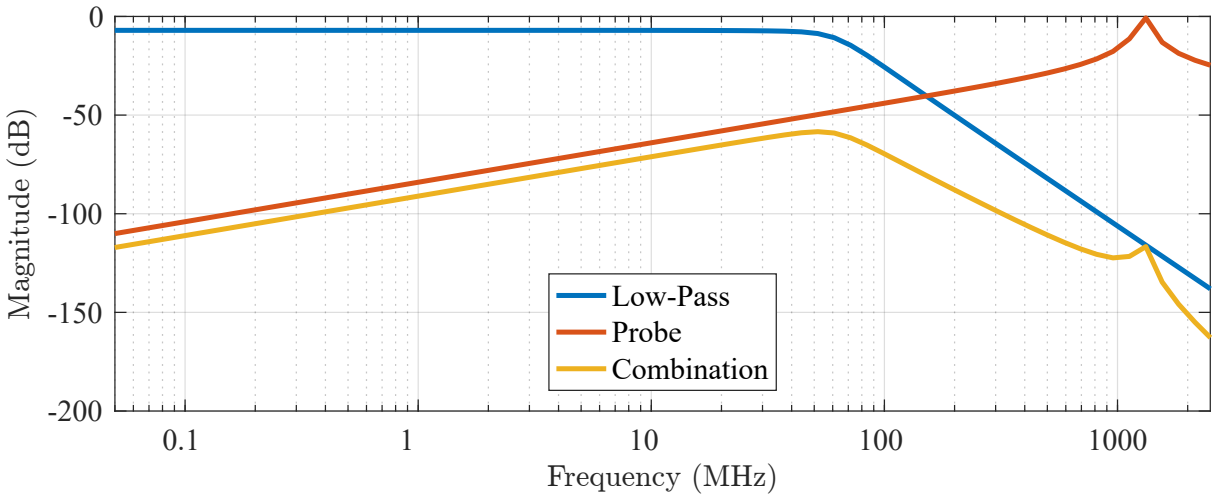


Figure 3.6: Magnitude information of the resulting low-pass filter. Additionally, the probe is considered and the combination of both is depicted.

The elements used to realize the aforementioned requirements for this filter are listed in Table 3.2.

Table 3.2: Low-pass filter element choices.

Parameter	Value	Parameter	Value
R_S	50 Ω	L_3	216 nH
L_1	82 nH	C_4	85 pF
C_2	75 pF	R_L	40 Ω

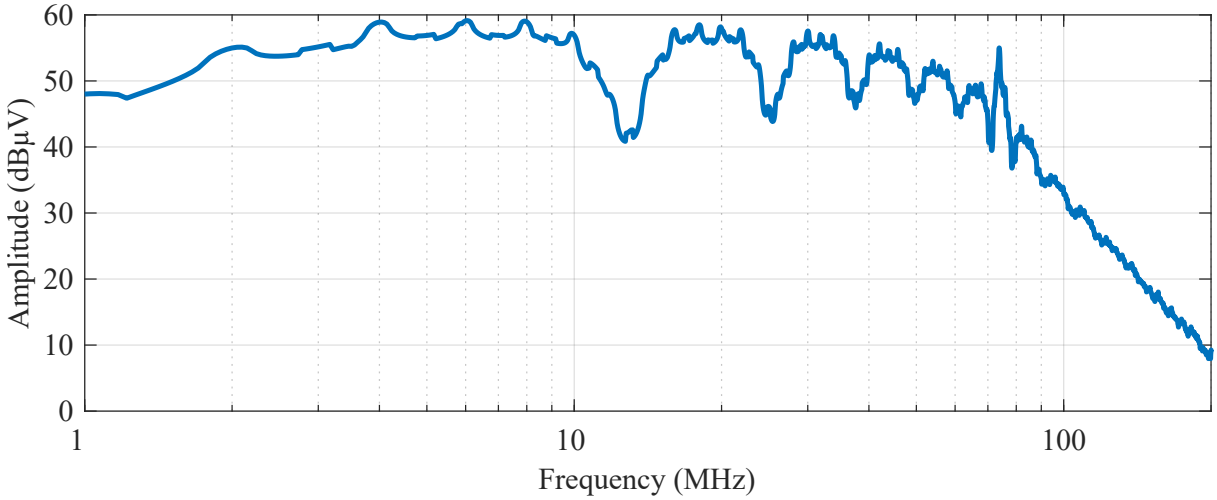


Figure 3.7: FFT from Fig. 2.15 combined with the low-pass filter's magnitude results in the weighted disturbance voltage spectrum.

Oscillation Amplitude

In contrast to the broadband emission caused by the general switching trapezoid, the overshoot or oscillation following a switching instance is a narrowband emission. Hence, a band-pass filter is more suitable to capture the amplitude of the overshoot and oscillation amplitude, which follows all switching transitions.

The oscillation filter needs to pass the oscillation frequency components and as little of the frequency components introduced by the slope as possible. For this purpose, a band-pass filter is selected with a lower cut-off frequency of 60 MHz and a upper cut-off frequency of 90 MHz. Similar to the slope filter, a fourth order ladder type filter is used. Its structure is shown in Fig. 3.8. The lower cut-off frequency is more important, as it ensures the attenuation of the frequency components introduced by the slope while the determined 69 MHz oscillation frequency is included in the passband centered around 75 MHz. The bandwidth is set this wide, because the oscillation frequency depends on the particular parasitics in the power loop of the converter and the dc-link voltage, V_{DC}. Furthermore, a smaller bandwidth results in smaller tuning capacitances, which would make the filter more susceptible to deviations due to parasitic elements within the filter. The magnitudes of the filter, the probe and the combination of both is depicted in Fig. 3.9. The elements used to realize the aforementioned requirements for this filter are listed in Table 3.3.

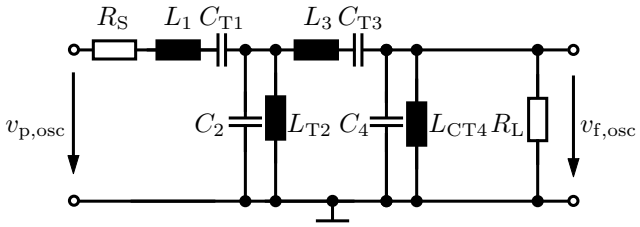


Figure 3.8: Structure of the band-pass filter used to separate the influence of voltage slope from the oscillation amplitude.

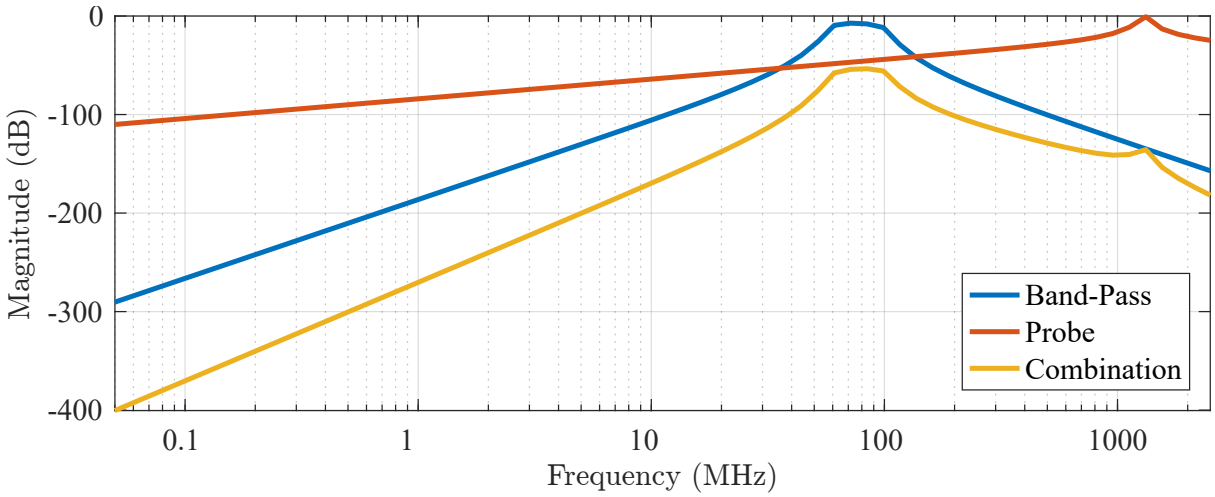


Figure 3.9: Magnitude information of the resulting band-pass filter. Additionally, the probe is considered and the combination of both is depicted.

Similar to Fig. 3.7 the system behavior using the oscillation sensor can be visualized. Therefore, the frequency components of the measurement are weighted with the transfer function of the probe and oscillation filter. The result is depicted in Fig. 3.10 and clearly shows the emphasis on the resonance frequency at 75 MHz.

3.2.3 Amplification and S&H

To overcome the need for a high speed ADC and make use of the internal ADC of the FPGA, the filter output has to be amplified and sampled. The scaling is achieved by using high bandwidth OPs that additionally buffer the filtered signal and feed it to a sampling capacitor. This capacitor C_{hold} holds the amplitude until it has been sampled, after which it will be reset.

Since the slope and oscillation amplitude filters have different output characteristics, the S&H circuits have to be designed differently. The oscillation following a switching instance is a decaying sine wave, which is symmetric in terms of amplitude and independent from turn-on or turn-off event. Subsequently, it is buffered and amplified by $A_{1,o}$ in Fig. 3.11b.

Table 3.3: Band-pass filter element choices.

Parameter	Value	Parameter	Value
R_S	50 Ω	L_3	390 nH
L_1	180 nH	C_{T3}	11 pF
C_{T1}	22 pF	C_4	140 pF
C_2	120 pF	L_{CT4}	39 nH
L_{T2}	33 nH	R_L	40 Ω

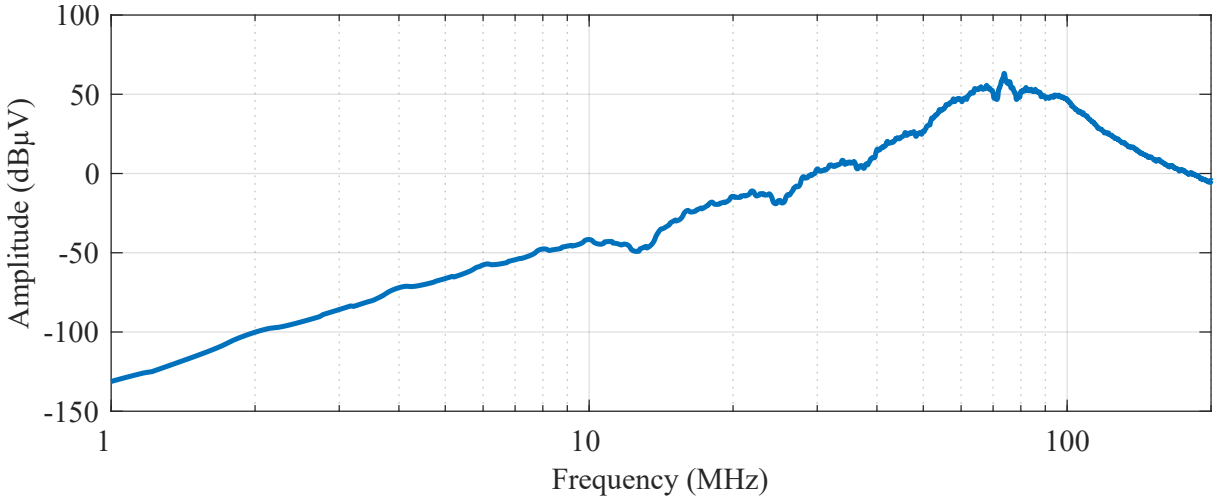
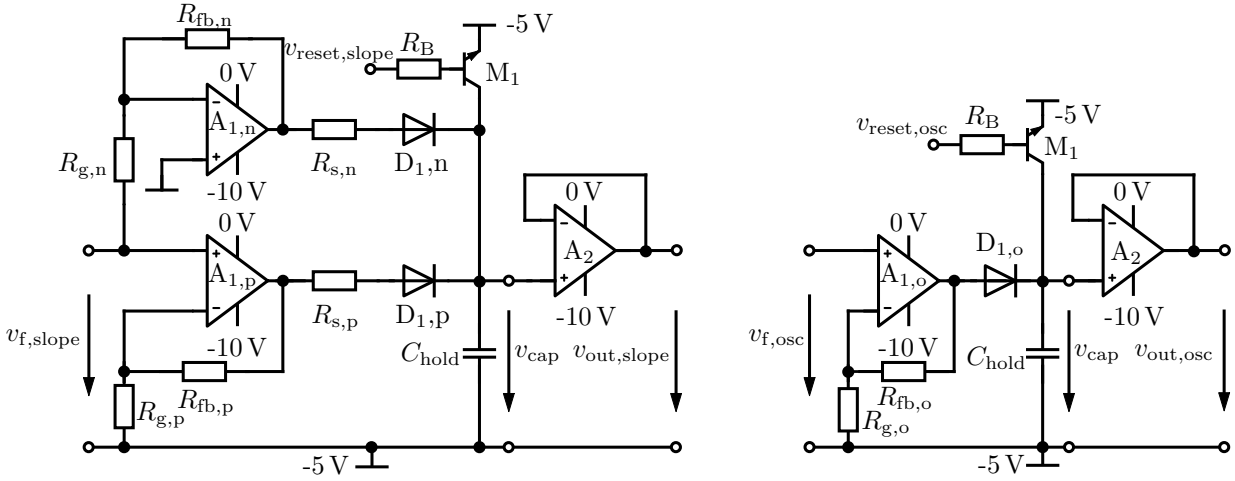


Figure 3.10: FFT from Fig. 2.15 combined with the band-pass filter's attenuation.

The voltage slopes on the other hand, cause either a positive or negative input for the S&H element. Therefore, an inverting configuration has to be included into the circuit. $A_{1,n}$ and $A_{1,p}$ are the respective OPs for the S&H of the slope sensor in Fig. 3.11a. The gains in the input amplifiers $A_{1,\,n/p/o}$ are set to achieve a stable operation and reach the desired voltage on the hold capacitor.

For both configurations, C_{hold} is decoupled from the output of the OPs using a set of diodes D_1. To prevent the ADC from discharging C_{hold}, the voltage is buffered once again using the OPs A_2 in the respective figure.

After sampling the output voltages $v_{out,slope}$ and $v_{out,osc}$ from both sensors, the reset transistor M_1 is triggered. This discharges the capacitor C_{hold} and prepares it for the next switching instance.



(a) Bipolar S&H of the slope sensor.

(b) S&H of the oscillation amplitude sensor.

Figure 3.11: Schematics of the S&H and amplification stages for both sensors. In both v_{cap} is driven by OPs which scale the voltage to 1 V.

3.3 Sensor Characterization

For the characterization of the sensors, earlier measurement results have been used as input for an LTspice simulation. The model contains the probes as well as filters and is used to determine the expected probe and filter output waveforms. Afterwards, the probe outputs are synthesized using a waveform generator and fed into a prototype PCB containing the filters and S&H circuits. Additionally, the cross excitation between the two sensor types and the synthesized input signals can be investigated.

The following sections present the synthesized signals, the evaluation of the filters on the PCB, a characterization of the behavior of the filters in combination with the S&H and finally measurement results at 400 V on the final prototype.

3.3.1 Test Signal Synthesis

The simulation model contains a behavioral voltage source replicating the switching behavior of the semiconductor devices. To obtain the 'measured' v_p in Fig. 3.12 real v_{DS} measurement data is fed into a simulation model of the probe. A distinctive negative excitation is visible followed by some oscillations. This negative excitation is caused by the recorded data of a turn-on event. The goal is to synthesize the first excitation using a signal generator, as it represents the reaction of the probe to the voltage slope during a

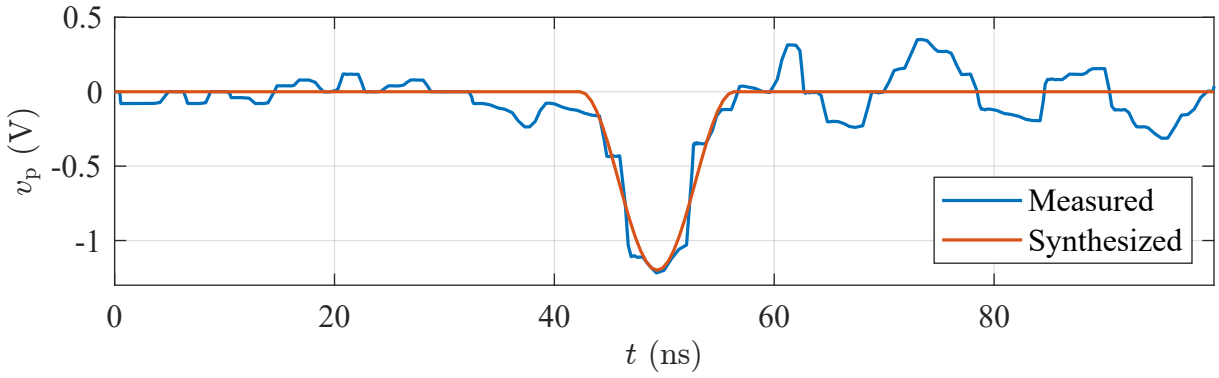


Figure 3.12: Comparison of 'measured' probe response to a slope excitation and synthesized probe output using a signal generator.

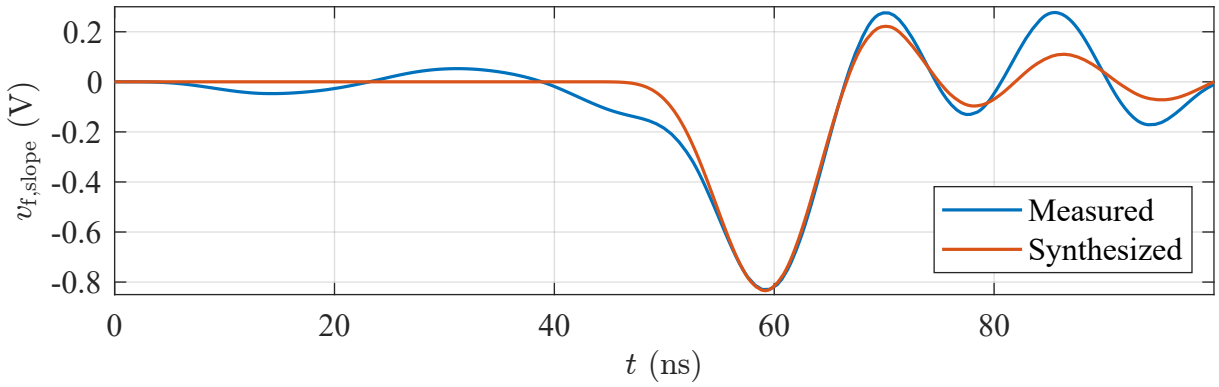


Figure 3.13: Comparison of the low-pass filter outputs in the simulation and the response of the filter to the synthesized excitation.

switching event. Therefore, a single period of a sine wave with the period T, peak-to-peak amplitude a and offset $a/2$ has replicated to synthesize the output of the probe.

Figure 3.13 depicts the filters' response to the 'measured' and synthesized input. The characteristic oscillations in the two simulations are in good accordance. Furthermore, the propagation delay introduced by the low-pass filter can be extracted. The distance between the excitation in Fig. 3.12 and the response in Fig. 3.13 is approximately 9 ns.

A similar process can be applied to the band-pass filter. The measurement used to excite the probe originates from a turn-off event with high oscillations. Two distinctive characteristics of the 'measured' waveform are visible in Fig. 3.14. Firstly, a singular high amplitude pulse at 50 ns. Secondly, the uniform set of oscillations after the first pulse. They are used as the model for the waveform to be synthesized.

To recreate the oscillations a sine wave is synthesized and repeated three times. The response of the filter to the 'measured' and synthesized simulation input is shown in Fig. 3.15. No notable response is shown on $v_{f,osc}$ for the singular pulse caused by the

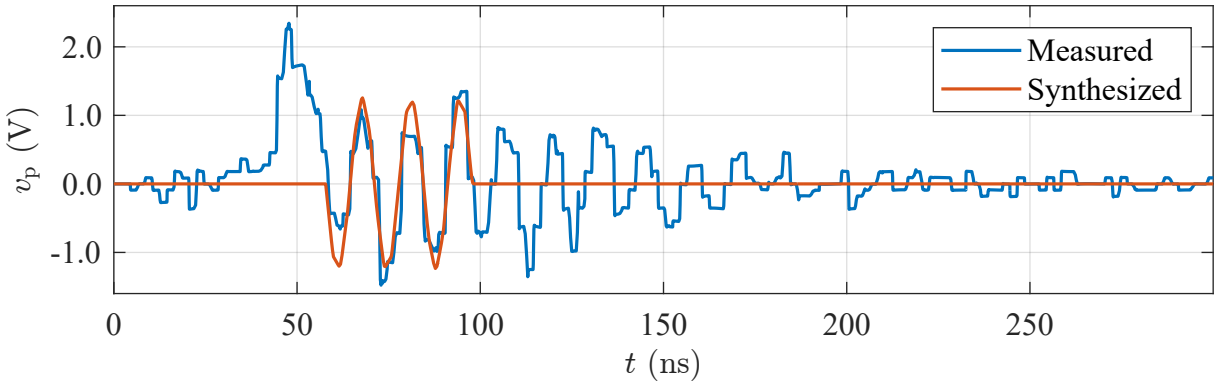


Figure 3.14: Comparison of 'measured' probe response to an oscillation and synthesized probe output using a signal generator.

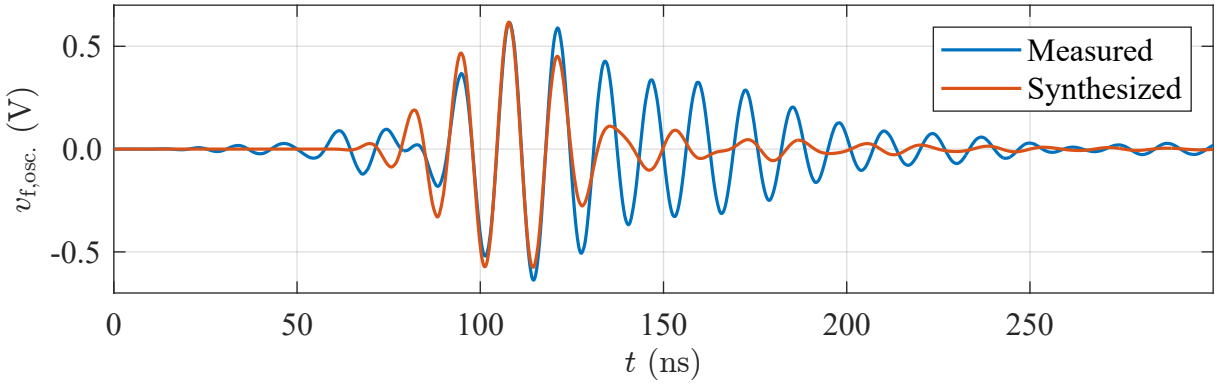


Figure 3.15: Comparison of the band-pass filter outputs in the simulation and the response of the filter to the synthesized excitation.

switching slope. However, the filter does allow the transmission of the sine wave, as its fundamental frequency is inside the band-pass filter's pass-band.

In conclusion, simulations show a good agreement between the 'measured' and synthesized probe output representation. Therefore, the synthesized signals can be used to evaluate the characteristics of the amplification and S&H stage on a low-voltage (LV) PCB and the final high-voltage (HV) prototype. An additional comparison between the bare filters without damping and extra elements and the filters implemented on the prototype PCB is done in the appendix Section A.2.

3.3.2 Characterization of Filters and S&H

After the evaluation of the filter performance in simulations and impedance measurements, the characterization of the sensor's capabilities is done in two steps. Firstly, the synthesized probe output is used to excite the filters on the LV prototype. Then the gate

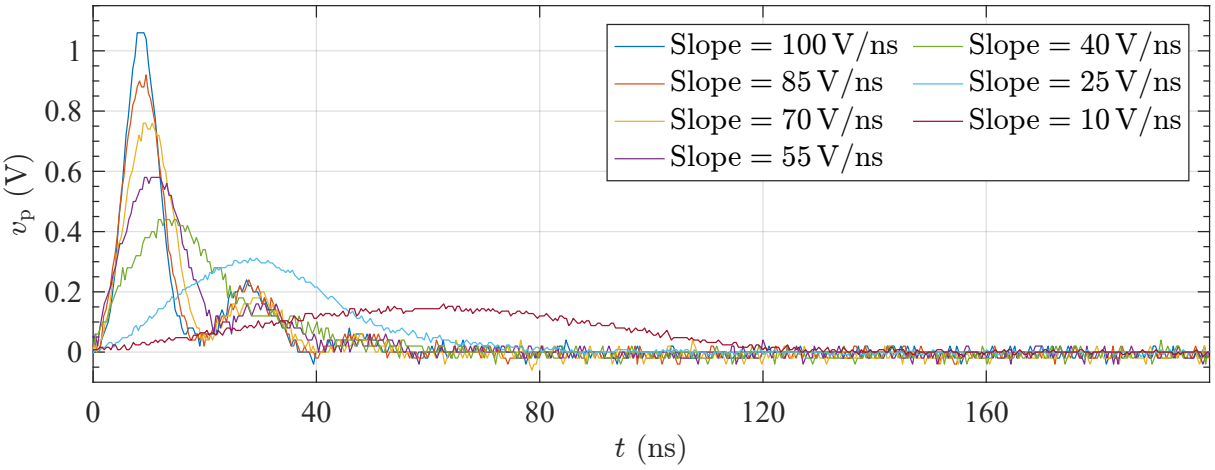


Figure 3.16: Synthesized turn-off slope excitation used for the characterization of the sensor on the low-voltage PCB. The variations in the waveforms correspond to the behavior of different switching slopes.

profile is varied using the AGD on the final prototype. For each variation the FPGA records the output voltage of the sensors and the results are used to characterize the sensors.

Low-Voltage Characterization

The characterization of the sensor design is done first on a LV test PCB. It incorporates the filters and S&H elements. The aforementioned synthesized probe output signals are fed into the filter input ports and the output voltage v_{out} is measured. If the input signal is scaled in a way to reflect different voltage slopes of a switching instance, the output can be plotted over the input setting and the overall transfer function of the sensor is produced. The scaling is done by adjusting the peak amplitude and width of the pulses in a way that keeps the area below the synthesized input constant.

Figure 3.16 depicts the various input signals which represent switching instances between $10\,\mathrm{V/ns}$ and $100\,\mathrm{V/ns}$. During tests with the maximum synthesized slope signal the probe resistance is tuned to match the S&H output voltage to the ADC's maximum input voltage of 1 V. The output of the sensor v_{out} reacts as designed and translates the input pulses to voltages between 0 V and 1 V. This is visible in Fig. 3.17. The black line represents the maximum cross excitation of the slope sensor if it is excited by a signal representing an oscillation. Therefore, very low values measured by the slope sensor could also be a measurement artifact caused by an oscillation. However, as can be seen in Fig. 3.18 the cross excitation reaches only a fraction of the overall range. Additionally, this figure shows an almost linear relationship between the synthesized voltage slope and the slope sensor's output voltage. The same characterization is done for the turn-on slope and the oscillation sensor. The results can be found in Section A.3 of the appendix.

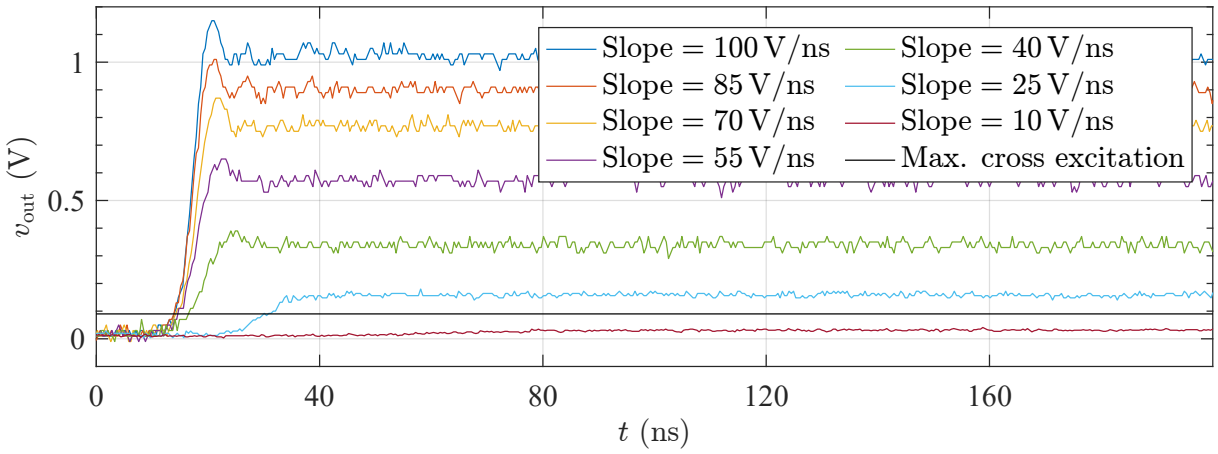


Figure 3.17: Sensor output voltages after an excitation with the waveforms shown in Fig. 3.16. Additionally, the cross excitation amplitude of the maximum oscillation input into the slope filter is shown in black.

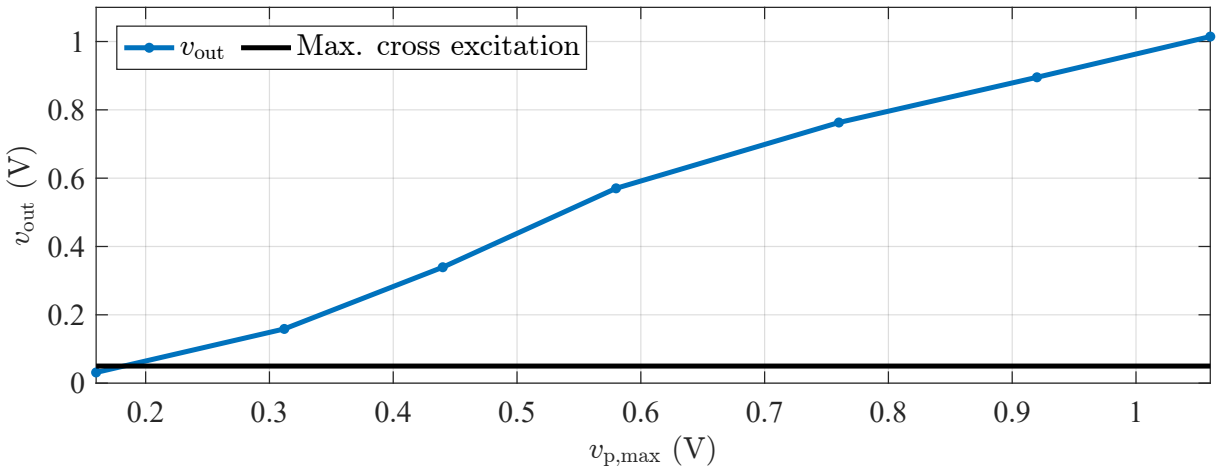
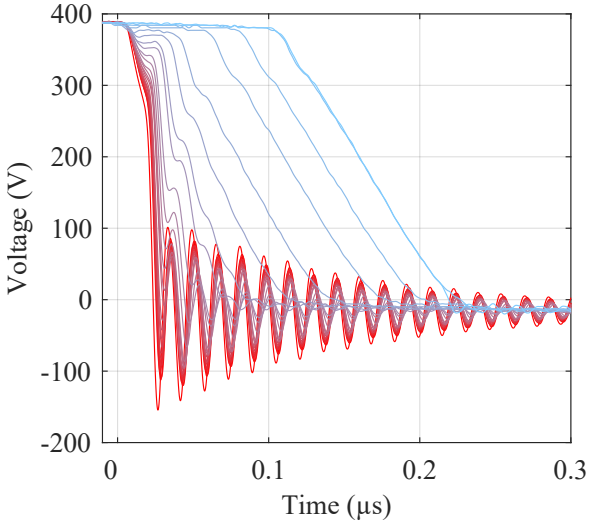
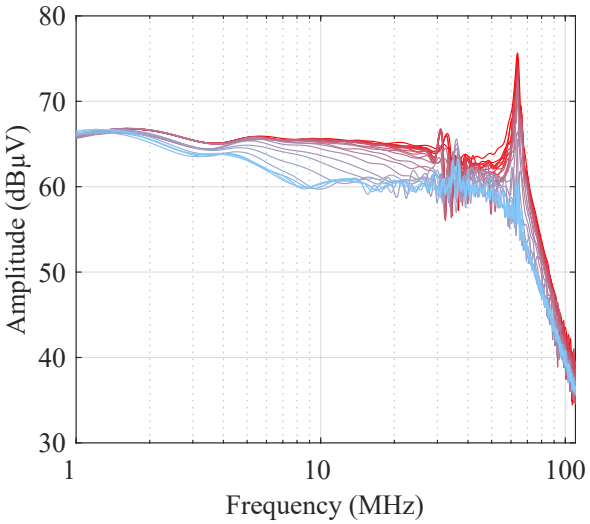


Figure 3.18: Slope sensor's output voltage v_{out} over the peak probe voltage $v_{p,max}$ for synthesized turn-off events. Besides small deviations the sensor output closely follows the linear relationship between the filter input and sensor output.



(a) v_{DS} across the MOSFET for which the switching characteristics are changed. Red corresponds to a fast and blue to a slow switching profile.



(b) FFT of the v_{DS} measurement multiplied with the transfer function of the probe and filter.

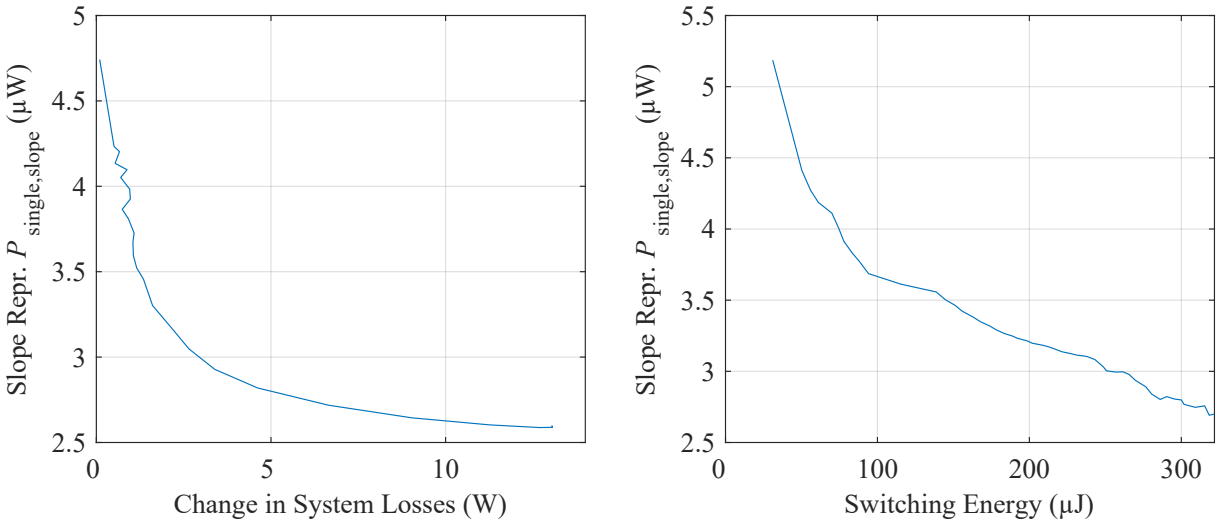
Figure 3.19: Sweeping through the switching profile and the effect of the changes on time and frequency domain characteristics of the switching events.

High-Voltage Characterization

Similarly, to the analysis of the simulation results done in Section 2.4.2, a set of measurements is recorded using the aforementioned AGD. Additionally, the sensors described in this chapter are connected to the semiconductor device and the integrated FPGA records the sensor's output with its ADC. Figure 3.19a depicts the time domain measurement of the drain-source voltage across the semiconductor device during a turn-on event. This measurement is done at the peak of the sine current through the phase leg, which results in a drain current of 25 A. Based on the switching instance shown in the graph, an FFT is done to analyze the switching behavior in the frequency domain. As presented in Section 2.4.2 the spectrum is multiplied with the transfer function of the probe and slope filter. The resulting weighted frequency spectrum is shown in Fig. 3.19b.

Two areas of interest were identified before. Firstly, the wide frequency range from 1 MHz to 60 MHz, which represents the influence of the changing fall time and therefore the voltage slope. Secondly, a narrow-band area around 75 MHz. Here, the resonance of the switching cell is clearly visible. Both areas show decreasing amplitudes going from light red to light blue graphs. With the changing color, the adaptive gate driver was set to adapt the switching slope towards higher fall times.

In comparison to the simulation results from Section 2.4.2 and especially Fig. 2.16 some differences are visible. An imperfect representation of the switching behavior in the simu-



(a) Emission representation over measured system losses when only changing the turn-on switching profiles of one switch of the prototype.

(b) Emission representation over simulated switching losses as first presented in Fig. 2.16.

Figure 3.20: Comparison of prototype behavior and simulation regarding the dependency of the emissions to the losses.

lation model and additional parasitic elements are most likely the cause for higher negative overshoots and a different shape of the voltage transition. This is especially visible for the fast switching instances, while the slower transitions are better represented in the simulation.

The next step is to compare the emission representation derived in Section 2.4.2 to the same value calculated from these single switching instances. For this, the power spectrum is calculated again and the sum of the elements between 1 MHz and 60 MHz is added up. The loss measurement for the real measurements is done using a power analyzer, which records the dc power going into the converter. Because only one switch of the three-phase converter changes its switching behavior for the turn-on events, the changes in the system loss measurement are only caused by the switching characteristics of the depicted waveforms. Plotting the slope representation over the change in system losses is done in Fig. 3.20a. In comparison to the slope representation calculated from the simulation results, which are depicted in Fig. 3.20b, the measurements show a stronger tendency for an asymptotic behavior towards the extreme switching characteristics. Therefore, changing the gate profile away from either the very fast or slow slope results in a drastic decrease of emissions or a great reduction of losses. This indicates the existence of a Pareto optimal line, on which an operating point can be chosen that fulfills the systems need for efficiency or EME.

Finally, a comparison between the sensor performance, the emission representation and oscilloscope measurements can be done. Figure 3.21 depicts the ADC reading and scaled

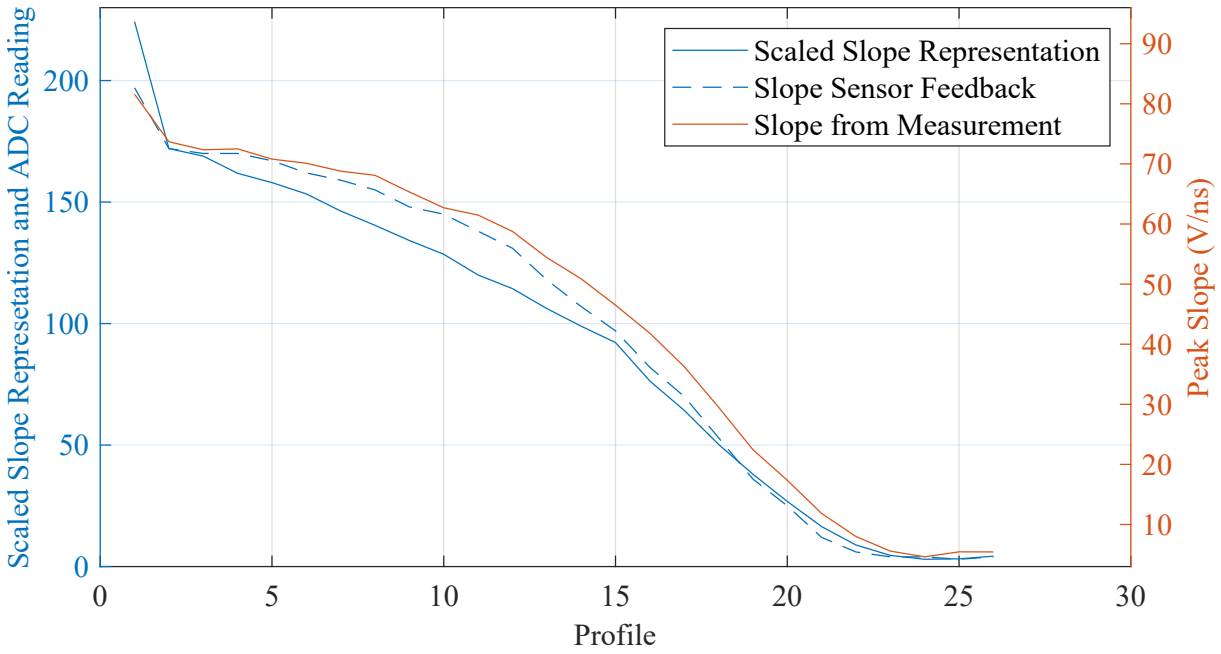


Figure 3.21: Slope representation and the ADC reading of the slope sensor plotted against the peak slope of v_{DS} while varying the gate profile.

emission representation on the left axis and the peak voltage slope calculated from the oscilloscope measurement on the right axis. In order to plot the ADC reading and the emission representation on one axis, the offset from zero is compensated and scaled linearly to match the amplitude of the ADC reading. Both graphs have a very similar shape, which indicates the capability of the sensor to represent the emission behavior of the switching instances. Additionally, the peak slope graph matches the shape of the slope sensors feedback even better. Therefore, the sensor reading is validated against the emission representation and the oscilloscope measurement.

A similar analysis can be done for the oscillation sensor. Figure 3.22 depicts the scaled oscillation emission representation, the oscillation sensor reading and the minimum value of the negative voltage overshoot. Similar to the analysis of the slope sensor, the oscillation sensor shows a close correspondence to the oscilloscope measurement. The scaled oscillation representation has a comparable difference to the oscillation sensor feedback as is visible between the emission representation of the voltage slope and the slope sensor. However, the behavior across the range of changes in the gate profile is very similar in all sensors and emission representation values.

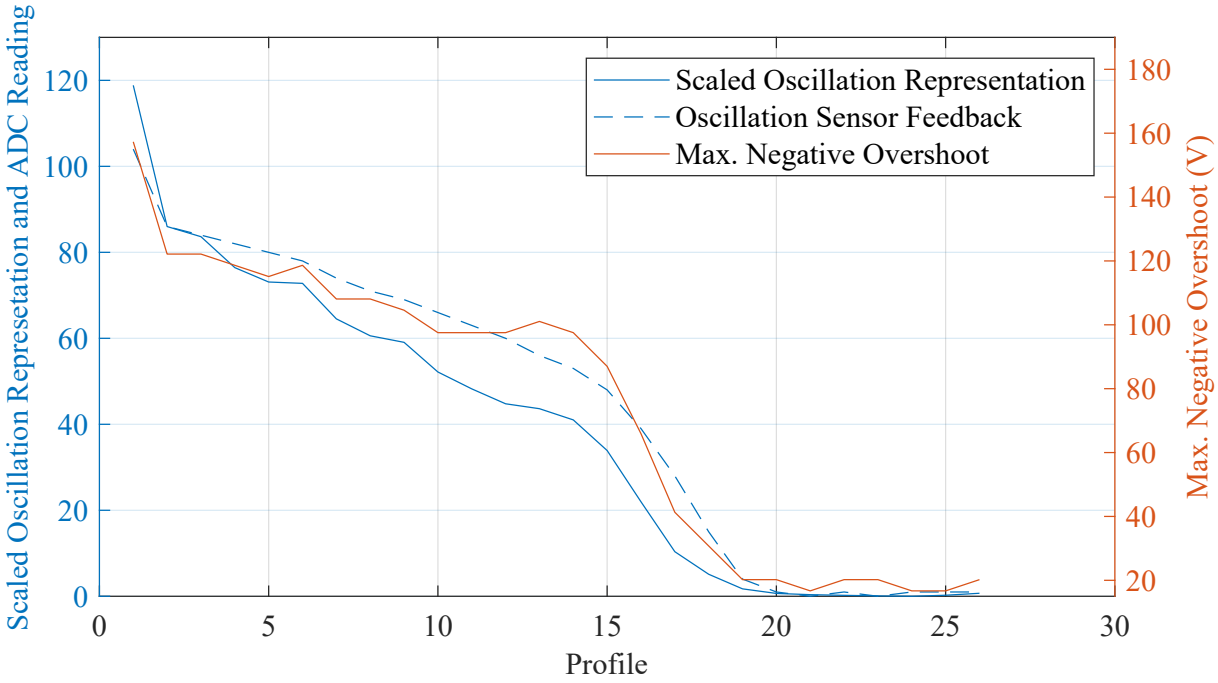


Figure 3.22: Oscillation representation and the ADC reading of the oscillation sensor plotted against the peak slope of v_{DS} while varying the gate profile.

3.4 Summary

Recap

In this chapter, the sensing elements of the control loop were introduced in detail. Firstly, an overview over recent research into sensing approaches for switching characteristics was given. The most popular approaches are to use a capacitive coupling of v_{DS} or to use the Kelvin-source inductance as probes for the switching characteristics. Then, based on an analysis of the semiconductor devices switching characteristics, the bandwidth requirements for the senors were derived. Afterwards, the topologies of the sensors, separated into slope and oscillation sensor, were introduced. The design of each of the sensor stages - probe, filter and S&H - was explained in detail. After the design insight, the sensors were characterized by using synthetic test signals and a 400 V operating point in which the gate profiles were adapted to produce a variety of voltage slopes and oscillations.

Conclusion

Placing a sensor for switching characteristics on the same PCB as the AGD, allows implementing a closed control loop. The sensors provide measurements, which represent the switching characteristics with regards to the voltage slope and oscillation amplitude.

In consequence, their output is used as feedback path for the control loop and allows adapting the switching behavior according to a comparison of set points with the sensor measurements.

4 Closed-Loop EME Control Algorithm

As a consequence of the development of the AGD and EME sensors, the on-board FPGA can be used to evaluate the sensor outputs and to adapt the gate profiles. This is done according to the algorithm which is presented in this chapter. A brief overview over the literature regarding different approaches for closed-loop controlled gate drivers is given. Subsequently, the control algorithm developed for this thesis is introduced. The general structure, an insight into the control settings and a detailed description of the internal implementation of the control algorithm is given. Afterwards, two examples using different control strategies in different operating conditions are presented.

4.1 Literature Review

Control approaches, without closed-loop feedback between gate drivers and sensing elements, have been reviewed in Chapter 2. Here, only research, which proposes closed-loop control of the switching behavior, is presented. Between research approaches, there are differences in the time scope of the control loop, the adaptability of the parameters, the operating points and the types of measurements used as feedback.

Firstly, an approach that uses external measurement devices to analyze the switching behavior is reviewed. In [34], a sinusoidal output is divided into sections and the switching characteristics for each section are analyzed offline. Based on this analysis, LUTs are created to change the gate drivers' behavior and the desired switching characteristics are adapted iteratively.

The authors of [43] propose an approach which is closer to an integrated closed-loop control. Their driver integrates the voltage across L_S to measure the amplitude of the sinusoidal load current and adjusts the gate control according to requirements set in LUTs. The contents of the LUTs are derived analytically beforehand. In terms of operating points and measurements, no EME analysis is done, the ac operating point is not varied and only loss measurements of single switching instances are shown. Additionally, no measurements of the dynamic behavior of the control are presented.

The authors of [44] use a feedback signal, which is derived from the inductance L_S in the power path, as negative input for their gate driving circuitry. This way, a dynamic reaction to changes in the switching current is possible. However, the adaptability of the

influence of the feedback on the gate driver can only be partially influenced externally. Furthermore, no dynamic adjustment of the control or the ac operating point is shown and no emission measurements are done.

The closest approach to implementing a closed-loop controller is presented by [18]. An integrated gate driver for a 400 V GaN semiconductor device is proposed. The complete closed-loop control loop is integrated into an ASIC to achieve a very high control bandwidth. But, the study does not show ac operating points or an adjustable control loop.

In [26] the AGD from Chapter 2 and sensors from Chapter 3 are combined to present a closed-loop control approach for SiC MOSFETs. However, no ac operating point and emission measurements are shown.

In general, no complete on-board, closed-loop, dynamic control of switching characteristics and EME is presented in the literature.

4.2 Control Algorithm

The controller block of the closed-loop control scheme presented in this thesis is highlighted in Fig. 4.1. It receives emission set points, compares them to the sensor measurements and decides how to adapt the gate gate profiles for the next switching event. The control algorithm runs on each FPGA of each driver module. Six driver modules are connected to the six switches in the three-phase converter. The implementation of the algorithm in very high-speed integrated circuit hardware description language (VHDL) on the FPGAs can be simplified to a closed-loop controller, which contains the components depicted in Fig. 4.2. In the first step, internal PI values based on the set point and sensor readings are calculated. Afterwards the PI values are evaluated and according to the control settings, changes to the gate current profile are made.

The following sections give an overview over the control algorithm and exemplary operating points emphasizing the capabilities of the control algorithm.

4.2.1 Overview

Figure 4.2 depicts an overview of the relevant signal paths and modules implemented in the FPGAs. All modules inside the FPGA exist for turn-on and turn-off switching events independently. This way, the next turn-on event is prepared just after the last turn-on event has been evaluated. Therefore, the two controllers run independently and in parallel. The differently colored areas mark the clock speeds the respective regions are running on. To maximize the gate driver's dynamics, the reference output module for

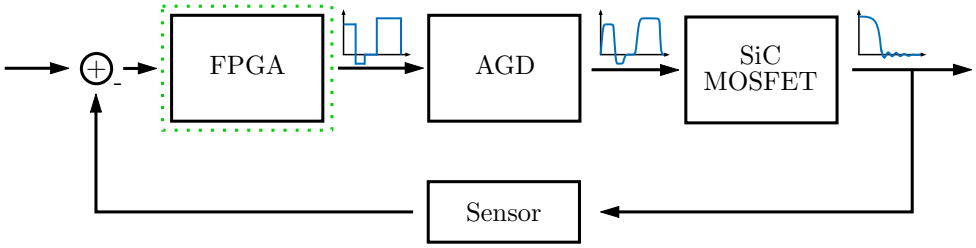


Figure 4.1: Control loop emphasizing the FPGA containing the control algorithm.

the AGD is running as fast as possible. On the Artix-7 this results in a clock frequency of 400 MHz for this implementation. This is possible, because only the FIFO reader and very simple logic are running at this clock speed. Therefore, interconnections to other modules are reduced and timing issues are prevented.
The FIFO guarantees a good performance, while still maintaining data integrity between two different clock domains. It is filled from the 100 MHz side. Here, all communication, control and evaluation logic is running. This allows more complex logic usage and less tight timing constraints.The third and last clock region is dedicated to the internal ADC. It operates at 240 MHz to allow a maximum sample rate of 1 $^{\mathrm{MS}}/_{\mathrm{s}}$ at a resolution of 12 bit.

In the following subsections, the communication interface and the options for the control settings will be explained in greater detail. The inputs for the control settings are visible on the bottom border of Fig. 4.2.

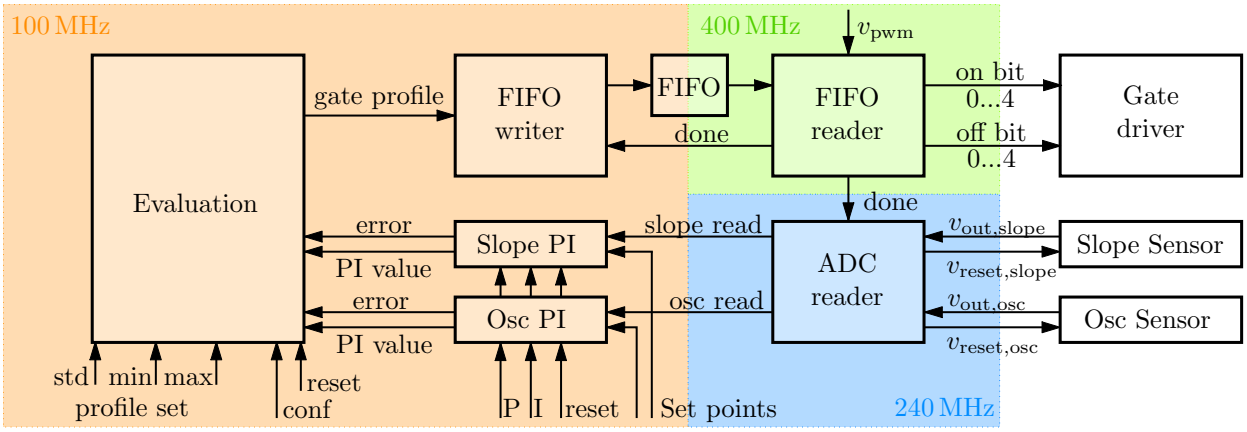


Figure 4.2: Structure of the control loop which is implemented on the FPGA on each driver module.

4.2.2 Communication

To allow changes in the operating behavior of the converter itself and especially of the control loop, a communication network is set up. Every link of the network runs the universal asynchronous receiver/transmitter (UART) protocol. Between the testbench

PC and the MCU an optical UART link is established. PWM and gate control settings are transmitted here. Onboard the prototype itself, the MCU is able to address each driver module individually. This is done by using a set of multiplexers, which are controlled by the MCU. Therefore, information via UART can only be sent to one driver at a time. Feedback, such as sensor readings or control parameters, from the FPGAs has to be requested by the MCU, because only the MCU can activate the UART channels to each driver. This optimizes the communication because the FPGAs only need a PWM input and work independently in all other aspects. If the control settings are to be changed during operation however, each driver module has to be updated individually. This can be done while the converter is running.

In addition to the UART interfaces, each driver module shares a set of dedicated logic lines with the MCU. They carry the PWM signals or enable the control algorithm from the MCU to each driver. Also, a fault can be communicated from the driver modules back to the MCU.

4.2.3 Control Settings

The control settings can be divided into two categories. Firstly, the AGD needs basic information how the switching profile should look like. The basic structure of the profiles is introduced in Section 2.3.2. Since the controller will adapt it, a certain range of allowed changes is needed to ensure safe switching events. The range of changes are given by the minimum and maximum profiles provided in addition to the standard profile. All three profiles are contained in a gate profile set which is one of the characteristics of a control approach.

The second method of influencing the controller behavior is to change the internal variables. A variety of custom thresholds, gains and further settings are allowed to be changed. They are contained in the control settings sent to the drivers by the test bench PC. The profile set and control variables are introduced in the following sections.

Gate Profile Set

Because the controller uses the gate profiles to adapt the switching behavior, boundaries have to be introduced in order to guarantee safe operation. In case of the implemented controller, additionally to the standard profile, a minimum and maximum version of the standard profile are given. Therefore, a 3x3 matrix describes each state. Figure 4.3 depicts all three profiles for an exemplary turn-on optimization. It is noteworthy, that the minimum and maximum profile will not create a corridor around the standard profile because the state duration can also be varied, which will distort the appearance.

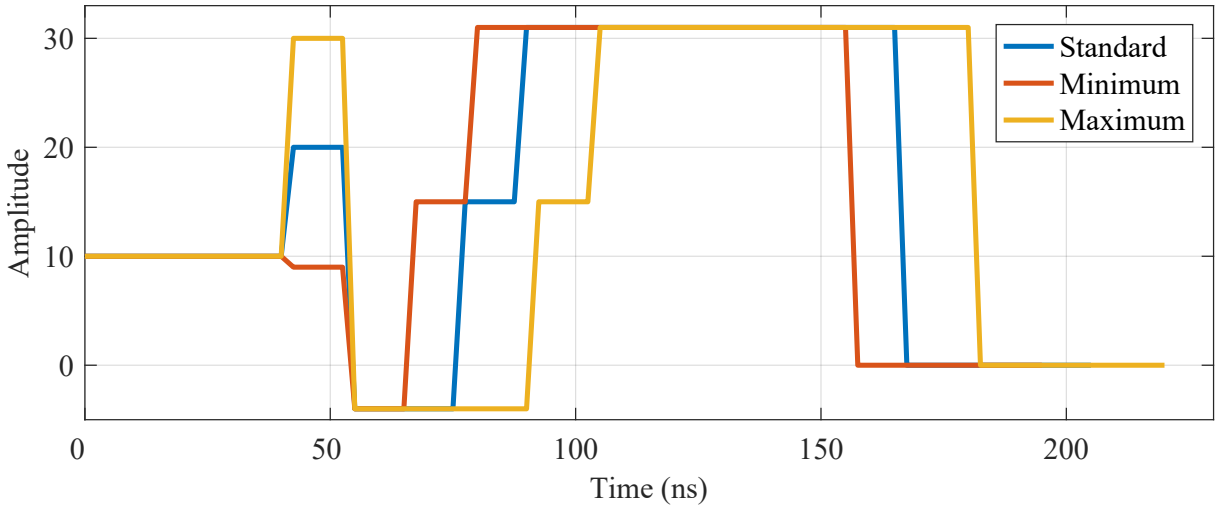


Figure 4.3: Example turn-on optimization profile set.

A more detailed representation of the exemplary profile set is listed in Table 4.1.

Table 4.1: Profile set depicted in Fig. 4.3 in a detailed table representation.

Name	S_1			**S_2**			**S_3**			S_4			S_5		
variable	on	off	dur	**on**	off	dur	on	off	**dur**	on	off	dur	on	off	dur
max	10	0	17	**31**	0	5	6	10	**15**	16	1	5	31	0	31
std	10	0	17	**21**	0	5	6	10	**9**	16	1	5	31	0	31
min	10	0	17	**10**	0	5	6	10	**5**	16	1	5	31	0	31

In this example, the states S_2 and S_3 allow the controller to use either the turn-on amplitude or the duration as control variables. The amplitude a_2 can be varied between 10 and 31 steps and the duration d_3 between 5 and 15 clock cycles at 400 MHz. This results in a possible adjustment of the duration between 12.5 ns and 37.5 ns.

Because adapting different parameters results in different effects on the switching characteristics, the control algorithm receives another set of variables. This way, it can prioritize the different parameters and decide in which direction to adjust them. The control variables are introduced in the next section.

Control Variables

In addition to the gate profiles, the controller receives information on whether and how to change which parameter for up to three possible parameters. A parameter in this case can be any column of Table 4.1 for the turn-on controller. The turn-off controller is given similar information regarding the turn-off profile set.

Therefore, four choices have to be made for each parameter and on- or off-transition:

- Parameter type (amplitude on, amplitude off or duration of state)
- Position of state in profile
- Sign/Direction of adjustment relative to the error calculated in the PI controller
- Enable/Disable decides if this parameter is active

Table 4.2 contains the aforementioned variables for the turn-on controller. The direction variable indicates if the specified parameter is increased or decreased depending on the sign of the calculated error between the set point and sensor measurement. Its behavior is described in (4.1).

$$dir = 1 \begin{cases} error > 0 \Rightarrow \text{increase parameter} \\ error < 0 \Rightarrow \text{decrease parameter} \end{cases}, dir = 0 \begin{cases} error > 0 \Rightarrow \text{decrease parameter} \\ error < 0 \Rightarrow \text{increase parameter} \end{cases} \tag{4.1}$$

Table 4.2: Control variables corresponding to the profile set listed in Table 4.2.

# Parameter	Type	Position in Profile	Direction	Enable/Disable
1	amp. on	2	1	Enable
2	duration	3	0	Enable
3	-	-	-	Disable

Furthermore, the set points for the PI controllers have to be defined and transmitted. These set points are compared to the ADC readings of the corresponding sensor and are the basis for the PI calculation.

The final parameters are the gains of the PI elements of the turn-on and turn-off controller. All of the aforementioned settings are set on the test bench PC, transmitted through the MCU and then stored on each driver individually. This way, differences in the driver hardware or variations in the parasitics of the semiconductor devices can be addressed.

4.2.4 Evaluation Module

The evaluation module of the controller exists for both turn-on and turn-off switching events separately. It receives information about the PI values, the profiles, the controller configuration, the sample state of the ADC module, the state of the gate output and the enable/disable state of the control. Internally, a latch ensures all input values are

considered before a state machine initiates the evaluation process after each switching instance. The next sections will go into detail on the most important parts of the evaluation module.

Applying Updated Settings and Reset

The evaluation module checks if new profiles and settings are available from UART and updates the local variables according to the new input. After an update of the control variables or a manual reset of the internal variables, the standard profile is applied to the gate and all internal PI values are reset. Without a prior reset, the controller bases its adaptions to the gate profile on the amplitude of the difference between set point and ADC reading and the changes made in the previous switching iteration. To achieve this, the next state of the evaluation module takes different thresholds and boundaries into account. These will be explained in the next sections.

Control Thresholds

The behavior of the controller is mainly defined by the control variables and parameters, but additional checks and thresholds are introduced to optimize the controller. These additions to the PI-controller help to handle the non-linear characteristics of the control loop and reflect the discrete character of the control algorithm. The non-linearity is caused by the different effects the different control parameters have and the discretization of the adjustment of the control parameters. In total, there are the three following additions to the PI-controller.

Control Parameter Change Deteriorates ADC Reading When the last change, applied to the gate profile by the evaluation module, causes a deterioration of the ADC reading, the change to the profile is reversed. In the next switching cycle, the previously adapted parameter is kept constant and the next parameter is chosen to be changed.

Distance from Set Point to PI Value With every new switching instance the sensors are sampled and the corresponding ADC reading is the input for the PI-controllers. The output of the controllers is the error between the set point and the ADC reading as well as the internal PI value, which is calculated from the error and the PI gains. Depending on the PI value in relation to the thresholds T_1 to T_3, bigger or smaller steps are taken to change the profiles. Figure 4.4 visualizes this method. This speeds up the adaption of the control parameters, if the set point is far from the current ADC reading. The sign of these steps is inverted if the direction setting of a parameter is set to zero.

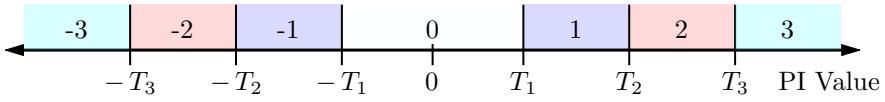


Figure 4.4: Control threshold levels used to determine the adaption step size. The sign of the steps is determined by the sign of the PI value and the direction setting for each control parameter.

Reaching a Profile Boundary The previously introduced steps are allowed to adapt the corresponding parameter until either the minimum or maximum value provided in the profile set is hit. If a boundary is hit, the next parameter is chosen to be adapted. In case the last parameter is reached, the controller is not able to make further adaptions to the gate profile. Before the changes in the profiles are handed over to the AGD, the parameters are compared to the limits and corrected if they violate the boundaries.

Applying the Changed Profiles to the Gate Driver

The controller calculates the changes for the control parameters and applies them to the profile. Afterwards, the profile is provided to the AGD. At the same time, the previous profile is saved. Thus, the controller is able to take changes back, if they lead to a deterioration of the switching behavior. If the evaluation module does not finish or an invalid profile is created for any reason, a watchdog module will provide a default profile to the AGD to ensure safe operation. This default profile will not satisfy the emission set points, but allow a reset of the controller or indicate a fault to the MCU if the controller does not resume proper operation.

Blanking the Controller

The blanking state indicates whether the selected driver is able to influence the switching characteristics in the present section of the sine period. This depends mainly on the sign of the phase current and whether the switch is a high- or low-side switch. Because the drivers have no integrated current measurement, they rely on analyzing the switching behavior during the sine period. As Fig. 4.5a shows, a clear pattern with two characteristic cuts is visible in the ADC readings on the y-axis. These cuts indicate switching instances at very low load current amplitude. Therefore, the driver, without the need for a current sensor, can locate the positions of the zero crossings of the load current. The x-axis contains the index of the switching iterations after the feedback was requested. Consequently, it represents the time, but is counted in switching periods.

Between iteration 13 and 50, the driver, which provides this feedback, is able to influence the switching behavior. Therefore, the evaluation module is not in blanking mode and the full control loop is active. During the rest of the sine period, the control is in blanking

mode and the control parameters are frozen. The controller remains in this state until it detects a steep decline in the turn-on slope readings. If the controller is in blanking mode, no changes are made to the gate profiles and the PI value calculation is blocked. This way, the controller can start into the next active half period with the same parameter values as was applied for the last switching iteration of the last half sine period.

4.2.5 Feedback

The driver is capable of storing and forwarding ADC readings and profile settings of up to 110 switching iterations. The following sections will go into detail on how and which information can be made available.

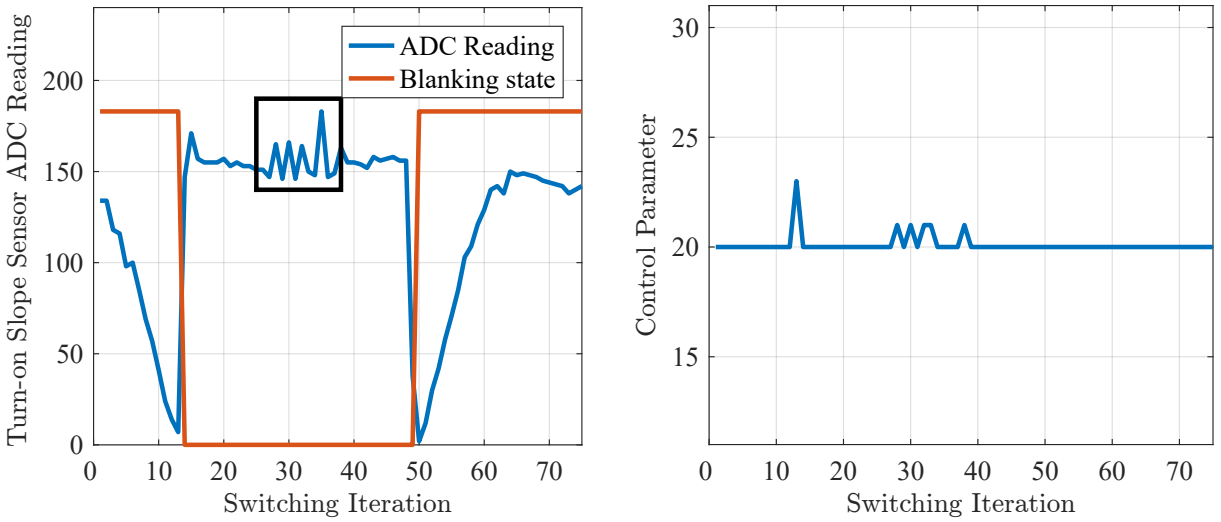
Because the drivers can not open the UART link by themselves the MCU sends a command to the driver to initiate the collection of the feedback. After the driver receives the feedback command, it starts to collect the following information for turn-on and turn-off switching events:

- Amplitude and duration parameters of the first four states of the reference gate profiles, including the changes the controller applies
- Sensor readings for slope and oscillation sensors
- Internally calculated PID values
- Optimization state, which indicates the active control parameter
- Blanking state

Figure 4.5a contains an exemplary ADC reading of a turn-on slope sensor. The x-axis is depicting the count of switching iterations after the feedback was requested. Each count corresponds to a full switching cycle containing a turn-on and turn-off instance.

Figure 4.5b depicts the changes to the control parameter as the controller requests them during the active control period. In comparison to Fig. 2.11, this style of graph is better suited to emphasize the changes in the control parameters over time if the remaining states of the profile are of no interest. Between iteration 11 and 39, changes in the amplitude of the second state's turn-on amplitude can be seen.

The oscillation, which is highlighted on the ADC reading between iteration 25 and 39, is caused by a mismatch of the control settings and the effects that the changes of the gate profile have on the switching characteristics. In this case, a change of the control parameter by one point causes a high step in the ADC readings. There is several ways



(a) ADC Reading of turn-on slope sensor and scaled blanking state.

(b) Control parameter $a_{2,\mathrm{on}}$.

Figure 4.5: Turn-on and turn-off parameter changes as received by feedback during control period.

to counteract the oscillation effect. Firstly, decrease the control gains to decrease the severity of the changes in the internal PI values. Secondly, increase the thresholds for retracting the last change which lead to a worse sensor reading as the state before. Finally, adapt the profile to show a more granular effect, of the small changes to the profile, on the switching characteristics. Overall, the control algorithm offers many degrees of freedom to allow for better control. However, for an EME measurement a single switching instance with different characteristics does not have a high impact. This is due to the averaging effects of emission measurements, which take up to several minutes. Therefore, the overall performance of the controller is more important than the overshoots and minor oscillations.

4.3 Control Examples

The following section will present two control examples to demonstrate how the control algorithm works. The first example is a dc operating point, in which no load is connected to the switching node. The second example demonstrates the control algorithm in an ac operating point.

4.3.1 DC Control Example

This example presents a synthetic operating point, which solely aims at providing an environment without many disturbances for the control algorithm. Without any load connected, there is no load current. Therefore, all switching instances have the same characteristics which are only dependent on the gate driving characteristics and the controller's dynamic behavior. The following sections contain details on the control parameters and measurement results for this exemplary operating point. Parts of this analysis have been shown in [26].

Control Parameters

In this simple synthetic operating point, the goal is to reach the set point for the slope sensor's ADC reading of the turn-on instances. To achieve this, the controller is allowed to adapt multiple control parameters of the gate profile. Table 4.3 contains the profile set describing the standard, maximum and minimum parameter values the controller is confined to. The controllable parameters are bold.

Table 4.3: Profile set used in this synthetic dc multi-parameter control example. The bold columns mark the parameters which are adapted by the controller.

# State	S_1			S_2			S_3			S_4		
Parameter	**on**	off	**dur**	on	off	dur	on	off	**dur**	on	off	dur
max	**31**	0	**15**	0	12	2	0	0	**31**	31	0	25
std	**31**	0	**13**	0	12	2	0	0	**13**	31	0	25
min	**17**	0	**7**	0	12	2	0	0	**13**	31	0	25

Table 4.4 lists the control variables for this control example. For each parameter, the type, position, direction and enable information are saved and transmitted to the FPGA. The duration of S_1 is the parameter with the highest effect on the switching characteristics and will be adapted first. $a_{1,\text{on}}$ and d_3 are the following parameters, that allow a more granular adaption of the switching characteristics.

Table 4.4: Control settings for multi parameter dc example.

# Variable	Type	Position in Profile	Direction	Enable/Disable
1	duration	1	1	Enable
2	amp. on	1	1	Enable
3	duration	3	0	Enable

Additional control settings are the PI gains and the set point. The gains for the P and I controller are implemented as conventional parameters of a control loop. In this example

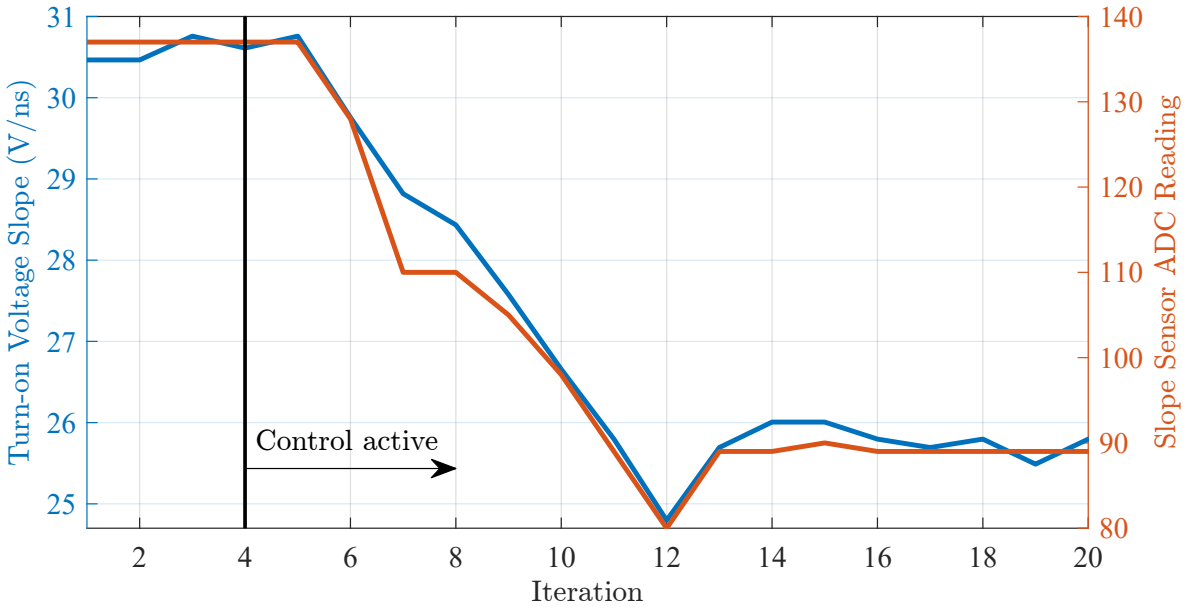


Figure 4.6: Results comparison between slope sensor measurement and oscilloscope measurement [26].

the proportional gain $K_{\mathrm{P,on}}$ is set to 4 and the integral gain $K_{\mathrm{I,on}}$ to 9. The range of gains is limited to values between 1 and 31. Furthermore, the set point, as indicated in Fig. 4.2, is used as reference value for the controller. Because it is compared to the ADC readings, values between 0 and 255 are valid.

Results

The results of the control algorithm's operation are depicted in Fig. 4.6. Here, the voltage slope measured with an oscilloscope and calculated between 90 % and 10 % of V_{DC} is depicted on the left y-axis. The right y-axis shows the slope sensor's ADC reading. Both are in good agreement and show a decline of the sensor reading from 135 to 89 between iteration 5 and 14. In the slope sensor reading, two distinctive steps at iteration 7 and 12 are visible. Their origin will be explained by analyzing the changes which the controller applies to the control parameters.

Figure 4.7 contains the values for the control parameters and how they changed with every switching iteration. At iteration 4, the controller is activated and all values are set to their standard value. According to Table 4.4 d_1 is adapted first. Following its direction setting, the parameter is decreased because the set point is below the measurement taken by the slope sensor. Therefore, the duration decreases until d_1 reaches its minimum value, which is limited by the minimum profile given in Table 4.3. After a full switching cycle the second parameter is adapted in the same manner. The transition between two control

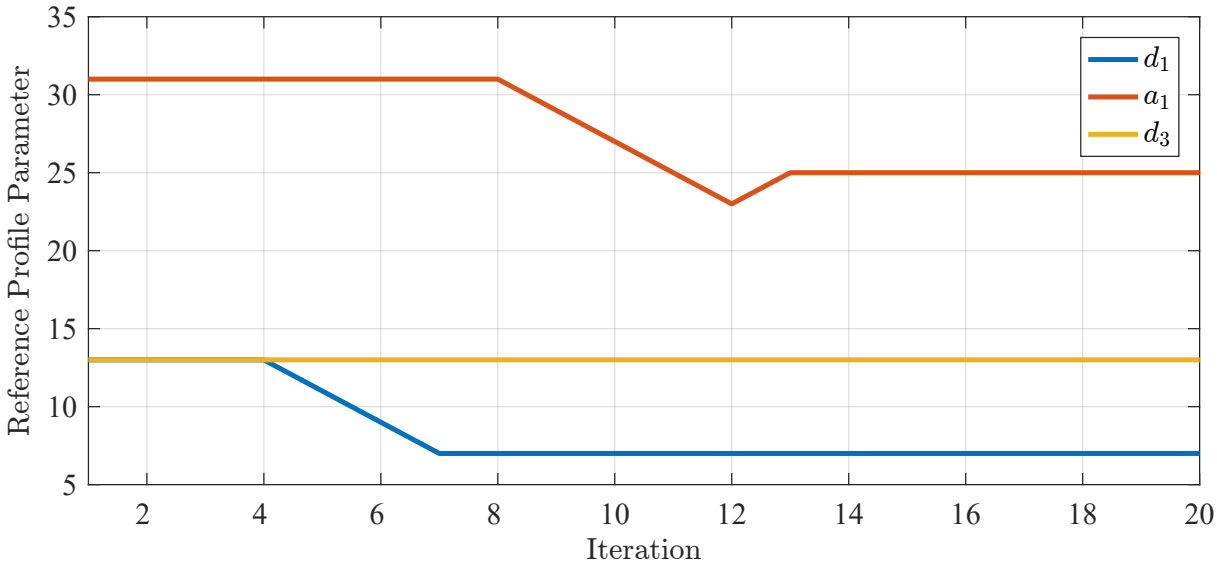


Figure 4.7: Variation of control parameters over the course of the dc control example [26].

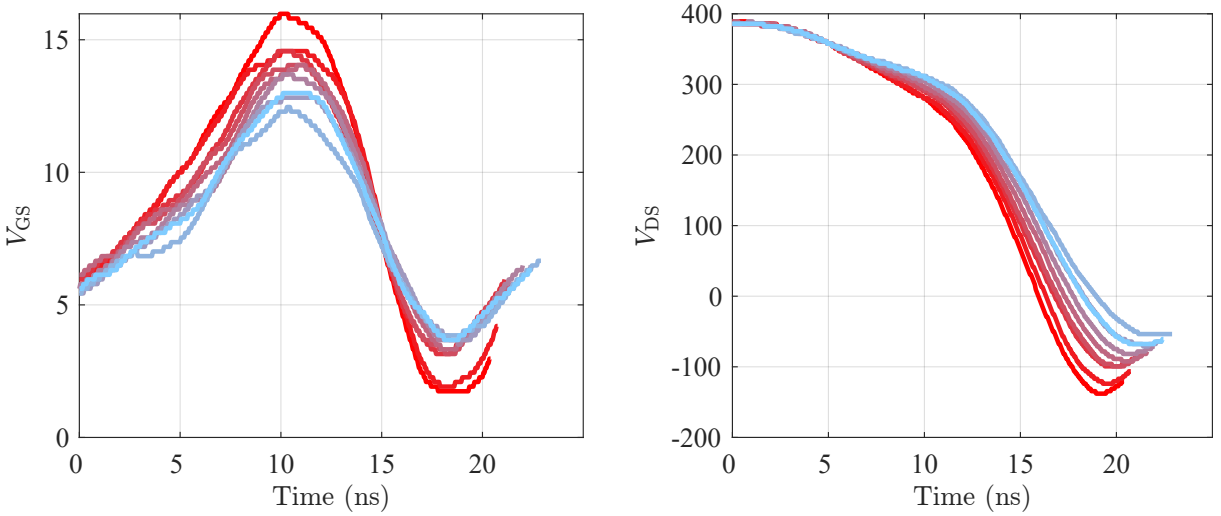
parameters takes a full switching cycle, which is visible between iterations 7 and 8 where no changes are made to the parameters.

At iteration 12, a negative overshoot in the measurements of the sensor and the oscilloscope occurs. The controller recognizes this negative overshoot and reverts the last change. This results in switching characteristics which are very close to the desired set point. Therefore, the third parameter is not used in this example.

In the time domain, the changes to the control parameters result in the waveforms depicted in Fig. 4.8. With increasing iteration index the color of the plots changes from light red to light blue. Besides the changes in the voltage slope, the negative overshoot is also reduced from $-138\,\mathrm{V}$ to $-67.7\,\mathrm{V}$.

The large negative voltage swing on v_{GS} in Fig. 4.8a is caused by the characteristics of a current source gate driver. In contrast to a conventional voltage source drivers, which is represented by a short circuit in its equivalent circuit, a current source is represented by an open connection. During the falling edge on v_{DS}, C_{GD} is discharged. The charge, which is pulled out of this capacitance, can not be provided by the current source gate driver and will be provided by C_{GS}. This forces the voltage across C_{GS} to drop during the turn-on transition of v_{DS}. Therefore, negative pulses on v_{GS} are apparent during turn-on and positive pulses for turn-off events. For a voltage source driver, this effect results in the miller plateau as depicted in Fig. 2.3a.

If the set point for the controller is defined in a way that the resulting switching transition takes longer than the first three states combined, the third parameter has to be used to prolong the last state. According to its direction setting, it will be increased if the PI-



(a) Progression of v_{GS} during the controllers operation.

(b) Progression of v_{DS} during the controllers operation.

Figure 4.8: The colors of the plots progress from light red to light blue with increasing number of iteration in the previous figures. Therefore, the final measurements are not the most extreme, but one step back from the lowest or highest values at 10 ns and 20 ns respectively.

error is negative. This gives the voltage transition more time to finish before the gate is rapidly brought into a safe turn-on state by charging it to V_{on}. The final charging to V_{on} is omitted in Fig. 4.8a, because the switching event is over before the gate is fully charged.

4.3.2 AC Control Example

Based on the previously shown control capability, the following example replaces the synthetic dc behavior with an ac operating point. The prototype operates in three-phase sinusoidal inverter mode now. A purely inductive three-phase load is connected to the output of the converter. Therefore, this example resembles a traction inverter application in terms of the operating conditions for the semiconductor devices. In the following sections, the experimental setup and measurement results are presented.

Experimental Setup

For this example, the converter is operated at 50 kHz and 500 V dc-link voltage. A RMS load current of 17.5 A is modulated at a fundamental sine frequency of 500 Hz. Analyzing the behavior of a single switch in one phase is sufficient, to show the control algorithm

operate under ac conditions. Therefore, the measurements are limited to v_{DS} across a low-side switch. However, the feedback of a high-side driver is recorded and shown in the next section. Because the high-side driver is only capable of influencing the switching characteristics when the phase current i_{AC} is positive, feedback polling is started during the opposite sine period. This way, the positive part of the load current waveform is in the center of the feedback data.

Both, the high- and low-side drivers have been given the same set points for the controller and the slope sensor is chosen as input for the PI controller. For the turn-on controller the set point is 90, for turn-off 30.

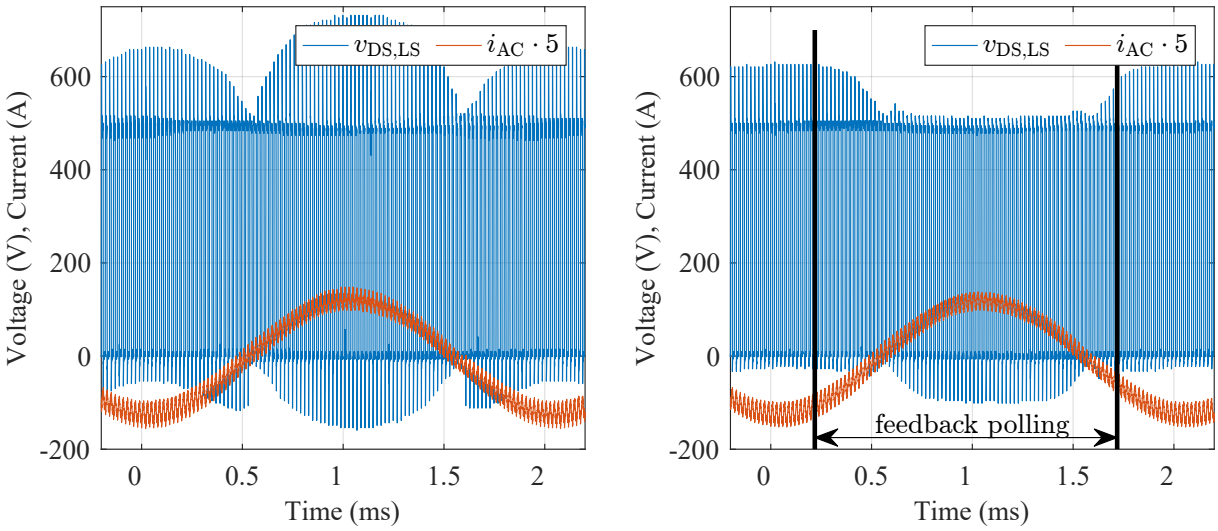
Measurement Results

To support the analysis of the control algorithm in this ac operating point, three types of measurements are used. Firstly, conventional time domain oscilloscope measurement of v_{DS} and i_{AC}. The second type is derived from the first. An analysis of each switching instance in the oscilloscope measurement is done and the voltage slopes are extracted. The third measurement is the feedback recorded by the driver itself. For each measurement, the standard operation and controlled operation are compared.

Figure 4.9 depicts the oscilloscope measurement for one phase. The periodic, sinusoidal load current is shown in orange. Its amplitude is scaled for better visibility on the same y-axis as the voltage measurement. As mentioned before, the high-side driver is in control of the switching characteristics during the time, the load current is positive. Therefore, the measurement results between 0.5 ms and 1.5 ms are of interest. Figure 4.9a and Fig. 4.9b exhibit major differences in the voltage overshoot in these areas. To investigate the differences in the voltage slopes, the second and third measurement type are presented and evaluated.

In Fig. 4.10, the y-axis contains the calculated voltage slope measured between 10 % and 90 % of v_{DC}. Each marker represents one switching slope and the colors indicate the control mode. The gray patches indicate the turn-on events for the respective switches. Because v_{DS} is measured across a low-side device and the analysis is done for the high-side driver, the turn-on and turn-off slopes are flipped. A turn-on event of the high-side driver causes a rising edge on v_{DS} and the opposite polarity occurs for a turn-off.

The two vertical black lines enclose the switching iterations for which the gate driver recorded the sensor readings internally. They also indicate the area of interest for this driver's control capabilities. In between iteration 20 and 65 the turn-on slope of the disabled mode exhibits a concave shape. The controller is able to counteract the influence of the sinusoidal load current and achieve a constant turn-on slope over time. However, at the beginning of the control period at iteration 18, a small overshoot is visible in the turn-on slopes. Here, the controller recognizes the start of the new control period, but the



(a) Control disabled.

(b) Control enabled.

Figure 4.9: Comparison of v_{DS} and load current measurements for disabled and enabled control.

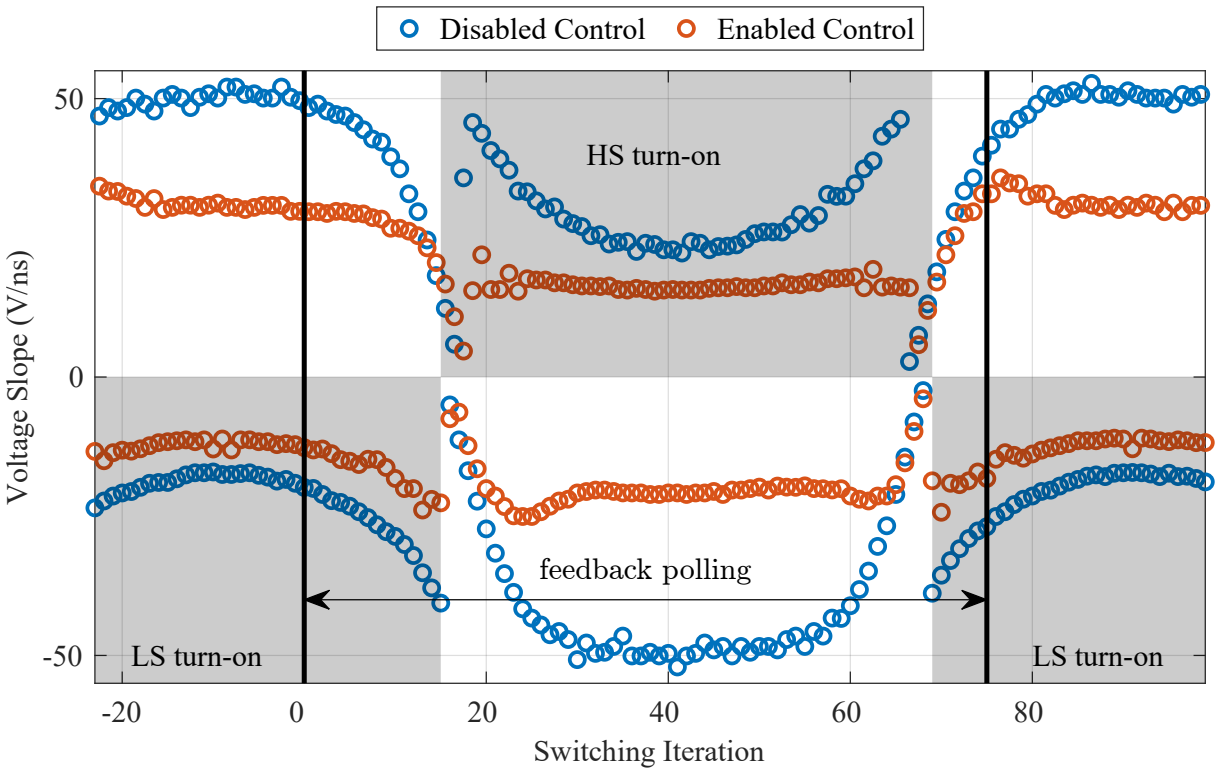
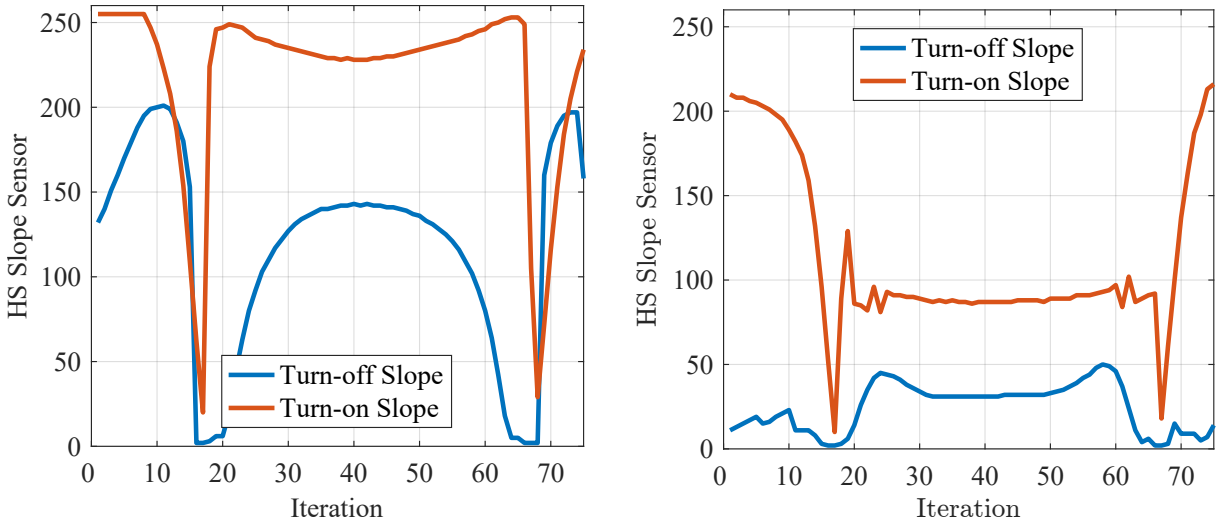


Figure 4.10: Calculated turn-on and turn-off slopes for disabled and enabled controller.



(a) Recorded feedback for the disabled controller.

(b) Recorded feedback for the enabled controller.

Figure 4.11: Comparison of feedback from the high-side driver during disabled and enabled control mode for turn-on and turn-off slopes.

very first switching instance is not under the same conditions as the last instance of the previous control period. Therefore, the control parameters have to be adapted to reach the set point again, which causes a slight overshoot in the voltage slopes. Due to the averaging nature of EME measurements, the minor portion of non-optimized switching events do not prevent an improvement of the converter emissions.

The turn-off slopes inside the white patches are very dependent on the load current. This dependency is visible in the sinusoidal shape of the calculated turn-off slopes between iteration 18 and 70. Adopting to this shape of disturbance is a challenge for the controller as is evident from the larger and wider negative overshoot in the turn-off slope measurements at iteration 23. The biggest drawback of the control algorithm is visible in this situation. However, implementing a true PI controller with direct impact on the control parameters would require a better vertical resolution in the possible adaption steps. This way, discretization errors could be avoided and the evaluation module simplified. Nevertheless, the controller is able to reach a constant value and keeps it until the load current forces the switching speeds to decrease below the desired speeds.

Figure 4.11 depicts the sensor reading of the high-side driver for the disabled and enabled operation mode. The relevant areas are again between iteration 17 and 67. For the disabled control measurement, the slope sensor samples values close to its maximum amplitude of 255. Additionally, the correlation between the shapes of oscilloscope and sensor measurements is as good as evaluated in Chapter 3. This is especially true for the overshoot on the turn-on slope at iteration 19 in Fig. 4.11b.

4.4 Summary

Recap

In this chapter, the control algorithm, which enables the closed-loop control of EME and switching losses, was presented. Firstly, an overview over the closed-loop control and the few publications in this field of research was given. The approaches differ in the time scope, feedback bandwidth, control goals and usage of external devices. Secondly, the communication setup between the test-bench PC and MCU and drivers has been introduced. Afterwards, the control parameters and variables are presented and their implementation in the control algorithm was proposed. Based on the settings provided to the controller, the evaluation of the PI values and adaption of the control parameters was explained. Finally, the controllers' performance was benchmarked in a dc and ac operating point.

Conclusion

The algorithm presented in this chapter is capable of achieving a closed-loop control of the switching characteristics of continuously running power electronic converters. In a dc example, multi-parameter enabled control settings allow a precise adjustment of the voltage slope to the set point chosen beforehand. The ac example proves the capability of this algorithm to control the voltage slopes in an application with sinusoidal disturbance introduced by an ac load current. Furthermore, by providing information about the internal variables and changes to the control parameters for up to 110 consecutive switching events, the control algorithm's performance can be evaluated. For the aforementioned examples, this feedback shows the successful control of the voltage slopes while the controller is active.

5 Evaluation of Control in Three-Phase Converter Operation

The final chapter evaluates the performance of the presented controller in selected operating conditions. After a detailed description of the testbench setup and measurement methods is given, measurement results at varying control settings, dc-link voltages and RMS load currents are presented. The variation of the control settings is based on two control modes. In the first mode, the controller is enabled and the set points of all drivers are changed by scaling them according to their maximum range. The second mode disables the controller and manually scaled control parameters are applied to emulate a non-adaptive operation gate driver. The evaluation of the control performance is based on the comparison of time and frequency domain measurements and by using the metric introduced in Section 2.4.2. Additionally, the variation in operating voltage and current is used to illustrate the controllers' resilience against changes of the outside operating conditions.

5.1 Testbench Setup

In general, the testbench is set up close to the regulations listed in international special committee on radio interference (CISPR) 25. This way, conducted emission measurements close to the standards can be achieved. The major differences to a regular testbench used for power electronic prototypes are the usage of LISNs, a reference ground plane and a measurement receiver. High-Voltage LISNs provides a defined impedance towards the power supply and a measuring point for high frequency (HF) disturbance voltages on the dc-link. The reference ground plane resembles the chassis or housing of a car and 50 mm spacing blocks are used to keep conductors and equipment at a constant distance from the ground plane. In addition to the standard time domain measurements of system voltages and currents, a measurement receiver records the disturbance voltage at the HF measurement port of the LISN.

The gate driver presented in Chapter 2 and the sensors introduced in Chapter 3 are combined on the modular PCB depicted in Fig. 5.1 and Fig. 5.2. Additionally, an FPGA is placed on each driver module. Six of these modules are placed in between a LV-PCB and a HV-PCB. Figure 5.3 shows the full converter without any outside connections. Towards the left and close to the MCU (yellow) is a USB interface used for the UART

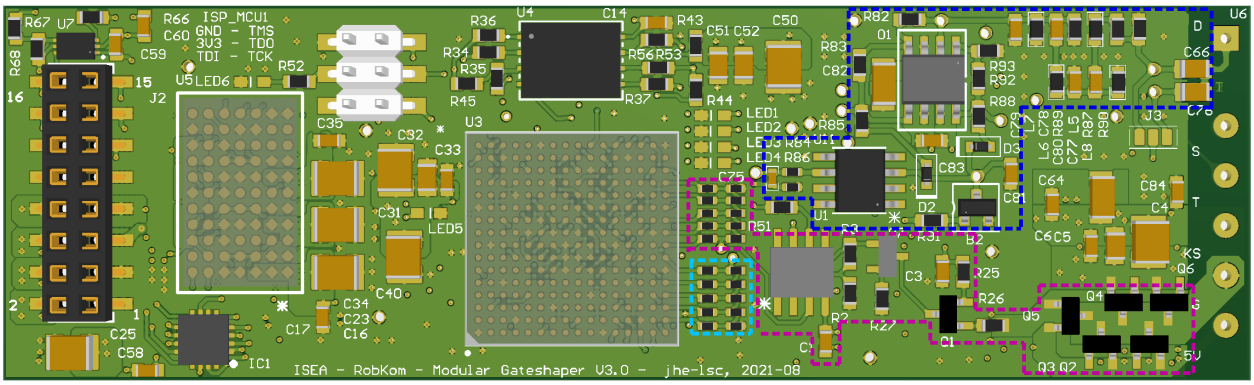


Figure 5.1: Top side of driver PCB containing the FPGA, resistor ladder (light blue), slope sensor (dark blue) and the turn-on driver (dark purple).

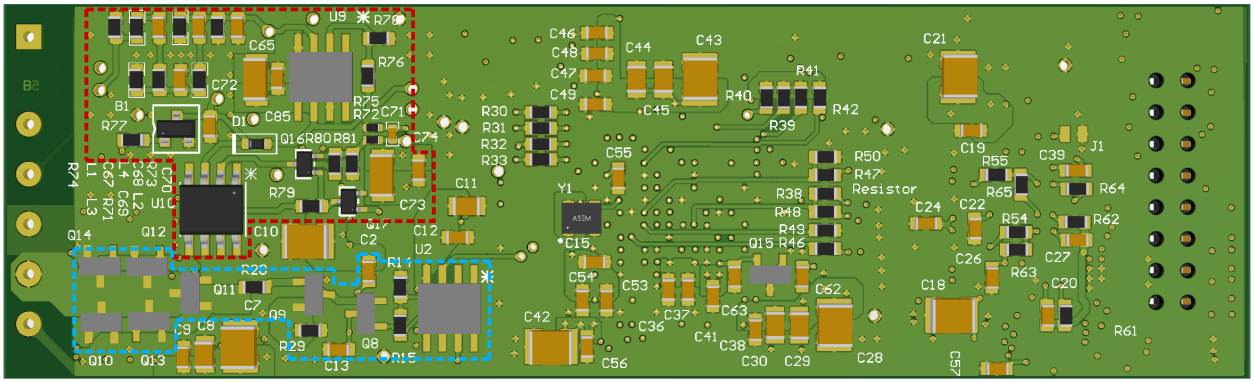


Figure 5.2: Bottom side of driver PCB with oscillation sensor (dark red) and turn-off driver (light blue).

communication and on the top left the first isolation stage of the power supply is located. Progressing to the right, six independent isolated dc-dc converters are implemented, which provide up to 6 W each and have a very low coupling capacitance of 1 pF. Therefore, the two stage power supply for the gate drivers minimizes the disturbances transmitted through the LV-PCB and the disturbance voltage measurements are not influenced by the parasitic behavior of the LV power supply.

The six gate driver modules are connected between the LV and HV-PCB. The HV-PCB encompasses three half-bridge switching cells. Each cell is equipped with a 0.8 µF ceramic local dc-link capacitance and the phase output is located closely to it. In addition to the local dc-link capacitance, 54 µF of foil capacitors are placed on the HV-PCB. The load itself is an artificial machine load (AML) which consists of three air coils that are connected in a star configuration.

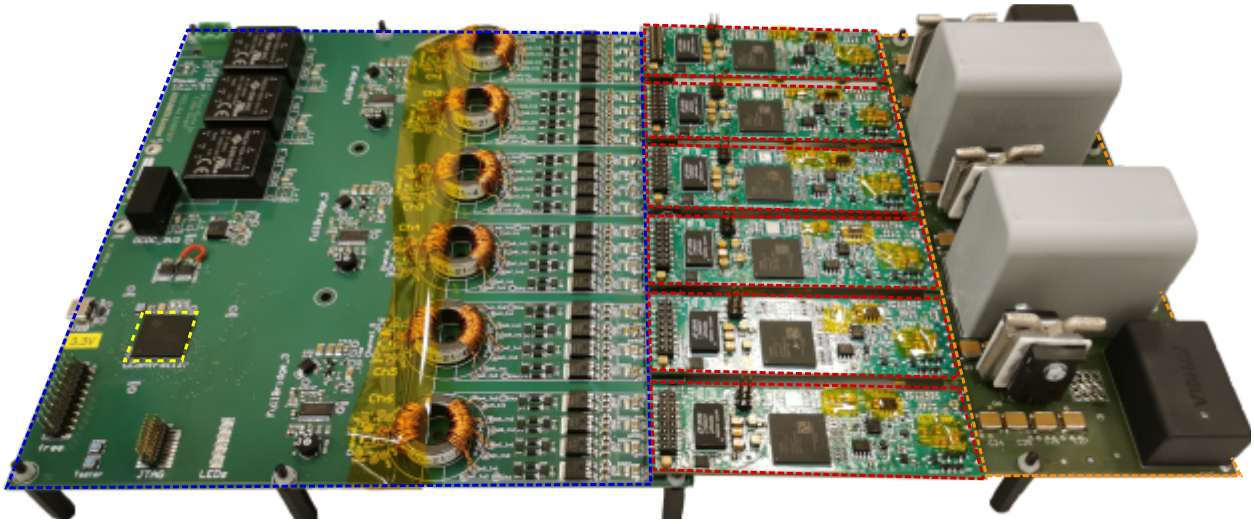


Figure 5.3: The complete converter consists of the low voltage PCB (dark blue) housing the MCU (yellow), the gate driver modules (red) and the high voltage PCB (orange).

Before presenting the measurement results, the measurement methods are introduced. Many aspects of the testbench and measurement devices have an impact on the measurement results. Therefore, all measurement devices and methods as well as the control settings are introduced in the following sections.

5.1.1 Time Domain Voltage and Current Measurement

A Lecroy Waverunner 9404 oscilloscope is used for capturing time domain measurements up to 64 MS at 20 $^{\mathrm{GS}}/_{\mathrm{s}}$ on all four channels. The high memory depth and sample rate is especially useful for measurements of full sine periods. In post processing, they can be used to extract rise and fall times as well as overshoot amplitudes for every switching instance in the recorded data.

The trigger signal is provided by an FPGA and its timing in relation to the phase of the sinusoidal output depends on the setting chosen by the user. A unique position in the sine period is determined by choosing whether the duty cycle should rise at a specific duty cycle. This way, specific points in the sine period can be targeted and repeatable measurements taken.

Differential HV probes manufactured by PMK with 400 MHz bandwidth are utilized to capture voltages in the range of ±50 V for v_{GS} and up to 1 kV for v_{DS}. Their high common mode rejection ratio (CMRR) and the wide range of attenuation settings make them viable for measurements in this environment.

Table 5.1: Scan table for measurements between 50 kHz and 200 MHz in three frequency ranges.

Parameter	Range 1	Range 2	Range 3
Start frequency	50 kHz	150 kHz	30 MHz
Stop frequency	150 kHz	30 MHz	200 MHz
Stepsize	400 Hz	4 kHz	40 kHz
Resolution BW	1 kHz	9 kHz	120 kHz
Measurement time	50 ms	5 ms	500 µs
Auto ranging	Off	Off	Off
RF attenuation	35 dB	45 dB	30 dB
Preamplifier	On	On	On
Auto preamp.	Off	Off	Off

For current measurements a HIOKI clamp-on probe with 30 ARMS rating and 0 Hz to 100 MHz bandwidth is used.

5.1.2 Frequency Domain Disturbance Voltage Measurement

A Rhode & Schwarz ESL3 spectrum analyzer and measurement receiver is utilized to record the disturbance voltage at the HF port of the LISN in the DC+ path. It is protected by a pulse limiter, which cuts off voltages above 100 dBµV. Additionally, the pulse limiter encompasses an attenuation of 10 dB between 0 Hz and 200 MHz. Cutting off amplitudes above 100 dBµV will lead to distorted measurements. Therefore, additional 10 W 6 dB and 5 W 20 dB attenuators are connected at the outputs of the LISNs. The total external attenuation adds up to 36 dB and is considered in the post processing of the frequency domain measurements.

Besides the external setup of the measurement receiver, the internal settings play a major role in properly recording the disturbance voltages over a wide frequency range. Here, the properties of a measurement receiver are of advantage. By defining a scan table, the device is able to adapt its filter bandwidth and measurement settings depending on the frequency it is sampling. This way, narrow filters are applied in the low frequency (LF) region and they widen in the HF range. Table 5.1 contains the scan table, which is used for the measurements in this chapter. In all ranges the detector is set to peak detection which results in the highest amplitude and quickest measurements.

The precision achieved by the ESL3 is given to be below 0.5 dB for the frequency range between 10 MHz and 3 GHz. At 65.83 MHz the absolute uncertainty is listed to be below 0.3 dB [45].

5.1.3 Loss Measurement

In order to evaluate the EME performance, the metric introduced in Chapter 2 is plotted over the losses. Because the switching cells of the prototype do not include a means of measuring the drain current, no direct switching loss calculation is possible. However, if the overall power into the converter is measured and the ac load current is known, the switching losses can be extracted from the system losses. The system losses are acquired using a Keysight power analyzer PA2201A, which is connected directly after the TopCon HV source and an additional filter is placed between the power analyzer and the LISN. This way, the influence of the power analyzer on the frequency domain measurement is minimized. The accuracy of the power measurement using the PA2201A is given with 0.1 % [46].

The separation of the switching losses from the system losses can be done by calculating the conduction losses and subtracting them from the system losses. Conduction losses in the semiconductor devices are dependent on the $R_{\mathrm{DS,on}}$, which again is dependent on the junction temperature and the drain current. Both, the temperature, estimated from simulations, and current in the following operating points are in a range, in which the $R_{\mathrm{DS,on}}$ is very close to its nominal 21 mΩ [41]. For the resistance of the ac load, an impedance measurement of the air coils has been done. Because the coils are not wound from litz-wire, the resistance changes with the frequency due to the skin effect. Therefore, the resistance is measured at multiple frequencies between 0 Hz and 100 kHz. From these measurements, a function for the frequency dependent resistance is fitted and evaluated at the frequency components calculated in an FFT of the load current. The sum of the power calculated at each frequency component represents the total conduction losses in the load, as is described in (5.1).

$$P_{\mathrm{load,cond}} = \sum_{f} \left(i_{\mathrm{load}}\left(f\right)^2 \cdot r_{\mathrm{load}}\left(f\right) \right) \tag{5.1}$$

Finally, the switching losses can be extracted from the system losses by subtracting the conduction losses of the load and the semiconductor devices from the system losses, as is indicated by (5.2). The switching losses calculated with this procedure, are the losses of all six SiC MOSFETs. Because all controllers are using similar control settings and set points, the losses are not calculated for single switches.

$$P_{\mathrm{SiC,switch}} = P_{\mathrm{loss,system}} - P_{\mathrm{load,cond}} - P_{\mathrm{SiC,cond}} \tag{5.2}$$

Table 5.2: Profile set used for the parameters of the turn-on controller.

# State	S_1			S_2			S_3			S_4		
Parameter	on	off	dur	on	off	dur	on	off	dur	on	off	dur
Max.	10	0	17	**31**	0	3	5	0	131	31	0	31
Std.	10	0	17	**31**	0	3	5	0	131	31	0	31
Min.	10	0	17	**10**	0	3	5	0	131	31	0	31

Table 5.3: Control variables for turn-on controller.

# Variable	Type	Position in Profile	Direction	Enable/Disable
1	amp. on	1	1	Enable
2	-	-	-	Disable
3	-	-	-	Disable

5.1.4 Control Settings

As introduced in Chapter 4, the behavior of the control algorithm is defined by its parameters and variables. The settings used by the controllers for the following measurements are introduced in this section. Because the combinations of driver, semiconductor device and sensor are not equal for all six MOSFETs, the control settings are customized for each driver. However, very similar gate profiles and corresponding control variables are used. Therefore, it is sufficient to introduce the settings of one driver. The low-side driver of phase 2 is chosen.

Table 5.2 and 5.4 contain the profile sets provided to the controller. The control parameter is printed bold and chosen to be $a_{2,\mathrm{on}}$ for the turn-on controller and $a_{3,\mathrm{on}}$ for the turn-off controller. The variables defining the controller behavior are given in tables 5.3 and 5.5. They indicate the chosen control parameter and how the control algorithm adapts it.

The first pulse in each profile charges or discharges the gate close to a point where the next state actively controls the switching behavior. For the turn-on controller this results in a slow, but wide pulse with an amplitude of 10 and a duration of 42.5 ns. The following state allows a variation of the turn-on amplitude between 10 and 31 for a short pulse of 7.5 ns. This combination followed by a long pause results in a good controllability over a wide range of voltage slopes.

For the control of the turn-on events, the feedback of the slope sensor is used. It provides a good utilization of the dynamic range of the sensor and is in good agreement with the real switching behavior. The feedback for the turn-off control loop is chosen to be the oscillation sensor. As shown in Fig. 4.9a, the overshoot and oscillation amplitude is

strongly dependent on the current amplitude for turn-off events. Therefore, the oscillation sensor is a valid choice.

In contrast to the turn-on controller, the turn-off controller discharges the gate past the threshold voltage and slows down the turn-off process after the load current commutation is started. To achieve this, the driver discharges the gate at a fast rate for 32.5 ns and then charges it at varying currents for 30 ns. Therefore, the control parameter is chosen to be the turn-on amplitude of state S_3.

Table 5.4: Profile set used for the parameters of the turn-off controller.

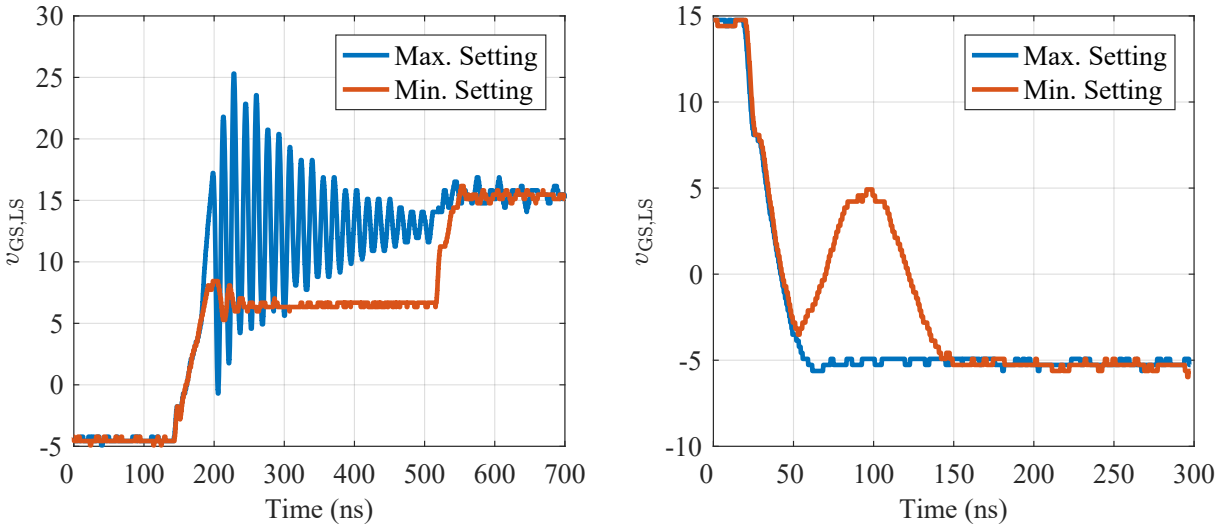
# State	S_1			S_2			S_3			S_4			S_5			S_6		
Parameter	on	off	dur	on	off	dur	on	off	dur	on	off	dur	on	off	dur	on	off	dur
Max.	0	29	13	0	0	1	**31**	0	12	0	5	30	0	10	11	0	31	31
Std.	0	29	13	0	0	1	**11**	0	12	0	5	30	0	10	11	0	31	31
Min.	0	29	13	0	0	1	**11**	0	12	0	5	30	0	10	11	0	31	31

Figure 5.4a and Fig. 5.4b depict the gate-source voltages for turn-on and turn-off instances respectively. In both figures, the maximum and minimum setting are shown. The maximum settings in Fig. 5.4a exhibit high oscillations. These oscillations are caused by the non-ideal measurement setup and do not represent the voltage across the gate-source capacitance C_{GS}. The parasitics introduced by the HV probe and the parasitics of the gate loop are excited by the switching transition. Therefore, the peak voltages in this measurement are not present across C_{GS}, but they include the aforementioned parasitics.

The general converter operating point is chosen to 400 V, the switching frequency is set to 50 kHz and the fundamental sinusoidal frequency is 700 Hz. With a modulation index of 12 %, an RMS load current of 17 A is reached.

Table 5.5: Control variables for turn-on controller.

# Variable	Type	Position in Profile	Direction	Enable/Disable
1	amp. on	3	0	Enable
2	-	-	-	Disable
3	-	-	-	Disable



(a) Turn-on v_{GS} of the low-side switch in phase 2.

(b) Turn-off v_{GS} of the low-side switch in phase 2.

Figure 5.4: Gate Profile settings for maximum and minimum switching speeds chosen for the control in this chapter.

5.2 Analysis and Discussion of Control Performance

With the presented testbench, the control performance is analyzed by varying different operating conditions. The following sections contain the measurement results for variations in the control modes, the dc-link voltage and load current as well as a discussion of the control performance for each operating point.

5.2.1 Variation of Set Points

The first analysis is done based on the measurement results of experiments under varying set points. By changing the set points for all drivers, the global level of emissions is adapted while the controller dynamically adjusts the gate profiles based on the feedback provided by the sensors. Alternatively, the controller is disabled and the gate profiles are set to scaled variations within the range given in the profile sets. Therefore, the control settings ate noted as % and the slowest switching events occur for a controller setting of 0 % in both modes. For both operating modes, time and frequency domain measurements are recorded and used for a comparison of the metric for the emissions and losses at the respective controller setting. In the next sections, first the time, then the frequency domain measurements and finally, the recorded feedback are presented. Afterwards, the manually scaled gate profiles are applied and a similar evaluation is done. Additionally, the behavior of both modes in the frequency domain is compared. Subsequently, an evaluation of the emission representation and switching losses is done and discussed.

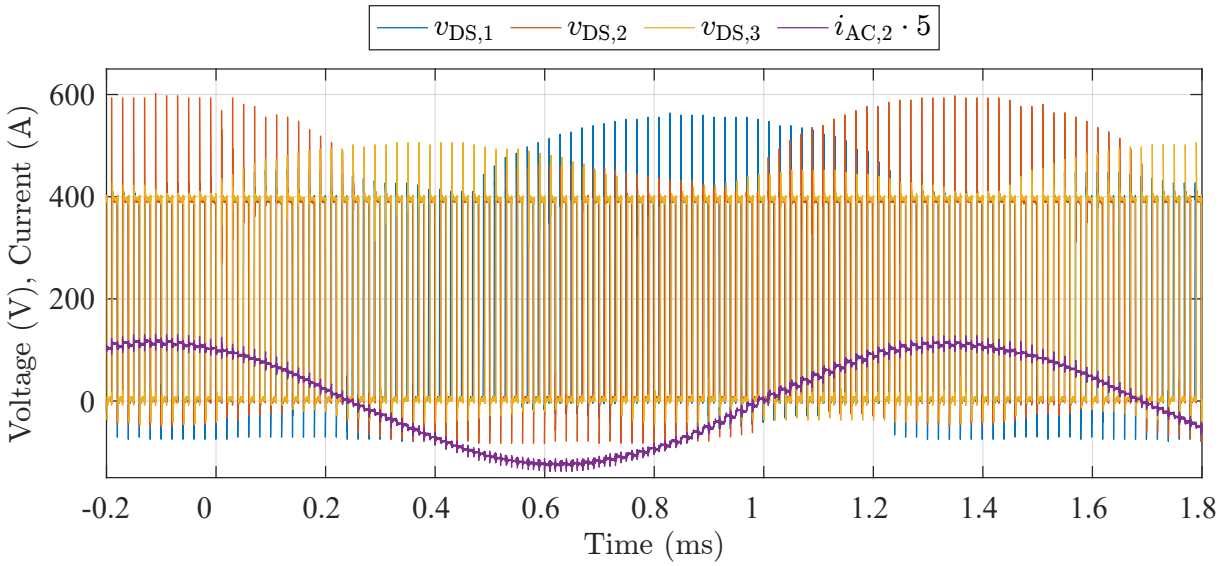


Figure 5.5: Time domain measurement of v_{DS} for all three phases and load current of second phase. The control is set to a 100 % and maximum switching speed and emissions are present.

Time Domain Measurement

The time domain measurements are started by recording v_{DS} across the low side devices and the load current of the second phase. Figure 5.5 contains the respective measurements with controllers set to 100 %. Disabling the controller forces it to apply the default gate profiles, which are the ones causing the highest emission and lowest losses.

Similar to the ac example in Section 4.3.2 the changes in the overshoots are following the sinusoidal shape of the current. However, a substantial difference in the maximum overshoot amplitude between the phases is visible. This difference is caused by variations of the parasitics of the semiconductor devices. For phase 2 the overshoot is reduced from 200 V to 10 V. Because the controller can accommodate differences in the switching behavior and each driver receives a custom profile set, no further attention is paid to the asymmetries between the phases in this chapter.

Figure 5.6 depicts the phase voltages and load current while the controller is active. The set point is chosen to the lowest value in the ranges of each driver and the drastic reduction in the overshoots is visible from the time domain measurement. Between Fig. 5.5 and Fig. 5.6 it is notable that all drivers successfully control the switching behavior in a way that decreases the overshoots to a minimum.

To analyze the switching behavior in regards to the voltage slopes, a similar analysis to Section 4.3.2 is performed. The voltage slope of every switching instance in phase 2 is analyzed and the resulting slopes are plotted in Fig. 5.7. Furthermore, the color of the

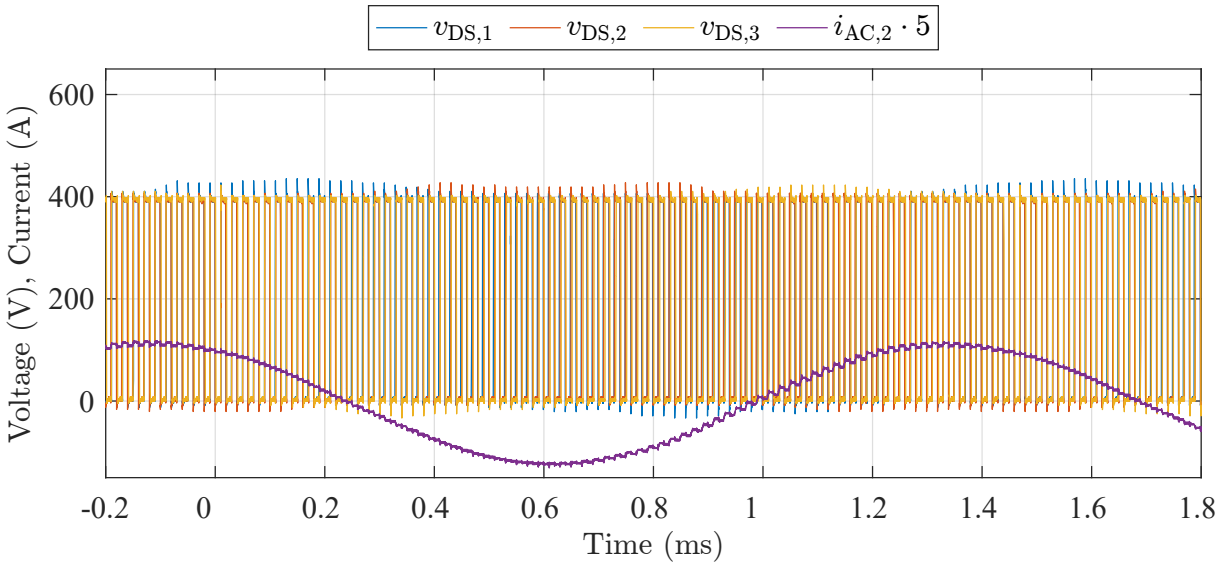


Figure 5.6: Time domain measurement of v_{DS} for all three phases and load current of second phase. The controller is targeting the lowest possible set-point.

markers change according to the set points of the controller. Light red markers represent the switching events for the slowest setting of the controller, which corresponds to the measurements in Fig. 5.6. Each step towards light blue indicates an increase of 10 % of the range of possible set points. Finally, the light blue markers correspond to the measurement depicted in Fig. 5.5.

The gray patches indicate the turn-on events. While the lower patches correspond to the low-side driver, the upper patches indicate switching events driven by the high-side driver. The white patches contain the turn-off events in the opposite manner.

The changes in the voltage slopes between the different set points indicate some discretization effects. They occur in the scaling of the set points for the turn-on controller of the high-side driver, where some slope values are not reached for rising edges between iteration 60 and 95. Furthermore, differences in the performance of the turn-on and turn-off controllers are visible. The turn-off controllers have a limited impact on the voltage slopes, as is visible from the respective white areas in Fig. 5.7. The reason for this has been given in Section 4.3.2. However, the effect is more severe in this operating point with the presented control settings.

The turn-on control performance is significantly better than the turn-off. However, the low-side driver's distribution of voltage slopes over the achievable range is more even compared to the high-side driver. Overall, a considerable change in the voltage slopes is evident and the changes scale with the variation in the set points. In parallel to the time domain measurement, the aforementioned measurement receiver was used to record the disturbance voltage and plot it over the frequency spectrum.

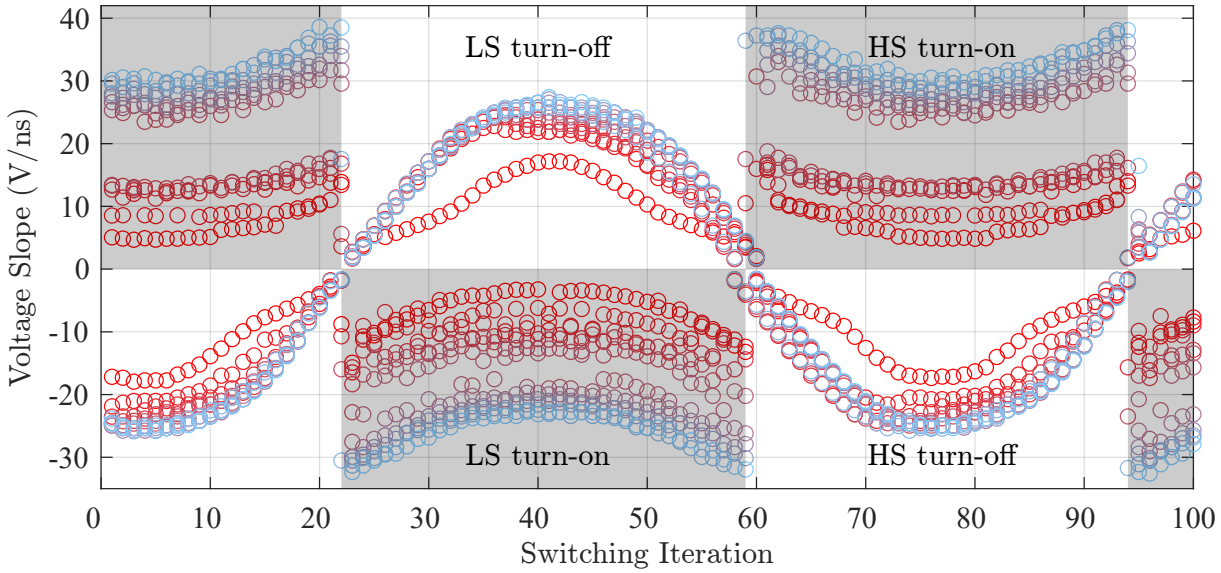


Figure 5.7: Voltage slopes calculated from time domain measurement in phase 2, for active control with varying set points.

Frequency Domain Measurement

Figure 5.8 contains the data recorded by the measurement receiver. The colors correspond to the same settings as in Fig. 5.7 and are labeled according to their relative set point. In the frequency range from 50 kHz to 200 MHz many characteristic areas can be identified. To increase the visibility of the effects a moving average of ten elements was applied to the emissions measurement.

Firstly, the boundaries between the measurement ranges can be identified by the characteristic sharp cuts in the amplitude. At 150 kHz and 30 MHz a change in the resolution bandwidth inside the measurement receiver causes changes in the amplitude of the noise floor and the horizontal resolution. The resolution bandwidth of 9 kHz allows a good representation of the switching frequency and the first few repetitions and multiples of it. However, after changing the resolution bandwidth, according to the scan Table 5.1, to 120 kHz, multiples of the switching frequency are barely detectable.

The frequency components at multiples of the switching frequency have been introduced in Section 2.4. However, a measurement of the disturbance voltage v_{dist} on the dc-link is impacted by many more factors than just the switching slopes and overshoot or oscillation amplitudes. The emission behavior in the lower frequency region up to 15 MHz is heavily influenced by the characteristics of the LISN, the dc-link capacitors and the load connected to the converter [47]. Here, adaptions to the gate drivers have no impact on the disturbance voltage as explained in Section 2.4. Therefore, the lower frequency region is of less interest and the following analyses of the measurements in the frequency domain

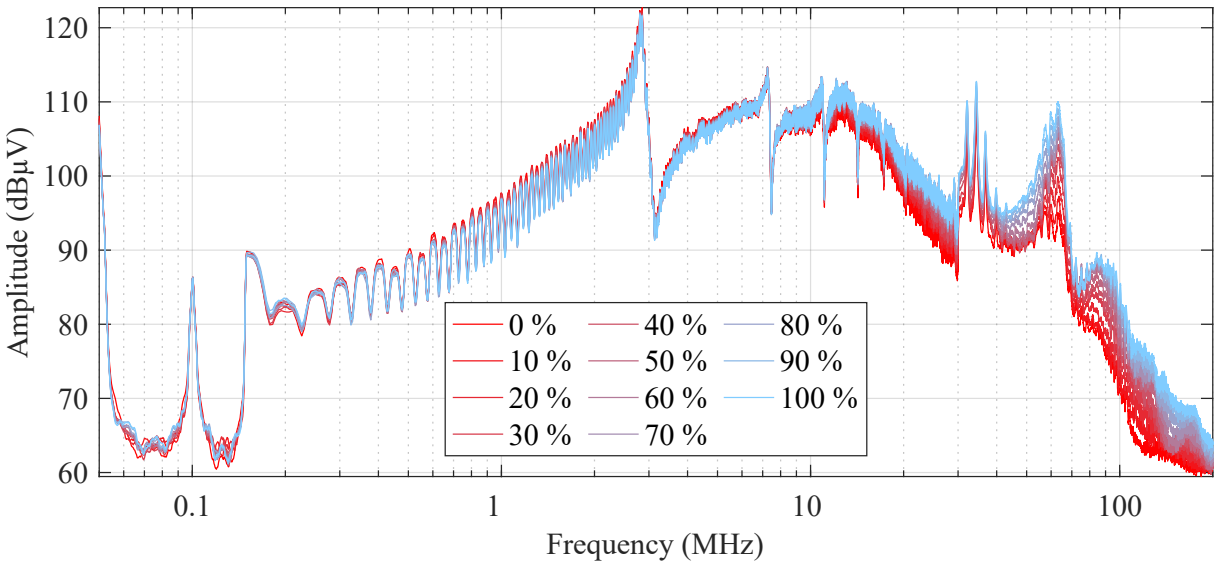


Figure 5.8: Disturbance voltage frequency domain measurement with a moving mean filter with a width of 10 elements. The changes between the measurements are achieved by changing the set points according to Section 5.2.1. The gate voltages applied for the 0 % and 100 % settings are depicted in Figure 5.4.

will focus on the spectral components above 10 MHz. Figure 5.9 depicts the disturbance voltages in the aforementioned frequency range.

In this region, the effects of the changing gate control parameters are visible. Starting at 10 MHz, a broadband decrease of the disturbance amplitude is visible. At lower frequencies, the reduction in the disturbance is only a few dB. The decrement increases to up to 10 dB at 90 MHz. This effect is caused by the decrease in voltage slope according to the set points' progressing from one measurement to the next. An additional attenuation of the disturbance amplitude is visible at 63 MHz. Here, the resonance frequency of the switching cells is dominant. Therefore, the narrowband emission is caused by the oscillation and overshoot following the switching events. The disturbance voltage decreases by up to 16 dB at the resonance frequency. In between the variations of the set points, the disturbance amplitude is spread out almost linearly. The exact relation between disturbance amplitude and set point will be discussed in Section 5.2.1.

Turn-on Slope Feedback

In addition to the measurements in the frequency and time domain, the drivers themselves record the sensor outputs for each switching event. As explained before, these measurements are the input for the internal PI controller inside the FPGA. The relevant sensor readings for the control settings used in this chapter are the turn-on slope and the turn-off oscillation. Figure 5.10 depicts the readings corresponding to the slope sensors

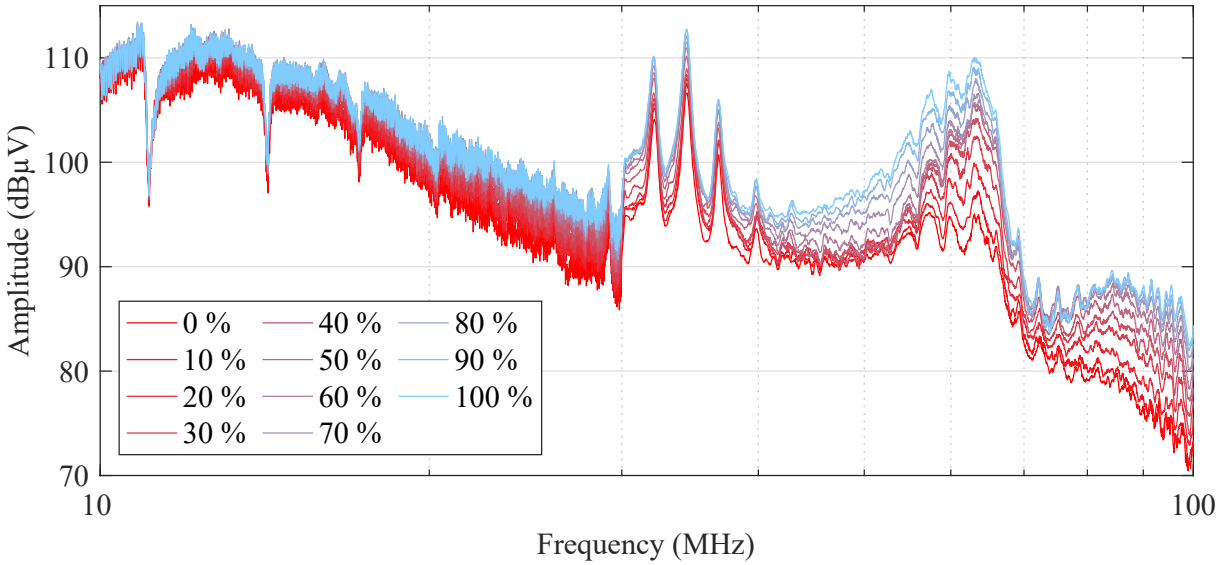
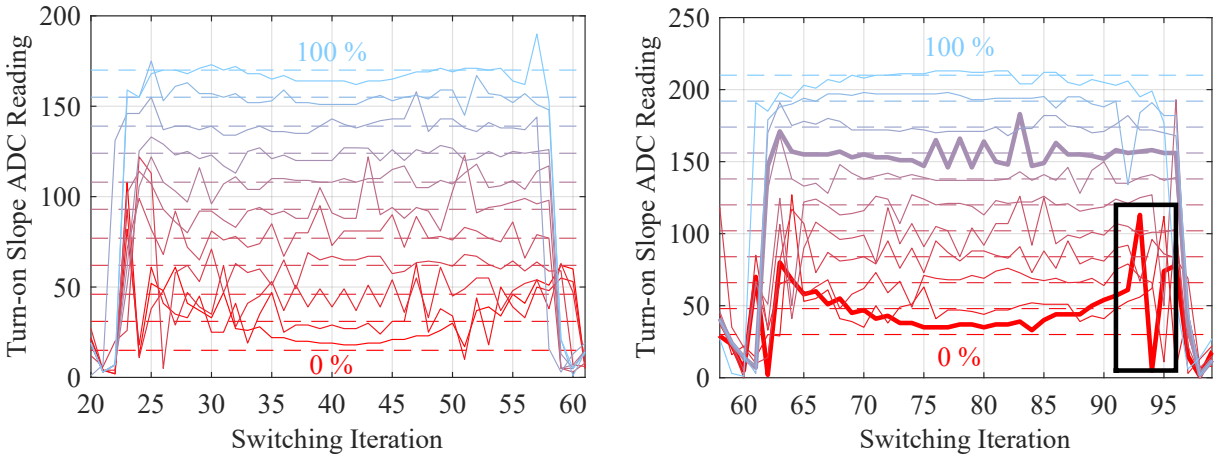


Figure 5.9: Disturbance voltage frequency domain measurement with a moving mean filter with a width of 10 elements. Zoomed into the relevant parts, for active control with varying set points. The changes between the measurements are achieved by changing the set points according to Section 5.2.1. The gate voltages applied for the 0 % and 100 % settings are depicted in Figure 5.4.

and Fig. 5.11 the feedback from the oscillation sensors. The figures depict the high- and low-side drivers' sensor readings separately because they are responsible for the switching behavior in different phases of the sine period.

The dashed horizontal lines represent the scaled set points for the drivers used during each variation. A good agreement between the sensor readings and the set points is visible for the turn-on slopes of the low-side driver. The upper thick line in Fig. 5.10b highlights oscillations of small amplitude between iteration 75 and 85 at a level of 150 points, which are caused by the aforementioned discretization and minor instability in the controller. Oscillations of higher amplitudes that include sensor readings, which are unlikely for the operating point, are visible in the black box at iteration 93 on the lowest variation, plotted as thicker line. They are the result of communication errors between the corresponding FPGA and the MCU. In post processing, some of the communication errors are corrected by inserting measurement values which are deducted from the surrounding shape of the measurement. An exemplary comparison between the corrected ADC reading and the original is depicted in Fig. A.10.

In contrast to Fig. 5.7, the gap in the voltage slopes is not visible in Fig. 5.10b. The original measurements of $v_{\mathrm{DS},2}$ are plotted in Fig. A.9 and depict the reason for the non-linear distribution of the calculated slopes with regard to the control settings. With increasing switching speed, the start of the oscillation causes a step in the voltage transition, which causes the observed artifact in the slope calculation between 10 % and 90 % of V_{DC}. This is caused by the changing damping ratio of the switching cell. During the turn-on process



(a) Turn-on slope feedback of low-side driver connected to phase 2.

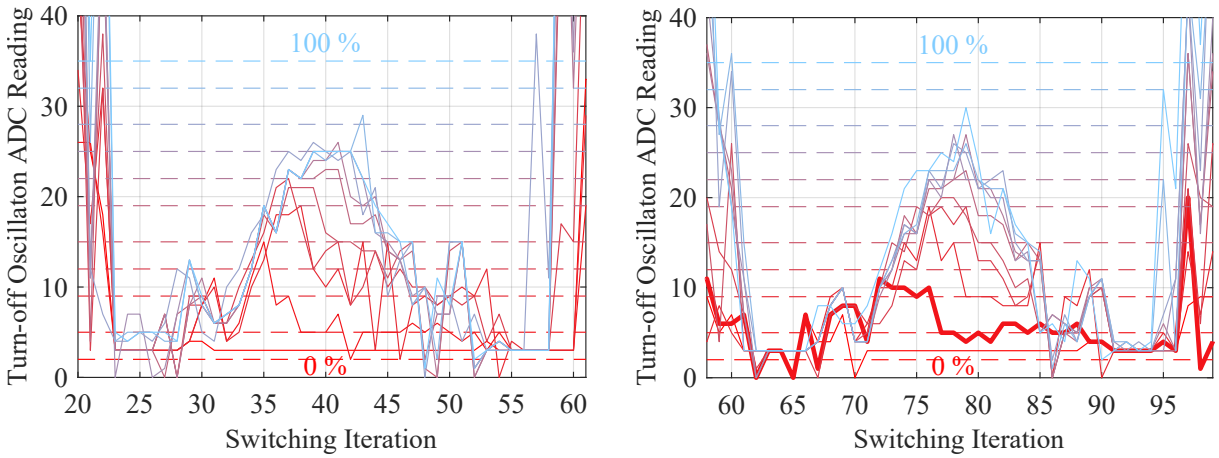
(b) Turn-on slope feedback of high-side driver connected to phase 2.

Figure 5.10: Comparison of turn-on slope feedback from low- and high-side drivers for different set points. The color coding is in accordance with the frequency domain measurements in Fig. 5.9.

the $R_{\mathrm{DS,on}}$ depends on the gate-source voltage v_{GS}. Since the changing gate profiles change the timing of the actual v_{DS} voltage commutation in relation to v_{GS}, each profile results in a differently damped system.

Turn-off Oscillation Feedback

For the feedback of the turn-off events, the oscillation sensor is evaluated because its output is used as input for the turn-off control. In Fig. 5.11, the dashed lines mark the set point for the corresponding variation again. The highest value in this case has been chosen to be above the peak oscillation sensed during operation at the fastest switching speed. Therefore, the sensor reading does not reach the targeted set point for the blue variations. In a similar manner, the lowest setting - 0 % - is below the lowest sensor reading. This leads to an effectively disabled controller for the extreme variations of the controller settings, because the controller clips to either the maximum or the minimum value of the parameter range provided by the control parameters. As explained in Section 4.3.2 the turn-off control shows a greater and wider overshoot before the set point is reached. The measurement at 10 % - marked with a thicker line - exhibits this behavior. Overall, the resulting shape of the sensor readings shows a shift of their peak to the left and a plateau on the level of the set point for the lower variations.



(a) Turn-off oscillation feedback of low-side driver connected to phase 2.

(b) Turn-off oscillation feedback of high-side driver connected to phase 2.

Figure 5.11: Comparison of turn-off oscillation feedback from low- and high-side drivers for the variations in the set points. The color coding is in accordance with the frequency domain measurements in Fig. 5.9.

Constant Scaled Profiles

Instead of letting the controller adapt the gate profiles, the variations between the next measurements are done manually in the control parameters. For each driver the control parameter was scaled in 10 % increments according to its maximum range in between measurements. This results in a behavior, which is similar to a non-adaptive gate driver. Figure 5.12 contains the voltage slopes calculated from each time domain measurement taken in between variations. In comparison to Fig. 5.7, the turn-off slopes in the white areas are spread out more, especially towards the beginning of each half wave. The turn-on slopes - in the gray areas - show a similar distribution to the measurements with the controller enabled. However, in the lower range the active controller allows a more gradual change in between measurements.

This is also reflected in the frequency domain measurements. Figure 5.13 depicts the frequency range between 10 MHz and 100 MHz again and overall similar changes between the minimum and maximum setting are visible. However, the vertical distribution of measurements is not as good as with the active controller. This indicates a non-linear dependency of the emission level on the control parameter that the active control is able to compensate.

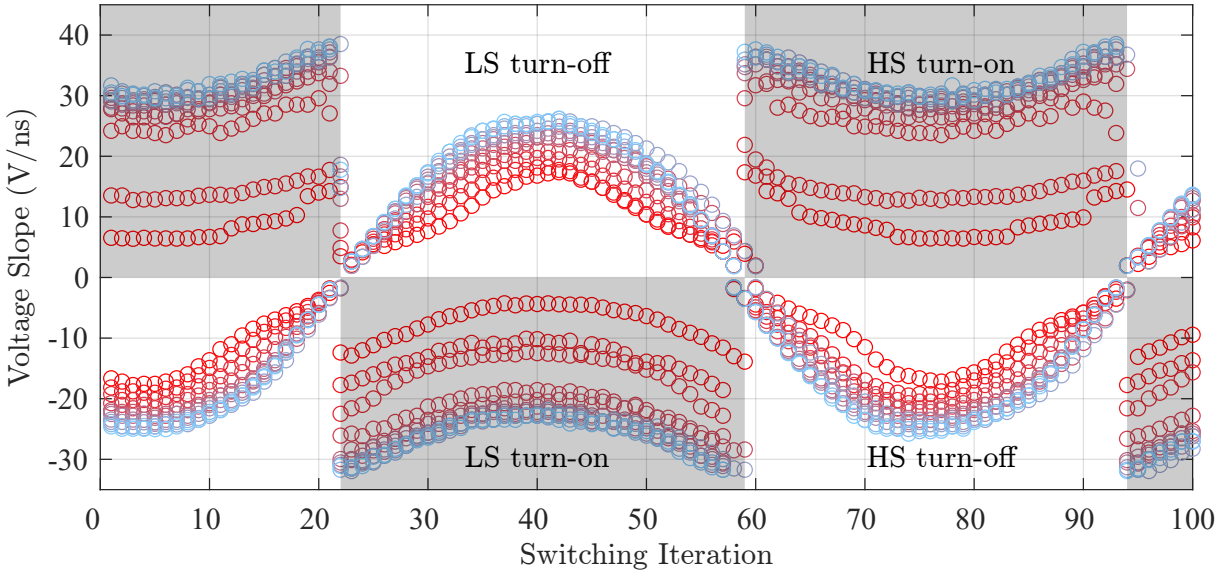


Figure 5.12: Voltage slopes calculated from time domain measurement in phase 2 while constant gate profiles are applied.

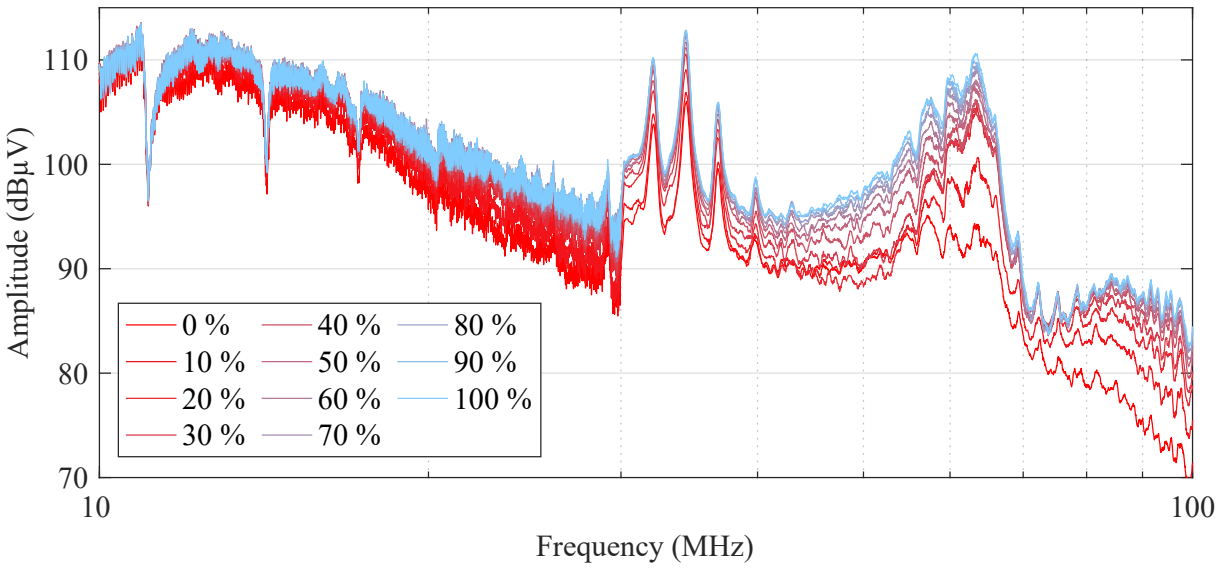


Figure 5.13: Disturbance voltage frequency domain measurement with a moving mean filter with a width of 10 elements. Zoomed into the relevant parts, for active control with manually scaled control parameters.

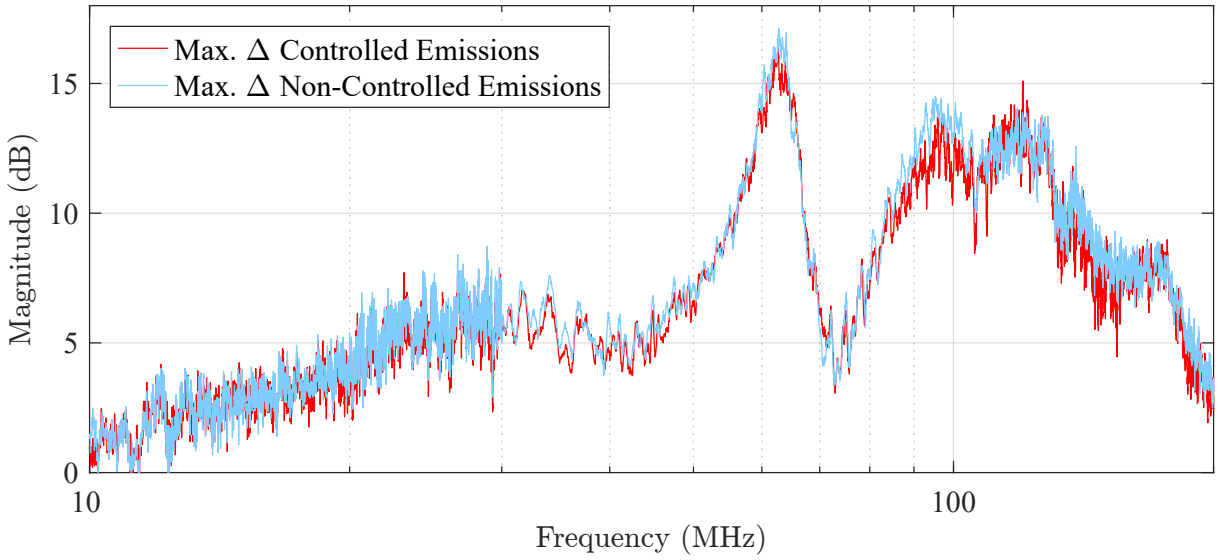


Figure 5.14: Differences in disturbance voltage measurements between high and low set points at 400 V to 600 V in enabled control mode.

Analysis of Differences in Disturbance Voltage Spectra

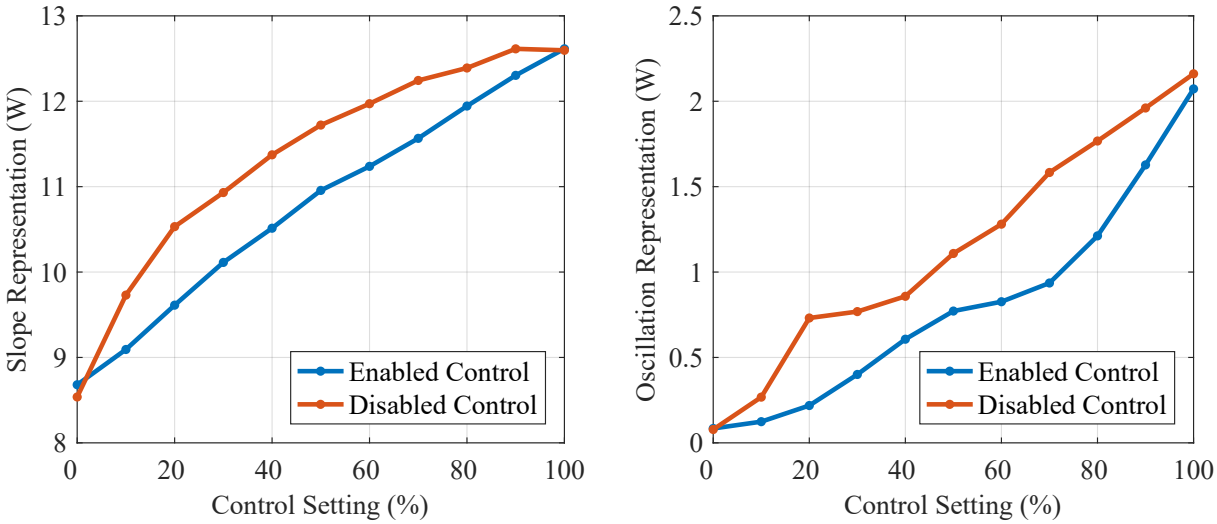
After the measurements methods are presented in the previous sections, the analysis of the operating behavior and control performance can be done. The non-adaptive mode is used as a reference to compare the controllers performance to. In a first step, this is done for the frequency spectrum.

Figure 5.14 contains the difference between the two extreme settings, 0 % and 100 %, of each control mode. It is visible, that both operation modes result in a very similar change between their extreme settings. This is due to the saturated behavior of the active controller when extreme set points are chosen.

Up to 10 MHz the differences are very small and only rise towards higher frequencies. The best improvements over the fastest set point are at the resonance frequency of the switching cell. At 63 MHz, the difference between the minimum and maximum settings are 17 dB and 16 dB for the controlled and non-controlled mode, respectively. Additionally, between 50 MHz and 125 MHz the spectral components have been decreased by 10 dB over a wide frequency range.

Evaluation of the Control Performance in Disabled Mode

The evaluation of the control performance is done by calculating the emission representation for the voltage slopes and the narrowband oscillation according to (2.4). Figure 5.15 contains the emission representations for both frequency ranges and control modes. The



(a) Slope representation calculated from frequency domain measurements between 1 MHz and 60 MHz.

(b) Oscillation representation calculated from frequency domain measurements between 60 MHz and 90 MHz.

Figure 5.15: Comparison of Emission representations over their respective control target setting for the enabled control mode.

slope representations, which are calculated from the spectral components between 1 MHz and 60 MHz are depicted in Fig. 5.15a. For the enabled control, a linear relation between the scaled control parameter and the slope representation is noticeable. The disabled control mode shows a moderate saturation effect towards the higher values of the scaled gate profile settings.

Figure 5.15b illustrates the opposite behavior. The oscillation representation of the disabled control mode is linear for all variations except the measurement at 20 % control setting. However, the goal for the controller in this chapter is to influence the overall emission behavior. Therefore, the behavior of the slope representation in the enabled control mode is more relevant, which is reflected in the higher absolute level of the slope representation.

The second important metric for the evaluation of the control performance is the losses added when decreasing the EME. When decreasing EME, the additional losses are the second important metric for the evaluation of the control performance. As described in Section 5.1.3, the system losses are only recorded at the dc-link connection. They are depicted in Fig. 5.16 for the two control modes and all variations. It is visible, that the system losses for both control modes are close and the enabled mode causes slightly more overall losses between 10 % and 80 %. However, with the knowledge about the load currents, the conduction losses of the load and the semiconductor devices can be extracted.

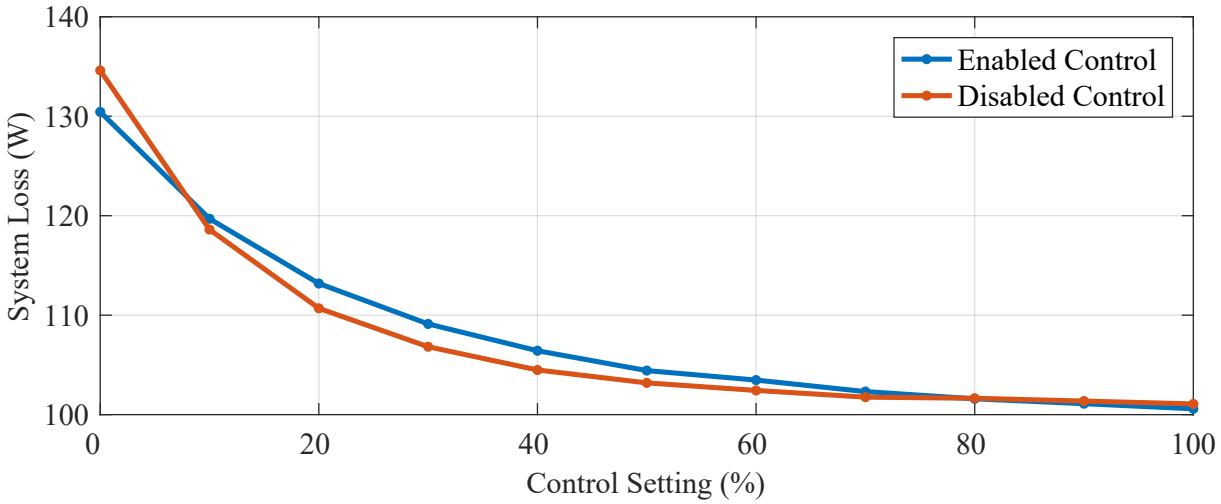


Figure 5.16: Comparison of overall System losses at 400 V and 17 A RMS.

This separation is carried out in Fig. 5.17. Here the dashed lines represent the disabled control mode. The conduction losses in the load and semiconductor devices are at constant levels, which show minor changes due to slightly different current amplitudes for each variation. Overall, the loss distribution is in good agreement between the enabled and disabled control modes. The major changes in the system loss are clearly caused by the changes in the switching losses. Furthermore, similar to the previous figure, the switching losses in the 0 % setting are noticeably higher for the disabled mode. This is due to the advantage of allowing faster gate profiles in the low-current areas for the turn-off events. Here, the controller allows the gate profile to be faster because the feedback from the sensors is still low.

After extracting the switching losses from the system losses, they can be used to evaluate the compromise between EME and converter efficiency. In Fig. 5.18 the emission representations for the slope and oscillation frequency regions are plotted over their respective switching losses. This way of presenting the data allows an evaluation of losses at the same emission levels. For both frequency regions, the measurements with the enabled controller have lower losses, because the corresponding line is further left for all variations. Similarly, in Fig. 5.18b the oscillation representation of the measurements with active control are to the left of the disabled mode.

Figure 5.19 depicts the emission representation for the frequency range from 1 MHz to 200 MHz. Therefore, the changes in the slope and the oscillation are both contained in this metric. The overall shape of the data is similar to the previous figures and a clear improvement of the compromise between system efficiency and EME is visible for the enabled controller.

The best improvement can be achieved at moderate emissions and loss levels. An exemplary point is chosen for the controlled emissions and the improvements for either the emissions or the losses can be extracted. At the same amount of switching losses, the

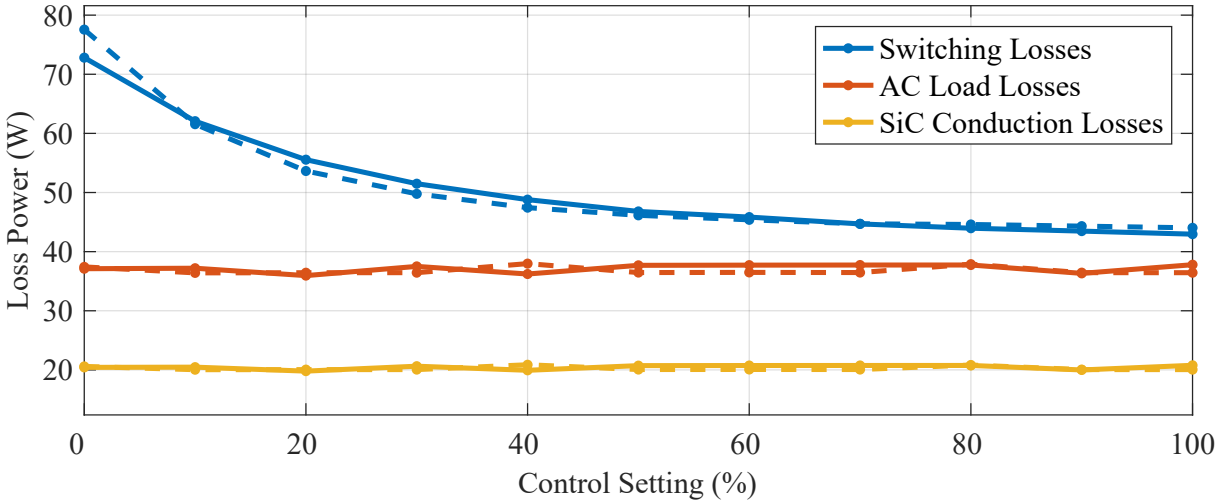
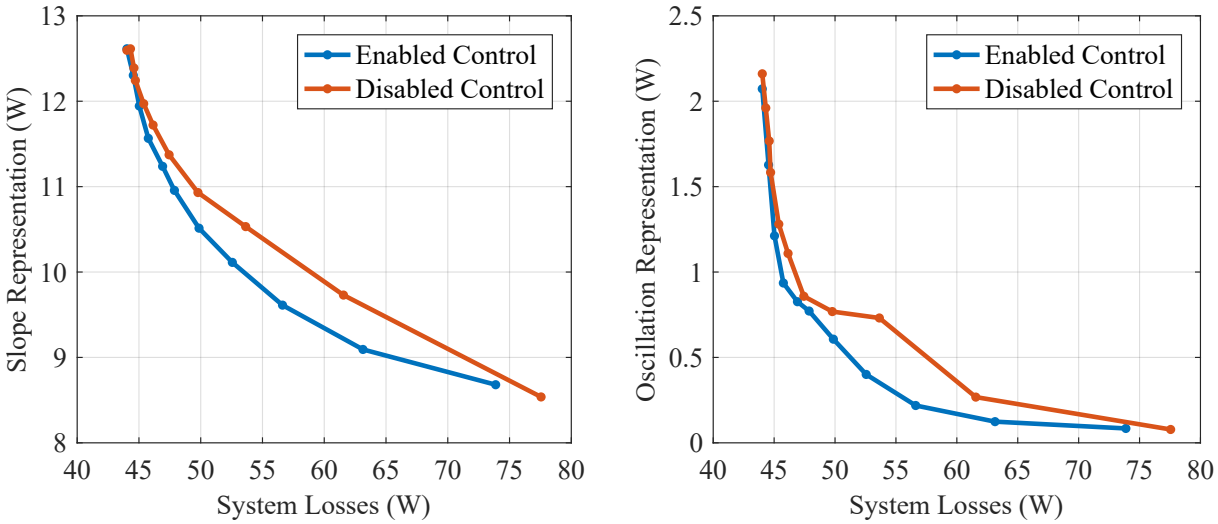


Figure 5.17: Comparison of switching, load conduction and semiconductor conduction losses. The dashed plots correspond to the disabled control mode.



(a) Slope emission representation over system losses.

(b) Oscillation emission representation over system losses.

Figure 5.18: Comparison of the slope and oscillation metric over the system losses.

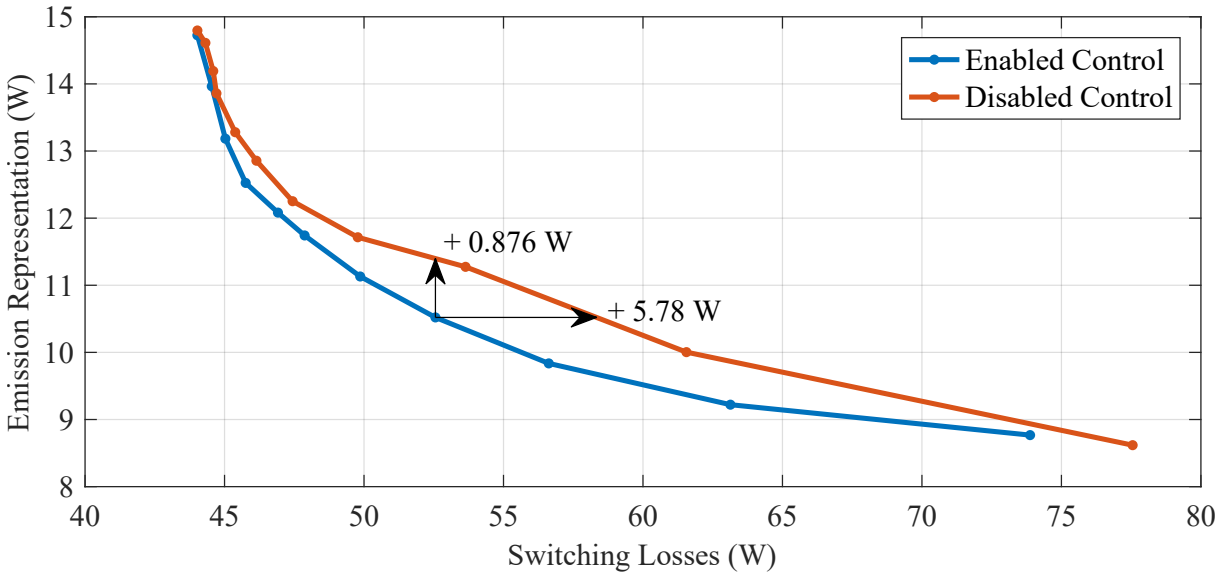


Figure 5.19: Emission representation between 1 MHz to 200 MHz over system losses at 400 V.

emission representation can be reduced by 0.88 W. For this emission level, this is a reduction of 7.69 % based on the emission level of the disabled control mode. The reduction of switching losses at the same emission level amounts to 5.78 W. In relation to the switching losses of the disabled control mode, this is a reduction by 9.91 %.

5.2.2 Variation of DC-Link Voltage

After the analysis of the control performance for changing set points, the performance of the controller facing different operating voltages is examined in this section. During the following measurements, the same control settings as described in Section 5.1.4 are used. The dc-link voltage is set to 400 V, 500 V and 600 V. At the same time, the modulation index is reduced to keep the load current amplitude constant in between the variations. To illustrate the control performance, two measurements are recorded for each voltage level. The first is at a 100 % of the set point range of the control setting. Additionally, 10 % are chosen as the second operating point. This second control target allows the controller to actively adapt the gate profiles instead of staying in the slowest gate profiles possible, which would be the case for 0 %.

Figure 5.20 depicts the voltage slopes calculated from oscilloscope measurements. For ease of interpretation, the 500 V measurement is omitted here but shown in the appendix in Fig. A.11. Similar to previous illustrations of the voltage slope, the gray areas mark the turn-on events. The first patch corresponds to the switching instances influenced by the low-side driver. For the turn-on events, the difference caused by the variation of the dc-link voltage is only visible in the measurements at 100 %. Here, the slopes marked

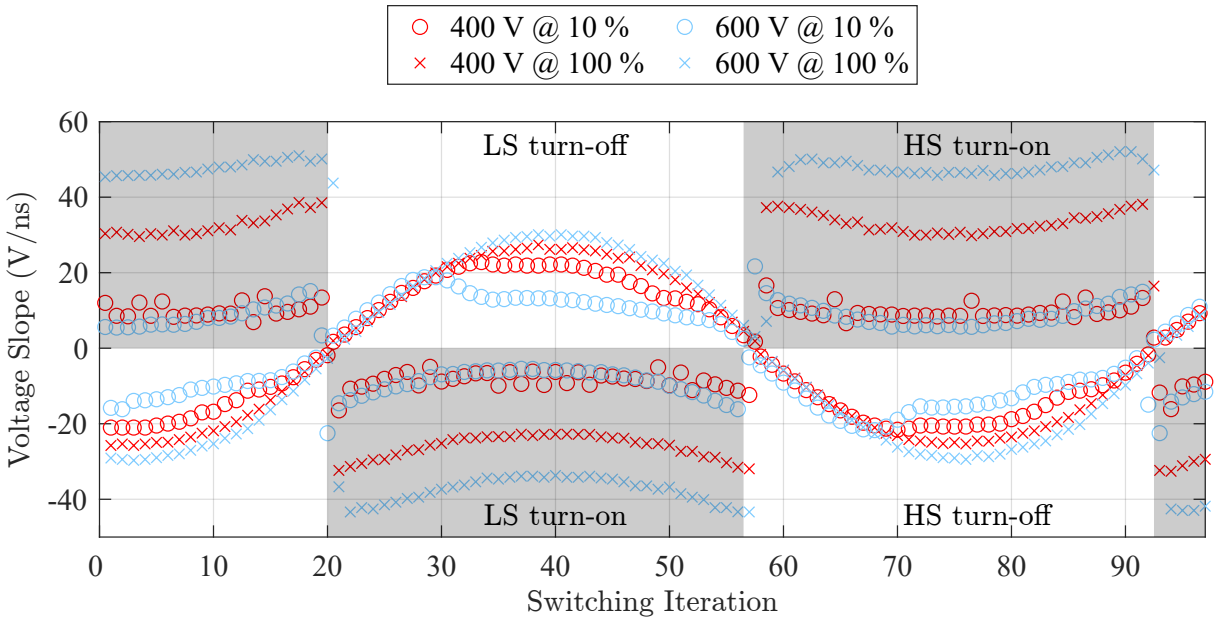


Figure 5.20: Voltage slopes during variation of dc-link voltage from 400 V to 600 V for high and low set points.

with "x"in the gray patches show increasing values, for the increasing dc-link voltage. At the same time, the measurements taken while the controller is set to 10 % only show small deviations between the two variations. This indicates that the controller is able to adapt the voltage slope according to a set point for the turn-on independent from the dc-link voltage.

Because the turn-off controller uses the oscillation sensor as input, the corresponding switching events in the white areas show significant differences between the different dc-link voltages. These differences are caused by the changing resonance frequency, which in turn is caused by the voltage dependent output capacitance of the SiC MOSFETs. This leads to a different interpretation by the oscillation sensor.

Instead of the voltage slope for each switching event, Fig. 5.21 depicts the peak voltage after a switching instance. This illustrates the overshoot behavior of the converter during the variations of the dc-link voltage. The largest change is noticeable for the turn-on events again. However, instead of increasing peak voltages, a decrease in the peak amplitude is visible. This is due to the decrease in C_{OSS} of the semiconductor devices for increasing dc-link voltages.

In a similar manner to the voltage slopes, the control performance is very good for the turn-on events. However, the turn-off peaks are only shaved off by about 30 % of their respective maximum peaks.

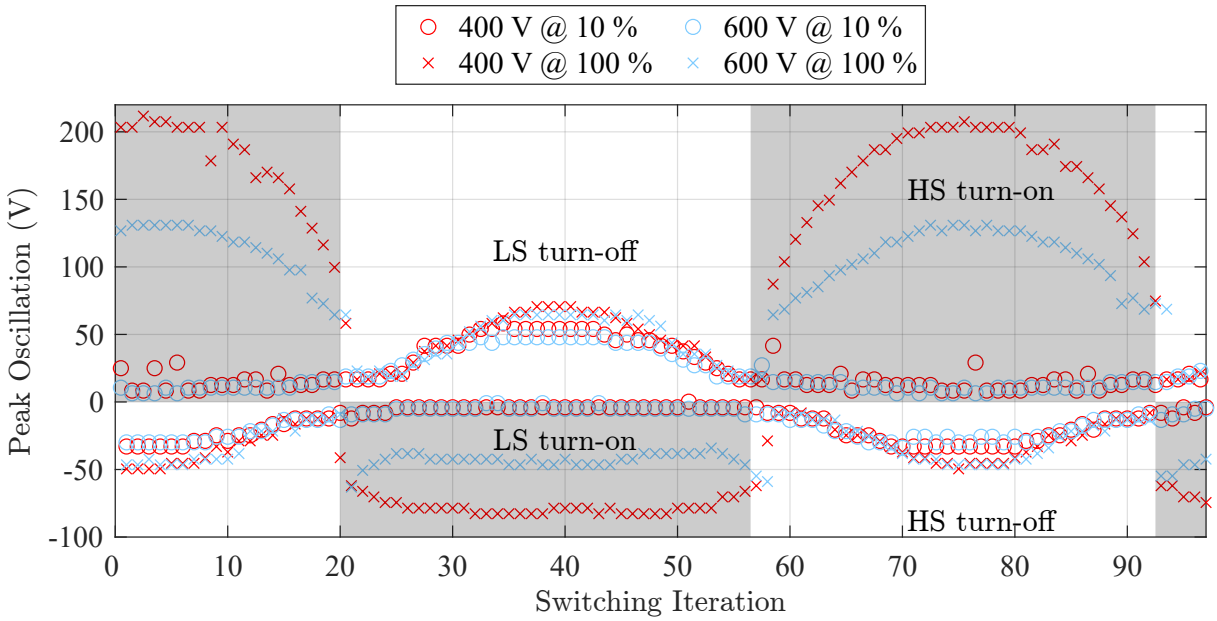


Figure 5.21: Peak oscillation amplitude during variation of dc-link voltage from 400 V to 600 V.

The change in the resonance frequency is clearly noticeable in Fig. 5.22. This figure depicts the difference between the disturbance voltage measurements at 100 % and 10 % at their respective dc-link voltage. At 63 MHz the original resonance is visible and the peaks shift towards higher frequencies with increasing dc-link voltage. For 500 V and 600 V the resonances are at 66.7 MHz and 69 MHz respectively.

The overall amplitude of the difference in the range of 10 MHz to 30 MHz increases with higher dc-link voltages. This is caused by the overall trend of increasing emissions for higher voltages and the controller being able to maintain the low emission level, in spite of the change in the dc-link voltage. Therefore, the improvements between the measurements at 600 V is about 3 dB better than the difference at 400 V.

To retrace the controller's actions, a closer look at the sensor readings is done in the following figures. Firstly, Fig. 5.23a shows the feedback recorded by the slope sensor during the turn-on events. The dashed lines represent the 100 % measurements at the various dc-link voltages. Similar to the calculated slopes in Fig. 5.20 the slope sensors ADC readings show an increasing slope for increasing dc-link voltages. However, the measurements for the 10 % setting indicate a successful control by keeping the slopes at a low level. The slight concave shape of the sensor readings indicate, that the control parameters are at their maximum level towards the beginning and end of the control period and can not decrease the slope any further for the 600 V variation. Additionally, the typical overshoot in the beginning of the control period occurs in the 600 V variation at 10 % set point.

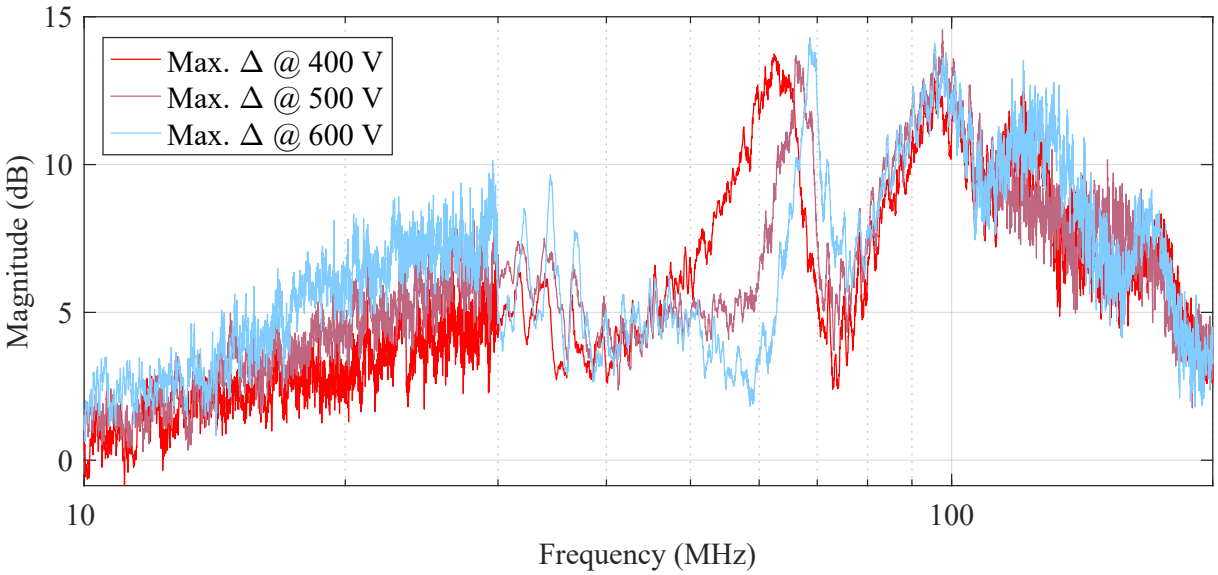
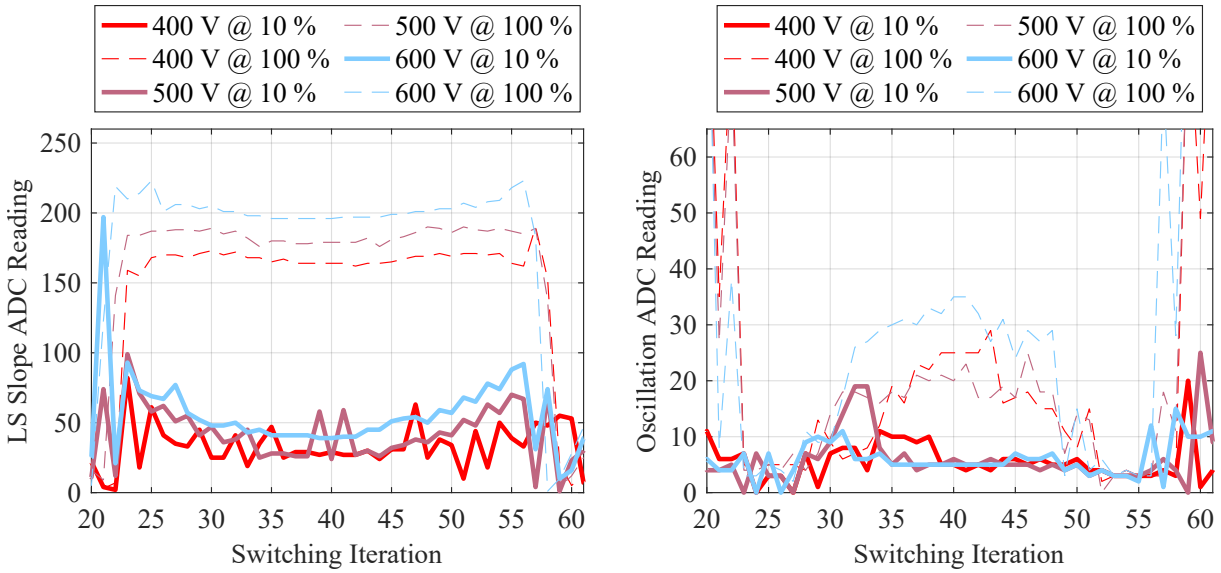


Figure 5.22: Differences in disturbance voltage measurements between high and low set points at 400 V to 600 V in disabled control mode.

Secondly, the feedback provided by the oscillation sensor is presented in Fig. 5.23b. The most notable characteristic of the recording is the inverse relationship between the peak amplitude measured in Fig. 5.21 and the sensor readings. Although for the 100 % set point, the peak voltage amplitude decreases with increasing dc-link voltage, the sensor reading increases. This is caused by the shift of the resonance towards higher frequencies. At 69 MHz the resonance is closer to the center of the pass-band of the oscillation filter. Therefore, the probe output is less attenuated and the dynamic range of the sensor is better utilized. Furthermore, the typical overshoot at the beginning of the sine half wave is visible for the 10 % set point configuration. However, the measurement at 600 V shows the smallest overshoot. This is because the controller entered the blanking period at a better parameter value compared to the other dc-link voltages. The controller's behavior is additionally analyzed using the changes the controller makes to the control parameters in Fig. 5.24.

Figure 5.24a depicts the control parameter values corresponding to Fig. 5.23a. The noticeable peak towards the beginning of the measurements, is the controllers reaction to a single slow switching event during the low current phase in between control periods. As a reaction to the sensor reading below the set point, the controller increases the control parameter. However, at the next switching instance enough load current is present to allow a high voltage slope. This steep slope is recognized by the controller and the last change in the control parameter is reversed. Therefore, the overshoot only occurs for a single switching instance. In the center of the control period, the controller hits the lower limit of the control parameter for the 600 V variation. This causes the concave shape in Fig. 5.23a. For the lower voltages, the controller is still actively controlling the parameter to keep the sensor reading at the set point.



(a) Slope turn-on feedback.

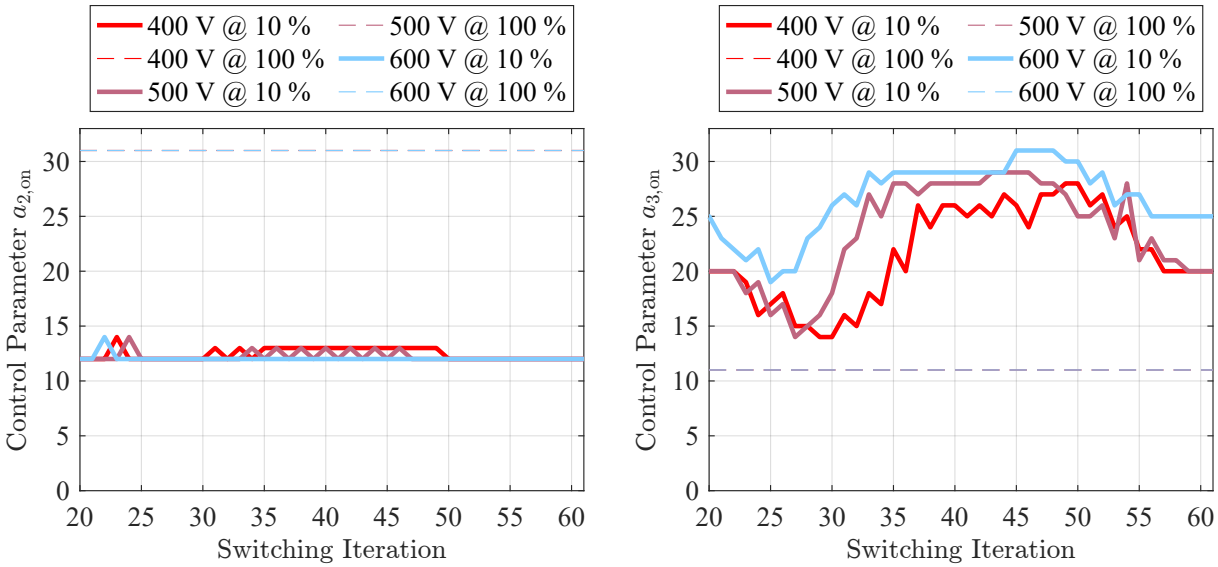
(b) Oscillation turn-off feedback.

Figure 5.23: Slope and oscillation sensor readings for the low-side switches in phase 2 at different operating voltages.

The turn-off control shows more adaptions to the control parameter, as is illustrated in Fig. 5.24b. This is due to the greater dependency of the turn-off switching characteristics on the load current, compared to the turn-on process. The aforementioned shortcomings of the control algorithm for this kind of disturbance are visible between iterations 10 to 22. Here, the controller senses a low oscillation and tries to increase the switching speed by decreasing the positive component of the turn-off profile. However, as soon as the load current rises, the oscillation amplitude increases and the controller has to reverse several changes to the control parameter. During these steps, the oscillation amplitude produces the overshoot visible in the oscillation sensor reading. Afterwards the controller is able to maintain the oscillation amplitude at the desired level. Towards the end of the control period, the controller tries to increase the switching speed again, but is not able to. As soon as the sign of the current flips, the control parameters are frozen and will be unfrozen after the blanking state ends.

5.2.3 Variation of AC Current

In this section, instead of a variation in the dc-link voltage, the RMS load current amplitude is changed in between measurements. The following measurements are recorded at 400 V and load currents of 17 A, 19.5 A and 22.5 A. Lower load current amplitudes are omitted because the trade-off between EME and switching losses is more important for moderate to high load currents. To analyze the resilience towards changes in the load current amplitude, the same measurement methods as in the previous experiments are used. Furthermore, the controller targets 10 % and 100 % set points again.



(a) Changes in the turn-on control parameter.

(b) Changes in the turn-off control parameter.

Figure 5.24: Comparison of the control parameters' progression during the control period.

Firstly, the voltage slopes are calculated from oscilloscope measurements and plotted over the corresponding switching iteration. For varying currents, this leads to the data depicted in Fig. 5.25. Again, the second variation is omitted to increase readability. All three variations are contained in Fig. A.13. There is only a difference of about 10 % in the voltage slopes for the turn-on events at 100 % set point between the two current variations. This is comparable to the good agreement between the turn-on voltage slopes at 10 % set point. Therefore, the turn-on controller is able to maintain a constant voltage slope for the different current amplitudes. However, the turn-off slopes in the 10 % and 100 % setting both change with the variation of the load current amplitude. In consequence, the turn-off controller's performance is dependent on changes in the load current.

Figure 5.26 depicts the peak oscillations amplitudes for the variations in the load current and set points. Similar to the voltage slopes, the peak oscillation amplitudes of the turn-on events change by a small amount between the current variations. The overshoots of the turn-on instances, for which the set point is 10 %, are limited to the same values no matter the changes in the load current. In case of the turn-off events, the peak oscillation amplitude increases by up to 20 % between the load current amplitudes for the 100 % set point. The overshoots produced by the 10 % set points however, remain at a similar lower level. Therefore, the turn-off controller's performance is dependent on changes in the load current amplitude.

In the next measurement, the differences between the disturbance voltage measurements of the set points at different load currents are analyzed. They are depicted in Fig. 5.27. Besides slightly shifted peaks in frequency and slight reduction of the emission level at

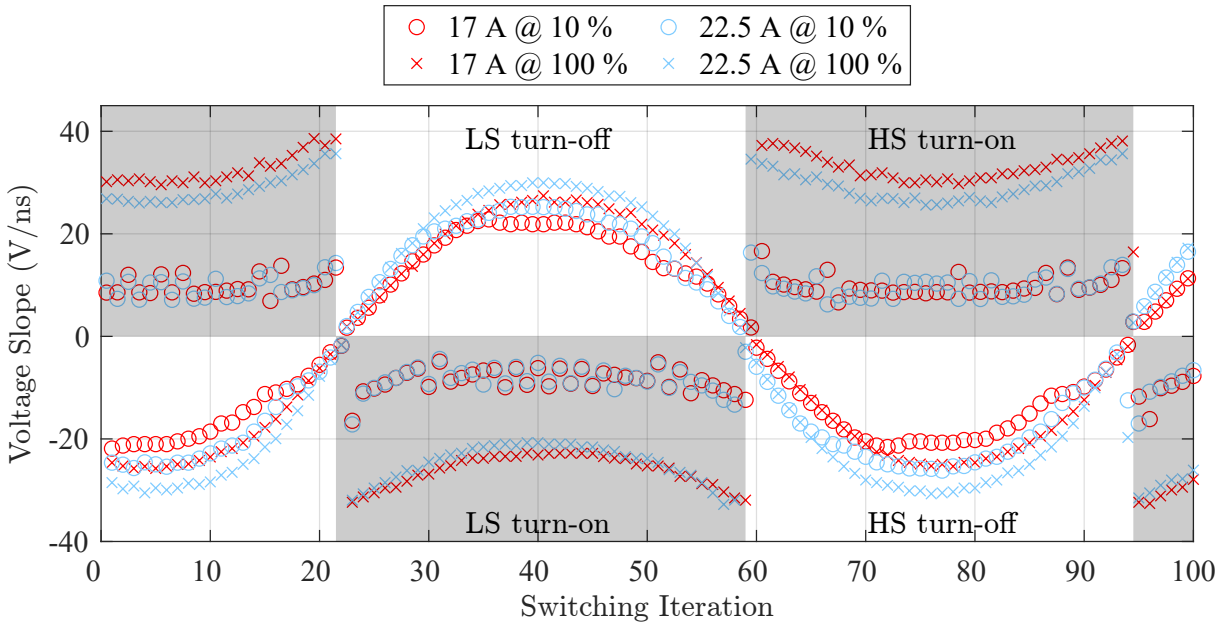


Figure 5.25: Voltage slopes calculated for a full ac sine period with a variation of the control setting from 10 % to 100 % and the load current from 17 A to 22.5 A.

100 MHz no notable changes are apparent in these measurements. This indicates a minor impact of the turn-off characteristics on the overall EME in this operating point.

As is expected from the analysis of the time domain measurements, no noticeable changes in between the different load current amplitudes are visible on the slope sensors feedback in Fig. 5.28a. In contrast, the measurements of the oscillation sensor in Fig. 5.28b at the maximum switching speed result in a change of about 22 points at iteration 40. However, the measurements with the controller set to 10 % exhibit very similar characteristics across the current variations. Because the difference in the disturbance voltage measurements is negligible, this indicates, that the influence of the changes in the turn-off characteristics on the frequency spectrum are also negligible.

The control behavior is reflected in Fig. 5.29a and Fig. 5.29b where a similar characteristic is seen for the variations of the dc-link voltage. This time the turn-on controller in Fig. 5.29a does not reach its lower limit during the center part of the control period. Furthermore, the singular peak, which causes the overshoot in the slope measurements, at iteration 23 is visible again. Figure 5.29b exhibits the same characteristics as Fig. 5.24b, where a slightly quicker recovery from the dip in the control parameter is apparent for the higher load current amplitudes.

The analysis of measurements at changing load currents yields the following conclusions:

- The turn-on controller's performance is independent of the load current.

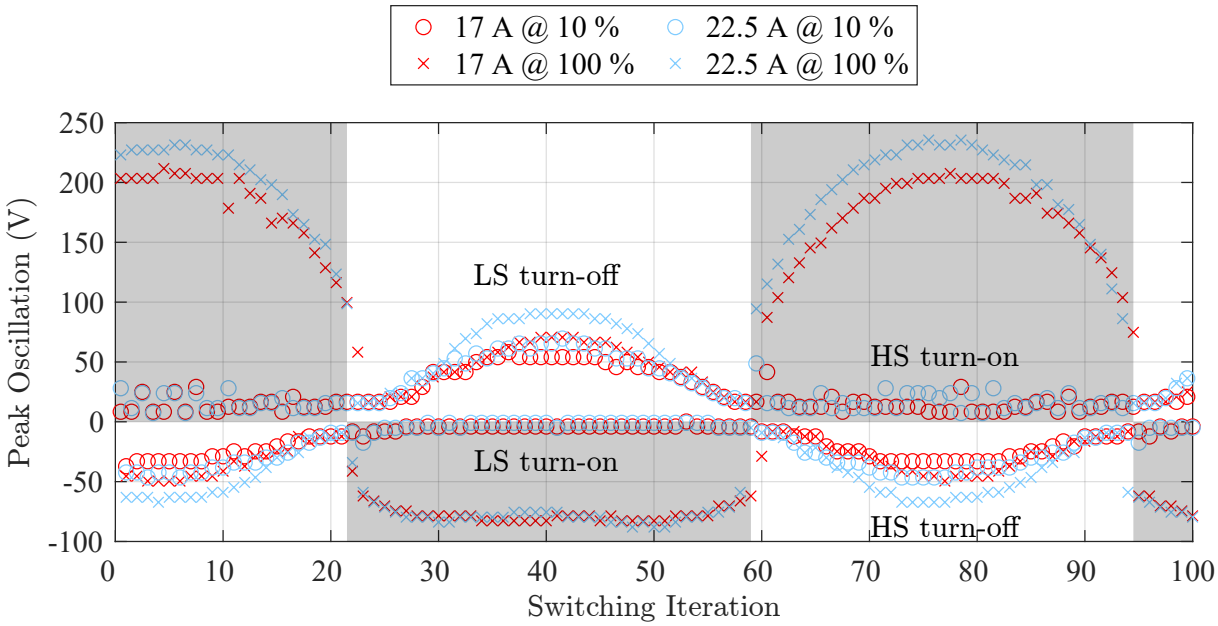


Figure 5.26: Peak oscillation amplitude for a full ac sine period with a variation of the control setting from 10 % to 100 % and the load current from 17 A to 22.5 A.

- In this operating point, changes in the turn-off behavior have a negligible impact on the overall EME
- The oscillations sensors' dynamic range has to be extended towards low amplitudes.

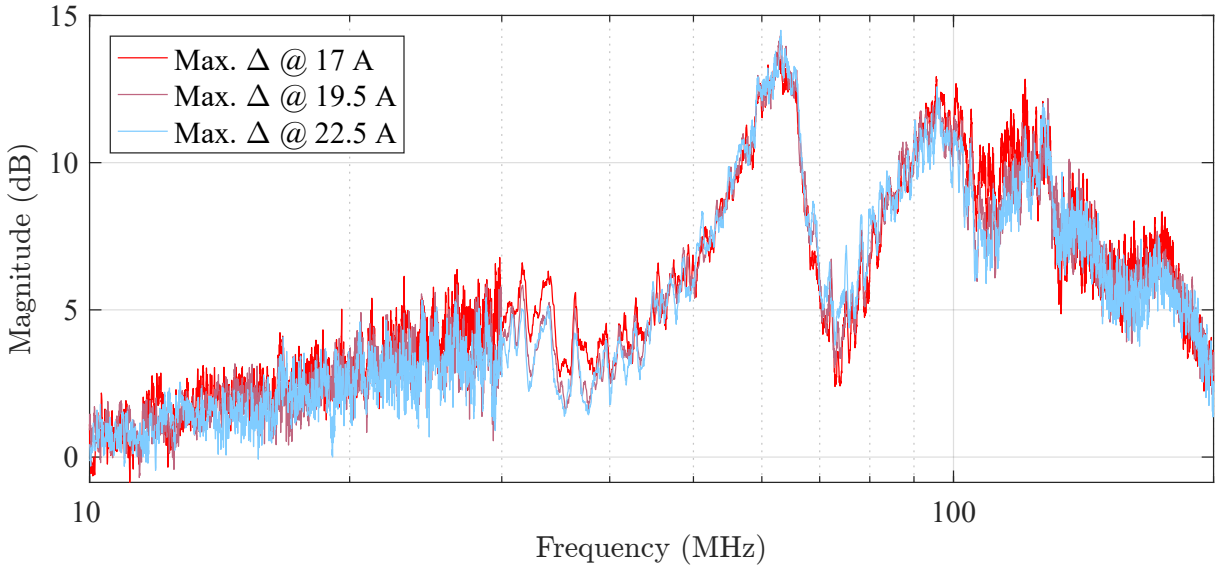
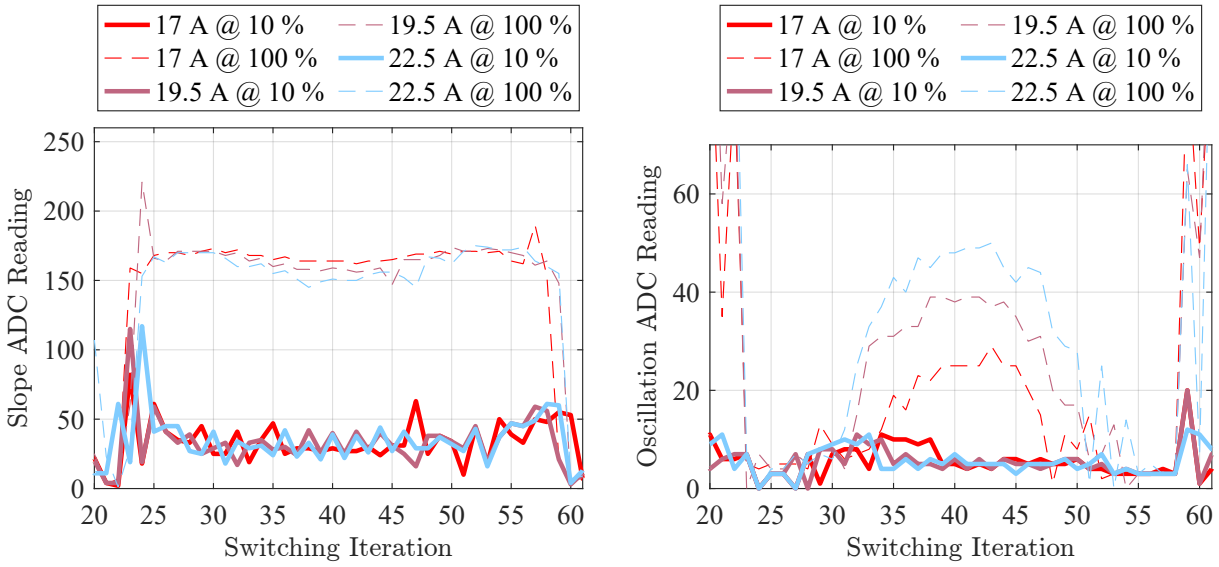


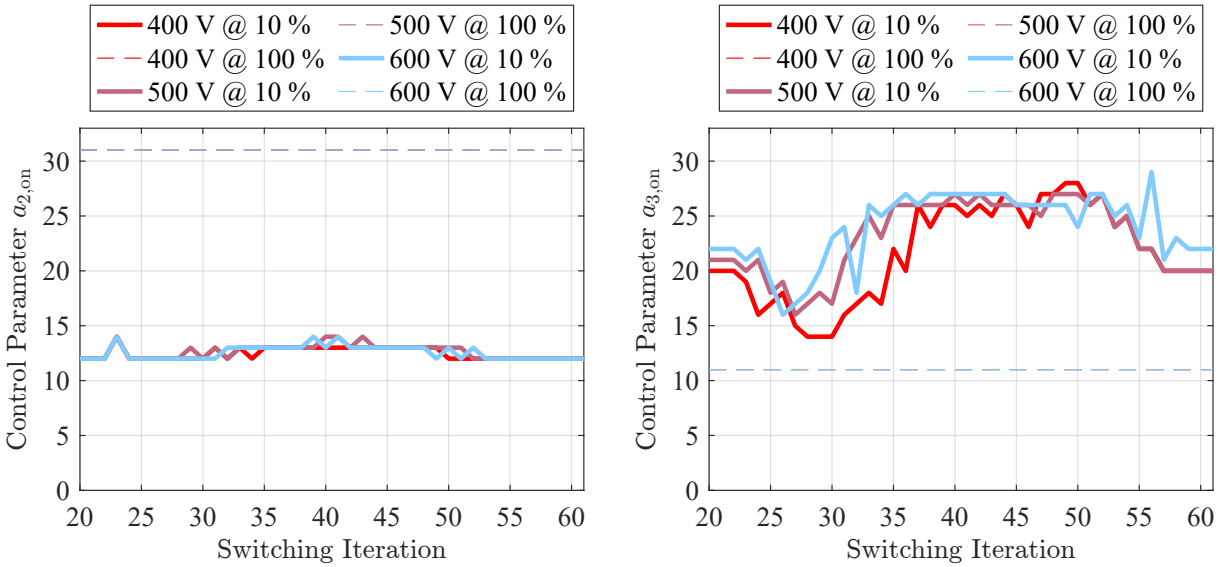
Figure 5.27: Differences between high and low set point at ac current from 17 A to 22.5 A.



(a) Slope turn-on feedback.

(b) Oscillation turn-off feedback.

Figure 5.28: Slope and oscillation sensor readings for the low-side switches in phase 2 at different load currents.



(a) Changes in the turn-on control parameter.

(b) Changes in the turn-off control parameter.

Figure 5.29: Comparison of the control parameters' progression during the control period.

5.3 Summary

Recap

In this chapter, the performance of the controller was evaluated in a continuously operating traction inverter. Because the inverter setup and measurement methods influence the control results, they were described in detail. The PCBs, measurement equipment and measurement methods were presented. Afterwards, the performance of the closed-loop controller was evaluated while sweeping through control settings, the dc-link voltage and a range of RMS load current amplitudes.

Conclusion

The evaluation of the control performance is based on the variation of the set point, the variation of the dc-link voltage and RMS load current amplitude. The first of the three variations highlights the capabilities of the controller to adapt the switching characteristics according to the selected EME level. When instead of the set points, the control parameters are changed, the drivers behave as non-adaptive gate drivers and this mode is used as a reference for the active control mode. The sweeps through the control settings result in a portrayal of the compromise between switching losses and the amount of EME created at the respective operation point. For all emission levels, an improvement in the switching losses over the non-controlled reference mode is achieved and at moderate emissions and losses, an improvement of up to 9.91 % of the switching losses is reached.

To test the resilience of the controller against changes in the operating conditions, either the dc-link voltage or the load current is varied, while the other is held constant. This way, only a singular change in the operating conditions is made and the correlation between the operating point and changes in the control performance are analyzed. For the turn-on events, no noticeable changes in the controllers performance are apparent. This indicates that the turn-on controller is able to achieve defined set points regardless of the load current or dc-link voltage. In contrast, the turn-off events, which are controlled by the oscillation sensor, exhibit a greater dependency to the operating conditions. This is in part due to the changing resonance frequency and its position in the passband of the oscillation sensor and due to the greater dependency of the turn-off characteristics on the load current. However, the control algorithm performed as expected and its behavior is resilient towards changes in the operating conditions.

6 Conclusions and Outlook

In this thesis, all aspects of a driver integrated closed-loop control for EME and switching losses were presented. This last chapter briefly summarizes the previous chapters, highlights the contributions to the development of intelligent gate drivers and draws conclusions based on the findings for each topic. Additionally, an outlook towards possible future work is given.

6.1 Summary

The previous chapters lead through the control diagram one element at a time.

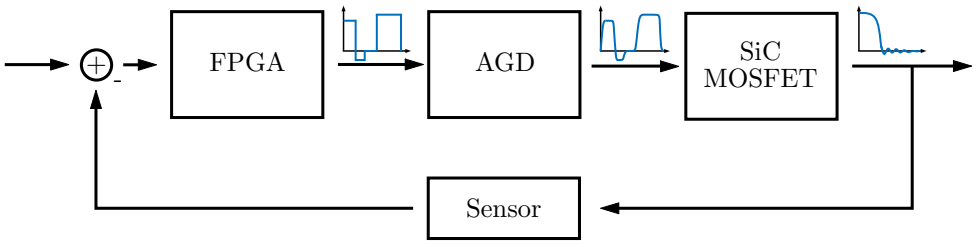


Figure 6.1: Control loop introduced in this thesis.

Firstly, Chapter 2 presented the AGD. An introduction into the setup of the switching cell and its parasitics was given to provide a baseline for the following analyses regarding the switching characteristics. Afterwards, the topology of the adaptive current source driver was presented. Measurements that used different settings of the AGD were used to derive a metric to represent the switching characteristics of the semiconductor devices.

Secondly, the sensing element, which provides the feedback for the control circuit, was presented. An extension to the approaches that were proposed in previous research is suggested. This extension allows a distinction of the switching characteristics into the switching slope and oscillation amplitude. The new sensor topology was presented and its performance characterized.

Thirdly, Chapter 4 proposed the closed-loop control algorithm. The modules used to implement the control algorithm on the FPGA have been described in detail. Furthermore, two exemplary operating points demonstrated the feasibility of using the control algorithm in dc and ac applications.

The final chapter evaluated the control performance of the closed-loop controller in a three phase inverter application. Because the evaluation was done based on four different measurement methods, each of them was introduced. Besides the multiple measurement methods, a variation of the control settings and a variation of the operating voltage as well as load current were utilized to provide a diverse field of operating points. Time domain measurements and the feedback provided by the sensors were used to analyze the controllers behavior during the sinusoidal excitation in various operating points. From the frequency domain measurement and the switching losses an assessment of the control performance was done.

6.2 Contributions

This section highlights the contributions of this thesis that exceed existing research approaches.

Scalable Adaptive Current Source Gate Driver A new adaptive current source gate driver topology is proposed. In comparison to other AGD topologies, this driver enables precise, dynamic and flexible control over the gate current and therefore, the switching behavior of the semiconductor device. By implementing the DAC stage in the signal path of the driver, it can be scaled to the resolution required, independent from the power stage. Adaptive resistive drivers scale their resolution by copying their output stage. Furthermore, the output stage allows a parallelization of transistors to scale the maximum gate current according to the requirements of the connected semiconductor device.

Representative Metric for Switching Characteristics and EME This thesis proposes a metric which represents the emission behavior of semiconductor devices in several aspects. The previous approach sums up a section of a weighted power spectrum which is calculated from the FFT of singular switching events. However, the approach limits the representation to one frequency range and constant weighting factor. By using the transfer functions of the filters developed in this thesis, a dynamic weighting factor is introduced. This way, a distinction between different switching characteristics can be made which is amplified by the selection of the frequency range. Furthermore, in addition to the representation of single switching events the metric can be used for disturbance voltage measurements of continuously operated converters. If the transfer function is omitted and the frequency ranges are set according to the expected switching characteristics, the metric represents the converter's behavior with regards to its EME. Therefore, this metric can be used to compare different emission levels at the respective switching losses and optimize the trade-off between EMI and efficiency.

Sensing Different Switching Characteristics To allow control over the emission behavior of a converter, information about different aspects of the switching events is required. Previous sensing approaches propose a singular evaluation of a derivative of the switching dynamics. These approaches are extended by the separation of the voltage slope and oscillation amplitude of the switching events. This way, independent feedback with regards to the voltage slope and oscillation amplitude is provided to the controller.

Dynamic Closed-Loop Control Algorithm Finally, all elements necessary for a closed-loop control are available. In comparison to control approaches presented in previous research, the algorithm proposed in this thesis allows a dynamic adjustment of the control behavior and can operate continuously in a traction inverter. Therefore, this control platform allows the evaluation of control settings in various operating points and with various priorities.

6.3 Conclusions

Three major conclusions can be drawn from the work that is presented in this thesis. Firstly, **AGDs are able to influence the switching characteristics with regards to EME** and switching losses. The measurements in Chapter 2 and the proposed metric representing the emission behavior, show a high correlation between the gate driver settings and the emission behavior of the switching events.
Secondly, **sensors can be used to measure the emission behavior** of power electronic converters. Chapter 5 demonstrates, that there is a direct dependency of the sensor readings and the EME behavior of the converter. Therefore, the sensors can be used to estimate the converters emissions and indicate the adjustments required to adapt the switching behavior.
Subsequently, the **control algorithm is able to improve efficiency and emissions at the same time**. By using the proposed AGD, sensors and control algorithm the converter's switching behavior can be controlled in a way that the EME and switching losses are improved at the same time. Instead of using double pulse tests, this is shown in a continuously running three-phase inverter.

6.4 Outlook

Based on the presented findings, future work on closed-loop controlled or intelligent gate drivers in several areas can be done. The **biggest challenge** in adoption of intelligent drivers into market ready applications is the **integration into single integrated circuits (ICs)**. The control logic, sensor evaluation and gate driving stage can be integrated

into an ASIC which drastically decreases the cost and PCB area required. Additionally, purpose-built control logic and driving stages will decrease the propagation delay between the sensor evaluation and adaption of the switching behavior. The development of such an ASIC has been part of the RobKom project and was part of the workpackages of the chair of integrated analog circuits and RF systems (IAS) at RWTH.

Secondly, a **revision of the gate driver** PCBs would give the opportunity to improve the vertical resolution of the current driver. The usage of the emitter followers as reference current sources in the driver topology requires a minimum voltage before any reference current is produced. By adapting the R2R ladder's scaling, the steps needed to reach this voltage can be minimized and the vertical resolution for the remaining current range will improve. Alternatively, the number of output bits of the FPGA could be increased to offer finer adjustments in the reference amplitude.

In addition to the updated driver hardware, a **different loads or topologies can be optimized** using the presented control platform. Instead of the artificial machine load, a real electrical machine could be connected. This would improve the prediction of the emission behavior by adding the relevant parasitic elements to the load. The control platform is independent from the topology since the control algorithm is running on the drivers. Therefore, tests with dc-dc converters can be conducted.

Lastly, this control platform allows **further optimization of the control settings, feedback sensor's bandwidths and the control algorithm** itself. Instead of the single parameter used in the control of Chapter 5, the controller can be supplied with more refined multi-parameter profile sets. This could further improve the gains this controller already achieved with regards to EME and switching loss reduction. For the purpose of allowing a wide range of operating points, the sensors' bandwidths have been chosen wider as a purpose-built design would require. For operations at fixed dc-link voltages a narrow band-pass filter can be used to allow a closer control of the oscillation behavior. The evaluation module in the implemented control algorithm adapts the discrete behavior of the 5 bit reference output to the range of the 12 bit feedback resolution. If the amplitude resolution of the driver is increased, the controller implementation can be simplified and designed closer to conventional control approaches.

A Appendix

A.1 Simulation Model

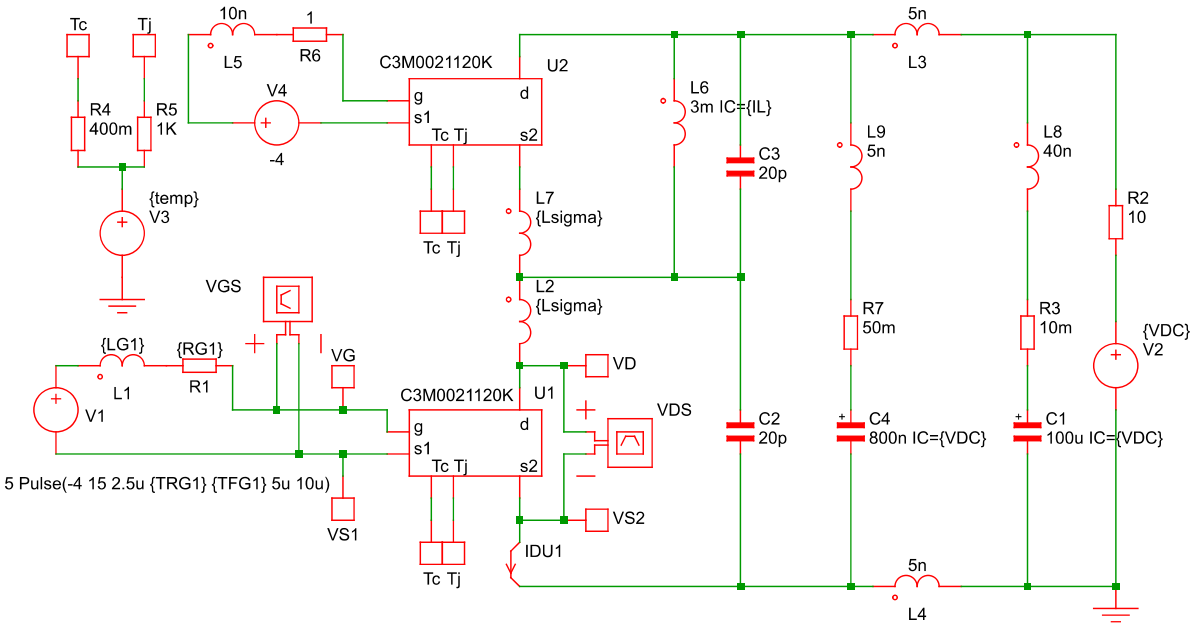
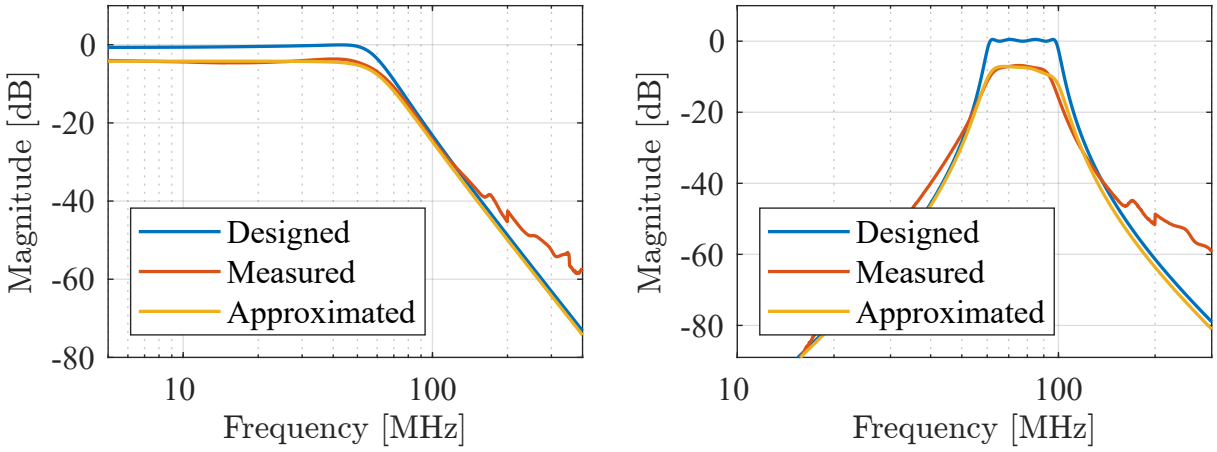


Figure A.1: Parametric simulation model created in SIMetrix.

A.2 Evaluation of Implemented Filters

Following the design of the filters, an analysis of the real performance in the prototype is done. Using a vector network analyzer (VNA) the red measurements in Fig. A.2 are acquired. Besides the non-ideal behavior above 150 MHz, an overall drop of the magnitude of the pass-band and a less sharp cut-off behavior at the skirts is visible. The degraded start of the skirts can be explained by discrepancies between the designed and used values of the passive elements. Only certain discrete values can be acquired and they come with tolerances for capacitors of at least 1 % and for inductors of 5 %. Additionally the parasitics of the passive elements have not been modeled during the initial design phase. These factors explain the changes close to the cut-off frequencies.

The overall drop in magnitude can be replicated by adding a parallel *RC* load to the filters. This is introduced by the measurement equipment during the tests. When implementing the additional load and introducing the parasitics of the passive elements, the yellow graphs show the resulting behavior.



(a) Lowpass Filter.

(b) Bandpass Filter.

Figure A.2: Comparison of measured and designed filters.

A.3 Additional Sensor Characterization at Low-Voltage

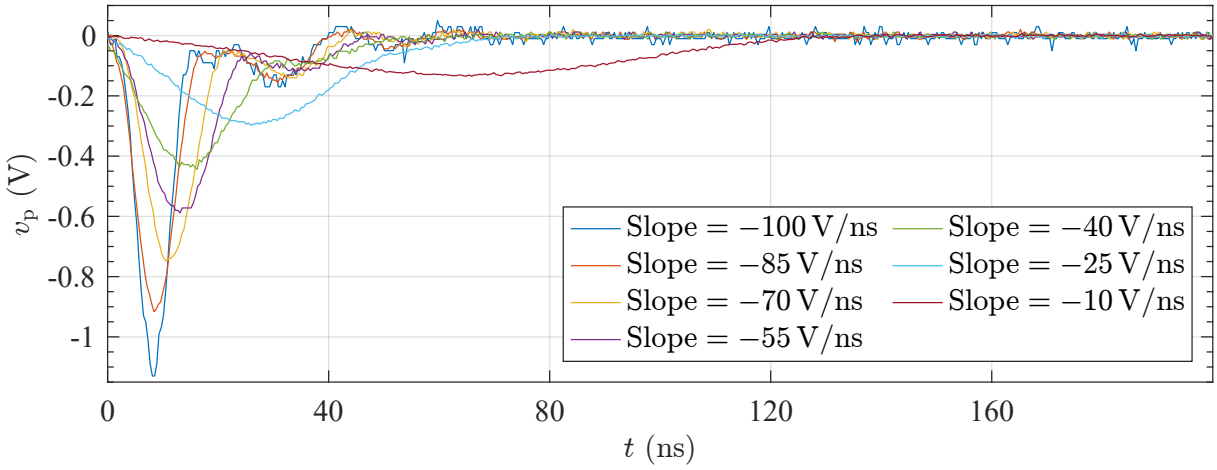


Figure A.3: Synthesized turn-on slope excitation used for the characterization of the sensor on the low-voltage PCB. The variations in the waveforms correspond to the behavior of different switching slopes.

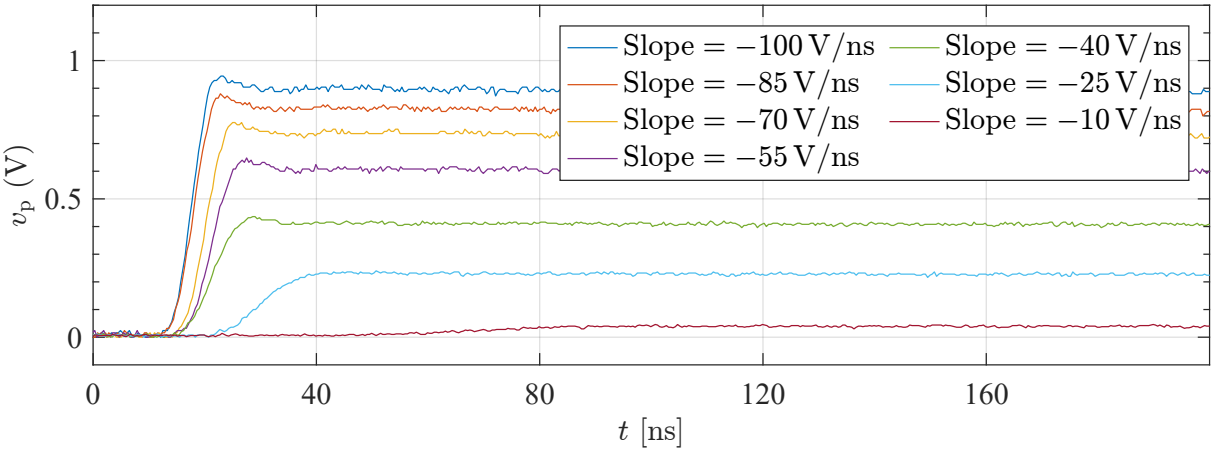


Figure A.4: Turn-on slope sensor output voltages after an excitation with the waveforms shown in Fig. A.3. Additionally, the cross excitation amplitude of the maximum oscillation input into the slope filter is shown in black.

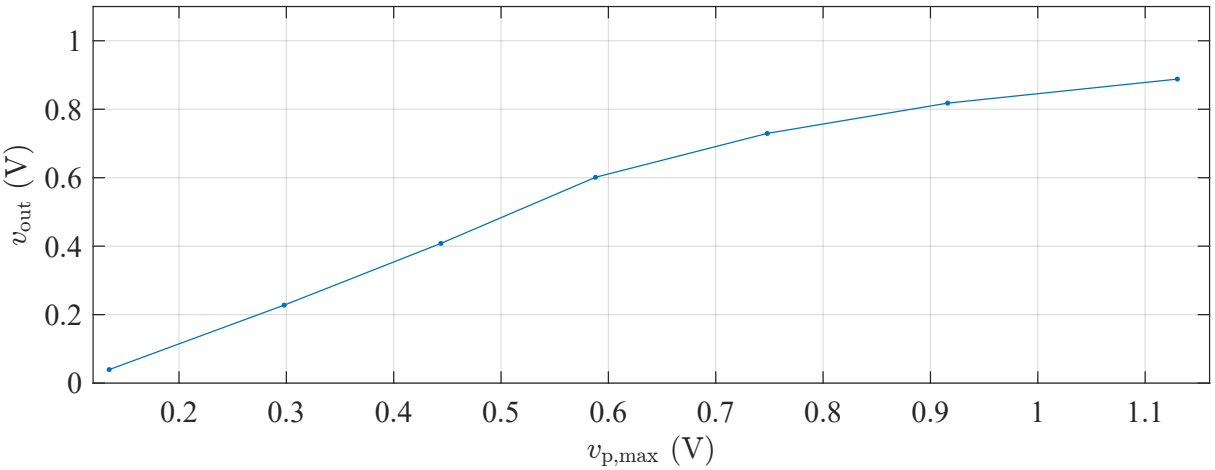


Figure A.5: The dependency between the sensor output voltage v_{out} and filter input $v_{p,max}$ of the turn-on slope sensor exhibits an increased saturation effect at greater input signals compared to the turn-off variant depicted in 3.18.

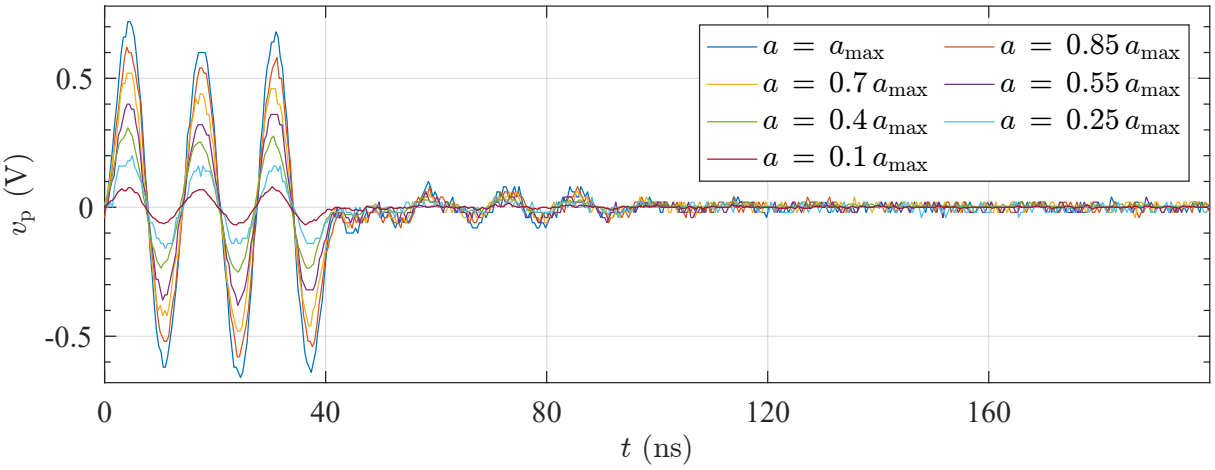


Figure A.6: Synthesized oscillation excitation used for the characterization of the sensor on the low-voltage PCB. The variations in the waveforms correspond to the behavior of different switching slopes. For this sensor no difference between turn-on and turn-off has to be made.

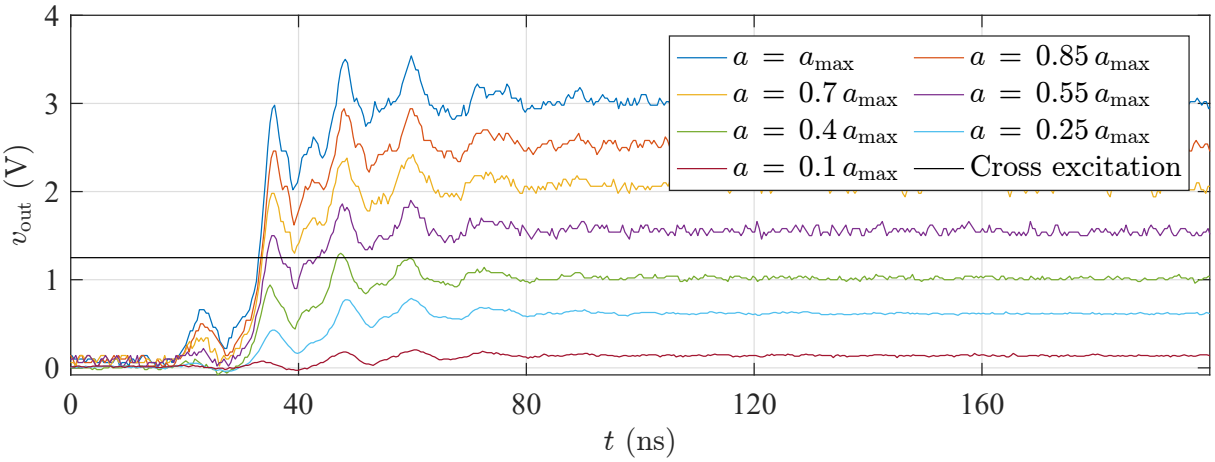


Figure A.7: Oscillation sensor output voltages after an excitation with the waveforms shown in Fig. A.6. Additionally, the cross excitation amplitude of the maximum slope input into the oscillation filter is shown in black.

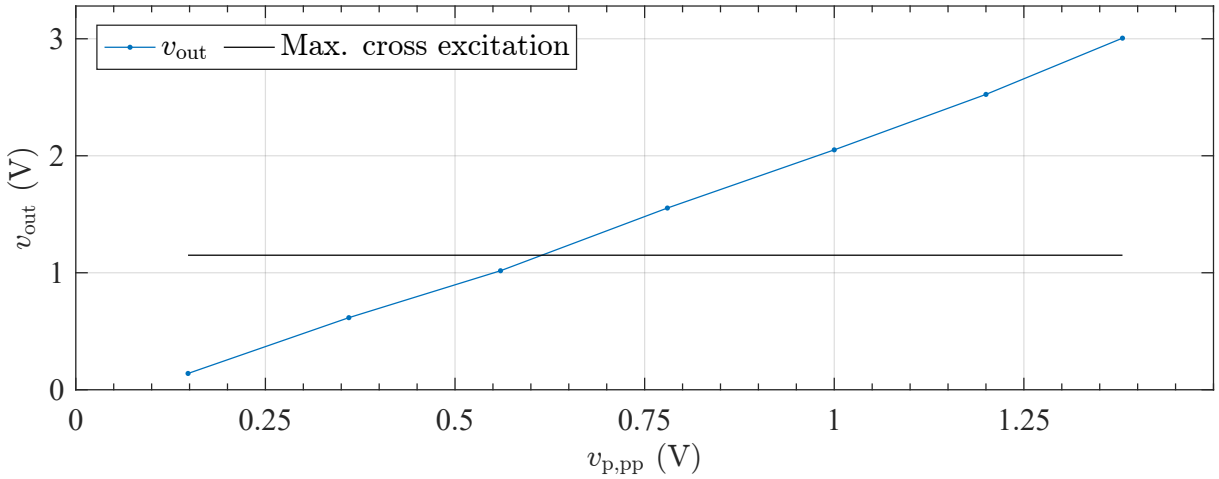


Figure A.8: The dependency between the sensor output and filter input of the oscillation sensor is linear. However the cross excitation caused by excitation of the oscillation filter from slope inputs is quite high.

A.4 Discretization in Slope Calculation

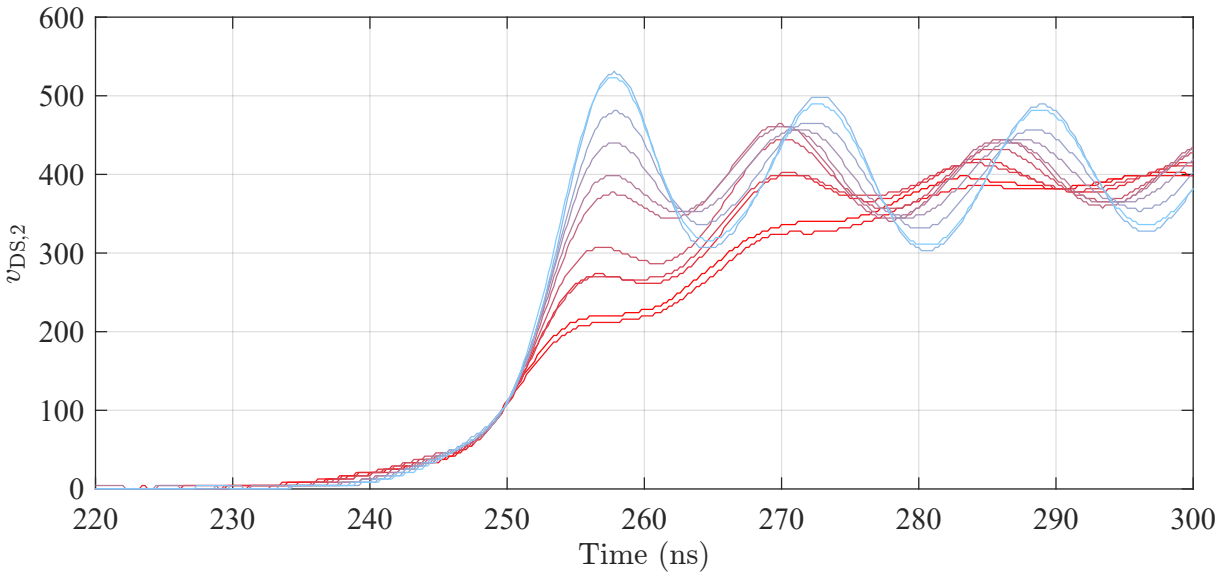
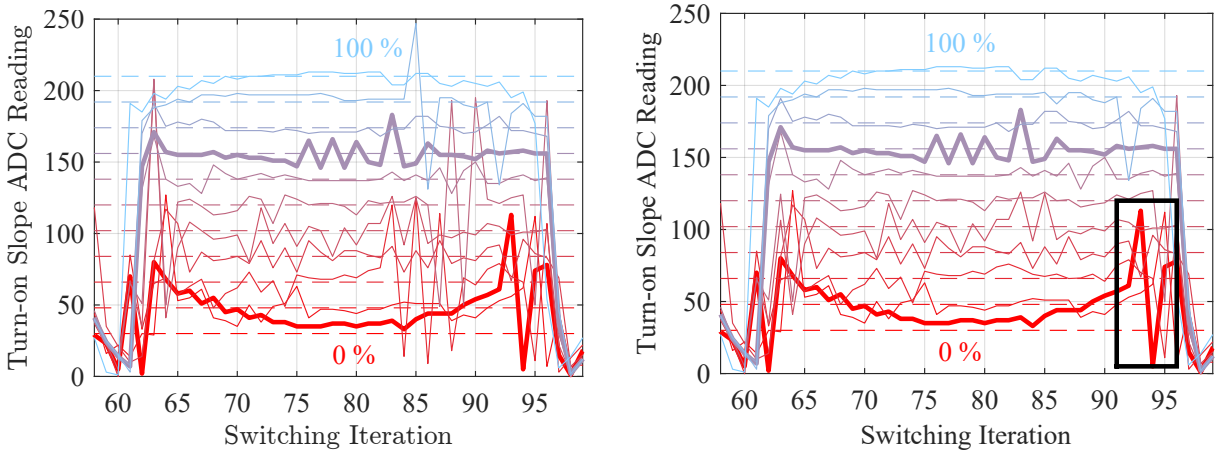


Figure A.9: Gap in calculated slopes is caused by way of choosing the start and end points of averaging interval. With decreasing switching speed, a step progresses further down and causes the gap in the otherwise linear dependency of the slope on the set point.

A.5 Communication Error Correction Example



(a) Turn-on slope feedback of high-side driver connected to phase 2 without communication error correction.

(b) Turn-on slope feedback of high-side driver connected to phase 2.

Figure A.10: Comparison between turn-on slope feedback with and without communication error correction.

A.6 Complete Slopes and Peak Oscillations for Voltage and Load Current Variation

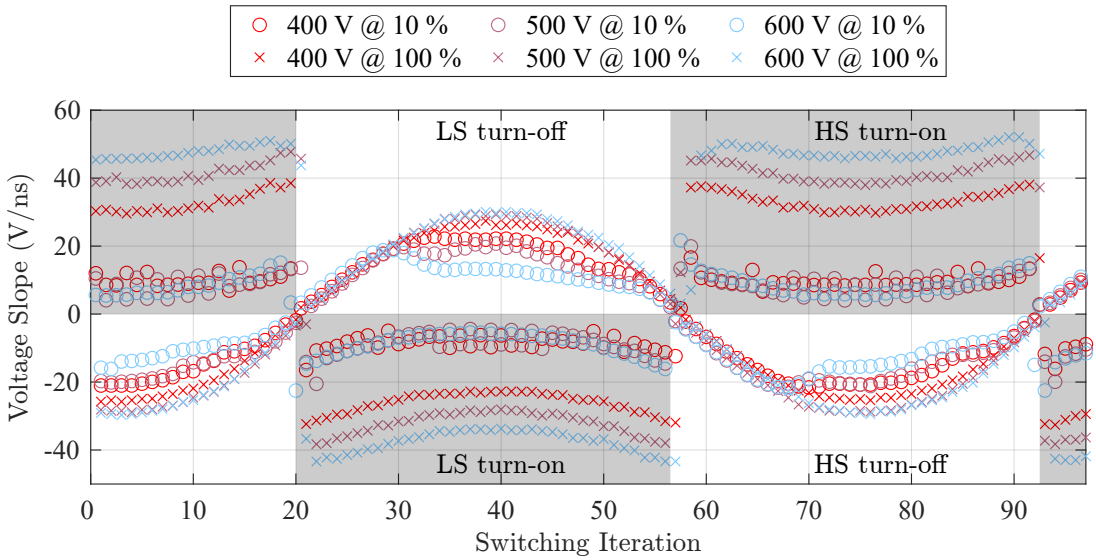


Figure A.11: Voltage slope during variation of dc-link voltage from 400 V to 600 V.

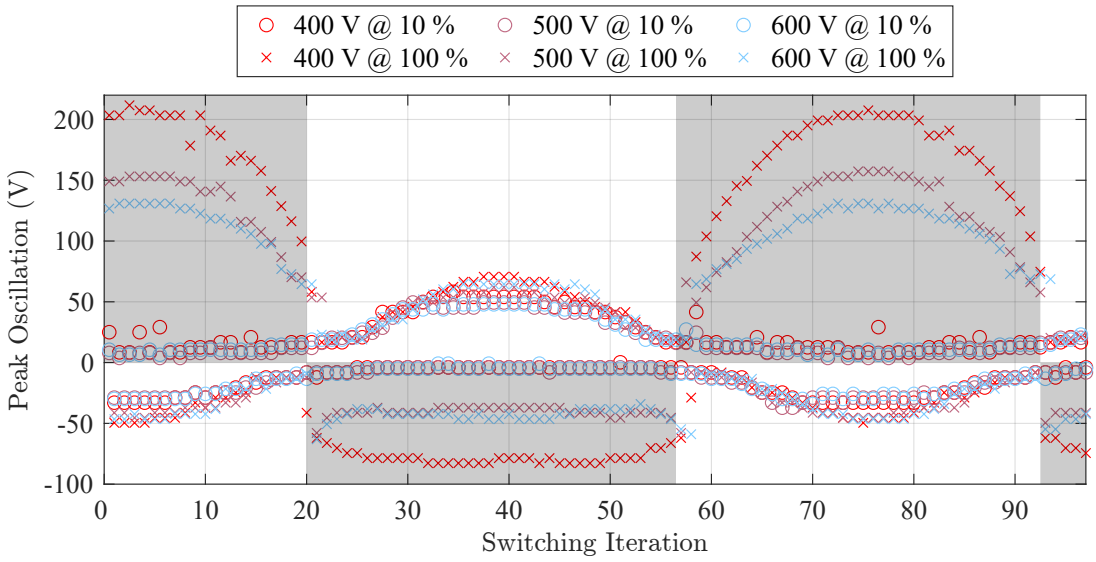


Figure A.12: Peak oscillation amplitude during variation of dc-link voltage from 400 V to 600 V.

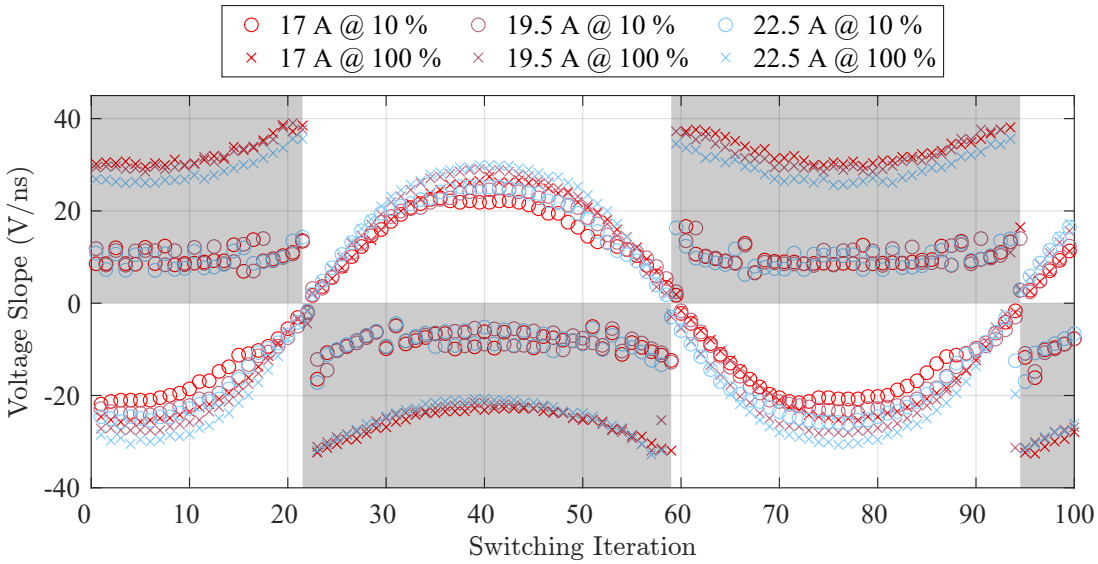


Figure A.13: Voltage slopes during variation of AC current from 17 A to 22.5 A.

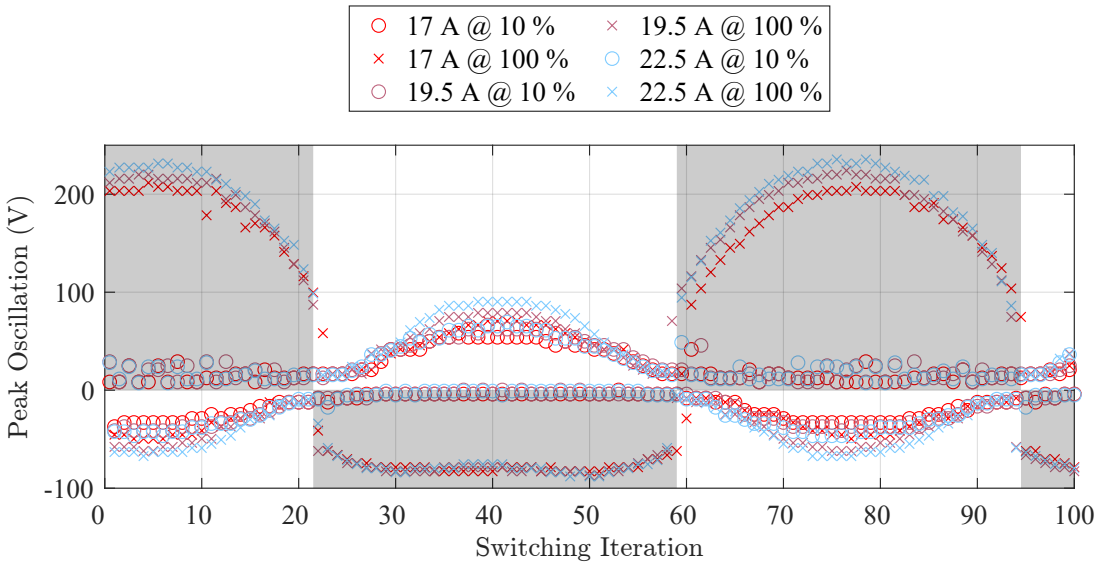


Figure A.14: Peak oscillation amplitude during variation of AC current from 17 A to 22.5 A.

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Weber, Felix Martin
Stability of lithium electrolyte interphase enabling rechargeable lithium-metal batteries
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The superior characteristics of wide bandgap semiconductors in terms of lower switching losses compared to silicon devices lead to increased power densities, which are especially advantageous for mobile applications. However, this advantage comes at the cost of faster switching transitions which are disadvantageous in terms of electromagnetic emissions. Additionally, the increased requirements for optimized switching cell designs lead to decreased parasitic elements. These developments shift the emission characteristics of the switching behavior to higher frequencies. This and the overall rise in emissions can cause interference in communication protocols or radio applications.

This work presents a gate-driver-integrated closed-loop control of electromagnetic emissions in wide bandgap power electronics. The driver itself analyzes and adjusts the switching characteristics to meet a given emission level. Therefore, no outside measurements or controller is necessary, as is the case for existing approaches. In the context of wide bandgap semiconductors, this allows to overcome the state-of-the art static design methodology of choosing a fixed gate resistor during design, which is only optimized for the worst-case operating conditions and offers no flexibility.

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