Process engineering for wafer-level integration of graphene into industrial applications

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Abstract

Due to the outstanding mechanical, thermal, and electrical properties of graphene compared to conventional industrial material systems in semiconductor fabrication lines, its use can improve the performance of existing silicon-based applications. Possible application examples for graphene-based applications are in the field of micro- and nano-electromechanical systems as a membrane for loudspeakers, microphones, and pressure sensors, in the field of heat dissipation applications as a heat spreader, and in the field of electronic applications as an active element for high-frequency transistors and Hall sensors. To realize this, it is necessary to integrate graphene into existing semiconductor processes to enable its commercial use.

In the presented work, the integration of graphene into complementary metal-oxide-semiconductor (CMOS) compatible silicon-based technologies in semiconductor fabrication lines is investigated. The transfer of graphene at the wafer level with a wafer-bonding technique is analyzed concerning yield, contamination, handling, and scalability and is compared to standard wet transfer. The impact of the surface properties on the electrical behavior of graphene on an isolating substrate is examined and a new methodology is used for the control at the wafer level. Furthermore, the performance of graphene-based applications was investigated using the Hall sensor as an example with different integration approaches and compared with conventional silicon-based applications. Finally, a process flow was developed for the fabrication of graphene-based Hall sensor and test structures in a CMOS-compatible semiconductor fabrication environment using nanocrystalline graphite and the fabricated structures were electrically and optically investigated.

Zusammenfassung

Aufgrund der herausragenden mechanischen, thermischen und elektrischen Eigenschaften von Graphen im Vergleich zu konventionellen industriell genutzten Materialsystemen in Halbleiterfertigungslinien kann dessen Verwendung die Leistung bestehender siliziumbasierter Anwendungen verbessern. Mögliche Anwendungsbeispiele für Graphen-basierte Applikationen sind im Bereich der mikro- und nano-elektromechanischen Systeme als Membran für Lautsprecher, Mikrofone und Drucksensoren, im Bereich der Wärmeableitung als Wärmespreizer und im Bereich der elektronischen Anwendungen als aktives Element für Hochfrequenztransistoren und Hall-Sensoren. Um dies zu realisieren, ist es notwendig, Graphen in bestehende Halbleiterprozesse zu integrieren, um eine kommerzielle Nutzung zu ermöglichen.

In der vorliegenden Arbeit wird die Integration von Graphen in komplementäre Metall-Oxid-Halbleiter (CMOS) kompatible Silizium-basierte Technologien in Halbleiterfertigungslinien untersucht. Der Transfer von Graphen auf Waferebene mit einer Wafer-Bonding-Technik wird im Hinblick auf Ausbeute, Verunreinigung, Handhabung und Skalierbarkeit analysiert und mit dem Standard-Nass-Transfer verglichen. Der Einfluss der Oberflächeneigenschaften auf das elektrische Verhalten von Graphen auf einem isolierenden Substrat wird untersucht und eine neue Methode zur Kontrolle auf Waferebene angewendet. Darüber hinaus wurde die Leistungsfähigkeit von Anwendungen auf Graphenbasis am Beispiel des Hall-Sensors mit verschiedenen Integrationsansätzen untersucht und mit herkömmlichen Anwendungen auf Siliziumbasis verglichen. Schließlich wurde ein Prozessablauf für die Herstellung von Graphen-basierten Hall-Sensoren und Teststrukturen in einer CMOS-kompatiblen Halbleiterfertigungsumgebung unter Verwendung von nanokristallinem Graphit entwickelt und die hergestellten Strukturen wurden elektrisch und optisch untersucht.

Contents

List of Abbreviations

2D	Two Dimensional
AFM	Atomic Force Microscopy
AMR	Anisotropic Magnetoresistance
Al	Aluminum
ALD	Atomic Layer Deposition
APCVD	Atmospheric Pressure Chemical Vapor Deposition
ASIC	Application-Specific Integrated Circuit
ASIL	Automotive Safety Integrity Level
BEOL	Back-End-of-Line
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical Mechanical Polishing
CV	Capacitance-Voltage
CVD	Chemical Vapor Deposition
DHF	Diluted Hydrofluoric Acid
DI	Deionized
EBSD	Electron Backscatter Diffraction
EDX	Energy-Dispersive X-Ray
FEOL	Front-End-of-Line
FET	Field Effect Transistor
FIB	Focused Ion Beam
GF	Gauge Factor

GMR	Giant Magnetoresistance
HTO	High-Temperature Oxide
HEMT	High Electron Mobility Transistor
LCR	Inductance-Capacitance-Resistance
LPCVD	Low-Pressure Chemical Vapor Deposition
LSM	Laser Scanning Microscopy
MEMS	Micro-Electromechanical Systems
MMA	Methyl-Methacrylate
NEMS	Nano-Electromechanical Systems
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PVD	Physical Vapor Deposition
RH	Relative Humidity
RIE	Reactive Ion Etching
RPT	Rapid Thermal Processing
SDT	Semidry Transfer
SEM	Scanning Electron Microscopy
SPV	Surface Photo Voltage
TEOS	Tetraethylorthosilicate
TLM	Transfer Line Method
THz	Terahertz
THz-TDS	Terahertz time-domain-spectroscopy
TMR	Tunnel Magnetoresistance
TRT	Thermal Release Tape

TXRF	Total Reflection X-ray Fluorescence
WT	Wet Transfer
XPS	X-ray photoelectron spectroscopy

1. Introduction

1.1 Motivation

Since its discovery in 2004 by Geim and Novoselov [1], graphene has been the focus of current worldwide research [2], as it exhibits special physical properties due to its chemical structure, e.g. high charge carrier mobility [3]–[9] compared to conventional material systems like GaAs and InAs [10], [11], high thermal conductivity [12], high mechanical stiffness [13], etc. This leads to a variety of applications with graphene as an active element, e.g. for high-frequency transistors [14] and Hall sensors [3]–[9] due to the high charge carrier mobility, for heat spreader in hotspot areas [15], for membranes for loudspeakers, microphones, and pressure sensors for improved acoustic quality and electrical sensitivity [16]. For the realization of these graphene-based devices, it is necessary to produce them in high volumes with high throughput and reproducibility. In the semiconductor industry, this is realized by the fabrication of these devices on base-material wafers (silicon, III-V semiconductor, etc.) up to a size of 300 mm and more. Therefore, it is necessary to integrate graphene into these industrial semiconductor processes to ensure commercialization by high volumes at a competitive price. Integration means the transfer of graphene into existing semiconductor processes and technologies so that new processes and technologies for graphene devices are not required. An important factor for integration is complementary metal-oxide-semiconductor (CMOS) compatibility with conventional semiconductor technologies. In general, CMOS compatibility is conformity with the requirements for the production of integrated digital and analog circuits (e.g. concerning contamination class), which are necessary for device functionality and control. To guarantee these requirements it is important to ensure the CMOS compatibility of processes which are currently used for the production of graphene-based applications for research and development. Material systems for the realization of high performance graphene-based devices [11] are in many cases cannot be used in classical semiconductor fabrication lines due to their contamination class, industrial availability and price. These critical points are the motivation of this work, which focuses on the integration of graphene into industrial processes and the control of the properties of graphene-based applications with conventional semiconductor process methods that ensuring CMOS compatibility. The term graphene in this work only focusing on monolayer graphene and its integration and not on bilayer or multilayer graphene. In addition, the focus is on one of the current critical steps for graphene integration, the transfer from the growth substrate (usually a metallic substrate) to an industrially grown target substrate (e.g. SiO_2) with

respect to contamination, handling and scalability (chapter 3.1). Furthermore, semiconductor-compatible processes are investigated, which can be used for the specific functionalization of graphene-based devices and are applicable on wafer level (chapter 3.2). In addition to the integration approaches, it is also necessary to investigate fabricated graphene-based applications (in this case Hall sensors) with industrial processes regarding their performance and electrical quality of the material system, which is also a part of this work (chapter 4). Finally, a process flow is developed using existing semiconductor processes for wafer-level integration of graphene-based Hall sensors and the verification of its feasibility (chapter 5).

1.2 Content of the work

This work is divided into five main chapters, which are summarized below:

Chapter 2: In this chapter, the basics are about the electrical properties and physics of graphene, and its potential application fields are discussed. The objective of this chapter is to establish the basis for the later discussions in the experimental part.

Chapter 3: In this chapter, the integration of graphene into industrial semiconductor processes is investigated. The focus of chapter 3.1 is the realization of the transfer of graphene from its growth substrate to a target substrate at the wafer level. A process window for an automatable wafer bonding process is determined and subsequently, a corresponding wafer-level transfer tool is designed and developed for implementation. Transfer experiments were performed with an in-house built transfer tool from 6-inch graphene to 8-inch SiO_2/Si wafer and were optically and electrically analyzed and compared with wet transferred graphene at wafer level as a reference. In chapter 3.2 a methodology is investigated for the control of the electrical properties of graphene on an isolating substrate. This is done by the introduction of aluminum and ammonia in SiO_2 to form negative and positive ionic charges on the SiO_2 surface for the control of the electronic properties of graphene. The transferred graphene onto the isolating substrates is electrically characterized to measure the impact of the surface charge on the charge carrier density and charge carrier mobility in graphene and the impact on the contact resistance from graphene to nickel electrodes.

Chapter 4: In this chapter, the performance of graphene-based devices is investigated. The focus is on graphene in a Hall sensor application, as they outperform commercial Hall sensor material

systems in terms of magnetic sensitivity due to the high charge carrier mobility in graphene. In chapter 4.1, the approach was chosen to produce a free-standing graphene membrane as a Hall sensor, since it has been shown that undisturbed graphene is closer to the electrical properties of the theoretical value than supported graphene. Chapter 4.2 focuses on the integration of graphene into a classical silicon-based Hall sensor material system to investigate the performance of graphene-based Hall sensors in this environment.

Chapter 5: In this chapter, a process flow is developed and realized to ensure the fabrication of graphene-based devices at the wafer level in high volumes. This is done with thin graphite layers instead of graphene, since the development and optimization of processes on graphite, which has surface properties very close to those of graphene, accelerates the implementation in semiconductor manufacturing due to its availability. The process flow can also be directly applied to graphene after the process optimization on thin graphite layers.

2. Foundation

Graphene exhibits excellent electronic properties and is therefore a promising candidate for future electronic applications. Graphene consists of only one atomic layer of carbon atoms connected by covalent bonds in an sp^2 configuration, forming a two-dimensional hexagonal crystal lattice with two carbon atoms per unit cell. The π-orbitals of the carbon atoms are oriented perpendicular to the sheet plane, resulting in an atomic layer thickness of 0.34 nm [17]. The band structure in graphene has a uniqueness at the corners of the Brillouin zone at the K and K' points where the conduction and valence bands touch, which are called Dirac points due to the linearity of the dispersion relation at these points [18].

This chapter contains information about the electrical properties and physics of graphene and its potential application fields. The objective of this chapter is to establish the basis for the later discussions in the experimental part (chapters 3, 4, and 5).

2.1 Electrical properties of graphene

Suspended graphene exhibits extremely high electron mobility up to 200,000 $cm^2/V{\cdot}s$ at room temperature [19] and similar values were also achieved for encapsulated graphene with hexagonal boron nitride (h-BN) [11]. The massless electrons in the π-bonded, non-hybridized orbitals are responsible for these values. The band structure in graphene has a linear shape near the Dirac points, and the conduction band and the valence band are symmetrical. Therefore, for low-energy excitations, the properties of electrons and holes are identical, except for the sign of their charge.

If graphene is on a carrier substrate and non-encapsulated, the electronic properties of graphene are influenced by the surface of the substrate (e.g. SiO_2) and adsorbed molecules [20]. The surface charge density of the substrate and the molecules affects the Fermi energy in graphene through charge transfer doping, which modifies the doping level in graphene and thus its electrical properties. In the case of a positive surface charge density of the substrate, charge transfer doping generates a negative mirror charge in the graphene layer, which leads to a local increase of the Fermi energy and hence to a higher electron doping. In addition, the ballistic transport of electrons in CVD graphene is limited by lattice defects and grain boundaries during growth. As a consequence, the electron mobility in graphene on SiO_2 is in many experiments far below the

value of suspended graphene, in the range of around 1,500 $cm^2/V \cdot s$ [21]–[23]. As a result, the type of substrate and the graphene synthesis method are directly influencing the electrical performance.

The electronic properties can also be manipulated by externally applied electric fields via the electric field effect. Here, Fermi energy in graphene is energetically increased and decreased via an applied electric field, depending on the sign of the electric voltage. For this purpose, the graphene must be separated from the counter electrode via an isolator. This allows the determination of the absolute charge carrier concentration and its sign.

2.2 Potential application fields of graphene

Due to the vanishing band gap and the high charge carrier mobility of graphene at the Dirac point, and also its high sensitivity to atmospheric conditions, graphene is predestined for its use as a field effect transistor (FET), a Hall sensor, and a gas sensor. Also due to its high thermal conductivity, graphene can be used as a heat dissipation layer in hot spot regions of devices to increase its lifetime. Furthermore, graphene is suitable as a membrane material due to its 2D character with high mechanical stability and can be used as an active element for microphones, loudspeakers, accelerometers, pressure sensors, etc. In the following, the applications that were used as examples in this thesis are discussed and the advantages of graphene compared to conventional technologies are highlighted. To complete the picture, graphene is also discussed as an active element in the transistor, as this application also promises significant potential, but is not investigated in this work.

Hall sensors

Hall sensors are widely used for low-power applications in industry and are integrated by CMOS technologies to be cost-effective with high performance [24], [25]. Compared to magnetic sensor technologies based on magnetic resistivity effects like AMR (anisotropic magnetoresistance), GMR (giant magnetoresistance), and TMR (tunnel magnetoresistance), the Hall effect sensor technology is linear in a wide range of magnetic field strength and can therefore be used in a wide dynamic range of flux density in an open loop configuration [26].

There are many application fields for Hall sensors, especially in the automotive industry, where they are used for robust replacement of potentiometers, linear and angular position sensors, and ASIL (Automotive Safety Integrity Level) applications such as the position of throttle and pedal and steering torque sensing [27]. The important parameters for Hall sensors are the temperature stability, sensitivity, and magnetic offset of the Hall element, which is a thin semiconductor plate with a Greek-cross-shaped geometry [25]. In general, Hall sensor technologies can be classified into two groups, the first one with a monolithic silicon-based Hall plate integrated with CMOS compatible integrated circuit based on silicon for data processing (ASIC: application-specific integrated circuit), often combined with ferromagnetic concentrators, and the second one with III/V semiconductors as a Hall plate connected to the ASIC [26]. The ASIC can either be integrated directly with the Hall plate in case of CMOS compatibility or assembled via wafer bonding for non-CMOS compatible material systems.

The sensitivity S_v of Hall sensors is determined by the charge carrier mobility μ of the active sensor material ($S_v \propto \mu$) and its geometry ($S_v \propto L/W$), with L as the length and W as the width of the Hall plate. Silicon has at room temperature and a dopant concentration of 10^{17} cm^{-3} an electron mobility of approx. 1,241 $cm^2/V{\cdot}s$ [28], which is in comparison to III/V semiconductors like GaAs with 8,500 $cm^2/V{\cdot}s$ and InAs with 33,000 $cm^2/V{\cdot}s$ [10] approximately a factor 7 to 27 smaller. The detectability of monolithic silicon-based Hall sensors with a silicon-based ASIC is therefore limited to the microtesla range, whereas Hall sensors based on 2D electron gases have a detectability down to the nanotesla range [26].

The magnetic offset, which results from differences in current density distributions in the Hall plate [29] (e.g. due to non-symmetric Hall plate geometry or misalignments of sense contacts [30]), is in the range of millitesla for silicon-based Hall plates and 2D Hall plates in the submillitesla and millitesla range [26]. This offset can be reduced by using the spinning-current modulation technique, in which the bias and current of Hall plate contact pairs are very fast exchanged through the measurement. A reduction of the magnetic offset with the spinning-current method down to microtesla ranges is therefore realizable [26].

A third important parameter for Hall sensors is temperature stability, which is dependent on the material of the Hall plate. They can be categorized into two groups, small-band gap materials with a high-temperature dependence and wide-bandgap materials with medium-temperature dependence. Small band gap materials (e.g. InSb or InAs) have a higher sensitivity than wide band gap materials (e.g. GaAs) due to the influence of temperature on the charge carrier concentration and mobility. [30]

Graphene as an active element for Hall sensors shows charge carrier mobilities of approximately 20,000 $cm^2/V{\cdot}s$ on SiO_2 and of approximately 200,000 $cm^2/V{\cdot}s$ as a free-standing membrane and outperforms silicon-based Hall plates with a factor of around 16 to 160 in sensitivity with the same sensor geometry [19]. It also outperforms the charge carrier mobility of GaAs and InAs and can furthermore be implemented with CMOS compatible processes [16] and can be integrated as for silicon-based Hall plates without the necessity of wafer-bonding like non-CMOS materials (GaAs, InAs). Also, the offset of graphene-based Hall sensors is in the range of silicon-based ones [16] and can also be reduced by using the spinning-current method as for conventional Hall sensors.

Membrane-based applications

Membrane-based applications are widely used for the conversion of an external stimulus into an electrical signal and are included in the field of micro- and nano-electromechanical systems (MEMS/NEMS). Applications such as microphones, pressure sensors, accelerometers, and mass and gas sensors use this principle [19] and are applied in many application fields such as the industry and the consumer market [31]. In most applications, the readout is done with an electrical transduction mechanism, because it is easy to integrate into practical membrane-based sensor devices [19].

The major electromechanical transduction and readout techniques applicable to 2D material membrane-based sensors are piezoresistive readout, transconductance readout, and capacitive readout [19]. The advantage of graphene compared to conventional silicon-based membranes is that the membrane thickness can be scaled down to one atomic layer due to the high stiffness of graphene, resulting in increased sensitivity for a small stimulus (e.g. small pressure differences). However, not all transduction mechanisms are suitable for graphene-based membrane applications, as their electrical material properties are not suitable for all types of mechanisms. For example, in the piezoresistive readout, the gauge factor (GF) is a measure of the transduction efficiency of the membrane deflection into an electrical signal [19]:

$$\mathrm{GF} = \frac{\Delta \mathrm{R}/\mathrm{R}}{\Delta \mathrm{L}/\mathrm{L}} = 1 + 2\nu + \frac{\Delta\rho/\rho}{\varepsilon} \qquad 1\text{-}3$$

It is dependent on the ratio of the change of electrical resistance ΔR to the change in mechanical strain $\Delta\varepsilon = \Delta L/L$, and its geometric deformation is given by the term 1+2ν, with ν as Poisson's ratio [19]. Compared to silicon with a gauge factor of -100 to 200 [32], graphene has a gauge factor of only 2 to 6 [33]–[36] and is about a factor of 30 less sensitive. As an alternative to

graphene, 2D materials like $PtSe_2$ and MoS_2 [37], [38] show gauge factors compared to silicon [39]–[42].

In the capacitive transduction mechanism, the capacitive C is indirectly proportional to the membrane deflection δ $(C = A\varepsilon_0/(h - \delta))$, and therefore the responsivity $\Delta C/\Delta\delta$ scales with $A\varepsilon_0/h^2$, with h as the distance of the membrane to the counter electrode [19]. The responsivity increases with increasing membrane area A and with decreasing distance h to the counter electrode. But the feasibility of such structures is not always technologically possible, since small membrane distances to the counter electrode are not easy to produce with increasing membrane area [19], [43]. The sag of the membrane due to its weight or due to mechanical stress also plays an important role, so small distances cannot always be realized. Similarly, a smaller distance h leads to a reduction of the maximum membrane deflection and thus to a reduction of the dynamic pressure range for operation [19]. Graphene and other 2D materials have a low inertia due to their atomic thickness and are therefore deflected by small dynamic or static pressure changes, resulting in an electrical sensor signal.

As the third most common transduction mechanism, the change of conductivity in the membrane is measured by its deflection. The measurement principle is based on a three-terminal geometry, in which the membrane is connected with two terminals (Source and Drain) and with a third terminal as the counter electrode (Gate). When the membrane is deflected by an external force, the charge in the membrane is changed by its displacement to the gate electrode $(Q = C \cdot U)$, which results in a change of the charge carrier density and therefore in a change of the conductivity. This electrical readout mechanism is therefore very sensitive for 2D membranes (e.g. graphene) [37], [38]. [19]

Transistors (FETs)

Transistors are commonly used as a switch or an amplifier for the realization of digital and analog electronics and have a variety of application fields [44], [45]. Important electrical parameters for transistors are the switching speed, i.e. the time in which the transistor can be switched on and off, and the power that a transistor can transport.

Transistor channels based on 2D materials cannot transport high power $(P = R \cdot I^2)$, because of its two-dimensionality the current density j is very high $(j = I/A)$, with A as the cross-section area, for small currents. This high current density generates a high amount of heat, which leads the 2D

material to heat up very fast to its melting point, because of its small thermal mass, which destroys the material and therefore the channel.

In the case of the switching speed of transistors, there are two important figures of merit, the cutoff frequency f_c and the maximum frequency of oscillation f_{osc}, which are given by the following equations

$$f_c = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \quad 1\text{-}1$$

$$f_{osc} = \frac{g_m}{4\pi C_{GS}\sqrt{g_{DS}R}} \quad 1\text{-}2$$

with g_m as the transconductance parameter, g_{DS} as the channel conductance, C_{GS} and C_{GD} as the capacitance between gate/source and gate/drain terminals and R as the induced gate charging resistance by electric field [45]–[47]. The cutoff frequency and the maximum frequency of oscillation are proportional to the charge carrier mobility of the semiconducting device and inversely proportional to the channel length. The direct proportionality of the two figures of merits (f_c and f_{osc}) to the charge carrier mobility shows that graphene-based transistors can be used in the field of high-frequency electronics since the theoretical charge carrier mobility is greater than that of other electron gases [3]–[10]. In previous works, it has been demonstrated that monolayer graphene transistors have cut-off frequencies in the range of 14.7 GHz to 500 GHz at different channel lengths [47]–[53] and this value is comparable with that of InP and GaAs high electron mobility transistors (HEMTs) [54], [55]. Moreover, it was reported that the maximum frequency of oscillation for graphene-based transistors ranges from 30 GHz to 200 GHz and shows, therefore, lower values compared to silicon-based transistors [47]. The reason for this is the increasing channel conductance in graphene-based transistors by an increasing channel current through high drain-source voltages caused by interband tunneling and the quasi-ballistic nature of carrier transport in graphene [46]–[48], [56]. [57]

An additional important electronic parameter of transistors is the on-to-off current ratio, which is the ratio of the on-state and the off-state current without any applied gate voltage. A large value of this ratio indicates a high performance with a low leakage current, which is a required property for transistors [45]–[47]. For modern digital electronics, a large on-to-off current ratio is necessary (10^3 to 10^4) [58] and is scaling with the electronic band gap of the semiconducting device [46], [47], [59]. This parameter shows that monolayer graphene with its vanishing bandgap is not predestined for use as a transistor for digital applications. However, for high-frequency electronics, not such a high value for the on-to-off current ratio is required and enables graphene as a potential base material [56], [60]. [57]

3. Process development for graphene integration

This chapter focuses on processes for the integration of graphene into CMOS-compatible device environments. Chapter 3.1 contains a methodology to transfer graphene from its growth substrate to a target substrate (SiO_2), considering CMOS compatibility and industrial realization. In chapter 3.2, a method is presented to control the electrical properties of transferred graphene on an isolating substrate using established semiconductor processes. The objective here is to define electrical areas (active electrical area, passive contact area) by modifying SiO_2 layers, which are dependent on the field of application.

3.1 Wafer-scale transfer of graphene

To produce graphene-based applications, it is necessary to remove graphene from its growth substrate (e.g. metal-catalyst like copper [61], [62]), and transfer it to a substrate that will serve as a handling wafer in the subsequent integration process. Defects in graphene or undesirable changes in intrinsic material properties during the transfer must be avoided. There are different strategies to transfer graphene from its growth substrate to a target substrate [63], [64], but it can be concluded that a controlled manipulation (defects, contamination) of the graphene by the available transfer methods is not yet possible. Depending on the transfer method, for example, the electron mobility of the graphene can vary from 350 cm^2/Vs to 7,100 cm^2/Vs [63]. In addition, the transfer process must be scalable, free of metallic and organic contaminations, and automatable.

For the realization of a wafer-level transfer method, which meets these requirements, it is necessary to use a growth substrate for graphene, which is not metallic, e.g. sapphire. It has been shown that on sapphire single layer graphene can be grown with a high charge carrier mobility, and therefore free of any metallic contamination. Furthermore, the growth is scalable up to the current requirements of the semiconductor industry [65]. However, sapphire growth has a disadvantage compared to metallic growth substrates, which is not based on physical properties or feasibility, but rather the cost factor of this methodology, which is not negligible on an industrial scale. Since metallic substrates are significantly more economical than sapphire regarding costs,

the transfer process of graphene from metallic substrates instead of sapphires will be investigated in the following.

Copper is presently used as a growth substrate because graphene can be deposited on it as also other metal substrates in high quality over its entire surface [64], [66], [67]. For the chemical vapor deposition (CVD) of graphene, a copper foil is used instead of the standard copper thin film technology, which is used in the semiconductor industry. Graphene, deposited on copper foil by chemical vapor deposition, shows a high quality comparable to exfoliated graphene [67]. The reason for this is the size of the individual grains of copper. The copper foil has higher crystal sizes compared to copper deposited by thin-film technology [68]. For chemical vapor deposited graphene on copper, crystal sizes of copper are mirrored to the grown graphene. Since grain boundaries between the crystals of copper substrates and therefore of graphene are defects, graphene on copper foil has fewer defects and therefore better properties due to larger crystal sizes [69]. In this work, graphene is used as the starting material, which has been deposited on a copper foil that was purchased from Graphenea. The dry transfer was chosen as the transfer method since it is easier to control during transfer due to the use of carrier wafers compared to wet transfer, and therefore more automatable. An important factor during dry transfer is the adhesion of graphene to the target substrate. The adhesion work of graphene to the carrier must be overcome during dry transfer to detach the graphene from it to the target substrate. The adhesion of graphene is dominated exclusively by Van-der-Waals forces [70]. [71]

It has been demonstrated in previous works that wet transfer of graphene is a method to transfer it from a growth substrate to a target substrate with good electrical quality [72]. This approach works to a certain degree of scaling, but the handling of this process at the wafer-level causes defects during transfer [73]. Therefore, it is necessary to use a methodology that transfers the graphene from its growth substrate to the target substrate without defect formation during handling and without the problem of wafer-level scalability. Here, the approach of wafer bonding for dry transfer was used, i.e. pressing graphene on a carrier wafer onto the target wafer. The method of wafer bonding is standard in the semiconductor industry and is therefore a promising method to transfer graphene onto the target wafer. Therefore, a transfer tool will be constructed that enables the wafer bonding approach for the dry transfer of graphene. Before the construction phase, a possible process window is determined at the chip level to define the requirements for the transfer tool. In addition, different carrier materials are used for graphene transfer and their suitability is assessed. [71]

3.1.1 Definition of a process window for dry transfer

In this chapter, a process window for dry transfer is determined. Only thermal release tapes (TRT), PMMA (Polymethyl methacrylate), and a combination of both materials were used. For the experiments, a Thermal Release Tape from Nitto Denko Revalpha was used (Part No. 3198MS), with an adhesion of 2.5 N per 20 mm in width and a release temperature of 120 °C. In all experiments, a 300 nm thermal silicon dioxide on silicon was used as the target substrate. For experiments on the chip-level, the maximum transferred graphene area was 2.24 cm^2 by using a wafer bonder M6 from Karl Süss. For surface functionalization of the target substrate (SiO_2), the parameters of oxygen plasma treatment (power, oxygen flow, etc.) for hydrophilization were not changed during all experiments. Samples were pre-treated with a wet cleaning step to remove polymer residues from the graphene. This consists of acetone, isopropanol, and water treatment. The samples were then heated at 400 °C in a nitrogen atmosphere for two hours to remove residual liquid media from the pre-treatment. This process step was not changed during the experiments and is also referenced as a standard cleaning step. The consideration of yield of the transfer result is divided into macroscopic and microscopic levels. The term macroscopic is used when the investigated area is in the order of millimeters to centimeters. In contrast, the microscopic term is used to refer to the order of magnitude of a few micrometers. This area can therefore be assessed with a laser scanning microscope. To evaluate the transfer at the atomic-level, Raman spectroscopy measurements were performed on the transferred samples to conclude defects during the transfer process [74]. In the following, contact angle measurements were done to determine the surface energy of the used materials during transfer, to be able to assess the feasibility and quality of the transfer. [71]

3.1.1.1 Contact angle measurements to determine the surface energy of the transfer materials

With the use of contact angle measurements and the resulting surface energies, statements can be made about the adhesion work that has to be applied to separate two solids from one another. Since adhesion is an important factor in the dry transfer process, as it determines the transfer quality, this measurement can be used to determine the feasibility of the transfer process. The theoretical basis for determining the surface energy is described in appendix A1. Here, only the

results of contact angle measurements and the resulting surface energies of the used materials are considered. Table 3-1 shows contact angles determined with water and diiodomethane as test liquids as well as surface energies, which were calculated out of them.

Table 3-1: Surface energies of the used materials, determined from contact angle measurements of water and diiodomethane.

Material	**Contact angle in [°]**		**Surface energy [mN/m]**		
	Water	Diiodomethane	polar portion	dispersive portion	total
Graphene on copper	76.6	40	8.32	35.73	79.79
Copper	92.8	37.8	1.46	38.27	78.00
SiO_2 (with O_2 plasma treatment)	7.40	51.40	42.90	29.51	101.93
SiO_2 (w/o O_2 plasma treatment)	34	48.50	32.08	31.08	94.23
Thermal Release Tape	87.3	57.80	5.9	28.85	34.79

From Table 3-1, the following conclusions can be made: Graphene is hydrophobic since the dispersed part of the surface tension predominates over the polar part. Oxygen plasma treatment of SiO_2 makes it highly hydrophilic, recognizable by the small contact angle of water compared to untreated SiO_2 and by the increase in the polar fraction of surface energy. The polar surface energy of SiO_2 changes from 32.08 mN/m to 42.90 mN/m and dispersive surface energy remains almost constant, but with an overall small change in total surface energy from approx. 8 % from 94.23 mN/m to 101.93 mN/m. This suggests that oxygen plasma treatment has a rather small influence on the adhesion energy between silicon oxide and graphene because it is expected that a relatively small change in the total surface energy of SiO_2 leads to a slight change in adhesion energy. To enhance the adhesion between hydrophobic graphene and SiO_2 a rather increase of the dispersive part would be necessary. SiO_2 has a higher total surface energy than the thermal release tape after release. Due to this difference, the adhesion of graphene to SiO_2 will be higher than to the thermal release tape. Therefore graphene should be well transferable from release tape to SiO_2 [75].

The adhesion of graphene to copper is greater than that of graphene to the thermal release tape because the total surface energy of copper is greater than that of the tape. This indicates that dry transfer with the Thermal Release Tape as a carrier is not feasible. Therefore, the dry transfer should leave graphene on the original copper substrate after the mechanical removal of the tape. It should be noted, that this is only an estimation of the adhesion, as it is not measured directly, but can be interpreted indirectly via the surface energy of the material surfaces.

3.1.1.2 Determination of the process window for the transfer process

For the evaluation of the influence of various transfer sub-processes (lamination of copper foil with graphene on thermal release tape, copper removal, and transfer of graphene on the tape to the target substrate), it is necessary to investigate the transfer after each process step. The transfer process is a sequence of three adjacent black boxes (1: laminate graphene on copper foil to thermal release tape, 2: copper removal, 3: transfer of graphene from tape to target substrate). However, a major problem arises when graphene is on the thermal release tape, as neither optical microscope analysis nor Raman analysis is useful here, as the tape produces low contrast of graphene and the Raman spectrum of the tape overlay with that of graphene, making it impossible to evaluate the transfer from point 2. During the dry transfer, copper is mechanically removed after transfer to the thermal release tape at point 2. Since this process is not optimized, graphene transfer cannot be guaranteed with high quality and yield. Therefore, only the semidry transfer (the term semi because of wet chemical copper etching) process will be evaluated in the following, since copper removal is carried out wet-chemically, and this has already been evaluated and optimized from previous works.

In the following, the process window for the semidry transfer process is evaluated. The copper removal was conducted wet chemically with a 0.1 molar ammonium persulfate solution, followed by cleaning in a water bath. The bonding processes were carried out at room temperature, and the target substrate was treated with oxygen plasma to remove contaminants in all experiments. The influence of oxygen plasma on surface energy is low (Table 3-1 in chapter 3.1.1.1) and should have therefore no large effect on transfer quality. It should also be noted that the back side of copper foil was not further processed to remove graphene/carbon residues. Therefore, remaining graphene flakes on the backside from the CVD growth process may influence the quality of the transfer, as these can be deposited on graphene on the top side during copper etching.

The quality of the transfer is evaluated using laser scanning microscopy with a microscope from Olympus (OLS4000) in combination with the image processing software *ImageJ*. For this purpose, the optical image was converted into a black-and-white image, and the threshold value for the black-and-white conversion was adjusted in such a way that graphene differs from the target substrate. The black or white portion of the image was then determined with an error of approx. 5 %. Raman spectroscopy with a self-made in-house tool at a wavelength of 532 nm, a power density of 12.56 $\mu W/\mu m^{2,}$ and an integration time of 80 s was also used to investigate the transfer of the graphene layer on a microscopic level. The number of layers was extracted from the

intensity ratio of I_G/I_{2D}, and the defect density from the intensity ratio I_G/I_{2D}. For the investigation of the effect of the pressure of bonding step 1, the pressure for bonding step 2 is kept constant at 4 N/mm². This value for the second bonding step was chosen because a too-low bonding pressure probably leads to poor adhesion between graphene and the target substrate and thus the influence of the first bonding step cannot be evaluated.

The individual tests for determining the process window are listed below:

- Bonding step 1 (graphene on copper foil on thermal release tape) is varied from 0.5 to 4 N/mm^2, while bonding step 2 (graphene on TRT on target substrate) is kept constant at 4 N/mm^2
- After identification of the optimal pressure during the bond process 1, this value is kept constant and bond process 2 is varied from 1 to 5 N/mm^2
- The time for the bonding steps was in all experiments 10 min
- The temperature was kept constant at room temperature during all process steps and raised to 150 °C for the release process
- The system atmosphere during bonding was nitrogen

Bonding step 1: Graphene on copper foil onto thermal release tape

Figure 3-1 a) contains the yield of the graphene layer after transfer to the target substrate SiO_2, which was determined by optical contrast. On average, the amount of transferred graphene is in the range of 70 to 80 %, which indicates that the bonding pressure for the lamination of copper foil with graphene on thermal release tape is not critical for the transfer of graphene during this bonding process.

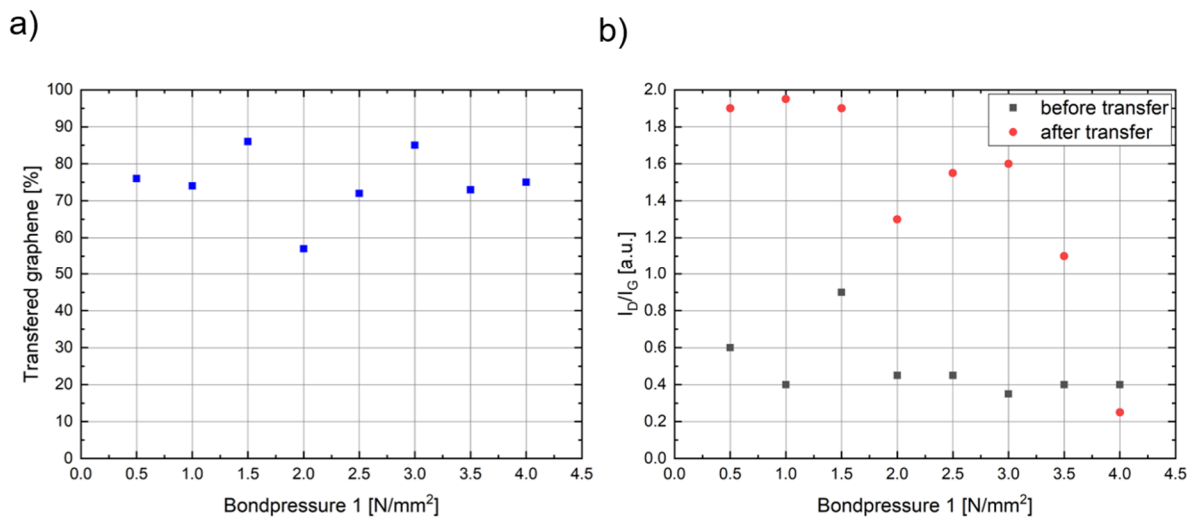


Figure 3-1: Evaluation of transfer quality with the variation of bond pressure in bonding step 1. a) Yield in percent of transferred graphene depending on the bond pressure at the first bonding step; b) Ratio of I_D/I_G as a function of the bond pressure at the first bonding step.

Figure 3-1 b) shows the dependence of the intensity ratio of I_D to I_G of the Raman modes of graphene, which are an indicator of defects and thus of the quality of the transfer [74] with different bonding pressures, before and after transfer. Before transfer, the I_D to I_G ratios are on average in the range of 0.4 to 0.6, but they increase after transfer. However, there is a tendency for the ratio of I_D to I_G to decrease with increasing bond pressures. This means that at bond step 1 the bonding pressure should be selected high to ensure the highest possible graphene transfer quality. In combination with the results shown in Figure 3-1 a), which indicate that the bonding step does not influence the yield of graphene transfer, it is necessary to select the bonding step high to ensure a high-quality (defect-free) transfer. The tendency that transfer quality regarding defects (determined from the I_D/I_G ratio) increases with increasing bond pressure can be explained by the transfer of the surface profile of the copper foil, which has a high waviness [76], into the thermal release tape. As the bonding pressure increases, the waviness is more and more reflected by the indentation in the thermal release tape, which is elastic, and therefore increases the contact area between graphene on copper foil and the thermal release tape. As a result, graphene which is in contact with the thermal release tape is not damaged during copper etching due to the lack of support of the carrier layer. However, it should be noted that this statement is not verified by analysis and is only concluded from the tendency of the measurement results, which shows that defects of transferred graphene decrease with increasing bonding strength. For the investigation of the effect of the bond pressure of bond step 2, the value for bond step 1 is kept at 4 N/mm², since the highest transfer quality was observed at this bond pressure.

Bonding step 2: Graphene on thermal release tape onto SiO_2

The results of the dependence of bond force at bond step 2 with the yield of transferred graphene on SiO_2, which were determined by contrast measurements, are shown in Figure 3-2 a). It can be seen that the transfer yield of graphene on SiO_2 is in the range of 80 % up to nearly 100 %. However, there is no tendency of a bond force to graphene coverage on SiO_2 from these measurements, because they show similar values in all experiments. The quality of transferred graphene regarding defect density is shown in Figure 3-2 b) as a function of bonding force. However, no tendency of I_D/I_G ratio with the bond force of bond step 2 can be detected. In addition, the I_D/I_G ratios are on average lower after transfer than before transfer, which is because the measured graphene area with Raman spectroscopy before the transfer is not the same as after transfer due to the small measuring area of the Raman system. The low I_D/I_G ratio is consistent with the results from Figure 3-1 b), because the bond pressure of 4 N/mm² in bond step 1 also showed a low I_D/I_G ratio.

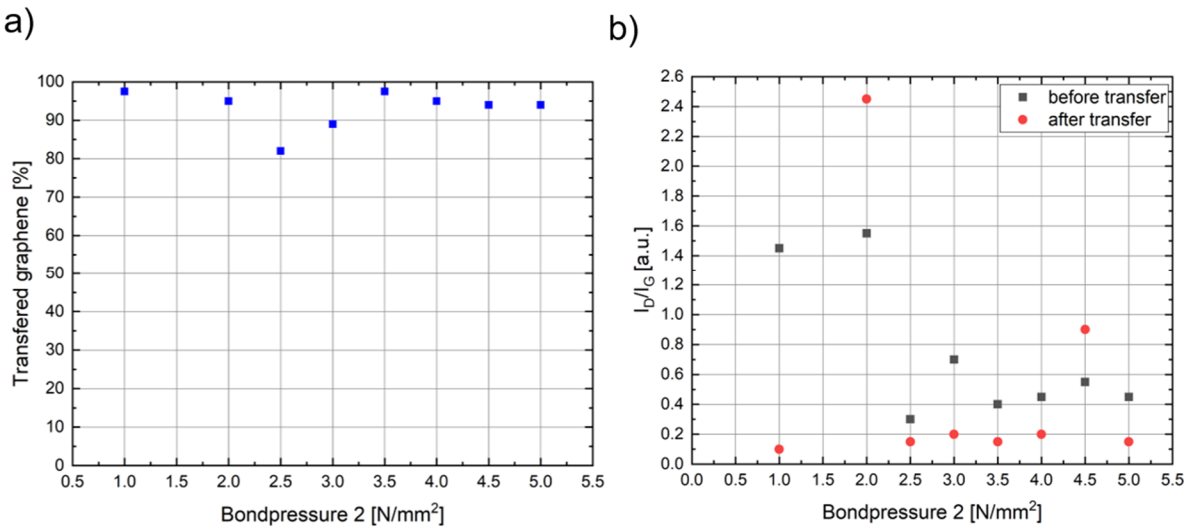


Figure 3-2: Evaluation of transfer quality with a variation of bond step 2. a) Yield in percent of transferred graphene depending on the bond pressure at the second bonding step, b) Ratio of I_D/I_G as a function of the bond pressure at the second bonding step.

This indicates that the quality of transferred graphene about defects at a microscopic level is largely determined by bonding step 1 and not by bonding step 2. The huge difference in I_D/I_G ratio for bond pressures at 1 N/mm², 2 N/mm², and 4.5 N/mm² do not match with this tendency, and can only be concluded that the measurement regions for Raman analysis were different. Therefore, the results for these bond pressures (1 N/mm², 2 N/mm², and 4.5 N/mm²) have to be doubted and are not taken into account for the conclusion that bond step 2 has a minor influence

on the defect density on a microscopic level of transferred graphene. Based on these results at the chip-level it can be concluded that the bond pressure must be in the range of 4 N/mm^2 and higher for a high-quality transfer of graphene from copper foil to the target substrate (SiO_2).

3.1.2 Development of a wafer-level semidry transfer tool

Based on the results from chapter 3.1.1, a transfer tool is constructed that has the requirements for transferring graphene from its growth substrate (copper foil, sputtered copper, etc.) to any target substrate through the use of a polymer carrier (thermal release tape). In the preliminary tests at the chip-level, a transfer tape with an adhesion of 2.5 N per 20 mm in width was used, i.e. with the lowest available adhesion from Nitto. Adhesion is a factor in the development of the transfer tool, as it is dependent on the thermal release tape and on influences of temperature, bond force, and atmosphere, which are purely set by the transfer tool. The requirement on the transfer tool is therefore that a high force must be applied to the sample during the bonding step 1 (4 N/mm^2) and the temperature of the base plate must heat the sample after bonding step 2 to the required release temperature (max. 200 °C, as this release temperature is maximal for the thermal release tape portfolio of Revalpha) to reduce the adhesion of the thermal release tape and to enable the transfer of graphene to the target substrate. Furthermore, the chamber of the transfer tool must be floatable with nitrogen to allow an inert atmosphere as in the preliminary tests. [71]

Accordingly, a wafer-level transfer tool is designed and manufactured to meet the above requirements. This is achieved by a mechanical press from Rotek, which serves as the basic framework for the transfer unit and guarantees at wafer level a mechanical pressure of up to 9.4 N/mm^2 on 200 mm wafer diameter, which exceeds the specifications from chapter 3.1.1, to compensate for necessary scaling effects of the transfer by higher bond forces. A mechanically strengthened precision hot plate from GMaier is used as the base plate, which can supply a maximum temperature of 230 °C to ensure the release of the thermal release tape. A stainless steel cylinder with a precision surface treatment to keep the surface roughness as low as possible is used as a stamp which serves as a counterpart of the base plate. The parallelism of the stainless steel cylinder, as well as the precision hot plate surface, are also taken into account, as these should be as parallel as possible, otherwise, the wafers can break during the bond process. [71]

To ensure an inert process atmosphere during transfer, a chamber consisting of Bosch profiles with reinforced glass walls and an aluminum plate on the backside is constructed around the hot plate and the stainless steel stamp. The spaces between the Bosch profiles and the walls are filled with silicone gel and cured to ensure impermeability. Two gas connections are installed on each side wall to purge the process chamber with inert gases to reduce humidity. The combination of gas inlets and the precision heating plate gives the possibility to control the number of adsorbed gas molecules on the target substrate, as well as on graphene on thermal release tape to control the adhesion properties of the transfer process. Additionally, the hydrophobicity of the substrates can be controlled, because the number of polar H_2O adsorbates on the substrate surfaces depends on the desorption rate R, which should be high to ensure a hydrophobic surface. To keep the desorption rate low, the temperature must be kept high ($R \propto \exp(-1/T)$), and the number of H_2O molecules n_{H_2O} in the process, the atmosphere must be kept low ($R \propto n_{H_2O}$) [77]. The process configuration consists of gas inlets, for the influence of the number of H_2O molecules in the atmosphere (N_2 purging), and the precision hot plate for the control of process temperature and the control of substrate hydrophobicity. [71]

To monitor the transfer process, a WIKA hydraulic sensor is used to control the mechanical process pressure, a GMaier temperature monitor device to control the temperature of the hot plate, and an Adafruit humidity sensor for an in-situ recording of humidity in the process chamber, which is positioned at the outlet of the process chamber on the aluminum plate at the back side of the chamber. Figure 3-3 a) shows the wafer-level transfer tool with the described components. [71]

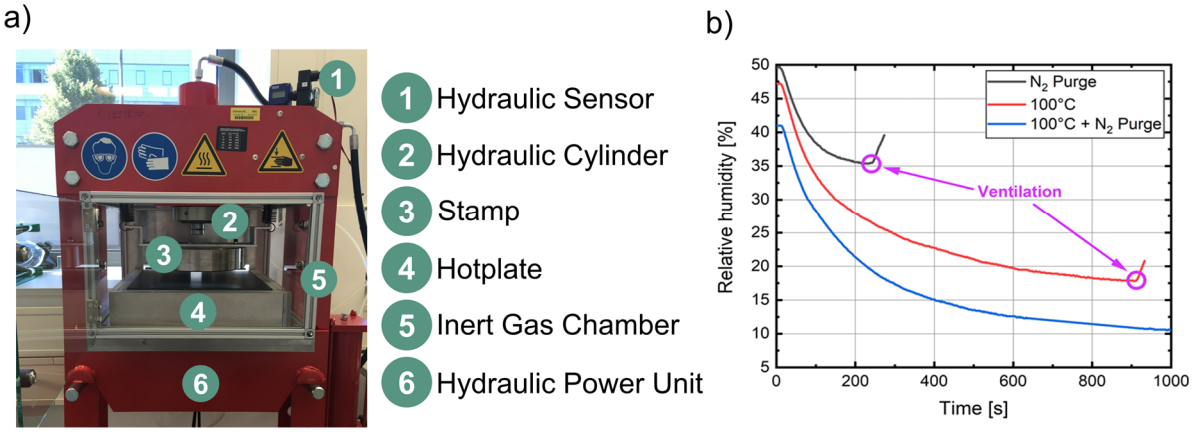


Figure 3-3: Wafer-level transfer tool with its specifications. a) Image of transfer tool for the dry and semidry transfer of graphene on a metallic substrate to any target substrate. b) Relative humidity in the process chamber with different process conditions.

The progression of relative humidity (RH) in the process chamber with nitrogen purge without a hot plate, 100 °C heating without nitrogen purge, and the combination of both are shown in Figure 3-3 b). During the heating process, the time starts when 100 °C is reached, without heating immediately when the nitrogen purge is switched on. It can be seen that the combination of heating at 100°C and nitrogen flux is the most efficient, as the humidity goes into saturation at very low values compared to the other two experiments. The bonding pressure during the heating process at 100 °C decreases with time, because of self-heating the hydraulic unit can no longer maintain stable pressure during the process. During the experiments, it has been seen that at bonding pressures of 3-4 N/mm^2, the reduction of the pressure with time is negligible. For all upcoming transfer experiments, 3 N/mm^2 was set as the maximum for a stable transfer process. Table 3-2 contains a list of the important specification parameters for the wafer-level transfer. [71]

Table 3-2: Specifications of the wafer-level transfer tool

	Specifications	
	Min.	Max.
Bond Pressure	-	9.4 N/mm^2
Temperature	23 °C (room temperature)	220 °C
Relative Humidity	10 %	50 % (atmosphere)

With the developed wafer-level transfer tool for the transfer from graphene on copper to a CMOS-compatible target substrate, wafer-level experiments were performed in chapter 3.1.3 and the quality of the transfer was analyzed regarding the amount of transferred graphene (optical contrast determination, similar to chapter 3.1.1.2), metallic contamination (total reflection X-ray fluorescence), carbon contamination of polymers (X-ray photoelectron spectroscopy) and electrical quality (Terahertz time-domain spectroscopy and electrical sheet-resistance-measurements).

3.1.3 Wafer-level transfer experiments

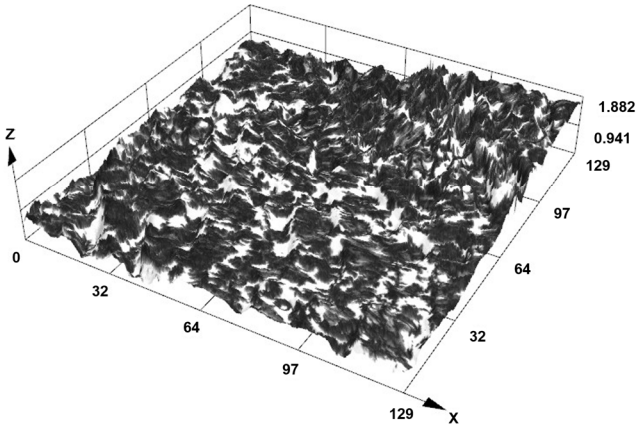
In this chapter wafer-level semidry transfer experiments were performed with graphene, which was supplied by Graphenea. The transfer process was conducted with the in-house developed wafer-level transfer tool from chapter 3.1.2 and with the use of the Thermal Release Tape from Nitto Denko Revalpha Part No. 3198MS, which was also used during the preliminary experiments in chapter 3.1.1.2. As a reference, a wafer-level wet transfer was also performed to evaluate the

quality of the semidry transfer process. Figure 3-4 illustrates the schematic process flow of the wet and semidry transfer process. [71]

Figure 3-4: Schematic process sequence for wet and semidry transfer at the wafer level.

Before the transfer experiments at the wafer level with graphene on copper were carried out, the starting material (graphene on copper) was first analyzed to be able to interpret the effect of the transfer on the graphene quality more precisely. In the beginning, the copper foil with graphene was analyzed with 3D Laser Scanning Microscopy to determine the surface structure of the copper foil with graphene and EBSD (Electron Backscatter Diffraction) measurements to determine the crystallite size and orientation of the copper foil. From the information of the EBSD analysis of the crystal size and orientation of copper, it is possible to conclude the crystallinity of graphene. The results of the measurements are shown in Figure 3-5.

a) 3D profile of copper foil with graphene



b) EBSD analysis of copper foil with graphene

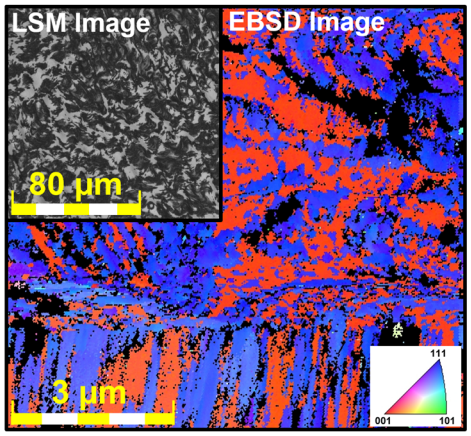


Figure 3-5: Optical analysis of the copper foil with graphene on top. a) 3D profile of the copper foil from laser scanning microscopy. b) EBSD analysis of the copper surface out of the area from the laser scanning microscopy image. It can be seen that the copper crystallite size is in the nanometer range.

The optical surface analysis was performed with a 3D laser scanning microscope from Olympus (OLS4000). Figure 3-5 a) shows the measured surface profile of the copper foil with graphene. It can be seen that the surface has a high surface topography, which confirms the assumption from chapter 3.1.1.2, where it was assumed that the copper foil has a high waviness. From the optical data, the surface roughness was determined with the software of the laser scanning microscope. The square roughness of the surface is on average 140 nm, which is in comparison to conventional substrates by three orders of magnitude larger [78] (see also chapter 3.2.1, Table 3-5). Thus the assumption from chapter 3.1.1.2, that the bond force during the bonding step of the copper foil with graphene onto the thermal release tape must be high to adopt the topography of the copper foil into the thermal release tape, is not unjustified.

Figure 3-5 b) shows the result of the EBSD analysis, which was carried out with an EDAX Pegasus EDX/EBSD system attached to a Zeiss Ultra55-FE-SEM. This shows that the crystallite size of the copper surface with graphene is in the nanometer range, and has, therefore, a high grain boundary density. This result indicates that the individual graphene domains on the copper foil are not cross-linked over a large area. The grain boundary edges in the graphene layer are more susceptible to external influences such as mechanical in-plane stresses (e.g. from the bonding process), which can result in a transfer of graphene to the target substrate in small flakes instead of large flakes.

Since the base material (graphene on copper) has been analyzed, in the following the first bonding process step (graphene on copper onto thermal release tape) is carried out and investigated. As in the preliminary tests from chapter 3.1.1.2, a bonding force of 4 N/mm^2 for 10 min was applied

in a nitrogen atmosphere at room temperature with a relative humidity of 50 %. In contrast to the preliminary tests, the thermal release tape (TRT) was laminated with the back side on a silicon wafer without bubbles to guarantee the stability and handling of the TRT/silicon carrier. After the bonding step, the graphene/copper/TRT/silicon stack was placed in an acid bath with 0.1 molar ammonium persulfate solution for 4 h to remove the copper, followed by a water bath to reduce copper contamination. A stirring fish was placed perpendicular to the wafer surface during the etching step to increase the exchange of the acid due to parallel convention along the wafer surface. The parallel convection ensures better mixing of the etch media and decreases the visible carbon contamination from the copper back side. After purification, the graphene on the TRT was then dried for approximately 12 h in atmospheric conditions to reduce the amount of absorbed water molecules in the TRT tape from etching and purification. If this process step is skipped, the absorbed water molecules in the TRT can reduce the transfer quality because at the second bonding step the TRT tape is compressed and the absorbed water molecules are pressed out, which results in a water film at the interface of graphene and SiO_2. The water molecules would reduce the adhesion between graphene and SiO_2, resulting in a poor transfer result. [71]

The exposed graphene on the thermal release tape on silicon was then examined by laser scanning microscopy to investigate the transfer result. In chapter 3.1.1.2, it was already mentioned that the optical contrast of graphene on the thermal release tape is too low to evaluate the transfer. Since the thermal release tape is now on a silicon carrier, the optical contrast of the graphene on the TRT is improved by the silicon, which enables optical analyzation. In Figure 3-6 the comparison of the optical laser scanning microscopy images of the TRT/silicon and the graphene/TRT/silicon stack is shown.

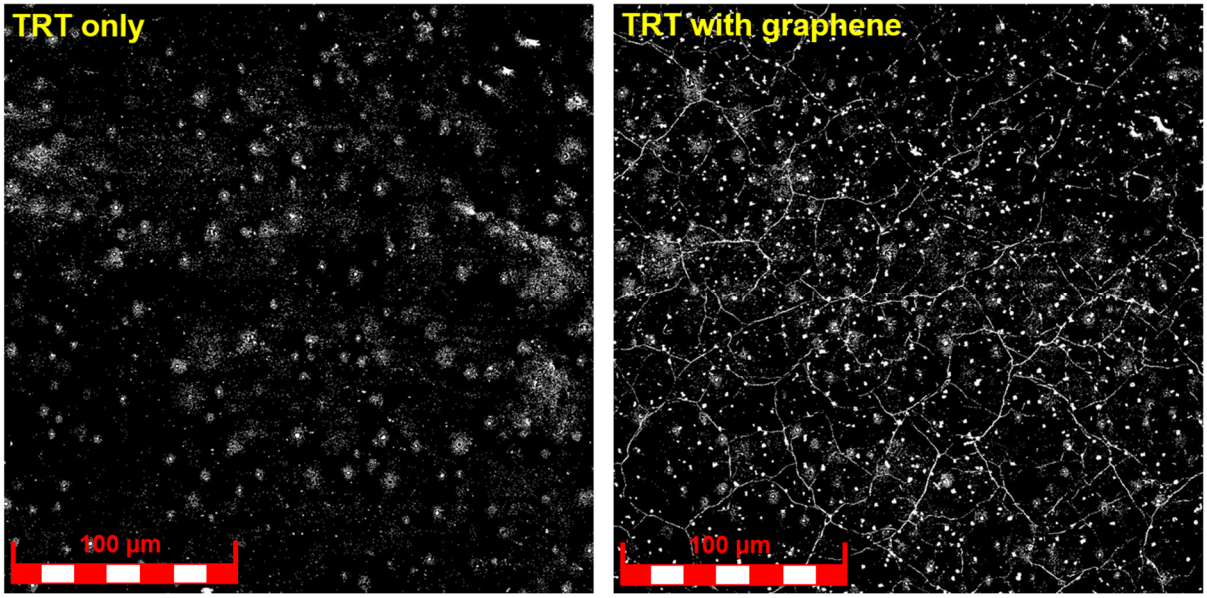


Figure 3-6: Laser Scanning Microscopy image of the thermal release tape (TRT) without (left) and with graphene (right). The right figure shows that after the graphene has been transferred to the TRT and after copper etching, the graphene edges are visible in the LSM image. This is an indicator that the graphene is present on the TRT after the copper etching step.

The laser scanning microscopy images with and without graphene on the TRT/silicon stack in Figure 3-6 show a significant difference. It is visible that the stack with graphene is imaged with its macroscopic grain boundaries in the optical micrograph. The visible domain sizes of the transferred graphene on the TRT are much larger than those obtained by EBSD analysis from Figure 3-5 b). The reason for this could be that only the crystal boundaries were detected by laser scanning microscopy, which has a higher percentage of copper contamination, and thus the contrast is visible in the optical image due to the high absorption of copper. Due to the limited lateral resolution of the laser scanning microscope, grain boundaries in the graphene layer that are in the sub-micrometer range (e.g. those detected in EBSD analysis) cannot be identified. Therefore it can be assumed that the visibly separated macroscopic graphene domains detected by laser scanning microscopy analysis are further subdivided into nanometer domains, as the EBSD analysis results in Figure 3-5 b) imply.

In the following, the transferred graphene on the TRT/silicon stack was transferred on a thermal grown 300 nm SiO_2 on silicon, with a bonding pressure varying from 1 N/mm^2 to 3 N/mm^2 in 1 N/mm^2 steps for the second bonding step for 10 min bonding time. From the preliminary tests from chapter 3.1.1.2, it was shown that the bonding pressure of the second bonding step has no significant effect on the transfer quality, but this could be changed by upscaling to 200 mm wafers. Therefore, the second bond pressure was varied to reflect this influence in the transfer result.

Three wafer-level transfer experiments were carried out in the following, with constant process parameters of bond step 1 (see above) and varying bond pressures for bond step 2. The process atmosphere during bond step 2 was nitrogen at a hot plate temperature of 80 °C to lower the relative humidity and therefore to reduce the water adsorbates on the SiO_2 and graphene interface, which results in a relative humidity of approximately 20 %. The transfer quality and yield of the 6-inch graphene layers on the SiO_2/Si target substrate were determined by wafer-level contrast spectroscopy, which was performed with a VHX digital microscope from Keysence, and the optical data were evaluated with the image processing software PicEd Cora. [71]

In the following, the transfer wafers with different transfer techniques and parameters are abbreviated with **w**et **t**ransfer (WT) and **semidry t**ransfer (SDT), followed by a number for better traceability. Table 3-3 shows the matrix of all experiments and the used wafer marking. [71]

Table 3-3: Matrix of transfer experiments of wet and semidry transfer with the corresponding wafer identifiers [71]

	Wet transfer	Semidry transfer		
2nd Bond Pressure	**-**	**1 N/mm²**	**2 N/mm²**	**3 N/mm²**
Sample Marking	**WT#1, WT#2, WT#3**	**SDT#1**	**SDT#2, SDT#3**	**SDT#4**

Coverage and yield

To evaluate the quality of the transferred graphene on the target substrate, a contrast image was recorded and used to determine the yield. This is shown in Figure 3-7, using the semidry transfer wafer with a second bond pressure of 2 N/mm² (SDT#2). On the right in Figure 3-7 is a white light image of the transfer result and on the left is the corresponding contrast image. In the contrast image, clear differences in the graphene regions on SiO_2 can be seen, which result from the different transfer qualities of the graphene layer through the transfer process and from the remaining polymer residues of the thermal release tape. Due to the resolution of the VHX digital microscope, only macroscopic transfer areas can be investigated. However, the macroscopic contrast image is an indicator of the graphene layer homogeneity on SiO_2 and based on this analysis, areas can be selected for microscopic analysis with a laser scanning microscope. In the contrast image, areas with graphene are shown in green, and areas without graphene are shown in blue on a macroscopic level. In red is the area of the wafer flat which is not covered with graphene due to the wafer shape of the copper foil. This area is not further considered in the following. [71]

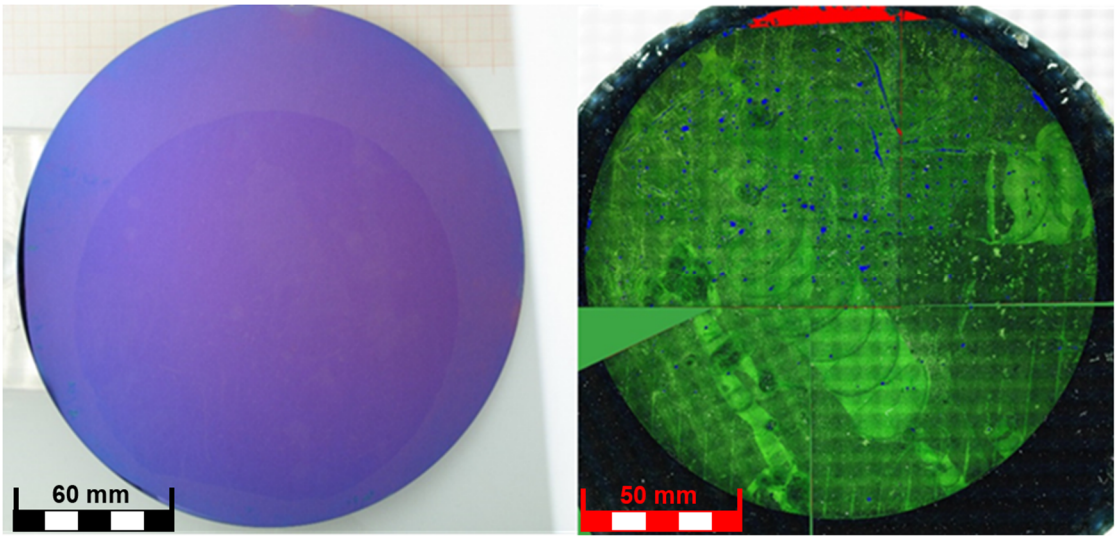


Figure 3-7: Wafer-level optical coverage determination of semidry transferred graphene with a bond pressure for the second bond step of 2 N/mm² (SDT#2). [71]

Figure 3-8, Figure 3-9, and Figure 3-10 show the extracted contrast measurement data from the three different wafer-level experiments with a bond pressure of 1 N/mm² (SDT#1), 2 N/mm² (SDT#2) and 3 N/mm² (SDT#4) for the second bonding step. The microscopic contrast determination was performed with laser scanning microscopy to evaluate the microscopic graphene transfer quality. The determination of the proportion of substrate, monolayer, and multilayer graphene domains is extracted from optical contrast measurements. The term multilayer graphene means in this case graphene that is already grown as multilayer graphene from the CVD process on copper, wrinkled during the transfer process, rolled up from residual carbon from the copper back side during copper etching, or from polymer residues due to the transfer. The procedure for the optical contrast determination of the proportions is described in Appendix A.2. The methodology differs from the method described in chapter 3.1.1.2, in which a black and white image is converted from an optical image, and the graphene and substrate proportion is determined by manually adjusting the brightness. With this new method, it is now possible to guarantee a high throughput and generate more comparable data by automated image conversion and extraction of the graphene, multilayer, and substrate portions. [71]

Figure 3-8 shows the contrast image of the semidry transfer experiment at a bonding pressure of 1 N/mm² for the second bonding step (SDT#1). The transfer yield of the graphene layer varies from 28.8 % to 61.3 % distributed over the wafer and with domains that do not have any graphene at all (marked blue). Areas with multilayer graphene vary from 2.40 % to 5.20 %, representing the areas where the graphene is wrinkled during transfer or graphene that has been transported from the back side of the copper foil through the copper etching step to the front side by convection in

the etching solution. Polymer residues were also included in these areas since multilayer areas and polymer residues cannot be optically separated from each other. As grown multilayer graphene domains were not considered, because these are not the result of the transfer process and should be statistically the same on all graphene on copper foil wafers. [71]

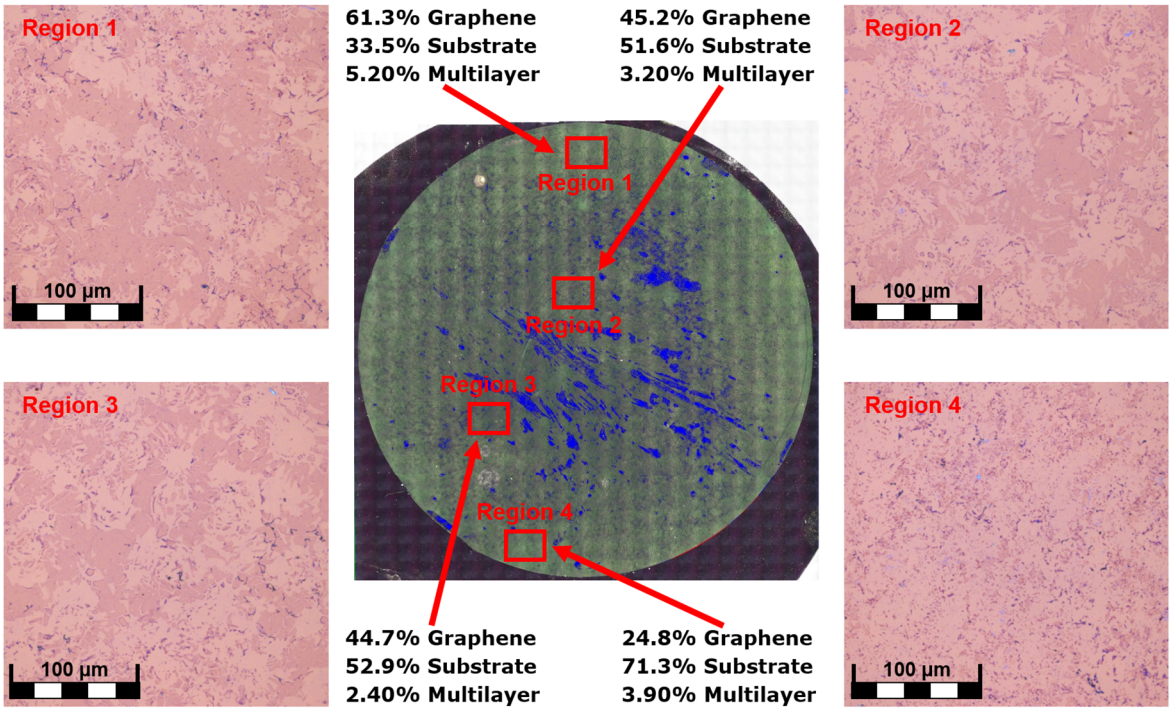


Figure 3-8: Contrast image of the semidry transfer result at a bond pressure of 1 N/mm² for the second bond step (SDT#1). The transfer yield of the graphene layer varies from 24.8 % to 61.3 % distributed over the wafer. [71]

Figure 3-9 shows the transfer result at a bond pressure of 2 N/mm² (SDT#2) for the second bond step and shows a graphene transfer yield of 17.2 % to 87.4 % distributed over the wafer. Compared to the transfer result of 1 N/mm² for the second bonding step in Figure 2-8, the proportion of areas where no graphene was transferred is smaller. In addition, Figure 3-9 shows an increased inhomogeneity of transfer quality over the wafer compared to Figure 3-8. The reason for the increased quality fluctuation was not exactly determined. The reason for this could be a local peeling of the thermal release tape from the silicon carrier wafer during the transfer, and thus the planarity is no longer given and therefore an undirected force distribution during the bonding step occurs, which can lead to an inhomogeneous graphene transfer quality. Domains with multilayer graphene vary from 2.30 % to 17.4 % and have been increased in comparison to the transfer result with 1 N/mm². Since this is just one transfer experiment, no statistical statement can be made, therefore it cannot be exactly clarified whether the increased multilayer graphene areas originate. Reasons for a higher multilayer graphene portion could be due to the higher

bonding pressure of the second bonding step, a higher portion of grown multilayer graphene domains during the CVD process, or other influencing variables such as poorer convection during the etch process of the copper foil or an increased carbon concentration on the copper back side. [71]

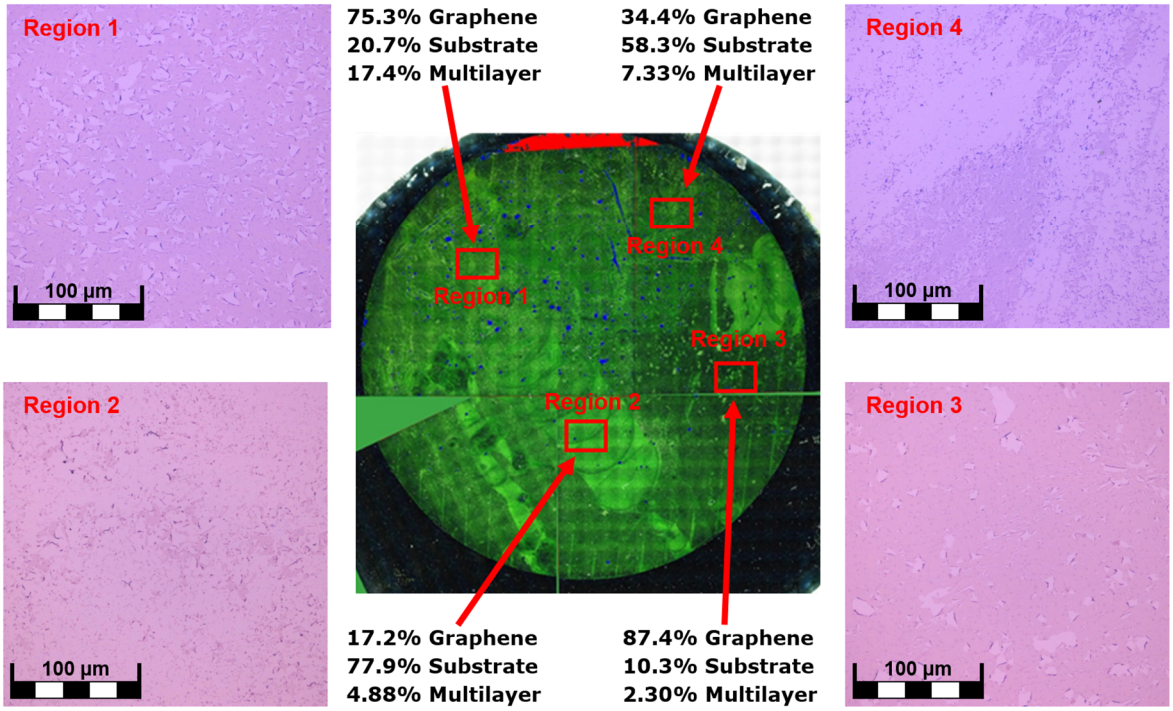


Figure 3-9: Contrast image of the semidry transfer result at a bond pressure of 2 N/mm² for the second bond step (SDT#2). The transfer yield of the graphene layer varies from 17.2 % to 87.4 % distributed over the wafer. [71]

Figure 3-10 shows the transfer result at a bond pressure of 3 N/mm² (SDT#4) for the second bond step and shows a transfer yield of graphene from 71.0 % to 90.8 %. Areas of non-transferred graphene are increased compared to the transfer result with a bond pressure of 2 N/mm² (SDT#2) in Figure 3-9. Multilayer graphene areas vary from 1.39 % to 2.80 % and have decreased compared to the previous experiment and were comparable to the result at the bond pressure of 1 N/mm² (SDT#1) in Figure 3-8. This shows that the high amount of multilayer graphene domains at the bond pressure of 2 N/mm² (SDT#2) in Figure 3-9 is compared to SDT#1 and SDT#3 the outlier and is not process-related due to the higher bond pressure but due to the variation of the starting material. [71]

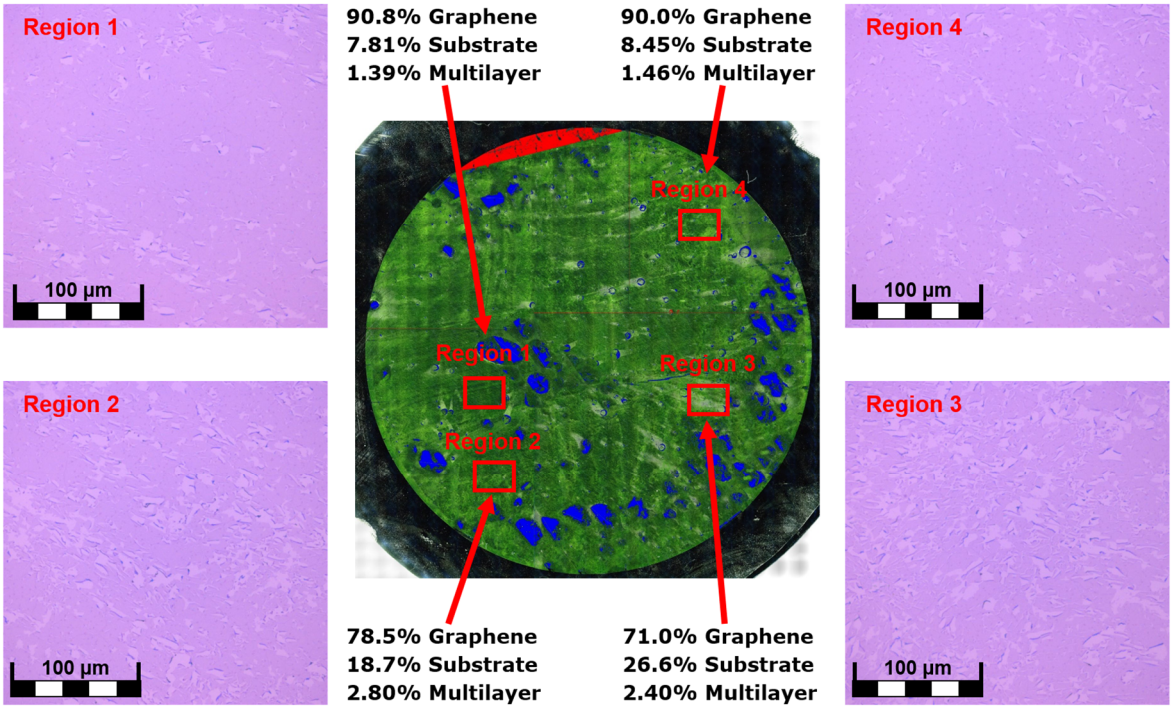


Figure 3-10: Contrast image of the semidry transfer result at a bond pressure of 3 N/mm² for the second bond step (SDT#4). The transfer yield of the graphene layer varies from 71.0 % to 90.8 % distributed over the wafer. [71]

In addition to the semidry transfer experiments, an identical analysis with wet transfer graphene was performed to compare the quality of the semidry transfer with a conventional transfer methodology. The wet transfer was performed according to [79] with a 6-inch graphene on copper foil wafer from Graphenea with PMMA on top without using a stirring fish as in the case of the semidry transfer, because of the low stability of the PMMA/graphene stack after copper removal. The same process parameters were used for copper etching, purification, and polymer cleaning as for semidry transfer for a better comparison of both transfer techniques, and the result is shown in Figure 3-11 (WT#1). It can be seen that with a transfer yield of 97.9 % to 99.2 %, the quality of the conventional transfer method is significantly better than the results of the semidry transfer experiments. It should be mentioned that this high transfer yield is only related to wafers in which the graphene was not cracked during transfer due to mechanical stresses in combination with low stability from the thin PMMA carrier. There were four preliminary tests in which the graphene was destroyed during handling at the intermediate transfer step from the copper etching solution to the water baths due to the high mechanical stress, resulting in a yield of 0 %. The wet-transferred graphene layers show also a significantly lower contrast on the SiO_2 than in the semidry transfer experiments, which suggests that the polymer contamination of the semidry transfer is higher. [71]

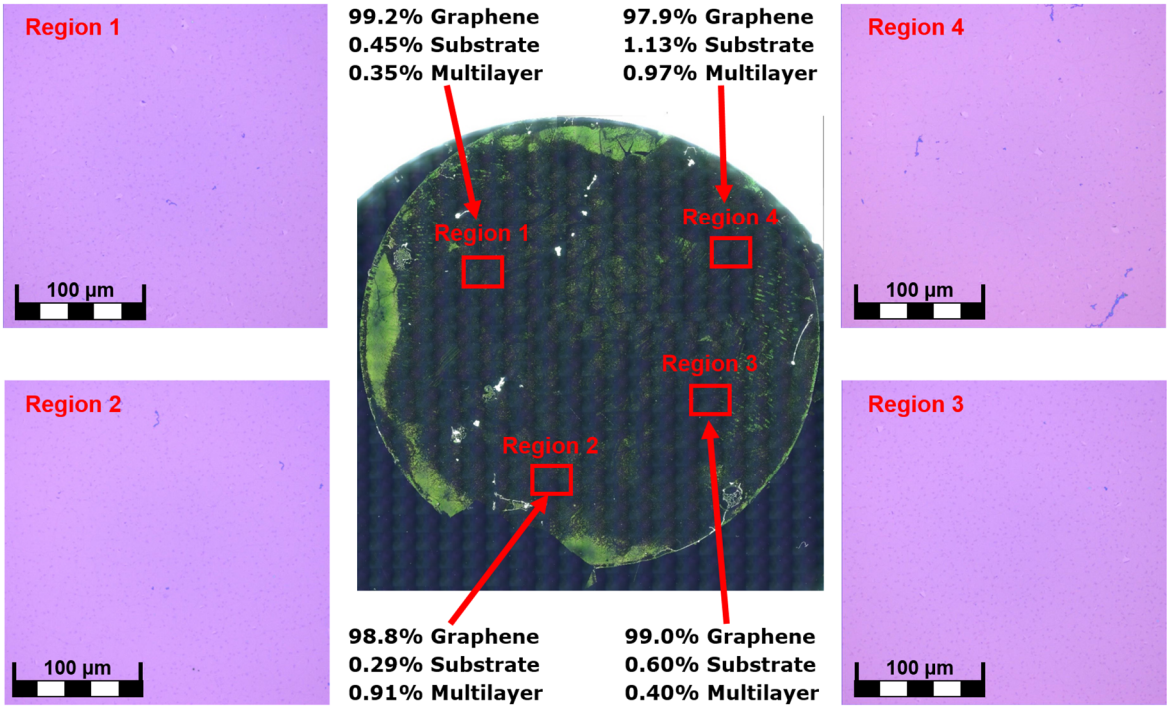


Figure 3-11: Contrast image of the wet transfer experiment (WT#1). The transfer yield of the graphene layer varies from 97.9 % to 99.2 % distributed over the wafer. [71]

If we compare the semidry transfer experiments with the classical wet transfer experiments using contrast microscopy, the transfer yield of the wet transfer is higher than in the semidry transfer experiments. At the highest bonding pressure for the second bond step of 3 N/mm^2 (SDT#4) a microscopic transfer yield of up to 90.8 % can be achieved, but not homogeneously distributed over the wafer. Compared to a microscopic transfer yield of up to 99.2 % homogeneously over the wafer for wet transfer, shows that the semidry transfer process still needs to be optimized here. There is a tendency for the bonding pressure of the second bonding step to be an important factor during the experiments at the wafer level because if the bonding pressure is increased, the transferred graphene layer to the target wafer is of higher quality than with lower bonding pressures. This contradicts the statement from chapter 3.1.1.2 since no tendency of the second bonding step on the quality of the graphene transfer was evident. The influence of this parameter on the transfer result could have a different impact than on sample sizes due to the scaling effects of the transfer. Thus, with a further increase of the bond pressure at the second bond step, the transfer result should also improve, but this cannot be proven due to the limitation of the transfer tool at higher temperatures to 3 N/mm^2. [71]

Contrast microscopy has shown that the transfer quality in terms of transfer yield of graphene to the target wafer is higher in wet transfer than in semidry transfer. Handling during the transfer

process is easier and more automated in semidry transfer than in wet transfer since the PMMA/graphene layer is transferred wet-chemically to the target substrate without a carrier wafer. With sample sizes of a few centimeters, this process is relatively easy to handle, but if the process is scaled up to a 6-inch wafer size, or in the future to an 8-inch or 12-inch, this becomes more critical and has an enormous impact on the transfer result. Therefore, the semidry transfer will play a more important role in the future if the graphene can be grown on 8 or 12-inch copper substrates. [71]

Now it is still to be clarified why the transferred graphene layers using semi-dry transfer are flaky and not homogeneous over the wafer. At release temperature, the thermal release tape increases the size of the adhesive bubbles which is connected with the loss of the adhesive force of the tape. The increase in the size of the adhesive bubbles could lead to a higher in-plane stress in the graphene layer, causing it to crack and become flaky. To prove this, optical microscopy is applied before and after the release of the tape, as shown in Figure 3-12.

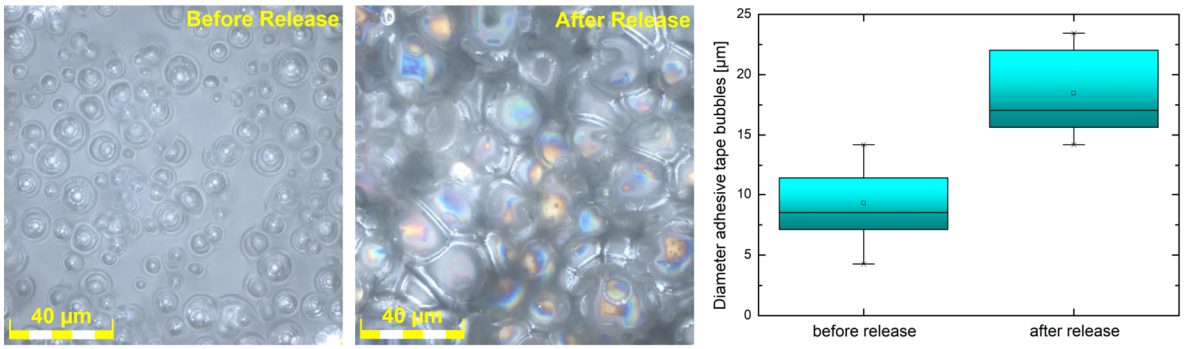


Figure 3-12: Statistical analysis of bubble size of the adhesive film of the thermal release tape before and after release using optical microscopy. The diameter of the adhesive bubbles increases from 9.3 µm before to 18.5 µm after release. The expansion of the bubbles could be the reason for the flaky graphene layer on the target substrate since the surface tension of the expanding bubbles causes the graphene to tear down.

Figure 3-12 shows that the adhesive bubbles are much smaller before release than after release. The diameter of the bubbles almost doubles during the release process, which leads to the consequence that the graphene layer is flaky since it is exposed to mechanical in-plane tension due to the enlargement of the adhesive bubbles. Therefore, a requirement for the transfer tape is that the adhesive bubble diameters are increased only slightly during the release process so that the tension in the graphene layer does not become too high and the layer does not crack to guarantee a continuous graphene layer on the target substrate.

Contamination

To determine the metallic contamination level of the graphene transfer via the wet and semidry method, TXRF (Total Reflection X-ray Fluorescence) measurements were performed with a Bruker TXRF measuring system TREX630. Separate wafers with wet and semidry graphene have been prepared for this purpose (WT#2 and SDT#3). [71]

The wet transfer at the wafer level was performed according to [79] in the same way as for WT#1 from Figure 3-11 (WT#2) and the semi-dry transfer graphene was performed with the same parameters as for SDT#2 from Figure 3-9 with a bonding pressure of 2 N/mm^2 of the second bond step (SDT#3). In addition, a reference wafer with SiO_2 on silicon was examined to identify possible pre-contamination of the wafers. To be able to give as much information as possible about the metallic contamination on the wafers, they were mapped over the complete surface with the TXRF system. Since during transfer, the only critical metal is copper which originates from the copper foil, this specific metal was analyzed via the TXRF measurements. The results of the three examined wafers with and without graphene are shown in Figure 3-13. [71]

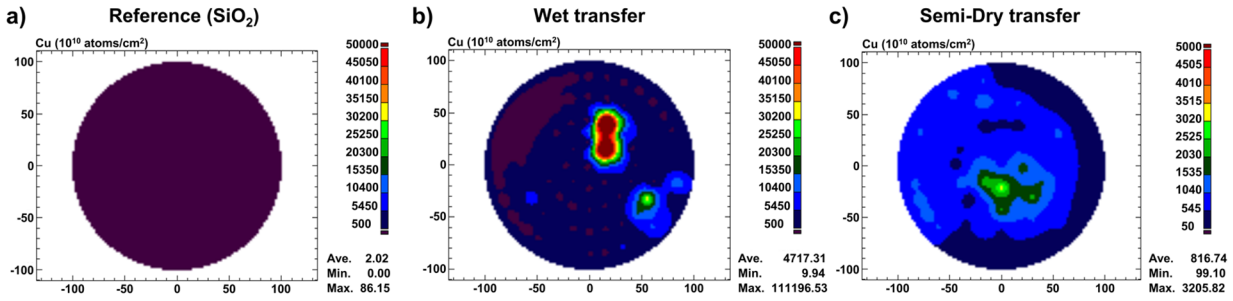


Figure 3-13: TXRF measurements for the analyzation of copper contaminations during the transfer of a reference wafer with SiO_2 on silicon in a), a wet transfer wafer with graphene transferred according to [79] (WT#2) in b) and a semidry transferred graphene wafer with a second bond pressure of 2 N/mm^2 (SDT#3) in c). [71]

From the result of the TXRF measurement in Figure 3-13 a), it can be seen that the reference wafer has on-average copper contamination of $2.02 \cdot 10^{10}$ atoms/cm^2, which is within the range of the acceptable front-end-of-line (FEOL) contamination level in semiconductor fabrication lines, but still critical for highly integrated circuits since even low metallic concentrations (10^{10} - 10^{11} atoms/cm^2) have a significant impact on the electrical properties of silicon-based devices [80], [81]. It is therefore necessary to keep the level of metallic contamination as low as possible. If we now compare the average copper contamination level of the wet transferred ($4.7 \cdot 10^{13}$ atoms/cm^2) and semidry transferred ($8.2 \cdot 10^{12}$ atoms/cm^2) wafers in Figure 3-13 b), c) with the reference wafer from a) ($2.02 \cdot 10^{10}$ atoms/cm), we see that both have a significantly higher copper contamination level. The lower specification limit of the TXRF tool is 10^{10} atoms/cm^2, so

copper contamination levels that are lower than 10^{10} atoms/cm^2 cannot be displayed in the measurements. From the TXRF measurements it is also evident that the copper contamination level during wet transfer is locally very high on two spots on the wafer ($25 \cdot 10^{13}$ atoms/cm^2 and $45 \cdot 10^{13}$ atoms/cm^2) and lower on the rest of the wafer. This result can be attributed to the poor exchange of the etching media during copper etching, as no stirring fish could be used due to the low stability of the PMMA/graphene stack at progressed copper foil removal. For semi-dry transfer also a local hot spot can be seen with a copper contamination level of about $25 \cdot 10^{12}$ atoms/cm^2, which is also lower than the average value of the wet transfer, but with a lower average contamination level on the rest of the wafer. [71]

For the determination of the carbon contamination level on the transferred graphene, XPS (X-ray photoelectron spectroscopy) measurements with an ESCALAB 250 Xi XPS system from Thermoscientific were performed. This was done on a SiO_2 reference wafer, a wet transfer wafer [79] (WT#3), and a semidry transfer wafer with a bonding pressure of 3 N/mm^2 (SDT#4). The sample sizes for XPS measurements are setup limited to some millimeters and therefore only a local investigation on the wafer is realizable. For this purpose, the wafers were broken into small pieces and only one piece at the wafer center was analyzed to determine the degree of carbon contamination after transfer. The results of the XPS measurements are shown in Figure 3-14. [71]

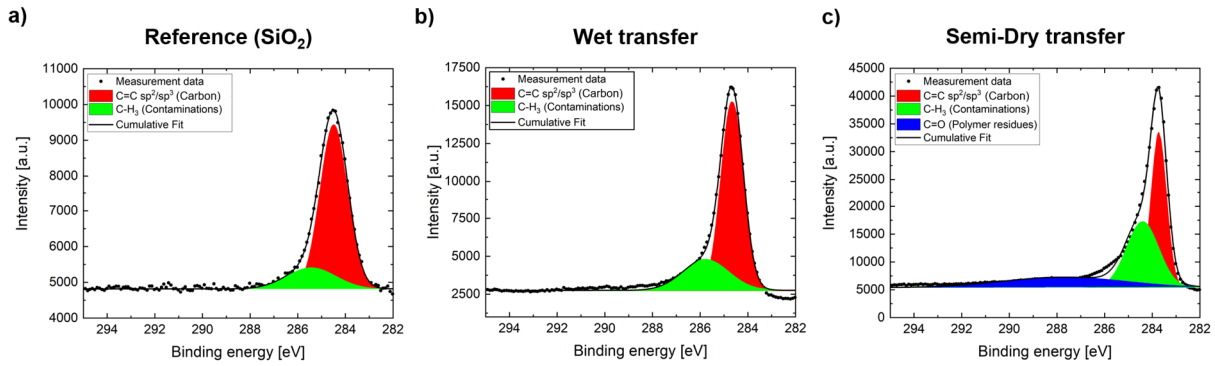


Figure 3-14: XPS measurements of a reference wafer with SiO_2 on silicon in a), a wet transfer wafer with graphene transferred according to [79] (WT#3) in b), and a semidry transferred graphene wafer with a second bond pressure of 3 N/mm^2 (SDT#4) in c). [71]

From the XPS measurement results in Figure 3-14, it can be seen that the carbon contamination is higher in semidry transfer than in wet transfer. Carbon is also present on the reference SiO_2 wafer as a result of handling the wafer piece into the XPS system chamber. The identified carbon bonding species on the reference wafer are sp^2/sp^3 hybridized carbon and methyl ($C\text{-}H_3$) groups. The sp^2/sp^3 hybridized carbon is indicative of the presence of combined C-C (sp^3) and C=C (sp^2) carbon binding types, the exact proportions of sp^2 and sp^3 hybridized carbon cannot be determined

because the binding energy signals are overlapping and therefore not separable from the XPS spectrum. The presence of methyl groups does not indicate the exact binding type of the carbon, i.e., whether it is amorphous or crystalline, because they are present at the edges of the carbon compounds. [71]

As well sp^2/sp^3 hybridized carbon and also methyl groups were detected on the wet transfer wafer, but with a higher XPS signal intensity than on the reference wafer. This indicates that the increased presence of sp^2/sp^3 hybridized carbon and methyl groups is due to polymer residues and the graphene layer itself. Graphene contains methyl groups at the edges and C=C double bonds within the sp^2 hybridized surface, polymers like PMMA also have methyl groups at the connection edges as well as other carbon-containing compounds such as carbonyl groups (C=O). In PMMA, the monomer MMA (methyl methacrylate) has two methyl groups and one carbonyl group. In Figure 3-14 b) there is no presence of carbonyl groups in the XPS signal, which indicates that a very low PMMA concentration after the transfer is existent, which is lower than the sensitivity of the XPS tool. Therefore, the main sp^2/sp^3 carbon compounds and methyl groups on the wet transfer wafer come from the graphene layer. [71]

Carbonyl groups are also present on the semidry transfer wafer in addition to the sp^2/sp^3 hybridized carbon and methyl groups, indicating the presence of polymer residues (Figure 3-14 c)). Since a polymer-containing thermal release tape was used instead of PMMA during the semidry transfer, the carbonyl groups originate from the tape and indicate higher polymer contamination. The increased proportion of carbonyl groups also explains the higher XPS signals of the sp^2/sp^3 carbon species and the methyl groups, indicating overall a higher polymer contamination level in semidry transfer than in wet transfer. Since the same polymer purification parameters were used in the wet transfer and semidry transfer, it can be concluded that one reason for the higher carbon contamination could be that the polymer residues after the release of the thermal release tape, before the cleaning steps with acetone and isopropanol, are higher in the semidry transfer than in the wet transfer with PMMA. A second reason could be that the additional chemical components in the TRT residues, which are not precisely specified by the manufacturer, result in a lower removal rate of the polymer residues by acetone due to increased binding forces of the components in the TRT to graphene compared to PMMA or a combination of this mechanism with higher TRT residues. [71]

From the TXRF analyses in Figure 3-13, it could be proven that the copper contamination level is on average higher in wet transfer than in semidry transfer, with a few contamination hot spots for both transfer types. The XPS analysis in Figure 3-14 shows that the degree of contamination by

polymers such as PMMA and thermal release tapes is different, leading to higher contamination in the semidry transfer than in the wet transfer. Based on this result, the electrical sheet resistance and electrical conductivity of graphene were extracted in the next step by terahertz time-domain spectroscopy [82]–[84] for both transfer techniques to investigate the influence of contamination on the electrical behavior of graphene. [71]

THz spectroscopy and electrical measurements

In addition to the transfer quality and the degree of contamination of the graphene layer during the transfer process, it is also important to investigate the influence of the transfer on the electrical properties of the graphene layer. This was realized by using Terahertz time-domain-spectroscopy (THz-TDS) on the wafer level and electrical measurements on the device level. The THz-TDS were performed with a Terahertz (THz) measuring system from Protemics, which allows for the extraction of electrical parameters like electrical sheet resistance and conductivity from the THz signal [82]–[84] on the wafer level. The setup consists of a THz pump/probe setup with a femtosecond fiber-laser at a pulse length of 100 ps at a wavelength of 780 nm and a photoconductive near-field micro-probe detector (TeraSpike TD-800-X-HR-WT) [83]. From the transmission signals of the THz setup, the sheet conductivity of the graphene layer σ_{sh} can be calculated with the Tinkham formula [85]: [71]

$$T(\omega) = \frac{T_{SL}(\omega)}{T_S(\omega)} = \left(1 + \frac{\sigma_{sh}(\omega) \cdot Z_0}{(n+1)}\right)^{-1} \qquad 2\text{-}1$$

With T_{SL} as THz transmission through substrate and graphene and T_S as THz transmission only through the substrate, n as the THz refractive index of the substrate and Z_0 as the free space impedance ($Z_0 = 377\ \Omega$) [85]. Not-covered wafer areas with graphene were used for the determination of T_S since the wafer has a higher diameter as the graphene. Figure 3-15 shows the comparison of the electrical parameters (electrical sheet resistance and conductivity) of wet (WT#1) and semidry transfer (bond pressure of 2 N/mm^2; SDT#2), determined from the THz signal with the corresponding contrast images. [71]

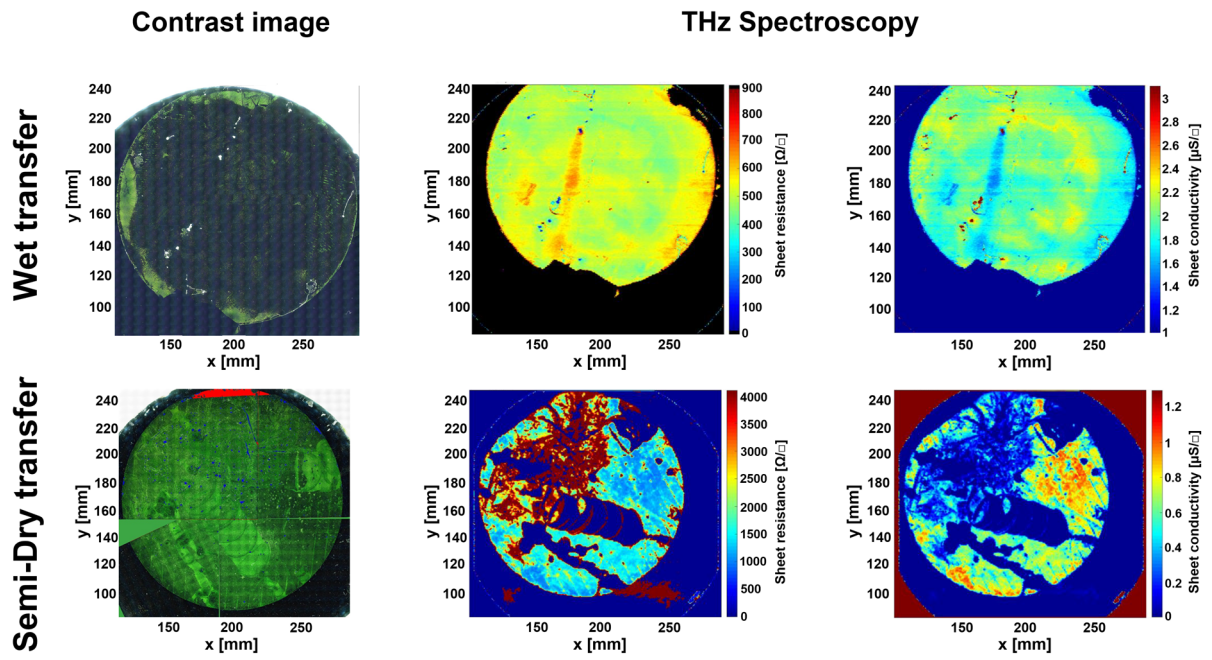


Figure 3-15: Terahertz time-domain-spectroscopy extracted electrical sheet resistance and conductivity of wet (WT#1) and semidry transferred graphene (SDT#2) in comparison with the corresponding contrast images. [71]

In the results of THz spectroscopy, it should be taken into account that the electrical parameters of the target substrate (SiO_2/Si) were subtracted from the signal, so that the areas where graphene is not present, sheet resistance, and conductivity have a value of zero. From the results of the THz spectroscopy measurements of the wet and semidry transfer, it can be seen that the electrical sheet resistance of the wet transfer is on average in the range of 450-550 Ω/□ (average electrical conductivity of 1.8-2.2 μS/□), and on average of the semidry transfer in the range of 1000-1650 Ω/□ (average electrical conductivity of 0.6-1 μS/□), which is by a factor of 2 to 3 higher. [71]

To confirm the electrical parameters extracted from the THz signals, the same wet- and semidry-transferred wafers are then structured into van-der-Pauw measurement crosses for the electrical measurements. For this purpose, the wafers are delivered to RWTH Aachen University, where they are lithographically processed and electrically measured. Wet-transferred graphene showed an electrical sheet resistance of 100-400 Ω/□ and a charge carrier mobility of 1000-1200 $cm^2/V{\cdot}s$, which is in good agreement with the extracted sheet resistance from THz spectroscopy (450-550 Ω/□). The electrical sheet resistance of semidry-transferred graphene shows values in kΩ range and no charge carrier mobility could be measured, which indicates that the graphene flakes were too small to get a continuous layer between the four-point terminals. These can also

be seen in Figure 3-16 on two different devices of the semidry transfer wafer before (a) and after (b) graphene structuring. [71]

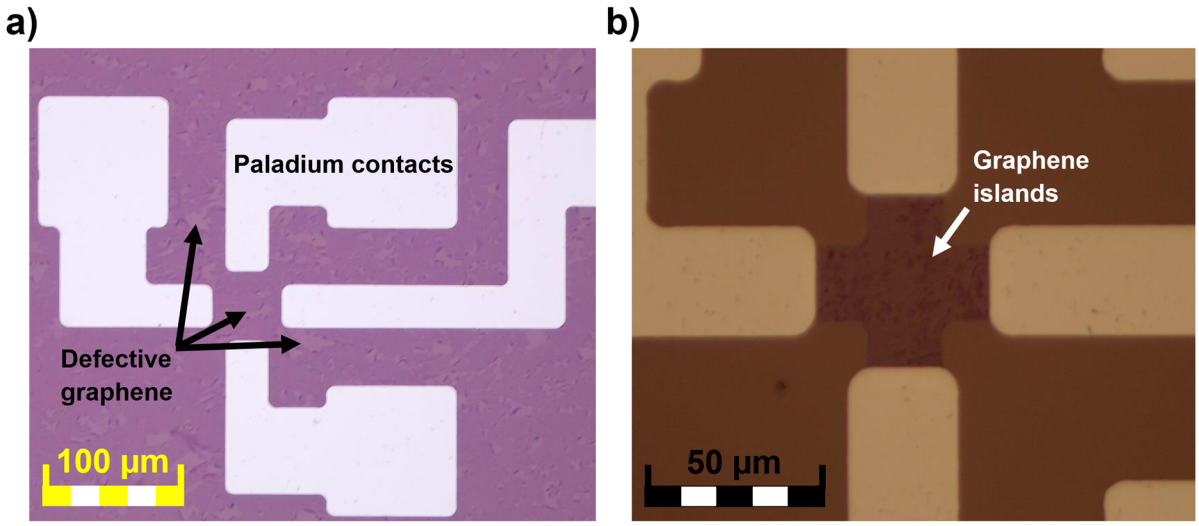


Figure 3-16: Optical images of two different test structures on the semidry transfer wafer (SDT#2) before (a) and after lithography structuring (b). [71]

The reason for the higher sheet resistance in THz spectroscopy and electrical measurements of semidry-transferred graphene could be linked to the higher measured proportion of carbonyl groups (polymeric contamination) in semidry transfer from the XPS measurements. These act as scattering centers for the electrons in the p_z orbitals in graphene through its ionic charge centers ($C{=}O^-$) and thus increase the electrical sheet resistance and reduce the electrical conductivity. The copper contamination can be excluded as a significant source of influence on the electrical sheet resistance since hot spots were identified from TXRF measurement on the wet transfer and semidry transfer wafers and these should therefore be reflected in the THz measurements on both wafers. [71]

3.1.4 Conclusion

Based on the defined process window for the semidry transfer of graphene on a sample basis in chapter 3.1.1, a self-made in-house tool was developed to enable the semidry transfer on the wafer level in chapter 3.1.2. Semidry transfer experiments were performed at the wafer level with different transfer parameters based on the observations in chapter 3.1.1 and compared with wet-transferred graphene at the same wafer size. From the transfer results in chapter 3.1.3 can be

concluded that the wet transfer has lower resistivity values than the semidry transfer, which was measured electrically at the device level on van-der-Pauw measurement structures and also extracted by THz spectroscopy. The improved electrical performance of wet-transferred graphene can be explained by the higher polymer contamination detected in the XPS measurements during semidry transfer. The XPS signals of methyl (CH_3) and carbonyl (C=O) groups are significantly higher in semidry transfer, which originates from the higher amount of polymer residues from the thermal release tape as from PMMA in wet transfer. The ionic charge centers from the carbonyl groups ($C=O^-$) act as scattering centers for the underlying graphene and lead to a higher electrical sheet resistance. TXRF measurements have shown that semidry-transferred graphene has a lower copper contamination level than wet-transferred graphene because of the improved copper etching process by using a stirring fish for better exchange of the etching medium due to the higher stability of the graphene layer with the TRT/silicon carrier. The copper contamination level is also a very important factor for the integration of graphene into the front end of line processes, which is limited by copper contamination levels of approximately 10^{10} atoms/cm^2. The yield of the transferred graphene is higher in wet transfer as in semidry transfer, but only at wafers in which the wet-transferred graphene is not cracked due to mechanical stresses and therefore destroyed. [71]

These results show that currently, both transfer techniques have their advantages and disadvantages in terms of transfer yield, metallic or polymeric contamination, and electrical performance. The wet transfer shows with the used transfer parameters a higher potential for fabrication of graphene-based devices with good electrical performance in applications such for example Hall sensors, but cannot be realized at the moment in silicon fabrication lines because of the high copper contamination levels. The use of higher concentrated etching media during copper etching could reduce residual copper contamination in both transfer methods and by using alternative growth substrates such as sapphire this contamination could be completely avoided [86]. Handling during wet transfer is a critical factor during the transfer process, as the graphene is only stabilized by the overlying PMMA after copper etching and is therefore only marginally resistant to external influences. This problem can be reduced by using thicker polymer support layers that offer higher mechanical strength. This disadvantage of wet transfer in handling is an advantage of semidry transfer, as the use of a carrier wafer makes the graphene more controllable during the transfer process, which is an advantage in terms of automation of this process. The higher polymer contamination level due to residues of the thermal release tape can be decreased by a longer cleaning process time with higher concentrated media to reach the same contamination level as the wet transfer. The electrical performance of the transferred graphene

could also be improved by reducing the polymer-containing residues in semidry transfer, and thus also the polar parts of the C=O bond. [71]

Both transfer techniques have their advantages and disadvantages in the end, but these can be overcome by optimized processes and tools. Therefore, both transfer techniques can play an important role in the future integration of graphene into industrial semiconductor production lines. The current status of both transfer techniques out of this work is summarized in Table 3-4. [71]

Table 3-4: Summary of the current status of the wet and semidry transfer in terms of handling during transfer, degree of automation, transfer yield, polymeric and metallic contamination, and electrical sheet resistance of the transferred graphene (+/++/+++ = low/medium/high). [71]

	Wet transfer	Semidry transfer
Handling during transfer	+	+++
Degree of automation	+	+++
The yield of transferred graphene	+++	++
Metallic contamination	++	+
Polymeric contamination	+	++
Electrical performance	+++	++

3.2 Control of electronic properties in graphene for reproducible device performance

The electronic behavior in graphene is influenced by the direct environment (substrate, encapsulation layer) since it consists only of one surface. The main influencing factor besides contamination, e.g. by transfer, is the surface of the substrate or the encapsulation layer (e.g. ALD Al_2O_3, etc.). The dominant factor of the impact on the electrical properties of the graphene layer is the surface charge density because surface roughness plays a minor role since industrial silicon-based isolators have a low surface roughness in the sub-nanometer range [87]. The surface charge density is substrate-dependent and is affected by the manufacturing method (CVD, PECVD, ALD, etc.) and its parameters (carrier gases, growth temperature/time, etc.). Therefore, it is necessary to control the surface charge density of the substrate to define active (e.g. sensor region) and passive (electrical contact) areas to guarantee a high performance of the application. The content of this chapter is the adjustment of the surface charge density of standard silicon-based isolators (especially SiO_2) via CMOS-compatible processes (chapter 3.2.1) and the determination of the effect of the modified substrates on electrical charge carrier density and charge carrier mobility (chapter 3.2.2.2) in graphene and the contact resistance between graphene and nickel interfaces (chapter 3.2.2.3).

3.2.1 Dielectric surface charge modification

The electrical properties of graphene are determined by the surface properties of the direct environment, which are usually isolators. Standard isolators in today's CMOS-compatible semiconductor factories are for example SiO_2 and Si_3N_4, but there are many others (e.g. Al_2O_3, ZrO_2) that are not investigated here. The surface of isolators is mainly determined by the surface charge and the surface roughness. For polished silicon surfaces, which serve as a substrate for the overlying isolating layer (e.g. SiO_2), the surface roughness is in the sub-nanometer range [87]. To determine the influence of the deposition process of SiO_2 and Si_3N_4 on the final surface roughness of the isolators, atomic force microscopy (AFM) measurements were performed. This was done with a µmasch ultrasharp tip in an NSC18 system and a Ti-Pt coating on the tip side, and a scan rate of 1 Hz with an angle of 90° in non-contact mode with a lateral resolution of 256 lines [78]. For roughness determination, a 300 nm thick silicon dioxide film on silicon was thermally

grown in a furnace at temperatures of 1000-1200°C and a 60 nm thick silicon nitride film on silicon was deposited with a low-pressure chemical vapor deposition (LPCVD) process with ammonia and dichlorosilane (SiH_2Cl_2) at temperatures of 700°C to 850°C in a furnace [78]. P-doped silicon with a doping concentration of 10^{15} cm^{-3} [78] was used as a substrate. Thermal-grown SiO_2 on silicon shows a root-mean-squared roughness R_q of 182 pm and deposited Si_3N_4 via LPCVD on silicon shows a root-mean-squared roughness R_q of 136 pm [78]. This result indicates that the influence of the surface roughness of SiO_2 and Si_3N_4 on the electrical properties of graphene is comparable due to the same order of magnitude of the roughness parameters. From previous works, it was shown that the SiO_2 surface induces a compressive strain in the graphene layer in the order of -0.1 % [88], and this should be also for Si_3N_4 due to similar surface roughness.

As the surface roughness of SiO_2 and Si_3N_4 are comparable, and therefore also there influence on the electronic properties of graphene, it is necessary to investigate the impact of the surface charges of the substrates on the electronic properties of graphene. The surface charges are dependent on the manufacturing process and the manufacturing parameters (pressure, temperature, etc.) of the substrates. For the determination of the influence of the manufacturing process and its parameters on the surface charge of SiO_2, surface photo voltage (SPV) measurements were performed with a Surface Charge Analyzer SCA-2500 from SemiTest for three different growth methods (dry oxide, tetraethylorthosilicate (TEOS) and high-temperature oxide (HTO) oxide):

Dry oxide	$\mathrm{Si} + \mathrm{O_2} \rightarrow \mathrm{SiO_2}$
TEOS	$\mathrm{Si(OC_2H_5)_4} \rightarrow \mathrm{SiO_2} + \mathrm{decomposition\ products}$
HTO	$\mathrm{SiH_2Cl_2} + \mathrm{2N_2O} \rightarrow \mathrm{SiO_2} + \mathrm{\ decomposition\ products}$

The surface charge of SiO_2, which was produced by different growth processes, shows a variation of $6.7 \cdot 10^9$ C/cm² for dry oxide, $1.6 \cdot 10^{11}$ C/cm² for TEOS, and $4.1 \cdot 10^{10}$ C/cm² for HTO. At these processes, the temperature ($T_{dry\ oxide} = T_{HTO} = 1000$ °C, $T_{TEOS} = 750$ °C) differs as well as the deposition mechanism and therefore the difference in surface charge from the combination of these parameters. Similarly, SPV measurements were performed on the fabricated thermal SiO_2 and LPCVD Si_3N_4 on silicon, which have surface charges of $1.45 \cdot 10^{10}$ C/cm² and $1.22 \cdot 10^{12}$ C/cm² respectively. This result shows that the manufacturing process of a substrate has an influence on the surface charge as well as different substrates, which leads to the fact that the electrical properties of graphene and its electrical performance are substrate-dependent.

Electrical graphene-based applications consist of different device areas, which can be roughly categorized into an active (performance) area and a passive (contact) area. Depending on its application, graphene can be used as e.g. a Hall sensor, where a high charge carrier mobility is necessary for the active area for optimal device performance. The passive area is in all cases defined as the graphene in the contact region, were a low electrical sheet resistance is necessary for low ohmic contacts. To define active and passive areas with different surface charge values in magnitude and sign in the graphene-based application, it is necessary to develop a method to ensure this at the wafer level on a CMOS-compatible substrate. This is achieved by introducing fixed ionic charges at the substrate surface (especially SiO_2) via diffusion of ammonia (NH_3) and aluminum to the SiO_2 surface to form positive [89] and negative [90] surface charges [78].

The manufacturing process for adjusting the surface charge at the SiO_2 surface via NH_3 and aluminum diffusion via temperature is shown schematically in Figure 3-17. By introducing NH_3 molecules via an annealing step at approx. 1100 °C for 1 min, the NH_3 molecules diffuse into the 340 nm thick SiO_2 and form fixed positively charged $NSiO^+$ networks [78], [89] (Figure 3-17 a)). The reason for the formation of a positive charge network is that oxygen atoms have an electronic configuration of $[He]2s^2 2p^4$, whereas nitrogen has one electron less and a configuration of $[He]2s^2 2p^3$. The difference of one electron leads to the p_y-orbital being only filled up with one electron. This allows the nitrogen to "trap" another electron in that orbital and, therefore, creates an overall positive charge by taking an electron from the system [91]. In addition to the fixed positive charges, the ammonia molecules also diffuse below the SiO_2 surface and form negative charges ($NH_3^{\delta-}$, NH_2^-) [92].

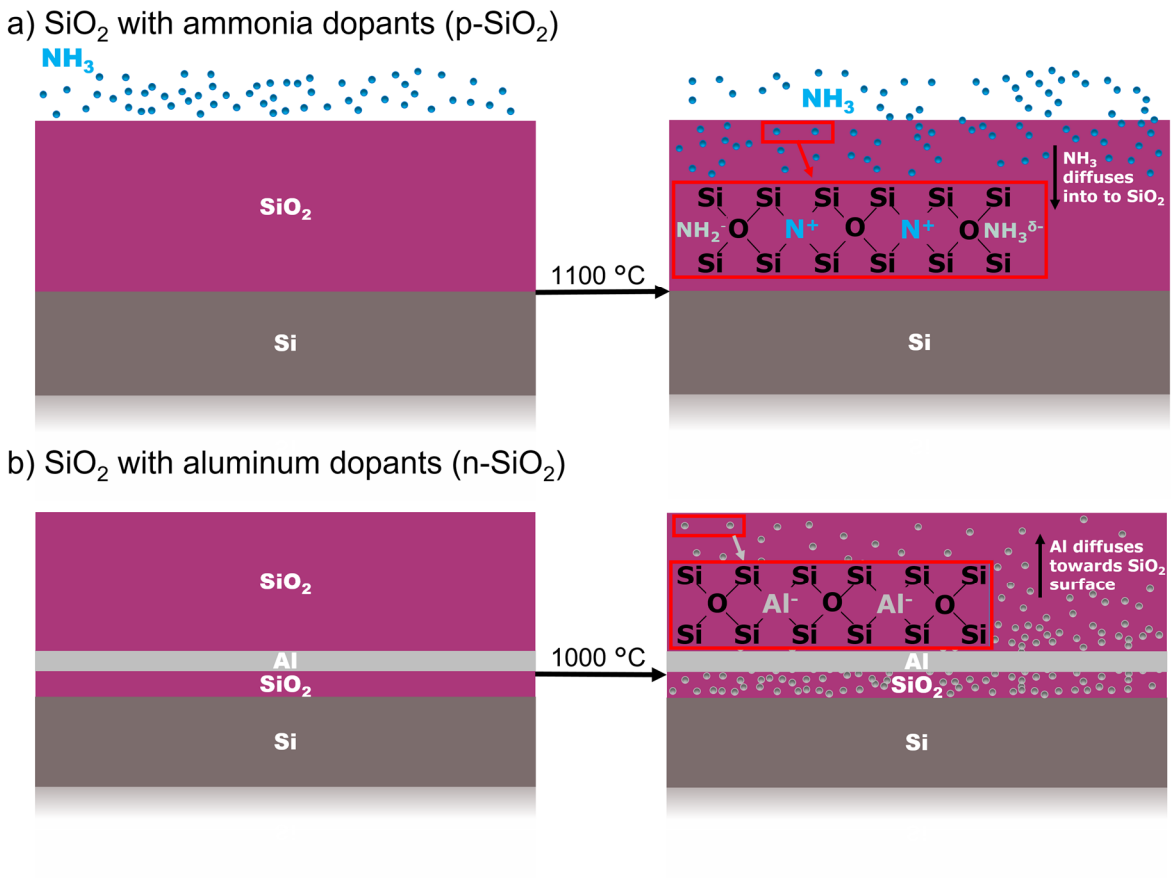


Figure 3-17: Schematic illustration of the manufacturing process of charged dioxides with the introduction of ammonia in a) and aluminum in b) with a thermal temper process to form fixed ionic charges at the SiO_2 surface. [78]

In the case of negatively charged SiO_2, an aluminum layer is introduced over atomic layer deposition between a SiO_2 layer system with a total thickness of 245 nm and was tempered at 1000 °C for several minutes (Figure 3-17 b)). The aluminum diffuses to the surface of the SiO_2 layer and forms here fixed negative $AlSiO^-$ networks [78], [90]. These networks are formed because aluminum has an electron configuration of $[Ne]3s^23p$, while silicon has one more electron and thus an electron configuration of $[Ne]3s^23p^2$. Therefore, a silicon atom has one more possibility to form a bond than aluminum does. By replacing some of the four binding silicon atoms with three binding aluminum atoms an AlSiO-network is created [90]. In the following, SiO_2 layers tempered with NH_3 are referred to as p-SiO_2, and those tempered with aluminum are referred to as n-SiO_2 (n/p denotes the charge sign of the surface (-/+)).

For the determination of the surface charge and surface roughness of the modified SiO_2 layers, surface photo voltage (SPV) and atomic force microscopy (AFM) measurements were performed. The measurement data of roughness and surface charge of the modified oxides and the standard substrates (SiO_2 and Si_3N_4) are collected in Table 3-5 [78].

Table 3-5: Experimental data from atomic force microscopy (AFM) and surface photo voltage (SPV) measurements of the substrates. From AFM measurements the root-mean-squared roughness R_q and the average roughness R_a is extracted. Average surface charge $\bar{q}$ of substrates is extracted via SPV measurements. [78]

Substrates	R_q [nm]	R_a [nm]	Surface charge $\bar{q}$ [C/cm²]
Si_3N_4	0.136	0.110	$1.22 \cdot 10^{12}$
SiO_2	0.182	0.105	$1.45 \cdot 10^{10}$
n-SiO_2	0.144	0.096	$-6.00 \cdot 10^{10}$
p-SiO_2	0.175	0.113	$5.38 \cdot 10^{11}$

From the SPV and AFM measurements on the substrates, it can be seen that the modified oxides (n/p-SiO_2) show a root-mean-squared roughness of 144 pm for n-SiO_2 and 175 pm for p-SiO_2, which are similar to the standard isolators SiO_2 (182 pm) and Si_3N_4 (136 pm), but with different surface charge densities. The absolute values of the modified SiO_2 layers ($-6.00 \cdot 10^{10}$ for n-SiO_2 and $5.38 \cdot 10^{11}$ for p-SiO_2) are different compared to the standard isolators ($1.45 \cdot 10^{10}$ for SiO_2 and $1.22 \cdot 10^{12}$ for Si_3N_4) and differs also in the sign of the charge for n-SiO_2, which indicates a successful adjustment of the surface charge by the tempering process with ammonia and aluminum. [78]

In the next step the chemical resistance of the adjusted surface charge to oxygen plasma is investigated, since during wet transfer the sample is first hydrophilized with oxygen plasma to ensure better wettability and for removal of carbon-containing contaminations. The oxygen plasma affects the surface properties of the substrate in case of wettability (see here also 3.1.1.1, Table 3-1) and thus could have an impact on the previous adjustment by ammonia and aluminum. The exact influence of the oxygen plasma treatment on the surface charge density is currently unknown and will be investigated in the following. The influence of the oxygen plasma properties is dependent on the plasma power, process duration, oxygen flow, etc., but in the following, only the influence of the oxygen plasma process with the parameters for the hydrophilization of the surface before the wet transfer is examined. The surface charges at the silicon/isolator interface of the standard isolators (Si_3N_4 and SiO_2) were measured by capacitance-voltage (CV) measurements to investigate the impact of the oxygen plasma. For the CV measurement, the isolating layer needs to be thin to analyze the impact of oxygen plasma at the silicon/isolator interface without any large attenuation of its power. The modified oxides could not be measured after plasma treatment with CV, as they cannot be homogeneously produced in such thin layers. No additional SPV measurements could be carried out after hydrophilization because the

contamination classes of the plasma system and the SPV system are different and therefore only CV measurement was done.

A thin LPCVD Si_3N_4 and a thin thermal SiO_2 (each 20 nm) on silicon were used to detect the influence of the oxygen plasma on the surface charges at the silicon/isolator interface since the oxygen plasma can penetrate down to the silicon/isolator interface at such thin layers [93]. Si_3N_4 and SiO_2 were hydrophilized via oxygen plasma for 120 s at a power of 50 W and an oxygen flow of 20 sccm in a MyPlas PECVD system from Plasma Electronics. Afterward, 100 nm thick nickel contact pads were produced on the isolators with a contact area of 7853.98 µm² via i-line photolithography with a mask aligner from Karl Süss to form a capacitor structure with the underlying silicon for the CV measurement. Here, a positive photo resist S1805 from Microchemicals was used and exposed for 3 s and developed with a metal ion-free developer AZ 726 MIF from MicroChemicals for 60 s. In the next step, 100 nm nickel was deposited with a physical vapor deposition tool by Tectra and afterward, the contact pads were exposed with a following lift-off process. The (100) silicon below the isolators has a hole majority electrical charge carrier density of 10^{15} cm^{-3}. The fixed interfacial charge Q_f can be extracted from the CV measurement using the equations A3-1, A3-2, and A3-3 from Appendix A3, with the potential Φ_{MS} from the silicon and the nickel electrode (Φ_{MS} = 0.24), a measuring temperature of 23°C and the permittivities of the isolators ($\varepsilon_{r_{SiO_2}}$ = 3.9 and $\varepsilon_{r_{Si_3N_4}}$ = 7). The measurements on 20 nm thick Si_3N_4 and SiO_2 after oxygen plasma showed that the average isolator charge of Si_3N_4 is slightly lower compared to before oxygen plasma treatment ($\bar{q}_{before}$ = 1.22·10^{12} cm^{-2} and $\bar{q}_{after}$ = 4.85·10^{11} cm^{-2}). However, on SiO_2 the opposite has been measured, here the average isolator charge is higher after oxygen treatment ($\bar{q}_{before}$ = 1.45·10^{10} cm^{-2} and $\bar{q}_{after}$ = 9.64·10^{10} cm^{-2}). Since the fixed isolator charges were extracted by different measuring methods (SPV and CV), it is not possible to identify where the difference comes from, from the measuring method itself or the influence of the oxygen plasma. Also, the processing time for the growth of the thin SiO_2 and Si_3N_4 layers is shorter than for the thicker layers, which can also influence the total surface charge on the interface of the isolator and silicon. However, it can be stated that the absolute value of the measurements before and after oxygen plasma treatment is similar, which leads to the conclusion that hydrophilization influences the isolator charge, but cannot be separated by the measurement accuracy of the two measurement methods. [78]

To investigate the influence of oxygen plasma on the structural surface condition of the SiO_2 and Si_3N_4 layers, XPS measurements were performed with an ESCALAB 250 Xi XPS system from Thermoscientific, and here the ratio of oxygen to silicon was investigated. The XPS measurements show that the ratio of O/Si on the Si_3N_4 surface (O/Si_{before} = 1.36, O/Si_{after} = 5.66) increases more

strongly than on the SiO_2 surface (O/Si_{before} = 5.75, O/Si_{after} = 6.02) due to oxygen plasma treatment. Therefore it can be assumed that the Si_3N_4 surface is partially transformed into a SiO_2 surface during oxygen plasma treatment. If the hydrophilization process is carried out at higher plasma powers and longer plasma durations, the surface charge profiles of both isolators should be equalized over time. It is therefore advantageous to carry out the hydrophilization process as fast as possible with very low plasma power in order not to influence the chemical surface properties of the isolators. From this, it can be concluded that the surface charge, which is specifically adjusted for the n/p-SiO_2, will change its absolute value, but the sign of the surface charge should remain. [78]

In addition to the change of the surface charge of the doped oxides by the introduction of ammonia and aluminum, it is also necessary to investigate the influence on the relative permittivity ε_r of the ionic charge centers on that of standard SiO_2, since in the following sub-chapter 3.2.2.2, the charge carrier concentration in graphene on the substrates is calculated via the gate capacitance [94]. The change of the relative permittivity was determined by measuring the capacitance of a MOS structure with 300 nm SiO_2 as an isolator, with an active contact area of 0.008 mm² produced via i-line photolithography with the same process flow as for the contact pads for CV measurements, with a precision LCR meter of HP and a known relative permittivity of 3.9 [95] for SiO_2. From this measurement, the capacitance of the measuring station could be determined and deducted from the measurements of the doped oxides. The capacitance measurement with the modified SiO_2 substrates shows that the relative permittivity ε_r of p-SiO_2 is 4.3 and for n-SiO_2 is 3.7. [78]

After SPV, AFM, and CV measurements on the modified and standard isolators, the influence of ammonia and aluminum in SiO_2 layers on the surface charge, roughness, optical properties, and chemical resistance is investigated and the influence on the electrical properties of graphene can be further determined. In the following chapter, the charge carrier concentration in graphene on SiO_2, Si_3N_4, and n/p-SiO_2 will be extracted via the gate capacitance and the influence on the charge carrier mobility via Hall-effect measurements. Also, the influence of the substrates on the contact resistance between graphene and nickel interfaces is determined by transfer line method (TLM) measurements.

3.2.2 Control of electronic properties of graphene

This chapter focuses on the preparation of graphene-based van-der-Pauw and TLM structures on SiO_2, Si_3N_4, and n/p-SiO_2 (3.2.2.1) for the determination of the influence of the substrate surface properties on the electrical behavior of graphene (3.2.2.2) and graphene and nickel interfaces (3.2.2.3).

3.2.2.1 Device preparation

To determine the charge carrier concentration and charge carrier mobility in graphene and the contact resistance between graphene and nickel interfaces on the substrates (SiO_2, Si_3N_4, and n/p-SiO_2), van-der-Pauw and TLM structures were produced. The graphene was deposited on copper by chemical vapor deposition (CVD) and purchased from the supplier ACS Materials (Trivial Transfer Graphene). The graphene layers were afterward transferred wet-chemically [79] on the substrates (standard Si_3N_4 and SiO_2, and p/n-SiO_2) from chapter 3.2.1. Previously, the substrates were cleaned and hydrophilized via oxygen plasma with a MyPlas PECVD system from Plasma Electronics for 120 s at a power of 50 W and an oxygen flow of 20 sccm. The transferred samples were dried under atmospheric conditions for 6 h and then the PMMA carrier layer was removed with acetone and isopropanol. [78]

In the next step, alignment markers were deposited on the samples via i-line photolithography with a mask aligner MA56 from Karl Süss. Initially, the samples were spin-coated with an approx. 1.2 µm thick positive resist (S1805 from MicroChem) and then heated at 110 °C for 60 s. The photoresist was then photochemically treated via i-line exposure for 3 s and subsequently developed in a metal-ion-free trimethylammonium-based developer (AZ 726 MIF from MicroChemicals) for 60 s. Afterward, the samples were coated with a 50 nm thick nickel layer via physical vapor deposition (PVD) with a PVD tool from Tectra. The alignment markers were exposed via a lift-off process in acetone in combination with ultrasound treatment. [78]

The next step is to produce the van-der-Pauw and TLM structures. A PMMA/aluminum/photoresist hard mask was used for the structuring, as XPS measurements with an ESCALAB 250 Xi XPS system from Thermoscientific had shown that only with the use of the photoresist as a hard mask for oxygen structuring, C=O components are present after polymer removal (Figure 3-18 a)). The

oxygen plasma structuring process leads to the encrustation of the polymer and thus to an increase in the crystalline character of the polymer in these areas. Subsequent wet chemical removal steps can no longer remove these encrusted polymer areas, which is reflected in the high C=O content. The hard mask can reduce the amount of C=O components, but not completely prevents the polymer encrustation (Figure 3-18 b)). [78]

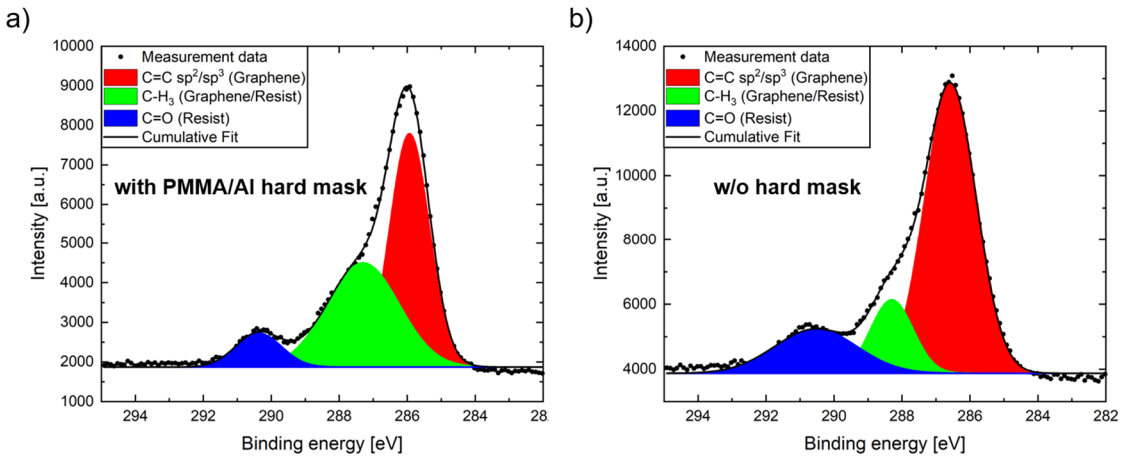


Figure 3-18: XPS measurement on structured graphene with a hard mask in a) and without a hard mask in b). It can be seen that the binding fractions of carbonyl groups (C=O), which originate from encrusted polymers during oxygen plasma structuring, can be reduced by the hard mask. [78]

For the hard mask, a 200 nm thick PMMA layer was first deposited on the samples via spin-coating and then baked for 10 min at 110 °C. A 20 nm thick aluminum layer was then evaporated over physical vapor deposition and then the photoresist with the same parameters as for the alignment markers was coated. The samples were then exposed by i-line photolithography for 3 s, then developed for 60-120 s (here the photoresist and the underlying aluminum were removed), and then PMMA and graphene were removed by oxygen plasma for 300 s at a power of 50 W and an oxygen flow of 20 sccm. The hard mask was removed via a cascading acetone/developer/acetone cleaning with ultrasonic treatment. [78]

After the structuring process, contact pads for the charge carrier concentration and charge carrier mobility measurements, and contact resistance measurements were defined on the samples. During this step, the same parameters were used for photolithography as for the alignment marker fabrication, and then 100 nm nickel was deposited via physical vapor deposition, and the contacts were exposed via a lift-off process with acetone and ultrasound treatment. In Figure 3-19, a manufactured van-der-Pauw structure without (a) and with (b) a hard mask is illustrated via a laser scanning microscope OLS4000 from Olympus. It can be seen that without using the

PMMA/aluminum/photoresist hard mask, a visible encrusted polymer layer can be seen on the graphene structure, which was also previously identified by XPS measurements. [78]

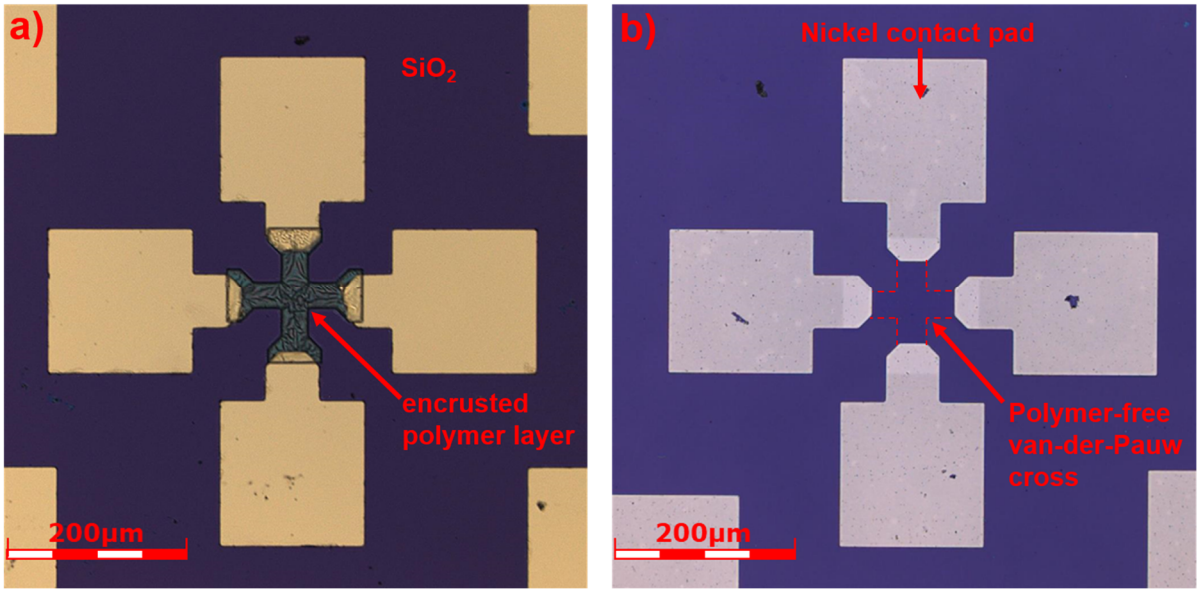


Figure 3-19: Optical microscope images of the van-der-Pauw structures with and without a hard mask. a) A thin photoresist layer is visible on the structured graphene layer defined by oxygen plasma etching. This is due to the encrustation of the photoresist during the oxygen plasma step. b) A structured graphene layer without polymeric residues due to the hard mask, which prevents the curing of the photoresist during oxygen plasma treatment. [78]

3.2.2.2 Impact of the substrate surface on the electrical properties of graphene

The charge carrier concentration in graphene on the substrates Si_3N_4, SiO_2, and p/n-SiO_2 was determined by measuring the electrical sheet resistance with applied back-gate voltage on seven test structures on Si_3N_4, nine on SiO_2, six on n-SiO_2 and seven on p-SiO_2. The van-der-Pauw test structures have been measured with an Agilent 4156B semiconductor parameter analyzer with four electrical manipulators with tungsten needles for contacting in a vacuum at a pressure of about 10^{-3} mbar. The setup consists of a copper coil below the sample, which induces a magnetic field of up to 80 mT at a current of 15A. As a reference, a commercial Hall-effect sensor from Infineon (TLE4997E2XALA1) was operated by a Keithley2000 power supply. The Fermi energy in graphene was modified by the electric field effect through the contacted back gate from -100 V to 100 V. The electrical sheet resistance in graphene was determined by equation 2-2, at an applied current of 1 mA. [78]

$$R_{\square} \cong \frac{\pi}{\ln 2}\frac{V}{I} \qquad 2\text{-}2$$

Here, V is the applied voltage, and I the forced current. Through back gate voltage sweeps and simultaneously measuring the sheet resistance of graphene, the Dirac point voltage V_D have been extracted at the point with the highest sheet resistance value. [78]

The electrical charge carrier density in graphene was calculated by using the following equation [94]:

$$n(V_g) = \frac{C_g}{e \cdot A}(V_{bg} - V_D) \qquad 2\text{-}3$$

With V_{bg} as back gate voltage, C_g as the capacitance of the respective isolator material, A as the device area (0.008 mm²), e as the elementary charge and V_D as the Dirac voltage [78].

Figure 3-20 shows the Dirac voltage and the electrical charge carrier distribution in graphene on the different substrates. On SiO_2 and Si_3N_4, graphene exhibits a negative Dirac voltage and therefore has electrons as the main charge carriers. The reason for this is the positive surface charge of SiO_2 ($q = 1.45 \cdot 10^{10}$ cm^{-2}) and Si_3N_4 ($q = 1.22 \cdot 10^{12}$ cm^{-2}), which produce a negative image charge in graphene (electrons). The influence of the oxygen plasma during the transfer process (chapter 3.2.2.1), which was determined by CV measurements, changed the surface charge only minimally and could not be determined exactly by the different measuring methods. Therefore, the surface charge before oxygen plasma treatment is considered in the following. The absolute value of the negative charge carrier concentration in graphene is higher on Si_3N_4 than on SiO_2, which is due to the higher positive surface charge of the Si_3N_4 surface. The distribution of the charge carrier concentration in graphene is significantly higher on Si_3N_4 than on SiO_2. The reason for this could be the partial transformation of the Si_3N_4 surface during the oxygen plasma step at the transfer process, which creates domains of higher positive (Si_3N_4) and less positive (SiO_2) regions, which could be the reason for the higher distribution. But this does not explain the occurrence of hole concentrations in graphene on Si_3N_4 (positive Dirac voltage), because the electron concentration should not be lower than in graphene on SiO_2 (due to the conversion of Si_3N_4 into a SiO_2 surface). It can be assumed that the positive Dirac voltage (and thus holes as majority charge carriers) could result from impurities caused by the structuring process because in Figure 3-18 from chapter 3.2.2.1, XPS measurements have shown that by using a hard mask during the structuring process the amount of $C{=}O^-$ bonds could not be completely removed. These negative dangling bonds

induce a positive image charge in graphene and could be the reason for the appearance of holes as majority charge carriers in graphene on Si_3N_4. [78]

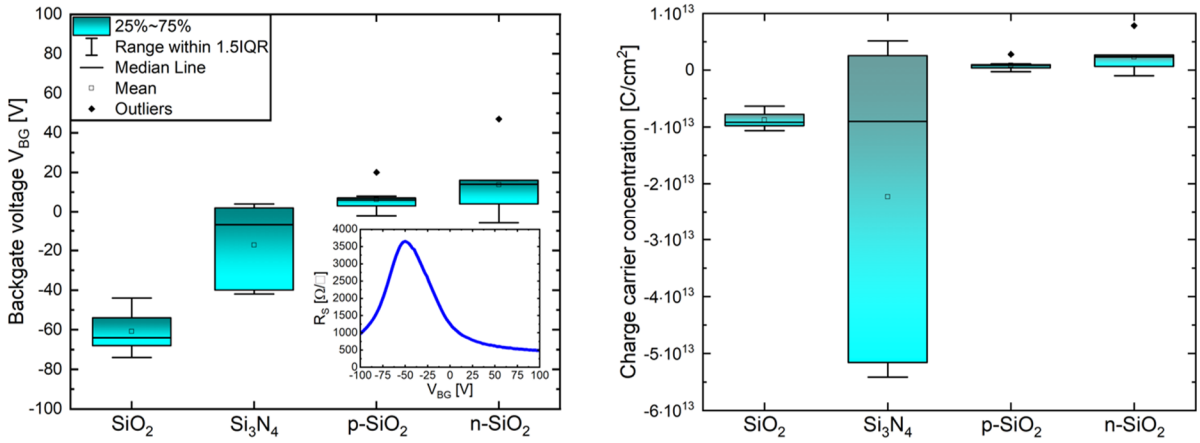


Figure 3-20: Dirac voltage and statistics of charge carrier concentration in graphene on different substrates, extracted from back-gated electrical sheet resistance measurements in vacuum. The Dirac voltage was determined at maximum sheet resistance in graphene during the back-gate sweep and corresponds to the charge neutrality point. Positive Dirac voltages correspond to positive charge carriers (holes) and negative Dirac voltages correspond to negative charge carriers (electrons) in graphene. Si_3N_4 and SiO_2 lead to electron doping in graphene because the surface is positively loaded by silanol groups. Diffusion of aluminum (Al) and ammonia (NH_3) in SiO_2 leads to a low negative surface charge of the SiO_2 surface and thus to p-doping in graphene. [78]

The charge carrier concentration of graphene on the p/n-SiO_2 substrates (Figure 3-20) shows mostly positive Dirac point voltages (hole concentration) for n- and p-SiO_2, with outliers to negative values. In contrast to the standard isolators Si_3N_4 and SiO_2, no CV measurements were performed on the modified oxides after oxygen plasma treatment, because as explained in chapter 3.2.1, these isolators cannot be produced in this thin film thickness due to the difficult control of the charge homogeneity across the layer thickness. It can be concluded from the results of chapter 3.2.1 for Si_3N_4 and SiO_2, that the oxygen plasma process has a small influence on the magnitude and sign of the surface charge. Applying these observations to the measurement results of the charge carrier concentration in graphene (Figure 3-20 b)), extracted from the electrical sheet resistance measurements, it can be seen that a similar charge carrier density in graphene can be measured on both modified isolators ($-1 \cdot 10^{12}$ cm^{-2} to $7.8 \cdot 10^{12}$ cm^{-2} on n-SiO_2 and $-2.8 \cdot 10^{11}$ cm^{-2} to $2.8 \cdot 10^{12}$ cm^{-2} on p-SiO_2). Compared to the surface charges on the modified oxides ($-6.00 \cdot 10^{10}$ cm^{-2} on n-SiO_2 and $5.38 \cdot 10^{11}$ cm^{-2} on p-SiO_2) from SPV measurements, this measurement results in a deviation of the expected charge carrier concentration behavior in graphene. [78]

The reason for this behavior could be due to the combination of the oxygen plasma process impact on the surface charges of the modified oxides and the additional charges caused by polymer residues during the structuring process. The negative $AlSiO^-$ networks in n-SiO_2 are located

directly below the surface and in the bulk [90] and are therefore only slightly influenced by the oxygen plasma, since the $AlSiO^-$ volume charge in n-SiO_2 below the surface is high. The oxygen plasma treatment produces Si-O-H^+ dangling bonds [96] on the SiO_2 surface which slightly attenuates the absolute negative surface charge. In addition, the negative C=O^- charges of polymeric impurities during the manufacturing process of the van-der-Pauw structures increase the total negative surface charge. Thus, the sum of the contributions of the individual charges is negative, with the main part coming from the $AlSiO^-$ charge centers. This leads to a local charge carrier concentration fluctuation due to the inhomogeneity of the charge distribution, which results in graphene regions with different hole concentrations. The positive surface charge contribution caused by the Si-O-H^+ dangling bonds attenuates the overall negative charge of the surface and in some cases even reverses its polarity, so that it is positive in total and therefore electrons act as the major charge carrier in graphene. [78]

In p-SiO_2, the $NSiO^+$ networks are located directly below the surface at a depth of up to about 1 nm [97], [98], which are almost destroyed by oxygen plasma treatment [99] and release positive Si-O-H^+ charges on the surface. This positive charge is attenuated by negatively charged ammonia molecules ($NH_3^{\delta-}$, NH_2^-), which originate from the nitration process of the SiO_2 layers [92]. Thus the total charge on the surface is almost zero since the three charge components (residual positive $NSiO^+$ networks, negatively charged ammonia molecules, and positive Si-O-H^+ charges) balance each other. In addition, as in the case of n-SiO_2, there are also negative C=O^- charges due to polymer contamination, which is why a negative charge is present in the graphene environment in combination with the coexisting charge components. Therefore, the majority of charge carriers in graphene are holes, with a small proportion of electron regions in graphene due to the charge inhomogeneity on the surface, which is reflected in the electrical measurements. [78]

Besides the impact on charge carrier concentration, charge carrier mobility μ was measured with the same measurement system in a vacuum as it was used for the electrical sheet resistance measurements and extracted using the following equation:

$$\mu = \frac{1}{V}\left|\frac{\partial V_H}{\partial B}\right|\frac{L}{W} \qquad 2\text{-}4$$

With V as the applied voltage, W and L are the width and length of the test structure (in the case of a van-der-Pauw cross is $L/W = 1$) and V_H is the measured Hall voltage at an applied magnetic field B. [78]

The results of the charge carrier mobility measurements are shown in Figure 3-21. The charge carrier mobility for electrons at the Dirac point is higher on the standard isolators Si_3N_4 (10.300 $cm^2/V{\cdot}s$) and SiO_2 (6.000 $cm^2/V{\cdot}s$) than on the modified SiO_2 substrates with aluminum (2.000 $cm^2/V{\cdot}s$) and ammonia (3.400 $cm^2/V{\cdot}s$) dopants. The origin of this trend could be the higher number of surface charge states on the modified oxides. In addition to the positive silanol groups [100] of SiO_2 and Si_3N_4 surface (created by oxygen plasma treatment), the fixed ionic charge centers $AlSiO^-$ and $NSiO^+$ are additionally present on the SiO_2 surface, which influences the surface state density of the SiO_2 layer. Thus, there are more scattering centers on the p/n-SiO_2 surface than on the standard isolators, which leads to a reduction of the charge carrier mobility. Graphene on Si_3N_4 has the highest electron mobility of 10.300 $cm^2/V{\cdot}s$, which is due to the low surface roughness of 0.136 nm (Table 3-5) [88], [101], compared to SiO_2 with 0.182 nm. [78]

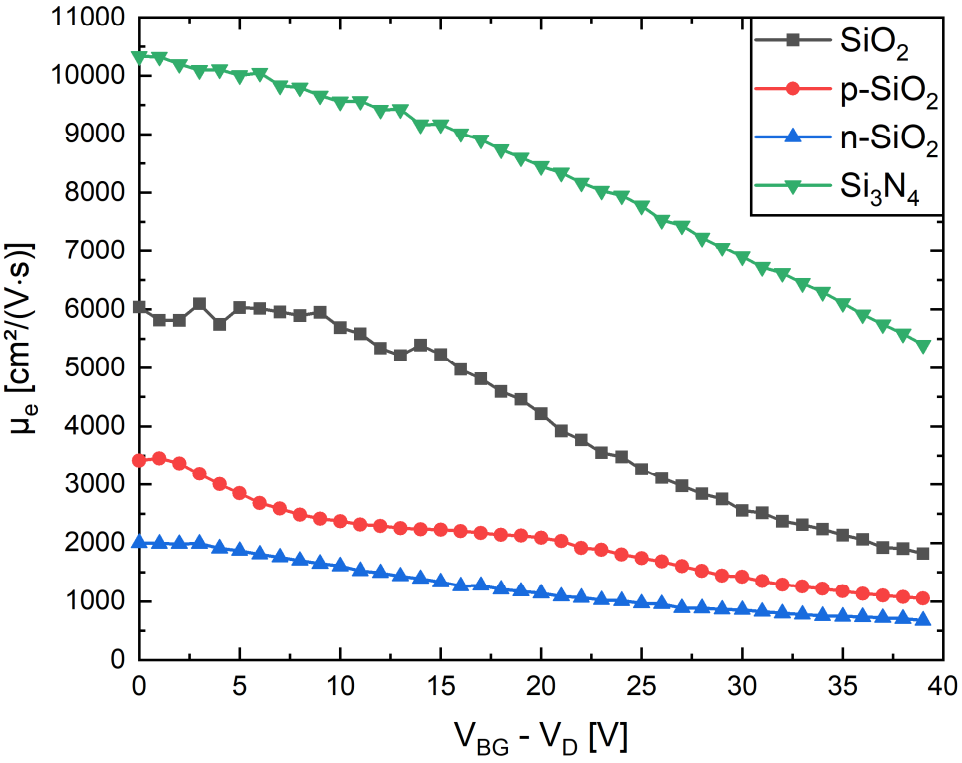


Figure 3-21: Charge carrier mobility of electrons μ_e from Hall measurements in vacuum in graphene plotted against the difference of back gate voltage V_{BG} and Dirac voltage V_D. The charge carrier mobility of electrons is higher on the standard isolators Si_3N_4 and SiO_2 than on the modified p/n-SiO_2. The origin of this tendency could be the higher number of surface charge states on the modified oxides. The charge carrier mobility on Si_3N_4 is higher than on SiO_2 due to the lower surface roughness. [78], [88], [101]

3.2.2.3 Contact resistance behavior between graphene and nickel interfaces on the substrates

Besides the influence of the modified SiO_2 substrates with aluminum and ammonia on the charge carrier concentration in graphene by defined surface charge manipulation, this method can also be used to adjust the contact resistance Rc between graphene and metals, because Rc depends on the charge carrier concentration n ($Rc \propto \sqrt{n^{-1}}$) of the bulk material (graphene). To prove this, TLM structures (chapter 3.2.2.1) were fabricated on SiO_2 and p/n-SiO_2 (comprises of 13 on SiO_2, 12 on p-SiO_2, and 9 on n-SiO_2), with nickel as contact metal, and the contact resistance was determined without electric field effect between nickel and graphene to observe the doping influence of the substrates on the intrinsic behavior in graphene. For this purpose, an Agilent 4156B semiconductor parameter analyzer was used at a measurement current of 100 µA. The distance of the contacts varied from 50 µm to 800 µm, whereby the distance from the contacts was doubled, with a channel width of 115 µm. The results are shown in Figure 3-22.

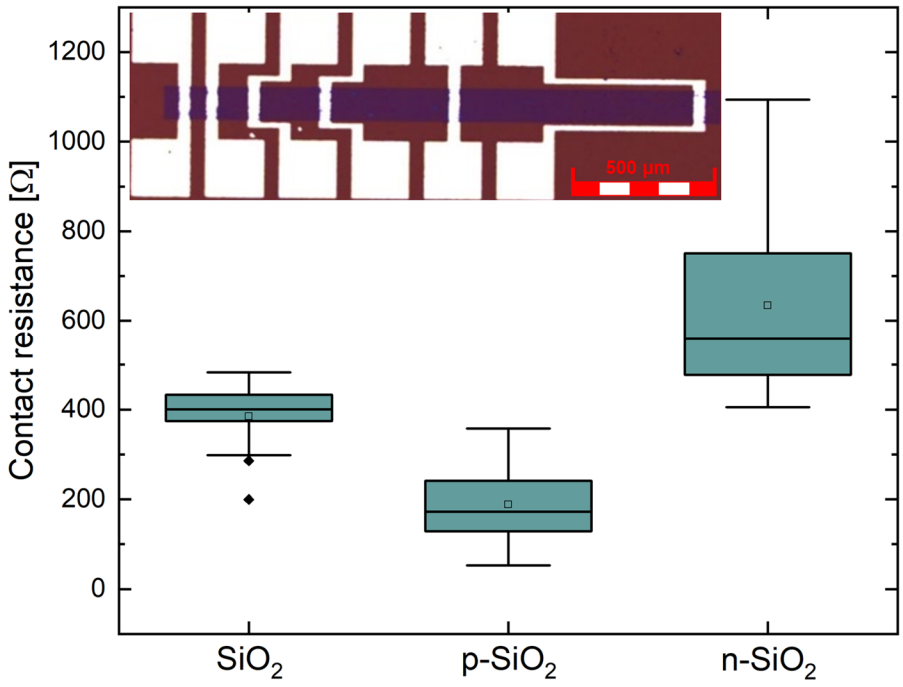


Figure 3-22: Contact resistance between nickel and graphene on SiO_2, p- and n-SiO_2, extracted from TLM measurements, with a micrograph of a TLM structure as inset. It can be seen that the contact resistance is not dependent on the charge carrier concentration in graphene and therefore on the sign and value of the surface charge of the underlying substrates. The reason for this could be polymer residues from the structuring process of the TLM channels, which were detected by XPS measurements (Figure 3-18)

The TLM measurements on the different substrates in Figure 3-22 show that the distribution and value of the contact resistances are not dependent on the surface charge and therefore on the charge carrier density in graphene n ($R_c \propto \sqrt{n^{-1}}$). The average contact resistance between nickel and graphene is approximately 385 ± 77 Ω on SiO_2, 188 ± 92 Ω on p-SiO_2, and 634 ± 226 Ω on n-SiO_2. The data show that the contact resistance is not a function of the surface charge of the substrates, because the contact resistance of graphene on SiO_2 (high n in graphene) should be lower than on the doped oxides (n small in graphene). The reason for this could be polymer residues after photolithography (Figure 3-18), since these form a thin isolating layer between the graphene and the nickel electrodes and thus dominate the contact resistance.

Due to the limitation of the remaining polymer contamination during the structuring process, it cannot be proven that the modified surface charge of n/p-SiO_2 has an influence on the contact resistance between graphene and nickel (or generally metal contacts) compared to standard SiO_2. Therefore it is necessary to use an improved structuring process to achieve this. For this purpose, contact resistance measurements were carried out at RWTH Aachen University, with an optimized manufacturing process for the contact resistance structure, which results in a low polymer contamination level on the graphene surface. For this purpose, an edge contact is used as contact geometry (nickel and graphene overlap only at the edge of the channel structure), because this process is very contamination-free and should therefore produce low contact resistances. [78], [102]

For the fabrication of the edge contact structures graphene was wet-transferred to the target substrates and cleaned as for the fabrication of the van-der-Pauw and TLM structures in chapter 3.2.2.1. The graphene channels were prepared by oxygen plasma etching at a chamber pressure of 50 mTorr, a plasma power of 10 W, and an oxygen flow of 50 sccm. For the fabrication of the edge contacts, the graphene in the contact area was removed with oxygen plasma and Micro Raman spectroscopy at a wavelength of 532 nm, and a power of 1 mW was used to ensure that the graphene was still present at the edge area providing the edge contact. 25 nm thick nickel contacts were deposited in the contact areas by a sputtering process [78], [102]. As in the TLM measurements with the top contact geometry, no field effect was used and only the influence of the intrinsic graphene properties on the contact resistance was investigated. For calculation of the slope of the V-I curve between two contact pads, the voltage was swept from -0.5 V to 0.5 V in 0.005 V steps, and the channel current I was measured, and from this, the total resistance was determined. From this measurement, the contact resistance was extracted from the linear ratio of the total resistance between two contact pads and the increasing contact distance. The results of the measurements are shown in Table 3-6. [78]

Table 3-6: Comparison of the intrinsic properties of graphene (charge carrier concentration n and sheet resistance R_S at 0 V back gate voltage) and the resulting contact resistance R_C between graphene and nickel. [78]

Substrate	$\mathbf{n}\ [10^{11}\ \mathbf{cm^{-2}}]$	$\mathbf{R_S}\ [\Omega/\square]$	$\mathbf{R_C}\ [\Omega \cdot \mu\mathbf{m}]$
SiO_2	-93.4 ± 5.18	1057.9 ± 236.2	683.3 ± 292.5
p-SiO_2	13.2 ± 8.43	2864.4 ± 1251.1	795.8 ± 314.2
n-SiO_2	21.7 ± 33.8	4021.7 ± 1564.6	1046.6 ± 455.6

The measurement results show that the distribution of the contact resistance and its value in absolute terms is on average dependent on the concentration of charge carriers in graphene on the examined substrates, and thus indirectly dependent on the surface charge. It was found that the average contact resistance of nickel to graphene on the modified oxides with aluminum and ammonia is higher (1046.6 Ω·µm on n-SiO_2 and 795.8 Ω·µm on p-SiO_2) compared to the standard SiO_2 (683.3 Ω·µm). The contact resistance dependence is not exactly consistent with the charge carrier concentration n in graphene. It can be seen that n is slightly smaller on p-SiO_2 (n = 13.2·10^{11} cm^{-2}) than on n-SiO_2 (n = 2.17·10^{12} cm^{-2}). This difference can be explained by the fact that the electrical sheet resistance of the graphene layer is on average lower on n-SiO_2 (R_S = 4021.7 Ω/□) than on p-SiO_2 (R_S = 2864.4 Ω/□). The higher electrical sheet resistance and charge carrier concentration of graphene on n-SiO_2 than on p-SiO_2 could be explained by an initial lower graphene quality because contamination and defects during transfer and processing can lead to an increase in these parameters.

3.2.3 Conclusion

Modifying SiO_2 with the diffusion of aluminum and ammonia successfully manipulated the surface charges compared to normal SiO_2. It was found that these surface charges are not stable in plasma processing steps. This problem can be avoided by using transfer methods, which do not require a plasma process during transfer [71]. Similarly, the electrical properties of graphene could be manipulated by the modified oxides. It has been shown that graphene on the modified substrates shows a very small variation in charge carrier concentration and shifts the charge neutrality point close to 0 V (low charge carrier concentration). As a consequence, the intrinsic electrical sheet resistance of graphene on p/n-SiO_2 without an applied back gate is higher than on normal SiO_2. Also, the charge carrier mobility in graphene on the modified oxides is smaller compared to graphene on standard SiO_2 due to the larger number of surface charge states, which

act as scattering centers and thus reduce the charge carrier mobility in graphene. Contact resistances between graphene and nickel have shown that the contact resistance shows the same behavior as the electrical sheet resistance, which is higher between graphene and nickel on the modified oxides compared to standard SiO_2. [78]

It has been shown that the influence of aluminum and ammonia in SiO_2 affects the electrical properties of graphene. Charge compensation in graphene could be achieved by encapsulation to prevent the influence of the atmosphere on the electrical properties [103]. Since the encapsulation layers also have a certain surface charge (depending on the material), this can be compensated by the substrate and thus ensure charge neutrality in graphene. Figure 3-23 shows a process flow as a schematic example using normal SiO_2 as substrate (positive surface charge) and the subsequent diffusion of aluminum, which was deposited via Atomic Layer Deposition (ALD), in the active areas to create a negative surface charge. If the graphene is transferred to the substrate without plasma processing and encapsulated with ALD SiO_2, the positive charge of the ALD SiO_2 layer and the negative charge of the n-SiO_2 substrate compensate for each other.

The encapsulated graphene is nearly charge neutral after contacting in the active region and the passive contact region. The majority of charge carriers are electrons due to the positive SiO_2 surface (Table 3-6). This leads to a high charge carrier concentration under the contact and thus a low contact resistance to the metal (for nickel see Table 3-6) and a negligible charge carrier density in the active region (near the Dirac point). Thus, in the case of a transistor, the graphene device can be switched at low power (since the applied back gate voltage is low) and negligible power is dissipated at the contact due to the low contact resistance.

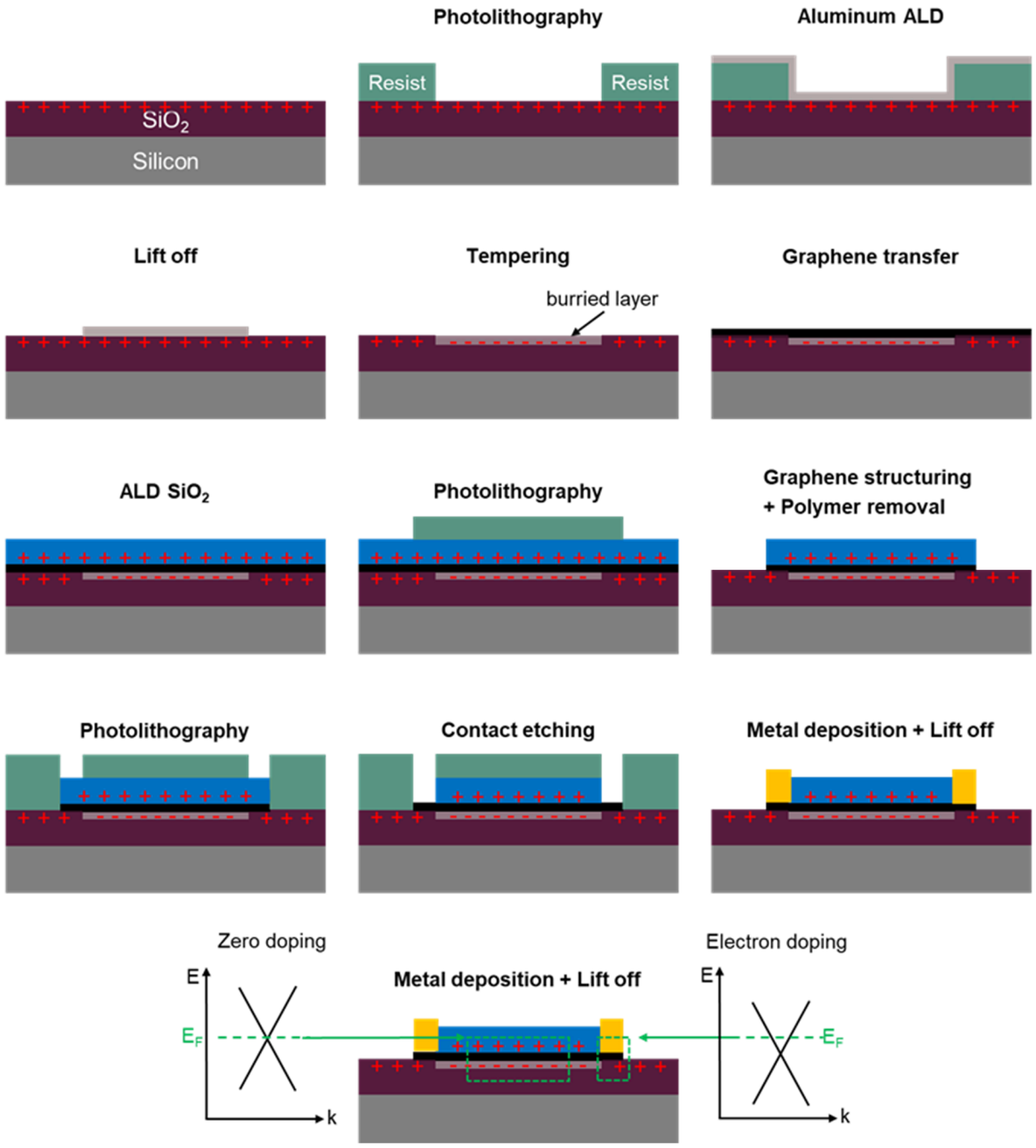


Figure 3-23: Process flow for the creation of an encapsulated graphene device with an aluminum diffusion layer for charge compensation in the active area below the graphene channel. The sequence is from left to right and from top to bottom. Below the process flow a graphene-device is shown with the respective fermi energies in the active area (encapsulated graphene) and passive area (contact region).

4. Performance of graphene-based devices

In this chapter, the performance of graphene-based devices in CMOS-compatible environments is investigated. In this case, a Hall sensor is used as a demonstrator since the electrical properties of graphene can be extracted from it. In section 4.1, the feasibility of Hall sensors based on freestanding graphene and their electrical properties and performance are investigated. Furthermore, in section 4.2, the performance of encapsulated graphene-based Hall sensors is investigated and the influence of the direct environment is analyzed.

4.1 Freestanding graphene-based Hall sensors

In this section, the fabrication and electrical characterization of a free-standing graphene-based Hall sensor are investigated. This is achieved by transferring and structuring a CVD graphene layer onto a Hall sensor support structure and the electrical extraction of the characteristic Hall sensor parameters.

4.1.1 The manufacturing process of the Hall sensor support structure

The Hall sensor support structure serves as a substrate for the graphene which consists of underlying cavities and contact pads. The development of the Hall sensor support structure was not part of this work, but in the following, the manufacturing process of the support structure and its functionality are discussed.

Figure 4-1 a) schematically illustrates the process steps for the production of the Hall sensor support structure [16]. Initially, trenches were etched into an 8" silicon wafer for the stabilization of the sensor structure and filled with SiO_2 via CVD (Chemical Vapor Deposition) (1). The SiO_2 serves as a protection layer for the polysilicon from reactive ion etching in step 8, which was subsequently deposited via APCVD (Atmospheric Pressure CVD) (2). Since the polysilicon layer is not homogeneously flat on the surface due to the fill-up of the trenches, the top layer was removed up to the SiO_2 surface via chemical mechanical polishing (CMP) and then a thin

polysilicon layer was deposited again via APCVD (3). In the following, a thin nitride layer was deposited over PECVD (Plasma Enhanced CVD) and then etched with phosphoric acid at the active sensor structure and the contact hole region (4). At the active sensor structure, the polysilicon layer was also removed via KOH etching to expose the underlying dioxide (4). [16]

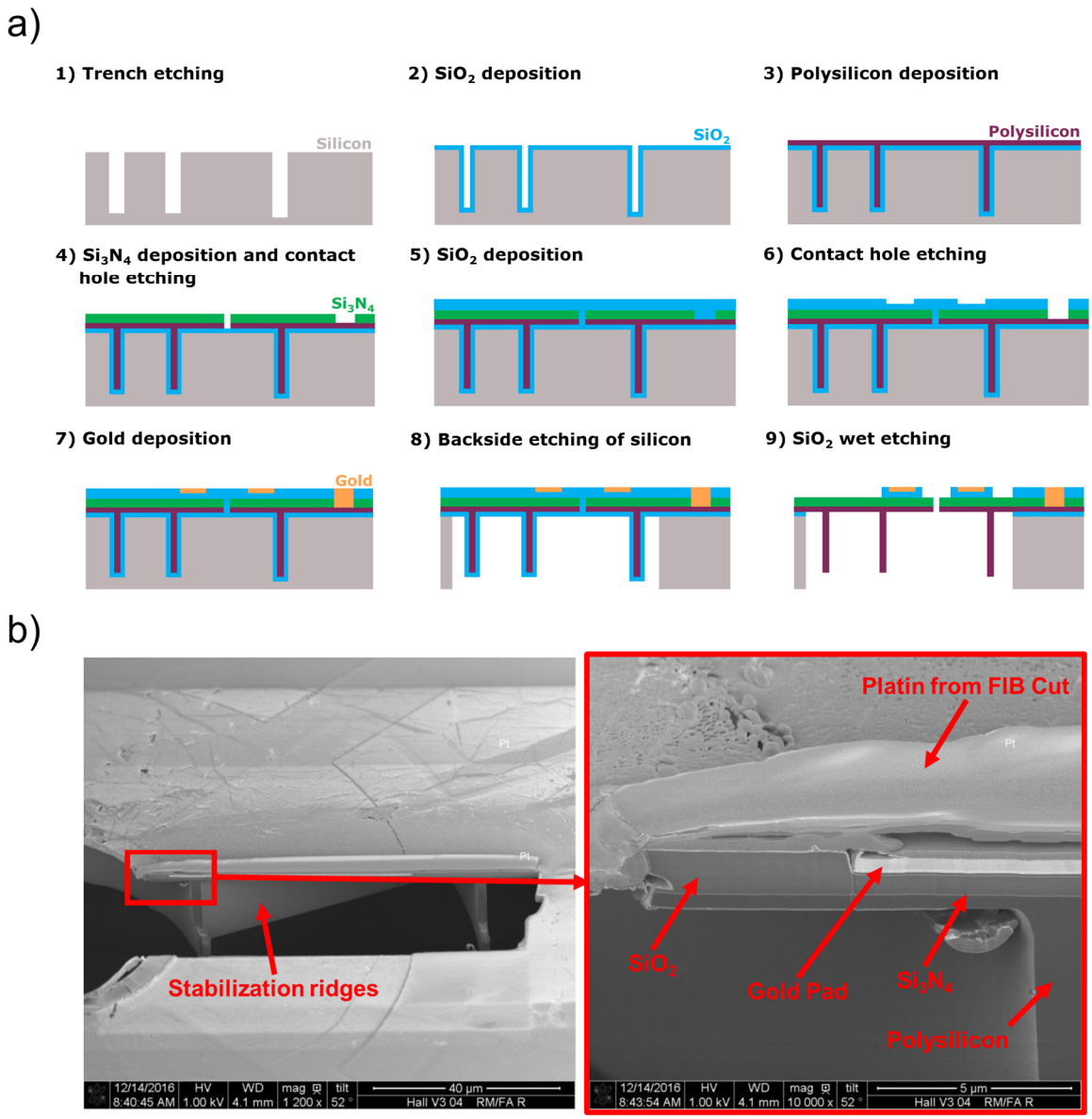


Figure 4-1: Schematic process sequence for the fabrication of the Hall sensor carrier structure in a) and a corresponding FIB cut results of the Hall sensor structure on the support carrier in b). [16]

In the next step, a SiO_2 layer was deposited via CVD (5) and then removed with hydrofluoric acid (HF) to expose the contact pads (6). Then a thin gold layer was deposited in the contact area, which serves as a contact metal (7). Subsequently, the silicon layer and the dioxide layer at the

trenches were removed via reactive ion etching (Bosch etching) from the back side to create the cavity (8). Finally, the dioxide was removed with HF to expose the structure (9). In Figure 4-1 b) a FIB cut of the Hall sensor support structure with the corresponding explanations of the individual layers and structures is shown. [16]

4.1.2 Preparation of the graphene membrane

The graphene membrane, which acts as an active sensor element, was initially located on a polymer substrate and was coated with PMMA and supplied by Graphenea (Easy Transfer Graphene). The polymer carrier, which acts as a sponge, was sprinkled with DI water until it was completely soaked. Thus the graphene layer with the PMMA carrier can be easily removed by immersion in a water bath and picked up with the target substrate, in this case, the Hall sensor support structure. [16]

The Hall sensor support structure was chemically pre-treated to modify the adhesion of the graphene membrane and prevent the membrane from sinking into the cavity and therefore cracking of the membrane due to high mechanical stresses. There were two methods used for the pre-treatment and the improvement of the adhesion between graphene and the support structure. In the first method, the Hall sensor carrier structure was treated with oxygen plasma for 120 s at a power of 50 W and an oxygen flow of 20 sccm with the plasma system MyPlas from Plasma Electronics to hydrophilize the surface of the support structure and at the second method, an hydrofluoric acid dip of the support structure was done for the hydrophilization of the surface. In addition to the hydrophilization effect, the surface (which consists mainly of SiO_2) was slightly etched by the hydrofluoric acid and thus the surface roughness of the support structure has been increased. Furthermore, fluorine bonds have been formed on the SiO_2 surface, which forms induced charges in the graphene surface. The effects of increased roughness and induced charges increase the adhesion energy of the graphene layer to the substrate and therefore lower the possibility that the membrane sinks into the cavity. [16]

After the transfer of graphene onto the support structure, a part of the samples was air-dried at room temperature for 6 h and the remaining parts were dried with a critical point dryer (CO_2) at a temperature higher than 31°C and a pressure higher than 73.8 bar for 1 h. After the drying process, the PMMA layer was removed by different techniques to find the optimal process. For this purpose, the PMMA from the air-dried samples was for some parts removed by dipping in

acetone (standard wet transfer), for other parts the PMMA was removed by thermal decomposition in an RTP (rapid thermal processing) chamber at 400°C for 2 h in a nitrogen atmosphere at a heating/cooling rate of 20 °C/s, and for the rest of the samples the PMMA was removed by acetone steam for 12 h. PMMA removal via the three removal techniques mentioned above was also done for the samples dried via the critical point dryer. During the removal of the PMMA layer by the acetone dip, the support structure with the graphene was immersed perpendicular to the acetone surface to reduce the capillary force of the surface on the graphene membrane, as the graphene membrane can be destroyed by it, and ensuring a higher yield. In the case of the acetone vapor, the sample was positioned so that the graphene faced the acetone with a small angle. Therefore, condensed acetone, which has already dissolved PMMA, can run off over the sample holder and avoid acetone droplet formation. These droplets can cause the graphene membrane to crack due to their weight. [16]

To ensure complete coverage of the Hall sensor support structure with graphene, it is essential to optically inspect the transferred graphene on the carrier structure. This was accomplished by using an Olympus model LEXT OLS4000 3D laser microscope, with a spatial resolution of 16x16 µm and a magnification of up to 17,280x. A diode laser with a wavelength of 405 nm was used for confocal laser imaging. The focal plane of the laser can be varied in the z-direction so that a 3D image of the sample can be acquired. The image depth of focus varies between 1 nm and 10 nm depending on the nature of the sample surface (e.g. the depth of focus decreases for highly reflective surfaces). The height profile of the graphene membrane was calculated from the optical interference of the laser with the graphene and the carrier structure at a scanning speed of about 100 nm/s. From the height information of the optical measurements, the homogeneity of the transferred graphene layer can be analyzed to ensure an optimal device performance of the graphene-based Hall sensor (Figure 4-2 a)). [16]

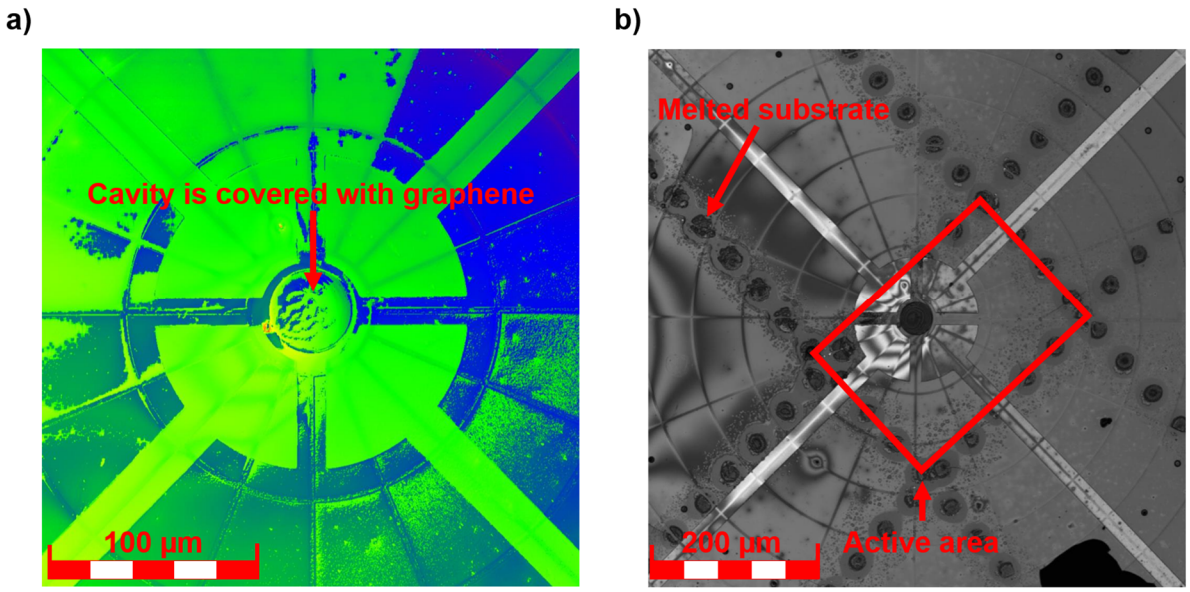


Figure 4-2: Optical characterization of a graphene-based Hall sensor structure. a) Height profile of a graphene membrane, which was determined by laser scanning microscopy. From the image information, it can be seen that the membrane is continuous. b) Laser-structured graphene on a Hall sensor structure. It can be seen that the laser structuring leads to a melting of the substrate due to its low thermal mass. [16]

As the entire Hall sensor support structure was covered with graphene, all contacts between the individual structures were electrically shortened and preventing the operation of the graphene-based Hall sensor. Therefore, it is necessary to separate the active and passive device areas via a structuring of the graphene layer. Three structuring methods were used to separate active and passive areas, one mechanical and two optical methods. During mechanical structuring, the graphene was removed by scratching, but this led to high stresses in the graphene layer and thus to the cracking of the graphene membrane. The second attempt was to structure the graphene via photolithography processes, as was done in chapter 3.2.2.1. It has been shown that during photoresist deposition via spin coater, the graphene membrane also cracks due to the high mechanical stress during spin coating. The third structuring approach was to remove the graphene via laser radiation since this non-contact process did not induce any mechanical stresses in the membrane. For this, a pulsed ytterbium fiber laser from Han's Laser Technology Industry Group with a wavelength of 1064 nm, a peak power of 500 mW, and a cutting frequency of 40 kHz for 10 ns was used. The total pulse duration is 600 ns, but at the remaining 590 ns the emission of the laser is much weaker at undefined power. A laser-structured graphene Hall sensor structure is shown in Figure 4-2 b). [16]

After process analyzation, the optimal process sequence for the production of graphene-based Hall sensors is the wet chemical transfer of the graphene with a PMMA carrier after previous

oxygen plasma treatment of the Hall sensor support structure. The graphene membrane is then dried under atmospheric conditions and the PMMA carrier is subsequently removed with acetone vapor for 12 hours. Besides the optimization of the process parameters, a very low yield of approximately 0.2 % could be achieved, since about 1000 devices were produced and out of these 2 devices could finally be characterized. [16]

4.1.3 Electrical performance of freestanding graphene-based Hall sensors

Electrical parameters such as charge carrier mobility, charge carrier concentration, voltage, and current-dependent sensitivities, which are characteristic of Hall sensor elements, are determined in this chapter with the manufactured free-standing graphene-based Hall sensors from subchapter 4.1.2. The electrical measurements were performed in a vacuum chamber with an Agilent 4156B semiconductor parameter analyzer. The Hall sensor structures were contacted with four electrical tungsten manipulator needles which were connected to a semiconductor parameter analyzer. The magnetic field was generated by a custom-made copper coil below the Hall sensor structures, and was regulated by the current flow in the coil with a maximum magnetic field of 80 mT, which was generated at a maximum current flow of 15 A. A commercial Infineon TLE4997E2XALA1 Hall-effect sensor powered by a Kethley2000 power supply was used as the reference magnetic field sensor. The charge carrier mobility and concentration were determined at an applied voltage of 1 V and an applied current of 1 mA, while the magnetic field was swept from 0 to 80 mT. The characteristic parameters such as charge carrier mobility μ, charge carrier concentration n, magnetic offset B_{off} and current and voltage-dependent sensitivities S_I and S_V were determined by equations 4-1 to 4-4 (with V_H as the Hall voltage and V_{off} as the Hall voltage without magnetic field). [16]

$$S_V = \frac{1}{V_C}\left|\frac{\partial V_H}{\partial B}\right| = \mu \qquad 4\text{-}1$$

$$S_I = \frac{1}{I_C}\left|\frac{\partial V_H}{\partial B}\right| \qquad 4\text{-}2$$

$$n = \frac{I_C}{e \cdot |\partial V_H / \partial B|} \qquad 4\text{-}3$$

$$B_{off} = \frac{V_{off}}{S_V} \qquad 4\text{-}4$$

As mentioned in the previous subchapter 4.1.2, the yield was 0.2 %, which corresponds to a measurable number of devices of 2. These two devices have an active free-standing graphene area of 78.5 µm² and 314 µm², and a passive graphene area on the supporting substrate of 50,974 µm² and 50,891 µm², as a result of laser structuring. The characteristic Hall sensor parameters of the two devices are listed in Table 4-1. [16]

Table 4-1: Extracted Hall sensor parameters from the Hall-effect measurements [16]

Hall sensor parameter	A_{active} = 78.5 µm²	A_{active} = 314 µm²
$\mu\ [cm^2/(V \cdot s)]$	6,240	11,900
$n\ [10^{11}\ cm^{-2}]$	10	-5.33
$S_V\ [V/(V \cdot T)]$	0.62	1.19
$S_I\ [V/(A \cdot T)]$	624	1190
$B_{off}\ [mT]$	16	48

Figure 4-3 shows the Hall voltage dependence of the two Hall sensor structures with graphene as an active sensor element with an applied magnetic field. [16]

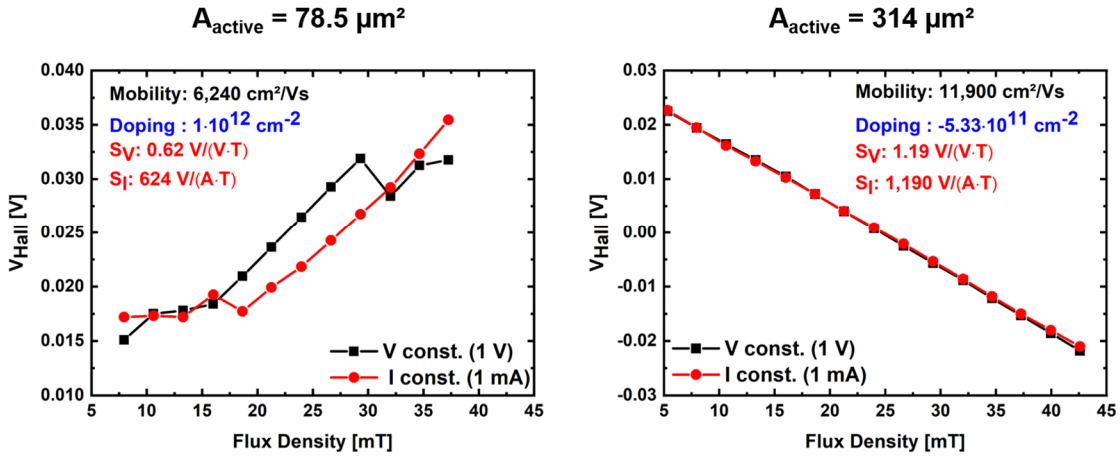


Figure 4-3: Hall effect measurements of suspended graphene devices. Sample 1 (left) shows a lower charge carrier mobility and therefore lower voltage and current-dependent sensitivity compared to sample 2 (right). The reason is a higher cavity area in sample 2 (314 µm²) than in sample 1 (78.5 µm²). A higher doping concentration in sample 1 is an indicator of a higher proportion of substrate doping due to a higher passive graphene area. [16]

From the measured data it can be seen that the total charge carrier mobility of graphene over the cavity and on the substrate is greater with a larger active membrane area (A_{active}) compared to the passive graphene area, which is limited by laser structuring ($A_{passive}$ is similarly large on both devices, 50,974 µm² and 50,891 µm²). The measured Hall voltage of the devices is a function of

the mean value of the charge carrier concentration of the free-standing graphene and the graphene on the substrate ($V_H = \langle n \rangle^{-1}$ [104]), which is the reason that the Hall voltage respectively the charge carrier mobility is greater with the larger active membrane area (μ = 6,240 $cm^2/V{\cdot}s$ at A_{active} = 78.5 μm^2 and μ = 11,900 $cm^2/V{\cdot}s$ at A_{active} = 314 μm^2), since the charge carrier concentration is smaller in the free-standing graphene layer ($n = 10^{12}$ cm^{-2} at A_{active} = 78.5 μm^2 and $n = -5.33{\cdot}10^{11}$ cm^{-2} at A_{active} = 314 μm^2) because no doping influences are induced by substrate surface states. Additionally, the position of the contacts has also an influence on the measured charge carrier mobility, because contacts that are located outside of the active area give a lower Hall mobility value than contacts inside the active area. [16], [105]

The electronic response of Hall sensors is specified by the current and voltage sensitivity and the magnetic offset. The voltage and current sensitivities of the two measured graphene-based Hall sensors are 0.62-1.19 V/(V·T) and 624-1190 V/(A·T). These values exceed the performance of commercial silicon-based CMOS Hall sensors based on the Hall effect (0.07 V/(V·T)) and 0.07 V/(A T) for S_V and S_I) [106], which can be derived from the higher charge carrier mobility in free-standing graphene. Commercial Hall sensors show magnetic offsets in the range of 10 mT for the same sensor geometries (van-der-Pauw) [107], which is comparable to the measurements results from Table 4-1. The origin for this offset is the non-symmetric geometry of the active graphene area due to the misalignment of laser structuring and the in-plane tension of the graphene membrane, which is also present in CMOS Hall devices [108]–[110] (Table 4-1). [16]

4.1.4 Conclusion

The manufacturing process of suspended graphene-based Hall sensors from subchapter 4.1.2 is not suitable for mass production due to the low yield of 0.2 % and therefore it is not possible to make a statistical statement about the electrical performance. From the results of the two sensor devices of subchapter 4.1.3, it has been shown that the electrical parameters of Hall sensors based on free-standing graphene can exceed those of silicon-based ones [16]. The attempt to fabricate suspended graphene-based Hall sensors on existing support and contact structures has proven to be unreproducible and a different approach is needed to produce high-quality Hall sensors with high yield. The limiting factor during membrane production is the low mechanical resistance of the graphene against the capillary forces of liquid media during transfer and the gold contact structure topography at the edge of the membrane, which causes the graphene to crack.

A dry transfer approach (chapter 3.1, [111]) in combination with metal contacts, which are not directly located at the cavity, could improve the yield of graphene-based Hall sensor production.

A disadvantage of suspended graphene-based Hall sensors is that they may exhibit cross-sensitivities to atmospheric conditions [112] and need to be packaged in a vacuum. Inert gases cannot be used in packaging because they are sensitive to temperature fluctuations (expansion, compression) and thus deflect the graphene membrane and create mechanical stress, affecting the sensor signal. Due to the lack of a packaging process for graphene membranes under vacuum and the low yield of the fabrication process, no statistical analysis of suspended graphene-based Hall sensors can be made. Therefore, to investigate the current state of development of graphene-based Hall sensor technology, it is necessary to package the graphene layers in a production-ready CMOS-compatible environment for a higher yield [16]. The fabrication, electrical and optical characterization, and statistical evaluation of the resulting Hall sensor parameters are discussed in the following chapter 4.2.

4.2 Encapsulated graphene-based Hall sensors

In this chapter, packaged graphene-based Hall sensors in a dielectric environment are characterized and statistically evaluated. The aim is to investigate the electrical properties of graphene-based Hall sensors regarding their sensitivity (charge carrier mobility and concentration) and power consumption (electrical sheet resistance). The influences of the direct dielectric environment and the manufacturing process on the quality of graphene-based Hall sensors are investigated as well as the dielectric electrical properties of the encapsulation layer (breakdown field strength, leakage current).

4.2.1 Device preparation

For the production of graphene-based Hall sensors, commercial graphene from ACS Materials was transferred to Si_3N_4 via wet transfer [79]. LPCVD Si_3N_4 was used as a substrate because in chapter 3.2.2.2 the highest charge carrier mobility μ was measured and therefore the highest voltage sensitivity S_V can be achieved ($S_V = \mu$). For the experiments, 60 nm and 205 nm Si_3N_4 on highly doped silicon (ρ_S = 2.3 mΩ·cm) were used to vary the range of the applied voltage at higher layer thickness and to change the voltage-related charge carrier injection n ($n \propto C_{Gate} \propto 1/d$). After transfer, the graphene was cleaned with acetone and isopropanol and then thermally annealed at 400 °C for 2 h in a vacuum to remove residual polymer contaminations. A 60 nm ALD Al_2O_3 was subsequently deposited on graphene in a furnace with TMA (trimethylaluminum) and H_2O as precursor gases with a pulse duration of about 10 s per precursor injection phase. The ALD Al_2O_3 layer is used as a hard mask during the structuring process to minimize polymer encrustation (subchapter 3.2.2.1) and as a protection against the atmosphere to prevent undesired doping influences [112]. Nickel alignment markers were first generated by i-line photolithography with a mask aligner MA56 from Karl Süss and a positive resist S1805 from Microchem. The photoresist was exposed for about 80 s and then developed for 90 s in a TMAH-based developer (AZ 726 MIF from Microchemicals). A 10 nm thick nickel layer was then deposited on the samples by physical vapor deposition and the alignment markers were created by a subsequent lift-off process. In the following, the van-der-Pauw measurement structures, which are used for the measurement of the Hall sensor parameters, were processed by photolithography with the same process as for the alignment markers and subsequently etched with diluted hydrofluoric acid

(approx. 0.1 % HF) to remove the ALD Al_2O_3 layer. Afterwards the exposed graphene was removed with an oxygen plasma treatment with an oxygen flow of 20 sccm at a power of 50 W for 30 s in a MyPlas PECVD system from Plasma Electronics. The residual resist was then removed with acetone and isopropanol in combination with an ultrasonic treatment. Finally, the metal contacts were created by photolithography with the same process as for the alignment markers, followed by removing the ALD Al_2O_3 layer with diluted HF and the deposition of 15 nm nickel via physical vapor deposition, and exposed by a lift off process. In addition to the four contacts of the van-der-Pauw geometry, a top electrode was positioned above the ALD Al_2O_3 cross, with an area slightly smaller than the encapsulated graphene to prevent electrical short circuits at the edges due to misalignment during the photolithography process. The top electrode was used to characterize the electrical properties of the ALD Al_2O_3 layer (breakdown field strength, leakage current).

Figure 4-4 a) shows an optical image of the final van-der-Pauw structure with the encapsulated graphene by ALD Al_2O_3. In addition, a FIB cut in the active region (60 nm Si_3N_4 + graphene + 60 nm ALD Al_2O_3 + 15 nm nickel) was prepared and analyzed with scanning electron microscopy (SEM) (Figure 4-4 b). It can be seen that the grown and processed layers of the final test structure partially cannot be resolved due to their small thickness (15 nm nickel). The grown ALD Al_2O_3 layer is thinner than the expected 60 nm (19.2 nm) because the SEM analysis shows a clear optical transition between the 60 nm thick Si_3N_4 and the ALD Al_2O_3, which are separated from the graphene layer. This suggests that the nucleation of the ALD Al_2O_3 layer on graphene is in this case significantly lower than on silicon, for which the process was optimized and calibrated.

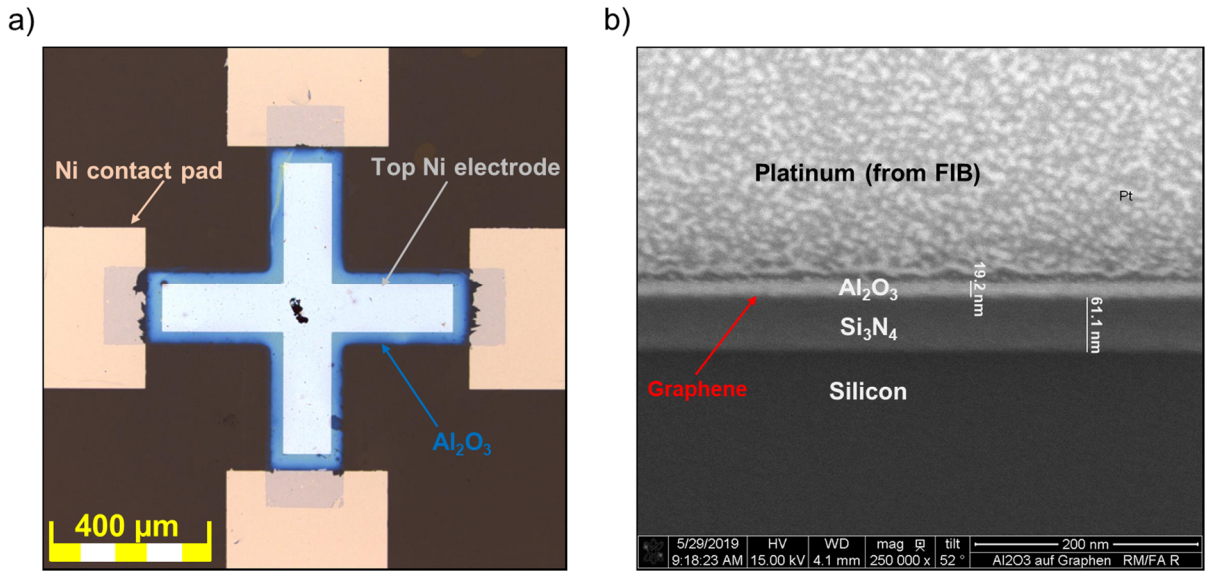


Figure 4-4: Micrograph of an encapsulated graphene-based van-der-Pauw test structure with a nickel top electrode in a), and an SEM cross-section image of a FIB cut in the active region in b).

For the characterization of the encapsulated graphene-based Hall sensors in a van-der-Pauw measurement geometry with a nickel top electrode, electrical sheet resistance and mobility measurements in combination with electric field effect measurements were performed as described in chapter 3.2.2.2, using the silicon substrate as a back gate electrode. The influence of the ALD Al_2O_3 layer on the electrical properties of graphene was investigated by analyzing the Dirac point voltage for encapsulated and non-encapsulated (unprocessed) graphene. For non-encapsulated graphene, a wet transferred 6-inch graphene wafer on SiO_2 was purchased from Graphenea and electrically characterized using the Eddy Current Method with the EddyCus TF map 2525SR system from Suragus, which measures the electrical sheet resistance of the graphene layer. The defect density and the number of layers of graphene were statistically determined by Raman spectroscopy. In a further step, breakdown voltage measurements on the grown ALD Al_2O_3 layers on top of graphene were performed to analyze the electrical quality of the isolator. For this purpose, the voltage was applied between the top electrode and graphene, and the leakage current was measured until the breakdown.

4.2.2 Characterization of encapsulated graphene-based Hall sensors

The integrated graphene layers were electrically investigated via the van-der-Pauw test structure to determine the sheet resistance at the Dirac point and the charge carrier mobility and charge carrier concentration. The charge carrier mobility μ_{DTM} was calculated using the direct transconductance method ($\mu_{DTM} = g_m \cdot A/C_g$), with $g_m = \partial\sigma/\partial V_g$ as transconductance, A as the active area of the van-der-Pauw cross ($L = W$), σ as the electrical conductivity of graphene ($\sigma = 1/R_s$), V_g as the voltage between the back gate and graphene and C_g as gate-capacitance ($C_g = \varepsilon_0 \varepsilon_r A/d$), with d as Si_3N_4 thickness (d = 60 nm). The charge carrier concentration in graphene was not controlled by the top gate (via Al_2O_3), because the dielectric strength measurement destroys the isolating layer and therefore no electrical measurements cannot be performed afterward.

Figure 4-5 a) shows the electrical sheet resistance statistic of the encapsulated (processed) graphene layers, which was extracted from the van-der-Pauw measurements, in comparison to the electrical sheet resistance of non-encapsulated (unprocessed) graphene from the Eddy Current measurements. The electrical sheet resistance varies from 240.19 Ω/□ to 1,867.18 Ω/□ with an average value of 856.98 Ω/□. The electrical sheet resistance of the processed graphene layers has a high variance, which is caused by the thickness variation of the graphene during its growth process (single and multilayer domains), the contamination during transfer, and the effect of the transfer on the quality of graphene by handling (defects). The processing of the graphene during the fabrication of the test structures plays also a role, in particular the influence of the encapsulation process of the graphene with ALD Al_2O_3, which could lead to an increase in defect formation. To make the influence of the encapsulation process visible, a wet transferred 6-inch wafer on SiO_2 was purchased from the manufacturer Graphenea as a reference and measured contactless with the Eddy Current method, and the extracted sheet resistance data is also shown in Figure 4-5 a). Before processing the wet transferred graphene had electrical sheet resistance fluctuations in the range of 283.54 Ω/□ to 526.69 Ω/□, with an average value of 517.84 Ω/□. Compared to the electrical sheet resistance values after processing, with an average value of 856.98 Ω/□ and a fluctuation from 240.19 Ω/□ to 1,867.18 Ω/□, the growth process of the ALD Al_2O_3 layer on the graphene and its impact on the electrical quality is not negligible. The reason for this could be the formation of covalent bonds between the Al_2O_3 and the graphene edges from defects so that free electrons in the graphene system are localized by covalent bonding and no longer contribute to the electrical transport, which leads to an increase in electrical sheet

resistance. But this is only an assumption, the exact reason for the higher fluctuation of the sheet resistance, accompanied by the degradation of the graphene quality is not known.

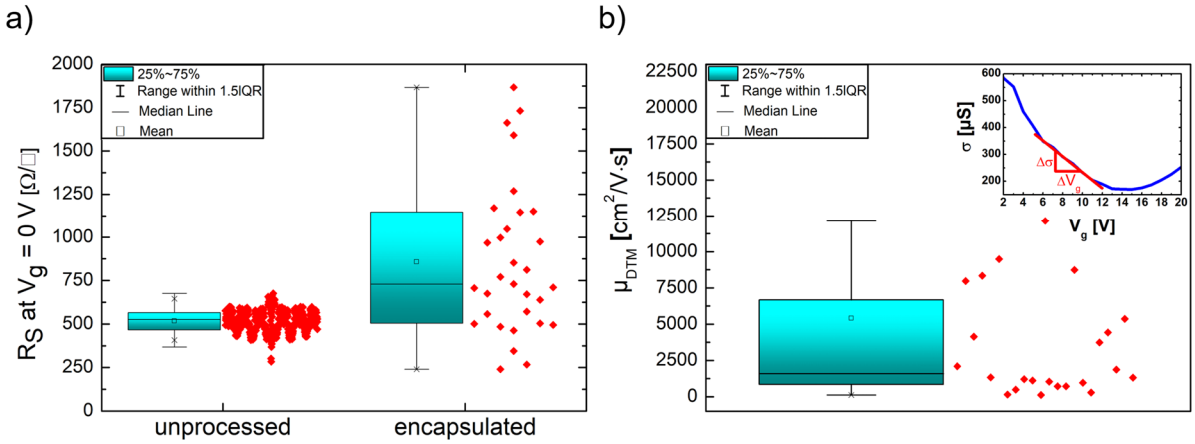


Figure 4-5: Electrical sheet resistance and charge carrier mobility of unprocessed and encapsulated graphene. a) Zero-biased electrical sheet resistances of unprocessed and encapsulated graphene; b) Charge carrier mobility from direct transconductance measurements extracted from the sheet resistance measurement results. The inset of the graph shows the point from the measurement where the transconductance mobility is calculated.

Figure 4-5 b) shows the statistical distribution of the charge carrier mobility from direct transconductance measurements. The inset of the graph shows an example of an electrical conductivity measurement ($\sigma = 1/R_s$) as a function of the applied back gate voltage from 2 V to 20 V. The extracted charge carrier mobility was calculated at the point with the highest slope in the back gate voltage-dependent electrical conductivity measurement. The encapsulated graphene layers have a charge carrier mobility variation of 121.98 cm²/V·s to 12,187.50 cm²/V·s, with a median value of 1,597.58 cm²/V·s. The extracted transconductance measurement values are usually below the real charge carrier mobility, due to the ignorance of contact resistances [113]. The median charge carrier mobility of 1,597.58 cm²/V·s is lower than for 2D electron gases like GaAs with 8,500 cm²/V·s and InAs with 33,000 cm²/V·s [10]. The measurements show a high variation of the charge carrier mobilities, which is mainly due to the processing influence on the graphene, and is consistent with the electrical sheet resistance measurements from Figure 4-5 a).

The charge carrier mobility μ for Hall sensors is important as it determines the voltage-dependent sensitivity S_V ($\mu \propto S_V$). This means that Hall sensors, which would be manufactured on a graphene basis, have a lower voltage-dependent sensitivity to materials like GaAs and InAs. It should be noted that these materials are not CMOS compatible and cannot be integrated into existing silicon-based technologies. Typically, devices based on non-CMOS compatible materials are combined with silicon technologies via wafer bonding [114], and integration takes place via the bonding

interface. This is not the case with graphene so this is an advantage because silicon-based technologies can be adopted here without the integration of new technologies based on graphene. The charge carrier mobility in graphene is limited by the surface properties of the used materials and its growth processes for the encapsulation of graphene [115]. The interaction of the surface of the encapsulation layer with graphene, which is dominated by the surface charge density and the chemical bonding mechanism of the encapsulation material to graphene, plays a significant role in the quality of the encapsulated graphene layer, as shown in the electrical sheet resistance measurement distribution in Figure 4-5 a). This problem can be solved by selecting materials that have a low surface charge density and a low surface roughness. It has been shown that the charge carrier mobility in graphene increases with a substrate surface providing these properties [78], [116]. As the direct growth of encapsulation layers influences the electrical properties of graphene drastically (Figure 4-5 a)), the usage of protective layers that have only van-der-Waals interactions with graphene could lower the interaction with it. Previous works have shown, that transferred layers based on boron nitride improve the electrical performance of graphene [7].

The results from electrical sheet resistance and charge carrier mobility measurements have shown a high variation, which is due to the ALD Al_2O_3 encapsulation layer as concluded from Figure 4-5 a). To confirm the high electrical measurement variation due to defect formation in graphene by covalent bonds to Al_2O_3, Raman spectroscopy measurements were performed on the individual devices. For the analysis of the chemical structure of the integrated graphene layers in the van-der-Pauw test structure, the intensities of the characteristic Raman modes in graphene (D-, G- and 2D mode) were recorded by Raman spectroscopy and the ratios of I_D/I_G (defect density [117]) and I_G/I_{2D} (number of layers [118]) were formed. For the measurement, a Raman spectroscopy system from Horiba with a laser excitation wavelength of 532 nm (2.33 eV) was used with a spot size of ~1.05 µm in the x and y directions. The spot size was obtained by using a 100x objective with a long working distance focusing lens with 0.21 mm and a numerical aperture of 0.90. A single-mode optical fiber and a spectrometer with a grating of 1,800 lines/mm were used for the detection of the Raman modes. All measurements were performed with linear laser polarization with a power density of 5.77 mW/µm^2, an integration time of 1 s and an accumulation number of 2 (specific setting parameter of the Raman system). The intensities of the D, G and 2D mode were extracted from a Lorentzian fit function. Figure 4-6 a) shows the sum of the intensity ratios of the individual graphene test structures.

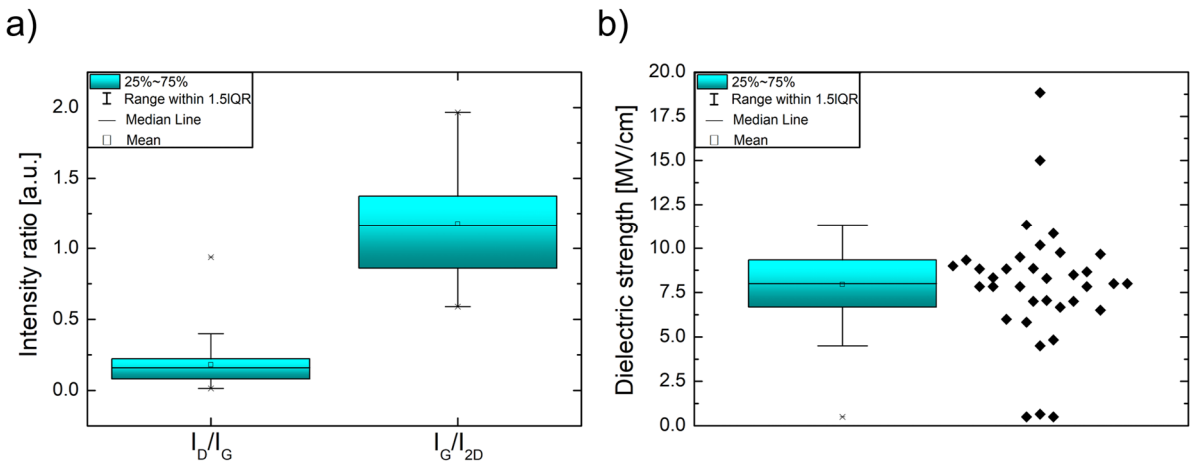


Figure 4-6: Quality of encapsulated graphene and encapsulation layer. a) Extracted intensity ratios of D- and G-mode (defect density) and G- and 2D-mode (number of layers) from the Raman spectra of the encapsulated graphene layers. An average I_D/I_G ratio of 0.180 and I_G/I_{2D} ratio of 1.18 can be calculated, which indicates that the graphene layers have a high defect density and the layer number extraction cannot be done because it is defect density-dependent; b) Dielectric strength of ALD Al_2O_3 on graphene extracted from breakdown voltage. The measurements show an average dielectric strength of 7.95 MV/cm with a standard deviation of 3.47 MV/cm

The measurements in Figure 4-6 a) show an average I_D/I_G ratio of 0.180 with a standard deviation of 0.166. This indicates that the defect density of the encapsulated graphene layers is non-negligible and increases from its initial zero value before encapsulation because no D-Peak was visible in the Raman Spectra. It can also be seen that the I_G/I_{2D} ratio has an average value of 1.18 with a standard deviation of 0.386. Before encapsulation, the graphene layers have a 2D-mode intensity in most cases higher than the G-mode intensity $I_G/I_{2D} < 1$ but indicates that the graphene layers initially are not only monolayers. This increase in the I_D/I_G ratio and the increase in the I_G/I_{2D} ratio supports the statement, that the ALD Al_2O_3 layer creates defects in graphene and thus increases the intensity of the D-mode. The increase in the intensity of the D-mode also decreases the intensity of the 2D-mode due to defect activation, whereby the phonon backscattering process is no longer elastic and the oscillation of the 2D-mode is suppressed [119].

Finally, the quality of the deposited ALD Al_2O_3 layers on graphene was electrically analyzed. For this purpose, breakdown voltage measurements were performed and the dielectric strength was determined. For the breakdown measurement an increasing potential difference was applied between the top electrode and graphene and the electrical current between the graphene and the top gate was measured. At the point in which the current exceeds the current compliance of 1 mA, the voltage value was detected as a breakdown, since the leakage current is within the range of the device current. The measurement results in Figure 4-6 b) of the dielectric strength show an average value of 7.95 MV/cm with a standard deviation of 3.47 MV/cm. This mean value is in the range of the dielectric strength of ALD Al_2O_3 on silicon and metallic substrates (5.3 - 8.5 MV/cm)

[120]. The electrical properties of ALD Al_2O_3 are comparable to the state of the art, which means that electrical robustness is not a critical parameter for the production of encapsulated graphene-based devices.

4.2.3 Conclusion

In summary, the integration of graphene into CMOS-compatible device environments, especially for Hall sensor fabrication, is currently not as good as conventionally used material systems for Hall sensors. A decisive factor is the quality of the graphene starting material, which is usually grown on copper since the available graphene layers are on average single-layered but have multilayer graphene domains, thus limiting the maximum achievable charge carrier mobility. Furthermore, the encapsulation of the graphene layers is a critical parameter, since it has been shown that the electrical device properties decrease during encapsulation. This was proven by Raman spectroscopy measurements and the extraction of the defect density from the I_D/I_G ratio, which is increased after the encapsulation process. This can be improved by the use of weakly interacting materials, such as h-BN [121]. The electrical robustness of the grown ALD Al_2O_3 encapsulation layers is comparable to conventional ones in standard material systems in the semiconductor industry.

5. Wafer-level integration approach of graphene in industrial semiconductor fabrication

In this chapter, the integration compatibility of thin carbon films in existing CMOS FEOL processes was investigated. Thin carbon layers were investigated instead of graphene because currently the process compatibility concerning contamination (see chapter 3.1.3) is not FEOL compatible and further optimization is required. Further techniques to reduce the contamination level (metallic and organic) of graphene on dielectric substrates exceed the scope of this work and therefore thin carbon layers were used for the integration experiments instead of graphene. This chapter aims to analyze and characterize the influence of semiconductor processes on the electrical properties of carbon-based applications. To realize this, a process flow was developed (chapter 5.1) to integrate thin carbon layers into Hall sensor and TLM structures without influencing them chemically during the fabrication process and thus without changing the electrical properties. Subsequently, the fabricated Hall sensor and TLM structures were electrically and optically examined (chapter 5.2) to investigate the influence of the manufacturing process on the electrical properties of the final structure. For the investigation of the final sensor structure, electrical transmission measurements, Raman spectroscopy, and combined FIB (Focused Ion Beam) and SEM (Scanning Electron Microscopy) measurements were conducted.

5.1 Test structure design and process flow

To investigate the influence of CMOS FEOL processes on the physical and chemical properties of thin carbon layers, Hall sensor structures in a van-der-Pauw geometry were created in which the carbon layer acts as an active sensor material. The process was adapted in such a way that future studies of the process's influence on graphene can be carried out by replacing the carbon deposition process with the graphene transfer process. The carbon-based process flow serves as a blueprint for future graphene experiments, if it meets the FEOL requirements in terms of contamination. Since Hall sensor structures can be used to determine charge carrier mobility and charge carrier concentration of the sensor material, and in the case of graphene they are therefore sensitive to the interface properties, this structure is suitable for the use in quality control of the integration process. From the measured charge carrier concentration and charge carrier mobility

of the sensor material from Hall measurements, conclusions can be drawn about defect formation due to the growth and deposition of the layers, contamination level, and surface charge changes caused by the processed layers. The electrical sheet resistance of the active sensor layer can also be determined by using the van-der-Pauw structure, which is also an indicator for the above-mentioned process influences and can be used to indirectly determine the contact resistance between the carbon/metal interface.

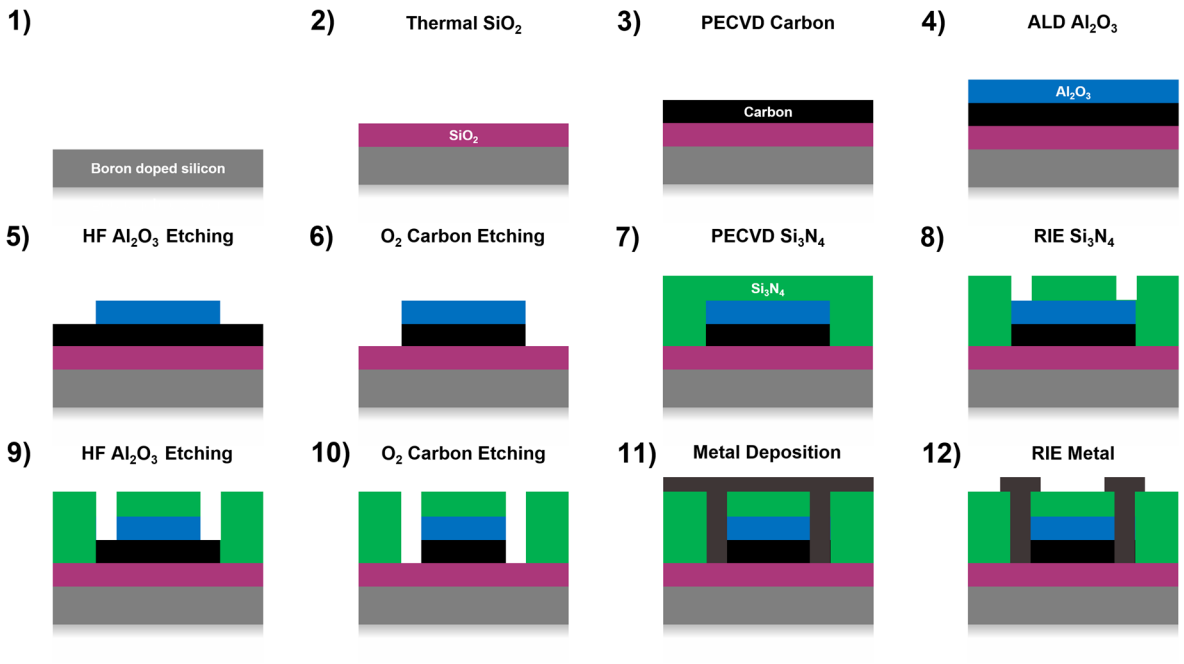
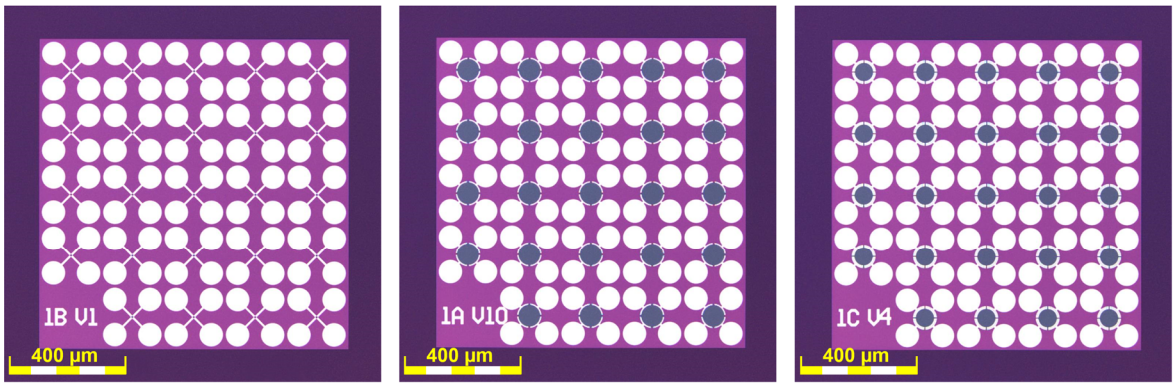


Figure 5-1: Schematic process flow for the fabrication of the carbon-based test structures on the wafer level.

Figure 5-1 shows the schematic fabrication process of the test structures using a Hall sensor structure as an example. All used processes and their parameters have not been adapted to carbon-containing materials and are used in this form for existing silicon technologies. For the fabrication of the test structures a 300 nm thick SiO_2 layer on p-doped silicon (boron doped with a dopant concentration of approximately 10^{15} cm^{-3}) was thermally grown and subsequently, a 10 nm thick carbon layer was deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition). The carbon layer was then annealed for 60 min at 700 °C in an N_2 atmosphere to increase the crystal size of the nanocrystalline carbon layer to increase the graphitic character [122]. A 6 nm thick Al_2O_3 layer was deposited via ALD (Atomic Layer Deposition) at 200 °C with TMA (trimethylaluminum) and H_2O as precursor gases subsequently. The test structures were created by i-Line photolithography and a DHF (Diluted HF) step for 1 min to remove the ALD Al_2O_3, followed by wet chemical removers and oxygen plasma to remove the photoresist and the uncovered graphite. Subsequently, a 100 nm thick Si_3N_4 layer was deposited via PECVD which

serves as an additional barrier against humidity and increases the long-term stability of the sensor against the atmosphere. The contacts were structured by photolithography and the Si_3N_4 layer was removed by RIE (Reactive Ion Etching) with an etch stop on Al_2O_3 in the contact region. Afterward, the photoresist was removed by wet chemical removers and oxygen plasma. Here the Al_2O_3 protects the underlying graphite layer on the contact region. The Al_2O_3 layer was etched with DHF for 1 min with an etch stop on graphite. A 10 nm thick non-magnetic Ni/Cr layer was then deposited, followed by a 200 nm thick AlCu layer. The contact pad separation was done by photolithography and subsequent RIE etching of the metals with an etch stop on Si_3N_4. In the last step, the resist was removed as in the previous steps. Figure 5-2 shows the fabricated structures and their modifications in size and design.

a) van-der-Pauw structures



b) TLM structures

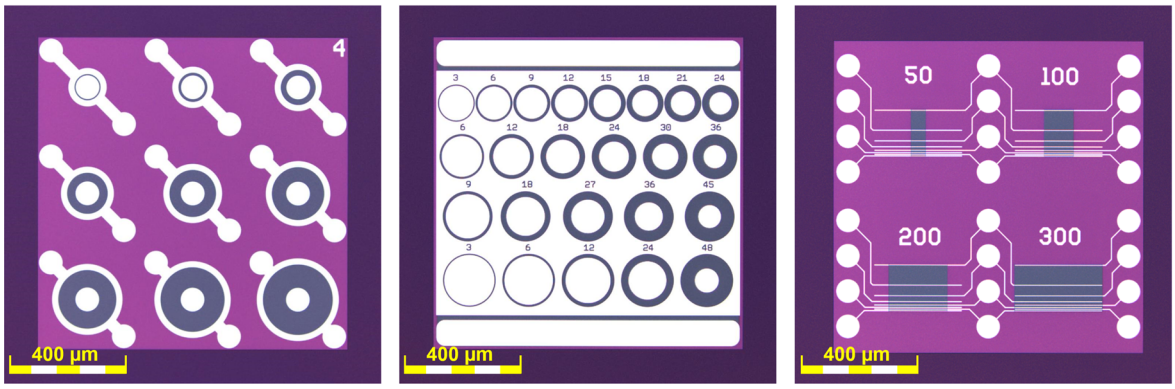


Figure 5-2: Optical micrographs of all test structures and their modifications in design and size. a) van-der-Pauw and b) TLM structures.

In the following chapter, the influence of the manufacturing process of graphite-based test structures was evaluated using the Hall sensor structure. Electrical transmission measurements were carried out to investigate the interface between the metallic contact and graphite. To support

this measurement method, FIB (Focused Ion Beam) cross-sections were prepared at the contact area to investigate the layer arrangement of the structure. Afterward, the deposited graphite layer was analyzed by Raman Spectroscopy to determine their homogeneity and thus to draw conclusions on the measured electrical resistance.

5.2 Characterization of carbon-based test structures

In this chapter, the fabricated Hall sensor test structures in a van-der-Pauw geometry were electrically and optically characterized. In the beginning, electrical transmission measurements were carried out to determine the magnitude of the contact resistance between nanocrystalline carbon and the contact metal. From two-point measurements between two opposite contacts an electrical resistance in the range of 200-300 Ω from the center to the edge of the wafer is determined at the Hall sensor test structures (Figure 5-3). This leads to the conclusion that there is no Al_2O_3 residual layer at the interface between graphite and metal, which would remain due to a too-short etching time, and leads to total resistances in the kΩ or MΩ range. Therefore, it can be concluded from the electrical transmission measurements that the etching time of Al_2O_3, which is critical for the contact resistance, is not too low.

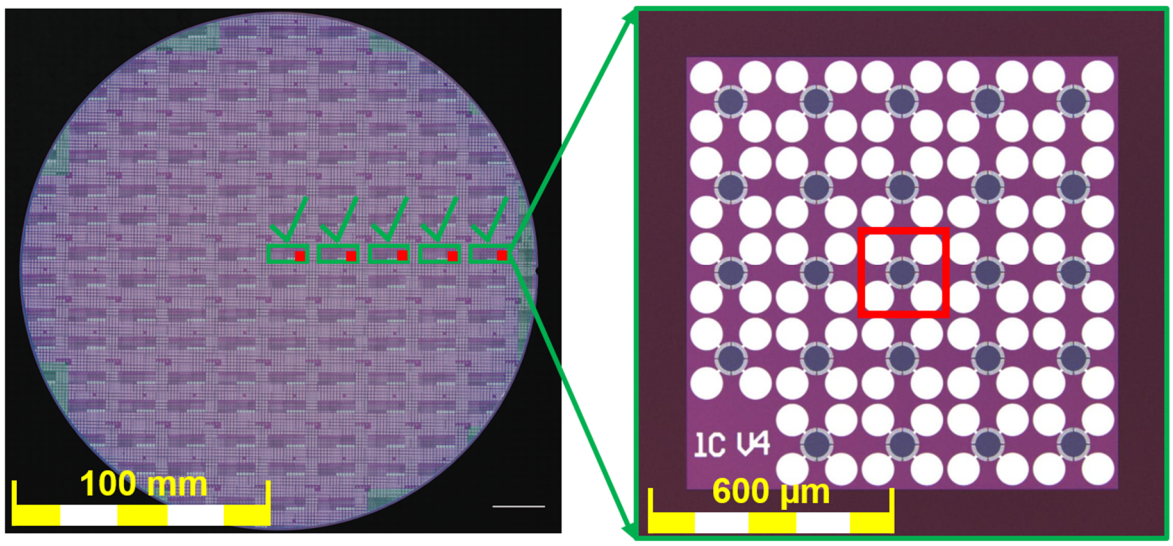


Figure 5-3: Image of a processed wafer with test structures and overview of tested devices (left), and an optical overview of a Hall sensor test structure field on a test chip (right) with the highlighted device under test

To confirm the results of the electrical measurements, the cross-section of the Hall sensor structure was optically analyzed. For this, a focused ion beam (FIB) cut with argon ions was carried out at the transition between the contact area and the active structure, and the cross-section was investigated by scanning electron microscopy (SEM). The SEM image of the cross-section is shown in Figure 5-4. On the left side in Figure 5-4 the region is marked (red line), where the FIB cut was done and where the SEM cross-section was investigated. On the right side of the figure, the SEM cross-section with the corresponding layers is shown. It can be seen that the deposited layers are as expected, both in thickness and structure.

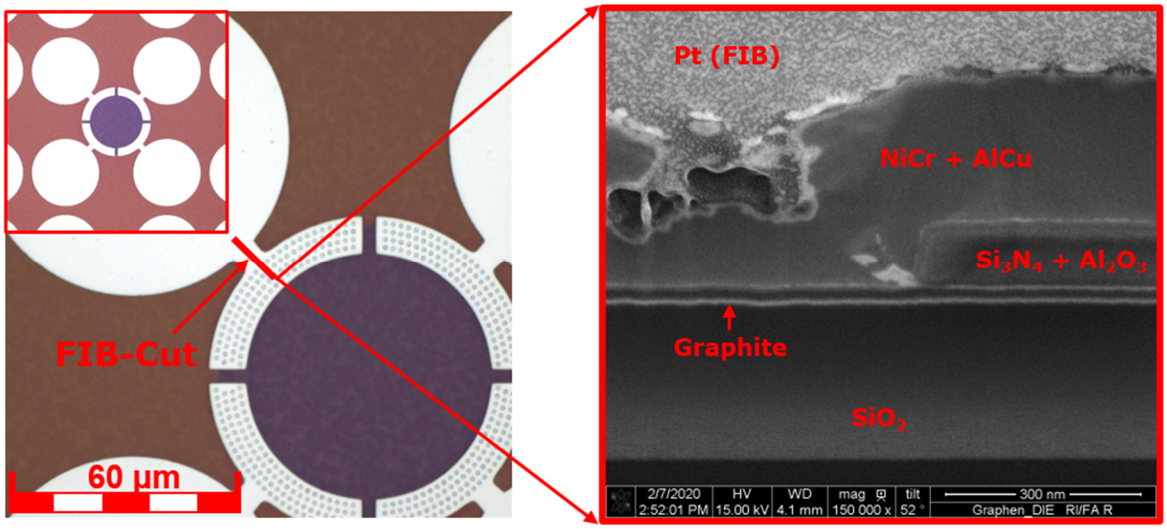


Figure 5-4: FIB-cut of graphite-based van-der-Pauw structure at the contact area. From the SEM image (right) it can be seen that the structure and layer dimensions are as expected from the process flow.

Through electrical transmission measurements and the optical inspection via combined FIB cut and SEM, the contact formation and layer arrangement, and layer dimensions of the Hall sensor structure were investigated and verified. The results showed that the fabricated structure meets the expectations after the process flow. Now it has to be ensured that the deposited carbon layer is homogeneously below the Al_2O_3 and Si_3N_4 layer stack to investigate the influence of the deposition process on it. For this purpose, the carbon layer in the active area was examined by Raman spectroscopy with a Raman spectrometer from Horiba with a laser excitation wavelength of 532 nm (2.33 eV). The spot size was obtained by using a 100x objective with a long working distance focusing lens with 0.21 mm and a numerical aperture of 0.90. A single-mode optical fiber and a spectrometer with a grating of 1,800 lines/mm were used for the detection of the Raman modes. All measurements were performed with linear laser polarization with a power density of 5.77 mW/µm^2, an integration time of 1 s, and an accumulation number of 2 (specific setting

parameter of the Raman system). For the analysis of the homogeneity, the intensity of the G-mode was extracted with a Lorentzian fit function (Figure 5-5), which is located at a wave number of about 1600 cm^{-1}. It can be seen that in the active region, the carbon layer is homogeneous and shows only a small variation in the intensity of the G-mode. From this, it can be concluded that the deposited layer stack of Al_2O_3 and Si_3N_4 has a small influence on the chemical structure of the carbon layer. This analysis is even more informative in the case of graphene since doping and defect density can be determined from the Raman spectrum of graphene [16] and thus a clear statement about the influence of the Al_2O_3 and Si_3N_4 layer stack on the electrical properties of graphene can be made.

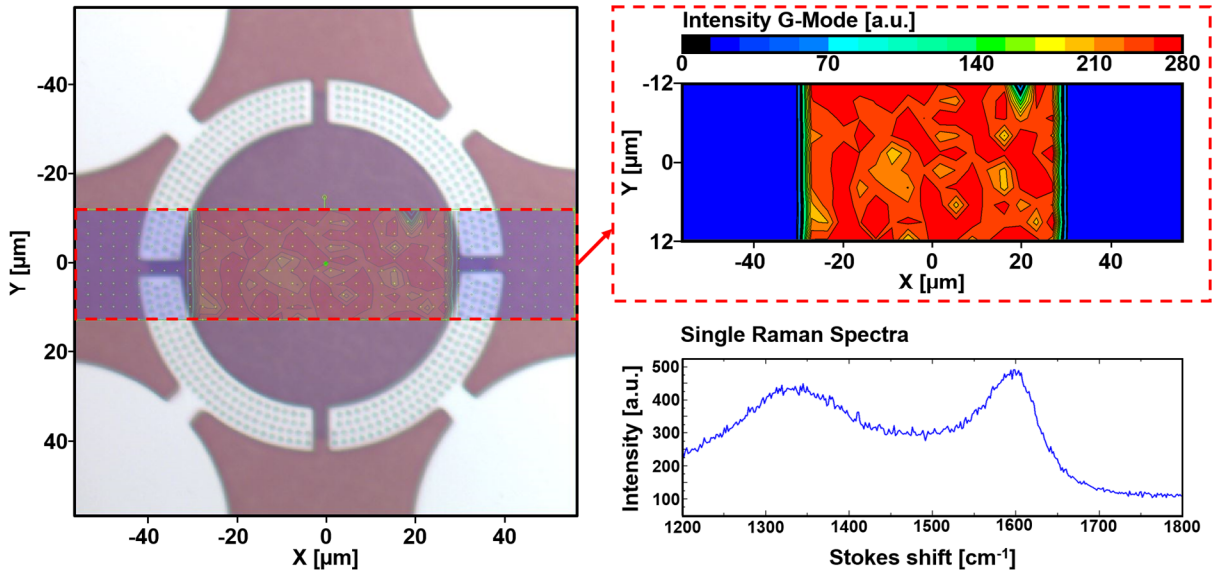


Figure 5-5: Raman analysis of the carbon layer structure in the active region. It can be seen that the G-mode intensity is mainly in the range of 240 to 280 in arbitrary units with background subtraction in the active sensor area, which indicates that the carbon layer is homogeneous in the active area.

5.3 Conclusion

The results from the integration process for graphene and related materials (in this case carbon) have shown that the process flow and parameters are sufficient for the production of Hall sensor structures. The individual processes have not been adapted for carbon-containing materials and are used in this form for existing silicon technologies. Electrical and optical analyses have shown that an ohmic contact can be achieved and that the layer arrangements and dimensions correspond to the specification of the individual processes. Replacing nanocrystalline carbon with

graphene could impact some processes that do not reach their specifications (e.g. ALD Al_2O_3 layer thickness) due to the different chemical surface structures of graphene to carbon.

The next step is to integrate graphene into the existing process flow to generate significant statistics of the process influences from the deposition of the ALD Al_2O_3 layer, the etching processes of graphene, and the metallization process via a high number of test structures per wafer. To achieve this, it is necessary to reduce the degree of contamination (metallic and carbon-based) during transfer to make it compatible with CMOS FEOL and BEOL processes. In chapter 3.1.3, TXRF and XPS measurements on wet and semidry transferred graphene at wafer level detected high copper contamination levels above the upper limit of the semiconductor manufacturing specification. The aim should be to reduce the copper contamination level of the transferred graphene layers by subsequent cleaning processes and a more optimized transfer method, and then to integrate the graphene into the existing process flow (chapter 3.1.3.).

6. Summary and Outlook

In this work, the feasibility of the integration of graphene into semiconductor fabrication lines was investigated with a focus on the transfer process, the influence of semiconductor processes and materials on the electrical properties of graphene, and the electrical performance of integrated graphene layers in a Hall sensor structure. Furthermore, the realization of test structures on the wafer level with industrial semiconductor manufacturing processes was investigated for the future production of graphene-based devices.

For the transfer of graphene from its growth substrate to a CMOS-compatible target substrate (in this work SiO_2), wet and semidry transfer technique was assessed to determine its advantages and disadvantages in terms of automation (handling), quality, contamination, and electrical performance of the transferred graphene sheets (chapter 3.1). For this purpose, an in-house transfer tool was developed to realize semidry transfer on the wafer level. Transferred 6-inch graphene on a copper substrate to an 8-inch SiO_2 wafer were analyzed via optical contrast spectroscopy, TXRF, XPS, Time-domain THz spectroscopy, and electrically to determine transfer yield and quality, metallic and polymeric contaminations, electrical sheet resistance and conductivity and charge carrier mobility. The wet transfer shows a higher quality in the transferred graphene sheets but is connected with the difficult handling of the 6-inch graphene layer due to the low stability. Therefore wet transfer results have a yield of almost 100 % or zero due to the destruction of the graphene sheet during transfer. The semidry transfer has a lower transferred graphene quality than wet transfer but is better controllable by the potential for the usage of carrier wafers, which is not the case for wet transfer. This leads to transfer yields for semidry transfer that are always higher than zero and with a dependence on transfer quality with increasing bond pressure. Regarding contamination shows semidry transfer with lower copper contamination as wet transfer, but still above the front-end-of-line specification, but with higher polymeric contamination as the wet transfer. The electrical properties of graphene sheets are higher in wet transfer than in semidry transfer, which results in a better performance of graphene-based applications. Both transfer techniques have the potential for implementation in future graphene-based technologies at the wafer level in semiconductor fabrication because the disadvantages of the transfers can be reduced by optimizing the transfer parameters. The contamination level for both transfer techniques can be decreased by a higher copper etching concentration and a higher polymeric purification media concentration. The electrical performance of transferred graphene sheets can be increased in semidry transfer by a higher bonding pressure during transfer. [71]

The influence of semiconductor material surfaces was investigated by transferring graphene onto CMOS-compatible SiO_2, Si_3N_4, and modified SiO_2 by introducing ammonia and aluminum to change the surface charge potential (chapter 3.2). It has been shown that graphene on Si_3N_4 shows higher charge carrier mobility than on SiO_2 and modified SiO_2 substrates which are related to a lower surface roughness of Si_3N_4 [78], [88], [101]. Graphene on SiO_2 and modified SiO_2 substrates shows a smaller charge carrier concentration variation as on Si_3N_4 due to the combined SiO_2 and Si_3N_4 surface regions on Si_3N_4 after oxygen plasma processing for transfer. Contact resistance between graphene and nickel is higher on modified SiO_2 substrates than on standard SiO_2, which is related to a higher electrical graphene sheet resistance on these substrates due to a lower surface charge. These findings can be used for the combination of standard SiO_2 and modified SiO_2 surfaces with encapsulation layers for the definition of active and passive areas for graphene-based devices. In the active regions, the charge carrier concentration in graphene is low (high charge carrier mobility) due to the charge compensation of the substrate surface and the encapsulation layer, which ensures high device performance. In the passive regions at the electrical contacts, the charge carrier density in graphene is high (low sheet resistance) due to the substrate surface of standard SiO_2, resulting in low contact resistance and therefore the improvement of the power consumption of the device. [78]

Furthermore, the potential of graphene-based Hall sensors was investigated in different device environments (chapter 4). For this, suspended graphene membranes (chapter 4.1) and encapsulated graphene sheets (chapter 4.2) were fabricated and electrically measured to analyze the impact of the direct material environment of graphene on its electrical performance. A special focus is on charge carrier mobility because this physical material parameter is proportional to the electrical sensitivity of the device to external magnetic fields. The self-supporting graphene membranes were wet-chemically transferred onto a specially fabricated support structure and the membrane was separated from the graphene on the substrate via a laser structuring process. The yield of this manufacturing process is about 0.2 % since the low membrane stiffness leads to the cracking of the graphene during fabrication due to external mechanical influences. Suspended graphene membranes show charge carrier mobilities which are higher compared to supported graphene sheets on SiO_2 [78] and electrical sensitivities which exceed commercial CMOS Hall sensors based on the Hall effect. This result shows that free-standing graphene membranes have the potential to outperform existing silicon-based Hall sensor technologies. However, the manufacturing process and final sensor design are not yet optimized as these processes and device designs result in low yields with cross-influences from the atmosphere. For this purpose, it is necessary to use another transfer approach to transfer the graphene to a sensor structure, e.g.,

by using dry transfer processes, since most of the collapses of the membranes happen when it is interact with the liquid media during the wet transfer. To reduce the interaction with the atmosphere, it is necessary to package the fabricated Hall sensors with commercial packaging technologies.

Moreover, Hall sensors based on encapsulated graphene sheets in a van-der-Pauw geometry were fabricated and electrical characterized to determine the electrical device performance. The goal was to generate a high statistic of the electrical parameters of encapsulated graphene sheets on a sample basis with processes, which are commonly used in industrial semiconductor fabrication lines. The measured charge carrier mobility was lower compared to Hall sensors with suspended graphene membranes but is in general in the same range as was shown in previous works [78]. The electrical properties of the grown Al_2O_3 encapsulation layer on graphene by atomic layer deposition were comparable to those of conventional Al_2O_3 layers on silicon. These results showed that it is currently possible to fabricate graphene-based Hall sensors using conventional semiconductor processes but with a high variance of the electrical parameters. This is mainly due to the varying quality of the starting material (graphene on copper) and the influence of the transfer process, which makes it impossible to produce graphene-based Hall sensors with consistent electrical properties across multiple devices. This problem can be solved through an optimized growth and transfer method and then the manufacturing process for Hall sensors based on graphene will be ready for industrial use.

Finally, the feasibility of a process flow for the fabrication of encapsulated graphene-based Hall sensors and test structures in an industrial semiconductor fabrication line was investigated (chapter 5). Due to the existing limitations of available transfer methods and their high metallic contamination potential, it is currently not possible to integrate transferred graphene layers on the wafer level into a front-end-of-line manufacturing process. As a consequence, thin nanocrystalline carbon layers were used as a reference for graphene, and the degree of crystallinity was increased by annealing processes. It was demonstrated that the process flow for the fabrication of graphene-based Hall sensors and test structures produces operating devices distributed over the wafer. The next step is to implement graphene as an active layer instead of the nanocrystalline carbon layer with the same process flow. For this purpose, it is necessary to optimize the transfer methods to their metallic contamination, so that the graphene can be implemented in a front-end-of-line process flow.

In summary, the processes and methods developed and analyzed in this work have advanced the realization of industrially fabricated graphene-based devices. It was shown that the investigated

transfer methods can enable the transfer of graphene from its growth substrate to a desired target substrate at the wafer level with the potential of automation for high throughput. Furthermore, by modifying SiO_2 surfaces with the introduction of aluminum and ammonia, a new method has been developed to control the electrical properties of graphene layers and thus the performance of graphene-based devices. In addition, the feasibility of Hall sensors based on free-standing and encapsulated graphene sheets was investigated and has shown that their performance in the case of suspended graphene membranes exceeds that of commercially available Hall sensors based on the same sensor technology. Finally, it was also shown that a developed process flow for the industrial production of Hall sensors and test structures based on nanocrystalline carbon is feasible on the wafer level and leads to a high yield. If nanocrystalline carbon is replaced with graphene in the future by an optimized transfer process with a lower contamination impact, this will lead to the final step of the integration of graphene into the industry.

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Appendix

A1. Theory for the determination of surface energy by contact angle measurement

The surface energy of a solid γ is the energy that must be applied to create a new surface. The adhesion work W_{12} is the work that is necessary to separate two solids from each other. It can be described by the formula

$$W_{12} = \gamma_1 + \gamma_2 - \gamma_{12} \qquad \text{A1-1}$$

with γ_1 and γ_2 as surface energies of the respective solids and γ_{12} as the interfacial energy between the two solids. The interfacial energy γ_{12} of two solids cannot be determined by contact angle measurements. More precisely, their determination is associated with greater effort [123], [124]. However, according to Johnson–Kendall–Roberts (JKR) theory, the adhesion energy for the adhesive contact between two elastic solids is proportional to the surface energies [125], [126].

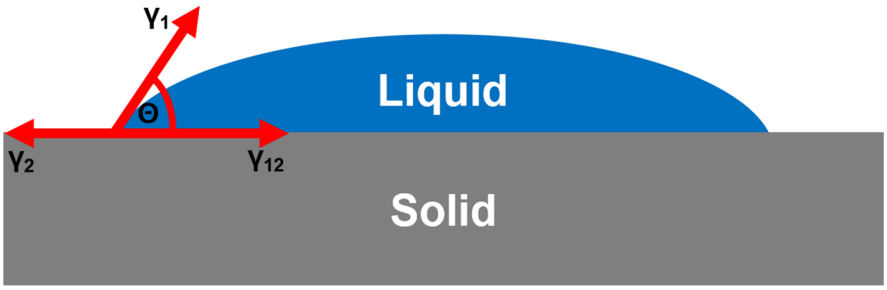

Figure A.1: Liquid droplet on a solid surface in a state of equilibrium

For contact angle measurements, a liquid drop with a surface tension of γ_1 is applied to a solid surface with a surface energy of γ_2. In the state of equilibrium (Figure A.1), a contact angle θ is established between the liquid and the solid, which can be described by the Young equation:

$$\gamma_2 = \gamma_{12} + \gamma_1 \cos(\theta) \qquad \text{A1-2}$$

The contact angle θ is related to the surface tension of the liquid γ_1 and the surface energy of the solid γ_2. There are different models for the interfacial energy γ_{12} for the interaction between liquid and solid surfaces. The models relate the interfacial energy γ_{12} to the surface energy γ_2 and to the surface tension γ_1. Therefore it is possible to determine the surface energy by contact angle measurements.

For the modeling of the interfacial energy, the equations A1-3 and A1-4 described in [127] are used.

$$\gamma_{12} = \gamma_1 + \gamma_2 - \frac{4\gamma_1^d\gamma_2^d}{\gamma_1^d + \gamma_2^d} - \frac{4\gamma_1^p\gamma_2^p}{\gamma_1^p + \gamma_2^p} \quad \text{A1-3}$$

$$\gamma_{12} = \gamma_1 + \gamma_2 - 2\sqrt{\gamma_1^d\gamma_2^d} - \frac{4\gamma_1^p\gamma_2^p}{\gamma_1^p + \gamma_2^p} \quad \text{A1-4}$$

In both models, the surface energy or surface tension is divided into a polar γ_i^p and a disperse γ_i^d fraction:

$$\gamma_i = \gamma_i^d + \gamma_i^p \quad \text{A1-5}$$

The adhesion of graphene to a substrate is only due to Van-der-Waals interactions [70]. The Van-der-Waals forces consist of the interaction between two permanent dipoles, an interaction between a permanent dipole and an induced dipole, and the interaction between two non-polar but polarizable bodies with temporary dipoles. These are named in order of interaction by Keesom, Debye, and London interaction [128]. The individual parts of the Van-der-Waals interactions can be either γ_i^p or γ_i^d. The London interaction corresponds to the dispersed part of the surface energy, while the polar fraction of the surface energy contains the Debye and Keesom interactions [129]. In chapter 3.1.1.1, equation A1-3 is used to determine the surface energy of polymers such as thermal release tapes, while equation A1-4 is used to determine the surface energy of silicon, graphene, and copper.

Table A.1: Test fluids used for contact angle determination

Test liquid	**Surface tension in mN/m**		
	dispersive portion	polar portion	total surface tension
Water	26.4	56.4	72.8
Diiodomethane	50.8	1.3	52.1

For the determination of the surface energy during contact angle measurements, the contact angle θ must be determined for two different test liquids with known polar and dispersed fractions. During the experiments, water and diiodomethane were used as test liquids. Table A.1 summarizes the surface tensions of the test liquids.

A2. Methodology for graphene coverage extraction from optical microscopy

The determination of the degree of coverage of graphene on SiO_2 or other supporting isolators is important in identifying the quality and yield of the transfer method. Based on optical micrographs of the graphene layer on the substrate, the contrast of the graphene layer as well as multilayer domains can be determined. This allows a fast and contactless determination of the transfer quality and yield of the transferred graphene layers. Figure A.2 schematically shows the procedure for the extraction of the degree of coverage of graphene on isolators using an optical image of the region of interest.

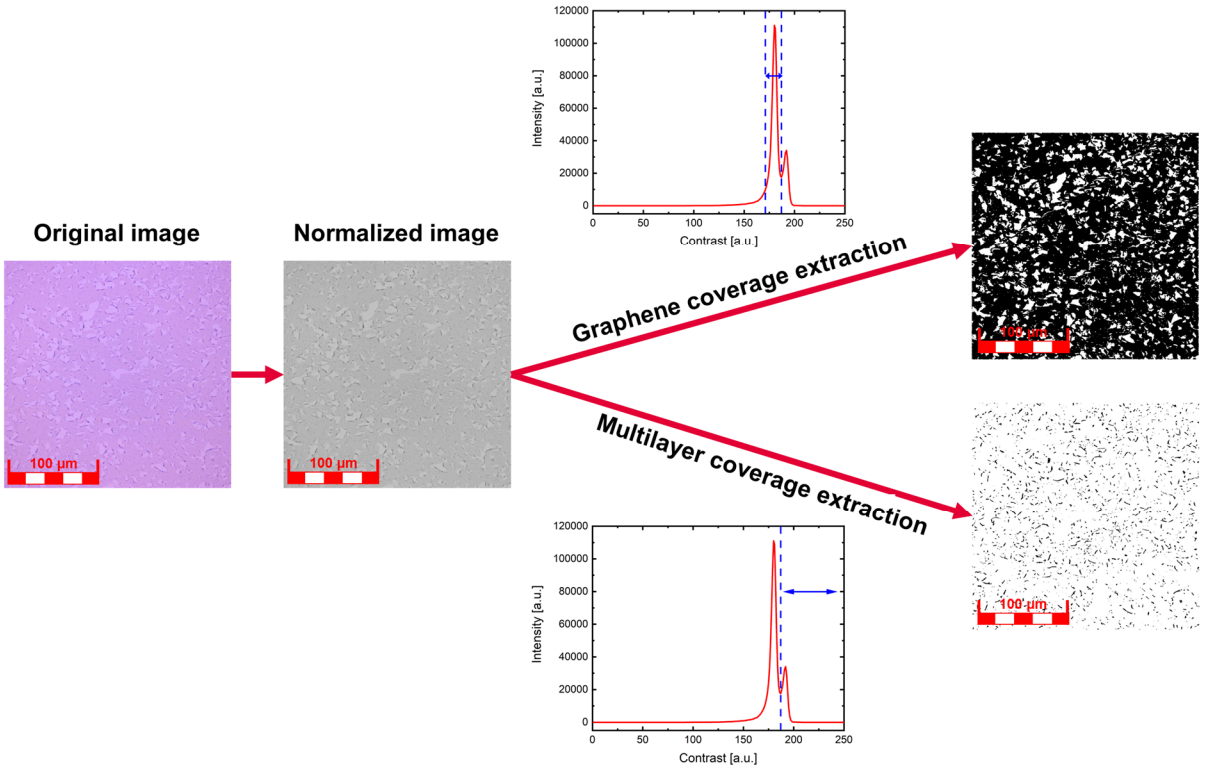

Figure A.2: Procedure for the extraction of graphene coverage with optical contrast microscopy

In the beginning, an optical microscope is used to visualize the investigated area and in the next step, the extraction of the degree of coverage is performed with Matlab R2018b. For this purpose, the optical image is converted into a monochrome image and the intensity values in the image are fitted and normalized to obtain a constant intensity distribution over the entire image. The intensities are then statistically sorted according to their contrast values. From this analysis, the intensities of the substrate, monolayer graphene, and multilayer graphene domains are obtained.

The areas of highest contrast are assigned to the multilayer graphene domains, the lower contrast values to monolayer graphene, and the lowest contrast values to the substrate. Based on the intensity values, which correspond to the occurrence of the contrast values or the graphene/multilayer domains, the percentage proportion is calculated out of it. The assigned contrast values of monolayer and multilayer graphene are marked in red in Figure A.2. The contrast distribution of the substrate is homogeneously distributed and not distributed like that of monolayer and multilayer graphene. This is achieved by integrating over the whole contrast range from 0 to the range of contrast distribution of the monolayer graphene.

A3. Theory of CV measurements on oxide/silicon interfaces

With capacitance-voltage (CV) measurements, the total charge in isolators and the interfacial charge between the isolator and silicon interface can be determined. The interfacial charge between the isolator and silicon interface should be the same as on the isolator surface due to the homogeneous charge distribution in the isolator, which is valid for thin isolators [130]. Therefore the interfacial charge between the isolator and silicon interface can be determined by CV measurement and conclusions can be drawn about the surface charge of the isolator. The fixed interfacial charge Q_f can be determined by the following equation [131]:

$$Q_f = (\Phi_{MS} - V_{FB})C_{Isolator} \qquad \text{A3-1}$$

With Φ_{MS} as the potential difference between the contact metal and silicon, V_{FB} as the flat band voltage and $C_{Isolator}$ as the isolator capacitance. The flat band voltage V_{FB} can be determined from the flat band capacitance C_{FB}, which is calculated by equation A3-2 [132]:

$$C_{FB} = \frac{C_{Isolator}C_{sFB}}{C_{Isolator} + C_{sFB}} \qquad \text{A3-2}$$

And C_{sFB} as [132]:

$$C_{sFB} = e\sqrt{\frac{\varepsilon_r \varepsilon_0 N_D}{k_B T}} \qquad \text{A3-3}$$

With ε_r as the permittivity of the isolator, ε_0 as the permittivity of the air, k_B as the Boltzmann constant, T as the measuring temperature and N_D as the majority charge carrier density in silicon. From this, V_{FB} can be extracted from the measurement data at the point where the measured capacitance has the value of C_{FB} and then the interfacial charge Q_f can be calculated.

List of Publications & Patents

Publications

- König, M., Ruhl, G., Gahoi, A., **Wittmann, S.**, Preis, T., Batke, J. M.,Costina, I. & Lemme, M. C. (2019). Accurate Graphene-Metal Junction Characterization. *IEEE Journal of the Electron Devices Society*, *7*, 219-226.
- **Wittmann, S.**, Glacer, C., Wagner, S., Pindl, S., & Lemme, M. C. (2019). Graphene Membranes for Hall Sensors and Microphones Integrated with CMOS-Compatible Processes. *ACS Applied Nano Materials*, *2*(8), 5079-5085.
- **Wittmann, Sebastian**, and Max Christian Lemme. "Integration of graphene in CMOS compatible device environments." MikroSystemTechnik 2019; Congress. VDE, 2019.
- **Wittmann, S.**, Aumer, F., Wittmann, D., Pindl, S. Wagner, S., Gahoi, A., Reato, E., Belete, M., Kataria, S., Lemme, M. C. "Dielectric surface charge engineering for electrostatic doping of graphene." ACS Applied Electronic Materials 2.5 (2020): 1235-1242.
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Conference & Workshop Presentations

- **S. Wittmann**, M. C. Lemme. „Integration of graphene in CMOS compatible device environments“, *VDE MikroSystemTechnik Kongress*, October 2019 (poster)
- **S. Wittmann**. „Process engineering for wafer-level integration of graphene into industrial applications”, *Wafer-scale Integration of 2D materials Workshop*, November 2019 (presentation)

Patents

- Glacer, C., Pindl, S., Weber, W., & **Wittmann, S**. (2020). U.S. Patent Application No. 16/548,144.

Curriculum Vitae

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