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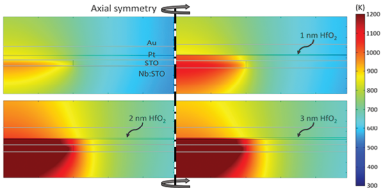

Enhancing the switching speed of oxide-based memristive devices at a low voltage level is crucial for their use as non-volatile memory and their integration into emerging computing paradigms such as neuromorphic computing. In this work, a x1000 acceleration of the SET speed, or up to 30% reduction of the operating voltage in filamentary valence change mechanism (VCM) memristors is demonstrated by thermally confining the Joule heating generated during the switching process.

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Resistive Switching Acceleration Induced by Thermal Confinement

Alexandros Sarantopoulos, Kristof Lange, Francisco Rivadulla, Stephan Menzel, and Regina Dittmann*

Enhancing the switching speed of oxide-based memristive devices at a low voltage level is crucial for their use as non-volatile memory and their integration into emerging computing paradigms such as neuromorphic computing. Efforts to accelerate the switching speed often result in an energy trade-off, leading to an increase in the minimum working voltage. In this study, an innovative solution is presented: the introduction of a low thermal conductivity layer placed within the active electrode, which impedes the dissipation of heat generated during the switching process. The result is a notable acceleration in the switching speed of the memristive model system $SrTiO_3$ by a remarkable factor of 10^3, while preserving the integrity of the switching layer and the interfaces with the electrodes, rendering it adaptable to various filamentary memristive systems. The incorporation of HfO_2 or TaO_x as heat-blocking layers not only streamlines the fabrication process but also ensures compatibility with complementary metal-oxide-semiconductor technology.

1. Introduction

Memristive devices based on the valence change mechanism (VCM) have exhibited substantial potential not only in the domain of digital emerging memories but also in analog neuromorphic and in-memory computing applications.[1–10] Considering these applications, many endeavors have been directed toward enhancing the performance of memristive devices, with a particular focus on increasing the switching speed and minimizing the switching voltages.

Numerous studies have delved into the physical mechanisms behind the switching speed of memristive devices. These investigations have successfully showcased impressive switching speeds, often reaching the nano- and picosecond range.[11–15] Specifically, the interplay of both field and temperature acceleration results in a markedly non-linear relationship between switching speed and switching voltage.[16] The increase in switching speed is at the expense of the voltage; for one of the fastest filamentary resistive switching systems (Ta_2O_5-based memristive device), a switching voltage of $\geqslant 2$ V is required to switch the device with a 10 ns pulse, while switching the device with picosecond pulses, the necessary voltage is above 9 V.[14] Hence, developing strategies to boost switching speed at a designated low switching voltage is imperative. This not only aids in minimizing power consumption but also aligns with the voltage requirements of highly scaled complementary metal-oxide-semiconductor (CMOS) transistors, essential for the CMOS co-integration of memristors.

Commonly, the most relevant parameters affecting the switching speed are besides the energy barrier for oxygen motion within the switching layer, the filament size and the oxygen exchange at the interface to the oxidizable electrode.[17–20] In addition, for eightwise resistive switching devices, the oxygen exchange reaction with the Pt top electrode is often the rate determining step of the switching process, dictating the switching speed of the device.[21–24] The filament size is to some extent an inherent property of the switching material, although external factors (e.g., the current compliance) significantly influence the filament dimensions.[25] Smaller filaments cause a stronger confinement of the current, amplifying Joule heating and consequently contributing to an increased switching speed.[16,19,26–28]

Joule heating generated in the course of the switching process, increases the diffusion of oxygen vacancies in filamentary ReRAM devices, which leads to a substantial acceleration of the switching speed.[16,27,29–31] In order to minimize the heat losses through the thermally conductive metal electrode, the use of an electrode material with low thermal conductivity might enable

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aelm.202400555

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DOI: 10.1002/aelm.202400555

further switching speed acceleration. Although it is common and well accepted that thermal management is crucial for phase change materials,[32–39] for valence change memory devices this strategy has not been exploited so far, in terms of switching speed and operation voltages.

In attempts to take advantage of a thermal enhancement layer, the introduction of low thermal conductivity layers at the oxide/metal interface resulted in a larger window between the high resistive state and the low resistive state (ON/OFF ratio) and in improved multilevel switching.[26,40–43] Nonetheless, a comprehensive physical explanation elucidating the influence of the thermal enhancement layer on device performance was absent. Moreover, directly interfacing the thermal enhancement layer with the memristive material, will significantly influence interface reactions, resulting in changes of the oxygen vacancy concentration and the oxygen exchange reaction with the electrodes. Therefore, modifying the switching layer and interfaces to improve switching speed may have a negative impact on other relevant properties, such as resistance range and programmed state retention.[22]

In this work, the devices are based on $SrTiO_3$ (STO), due to its very well known defect chemistry, ion diffusion mechanisms, and its wide use as a model system in VCM resistive switching, both in experiments and modeling.[16,20,23,44–46] Although a relatively slow switching system[16,22,28,29] compared to others, the gradual switching nature of STO-based ReRAM devices makes the system appealing to try and accelerate its switching speed. The larger filament size, combined with an increased series resistance introduced by the Nb:STO ohmic electrode, results in the prevention of a thermal runway, giving rise to the gradual nature of the switching behavior of STO-based ReRAM devices.[28] On the other hand, the exact same reasons are the ones responsible for its slower switching speed. It is also important to highlight that the STO-based devices studied here exhibit eightwise resistive switching,[24] which is inherently different from the counter-eightwise switching observed in the faster VCM systems, such as HfO_2 and TaO_x.

It is important to note that modifying the materials and geometry of the device can have a detrimental effect on the overall performance. In particular, the interplay between thermal and electrical conductivity is crucial to our approach, as the two properties are closely intertwined. Ideally, a material with high electrical conductivity and very low thermal conductivity would be able to act as a thermal barrier layer without sacrificing electrical conductivity, thus providing resistive switching acceleration and a reduction in operating voltages. Since it is difficult to have both properties in CMOS-compatible materials as an electrode replacement, the combination of materials, dimensions and overall implementation must be such that the trade-off between thermal acceleration and increased resistance has a positive sign and the overall result is beneficial to device performance.

In this context, we present a novel approach for thermal management of VCM devices, which provides a solution for this trade-off. By incorporating a heat blocking layer (HfO_2 or TaO_x) positioned within the active electrode of our STO model system VCM devices, we have been able to achieve a remarkable acceleration in switching speed, reaching up to 10^3 times faster in terms of time. In addition, this approach enables an approximate 30% reduction in the switching voltage required to sustain the switching speed. This not only improves the energy efficiency of ReRAM cells, but also positions them well for integration with low-voltage transistor technology. The choice of HfO_2 or TaO_x as heat barrier materials facilitates the implementation of our approach due to the wide availability of the materials and the simplicity of their fabrication process.

2. Results and Discussion

Our first approach to the thermal engineering of our devices is by introducing a heat-blocking layer of TaO_x inside the Pt active electrode in a stack sequence of Nb:STO/STO(15 nm)/Pt(10nm)/TaO_x(30nm)/Pt(20nm) (**Figure 1**a). TaO_x is a widely used material for resistive switching, whose electrical and thermal conductivity can be tuned by its oxygen stoichiometry,[47] which allows us to explore the trade-off between low thermal conductivity (efficient heat-blocking) and low electrical conductivity (increased series resistance in the active electrode). We employed two different oxygen stoichiometries: $TaO_{1.2}$ and $TaO_{0.6}$, with electrical conductivities of 1.4×10^4 and 3.75×10^5 S m^{-1}, respectively (see **Table 1**; Figure S1, Supporting Information).

Due to the gradual switching nature of STO-based memristive devices, there is no clear forming and switching step during the I–V sweeps. For that reason, we define forming and DC-switching voltage as the necessary voltage to reach the selected current compliance (CC), while SET voltage will refer to the voltage pulse that invokes a change of the resistance of the devices $R_{HRS}/R_{LRS} \geqslant 10$. The reference STO/Pt and STO/Pt/TaO_x/Pt devices exhibit eightwise switching typical for STO-based ReRAM devices (Figure 1b).[21,48–50] During forming and DC-switching the CC was kept at 10 mA and the devices present very stable behavior after multiple cycles. The forming and DC-switching voltage is similar between the reference STO/Pt and the $TaO_{0.6}$ devices, however, the devices with the $TaO_{1.2}$ interlayer exhibit increased values (see Figure S3, Supporting Information) due to the voltage drop at the STO, caused by the reduced electrical conductivity of the $TaO_{1.2}$ layer.

To probe the effect of TaO_x on the heat dissipation across the metal electrode, we have measured the thermal conductivity using frequency domain thermoreflectance (FDTR).[51,52] The results of the thermal boundary resistance (TBR) across the Pt interface with the STO are presented in Figure 1c. For the fittings, the TaO_x interlayer was treated as thermal interface between Pt and STO. We have investigated TaO_x films with different thickness, to improve the accuracy of the thermal analysis (for more details see Table 1; Figures S4–S7, Supporting Information). The reference sample of STO/Pt presents the lowest TBR = 4.83 ± 11% m^2K GW^{-1}, while the TBR increases linearly with the thickness of the TaO_x barrier, and it is higher for $TaO_{1.2}$ compared to the more electrically conductive $TaO_{0.6}$. The thermal conductivity of TaO_x can be estimated from the linear fit of the plot in Figure 1c and the thickness of the oxide layer, resulting in $\kappa_{TaO_{1.2}} = 1.2$ and $\kappa_{TaO_{0.6}} = 5.9$ W m^{-1} K^{-1}. The obtained values are very similar to previous reports of TaO_x thin films, supporting our analysis.[47]

The effect of the thermal barrier in the SET speed of the samples is summarized in Figure 1d. The SET speed for the reference sample of STO/Pt is in good agreement with previous studies, namely, we observe a strongly non-linear decrease of the required SET pulse length with the SET voltage height.[16,22] Regarding the STO/Pt/TaO_x/Pt devices, the two different oxygen concentrations

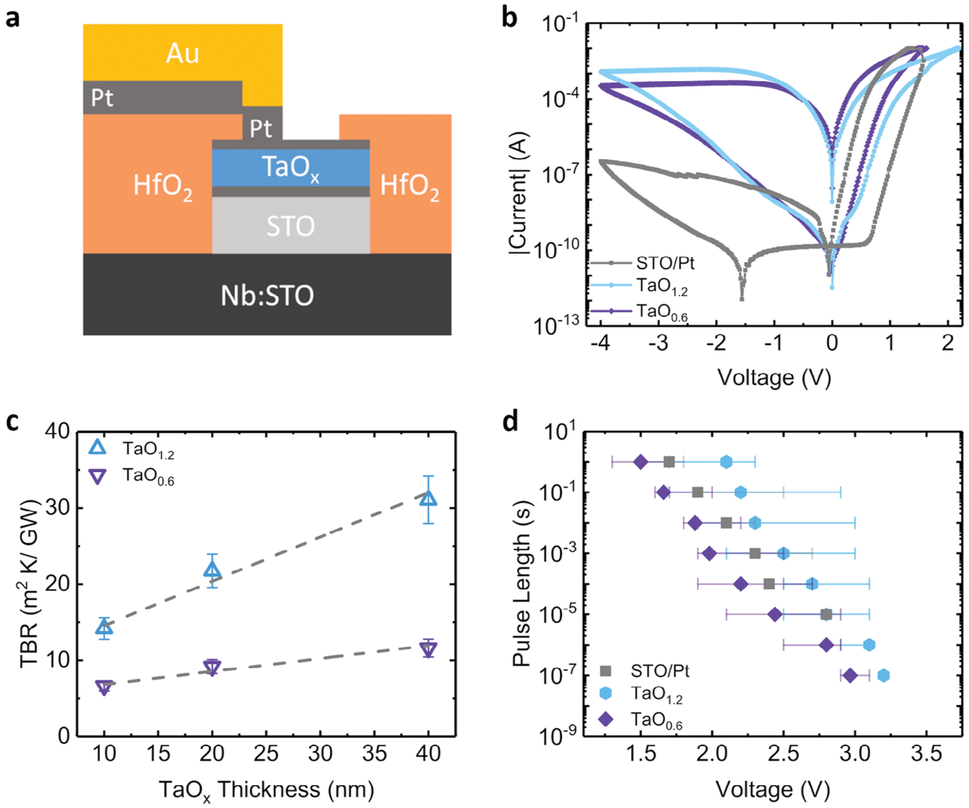

Figure 1. TaO$_x$ heat-blocking interlayer. a) Device layout sketch showing the TaO$_x$ layer placed inside the Pt active electrode. b) *I–V* sweeps for the devices of the different samples, the reference STO/Pt stack (gray) and the devices with the TaO$_x$ interlayers of different oxygen content. c) Thermal boundary resistance values for different thicknesses of the TaO$_x$ interlayers, in the two different oxygen concentrations. The dashed gray lines are the linear fit used to extract the thermal conductivity (slope) and the thermal resistance (intercept) of the thin films. d) SET speed measurements for the reference sample STO/Pt and the devices with TaO$_x$ interlayers.

of the oxygen-deficient tantalum oxide exhibit very different behavior: the TaO$_{1.2}$ interlayer has a slower SET speed than the reference STO/Pt sample, for the whole range of voltages used in the measurements. On the other hand, TaO$_{0.6}$ devices exhibit accelerated SET speed for the whole range of voltages compared to the reference sample STO/Pt. The difference is at least one order of magnitude in terms of pulse length, or a voltage reduction of ≈ 15% at given pulse lengths.

In our second approach to thermal engineering our devices, ultra-thin layers of electrically insulating HfO$_2$ were placed inside the Pt active electrode, as depicted in **Figure** 2a. The stack sequence is Nb:STO/STO(15 nm)/Pt(10nm)/HfO$_2$(1–3nm)/Pt(20nm). HfO$_2$ exhibits a very low thermal conductivity, making this a promising candidate as a heat-blocking barrier. Since the HfO$_2$ interlayers are electrically insulating, their thickness has been kept sufficiently small to avoid an increased series resistance inside the Pt electrode and make sure that the HfO$_2$ interlayer does not contribute to resistive switching. To confirm this point, additional control samples of Pt/HfO$_2$/Pt were prepared and measured in the same range of voltage and current as the original devices, showing no signs of distinguishable HRS and LRS (see Figure S2, Supporting Information). The *I–V* sweeps in Figure 2b present eightwise resistive switching mode. The reference STO/Pt and 1 nm HfO$_2$ interlayer devices exhibit similar forming and DC-switching voltage, however the devices with 2 and 3 nm HfO$_2$ exhibit increased forming voltage and slightly higher DC-switching voltage (see Figure S3, Supporting Information) due to the increased series resistance of the thicker HfO$_2$ interlayers.

Table 1. Electrical and thermal properties.

Sample	σ [S m^{-1}]	κ [W m^{-1} K^{-1}]	TBR [m^2 K GW^{-1}]
STO/Pt	6.2×10^6	44.5	4.8
TaO$_{1.2}$	1.4×10^4	1.2	26.1
TaO$_{0.6}$	3.75×10^5	5.9	10.2
HfO$_2$ (1 nm)	–	0.53	18.8
HfO$_2$ (2 nm)	–	0.53	20.5
HfO$_2$ (3 nm)	–	0.53	22.1

For the analysis of the heat-blocking efficiency of the HfO$_2$ interlayers, we measured the thermal resistances with FDTR. As discussed before, to improve the accuracy of the analysis, we treated the Pt/HfO$_2$/Pt as a single thermal resistance between the metal transducer and the STO film, in our fittings (for more details see Table 1; Figures S4–S7, Supporting Information). The results of the TBR of these interfaces are presented in Figure 2c. Introducing just 1 nm thick interlayer of HfO$_2$ increases the TBR substantially (18.8 ± 10% m^{2}K GW^{-1}) with

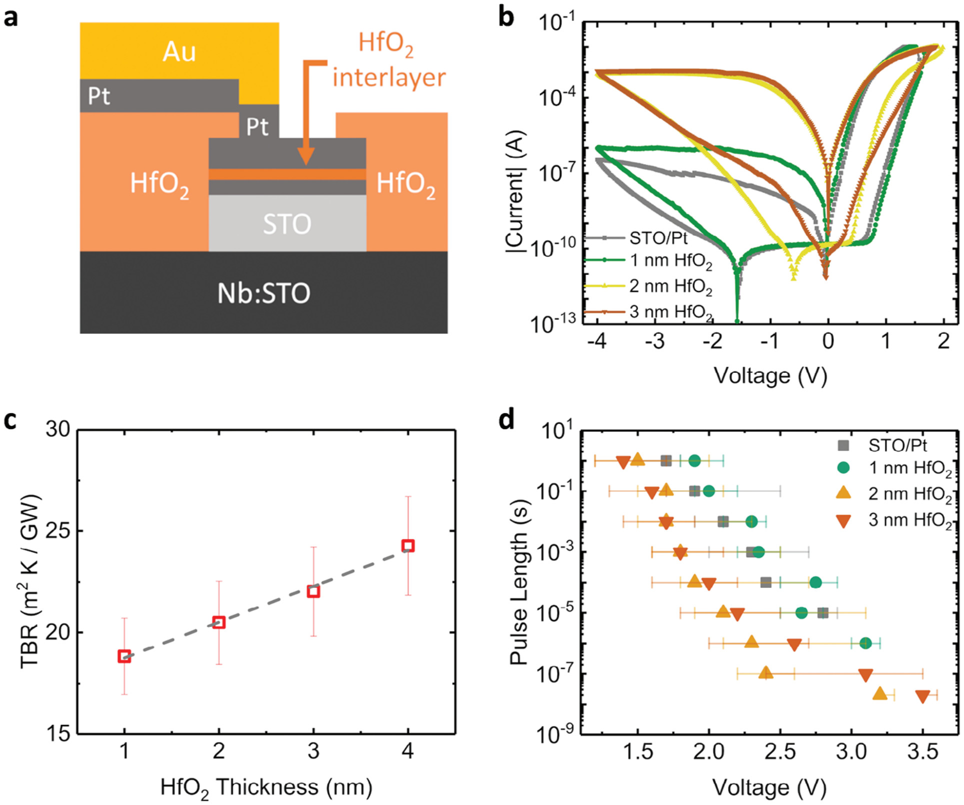

Figure 2. HfO_2 heat blocking interlayer. a) Device layout sketch with the insertion of the HfO_2 interlayer inside the Pt active electrode. b) *I–V* sweeps for the devices of the different thickness HfO_2 interlayers inside the Pt active electrode. c) Thermal boundary resistance values for different thicknesses of the HfO_2 interlayers ranging from 1 to 4 nm thickness. The dashed gray line is the linear fit used to extract the thermal conductivity (slope) and the thermal resistance (intercept) of the thin films. d) SET speed measurements for the reference sample STO/Pt and the three different thicknesses of the HfO_2 interlayers.

respect to STO/Pt in the reference sample ($4.83 \pm 11\%$ m^2K GW^{-1}). The TBR increases linearly with the thickness of HfO_2, reaching $24.2 \pm 11\%$ $m^2K\,GW^{-1}$ for the 4 nm interlayer. Using the values for the thermal boundary resistance and the thickness extrapolation approach,[53–55] we estimated a thermal conductivity of the HfO_2 layer $\kappa = 0.54 \pm 10\%$ W m^{-1} K^{-1}, in very good agreement with the literature.[55,56]

The results for the SET speed measurements are plotted in Figure 2d: the devices with 1 nm-thick HfO_2 barrier exhibit a similar speed as the control sample, slightly slower at lower voltages and slightly faster at higher voltages. Increasing the thickness of the HfO_2 interlayer produces a significant improvement, even at lower voltages. With increasing pulse height, the difference between reference and HfO_2 interlayer devices becomes more pronounced. The results show an acceleration of the SET process for a given pulse length, of x10^3, reducing the SET time from 100 µs to 100 ns in the range of 2.3–3.2 V. Also, the results may be described from an energy efficiency point of view, noting that the same pulse length reduces the required voltage pulse by ≈ 20% at the lower voltages, and up to ≈ 30% at higher voltages.

In order to quantify the effect of the HfO_2 barrier on the dissipation of heat across the Pt layer we simulated by finite element method (FEM) simulations, using the device structure shown in Figure S8 (Supporting Information). This structure is based on the device layout sketched in Figure 2a. The only exterior electrical as well as thermal contacts are located at the outer edge of the Au layer and at the bottom of the Nb:STO layer. In Table S2 (Supporting Information), the material parameters used for simulation are listed. Taking as input the experimental data from the *I–V* sweeps, we were able to calculate the maximum temperature reached at the filament vicinity for all samples, depicted in **Figure 3**a. The 2 nm HfO_2 interlayer sample exhibits a longer sustained temperature due to the slightly higher voltage that needed to be applied in order to reach the CC for the *I–V* sweep, compared to the other devices (see Figure 2b). Moreover, the heating efficiency of each sample has been calculated and plotted in Figure 3b. An overview of the local maxima for the temperature within the STO layer is presented in Figure 3c–f as 2D temperature profiles. The arrows indicate the position of the HfO_2 interlayers within the Pt electrode.

Figure 3c–f shows 2D temperature profiles for the reference STO/Pt device and the three HfO_2 interlayer thicknesses, at $t =$ 0.1 s when the overall highest temperatures are observed. The calculated temperature at the filament region within the STO layer increases with the HfO_2 interlayer insertion compared to the reference device, further increasing for the thicker interlayers. At the position of the interlayer (marked with arrows in Figure 3) the temperature exhibits an abrupt decrease at the upper part of the interlayer, highlighting the increased thermal resistance of the HfO_2 within the platinum electrode. For thicker

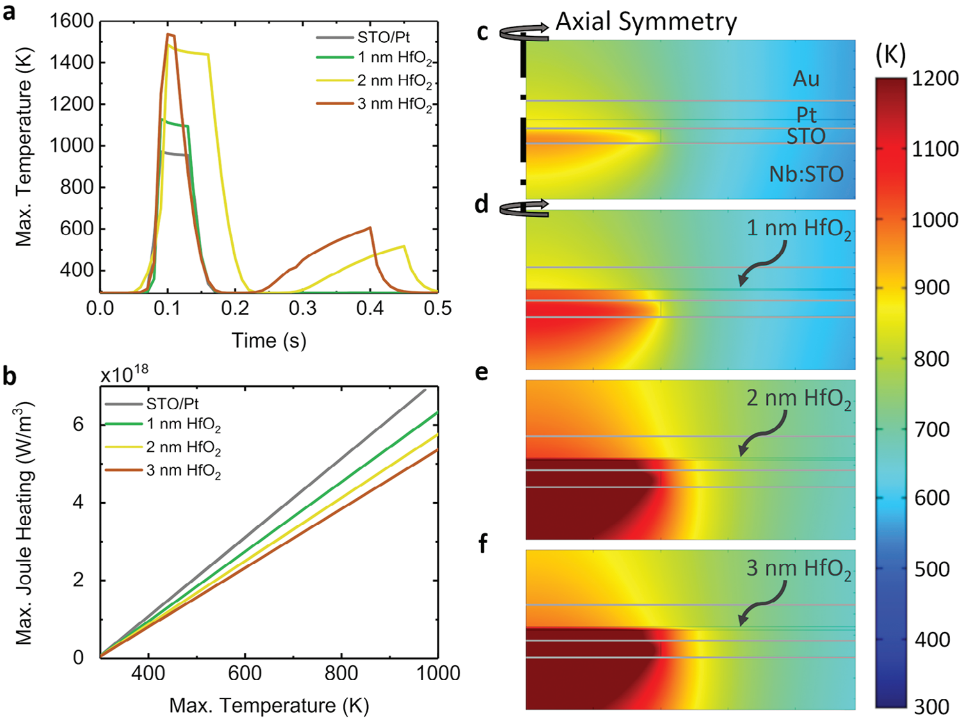

Figure 3. Calculations of local temperature. a) Maximum temperature reached for each sample calculated by the currents of the *I*–*V* sweeps as input, as a function of time. b) Heating efficiency of each sample based on the necessary Joule heating needed to reach the maximum temperature for each sample. 2D temperature profiles at $t = 0.1$ s for the reference STO/Pt configuration without interlayer c) and the configurations with HfO_2 interlayer thicknesses of d) 1, e) 2, and f) 3 nm, respectively. A vertical boundary line in the STO layer marks the outer edge of the filament. The additional horizontal line in the Pt layer reflects the two-step platinum evaporation, in order to ensure that the observed behavior is due to the insertion of the interlayers. The arrows indicate the position of the interlayers inside the Pt electrode.

interlayer, the temperature difference at the two sides of the interlayer becomes larger. As a consequence of the heat-blocking effect of the HfO_2 interlayer, the temperature at the filament region can be up to ≈500 K higher for the thicker interlayers compared to the reference STO/Pt devices. Here we must note that the temperature calculations are very sensitive to the choice of the filament dimensions. We have chosen the filament radius as $r_{filament} = 200$ nm, based on previous reports on STO-based ReRAM devices.[50,57] The results on the local temperatures and the heating efficiency for other filament diameters are presented in Figure S9 (Supporting Information).

All the samples studied in this work exhibit similar *I*–*V* characteristics as have been reported in the literature for crystalline STO devices.[21,49,50] Here it is important to remember that the slightly increased DC-switching voltage for the devices with the heat-blocking layers refer to the voltages required to reach the 10 mA of CC during the *I*–*V* sweeps (Figures 1b and 2b), and not to the voltage pulses required to SET the devices with an ON/OFF ⩾ 10 presented in Figures 1d and 2d. The forming voltage for almost all devices with embedded interlayers, except for the case of the high electrically conductive $TaO_{0.6}$ (see Figure S3, Supporting Information) are slightly increased compared to the reference STO/Pt devices. This is due to the increased series resistance introduced by the interlayer, which leads to a voltage drop across the device, resulting at a lower voltage that is actually applied at the STO/Pt interface. Nevertheless, the DC-switching voltage is in the similar range for all the devices (see Figure S3, Supporting Information). In addition, all devices with different configurations of heat-blocking layers have exhibited similar behavior to the reference STO/Pt devices when subjected to endurance measurements for 10.000 cycles (Figure S10, Supporting Information). However, despite completing the endurance cycling exhibiting good reliability, the devices with enhanced thermal confinement exhibit a slight increase in the cycle-to-cycle variability, compared to the reference STO/Pt devices.

Although the dissipation of heat through the Nb:STO substrate is also important, the active role of the STO/Pt interface, with oxygen being stored/released in Pt during the SET/RESET process, makes the local temperature at this interface particularly relevant for the speed of this process. Moreover, the lower thermal conductivity of the Nb:STO substrate ($\kappa = 8.7 \pm 10\%$ W m^{-1} K^{-1}) compared to the Pt electrode ($\kappa = 44.5 \pm 10\%$ W m^{-1} K^{-1}) ensures that the heat dissipation through the Pt is much larger, making it our point of focus for the thermal confinement approach. It has been reported in the literature[58,59] that in crossbar arrays of CMOS compatible filamentary ReRAM devices the heat is mainly transported via the electrode, highlighting the need for a strategy to block the heat in this main dissipation path. The FDTR measurements have confirmed the heat blocking efficiency of the TaO_x and HfO_2 interlayers, compared to the Pt electrode, reducing the heat dissipation along this channel, which in turn increases the local temperature and increases the mobility of oxygen vacancies during the SET process.[26,42,43,60,61] The increased local temperature is also confirmed by the calculated temperatures in

Figure 3a,c–f, where the temperature increase is ≈150 K for the 1 nm-thick HfO_2 interlayer and ≈500 K for the 2 and 3 nm-thick interlayers. The accelerated ionic movement is confirmed by the results of the SET speed presented in Figures 1d and 2d, where the SET speed is increased when the heat confinement effect is larger. Moreover, the samples with thicker HfO_2 interlayers exhibit a higher heating efficiency (see Figure 3b), meaning that in order to reach the same temperature, less Joule heating is needed for the samples with thicker HfO_2 interlayers. This directly translates to reduced current levels in order to achieve the same temperatures, thus improving the energy efficiency of the devices.

On the other hand, the electrical resistance between the two Pt electrodes in the $Pt/HfO_2/Pt$ samples is ≈ 50, 60, and 75 Ω, for 1, 2, and 3 nm of HfO_2, respectively (see Figure S2, Supporting Information). The electrical conduction through the HfO_2 layers is most likely due to lower density and possible local inhomogeneities of the sputtered HfO_2 in this thickness range that prevents complete electrical insulation between the two Pt layers. Considering the CC of 10 mA at higher voltages, the estimated voltage drop would correspond to 0.5, 0.6, and 0.75 V, respectively. This small increment in electrical resistance is overcompensated by the much larger increase in TBR, which goes from 18.8 to 20.5 $m^2K\ GW^{-1}$, along this series. Thus, this analysis suggests that the positive effect of ionic acceleration due to a higher local temperature, compensates the negative impact on the electrical conductivity of the Pt active electrode after inserting the heat-blocking layer. This trade-off between ionic acceleration and increased series resistance is clearly visible in the results of the SET speed of the HfO_2 interlayer samples, compared to the reference STO/Pt devices (Figure 2d). The ionic acceleration for the 1 nm-thick HfO_2 interlayer is compensated by the increase in series resistance inside the Pt electrode. However, the positive effect of the thermally accelerated ionic motion is highlighted for the devices of the 2 and 3 nm-thick HfO_2 interlayer, achieving faster SET times up to 3 orders of magnitude compered to the devices of the STO/Pt reference sample.

In the case of the TaO_x samples, we observe a similar behavior, with the TBR increasing linearly with increasing thickness. The different slopes in the linear increase of the TBR for the two different oxygen concentrations of the TaO_x samples reflect the different thermal conductivity values obtained earlier. The TBR value for the more oxygen-deficient $TaO_{0.6}$ is closer to the TBR value for the reference STO/Pt interface, due to its high electrical conductivity and different stoichiometry compared to its less oxygen deficient $TaO_{1.2}$. In the latter case, the TBR values are much higher, closer to the values obtained for the HfO_2 interlayers. This effect is also reflected in the results of the SET speed depicted in Figure 1d, where the more electrically and thermally resistive $TaO_{1.2}$ interlayer devices exhibit slower SET speeds for the whole range of voltages and times. On the other hand, the more electrically (and thermally) conductive $TaO_{0.6}$ interlayer devices show a constant acceleration of the SET speed of up to one order of magnitude in terms of time, compared to the STO/Pt devices. Here, it is important to point out that the TBR values of the TaO_x interlayers are becoming comparable to the HfO_2 interlayer TBR values, when the thickness of TaO_x is above 20 nm for the case of the less oxygen-deficient $TaO_{1.2}$ and always lower for the case of $TaO_{0.6}$ even at 40 nm. The trade-off between thermal and electrical conductivity should be carefully taken into consideration and the thickness and stoichiometry of the heat-blocking interlayers should be optimized accordingly.

Our results have confirmed the hypothesis that blocking the heat dissipation at the active metal electrode of a filamentary VCM device can increase the local temperature at the filament region, resulting in accelerated SET process. In more industrially relevant and widely implemented CMOS-compatible systems, such as HfO_2 or TaO_x, speed might not be the primary goal, since both systems have exhibited record breaking speeds. However, by implementing our strategy of blocking the heat in its main dissipation path, one could operate the devices at the same speed while applying lower voltage pulses, resulting in a more energy-efficient device operation.

In conclusion, introducing the heat-blocking interlayers has been successful with respect to the acceleration of the switching speed of the STO-based ReRAM devices, achieving up to 10^3 faster times. However, the switching speed is not the only crucial parameter in the device operation, where the operating voltage for the devices dictate the energy consumption of the device array in potential computing architectures. We have shown that by implementing the thermal confinement approach, the devices can be operated at the same switching speeds, but at ≈ 30% lower voltages. This reduction in energy cost can be even more appreciated when the energy consumption of the overall number of devices and operations are taken into account. This opens a window toward more efficient device operation with a strategy that is CMOS compatible, making our approach easily implemented in established processes of ReRAM device fabrication.

3. Experimental Section

Sample and Device Fabrication: The STO thin films were fabricated by pulsed laser deposition (PLD), grow epitaxially on Nb-doped (0.5%wt) STO substrates, at 800°C and 0.1 mbar O_2 pressure, at 5 Hz. The growth process was monitored by reflection high-energy electron diffraction (RHEED) and the observation of oscillations confirmed the layer-by-layer growth. The STO films were intentionally grown as Sr-rich, which according to previous works, enhances the retention performance of the devices,[60] but can also lead to slower SET speed.[22] The surface morphology was examined by atomic force microscopy (AFM) images and the crystalline quality by X-ray diffraction (XRD) measurements.

Once the STO thin films were structurally characterized, 10 nm of Pt were thermally evaporated to form the Schottky barrier with the STO thin film. To minimize the sample-to-sample variability on the performance of the devices, the same 10 × 10 mm STO thin film was used to prepare the different samples, by cutting it into four different pieces. The pieces were separated after the evaporation of the Pt top electrode, to ensure that the STO/Pt interface meets the quality standards and is undisturbed by possible side-effects during the cutting of the sample. In continuation, three samples underwent the HfO_2 interlayer sputtering deposition of 1, 2 and 3 nm thickness while one was kept as a reference sample. The TaO_x interlayers were sputtered using a Ta target with background atmosphere of Ar mixed with 1% O_2 gas, at different pressures. The amorphous TaO_x and HfO_2 heat-blocking layers were sputtered at room temperature, under tailored, and fully oxidizing conditions, respectively. In the next step, an additional 20 nm of Pt was evaporated on all samples, so any different performance of the devices were attributed to the presence and thickness of the interlayers, when compared to the reference sample. The stoichiometry of the HfO_2 was confirmed by X-ray photoemission spectroscopy (XPS) in situ after sputtering, while the stoichiometry for the TaO_x interlayers was determined based on previous work by T. Heisig et al., from which the sputtering parameters where adapted.[48]

The patterning of the devices was performed by optical lithography in three different steps. First, the device area ($8 \times 6\ \mu m$) was patterned and then the rest of the Pt/Interlayer/Pt was etched away, together with the 15 nm of STO underneath. In the next step, the contact area of the subsequent top leads was defined and the rest of uncovered area was sputtered with $\approx$ 45 nm of HfO_2 to electrically insulate the bottom electrode (Nb:STO substrate) from the subsequently thermally evaporated top leads. As a last step, the top leads were patterned and thermally evaporated, 10 nm of Pt and 60 nm of Au. For the samples with the reduced tantalum oxide as a thermal barrier, the same procedure was followed. In order to avoid any further oxidation of the TaO_x thermal barriers, an additional 10 nm of Pt were sputtered in situ. The rest of the lithography process was similar, as described before.

The devices were formed with a positive voltage applied to the top electrode, while the bottom electrode (Nb:STO substrate) was grounded. After the forming step, the devices were switched multiple times, using voltages of +2.5 and −4.0 V for the SET and RESET process respectively. The forming and SET process were limited by a 10 mA current compliance.

Frequency Domain Thermoreflectance (FDTR): The thermal conductivity of the different layers and their thermal boundary conduction were measured with the frequency domain thermoreflectance (FDTR) technique.[51,52] This is a non-contact pump–probe optical technique based on the dependence of the reflectance of a metal transducer with its local temperature. In this technique, a sinusoidally modulated continuous wave (cw) pump laser ($\lambda = 488$ nm, $f = 0.5 - 5$ MHz) is directed on the sample surface, coated with a metallic transducer layer (Au: 40–60 nm), and produces a modulation of the surface temperature. The change of the thermoreflectance of the Au is monitored by the probe cw laser. The effective thermal conductivity κ_{eff} and the thermal boundary resistance (TBR) between the different layers is calculated by the phase lag between the pump and the probe signals.

To extract the thermal conductivity κ and the thermal boundary resistance (TBR) from the FDTR phase-shit curves, a model was fitted with them wherein total energy conservation and energy transfer between layers are imposed by a transfer matrix, as explained elsewhere.[51] More details of the technique and results on the thermal conductivity of thin films can be found in [53,62]. To reduce the number of fitting parameters, the thermal conductivity was first measured of the Nb:STO substrate ($\kappa = 8.7 \pm 10\%$ W m K) and subsequently of the STO thin film ($\kappa = 5.4 \pm 10\%$ W m^{-1} K^{-1}). The thermal conductivity of the Au and Pt layers were determined by measuring the electrical conductivity and using Wiedemann–Franz's law ($\kappa/\sigma = LT$), and then were further adjusted for optimal fitting of the data.

Electrical characterization & Kinetics measurements: The electrical characterization of the devices for the *I–V* sweeps were performed on a probe station where the top electrodes were contacted via tungsten whisker needle and the Nb:STO substrate (bottom electrode) was contacted through aluminum wire-bonding. As a current source, a Keithley 2611A Source Meter was used. The typical voltage step was 30 mV s^{-1} with a waiting time of 5 ms between each step. The voltage was increased from 0 to +3 V for the electroforming of the devices, followed by a sweep from 0 to –4 V, to reset the devices to their high resistive state. Subsequent *I–V* sweeps were repeated from 0 to +2.5 to –4 V and back to 0 V in order to cycle the devices and ensure their stable behavior. The resistive state of the devices were determined by *I–V* sweeps from –0.3 to + 0.3 V, and using a linear fit of the slope. The current compliance was set at 10 mA for all devices. The pulsed measurements were performed at a different probe station using tungsten whisker needles, as described before, and as a power source, a Keithley 4200, using a custom software written in a LUA environment.

The SET speed of the devices were measured according to the following protocol: the device was reset to a high resistive state (HRS) by applying pulses of defined length (time) and progressively increasing height (voltage), until a defined value was reached (600 MΩ ±20%). The value of the device resistance was measured with a read-out (RO) pulse with height of 0.3V and 60ms length, before and after every reset pulse. Once the defined HRS was reached, the SET pulses begin, starting with the lowest height (1.5V) and applying pulses with increasing length of one order of magnitude (here it started with 20 ns instead of 10 ns due to the equipment limitation). As in the RESET process, before and after each SET pulse, the resistance was read-out at 0.3V. If one of the pulses bring the device resistance to a value lower than the defined HRS, the RESET process started again, preparing the device for the next SET pulse. When a SET pulse achieved a successful SET event, the rest of the pulse lengths for the same voltage were skipped and the process continues with for the next pulse height in the sequence. Here, a successful SET is defined as a event when $\frac{R_{HRS}}{R_{LRS}} > 10$.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by the DFG (German Science Foundation) within the collaborative research center SFB 917 "Nanoswitches", by the Helmholtz Association Initiative and Networking Fund under Project No. SO-092 [Advanced Computing Architectures (ACA)] and the Federal Ministry of Education and Research (Project NEUROTEC, Grants No. 16ME0398K and No. 16ME0399).

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

resistive switching, switching speed, thermal management

Received: July 17, 2024
Revised: August 2, 2024
Published online:

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