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Solid-State Electrochemistry of SiC Ceramics - Experiment vs. Simulation

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Abstract

Owing to their outstanding mechanical properties SiC-based ceramics are difficult-to-machine materials. Electrochemical Machining (ECM) is a promising alternative technology. However, in contrast to the ECM of metallic materials machining the electric and dielectric properties of semiconductors like silicon carbide plays a crucial role regarding in the efficiency of the process. Corresponding investigations are therefore necessary to better understand the influence of the mentioned properties on the ECM process and to be able to offer appropriate material development. The present study demonstrates a complementary approach of experiment and simulation to describe the electrochemically relevant solid-state properties of SiC ceramics. Impedance spectroscopy and voltage-ramp short-circuit tests provide experimental data on the resistance properties of SiC ceramics, which are used as input for the simulation. The results of the electrodynamic and thermodynamic simulations provide information about the differential voltage depending current density and lateral temperature distributions. This study emphasized the combination of experimental and simulation results to analyse the material properties of SiC for ECM.

1 Introduction

SiC ceramics are known for their exceptional mechanical strength, thermal stability, and chemical resistance. These characteristics make SiC suitable for a wide range of applications, such as abrasives, pumps, and valves in pyrometallurgy [1-4]. Otherwise, mechanical machining of SiC is usually associated with high wear on the tools and low process speed. While machining techniques such as laser beam machining (LBM) and electrical discharge machining (EDM) are feasible, they are also time consuming due to the high melting point of SiC [5, 6].

In contrast, electrochemical machining (ECM) is a promising alternative process, as the machining speed is independent of the mechanical properties and there is no significant tool wear [7]. Typically, the electrical properties of the metallic materials can be disregarded in the ECM process. However, this does not apply to semiconductors such as SiC, which are characterised by significantly lower conductivity compared to metals and a corresponding dielectricity. Therefore, experimental investigations of these properties are essential to understand their subsequent influence on ECM. Numerical simulation models that enable electrodynamic and thermodynamic simulations can be used to gain insights into the differential current density and lateral temperature distribution. Ideally, the overall results can be used to predict the processing parameters of the material in the ECM process. Furthermore, a rapid transfer of the simulation to other cathode geometries is easily conceivable.

2 Experimental setup and methods

2.1 Material

Three solid-state sintered SiC (SSiC) samples with different types and contents (confidential) of sinter additives were produced by Fraunhofer IKTS. The properties of the materials are summarized in Table 1.

Table 1: *Properties of the investigated SSiC materials.*

sample	*sinter additive*	*density*	*thermal conductivity at 20 °C*
SSiC-1	AlB_2	$3.11\ g\ cm^{-3}$	$109\ W\ m^{-1}\ K^{-1}$
SSiC-2	AlB_2	$3.07\ g\ cm^{-3}$	$105\ W\ m^{-1}\ K^{-1}$
SSiC-3	Al_4C_3	$2.98\ g\ cm^{-3}$	$74\ W\ m^{-1}\ K^{-1}$

2.2 Solid-state electrochemistry

The experimental setup for determining the relevant electrical and dielectric properties was designed to replicate the typical drilling process in ECM. Therefore, a spring pin (outer diameter 0.22 mm) was placed on the material surface and fixed with conductive silver paste (Plano GmbH) to establish the ohmic contact. The silver paste droplet was considered as the measurement area. The ohmic contact of the samples (11 mm · 11 mm · 1.34 mm) was established by attaching them to a copper plate by conductive silver paste. (Figure 1 a).

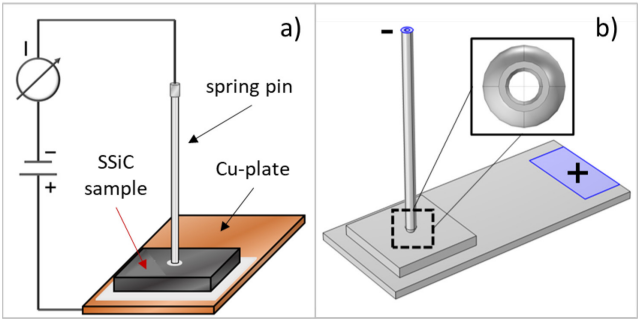

Figure 1: *a) Experimental setup for solid state electrochemical measurements [8] and b) simulation geometry.*

The electrical properties were investigated using two methods. First, the electric and dielectric properties of SSiC-samples were determined using stationary impedance spectroscopy. The equivalent circuit shown in Figure 2 was used to interpret the measured impedance spectra. Metals have no dipoles and therefore no capacitive properties. Due to the high electrical conductivity of the copper plate (Cu), the silver conductive paint (Ag), and the metallic spring pin, all can be neglected. For the semiconducting SiC, both, capacitive (C) and ohmic properties (R) were considered.

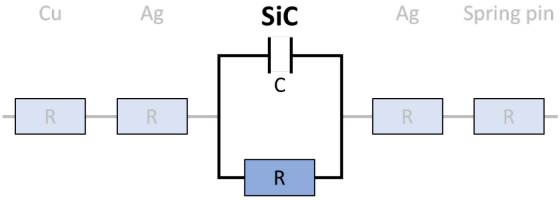

Figure 2: *Equivalent circuit of the solid-state electrochemical cell using SSiC as anode material.*

Second, the voltage-dependent, differential electrical resistance was investigated by dynamic voltage ramp tests. Additionally, a thermocouple was

incorporated into the setup of voltage ramp tests to measure the sample's temperature during the test. The tip of the thermocouple was fixed approximately 1 mm from the position of the spring pin on the sample surface. The experimental parameters of both investigations are summarized in the following Table 2.

Table 2: *Experimental parameters for electrical and dielectric characterisation.*

Impedance spectroscopy		***Voltage ramp test***	
DC	*0.01 V*	*Voltage range*	*0 V – 100 V*
AC	*0.01 V*	*Scan rate*	*0.01 / 0.1 / 1 V·s^{-1}*
Frequency	*0.1 Hz – 1 kHz*	*Current limit*	*2 A*

2.3 Simulation

To evaluate the temperature distribution during experiments as a result of Joule heating, a 3D model was developed using COMSOL Multiphysics ® software. This model uses COMSOL interfaces “Electric Currents”, “Heat Transfer in Solids” and “Electromagnetic Heating” to couple thermodynamics and electrodynamics. The geometry for the simulation was derived from the experimental setup and can be seen in Figure 1 b). The spring pin was placed on the SSiC sample, which in turn lay on copper plate. The upper surface of the pin was defined as a negative contact, and the upper surface on right edge of the copper as a positive one (both surfaces are blue in Figure 1 b)). Voltage as function of time was defined based on data from experiments. At all surfaces, a convective heat flux with a heat transfer coefficient of 100 W (m2·K)-1 and a external temperature of 23.9 °C was defined. The material properties of the spring pin and the copper plate were defined according to materials from the COMSOL Material Library: "AISI 4340 Steel" and "Copper" respectively.Thermal conductivity of the SSiC was defined according to experimental results (Table 1). Electrical conductivity of SSiC-1 was modelled from experimental data using the following equation as a function of applied voltage and temperature:

$$\sigma = 39.425\ [S/m] \cdot \ln(2\ [1/V] \cdot U + 0.8) + 0.7215\ [S/(m \cdot ℃)] \cdot T - 12.7\ [S/m]$$

Other material properties of the SSiC-1 sample were taken from COMSOL material library (material “SiC”).

3 Results

3.1 Solid state electrochemistry

Firstly, the electrical properties of the SSiC materials were analysed using stationary impedance spectroscopy. The phase angle ϕ shown in Figure 3 maintains a constant value of zero for all samples across the entire frequency range, indicating ohmic behaviour.

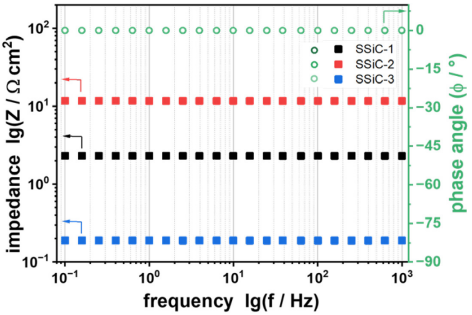

Figure 3: *Bode plot of the investigated SSiC materials.*

Since no capacitive behaviour can be determined in the measured frequency range, the impedance can be equated to the ohmic resistance. This resistance includes the resistance of the SSiC sample and the resistances of all ohmic contacts but is almost exclusively determined by the resistivity of the ceramic. The resistivity of the ceramic was calculated using the sample thickness of 1.34 mm and the size of the silver droplet as a measuring area. The results of the resistances are summarized in the Table 3. To verify the ohmic property, the capacitive reactance was calculated:

$$C = \varepsilon_r \cdot \varepsilon_0 \cdot \frac{A_{measurement\ area}}{d_{SSiC\ sample}}, \varepsilon_R(SiC) = 10\ [9]\ ;\ |X_C| = \frac{1}{2 \cdot \pi \cdot f \cdot C}$$

This reactance amounts to $2.41 \cdot 10^7$ Ω cm² at a frequency of 10^3 Hz, which is approximately seven orders of magnitude above the effective resistance (see Table 3). In the SiC equivalent circuit (Figure 2), the current flows through the resistance, and conduction through the capacitor would occur only at very high frequencies > 10^9 Hz and is not visible in the measured frequency range. The results of solid-state impedance spectroscopy indicate that the addition of various sintering additives enables the adjustment of specific electrical conductivities that are necessary for the ECM process. Secondly, dynamic voltage ramp tests were conducted to analyse the varistor properties of SiC (Figure 4 a).

Table 3: *Effective and specific resistance of the SSiC materials.*

sample	*effective resistance*	*effective specific resistance*
SSiC-1	*2.31 Ω cm²*	*17.24 Ω cm*
SSiC-2	*11.66 Ω cm²*	*87.01 Ω cm*
SSiC-3	*0.19 Ω cm²*	*1.41 Ω cm*

Surprisingly, only the sample SSiC-2 shows the typical varistor behaviour. From 12 V (scan rate 0.01 $V \cdot s^{-1}$), the current density increases exponentially until the current limit of the potentiostat of 2 A is reached. The voltage in question is referred to as the switch voltage. Below this voltage, varistors show linear relation between current and voltage depending on the temperature [10] due to Joule heating Q (Figure 4 b).

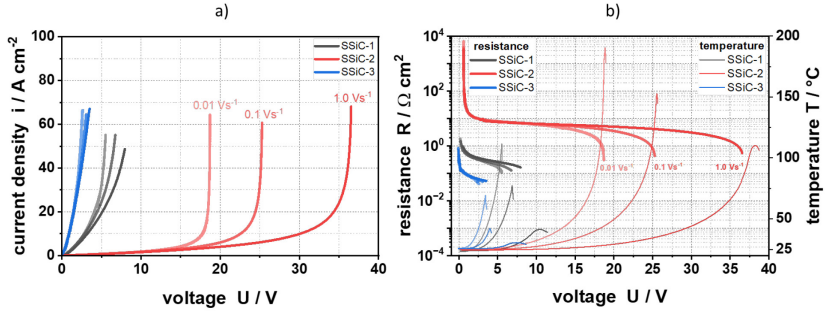

Figure 4: *a) Current density-voltage curve and b) resistance-temperature-voltage curve of the voltage ramp test.*

As well-known, heating reduces the resistance of the semiconductors. If the scan rate increases, the temperature of the sample decreases, due to the reduced heat impact ($dQ = (U^2/R)\,dt = I^2(t)Rdt$ [11]). This also leads to higher switching voltages. In accordance with the resistances listed in table 3, the resistances of SSiC-1 and SSiC-3 are lower in the voltage ramp tests. Due to the higher conductivity of these materials, the current density-voltage curve (Figure 4 a) of varistor behaviour shifts more towards that of a typical semiconductor. Lower voltages are required to reach the current limit, which also results in lower temperatures. Furthermore, the dependence on the scan rate diminishes as the conductivity of the materials increases. From the solid-state tests, it can be concluded that SSiC-1 and SSiC-3 could potentially be processed by ECM at low voltages of less than 10 V. In contrast, higher voltages would be necessary for SSiC-2. However, the required voltage could be reduced by heating the material during the ECM process.

3.2 Simulation

Figure 5 a shows the results of the simulation for SSiC-1: the total resistance of the simulated system and the temperature at a point 1 mm away from the centre of the spring pin contact. The temperature increases faster with decreasing scan rate. The maximum temperature in the model agrees well with the experiment for the scan rate of 0.1 V·s^{-1}, but is overestimated for a scan rate of 0.01 V·s^{-1} and underestimated for a scan rate of 1 V·s^{-1}. Also, the temperature growth rate differs from the experimental results, which may indicate a difference between real thermodynamic conditions and those selected in the model.

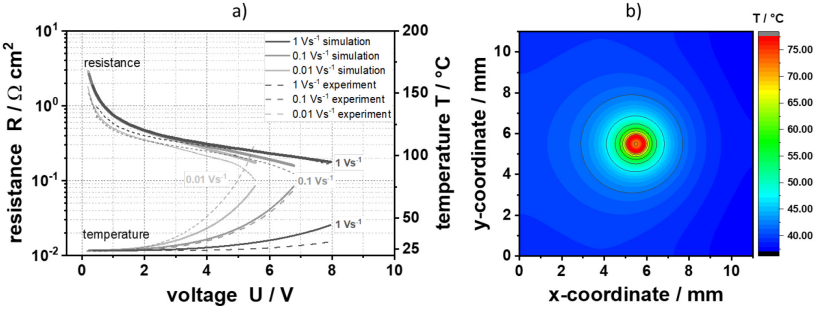

Figure 5: *Simulation results a) resistance-temperature-voltage curve of the voltage ramp test (SSiC-1) and b) temperature distribution over the SiC surface for 1 V·s^{-1} at final voltage of 7.95 V.*

In addition, the decreasing resistance in figure 5 a indicates that the electrical conductivity of SSiC increases with increasing temperature. *Figure 5 b)* shows the temperature distribution over the SSiC surface for a scan rate of 1 V·s^{-1} at final voltage of 7.95 V. The maximum of 77.6 °C is observed at the points of direct contact of the spring pin with the SSiC, while the maximum temperature at the measuring point corresponding to the experiment was only 44.4 °C.

4 Summary

Through variation of the sintering additives, the electrical conductivities required for the ECM process were adjusted. Thereby, the increasing of sintering additives do not result in a simple relation of resistivity ρ and sintering additive concentration c ($\rho \sim c^{-1}$), but in principle change of conductivity at low additive concentration. With increasing conductivity, the electrochemical behaviour of SSiC was shifted from typical varistor behaviour towards that of a typical semiconductor. Initial simulations demonstrated good agreement with experimental

results. By further improving the simulation models, it is ideally possible to predict process parameters for future SiC materials.

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