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Abstract

In this roadmap we consider the status and challenges of technologies that use the properties of a rectifying metal-semiconductor interface, known as a Schottky barrier (SB), as an asset for device functionality. We discuss source gated transistors, which allow for excellent electronic characteristics for low power, low frequency environmentally friendly circuits. We also consider reconfigurable field effect transistors. In such devices, two or more independent gate electrodes can be used to program different functionalities at the device level, enabling ultra-secure embedded devices. Both types of transistors can be used for neuromorphic systems, notably by combining them with ferroelectric SB transistors which enable a large number of analog states. At cryogenic temperatures SB transistors can advantageously serve for the control electronics in quantum computing devices. If the source/drain of the metallic contact becomes superconducting, Josephson junctions with a tunable phase can be realized for scalable quantum computing applications. Developing applications using SB devices requires physics-based and compact models that can be used for circuit simulations, which are also discussed. The roadmap reveals that the main challenges for these technologies are improving processing, access to industrial technologies and modeling tools for circuit simulations.

1. Introduction

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As the semiconductor industry moves towards ever smaller transistors and as smart devices emerge in our daily lives, new types of materials for novel circuits and hardware are emerging as viable alternatives to conventional silicon technologies. While new materials offer promising alternatives for their sustainability, flexibility or transparency, an important parasitic often arises that is due to heterogeneous contacts. It results in nonlinear behavior at the interface, due to the potential energy barrier, and is known as the Schottky barrier (SB). An emerging field of electronics proposes that, in some circumstances, such devices and circuits can advantageously realize analog, digital and cryogenic systems.

This idea has its roots in the use of SBs as the source and drain contacts in an otherwise conventional MOSFET, which was first considered in the 1960s [1]. It has been reconsidered many times over the past 60 years, as reviewed in [2–4]. Recently, the advent of SB carbon nanotube circuits is a promising direction [5, 6], however, the large majority of carbon nanotube devices seek to minimize the SB and not use it as an asset.

In this roadmap, we address the class of devices that use the SB as an advantage and focus on the status and challenges that are faced. We first consider source gated transistors (SGTs), where the SB between the source contact and the channel controls transport. Transistors can be realized in a large variety of different material systems (amorphous silicon or oxide semiconductors, organic semiconductors), the most promising of which are flexible and environmentally friendly. These devices have great potential to be easily scalable in the nano-scale regime, because transport is dominated by the source and, for the most part, short channel effects do not degrade device performance [7]. This allows for excellent device characteristics for low power, low frequency environmentally friendly and highly scalable circuits. The most promising applications for these devices are for analog electronics, sensor readout, and especially in edge and neuromorphic devices.

Neuromorphic devices in any material system can potentially take advantage of ferroelectric SBFET synapses. These devices allow for low temperature processing, avoiding the difficulty in realizing high energy implantation activations in conventional silicon devices. In addition, their intrinsic ambipolarity enables both excitatory and inhibitory behavior and the realization of a large number of analog states.

Another emerging computing paradigm where SB devices can have an important impact is quantum computing at cryogenic temperatures. One field of application is to employ SB devices in low temperature electronics, especially for the control circuits of spin-based qubits, where their simpler fabrication, robustness to freeze-out [8] and improved switching compared to conventional silicon transistors are important advantages. The second application is to use source/drain metals that become superconducting at low temperatures in order to enable Josephson FETs. Josephson coupling occurs when the semiconductor acts as a weak link between the superconductivity in each electrode so that the probability of transport into either superconducting electrode depends on the phase difference. Its realization in a gated structure, where the carrier density of the channel can be modulated, enables the realization of a gate tunable transmon or 'gatemon' [9].

While SGTs take advantage of the semiconductor thickness to realize devices where the SB is controlled by the gate, an geometry is to consider adding additional gates in a planar geometry. Such reconfigurable field effect transistors (RFETs) can be biased either as n-type or p-type and be programmed for different functionality. These devices are particularly promising from a security perspective because device operation is determined by programming so that circuit functionality cannot be understood by reading the circuit design and layout in a foundry. In addition, programming at the device level can inhibit potential attacks and protect data from threats. RFETs can be used for analog or digital circuits and have promising applications in both neuromorphic computing and for quantum computing.

The roadmap thus encompasses SB devices realized in a wide range of different of materials and for different applications, but they face similar challenges, as highlighted in table 1. As with most emerging devices realized in a laboratory, one major challenge is to realize compact models that can be used to design circuits for applications. The specific problem is that such devices can have parasitics due to temperature, light or humidity that result in models that may not be able to describe all the observed effects. Distinguishing such effects from those due to the particular geometries, as in SGTs and RFETs can be an important challenge. Nevertheless, models are essential to explore the more complex circuits designs needed in SGT and RFET technologies.

SB devices often do not make use of source/drain doping and as a result involve fewer high temperature anneals and fewer processing steps. Their processing should be more sustainable than comparative silicon technologies, but a full analysis has not yet been done. As with most emerging technologies, process

Table 1. Overview of grand challenges in SB devices.

Grand challenges for SB devices
Compact modeling for accurate circuit design
Realizing SB transistors in sustainable technologies
Process optimization for high performance devices and circuits
Increased complexity of circuit designs (SGTs, RFETs)
Engineering devices for optimal functionality
Increasing switching speed
Variability, yield reliability

optimization is key to realizing high performance devices and functionality. This remains a challenge for all the SB devices considered here.

The presence of the SB can result in lower switching speeds than in other devices. This can be improved with some engineering tricks but remains an important concern. Finally, variability and yield reliability can be an issue for the SB devices. However, for the majority of the devices in this roadmap, these concerns should not exceed those typically faced for electronics.

The most promising applications will likely be dictated by their integration, for instance using SGTs as control circuits displays using amorphous oxides or as analog readout and/or neuromorphic classification circuits for wearables made with organic electronics. Nevertheless, the implementations and uses developed in one material system that might solve a problem for a particular application can be translated into other applications, creating potentially interesting synergies. One of the promising features of SGTs is the ability to enable very stable gain in devices that can be fabricated in using sustainable manufacturing processes. They are and increasingly interesting option in an environment with where edge devices and sensors are becoming ever more ubiquitous.

A large part of the roadmap considers devices that are compatible with CMOS technologies, notably, the ferroelectric SBFETs as synapses, cryogenic devices and RFETs. SBFETs can add increased functionality, potentially reducing circuit overhead. This is most notably the case for RFETs, which have an added bonus of increased hardware security. SBFETs are also promising for neuromorphic applications with complex classification tasks because of their ability to mimic many biological features. Finally, cryogenic SBFETs are most promising for control electronics for low temperature quantum computing applications, where high performance and reduced processing steps can offer a true competitive advantage.

The emerging field of electronics encompassing SB devices includes many different fields of applications. One challenge is to group together the important results to provide a cross-pollination for future work, which is the objective of this roadmap.

2. Source-gated thin-film transistors

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Status

Thin-film transistors (TFTs) offer tremendous flexibility of implementation for a wide variety of electronic applications. In general, the largest possible current density is preferable in the on-state and is achieved in part by reducing the effects of energy barriers arising at the semiconductor-contact interface. However, this can be difficult in practice and there are numerous applications that do not require the highest possible current density, transconductance and switching speed. Such applications, including certain key parts of display pixel circuits, biological or chemical sensors, signal amplification, uniformity of performance, and power efficiency, are of increasing importance.

A class of TFTs, that counterintuitively rely on the deliberate introduction of contact energy barriers, are able to meet these requirements. They can be implemented in a wide variety of material systems and fabrication processes. Of these contact-controlled transistors, the source-gated transistor (SGT) [10, 11], as depicted in figure 1, has been extensively studied [12–15] and shows significant promise. The main advantages of this technology is low saturation voltage, low power operation and potentially increased stability and uniformity of TFT output.

Current and future challenges

Despite its relatively long history, and the recent advances in reducing the inherent temperature coefficient of its drain current [15], the SGT still faces challenges for widespread implementation. Firstly, the structure requires an overlap between the source and gate contacts arranged in a staggered-electrode configuration, which is not always accessible in commercial fabrication processes. Secondly, the requirement for a rectifying contact at the source can lead to added complexity in manufacturing, as such contacts may need an additional separated patterning step compared to conventional TFTs within the same design [16]. Moreover, creating Schottky contacts with suitable uniformity is challenging in many technologies due to surface morphology, interface behavior during material deposition, and even surface reactions during operation [17]. Finally, the operating principle governing the transistor relies on a relatively low gate insulator capacitance to achieve early saturation [18]. As a result, high gate voltages may be required. This is potentially problematic in battery-powered wearables or in circuits that switch frequently.

Advances in science and technology to meet challenges

The adoption of contact-controlled transistors for applications depends almost exclusively on the ability to engineer structures and circuits that bring superior performance justifying the additional processing cost [14]. One advantage of SGTs is that increasing the transconductance and current density can be realized through scaling, both laterally and vertically, by taking advantage of the reduced short-channel effects in SGTs. This scaling will enable the use of lower energy barriers at the source for increased charge injection. In principle, scaled SGTs should be able to provide the same current density as TFTs made with the same technology, where low output conductance measured in saturation is sought [14].

Semimetals may also provide a route to increasing current density, by virtue of the relatively high mobility that these materials could attain when used as active layers [19], as shown in figure 2. The challenge here, however, is realizing a uniform and controllable source contact. Potential improvements regarding the uniformity of rectifying contacts, particularly in the case of metal oxide semiconductors and semimetals, may come from the use of: interfacial layers [17], including self-assembled monolayers; nanoscale insulators or semiconductors, deposited through atomic layer deposition; or even two-dimensional semiconductors inserted between the source metal and the active layer. Not only would these methods allow improved uniformity of injection across a large area, but they may provide a route to drastically reducing the temperature dependence of drain current. Following in the footsteps of emerging display technologies in which heterogeneous integration of structures, such as micro-LEDs, is realized via transfer techniques, atomically perfect crystals and van de Waals contacts are being employed together to greatly boost the net current density through the device.

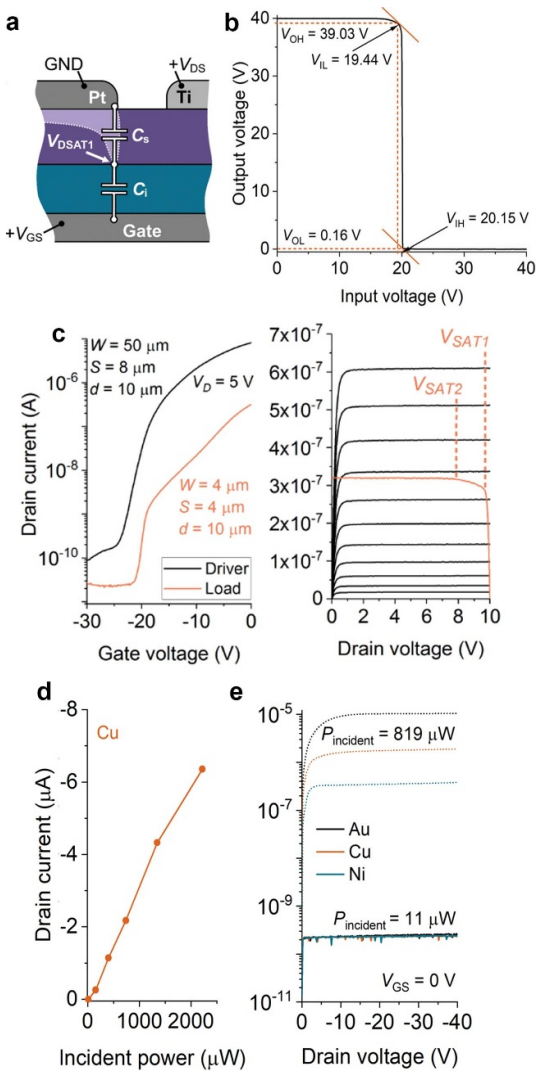

Figure 1. (a) Cross-section of a InGaZnO source-gated transistor (SGT) with a Pt source contact; and (b) complementary high-gain inverter using amorphous oxide InGaZnO and organic DNTT SGTs. Reproduced from [13] with permission from the Royal Society of Chemistry. (c) Transfer and output characteristics of low-temperature polycrystalline Si SGTs demonstrating favorable high gain-promoting flat saturation. © [2020] IEEE. Reprinted, with permission, from [14]. (d) Organic photo-SGTs (OPSGTs) in DNTT with linear photo response; and (e) OPSGTs with Ni contacts demonstrating low voltage, flat saturation. [15] John Wiley & Sons. © 2023 The Authors. Advanced Optical Materials published by Wiley-VCH GmbH.

In all these cases, the semiconductor-insulator interface still represents an important site for optimization. Distinct from conventional TFTs, SGTs rely on a concentration of electric field at the edge of the source [10]. While essential for achieving early saturation, this may lead to reliability problems if not designed correctly, from a surface and interface point of view [18].

Finally, successful implementation in meaningfully complex circuit designs will rely critically on the availability of suitably functional compact models, as discussed in section 11. Efforts are incipient [20], and it is important to stress that not all regions of the operating characteristics of the SGT are equally important for accurate modeled. Therefore, concentrating on minimally viable empirical or physical models in the first instance will yield the necessary step-change for adoption in the design flow.

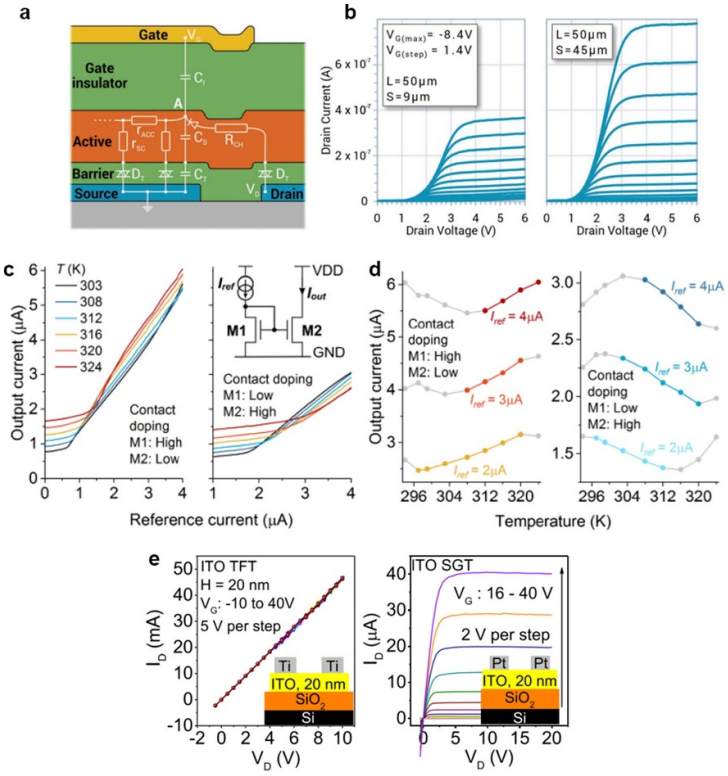

Figure 2. (a) Cross-section schematic, and (b) output characteristics for InGaZnO tunnel-contact SGTs. [17] John Wiley & Sons. © 2019 The Authors. Published by WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim (c) and (d) SGT current mirrors (inset) with differing contact properties can produce an output current with negative temperature dependence. © (2021) IEEE. Reprinted, with permission, from [16]. (e) Left: ITO TFT showing absence of transistor operation, Right: ITO SGT showing expected SGT behavior. Reproduced from [19]. CC BY 4.0.

Concluding remarks

Source-gated transistors have been simulated, fabricated, and characterized, for the best part of two decades. The main advantage is low saturation voltage, low power operation and increased stability and uniformity during TFT operation. Their operating principles are well developed, with some rules-of-thumb allowing simple initial implementation in practically any thin-film technology (see sections 3 and 4). The main process challenges are the increased complexity of fabrication, the potentially higher gate voltages necessary and the uniformity of the rectifying contacts. The development of compact models will greatly aid the adoption within more complex circuit designs, and material-specific interface controls will provide the necessary performance and uniformity characteristics for viable inclusion as functional building blocks in emerging sensors and active matrices. High intrinsic gain can be problematic if attempting to maintain a suitable bias point in open-loop configurations. Therefore, we expect this property to be most valuable in closed-loop applications such as voltage references, buffers, amplifiers, and also in current-biased circuits. We expect that SGTs are most promising for realizing custom-designed analog readout for sensors, and edge computing using neuromorphic architectures.

3. Amorphous oxide semiconductor SGTs

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Status

Amorphous oxide semiconductors (AOSs) are materials with high carrier mobility, high transparency, scalability to large substrates and the possibility of processing at low temperatures, making them very attractive for the next generation displays, various optical and electronic devices. Thin film transistors (TFTs) employing indium gallium zinc oxide (IGZO), the leading AOS material, have already been adopted into commercial displays [21]. In source gated transistor (SGT), the device operating speed is usually lower than conventional TFTs, due to the energy barrier at the source contact [10]. However, if AOSs are used as the active layers in SGTs, high performance can still be achieved due to their intrinsic carrier mobility, which is more than an order higher than amorphous silicon.

Table 2 summaries recent AOS SGTs. Most devices were made of IGZO by sputter deposition. The dielectric films are either thermal silicon dioxide or atomic layer deposited (ALD) Al_2O_3. The energy barrier at the source contact was realized by three methods: Schottky contact, tunneling contact, and combination of field plate with a high work function metal. Figure 3(a) show the cross section of a bottom-contact top-gate tunneling contact IGZO SGT [17]. It typically exhibits flat saturated output characteristics with low saturation voltage, high tolerance to transistor geometry such as the channel length and source length (figures 3(b)–(e)). However, a small intrinsic gain of 20 is reported, indicating careful process optimization was needed.

A notable device listed in table 2 is the Schottky-barrier IGZO SGT reported by Zhang *et al* [19]. This device exhibits a very high intrinsic gain of 29 000, no discernible threshold voltage shift under prolonged gate bias and illumination stress, and high immunity from effect of extremely short channel length as small as 360 nm.

Current and future challenges

Despite prolific use of IGZO in TFTs, there are only few reports on IGZO SGT as shown in table 2. The performance of IGZO SGTs is still poor and performance indicator like intrinsic voltage gain has rarely been reported. Therefore, dV_{D_SAT}/dV_{GS} is compared for the SGTs in table 2.

When fabricating devices, using a high work-function metal alone does not guarantee a rectifying Schottky contacts in AOS TFTs. Most AOSs are degenerate semiconductors with surface very sensitive to atmosphere and process conditions. During metal contact evaporation, the AOS surface is easily reduced, which hinders the barrier formation. Therefore, additional process steps are needed to counter this problem, such as the O_2 plasma treatment of the AOS surface prior to metal deposition, or deposition of metal in O_2/Ar atmosphere for forming a very thin oxygen-rich metal layer at the interface with semiconductor [19].

Previous simulation using polysilicon devices suggests that thinner field plates should produce SGT with best performance [22]. However, our recent IGZO SGTs show the opposite results [23]. Therefore, some device characteristics are not applicable across the different material systems.

The current AOSs are predominantly n-type semiconductors (also reflected in table 1). The development of equally high-performance p-type oxide semiconductors is critically important for realizing CMOS circuits.

Advances in science and technology to meet challenges

Optimization of process parameters and device geometry is vital for producing high quality oxide SGTs that are usable in circuits. Such efforts are aided by device and circuit simulations. Currently, most reports of IGZO SGTs are for individual devices, and circuit level demonstration is still lacking. SGT architecture can tolerate variation from the process parameters or that arising from device to device, however this has yet been verified experimentally in AOS SGTs.

In terms of materials, IGZO is a complex quaternary oxide. Simpler tertiary or binary oxides like zinc tin oxide or indium oxide should be explored for easier and cheaper processing [26]. Recent advances in precursor chemistry has enabled deposition of high quality, phase pure p-type SnO by ALD technology [28]. To increase carrier mobility of SnO, doping or alloying with other materials is currently studied.

Table 2. Summary of the AOS SGTs (L: channel length, S = source length).

Barrier type/contacts	Channel/Dielectric	Technology	L ; S (μm)	dV_{DSAT}/dV_{GS} (V/V)	Year	References
Schottky/TiW	ZnO/Hf_2O	ALD/ALD	16; 15	—	2013	[24]
Tunneling/Graphene + Ti	IGZO/SiO_2	Sputter/Th.ox.	18; -	—	2017	[25]
Schottky/Pt	IGZO/SiO_2	Sputter/Th.ox.	60; 1200	∼0.1	2019	[19]
Tunneling/Ni	IGZO/Al_2O_3	Sputter/ALD	50; 45	0.12	2019	[17]
Schottky/Au	In_2O_3/SiO_2	Sol./Th.ox	5; -	0.8	2023	[26]
Field plate/Pt	IGZO/Al_2O_3	Sputter/ALD	50; 45	0.12	2024	[23]
Field plate/Ti	IGZO/SiN-SiO_2	Sputter/CVD	50; 40	∼0.4	2023	[27]

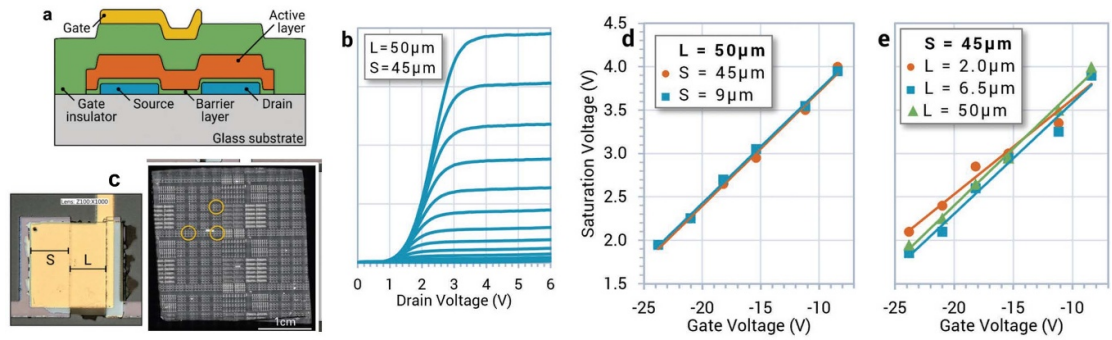

Figure 3. (a), (c) Cross section, images of a single SGT and the fabricated devices on glass substrate, (b) output characteristics, (d), (e) saturation voltage as a function of gate voltage for various channel length, L and source length, S of the tunneling contact IGZO SGT. [17] John Wiley & Sons. © 2019 The Authors. Published by WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

Concluding remarks

IGZO SGTs with various types of contact barriers has been demonstrated, showing typical flat output characteristics with low saturation voltage. Carefully optimized SGT devices are highly stable, and they exhibit extremely high intrinsic gain of 29 000. These are very promising results and indicate that it is a good strategy to be marrying high performance material like AOS with robust device design like SGT. IGZO SGTs are promising for integrating with flat panel displays using scaled transistors with this high intrinsic gain. However, many challenges remain, such as process optimization, production of high performance devices and circuits, development of p-type oxide materials, and simulation of device and integrated circuits.

4. Organic SGTs

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Status

Organic semiconductors are promising materials because they do not contain rare metals, are printable, crystallize near room temperature, are mechanically flexible, and can be designed at the molecular level [29]. Due to the weak van der Waals intermolecular interactions, printing organic semiconductors dissolved in organic solvents can easily form crystalline semiconductor films in air near room temperature. Their flexibility and designability make them suitable for a variety of emerging applications, including flexible/stretchable electronics and wearable biosensors.

Organic SGTs (OSGTs) were first demonstrated in numerical simulations in 2009 and 2013 [30, 31]. Experimental studies of OSGTs started in 2019 and showed intrinsic gains greater than 1000 for both p- and n-type OSGTs [18, 32–38]. Major studies are summarized in table 3. Most studies used staggered structures (top-gate bottom-contact or bottom-gate top-contact), with the exception of the bottom-gate bottom-contact (BGBC) structure in reference [32]. Source and drain electrodes were made of same materials in most cases, except for references [18, 33]. Several techniques have been used to improve OSGT characteristics, such as tuning SB heights, contact interlayers, controlling the thickness of semiconductor and dielectric layers, and field plates. SBs at source electrodes can be tuned by the ionization energy of organic semiconductors [33, 37], metal work functions [18, 33, 34], electrode surface treatments such as self-assembled monolayers (SAMs) [34, 35, 37], and interlayers such as a few nm thick Ga_2O_3 between metal and semiconductor layers [38]. Increasing the thickness of dielectric layers relative to semiconductor layers can reduce pinch-off drain voltages [18]. Field plates, sometimes referred to as field-relief structures, prevent leakage current through the SBs at the edge of source electrodes due to high lateral electric fields and significantly improve intrinsic gain (figures 4(a)–(c)) [35, 37]. OSGT-based common-source amplifiers were also demonstrated to exhibit their high gain of 700 with field plates (FP) (figure 4(d)), which enables the peak of the electric field to be dissipated away from the injecting edge of the source electrode.

Current and future challenges

There are few reports on the dynamic characteristics of OSGTs. Jiang *et al* reported that the gain-bandwidth products of their OSGT-based common-source amplifiers were in the range of 1 Hz–1 kHz [32]. Since the drain currents of OSGTs are generally small due to SBs and low carrier mobilities, increasing the bandwidth of OSGT-based amplifiers is challenging.

Variability is another important factor of OSGT-based integrated circuits. Since the currents in SGTs are limited by contacts, variability in channel lengths is less important than conventional organic FETs. However, the variability in contact characteristics can also be significantly large. The variabilities in threshold voltages of OSGTs are usually more than 0.1 V and result in input offset voltages in amplifiers.

It is also important to improve air stability, long-term stability, and thermal stability. The air stability of organic semiconductors has been significantly improved by increasing the electron affinities of n-type organic semiconductors. As a result, most OSGTs can be used in air without gas barrier layers. However, the long-term stability is not good enough, especially under gate bias. The gate bias stress usually causes the threshold voltage to shift by more than 0.1 V, and sometimes the transconductance changes as well. The upper temperature limit for organic semiconductors is typically 100 °C–200 °C. There is a trade-off between the thermal stability and solubility of organic semiconductors; rigid molecular structures usually improve thermal stability and reduce solubility.

Advances in science and technology to meet challenges

In general, integrated circuits must be designed for each purpose because there are many trade-offs among the performance characteristics of integrated circuits, such as gain, bandwidth, power consumption, and voltage range. Multi-objective optimizations of device structures and circuit designs are required to realize practical applications of OSGTs. Compact models for circuit simulation are required for optimizing circuit designs.

Variability and bias stress in threshold voltages must be minimized at the device level or compensated by differential techniques. Differential amplifiers compensate for device variability by using pairs of matched transistors. For example, common-centroid layout helps to reduce variability due to the gradients of fabrication and operation conditions.

Table 3. Summary of the experimental studies of organic SGTs.

Polarity	Materials	Intrinsic gain	Fab. Method	Notes	Year	References
P	Ag/C_8-BTBT	1100	inkjet	BGBC	2019	[32]
P	Pentacene/Al	—	evap.	—	2019	[33]
N	BPE-PTCDI/Au	—	evap.	—		
Both	PDBT-co-TT/Al	—	spincoat/evap.	—		
N	N2200/Au	—	spincoat/evap.	—		
P	Cr/PIFPA	—	evap./spincoat	—	2021	[34]
P	Cr,Cu,Ti,Al/DNTT	—	evap.	—	2021	[18]
N	Ag/N2200	>40	inkjet	field plate	2022	[35]
P	ITO/PDPP4T	160	-/spincoat	—	2023	[36]
P	Ag/PFBT/Ph-BTNT-C10	920	inkjet/dispenser	field plate	2023	[37]
N	PTCDI-C8/Ga_2O_3/EGaIn	86 200	evap./injection	oxide layer of EGaIn	2023	[38]

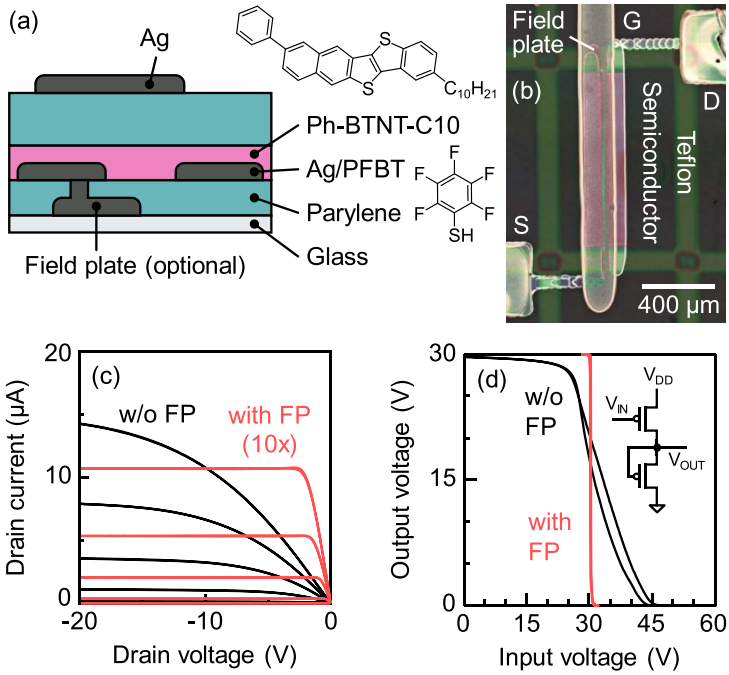

Figure 4. (a) Structure, (b) optical microscope image, and (c) output characteristics of OSGTs with and without field plates (FPs). (d) Voltage transfer characteristics of OSGT-based common-source amplifiers with and without FPs. [37] John Wiley & Sons. © 2023 The Authors. Advanced Electronic Materials published by Wiley-VCH GmbH.

There is considerable room for improvement in process optimization. This is because the printing process has a large number of conditional parameters, such as printing temperature, annealing temperature, solvents, additives, printing speed, ink concentration, and ink volume, and optimizing all of them is time-consuming and costly. Highly efficient experiments, including combinatorial experiments and Bayesian optimization, have the potential to greatly accelerate these studies.

The development of a new high-performance organic semiconductor material can be a breakthrough in this field because of the large degree of freedom in the molecular design of organic compounds. There are more than 1000 000 organic compounds in the Cambridge Crystallographic Database and the number is growing. New functionalities of organic semiconductors such as stretchability, self-healing, photosensitivity, chemical and biological sensitivity are also being studied.

Concluding remarks

Several p-type and n-type OSGTs and OSGT-based amplifiers have been demonstrated, and high gains in excess of 1000 or sometimes close to 100 000 have been reported. These performances indicate that OSGTs are promising devices for signal processing in flexible, printed, and wearable electronics. Several challenges remain, such as multi-objective optimization, compensation for device variability, and long-term stability. Advances in circuit design using compact models, sophisticated differential techniques, process optimization using high-efficiency experiments, and development of new organic semiconductor materials would address these challenges.

5. Analogue and neuromorphic contact controlled TFTs

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Status

SGTs provide low saturation voltage, low power operation and increased stability and uniformity compared to conventional TFTs. These advantages are particularly important for circuits involving readout of analogue sensors and neuromorphic applications [14]. The slower speed in SGTs, due to the extra capacitance at the gate, is usually less relevant for analogue sensors because their time scale is based on the sensor reading. The typically lower drive current of the SGT compared to a conventional TFT is advantageous here because low power dissipation in these circuits is a priority. SGTs are thus very suitable for readout circuits for analogue sensors but also very promising for classification circuits attached to these circuits, enabling smart embedded applications.

Recent innovations in analogue circuits that utilize SGTs have demonstrated how they can be used advantageously for sensor applications [14]. A compact circuit block of an amplifier using two SGTs has achieved the highest reported gain of 49 dB. The current mirror circuit also using two SGTs has a unique property allowing the control of temperature dependence. This demonstrates the potential of SGTs in lowering component count in certain circuits, which is highly desirable in thin-film technologies. Potential analogue circuit applications include temperature sensors, high gain amplifiers and pixel drivers.

Many of the advantages of SGTs, such as low power operation and greater tolerance to variability due to the flat and stable drain current, are promising for their use in neuromorphic circuits. In traditional MOSFET technologies, spiking neuron circuits are typically operated in the deep subthreshold to take advantage of the exponential dependence of V_g to achieve spiking action and to optimize energy consumption. In flexible technologies, however, using low cost and low temperature processes leads to much greater variability in device processing. SGTs thus may provide a work around for realizing neuromorphic circuits with low variability in flexible electronics.

Aside from conventional SGTs, a new contact-controlled structure has shown significant potential for neuromorphic applications. The multimodal transistor (MMT) [39], depicted in figure 5, uses separate connections to independently control the barrier at the source and the conductivity of the channel. While structurally similar to the RFET in sections 9 and 10 and other TFTs with auxiliary gates, the MMT utilizes the gate responsible for controlling the injection at the source as the main input to the device, which brings additional functionality in a compact layout footprint. Further refinements have led to the realization of floating gate devices, as possible synapses [39] and ReLU activation function demonstrations [40]. One particularly promising application is thus a sensor readout connected to a classification circuit for low power wearable health or environmental monitoring.

Current and future challenges

One of the challenges preventing circuit designers from using SGTs is the lack of compact models, which are necessarily for SPICE circuit simulations. Although an SGT has a similar structure to a thin film transistor (TFT), SGT models critically need to include the detailed physics at the source electrode in addition to the channel. As a result, a model cannot be adapted directly from typical TFT compact models [41]. On the other hand, a TCAD model [42] is too slow to remain competitive against alternative transistor designs and is very cumbersome for circuits. Designing a specialized SGT compact model that implements dominant effects is therefore an important challenge for implementing competitive analogue and neuromorphic circuits.

Although SGT effects have been thoroughly researched and documented, they are not yet completely quantified [19], which is why modeling remains an important obstacle. The SGT behavior is more complex than a typical TFT, as the SB creates new regimes of operation, which need to be included [18]. Finally, as we saw in sections 3 and 4, SGTs can be realized in many materials (organic, oxide, a-Si), resulting in different regimes and conduction mechanisms, as well as different trap interfaces at the source/semiconductor interface. A generic model may therefore not be able to capture all the physics for individual technologies.

For analogue electronics in general it is important to reduce the temperature difference between essential transistors to minimize non-ideal behaviors. To accomplish this, a rigorous layout design is required. This is especially relevant for SGTs, because their behavior can vary widely with temperature due to the SB [43]. A requirement for robust models is therefore that it can accurately account for temperature dependencies.

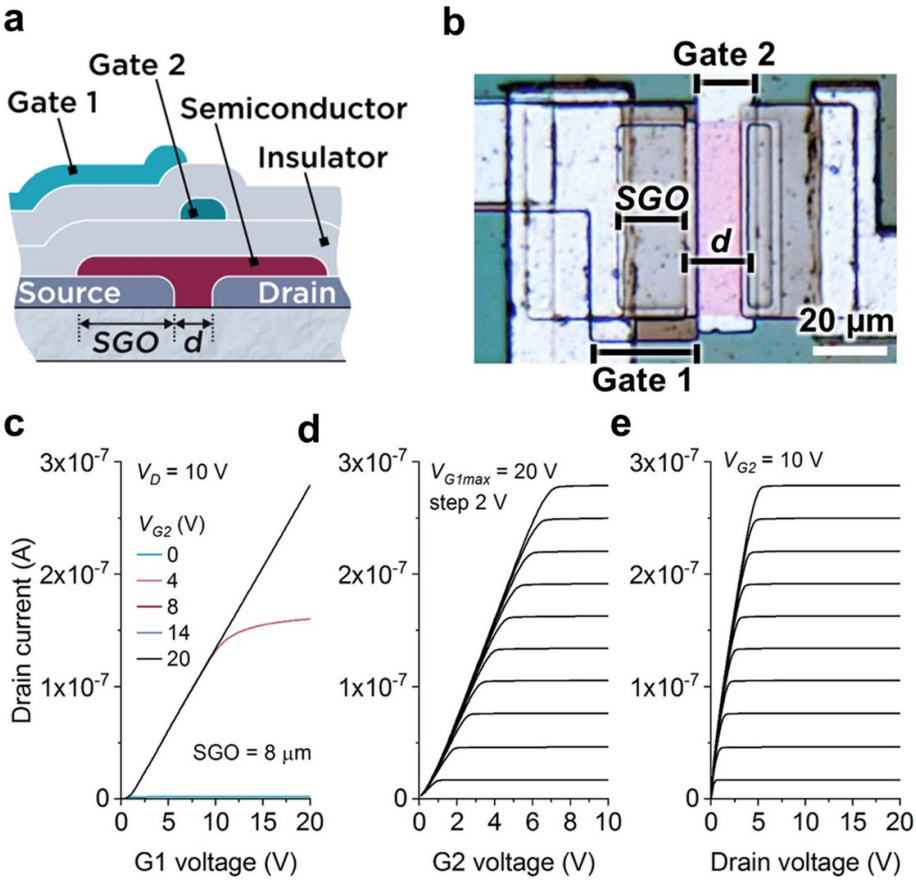

Figure 5. Depiction of the multimodal transistor. (a): cross section of a device, (b) optical micrograph of MMT realized in microcrystalline silicon, (c) TCAD simulations showing the I_d vs V_{g1s} characteristics where G2 allows or blocks the current flow without, (d) simulated I_d vs V_{g2s} characteristics, (e) I_d vs V_{ds} for different V_{G2}, demonstrating low voltage saturation and high output impedance. Reproduced from [40], with permission from Springer Nature.

Another challenge is optimizing the sub-threshold behavior, especially if neuromorphic circuits are going to be realized in this regime. In general, the sub-threshold has not been thoroughly investigated in either typical TFTs or SGTs. Future applications would greatly benefit from detailed investigations both in terms of modeling and physical realizations in the sub-threshold.

Advances in science and technology to meet challenges

As we have seen in the status section, simple circuits with two transistors have been demonstrated to prove that analog and neuromorphic circuits are viable and promising in SGT implementations [1]. While two transistor circuits can be and have been modeled in TCAD, implementing more complex circuits would be a significant computational bottleneck [42].

There have been recent developments in compact modeling of SGTs. First, an empirical compact model [20] has been developed, as shown in figure 6. It was instrumental in the analysis of the dominant effects present and the proportion to which they affect the behavior of the device. This led to the development of the first SGT physical compact model, which can be used to represent an SGT in SPICE simulations of DC circuits. It now allows circuit designers to use SGTs in common operation conditions, as only the most impactful dominant effects where implemented. The physical compact model needs to be developed further for use in broader applications. Additionally, for the SGT to be used by analogue circuit designers, a charge based compact model needs to be developed to allow for accurate implementation in AC circuits. Finally, designing compact models the fit different technologies can be challenging, so technology specific SGT compact model that are likely to be needed.

Compact modeling will allow the consideration of how design can meet the two other challenges facing this technology: variations in temperature and developing circuits in the sub-threshold regime. Using a compact model with implemented temperature dependence may provide insight into how the device might behave for a given range of temperatures, to ensure that the design is fit for purpose. It will also enable the design of optimized SGT circuits. Similarly, to find the best neuromorphic implementations for SGTs,

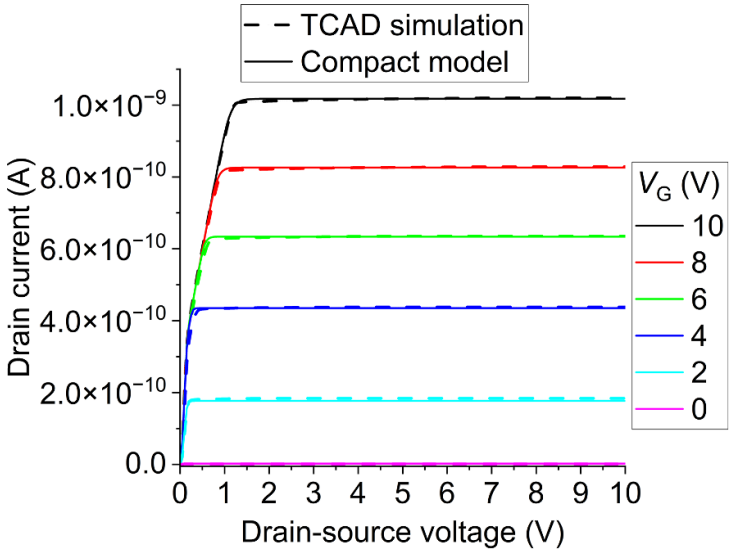

Figure 6. Output characteristics of the SGT physical compact model. The model was verified to be reasonably accurate using TCAD data. © (2019) IEEE. Reprinted, with permission, from [42].

compact modeling would allow testing of their implementations prior to realization as well as Monte Carlo simulations to test circuit robustness.

Ideally the modeling of the SGTs will be extended to include an AC compact model, however, this adds a unique set of challenges. In particular, the technology in which the device is developed is likely to exhibit different characteristics that would strongly impact such a model. Significant time would need to be invested to tune such parameters. The most important of these involve the charge trapping and dependence on environmental conditions such as light, moisture and temperature.

Concluding remarks

Contact controlled transistors and SGTs have demonstrated great promise for analogue and neuromorphic circuits, based on the characteristics of single or a couple of transistors. The most promising applications are likely to be embedded classifications for health monitoring or environmental sensor readout. The advantage of SGTs compared to CMOS is their comparative advantage in to integrating with flexible materials and substrates. Future potential circuits will be possible with the development of compact models that would enable their simulation and eventual fabrication. Similarly, possible industrial applications will become more viable with high-quality models for design optimization [20].

6. Ferroelectric SBFET as artificial synapses

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Status

Neuromorphic computing, inspired by the architecture of the human brain, offers a promising solution to overcome the von Neumann bottleneck, positioning itself as the forefront in advanced computing for big data processing. Among the various artificial neuron devices, ferroelectric FETs (FeFETs) stand out as a compelling candidate, boasting CMOS compatibility, scalability, high endurance, excellent performance, and high energy efficiency, along with exhibiting various synaptic behaviors akin to the human brain [44, 45]. The FeFET, structured similarly to a MOSFET, utilizes CMOS-compatible HfO_2-based ferroelectrics as the gate oxide. The polarization switching of the ferroelectric layer induces a shift in the threshold voltage (V_{TH}), enabling its use as non-volatile memory. To preserve the ferroelectric properties of an HfO_2-based ferroelectric film, it is imperative to avoid high-temperature annealing for source/drain implantation activation following the deposition of the HfO_2-based ferroelectric. In light of this consideration, the ferroelectric Schottky barrier MOSFET (FE-SBFET) structure, as depicted in figure 7, emerges as highly appealing. This structure offers the advantage of relatively low-temperature processing, eliminating the need for both ion implantation and thermal activation of source/drain contacts at elevated temperatures. On the other hand, the more gradual modulation of the Schottky tunneling through the ferroelectric polarization in the FE-SBFET can increase the number of analog states, crucial for achieving high learning accuracy. Artificial synapses with FE-SBFETs on SOI have been reported [46–48], where epitaxial $NiSi_2$ at source/drain provides atomic flat interfaces to silicon, highly recommended for a uniform SB contact with minimal variations.

The excitatory and inhibitory neuron behavior can be easily imitated by the ambipolar switching of FE-SBFETs, a characteristic property of SBFETs. This can be achieved by selecting holes/electrons as the excitatory/inhibitory neurotransmitters. The use of an SOI substrate allows for an additional modulatory neuron by the back-gate to further adjust the synaptic weights. A 4-terminal synapse can be realized by using dual gates to individually control the source and drain SBs. In this case, modulation is much more efficient than using the back-gate, as illustrated in figures 7(d) and (f). These devices with $Hf_{0.5}Zr_{0.5}O_2$ (HZO) as the ferroelectric layer showed good synaptic properties with 50 analog states (figures 7(e) and (f)), good linearity long-term potentiation/depression (LTP/LTD) linearity and symmetry, very small circle-to-circle variations, low power consumption and high speed [46].

Current and future challenges

To create a synapse array for neuromorphic computing, precise control of synaptic weight through the domain polarization of the FeFET is crucial, along with high endurance and scalability. Nevertheless, challenges are present for both FeFET and FE-SBFET. The reported FE-SBFETs demonstrated a short retention time at low voltages, similar to FeFETs. The retention duration is influenced by the polarization state of the ferroelectric layer, with longer retention achievable at higher electric fields surpassing the coercive field. However, the use of higher voltage may increase power consumption and reduce the endurance. The retention time also depends on the ferroelectricity of the material, suggesting a need for improvement in this aspect. Application-specific considerations dictate the required retention time, with hardware applications necessitating an extended retention time, typically on the order of hours [49]. Conversely, for online learning, the retention time is not a critical factor.

Interface traps in FeFETs significantly impact device performance. The FeFET threshold voltage shift caused by traps in the ferroelectric layer opposes that caused by ferroelectric domain polarization. Consequently, the presence of interface traps can result in a smaller memory window for both FeFETs and FE-SBFETs, degrading the controllability of synaptic weight by domain polarization. Moreover, interface traps degrade memory endurance and the reliability, posing a significant challenge for HfO_2-based ferroelectric devices. Interface engineering to reduce interface states is essential for both FeFETs and FE-SBFETs.

Scalability presents a significant challenge for FE-SBFETs, akin to FeFETs. The HfO_2-based ferroelectric material faces difficulties in scaling in both thickness and area. Thinning the layer weakens ferroelectricity, and causes higher leakage currents that compromise device endurance. The domain size and distribution also restrict scaling of the device channel length, resulting in significant device-to-device variation as the gate length decreases. In FE-SBFETs, the SB at the source and drain overlaps in the middle of the channel [50], imposing an additional limitation on scaling. Addressing this issue requires lower SB source/drain contacts.

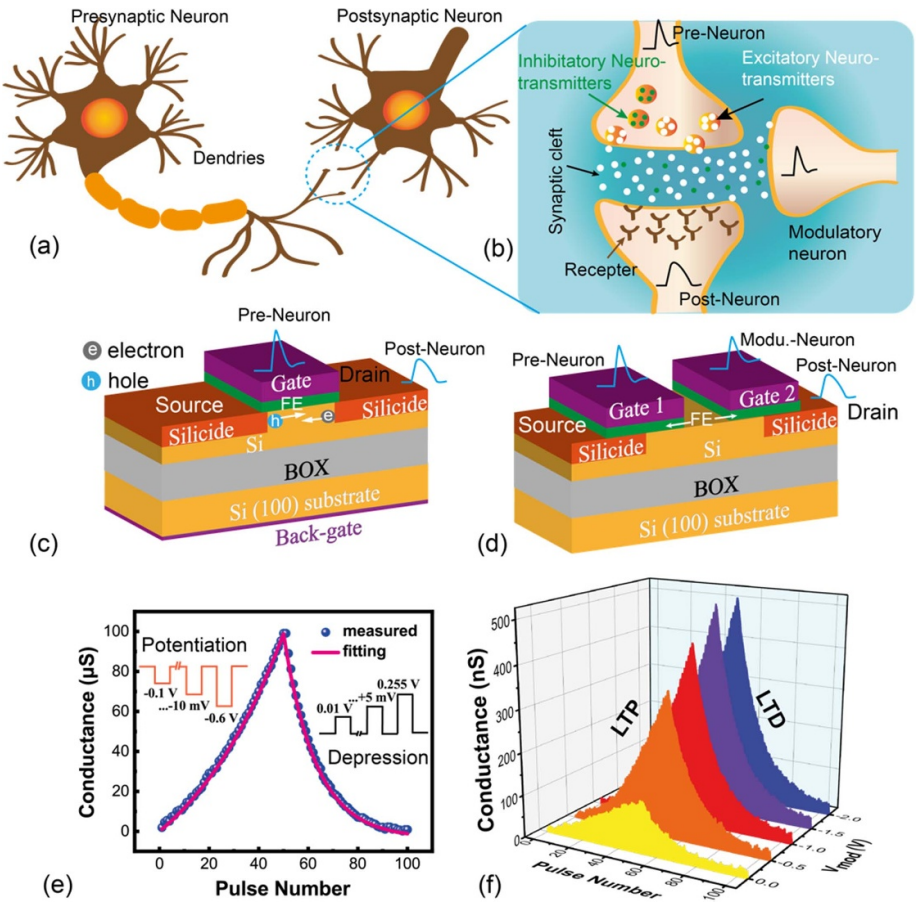

Figure 7. (a) illustration of biological neurons, and (b) a synapse connecting a pre-synaptic neuron and a post-synaptic neuron, with weight modulation by the modulatory neuron. (c) structure of a single gate FE-SBFET, and (d) a dual gate FE-SBFET for artificial synapses, where both are designed to utilize electrons/holes can be used as excitatory or inhibitory neurotransmitters. (e) LTP/LTD characteristics of a single gate FE-SBFET with HZO as ferroelectric layer, showing 50 states with good linearity and symmetry, influenced by the input pulse configurations shown in the figure. (f) LTP/LTD characteristics of a dual-gate FE-SBFET artificial synapse, showcasing the modulation brought by the second gate as illustrated in (d). (b)–(f) [46] John Wiley & Sons. © 2022 The Authors. Advanced Electronic Materials published by Wiley-VCH GmbH.

Advances in science and technology to meet challenges

To address the challenges mentioned above, focused research is required on materials, device structures, and their fabrication and integration processes. Recent advancements in ferroelectric layer research aim to enhance the HfO_2 ferroelectric material quality and the performance of FE-SBFETs. One promising avenue involves the utilization of superlattice ferroelectric structures [8, 9]. By implementing superlattices, researchers seek to optimize the ferroelectric properties, such as polarization switching, retention characteristics, layer thickness scaling, endurance and reliability. Investigating and implementing novel superlattice configurations in the ferroelectric layer represent a key frontier in pushing the capabilities of FE-SBFETs. Addressing interface traps is another critical aspect of optimizing FE-SBFET performance. Innovations in interface engineering, including the reduction of the HfO_2 ferroelectric interfacial layer thickness, the use of very thin high-k materials as the interfacial layer, and other passivation technologies have substantially improved device endurance and reliability.

In terms of device structure, Fully Depleted Silicon-On-Insulator (FDSOI) technology enhances the symmetrical ambipolarity of FE-SBFETs, enabling the fabrication of devices with varied synaptic behaviors. Additionally, Gate-All-Around (GAA) nanowire technology contributes to increased gate control and fewer interface traps, further bolstering FE-SBFET performance. Lower the SB height can further enhance the scalability of FE-SBFETs. This could be achieved by using dopant segregation to lower the effective SBH.

The integration of two-dimensional (2D) materials into the channel is a groundbreaking step, utilizing their unique electronic properties to minimize interface traps and augment device response. This multidisciplinary strategy, encompassing advanced materials and engineering techniques, represents a comprehensive approach to addressing the challenges facing FE-SBFETs, particularly in the realm of neuromorphic computing. Such synergistic advancements in ferroelectric layers and interface optimization are key to unlocking the full potential of FE-SBFETs.

Other semiconductor materials, such as oxide semiconductors, Ge, and SiGeSn, offer unique properties. Their integration with ferroelectric materials for neuromorphic computing applications presents also an interesting area of study.

Concluding remarks

In conclusion, FE-SBFETs demonstrate significant potential as artificial synapses, marking a promising path forward in the field of neuromorphic computing. The devices described here naturally allow for integration with analog RFET SB devices described in section 10 because the processing challenges faced are similar. FE-SBFETs realized using organic materials would naturally integrate with the SGTs described in the previous section. Their capacity to replicate key synaptic functions of the human brain, including short-term and long-term plasticity, as well as excitatory and inhibitory neural behavior due to their ambipolar nature, positions them as essential components for creating more efficient, brain-like computing systems. The ability of ferroelectric SBFET artificial to integrate different technologies and reproduce a wide range of biomimetic functionality make them most promising for complex classification tasks or reconfigurable systems which can take advantage of this versatility. However, the field still demands extensive research in material science, innovative device concepts, device engineering, and integration techniques to enhance device performance further. Additionally, the development of artificial neurons based on FE-SBFETs, which has not yet been reported, represents a critical area for future exploration to fully harness the capabilities of FE-SBFETs in neuromorphic computing applications.

7. Cryogenic Schottky-barrier field effect transistors

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Status

Spin qubits realized in ^{28}Si have recently gained an increasing attention due to their integration with the highly mature CMOS fabrication technology. This combination allows for the implementation of qubits in a nuclear-spin-free semiconductor, which offers relatively long coherence times. However, the set-up, coupling and manipulation of the qubits requires addressing gate electrodes. Given the need for a substantial number of physical qubits to realize error correction in quantum computing systems, complex and sophisticated classical control electronics are required. This system must function efficiently at cryogenic temperatures and ultralow power levels. A significant challenge at these temperatures is the doping in conventional nanoscale MOSFETs, as highlighted in recent studies [8]. Issues like dopant deactivation in source and drain contacts are exacerbated by dielectric mismatch and quantum confinement, impacting device performance. Additionally, while conventional MOSFET theory suggests that cryogenic operation should allow for extremely low supply voltages, real devices often exhibit suboptimal switching behavior. This is primarily due to band-tails at the conduction/valence band edges, leading to a phenomenon known as subthreshold swing (SS) saturation in cryogenic MOSFETs [51]. An emerging solution to these challenges lies in the use of metal source/drain contacts. These contacts show promise in addressing the aforementioned issues, offering a potential pathway to more effective integration of spin qubits and classical control electronics in cryogenic environments.

Current and future challenges

Metals obviously avoid any issues related to dopants and provide a high conductivity. The high Schottky-barrier on the order of half the band gap that builds-up at the metal-silicon contacts is certainly too high for proper cryogenic functionality. However, utilizing dopant segregation after ion implantation into the silicide allows a strong reduction of the effective SB height (note that in this case deactivation of dopants is irrelevant) [52]. Interestingly, a small SB can be advantageous for cryogenic operation. One of the reasons is that cryogenic MOSFETs are less scalable compared to their room-temperature counterparts [8, 53]. To ensure the required low operational voltage, the potential barrier that impedes current flow in the off-state of the device is only a few milli-electron volts in height. This results in a much larger direct source-to-drain tunneling effect at cryogenic temperatures compared to room temperature, where the barrier heights are typically about half the bandgap. In ultrathin-body devices, potential variations (such as the p-n junctions and the potential distribution of the Schottky-barriers) have a spatial extend of the screening length λ (see figure 8(a)). For conventional cryogenic MOSFETs, the effective channel length in the off-state is then approximately $L \approx 2\lambda$ where L is the metallurgical channel length between the source and drain electrodes. In SB-FETs, on the other hand, the full length L blocks the off-state current and thus, cryogenic SB-FETs can be scaled to smaller dimensions compared to conventional MOSFETs. Moreover, the potential distribution of the Schottky-barrier acts as a filter preventing current flow through the band-tails thus holding promise to yield cryogenic transistors that switch with steeper slope compared to conventional MOSFETs; this scenario is schematically shown in figure 8(b) [52, 54]. The drawback of the presence of a Schottky-barrier is certainly the reduced on-state performance that is to be expected, particularly at cryogenic temperatures. As a result, an optimization of the Schottky-barrier height and the potential distribution of the Schottky-barrier needs to be found in order to obtain cryogenic transistors with steepest switching but sufficient on-state performance as illustrated in figure 8(c).

Advances in science and technology to meet challenges

Figure 9(a) shows a schematic together with a transmission electron microscopy cross-section of gate-all-around nanowire FET with $NiSi_2$ source/drain electrodes, HfO_2 gate dielectric and a TiN metal gate [55]. Ion-implantation into the silicide with subsequent annealing in order to facilitate dopant segregation at the silicide-silicon interface is used to manipulate the Schottky-barrier height at source and drain [52]. Transfer characteristics of this device are measured at cryogenic temperatures (5.5 K) and the inverse subthreshold slope SS is extracted and plotted as a function of $\log(I_d)$ (see figure 9(b)). The device shows an almost ideal behavior with a record steep SS at 5.5 K. Moreover, the inverse subthreshold does not show saturation when studied as a function of temperature. As a result, even smaller SS values at lower temperatures can be expected.

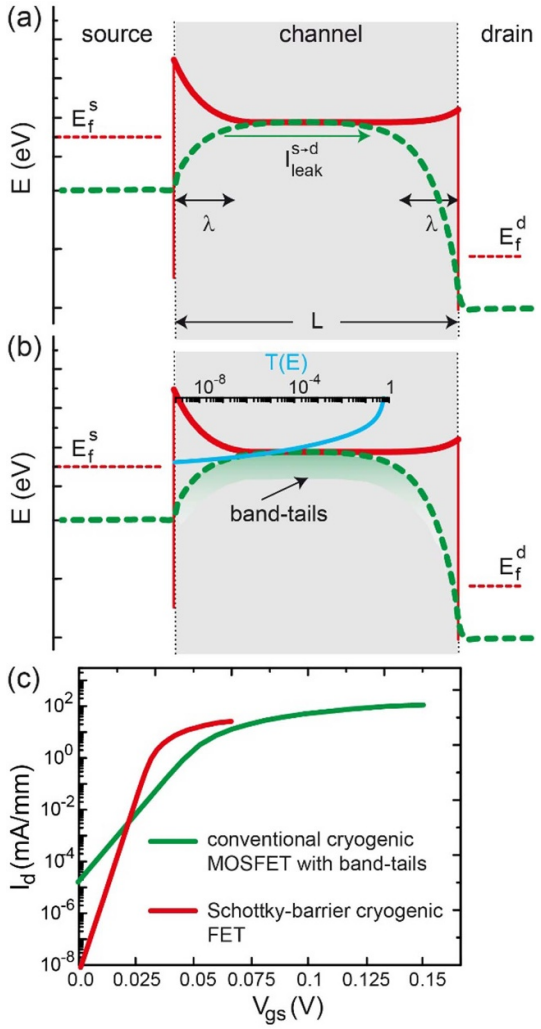

Figure 8. (a) Conduction band profile in a conventional MOSFET (green) and a SB-FET (red). A lower leakage due to direct source-to-drain tunneling $I_{leak}^{s\text{-}d}$ is obtained in the latter case. (b) Band-tails deteriorate the switching in conventional cryogenic MOSFETs. The strong dependence of the tunneling probability $T(E)$ in SB-FETs suppresses carrier injection into band-tails. (c) Optimized SB-FETs enable better switching and in the reduced V_{ds}-range an improved on-state performance.

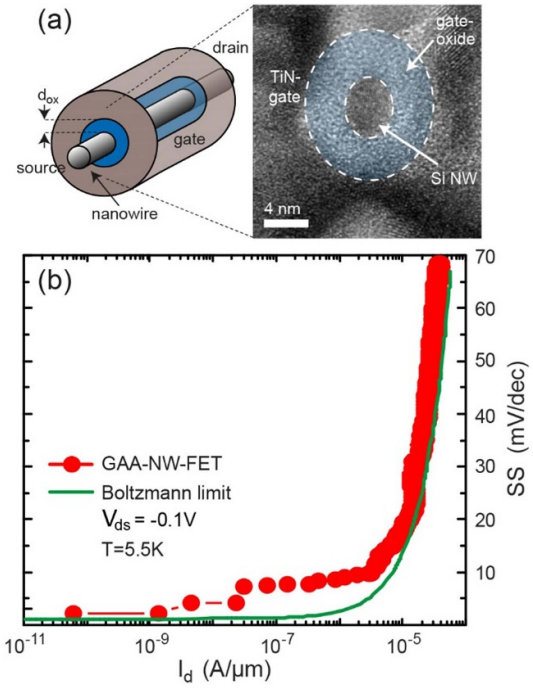

Figure 9. (a) Schematic (left) and transmission electron microscopy cross-section of a GAA nanowire FET with $NiSi_2$ source/drain contacts. (b) Subthreshold swing as a function of I_d of the device shown in (a) at 5.5 K. © (2023) IEEE. Reprinted, with permission, from [55].

Concluding remarks

Cryogenic SB-FETs may be a viable solution for classical electronics operating at very low temperatures. They are particularly interesting for support circuits for low temperature quantum computing applications. Important assets are their improved scalability and the filter properties of the Schottky-barrier that allow reducing the impact of band-tails. The optimum Schottky-barrier certainly depends on the amount of band-tails, which in turn depends on charged defects, the treatment of the MOS interface etc [7, 8]. As a result, with appropriate engineering of the Schottky-barrier together with a reduction of band-tails, optimum device functionality in terms of steepest switching and high on-state performance of cryogenic electronics may become reality.

8. SBMOFSETs for Josephson FETs

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Status

The increasing demand for quantum information processing has set a particular focus on SBFETs with highly transparent superconducting metal- or silicide-semiconductor junctions, also known as Josephson junctions. Schematically shown in figure 10(a), these structures are the key components of Josephson FETs (JoFETs). Importantly, typical FET structural parameters such as the device footprint and electrical properties such as on/off-ratios, subthreshold-swings and threshold voltages are mostly irrelevant for JoFETs. Instead, when operated at cryogenic temperatures i.e. below the superconducting transition temperature of the metallic leads, electrostatic gating in JoFETs not only modulates the charge carrier density within the semiconductor but can also modify the proximity induced critical current of the junction i.e. the exchange of superconducting cooper pairs from source to drain through the semiconductor channel (see figure 10(b)). Interestingly, JoFETs resemble a LC resonator with quantized excitations, exhibiting a dissipationless nonlinear inductance where the lowest two energy levels can be isolated to form a qubit. Historically, III–V semiconductors such as InAs and InSb have been the material of choice, which is inherently related to their high electron mobility and low effective mass. With respect to group IV semiconductors, first JoFETs were based on highly p-doped SBFETs with Pb contacts [56] or by integrating superconducting Nb layers atop highly doped source/drain regions [57]. Based on these findings, the idea of using in-diffused superconducting silicides or even single-elementary metal source/drain regions began to emerge. Such monolithic contacts would simultaneously reduce the gate-field screening effect of the leads and therefore would enable better electrostatic gating capabilities. Moreover, gate overlapping source/drain contacts are possible that provide significant junction transparencies. If in a further step a two-gate architecture, structurally similar to a RFET, would be used, even a decoupling i.e. individual control over the interface transparency and the charge carrier concentration of the channel would be possible. Notably, as the transport in SBFETs is occurring further away from the semiconductor-oxide interface compared to MOSFETs, JoFETs based on SBFFETs are predicted to have significantly lower surface scattering in the channel [3]. Consequently, a higher mean-free path of the channel is expected, which contributes to a higher degree of ballistic charge carriers compared to MOSFETs with the same channel length.

Current and future challenges

Current challenges involve integrating JoFETs as fundamental building blocks in superconducting quantum interference devices (SQUIDs) for superconducting qubit systems. SQUIDs consist of two JoFETs in parallel and are capable of sensing small variations in external magnetic fields by quantum interference effects within the structure [58]. Moreover, by superimposing independent gate electrodes to each QD, an external quantum control can adjust the SQUID properties, correcting fabrication inhomogenities. The SQUID circuit topology might allow for the exploration of memories based on the single magnetic flux quantum, e.g., when coupling two SQUID structures in respective storage and readout loops. Alternatively, the concept of gate-tunable transmons with reduced noise and cross-talk has recently emerged based on InAs nanowires to replace the SQUID loops. For both concepts, highly transparent interfaces between superconductors and semiconductors are among the key challenges of JoFETs. Especially, overcoming the SB requires the fabrication of high-quality electrical contacts with abrupt, impurity- and oxide-free interfaces to semiconducting channels. With respect to III–V semiconductors, this can be achieved i.e. by *in situ* MBE growth of crystalline Al or Nb shells onto bottom-up synthetized InAs and InSb nanowires [59]. Using this technique sub-gap states could be suppressed and highly transparent Al contacts with Fermi level pinning to the conduction band were realized. Intensive research has focused on realizing topological superconductivity and Majorana zero-modes with InAs nanowires with superconducting half-shells [60].

Recently, Ge nanostructures have attracted a considerable attention for quantum information applications [62]. This is mainly attributed to a combination of a comparatively large excitonic Bohr radius of 24.3 nm vs. 4.9 nm for Si, allowing for strong quantum confinement at relaxed dimensions. Ge further features low effective masses for electrons and holes allowing for a high transmissibility when used as a tunneling barrier. Importantly, Ge also possess a strong and gate-tunable spin–orbit coupling of holes, especially when a one-dimensional hole-gas is observed in vertical SiGe-Ge-SiGe stacks, as depicted in figure 11. Last, but not least, SiGe/Ge shows an excellent compatibility with Si technology and established CMOS fabrication schemes.

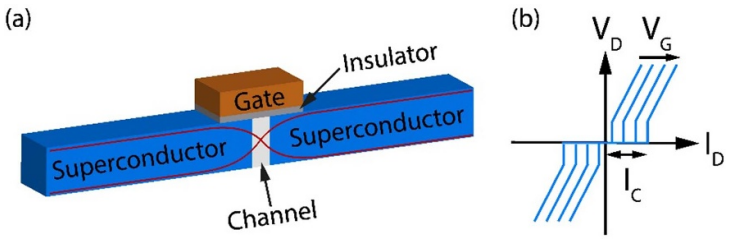

Figure 10. (a) Schematic illustration of a JoFET with source/drain overlapping gate-electrode for better electric control of the junction and the channel. The red curves schematically represent the overlapping wave-functions enabling proximity induced superconductivity in the channel. (b) Schematic illustration of the *V*/*I* characteristic of a JoFET showing a gate-tunable supercurrent.

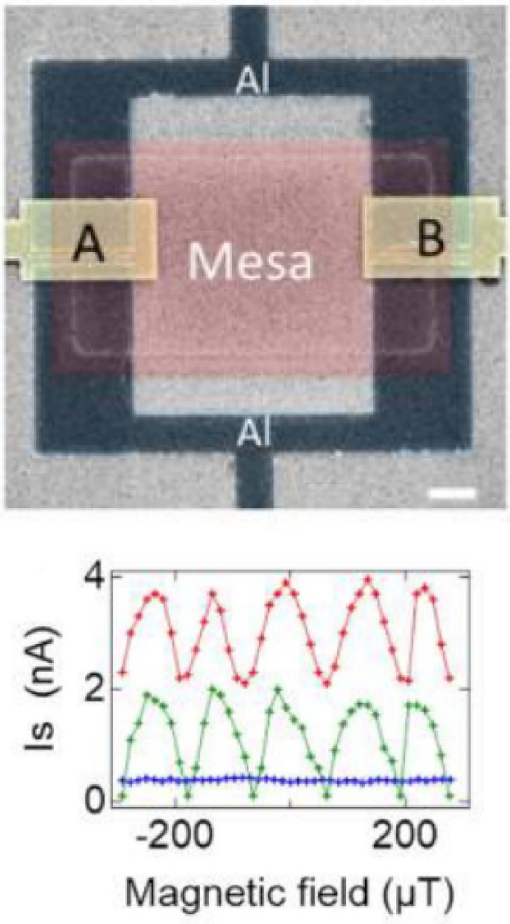

Figure 11. False-color SEM image of a SiGe/Ge/SiGe quantum well based SQUID and respective switching current vs. magnetic field. (a) Reprinted with permission from [58]. Copyright (2019) American Chemical Society. (b) Reproduced from [61] with permission from the Royal Society of Chemistry.

Advances in science and technology to meet challenges

Related to their strong spin–orbit interaction and electrically tunable g-factors, hole gases in vertical and radial Ge/Si heterostructures are interesting platforms for hybrid superconductor-semiconductor devices. In this regard, the highly transparent Al-Ge interfaces formed by a thermally induced exchange reaction show a high uniformity and an abruptness down to the atomic level, due to the epitaxial relation between the Al and Ge regions [61]. These junctions constitute high-quality Schottky contacts with a small barrier for holes, which is an important prerequisite towards hybrid Ge-based quantum technologies. Even more recently, a thermally-activated solid phase reaction between Pt and a vertical SiGe-Ge-SiGe stack resulted in germanosilicide contacts that showed a near-unity transparency (see figure 12(a)) [63]. Several interesting findings have arose using this type of contacts, such as the observation of a hard superconducting gap in a Ge/Si core/shell nanowire Josephson transistor up to in-plane magnetic fields of 250 mT, which might pave

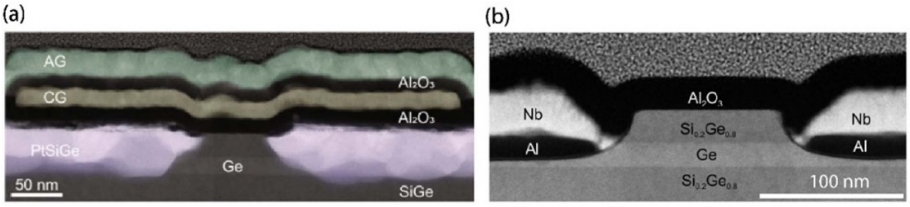

Figure 12. TEM cuts showing Ge based JoFETs with (a) PtSiGe germanosilicide contacts. Reproduced from [63], with permission from Springer Nature. And (b) stacked Al-Nb contacts for enhanced proximity-induced superconductivity in Ge. Reprinted figure with permission from [65], Copyright (2021) by the American Physical Society.

the way towards creating and detecting Majorana-zero modes in this system [64]. The work therefore constitutes an important step towards the co-integration of spin, super-conducting, and topological systems for scalable quantum information processing based on a CMOS compatible Si/Ge platform. Moreover, stacking Nb atop Al contacts, highly transparent and lowly-disordered contacts capable of withstanding magnetic fields beyond 1.8 T have been shown. For this work, the Al contacts interfacing the vertical SiGe/Ge/SiGe stack were deposited directly after the epitaxial growth of the semiconducting channel within the same MBE chamber, which ensures oxide-free metal-semiconductor interfaces (see figure 12(b)). This might catalyze the integration of pin qubits and proximity-induced superconductivity on the same chip [65].

Concluding remarks

JoFETs form the basis of many quantum electronic devices such as parametric amplifiers, superconducting qubits, microwave and magnetic field detectors and those realized here would have a particular advantage of facile integration with more traditional CMOS electronics. SB devices with source/drain contacts that become superconducting at low temperatures are promising for the realization of JoFETs. In silicon devices, the advantages are that the use of silicides can provide greater control over the channel length and because the transport can be realized below the semiconductor surface. These promises, however, have not yet been able to compensate for a lack of transparency of the contacts. Realizations in III–V semiconductors can achieve more controlled interfaces and metal-Ge heterostructures enable stronger quantum confinement and strong and gate-tunable spin–orbit coupling. Importantly, metal-Ge heterostructures are the easiest to integrate into CMOS technologies and may therefore be the most promising.

9. Operational principles of reconfigurable field effect transistors

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Status

Reconfigurable field-effect transistors are SB devices that are equipped with two or more independent gate electrodes. The additional, so-called program gates allow a configuration of the device functionality at run-time while the remaining control gate is used to switch the transistors conductance. For instance, with dual gates (DG) an operation as n-type and p-type transistor can be adjusted; if a third gate electrode is added, i.e. triple gated (TG), the implementation of n-type, p-type as well as band-to-band tunnel transistors (TFET), impact ionization and positive feedback transistors becomes feasible [66]. The latter three cases are particularly attractive for mobile applications since these allow high performance circuits (n-type and p-type RFET operation) to be adjusted to low power operation whenever necessary or applicable. Additionally, employing Ge rich-Si_xGe_{1-x} and Ge channels negative differential resistance RFETs in n-type can be realized in both DG and TG geometries. Figure 13 shows the DG and TG geometries along with the most common operations for p- and n-type dominated charge transport as depicted with schematic band diagrams. Here, the polarity is set by blocking the unintended charge carrier type at the drain Schottky junctions through band bending upon application of the program gate voltage (V_{PG}). In contrast, the junctions are more transparent for the injection of the intended charge carrier type by a combination of thermal field emission (TFE) and thermionic emission (TE). Conductance across the channel can be tuned directly at the injecting SB by TFE and TE for DG-RFETs and by TE within the channel for TG RFETs. Because adding gate electrodes to the individual devices increases the complexity of each transistor an optimization of device operation with the least number of gate electrodes is required. As depicted in figure 14, DG-RFETs can be operated either in the program-gate-at-source (PGAS) or program-gate-at-drain (PGAD) configuration [67]. While PGAS leads to a better switching device, PGAD facilitates lower off-state leakage and a reduction of the sub-linearity of the output characteristics. Adding a third gate allows combining steep switching with low off-state leakage.

Current and future challenges

In any case the sub-linear behavior typical of Schottky-barrier devices will be present due to the carrier injection through the SB at source. Moreover, the on-state performance is ultimately limited by tunneling of carriers through the source-side Schottky-barrier. As a result, further optimizations of RFETs employing nanostructure consisting of, e.g. graded lateral heterostructures that exhibit a small band gap material in order to guarantee a high carrier injection with symmetric n- and p-type operation while yielding low off-state leakage is necessary. Alternatively, novel gate-tunable source contacts may be required to improve the current drive capability of RFETs and avoid the sub-linear small bias behavior. Furthermore, the implementation of RFETs that enable a low power band-to-band tunneling operation mode require carefully designed fabrication process flows in order to realize single digit nanometer separations between program and control gates, both featuring a gate dielectric with ultrathin effective oxide thicknesses in order to optimize TFET performance. If all these optimizations can be realized and implemented, future RFETs will enable circuits with increased functionality combined with high-performance or low power operating modes.

Advances in science and technology to meet challenges

For digital applications, the reduction of power consumption as well as the enhancement of switching speed need to be improved in RFETs. Switching speed mainly depends on the drain drive current of the device, which is limited by the injection of charge carriers through the Schottky junctions. The main current contribution in the on-state is thermal field emission, which increases with smaller barrier heights, barrier widths and effective tunneling masses [69]. Compared to the first established RFET junctions composed of NiS_xi_{1-x}/Si [68, 70, 71], Ni_xGe_{1-x}/Ge [72] and Al/Ge based RFETs [73] have been explored, having the benefit of a smaller band gap and smaller effective masses in Ge. Nevertheless, Ni_xGe_{1-x} phases are difficult to stabilize and Al junctions pin close to the valence band edge of Ge. Recent advances in Si_xGe_{1-x} [74] layers on silicon on insulator lead to the formation of Al/thin-Si/Si_xGe_{1-x} and even Al/thin-Si/Ge junctions allowing for Fermi level pinning that provides balanced barrier heights between electrons and holes and symmetric on currents as required for symmetric RFET operation.

To fully mitigate the negative effects of low drain currents given by the limited injection of charge carriers through Schottky junctions, pinning-free junctions can be introduced at the injecting electrodes, as shown for SBFETs in [67] e.g. by integrating an ultrathin Si_3N_4 interlayer between the metal and the Si channel.

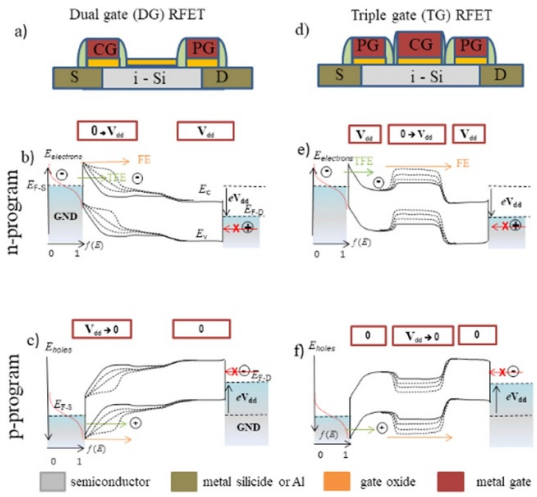

Figure 13. RFET realizations with dual (DG) and triple (TG) independent gate geometries (a), (d). Corresponding schematic band diagram for n- and p-type conduction. Reproduced from [66]. © IOP Publishing Ltd. All rights reserved.

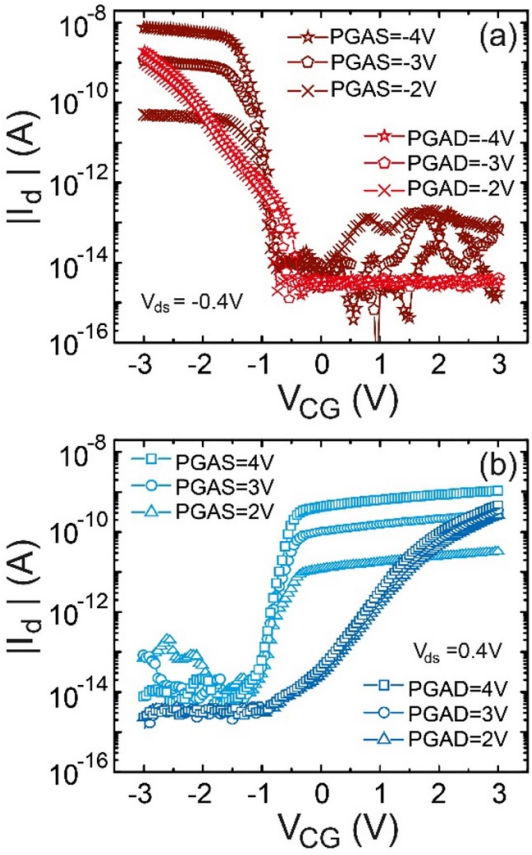

Figure 14. Transfer characteristics of the PGAD and PGAS programming modes for an RFET for (a) n-type configuration and (b) p-type configuration. © (2021) IEEE. Reprinted, with permission, from [68].

Concluding remarks

The main benefit of RFETs for digital applications is the ability to alter their functionality post-fabrication, which can reduce overall chip area and enable improved security. The main challenges are improving the sub-linear behavior and the more complex processing. Improvements in modeling and the development of industrial foundries would provide great benefits for future development.

10. Analog circuit design with reconfigurable field effect transistors

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Status

RFETs are innovative SB devices that can be dynamically reconfigured between n-type, p-type, or ambipolar mode. RFETs typically utilize an undoped channel and thus can be operated to change their conduction properties post-fabrication by electrostatically controlling the carrier transport via a geometry with multiple independent gates [75]. While RFETs with adjustable n- and p-type functions have been heavily discussed for digital circuit design, the exploitation of their analog properties is rather under-explored so far. This is mainly reasoned by the fact that classical high-frequency analog circuit design is often dictated by performance figures of merits, such as transconductance efficiency (*gm/Id*), transit frequency (*gm/Cgs*) and intrinsic gain (*gm/gds*). Relying on tunneling injection through a SB limits both saturation current $I_{d,sat}$, and transconductance g_m. However, apart from peak performances, RFETs have a lot to offer to analog designers. First of all, all RFETs are ambipolar transistors at heart. The perfect parabolic shape of the ambipolar transfer characteristic can be exploited to achieve an integrated frequency doubler without the need for inductive elements [76]. When the devices are programmed, blocking the carrier injection directly at the junction enables very stable, ultra-low leakage off-states, leading to a high on/off ratio. Relying on nominally undoped channels and a carrier transport, which is rather oriented to the bulk than to the interface of the nanoscale channel, promise a higher resistance against 1/f noise [77]. Also, it has been demonstrated that a subthreshold swing well below the thermal limit of 60 mV dec^{-1} at room temperature can be achieved in RFETs by inducing a self-limiting avalanche effect with a positive feedback loop [78]. All these features make RFETs attractive for analog circuit applications in the low-frequency domain, such as bio-sensing, brain–computer interfaces, or artificial neuronal networks. In addition, it should be considered that analog circuit design is much less formal than digital design, leaving a higher degree of freedom to the designer to find a customized solution. This is where the extended functionality of RFETs based on transport through SBs has the potential to really shine, as the individually accessible program gates provide an extra degree of design freedom.

Current and future challenges

To date the exploitation of RFETs for analog circuit design has focused on conceptual work on small functional elements, such as half-circuits, current mirrors, or differential pairs. For example, it has been reported that by adjusting the biasing voltage of the SBs in a reconfigurable current mirror, the highly sought-after property of a perfectly linear drain current response can be achieved over a large voltage range [79]. V_{PG} can also be used to dynamically tune the transconductance gm of a differential half circuit. This tunability even extends if the RFET is switched seamlessly between all three operation modes [80]. For example, dynamic switching between frequency doubler, signal follower, and 180° phase shifter has been experimentally demonstrated using a single RFET (figure 15). Based on this functionality, a highly compact design can be conceived that enables binary-frequency- shift-keying (BFSK) and binary-phase-shift-keying (BPSK) [81]. Among all the examples, differential pairs are fundamental as they pose the input stage of every operational amplifier [79, 82]. Albeit being relatively simple structures, they can showcase various features like single-balanced differential mixers.

The main current challenge in application development is to translate these promising properties of the functional units into an added value for an actual circuit or system (figure 16). Noteworthy, the largest system showcased in simulations consists of eight transistors, while the largest hardware demonstrator still consists of only a single transistor. The reason for this is twofold: On the one hand, RFETs are still an experimental technology, which limits both the number of functional devices available on-chip as well as the possibilities regarding passive integration and back-end-of-line (BEOL) capabilities; on the other hand, the altered transport physics combined with the unique multi-gate structure limits the availability of circuit design models. To date, no compact model is available that can reflect all RFET properties in an analog circuit simulator. Stable models have been established to close this gap, but are quite limited in terms of both precision and simulation speed [81]. Thus, short- term developments should first focus on improving device yield, variability, and reliability while tackling passive co-integration and model development. These advancements will excel in analog design space exploration and system-level demonstrations in the mid-term. In the long run, the peak performance and benchmarking questions will gain importance again.

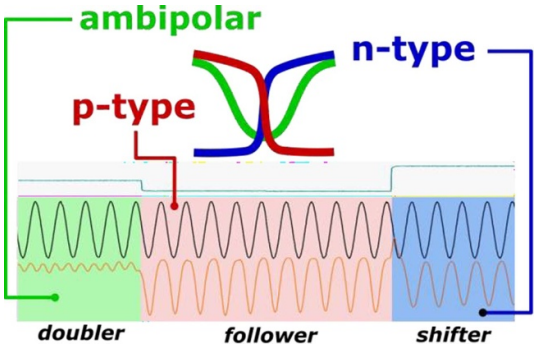

Figure 15. Illustration of the three RFET operation modes and its utilization for analog frequency processing.

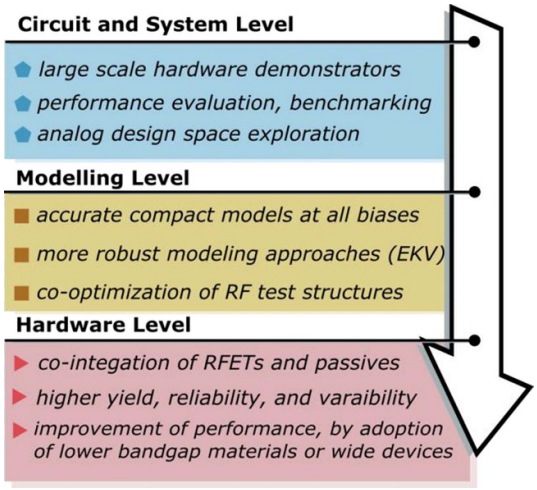

Figure 16. Cross layer perspective on the challenges of RFET development for analog circuit applications.

Advances in science and technology to meet challenges

The most important technological advancement needed to bring RFETs to the application domain is to allow circuit designers to tape-out and measure their own chips on a reliable industrial platform, allowing to integrate RFETs with passive elements. A big step towards this aim was recently showcased on the 22 nm FDSOI technology, by successfully processing reconfigurable SB-based devices on industrial scale 300 mm wafers for the first time [76, 80]. A natural next step in this development is a complete co-integration flow that allows for working N-FET, P-FET and RFET devices side-by-side. After this is achieved, developments should focus on improving yield, reliability and performance. Important factor for analog designs is to have the option of providing very wide channels in order to yield sufficient output currents. However, classically, wider channels lead to a less stable SB interface. New contact materials such as c-Al or NiTi-alloys can help to achieve a stable process integration. Arrays of multiple devices in parallel might be needed, and low bandgap channel materials, such as germanium or indium-arsenide, can help improve the performances [75]. Besides the hardware, analog designers require accurate compact models that seamlessly transition between all interesting bias points. Unlike in digital design, the small signal behavior in each individual operation point is more critical for analog designs [83]. RF test structures have to be conceived and characterized to determine the scattering parameters (S-Parameters) of both devices and functional units and help with accurate modeling. If a full physics description of the devices cannot be achieved in a short time frame, more mathematical approaches like the EKV model for MOSFETs might help to speed up the circuit development [84].

Concluding remarks

The high tunability of their electrical characteristics make SB-based RFETs an interesting emerging device concept for analog circuit design. Several highly sought-after features, like direct frequency doubling or linear current response, can be generated directly from single devices. Nevertheless, the low technology-readiness level of the technology is a major hurdle for commercial application development. Variability, yield, and reliability, as well as model development, are the most important challenges in the near future. Thus, great efforts have to be made on both the hardware and modeling sides to encourage analog circuit designers to exploit this disruptive new technology.

11. Challenges in SB transistors devices modeling

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Current and future challenges

Modeling SB transistors presents unique challenges compared to traditional field-effect transistors (FETs). The critical parameters influencing SB transistor performance include the SB height, thermal effects, contact resistance, quantum tunneling, surface states, high-frequency effects, material properties, electron–hole recombination, non-ideal behavior, technology scaling, integration challenges, and current continuity.

The SB height, a crucial factor in device performance, is challenging to model accurately due to its sensitivity to metal work function, interface states, and temperature. The exponential influence of the barrier height on current necessitates precise modeling, considering factors like the metal work function, interface states, and temperature dependence [85]. Various classical models exist in literature, introducing simplifications for circuit simulators but may not fully capture the complexity of the system.

Thermal effects, including temperature-dependent barrier height and self-heating impact, pose challenges in predicting device behavior under different operating conditions. The Schottky contact resistance, influenced by metal-semiconductor interactions, requires accurate modeling for overall device performance. Quantum tunneling becomes significant in high SB height scenarios, affecting carrier transport across the barrier, demanding accurate quantum effects modeling.

Surface states and traps at the metal-semiconductor interface introduce variability, especially at low temperatures, challenging accurate modeling due to their complex interaction with the SB. High-frequency effects such as parasitic capacitances and resistances are crucial to model for understanding device performance at elevated frequencies. Accurate material properties, including metal and semiconductor work functions, are essential, and variations due to manufacturing processes add complexity.

Electron–hole recombination at the metal-semiconductor interface affects the device's dynamic behavior, requiring precise modeling for realistic simulations. Non-ideal behaviors like leakage currents and non-linearities present challenges in capturing and modeling for an accurate device representation. Technology scaling challenges become pronounced as SB transistors scale down, addressing increased variability, quantum effects, and manufacturing impacts.

State-of the-art TCAD tools, e.g. Silvaco and/or Synopsys toolchain in general can be used for SB transistor device modeling. A bench of built-in models are offered, which are commonly used in the research community, i.e. WKB approximation, FN tunneling, etc. or even more advanced approaches as TMM method. The use of custom models in a sense of analytical equation-based models is not applicable at the moment. However, for example in [85, 86] a strong exchange with the vendor in application of different models for the SB lowering effect led to a more precise simulation of SB MOS Devices and according to the need of correct band diagrams including the applied SBL model at the SB. This was implemented in later versions of the TCAD simulation tool. Nevertheless, having more than one SB in series, forward or reverse biased, as it is the case in SB transistors, and including the effect of SBL and accurate tunneling models is still a challenge for convergence.

However, one has to tackle similar convergence difficulties with SB devices as for classical ones, especially when targeting low temperature simulations down to 4 K or lower. Here, only a few charge carriers influence the simulation result and therefore several settings in the solver section need to be adopted, with accuracy, precision and number format up to 256 bit. Even then it is difficult for the solver to converge. Here, a different step size might help. Alternatively, the 'hit it method', where a certain bias point is used at the start, can be employed if the inaccuracies of the first simulation steps are taken into account. However, the higher the precision the longer the simulation time.

Furthermore, the structure and its resulting mesh also greatly influence the simulation time. Starting from simple CAD structures and enhancing these with more accurate process simulation (see figure 17) results can impact the device simulations from a few minutes up to several hours. The behavior is similar to classical device topologies and identical empirical guidelines apply such as enhancing from 2D to 3D leads to a cubic mesh point dependency.

Integrating SB transistors into circuits poses additional challenges, requiring modeling of their interaction with other devices. Current continuity in SB transistors is influenced by various factors, and a compact model must identify the most dominant effect for current limitation.

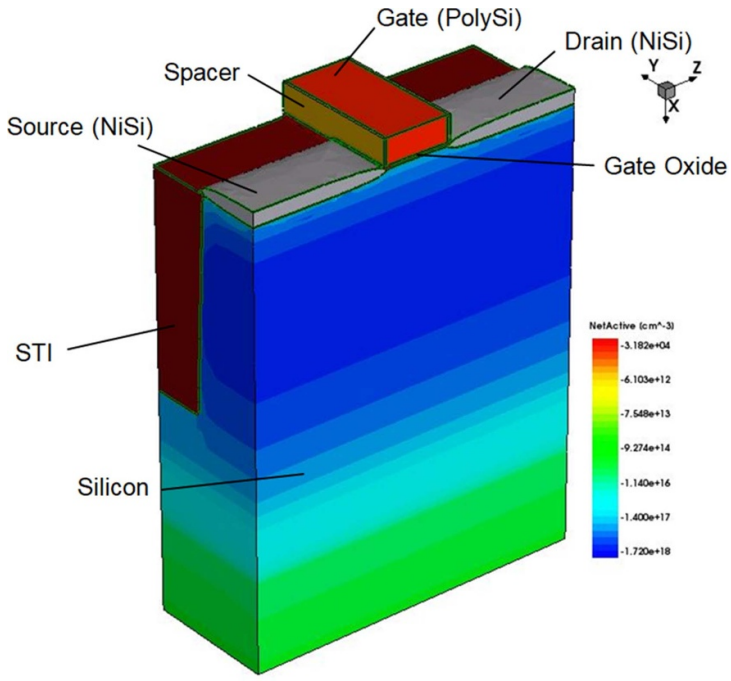

Figure 17. Fully processed model of a bulk Schottky barrier MOSFET with Synopsys process.

Advances in science and technology to meet challenges

The challenges in modeling SB transistors involve accurate representation and integration of various factors related to technology and characterization. This summary will focus on the modeling aspect while bridging the interface towards technology and characterization.

A critical parameter in SB transistor modeling is the SB height, which exerts exponential influence on current. Small deviations or inaccuracies in modeling can significantly impact this parameter. Interface states play a dominant role in affecting the barrier height, with direct cross sensitivity on band edge and temperature-dependent bands. Achieving an accurate model requires a deep understanding of the physical insights and the coupling of effects in one model, including the modeling of thermal effects for predicting device behavior under different conditions.

The Schottky contact resistance, metal-semiconductor interactions, and specific properties, including quantum tunneling, are crucial aspects that must be accurately modeled, especially for nanoscale SB transistors. Quantum effects become significant in high SB height scenarios with strong band bending, and accurate modeling of these effects is essential for predicting device behavior [87].

Interface states, in the form of surface states and traps, can induce oscillations in the I–V characteristics of tunneling current at low temperatures, posing a challenge due to their complex interaction with the SB [88]. Modeling high-frequency effects is also essential for understanding the device's performance at elevated frequencies.

Material properties, dependent on characterization techniques, are a vital consideration for modeling. Current continuity is crucial, with SB transistors having limitations in device current due to injecting SB at the source region or the inversion/accumulation channel formed by the gate. A compact model must weigh these effects against each other to identify the most dominating effect for current limitation. Incorporating these considerations into a model allows for accurate representation of electron–hole recombination, non-ideal behaviors, and integration challenges for system-level simulations.

In conclusion, a comprehensive model is necessary, providing compact explicit equations for circuit simulators. This model must consider various parameters, from SB height and interface states to quantum effects, material properties, and current continuity, to accurately predict the behavior of SB transistors in diverse conditions. TCAD simulation tools can help to generate compact models by analyzing the electrostatics of the device topology as well as transport mechanisms and allowing the determination of the most critical parameters to be considered in a compact model. The eventual realization of an interface for custom models, based on a community effort, would enable for more flexibility in testing new approaches.

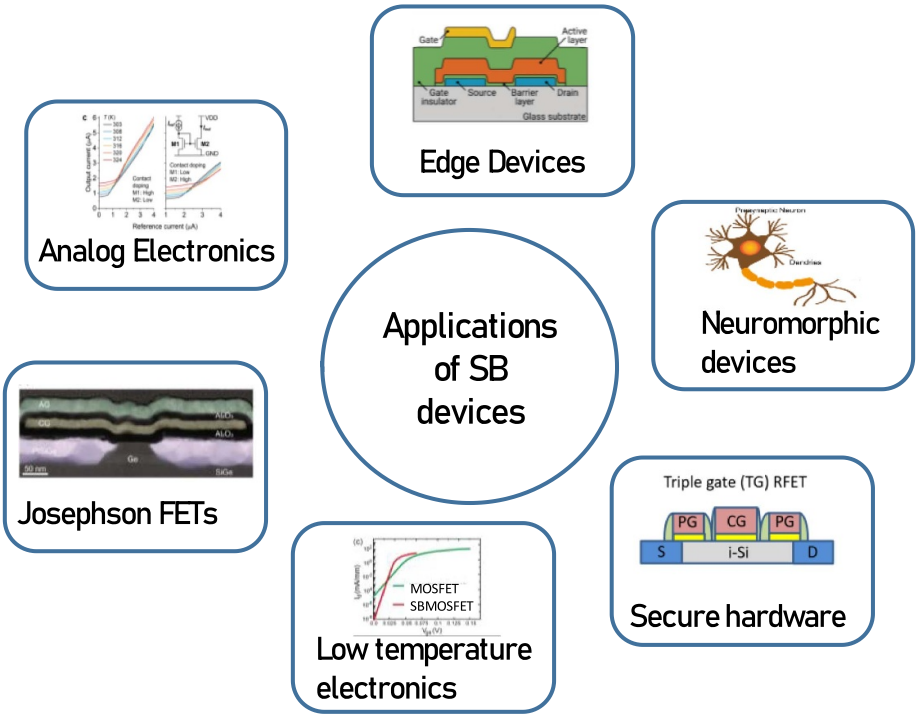

Figure 18. Illustration of the different applications of SB devices.

Concluding remarks

Modeling of SB transistors must consider many different physical effects in a very concise and compact way, preferably derived from fundamental physical equations. The balance between physically meaningful model parameters, which make possible a predictive circuit simulation, and purely empirical parameters, necessary for a closed form implementation in a circuit simulation environment, is a main challenge. The presence of two SBs interacting with the device channel potential further complicates the derivation of a compact model. This challenge may get easier when the source SB dominates the device behavior, as it is the case in SGT [20] or in short channel devices [89]. However, new SB transistor concepts such as the reconfigurable FET [90, 91] pose further challenges because here the SB at the source or at the drain or the channel region can limit the device current separately for electrons or holes, depending on the device configuration as a p- or n-type transistor.

12. Conclusions and perspective

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While the scope of this roadmap is quite broad, the interest in combining these different aspects into a single document should now be apparent. Mainly there are many challenges that the different devices have in common and that might lead to synergies for improvements in what might seem *a priori* very different objectives. We believe that the future applications of SB transistors depend on the materials in which they are fabricated, but an overview of their potential is given in figure 18.

The future of source gated transistors (SGTs) lies not only in the advances in materials, deposition, and patterning techniques, but also in emerging transistor structures that bring increased functionality in a compact footprint. The multimodal transistor, figure 5 [92], extends the concept of SGT by separating the control over charge injection and charge transport within the device, with implementations possible across a multitude of material systems. Early development hints at significant advantages in both circuit reduction and performance/reliability improvements. Some examples that benefit from the unique functionality of the MMT are digital-to-analog converters (DACs) [93], multiplying DACs [92], XNOR/XOR logic [94], pulse width modulation (PWM) [95], and rectified linear units (ReLUs) in artificial neural networks (ANNs) [40], when designed with constant transconductance in saturation [92]. Moreover, separate gating of carrier injection from channel conduction allows for reduced hot-carrier effects [96], amongst other undesirable phenomena, produced by high electric fields at the source edge, where the semiconductor is fully depleted. SGTs can offer a real advantage of high intrinsic gain for closed-loop applications such as voltage references, buffers, amplifiers and current-biased circuits. They are most promising for applications in analog readout for sensors, and edge computing.

To integrate ferroelectric transistors and neuromorphic functionality, materials issues should focus on engineering the properties of the ferroelectric layer to optimize the layer thickness and understand the nature of the trap states. While FE neurons can be envisioned, the FE synapses can in principle be easily integrated into other SB devices due to similar processing optimization. While FE synapses with HfO_2 naturally integrate with RFETs, organic ferroelectrics can be envisioned to work with organic SGT devices.

Operating SB devices at low temperatures provides a natural advantage compared to traditional doped source/drain devices due reduced processing, improvements in device scaling and immunity to freeze-out. The main challenge is that the on-state voltage is reduced compared to conventional silicon source/drain FETs due to the large resistance from the SB. While PtSi devices exhibit comparable performance at low temperatures for p-type transistors [97], the equivalent in n-type devices has not been demonstrated. One promising technique may be the use of modulation doping of Si nanowires, which was recently demonstrated for p-type devices [98]. Similar, the improvements for JoFETs requires an important effort in materials optimization, with a proposed moved towards Ge devices.

The motivation behind RFET technologies is to increase the system functionality at a given feature size, without additional scaling of the critical dimensions. One the one hand, this can be executed by static programming of the functionality to yield more compact digital designs. A recent small-scale example is a compact, static 1-bit full adder operational with only 8 transistors [99]. On the other hand, the self-dual nature of RFET can be used to design dynamic reconfiguration of the circuit functionality, e.g. switching NAND to NOR, or XOR to XNOR [100, 101]. This allows for more efficient circuit designs, e.g. as demonstrated for arithmetic logic units [102]. Recently it was demonstrated that up to 8 functions can be mapped on a single gate composed of only four RFETs [103]. This feature of circuit polymorphism is especially promising for hardware security applications [104]. Utilizing reconfigurability circuits can be used to camouflage its functionality from layout reverse engineering as well as power or timing attacks [105, 106]. In addition, first analog applications are currently under investigation. The main challenges in terms of RFET device development going forward is enhancing the switching speed. The foreseen solutions involve improving the materials used for devices such as moving towards Ge or Si_xGe_{1-x} based channels to improve the charge carrier injection. In order to scale the promising concepts to industrial applications, the fabrication of RFETs need to be transferred into foundry processes, and the modeling of the unusual properties as well as circuit design need to be addressed.

One of the main challenges in developing emerging technologies is the difficulties in modeling and simulating their behavior. This stems from the realization of devices in a research laboratory and the

necessarily large range of physical effects that can be present and which are not necessarily constant from laboratory to laboratory and even over time in the same laboratory. While many of the physical effects are identified, integrating them into a single analytical model is not possible. The realization of the emerging technologies discussed here in the context of a relatively mature foundry would enable modeling more consistent with circuit fabrication. Alternatively, empirical [20] or machine learning methods [107] can be employed if enough experimental data is available.

Overall we have seen that many of the challenges facing these apparently very different types of devices are very similar. Fabrication in foundries in order to realize more complex circuits is a challenge for both SGTs, rFETs and cryogenic devices. Realizing models that can accurately describe device behavior and enable circuits simulations remains a major challenge. For SGTs and rFETs, circuits are more complex than in more conventional realizations, but come particular advantages for device operation. While engineering an ideal metal/semiconductor contact remains an important goal, for many of the technologies explored in this roadmap it is not a limiting factor for using SB transistors in applications.

Data availability statement

The data cannot be made publicly available upon publication because they are not available in a format that is sufficiently accessible or reusable by other researchers. The data that support the findings of this study are available upon reasonable request from the authors.

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