DEVELOPMENT OF SPIN-QUBIT DEVICES BASED ON ZNSE/ZNMGSE HETEROSTRUCTURES

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CONTENTS

ABSTRACT

Electrostatically defined quantum dots (EDQDs) are a promising platform for a successful implementation of universal quantum computing utilizing millions of qubits. After single and two qubit gate fidelities above the quantum error correction threshold were demonstrated in isotopically purified Si quantum wells (QWs), scaling up the qubit number remains a major challenge [1, 2]. One aspect is linking distant qubits, as well as realization of an efficient spin-photon interface that enables linking of quantum processors [3, 4].
To explore the potential improvement of ZnSe versus Si as host material for EDQD applications, this work investigates ZnSe motivated by six promising material properties: ZnSe is free of nuclear spins if isotopically purified, it provides a coherent spin-photon interface, it can be grown defect free, it has no threading dislocations, it has no valleys and it exhibits a strong spin-orbit coupling [5–8]. However, ZnSe is an underdeveloped material platform lacking Ohmic contacts with low resistivity at the operation temperature of quantum devices ($T \leq 4\,\text{K}$). To unlock the electrical exploration of the potential of a proposed EDQD in a ZnSe/ZnMgSe heterostructure, I investigate electrical contacts including doping, surface treatment and metallization techniques. By optimization of the metal-semiconductor interface, I report a record low contact resistivity ($\rho_\text{c}=4\times10^{-5}\ \Omega\text{cm}^2$ at 4 K) for Ohmic contacts by all *in-situ* fabrication including epitaxial doping, entirely conducted in-house with our collaboration partners at Forschungszentrum Jülich [5]. Regarding scaling, we modify our approach to locally contact a ZnSe channel ($\rho_\text{c}\sim1.4\times10^{-3}\ \Omega\text{cm}^2$ at 4 K), but find this technique incompatible with a ZnSe QW, facing limits in etch precision.
For gated Hall-bar devices on ZnSe/ZnMgSe heterostructures, observation of the field effect demonstrates basic device functionality at 4 K. However, lacking local Ohmic contacts, parasitic effects presumably originating from planar doping such as parallel conduction outside the ZnSe QW and recharging of defects compromises device performance.
To avoid performance limitations originating from planar doping, we develop an alternative *in-situ* process well suited to locally contact a ZnSe QW [9]. Based on selective epitaxial growth utilizing a shadow mask, our approach yields $\rho_\text{c}\sim2.5\times10^{-3}$ Ωcm^2 at 4 K, demonstrated for for a triangular ZnSe QW. The presented technique enables exploration of all-electrical ZnSe quantum devices at low temperature ($\text{T}\leq 4\,\text{K}$).

ZUSAMMENFASSUNG

Elektrostatisch definierte Quantenpunkte (EDQD) sind eine vielversprechende Plattform für eine erfolgreiche Umsetzung des universellen Quantencomputers mit Millionen von Qubits. Nachdem in isotopisch gereinigten Si-Quantentöpfen (QWs) eine Gattertreue von einem und zwei Qubits oberhalb der Genauigkeitsgrenze von Quantenfehlerkorrektur nachgewiesen wurde, bleibt die Erhöhung der Qubitanzahl eine große Herausforderung [1, 2]. Ein Aspekt ist die Kopplung entfernter Qubits sowie die Realisierung einer effizienten Spin-Photonen-Schnittstelle, die die Kopplung von Quantenprozessoren ermöglicht [3, 4].

Um die potenzielle Verbesserung von ZnSe gegenüber Si als Ausgangsmaterial für EDQD-Anwendungen zu untersuchen, wird in dieser Arbeit ZnSe aufgrund von sechs vielversprechenden Materialeigenschaften untersucht: Isotopenreines ZnSe ist frei von Kernspins, erlaubt kohärente Spin-Photon-Kopplung, kann defektfrei, ohne Schraubenversetzungen, gewachsen werden, es hat keine Täler und weist eine starke Spin-Bahn-Kopplung auf [5–8]. ZnSe ist jedoch eine unterentwickelte Materialplattform, der es an ohmschen Kontakten mit niedrigem Widerstand bei der Betriebstemperatur von Quantenanwendungen ($T \leq 4\,\mathrm{K}$) mangelt. Um die elektrische Erforschung des Potenzials eines vorgeschlagenen EDQD in einer ZnSe/ZnMgSe-Heterostruktur zu ermöglichen, untersuche ich elektrische Kontakte einschließlich Dotierungs-, Oberflächenbehandlungs- und Metallisierungstechniken. Durch die Optimierung der Metall-Halbleiter-Grenzfläche konnte ich einen rekordverdächtig niedrigen Kontaktwiderstand ($\rho_c = 4 \times 10^{-5}\,\Omega\mathrm{cm}^2$ bei 4 K) für ohmsche Kontakte durch vollständige *in-situ*-Fertigung, einschließlich epitaktischer Dotierung, erzielen, die wir mit unseren Kooperationspartnern am Forschungszentrum Jülich durchgeführt haben [5]. Hinsichtlich der Skalierbarkeit modifizieren wir unseren Ansatz, um eine ZnSe-Schicht lokal zu kontaktieren ($\rho_c \sim 1.4 \times 10^{-3}\,\Omega\mathrm{cm}^2$ bei 4 K), aber stellen fest, dass diese Technik aufgrund begrenzter Ätzgenauigkeit nicht mit einem ZnSe-QW kompatibel ist.

Bei Hall-Bar-Bauelementen auf ZnSe/ZnMgSe-Heterostrukturen mit elektrischem Gatter zeigt die Beobachtung des Feldeffekts die grundlegende Funktionalität der Bauelemente bei 4 K. Da jedoch lokale ohmsche Kontakte fehlen, beeinträchtigen parasitäre Effekte, die vermutlich von der planaren Dotierung herrühren, wie Parallelleitung außerhalb der ZnSe-QW und Aufladung von Defekten, die Leistung der Bauelemente.

Um Leistungseinschränkungen durch planare Dotierung zu vermeiden, entwickeln wir einen alternativen *in-situ*-Prozess, der gut geeignet ist, einen ZnSe QW lokal zu kontaktieren [9]. Basierend auf selektivem Epitaxiewachstum unter Verwendung einer

Schattenmaske liefert unser Ansatz $\rho_\mathrm{c} \sim 2.5 \times 10^{-3}\,\Omega\mathrm{cm}^2$ bei 4 K, gezeigt für einen triangularen ZnSe QW. Die vorgestellte Technik ermöglicht die Erforschung vollelektrischer ZnSe-Quantenbauelemente bei niedrigen Temperaturen (T$\leq$ 4 K).

1

INTRODUCTION AND STRUCTURE OF MANUSCRIPT

1.1. INTRODUCTION

The great promise of quantum computation is exponential speedup in solving relevant problems of our time, exceeding the computational power of classical computers. With quantum advantage demonstrated already in 2019, useful applications to come range from cryptography (prime factorization by i.e. using Shor's algorithm) to big data search (i.e. Grover's algorithm) or quantum simulations (i.e. Haber-Bosch process) [10]. The time line for quantum computers to solve relevant problems, expected for $10^6 - 10^8$ physical quantum bits (qubits) employing quantum error correction, is subject to research, investment and physics and hard to foresee [11]. With a global long time invest in quantum computing continuously increasing without a predictable time for the return on invest, meanwhile noisy intermediate-scale quantum (NISQ) applications could prove useful [12]. Up to now, the race for the best technology is open, and establishment of problem specific hardware solutions, as seen in classical computing for graphic cards, are likely to develop [13].

Technologies for universal quantum computers being experimentally investigated today make use of qubits defined in superconducting circuits, ion traps, or in semiconductors [11, 12, 14, 15]. Some applications foresee realization of a quantum network, where quantum entanglement is envisioned as natural protection versus attacks by third parties [3]. One challenge for all platforms is realization of short and long range coupling of qubits, while maintaining both electrical control and high coherence times of quantum states (T_2^*) compared to gate times [16]. Regarding long range coupling, given a spin-photon interface, photons at telecommunication-band photons in optical fibers are the naturally preferable carrier of quantum information of choice, facing challenges in reaching high transfer rates [3, 4]. Another major challenge is scale up to millions of error-corrected, logical qubits. The technological lead in scale up of semiconductor industry established for classical electronics, the transistor node size reaches 2 nm this year, could play off when pursuing electrostatically defined quantum dots build on planar heterostructures [17].

This thesis is about exploration of ZnSe for electrical quantum applications, since it offers both electrical and optical control on quantum systems and has many useful material properties that make the material interesting for spin qubit applications [3, 6, 18–20]: ZnSe is an optically active material with a direct bandgap that allows for coherent spin-to-photon conversion. To demonstrate this experimentally, electrons bound to a F donor in a ZnSe quantum well were used for the implementation of a single photon source [6]. ZnSe is free of valley states, that contribute a relevant decoherence channel in Si [5, 21]. In addition, ZnSe provides high crystal quality (no threading dislocations) when grown in fully strained epilayers [6, 22]. By isotopical purification, ZnSe can be made a spin vacuum, with expected improvement of coherence time for spin qubits [1, 7, 23]. ZnSe offers a high spin-orbit coupling, that could ease addressability and control of qubits [8, 23, 24].

Although being a wide band gap semiconductor, and not SiMOS compatible, the interesting material properties of ZnSe motivate me to explore approaches directed at implementation of an EDQD device in ZnSe. One needs to keep in mind, the time advantage by Si semiconductor industry is more than half a century, making this material one of the best known materials in the world, which does not necessarily mean it is naturally best suited for hosting a quantum computer. For example, two qubit gates with a fidelity at the threshold for quantum error correction have been achieved using industrial fabrication standards (SiMOS) recently, but without control over valley states, addressability of Si qubits remains a challenge [1, 21, 25, 26]. Goal of this thesis is to explore the potential for ZnSe based quantum devices using the technology of EDQDs realised on a ZnSe/ZnMgSe heterostructure.

The optical properties of ZnSe are well known from research and development and applications of LEDs in the blue spectrum, and other optical applications, such as single photon sources or solar cells [27]. However, electrical properties of ZnSe are less well understood, experimentally constricted by the challenge that Ohmic contacts with low resistivity are not easy to realise. My work addresses the issue of contacting n-ZnSe, prequesite to exploration of (quantum) effects at operation temperature of a quantum computer [5].

1.2. STRUCTURE OF MANUSCRIPT

In Chapter 2, I introduce the basic concepts for a semiconductor-based qubit encoded in the spin degree of freedom of a single electron. For this approach, I will motivate ZnSe as a very promising material platform. The chapter is structured in two sections: At first, in the context of the target approach, general requirements for EDQD based spin qubits in semiconductors are discussed. Second, from these requirements I derive a concrete layout for an EDQD device in ZnSe.

In Chapter 3, I address the topic of electrically contacting the II-VI semiconductor. This chapter covers the main objective of my work, reproducible fabrication of low resistivity contacts to n-ZnSe. At the beginning of this chapter, I introduce the physics of the metal-semiconductor contact and discuss, how the experimentally relevant specific contact resistivity can be assessed. I characterise and discuss the performance of Ohmic contacts obtained by various fabrication techniques, that are separately specified in Chapter 5. Electrical characterization of Ohmic contacts is performed at low temperature of 4 K and low bias voltage, to mimic to conditions at which contacts to qubit devices are typically operated. At the end of this chapter, as one of the two central achievement of this thesis, I identify *in-situ* deposited metal contacts on n-ZnSe as optimal.

In Chapter 4, electron scattering in ZnSe will be discussed to illuminate the processes relevant when electrostatically defining an electron quantum dot. Fundamental questions to be addressed are the major processes for electron scattering and the mean free path for the operation temperature of quantum devices. Section 4.2.2 discusses the Metal-Insulator Transition in ZnSe and ZnMgSe, relevant for allowing electrical readout that requires electron reservoirs and Ohmic contacts operating at $T \leq 4\,\mathrm{K}$.

In Chapter 5, I describe the processes used for fabrication of ZnSe based devices. The first section of this chapter explains the fabrication routine followed for fabrication of electrical devices with gate control (Sect. 5.1). In the following sections, I outline in detail the individual process steps, epitaxial crystal growth (Sect. 5.2), doping and fabrication of contacts or gates. I close the chapter with the verification of the combined process flow, demonstrating basic functionality of all control gates for a device similar to the proposed ZnSe EDQD device (Sect. 5.7).

In Chapter 6, a gated Hall-bar fabricated on a ZnSe/ZnMgSe heterostructure is presented as final device, entirely fabricated in-house. The discussion contains evaluation of electrical performance of this device at room temperature and 4 K, addressing transport through the device, tunability of transport and gate isolation. Finally, the limitations of the device performance will be analysed and related to the fabrication process.

In Chapter 7, I provide a solution for local Ohmic contacts which continues on the previously identified *in-situ* method (Chap. 3). This approach opens the perspective to address the challenge of local doping identified as requirement in fabrication of Ohmic contacts (Chap. 3) and device performance of gated Hall-bars (Chap. 6). The basic principle is formation of local Ohmic contacts in the vicinity of a 3D shadow mask, enabled by selective epitaxial growth harnessing a shadow effect. In a first step, the basics of the selective epitaxial growth process is analysed, subject of a paper draft I co-authored [9]. Second, our fabrication process is successfully modified to form local Ohmic contacts to a ZnSe/ZnMgSe QW. With our proof of concept experiment, we enable future exploration of all-electrical quantum devices in II-VI material.

Finally, I give a brief summary of the results of this work and and an outlook in Chap. 8.

2

PROPOSAL OF AN EDQD DEVICE IN ZNSE

Motivated by the promising material properties introduced above, this chapter proposes a device concept for realization of electron spin qubits in ZnSe. Technologically, our concept is based on electron spin qubits implemented in electrostatically defined quantum dots (EDQDs) in group III-V or group IV semiconductors.[1] In these material systems, EDQD devices have been intensively investigated and improved over the last two decades [1, 28, 29]. Key features of EDQD devices are Coulomb blockade and Pauli-blockade implemented along (single shot) readout and single electron (qubit) control to be reflected in the device design.

We envision implementation of a ZnSe spin qubit, using bandgap engineering and structuring methods. The first section describes the layout for our ZnSe based EDQD device (Sect. 2.1). Thereafter, we discuss important key figures of the qubit device in Sect. 2.2, such as physical requirements for qubit operation and technical boundary conditions given for a typical laboratory environment [11, 30].

2.1. DEVICE CONCEPT

The technology utilised by EDQD devices is well known for about two decades. Basic technological concepts for the isolation of single electrons, electrical readout and control are nicely introduced in Ref. [31]. Although our concept is compatible with systems hosting a large number of qubits, this work focuses on a very basic system

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[1] Lars Schreiber and Alexander Pawlis initiated the project and developed the main idea of a electron spin-qubit utilizing a ZnSe/ZnMgSe HS. The electrical structure of the HS was calculated by Alexander Pawlis, Johanna Janßen and me using a solver developed by Nils von den Driesch. I designed the gate layout for spin-qubit devices on ZnSe based on a layout designed for Si devices by Bernhard Klemt. I calculated theoretical noise levels arising from Ohmic contacts and deduced project goals on contact resistivity in collaboration with Arne Hollmann and Lars Schreiber. I deduced the free mean path for ZnSe reported in the literature with the support of Lars Schreiber. The literature review on the thermal budget of ZnSe, the charge noise and the spin-orbit interaction was conducted by me.

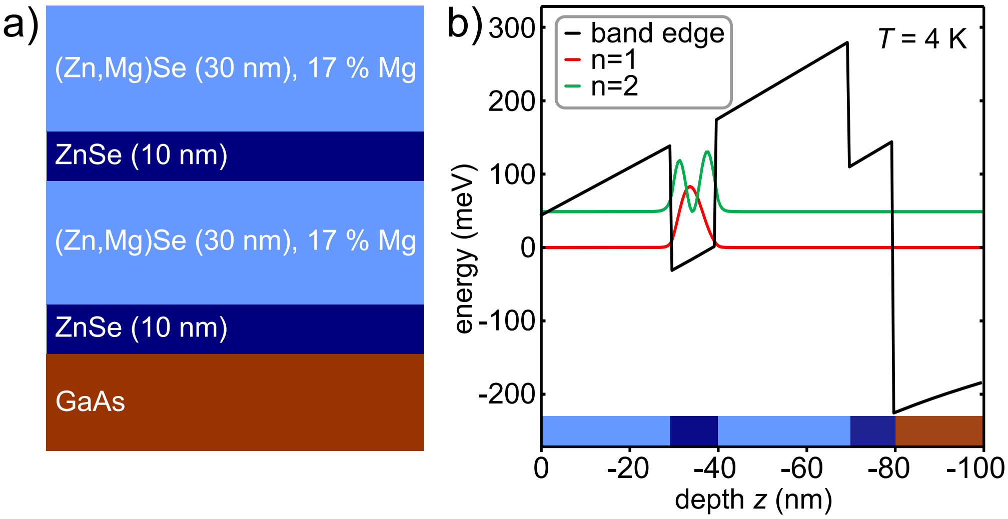

Figure 2.1: Simulation of the conduction band edge of a ZnSe/ZnMgSe heterostructure and low energy electron states. a) Layer stack for the undoped target heterostructure with a 10 nm thick ZnSe QW embedded in two 30 nm thick ZnMgSe barriers with a Mg content of 17 %. This system is separated by a 10 nm thick ZnSe buffer from a GaAs substrate. b) Simulated probability distribution of the electron wave function (1D Poisson-Schrödinger solver) versus z (along growth direction) for $T = 4\,\mathrm{K}$. The z axis is color coded corresponding to panel a). By (electrical) control of the chemical potential in the ZnSe QW, electrons can be confined to the ZnSe QW, see the probability distribution for the corresponding wave function of the ground state (red line). All boundary conditions and parameters entering the simulation (CB/VB offset, assumptions on strain) are listed in Tab. A.1.

with two qubits [32]. In short, the qubit is encoded in the spin degree of freedom of a single electron. An external magnetic field defines the quantization axis of the quantum state, that can be represented on the Bloch sphere. By convention, the poles correspond to the spin up and spin down state, and are chosen as basis states subject to quantum operations (quantum gates). Nanostructure gates are implemented to individually manipulate the chemical potential, the position and spin state of the electrons, using the field effect and electron spin resonance (ESR) [31]. Electrical readout of the qubits is performed using single electron transistors (SETs) electrostatically coupled to the qubit [28].

Targeting electrostatic control of the electron dot in three dimensions, we combine two approaches: Along the growth axis z, a QW potential is obtained by bandgap engineering and in lateral directions multiple control gates allow for adjustment of confinement potentials and energy levels of individual electrons, to be explained in the following. The nomenclature EDQD reflects the intention of full electrical control in devices in combination with ESR, in contrast to other semiconductor based spin qubit systems like defect centers or nuclear spins which are more localised [31, 33, 34].

2.1.1. BANDSTRUCTURE ENGINEERING

Technically, the QD is realised as EDQD in an HS allowing for full control of the electric confinement potentials and related energy levels of the QD that we calculate using the Schrödinger equation. Since the electron wave function is a product function of solutions for each of three dimensions, energy levels of the electron in the ZnSe quantum well are adjustable by the electric potential in lateral and vertical direction, separately. At first, we solve the Schrödinger equations and Poisson equation in z for a ZnSe/ZnMgSe HS as depicted in Fig. 2.1 a). The proposed HS features a 10 nm thick ZnSe QW embedded in two 30 nm thick ZnMgSe barriers with a Mg content of 17 %, separated by a 10 nm thick ZnSe buffer from the GaAs substrate. Regarding the ZnSe/ZnMgSe HS, basically three parameter sets, namely Mg concentration x_{Mg} in the barriers, layer thicknesses and doping profiles can be used for optimizations, referred to as bandstructure engineering. Dimensions and QW band offset of this HS are motivated by suitable values established in other material systems [16].

We use a 1D Schrödinger-Poisson solver to obtain the conduction band (CB) edge and the wave functions and energy levels of states with corresponding population probabilities in the ZnSe/ZnMgSe HS (Fig. 2.1 b), for details of the boundary conditions see Tab. A.1 in the appendix. The ground state is defined as the state located in the ZnSe QW lowest in energy and assign zero energy to it. By definition, states in the GaAs substrate are neglected. This assumption can be made, since these states are not electrically connected neither to an Ohmic reservoir nor the QW. The tunnel barrier between the ZnSe QW and the GaAs is wide and high, with ~40 nm and ~200 eV, respectively.

Fig. 2.1 b) displays the solution of the solver for the first two states in the II-VI region. For the given z confinement, both the ground state (n=1) and the first excited state (n=2) are located in the ZnSe QW, where n denotes the number of nodes of the wave function (along z). The state with n=2 has an orbital energy ~50 meV higher compared to the ground state energy and can thus not be occupied at $T \leq 4$ K. All other states, including those in the upper ZnMgSe barrier (see Fig. A.1), are even higher in energy and also not occupied.

In summary, bandstructure engineering can confine electrons in the introduced ZnSe/ZnMgSe HS, where they exclusively populate the lowest state located in the ZnSe QW if the Fermi level is sufficiently high. These electrons represent a 2D electron gas (2DEG), effectively confined in z-direction by strong electric fields originating from the ZnSe/ZnMgSe heterointerfaces at both sides of the ZnSe QW. From an experimental point of view, the Fermi level can be controlled by connecting Ohmic reservoirs to the ZnSe QW, and by control of the chemical potential in the ZnSe QW with respect to the adjacent regions. Next, we discuss what a device that allows such elec-

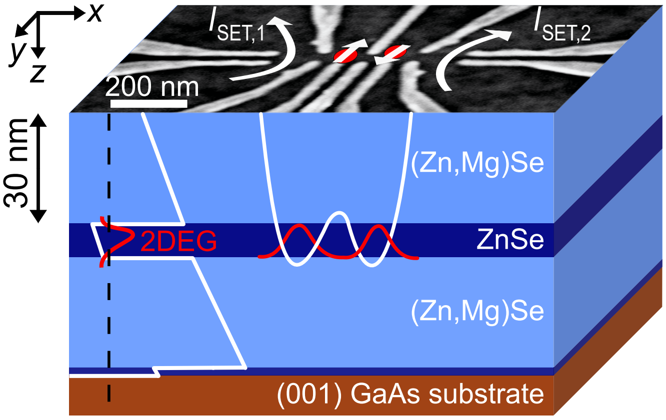

Figure 2.2: Concept for a ZnSe based EDQD device. Device schematics with electrons electrostatically confined to a 10 nm wide quantum well by a ZnSe/ZnMgSe heterostructure. The edge of the CB is shown on the left (white line) according to the 1D simulation (Fig. 2.1). In accumulation mode, a 2DEG is formed in the ZnSe QW, see the corresponding wave function of the orbital ground state in z (left, red line). By electrical control of nanostructure gates at the surface of the device (bright, top), two adjacent single electron dots and adjacent SETs are defined. White arrows denote the current used for electrical readout (left/right) or electron spins (center). A global accumulation gate covering all gates in the depicted region is not shown.

trical control might look like.

2.1.2. ARCHITECTURE OF A ZNSE BASED EDQD DEVICE

The full architecture of the envisioned ZnSe EDQD device is schematically depicted in Fig. 2.2. Electron wave function and electron dots are represented by red lines and dots, respectively. The conduction band (CB) edge of the ZnSe/ZnMgSe HS introduced above (white lines in Fig. 2.2) leads to a 2D confinement of electrons in the ZnSe, where they form a 2DEG. Nanostructure gates, as exemplary depicted in the uppermost area in Fig. 2.2, are utilised to achieve the desired functionality of an EDQD device by shaping the 2D potential in the ZnSe QW: For electrical readout, a SET is formed, adjacent to two single electron dots. Fig. 2.2 depicts the four gates to the left (right) that laterally define the current path $I_{\mathrm{SET},1(2)}$ (white arrow) in the 2DEG. Adjacent to the SETs, single electron dots (red dots) can be defined in the center of the device using another set of gates. In addition, a voltage applied to a global top-gate (not shown in Fig. 2.2) can tilt the potential along z and thereby shift the Fermi level as well as the distance between electron and heterointerface.

In the following, I will outline requirements for qubit operation of the EDQD device described above considering experimental and physical boundary conditions. A fabrication process for realization of such an EDQD device is introduced in Chap. 5.7

and transport in a ZnSe/ZnMgSe HS utilizing premature gated Hall-bar devices is discussed in Chap. 6.

2.2. OBJECTIVES

Here, I motivate some requirements for full functionality of our target EDQD device proposed above. For simplicity, this discussion covers only single-qubit gates. Single-qubit gates correspond to rotations of the electron spin state on the Bloch sphere by a specific angle along one of the two independent control axes. One way to characterise qubit gates is the gate-fidelity, a measure that can be used to describe parasitic under/over-rotation which can result from noise or imperfect gate operations [35, 36]. Effects relevant for the following discussion are charge noise (spin orbit mediated spin to charge coupling), hyperfine-interaction (spin - spin coupling) or Johnson noise (thermal noise) [11]. These effects directly or indirectly couple to the electron spin which can be effectively probed as loss of gate fidelity.

2.2.1. OPERATING TEMPERATURE

The operating temperature of electrostatically defined electron spin qubits in semiconductors must be small enough for thermal excitations not to harm qubit operation. This sections discusses the first energy levels of excited states that could compromise quantum operations if thermally excited. We look at the excitation energy of the first excited orbital state (along z or x/y) or spin state and compare these to the thermal energy $k_\mathrm{b}T$. For this discussion we assume thermal excitation into states $5k_\mathrm{b}T$ above the ground state can be neglected.

In an external magnetic field of flux density B_ext, the two electron spin states are split by the Zeeman energy [37]

$$E_\mathrm{z} = g\mu_\mathrm{B}B_\mathrm{ext}, \tag{2.1}$$

where g denotes the electron g-factor and μ_B the Bohr magneton. Assuming g=+1.1 for ZnSe and $B_\mathrm{ext} = 1\,\mathrm{T}$, the Zeeman energy equals 60 µeV ($\sim 5k_\mathrm{b}\cdot 0.15\,\mathrm{K}$) [38]. Therefore it is required to operate the qubit device at a temperature $T \leq 0.15\,\mathrm{K}$.

Another aspect to be considered is to exclude thermal excitation of orbital z states by proper bandstructure engineering. In first approximation, the level energy $E_\mathrm{orb,z}$ depends quadratically on the width of the QW for a sharp 1D potential of infinite height [37]. For realistic systems, the overall height and the sharpness of confinement potentials matter, which is covered by our 1D Poisson-Schrödinger solver shown above (Sect. 2.1.1). The overall height of the in-built confinement potential (170 meV) at the ZnSe/ZnMgSe heterointerface is in the range of 100–200 meV achieved in typical Si/SiGe or GaAs/AlGaAs heterostructures [39, 40]. We obtain an energy difference of 50 meV ($\sim 5k_\mathrm{b}\cdot 125\,\mathrm{K}$) from our simulation (Fig. 2.1), for which thermal excitation from the ground state into the first excited state is impossible.

More relevant is the level energy resulting from lateral confinement in x and y compared to z-confinement. The level splitting $E_\mathrm{orb,xy}$ attributed to the orbital level splitting of x, y states of the single electron confined in a QD is lower since the potential is smoother in lateral direction. Assuming the lateral confinement potential to be quadratic, the Schrödinger equation represents a harmonic oscillator and relate the energy difference between levels to the dot size, regardless of the orbit number. With the diameter d defined as half the full width at half maximum of the ground state wavefunction, one obtains [21, 41]:

$$E_{\mathrm{orb,xy}} = \frac{\hbar^2}{m_{\mathrm{eff}}(d/2)^2} \tag{2.2}$$

In ZnSe, we assume an electron g-factor of +1.1 and m_{eff} of 0.147 m_{e} [8, 38, 42]. To estimate the orbital splitting energy, we assume a realistic value of $d \sim 40\,\mathrm{nm}$, as has been determined in a Si based EDQD device, which equals half the gate pitch as well as the depth of the QW [21]. With these numbers Eq. 2.2 yields an orbital splitting energy of 0.72 meV ($\sim 5 k_{\mathrm{b}} \cdot 2.8\,\mathrm{K}$) [42]. This value is significantly larger than the Zeeman energy and therefore does not restrict the operating temperature.

Considerations relating to the operation temperature are taken for level splittings resulting from QW confinement ($E_{\mathrm{orb,z}}$), lateral QD confinement ($E_{\mathrm{orb,xy}}$) and the spin splitting in magnetic field (E_{z}). Among these, the by far lowest energy difference is E_{z} of about 60 μeV at 1 T which suggests to operate qubits at $T \leq 0.15\,\mathrm{K}$ or at higher magnetic field.

So far, impact on the qubit by Johnson noise, mediated from Ohmic contacts and reservoirs to the 2DEG, or Shot noise, has not been considered in the discussion of the operation temperature, but are separately addressed in the following section.

2.2.2. OHMIC CONTACTS

Solving of realistic problems by a quantum computer is expected for operation of about $10^6 - 10^8$ physical qubits using quantum error correction methods [11]. Focusing on the EDQD device architecture presented above, local Ohmic contacts are required for qubit initialization and readout utilizing SETs. In the following, we discuss technical and physical limits of such a system to deduce a requirement on the contact resistivity ρ_{c} of Ohmic contacts.

To guarantee sensitivity of SET readout, Ohmic contacts need to be less resistive than the typical resistance of a quantum point contact that is in the order of the von Klitzing constant ($R_{\mathrm{K}} \sim 26\,\mathrm{k\Omega}$) [43]. SETs are typically operated at a bias of <1 mV, in order not to exceed the charging energy of an EDQD [29, 31, 44].

Noise affecting the qubit is partly originating from Johnson noise generated at the Ohmic contact. For some realistic assumptions, parameters from SET readout of a Si device are used with a typical readout current I of 1 nA, an electron temperature T_{e} of 130 mK, a contact resistance R_{c} of 10 kΩ per contact and a readout bandwidth Δf of 10 kHz [21, 39]. With these boundary conditions the thermal Johnson-Nyquist noise V_{rms} can be derived to be [45]

$$V_{\mathrm{rms}} = \sqrt{4 k_{\mathrm{b}} T R_{\mathrm{c}} \Delta f} = 27\,\mathrm{nV} \tag{2.3}$$

$$\frac{V_{\mathrm{rms}}}{\sqrt{\mathrm{Hz}}} = 0.27\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}. \tag{2.4}$$

This noise level is not negligible, since it is a tenth of the contribution from charge noise observed at $f = 10\,\mathrm{kHz}$ limiting spin coherence time in a Si spin qubit device [16].

Furthermore, the qubits could be affected by Shot noise, current fluctuations σ_{i} in the SET. With the same boundary conditions, the Shot noise can be derived [46]:

$$\sigma_{\mathrm{i}} = \sqrt{2eI\Delta f} = 1.8\,\mathrm{pA} \tag{2.5}$$

$$\frac{\sigma_{\mathrm{i}}}{\sqrt{\mathrm{Hz}}} = 18\frac{\mathrm{fA}}{\sqrt{\mathrm{Hz}}} \tag{2.6}$$

Converted to a voltage noise, Shot noise is comparable but smaller than Johnson noise in our case.

To rule out resistive heating as a potential limitation for technological applications, we consider 10^8 qubits to be read out by SETs operated at 1 nA with a single contact resistance not exceeding $10\,\mathrm{k}\Omega$. This estimate is aggressive, since the qubit count is quite ambitious and multiple qubits can be reliably read out by a single SET, at current levels lower than assumed. Still, the resistive heating power of 10 µW is well below the cooling power of several 100 µW available at 100 mK in typical mixing cryostats.

To sum up, the assumptions on Ohmic contacts made here for EDQD devices base on electrical qubit readout using SETs and include resistive heating, Shot noise and Johnson noise arising from Ohmic contacts affecting qubit performance. Including the perspective of up-scaling to billions of qubits, we argue local Ohmic contacts with reproducible $\rho_{\mathrm{c}} < 1\times10^{-2}\,\Omega\,\mathrm{cm}^2$ are required. In absolute resistance, this corresponds to Ohmic contacts with $R_{\mathrm{c}} < 10\,\mathrm{k}\Omega$, operated at a bias typically below 1 meV and $T < 4\,\mathrm{K}$.

2.2.3. THERMAL BUDGET FOR FABRICATION

Fabrication of ZnSe/ZnMgSe based quantum devices requires compliance with a thermal budget for all fabrication processes to avoid defect generation in the quantum region. Crystal defects can result from in-diffusion of atoms, like intentionally utilised, outside the quantum region, in the case of diffusion contacts [47]. The opposite effect, out-diffusion, can occur preferably for group II elements leaving behind vacancies, relevant for temperatures typically above the growth temperature [48]. This effect will be discussed in Chap. 3 in more detail. We note, state-of-the-art fabrication methods for Ohmic contacts based on diffusion, utilise annealing at T ~250–300 °C, operating close to a regime where the substrate degrades [49, 50].

Diffusion of crystal atoms is of particular concern for quantum devices featuring a QW. Here, the thermal budget can be estimated from the growth temperature (290 °C), where strain relaxation-driven diffusion at the QW heterointerface is relevant [7, 51, 52]. Specifically for ZnSe/ZnMgSe heterostructures, diffusion of Mg is expected to occur for $T \sim 430\,°C$ [53]. Presence of p-tpye defects promotes diffusion, known as Fermi level effect, causing significant Mg diffusion starting already at 360 °C for a p-type defect concentration of $1 \times 10^{17}\,\mathrm{cm}^{-3}$ [53]. Since the quantum region of our target device is undoped, this effect does not play a role.

Finally, effects not specifically addressed here, like strain induced by the metal gates with different expansion coefficients than the substrate, could be relevant for device fabrication [54]. Based on the state-of-the-art in the research field, we conclude, a thermal budget of 250–300 °C on a time scale of minutes to be well suited for processing ZnSe based quantum devices [49].

2.2.4. CHARGE NOISE

For the most advanced semiconductor spin qubit platform, Si, charge noise is the limiting factor for high fidelity operations of single and two qubit gates, if not nuclear spin noise [1, 2, 16]. By artificial spin orbit coupling, charge noise can couple to the electron spin as electric field fluctuations caused by charge redistribution in the vicinity of the qubit shake the electron. For two qubit gates, charge noise affects the exchange coupling [55]. While quasistatic noise can in principle be corrected for, charge noise faster than the gate time compromises gate fidelity [55, 56].

Experimental evidence for charge noise is a $1/f$ frequency dependence of spectral noise density arising from an ensemble of two level fluctuators (TLF) [16, 55]. Charge noise can be measured using the power spectral noise density of an electrical quantum system like a SET or double qubit [56]. The charge noise originates from rechargeable defects in the vicinity of the quantum system. Typically, defect concentrations are highest at interfaces, most importantly at the semiconductor-oxide interface. Accordingly, charge noise in Si QWs is lower than in SiMOS devices, where the qubits are very close to the semiconductor-oxide interface, also reflected in gate fidelities [1, 25, 56]. However, ongoing efforts in gate stack optimization of the of CMOS devices with industrial methods promises significant improvement of charge noise toward levels obtained in Si QWs [57].

We conclude, our proposed EDQD device in a ZnSe/ZnMgSe HS is well suited for exploration of quantum applications, since the layer sequence guarantees a separation of the ZnSe QW from the metal-oxide interface. Low defect fabrication of the crystal, oxide and metal-oxide interface must be considered in all fabrication processes to ultimately be evaluated in terms of charge noise. Important will be crystal quality and spin-orbit interaction which can couple charge noise to the qubit, as outlined in the next paragraph.

2.2.5. SPIN-ORBIT INTERACTION

ZnSe crystals exhibit zinc blende structure, the same as ZnMgSe in the composition used within this work. The crystal symmetry of zinc blende is described by the point group $\mathrm{F\bar{4}3m}$. Anion and cation sites are located in face-centered cubic lattices shifted by one bond distance with respect to each other. This represents a diamond cubic structure, but since more than one atom type is involved zinc blende structure does not provide inversion symmetry. In semiconductors without inversion symmetry, electrons orbiting in an electric field experience an internal magnetic field, which is thus expected for ZnSe and ZnMgSe. With the electron orbit being affected by the internal magnetic field, spin and momentum are effectively coupled, referred to as spin-orbit interaction (SOI). One differentiates two contributions to this effect that arise from different origins of the electric fields [29, 31]: The Dresselhaus contribution results from local electric fields as present in Zinc blende structures and has a prefactor specific to the material and z confinement [31]. In contrast, the Rashba contribution arises from structural inversion asymmetry introduced by asymmetric confinement potentials [29].

For electrons, the spin orbit splitting of the conduction band and the effective electron mass m_{eff} affect α_{SO}, the spin-orbit coupling constant [23, 58, 59]:

$$\alpha_{\text{SO}} = \frac{2\gamma_{\text{c}}}{\hbar^3}\sqrt{2m_{\text{eff}}^3 E_{\text{g}}} \tag{2.7}$$

With γ_{c}=1.62 eVÅ^3, the spin splitting coefficient, one obtains for ZnSe (group II-VI) α_{so}=0.021 [23]. In comparison, this coupling constant is slightly smaller than in other compound semiconductors such as CdTe (0.079, group II-VI)) and GaAs (0.067, group III-V), but significantly larger than in Si (group IV), where both the band gap and spin splitting are smaller [11, 21, 60, 61]. For 2D systems strongly confined along growth direction (001), the Dresselhaus Hamiltonian H_{D} reduces to the linear terms [31]

$$H_{\text{D}}^{2D,(001)} = \beta(-p_{\text{x}}\sigma_{\text{x}} + p_{\text{y}}\sigma_{\text{y}}), \tag{2.8}$$

where $p_{\text{x,y}}$ and $\sigma_{\text{x,y}}$ denote the momentum and Pauli-matrix, respectively. The prefactor β depends on the material and contains information on the confinement entering as $< p_{\text{z}}^2 >$.

The Hamiltonian H_{R} for Rashba SOI arising from the hetero interface asymmetry can be written as [31]:

$$H_{\text{R}} = \alpha(-p_{\text{y}}\sigma_{\text{x}} + p_{\text{x}}\sigma_{\text{y}}) \tag{2.9}$$

The prefactor α depends on the electric field E_{z} at the interface and material properties.

We are interested in the consequences of SOI for the proposed ZnSe/ZnMgSe target device. Firstly, regardless whether SOI originates from the Dresselhaus or Rashba effect, an electron moving ballistically in the 2DEG will experience a spin rotation forced by the internal magnetic field. The rotation angle is determined by the strength of the SOI and the distance traveled, and the distance resulting in a π-rotation is defined as l_{so}, the spin orbit length [31]:

$$l_{\text{so}} = \frac{\hbar}{\beta m_{\text{eff}}} \tag{2.10}$$

Here, β is defined as $g\mu_B B_{int}/v_s$ with the electron velocity v_s [8]. Experimental values for l_{so} in ZnSe are 21 µm and 2.1 µm determined for ZnSe bulk and a ZnSe QW, respectively [8, 23]. The layerstack of the referenced heterostructure is comparable to the one presented above but with $x_{Mg} = 8\,\%$ in the barrier and a QW width of 15 nm [23]. The values for l_{so} found in ZnSe compare well to l_{so} observed in GaAs QWs 1–10 µm [31, 62]. For a ZnSe QD smaller than the spin orbit length, which is given for the proposed architecture of the ZnSe/ZnMgSe EDQD device, no net spin rotations are expected [31]. Predictive spin rotations, which occur when shuttling over long distances, can be easily corrected [63].

Charge noise couples by spin orbit interaction to the electron spin and thus contributes to spin relaxation reducing T_1 [64]. An oscillating electrical field which effectively acts as induced magnetic field, drives spin rotations [65]. Regarding operation of spin qubits, especially Rashba SOI can be electrically tuned, as experimentally demonstrated in strongly confined system exhibiting large SOI like hole spins in Si FinFETs, one would expect similar tunability in ZnSe [66]. Strong SOI is beneficial for electrical qubit control, however gate fidelity gets compromised by charge noise coupling to the spin at the same time [66]. Whether or not this mechanism becomes relevant for ZnSe is highly speculative and will be the subject of future research.

We expect, a strongly confined electron in a QW with dot diameter well below the spin orbit length to be unaffected by spin rotations from the Dresselhaus (and Rashba) terms. Predictive spin rotations occurring for long range shuttling can be in principal corrected. One expects electrical tunability of SOI (direct Rashba SOI) and g-factor in strongly confined systems (such as nanowires or laterally confined QDs in a 2DEG) where electric dipole spin resonance (EDSR) becomes possible even without the need for micromagnets [66]. However, for qubit applications, increased spin relaxation resulting from charge noise mediated by SOI has to be balanced.

2.2.6. FREE MEAN PATH

One basic criterion for electron confinement to a QD or operation of SET or QPC is the mean free path l_{mfp}. As discussed above the relevant externally given length scale is the gate pitch roughly fixing the dot size l_{dot}. For $l_{dot} < l_{mfp}$ i.e. in the absence of scattering centers or potential variations introduced by charged defects the electron wave function i.e dot size or Fermi level can be well controlled by defining the dot potential applying a set of gate voltages. A large mean free path is thus desired for a predictable QD definition as required for fast tuning and scale up towards millions/billions of qubits. The relevant regime for qubits is a minimal carrier density since the qubit is in the charge ground state with only one electron. On a macroscopic level, the percolation threshold is experimentally accessible by a measurement of electron mobility in the limit of low carrier concentrations, utilizing the field effect in gated hallbar devices.

Regarding the device architecture, we require the desired gate pitch to be compatible with reproducible fabrication of nanostrucutre gates. In an academic setting, a gate pitch of 35 nm can be reached on group IV substrates with a two gate layer technique [63]. Since for single layers a comparable gate pitch has been reported for group IV and group III-V substrates, we are optimistic to fabricate our target device with nanostructure gates in one layer with a pitch of 70 nm on a III-V substrate [67–71]. To exclude ballistic scattering for the electron in the QD with extension of half the gate pitch, we require the mean free path to be way larger than the dot size, thus $L_{\mathrm{mfp}} \gg 35\,\mathrm{nm}$ [37]. For two qubit or shuttling operation, a very similar requirement can be formulated: Electron transport is required to be free of scattering events for a travel range equal to the interdot distance, twice the gate pitch for our device layout.

2.3. SUMMARY AND CONCLUSIONS

As a final note, we have proposed a target device for semiconductor spin qubits operating in a ZnSe QW. Motivated by physical requirements on electron confinement, we present an EDQD device with a specific 3D architecture. The operation principle and physical requirements are qualitatively described. Basic requirements on device operation, operation temperature, Ohmic contacts, thermal budget for fabrication, charge noise, spin orbit interaction and mean free path, to be considered in fabrication and characterization of (premature) devices are outlined. Prerequisite for exploration of all-electrical ZnSe based quantum devices is realization of a local Ohmic contact with low resistivity operating at 4 K to a ZnSe QW, not demonstrated so far, which represents a major challenge for this work.

3

LOW-RESISTIVITY OHMIC CONTACTS TO N-ZNSE

This chapter provides a coherent discussion on electrical properties of the electric contact to ZnSe and ZnMgSe crystals including large parts of a joint publication I co-authored [5].[1] To leverage the advantages of the ZnSe/(Zn,Mg)Se system for quantum device applications, the goal is to define locally doped Ohmic contacts. In specific, we target Ohmic contacts with linear IV characteristics and reproducible contact resistances of less than $1 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$ corresponding to a maximal contact resistance of $10\,\mathrm{k}\Omega$, operating at low bias and $T \leq 4\,\mathrm{K}$, as motivated in Sect. 2.2.

The chapter is structured as the following: State of the art fabrication techniques and resulting resistivities for Ohmic contacts to n-ZnSe are summarised in Section 3.1. The method used for quantitative characterization of contact resistivity is the transmission line model (TLM), outlined in Section 3.2.1. Different experimental approach-

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[1] The experimental work on Ohmic contacts was started by Alexander Pawlis, Johanna Janßen, Lars Schreiber and Arne Hollmann. Johanna Janßen provided prescreening of samples at RT. I joined the development one year after project start and participated in it proactively from that time on (coordination/supervision of RT/LT measurements, device fabrication). The selection of materials experimentally tested was taken by Johanna Janßen and Alexander Pawlis and Lars Schreiber based on the physics of a Schottky contact (Sect. 3.2). My main contribution was the electrical analysis of contact resistivity with a focus on low temperature performance. Implementation of a finite element solver (Sect. 3.2.2) helped to improve precision of our results on specific contact resistivity significantly (Sect. 3.4, 3.5). This work was supported by Malte Neul (setup of the solver, first simulation runs and fitting to data) and Till Huckemann (data acquisition, data analysis, literature research on TLM and comparison the solver). Lars Schreiber triggered the discussion of effective contact area and on the ratio of contact versus sheet resistance, which led to detailed investigations based on the TLM. The contributions are supplemented at the end of this chapter. Alexander Pawlis drove the development towards insitu doping and insitu metallization and insitu contacting insitu by local regrowth after my study of exsitu processing on insitu-doped samples did yield high spread of contact resistance (Ar milling, wet etching, in Sect. 3.4). Johanna Janßen started with implantation doping (Sect. 3.3.2) and insitu/exsitu contacts including annealing experiments, the ladder continued by her on exsitu and insitu contacts on insitu doped samples (Sect.3.3.1).

es for contact formation will be discussed including analysis of limiting effects. It is differentiated between contacts to various types of substrate (bulk or heterostructure) and device designs (planar or local doping), fabricated by the methods described in detail in Chap. 5.

Although electrical contact resistivity at $T \leq 4\,\mathrm{K}$ is the parameter of interest, prescreening of devices at room temperature is performed to filter out rectifying contacts. In total, different approaches for Ohmic contact formation to bulk ZnSe were tested, namely implantation, diffusion, epitaxial doping or selective epitaxial growth (regrowth), see Sections 3.3.2, Section 3.3.1 or Section 3.4.2, respectively. Hereby, Section 3.3 is separated into two parts: Firstly the contact properties of various contact metals on highly doped bulk n-ZnSe will be discussed while the second part addresses the importance of (oxide free) metal-semiconductor interfaces. To address local doping, I finally present a regrowth technique (patented [72]). The key ingredients are the best contact solution for bulk ZnSe combined with etching techniques and local doping by selective epitaxial growth. The chapter concludes with the presentation of results on Ohmic contacts to quantum well structures obtained by epitaxial doping and subsequent *in-situ* metallization, see Sect. 3.5 and a final discussion of all results.

3.1. STATE OF THE ART

Generally, low-temperature Ohmic contacts to n-type II-VI semiconductors are an unexplored field with sparse results so far. Most of the suitable metals lead to considerably high contact resistances already at room temperature: For example in n-type ZnTe several metals (Al, Mg, W, InHg) were studied in Ref. [73], the best performance was found for tungsten contacts yielding contact resistivities of $\sim 4 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$. For n-type CdTe slightly lower resistivities of $\sim$1-$2 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$ were achieved with in-diffused In contacts [74].

Typically, the contact resistance can be reduced by in-diffusion of the ohmic metals in a post-metallization annealing procedure [47]. In ZnSe, this approach is counterproductive, as this can lead to disordering related generation and diffusion of group-II vacancies to the ZnSe surface [75]. Laks et al. reported that Zn-vacancies form complexes with p-type conductivity in ZnSe [48]. Together with the efficient thermally induced diffusion these defects likely can compensate the n-type conductivity below the Ohmic contacts. Contact resistivities of $\sim$1-$5 \times 10^{-1}\,\Omega\,\mathrm{cm}^2$ are reported for ZnS using Indium alloyed with different metals [76]. Similarly, most of the suitable metals for ZnSe also lead to considerably high contact resistances exceeding $1 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$ (for In and Mg contacts [77]) and poorly linear current-voltage characteristics at low operating voltages. The lowest room temperature contact resistance ($3.4 \times 10^{-4}\,\Omega\,\mathrm{cm}^2$) has been observed with annealed Ti/Pt/Au contacts on highly Cl-doped ($2 \times 10^{19}\,\mathrm{cm}^{-3}$) n-type ZnSe [78]. In Refs. [79, 80], successful Ohmic contacts to a 2DEG in manganese doped ZnSe/ (Cd,Mn)Se heterostructures and superlattices was demonstrated by in-diffusion of Indium into the ZnSe. But in all these studies no

quantitative analysis of the contact performance especially at $T \leq 10\,\mathrm{K}$ is reported.
Contact resistivities are unacceptably high for n-ZnSe if not sophisticated fabrication routines for surface preparation are applied [77]. The regime of ohmic conduction is reached for highly doped n-ZnSe contacted after removal of surface oxide and optionally annealing of the contact [78, 80]. For diffused contacts to QWs, no quantitative analysis results on ρ_c for $T \leq 10\,\mathrm{K}$ are available in the literature. Still, transport characterization of II-VI heterostructures at $T \leq 10\,\mathrm{K}$ was possible. State of the art of fabricating Ohmic contact to ZnSe has only slightly changed since then when the research field was most active in development of optical devices emitting in the green and blue spectrum [81]. In diffusion contacts with large footprints incompatible with micro- or nanostructures were widely used to contact bulk samples and heterostructures. In-balls typically have a diameter of 100–200 µm prior to annealing at temperatures similar to the growth temperature for a few minutes, alternatively In contacts can be produced using a soldering iron. After annealing, i.e. soldering, the contact size is increased and can reach up to 500 µm. A significant reduction of the contact size is hindered by technical limitations of such manual processes and would require advanced machinery with a micromanipulator. With the large footprints described it is obvious In diffusion contacts are not compatible with scalable architecture, as discussed in Sect. 2.2.2 and cannot meet the requirements for Ohmic contacts with low resistivity at low temperature ($T \leq 4\,\mathrm{K}$). An alternative method used for n-type GaN is contact formation by surface doping based on out-diffusion of one crystal compound [81]. This approach cannot be transferred to ZnSe since the charge of corresponding p-type Zn vacancies has opposite sign. In turn, out-diffusion of the Se is possible, although less efficient, since Se is more stable than group II elements [53, 82].
Fabrication of Ohmic contacts to spin qubit devices poses another challenge. The main difference compared to contacting bulk layers is an undoped layer of semiconductor capping the conducting channel (QW). Gate control of the potential landscape in the QW is incompatible with high n-type doping in the qubit region due to screening of the gate voltage, see Chap. 2. Local doping can overcome unintentional screening when doping is restricted to contact regions laterally separated from the undoped qubit. Standard approaches for local doping are ion implantation utilizing an implantation mask or diffusion contacts. In the latter, donors are incorporated into the semiconductor in high concentrations by deposition of a metal or a metal stack and subsequent diffusion by annealing. Different mechanisms interplay, alloying and diffusion, resulting in an Ohmic contact to the QW [83]. Alternatively advanced nanofabrication offers a broad range of etching techniques enabling to contact the QW from the top or the side [83].

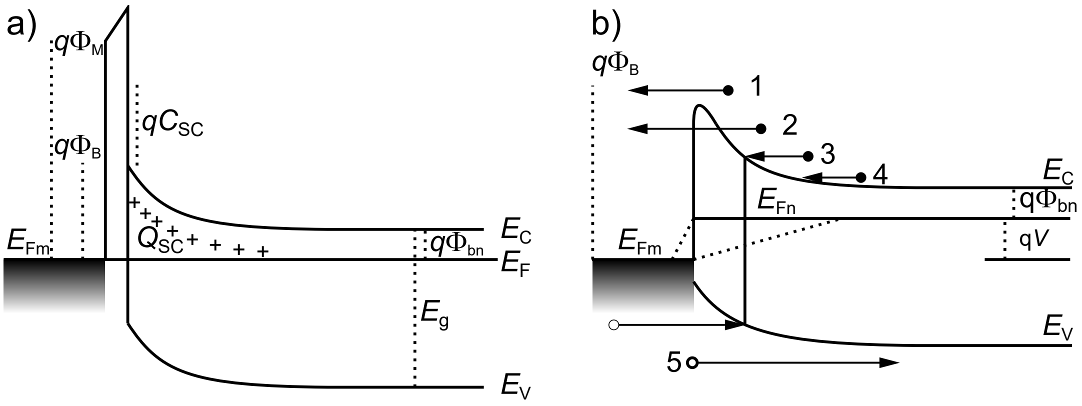

Figure 3.1: Schottky contact model and transport mechanisms. a) Schematic of the Schottky contact for n-type semiconductors. b) Transport mechanisms at the Schottky contact are thermionic emission (1), tunneling (2), recombination (3), and diffusion of electrons (4) or holes (5). Figure adopted from Ref. [84].

3.2. THEORETICAL DESCRIPTION AND CHARACTERIZATION METHODS

THEORY OF METAL SEMICONDUCTOR JUNCTION

A Schottky contact establishes when a metal and semiconductor are brought to contact. According to theory, the Fermi levels of both metal and semiconductor align in equilibrium [84]. As a consequence of charge neutrality, all charges in the semiconductor close to interface are distributed following the Poisson equation, see Fig. 3.1 a). The Schottky barrier height (SBH) Φ_B is then

$$\Phi_\mathrm{B} = \Phi_\mathrm{M} - \chi_\mathrm{SC}, \tag{3.1}$$

where Φ_M and χ_SC denote the work function of metal and electron affinity of the semiconductor, respectively [84]. Importantly, the Schottky model is only true in absence of interface charges. For this, a prominent example are metal induced gap states that effectively fix the Fermi level at a specific energy, an effect called Fermi level pinning [85]. In consequence, for real interfaces Eq. 3.1 is not always fulfilled and the SBH is affected by interface charges at the metal-semiconductor interface, which notably is sensitive to the fabrication process. ZnSe has an electron affinity of 4.09 eV and reasonable validity of the Schottky model is reported for this material [86–88].

Several charge transport mechanisms are possible at the metal-semiconductor interface, depicted in Fig. 3.1 b) for a n-type semiconductor [11, 84]. Not all mechanisms are relevant for this work targeting low resistivity Ohmic contacts operating at $T \leq 4\,\mathrm{K}$ in a low bias regime, as outlined in Chap. 2.2. Thermionic emission of electrons is small at small bias voltage and gets fully suppressed at $T \leq 4\,\mathrm{K}$. Recombination and diffusion of holes as minority charge carriers is negligible in highly doped semiconductors as present in the contact region. On the other hand, tunneling is independent of temperature and the corresponding resistance solely depends on the tunnel barrier. Deduced from the Schottky model the following aspects favour high tunnel currents [50, 88]:

A low Φ_B, a metal-semiconductor interface free of oxide, a shallow depletion zone equal to high carrier concentration and a semiconductor with low bandgap. Addressing these aspects, very low contact resistivities as low as $4 \times 10^{-8}\,\Omega\,\mathrm{cm}^2$ i.e for Erbium-Silicon corresponding to about $10\,\mathrm{m\Omega}$ for $100\,\mu\mathrm{m}^2$ square sized contacts can be achieved [89]. However, comparable contact resistivities for ZnSe are not possible for material specific physical limitations: ZnSe provides a high band gap of E_g =2.67 eV (RT) in combination with a lower maximum in carrier concentration, both not in alignment with the criteria formulated [50]. In addition, reduction of the tunnel barrier by annealing is incompatible with the available thermal budget discussed in Sect. 2.2.3. These restrictions set higher demands on the choice of the right contact material and fabrication processes.

From a theoretical point of view, lowest contact resistivities are expected for contacts with maximal substrate doping and minimal Φ_B, adjustable by selection of the metal with matching work function. The width of the tunnel barrier depends on the carrier concentration in the Wentzel–Kramers–Brillouin (WKB) approximation [90, 91]. The temperature stability of the contact resistivity is high for tunneling because the carrier concentration is independent of temperature for degenerate doping concentrations. Low SBHs (0.5–0.7 eV), determined by current-voltage (IV) and capacitance-voltage (CV) profiling, were reported for the contact materials Mg, Al and In, but still these results depend on experimental details [50, 87, 88]. A different method based on calculation of defect potentials in ZnSe:Cl leads to even lower values of 0.1 eV, when calibrated to the maximal carrier concentration in $Zn_{1-x}Mg_xSe$ [92, 93].

Apart from variations related to sample fabrication, the choice of the characterization method, IV or CV, can affect the FLP observed on the same samples by up to 50 meV [87, 88]. Ultimately, the most valid benchmark for specific contact resistivity are transport measurements, as presented in the next section.

CHARACTERIZATION AND ANALYSIS OF SPECIFIC CONTACT RESISTIVITY

This section points out the benefits and limitations of the methods deployed for electrical characterization of contacts. Here IV profiling and subsequent analysis based on the Transmission Line Model (TLM) is employed to disentangle substrate from contact resistivity.

Experimental IV data is interpreted using the TLM (Sect. 3.2.1) combined with finite element simulations (Sect. 3.2.2) where required. Complementary to IV profiling in 2- or 4-terminal configuration, van der Pauw Hall measurements can confirm the obtained resistivity. In principle, 2-terminal measurements as part of van der Pauw Hall measurements also probe the contact resistance, but with insufficient sensitivity, as separately discussed in Sect. A.2.

3.2.1. TRANSMISSION LINE MODEL

The validity of the TLM for application to metal contacts on ZnSe and the corresponding assumptions are discussed. A metal contact to a semiconductor substrate is schematically depicted in Fig. 3.2 a) and the related circuit diagram representation (Fig. 3.2 b). Early theoretical work has described this effect using the (extended) transmission line model (E)TLM by describing such a resistive network of nodes using conformal mapping [94, 95]. Both, the metal-semiconductor interface and the semiconductor are resistive, described by ρ_c and ρ_b, while the lateral metal resistance typically is negligible. In ETLM, the contact resistivity includes a resistive contribution from the substrate, see Fig. 3.2 c). Application of a bias voltage V to the contact results in a potential drop across the system and a corresponding current distribution. In the extreme cases of very high (low) contact resistivity at this interface layer an (in)homogeneous current distribution establishes. In the literature, the effect for such inhomogeneous current distributions is often referenced as current crowding, intuitively accounting for the inhomogeneiety with a maximal current density at the edge[2] of the contact [94].

The transfer length L_t is a useful parameter to describe the lateral voltage drop below a contact by a characteristic length scale. For a contact to a substrate of thickness t and bulk (sheet) resistivity ρ_b ($R_\mathrm{s} = \rho_\mathrm{b}/t$), one defines L_t as follows:

$$L_\mathrm{t} = \sqrt{\frac{\rho_\mathrm{c}}{R_\mathrm{s}}} \tag{3.2}$$

In lateral direction, the potential below the contact will drop to $1/e$ after L_t when moving from the edge to the center of the contact, as visualised in Fig. 3.2 d) in terms of normalised current density. For very long contacts compared to L_t the current distribution peaks at the contact edge, while it is more homogeneous for short contacts. Reduction of contact size (a) is in general preferable to reduce footprints of Ohmic contacts, limited by compromising R_c when a approaches L_t.

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[2] in lateral direction

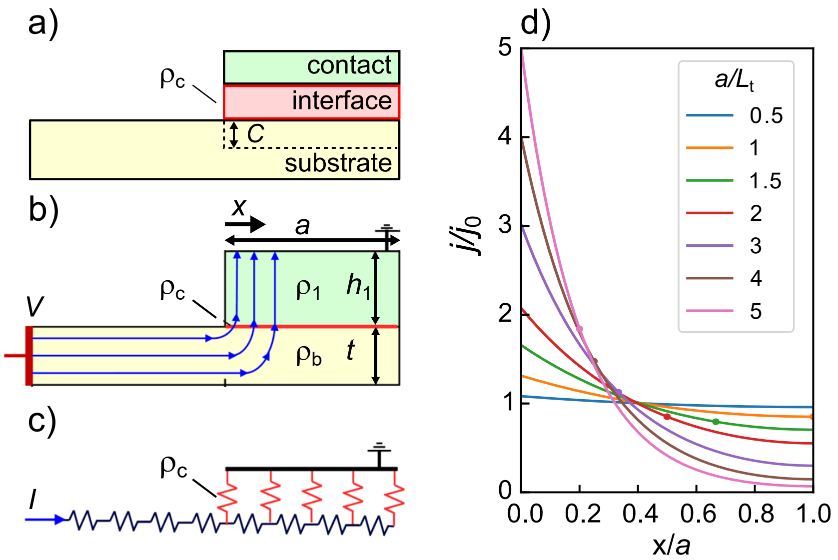

Figure 3.2: Extended transmission line model. a) Contact profile of the contact resistance for (E)TLM. ETLM accounts for an vertical potential drop in the substrate on a relative length scale C, effectively increasing contact resistivity. b) Exemplary solution for the electric filed in a contact with applied bias V. x denotes the lateral position starting at the contact edge [96]. c) Circuit diagram representation of (E)TLM with negligible metal resistivity. d) Normalised current density distribution j/j_0 below the contact for different degrees of current crowding parameterised as a/L_t. The x-coordinate of the dots corresponds to L_t. Figure adopted from Ref. [94, 96].

The total resistance R_tot of a TLM device defined on a mesa with contacts of the same width W separated by length L can be derived by [94]

$$R_\mathrm{tot}(L) = \frac{R_\mathrm{s}}{W} L + 2R_\mathrm{c} \tag{3.3}$$

$$R_\mathrm{c} = \frac{R_\mathrm{s} L_\mathrm{t}}{W} \coth\left(\frac{a}{L_\mathrm{t}}\right) \tag{3.4}$$

$$\lim_{a/L_\mathrm{t}\to\infty} R_\mathrm{c} = R_\mathrm{s} \frac{L_\mathrm{t}}{W}. \tag{3.5}$$

Expression Eq. 3.5 addresses sufficiently large contacts with $a >> L_\mathrm{t}$ where the coth approaches one. This approximation is valid with errors smaller than 0.5 % for $a > 3L_\mathrm{t}$, which is fulfilled for *in-situ* contacts on highly doped substrates as discussed later in this chapter.

With these approximations Eq. 3.3 transforms in the following way:

$$\begin{aligned} R_{\mathrm{tot}}(L) &= \frac{R_{\mathrm{s}}}{W} L + 2R_{\mathrm{c}} \\ &= \frac{R_{\mathrm{s}}}{W} (L + 2L_{\mathrm{t}}) \\ &= \frac{R_{\mathrm{s}}}{W} L + 2\frac{\sqrt{\rho_{\mathrm{c}} R_{\mathrm{s}}}}{W}. \end{aligned} \tag{3.6}$$

One can read from this representation, that twice L_{t} and twice R_{c} correspond to the intersects of the graph of $R_{\mathrm{tot}}(L)$ for $R_{\mathrm{tot}} = 0$ and $L = 0$, respectively. Both parameters give access to the physical properties ρ_{b} and ρ_{c} (final form of Eq. 3.6).

For ETLM, formally the same equations apply for the corrected parameters $\rho_{\mathrm{c,eff}}$ and $L_{\mathrm{t,eff}}$ [94]:

$$r_{\mathrm{c}} = \frac{\rho_{\mathrm{c}}}{\rho_{\mathrm{b}} t} = \left(\frac{L_{\mathrm{t}}}{t}\right)^2 \tag{3.7}$$

$$\rho_{\mathrm{c,eff}} = \rho_{\mathrm{c}} + C\rho_{\mathrm{b}} t = \rho_{\mathrm{c}} \sqrt{1 + \frac{C}{r_{\mathrm{c}}}} \tag{3.8}$$

$$L_{\mathrm{t,eff}} = t\sqrt{r_{\mathrm{c}} + C} = L_{\mathrm{t}} \sqrt{1 + \frac{C}{r_{\mathrm{c}}}} \tag{3.9}$$

Here, r_{c} relates the specific contact resistivity to the vertical resistivity in the substrate. Introduced in the ETLM, the vertical potential drop on length scale C (see Fig. 3.2) in the semiconductor leads to corrections for $\frac{r_{\mathrm{c}}}{C} >> 1$. In contrast, the TLM is valid for $\frac{r_{\mathrm{c}}}{C} >> 10$ [96]. In agreement with experimental work, $C = 0.19$ has been determined by conformal mapping [94, 97].[3] Since r_{c} is at least in the range of hundreds for ZnSe (see Tab. 3.6) the correction terms of the ETLM model, $\frac{r_{\mathrm{c}}}{C}$ in Eq. 3.8/3.9, can be easily neglected.

Physically interpreted, the approximations of TLM hold for the chosen contact design and contact properties, as the semiconductor can be described as a horizontal system, regardless of it's vertical structure [94]. For our experiments this is the case as substrate thickness is small compared to the contact length and the ratio of contact versus bulk resistivity is high.

For the following study of Ohmic contacts to n-ZnSe we denote the following: Characterization of contact pairs with increasing contact spacing (TLM structures) allows to experimentally disentangle contact and sheet resistance, according to Eq. 3.3. Further the TLM provides a method to assess physical properties of the metal-semiconductor contact, ρ_{c} and ρ_{b}, sufficiently well. Finally, the related L_{t} gives an intuitive impression on the effective dimension of the contact. The use of the ETLM does not

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[3] The theoretical value for C is $(\ln(4)/\pi)^2$, according to the nomenclature of [94] which accounts for a single contact.

improve accuracy compared to the TLM, since the approximation of a thin, resistive semiconductor layer is a valid description within this work, and is therefore not considered further. This toolbox for investigation of the metal-ZnSe contact interface is completed by electrostatics simulations of 3D devices.

3.2.2. FINITE ELEMENT SOLVER FOR RESISTIVITY ASSESSMENT

As outlined above, the physical parameters of interest, contact and bulk resistivity are to be extracted from experimental data $R_{\mathrm{tot}}(L)$ using the TLM. However, for non-uniform current transport perpendicular to the bias gradient Eq. 3.6 based on the TLM cannot be applied. In some special cases, conformal mapping can account for deviations from uniformity [95]. Here, without compromising flexibility, we employ a finite element solver to account for the full 3D nature of the devices concerned. The device profile is implemented as a stack of contact, interface and substrate layer, see Fig. 3.2 a). Typical input parameters of the solver are given in Tab. 3.1. For technical reasons, the resistive interface is implemented with a finite thickness t_{i} and bulk resistivity ρ_{b} related by

$$\rho_{\mathrm{c}} = \rho_{\mathrm{b}} / t_{\mathrm{i}}. \tag{3.10}$$

Table 3.1: Typical input parameters of the finite element solver. Left columns: Given input values for modelling a low resistivity contact (Al *in-situ*) on highly doped bulk ZnSe substrate ($n \sim 1 \times 10^{19}\,\mathrm{cm}^{-3}$). The given values correspond to device dimensions (t), or literature values (ϵ_{r}, ρ_{b}), except the estimated values of the interface layer. Right columns: Related parameters derived from the input.

layer	t (nm)	ρ_{b} ($\Omega\,\mathrm{cm}$)	ϵ_{r}	R_{s} ($\Omega/\square$)	ρ_{c} ($\Omega\,\mathrm{cm}^2$)	r_{c}
metal	100	3×10^{-6}	inf.	0.3		
interface	10	100	10	1×10^{8}	1×10^{-4}	330
substrate	1000	3×10^{-3}	8.6 [98]	30		

Here, t_{i} is set to 10 nm which is in the upper range for realistic metal semiconductor interface layers (1–10 nm) and large enough to be correctly modeled by the solver [94]. Two metal contacts biased with 1 V are modeled as materials with a resistivity multiple orders of magnitude lower compared to the substrate. In this configuration, the sheet resistance is several orders of magnitude higher for the interface compared to the semiconductor substrate.[4] Physics related meshing ensures a lateral resolution smaller than L_{t}. As a result of the full 3D geometry of the modeled devices, the output is non-linear with device dimensions, as discussed later in this chapter. The next paragraph presents the capabilities of the solver in the given configuration.

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[4] Example for 1 µm thick, highly doped ZnSe sample with Al in-situ contact, see Fig. 3.10: $\rho_c = 2.3 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$; $R_{\mathrm{s,c}} = 2.3 \times 10^{7}\,\Omega/\square$; $R_{\mathrm{s,ZnSe}} = 39\,\Omega/\square$. Ratio for sheet resistivities is 6×10^{5}.

VERIFICATION OF THE FINITE ELEMENT SOLVER FOR EVALUATION OF CONTACT RESISTIVITY

For a given device geometry, a solution to the electrostatics problem is calculated by the finite element solver with a sufficient precision. As an example, the current density distribution in the resistive interface layer and in the substrate is shown in Fig. 3.3 a) and b), respectively. The solution is continuous and resolves lateral features down to a scale of 2 µm. Current density in the interface layer is highest where the contacts are connected to the mesa channel, see Fig. 3.3 a). Accordingly, the current distribution of the contact region is transferred into the substrate, where the highest levels are reached in the elongated mesa channel, see Fig. 3.3 b). As a result of boundary effects, strongly confined peaks in current density establish at the corners of the mesa channel (red dots in Fig. 3.3 b).

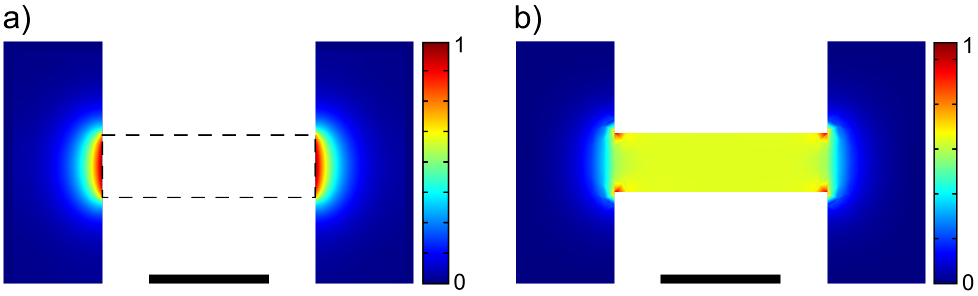

Figure 3.3: Exemplary solution of the finite element solver used for evaluation of contact resistivities. a) Current density (arbitrary units) at the metal-semiconductor interface depicted for a device with two contacts separated by a semiconductor channel (dashed lines). b) Current density (arbitrary units) in the semiconductor substrate. Scale bar is 100 µm and bias voltage is 1 V. A commercial finite element solver is used [99].

To test the functionality of the finite element solver, a parameter study for a TLM device without mesa etched channel is performed, see Fig. 3.4. Successful operation over a wide range of input parameters including the physically relevant regime is demonstrated, as well as for various contact spacings and geometries with and without mesa (discussed below in Sect. 3.4, see Fig. 3.10 and Fig. 3.12). As desired, the output in terms of total device resistance is linear in either ρ_c or ρ_b in extreme cases (dashed lines in Fig. 3.4). In an intermediate regime the output is non-linear, as the sheet resistivities of interface and substrate layer are comparable.

Quantitative agreement of the solver output in the given configuration with physical observables is identified for a specific parameter set (star in Fig. 3.4): Experimental data for *in-situ* deposited Mg contacts (R_{tot} =10 Ω) match the simulated resistance. The data point is in the region close to the diagonal axis (r_c = 100 or L_t=10 µm). Since $r_c \gg C$ and L_t is smaller than the contact dimensions, the TLM is a valid description.

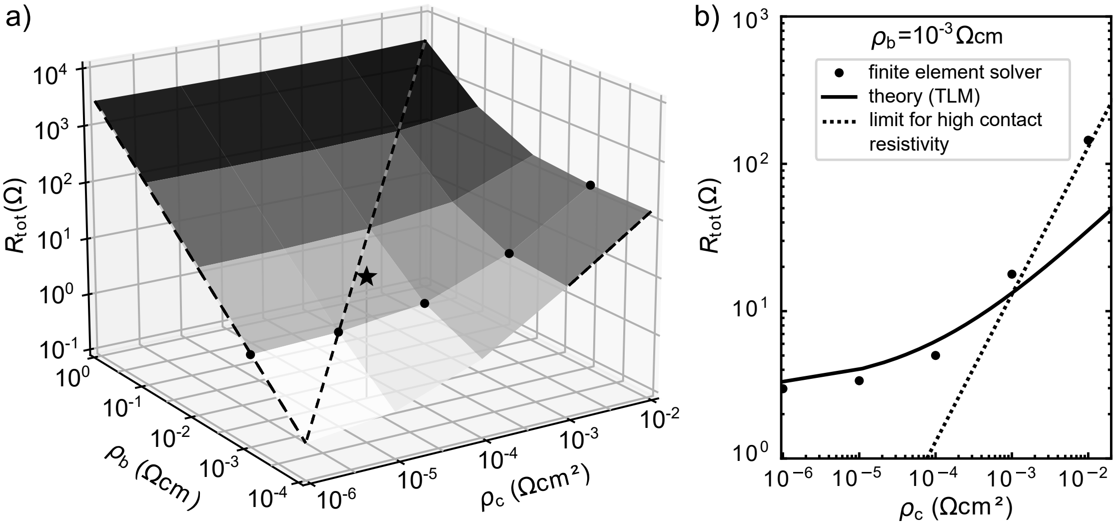

Figure 3.4: Evaluation of the finite element simulation. a) Simulated device resistance (grid points) in dependence on bulk and contact interface resistivity in logarithmic representation. Grey scale color coding serves as guide to the eye. The modeled TLM device consists of two 75x190 µm sized contacts spaced by 100 µm on a 1 µm thick substrate without mesa confinement. Dashed lines highlight linear dependencies. The star corresponds to experimental data of *in-situ* deposited Mg contacts. b) Comparison of simulated (device without mesa) and theoretical results (device with mesa) for ρ_b fixed at $1 \times 10^{-3}\,\Omega\,$cm.

With increasing contact resistivity ρ_c a continuous transition from negligible to dominating contribution of the contact resistance can be modeled, reproducing the theoretical predictions of the TLM [94]. This can be verified in Fig. 3.4: The output is almost independent on contact resistivity to the left of the diagonal axis in Fig. 3.4 a) as the device resistance is governed by the resistivity of the substrate, see Eq. 3.5. In contrast, far right of the diagonal axis, the contact resistance is proportional to ρ_c. For a detailed comparison the simulation is compared to theory, see Fig. 3.4 b). Input to the TLM are device dimensions as used for the solver, however for a device with simplified geometry without mesa. We find quantitative agreement with theory (solid line) and simulation (dots), and attribute the deviations observed to geometric effects not covered by the TLM. We note a transition from overestimation to underestimation for the TLM: First, this finding is in agreement with TLM overestimating R_c and hence R_{tot} due a current path restricted by the mesa. Second, as L_t approaches the dimensions contact, assumptions of the TLM break down and $R_{tot}(\rho_c)$ transitions from a square root to a trivial linear dependence (dotted line).

We have demonstrated the solver being capable of operation for all levels of spreading resistance, especially in the TLM regime. Given the consistency of theory, simulation and experiment in the relevant parameter space, the solver will be used in the following for assessment of specific contact resistivity.

3.3. OHMIC CONTACTS TO ZNSE OPERATING AT LOW TEMPERATURE

Formation of low resistivity Ohmic contacts to bulk ZnSe and ZnSe heterostructures is discussed in this section. For assessment of specific contact resistivityIV profiling in the framework of the TLM is used. Goal is demonstration of a low resistivity contact to ZnSe (ZnSe/ZnMgSe heterostructures) compatible with requirements of qubit operation at $T \leq 4\,\mathrm{K}$. Expressed in numbers, the target contact resistance is chosen as $10\,\mathrm{k\Omega}$ at a temperature of $T \leq 4\,\mathrm{K}$, see Chap. 2. Contacts are electrically precharacterised at room temperature prior to measurements at cryogenic temperatures. Contacts of insufficient performance at room temperature, namely high tunnel resistances, are excluded from characterization at $T \leq 4\,\mathrm{K}$.
To reach the desired contact resistance in contact formation, different approaches are tested since ZnSe exhibits several material specific challenges. Optimization of the metal-semiconductor interface with desirable low SBH is addressed by reduction of interface oxide, increasing of semiconductor doping concentration and choice of metal with suitable work functions. While this section focuses on the interpretation of experimental results, details on the fabrication processes based on diffusion, implantation, epitaxial doping, metallization (in-situ or ex-situ) and regrowth can be looked up in Chap. 5.

3.3.1. DIFFUSED CONTACTS TO II-VI SUBSTRATES

DIFFUSION CONTACTS TO BULK ZNSE AND BULK ZNMGSE

Typically, ZnSe is contacted by diffusion of the contact material into the semiconductor. The relevant mechanisms are surface dopants by introduction of free carriers and alloying below and at the metal-semiconductor interface [83]. Thermally activated ($T \geq 200\,^{\circ}\mathrm{C}$) diffusion of In into ZnSe results in specific contact resisitvities in the range of $0.05\,\Omega\,\mathrm{cm}^2$ [49]. Within this work, the In diffusion method was chosen for contact formation to both doped and undoped ZnSe and ZnMgSe substrates, enabling fast turnaround material characterization. In agreement with literature, contact resistivities in the order of $0.01\,\Omega\,\mathrm{cm}^2$ were found for ZnSe. Higher resistivities are expected for ZnMgSe since introduction of Mg increases the band gap energy and presumably thereby the SBH. In qualitative agreement with theory, we find increased contact resistivity of about $1\,\Omega\,\mathrm{cm}^2$ for highly doped ZnMgSe samples, further increasing with carrier density reduction in undoped samples (data not shown). In the following paragraph, the compatibility of diffusion with contacting the target II-VI heterostructure will be discussed.

DIFFUSION CONTACTS TO (UN)DOPED ZNSE QWS

Next, we address the question whether contact formation by In diffusion is still possible if the II-VI bulk substrate is replaced by a II-VI heterostructures hosting a QW. Main difference is the introduction of a ZnMgSe layer between conducting channel (ZnSe QW) and the contact layer, which could act as diffusion barrier or as additional potential barrier. Building on the TLM described above, the contact resistance further includes a contribution of the II-VI heterostructure. The vertical resistance and interface resistance for the II-VI heterointerface can be neglected since electrons provided by the contact can enter the QW by tunneling to the ground state (see Sect. 2/Fig. 2.2). This requires a doping concentration in the ZnMgSe that is above the MIT ($n_{\mathrm{MIT}}^{ZnMgSe}$=$7\times10^{17}\,\mathrm{cm}^{-3}$, see Sect. 4). Further, the vertical resistance in the upper barrier is expected to be small due to the small travelling distance (30 nm) and moderate carrier concentration in the ZnMgSe barrier of $n=5\times10^{17}\,\mathrm{cm}^{-3}$ slightly below the MIT.[5]

Here, I will discuss the limitations of the In diffusion process for contact formation: For a given ZnSe QW structure, optimal parameters for contact formation are to be identified. We use a doped ZnSe QW occupied by electrons in the ground state (see Chap. 2), effectively mimicking an accumulated charge carrier concentration in the QW as relevant for the final device. With a sheet resistance of the heterostructure of a few kΩ/□ at RT, contact resistances below the target value of 10 kΩ are aimed at.

For two contact types, In-balls and In contacts evaporated *ex-situ*, the annealing process is to be optimised by means of two free parameters: Temperature T and annealing time. Stronger, exponential influence of T is expected on diffusion versus linear effects in time. Fig. 3.5 shows experimental data for annealing of both contact types, for In-balls contacts and In *ex-situ* contacts in panel a) and b-d), respectively. Our annealing experiments are performed in forming gas atmosphere combined with HCl gas flow used for oxide removal during heat up.

Annealing, which promotes diffusion in the crystal lattice, leads to p-type Zn vacancy generation diminishing the net n-type carrier concentration, as observed for elevated temperatures > 200 °C (Sect. 3.3.2) [48]. Without growth conditions, i.e. in absence of partial Zn and Se pressure, we allocate the thermal budget below 250 °C,[6] which is lower than the growth temperature T =270 °C. Again, we indirectly observe out-diffusion of Zn as opposing effect simultaneously with diffusion of In at temperatures far below the growth temperature of 270 K, see Fig. 3.5.[7]

Fig. 3.5 a) depicts resistances for In ball contacts diffused for a few minutes at different temperatures. We correlate the variation in observed resistances on the same sample (indicated by color) to a lack of process control and reproducibility. In a sim-

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[5] $R_{\mathrm{c,vert}}$ =300 Ω (30 K) per contact estimated from resistivity data of typical sample, influenced by the transfer length of the contact system. For large contacts this value will adjust to be comparable to R_{S}.

[6] This temperature corresponds to the lowest annealing temperature probed.

[7] We also evidence out-gassing of Zn and related p-type vacancy generation for epitaxially (non-invasively) doped substrates, see Apx. A.3.

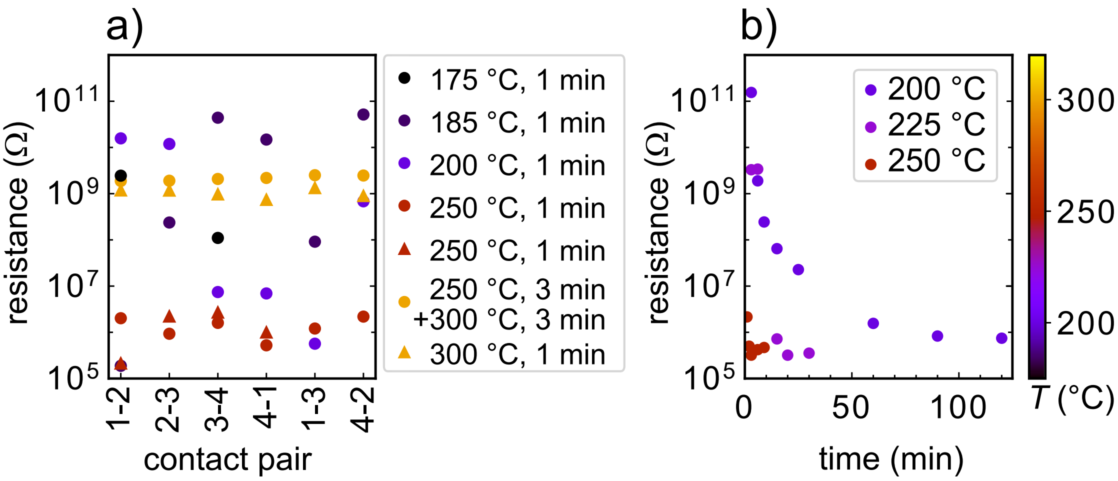

Figure 3.5: In *ex-situ* diffusion contacts to a II-VI heterostructure. Electrical characterization at RT of In *ex-situ* contacts formed by processes as indicated. a) Device resistance for In ball diffusion contacts annealed at different temperatures for one minute at target temperature. One sample (yellow dots) was annealed in two steps at 250 °C and 300 °C for 3 min each. Devices are sized $5\times5\,\mathrm{mm}^2$. The four contacts at the corners are sized $\sim 200\times200\,\mu\mathrm{m}^2$. b) Time series for diffusion process on *ex-situ* deposited In contacts at various temperatures. The experiment was stopped as subsequent annealing did not further reduce the device resistance. The TLM contacts of size $190\times75\,\mu\mathrm{m}^2$ are spaced by 180 µm. Measurement by Johanna Janßen. Analysis results are listed in Tab. 3.2.

ple picture, the absolute substrate resistance for the squared samples used is $R_s \cdot \square$, which is to be down-corrected by a geometry factor (~ 2-3) accounting for the configuration of terminals. The observed resistances are dominated by the contact resistances, since the observed spread of total resistances is high and orders of magnitudes larger than the substrate resistance. This conclusion we confirm by *IV* profiling where we find $R_s = 9 \pm 2\,\mathrm{k}\Omega/\square$ for a sample annealed twice for one minute at 250 °C (Apx. A.7). The sheet resistance was deduced using TLM based on differential resistances determined at ±3.5 V bias.[8] Furthermore, R_s is not altered by annealing at 250 °C for 3×1 min as verified for similar substrates with a doped QW (Apx. A.3). As a result, we obtain minimal contact resistances for a temperature of 250 °C of about 100 MΩ ($\rho_c \sim 100\,\Omega\,\mathrm{cm}^2$).

Higher or lower process temperatures further increase contact resistivity by several orders of magnitude. For high temperatures (300 °C) existence of a destructive mechanism attributed to outgassing of Zn and thereby creation of positively charged Zn vacancies in the substrate is deduced, compare also Sect. 5.5. A more detailed study

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[8] The resistance of a rectifying contacts drops significantly when operated in the in the breakdown regime reached for voltages above 2 V.

Table 3.2: *Ex-situ* diffused In contacts to II-VI substrates with doped QW. Overview of analysis results corresponding to the experiment shown in Fig. 3.5. Upper part: Values listed for 250 °C correspond to data plotted as red dots in Fig. 3.5 a). Lower part: Values for the minimal resistance and related annealing time t are listed for a given annealing temperature corresponding to Fig. 3.5 b). R_s are expectation values based on growth parameters and a van der Pauw Hall measurement. A homogeneous current distribution below the contacts is assumed for evaluation of ρ_c.

T (°C)	t (min)	R_c (Ω)	R_s ($\Omega/\square$)	ρ_c ($\Omega\,cm^2$)	L_t (µm)
		panel a	design	v.d.P. Hall	
175	1	5×10^7–2×10^9	1×10^4	2×10^4–8×10^5	1×10^4–9×10^4
185	1	1×10^5–2×10^{10}	1×10^4	4×10^1–8×10^6	6×10^2–3×10^5
200	1	3×10^5–1×10^{10}	1×10^4	1.2×10^2–4×10^6	1×10^3–2×10^5
250	1	3×10^5–1×10^6	1×10^4	1.2×10^2–4×10^2	1×10^3–2×10^3
300	1	1×10^9–2×10^9	1×10^4	4×10^5–8×10^5	6×10^4–9×10^4
		panel b	design	TLM	
200	120	3×10^5	1×10^4	4×10^1	6×10^2
225	20	1×10^5	1×10^4	1×10^1	3×10^2
250	3	1×10^5	1×10^4	1×10^1	3×10^2

of the diffusion process is presented in Fig. 3.5 b-d) for optimised conditions identified in the pre-study[9]. The annealed TLM structures of *ex-situ* deposited In contacts exhibit a better resistance level for the 200 °C anneal in the limit of long process time, compared to the value obtained for 250 °C after few min, see Fig. 3.5 b). In this low temperature (T=200 °C) regime, no destructive effects are observed since R_c continuously drops over the process time, saturating on a time scale of hours. Contact separation linked to sheet resistance does not affect the measurement outcome since R_c still dominates. For higher process temperature (T=250 °C) R (R_c) saturates quicker at the scale of minutes to a similar level, in agreement with thermally activated diffusion. However, for $T \geq 6$ min an increase in R (R_c) is observed presumably as a consequence of p-type Zn vacancy generation by Zn outgassing [48].

We note the desired optimum for R_c is not reached since experimental results deviate from expectation by a factor of 100 under optimised conditions (10 kΩ targeted vs. 150 kΩ observed). At cryogenic temperature R_c is expected to further increase as charge carriers in the contact region freeze out. Already at RT, the specific contact resistivity of 100 $\Omega\,cm^2$ observed in this study is incompatible with the target of $\rho_c < 1 \times 10^{-2}\,\Omega\,cm^2$ (Sect. 2.2). In comparison, ρ_c determined for In diffusion contacts to highly doped QWs is four orders of magnitude higher at RT compared to bulk ZnSe [49]. The discrepancy suggests an efficient suppression of In diffusion to the ZnSe

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[9] Differences of contact geometry and metallization process can be neglected since the resistivities compare well for both studies.

QW by the 30 nm thick ZnMgSe barrier. Notably, similar contact resistivity is known for undoped ZnMgSe, as discussed above in Sect. 3.3, underlining that the ZnSe QW is effectively decoupled from the contact metal.

To conclude, a process window for In diffusion contacts to undoped ZnSe/ZnMgSe heterostructures is identified and experimentally studied for annealing processes within and beyond the thermal budget ($T \leqq$200–250 °C). The process window found represents a trade-off for two processes with opposing effects on contact resistivity, In diffusion in ZnMgSe and outgassing of Zn. Even under optimised conditions, contact resistivities found do not fulfill the requirements. Mg content, barrier thickness and absence of p-type dopants[10] all counteract diffusion. All three aspects represent requirements (Chap. 2.2) identified for qubit fabrication that in consequence prohibit diffused Ohmic contacts to heterostructures with undoped barrier. Limitations of the contact resistivity are low diffusion rates in undoped ZnMgSe and thus high tunneling barriers preventing Ohmic contact formation. In contrast, the next paragraph covers how the contact resistivity can be reduced when introducing a finite charge carrier concentration to the barrier.

For this study of In diffusion contacts on epitaxially doped substrates the standard process for In diffusion was used (see Chap. 5). Cl doping concentration is chosen above, or at least close to n_c of the MIT. Three different substrates types are considered, bulk ZnSe, bulk ZnMgSe and a ZnMgSe heterostructure. In the case of ZnSe, temperature stable transport characteristics are determined in van der Pauw Hall measurements, as expected for degenerate doping concentrations above n_c, see Fig. 3.6. The normalised bulk resistivity shown behaves similarly as the differential resistance of the entire device, indicating a negligible contribution of the contact resistance. The ZnSe crystal exhibits high crystalline quality deduced from van der Pauw Hall measurements: Resistivity is optimal and mobility of 180 $\mathrm{cm^2/Vs}$ is high, only limited by scattering at charged Cl donor impurities at almost maximal doping concentration of $1.3 \times 10^{19}\,\mathrm{cm^{-3}}$.[11] Ohmic contact resistivity is lower than the measurement sensitivity of $0.02\,\Omega\,\mathrm{cm^2}$, demonstrating efficient contact formation by In diffusion to highly doped bulk ZnSe:Cl with a low tunnel resistance independent of temperature. As Mg is introduced to the system, the transport characteristics become dependent on temperature, in contrast to degenerately doped ZnSe:Cl, see data in red and black in Fig. 3.6. Although the doping concentration is above n_c, charge carrier concentration is not stable with temperature. Also, mobility decreases with T assigned to Anderson localisation (Chap. 4). The transport characteristics are discussed in more detail in Chap. 4. Here, the focus is on the differential resistance slightly deviating from the trend of the sheet resistance towards low temperature.

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[10] By a Fermi level shift introduced by p-type dopants, the so called Fermi-Effect, diffusion can be significantly enhanced [53].

[11] PL results reveal presence of deep defect levels at about 2 eV pointing at onset of compensation as consequence of a high doping concentration.

The discrepancy is attributed to the contact resistance becoming more important for lower temperature. The nature of the In diffusion contact to ZnMgSe has less contribution from tunneling, as demonstrated for ZnSe:Cl in Fig. 3.6).

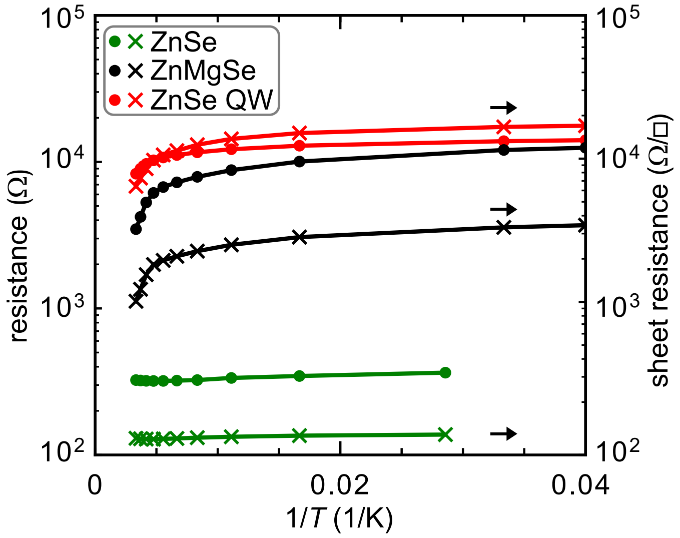

Figure 3.6: Comparison of device resistivities for different substrate types contacted by In diffusion. Differential resistance for bulk ZnSe (green) in comparison to bulk ZnMgSe (black) and a ZnSe QW in a ZnSe/ZnMgSe heterostructure (red). Circles and crosses correspond to device resistance and sheet resistance, respectively. All materials are highly doped with n about $1 \times 10^{19}\,\mathrm{cm}^{-3}$ and $1 \times 10^{18}\,\mathrm{cm}^{-3}$ for ZnSe and ZnMgSe, respectively. In case of the heterostructure, the lower buffer and barrier are undoped. The arrows indicate the corresponding axis for the sheet resistance. Measurement by Johanna Janßen and Nils von den Driesch.

In addition, electrical characteristics of In diffusion contacts to a QW structure are shown. Resistances increase with inverse temperature, but differently for the bulk versus entire device resistance. The discrepancy arises from the contact resistance to ZnMgSe barrier decoupled from bulk resistance that is dominated by the ZnSe QW. The resistivity of the QW structure can be interpreted as superposition of all effects present for bulk ZnSe bulk and bulk ZnMgSe.

In consequence, the contact resistance to the heterostructure with ZnSe QW is determined by ZnMgSe carrier concentration prone to freeze out. In principal, low contact resistivity can be realised ($\sim 0.01\,\Omega\,\mathrm{cm}^2$), enabling also contacts operating at $T \leq 4\,\mathrm{K}$, but at the cost of non-deterministic diffusion and adherence to the thermal budget constraint [77].

Further compatibility with qubit fabrication is restricted due to small thermal budget of the fabrication process amplified by poor compatibility with cleanroom processing. Further In is not compatible with standard cleanroom processing.[12]

3.3.2. CONTACTS TO FLUORINE AND CHLORINE IMPLANTED ZNSE

The contact resistance of contacts to semiconductors can be substantially reduced by the local enhancement of the free-carrier concentration in the semiconductor below the contact metal also in alternative ways to non-deterministic diffusion. In various material systems, efficient local doping was achieved by ion implantation [100–102]. Since the halogenides are prominent n-type dopants for II-VI semiconductors (Ref. [103] and references therein), we investigated the conductivity of ZnSe layers that were implanted with F or Cl. The heavier halogen Br is no relevant n-type donor due to formation of compensation centers under Br incorporation [104].

We performed the ion implantation into ZnSe with varying implantation energies and doses as shown in Tab. 3.3. These implantation parameters were estimated on the basis of stopping and range of ions in matter (SRIM) simulations: Firstly, we have chosen a maximum doping concentration of about 10^{19} cm^{-3} for comparison of all samples. Secondly, the implantation energy was adjusted to achieve the same penetration depth profiles for samples B and C. The latter were implanted with F and Cl, respectively, using only one implantation run. Furthermore, significantly lower implantation energies were chosen to minimise implantation damage. Alternatively, in sample A, Fluorine ions were implanted with three implantation runs with different energies and corresponding doses. These parameters allow to achieve a homogeneous doping profile in the order of 10^{19} cm^{-3} within a region of ~ 250 nm below the surface.

SRIM simulations (dashed lines) and quantified datasets (solid lines) from scattering ion mass spectroscopy (SIMS) of samples B and C are shown in Fig. 3.7 a). The

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[12] In does not form closed layer introducing adhesion problems or related underetching. Further In with high evaporation pressure is not compatible with dielectric deposition by CVD, also macroscopic In-balls are not compatible with low footprint qubit architecture.

Table 3.3: Overview of the implanted ZnSe samples used for our studies. Sample A was implanted with three different implantation runs to obtain a homogeneous doping profile below the contacts. Samples B and C were implanted only once to reduce implantation damage. The ion energies and doses were adapted to achieve the same depth profile for both ion species.

sample	ion	energy (keV)	dose (cm^{-2})
A	F$^-$	110	4×10^{14}
		50	1×10^{14}
		20	6×10^{13}
B	F$^-$	20	2×10^{14}
C	Cl$^-$	40	1.2×10^{14}

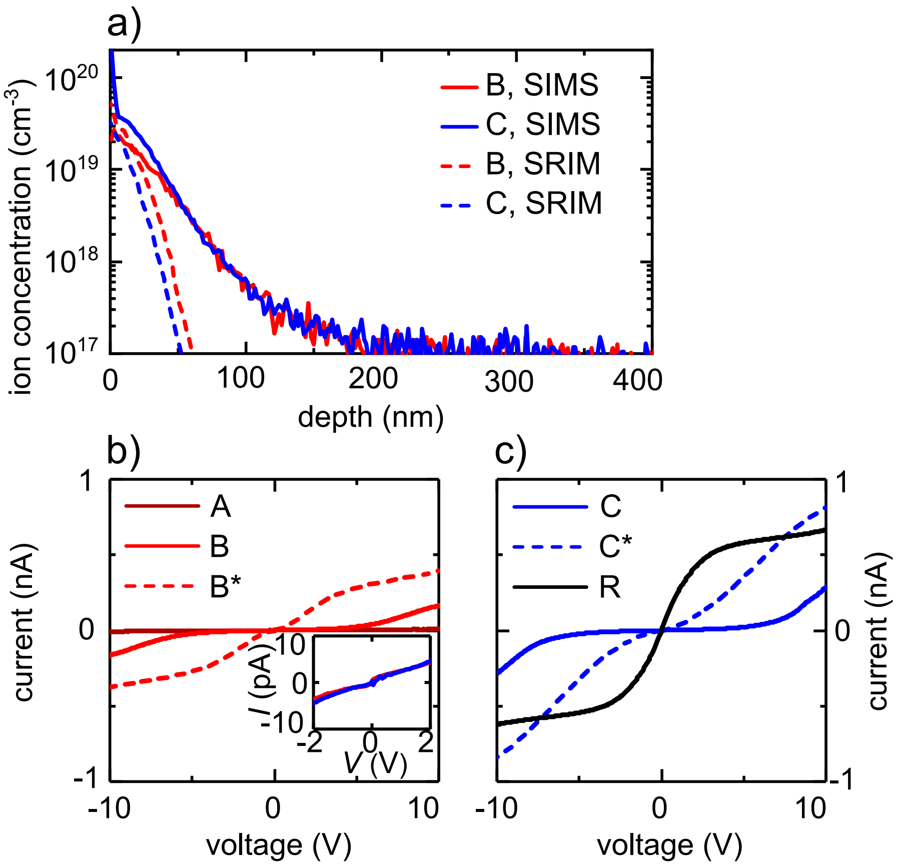

Figure 3.7: Contacts with local doping by implantation. a) Quantified SIMS depth profiles (full curves) and corresponding SRIM simulations (dashed lines) of the ion concentration in the samples B and C. b,c) IV curves obtained from implanted ZnSe samples. While different ion implantation parameters were used, all samples were measured with *in-situ* deposited Al contacts and 30 µm contact spacing. The asterisk marks annealed pieces of the samples. a) F implanted samples (A, B, B*). b) Cl implanted sample (C, C*) and undoped reference sample (R). The inset in b) represents an expanded view of the IV curves obtained from sample B and C for direct comparison at small voltages. Figure by Johanna Janßen [5, 105].

SIMS profiles were obtained from the as-grown samples implanted under a tilt angle of 7° (Sect. 5.3) without any annealing treatment. Note that the depth profiles of both samples are nearly the same as we intended with the parameter sets obtained from the preceding SRIM simulations. Experimental and simulated ion concentrations are in good agreement especially close to the surface, ignoring interface related measurement artefacts of SIMS within the first 5 nm. However, the calculated penetration depth at which the concentration drops to $1/e$ of its maximal value is about 15–20 nm, while that measured by SIMS is larger (about 30–40 nm for both ion species) due to substantial ion channeling.

Electrical properties of contact and bulk material are accessed experimentally by IV profiling at a needle probe station under ambient light conditions at RT. The electrical measurements for the samples listed in Tab. 3.3 are depicted in Fig. 3.7 b,c). Although we measured IV characteristics for TLM structures with contact distances between 30 µm and 180 µm, no contact spacing dependent splitting of the curves was observed. The absence of such a dependence indicates a predominance of the contact resistance over the bulk resistance. For each of the implanted samples, the results obtained for $L = 30\,\mu\mathrm{m}$ channel length are presented in Fig. 3.7 b,c).

The common feature of the curves of all implanted samples is the high total resistance in the order of $10^{11}\,\Omega$ to $10^{12}\,\Omega$ especially at low voltages. Considering the contact area, one deduces ρ_c in the range of 1×10^{7}–$1\times10^{8}\,\Omega\,\mathrm{cm}^2$, magnitudes higher than the requirements. Moreover, a severe nonlinearity of the IV curves in Fig. 3.7 b,c) is observed and reveals the presence of multiple current blocking regions below the contacts of all samples. Over the entire voltage range, the lowest current is measured in case of sample A which results from the severe implantation damage probably inducing Zn vacancies to this sample within the three implantation runs [106, 107]. A reduction of the implantation energy (sample B) distinctly increases the currents for voltages $> 5\,\mathrm{V}$, however, the resistance around 0 V is only slightly decreased.

The change from F to Cl ion implantation (sample C) further improves the IV characteristics at higher voltages, while the resistance around 0 V is similar to that of sample B. Although the Cl implantation was performed at higher acceleration voltages (Tab. 3.3), the conductivity of the samples is not further reduced. The latter indicates that Cl ions more efficiently compensate the effect of implantation damage than F ions. However, for reference, we measured an undoped and unimplanted sample R, which exhibits a remarkably improved IV characteristics and an about two orders of magnitude reduced resistance of approximately $3\times10^{9}\,\Omega$ around 0 V. This demonstrates that the implantation damage on the atomic lattice exceeds the benefits of doping ZnSe by Cl and F implantation.

First-principles total-energy calculations performed by Laks et al. [48] suppose that Zn vacancies form acceptors in n-type ZnSe. Moreover, there is strong experimental evidence for generation of acceptor type Zn vacancies by F or Cl implantation [106, 107]. Therefore, we conclude from the observed IV characteristics in Fig. 3.7 b,c) that our implantation technique leads to the formation of these Zn vacancies. The highest concentration of such defects is most likely located close to the surface, e.g. near the ZnSe/metal interface. Consequently, the p-like behaviour of the vacancies acts as a counterpart to the intended n-type doping.

The samples B* and C* are pieces of the F and Cl implanted samples B and C that were thermally annealed for 3 min at 250 °C to recover the crystal structure and further activate donors. The corresponding IV curves shown as dashed lines in Fig. 3.7 b,c) indicate a reduction of the resistance within one order of magnitude in both cases. However, subsequent further annealing of samples B* and C* for additional 3 min at

300 °C induced a substantial degradation of the contacts and again an increase of the resistance (Appendix, Fig. A.6). In conclusion, the limited thermal budget for ZnSe prevents formation of low resistivity contacts (ρ_c<0.01 Ω cm^2) by either diffusion or implantation lacking a sufficiently high free charge carrier concentration below the contacts.

3.4. CONTACTS TO EPITAXIALLY DOPED BULK ZNSE

EX-SITU CONTACTS TO EPITAXIALLY GROWN ZNSE:CL

The optimization of the contact metal is performed on ZnSe:Cl samples which are doped *in-situ* during MBE growth. The figure of merit is the metal contact resistivity ρ_c. We use a Cl concentration of $n_{\mathrm{Cl}} > 1 \times 10^{19}\,\mathrm{cm}^{-3}$, which is on the metallic side of the metal-insulator-transition (MIT). According to the Schottky model, metals with a workfunction matching the electron affinity of the semiconductor (χ=4.09 eV for ZnSe [86]) minimise the SBH (see Eq. 3.1) and thereby ρ_c. The metals In, Mg, and Al providing a low work function Φ_m of 3.9 eV, 3.19 eV, and 4.13 eV, respectively, have been intensively experimentally studied in Ref. [87]. Here, we study Ti, Al, and Mg together with Nb as another material with a low Φ_m of 4.0 eV [108]. For the fabrication of the *ex-situ* contacts, metal lift-off was used, see Chap. 5.

Fig. 3.8 a) shows the IV characteristics of *ex-situ* fabricated contacts at a fixed contact distance $L = 30\,\mu\mathrm{m}$. The data was obtained by four-terminal measurements in darkness at a needle probe station. The IV characteristics are non-linear for all metals and reveal a large resistance $R = 1/[\partial I/\partial V]_{V=0}$ around zero bias, which is the region of interest for qubit device operation. At elevated voltages, a higher current slope is observed which is symmetric for both electric field directions. The resistance R varies within one order of magnitude between samples and contacts and exhibits no monotonic dependence on the contact spacing (Fig. 3.8 b). Consequently, the device resistance is dominated by the contact resistance, in agreement with an estimated substrate resistance of only a few Ω. We assume that a thin native oxide on ZnSe (presumably $\mathrm{SeO_x}$) governs R as well as the breakdown characteristic at elevated voltages. Accordingly, the variation in R originates from nanoscale inhomogeneity of the junction.

The lowest contact resistivities we obtained with the *ex-situ* method are of the order of ρ_c ~0.01 Ω cm^2, see Tab. 3.4. This result is found for Nb and Al contacts while the contact resistance of Ti is substantially larger. Note, that we assumed a homogeneous current density at the contact/semiconductor interface for extraction of the contact resistivity in a regime, where the transfer length well exceeds the contact dimensions. As a side note, overview tables of the very same format will be provided throughout this thesis to ease a comparison of results on contact resistances. The contact resistivities found compare well to typical values reported in the literature for contacts fabricated *ex-situ* [77]. However, the requirements for Ohmic contacts defined in Sect. 2.2.2 can not be met. Since tunnel resistances are high and at $T \leq 4\,\mathrm{K}$

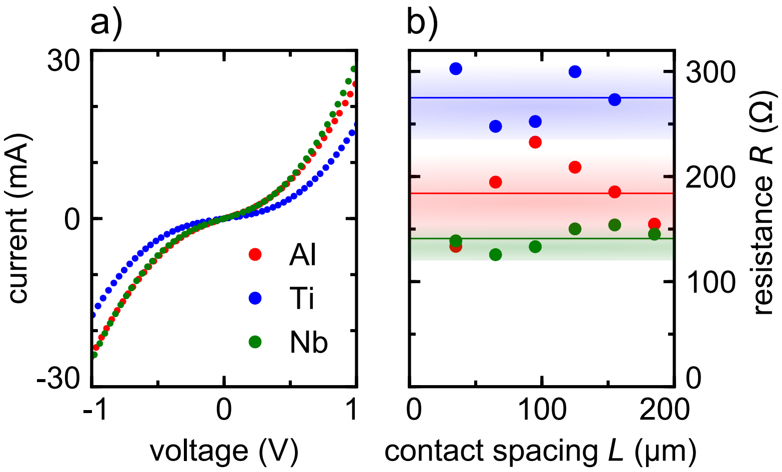

Figure 3.8: Metal contacts to highly doped n-ZnSe fabricated by the *ex-situ* method. a) IV characteristics for three contact metals (Al, Ti, Nb) measured at RT. The distance between the contacts sized $190 \times 75\ \mu m^2$ is $L = 30\,\mu m$ for all three ZnSe:Cl samples that are highly doped ($n_{Cl} \sim 10^{19}\,cm^{-3}$). b) Resistance R around zero bias as a function of the contact spacing L as extracted from the IV curves for Al, Ti and Nb (same color code as in panel a). Horizontal lines and shaded areas indicate the mean resistance and variance, respectively. Figure adapted from Ref. [5, 105].

thermal transport gets suppressed, a significantly increased contact resistivity is expected.[13] This urges for alternative contact methods providing lower ρ_c.

Table 3.4: Characterization of contacts fabricated *ex-situ* on n-type ZnSe:Cl. Upper part: Characterization results obtained at RT for various contact metals on untreated samples. Lower part: Results for samples with Ar treatment prior to metallization, including a reference (0 nm). Values given in the lower part specify lower bounds (see text).

contact	Ar mill (nm)	R_c (Ω)	R_s (Ω/□)	ρ_c (Ω cm^2)	L_t (µm)
Al	-	0.8×10^2	49	1.1×10^{-2}	1.5×10^2
Ti	-	1.3×10^2	49	1.9×10^{-2}	2.0×10^2
Nb	-	0.6×10^2	49	0.9×10^{-2}	1.4×10^2
Al	0 nm	2.0×10^3	49	0.3	0.8×10^3
Al	5 nm	8.5×10^3	49	1.2	1.6×10^3
Al	10 nm	6.5×10^3	49	0.9	1.4×10^3

The Ohmic contact performance of *ex-situ* samples is expected to be improved by oxide removal in high vacuum and subsequent metal deposition. To realise this experi-

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[13] In the case of *ex-situ* fabricated Al contacts ρ_c doubles to about $0.02\,\Omega\,cm^2$ at $T = 4\,K$.

mentally, we utilise ion milling prior to Al metallization in the same vacuum chamber and afterwards a standard resist lift-off technique to form the contacts.[14] For these experiments we used about 1 µm thick highly doped n-type ZnSe layers with a typical doping concentration of $n_{\mathrm{Cl}} > 1 \times 10^{19}\,\mathrm{cm}^{-3}$.

For Ar milled samples (*ex-situ*) the results of electrical characterization at room temperature are shown in Fig. 3.9 and Tab. 3.4. The IV curves obtained by four-terminal measurements in darkness are non-linear for two Ar ion milled samples and a reference. The electron transport is dominated by thermionic transport across a barrier when the oxide is present. For the ion milled samples, the differential resistance decreases at voltages of a few volt, but for zero bias R and thus ρ_{c} is increased by multiple orders, which was also observed for other contact metals. The strong increase in ρ_{c} is not fully reflected in Tab. 3.4 due to limited measurement resolution around zero bias when sourcing current, but was verified by sourcing voltage (data not shown). We assume that crystal defects, namely Zn-vacancies, are introduced by the invasive etching process with Ar ions and decrease the net charge carrier concentration in the region where the contact is formed [48]. Lower carrier concentration leads to an effectively higher contact resistance and higher breakthrough voltages. In addition to Ar milling, we also carried out wet etching as postgrowth surface treatment, but none of these processes led to substantial improvement of the contact performance.

IN-SITU CONTACTS TO EPITAXIALLY GROWN ZNSE:CL

In contrast to the doping techniques based on diffusion or implantation, *in-situ* doping during MBE growth can be well controlled, as described in Chap. 5. In the following, we will apply this epitaxial doping method to ZnSe with Cl donors for studying the metal contact resistivity ρ_c in this section. All samples provide a Cl concentration of $n_{\mathrm{Cl}} > 10^{19}\,\mathrm{cm}^{-3}$ which is on the metallic side of the MIT. In case of all *ex-situ* techniques, contact formation at the metal-ZnSe interface is hampered due to formation of a native oxide. XPS studies performed in Ref. [109] identified this native oxide as a thin $\mathrm{SeO_2}$ layer on top of the ZnSe surface. So far, in the literature the lowest ρ_c was reported for a layer stack of Ti/Pt/Au contacts where the oxide was wet-chemically removed prior to metallization [78]. Consequently, we focused our main efforts on entirely avoiding any oxide formation by making use of *in-situ* fabrication (e.g. maintaining UHV conditions between ZnSe MBE growth and the metallization step). Due to the low barrier height in the Schottky model, the contact metals Ti, Al and Mg were investigated in this study [84].

Fig. 3.10 a) shows the IV characteristics for the *in-situ* deposited metal contacts with a distance of $L = 30\,\mu\mathrm{m}$. The data was obtained by four-terminal measurements in darkness at a needle probe station. For *in-situ* contacts, R is in the order of $10\,\Omega$ and

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[14] Neutral Ar ions impinging onto the substrate surface physically remove the oxide. The process is run in an Ar atmosphere of 1.6×10^{-4} mbar and Ar ions are pre-accelerated by a voltage of 80 V before they are neutralised and hit the sample. With this process we determined typical etch rates of about 1 nm/s for ZnSe.

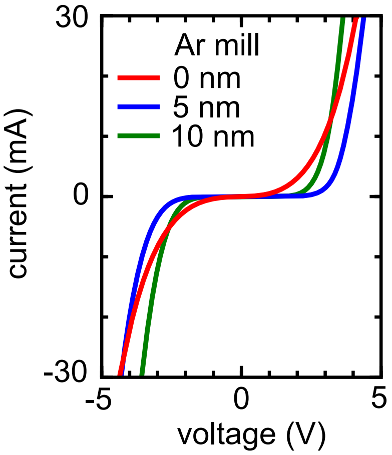

Figure 3.9: The effect of native oxide on ZnSe on the performance of Al contacts. The native oxide was removed by etching about 5 nm or 10 nm deep into the ZnSe surface via Ar milling. The corresponding IV characteristics (blue and green curves) indicate a substantial increase of the resistivity at low voltages compared to that of an untreated sample (red curve). The lateral contact spacing is $L = 30\,\mu\text{m}$. The IV data is obtained from current driven 4-terminal measurements with 0.1 mA resolution. Figure adapted from Ref. [5, 105].

the IV characteristic is linear in case of all three contact metals. Resistance variations between devices with same metal contacts are less than 10 %. Furthermore, the device resistance shows a clear monotonic dependence on the contact spacing L (Fig. 3.10 b). We confirm the expectation of substantially lowered contact resistance for a metal-semiconductor interface without interfacial oxide by comparing *in-situ* and *ex-situ* contact resistivities.

We now quantify the contact resistivities of the *in-situ* metal contacts. Fig. 3.10 b) shows a non-linear dependence of $R(L)$, since the samples do not provide a mesa etched linear transport channel. To include the fully three-dimensional nature of the current distribution in our device, we applied a finite-element solver and modeled the device following the routine outlined in Sect. 3.2.2. $R(L)$ is fitted using the ZnSe bulk resistivity ρ_b and the metal/ZnSe contact resistivity ρ_c as free parameters (solid lines in Fig. 3.10 b). According to the TLM (see Sect. 3.2.1), the current density under the metal contact drops on a length scale of the transfer length L_t as lateral bulk resistance competes with the vertical resistances of the metal-semiconductor interface, ρ_c. The simulation based fits (Fig. 3.10 b) provide both R_s and ρ_c, presented in Tab. 3.5). Since the width of the metal contact (along the bias gradient) is larger than L_t by a factor of 6 at least, Eq. 3.5 applies. The related transfer lengths and sheet resistances are 7.7 µm, 11.4 µm, 29.5 µm and 39 Ω/□, 29 Ω/□, 27 Ω/□ for the contact metals Al, Mg and Ti, respectively. The lowest contact resistance at room tempera-

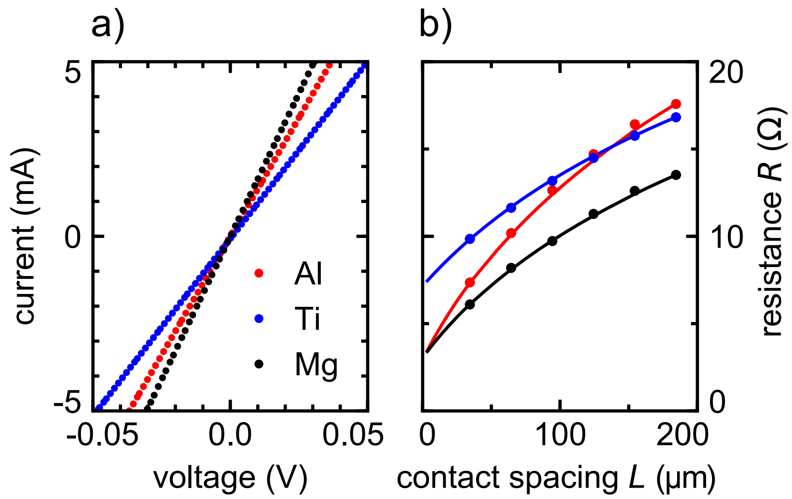

Figure 3.10: Metal contacts to n-type ZnSe fabricated by the *in-situ* method. a) IV data for different contact materials (Al, Ti, Mg) on separate ZnSe:Cl substrates ($n_{\mathrm{Cl}} \sim 10^{19}\,\mathrm{cm}^{-3}$). The lateral contact spacing is $L = 30\,\mu\mathrm{m}$. b) Total device resistance for Al, Ti and Mg as a function of the contact spacing L for samples without mesa etched linear transport channel (same color code as in panel a). Fits (R_s, ρ_c) to the data using the finite element solver are plotted as solid-lines. Analysis results are summarised in Tab. 3.5. Figure adapted from Ref. [5, 105].

ture $\rho_\mathrm{c} = 2.3 \times 10^{-5}\,\Omega\mathrm{cm}^{-2}$ is determined for Al. All results of contact resistivity for *ex-situ* deposited metals are presented in Tab. 3.5.

Table 3.5: Contact resistivities of contacts deposited *in-situ* on n-ZnSe (RT).

contact metal	R_c (Ω)	R_s (Ω/□)	ρ_c ($\Omega\,\mathrm{cm}^2$)	L_t (µm)
Al	1.4	39	2.3×10^{-5}	7.7
Mg	1.5	29	3.7×10^{-5}	11.4
Ti	3.6	27	24×10^{-5}	29.5

Remarkably, the contact resistances for Al and Mg of the samples fabricated with the *in-situ* method are well-below the value of $\rho_\mathrm{c} = 3.4 \times 10^{-4}\,\Omega\mathrm{cm}^2$ observed in Ref. [78]. In this reference, wet chemical etching of the ZnSe after exposition to air was investigated. With our proposed *in-situ* method, we observed to our knowledge the best room temperature values regarding the contact resistivity of n-ZnSe contacts. In particular, the low Φ_m metals Al and Mg show excellent values for both L_t and ρ_c. This progress allows us to study the Ohmic contact resistance at a temperature of 4 K.

3.4.1. OHMIC CONTACTS TO ZNSE OPERATED AT 4 K

Since all-electrical quantum devices such as EDQDs operate at low temperatures down to 10 mK, we study whether our Ohmic contacts remain operable at 4 K. At this temperature, thermionic charge transport across the Schottky or any other contact barrier is sufficiently suppressed. There is one quantitative result for ρ_c of Ohmic contacts to n-ZnSe at low temperature ($T \leq 4$ K) reported in the literature [110]. Richter reported on Al contacts fabricated *in-situ*, similar to our approach, that yield at 1–4 K a ρ_c of $2.6 \times 10^{-3}\,\Omega\,\mathrm{cm}^2$ [110]. The reported contact resistivity is not temperature stable and almost two orders of magnitude higher than our best result obtained at RT, which we attribute to lower tunnel barriers and higher carrier concentration in our experiments [111].[15]

Here, we show in Fig. 3.11 a) the IV characteristic at 4 K for Al, Mg, and Ti Ohmic contacts deposited *in-situ*. Wire bonding is used to electrically contact the structures. Using a 20 µm thick Al wire, typical wire-bond parameters are a bond power of 240 mW applied for 40 ms, which is adjusted to be as low as possible. We experienced insufficient adhesion applying Au ball bonding on the Al pads.

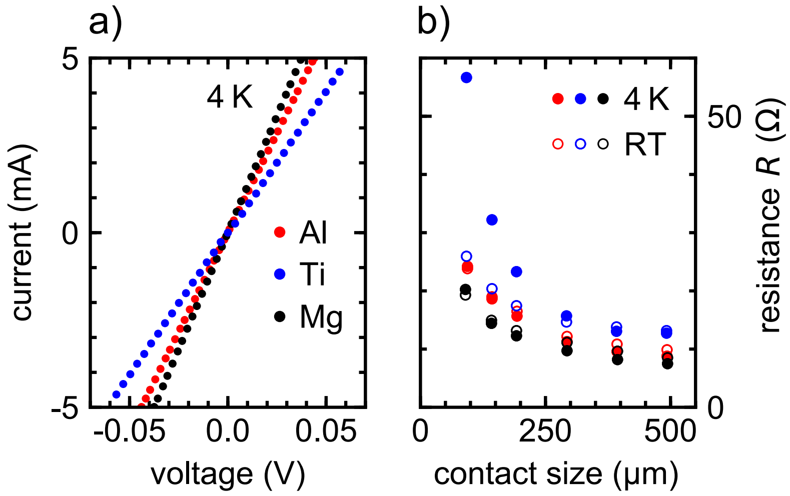

Figure 3.11: Properties of metal contacts to n-type ZnSe fabricated by the *in-situ* method.a) IV data measured at 4 K for different contact materials (Al, Ti, Mg) on ZnSe:Cl samples ($n_{\mathrm{Cl}} \sim 10^{19}\,\mathrm{cm}^{-3}$). The lateral contact spacing is $L = 200\,\mu\mathrm{m}$, contact size is 500 µm. b) Total device resistance for $L = 200\,\mu\mathrm{m}$ as a function of the side length of square-shaped metal contacts for Al, Ti, and Mg (same color code as in panel a). R is measured at room temperature (open circles) and at 4 K (dots), respectively. Resistances of setup wiring are subtracted. Figure adapted from Ref. [5, 105].

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[15] Presumably the carrier concentration of the reference experiment was not optimised, since substrate conductivity could be seven fold increased in later experiments as n reached $3 \times 10^{19}\,\mathrm{cm}^{-3}$ [111].

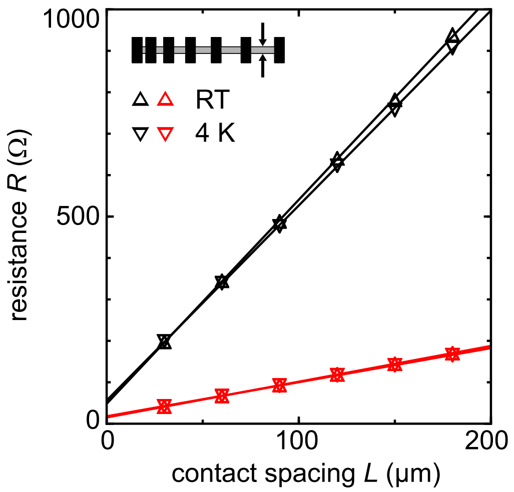

Figure 3.12: Characteristics of mesa devices with *in-situ* Al contacts at RT and 4 K. $R(L)$ for channel width 10 (50) µm depicted in black (red) gives direct access to bulk and contact resistivities that are similar for RT and 4 K. Simulations (lines) can reproduce the data by fitting ρ_c and ρ_s, see Tab. 3.6. The inset shows the device geometry used for definition of contacts (black) on a mesa etched doped ZnSe channel (black/gray). Arrows highlight the channel width specified. Figure adapted from Ref. [5, 105].

The data is corrected for resistances of the setup wiring by subtracting the separately measured temperature-dependent resistance offset of the setup or by using four-terminal measurements. We observe linear IV characteristics, the slopes of which are slightly dependent on the contact metal. Fig. 3.11 b) shows the extracted resistances for each contact metal as a function of the side length of the contact pads. The observed super-linear drop of the device resistance is expected, as the contact area increases quadratically with the contact size. Note that the resistances roughly coincide for 4 K and RT, since two effects, the bulk resistivity reduction (depending on electron mobility and bulk doping concentration) and the contact resistivity increase, seem to counterbalance. Most importantly, the contact resistance depends only marginally on temperature and we conclude that a thermionic part of charge transport across the metal/ZnSe junction is negligible.

The excellent performance observed for *in-situ* fabricated contacts enables us to quantitatively study contact resistance and transfer length of Al/ZnSe:Cl Ohmic contacts at 4 K. We have chosen Al contacts as they provide low ρ_c and are easy to fabricate. Two mesa devices on a $10\times10\,\text{mm}^2$ chip were characterised including error analysis. Typical fabrication tolerances in device dimensions of ~ 1 µm for optical lithography and ZnSe layer thickness variations of 2 % across the chip enter the error calculations. Structures with two different channel widths (10 µm and 50 µm) are investigated. Fig. 3.12 shows the device resistance R for the 10 µm and the 50 µm mesa samples with varying contact spacing for both RT and 4 K. The linear increase in R with increasing contact spacing equivalent to the mesa channel length is clearly visible. Remarkably, no significant temperature dependence of R is observed. The small decrease of $\frac{\partial R}{\partial L}$ at 4 K compared to RT qualitatively agrees with a small decrease of the bulk ZnSe resistivity observed by temperature dependent van der Pauw Hall measurements.

For quantitative results a finite element solver and the device geometry is utilized to determine transfer length and contact resistivity. $R(L)$ is fitted using ZnSe bulk resistivity and contact resistivity as free parameters. Fig. 3.12 shows good agreement of measurement and simulation. Based on these considerations, for Al, the specific contact resistivity at room temperature is determined with $\rho_c = (2.3 \pm 0.9) \times 10^{-5}\,\Omega\text{cm}^2$ for the 10 µm wide mesa device and $\rho_c = (6 \pm 2) \times 10^{-5}\,\Omega\text{cm}^2$ for the 50 µm wide mesa device. At 4 K, the contact resistivity increases for both structures up to $\rho_c = (4 \pm 2) \times 10^{-5}\,\Omega\text{cm}^2$ and $\rho_c = (17 \pm 3) \times 10^{-5}\,\Omega\text{cm}^2$ for the 10 µm and the 50 µm structure, respectively. A summary of all electrical analysis results for these two devices is presented in Tab. 3.6. Similar contact resistivities were also observed on multiple other devices on the same chip, where variations are attributed to microscopic variances at the contact interface originating from the fabrication process.

Table 3.6: Contact resistivities of Al contacts deposited *in-situ* on n-ZnSe.

T (K)	structure	R_c (Ω)	R_s ($\Omega/\square$)	ρ_c (Ωcm^2)	L_t (µm)
300	10 µm	25	44±3	$2.3 \pm 0.9 \times 10^{-5}$	7±2
300	50 µm	6	45.5±0.7	$6 \pm 2 \times 10^{-5}$	11±2
4	10 µm	28	42±3	$4 \pm 2 \times 10^{-5}$	10±2
4	50 µm	8	42±3	$17 \pm 3 \times 10^{-5}$	20±2

3.4.2. Local Ohmic contacts to bulk ZnSe using regrowth process

Following the above presented results of excellent Ohmic contact performance for *in-situ* Al contacts on ZnSe:Cl substrates doped during MBE growth, we developed a regrowth fabrication process to demonstrate local Ohmic contacts that are in principle suitable to access a buried conducting channel in a ZnSe-based heterostructure selectively. For this approach, we used a ZnSe:Cl substrate with a nominal thickness of 1 µm and a carrier concentration of about $7.5 \times 10^{17}\,\text{cm}^{-3}$, in this case at the dielectric side to the MIT. A device with locally doped contacts with a doping concentration of about $1 \times 10^{19}\,\text{cm}^{-3}$ was fabricated following the selective regrowth process described in Sect. 5.3. Notably, selectivity of epitaxial doping is enforced by introduction of a hard mask and etching prior to the contact formation by regrowth.

Additionally, a reference sample was fabricated. The cross-section drawing of the regrown and reference sample is presented in Fig. 3.13 a,b), respectively. By growth of

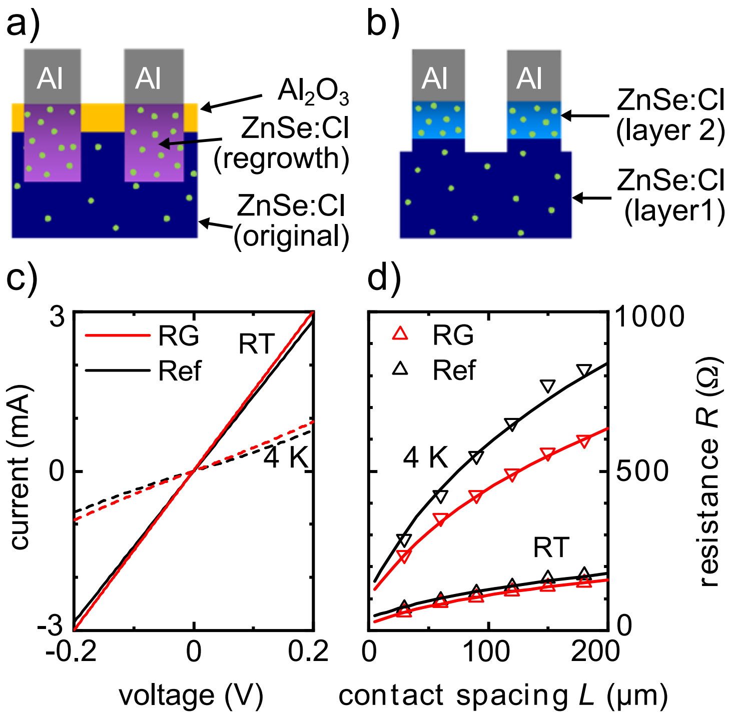

Figure 3.13: Local Ohmic contacts on a sample fabricated via the regrowth method (RG) and a corresponding reference sample (Ref), both measured at RT and 4 K. a) Schematic cross-section view of the regrowth sample and b) of the reference sample. c) IV characteristics for both samples with an exemplary contact spacing of 30 µm. d) Total resistance (symbols) as a function of contact spacing and the related simulations (lines). Figure by Johanna Janßen [5, 105].

the reference sample, we have reproduced another ZnSe:Cl substrate with the same thickness and doping concentration as the regrowth sample. However, in this case, an additional ZnSe:Cl layer (“layer 2”) about 30 nm thick with a doping concentration in the order of $1 \times 10^{19}\,\mathrm{cm}^{-3}$ was grown on top of the substrate during the same MBE run. This configuration consequently provides the ideal interface between the substrate and the highly doped ZnSe:Cl contact layer. Subsequently, the reference sample was metalised *in-situ* with Al to form the Ohmic contact and finally structured to restrict the current path between contacts to the lower doped ZnSe:Cl substrate ("layer 1"), as realised for the regrowth sample.

The comparison of the IV characteristics of both samples allows us to quantify the impact of the regrowth interface (i.e., between the etched ZnSe:Cl substrate surface and the regrown Al/ZnSe:Cl contact region) on the current transport. Fig. 3.13 c) shows the IV characteristics of the regrowth (red) and the reference sample (black) at RT (full curves) and 4 K (dashed lines). Remarkably, the behavior is nearly identical for both samples. At RT, the curves are linear, whereas they exhibit a slight nonlinear-

Table 3.7: Specific contact resistivities at RT and 4 K for Al contacts deposited *in-situ* on bulk n-ZnSe. Best fit results of finite element simulations to experimental data are given.

Sample	T	R_c (Ω)	R_s (kΩ/☐)	ρ_c (Ω cm^2)	L_t (µm)
RG	RT	11	0.38±0.05	$1.7 \pm 0.2 \times 10^{-4}$	6.7±0.4
Ref	RT	20	0.36±0.05	$5 \pm 1 \times 10^{-4}$	12±1
RG	4 K	53	1.8±0.2	$1.4 \pm 0.4 \times 10^{-3}$	9±1
Ref	4 K	61	2.0±0.2	$1.0 \pm 0.2 \times 10^{-3}$	7.1±0.7

ity at 4 K. Fig. 3.13 d) shows the total resistance of each sample as a function of the contact spacing. The contact resistivities are extracted from the related finite element simulations; ρ_c(RG)=$1.7 \pm 0.2 \times 10^{-4}$ Ω cm^2 and ρ_c(Ref)=$5 \pm 1 \times 10^{-4}$ Ω cm^2 at RT as well as ρ_c(RG)=$1.4 \pm 0.4 \times 10^{-3}$ Ω cm^2 and ρ_c(Ref)=$1.0 \pm 0.2 \times 10^{-3}$ Ω cm^2 at 4 K. We obtain similar results for the regrowth and the reference sample, which demonstrates the excellent quality of the regrowth interface and the absence of current transport barriers because of the etching and regrowth process. Furthermore, the resistances are distinctively increased at 4 K. Together with the nonlinearity of the IV curves, we attribute this effect to the comparably low carrier concentration of the ZnSe:Cl substrate ($n_{\mathrm{Cl}} \sim 7.5 \times 10^{17}$ cm^{-3}), which is considerably below the carrier concentration of the MIT and therefore also temperature dependent. This is consistent with the simulated values obtained for the sheet resistances at 4 K (R_s(RG)=1.8 ± 0.2 kΩ/☐ and R_s(Ref)=2.0 ± 0.2 kΩ/☐), which are about a factor of 50 higher than the sheet resistances obtained for the highly doped ZnSe:Cl substrate in the previous section. An overview of results from electrical characterization is presented in Tab. 3.7.

With our technology, demonstration of low resistivity contact to locally doped bulk ZnSe by selective regrowth is achieved. The key factor is a transfer of the the *in-situ* contact technique to selective growth on prestructured samples without compromising contact resistivity. Although pre-structuring is conducted *ex-situ*, we identify a regrowth process capable of restoring a high crystal quality also below the contact interface. Accordingly, low ρ_c at $T \leq 4$ K meeting our criteria for contacting all electrical quantum devices, was realised, see Tab. 3.7. Low ρ_c is enabled by addressing high crystalline and high interface quality with multi step *ex-situ* etching prior to contacting, without altering the contact formation process *in-situ*, see Chap. 5.10.[16]

However, compatibility of our regrowth process with a HS containing a QW of typically 10 nm thickness is limited for the following technical reason:

Pre-structuring *ex-situ* by dry etching causes crystal defects, leading to p-type defects in the n-type contact region and in consequence to increased contact resistivity. The profile of defects produced, dependent on process details, requires a subsequent wet etch to remove the damaged region. The wet etch process employed

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[16] A dry and a wet etching process (both *ex-situ*) after mask structuring (dry etching, *ex-situ*) is followed by atomic H cleaning (*in-situ*) prior to MBE growth and metallization (*in-situ*).

is based on potassium dichromate (Sect. 5.13). This inaccuracy strongly affects the contact properties. In the case of a thin residual ZnMgSe barrier covering the QW, contact resistivity is substantially increased. The same effect is expected for etching down the entire QW, contacted then from the side, as the contact area gets reduced by reduced several orders of magnitude. In consequence, contact formation requires an etch precision of ±3 nm on the lateral scale of contacts of for combined dry and wetchemical etching. This precision, typically achieved in isolated RIE or wet chemical etch processes, lies beyond our capabilities. We are not aware of a selective etch process based on other etchants or introduction of an etch stop layer featuring high selectivity between ZnSe and ZnMgSe. As an alternative solution, we investigate the potential of epitaxial doping of substrates with QW in the next section, aware of relaxing thereby the criterion of local doping.

Still, we could successfully demonstrate a selective regrowth contact to a thick ZnSe:Cl channel. This was possible, since for our HS with a conducting channel 100-fold thicker than a typical QW, the demands on etch precision were strongly relaxed.

3.5. AL IN-SITU CONTACTS TO ZNSE QWS

So far, we have discussed the contact resistivity for various metal contacts on n-doped ZnSe bulk crystals in this chapter. For *in-situ* deposited Al, we have identified sufficiently low specific contact resistivities that require high doping concentrations in the substrate, experimentally achieved by noninvasive epitaxial doping. Local doping by invasive doping techniques such as implantation or In diffusion were shown not to meet the requirements of spin qubit fabrication as a consequence of limited thermal budget (see Sect. 3.3.1). Neither is the regrowth process capable of contacting a QW (Sect. 3.4.2) as result of technological limitations. As an alternative solution, we transfer the technology for *in-situ* contacts developed for bulk ZnSe material to a heterostructures hosting a ZnSe QW. In the regime of a low contact resistivity governed by tunneling, we expect ρ_c to scale with $\sqrt{n/m_{\text{eff}}}$, as predicted and verified for group V and III-V semiconductors [90]. Our approach utilises control of the doping profile in a heterostructure to adjust the contact resistance.

AL IN-SITU CONTACTS TO DOPED ZNSE QWS

The importance of contact metal, interface quality and substrate doping for a contact to bulk ZnSe has been discussed in the previous sections. Now, we investigate the contact to a ZnSe QW. A high charge carrier concentration below the metal contact is essential to achieve a reduction of the tunnel barrier and thereby R_c and ρ_c, in alignment with the framework of Schottky contacts (Sect. 3.2). Therefore, in the case of ZnSe/ZnMgSe heterostructures, the ZnMgSe in the upper barrier has to provide a high free charge carrier concentration.

We experimentally investigate contact properties for ZnSe/ZnMgSe heterostructures with a doped QW. The HS with fixed dimensions and material composition hosts a

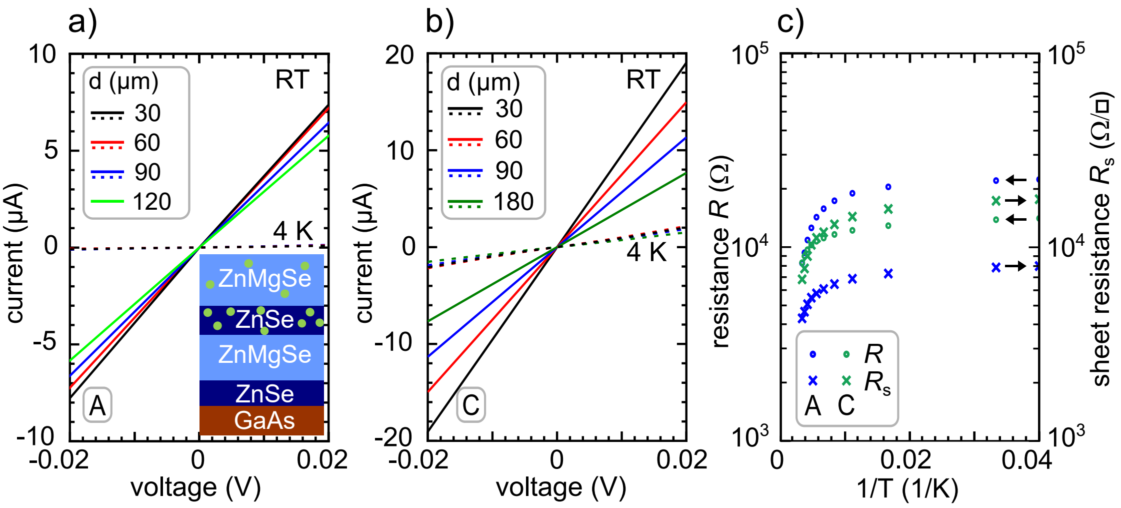

Figure 3.14: Characterization of *in-situ* Al contacts to doped QW structures. *IV* characteristics of a sample with a doping concentration in the upper barrier of a) $2 \times 10^{18}\,\mathrm{cm}^{-3}$ (substrate A) and b) $5 \times 10^{18}\,\mathrm{cm}^{-3}$ (substrate C). *IV* profiles are shown for different contact spacing d of TLM structures and temperature (RT/ 4 K). The insert displays a typical QW structure. c) Temperature dependent R (dots) and R_s (crosses) obtained by van der Pauw Hall measurements, arrows denote the corresponding vertical axis. Separate chips of both substrates A (blue symbols) and C (green symbols) for T=25–300 K were used for the two different measurement techniques utilised in panels a/b) or c). Hall measurement by Johanna Janßen.

conducting ZnSe QW, depicted in Fig. 3.14 a) in the insert. The carrier concentration below the contact is controlled by epitaxial doping of the ZnMgSe in the upper barrier. From band structure simulations we expect electrons from the upper barrier to either localise in a surface channel or in the QW, with a ratio depending on the specific doping concentration and surface potential, see Chap. 2/Fig. 2.2. In this study, we select various doping concentrations in the vicinity of the MIT of ZnMgSe ($7 \times 10^{17}\,\mathrm{cm}^{-3}$) for the upper barrier and a doping concentration well above the MIT of ZnSe ($5 \times 10^{17}\,\mathrm{cm}^{-3}$) for the ZnSe QW, although the final device should be undoped. Thereby we effectively create a system of two transport channels in parallel, with dominant conductivity in the QW channel, as will be shown later. Crystal damage during fabrication (Sect. 3.3.2) is avoided as the heterostructures are non-invasively doped by epitaxial doping with Cl and, after MBE growth, contacted by *in-situ* deposited Al (Sect. 3.4).

We investigate two heterostructures with the upper ZnMgSe barriers differing in doping concentration of 2×10^{18} and $5 \times 10^{18}\,\mathrm{cm}^{-3}$ for substrate A and C, respectively. Fig. 3.14 a, b) shows *IV* characteristics of TLM devices for both substrates at RT. We find increased conductivity and linearity for substrate C with higher carrier concentration, as tunneling out-competes thermally activated transport associated with non-linear IV profiles only observed for substrate A. Accordingly, observation of linearity at 4 K consolidates the strong influence of carrier concentration on barrier reduction, although at higher resistivity level compared to RT. Details on the results obtained at $T = 4\,\mathrm{K}$ can be looked up in the appendix, see Apx. A.8. The temperature induced decrease of conductivity is investigated further by van der Pauw Hall on separate chips with van der Pauw Hall contact design. Resulting temperature dependencies of differential and sheet resistance are presented in Fig. 3.14 c). Sheet resistivities of both substrates are comparable, but increase more strongly for substrate A at 4 K as consequence of higher resistivity in the upper ZnMgSe barrier, attributed to lower n. The characteristic change of sheet resistance points at the relevance of parallel conduction in the upper ZnMgSe barrier. Charge carriers in ZnMgSe freeze out at about 300–200 K and scattering of carriers at undoped impurities dominates, assigned to Anderson like localisation (Sect. 4.2.2). This effect is not only visible in the sheet resistance, but also in contact resistivity: We know, IV profiling is sensitive to ρ_c, since the surface doping concentration n_s at a heterojunction with tunnel contact affects the width of the depletion region and thereby the tunnel resistance. Looking along z-direction, carriers accumulate at the surface region of the upper barrier due to the band configuration given by the heterostructures set in our experiment. At RT, the measurement is affected by thermally excited electrons and ρ_c is not sensitive to the doping concentration. However, cooled down to 4 K, contacts on substrate A with lower carrier concentration exhibit non-linear IV characteristics. A quantitative analysis on ρ_c is provided in the following section. We suggest, the difference in linearity originates from different doping concentrations in the upper barrier. Our finding is in agreement with measurements of the carrier concentration using the van der Pauw Hall method (the same measurements as in Fig. 3.14 c), data for n not explicitly shown).

Expanding on the analysis outlined above, we study ρ_c as a function of doping concentration in the upper barrier. As a disclaimer, we note that errors on ρ_c and L_t are large, since the assumptions of the TLM model break down for a substrate with more than one layer. The reason is the existence of multiple interfaces (QW/barrier and barrier/contact) and in consequence the layer of the contact interface is no longer clearly defined. TLM devices on four substrates with different doping concentrations in the upper barrier ($n_{\mathrm{RT}} = 2\times10^{16}$–$1\times10^{18}\,\mathrm{cm}^{-3}$) are characterised by IV profiling at both RT and 4 K. The substrates A and B discussed above are included in this study:

The results from electrical characterization at RT and 4 K are shown in Fig. 3.15 and listed in Tab. 3.8. Almost constant sheet resistance is observed for the heterostructures tested, independent on n in the ZnMgSe:Cl barrier. This indicates the main channel is located in the ZnSe:Cl QW and not in the ZnMgSe:Cl barrier, as expected. Contact resistances derived from IVprofiles such as those depicted in Fig. 3.15 a) are well below 10 kΩ at RT for all substrates with doped barriers, see Fig. 3.15 b). However, the non-linearity in IV profiles and corresponding contact resistance for sub-

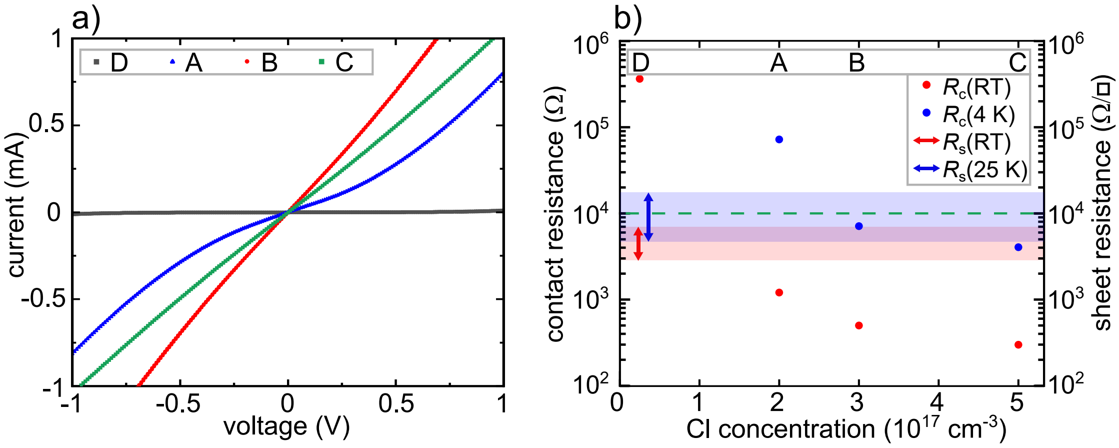

Figure 3.15: Electrical characterization of Al *in-situ* contacts to doped ZnSe QWs. a) Current-voltage characteristics for TLM devices with contact spacing of 30 µm, obtained at RT. Substrates A-D differ in the Cl concentration c_{Cl}^{SIMS} of the upper barrier. Measurement by Johanna Janßen. b) Dopant concentration in the upper barrier versus contact resistance determined by TLM at RT and 4 K, respectively. Sheet resistance measured at RT and $T = 25$ K lie within the regions highlighted in red and blue, respectively. The green dashed line shows the target resistance of 10 kΩ. Hall measurement by Johanna Janßen. Figure adopted from Johanna Janßen.

strate D (nominally undoped barrier) is substantially higher, attributed to formation of a Schottky contact as discussed in the previous paragraph. Our result is in agreement with the expectation of reduced tunnel resistance for sufficiently high doping concentrations close to or beyond the MIT of ZnMgSe (7×10^{17} cm^{-3}) (Sect. 4.1.2). In contrast, the main channel with highly doped ZnSe QW does not undergo the MIT. Increased sheet resistance at 25 K compared to RT is attributed to freeze out of minority charge carriers in the upper barrier, dependent on the doping concentration slightly below the MIT of ZnMgSe in our experiment.

To sum up, we find a strong correlation of contact resistivity with the carrier concentration below the contact. For low doping concentrations (substrates D, A) ρ_{c} is governed by thermionic emission that is strongly suppressed at 4 K. At high doping concentrations (substrates B, C), tunneling increasingly determines ρ_{c}. In absolute numbers we yield contact resistances below the target value of 10 kΩ at 4 K (ρ_{c}=6×10^{-4}–3×10^{-3} Ω cm^2), meeting the requirements for qubit operation (Sect. 2.2).

Further optimization of the Al *in-situ* contact resistivity by post metal anneal (Apx. A.3) could not improve the contact resistivity, which is again a consequence of p-type Zn vacancy generation as the thermal budget is exceeded (Sect. 3.3.1). One major disadvantage of contact formation by epitaxial doping, which does not allow for local doping, is the introduction of a parallel conducting channel to the QW. Also, increased scattering at Cl neutral impurities adjacent to the QW is expected. Introduction of a

10 nm thick spacer between QW and (remote) Cl dopants in the barrier did not result in ρ_c meeting the requirements for operation of electrical devices at $T \leq 4$ K. The electrical characteristics of that substrate was comparable to substrate A, where ρ_c was governed by thermionic emission and not tunneling.

Table 3.8: Contact resistivities of *in-situ* deposited contacts to ZnSe QWs. Electrical characterization of contacts for substrates A-D with a highly doped ZnSe QW (1×10^{19} cm^{-3}) and varying Cl concentration $c_{\mathrm{Cl}}^{\mathrm{SIMS}}$ in the upper barrier determined by SIMS. Since substrate D is nominally undoped the measurement sensitivity is listed for $c_{\mathrm{Cl}}^{\mathrm{SIMS}}$. R_c and R_s are determined by the TLM and van der Pauw Hall measurements, respectively. For $R_c >> \rho_s \times \square$ a homogeneous current distribution is assumed for derivation of ρ_c. Otherwise ρ_c and L_t is derived using the TLM. Due to technical limitations, R_s was determined at 25 K instead of 4 K. No measurement was performed at 4 K/25 K for the substrate with undoped barrier since high resistances exceeding the measurement limit are expected. The channel width (mesa) is specified in the second column. The substrate B has no mesa etched channel, therefore we assume a channel width equal to the contact width. Structural data (XRD) is specified in Tab. 5.2.

Substrate	$c_{\mathrm{Cl}}^{\mathrm{SIMS}}$ (cm^{-3})	width (µm)	R_c (kΩ)	R_s (kΩ/□)	ρ_c (Ω cm^2)	L_t (µm)
			300 K	300 K	300 K	300 K
D	2.5×10^{17}	50	350	5.4	5×10^{1}	1×10^{3}
A	2×10^{18}	50	1	4.3	1×10^{-3}	6
B	3×10^{18}	190	0.5	3.2	3×10^{-3}	10
C	5×10^{18}	150	0.3	6.8	7×10^{-4}	3
			4 K	25 K	4 K	4 K
D	2.5×10^{17}	50	-	8.2	-	-
A	2×10^{18}	50	70	8.0	1×10^{1}	4×10^{2}
B	3×10^{18}	190	7	5.0	1	23
C	5×10^{18}	150	4	18	3×10^{-3}	4

In summary, Ohmic contacts to ZnSe/ZnMgSe heterostructures with a ZnSe QW can be experimentally established by epitaxial doping combined with *in-situ* Al metallization. We observe a high sensitivity of the contact resistance on the carrier concentration in the barrier, attributed to a change of the tunnel resistance. We independently verify this for a manipulation of electron transport and concentration through temperature and doping control, respectively. The regime of Ohmic contacts where tunnel current dominates is reproducibly reached for a ZnMgSe barrier doping concentration $n > 1 \times 10^{18}$ cm^{-3} above the critical density of the MIT, where we report a minimal ρ_c of about 1×10^{-2} Ω cm^2. Further reduction of contact resistivity by post metal anneal is not achievable within the thermal budget.

3.6. CONCLUSIONS

Goal of this chapter was demonstration of a low temperature n-type Ohmic contact to ZnSe heterostructures with ρ_c below $1 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$ (4 K). Meeting this criterion motivated in Chap. 2.2 allows for compatibility with spin qubit operation. My work addresses the challenge in contacting wide band-gap ZnSe (ZnMgSe) by a comprehensive experimental study of state of the art fabrication techniques by means of substrate doping, selection of contact material, deposition technique and interface treatment. The classical Schottky metal-semiconductor contact is tuned to an Ohmic regime using fabrication techniques with high process control and reproducible output, see Chap. 5. As characterization method, IV profiling at both RT and 4 K combined with TLM structures was chosen to assess the contacts in terms of ρ_c and for the substrates van der Pauw Hall measurements to assess ρ_b and μ. This study covers contacting of both bulk and heterostructure substrates consisting of II-VI materials ZnSe and ZnMgSe. We provide a detailed summary of all results on contact resistivity in Tab. A.3.

ELECTRIC CONTACTS ACHIEVED BY EX-SITU DOPING TECHNIQUES: IMPLANTATION OR DIFFUSION

Regarding doping of the semiconductor, three approaches were pursued, implantation, diffusion and epitaxial doping of ZnSe. In the first project phase, subject of investigations was doping *ex-situ* by diffusion or implantation applied to undoped ZnSe substrates with the following outcomes. For diffusion contacts, no reference measurement prior to annealing is possible, since the annealing step ultimately activates the contact.

For implantation contacts, damage from ion bombardment remains irreversible since out-diffusion of Zn, evidenced by our experiments and those reported in the literature, counteracts carrier activation during annealing. In our experiments, the contact resistivity is limited to a level of about $\rho_c \sim 1 \times 10^7\,\Omega\,\mathrm{cm}^2$ at RT, see Sect. 3.3.2.

For diffusion contacts, the very same process of out-diffusion limits the contact resistivity at a level of $\rho_c > 0.01\,\Omega\,\mathrm{cm}^2$, see Sect. 3.3.1. Compared to ρ_c of implanted contacts, the difference originates from starting the annealing with an pristine crystal in the case of diffusion contacts and different doping material. We remark as a side note, that diffusion provides a poor degree of process control, which includes some risk for reduced yield.

Both doping processes rely on annealing counteracted by out-diffusion, limiting the net free charge carrier concentration. We find for both techniques ρ_c at a level of $\rho_c > 0.01\,\Omega\,\mathrm{cm}^2$ which is incompatible with requirements for operating spin qubits. To our knowledge, outgassing of Zn measured by i.e. optical or electrical methods has not been observed or considered relevant only at temperatures higher than 300 °C in the literature. Availability of a reduced thermal budget of 200 °C for defect free II-VI processing suggested (Sect. 5.5) might be interpreted as result of increased sensitivity of our measurement technique: The ZnSe-metal contact is highly sensitive to the free carrier concentration near the contact interface, compared to other approaches probing PL or trans-conductance in either a larger volume or IV profiling at overall higher resistivities.

We conclude, doping by implantation and diffusion is incompatible with low resistivity n-type Ohmic contacts to ZnSe, as out-diffusion of Zn cannot be suppressed.[17] Both *ex-situ* doping processes, thermally activated crystal healing following ion implantation or in-diffusion of dopants, require annealing processes exceeding the thermal budget of ZnSe. We conclude, that *ex-situ* doping processes, that are well established for the III-V and group IV material platforms, are not compatible with Ohmic contact formation to ZnSe (II-VI) as the thermal budget for group II-VI material is significantly lower. In consequence, non-invasive epitaxial doping is identified as favourable doping technique.

OHMIC CONTACTS ACHIEVED BY EPITAXIAL DOPING

Epitaxial doping with Cl during MBE growth, firstly established for ZnSe about three decades ago, yields highly doped n-ZnSe. From early on, record low resistivity ZnSe-metal contacts were realised on epitaxially doped n-ZnSe substrates [49, 78]. Setting the focus on low temperature performance ($T \leq 4\,\mathrm{K}$), this work addressed further optimization of ρ_c in this system.

For *ex-situ* processing, a study of various contact materials and interface treatments revealed high dependence of ρ_c on the semiconductor surface. We find a with low reproducibility of ρ_c, attributed to nanoscopic variances of the metal-semiconductor interface resulting from removal of native oxide by *ex-situ* processing. Ohmic contact formation is hindered by a tunnel barrier resulting either from native oxide or defects introduced by dry or wet etching.[18] Best results are achieved for Al contacts deposited *ex-situ* on bulk ZnSe with $\rho_c \geq 0.01\,\Omega\,\mathrm{cm}^2$, see Tab. 3.4. The results were hard to reproduce and not within the target regime $\rho_c < 0.01\,\Omega\,\mathrm{cm}^2$ although tunneling is a relevant transport mechanism.

Significant and reproducible reduction of ρ_c by two to three orders of magnitude could be shown for various metals by transition from *ex-situ* to *in-situ* processing, see Tab. 3.4 and 3.5. The reduction in ρ_c originates from absence of oxide at an almost ideal semiconductor-metal interface guaranteed by non-invasive fabrication, including both doping and contacting *in-situ*. Besides Mg, Al can be identified as ideal contact material with ρ_c as low as $2 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ at RT and $4 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ at 4 K. We assign tunneling as the dominant transport mechanism at the metal-semiconductor contact. Experimental evidence is a linear IV profile obtained at 4 K, where thermal transport is fully suppressed. For a given contact metal, in our case Al, ρ_c is expected to scale with the maximally available free carrier concentration, that is lower for group II-VI materials compared to group III-V or group IV materials [47, 89]. We have optimised the system featuring the lowest ρ_c of contacts to n-ZnSe reported in

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[17] Non-trivial methods like creation of a liquid or gaseous environment with partial Zn over-pressure are required to suppress out-diffusion [53, 112].

[18] Wetchemical treatment was found not to result in a reduction of ρ_c in a reproducible way.

the literature, with physically low potential for further reduction of ρ_c. As tunneling, the dominant transport mechanism at the contact, is not thermally activated, our contact approach is assumed compatible with novel, all electrical quantum devices operating at cryogenic temperatures. Still, the presented fabrication method of *in-situ* contacts lacks the possibility for local doping outside the region of the active device, i.e the qubit region in the case of spin qubits. We address the challenge of local control on the doping by two approaches, one being selective doping by regrowth and the second remote doping of QW structures.

OHMIC CONTACTS BY LOCAL DOPING IN A SELECTIVE REGROWTH PROCESS

In Sect. 3.4.2, local Ohmic contacts with low ρ_c=$1.4 \times 10^{-3}\,\Omega\,\mathrm{cm}^2$ at 4 K to a ZnSe HS are demonstrated. For the regrowth process, we obtain high crystal and interface quality by multi step etching performed *ex-situ* and *in-situ* before regrowth and metallization *in-situ*. However, due to technical limitations of etching precision, transfer of the regrowth process from thick channels to HS with a 10 nm thick QW is not possible.

OHMIC CONTACTS TO A ZNSE QW UTILIZING REMOTE DOPING

As discussed above in Sect. 3.3 and 3.5, II-VI bulk and II-VI heterostructures substrates with a QW can be contacted by In diffusion or *in-situ* deposited Al given a certain doping concentration, see Figs. 3.6, or Fig. 3.15, respectively. In perspective, however, utilization of II-VI substrates hosting dopants conflicts the requirement of a defect free qubit environment (see Chap. 2.2). On the downside, for undoped structures, the Schottky model predicts wide tunnel barriers and correspondingly unacceptably large ρ_c. As a compromise, we realise low contact resistivities to QW structures (RT/ 4 K) achieved by epitaxial doping of the ZnMgSe barrier above the QW. Resulting ρ_c is close to the target regime of ρ_c<$1 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$, see Fig. 3.14. It is to be noted that we will see in Chap. 6 that reduction of ρ_c by barrier doping expectably conflicts electric control of the potential landscape in the device.

CONCLUSION AND DISCUSSION

The combined experimental results on the contact resistivity obtained by the different fabrication techniques I investigated are composed in Tab. A.3. My best results for *in-situ* fabricated low resistivity contacts to bulk n-ZnSe are visualised in Fig. 3.16 a), in comparison to literature values [5, 78, 113]. In summary, we find a dependence of ρ_c on doping concentrations at the semiconductor-metal interface in agreement with the physics of a Schottky contact. For local Ohmic contacts no results were published so far by groups other than ours, see Fig. 3.16 b) [5]. As a consequence of lower doping we find lower ρ_c for our regrowth method.

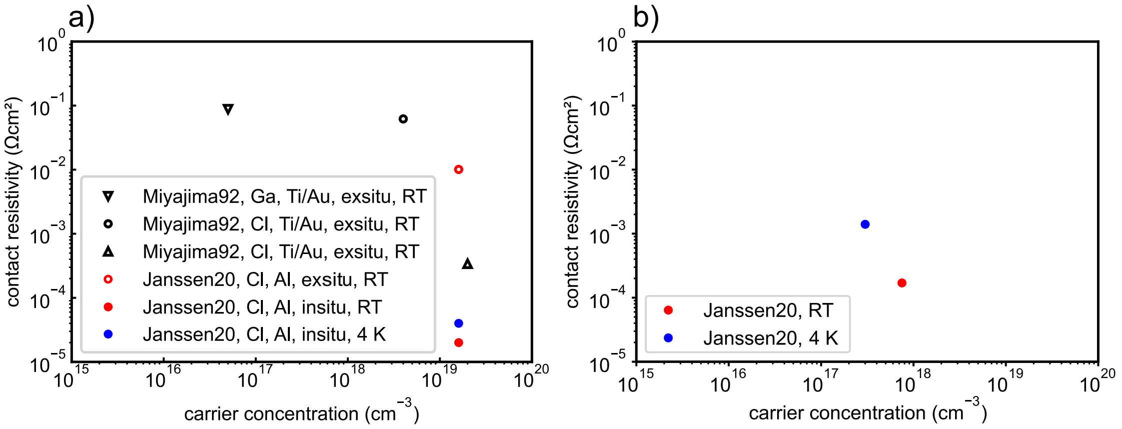

Figure 3.16: Specific contact resistivities for n-type ZnSe. a) Results for metal contacts to n-type bulk ZnSe with a carrier concentration as shown [5, 78]. The contact metal and deposition mode (*ex-situ*/*in-situ*) and measurement temperature is specified in the legend. b) Specific contact resistivity for local contacts to n-ZnSe [5, 105].

In the contact region, the carrier concentration set by epitaxial doping is prone to *ex-situ* processing or reduction by p-type Zn vacancy generation when the thermal budget of about 200–250 °C is exceeded. In addition, the tunnel barrier is substantially higher in presence of interface oxides, why *in-situ* fabrication of contacts is the preferable process. From experiments including various types of surface preparation we can conclude the sc-metal interface is most crucial for the contact quality to highly doped n-ZnSe, in alignment with literature results [78]. Contact resistivity increases whenever the interface quality is degraded, i.e by formation of a native oxide or *ex-situ* processing. This is evident from a direct comparison of contact resistivities fabricated *in-situ* or *ex-situ* indicating the presence of an enlarged tunnel barrier when an oxide or crystal defects are involved. The main result of this extensive material and process study is the excellent quality of Ohmic contacts to doped ZnSe/ZnMgSe devices based on *in-situ* deposited contacts, with Al as favourable contact material. The contact resistivity of $4 \times 10^{-5}\,\Omega\,\text{cm}^2$ determined for 4 K well is compatible with spin-qubit operation considering unused potential for miniaturization. With our findings we down-correct the recommended temperature budget for processing of ZnSe[19] to temperatures as low as 200 °C.

Still, the intensive study on contacting ZnSe did not provide a solution offering low resistivity contacts ($\rho_c < 1 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$) compatible with local doping as technical (Sect. 3.4.2) or physical limitations (Sect. 3.3.1) are reached for each technique proposed. Realization of local doping yielding low resistivity contacts, is a key challenge in exploration of novel all-electrical (quantum) devices in the II-VI material system. We take the first step towards local low resistivity contacts by demonstration of a selective regrowth approach, encountering limits in *ex-situ* fabrication when transitioning from bulk to QW substrates. Two decades of advances in nanofabrication predominantly in the field of superconducting qubits and nanowire technology led to exploration of selective growth and doping techniques based on shadow wall lithography, enabling all-*in-situ* fabrication [113–117]. Results of the transfer of shadow-mask lithography to the II-VI material system are presented in the last chapter of my work, see Chap. 7.

CONTRIBUTIONS

Johanna Janßen contributed to fabrication, experiment and analysis as phd student, with major contributions in development of the regrowth process and annealing process of In contacts. Christian Kamphausen, Till Huckemann and Benjamin Zenz contributed as master students in the following way: Christian Kamphausen contributed by electrical characterization of bulk ZnSe samples. Till Huckemann characterised *in-situ* fabricated contacts and the regrowth process by electrical measurements on bulk samples. Benjamin Zenz evaluated contact properties of both bulk samples and heterostructures including gated Hall-bar measurements. Valuable support was given by Malte Neul in configuration of the finite element solver and Till Huckemann in verification of the output. Johanna Janßen performed electrical measurements of Indium diffusion contacts and implanted contacts and further annealing experiments. Nils von den Driesch and Johanna Janßen performed van der Pauw Hall measurements. Lars Schreiber supervised transport measurements.

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[19] For experimental conditions of forming gas anneal for several minutes.

4

ELECTRON TRANSPORT IN ZNSE AND ZNMGSE

In this chapter, we start with a discussion on electrical transport in ZnSe (Sect. 4.1.1) to identify the relevant transport mechanisms later.[1] Aware of aiming for realization of a high mean free path >35 nm (Sect. 2.2.6), required for definition of quantum dots for electron confinement, we start with the more general case of bulk transport before investigating a 2DEG. Donor atoms can have a major influence on the electron's mean free path and induce metallic behaviour, thus knowledge on the critical density of the metal insulator transition $n_{\mathrm{c,MIT}}$ is important for the choice of doping concentration in the contact regions. In contrast, doping concentration in the QD region should be kept at a minimum. Therefore, I introduce the relevant models for the de-

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[1] Targeting low resistivity ohmic contacts, I put focus on the doping concentration, required to be above the concentration of the MIT. After discussions with Benjamin Zenz, I initiated a quantitative study of the MIT in ZnSe, which later became a main part in the master project of Benjamin Zenz. Benjamin Zenz conducted literature research, theory revision and data analysis. I contributed mainly in form of the acquisition of suitable data sets provided by the collaborators at PGI 9. Lars Schreiber supervised the data analysis and comparison to theory - outlined in the beginning of this chapter (Sect 4.1).

Throughout the research project electron transport in bulk ZnSe and ZnMgSe has been continuously monitored by the research team. All vdP Hall measurements have been conducted by the collaboration partners at PGI 9, namely Johanna Janßen, Nils von den Driesch and Benjamin Bennemann. Measurement analysis has been carried out by Johanna Janßen, Nils von den Driesch, Benjamin Zenz and by me, from which a selection is shown in Sect. 4.2. Error analysis for the experimental results has been carried out by me (Apx. A.2).

Experimental assessment of electron transport in 2DEGs (Sect. 4.3) is based on the same experimental and analytical methods also used for bulk ZnSe (ZnMgSe) in Sect 4.1. Johanna Janßen performed additional experiments under optical excitation for some samples, where otherwise no electrical contact could be realized at T<=30 K. I contributed to data analysis by introduction of a two channel model, relating experimental transport data from the 2DEG to that of the bulk material. Assessment of the transport mechanisms and the mean free path was supervised by Lars Schreiber.

scription of the Metal Insulator Transition (MIT) for (un)doped semiconductors in Sect. 4.1.2.

The experimental method for characterization of electrical transport is temperature dependent van der Pauw Hall mobility measurements, discussed in Sect. A.2. For assessment of the MIT, we assign the material either to the metallic or insulating side of the MIT.

With this analysis method applied we provide the experimental basis for assessment of electrical transport, see Sect. 4.2. Since metallic properties are required for the fabrication of ohmic contacts to ZnSe/ZnMgSe heterostructures operating at $T = 4\,\mathrm{K}$ (Chap. 3), we also determine the position of the MIT individually for the materials ZnSe and ZnMgSe, see Sect. 4.2.2.

Having discussed electron transport in the bulk, we can further investigate transport in a localised system, the 2DEG confined in an undoped ZnSe QW. We investigate very basic devices without gate control (Sect. 4.3), restricted by technological limitations. Finally, a summary of all characterization results and conclusions is provided in Sect. 4.4.

4.1. MODELS

Here, I introduce the main concepts used for the evaluation of electron transport. At first, a theoretical description of bulk transport in ZnSe solving the Boltzmann equation is depicted (Sect. 4.1.1) based on the work of Ruda et al. [118]. Second, different approaches to the MIT are discussed (Sect. 4.1.2).

4.1.1. ELECTRICAL TRANSPORT IN BULK ZNSE

The most complete description of electron transport in n-type bulk ZnSe was formulated by Ruda, who pointed out the relevance of longitudinal optical phonons for the piezoelectric semiconductor ZnSe [118]. With a variational method the electron mobility for ZnSe was derived from the Boltzmann transport equation. The temperatures considered are room temperature and 77 K, close to the temperature of maximal mobility for samples with non-degenerate doping [118]. In first approximation, the current $J = \sigma\mathbf{E}$ is the product of conductivity σ in presence of an electric field $\mathbf{E}$ [118]. The method includes a description of donors and acceptors, also covering (strongly) compensated systems where n and p type carriers compensate and lead to an effective reduction of the majority charge carrier density. Relevant scattering mechanisms considered are scattering with phonons, impurities, and other carriers [118]. For elastic scattering, as applicable to scattering with acoustic and piezoelectronic phonons and ionised impurities, the Boltzmann equation can be written in the relaxation-time approximation [118]

$$\left(\frac{\partial f}{\partial t}\right)_{\mathrm{coll}} = -\frac{\partial f}{\tau(\epsilon)}, \quad \partial f = f(k) - f_0(\epsilon). \tag{4.1}$$

Here, $f(k)$ denotes the distribution of momentum in the system, which reacts to

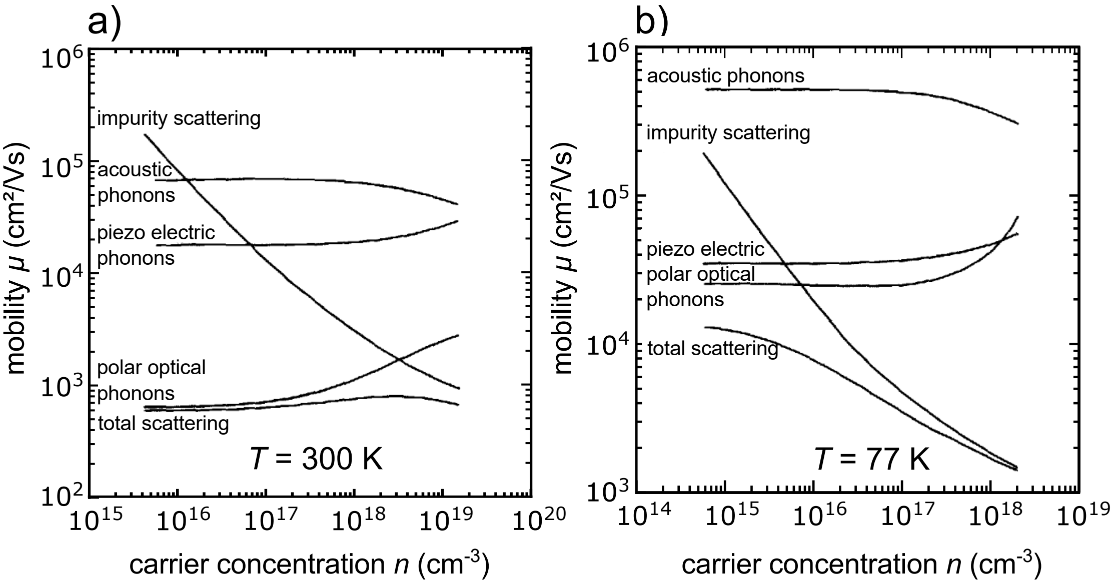

Figure 4.1: Theoretical prediction of electron transport in bulk ZnSe. Theoretically predicted mobilities for electrons in ZnSe at a) RT and b) 77 K, for ideal crystals without compensation. Figure adopted from Ref. [118].

external forces/perturbations on a time scale τ, the relaxation time for a scattering process for given momentum k and energy ϵ. The undisturbed distribution is $f_0(\epsilon)$. Using Fermi's Golden Rule for the calculation of scattering processes with a probability $P(k,k')$ for a change of momentum from k to k', one finds an expression for the relaxation time [118]

$$\frac{1}{\tau} = \frac{\Omega}{4\pi^2} \int_{k'} \int_{z=-1}^{1} (1-z) P(k,k') k^2 dk' dz. \tag{4.2}$$

Here, Ω denotes the integration volume and z the 3rd room coordinate. For acoustic phonons of energy E one finds the scattering time scales with the acoustic deformation potential ϵ_1 as follows [118]:

$$\frac{1}{\tau_{\text{acoust}}} \propto T\epsilon_1^2\sqrt{E} \tag{4.3}$$

The free charge carrier concentration n is the difference of the concentration of donors N_d^+ with activation energy E_d and acceptors N_a^- at a given temperature T [118]

$$\begin{aligned} N_\mathrm{d}^+ &= N_\mathrm{d}\left(1+2e^{\frac{E_\mathrm{d}+E_\mathrm{f}}{k_\mathrm{b}T}}\right)^{-1} \\ N_\mathrm{I} &= N_\mathrm{d}^+ + N_\mathrm{a}^- \\ n &= N_\mathrm{d}^+ - N_\mathrm{a}^- . \end{aligned} \tag{4.4}$$

Here, E_f denotes the Fermi level and k_b the Boltzmann constant and $N_\mathrm{d}, N_\mathrm{a}$ the concentration of the sum of ionised and neutral donors or acceptors, respectively. The concentration of ionised impurities is denoted as N_I. Impurity scattering is temperature dependent, and scales with N_I [118]

$$\frac{1}{\tau_\mathrm{imp}} \propto N_\mathrm{I} E^{\frac{-3}{2}} \mathscr{L}\left(\frac{E}{\beta_\mathrm{s}}\right) \tag{4.5}$$

using the following expressions [118]:

$$\begin{aligned} \mathscr{L} &= \frac{\sqrt{8}e^4 F(b)}{65\pi\epsilon_0 m_0^*} \\ F(b) &= ln(1+b) - [b/(1+b)] \\ b &= \frac{8m_\mathrm{e}E}{\hbar^2\beta_\mathrm{s}^2} \\ \beta_\mathrm{s}^2 &= \frac{ne^2}{\epsilon_0 k_\mathrm{b} T}\frac{\mathscr{F}_{-\frac{1}{2}}(\eta)}{\mathscr{F}_{\frac{1}{2}}(\eta)} \\ \mathscr{F}_{\frac{1}{2}} &= \frac{2}{\sqrt{\pi}}\int_0^\infty \frac{\epsilon^{\frac{1}{2}}d\epsilon}{1+exp(\epsilon-\eta)} \end{aligned} \tag{4.6}$$

Here, L is a logarithmic function that depends on E and $\beta_\mathrm{s}\left(\mathscr{F}_{-\frac{1}{2}}(\eta), \mathscr{F}_{\frac{1}{2}}(\eta)\right)$, where $\eta = \frac{E_\mathrm{f}-E_\mathrm{c}}{k_\mathrm{b}T}$ denotes the argument of the Fermi distribution and $\mathscr{F}_{\pm\frac{1}{2}}(\eta)$ the Fermi integral. The piezoelectric scattering time scales like [118]

$$\frac{1}{\tau_\mathrm{piezo}} \propto \frac{T^2}{E}. \tag{4.7}$$

Based on the solutions of the transport equation a final expression for the mobility as a function of free carrier concentration can be numerically derived, shown in Fig. 4.1. At room temperature, electron scattering at polar optical phonons or at ionised impurities, is dominant for high carrier concentration ($n > 3 \times 10^{18}\,\mathrm{cm}^{-3}$), see Fig. 4.1 a). In absolute numbers, electron mobilities of 600–800 $\mathrm{cm}^2/\mathrm{Vs}$ are predicted. Similarly, Fig.4.1 b) depicts predicted mobility and scattering mechanisms for 77 K. This temperature is chosen for it is close to the temperature where maximal mobility is observed for real samples featuring n as low as 1×10^{15}–$1 \times 10^{16}\,\mathrm{cm}^{-3}$

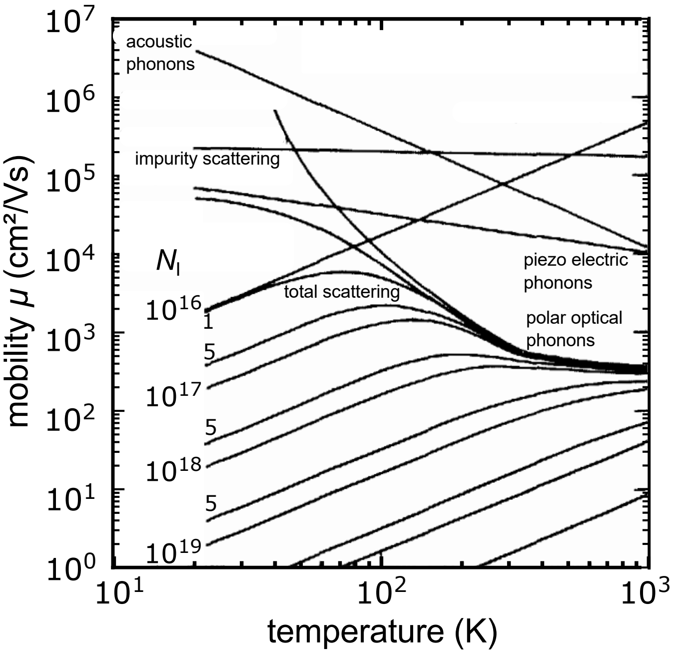

Figure 4.2: Reference model for the temperature dependent electron mobility in bulk ZnSe. Calculation for high quality ZnSe, assuming K=0 and η=-6 to ensure totally nondegenerate statistics. Lines denoted with N_I represent calculations for a fixed impurity concentration. Figure adopted from Ref. [118].

[112, 118]. Compared to RT, the same mechanisms limit mobility, but phonon scattering is weaker because the phonon density is lower at 77 K. In consequence, mobilities can reach up to $1 \times 10^4\,\mathrm{cm}^2/\mathrm{Vs}$ [118]. For n exceeding the carrier concentration of crystals with high purity, ionised impurity scattering becomes dominant ($n > 8 \times 10^{15}\,\mathrm{cm}^{-3}$) [112, 118].

Addressing crystal purity, the compensation θ is introduced to this model, defined by the ratio of charged acceptors N_a^- and donors N_d^+ [118]

$$\theta = \frac{N_\mathrm{a}^-}{N_\mathrm{d}^+}. \tag{4.8}$$

A related parameter, K, is often specified, defined as [118]

$$K = \frac{N_\mathrm{I}}{n} = \frac{N_\mathrm{d}^+ + N_\mathrm{a}^-}{N_\mathrm{d}^+ - N_\mathrm{a}^-} = \frac{1+\theta}{1-\theta}. \tag{4.9}$$

K and θ are related, since N_I and n are the difference or sum of N_a^- and N_d^+, respectively, see Eq. 4.4. By definition, the degree of compensation K (θ) can range from 0 to 1 (0 - ∞).

In short, compensation leads to a reduction of n at a given level of N_I that can be thus screened less efficiently and scattering increases [118]. The simulation results for different degrees of compensation can be looked up in Apx. A.10 [118]. Since we expect a low degree of compensation in our MBE grown samples (Chap. 5), the full temperature dependence of the electron mobility in high quality crystals, as predicted by the reference model for K=0, is relevant for the following investigation of electron transport (Fig. 4.2) [118]. The dominant scattering mechanism at $T \leq 80\,\mathrm{K}$ is impurity scattering, if $N_\mathrm{I} > 1 \times 10^{16}\,\mathrm{cm}^{-3}$, and piezoelectric phonon scattering for lower N_I.

4.1.2. MIT THEORY

Semiconductors exhibit variable and controllable levels of conductivity, that ranges from full isolation to metallic conduction. A system is said to be metallic if the conductivity in a semiconductor remains non-zero in the absence of thermal excitation, whereas it becomes zero in an insulator [119]. Bandgap energy, temperature, disorder and carrier concentration can strongly affect the conductivity. The MIT is the state, where the system turns from isolating to conducting properties, which can be obtained by different mechanisms to be introduced in this section, namely electron correlations based on a hopping model and disorder disturbing the band structure. This will lead us to the definition of the Mott criterion, at which the MIT occurs, utilizing the simple but quite universal hydrogen model. For this work, knowledge of the position of the MIT is relevant for design and fabrication of devices.

HYDROGEN MODEL

In the group II-VI semiconductor ZnSe, for introduced Cl atoms one of the seven valence electrons is not covalently bound to the Cl. The remaining electrons effectively sees one positive charge of the nucleus, to which it is attracted, a situation similar to the hydrogen atom. The binding energy E_H and orbit radius of donor bound electrons a_H^* can be derived using the hydrogen model introduced by Bohr. The movement of an electron in a semiconductor is described using Planck's constant h, the (effective) electron mass m_e (m_e^*), and the (relative) dielectric constant ϵ_0 (ϵ_r). From a semiclassical approach with an electron with charge e orbiting around a positive charge one obtains for the ground state energy[120]

$$E_\mathrm{H} = -\frac{\mathrm{e}^4 m_\mathrm{e}}{8\epsilon_0^2 h^2}\frac{m_\mathrm{e}^*}{m_\mathrm{e}\epsilon_\mathrm{r}^2} = -13.6\,\mathrm{eV}\frac{m_\mathrm{e}^*}{m_\mathrm{e}\epsilon_\mathrm{r}^2}. \tag{4.10}$$

Here, the prefactor of −13.6 e V represents the Rydberg constant for hydrogen, and the second factor corrects for a different dielectric environment and effective electron mass in semiconductors. For ZnSe, one obtains 27 me V as donor energy, taking realistic parameters into account (ϵ_r = 8.6 and m_e^*=0.145m_e, see Tab. A.2) [98, 121]. As E_H is typically small and thus electrons can easily be for example thermally excited to the conduction band, one speaks of shallow donors, such as Cl in ZnSe [122].

Similarly, one obtains for the radius of the orbiting electron [120]:

$$a_{\mathrm{H}}^{*} = \frac{4\pi\epsilon_0\hbar^2}{m_{\mathrm{e}}\mathrm{e}^2}\frac{m_{\mathrm{e}}\epsilon_{\mathrm{r}}}{m_{\mathrm{e}}^{*}} = 0.529\,\text{Å}\frac{m_{\mathrm{e}}\epsilon_{\mathrm{r}}}{m_{\mathrm{e}}^{*}} \tag{4.11}$$

Here, the prefactor 0.529 Å corresponds to the Bohr radius of a hydrogen atom. For ZnSe one obtains an effective Bohr radius of 3.1 nm with the same material constants specified above.

MOTT-HUBBARD TRANSITION

In the Hubbard model, electron-electron correlations are addressed by a repulsive Coulomb potential contributing with an energy U per additional electron. One considers a semiconductor with singly occupied states, such as donor states are. Electron transport is then possible in a hopping mode framework, taking tunneling probabilities, dependent also on the spin, and the number electron number per site into account. The Hamiltonian of such a system can be written as [120]

$$H = \sum_{\mathrm{i,j},s} t_{\mathrm{j,i},s} c_{\mathrm{j},s}^{\dagger} c_{\mathrm{i},s} + U \sum_{i} n_{i,\downarrow} n_{i,\uparrow}. \tag{4.12}$$

Here, $t_{\mathrm{j,i},s}$ denotes the tunnel probability for an electron with spin s to move from site i to site j. The electron number of a site i is described by $n_{\mathrm{i},s} = c_{\mathrm{i},s}^{\dagger} c_{\mathrm{i},s}$, where $c_{\mathrm{i},s}$ and $c_{\mathrm{i},s}^{\dagger}$ are the creation and annihilation operators for electrons, respectively. In an energy or band diagram of a semiconductor, where all donor sites are occupied by one electron, all electrons populate the lower band, whereas the population of the higher band separated by U is zero. The density of states (DOS) for such system is depicted in Fig. 4.3. Dependent on the donor density or inter-atomic spacing a, the DOS broadens as the sites move closer [123]. At some point, the lower and upper band touch, resulting in some finite occupation of the upper band. This is the moment, where the systems turns from insulating to metallic, reproducing the behaviour of the MIT by doping.

Next, we will discuss for a mechanism other than electronic correlations, namely disorder, how the MIT can be understood.

MOTT-ANDERSON TRANSITION

The MIT can also be driven by disorder introduced by various mechanisms like impurities and crystal stacking faults, but also by charged donors. Donors like Cl in ZnSe, sit in this case at the anionic site in the crystal, at random and not periodically distributed positions. Hence, the crystal periodicity, which is a requirement for the Bloch formalism, is disturbed [120]. The atoms introduce local potential variations, and thereby act as (shallow) trap states, as described by the hydrogen model (Sect. 4.1.2) for a localised electron. Depending on the depth and overall distribution of all potential perturbations, electrons populate localised or extended states. At zero temperature, without thermal excitation, only the later contribute to conductivity, i.e. a metallic (insulating) behaviour requires (un)populated extended states. This

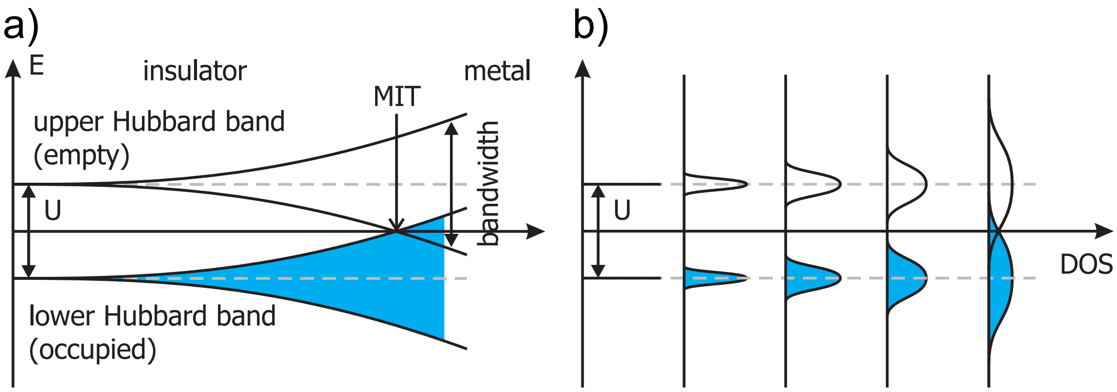

Figure 4.3: The Mott-Anderson transition based on hopping. a) Energy diagram for a system with increasing electronic correlation. The two bands are separated by the Coulomb energy U. As interactions increase, the bands broaden and touch as the MIT is approached. b) Different representation of in terms of the DOS. Figure adopted from Ref. [120, 123].

dependence on conductivity on disorder is the characteristic of the MIT induced by localisation, firstly formulated by Anderson [124].

In the DOS localisation leads to discretization of energies, see Fig. 4.4. Localised (extended) states have energy lower (higher) than the so called mobility edge E_μ [120]. A similar pictures of disordered systems are provided by scaling theory, or the concept of percolation theory [125]. The term percolation threshold is used, when a conductive path through a material does exist. This is the case for if the carrier concentration exceeds the percolation threshold n_p, at which a MIT occurs, discussed in detail later (Sect. 4.1.2). Next, both approaches can be combined, the Mott-Hubbard model and the Mott-Anderson model, to provide a complete picture of the MIT in 3D.

MOTT CRITERION

In the sections above we have seen how electronic correlations and disorder can induce the MIT. In real samples, both effects are present, motivating a combined theory based on the Mott-Hubbard transition and Mott-Anderson transition [123]. The main idea is, that the electron mean free path equals at least the mean inter-donor spacing, known as Ioffe-Regel criterion [120]. This leads to the Mott criterion, a quite simple expression for the critical density n_c in a 3D system [123]:

$$n_c^{1/3} \cdot a_\mathrm{H}^* \approx 0.25 \tag{4.13}$$

The very same expression is provided by percolation theory [126]. Simply spoken, the critical density is reached, when the electrons confined to a volume described by the effective Bohr radius, touch. It is to be noted, that the exact value of the proportionality constant of the Mott criterion is debatable, as several assumptions enter [119].

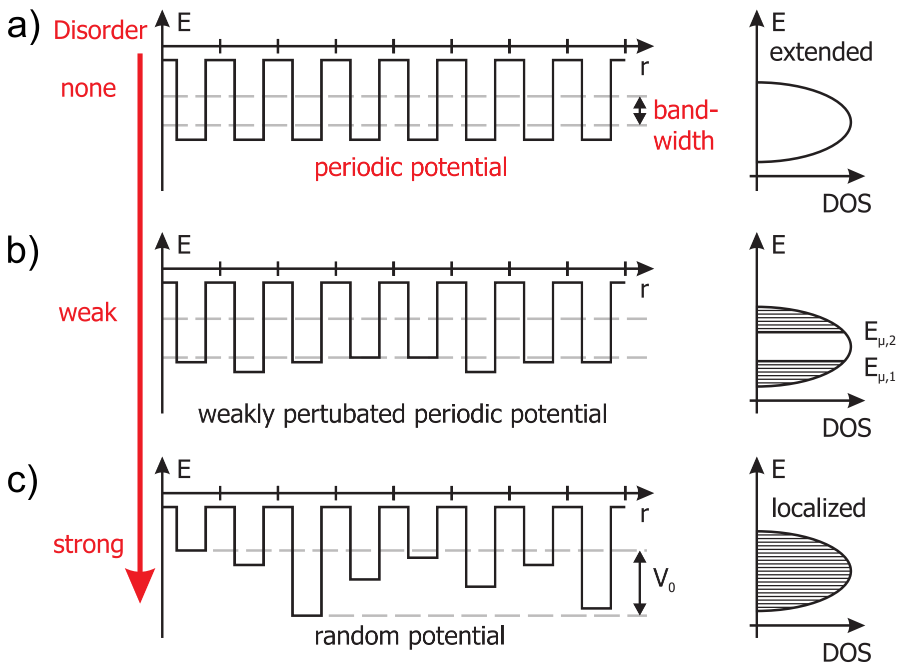

Figure 4.4: The Metal Insulator Transition in the Anderson model based on disorder induced localisation. a-c) As disorder in the system increases, increasing parts of the DOS correspond to localised states, depicted as lines. b) The threshold energy for localisation in the lower (upper) part of the impurity band is the mobility edge $E_{\mu,1(2)}$. c) For highly disordered systems with random potential, the mobility edges merge and extended states vanish. Figure adopted from Ref. [120].

Validity of the hydrogen model for semiconductors and metals has been experimentally verified for a very broad range of materials. Universality of the Mott criterion is high, since it correctly describes a broad range of materials, from semiconductors to metals, spanning many orders of magnitude for critical densities. Fig. 4.5 depicts n_c for Bohr radii ranging from 1 to 1×10^3 Å. Notably, the experimentally verified literature value for ZnSe and the theoretical expectation value for MgSe are indicated at $n_c = 4 \times 10^{17}$ cm^{-3} and 1.6×10^{18} cm^{-3}, respectively [122, 127].

For ternary systems, such as ZnMgSe, one can deduce material parameters, such as the lattice constant a, by linear interpolation following the empirical description by Vegard's law [128]:

$$a(\mathrm{Zn}_{1-x}\mathrm{Mg}_x\mathrm{Se}) = (1-x)\cdot a(\mathrm{ZnSe}) + x\cdot a(\mathrm{MgSe}) \tag{4.14}$$

In specific, for the lattice constant of $\mathrm{Zn}_{0.8}\mathrm{Mg}_{0.2}\mathrm{Se}$ embedding the QW in the final device, one obtains 0.5713 Å [121]. We apply this method to estimate the lattice constant and band gap energy of ZnMgSe, since for simulations of pseudo-potentials and some experimental work, a linear composition dependence for the electronic band

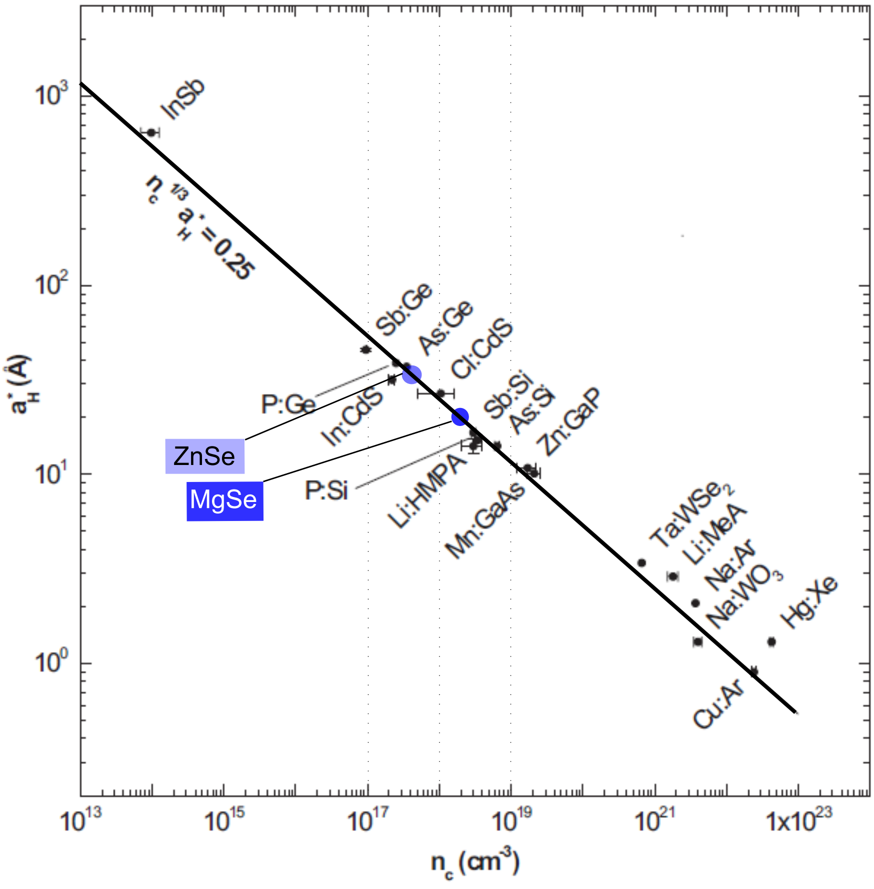

Figure 4.5: The MIT for various material systems in terms of the hydrogen model. Effective Bohr radius determined by the hydrogen model versus critical density of the MIT. Theoretical predictions for ZnSe and MgSe are indicated. The solid line represents the Mott-criterion (proportionality constant 0.25). Figure adopted from Ref. [120].

structure of ZnMgSe is found [129, 130]. Applicability of Vegard's law to ZnMgSe, a linear scaling of the lattice constant or band gap energy with composition, is most likely given, although debated in the literature [130, 131].

PERCOLATION THEORY FOR BULK AND 2DEGS

Percolation theory provides an alternative description (although similar to the Anderson-Mott transition, Sect. 4.1.2) for disordered systems. The system becomes conductive, when the free carrier concentration exceeds the percolation threshold n_p. Taking screening of the disorder potential into account, one defines a characteristic travel distance, that relates to a mobility for the given charge carrier distribution [55]. One finds an exponential expression for the longitudinal conductivity σ_xx

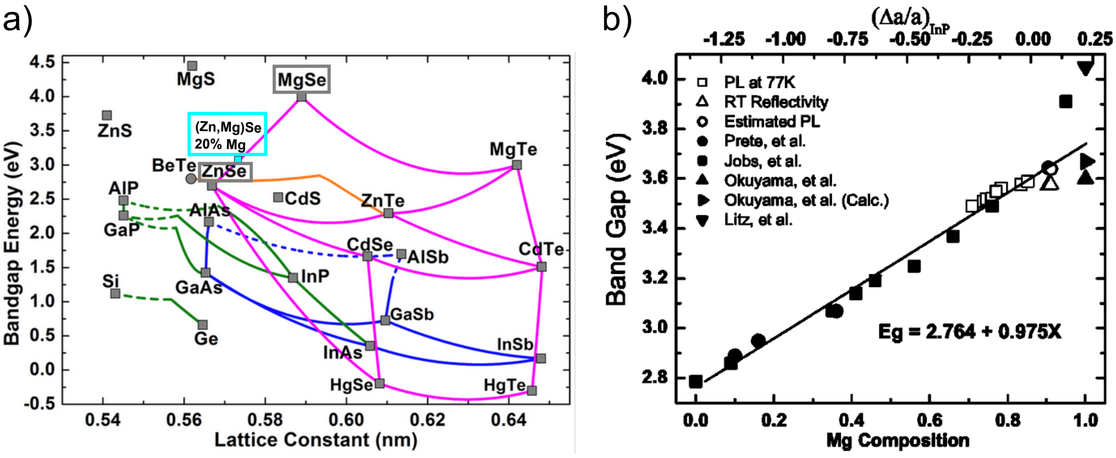

Figure 4.6: Bandgap versus lattice constant for Zincblende semiconductors. a) Theoretical prediction for band gap energy for various Zincblende semiconductors obtained by DFT [132]. b) Experimental study of the bandgap ZnMgSe as a function of x_Mg linear in lattice mismatch [130]. Figures in panels a) and b) are adopted from Ref. [132] and Ref. [130], respectively.

in a 2DEG derived from measurements in Si Hall-bars [55]

$$\sigma_\mathrm{xx} \propto \left(n - n_\mathrm{p}\right)^{1.31}. \tag{4.15}$$

This description requires $n > n_\mathrm{p}$, beyond which charge paddles become connected and the system is not fully governed by localised states. In consequence, a finite mobility μ_p can be observed. The exponent of 1.31 in case of 2D systems has been experimentally verified across different material platforms like electrons in GaAs, SiMOS or SiGe and holes in Ge [55, 133–136]. The absolute value of the percolation density, at which the system switches from insulating to metallic behaviour in a disorder driven MIT, allows to universally characterise the material quality [133]. For the percolation density, observed on a macroscopic scale, recent studies further suggest a direct relationship with charge noise, as experienced by a multi electron dot (SET) or spin qubits [55]. The level of charge noise experienced in these Si devices suggests a mean free path beyond the inter-qubit distance leading to two qubit fidelities allowing for fault tolerant quantum computing [55].

An alternative description of the percolation theory is based on variable range hopping, here for 3D [137]. For electrons in bulk materials at low, non degenerate, charge carrier concentrations, the current density j for an electrical field E is described by the exponential [137]

$$j(E) = j_0 \mathrm{e}^{\left(\frac{elE}{k_\mathrm{b}T}\right)}. \tag{4.16}$$

Here, j_0 denotes the current density in the limit of zero bias and l the scattering length, deduced for a parabolic DOS with a Coulomb gap around the Fermi level.

If the electronic correlations are not too weak, one finds a similar behaviour for the DOS, as depicted in Fig. 4.3. For ZnSe, correctness of the exponential (Eq. 4.16) has been experimentally shown for temperatures below 4 K [137]. For crystals with a low background doping concentration ($N_\mathrm{d} = 5 \times 10^{16}\,\mathrm{cm}^{-3}$) the scattering length was not dependent on temperature and related to the inter-donor distance [137]. However, for 2D systems in ZnSe, neither theoretical nor experimental studies of electrical transport is published in the literature, the later hindered by the contact problem at low temperature ($T < 10\,\mathrm{K}$).

To provide a comparison to the ZnSe material used in this work, I want to bring up a simpler picture for the scattering length, when fully determined by the inter-donor splitting. Assuming a typical background dopant concentration for ZnSe of 1×10^{16} cm^{-3}, the average inter-donor distance is 50 nm, similar to the scattering length reported in the literature [137]. This length is comparable to the gate pitch of 70 nm envisioned for the final EDQD.

4.2. ELECTRICAL TRANSPORT OF BULK ZNSE/ZNMGSE

Assessment of MBE grown ZnSe or ZnMgSe thin films involves material analysis after fabrication involving SIMS and XRD, see Chap. 5. In addition, we investigate electrical transport by van der Pauw Hall measurements at variable temperatures. For a detailed description of the measurement setup and measurement technique, see Apx. A.2. We identify the relevant scattering mechanisms by their characteristic temperature dependence following the theoretical model described in Sect. 4.1.1) [118].

Without gate control, electron energy and concentration are controlled by the measurement temperature or by substrate doping. Measuring the Hall voltage as a function of external magnetic field, we can deduce ρ, n and μ as a function of temperature. Based on the Mott criterion (Sect. 4.1.2) or the models described in the following, we can deduce further characteristics as the critical density of the MIT, impurity concentrations or the donor activation energy.

For variable range hopping, with a parabolic DOS that is equal to zero at E_f, one finds a temperature dependence for the sample's resistivity ρ [122]

$$\rho(T) = \rho_0 \mathrm{e}^{\left(\frac{T_0}{T}\right)^{\frac{1}{2}}}. \tag{4.17}$$

Here, ρ_0 is a proportionality constant and $k_\mathrm{b} T_0$ is to be considered as activation energy for electron transport that goes to zero when approaching the MIT. Alternatively, the free carrier concentration n can be described using non-degenerate statistics where one obtains for a single donor level [138]

$$n(N_\mathrm{a} + n)/(N_\mathrm{d} - N_\mathrm{a} - n) = g N_\mathrm{c} \cdot \mathrm{e}^{\left(\frac{E_d}{k_\mathrm{b} T}\right)^{\frac{1}{2}}}. \tag{4.18}$$

Here $g = \frac{1}{2}$ denotes the degeneracy factor. In the limit of low temperature, this equation can be typically approximated as $\log(n) \propto -\frac{E_\mathrm{d}}{2k_\mathrm{b}} \frac{1}{T}$.

Temperature dependent van der Pauw Hall measurements are conducted in ZnSe (ZnMgSe) bulk at temperatures ranging from 25–300 K. While ZnSe has been intensively studied in both theory and experiment [122, 139], transport data on ZnMgSe is only sparsely available [127, 140], especially for low temperature ($T \leq 4$ K). Our main control parameter on transport properties is the doping concentration, since utilization of the field effect is not possible facing technological limitations for the fabrication of local Ohmic contacts.

4.2.1. ELECTRICAL TRANSPORT OF BULK ZNSE

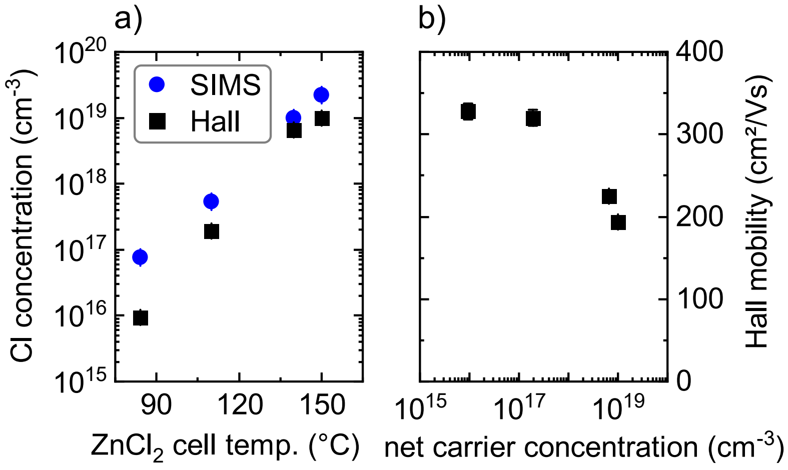

Figure 4.7: Doping calibration for epitaxially doped ZnSe:Cl. a) Doping and carrier concentration of bulk ZnSe characterised by SIMS or van der Pauw Hall measurements versus $ZnCl_2$ cell temperature. b) Electron mobility at room temperature versus $ZnCl_2$ cell temperature. Figure by Johanna Janßen [5, 105].

This section is based on a joint publication [5]. Halogens are known to be excellent donors for ZnSe and for technical reasons we prefer Cl, for which successful epitaxial doping has been reported [5, 141, 142]. Using similar growth conditions as in the latter references, we achieve Cl doping concentrations up to 2×10^{19} cm^{-3}. We confirm the doping concentration by SIMS and van der Pauw Hall as depicted in Fig. 4.7 a) [5]. Both measurements are in good agreement although the free carrier concentrations extracted from van der Pauw Hall measurements are slightly lower than the quantified doping concentrations revealed by SIMS [5]. This indicates that not all included Cl atoms are ionised and contribute to charge transport at RT [5].
Fig. 4.7 b) shows the corresponding mobilities in ZnSe:Cl we derive from the van der Pauw Hall measurements as a function of the carrier concentration [5]. At RT, we expect the prominent scattering mechanisms which limit the mobility in ZnSe:Cl to be longitudinal optical phonon scattering and impurity scattering (Sect. 4.1.1) [5, 118, 143]. Our data is in good agreement with typical literature values [5, 78, 118, 142]. The

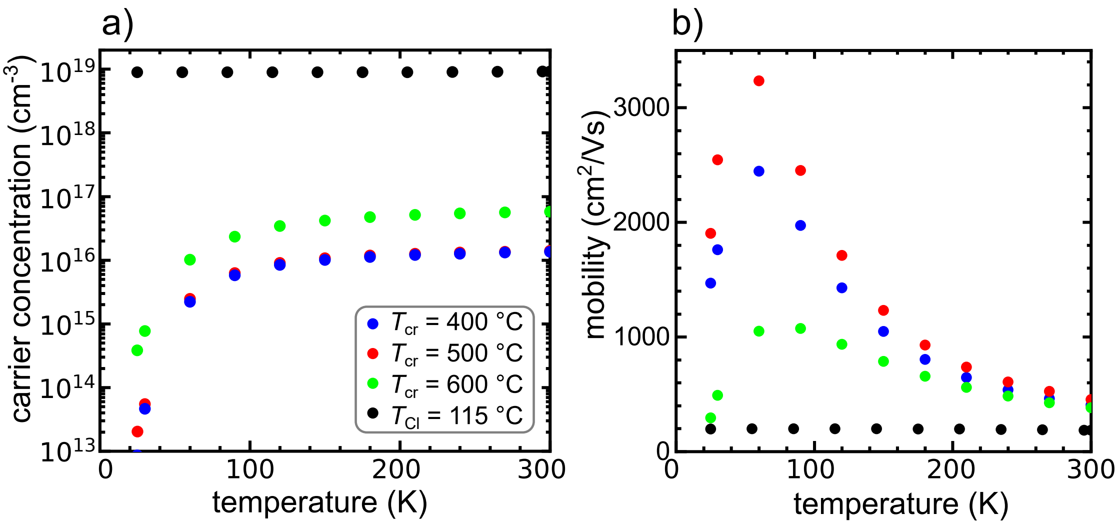

Figure 4.8: Temperature dependent transport in ZnSe:Cl for different doping concentration. Free carrier concentration versus temperature for ZnSe obtained from van der Pauw Hall measurements for four different thin films. The doped (undoped) thin films have a thickness of ~0.5 µm (2 µm) and are partly relaxed. The temperature of the $ZnCl_2$ cell (T_{Cl}) or of the valve cracker module (T_{cr}) is specified. b) Electron mobility versus temperature with the same colour coding as in a). Hall measurement by and figure adopted from Nils von den Driesch.

observed reduction of the mobility is expected for a higher concentration of donors acting as scattering centers and is in first approximation independent on the donor type [5, 144].

The temperature dependence of electron transport in ZnSe is shown for ZnSe with varying doping concentration in Fig. 4.8. At RT, electron density is $\sim 1\times10^{16}\,\mathrm{cm}^{-3}$ for nominally undoped samples, and $\sim 1\times10^{19}\,\mathrm{cm}^{-3}$ for highly doped samples, see Fig. 4.8 a). The carrier concentration is found to be stable for the sample with high n, since it is beyond the critical density of the MIT, and drops to zero for $T \rightarrow 0\,\mathrm{K}$ for the nominally undoped samples. Fig. 4.8 b) shows the temperature dependence of the electron mobility. For the highly doped sample mobility is temperature stable, representing metallic behaviour, with the dominant scattering mechanism being impurity scattering, as discussed above. For the nominally undoped samples, the mobility increases to a maximum between 60 K and 90 K, in agreement with the theory for longitudinal optical phonon scattering (Sect. 4.1.1). As the temperature is further reduced ($T \rightarrow 0\,\mathrm{K}$), impurity scattering becomes the dominant scattering mechanism. This effectively leads to a relative mobility reduction, with simultaneous freeze out of the carrier concentration for $T \rightarrow 0\,\mathrm{K}$, found by comparison with the theory (Sect. 4.1.1). It is not possible to fit the temperature dependent mobility data (Fig. 4.8 b) to the theory by means of N_I (K). Fixing T to 77 K or RT, the degree of compensation deduced from the theory for the nominally undoped samples is $K = 0.8-0.9$. This value is unreasonably high, since no compensation was observed in PL measurements (c.f. Fig. 5.6). I conclude the theory overestimates the degree of compensation and must be improved for future investigations. From the maximal mobility of the bulk ZnSe sample with low electron density, we estimate the electron mean free path to be 30 nm, which corresponds to the spacing of charged and neutral impurities [145].

4.2.2. ELECTRICAL TRANSPORT OF BULK ZNMGSE

In this section, we electrically characterise MBE grown bulk ZnMgSe dependent on the temperature. Using MBE, $Zn_{1-x}Mg_xSe$ can be grown with high control in a well controlled way for x_{Mg} up to 80 % where the crystal structure changes [131, 146]. In the literature, the discussion of electrical transport in the ternary system ZnMgSe is mostly restricted to assessment of n at RT, disregarding electron transport [92, 147]. Electron transport has only been discussed for ZnMgSe unintentionally doped crystals grown by the Bridgeman method, providing only limited understanding of scattering mechanisms [127, 140].

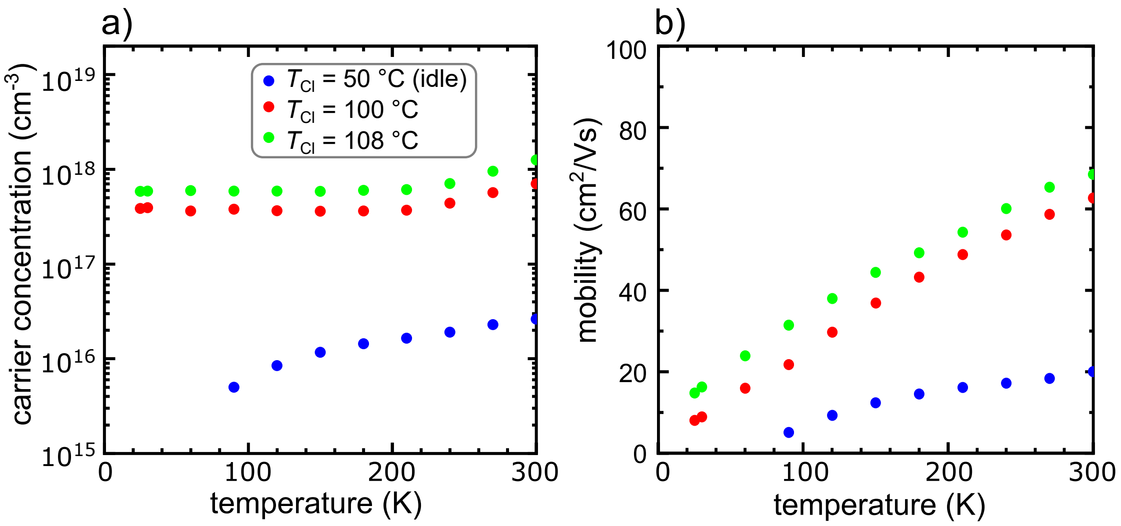

Figure 4.9: Temperature dependent transport in ZnMgSe:Cl for different doping concentrations. a) Free carrier concentration versus temperature for ZnMgSe obtained from van der Pauw Hall measurements. The doped (undoped) thin films have a thickness of ~250 nm (1500 nm) with a composition $x_{\mathrm{Mg}} = 17 \pm 2\,\%$ and are partly relaxed. The temperature of the $\mathrm{ZnCl_2}$ cell is specified (T_{Cl}). b) Electron mobility versus temperature. Hall measurement by and figure adopted from Nils von den Driesch.

In contrast, this work does provides a study of electron transport in $\mathrm{Zn_{1-x}Mg_xSe}$ (x_{Mg} =15–20 %) covering T =25–300 K, motivated by exploration of the electronic properties of the materials in the HS on which the target EDQD device is based.

Most ZnMgSe bulk crystals reported in the literature are found to be of inferior quality, and for some the origin of the donors is unknown [92, 140]. The following section thus provides a much clearer insight to the electrical properties of $\mathrm{Zn_{1-x}Mg_xSe}$ for x_{Mg} =0–20 % and identifies both the donor type as well as the position of the MIT. If not otherwise stated, ZnMgSe means $\mathrm{Zn_{1-x}Mg_xSe}$ with x_{Mg} =15–20 %.

Subject to our study are bulk ZnMgSe crystals epitaxially grown on GaAs, following the routines described in Sect. 5.2. Thickness of the substrates ranges from 200–500 nm, where internal strain is largely compensated by relaxation. Based on Vegard's law (Eq. 4.14), the estimated critical thickness for ZnMgSe (x_{Mg}=20 %) is about 60 nm. Based on the same arguments that apply for ZnSe (Sect. 3.4), we use Cl as dopant, since we consider Cl to be the donor of choice for ZnMgSe to be introduced *in-situ* by epitaxial doping.

For ZnMgSe:Cl grown in this study, not all incorporated Cl atoms could be activated resulting in partial compensation. Theory describes this effect by a compensation level 120 meV above the conduction band edge of ZnSe, which determines the maximum free carrier concentration in ZnMgSe [92]. Using SIMS characterization of our samples we verify, Cl incorporation is independent on the Mg concentration (c.f.

Fig A.13), contrary to observation of an order of magnitude effect reported in the literature [147]. In comparison, our experiments were conducted at a 20 °C lower substrate temperature and avoid growth conditions close to a Cl related growth rate reduction, which presumably leads to a higher compensation ratio [147].

Fig. 4.9 displays temperature dependent carrier concentration and mobility for a typical set of doped or undoped ZnMgSe samples. For $n \geq 7 \times 10^{17}\,\mathrm{cm}^{-3}$ at RT, we observe only a slight decrease of n as T approaches 0 K (Fig. 4.9 a), indicating n is at the metallic side of the MIT. However, the continuous reduction of mobility in these samples towards low temperature (Fig. 4.9 b) indicates localisation of electrons, following the interpretation of a lift of the mobility edge in the Anderson picture (Sect. 4.1.2).

At RT, electron mobility exhibits a trend to higher electron mobility for higher doping concentrations in our samples (Fig. 4.9 b), presumably resulting from efficient screening of N_I for high n. This trend indicates presence of strong disorder in the system, where an increase of the Fermi level induced by doping simultaneously increases screening, lowering the mobility edge and turning localised states into extended ones (Fig.4.4). Reduced efficiency of the donor activation reported in the literature is in agreement with our observation [147].

We note, scattering at charged impurities is not the dominant scattering mechanism at RT, while it is dominant in absence of Mg (Fig. 4.1 a). Mg introduces disorder (alloy disorder), as Mg represents neutral impurities leading to potential fluctuations on atomic scale. We conclude that most probably polar optical phonon scattering is dominant (Fig. 4.1 a), since this mechanism is more efficient than scattering at piezoelectric phonons (Fig. 4.1 a). At lower temperature, phonons freeze out, but this is compensated by simultaneous lowering of defect screening with freeze out of carriers accompanied by a reduction of thermal excitation of electrons, which contributes to localisation.

EXPERIMENTAL DETERMINATION OF THE MIT

Whether a semiconductor is metallic or isolating, can be easily deduced from it's transport characteristics for $T \to 0\,\mathrm{K}$. Recalling the models for the Mott-Anderson or Mott-Hubbard transition introduced above, the Mott criterion (Eq.4.13) predicts metallic or insulating transport characteristics for electron transport at zero temperature (Sect. 4.1.2). The donor activation energy is included in our discussion.

To study the MIT by verifying validity of the hydrogen model for our samples, we calculate the activation energy of shallow donors in ZnSe and obtain 27 meV (Eq. 4.10). With increasing strength of electron interactions for higher n, the assumptions of the hydrogen model with electrons tightly bound only to one donor atom break down, as states become more extended. In experiments, the lowering of activation energy induced by doping can be verified [138]. Fig. 4.10 displays the activation energy of donors in ZnSe versus the carrier concentration [138]. The underlying phenomenological expression [138]

$$E_\mathrm{d} = E_0 - \alpha \left(N_{\mathrm{d}^+}\right)^{\frac{1}{3}} \tag{4.19}$$

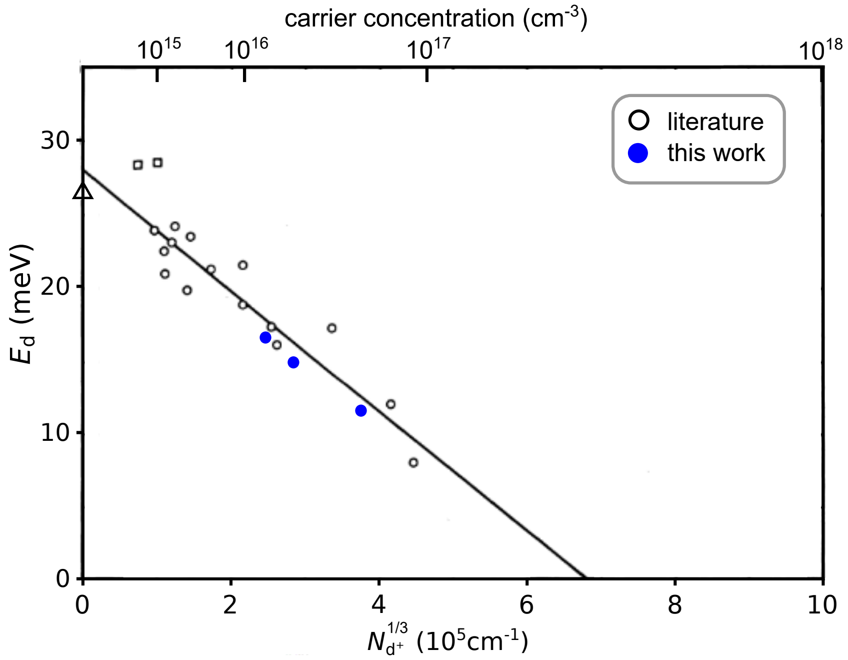

Figure 4.10: Activation energy of donors in ZnSe. The activation energy derived from $n(T)$ (Eq. 4.18) for shallow donors in ZnSe is depicted versus donor concentration N_{d^+}. Literature values for N_{d^+} (Al and halogen donors) and values of this work (Cl) are shown in black and blue, respectively. Most of the the referenced samples are nominally undoped grown from the melt [138]. Samples from this work are grown by MBE and are nominally undoped. The black line corresponds to a linear fit (Eq. 4.19) excluding the two data points marked by squares (experimental uncertainties) and the triangle (optical data). Figure adopted from Ref. [138].

covers the electronic correlations such as electron-electron repulsion, screening, polarization and charged defects as the doping concentration increases. Here, E_0 and α denote the activation energy in the limit of zero defects and a proportionality constant, respectively.
For $n = 1 \times 10^{15}\,\text{cm}^{-3}$ the activation energy is in agreement with the hydrogen model. However, as the electronic correlations increase with higher doping, the activation energy gradually reduces. For one of our purest crystals with a background doping concentration of $\sim 1 \times 10^{16}\,\text{cm}^{-3}$, we find $E_d = 15\,\text{meV}$.
Extrapolated to zero activation energy, which can serve as alternative description of the MIT, one expects full ionization of all donors at $3 \times 10^{17}\,\text{cm}^{-3}$. This value obtained from experimental work is quite close to the prediction from the Mott-criterion ($4 \times 10^{17}\,\text{cm}^{-3}$), see Sect. 4.1.2. Thus the experimental findings (Fig. 4.10) are in agreement with the formation of an impurity band that is lifted in energy to the conduction band with increasing impurity (doping) concentration.

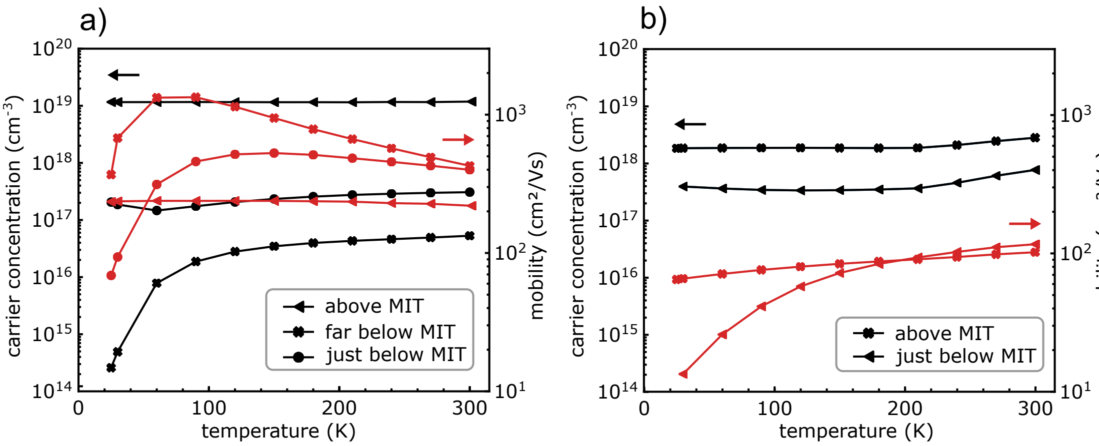

Figure 4.11: Electrical verification of the MIT in ZnSe and ZnMgSe. Carrier concentration and mobility versus temperature for a) bulk ZnSe and b) bulk ZnMgSe ($x_{\mathrm{Mg}} = 17 \pm 2\,\%$) obtained by van der Pauw Hall mobility measurements. The arrows denote the corresponding axis, the carrier concentration to the left (black) and the mobility to the right (red). The thickness of the partly relaxed thin films is 0.5 µm and 1 µm for ZnSe and ZnMgSe, respectively. Data providing more statistics for the evaluation of the MIT is provided in Apx. A.12. Hall measurement by Johanna Janßen and Nils von den Driesch. Figure adopted from Ref. [148].

The data for E_{d} shown in Fig. 4.10 is obtained from the temperature dependence of n following Eq. 4.18. Similar results for E_{d} and related record mobilities, were reported for ZnSe crystals purified by annealing in liquid Zn [112].

Our second approach to determine the MIT in ZnSe and ZnMgSe is assignment of electron transport characteristics to be either metallic or insulating for $T \rightarrow 0\,\mathrm{K}$ [148]. For van der Pauw Hall measurements for ZnSe and ZnMgSe, as discussed above (Fig. 4.8 and Fig. 4.9) we conduct the following analysis: A sample is assigned as metallic, if both n and μ are independent on temperature and remain finite for $T \rightarrow 0\,\mathrm{K}$, the indication for degenerate electron densities expected for $n > n_{\mathrm{MIT}}$. However, if n and μ approach 0 for $T \rightarrow 0\,\mathrm{K}$, the sample is assigned as insulating.

To illustrate our approach with exemplary data for ZnSe (ZnMgSe) bulk, please see Fig. 4.11 a(b)). The uppermost data curves correspond to samples with $n > n_{\mathrm{MIT}}$, since n and μ are independent on the temperature, and thus these samples are assigned as metallic. The other data sets represent vanishing electron transport in the limit of $T \rightarrow 0\,\mathrm{K}$, and are thus assigned as insulating. Following this analysis approach, on a larger data set (Fig. A.12), we obtain an experimental measure of n_{MIT}, corresponding to the boundary at which metallic or insulating characteristics is observed [148].

Our result for the MIT in ZnSe is in agreement with $n_{\mathrm{MIT}} = 1.3 \times 10^{17}$–$6 \times 10^{17}\,\mathrm{cm}^{-3}$ reported in the literature, induced either by doping or compensation [122]. For ZnMgSe ($x_{\mathrm{Mg}} = 17 \pm 2\,\%$) we find $n_{\mathrm{MIT}} = 4.5 \times 10^{17}$–$7 \times 10^{17}\,\mathrm{cm}^{-3}$. Comparable experimental work is not available in the literature, but our data agrees with our prediction based on Vegard's law (Eq. 4.14, for details see Fig. A.11). An overview of our results for ZnSe and ZnMgSe and those in the literature is shown in Fig. 4.12 and listed in Tab. 4.1.

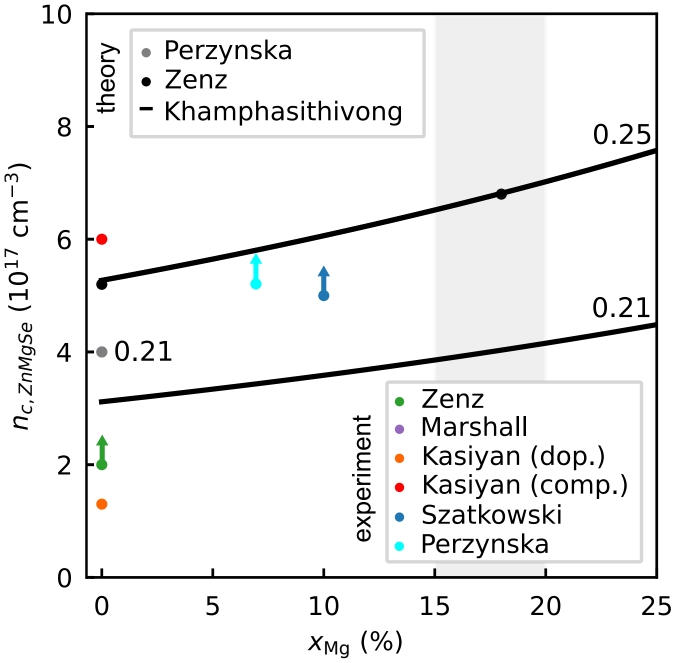

Figure 4.12: Overview on the critical density for different x_{Mg}. Shown are experimental results and theoretical predictions (Mott criterion) assuming applicability of Vegard's law for the derivation of the Bohr radius (Fig. A.11). For the solid lines the values 0.21 or 0.25 denote the proportionality constant assumed in (Eq.4.13). The shaded region highlights the composition of $Zn_{1-x}Mg_xSe$ typically used in our experiments ($x_{\mathrm{Mg}} = 17 \pm 2\,\%$). Arrows denote whether experimental data are upper or lower bounds. Different regimes, doping and compensation, are indicated by dop. or comp., respectively. Hall measurement by Johanna Janßen and Nils von den Driesch. The references are the following: Perzynska [116], Zenz [148], Khamphasithivong [this work], Marshall [149], Kasiyan [122], Szatkowski [140]. All data shown corresponds to Tab. 4.1.

Table 4.1: Experimental and theoretical data for the MIT in ZnSe and ZnMgSe.

n_{MIT} (1×10^{17} cm^{-3})	type	prefactor Mott (Eq. 4.13)	material	x_{Mg} (%)	Ref.
4.0(4)	experiment		ZnSe	0	[149]
1.3	experiment		ZnSe	0	[122]
>2	experiment		ZnSe	0	[140]
4	theory	0.21	ZnSe	0	[127]
>5e17	experiment		ZnSe	0	[142]
5.27	theory	0.25	ZnSe	0	this work
>2	experiment		ZnSe	0	[148]
6	experiment		ZnSe	0	[122]
6.7	theory	0.25	ZnSe	0	[118]
~5	experiment		ZnSe	0	[150]
20- 70	experiment		ZnSe	0	[151]
>1	experiment		ZnMgSe	7	[127]
6.8	theory	0.25	ZnMgSe	18	[148]
>4.5	experiment		ZnMgSe	18	this work
6.5	theory Mott	0.25	ZnMgSe	15	this work
7	theory Mott	0.25	ZnMgSe	20	this work
>5	experiment		ZnMgSe	10, 20	[140]
4.5	theory	0.21	ZnMgSe	20	[127]
16	theory	0.21	MgSe	100	[127]

4.3. ELECTRICAL TRANSPORT IN A ZNSE QW

In the last section of this Chapter, we transition from discussing electron transport no longer for the bulk, but for localised systems. In particular, we want to investigate electron transport in a 2DEG confined to a ZnSe QW in a ZnSe/ZnMgSe HS, similar to HS the target EDQD device is built on. We desire a first understanding of limiting factors for the electron mean free path. Our expectation is an increase of the electron mean free path as consequence in the more localised system (QW), compared to the bulk [80].

For an undoped QWs in a ZnSe/ZnMgSe HS, the transport characteristic in darkness is shown in Fig. 4.13 a) as a function of temperature. For technical reasons, no gate voltage can be applied and thus the charge carrier concentration in the QW can not be controlled directly. As a reminder, by van der Pauw Hall measurements we probe the electrical properties of a thin film, in our case two channels connected in parallel, the upper ZnMgSe barrier and the ZnSe QW. In darkness, the electrical properties of the system become fully insulating with decreasing temperature, as the mobility drops to zero (Fig. 4.13 a). The insulating behaviour of the sample is also reflected by missing data points for $T < 90\,\mathrm{K}$, as the resistivity limit of the measurement setup is exceeded. In contrast, the carrier concentration of about 1×10^{18} cm^{-3}

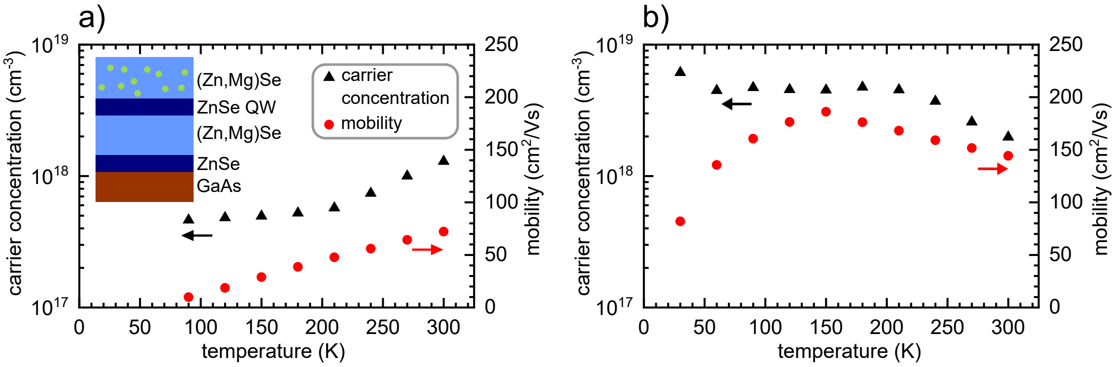

Figure 4.13: Temperature dependent transport properties of undoped ZnSe QWs. Electron mobility as a function of electron concentration and temperatures measured by Hall effect in a) darkness and b) under LED excitation at 365 nm. The device resistance is 21 MΩ (27 kΩ) for the measurement at 30 K without (with) LED illumination, deduced from linear IV characteristics (data not shown). Figure by Johanna Janßen [105].

is only slightly reduced for lower temperatures and saturates at a non-zero level in the range of the critical density of ZnSe/ZnMgSe (Sect. 4.2.2). We attribute the finite carrier concentration and a vanishing electron mobility for $T \rightarrow 0$ K to a localisation of electrons in the Anderson picture (Sect. 4.1.2). Since the ZnMgSe is highly doped and hence presumably disordered (Fig. A.13), the mobility edge drops with reduction of energy (T). The 2D electron density measured is $1.5 \times 10^{12}\,\mathrm{cm}^{-2}$ at RT and approaches $4 \times 10^{11}\,\mathrm{cm}^{-2}$ for $T \rightarrow 0$. We conclude that the main conducting channel to be ZnMgSe:Cl in the upper barrier, since $n(T)$ and $\mu(T)$ correspond to the characteristic observed for bulk ZnMgSe (Sect. 4.2), and states in the upper barrier are lower in energy compared to the lower barrier (Fig. A.1). This finding is underlined by observation of the same effect in about ten similar ZnSe/ZnMgSe HS with varying doping concentration in the ZnSe QW (Tab. A.5).

As alternative to gate control utilizing the field effect for manipulation of n, we use above bandgap excitation (365 nm) with an UV LED to create a non-ground-state equilibrium of the system. Hereby, the electron density of the system increases and the averaged mobility multiplies, which points at population of the ZnSe QW which exhibits less scattering centers than present in the upper ZnMgSe barrier (Fig. 4.13 b)). The 2D electron density measured is in the range of 2.5×10^{12}–$6 \times 10^{12}\,\mathrm{cm}^{-2}$, and the mobility vanishes for $T \rightarrow 0$ K.

These finding add to the model of parallel conduction in the upper barrier and the QW observed for doped ZnSe QWs (Sect. 3.5). Since the parasitic conduction in the upper ZnMgSe barrier dominates the conductivity of the system, no quantitative results on the mean free path of the ZnSe QW can be determined. We recall that the adjustment of the CB edge in the upper barrier versus the ZnSe QW, here limited by the requirement of planar doping for ohmic contacts, will be enabled by electrical control in a more advanced device, like a gated Hall-Bar or the target EDQD device implemented on an undoped ZnSe/ZnMgSe HS.

4.4. CONCLUSION AND DISCUSSION

Closing remarks, we analysed electrical transport of MBE grown ZnSe and ZnMgSe materials. By studying electron transport at low temperatures, interpreted by percolation theory, the electron density of the MIT (n_c) is determined. We allocate n_c for bulk ZnSe and bulk ZnMgSe ($x_{Mg} = 17 \pm 2\,\%$) to be in the ranges 1.3×10^{17}–$6 \times 10^{17}\,\mathrm{cm}^{-3}$ and 4.5×10^{17}–$6 \times 10^{17}\,\mathrm{cm}^{-3}$, respectively. It is to be noted, that compensation, which is assumed to be zero in this evaluation, strongly affects the position of the MIT, as well as experimental methods, when approaching the MIT from the dielectric or metallic side [122]. Our assumption is valid for ZnSe as compensation was only observed for highly Cl-doped or heavily processed samples, and not in typical ZnSe crystals. However, our assumption of no compensation for ZnMgSe is weak, as independent PL measurements have revealed compensation related to Cl donors. Further investigation of the effect of compensation on transport in ZnMgSe is beyond the scope of this work.

Analysis of transport properties of undoped ZnSe/ZnMgSe HS was not possible as technical limitations in local doping preventing contact formation for such structures were faced. Instead, results on remotely doped devices yield insight into the mean free path in the QW. The investigation of such heterostructures is continued employing gate control, see Chap. 6.

Results of this study on mean free path and mobility of electrons are derived from temperature dependent van der Pauw Hall measurements for T in the range of 30–300 K. Although the main focus is on the electron mean free path in ZnSe QW structures, valuable insights to material quality can be deduced from evaluation of bulk ZnSe and ZnMgSe epilayers. Most importantly, we find a maximal mobility of ($3 \times 10^3\,\mathrm{cm}^2/\mathrm{Vs}$) for bulk ZnSe in the LT regime (T ~60–90 K) limited by electron scattering with (neutral) impurities.

However, for ZnMgSe the electron mean free path is significantly reduced (about 3 orders of magnitude at 30 K) as a consequence of disorder in the system leading to an Anderson like localisation and related a drop of electron mobility. We conclude, although solubility of Cl in ZnMgSe is high, donor activation is less efficient than in ZnSe, as Cl is not only incorporated at the anion sites, which leads to disorder and compensation [147]. Furthermore, it is important to consider the relevance of alloy disorder, which can cause fluctuations in the conduction band energy that cannot be overcome at zero temperature. Similar observations have also been made in ZnCdSe [127].

In summary, by van der Pauw Hall mobility measurements we characterise electron transport in ZnSe bulk and 2DEGs in dependence of the temperature. Our experimental work is in agreement with other experimental work and theory for bulk ZnSe and provide new insights to electron transport at $T \leq 25\,\mathrm{K}$ and in localised systems (2DEG) [122, 140, 147]. We identify impurity scattering as limiting transport mechanism for bulk ZnSe and provide an estimate of 30 nm for the electron mean free path in our best crystal. An improvement of the electron mean free path in 2DEGs could not be demonstrated, originating from technical limitations in contacting an undoped ZnSe QW.

We have investigated the MIT for the materials the target device is composed of, ZnSe and ZnMgSe with $x_{\mathrm{Mg}} = 17 \pm 2\,\%$, since of relevance for fabrication of Ohmic contacts. In summary, our experimental result for ZnSe ($n_{\mathrm{c}} = 5 \times 10^{17}\,\mathrm{cm}^{-3}$) is in agreement with the literature and comparable to that for ZnMgSe ($n_{\mathrm{c}} = 7 \times 10^{17}\,\mathrm{cm}^{-3}$), see Fig. 4.12 and Tab. 4.1. By epitaxial doping during MBE growth, we can control metallic or insulating behaviour of bulk ZnSe (ZnMgSe), essential for fabricating Ohmic contacts to ZnSe based devices. For localised systems, in particular 10 nm thick ZnSe QW and a parallel triangular QW close to the surface of the device, we have found n of the MIT in the range 1×10^{11}–$1 \times 10^{12}\,\mathrm{cm}^{-2}$ for such 2DEG systems (c.f. Sect. 4.3). Closing remarks, improvements of the measurement precision is expected when n can be electrically controlled, in contrast to choice of the doping profile. As a reminder, such experiments require gated devices featuring local Ohmic contacts, the latter being one of the main objectives of this work.

CONTRIBUTIONS

Johanna Janßen, Benjamin Zenz contributed to measurement analysis. Evaluation of compensation following Ref. [118] was done by Benjamin Zenz. Benjamin Benemann, Nils von den Driesch and Johanna Janßen conducted van der Pauw Hall measurements.

5

FABRICATION OF II-VI HETEROSTRUCTURES AND ELECTRICAL DEVICES

The technology chosen in this project as qubit architecture is Electrically Defined Quantum Dots (EDQD) in ZnSe/ZnMgSe using the spin state of the electron. The field of EDQD spin qubits hardware is at the level of multi qubit devices with up to six coupled qubits in Silicon [152]. The qubit count of coupled qubits is still limited since long range coupling still poses a challenge [153]. High fidelity operation of single qubits is very well established and has also been demonstrated in heterostructures with isotopically purified Silicon for two qubit gates with fidelities above threshold for quantum error correction by surface code [1, 2]. Lacking low resistivity Ohmic contacts at low temperature ($T \leq 4\,\mathrm{K}$), the ZnSe platform has not reached the qubit level in electrically controlled devices, but this work outlines how first devices with such architecture could be fabricated. One requirement for high qubit quality is reliable and reproducible fabrication. The most important aspects for reproducible high quality heterostructure growth, formation of local Ohmic contacts and definition of isolated gates at the nanoscale, are all addressed in this chapter. We continuously monitor fabrication employing structural analysis based on X-rays, optical and electrical methods. Verification of individual process steps is provided using a set of imaging techniques, such as optical or scanning electron microscopy, or atomic force microscopy.

The chapter is structured as follows: An overview on world-wide state of the art fabrication techniques used for II-VI platform is given. In comparison, a process overview for gated Hall-bars and devices with qubit architecture on II-VI substrates as used in this work is given, followed by a detailed discussion of the processes involved: Structured in the order of device fabrication heterostructure growth (Sect. 5.2), contacting (Sect. 5.3), mesa etching (Sect. 5.4), thermal budget (Sect. 5.5) and deposition of gates and dielectric (Sect. 5.6) are covered.

This toolbox, capable of bandgap engineering and device fabrication in the ZnSe/ZnMgSe material system was developed within the Jülich-Aachen Research Alliance

(JARA) collaboration.[1] Electrical analysis of the devices is described in Chap. 3, 4 and 6 for the aspects Ohmic contact, transport and electrical control, respectively. This chapter concludes with a discussion of key parameters and processes required for high quality device fabrication in II-VI considering the criteria defined in Sect. 2.2.

STATE OF THE ART

Aware of the electro-optical capabilities of ZnSe with applications like photo detectors and sources operating in the blue spectrum, ZnSe has been grown and studied for multiple decades. Here, I give a non exclusive overview to sketch the different fabrication techniques used for the growth and structuring of ZnSe.

The material can be grown in high quality either from the melt or vapor using a variety of techniques. These range from liquid or vapor phase epitaxy over MOCVD to MBE [112, 142, 144, 154, 155]. An alternative approach, hot wall epitaxy, is more simple in comparison but compromises material quality [48, 156, 157]. Generally, for heteroepitaxially grown layers, material quality is strongly dependent on the thermoelastic strain, which favors a low substrate temperature and usage of GaAs substrates with low lattice mismatch to ZnSe. Both aspects can be addressed by MBE, offering a high degree of control, which is exploited i.e. for nanowire growth com-

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[1] The fabrication process for gated hallbar devices (presented in Chap 5.1) was coherently developed by Johanna Janßen and me, including design of processes and device layouts. I conducted device fabrication on HS grown by PGI 9 (see Sect. 5.2) and a majority of characterization in the cleanroom. Johanna Janßen supported fabrication by RIE etching and coordinated deposition of gate oxide, in most cases conducted by Benjamin Bennemann. Based on this process I developed a process for fabrication of EDQD devices and conducted the fabrication (Sect. 5.7).

The results on HS growth discussed in Chap 5.2. were generated by PGI 9 partners. Structural analysis was conducted by Alexander Pawlis, Nils von den Driesch and Alexander Shkurmanov. Optical analysis was conducted by Alexander Pawlis, Nils von den Driesch and Johanna Janßen and TEM by Bae Jinhee.

Fabrication of Ohmic contacts described in Sect. 5.3 was jointly developed with Johanna Janßen. Johanna Janßen started the project by investigation of the implantation approach. Johanna Janßen also discovered wet etching as suitable approach for structuring of contacts, which I used for device fabrication since then. Johanna Janßen and I contributed to establishment of the regrowth contact. Main contributions were process design (Johanna Janßen, Alexander Pawlis, Benjamin Bennemann), device fabrication (Johanna Janßen, I) and electrical characterization (Till Huckemann, I).

Mesa etching (Sect. 5.4) employed is based on a recipe established by the Pawlis group. I adapted the etch process to be compatible with fabrication of gated hallbars, basically by adding US agitation. Process monitoring was mainly conducted by me, with initial support by Johanna Janßen.

The thermal budget (Sect. 5.5) available for fabrication was deduced from a series of observations. Major contributions were made by Johanna Janßen (annealing/diffusion experiments), Alexander Pawlis/Nils von den Driesch (growth experience) and me (observation of electrical properties).

Isolation properties of devices with metal gates (Sect. 5.6) was experimentally investigated by Johanna Janßen (test structures), Benjamin Zenz and me (gated hallbars, fine gates of EDQD device). The contributions are supplemented at the end of this chapter.

bined with selective area epitaxy [43, 158]. In consequence, MBE is (arguably) the most successful growth technique for high purity ZnSe, typically operating with low substrate temperature in the range of 370–280 °C and even down to 150 °C when employing cracked Se [157]. For both growth schemes, epitaxial growth and growth of phase-pure nanowires, electrons can be confined by bandgap engineering. Generally, annealing after growth can improve crystal quality, but cannot be applied to HS avoiding degradation of the heterointerface [19, 112].

Furthermore, MBE features epitaxial doping with a degree of control, other than doping by diffusion or implantation, as discussed in Sect. 3.3.1 and Sect. 3.3.2, respectively [5, 107, 112]. In n-ZnSe, a maximal doping concentration of $n = 3\times10^{19}\,\mathrm{cm}^{-3}$ has been reported for MOPVE grown ZnSe:I, slightly lower values can be achieved in MBE grown ZnSe:Cl [5, 92, 144]. A record of $n = 3\times10^{20}\,\mathrm{cm}^{-3}$ was achieved in periodically doped ZnSe with a fraction of 1/7, resulting in superior electron mobility (Sect 4.4) compared to uniformly doped layers [151].

Ohmic contacts to p- or n-type ZnSe are typically made on heavily doped ZnSe, contacted by contact metals with appropriate work function or by diffusion of metals into the semiconductor (Ge, In) in an inert atmosphere [50, 77, 151]. However, major challenges are the contact performance at low temperature ($T \leq 4\,\mathrm{K}$), demanding preparation of an oxide-free metal-semiconductor interface, or contacting a QW [5, 78]. Post metal treatments can reduce contact resistivity, but come at the cost of crystal degradation, mediated by the same effect that limits performance of diffusion contacts [49]. It has to be noted, most electrical experiments for II-VI materials conducted at low temperature ($T \leq 10\,\mathrm{K}$) were performed using diffusion contacts, a technique incompatible with the requirements for scalable qubit fabrication, for details see Chap. 3.1.

For structuring of ZnSe, common techniques known from the semiconductor industry (top-down approach) are utilised. Structuring is achieved by employment of soft or hard masks (2D/3D) in combination with (selective) wet or dry etching or selective area growth [43]. Masks are defined using optical or electron beam (e-beam) lithography. Alternatively, selective epitaxial growth employing a shadow mask, is a promising technique allowing for all *in-situ* fabrication of quantum devices, as reported for other material systems [117, 159]. Within this work, we apply this approach to the II-VI system (Chap. 7). Regarding integration of ZnSe semiconductor to optical components, out-coupling of photons can be addressed by realization of micro lenses or photonic crystals. This is an active field of research aimed at development of an optical quantum network, but not part of this work [3, 160].

5.1. PROCESS OVERVIEW OF DEVICE FABRICATION

A set of standard device types is used for electrical characterization. Complexity of device architecture increases with functionality from transmission line method (TLM) structures to gated Hall-bar or qubit devices allowing for more electrical control in transport experiments aiming at single charge control in the quantum well

(QW). All steps required to fabricate these devices are summarised in the following for devices with Hall-bar (Sect. 5.1.1) and qubit architecture (Sect. 5.1.2). Simpler device types such as TLM structures are obtained by following just the first two steps for contact definition. For completeness an overview of all device types to scale is given in Fig. 5.8.

5.1.1. FABRICATION OF A GATED HALL-BAR DEVICE

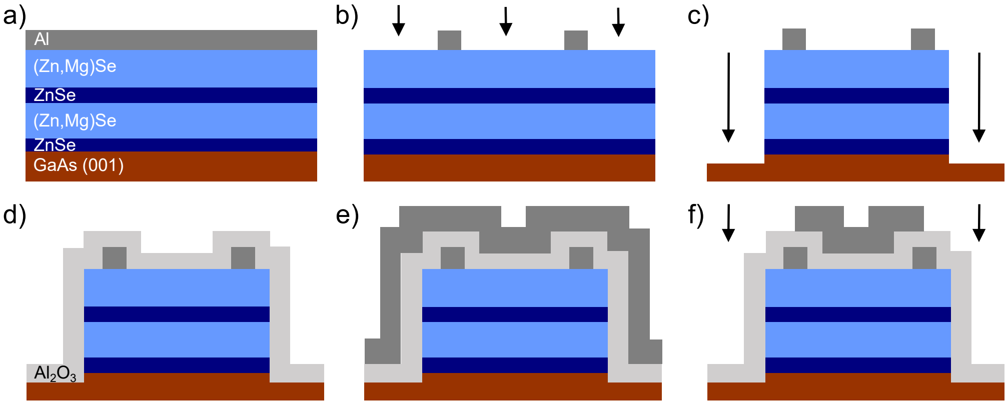

Figure 5.1: Schematic fabrication process for a gated Hall-bar device. a) II-VI HS grown by MBE and metallised *in-situ*. b) Contact definition by wet etch using a resist mask (not shown). c) Mesa etch using resist mask (not shown) and wet etchant based on $K_2Cr_2O_7$. d) Conformal deposition of AlO_x as gate dielectric. e) Al metallization and f) structuring by wet etch. b,c,f) Etched regions not protected by resist mask are indicated by arrows.

Device structuring involves six fabrication steps for gated Hall-bars depicted in Fig. 5.1a)-e): At first the II-VI HS is MBE grown on GaAs substrate and $in-situ$ capped with Aluminum (see Fig. 5.1 a), for details see Sect. 5.2. Second, Al contacts are defined by wet chemical etching using a resist mask (see Fig. 5.1 b), as described in Sect. 5.3. This method is preferred over dry etching for very high etch selectivity avoiding damage to the semiconductor surface. Third, a mesa channel is defined by wet chemical etching employing potassium dichromate as oxidizing agent (see Fig. 5.1 c), as described in Sect. 5.4. This step requires structuring aligned to previously defined contact structures with micrometer precision. Alignment is conducted at a half automated mask aligner or mask less pattern generator. In principle, mesa definition by dry etching is possible i.e. by reactive ion etching (RIE) using CHF_3. One disadvantage of this method is the added challenge of removing the resist mask hardened by the etch. Residuals of optical resist are not acceptable in the entire process line due to their incompatibility with deposition tools of gate dielectric.

Comparing these arguments I choose the wet etching process for high etch selectivity and reproducible resist removal at the cost of uncritical lateral underetching (ca. 1 µm). In a next step, gate dielectric is deposited (Fig. 5.1 d) by atomic layer deposition (ALD) using a plasma process adapted for the low thermal budget available (Sect. 5.5). An isotropic plasma assisted low temperature process was identified to result in conformal deposition of typically 18 nm AlO_x with sufficient isolation properties. The deposition process and oxide characterization are discussed in Sect. 5.6.

Finally, Al is deposited as gate metal (see Fig. 5.1 e) and etched using a resist mask defined by optical lithography (see Fig. 5.1 f). Al is chosen for ease of fabrication since it can be structured similarly to the Al contacts. A gate thickness of typically 100–150 nm is sufficient for Al to climb the mesa with positive flank and electrically connect mesa and non mesa regions. For gate structuring etching is preferred over metal lift-off for preserving the oxide. Developer based wet etching with an etch selectivity of about 10 (Al vs. AlO_x) is used resulting in a nm reduction of AlO_x thickness in uncritical regions outside gate structures. There is slight potential for improved etch homogeneity when going from wet to dry etching since ion damage of inactive oxide regions would be acceptable. Metal lift-off would require optical lithography including development prior to metallization which attacks the oxide in the region of interest. Independent measurements on multiple samples and devices yield an etch rate of 1–2 nm/min for ALD grown AlO_x and degradation of isolation properties.

Following the described steps a)-e) (Fig. 5.1) Hall-bars can be fabricated. The first step (Fig 5.1 a) includes formation of Ohmic contacts by epitaxial doping in the upper ZnMgSe barrier. The entire mask design for $10\times10\,\mathrm{mm}^2$ chips next to a run sheet with step by step instructions for cleanroom processing is attached in the Appendix, see Apx. A.14 and Apx. A.5, respectively.

5.1.2. FABRICATION PROCESS FOR EDQD DEVICES

Fabrication processes for EDQD devices are similar to those used for building Hall-bars but differ in gate definition. Figure 5.2 illustrates all fabrication steps required and is organised in three columns: For each of the six steps device profile (left), design (centered) and an image of a real device (right). The first three processes (Fig. 5.2 a, b, c) for HS growth, contact and mesa definition align with Hall-bar fabrication only differing in design layout (see Figure 5.8). The following nanostructure gate definition requires e-beam lithography, described in Sect. 5.6.3. Essential for good alignment even within a single layer e-beam processes are well defined e-beam markers (Fig. 5.2 d) for automatic detection. Following maker definition and e-beam lithography, Schottky gates without usage of dielectric are defined in a two step process, see Fig 5.2 e, f): In the mesa region nanostructure gates are realised as 5/15 nm thick Ti/Pt gates by e-beam lithography followed by metal deposition and lift-off. A last lithography and metallization step (5/150 nm Ti/Au) provides fan-out for the nanostructure gates as required for bonding.

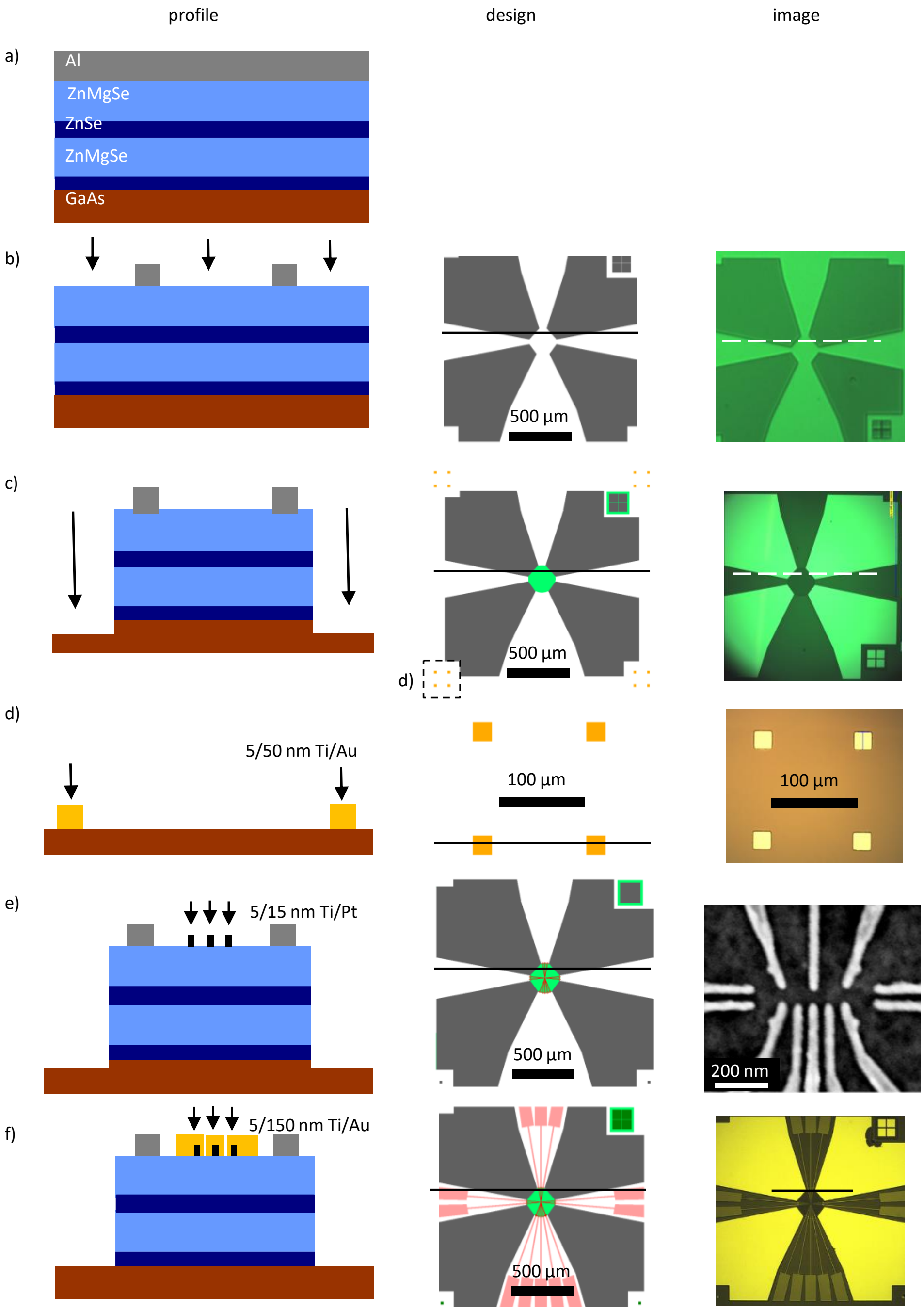

Figure 5.2: Fabrication process for II-VI devices with qubit architecture. Representation of the fabrication process (left), corresponding design (center) and images (right) for all fabrication steps a)-f). Images are obtained from optical microscopy for all panels but panel e) originating from SEM. a) HS growth in MBE is followed by b) contact and c) mesa definition by wet chemical etching (arrows). E-beam lithography requires d) alignment markers for definition of e) nanostructure Schottky gates realised by metal lift-off. f) Bond pads and fan-out lines are fabricated by metal lift-off. The profiles shown correspond to positions marked by black horizontal lines in the design column.

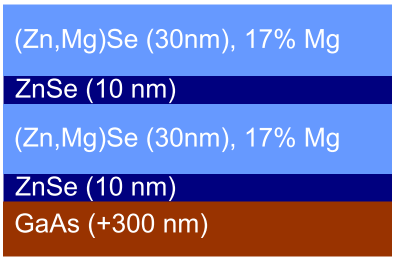

Figure 5.3: Target ZnSe/ZnMgSe heterostructure for MBE growth. Layer sequence for a typical heterostructure with ZnSe QW. The layer thicknesses for the II-VI system are indicated. Prior to II-VI growth, a 300 nm thick GaAs buffer is deposited on undoped GaAs wafers.

5.2. HETEROSTRUCTURE GROWTH BY MOLECULAR BEAM EPITAXY

MBE is used to fabricate high quality thin films as low defect concentrations are prerequisite for spin qubit operations in semiconductor systems. Good understanding and control of crystal growth by MBE allows to engineer the electrical properties of the heterostructures. Most importantly doping concentrations and confinement potential of the HS can be independently controlled by epitaxial doping, quantum well width and (Zn,Mg)Se barrier composition. The target heterostructure as introduced in Chap. 2 is depicted in Fig. 5.3.

MBE growth is realised in the Nanocluster tool within the collaboration with the group lead by A. Pawlis (FZJ/PGI 9). All II-VI thin films relevant for my work were grown by Alexander Pawlis or Nils von den Driesch. UHV conditions allow for growth of planar layers in a clean environment in Frank-van der Merwe mode [161]. An overview of all relevant MBE growth parameters is given in Tab. 5.1. Typically, undoped 2 inch GaAs wafers of thickness 325 ± 25 µm are used. Wafer orientation and growth direction z is (001). Prior to MBE growth, wafers are degassed and thereafter deoxidised by a thermal bake-out or atomic hydrogen treatment. For II-VI (III-V) growth the substrate is heated to substrate temperature[2] of 290 °C (580 °C) and exposed to molecular beams of Zn/Mg and Se (Ga and As). Particles are sourced by temperature controlled effusion cells filled with elemental materials, and leave the cell ideally as small molecules (Se_2/As_4) [157]. The Se, $ZnCl_2$ and As cells are equipped with a cracker module for better control on the size of the molecules. Molecular beams reach the substrate surface and adsorb with a probability expressed by a sticking coefficient. The thin films are grown in As-rich or Zn-rich conditions, where the growth rate is given by the molecular flux of the metal with a sticking coefficient close to one. Adsorbed particles diffuse on the surface and finally localise on correspond-

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[2] assumption: set value of substrate heating stage

ing lattice sites of cations or anions. The temperature dependent diffusion length of the atoms is in the order of few nm at typical substrate temperatures [162].

Table 5.1: Technical details on MBE growth at the Nanocluster tool in the FZJ.

MBE growth	GaAs	ZnSe	ZnMgSe
growth chamber (module)	M2	M12	M12
substrate temperature (°C)	580	290	290
growth orientation	(001)	(001)	(001)
growth rate (µm/h)	0.7	0.18–0.25	0.22–0.3
beam flux ratio (VI:II or V:III)	35-40	3	3.5
buffer thickness (nm)	300	10	10
background doping (cm^{-3})	1×10^{14}	2×10^{15}–3×10^{15}	2×10^{16}

Furthermore, structural defects are avoided by growth of fully strained, relaxation-free heterostructures not exceeding the critical thickness. There is the option to grow isotopically pure ZnSe with nuclear spin free isotopes opening the way to realization of a spin vacuum for spin qubits, as discussed in Chap. 2.1. In this project, we claim growth of heterostructures providing low defect concentrations enabled by the following measures and routines:

During epitaxial GaAs growth, As-rich conditions and the correct growth rates can be ensured using reflection high-energy electron diffraction (RHEED) [85]. After growth, structural analysis is performed using X-ray diffraction (Sect. 5.2). The doping profile can be (destructively) probed by secondary ion mass Spectroscopy (SIMS). Defects can be measured and identified by photoluminescence (PL) with outstanding sensitivity (Sect. 5.2). Related, transport measurements (IV profiling and van der Pauw Hall measurements, both temperature dependent) give access to the mobility and concentration of charge carriers, dependent on defect levels. To some extend, optical or scanning electron microscopy (SEM) can complement the quality assessment. For processing after growth other characterization techniques can help to address surface roughness, local distribution of donor atoms or material composition as well as height profiles, see Chap. 5. Each method can only cover a small fraction of the parameter space but combined monitoring allows to track crystal quality. For this work, most direct process control is provided by RHEED and XRD for structural analysis of surface and epilayers, respectively in combination with IV profiling and van der Pauw Hall measurements for evaluation of transport properties.

A representative growth process claiming high crystal quality is discussed in this paragraph. A typical growth process for a ZnSe/ZnMgSe heterostructure hosting a doped ZnSe QW (Fig. 5.3) is documented in Apx. A.17. For this structure, the doping profile is adjusted to allow for Ohmic contact to a highly doped ZnSe QW. After preconditioning, a 300 nm thick GaAs buffer is grown in module M2 to reduce the impurity concentration. The buffer growth effectively leads to a reduced defect concentration at the top of the buffer layer compared to the bottom, where defect concentration originating from the previously oxidised GaAs surface is largest. With our routine, we achieve impurity concentrations of $n_\mathrm{I} < 1 \times 10^{14}\,\mathrm{cm}^{-3}$ in undoped GaAs.

For II-VI growth, the sample is then brought to module M12 by a transfer system under UHV conditions. Similar to III-V growth, a II-VI buffer consisting of 10 nm ZnSe is grown. Growth rates are controlled by observation of RHEED oscillations. In comparison a smaller buffer thickness for the second buffer is sufficient since the surface of the 300 nm thick GaAs buffer is already free of oxide and impurity diffusion at the heterointerface is suppressed [157]. As a consequence of small lattice mismatch between GaAs and ZnSe, the ZnSe layer is fully compressively strained by 0.27 % at room temperature [163]. Only for thicknesses exceeding the critical thickness of at least 100–150 nm, the ZnSe epilayer begins to relax by formation of misfit dislocations [8, 22, 163, 164]. Accordingly, the degree of relaxation can be deduced in structural analysis from the mismatch of parallel lattice constants for ZnSe and GaAs (Sec. 5.2). Next, a 30 nm thick undoped ZnMgSe buffer layer is grown, followed by a 10 nm thick ZnSe QW doped with Cl supplied by the $ZnCl_2$ cell operated at a temperature of 115 °C. Then, a 30 nm thick upper ZnMgSe barrier is grown, highly Cl doped in the uppermost 20 nm to reduce the contact resistance. Finally, an Ohmic contact to the II-VI HS (see Chap. 3) is formed by Al metallization after UHV transfer to module M4. Smoothest Al surface roughness has been achieved with active substrate cooling. In the following sections, structural analysis of the grown QW heterostructure will be evaluated.

GROWTH ANALYSIS BY XRD

Target structures are desired to be fully strained ZnSe/ZnMgSe heterostructures free of relaxation and related structural defects. Since lattice mismatch for pure MgSe (4 %) is significantly higher compared to ZnSe [165] and the lattice constant linearly scales with x_Mg described by Vegard's law (Eq. 4.14), both x_Mg and total thickness of ZnMgSe barriers predominantly influence the critical thickness of the HS. Relaxation sets in when the total strain in the HS reaches a critical value and gets gradually compensated by formation of misfit dislocations [22]. Similarly, for the ZnSe/ZnMgSe QW system with a layer thicknesses comparable to our target structure, fully strained growth is reported at $x_\mathrm{Mg} = 13\,\%$ [6]. Whether the assumption of relaxation-free growth still holds for a higher Mg content of $x_\mathrm{Mg} \sim 17\,\%$, as required for the target structure, will be addressed in this section.

Non-destructive characterization by structural analysis probes the crystallinity and lattice parameters sensitive to relaxation with high resolution using X-rays from the Cu Kα line (1.5 Å, 8 keV) [166, 167]. Representative structural data is shown in Fig. 5.4 for a typical HS hosting a ZnSe QW. Recording a reciprocal space map (RSM) for the (224) reflex, we determine composition and strain relaxation using a fit model (Fig. 5.4 d). Knowing the degree of relaxation, layer thicknesses and composition are then obtained from a high resolution $\theta - 2\theta$ scan (Fig. 5.4 b). Typical measurement precision for x_Mg by high resolution XRD is less than 1 %, but details of the fitting routine and underlying models are out of scope for this work [168].

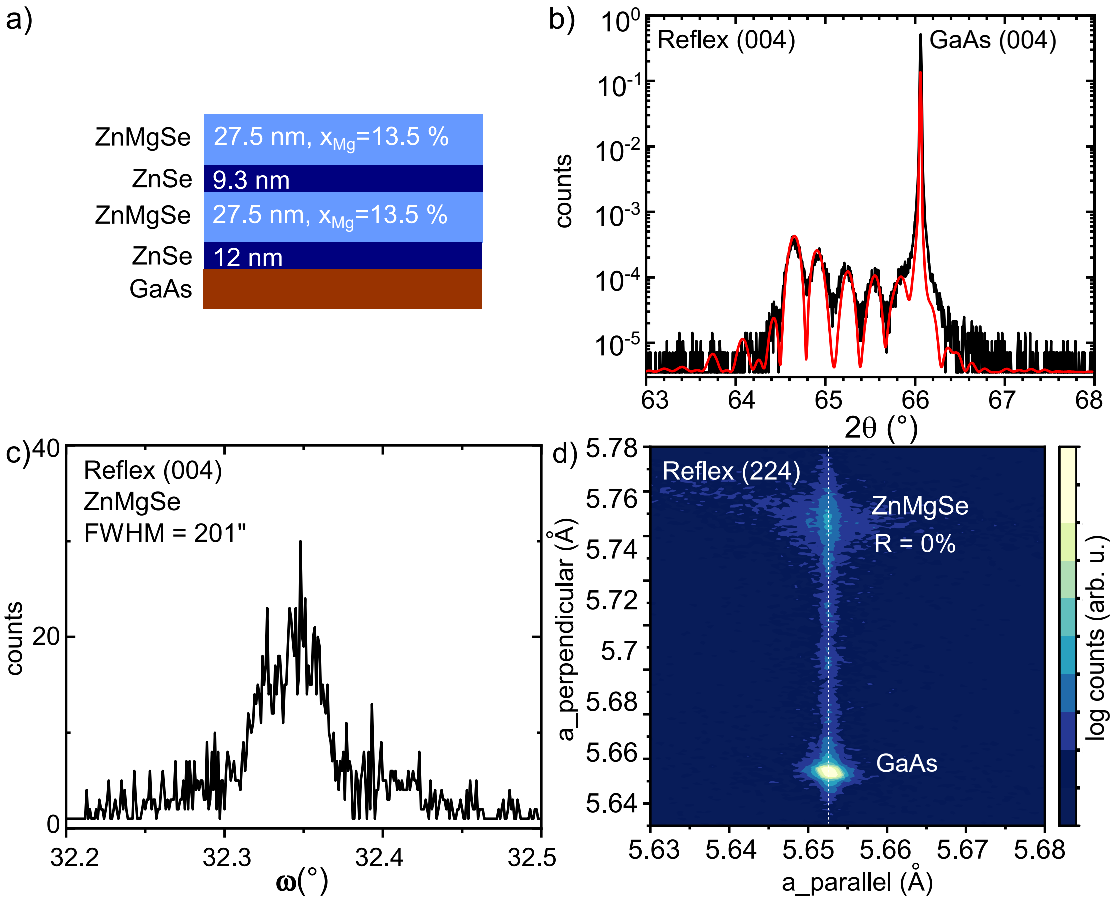

Figure 5.4: Structural analysis of epitaxial II-VI growth by XRD. a) Layer stack of a representative ZnSe/ZnMgSe heterostructure with thickness and composition from analysis results. b) $\theta - 2\theta$ scan data (black) and fit (red) measured at the (004) reflex. c) ω-scan yields a FWHM of 201 arc sec for the (004) reflex of ZnMgSe. d) RSM measured by XRD for the (224) reflex for lattice constants a_{parallel} (in plane) versus $a_{\text{perpendicular}}$ (growth axis). R denotes the degree of relaxation. XRD measurement and analysis by Nils von den Driesch.

Our structural analysis of a typical HS yields a QW thickness of 9.3 nm and 27.5 nm thick barriers with x_{Mg} =13.5 %. The results are close to the target parameters of 10 nm and 30 nm for QW and barrier thickness, respectively. The target barrier composition is x_{Mg} = 17 %, see Fig. 5.3. We note, the absolute deviation in x_{Mg} can be reduced by recalibration and be kept below 1 % in subsequent growth runs.

From a rocking curve measurement (ω-scan), the observed reflection peak width includes information on dislocation density. Peak shape is not part of this discussion. For typical ZnSe/ZnMgSe HS, the FWHM is increased compared to single layers, in this case to 201 arcsec, see the FWHM of the (004) ZnMgSe reflex in Fig 5.4 c), pointing at presence of alloy fluctuations.[3] Lattice parameters can be extracted from a RSM. From scanning the (224) reflexes parallel and perpendicular (along z) lattice constants are obtained as well as x_{Mg}. Indeed this structural analysis verifies relaxation-free growth since a_{parallel} of epilayer and substrate match within the measurement resolution. The lattice constant of ZnSe/ZnMgSe in z is 0.1 Å higher than in lateral direction as a consequence of the larger relaxed/cubic lattice constants. From statistical analysis of more than ten similar thin films an upper bound for x_{Mg} of an relaxation-free heterostructure with the dimensions of the target structure can be determined as 15 ± 2 % (data not shown).

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[3] The detected FWHM might be increased as a consequence of an sacrificial Al capping layer on the HS.

In summary, structural analysis confirms absence of structural defects for the QW structure discussed for the parameter space given above. Our analysis reveals epitaxial boundaries for the target ZnMgSe/ZnSe HS with a maximal valence band offset of 150 ± 20 meV at the ZnSe QW [121].

GROWTH ANALYSIS BY TRANSMISSION ELECTRON MICROSCOPY

In addition to XRD, evidence of relaxation-free growth is also expected to be obtained from transmission electron microscopy (TEM). This method provides the diffraction pattern of high energy electron beams transmitted through a thin lamella. We extract a lamella from a crystal using a focused ion beam (FIB). TEM is capable for probing crystallinity of the probe volume with a lateral resolution down to 1 Å, clearly resolving individual monolayers [169]. Although single atomic defects can not be resolved directly, electron scattering at extended structural defects leads to a change of signal. In combination with other observation methods, we use TEM for microscopic analysis of defects and layers of ZnSe/ZnMgSe HS.

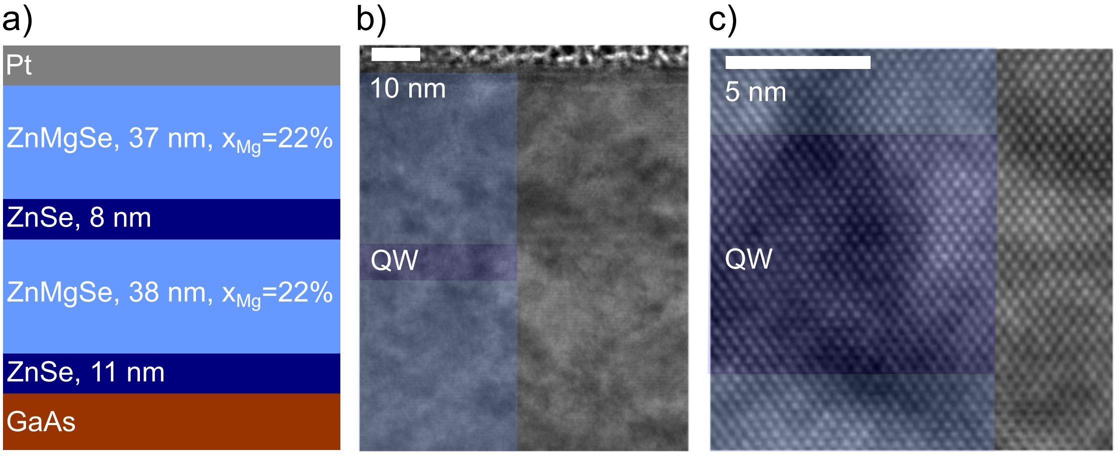

Figure 5.5: TEM of strained II-VI heterostructure with QW. a) Profile of the ZnMgSe/ZnSe HS. Thicknesses from XRD analysis are given, see also Tab. 5.2, HS C). b) (Partially falsecolored) TEM micrograph of ZnMgSe barriers confining a ZnSe QW highlighted in dark blue. c) High resolution TEM micrograph of the QW region. TEM measurement by Jin Hee Bae.

The profile of the HS investigated is shown in Fig. 5.5 a). For technical reasons related to lamella preparation, the HS is capped with a Pt protection layer. An *in-situ* grown Al layer has been removed previously. The TEM micrograph in Fig. 5.5 b) shows the QW region of the heterostructure. As a consequence of coherent growth, the lateral lattice constants almost match at the II-VI/III-V heterointerface (data not shown), in agreement with structural data (not shown). Also at the QW/barrier interface for ZnSe and ZnMgSe the lattice constants match, in consequence no defects are observed at this interface. For better visibility, the position of the QW (barrier) is highlighted in dark (light) blue at positions deduced from independent XRD measurements. Even high resolution TEM can not resolve a contrast at this interface or defects in the QW region scanned, see Fig. 5.5 c). The micrograph is dominated by regularly ordered intensity peaks (white) corresponding to zinc blende unit cells altered by uncorrelated contrast fluctuations, presumably corresponding to spatial variations in lamella thickness. This assumption is in agreement with observations from XRD where onset of relaxation is observed as the parallel lattice constant of 5.663 Å is slightly higher than for the GaAs substrate by about 0.01 Å. XRD yields a degree of strain induced relaxation of 15 %, attributed to high x_{Mg} of 22 % in this HS, beyond the epitaxial boundaries for relaxation-free growth specified in the previous section. Accordingly, misfit dislocations originating from the III-V/II-VI heterointerface have been observed in other scan regions (data not shown). Combining TEM and structural analysis, we can identify this HS as partly relaxed and thereby as exception, still providing high crystal quality as evidenced for the QW region scanned. We note, the majority of QW structures fabricated is relaxation-free found by XRD, but by chance non of such structures was recorded with TEM.

GROWTH ANALYSIS BY PHOTOLUMINESCENCE

Verification of high quality MBE growth is also provided by PL measurements as contactless and non invasive characterization method with high sensitivity to impurities. PL can detect low concentrations of defect levels in semiconductors without the need for structuring devices. When recorded at low temperatures, typically below 10 K, thermal excitation are less important and PL allows to identify and assign discrete peaks of excitonic nature. Moreover, PL is capable of spatially resolving single defects, and time resolved PL can record dynamics, but not of relevance for this work [157].

In this work, PL is used to study the quality of MBE grown II-VI thin films consisting of a single ZnSe layer or a ZnSe/ZnMgSe HS with QW. Here, a typical PL spectrum of an undoped bulk ZnSe layer for above bandgap excitation at 394 nm is shown in Fig. 5.6 a,b). Since the temperature is well below 50 K, the emission peak positions are thermalised [140, 157, 170]. For undoped samples, we observe dominant emission of the free exciton with a binding energy of the free exciton of 18 meV as a line centered at 2.796 eV with a full width at half maximum (FWHM) of 2 meV, in agreement with the literature [157]. The faint peak at 2.785 eV could indicate presence of donor bound excitons [157]. The relative energy shift results from the tensile strain in the ZnSe layer, dependent on the degree of relaxation and the growth temperature [157]. As expected for pure undoped crystals, only faint impurity peaks are identified and there are no donor-acceptor-pair (DAP) transitions present underlining the good control on MBE growth in the Pawlis group.

The PL spectrum of a HS with undoped QW and low Cl concentration in the upper barrier is depicted in Fig. 5.6 c,d). We observe an excitonic emission peak at 2.812 eV with a full width at half maximum (FWHM) of 4 meV, that we assign to free excitons in the ZnSe QW. Compared to the partly relaxed ZnSe bulk sample, the emission is blue shifted in the fully strained ZnSe QW, and in addition due to the confinement energy of the QW. Experimental work and simulation prove this blue shift, that equals 15 meV for our type of heterostructure, in agreement with our simulation (Fig. 2.1) [160]. Another emission peak is observed at 2.817 eV. This emission cannot originate from ZnMgSe, since the band gap energy is significantly higher (~150 meV), and excitons are more likely to recombine in the energetically lower ZnSe QW. Alternatively, we suggest the energy difference of 5 meV to originate from strain induced heavy and light hole splitting, reflected in the exciton emission, as reported in the literature for bulk ZnSe [157, 171].

We focus on the optimization of the MBE growth of doped ZnSe QWs and target at bright exciton emission (free or donor bound) while maintaining a low concentration of deep defects. The investigated HS are specified in Tab. 3.8 and Tab. 5.2 by means of structural composition and doping profiles. PL data for a growth series with varying Cl doping concentrations in the barriers and QW with spectra normalised to the exciton peak in the ZnSe QW is shown in Fig. 5.7 a). In this normalised representation, the PL spectra exhibit a dependence on Cl doping in the upper barrier on the broad deep

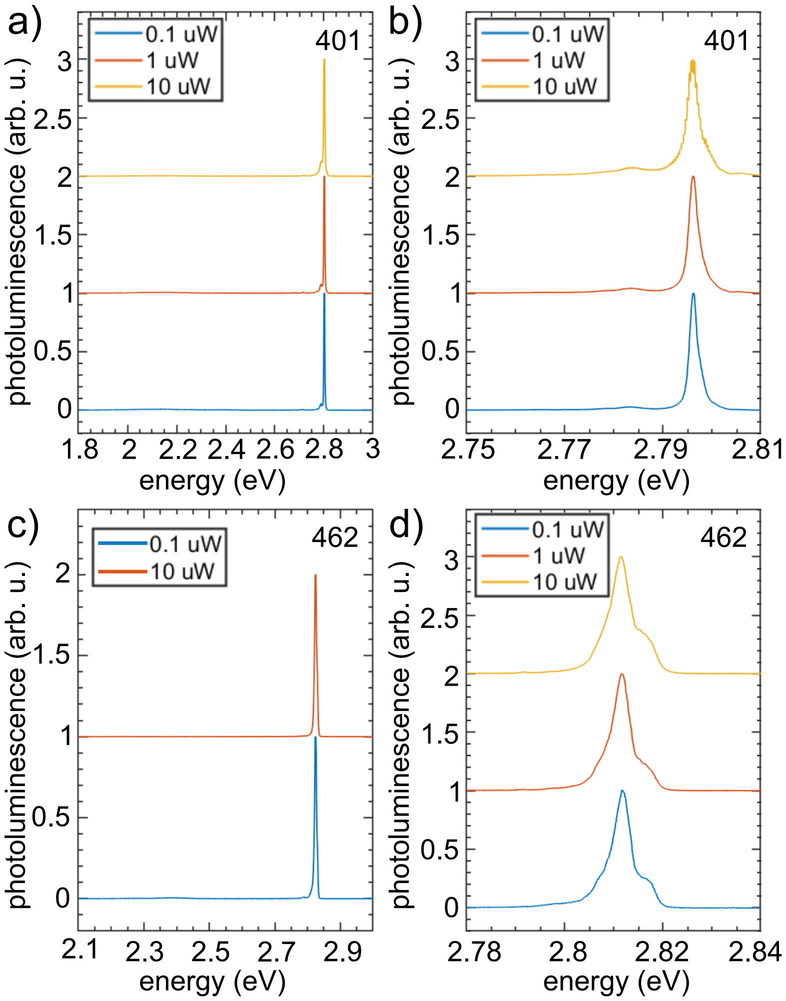

Figure 5.6: PL spectra of bulk ZnSe and ZnSe QW. μ-PL spectra of a) 1.8 µm thick, mostly relaxed and nominally undoped bulk ZnSe layer and b) fully strained, undoped ZnSe QW with low doping concentration in the upper barrier (4×10^{17} cm^{-3}). Above bandgap excitation is applied at 394 nm in pulsed (cw) mode for panels a,b (c,d). The measurement temperature is 10 K. The numbers in the upper right corner of each panel indicate the sample identifier. Figure by Nils von den Driesch.

emission peak at 2.1 ± 0.1 eV, that is artificially enhanced since the main effect is the reduction of the QW emission with doping concentration in the QW. Thus, higher Cl concentrations of up to 1×10^{19} cm^{-3} (quantified by SIMS) lead to a higher intensity of the deep level emission relative to the (donor bound) exciton emission of the QW (peak at 2.8 eV). Similarly also parasitic emission from donor bound excitons in the ZnMgSe barrier (2.8–2.9 eV) increases. This effect has been also discussed in literature: The ratio of the exciton peak to the deep level emission peak in pure ZnMgSe has been found to depend on the doping concentration of Cl forming vacancy-complex

Table 5.2: Description of ZnSe/ZnMgSe HS subject to PL characterization. HS are specified by Cl concentration ($c_{\mathrm{Cl}}^{\mathrm{SIMS}}$), ZnMgSe barrier composition and QW thickness (XRD). Values denoted with ∼ are estimates based on growth conditions. All HS are relaxation-free, except HS C (R=16 %). For HS A-D, $c_{\mathrm{Cl}}^{\mathrm{SIMS}}$ specifies the doping concentration in the upper barrier, the lower barrier is nominally undoped. For electrical specifications of HS A-D see Tab. 3.8.

HS	$c_{\mathrm{Cl}}^{\mathrm{SIMS}}$ (cm^{-3})	$c_{\mathrm{Cl}}^{\mathrm{SIMS}}$ (cm^{-3})	thickness (nm)	thickness (nm)	x_{Mg} (%)
	QW	barrier	QW	barrier	barrier
DD1	$\sim 5 \times 10^{18}$	$\sim 5 \times 10^{18}$	4.6	34	11
DD2	$\sim 5 \times 10^{18}$	$\sim 5 \times 10^{18}$	4.1	30	12
UD	$\sim 5 \times 10^{16}$	$\sim 5 \times 10^{18}$	5.4	33	12
UU1	$\sim 5 \times 10^{16}$	$\sim 5 \times 10^{16}$	4.2	32	12
UU2	$\sim 5 \times 10^{16}$	$\sim 5 \times 10^{16}$	4.7	29	11
D	$\sim 1 \times 10^{19}$	2.5×10^{17}	8.0	30	16.5
A	$\sim 1 \times 10^{19}$	2×10^{18}	∼10	∼30	∼17
B	$\sim 1 \times 10^{19}$	3×10^{18}	9.7	29	17.6
C	$\sim 1 \times 10^{19}$	5×10^{18}	7.5	38	22

centers which can be understood as compensation and gets more important with increasing x_{Mg} and disorder, see Refs. [92, 140] and references therein. From this experiment we identify HS UU1 and UU2 as optimal as they show highest intensity of the free exciton emission with respect to deep level emission, which we attribute to absence of Cl in both the ZnSe QW and the ZnMgSe barriers.

Next, we investigate the optical properties of the HS A-D shown in Fig. 5.7 b), the same as introduced and electrically characterised in Sect. 3.5, see Tab. 3.8. Again, for comparability, the spectra are normalised to the exciton peak in the ZnSe QW. Three prominent effects are identified: First, we observe a quite constant excitonic emission in the same order of magnitude, attributed to similarly high doping concentration in the QW. Second, looking in more detail, the QW emission slightly depends also on the Cl doping concentration in the upper barrier. The relative QW emission is highest for HS D with an undoped upper barrier and about ten fold reduced for the HS with doped upper barrier (HS A, B, C). Third, for the emission of HS with doped QW, the linewidth of about 100 meV is increased compared to the few meV linewidth of the undoped HS, UU1 and UU2 shown in Fig. 5.7 a), and those reported in the literature [140, 172, 173]. For the HS with doped QW, the linewidth is presumably increased as a consequence of compensation (Sect. 4.1.2) in ZnMgSe crystals in agreement with observations of compensated ZnMgSe crystals grown from the liquid [140]. Although grown at lower temperatures, a reason for compensation in our HS could be strong deviations from perfect MBE growth conditions by exceeding the optimal donor concentration.

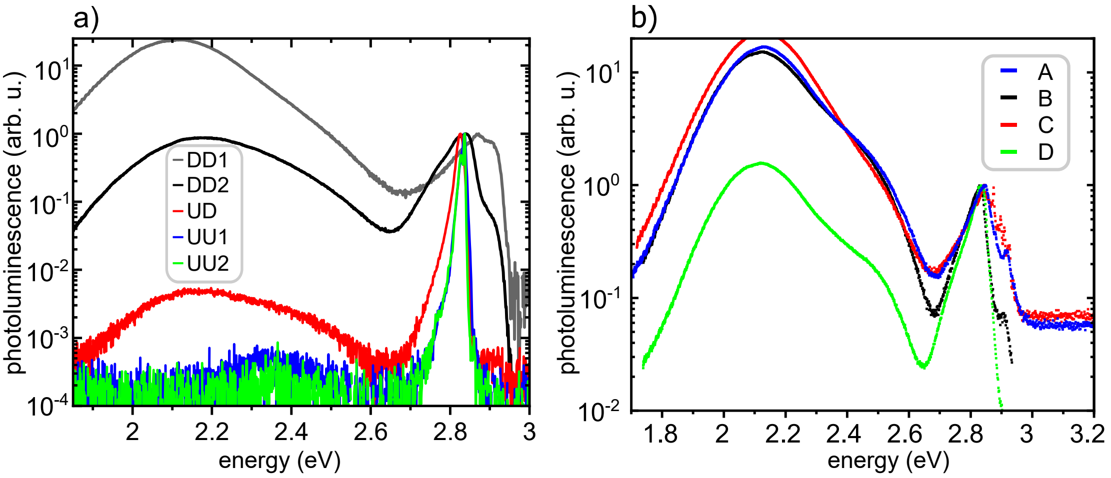

Figure 5.7: PL spectra of different ZnSe/ZnMgSe HS with QW for varying doping profiles. a) PL characterization at 10 K and excitation at 394 nm for doped QW structures. Spectra are normalised to the peak emission intensity of the QW. Concentration of Cl in the QW and upper barrier are in the order of 1×10^{19} cm^{-3} for HS DD1 and DD2. HS UU0 and UU1 are nominally undoped (1×10^{16} cm^{-3}). HS UD has a nominally undoped QW and doped barrier (1×10^{19} cm^{-3}). Nomenclature is chosen such to indicate the presence of doping (doped: D, undoped: U) for the QW and then for the barrier. b) PL spectra for 100 nW of doped ZnSe QWs grown for different doping profiles in the upper ZnMgSe barrier. For HS A-D the Cl concentration in the upper barriers determined by SIMS are listed in Tab. 5.2. Figure (panel a), PL measurement and analysis by Nils von den Driesch.

In summary, from the comparison of multiple ZnSe/ZnMgSe HS with a ZnSe QW we deduce a dependency of the free exciton emission on the Cl doping profile. In undoped HS, such as proposed for the target EDQD device, we can resolve a 5 meV large energy splitting, attributed to a light and heavy hole splitting of the free exciton emission. In intentionally doped HS, subject of electrical characterization of the contact resistance, we find Cl doping in the ZnMgSe barrier is accompanied by a deep level emission that likely originates from Cl incorporation in ZnMgSe not exclusively on group VI lattice sites. As this emission is four orders of magnitude smaller than the free exciton emission in undoped HS, this effect does not play a role for undoped quantum devices. In conclusion, a low background concentration, which we can reduce to a minimum of $n = 2 \pm 1 \times 10^{15}$ cm^{-3} (2×10^{16} cm^{-3}) for ZnSe (ZnMgSe), is essential for a high emission efficiency, associated with high crystal quality.

5.3. OHMIC CONTACTS

Discussion on physics of the Ohmic contact is covered by Chap. 3 also addressing doping of the semiconductor and different contact types. This section provides the technical details required for the fabrication of *ex-situ* contacts and the Al *in-situ* contact, with the latter being identified as low resistivity contact compatible with spin qubit applications (Sect. 2.2.2). Related, the regrowth contact is described as a derivative of the Al *in-situ* contact, which is compatible with local doping.

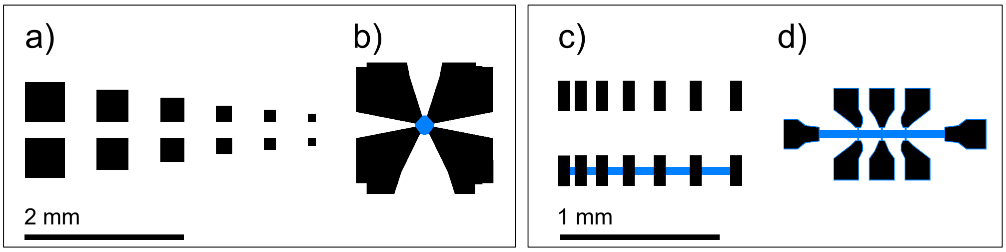

Figure 5.8: Overview of device layouts with different contact designs. Contact design for various devices. Metal contact pads are depicted in black and mesa etched current channels in light blue. a) square structure and a b) qubit device. c) TLM structures without and with mesa and d) Hall-bar device, here for a width of mesa channel of 50 µm. Scalebars differ in size for panels a,b versus c,d. Not shown are van der Pauw Hall structures with four Ohmic contacts (500 µm large) positioned at the corners of the sample.

Typically, for structuring of contacts different device layouts specific to the characterization method were used for each substrate, depicted in Fig. 5.8. TLM and van der Pauw Hall structures are used for basic transport characterization of substrate and contact. For more advanced transport experiments, devices with Hall-bar or qubit device architecture are used. Common for all layouts is large metal pad size compared to transfer length preventing current crowding to limit contact performance (discussed in Chap. 3) [94]. Contact dimensions are in the order of 100 µm, larger than the transfer length (order of 10 µm for doped substrates).

Contacts are fabricated by HS growth, *in-situ* metallization and subsequent metal etch in presence of a resit mask as described in the following two paragraphs:

OPTICAL LITHOGRAPHY

A standard process for optical lithography is used based on the positive process for image reversal resist AZ5214E (microchemicals)[4]. Resist thickness is 1.4 ± 0.1 µm after spin coating at 4000 rpm for 30–45 s and soft bake at 90 °C for 5 min. Samples are cleaned using solvents acetone (ACE) and isopropyl alcohol (IPA) under ultrasonification for 3 min each, dehydrated at 130 °C for 5 min and covered with adhesion

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[4] For details see technical data sheet: `https://www.microchemicals.com/micro/tds_az_5214e_photoresist.pdf`

promoter hexamethyldisilazane[5] at the same temperature. Resist thickness obtained is in agreement with the spin curve provided by the manufacturer. Exposure is conducted on the mask aligner MA2 or the maskless aligner MLA100 at parameters optimised by dose tests. Resist development is done in AZMIF326 (microchemicals) at RT for 60 s followed by cleaning in deionised water. The corresponding runsheet for fabrication in the HNF cleanroom is attached in the appendix, see Apx. A.5. Obtained resist resolution of optical lithography is about 0.5 µm[6] with respect to the design and allows for definition of feature sizes down to 1 µm.

SURFACE TREATMENTS

A variety of surface treatments compatible with cleanroom fabrication is known [174]. If native oxide formation is not avoided by *in-situ* fabrication, the native oxide is removed by either wet or dry etching in this work. A general characteristic of these processes is etch-rate, homogeneity and, if multiple materials are involved, selectivity. Details on an Ar milling process are provided in Sect. 3.4, and for different dry etching techniques, RIE or atomic hydrogen etching, in Sect. 5.3. In contrast to dry etching, selectivity of wet etching can be significantly higher [175]. The wet etching processes based on HF, potassium dichromate and TMAH used within this work are described in Sect. 5.3 and Sect. 5.4.

IMPLANTATION DOPING

For implantation doping, the ZnSe substrates are tilted by 7° during ion bombardment at energies of several 10 keV[7]. All ZnSe substrates studied have a thickness of about 1 µm (700–1100 nm) and were either epitaxially doped, or doped by implantation. Parameters for implantation are given in Tab. 3.3. Target value for the doping region is a level of $1 \times 10^{19}\,\mathrm{cm}^{-3}$ donor atoms in the bulk, well above MIT. For the implanted samples the depth profile of carrier concentration allows for a rather constant doping concentration up to a depth of about 20 nm and will decrease to zero for penetration depths larger than 50 nm according to SIMS characterization.

DOPING DURING EPITAXIAL GROWTH

As alternative to implantation, donor atoms can be applied non-invasively by epitaxial doping. N-type doping at concentrations of 2×10^{15}–$2 \times 10^{19}\,\mathrm{cm}^{-3}$ is obtained employing a temperature controlled $ZnCl_2$ effusion cell. Details on the characterization of doping in form of calibration data and discussion of electrical transport for ZnSe:Cl and ZnMgSe:Cl can be looked up in Chap. 4 in Sect. 4.2.1 and Sect. 4.2.2, respectively.

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[5] `https://www.microchemicals.com/products/adhesion_promotion/hmds.html`

[6] discrepancy of resist pattern with respect to design/mask

[7] Still significant channeling occurred since doping profiles (SIMS) are deeper than predicted by SRIM

CONTACT DEFINITION BY WETCHEMICAL ETCHING OF AL CONTACTS

A common technique for fabrication of ohmic contacts is metal lift-off based on optical lithography (Sect. 5.3). When taking advantage of an oxide-free metal-semiconductor interface obtained by *in-situ* fabrication, optical lithography can not be applied, since optical resist is not compatible with the epitaxial growth process in MBE under UHV conditions (Sect. 5.2). Thus, contact structures are defined by etching in combination with a resist mask applied after metallization. For the metal etch, preservation of high surface quality and low defect concentration of the II-VI HS is required ruling out RIE processes due to their invasive impact from physical etching. Instead, wet chemical etching with very high selectivity is chosen, compatible with subsequent metallization *in-situ*. The strong base (tetramethylammonium hydroxide) TMAH is known to attack Al [176]. Etch rate of this process for a concentration of 2.38 % TMAH (developer AZ326 MIF, microchemicals) is 0.23 ± 0.03 nm/s, see Fig. 5.9 a). The etch rate is averaged for the entire process of Al removal on the sample for Al layers with typical thickness of about 100 nm covered by a native oxide expected to be ~3 nm thick after hours of exposure to atmosphere [177].

Variations in etch rate observed can be explained by two aspects: The native oxide of Al is also etched by TMAH, although at a lower etch rate of ~0.02–0.03 nm/min which can be also expressed as high selectivity of about a factor of 10 for etching Al versus AlO_x. The combination of high selectivity combined with typical differences of the oxidised Al surface lead to significant variations in the etch time for a single sample. In addition etch rate can be affected by differences in agitation of etchant versus sample. Further the etch process is linearly dependent on TMAH concentration which can decrease over time when multiple samples are etched in series or a high amount of Al is etched (many samples). Reproducible etch results are obtained by a combination of process monitoring and overetching by at least 30 s, which terminates the process at the ZnSe surface acting as an etch stop. For more than 100 etch processes the yield is in the range of 95–100 % for a single contact. Stability of ZnSe in TMAH has been confirmed by optical, SEM and AFM inspection of the ZnSe surface. The TMAH based etching approach requires monitoring of the etch process. Since the samples exhibit a good contrast for reflecting metal versus absorbing semiconductor real time monitoring by bare eye or alternatively at the microscope is possible. Analysis of etched contacts verifies presence of resist underetching. This is observed by both SEM and AFM as the flank of contacts is very broad with about 3.0 ± 0.1 µm, see Fig. 5.9 b) (c, d) for SEM (AFM) characterization. Accordingly, a reduction in overall feature size by less than 1 µm has been determined by optical microscopy. The observed reduction of feature size is negligibly small compared to the overall size of contacts and thus does not affect the contact resistance. In summary, wetchemical etching of contacts with TMAH based developer is a feasible solution within an academic setting. By tolerating a reduction in feature size of up to 1 µm, our yield is sufficiently high and close to 100 %.

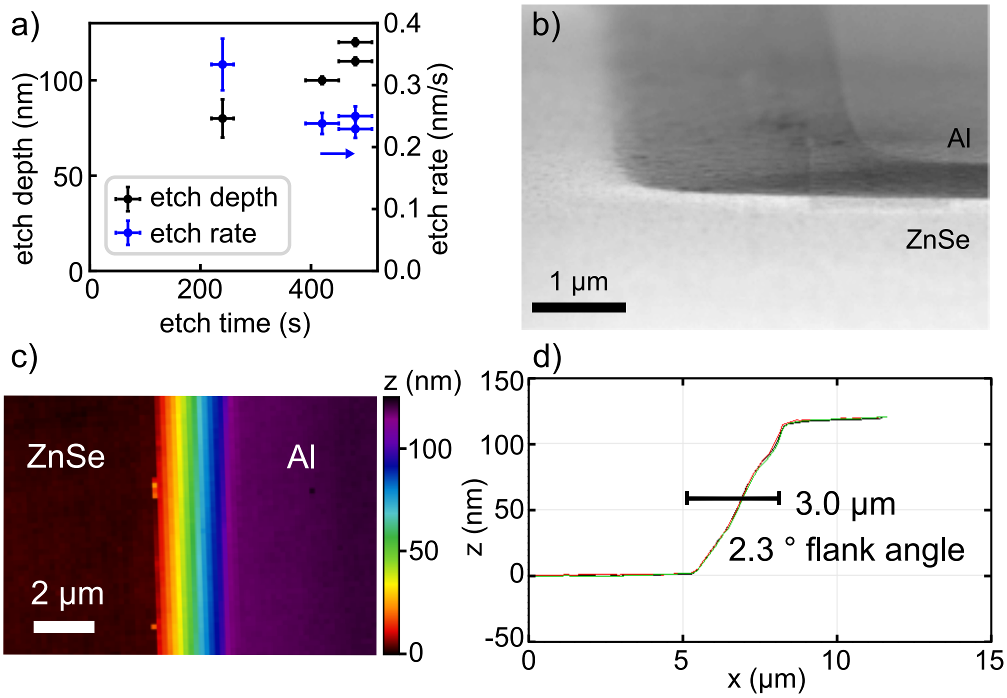

Figure 5.9: Contact definition by wetchemical etching. a) Etch process of Al contacts etched by TMAH based developer AZ326MIF for different samples with averaged etch rate. b) SEM micrograph in tilted view under 85°. c) AFM measurements of Al contact edge on ZnSe and d) corresponding height profiles taken at three different positions.

LOCAL OHMIC CONTACTS FABRICATED USING A REGROWTH PROCESS

To exploit the benefits of different approaches, we combine two of the previously described techniques, structuring and epitaxial doping targeting fabrication of local Ohmic contacts. Parts of the content of this subsection is published in [5]. Following the routines enabling excellent Ohmic contact performance with *in-situ* Al contacts epitaxially doped ZnSe:Cl substrates, we developed a regrowth fabrication process to demonstrate local Ohmic contacts to a buried conducting channel. The entire process is schematically depicted in Fig. 5.10.

For this approach, we used a ZnSe:Cl substrate with a carrier concentration above the critical density of the MIT. The sample was capped with AlO_x as a mask to enable subsequent selective epitaxial overgrowth with highly doped ZnSe:Cl. First, the sample was covered with the photoresist AZ 5214 E and openings for the designated Ohmic contacts were defined in the resist via optical lithography (Fig. 5.10 a). Then, the AlO_x was removed in these holes using HF (1 %) etching, and subsequently, we further etched about 35 nm deep into the ZnSe:Cl layer by RIE using a Cl_2/Ar mixture (50 sccm/5 sccm) (Fig. 5.10 b, c). To remove potential near-surface defects that may have been caused by RIE and smooth the ZnSe surface inside the hole, a wet

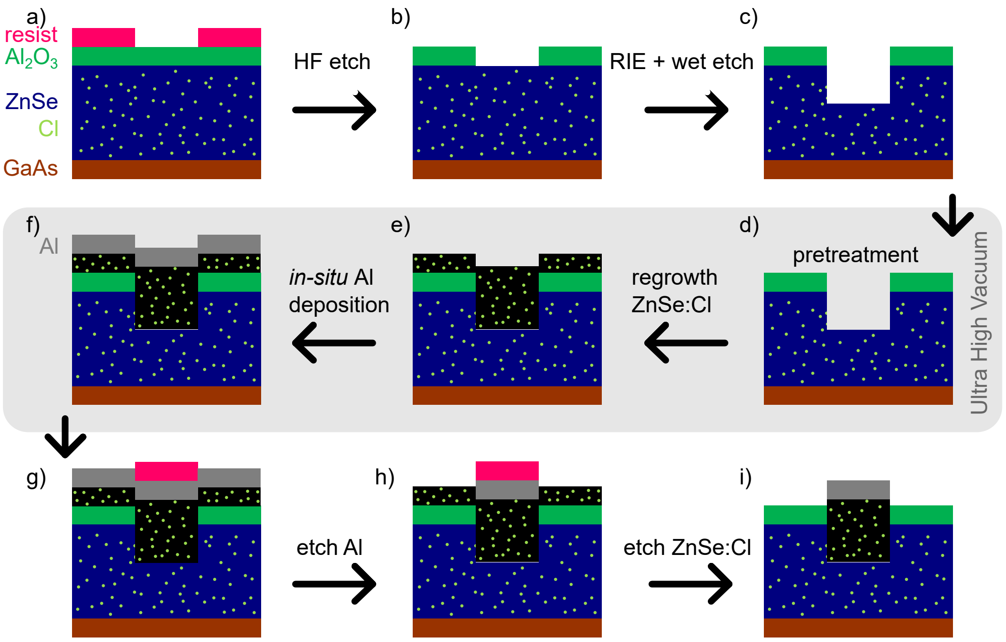

Figure 5.10: Schematic representation of the regrowth process. a) Resist mask, b) hard mask definition by HF, c) RIE etching, opening holes, transfer to MBE (UHV), d) cleaning, e) H purge f) regrowth ZnSe:Cl g) in situ metallization with Al h) contact definition i) removal of redundant regrown ZnSe. Figure adopted from Johanna Janßen [105].

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chemical etching step with a $K_2Cr_2O_7$:HBr:H_2O solution was conducted (Fig. 5.10 c). Afterward, the sample was transferred into UHV conditions within about 30 min. Before application of the epitaxial overgrowth, a thermal cleaning for 30 min at 150 °C together with hydrogen gas purge for 5 min was conducted to remove contaminants and oxide on ZnSe (Fig. 5.10 d) [178–180].

Following this surface treatment, the substrate temperature was ramped up to about 290 °C, while continuously providing a growth typical Zn flux (e.g., about 1×10^{-6} mbar beam equivalent pressure). Then, ZnSe:Cl with a doping concentration in the order of 1×10^{19} cm^{-3} was epitaxially regrown by MBE to fill up the predefined holes (Fig. 5.10 e). Finally, on top of the ZnSe:Cl, *in-situ* Al Ohmic contacts were deposited and the redundant material between the contacts was etched away from the AlO_x layer (Fig. 5.10 f-i).

The quality of the sample fabricated by regrowth is investigated electrically (Sect. 3.4.2) and by TEM analysis. A representative contact structure is selected from which a thin lamella (thickness <1 µm) is prepared by FIB structuring and glued to a sample holder for scanning. An overview of the contact profile is depicted in Fig. 5.11 a) next to TEM scan results of the contact edge and the regrowth interface (Fig. 5.11 b, c). In Fig. 5.11 b) the contact is located on the left side of the image. On the right side, no

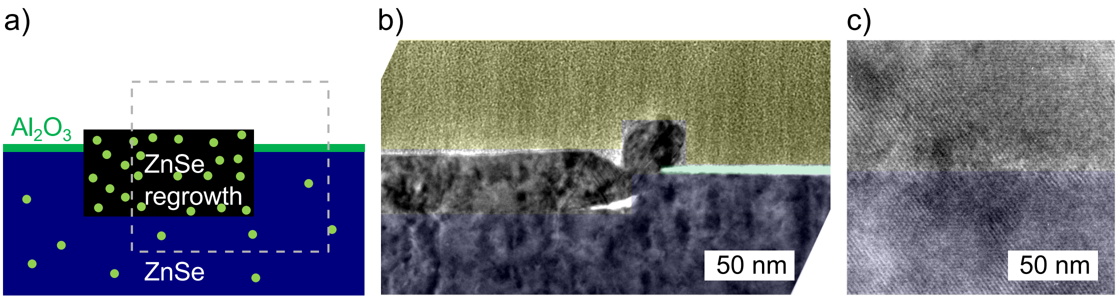

Figure 5.11: Defect analysis of regrown Ohmic contact by TEM. a) Profie of a regrown contact with the scan position highlighted. b) TEM micrograph of the contact edge. Falsecolor indicates ZnSe from the substrate prior to regrowth (blue), the hardmask (green) and regrown ZnSe (black) and Pt passivation (yellow). c) High resolution TEM result for the contact region with the defect free regrown ZnSe/ZnSe interface. TEM measurement by Marvin Jansen.

ZnSe is grown due to growth suppression of ZnSe on the amorphous AlO_x covering the sample outside contact regions. Perfect epitaxial growth at the ZnSe/ZnSe interface in the contact region can be concluded from a continuation of atomic stacking sequence and absence of line defects or dislocations, see 5.11 c). However, at the contact edges deviations from epitaxial growth arise due to non planar nature of the sample profile in this region. Here dislocations following 60° orientations are formed to reduce strain in the system [181]. The 3D nature of the contact edge leads to a non-uniform growth rate depending on the crystal orientation. The resulting 3D feature is small (0.1 µm) compared to the contact size and substrate thickness of about 100 µm and 1 µm, respectively. In consequence, the edge feature has no significant effect on the total contact resistance.

BONDING

Bonding is required for low temperature characterization in dewars (see Sect. A.2) or dilution refrigerators where probing with needles is no option. Routines for metallization and structuring of electrical contacts are documented in Sect. 5.1 and Sect. 5.3, respectively. After fabrication, structured samples are glued to IC carriers and then permanently electrically connected to ports of the carrier using a wire bonder. On the setup side the carrier is clamped by a socket on the dipstick providing in total 24 DC lines accessible by a break out box[8]. The best suited bonding machine available at the Physikzentrum in Aachen was chosen to reliably contact ZnSe samples: The west bond machine operating in wedge bonding mode provides best performance in terms of reproducible bonds. For the first bond the tool alloys an Al bond wire

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[8] Meanwhile more flexible solutions based on multiplexing have been developed within the group that were not available at the time of the experiments

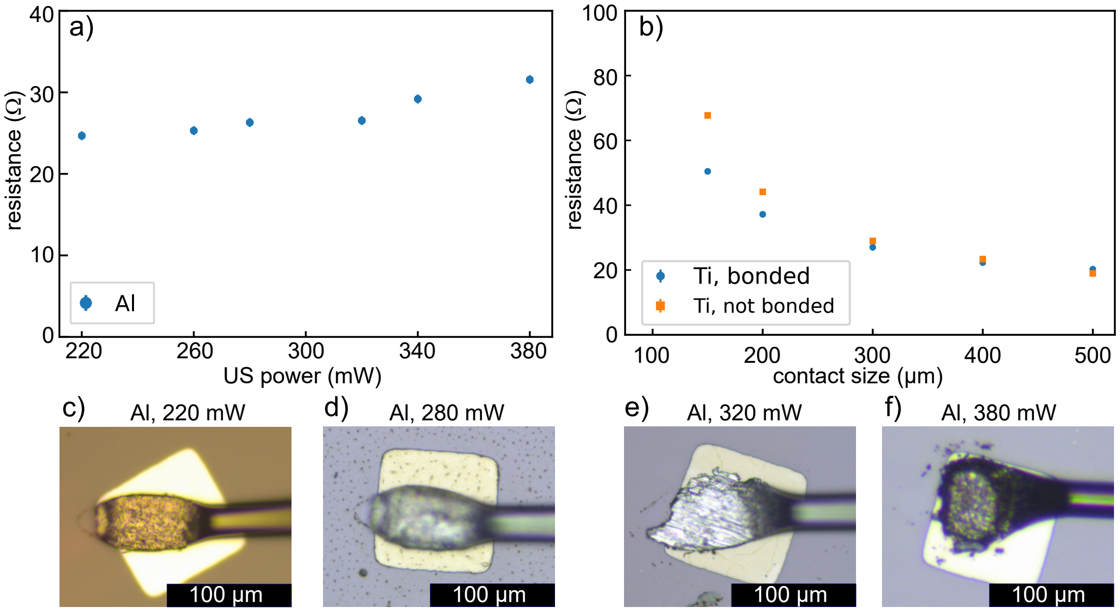

Figure 5.12: Wedge bonding of ZnSe samples. a) Electrical characterization of bonded Al contacts on ZnSe for increasing ultrasonic power P_{US}=220–380 mW over 40 ms and high force setting. Nominal pad size is $100\times100\,\mu\mathrm{m}^2$. b) Influence of bonding on contact performance for square structures with Ti in situ contacts at RT for increasing contact size bonded with P_{US}=240 mW at the west bond machine.

to a contact pad with adjustable force while supplying ultrasonic (US) power. The wire is spanned to the next pad where the procedure is repeated. Most important parameters to be optimised are force, time and power for ultrasonification that are to be tuned for a reproducible process without harming the device. Typical bonds add negligible serial resistance below 0.1 Ω to the wiring.

In this paragraph, I will discuss the result of the tuning procedure for Ohmic contacts to ZnSe samples obtained from the west bond machine operated by me. This machine was chosen since it outperformed the other two available machines[9] in terms of reliable adhesion of bonds for Al contacts on ZnSe. Fig. 5.12 a) depicts the tuning of bonding respective to ultrasonic power and success rate. A stable process window is identified for US power in the range of 220–280 mW. Here, the device resistance is not increased by destructive degradation of the device and the bond power sufficiently high to alloy the bond wire to the contact pad. For lower (higher) bond powers the mechanical stability of bonds is insufficient as a consequence of too low (high) amount of linked material introducing breaking points at the contact/bond (bondwedge/wire) interface, see Fig 5.12 c-f). Typically bonding yield is close to 100 % when bonding reference samples (Si substrate, Ti/Au contacts), however, for Al contacts on ZnSe adhesion of bonds is significantly lower leading to success rates

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[9] a) Automated wedge bonder (old bonder, 2nd Inst. Phys.) and b) gold ball wedge bonder (IHT).

down to below 50 % for a single bond. One explanation could be absence of Ti or Cr as adhesion promoter between ZnSe and Al. Another evidence for the sensitivity of the process to contact material is found by electrical characterization of Ti and Al contacts on highly doped ZnSe bulk samples, see Fig. 5.12 b) where structures were probed with needles and remeasured after bonding at P_{US}=240 mW. Typically device resistances are not altered by bonding at the chosen bond power, demonstrated here for structures of varying contact size (square contacts of different pad length) for Al contacts. However, for Ti, a systematic discrepancy of up to 20 Ω, a significant ratio of the contact resistance itself, is observed for small contact pads as the contact resistance is increased by bonding. The effect points at a fragility of especially small contacts with low mechanical resistance that can be explained by the relatively high stiffness coefficient of Ti compared to Al. Bond efficiency is at an acceptable level (50–100 %) to manually contact all relevant device types as the contact number per device is low and number of available devices is not limiting.

To conclude, the bonding process for Al *in-situ* contact pads on II-VI substrates was optimised and verified by electrical measurements for all relevant device types to reliably provide electrical contacts operating both at RT and T down to at least 4 K.

5.4. MESA ETCHING

Structuring of a current channel on planar samples is required for devices with FET or DQD architecture. Structuring is solved by wetchemical etching utilizing a resist mask defined by optical lithography well compatible with the required feature sizes larger than µm. An alternative approach to mesa etching could be (global) accumulation mode operation of all transport channels by control of dedicated accumulation gates. This sets stronger demands on the electrical properties of the HS and comes at the cost of higher effort in bandgap engineering. To maintain high flexibility in device operation (accumulation or depletion mode device) I decide for the mesa approach. Physical etching of the II-IV HS guarantees for suppression of transport in regions outside the mesa. There, undoped GaAs remains which does not conduct as no surface states are populated. Therefore an etch stop i.e. selectivity of the etch process is not essential. The only requirement on the etch profile and flank angle is set by gate compatibility: Gate metal needs to climb the mesa which can only be ensured by sufficient metal thickness or positive flank angles (≤90°) to provide electrical contact of gate metals in mesa and non-mesa regions.

Wetchemical etching is preferred versus RIE etching for ease of resist removal. Tests did show resist degradation and hardening even at low process times for the existing recipes (see Appendix) which were not further optimised. Instead, conceivable wetchemical etchants would be citric acid or nitric acid if there were no shortcomings in preparation (time-consuming dissolving overnight) and resist compatibility, respectively. The etchant of choice is a potassium dichromate based etchant which is known to be suitable for ZnSe/ZnMgSe etching while maintaining a good surface roughness [182]. Here a solution of $K_2Cr_2O_7$:HBr:H2O (1:130:250) is used for homo-

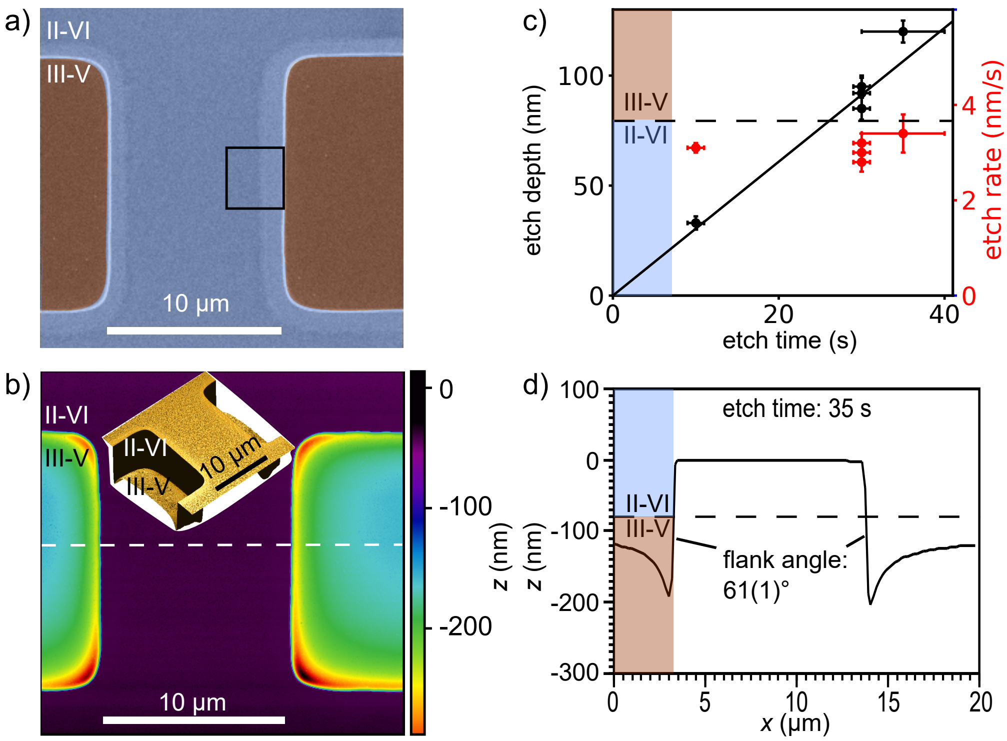

Figure 5.13: Mesa definition by wetchemical etching. a) Falsecolor SEM micrograph in top view for mesa etched ZnSe channel (centered). The brightness contrast highlighted by the black box is caused by under-etching of resist. b) Height distribution data of a nominal identical structure obtained by AFM. The insert shows a height pronounced 3D impression of the device. c) Etch depth (black) and etch rate (red) characteristics of $K_2Cr_2O_7$:HBr:H_2O for ZnSe/ZnMgSe HS derived from AFM and profilometry. The black line serves as reference for an etch process with constant etch rate. d) Height profile perpendicular to the mesa channel with flank angles quantified for the position indicated in b). In all panels II-VI mesa region (III-V substrate) is highlighted in blue (brown). Dashed lines denote the scan direction (panel b) or the position of the II-VI heterointerface (panels c, d).

geneous etch properties [182]. Diluted with water by 1:1 sufficient etch results for the mesa channel can be obtained with feature sizes only limited by resolution of optical resist, as demonstrated in Fig. 5.13. This etching process was adapted from the work of Alexander Pawlis' group and refined by me to include the use of ultrasound during etching.

Shapes defined by resist are preserved by mesa etching, as can be identified by SEM and AFM characterization, see Fig. 5.13 a,b). As intended II-VI material is completely removed outside mesa region highlighted in light blue. Absence of an etch stop leads to overetching in the III-V substrate (highlighted in brown in panel b) being very pro-

nounced at edges. The origin is not yet fully understood but is assumed to be related to redeposition reducing the effective etch rate in unstructured areas.
There, etching is most homogeneous and an etch rate of 3.3 ± 0.3 nm/s can be deduced, see Fig. 5.13 c). Data points are obtained as average values for different samples (etch time >30 s) and for a test sample (etch time 10 s), respectively. Fig. 5.13 d) depicts the height profile (AFM) of the etched channel for the position marked in panel b). The flank angle is positive with 61 ± 1° and gives green light for gate metallization using metal thicknesses lower than the mesa step size of such devices.
For detailed cleanroom instructions, possible failure modes of the ZnSe mesa etch and a description of the optimisations carried out, see Apx. A.18. In conclusion, a reliable wetchemical etch process has been identified with the reported parameters for mesa definition on heterostructures based on existing etch procedures.

5.5. THERMAL BUDGET

As discussed in Sect. 2.2.3, the thermal budged has to be low in order to suppress diffusion of the QW or dopants, expected to set in at $T \sim 430\,°\mathrm{C}$ [53]. For ZnSe samples with either Al *in-situ* grown or diffused In contacts, degradation of contact resistance was observed at even lower temperatures of 250 °C, as discussed in Chap. 3. All processing steps after MBE growth were kept at a temperature below 200 °C. Most importantly the process temperature of oxide deposition was reduced to 160 °C in a plasma assisted ALD process. During e-beam lithography, a temperature of 180 °C was applied twice for the soft-bake, each time lasting about 10 min. In summary, all fabrication processes used for device fabrication are below the critical temperature where substrate conductivity is harmed.

5.6. FABRICATION OF ISOLATED CONTROL GATES

In this section we cover the fabrication of metal gates on our devices and benchmark the isolation at RT and 4 K. As gate dielectric, we deposit and characterise ALD grown AlO_x in Sect. 5.6.1, later used for fabrication of FETs. Isolation properties of such FETs featuring a global top-gate are characterised in Sect. 5.6.2. Lastly, definition and isolation properties of nanostructure gates, contrary to a global gate, is described in Sect. 5.6.3.

5.6.1. ALD GROWN ALOX AS GATE DIELECTRIC

Thermal ALD processes for AlO_x are typically run at 300–350 °C exceeding the thermal budget for our ZnSe devices (see requirements in Chap. 2). Instead, an ALD plasma process was adapted to meet the thermal budget requirements for ohmic Al *in-situ* contacts to ZnSe QWs (with doped ZnMgSe barrier), see Chap. 3. A plasma process operating at a process temperature of 160° was used to avoid p-type Zn vacancy generation in the ZnSe substrate during deposition. Typical thickness of our ALD grown AlO_x is 18 nm, corresponding to 150 cycles. Our ALD tool (FlexALD, oxford instruments) is integrated in the Nanocluster system (FZJ). The ALD grown oxide was electrically characterised by measurement of breakthrough voltage V_{th}[10], using the approach and device design described by S. Kindel [183].

Electrical characterization data for this oxide using metal-insulator-metal (MIM) structures with a lateral scale comparable to our Hall-bar (FET) devices is displayed in Fig. 5.14 a). This pre-screening indicates sufficiently good isolation as V_{th} well exceeds 10 V, corresponding to a breakthrough at an electrical field $> 0.55\,\mathrm{V/nm}$. In a simple picture, leakage current scales with the number of defects in the oxide layer, pin holes, that are statistically distributed over the device area [183]. A systematic trend in current level versus device area is attributed to higher probability of finding pin holes in the oxide where locally isolation is reduced. Similarly, ALD grown HfO_x is characterised (Fig. 5.14 b). In comparison to AlO_x, the current levels are higher and V_{th} lower, indicating the isolation of HfO_x is less efficient. We decide for utilization of AlO_x for device fabrication for improved isolation properties and eased fabrication, since etch rates in HF are higher.

Next, we characterise the leakage current of II-VI based devices, here FETs, hosting an ALD grown AlO_x as dielectric. Thorough inspection of electrical properties such as (interface) defect density, hysteresis or the dielectric constant remains subject to future investigations. As appropriate measurement technique, I recommend the high frequency CV protocol developed by Jan Klos [184]. This technique allows for a more precise characterization of oxide defects addressing fixed and rechargeable charge defects and its dynamics, that could harm device performance of FET devices and is not covered by investigation of the leakage current.

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[10] We define the breakthrough voltage as the voltage, where the total current level exceeds 1 μA.

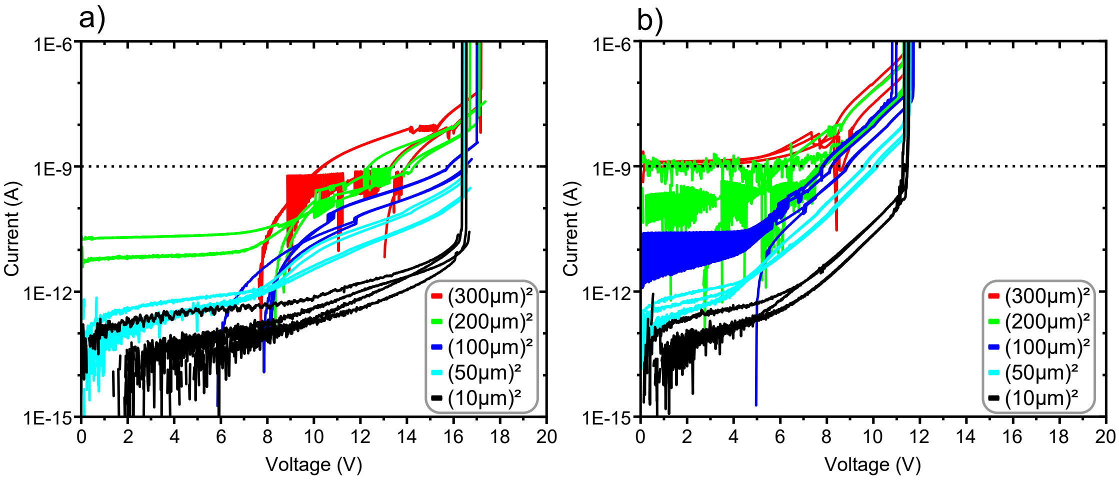

Figure 5.14: Electrical characterization of ALD grown AlO_x and HfO_x. Leakage current for MIM structures on Si measured in darkness at RT. a) (b) The dielectric consists of 18 ± 1 nm thick AlO_x (HfO_x) grown by ALD in a plasma process over 150 cycles at 160 °C. The oxide is embedded by Al contacts, structured without exposing the oxide to the TMAH based developer. The active device area is specified in the legend. Measurement carried out by Johanna Janßen.

5.6.2. ISOLATION PROPERTIES OF GATED DEVICES

Gate leakage is characterised by IV profilometry for two device types: Either Schottky gates with a small gate area ($\sim 500\,\mu m^2$) and no oxide underneath and global gates with a large area isolated by oxide from the substrate ($\sim 1\times10^5\,\mu m^2$). The designs for both device types EDQD and Hall-bar are depicted in Fig. 5.2 and Fig. 5.1, respectively. For both device types, Fig. 5.15 shows electrical measurements of the gate current I_{TG} (leakage current). The measurements are conducted at RT and at $T = 4\,K$, which is sufficiently low to suppress thermal carrier excitation across the metal (-oxide-) semiconductor interface and thus isolation properties can be considered comparable to the relevant regime for future spin qubit devices.

For a device with EDQD architecture the measurement of leakage current is depicted in Fig. 5.15 a, b). The measured device features 5/15 nm thick Ti/Pt metal gates on doped ZnMgSe ($n \sim 5\times10^{17}\,cm^{-3}$) without a gate oxide and Al contacts deposited $in-situ$. At RT, the IV curve is strongly non-linear and asymmetric, a well known behaviour of Schottky diodes. We conclude, Pt predominantly affects the height of the Schottky barrier and not Ti, since the work function of Pt is, other than Ti, not aligned with the electron affinity of ZnSe (which is presumably similar to the electron affinity of ZnMgSe). However, at 4 K, the electron transport is strongly suppressed, as the current does not exceed 0.5 nA for gate voltage up to 20 V. We attribute the observed hysteresis to capacitive effects in the measurement setup or to rechargeable defects between the gate and the conducting QW in the device, see also Sect. 6.2.

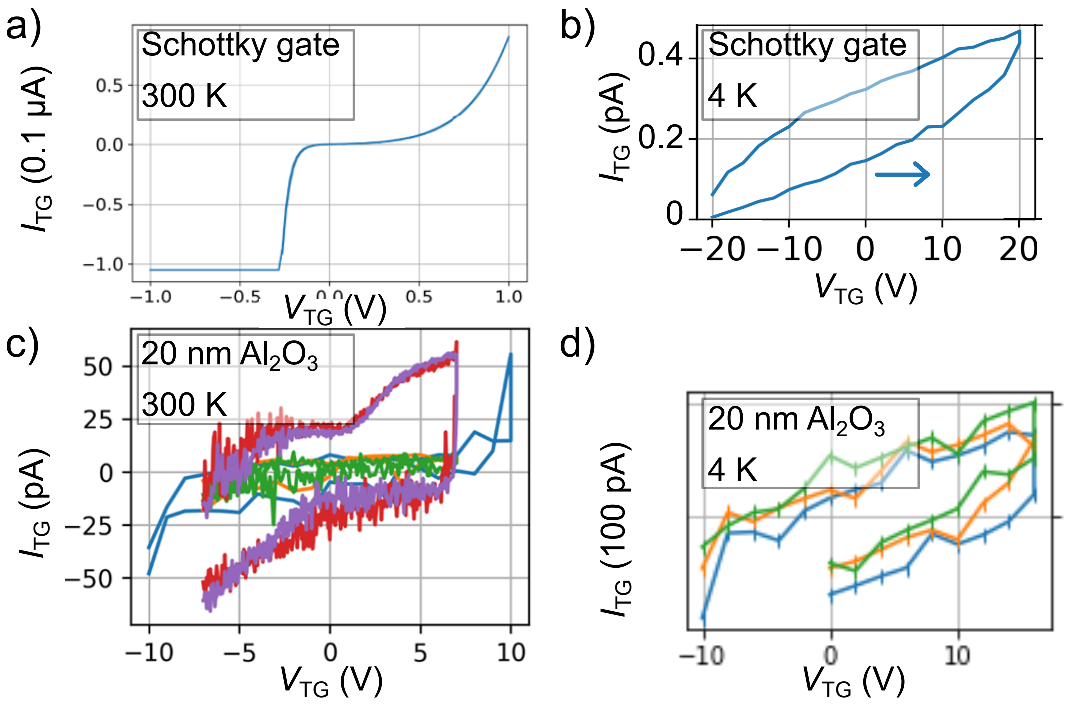

Figure 5.15: Leakage currents for different device architectures on ZnSe/ZnMgSe HS. a (b) Leakage current for Ti/Pt Schottkygates at RT (4 K). We choose a non-conservative level for the compliance at 1 µA. c (d) Leakage current (RT/4 K) for a gated Hall-bar on ZnSe/ZnMgSe HS, for 20 nm thick AlO_x gate dielectric at RT (4 K) for multiple devices, differentiated by colour.

The overall reduction in gate current we attribute to two effects: Freeze out of charge carriers in the upper ZnMgSe barrier, independently verified by van der Pauw Hall measurements, and suppression of thermal excitation at 4 K.

Similarly, we characterise FET devices repeating the same measurement procedure at RT and 4 K, see Fig. 5.15 c, d), respectively. The gate current is well below 1 nA already at RT, and even lower at 4 K, where similar hysteretic effects are observed as for Schottky gates. In summary, the gate leakage current observed is on a level well below the measured transconductance of our devices. We expect our fabrication processes to provide sufficient isolation to be compatible with gate control and read out of future quantum devices. However, based on current knowledge, we cannot quantify the level of rechargeable defects in our device, nor identify whether they are located in the substrate, metal-semiconductor interface or in the gate dielectric. Independent characterization of the gate dielectric on Si shows a strong dependence on details of the fabrication process, and remains subject to further investigations.

5.6.3. NANOSTRUCTURE GATES DEFINED BY ELECTRON BEAM LITHOGRAPHY

This subsection covers the fabrication of nanostrucutre gates required for electrical control of the target device (EDQD). As an example, the isolating properties of such a reference device are shown below in Sect. 5.7. In an academic setting, electron beam lithography is typically used to define small feature sizes below the diffraction limit of the photons from UV mask aligners (300–400 nm). Cross-linking of resist is obtained by electrons, accelerated to 50–100 keV, interacting with the resist by energy deposition.

Since the effective electron masses of ZnSe and Si are approximately the same, we expect similar electron scattering properties and therefore resolution for e - beam lithography on both types of substrate. Aiming at small pitch sizes (70 nm) for metal lift-off gates, I transferred an e-beam lithography process developed by Inga Seidler for Si/SiGe substrates to ZnSe/GaAs substrates (c.f. Sect. 2.2.6). For Si, this process enables high yield fabrication of nanostructures for process parameters independent of specific design [69]. A failure mode of this process type is improper metal lift-off, crucially dependent on gate pitch and resist profile. Successful metal lift-off requires vertical or negative resist flanks, i.e. an undercut. Here, we use two resist layers of different molecular length (50 k, 950 k) and thus electron absorption, to guarantee for an undercut, as schematically illustrated in Fig. 5.16 b). At the edges of structures we expect an undercut after development conducted in IPA and IPA/water, qualitatively verified by subsequent successful metal lift-off. All process parameters, cleanroom instructions (run sheet) and device design are provided in Tab. 5.3, Apx. A.5 and Fig. A.16, respectively.

Here, I present an overview on the main characteristics of the entire process shown in Fig. 5.16 a), c) and d) by means of resist coating, resist exposure and combined process window, respectively. Spin curves for the two types of resist are depicted in Fig. 5.16 a), for a single and a double layer. The spin curve for the single layer is in agreement with the specifications provided by the manufacturer, taking the reduced coating time and chip size into account [185]. Combining both resist types, we adjust the process to obtain a thin resist stack of 110 ± 10 nm thickness. We keep the wait time fixed at 5 s, during which layer 2 partly dissolves layer 1 prior to spinning.

Our process requires e-beam markers providing high contrast and small line edge roughness for alignment during the exposure process. We fabricate e-beam markers from Ti/Au of 5/50 nm thickness and a size of $20 \times 20\ \mu m^2$, using optical lithography with a glass mask, metallization and metal lift-off (Sect. 5.2 d). Our marker fabrication results in an alignment precision of less than 200 nm in the subsequent e-beam lithography process, where the devices are defined. Although not required for our purpose, an alignment precision below 10 nm can be realised by optimization of the writing process at the e-beam tool used, allowing for multilayered gate architectures [69].

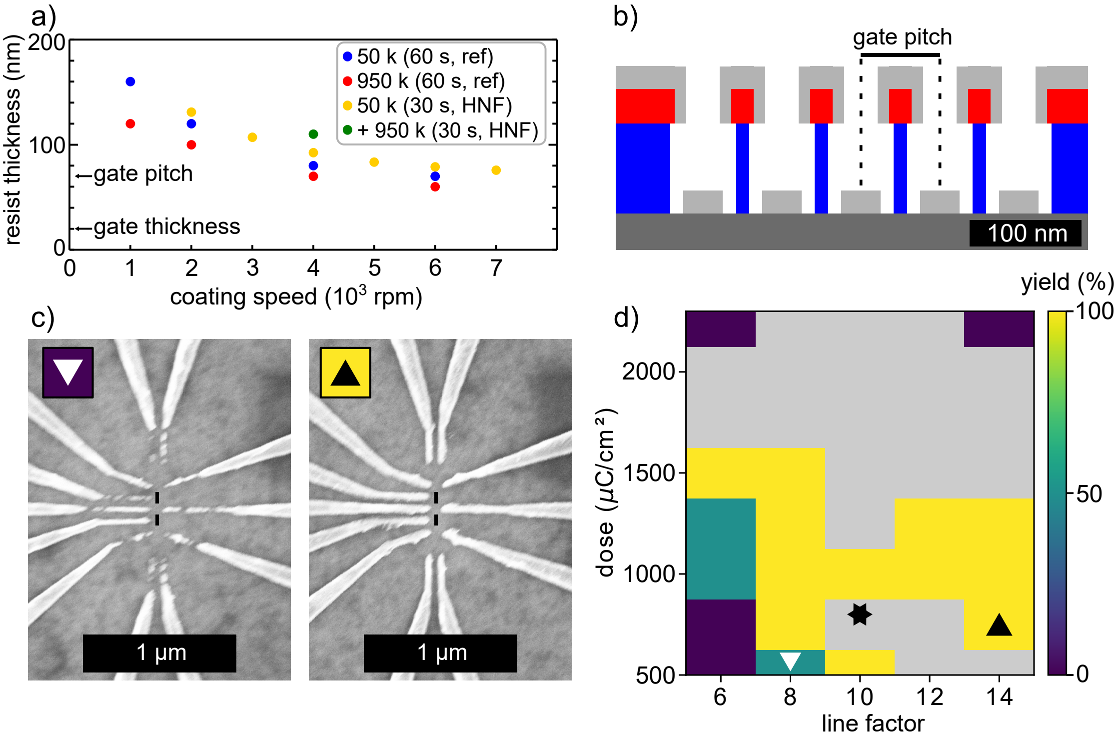

Figure 5.16: Nanostructure gate definition on II-VI substrates by e-beam lithography and metal liftoff. a) Specified spin curves (ref) for PMMA resist with 50 k (blue) and 950 k (red) molecular length, respectively, next to a spin curve reproduced in our lab for layer 1 (50 k) (orange). The green dot represents a double layer using the same rotation speed and time for both layers. The resist thickness is determined by ellipsometry. Arrows mark the gate thickness and gate pitch, also indicated in panels b, c). b) Schematic of the resist system after e-beam exposure, development and metal deposition. c) A subset of scanned devices with nanostructure gates is categorised (0/1) for the assessment of process yield. The minimal gate pitch is indicated by black lines in the center. d) Exposure parameters versus process yield, determined from inspection of ~75 devices. There is no data available for the grey regions. Triangles mark the parameter set corresponding to the devices shown in panel c) and the star those used for fabrication of complete devices (see text).

The process resolution is correlated to electron scattering in the III-V/II-VI substrate, depending on atomic mass which is lower for Si. To compensate for resist exposure originating from electrons back-scattered by the substrate, a proximity correction is made. The underlying Monte-Carlo simulation yields an effective scattering length of 20–30 µm for 100 kV acceleration voltage and locally down-corrects the e-beam dose, dependent on the gate design.

Prior to device fabrication, the process window for e-beam lithography is determined in a dose test, using the design of the target device: A gate structure compatible with formation of an EDQD with adjacent SETs, depicted in Fig. 5.16 c). Details of the dose tests conducted are provided in Tab. 5.3. We determine the process yield for a given set of parameters using SEM inspection, distinguishing gate structures with and without metal shorts. The result is shown in Fig. 5.16 d) for process B in a color map, obtained from scanning ~75 devices on two chips. We note a systematic dependency between the two process parameters, the global exposure dose and a line factor which is applied to the dose of the smallest structures. The lower boundary of the process window where a sufficient exposure dose is achieved (no failure observed), is found for a global dose of 525 (700/1300) µC/cm^2 and a line factor of 10 (8/6). Overexposure has the effect of shorting gates when their width exceeds the gate pitch, observed at a dose of 2250 µC/cm^2 for all line factors.

Table 5.3: Process details for e-beam lithography of ZnSe/GaAs substrates for small pitch gates obtained by metal lift-off.

parameter	unit	A	B
acceleration voltage	(kV)	50	100
substrate		III-V/II-VI	III-V/II-VI
dose	(µC/cm^2)	525-3500	525-3500
line factor		6-14	6-14
pitch size by design	(nm)	70	70
gate thickness, Ti/Pt	(nm)	5/15	5/15
e-beam markers, Ti/Au	(nm)	5/50	5/50
beam current (coarse/fine)	(nA)	3/ 0.15	3/0.15
nominal resolution	(nm)	5/1	5/1
process window			
min. dose/factor	(µC/cm^2)	525/10.5	525/10
max. dose/factor	(µC/cm^2)	-	1300/14
yield	(%)	95(5)	95(5)
screened devices		~ 75	~ 75

Choosing a suitable set of parameters determined from the dose test (Tab. 5.3, process B, Fig. 5.16 d)), we demonstrate successful definition of nano-structured devices with 70 nm gate pitch. The process yield is 81 % for all 16 mesa etched devices on a 10×10 mm^2 chip, for a dose of 800 µC/cm^2 and a line factor of 10, indicated by the star in Fig. 5.16 d). Our result represents a successful process transfer from Si based to III-V (II-VI) based materials, without compromising gate pitch. Therefore, we do not expect any limitations in process yield, which in principle allows for further scale-up.

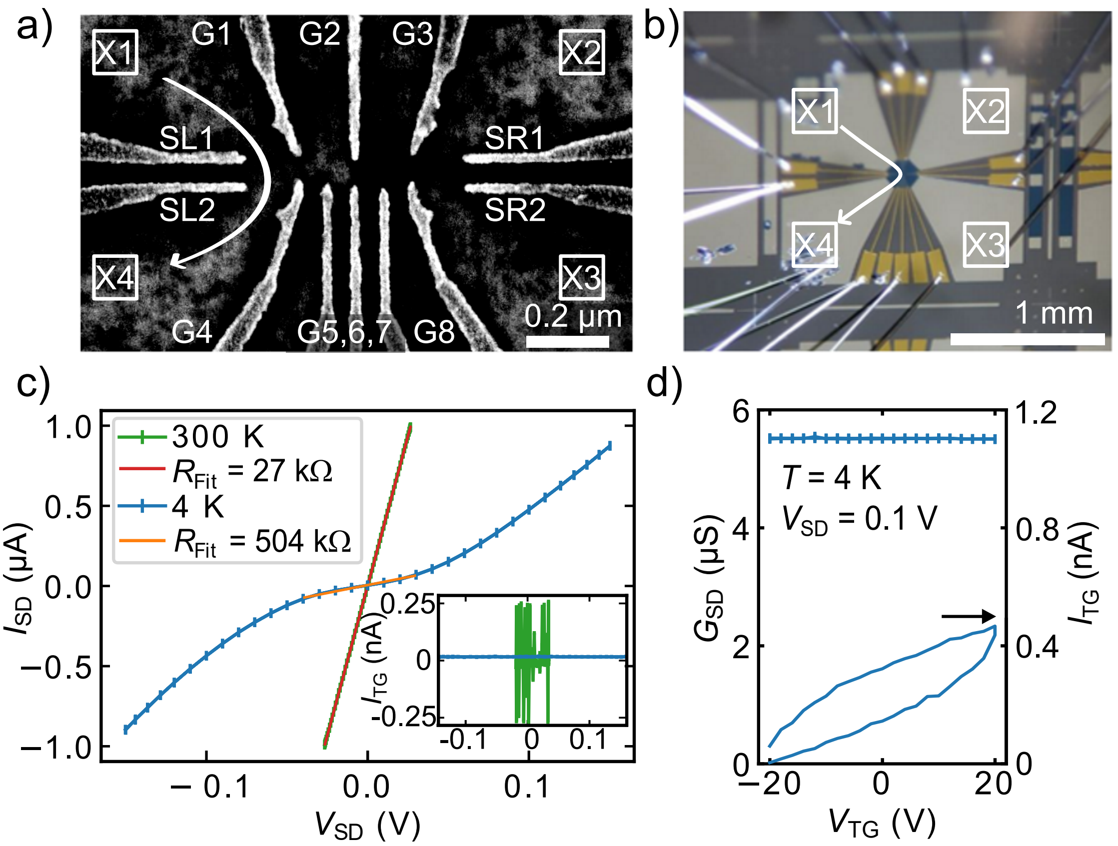

Figure 5.17: Electrical characterization of a device with EDQD architecture at RT and 4 K. a) Zoom in to nanostrucuture gates obtained by e-beam lithography (Sect. 5.6.3). The terminal configuration and gate labels are indicated. b) Micrograph of the device after bonding. For technical reasons, gates G5 and G7 are not contacted. c) IV characteristics of device resistance at RT and 4 K. All gate voltages are set to 0 V. The insert depicts the gate current (leakage current). d) Transconductance versus gate voltage V_{TG} applied to gates SL1, SL2, G2, G4, G6. Simultaneous sweep of all gate voltages. The gate current is plotted on the right vertical axis (arrow). Hold time is 5 s between individual measurements (data points), V_{SD} is 0.1 V.

5.7. Verification of the fabrication process for an EDQD device

Next, we combine all fabrication steps presented in the previous sections to verify their compatibility and check an exemplary device for connectivity and gate isolation. Following all fabrication steps depicted in Fig. 5.2, we fabricate a device with the architecture of the target device (EDQD). However, lacking a process to locally contact a ZnSe QW (Sect. 3.4.2), doping of the HS is required to achieve contact to and conduction in the QW (Sect. 3.5). In specific, parameters determined from a subsequent dose test (Fig. 5.16 d)/ star) were used to reliably obtain the desired nanostructure gates after metal lift-off. The resulting gate architecture and configuration of terminals for a bonded device is depicted in Fig. 5.17 a) and b), respectively. Next, we verify electrical connectivity of all four contacts and characterise two of them, X1 and X4, in detail. During this experiment, all top-gates are set to 0 V. We obtain a total resistance of 27 kΩ and 504 kΩ by fitting the IV curve for zero bias at RT and 4 K, respectively (Fig. 5.17 c). The device resistance is governed by the contact resistance, since the sheet resistance determined independently by a van der Pauw Hall measurement is significantly smaller (3–4 kΩ/☐). At 4 K, the IV curve is nonlinear, which we attribute to a freeze out of charge carriers in the upper barrier increasing the tunnel resistance, also observed in similar heterostructures (Sect. 3.4).

Next, we analyse the leakage current of the Schottky gates. At RT, we observe I_{TG} of ~0.2 nA, which we assign to the consequence of improper shielding for the measurement at RT. The rectifying behaviour and break through of the Schottky contacts at ~ 0.1 V can be observed, when applying a voltage directly to the top-gates, already described in Sect. 5.6.2. However, when properly shielded and cooled down to 4 K, the leakage current is only at the order of 10 pA and for gate voltages (electrical field) below ±20 V (±0.4 V/nm) no breakthrough is observed (Fig. 5.17 c,d).[11] Thus, our device is properly isolated. We conclude, Schottky gates on a II-VI HS produced following our device fabrication including the e-beam lithography process, is compatible with electrical contacting, readout and control of all electrical quantum devices (Sect. 2.2).

5.8. SUMMARY AND CONCLUSIONS

Pursuing the goal of identifying a suitable toolbox for fabrication of (planar, all-electrical) quantum devices with II-VI semiconductors, we have identified a set of processes for MBE growth and structuring and associated characterisation techniques, all of which are specific to the requirements of this work. Addressing the various requirements for realization of EDQDs in semiconductors (Sect. 2.2), we recap all fabrication processes introduced in this chapter in a restructured way:

OPERATION TEMPERATURE

For conditions comparable to the operating regime of qubits ($T \leq 4$ K, Sect. 2.2.1), with suppressed thermal excitation, we successfully demonstrate connectivity and sufficient gate isolation for reference devices operated at $T = 4$ K. The basic fabrication steps are *in-situ* fabrication (Sect. 5.3), prerequisite for low resistivity Ohmic contacts, and deposition of $\mathrm{AlO_x}$ by ALD with excellent isolation properties at 4 K (Sect. 5.15, Fig. 5.15 d). Furthermore, the HS and device architecture proposed and fabricated (Sect. 5.17 and 5.2, respectively) provides sufficient confinement to define spin qubits in ZnSe with orbital energy of excited states well above $k_{\mathrm{b}}T$.

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[11] At 4 K, the detected gate current is higher for the gate sweep than for the sweep of source drain voltage, which is attributed to a parasitic capacitive effects dependent on the measurement speed

OHMIC CONTACTS

Initialization and readout of spin qubits demands low resistivity Ohmic contacts ($\rho_c \leq 1 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$) to n-ZnSe operating at $T \leq 4\,\mathrm{K}$, see Sect. 2.2.2. Key requirement for Ohmic contacts to ZnSe is a doping concentration on the metallic side of the MIT ($n_c > 5 \times 10^{17}\,\mathrm{cm}^{-3}$) (Sect. 4.1.2). Doping has to be combined with choice of a proper metal (i.e. it's work function) and well controlled treatment of the metal-semiconductor interface in order to obtain a low SBH (Sect. 3.2). Experimentally we addressed low resistivity contacts to bulk ZnSe by metallization *in-situ* with Al (Sect. 5.3), or as alternative, a combination with preceding structuring and surface treatment of contacts, shown in the regrowth process (Sect. 5.3). For both approaches, we obtain a low contact resistance ($\sim 1 \times 10^{-3}\,\Omega\,\mathrm{cm}^2$) at an absolute contact resistance below $10\,\mathrm{k}\Omega$ at 4 K. Transfer of the first process to a ZnSe QW is possible (Sect. 3.5). However, local contacts to a QW structure can not be defined lacking a suitable technique for local doping. As solution, an approach utilizing a shadow mask is suggested inChap. 7, adding selectivity to the otherwise planar technique of epitaxial doping.

THERMAL BUDGET

Literature reports suggest a thermal budget for fabrication of ZnSe based devices of ~250–300 °C (Sect. 2.2.3). Compared to our work (Sect. 3.4, 3.5), this thermal budget has been found to be too aggressive for fabrication of high quality ZnSe/ZnMgSe as Zn vacancies form [49, 50, 53, 186]. Thus, we down-correct the thermal budget of ZnSe to 200–250 °C for processes on a minute scale in absence of partial Zn and Se pressure. Our experimental work suggests, contacts fabricated using diffusion or implantation require annealing beyond the thermal budget of ZnSe/ZnMgSe, and are thus incompatible with low resistivity contacts (Sect. 3.3.1, 3.3.2). In consequence, we can identify a set of other processes for fabrication of Ohmic contacts (Sect. 5.3) and gated devices (Sect. 5.1) within the thermal budget without degradation of crystal quality or contact resistivity.

CHARGE NOISE

Up to now, charge noise (Sect. 2.2.4) mediated by artificial spin-orbit coupling, predominantly affects qubit performance in Si based systems [1, 187]. Within this work, charge noise could not be quantified our experiments since a lack of local ohmic contacts and thus device control prevented measurements in the few electron regime. We indirectly probe charge defects by PL, CV profiling, or TEM, but still no absolute level of charge noise can be deduced. Using these techniques, the fabrication process was optimised for low defect densities in fully strained, undoped HS.

In specific, relaxation-free HS can be grown, verified by XRD and TEM. For undoped ZnSe (ZnMgSe), we find a low background doping concentration of $n = 1 \times 10^{16}\,\mathrm{cm}^{-3}$ ($2 \times 10^{16}\,\mathrm{cm}^{-3}$) in van der Pauw Hall measurements (Sect.5.2), that we consider as upper bound for ionised impurities. In order to prevent formation of p-type Zn vacancies, the thermal budget ($T = 200--250\,^\circ\mathrm{C}$, Sect. 5.5) in our fabrication processes is not exceeded after growth. Furthermore, we separate regions with charge defects introduced by doping (local ohmic contacts) from the active device region by design. Quantification of the density of charge defects, presumably governed by defects between semiconductor and metal gates, remains subject to further investigations (Sect. 5.6). So far, our study did not reveal other relevant sources for charge defects in ZnSe/ZnMgSe HS.

SPIN-ORBIT INTERACTION

In principle, the coupling strength of SOI is a material constant that is fixed for bulk ZnSe, but in a 2D QW prone to details of the heterostructure, such as sharpness of the heterointerfaces (Sect.2.2.5). For the proposed target device, a design with an interdot distance significantly lower than the spin orbit length (21 µm) is chosen [8]. Realization of corresponding nanostructure gates with a gate pitch of 70 nm in a reproducible way could be shown (Sect. 5.7). With a sufficient coupling constant, ZnSe based EDQDs could be driven by internal magnetic fields without the need to fabricate micro-magnets adjacent to each device.

When embedded in ZnMgSe barriers, the crystal lattice of the ZnSe QW is biaxially strained (Sect. 5.2), which can affect the symmetry of the HS. Deviations from symmetric systems have been observed in electrical transport, such as anisotropy (Sect. 4.3) in the QW, presumably related to SOI, which remains the subject of further investigation.

MEAN FREE PATH

The mean free path is required to be higher than the interdot distance of ~ 100 nm, see Sect. 2.2.6. Experimentally, high electron mobility of 3.2×10^3 cm^2/Vs, only a factor 3 lower than the world record, has been demonstrated within this project for undoped bulk ZnSe samples at ($T = 60$ K) [112]. This results underlines the high quality of II-VI bulk and HS that can be achieved using the available tools and knowledge. For undoped ZnSe bulk, the background doping concentration (charge impurities) of 1.5×10^{16} cm^{-3} corresponds to an average interdonor spacing of ~ 40 nm at RT.

However, transport properties measured in this work (n, μ) are not compatible with the target regime of 2D transport in undoped strained ZnSe QW with low carrier concentration. A regime of lower carrier concentrations could not be reached, since ohmic contacts were not compatible with electrical control. The lowest carrier concentration achieved in the ZnSe QW was 3×10^{17} cm^{-3} with an electron mobility of 500 cm^2/Vs at $T = 25$ K. These values are a lower bound for mobility since carriers were photo-excited and underlying dynamics could increase scattering. Further the effect of free carriers in the barriers has to be considered when interpreting the results. Again, more valuable information can be extracted from devices exhibiting a gate controlled field effect. The maximum electron mean free path derived from transport experiments in the bulk (30 nm, see Sect. 4.2.1) is, unlike required, lower than the interdot distance demonstrated by fabrication of nanostructure gates with the layout of the proposed EDQD device. However, significant improvements are expected when going from 3D to 2D systems when local ohmic contacts allow operation of FETs defined on our ZnSe/ZnMgSe HS.

CONCLUSION

At the end, we have established a process flow for growth and structuring of TLM devices, FETs and potentially EDQDs based on ZnSe/ZnMgSe material. MBE grown ZnSe and ZnMgSe exhibits high crystalline quality, demonstrated by growth of fully strained ZnSe QWs with a confinement energy (150 ± 20 meV) compatible with the target EDQD device. New in our processes is a higher Mg concentration in ZnSe/ ZnMgSe HS, optimised *in-situ* metallization of (local) ohmic contacts and realization of nanostructure gates with a pitch of 70 nm on a ZnSe (GaAs) substrate, all in compliance with a thermal budget of 200–250 °C. The processes are adopted to allow for high device quality in terms of defect concentrations determined by structural, optical and electrical characterization of microscopic structures. So far, the introduced fabrication techniques for realization of ohmic contacts and electrical control of devices have opposing prerequisites on the doping concentration of contact versus quantum region. A possible solution, based on local ohmic contacts utilizing selective growth mediated by a shadow mask, is proposed in the last chapter (Chap. 7). Closing remarks, the identification of a tool set covering growth, contacting and structuring of ZnSe motivates future exploration of the potential of ZnSe based quantum devices, like the EDQD device proposed.

CONTRIBUTIONS

II-VI substrates and heterostructures were grown by A.P (2017-2019) and Nils von den Driesch (2019-2022). Benjamin Benneman performed growth of III-V buffers, oxide deposition by ALD or e-beam evaporation, atomic hydrogen cleaning and metallization *in-situ*. Christoph Krause contributed to buffer growth and metallization *ex-situ*. Johanna Janßen assisted sample fabrication and analysis from 2016-2020 and electrically tested isolation of ALD grown oxides on Si. Janine Worbs, Jhih-Sian Tu or Rainer Benczek provided metallization of samples. Elmar Neumann did perform EDX analysis and FIB. Lidia Kibkalo contributed to lamella preparation by FIB. Uwe Breuer performed characterization by SIMS. Nils von den Driesch performed structural and van der Pauw Hall analysis. Stefan Trellenkamp and Florian Lentz operated the e-beam writer. Inga Seidler gave me a kick off introduction to e-beam lithography by sharing knowledge and recipes developed for Si devices. TEM analysis was performed by Marvin Jansen and Jin Hee Bae. Sample implantation was done in-house by Andre Dahmen using the ion implanter at PGI9. Besides processes in the Nanocluster, the infrastructure of the HNF was used for most fabrication processes [188].

6

MEASUREMENT OF THE FINAL DEVICE

Having introduced the basic transport phenomena in n-type ZnSe or ZnMgSe in Chap. 4 and fabrication processes for structuring, contacting and gating n-type ZnSe in Chap. 5, enables exploration of electrical control of gated devices. As a step towards charge readout and noise characterization of quantum devices utilizing a SET, the goal in this chapter is to investigate electron transport at comparable experimental conditions. Here, we utilise a field-effect transistor (FET) with a nominally undoped ZnSe QW, operated at 4 K, for transport measurements on a macroscopic scale. We will focus on measurements of transconductance to identify the relevant transport mechanisms (Sect. 6.2). The experiments discussed in this section are subject of Benjamin Zenz's master's thesis [148].[1] We conclude with a discussion of our results and the potential of the ZnSe/ZnMgSe platform for all-electrical quantum devices.

6.1. DESCRIPTION OF THE DEVICES AND THE MEASUREMENT TECHNIQUE

For our purpose we use the device design as shown in Fig. 6.1 b). On a ZnSe/ZnMgSe HS with a layer stack as depicted in Fig. 6.1 a), gated Hall-bar devices are fabricated following the routines outlined in Sect. 5.1.1. To investigate the influence of the QW on the electrical transport properties, we fabricate a series of devices on a HS without a QW in parallel. The HS used for these devices have a doped upper ZnMgSe barrier of varying thickness on an undoped lower ZnMgSe barrier of 50 nm thickness, see Apx.,Fig. A.22 a). We expect superior transport properties for devices with a ZnSe QW compared to the reference samples without, where the formation of a triangular QW in the ZnMgSe at the semiconductor-oxide interface is predicted by simulations. By

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[1] My main contributions were device fabrication and together with Benjamin Zenz and Lars Schreiber development of the measurement protocol (Sect. 6.1). All contributions are specified at the end of this chapter.

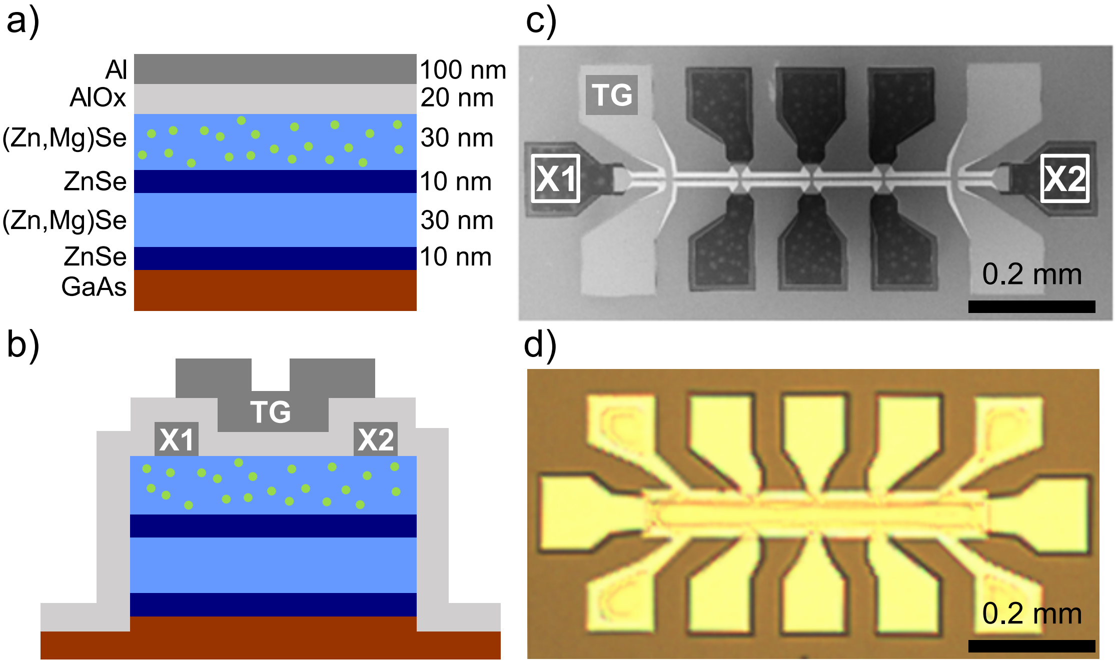

Figure 6.1: Gated Hall-bar on a HS with a nominally undoped ZnSe QW. a) Profile of a gated heterostructure with the Cl doping profile schematically illustrated as green dots. b) Device profile with contacts and top-gate labeled as "X1/X2" and "TG", respectively. c, d) Images of a typical gated Hall-bar device obtained by SEM and optical microscopy, respectively. The other six contact pads in the center region (dark in panel c) are not connected.

XRD we confirm growth of fully strained, relaxation free epilayers for all structures with a QW (data not shown), while relaxation is relevant for the reference samples since the total layer thickness is higher.

SIMS profiles of the Cl concentrations in these epitaxially doped structures are shown in Fig. 6.2 a) for a representative ZnSe/ZnMgSe HS with QW and in Apx. A.20 for similar ones. Measured Cl concentrations are 3×10^{18}–$1 \times 10^{19}\,\mathrm{cm}^{-3}$ in doped and $\sim 1 \times 10^{17}$–$3 \times 10^{17}\,\mathrm{cm}^{-3}$ in nominally undoped regions. Comparing these to the critical density of the MIT $n_c = 5 \times 10^{17}\,\mathrm{cm}^{-3}$ ($7 \times 10^{17}\,\mathrm{cm}^{-3}$) in ZnSe (ZnMgSe), see Chap. 4, we expect metallic or insulating behaviour at $T \to 0\,\mathrm{K}$ in doped and undoped regions, respectively, if compensation is negligible. The background doping concentration for these structures is tenfold increased compared to optimal conditions, associated to an increased Cl concentration in the Se source material. The unexpectedly high Cl concentration region in the lower buffer is a consequence from a calibration routine conducted during MBE growth, which we were not aware of when the samples were fabricated. Both, low background doping concentration and absence of Cl accumulation in the lower barrier were successfully achieved in subsequent growth runs, ver-

ified by SIMS (data not shown).
To investigate the effect of electron confinement on transport, we determine the transconductance of FETs in two terminal configuration by adjusting the voltages V_{SD} between two Ohmic contacts (X1, X2) and the top-gate voltage V_{TG}. Simultaneous to the source-drain current I_{SD}, from which the transconductance $G_{SD}=I_{SD}/V_{SD}$ is obtained, we probe the gate current I_{TG}. An optical impression of a representative gated Hall-bar and the terminal configuration is provided in Fig. 6.1 c, d). Dimensions of the conducting channel are 100 µm × 800 µm.

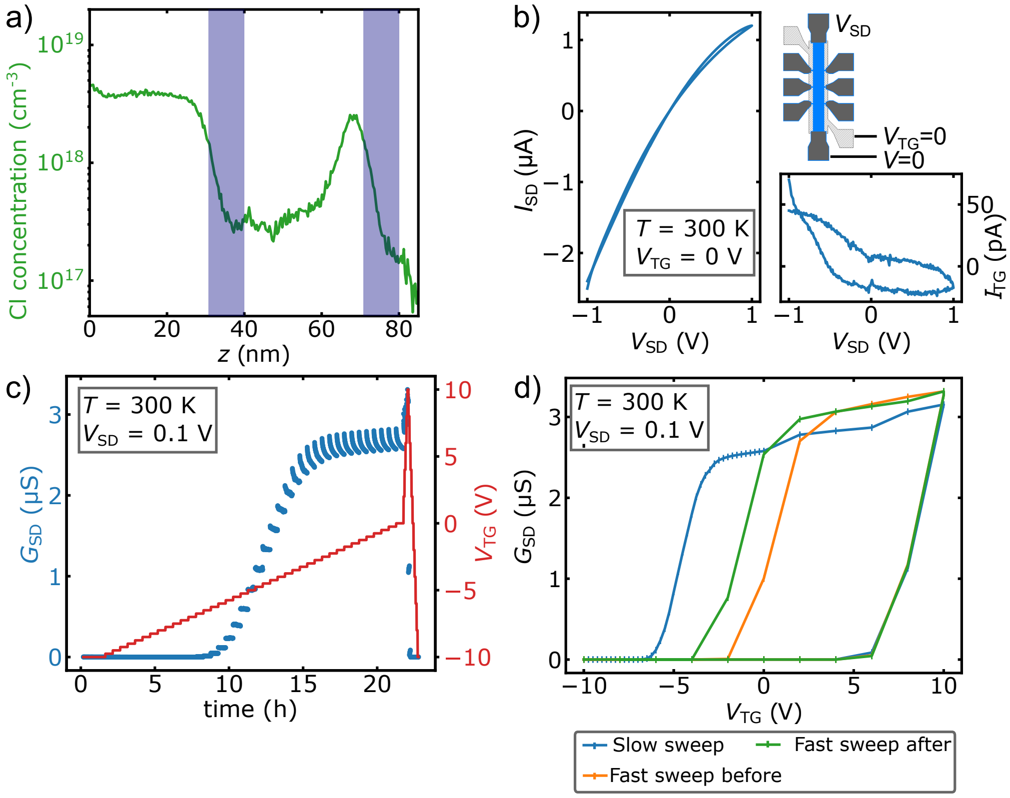

Figure 6.2: Measurement scheme for FETs on a ZnSe/ZnMgSe HS. a) Cl concentration profile obtained by SIMS, with the positions of the ZnSe QW and buffer highlighted in blue. b) Check of Ohmic contacts by IV profiling and check of gate isolation (I_{TG}) for a device with a 100 µm wide mesa channel in the given terminal configuration (see sketch). c) Measurement protocol for a FET at RT, lasting one day including initialization: G_{SD} versus time (V_{TG}, see right axis) is recorded in darkness at a needle probe station. d) G_{SD} versus V_{TG} for three sweeps performed in series, one fast scan with 20 s per point before (orange) and after (green) a slow sweep with 30 min per point (blue, c.f. panel c). The measurement was conducted by Benjamin Zenz. Figure adoped from [148].

For the gated Hall-bar inspected, the Cl concentration in the ZnSe/ZnMgSe HS determined by SIMS is depicted in Fig. 6.2 a). Quite similar doping profiles were achieved for a set of several ZnSe/ZnMgSe HS with a ZnSe QW (Apx. A.20) and are expected as well for the reference HS without QW. Prior to electrical measurements, samples are tested for connectivity. Applying a source drain voltage V_{SD} of ±1 V, a IV profile is obtained, see Fig. 6.2 b). The device resistances are typically in the order of MΩ at $V_{\mathrm{TG}} = 0\,\mathrm{V}$ and RT, governed by the sheet resistance, consistent with van der Pauw Hall resistivity measurements. Next, the transconductance is probed as a function of the top-gate voltage V_{TG}. Here, we use a specific measurement protocol adjusted to the electrical behaviour of our devices (Fig. 6.2 c). This is required to reach equilibrium, since devices exhibit a large gate hysteresis present on a time scale of multiple hours. In total, we characterise devices on seven different ZnSe/ZnMgSe HS, three without and four with a QW. The following section discusses the measurement results of a representative device of the latter type at RT and T=4 K.

6.2. ELECTRICAL CHARACTERIZATION OF GATED HALL-BARS

Here we show the electrical properties of a typical FET device fabricated on a ZnMgSe/ZnSe heterostructure. The upper barrier is intentionally doped, all other layers are not. The doping profile (SIMS) of the device is depicted in Apx. A.20 (green trace).

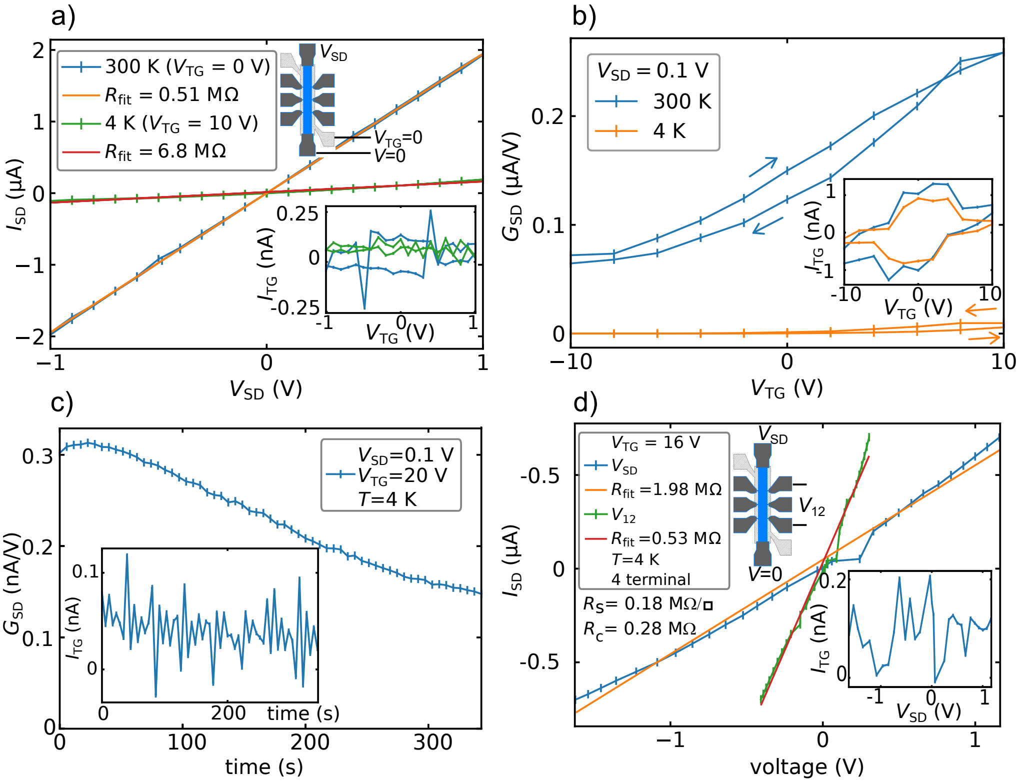

Figure 6.3: Characterization of the field effect for gated a Hall-bar on a HS with undoped QW. Electrical transport measurements are conducted at RT and 4 K in a, b, c) two terminal and d) four-terminal configuration, see device sketch for corresponding terminal configuration. a) *IV* characteristics of device resistance for a fixed top-gate voltage of V_{TG}=0 V at RT and V_{TG}=20 V at 4 K. Linear least-square fits to the data points are depicted in orange and red. b) Source drain conductance versus top-gate voltage at RT/4 K for fixed V_{SD}=0.1 V. Arrows indicate the sweep direction. c) Decay of the source drain conductance G_{SD} observed over a time span of 5 min at 4 K after rapidly ramping up V_{TG} from −10 V to 20 V. d) Transport measurement (4 terminals) through a ZnSe/ZnMgSe gated Hall-bar. *IV* characteristics and linear fits using two different pairs of ports to separate contact resistance R_c from sheet resistance R_s at V_{TG} = 16 V and 4 K. Inserts in all panels depict leakage current orders of magnitude lower than source to drain current. Benjamin Zenz conducted the measurement. Figure adopted from [148].

Connectivity to the semiconductor is achieved by *in-situ* fabrication of Al contacts to ZnMgSe:Cl (cf. Chap. 3). A typical linear IV characteristic is depicted in Fig. 6.3 a) for both room temperature and at T=4 K. Observation of a linear IV dependence at 4 K indicates the carrier concentration in ZnMgSe below the contacts is beyond the critical density of the MIT (Sect. 3.5), in good agreement with SIMS and van der Pauw Hall mobility measurements, which show no freeze out of the carrier concentration at T=30 K (Apx. A.5). For the given top-gate configuration, charge carriers are accumulated below the surface of the semiconductor in the top of the upper (Zn,Mg)Se layer. The total device resistance in this configuration is obtained from linear fits for low voltages V_{SD} to be 0.51 MΩ at RT (6.8 MΩ at 4 K). At RT, the contact resistance is in the order of 10 kΩ and the sheet resistance is 60 kΩ/□ measured in an independently conducted van der Pauw Hall measurement on a sample without top-gate.

The charge carrier concentration in the device, that enters G_{SD}, can be controlled using the field effect. Corresponding transconductance measurements at RT and T=4 K are depicted in Fig. 6.3 b). The sweep direction is indicated by arrows. After one second hold time at each set point in top-gate voltage, the source drain current is measured and the resulting conductance G_{SD} is obtained. We ensure the 20 nm tick gate dielectric to be isolating in the selected operation regime for the control voltage V_{TG} with $-10\,V \leq V_{TG} \leq 10\,V$ (inserts in Fig. 6.3 b). The leakage current I_{TG} is lower than the measured source drain current. Also, I_{TG} is below the measurement resolution of 1 nA deduced from the hysteresis in the leakage current which is a consequence of capacitive coupling in the setup wiring (other measurements of a), c), d) were performed at lower frequencies). Strong hysteresis of more than 2 V is present in the device which is attributed to recharging effects. Defects either located in the gate dielectric, at the interface of dielectric and semiconductor or in the semiconductor bulk material can offset the effective filed and thus influence the conductance. A more detailed analysis of the electrical properties of the device is conducted at 4 K:

The stability of the accumulation current is shown in Fig. 6.3 c) at T=4 K. As a function of time, the current drops toward zero current on a minute scale. The conductance saturates at a finite value of 0.2 nA/V after one hour, determined from a separate measurement (data not shown). By charging of defect states the top-gate voltage is effectively screened, resulting in a reduction of the accumulation current to zero. Prior to this non-equilibrium measurement, an initialization of the device was performed by setting the top-gate voltage V_{TG} to −20 V for 30 min and than ramping to 20 V. In this experiment, the leakage current is again independent from the source drain current as it is negligible in amplitude (100 fold smaller), see inset of Fig. 6.3 c). Finally, the contact resistance versus the sheet resistance is resolved in a similar non-equilibrium measurement (Fig. 6.3 d) using a similar initialization protocol (ramping V_{TG} from −20 V to 16 V). The sheet resistance can be obtained in a 4 terminal measurement, see insert of Fig. 6.3 d). By extrapolating the sheet resistance to the full mesa channel, taking the device geometry into account, one obtains a contact resistance R_c=0.28 MΩ and a sheet resistance R_s =0.18 MΩ/□ for this configuration.

6.3. CONCLUSION AND DISCUSSION

Optimizing the ZnSe/ZnMgSe HS profile offers further improvement on the electronic characteristics of the QW. The Hall-bar discussed is conductive at RT, while at 4 K, a large top-gate voltage of V_{TG} = 10 V is required for charge accumulation (Fig. 6.3 a). From the transconductance measurements alone, it remains unclear, whether the main conducting channel is the ZnSe QW or the ZnMgSe barrier. The linearly fitted device resistance includes the contact resistance. Fig. 6.3 b) shows transfer characteristics of the device, obviously demonstrating control of the conductance despite some hysteresis effect that is pronounced at RT and vanishing at 4 K. Remarkably, at low temperature (4 K) the control is reduced. At a fixed positive top-gate voltage, the accumulated charge carriers decrease on a time-scale of minutes (Fig. 6.3 c). The drop of conductance on a minute time-scale indicates screening of the top-gate induced electric field, presumably due to slow charging of shallow defects between the gate and QW. Screening of the top-gate voltage has also been observed in devices with similar doping profile in the upper barrier, but with a doped ZnSe QW (Sect. 5.7, Apx. A.19). At 4 K, the conductance is stable in time and significantly higher with the main conducting channel located in the ZnSe QW, independent on V_{TG} as a result of screening. We conclude, if not originating from the oxide or adjacent interfaces, the relevant defects could be Cl incorporated at interstitial or cation sites, which form more likely as the solubility limit of Cl in ZnMgSe is approached. Alternatively, O could be the origin of these defects, that can act as acceptor [157, 189]. These defects might also play a role for the hysteresis found at 300 K, but only lead to full screening at 4 K. We believe that Cl is more likely to cause the defects than O, as Cl is deliberately incorporated into the HS and is therefore expected to be much more abundant than O. In some samples, O was above the detection limit of the SIMS measurement, but could not be quantified.

We observed the screening of V_{TG} for all heterostructures probed with nominally undoped QW, but varying doping profiles (cf. SIMS data in Apx. A.20), however, the choice of profiles is limited by the requirement of a highly conductive channel between metal contact and QW in the regions below the Ohmic contacts. For the specific sample presented in Fig. 6.3, we measured a contact resistance of ~ 300 kΩ and a sheet resistance of 180 kΩ/□ at a fairly high top-gate voltage of 16 V (Fig. 6.3 d). At room temperature, the contact resistance is ~ 10 kΩ and the sheet resistance 60 kΩ/□, which is reasonable compared to the resistance of doped bulk ZnMgSe samples. The contact resistance of 300 kΩ observed at 4 K is already high and does not allow further reduction of the doping concentration in the contact region.

Closing remarks, we investigated electron transport in a set of gated Hall-bars fabricated on a ZnSe/ZnMgSe HS containing an undoped ZnSe QW at RT and 4 K. Overall, we experience a low degree of electrical control via a global top-gate, observed as large hysteresis and a time-dependent current changes, attributed to defects screening the top-gate voltage. Ultimately, the desired charge carrier control by the field effect in an undoped ZnSe QW can not be demonstrated.

We assume the presence of charge defects to affect electron scattering combined with screening of the control voltage by rechargeable defects in the characterised device. In our case, we rely on doping in the upper ZnMgSe barrier to address the problem of contacting, thereby introducing defects and charges. Lacking local Ohmic contacts, electrical control of FETs on undoped ZnSe/ZnMgSe HS is not possible in a reproducible way at 4 K. These findings motivate the fabrication of local ohmic contacts utilizing a shadow mask, presented in Chap. 7. It allows the doping profile and layer stack in the contact region to be optimised independently of the conductive channel.

CONTRIBUTIONS

Samples were grown by Alexander Pawlis and Nils von den Driesch. Johanna Janßen conducted van der Pauw Hall mobiliy measurements. Benjamin Zenz electrically characterised the samples at RT and 4 K. Uwe Breuer characterised the samples by SIMS. Lars Schreiber and Benjamin Zenz and I developed the measurement protocol for assessment of hysteresis and time stability of FET devices. Lars Schreiber supervised the experiments.

7

SHADOW WALL EPITAXY OF II-VI SEMICONDUCTORS TOWARDS ALL IN-SITU FABRICATION OF QUANTUM DEVICES

The previous chapters revealed limitations of device performance related to Ohmic contact formation. In this chapter we outline, how shadow wall epitaxy could promote the II-VI material platform to unlock all-*in-situ* fabricated quantum devices.[1] The first section outlines the key aspects of selective epitaxy in presence of a shadow wall deduced from non-electrical characterization methods. We report on selective growth of II-VI heterostructures with a high degree of process control without compromising material quality. The few µm large footprint of the shadow walls, depending on the patterning process and intended growth process, is comparable to a unit cell of a qubit processor and thus potentially compatible with a scalable qubit archi-

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[1] Alex Pawlis initiated the development of shadow wall lithography for the definition of Ohmic contacts. Alexander Pawlis, Nils von den Driesch, Yurii Kutovyi and I developed the shadow wall lithography (Sect. 7.1), with technical support by Benjamin Bennemann. An essential prerequisite, process development for shadow wall definition, was conducted by Yurii Kutovyi under supervision of Alexander Pawlis. I contributed to this development by taking minor parts of fabrication (wet etching) and post growth analysis acknowledging technical support from Elmar Neumann (SEM/FIB) and Anja Zass (AFM). As a result of my post growth analysis (element analysis/identification, shadow boundaries/angles) I suggested a conceptual change of the process design which could be implemented successfully (Sect. 7.2). The results from this development are summarized in a manuscript written by Nils von den Driesch [9]. The focus in Sect. 7.2 is on electrical characterization of the shadow wall contacts, which I supervised. I designed the device layout, Yurii Kutovyi fabricated the samples. Electrical characterization at RT was performed by me and Yurii Kutovyi and at 4 K by me. Data analysis based on the methods described in Chap. 3 was done by me for the first devices and continued by Yurii Kutovyi. All other contributions from collaborators to the scientific work are specified at the end of this chapter.

tecture. The content of this part (Sect. 7.1) is based on a preprint publication that is in review at the time of writing [9].

Second, I outline in Sect. 7.2, how to utilise shadow mask lithography in the II-VI material system for realization of selective growth of doped areas. These doped areas are required to form Ohmic contacts to an otherwise undoped ZnSe/ZnMgSe quantum well. The proposed process is optimised to yield low resistivity contacts operating at low temperature ($T \leq 4\,\mathrm{K}$). We report a low contact resistivity at RT and 4 K of about $1 \times 10^{-4}\,\Omega\,\mathrm{cm}^2$ opening the way to realise defect free II-VI quantum devices taking advantage of all-*in-situ* fabrication.

7.1. SELECTIVE EPITAXIAL GROWTH OF GROUP II-VI SEMICONDUCTORS UTILIZING A SHADOW WALL

In this work, low resistivity local Ohmic contacts to bulk ZnSe were realised by *in-situ* fabrication (Sect. 3.4.2) [5]. Among others, our result motivates investigation of quantum devices taking advantage of all-insitu processing [5, 117]. Examples are self assembled quantum dots or hybrid nanostructures fabricated by shadow wall epitaxy [117, 190–192]. Since the latter process is highly versatile it used in this work, where local Ohmic contacts to a ZnSe heterostructure are required. In (Sect. 7.1.1) and (Sect. 7.1.2) we present and validate the basic fabrication process of shadow wall epitaxy in the II/VI material system, respectively [9].

7.1.1. METHODS FOR DEVICE STRUCTURING AND SELECTIVE EPITAXIAL GROWTH

We fabricate shadow walls following the process schematically depicted in Fig. 7.1. Target height of the shadow walls is 5–7 µm aiming at a shadow length of a few microns available for contact definition. On pristine GaAs wafers a silicon dioxide (SiOx) layer is deposited by plasma-enhanced chemical vapor deposition (Fig. 7.1 a). Wall structures defined by optical lithography and metal lift-off with 300 nm thick Pt (Fig. 7.1 b) are then etched in two steps. First, SiOx is etched in a SF6/Ar and subsequently CHF3/Ar based RIE process, utilizing the Pt structures as hard mask (Fig. 7.1 c). A thin layer of SiOx remains on the GaAs substrate to protect the it from ion damage. Second, the GaAs substrate is exposed in a highly selective wet etch utilizing HF (Fig. 7.1 d). This last etch steps also reduces the wall width which can be compensated for in the mask design. All process details can be looked up in the appendix (runsheet, Fig. A.23).

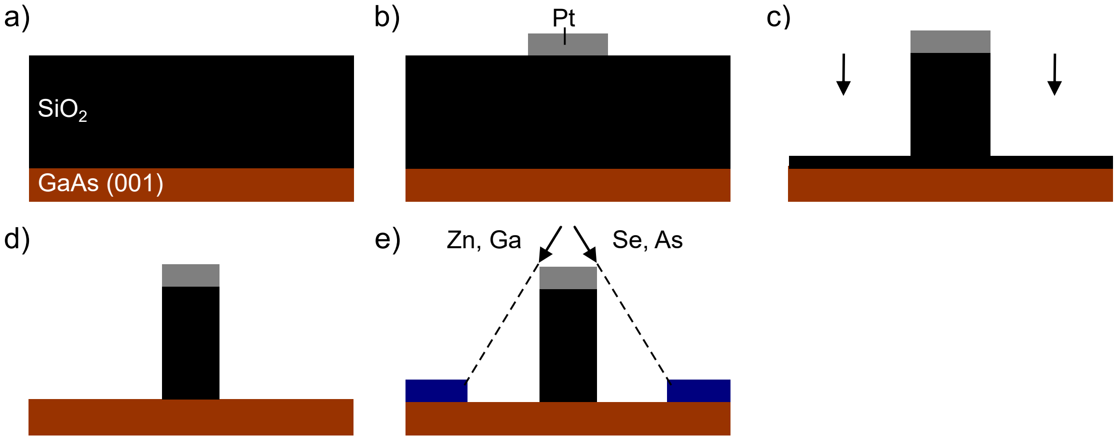

Figure 7.1: Schematic representation of the fabrication process for shadow walls. a) Deposition of the shadow wall material (SiOx) and its hard mask (Pt). Structuring of b) the hard mask and c), d) the SiOx wall in two steps. e) Selective epitaxial growth utilizing the shadow wall. Process development by Yurii Kutovyi.

Walls fabricated following the routine described above are ready for shadow wall epitaxy (Fig. 7.1 e). During the MBE growth, the walls cast a shadow with respect to each material source. Shadow regions and boundaries strongly depend on the wall design and the cell geometry of the MBE system. Maximal shadowing effects are expected when material fluxes are aligned perpendicular to the shadow walls. For our MBE system, effusion cells of group II(III) and group VI(V) material are opposite in the azimuth angle while all polar cell angles are fixed at ca. 30°. Details of the cells geometry utilised for shadow mask epitaxy are depicted in Fig. A.24. The shadow wall epitaxy process introduced is experimentally evaluated in the following section.

7.1.2. DEMONSTRATION OF SELECTIVE EPITAXIAL GROWTH

A growth experiment is carried out on two sample with pre-structured shadow walls, followed by SEM and AFM analysis. The shadow walls are fabricated as described above. On the first sample, a thin GaAs buffer (Fig.7.2 a) is grown, a common method prior to II-VI epitaxy. No layer growth is observed in the shadow regions highlighted by colour in blue and orange for the As and Ga shadow, respectively (inset in Fig.7.2 a, SEM image taken after partial wall removal by HF). In the absence of an elemental component, the growth rate is effectively suppressed [9, 191]. Droplets of presumably Ga are observed near the shadow wall in the As shadow. There, absence of As increases desorption of Ga from the substrate leading to droplet formation, which is not observed outside the As shadow [9].

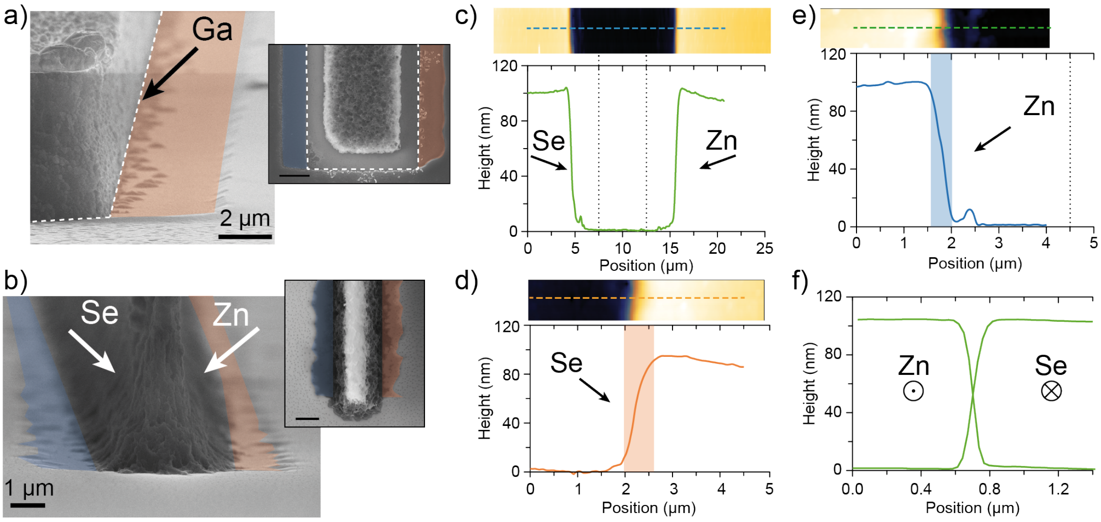

Figure 7.2: Demonstration of selective epitaxial growth. a) (b) SEM image (85° tilt) of an MBE grown GaAs buffer (ZnSe layer) with suppressed growth in shadow areas highlighted in colour. The footprint of the wall is highlighted by a white dashed line. Insets provide a top view. AFM profile of c) both layer edges for a wall parallel to the source fluxes, for d) the Se shadow edge and e) the Zn shadow edge. Insets depict a 2D overview scan from which the profiles are extracted. f) AFM profiles for both layer edges grown with fluxes aligned with the shadow wall. Arrows indicate the flux direction for each element. Figure by Nils von den Driesch.

On another prestructured sample, a single ZnSe layer with a nominal thickness of 100 nm is grown (Fig.7.2 b). Similar to GaAs growth, we observe two shadow regions related to Zn and As shadows, respectively. In direct comparison to GaAs, the shadow boundaries are rougher, attributed to a missing Pt hard mask of the shadow walls on this particular sample. We evaluate the selective epitaxial growth by AFM analysis of the ZnSe layer, focusing on profiles at the shadow boundaries for different directions. For technical reasons, the shadow walls were removed by HF before the

AFM measurement. For material fluxes perpendicular to the shadow wall, assigned as "shadow alignment" (ShA), the full profile is shown in Fig. 7.2 c) [9]. The total step height between shaded and exposed regions is consistent with the target layer thickness. Also the distance between wall and shadow edge is in agreement with the geometric shadow expected for our wall-cell configuration. We characterise the Zn and Se shadow edges in more detail (Fig. 7.2 d, e) by analyzing the step width. The step width of the shadow edge is about 0.5 µm for Zn and Se. This value is larger than typical feature sizes of less than 100 nm limited by diffusion [9, 191]. We argue that the width of the shadow edge can be explained by the geometry of the chamber, the cell and the height of the shadow wall, which gradually increases due to parasitic growth [9]. A thorough analysis of the Se shadow edge step shows a slight overshoot, attributed to reflection of Zn at the shadow wall that locally increases the growth rate under Se-rich conditions [9].

Similarly, we investigate the growth configuration where fluxes are aligned parallel to the wall, assigned as "non-shadow alignment" (NShA) [9]. Compared to ShA (Fig. 7.2 c), NShA (Fig. 7.2 f) produces sharper edges which are symmetric with respect to the flux directions. The steeper edge could be due to the anisotropy of side facet formation [9]. Consistent with the argument from above, we observe no local variations of the growth rate, since wall reflections do not occur in NShA. Overall our growth experiment yields shadow regions with full growth suppression for ShA and undisturbed epitaxial growth distant from walls, serving as a proof of concept for shadow wall epitaxy on the ZnSe platform.

The quality of similar layers growth by shadow wall epitaxy is assessed by XRD and PL analysis [9]. Two similarly grown ZnSe layers are investigated and a ZnSe/ZnMgSe HS with a locally shaded QW demonstrating the versatility of shadow wall epitaxy [9]. It is concluded that the prestructuring of the shadow walls does not compromise the quality of epitaxial growth [9]. PL analysis at 10 K of the ZnSe/ZnMgSe HS shows exciton emission from the QW as expected and confirms quantum well confinement [9]. In shadow regions, where no QW is grown, the composition of ZnMgSe determined by PL is in agreement with XRD results [9]. Our results motivate utilization of shadow wall epitaxy for all-in-situ fabrication of local Ohmic contacts.

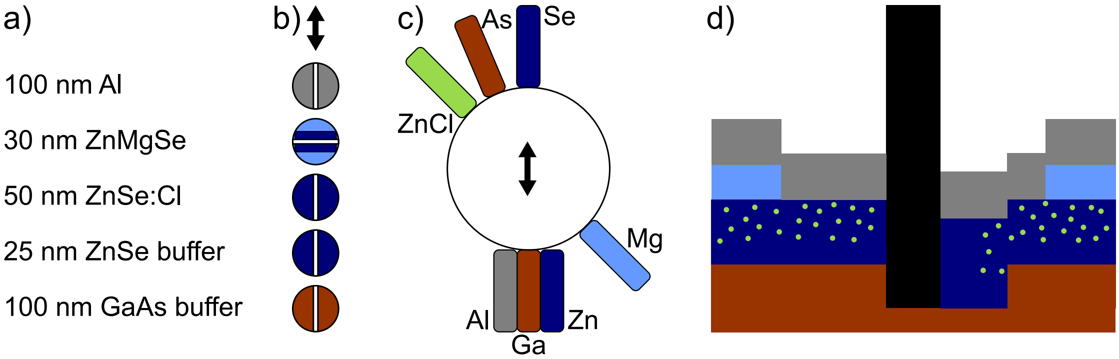

Figure 7.3: MBE growth process for electrical contacts by selective shadow wall epitaxy. a) Layer sequence from bottom to top for MBE growth and b) indicated flux orientation (arrow) relative to shadow walls (white lines). c) Cell orientation of MBE system and metallization chamber. d) Sample profile in vicinity of a shadow wall (black).

7.2. LOW RESISTIVITY OHMIC CONTACTS BY ALL IN-SITU FABRICATION UTILIZING SHADOW WALL EPITAXY

The results presented in the above section prove that shadow wall epitaxy is capable of selective epitaxial growth taking advantage of *in-situ* fabrication. In a previous chapter (Chap. 3/Sect. 3.4) I demonstrated the superior performance of Ohmic contacts due to oxide-free fabrication including metallization performed entirely *in-situ*. Now, aiming at local low resistivity contacts as desired for the operation of spin qubits, we are transferring the *in-situ* contact formation process to shadow wall epitaxy.

7.2.1. METHODS FOR IN-SITU GROWN OHMIC CONTACTS BASED ON SHADOW WALL EPITAXY

Aware of the concepts of selective epitaxial growth, we now extend our process for definition of local Ohmic contacts. Focusing on the fabrication of local Ohmic contacts, a simplified heterostructure lacking a lower barrier but featuring a doped ZnSe channel, fife-fold thicker than the ZnSe QW of final qubit device, is investigated. Here, free carriers are introduced to the conducting channel by epitaxial doping, in contrast to accumulation in the case of the final device. By choice Ohmic contacts shall form locally at the left side of shadow walls. The available degrees of freedom, namely layer sequence, material composition and flux orientation, are controlled by MBE, while shape, dimensions and positioning of shadow walls is controlled by mask design and the fabrication process.

Fig. 7.3 a), b) and c) display such a possible process in terms of layer sequence, flux orientation and cell geometry of the MBE system, respectively. For shadow wall epi-

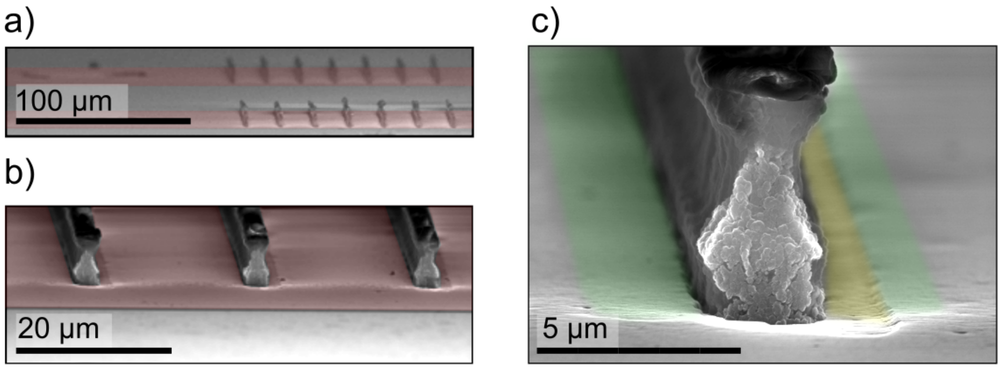

Figure 7.4: SEM micrographs of contacts defined by shadow wall epitaxy. a) Two electric terminals (red) of a TLM structure contain a set of parallel contact lines each. Contacts form at the left side of shadow-walls (dark). b) Individual terminals are structured by wetchemical post-processing of the Al surface layer (red). c) Profile of a single shadow wall. Shaded areas indicate the shadow regions for II-VI (green) and III-V materials (yellow). Micrographs are taken under 85° tilt by Yurii Kutovyi.

taxy we use pre-structured GaAs samples that were fabricated as described in Apx. A.23. The heterostructure consists of a GaAs and a ZnSe buffer, then a 50 nm thick and highly doped ZnSe:Cl layer capped by nominally undoped ZnMgSe and AlO_x, see Fig. 7.3 a). The GaAs and ZnSe layers are grown in NShA. The dielectric materials are grown in ShA exposing the underlying conducting channel only in the shadow region. Contacts are formed at the left side of shadow walls by choice of NShA for Al metallization. The target sample profile is depicted in Fig. 7.3 d).

The implemented design of shadow masks and contacts targets low contact resistance by maximizing contact area: While the contact width of a few microns is fixed by dimensions of the wall height and the MBE system, the contact length is a free design parameter. We choose a wall length of 100 µm at a wall height of ~ 5 µm. In addition, multiple walls and thereby contact areas are connected in parallel for each terminal of a TLM structure. The sample discussed here will be referred to as sample E.

Prior to electrical characterization, TLM devices are structured by *ex-situ* fabrication methods without altering the *in-situ* grown contact interface. An exemplary contact terminal of a TLM structure is depicted in Fig. 7.4 a) and b). Contact and device dimensions are comparable, but different compared to the TLM structures presented in Chap. 3. Still, the physical quantities specific contact resistivity ρ_c and sheet resistance R_s experimentally determined from TLM characterization are independent on lateral device dimensions.

The height profile of contacts fabricated by shadow mask lithography (Fig. 7.3 d) is rich in structure for two reasons: Firstly, the cell orientation in the equatorial plane defines the shadow length. In our case, a shadow length of 2.9 µm is obtained for ZnSe in perfect ShA associated to a step profile at the shadow boundary. However, the cell angles are not perfectly aligned in anti-parallel orientation in the equatorial plane for Mg vs Se (Ga versus As). The in plane angular deviation $\Delta\phi$ with respect to the other compound is 25° and 45° for As and Mg, respectively, see Fig. 7.3 c). This leads to different shadow configurations specific for group II-VI or III-V material with characteristic profile steps evident in SEM, see shaded regions in Fig. 7.4 c). Similarly, the Cl shadow length in the contact region to the left side of shadow walls is reduced as a fact of non-ideal NShA, which is subject to ongoing optimization of cell alignment. In the initial configuration ($\phi = 45°$) Cl dopants are introduced with an finite offset of 2.0 µm from the shadow wall, resulting in a ca. 1 µm wide contact area. Second, the azimuth cell angle for AlO_x deposition is comparatively flatter, correspondingly leading to an increased shadow length. Nonetheless, for the given cell geometry, a well-defined active contact area can be realised on the left side of the wall by proper sample rotation. The right side is assumed to be isolating after passivation in NShA. However, on the right side of the wall, side contacts to the ZnSe:Cl channel with a comparatively small contact area[2] can not be excluded based on current knowledge, but are expected to negligibly contribute to ρ_c.

For the proposed shadow mask technique and fabricated devices we expect an *in-situ* fabricated contact interface of low resistivity at the left side of shadow walls. In the following, we will discuss results from electrical characterization of such contact structures.

7.2.2. CHARACTERIZATION RESULTS OF LOCAL OHMIC CONTACTS GROWN IN-SITU BY SHADOW WALL EPITAXY

With the shadow wall epitaxy described above we fabricate local Ohmic contacts on a II-VI heterostructure. The heterostructure hosts a conducting ZnSe:Cl channel capped by undoped ZnMgSe which is expected to be not occupied by electrons. The sample is passivated by an oxide layer. Measurement data and analysis results from electrical characterization of TLM structures are presented in Fig. 7.5 and Tab. 7.1, respectively.

As expected for an *in-situ* fabricated Al contact on degenerately doped ZnSe:Cl (Chap. 3), IV characteristics are linear at both RT and 4 K, see Fig. 7.5 a). Also at tenfold increased resolution (data not shown) no deviations from linearity are detected.[3] Using the TLM and analysis methods described in Sec. 3.2.1, we quantitatively determine the contact resistance R_c, the specific contact resistivity ρ_c and sheet resistance R_s. For devices with mesa etched channel from the data shown in Fig. 7.5 b), we find low contact resistances of $0.40 \pm 0.05\,\mathrm{k\Omega}$ ($0.50 \pm 0.05\,\mathrm{k\Omega}$) at a sheet resistance of $3.1 \pm 0.3\,\mathrm{k\Omega}/\square$ ($3.6 \pm 0.3\,\mathrm{k\Omega}/\square$) at RT (4 K), see Tab. 7.1. The measured sheet resistance is lower than the expected value of about $0.6\,\mathrm{k\Omega}/\square$ for degenerately doped ZnSe

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[2] In our experiments, the aspect ratio, namely vertical versus lateral dimensions, is 1:20.

[3] A small voltage offset of about 1 mV was detected for positive voltages, attributed to measurement electronics.

channel of the same thickness. As our experiment is slightly more resistive than expected, this discrepancy will be addressed in the next section. Assuming geometric extensions and a homogeneous current distribution, the upper limit derived for ρ_c of $2.0 \times 10^{-3}\,\Omega\,\mathrm{cm}^2$ at RT ($2.5 \times 10^{-3}\,\Omega\,\mathrm{cm}^2$ at 4 K) lies within the target regime defined in Chap. 2.2.2. We solidify the analysis result from TLM by independent measures of the sheet resistance with the van der Pauw Hall method (Fig. 7.5 c) and obtain 4.0 kΩ/□ (5.7 kΩ/□) at RT (25 K).

Our observations compare well to resistivities determined by TLM at RT, but deviate for 4 K.[4] Since a different region of the substrate was probed, the pronounced discrepancy at 4 K could arise from sample inhomogeneieties affecting transport properties.[5] Due to the complex geometry of the contacts errors on the contact resistivity are large, since strongly dependent on assumptions. Taking the contact area on the

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[4] For the given device geometry the van der Pauw Hall method systematically overestimates R_s by about 10–20 %, which is not corrected in the data shown.

[5] Similar contact resistances and contact resistivities are also expected when a QW heterostructure is used.

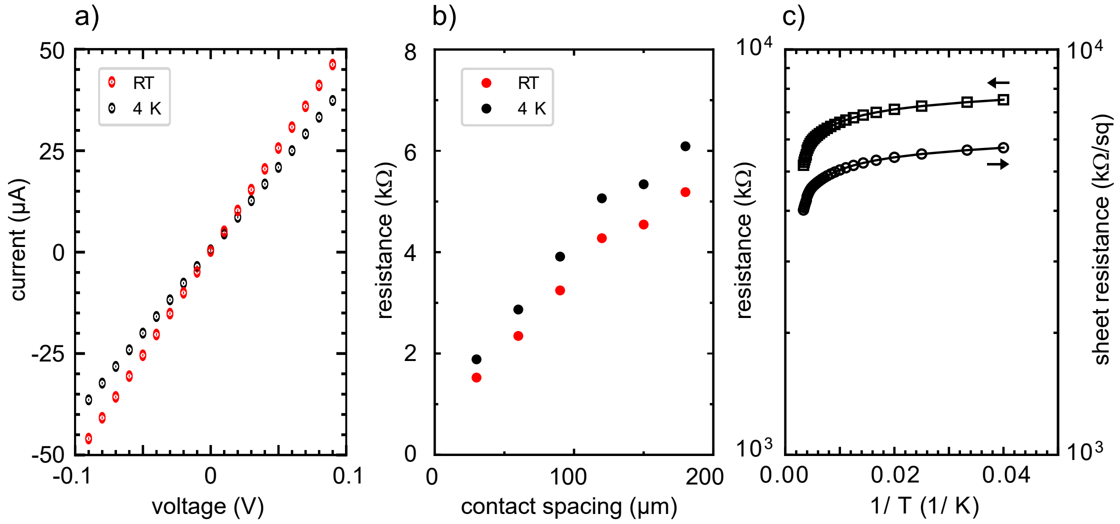

Figure 7.5: Electrical characterization of selectively grown Ohmic contact utilizing a 3D shadow mask. a, b) Electrical characterization of TLM devices on sample E with a 125 µm wide mesa channel. Measurements in 2-terminal configuration are performed in darkness at both room temperature and 4 K. For specifications of the sample and analysis results see Tab. 7.2. a) *IV* profile for a TLM device with contact spacing of 30 µm and b) resistances of a full TLM structure on the same chip. c) Arrhenius plot of resistivity measured by van der Pauw Hall (25–300 K) at a different section of the wafer/chip compared to the TLM structures. Device (sheet) resistance represented by squares (circles) is quantified on the left (right) axis. Hall measurement by Nils von den Driesch.

Table 7.1: Electrical characterization of local contacts obtained by shadow wall epitaxy probed at RT and 4 K. Analysis results for TLM devices without mesa etched channel. $R_{s,TLM}$ and $R_{s,vdP}$ denote R_s obtained by TLM or van der Pauw Hall measurements, respectively.

Sample	T (K)	R_c (kΩ)	$R_{s,TLM}$ (kΩ/□)	$R_{s,vdP}$ (kΩ/□)	ρ_c ($10^{-3}\,\Omega\,cm^2$)	L_t (µm)
E	300	0.40 ± 0.05	3.0 ± 0.3	4.0	2	19
E	4	0.50 ± 0.05	3.6 ± 0.3	5.7 (25 K)	2.5	21

left side of the walls into account, a conservative upper bound estimate on the specific contact resistivities can be given as $\rho_c = 1.5 \times 10^{-3}\,\Omega\,cm^2$ ($2.5 \times 10^{-3}\,\Omega\,cm^2$) for RT (4 K).

We note an increased bulk resistivity in this sample compared to ideal bulk samples with degenerate doping. A possible explanation is increased impurity scattering attributed to crystal defects caused during growth by SiO_2 residuals from prestructuring. A local variation in the distribution of SiO_2 residuals could also explain inhomogeneiety of resistivity observed by the electrical measurements at low temperature ($T \leq 30\,K$) for different regions of the sample. Further, the kink (Fig. 7.5 c) in the temperature dependence of the bulk resistivity at about 200 K is a well known characteristic of ZnMgSe and could indicate presence of a parallel conduction channel in the barrier of the HS that does not freeze out at 4 K (Chap. 4). To address the remaining inaccuracies, the following section examines the reproducibility of our experiment with a focus on sheet resistance.

Overall, by using shadow wall epitaxy we successfully demonstrate a local, low resistivity Ohmic contact with high temperature stability compatible with requirements of qubit operation.

7.2.3. REPRODUCIBILITY OF LOCAL OHMIC CONTACTS BASED ON SHADOW WALL EPITAXY

We investigate reproducibility of the local Ohmic contacts obtained by the shadow mask epitaxy following the process scheme suggested in Sect. 7.2.1. Repeating the fabrication process of sample E, the layer stack consists of a buried conducting channel capped by undoped ZnMgSe as isolation, see Fig. 7.3. All heterostructure properties are listed in Tab. 7.2.

The thickness of the conducting ZnSe channel is 50 nm. We choose a Cl doping of $8 \times 10^{18}\,cm^{-3}$ above the MIT to guarantee for a degenerate, temperature stable carrier concentration. Contact to ZnSe:Cl is formed by Al metallization in shadow regions not passivated by ZnMgSe or AlO_x. All other regions are not contacted due to the isolating properties of the passivation layers. The ZnMgSe layer with x_{Mg} 10 % or 20 % is nominally undoped. Undoped GaAs and ZnSe buffer layers are utilised to

Table 7.2: Contact resistivities of local contacts obtained by shadow wall epitaxy probed at RT. Contact dimensions and a homogeneous current density enter evaluation of ρ_c as specified here, yielding an upper bound estimate. ZnSe buffer, ZnSe:Cl channel and ZnMgSe barrier thicknesses are 25, 50 and 30nm respectively. Al contacts are 100 nm thick.

Sample	x_{Mg} (%)	n_{ZnMgSe} (cm^{-3})	t_{AlOx} (nm)	R_c (kΩ)	R_s (kΩ/□)	ρ_c (Ωcm^2)	L_t (µm)
D	20	-	20	0.30 ± 0.02	1.3 ± 0.3	1.3×10^{-3}	34
E	20	-	20	0.32 ± 0.02	3.0 ± 0.3	1.6×10^{-3}	15
F	10	-	20	0.78 ± 0.02	7.3 ± 0.3	3.8×10^{-3}	16
G	20	5×10^{17}	0	1.00 ± 0.05	9.2 ± 0.5	1.4×10^{-2}	16

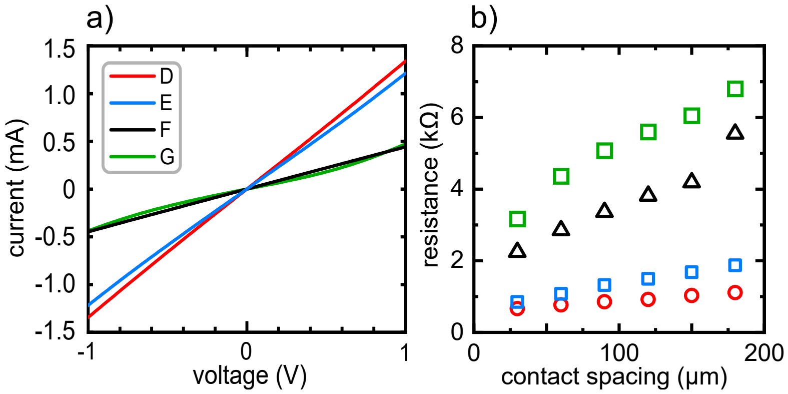

Figure 7.6: Electrical characterization results of multiple heterostructure contacted by shadow mask epitaxy. a) IV profiles of TLM devices without mesa for samples D-G. Contact spacing is 30 µm. b) TLM characteristics obtained by IV profiling at RT. The transport channel between contacts is not laterally confined by a mesa etch. The samples differ slightly in x_{Mg} in the upper barrier and choice of dielectric. Details on samples and analysis results (R_c, R_s, ρ_c and L_t) are provided in Tab. 7.2. Figure by Yurii Kutovyi.

reduce defect densities after shadow mask definition. For the chosen process parameters and contact layout a sheet resistance of about R_s =0.2–0.6 kΩ/□ and a contact resistance in the order of $R_s \cdot □ < 10$ kΩ are expected.

Results from electrical characterization at room temperature are depicted in Fig. 7.6 and related analysis results based on TLM are shown in Tab. 7.2.[6] Almost linear IV curves (Fig. 7.6 a) and monotonously increasing $R(d)$ (Fig. 7.6 b) demonstrate high

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[6] Results therein are derived from a similar data set for devices without mesa etched channel

degree of process control and reproducibility achieved in our experiments. At room temperature, we find contact and sheet resistances in the range of 0.3–1.0 kΩ and 1.3–9.2 kΩ/□, respectively. Upper estimates for ρ_c yield 1.3×10^{-3}–$1.2 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$ with the same conservative assumptions that were made in the previous section. Some differences remain between the experiments. From experimental data on highly doped bulk ZnSe one would expect ρ_s=0.6 kΩ/□ for a of 50 nm thick n-ZnSe channel, with $n = 1 \times 10^{19}\,\mathrm{cm}^{-3}$ and mobility $\mu = 150\,\mathrm{cm}^2/\mathrm{Vs}$ limited by scattering at ionised Cl impurities, see Sect. 4.2.1. Deviations occur if carriers populate the upper ZnMgSe barrier where they experience stronger scattering and overall ρ_s increases. Population of the upper barrier is more likely for lower tunnel barriers and higher doping concentrations. Our results exhibit the highest values for ρ_s, if either no passivation layer is applied or the barrier height ($\propto x_{\mathrm{Mg}}$) reduced, see sample F and G in Tab. 7.2, respectively. Precise quantification of electrical properties of the individual channels of each HS presented here requires further modeling of the band structure and gate dependent (Hall-bar) measurements. This is beyond the scope of this work, which is aimed at realization of an Ohmic contact to a QW. As mentioned earlier, transport characteristics of ZnMgSe were observed (Fig. 7.5), evidencing the relevance of parallel conducting channels at least in sample E. Nevertheless, independent of the exact transport properties of the channel(s), for the contacts upper limits for ρ_c can be estimated with some reductions in accuracy.

Given the nature of our conservative assumptions for assessment of contact resistivity (ρ_c =$2.5 \times 10^{-3}\,\Omega\,\mathrm{cm}^2$ at 4 K), one can expect a downward correction of ρ_c with improved understanding. So far there are no objections to reach the record level (ρ_c =$4 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$, 4 K) found for entirely planar samples without local contacts [5] as we could demonstrate defect free, all-*in-situ* fabrication of the contact interface (Sect. 7.1). The upper bound on ρ_c might be down-corrected to realistic values depending on the current distribution at the contact. A reasonable correction factor would lie in the range of 2–10, as motivated by finite element simulation (Sect. 3.2.2) of a single line contact (data not shown). Furthermore, the relevance of side contacts, which have been neglected so far, could affect ρ_c, but from geometrical considerations this effect is not expected to be dominant. Nevertheless, even the conservative estimate on contact resistivity ρ_c with the upper bound of $\rho_c = 2.5 \times 10^{-3}\,\Omega\mathrm{cm}^2$ at 4 K, the performance of contacts fabricated by shadow wall epitaxy already meets the requirements of qubit operation ($\rho_c \leq 1 \times 10^{-2}\,\Omega\,\mathrm{cm}^2$, Sect. 2.2).

7.3. DISCUSSION AND OUTLOOK

In summary, we have discussed selective epitaxial growth assisted by shadow walls in the context of locally contacting n-ZnSe as desired for EDQD devices. We present a fabrication process in the II-VI material system based on shadow mask technology developed over the last three decades [113, 159, 192]. Our approach makes use of shadow walls epitaxy [9]. The basic concept is to break the symmetry during epitaxy by introduction of shadow walls that selectivity of growth, desired for the definition of local contacts (Figs. 7.1, 7.3).

Specifically, we perform shadow wall epitaxy with a high degree of process control without compromising quality of the MBE grown II-VI (III-V) material, as deduced from structural and optical characterization methods [9]. For dimensions compatible with the target EDQD device, we can demonstrate the shadow effect (Fig. 7.2) and low resistivity of local Ohmic contacts (Fig. 7.5). Crystal growth is efficiently suppressed as soon as one crystal compound is shadowed. The sharpness of boundary regions is found to be limited by the MBE system or shadow mask used and not the diffusion length of atoms (Fig. 7.2). Considering the Al-ZnSe interface, we find ρ_c=$2.5\times10^{-3}\,\Omega\,\mathrm{cm}^2$ at cryogenic temperature, (Tab. A.3), meeting the basic requirements for operating an EDQD. The contact quality can be reproducibly be achieved at this level (Fig. 7.6, Tab.7.2), although reduction of analysis uncertainties is subject to future investigations. For the transition to electrically controlled devices (FET, Hallbar) and ultimately the target device (SET, EDQD), the heterostructure and charge carrier profile in the contact region has to be adapted [83].

In Sect. 5.3 a regrowth process has been presented for the fabrication of local Ohmic contacts to ZnSe substrates. Although low contact resistivities ($1\times10^{-3}\,\Omega\,\mathrm{cm}^2$) have been achieved at low temperature ($T\leq4\,\mathrm{K}$), the process could not be transferred to HS with QW due to technological challenges in structuring that are not of fundamental nature. Effectively, the technical limitations can be avoided by employing shadow mask techniques, where the structuring, crystal growth and contacting are separated in an elegant way. For a comparison of both methods, the interested reader may check Apx. A.6. With respect to Ohmic contacts with low ρ_c one could argue, regrowth processes have the potential for catching up with the optimal process we developed for bulk samples (Chap.5). Both process types rely on metallization following epitaxial growth *in-situ*, which we identify as compatible with shadow masks while maintaining crystal quality.

The high degree of processes control available for shadow wall epitaxy, not fully exploited so far, is a rich resource for further developments. For upcoming developments towards an EDQD device, implementation of an isolating dielectric is envisioned compatible with *in-situ* fabrication. A challenge will be integration of nanostructure control gates by ebeam-lithography while maintaining compatibility with shadow walls. Conceptually, suitable processes for both dielectric and control gates have been identified and tested for planar heterostructures within this work. Addressing the problem of locally contacting n-ZnSe, we utilised a process based shadow wall epitaxy. With our approach, Ohmic contacts with temperature stable, low specific contact resistivity could be successfully realised by taking advantage of all-*in-situ* processing, without using all degrees of freedom of the process. As an outlook, future developments target electrically controlled devices on undoped channels operated in accumulation mode, in contrast to contacting highly doped ZnSe:Cl layers as demonstrated here. The physics at the contact interface remain the same, independent on the generation of charge carriers by doping or accumulation.

To conclude, we identify selective epitaxy utilizing a shadow wall as a highly tunable method by which optical and electrical properties can be engineered without compromising crystal quality, which is especially important for quantum devices. Our demonstration of local contacts with low contact resistivity operating at cryogenic temperature opens the way to investigate all-*in-situ* fabricated quantum devices with full electrical control based on the technology and methods described in this work.

CONTRIBUTIONS

Samples were grown by Nils von den Driesch, assisted by Benjamin Bennemann. Jan Gruis and Jasmin Ehrler provided SiO2 deposited in the labs of Andrei Vescan at Compound Semiconductor Technology/RWTH. Christoph Krause performed deposition of the metallic cap of samples with shadow walls. Yurii Kutovyi and I developed the process design and device layout used for shadow wall lithography supervised by Alexander Pawlis. Nils von den Driesch performed van der Pauw Hall measurements. Yurii Kutovyi developed the fabrication process for shadow wall definition. Nils von den Driesch analysed the samples by structural methods. Jan Klos contributed ideas to structuring of shadow walls. Nils von den Driesch and Yurii Kutovyi conducted structural and PL analysis, respectively. Yurii Kutovyi and I performed electrical characterization of samples at RT and 4 K, respectively. Nils von den Driesch wrote the manuscript of the publication on selective epitaxial growth of II-VI semiconductors using shadow walls [9].

8

SUMMARY AND OUTLOOK

In this final chapter, I sum up the main results of all chapters and provide a brief outlook to future developments.

Chapter 1 provides you with an introduction to the field of research of semiconductor spin qubits and explain the interesting material properties of ZnSe which motivate the exploration of ZnSe for this technology. Thereafter, I outline the structure of this work.

In Chapter 2, the concept of EDQD based qubits is outlined. I introduce the concept of EDQDs in semiconductors and propose a specific layout for an ZnSe based EDQD device, aiming at exploration of the interesting electrical and optical material properties ZnSe provides (Sect. 2.1). The approach relies on bandgap engineering and electrically controlled potentials, to confine a single electron in a ZnSe/ZnMgSe HS, additionally employing control potentials mediated by nanostructure gates. In the second section, objectives affecting the performance of EDQD based spin qubits are discussed, specifically in relation to ZnSe (Sect. 2.2). Namely, operation temperature, contact resistance, charge noise, thermal budget, spin orbit coupling and mean free path are to be considered in this experimental work to identify suitable fabrication processes for such quantum structures.

In Chapter 3, I present a reproducible fabrication process for low resistivity Ohmic contacts to n-ZnSe operating at $T \leq 4\,\mathrm{K}$, the main objective of this work. Our finding is based on experimental work, testing of different experimental methods including doping by implantation, diffusion or epitaxial doping combined with metallization *ex-situ* or *in-situ*. Epitaxial doping out competes the other approaches providing both high quality crystals and high doping concentrations in a reproducible way. We report a low contact resistivity of $4 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ at $T \leq 4\,\mathrm{K}$, achieved by avoiding oxidation of the metal-semiconductor interface when performing both, epitaxial doping and metallization with Al *in-situ*. This low contact resistivity of Ohmic contacts to n-ZnSe is compatible with electrical readout of all-electrical quantum devices. However, our fabrication process is not compatible with contacting undoped quantum devices, due to technical limitations regarding local doping. This challenge is addressed using a selective regrowth process developed and validated within this work. Still, the selective regrowth process is incompatible with contacting a 10 nm thick ZnSe QW, attributed to limits of vertical etch precision. As alternative, I suggest a promising solution for local doping and local Ohmic contacts in the last chapter of my thesis (Chap. 7).

In Chapter 4, the mean free path in ZnSe/ZnMgSe HS or bulk is discussed. Recalling scattering theory, the limiting scattering processes for electrons in bulk ZnSe are identified as longitudinal phonon scattering at RT and impurity scattering at $T = 77\,\mathrm{K}$. Transport measurements in epitaxially doped bulk ZnSe:Cl are compatible with theoretical predictions at RT, but deviate at low temperature $T \rightarrow 0\,\mathrm{K}$, attributed to impurity scattering. Furthermore, we discuss electron transport in ZnMgSe for $x_{\mathrm{Mg}} \sim 17\,\%$ and attribute increased scattering to the presence of neutral impurity scattering at Mg atoms. For the operation of all-electrical quantum devices local ohmic contacts are a prerequisite and require degenerate doping in the contact region. We theoretically and experimentally investigate the critical density of the MIT in ZnSe and ZnMgSe. Our data is in good agreement with theory (Mott criterion) when accounting for the Bohr radius of donor bound electrons in ZnSe. However, for the ternary system ZnMgSe there is only sparse data available for electron transport and formulation of an accurate theory is beyond the scope of this work. In the last part of this chapter, electron transport in ZnSe/ZnMgSe HS with a ZnSe QW is discussed for $T = 300$–$25\,\mathrm{K}$. We find a dependence on electron scattering with the concentration of charged impurities, intentionally introduced by Cl doping. However, for undoped QWs, the mean free path of electrons is reduced by effects subject to future investigations utilizing devices with electrical control (FETs).

In Chapter 5, the methods and results of the fabrication process are discussed. In collaboration with the partners at FZJ, the entire fabrication can performed in-house, covering both MBE-growth of ZnSe/ZnMgSe HS and structuring of devices. Device fabrication is monitored all along the fabrication process using electrical methods supplemented with optical and structural methods. We introduce fabrication processes for gated Hall-bars and devices with EDQD architecture. All basic fabrication steps, structuring by dry or wet etching, optical or e-beam lithography, deposition of gate dielectric, and metallization are described and benchmarked. Addressing fabrication of low resistivity Ohmic contacts to n-ZnSe operating at $T \leq 4\,\mathrm{K}$, we present and evaluate implantation, diffusion, and *ex-situ* or *in-situ* fabrication, where best contact performance is found for *in-situ* fabricated Al contacts. Efforts in adapting this approach for realization of local ohmic contacts were successful when contacting bulk ZnSe, but not suited to contact a 10 nm thick ZnSe QW limited by etch precision. Closing remarks, our fabrication processes are adopted to allow for high device quality with low defect concentration, achieved by down-correction of the thermal budged for post-growth fabrication and the transition towards all-*in-situ* fabrication.

In Chapter 6, the final FET device, a gated Hall-bar fabricated on a ZnSe/ZnMgSe HS with a nominally undoped ZnSe QW, is electrically characterised. The source-drain conductance and leakage current is measured at RT and 4 K, demonstrating basic device functionality. However, the electrical control of the device was found to be poor, as the signal in accumulation mode decays over time, superimposed by a hysteresis effect in the control voltage. As explanation to both effects we motivate the presence of rechargeable defects located between the ZnSe QW and the gate, which effectively screen the control voltage. Most likely the defects originate from Cl, intentionally incorporated in the devices by planar doping to achieve ohmic contacts. For upcoming research, an alternative contact method based on selective epitaxial doping using a shadow mask is proposed.

In Chapter 7, I present a fabrication technique developed to solve the problem of local Ohmic contacts, which continues on the previously identified *in-situ* method (Chap. 3) [9]. Our approach, selective shadow mask epitaxy, is firstly applied for fabrication of Ohmic contacts in II-VI material, although shadow mask epitaxy is a well known concept in nanofabrication. In specific, we address the challenge of local doping identified as requirement in fabrication of Ohmic contacts (Chap. 3) and device performance of gated Hall-bars (Chap. 6). Our approach utilises full *in-situ* fabrication of prestructured substrates allowing for III-V/II-VI growth and contacting of a ZnSe QW in a ZnSe/ZnMgSe HS. In the first part of the chapter, the selective epitaxy is characterised in terms of material quality and selectivity. For our method, pre-structuring of shadow walls does not compromise crystal quality. In the second part, a highly specific solution is demonstrated for local Ohmic contacts to a II-VI HS and concluded with a proof of concept experiment: We have achieved a low resistivity local Ohmic contact with $\rho_c \sim 2.5 \times 10^{-3}\,\Omega\,\mathrm{cm}^2$ at a total contact resistance below $1\,\mathrm{k\Omega}$ at 4 K. The contact resistivity reported is not far off the best results obtained for bulk ZnSe (Tab. A.3) and has the potential for catching up, since the contact is fabricated *in-situ*. With the fulfilment of the requirements on contact resistivity defined in this thesis, we mark an important milestone, enabling investigation of all-electrical quantum devices in the II-VI material system.

A

APPENDIX

A.1. DEVICE IDEA

Table A.1: Parameters of the 1D Poisson-Schrödinger simulation for a ZnSe/ZnMgSe HS.

property	unit	experiment	simulation
CB offset			
E_d (ZnSe)	(meV)	$\leq$27 [138]	30 [118]
E_{gap} (MgSe)	(eV)	4.0 [131]	4.1 [121]
E_{gap} (ZnSe)	(eV)		2.82 [121]
CB offset ZnSe/ZnMgSe	(%)		70
CB offset ZnSe/ZnMgSe	(meV)		170
CB offset ZnSe/GaAs	(meV)		500
x_{Mg}	(%)	17	17
FLP	(eV)		0
CB offset QW	(meV)		~ 200
strain			
c_{11} (ZnSe)	(GPa)		82.6 [121]
c_{12} (ZnSe)	(GPa)		49.8 [121]
c_{11} (MgSe)	(GPa)		63.1 [121]
c_{12} (MgSe)	(GPa)		61.8 [121]
background doping			
n_{ZnSe} (Hall)	(cm^{-3})	1.5×10^{16}	1×10^{16}
n_{ZnMgSe} (Hall)	(cm^{-3})	2.7×10^{16}	2×10^{16}
ϵ_r (ZnSe)			8.6
ϵ_r (GaAs)			12.9
m_{eff} (ZnSe)	(m_e)		0.147 [121]
m_{eff} (MgSe)	(m_e)	0.23 [121]	0.19
m_{eff} (GaAs)	(m_e)		0.063

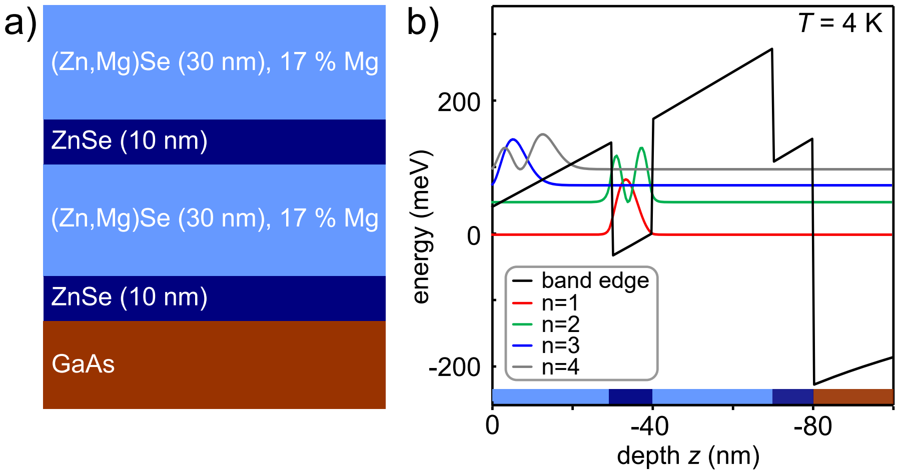

Figure A.1: Simulation of the conduction band edge of a ZnSe/ZnMgSe HS. a) Band structure for the undoped target heterostructure with an 10 nm thick ZnSe QW embedded in two 30 nm thick ZnMgSe barriers with a Mg content of 17 %. This system is separated by a 10 nm thick ZnSe buffer from the GaAs substrate. b) Simulated probability distribution of the electron wave function (1D Poisson-Schrödinger solver, FZJ) versus z measured from the surface of the HS (z axis color coded corresponding to panel a) for $T = 4\,\mathrm{K}$. With the groundstate defined as the lowest state in the II-VI HS, the first four states are depicted (n=1-4). All boundary conditions and parameters entering the simulation (CB/VB offset, assumptions on strain) are listed in Tab. A.1. This figure is complementary to Fig. 2.1, but additionally shows states n=3,4.

A.2. SETUPS FOR ELECTRICAL CHARACTERIZATION

Among a broad variety of characterization tools along the fabrication process the ultimate benchmark is taken under experimental conditions as close as possible to qubit operation. My focus is on electrical characterization of prototype devices mainly at $T = 4\,\mathrm{K}$, outlining the most relevant tools and methods that were used: The direct current (DC) needle Probe station (Section A.2), the Hall-setup (Section A.2), the 4K setup (Section A.2). Given the importance of LT transport data a coherent description of van der Pauw theory in alignment with experimental measurement methods including error analysis is provided in Appendix A.2.

DC NEEDLE PROBE STATION

Ohmic contact quality, sample resistivity and if applicable gate isolation or leakage at room temperature can be easily accessed in electrical measurements with a needle probe station. Mostly the silver devil at IHT [1] was used, the name reflects the shiny aluminum cover box shielding electrical signals and light. Samples are contacted using metallic (wolfram) needles manually controllable by xyz-stages and measured with a keithley semiconductor analyser[2]. Light shielding is especially important for high resistivity samples as optically excited electron-hole pairs get separated and can decrease the observed resistance. Typically two terminal measurements were performed if not resistivities were such low that the needle contact resistance was not negligible. In those cases four terminal method insensitive to the wiring resistance of the setup and needle contacts was used.

The DC current resolution limit is in the 10 pA regime for the low current SMU and the according filters applied. The setup is vibration damped to allow such low resistance measurements in DC mode with non soldered contacts. Two types of devices were characterised with this setup: Resistivity measurements on TLM structures and gated or ungated Hall-bar structures. To conclude, this setup is well suited for electrical precharacterization at room temperature of semiconductor devices in means of quality of ohmic contacts and gate functionality prior to cryogenic temperature experiments.

VAN DER PAUW HALL MEASUREMENT STATION WITH VARIABLE TEMPERATURE

Experimentally electron transport can be observed with the Hall effect. Moving electrons experience the Lorentz force F_L in the presence of external magnetic fields which allows to study electric transport beyond resistivity and conductance providing access to carrier densities and mobilities. Although interest is highest in electron transport at $T \leq 4\,\mathrm{K}$ a cryostat with a variable temperature sample stage is utilised for temperature dependent characterization helpful for identification of transport

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[1] DC Probe Station (Room Temperature), room number WSH 24B116, FOM-ID 43

[2] Parameter Analyser (Keithley 4200A-SCS), room number WSH 24B116, FOM-ID 11

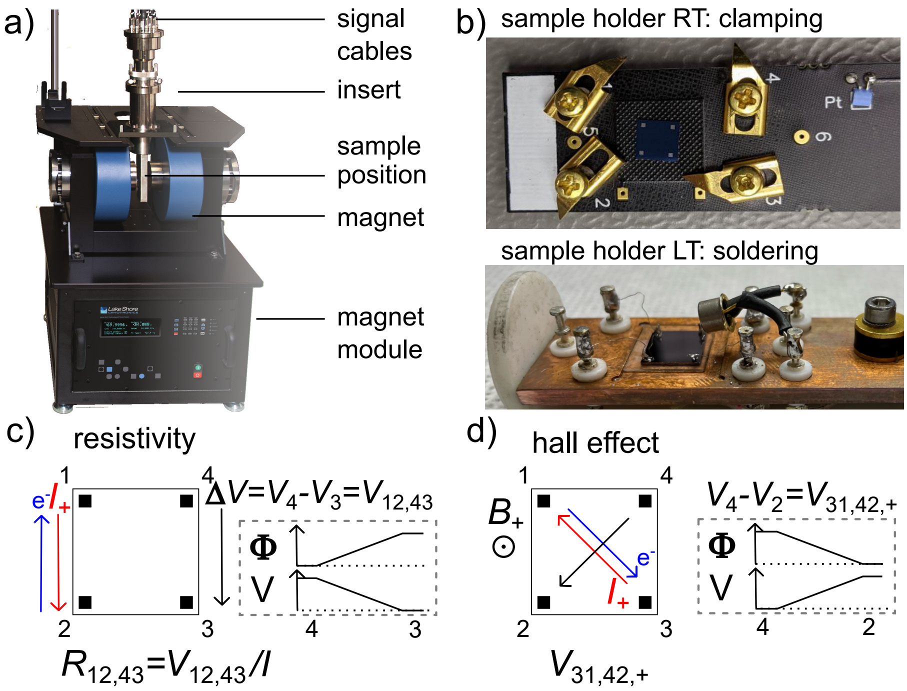

Figure A.2: Hall effect measurement setup. a) Variable temperature Hall effect measurement station with sample insert (for room temperature). b) Samples of size up to 10x10 mm² can be electrically connected by clamping or soldering to sample holders. The clamping option is intended for room temperature measurements only. All sample holders are equipped with a Pt temperature sensor. The sample holder labeled "LT" is equipped with an 365 nm LED. Specific measurement configurations using the van der Pauw Hall method for acquisition of c) resistivity and d) Hall voltage, according to the nomenclature introduced in Fig. A.3. Panel a) adopted from the manufacturer's catalog (lakeshore) [193].

mechanisms. In this section the van der Pauw Hall method is discussed in detail since it prov solid data on electron density and mobility at low temperature (T= 300–25 K).

EXPERIMENTAL SETUP

A commercially available Hall measurement station[3] supporting temperatures ranging from 300 K down to 10 K is available in the HNF at FZJ, see Fig. A.2 a). Cooldown within about one hour is enabled by a closed cycle refrigerator pumping He. Samples are soldered to a sample holder at the tip of the insert, see Fig. A.2 b). It features a sample size of 10x10 mm² and eight DC lines allowing for transport measurements in magnetic flux densities up to 1.67 T. The sample is placed in out of plane orientation in the center of the magnetic field where homogeneity is highest.

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[3] Lakeshore 8404, Hall measurement system, www.lakeshore.com/.../8400-series-hms

The configuration for four terminal measurement of resistivity or Hall voltage are depicted in Fig. A.2 c). In a resistivity measurement neighbouring contacts are selected for sourcing current and measuring voltage. For Hall voltage measurements a diagonal port configurations are chosen to maximise the signal. Details on the measurement and analysis method including current and field reversal under permutation of contacts are explained in Appendix A.2.

Resistivity can be probed in the range of 0.5×10^{-3}–$10 \times 10^{6}\,\Omega$ using a combination of a current source with pA resolution[4] and a voltage measurement unit[5]. Resistivity measurements are compatible with gating devices using a separate voltage source[6]. Beyond improving measurement accuracy by current and field reversal, averaging can be performed at the cost of measurement time. Lock-in amplification is not performed: The measurement software provides only signal modulation originating from magnetic field, but the setup can only supply DC fields. One insert is equipped with a LED of wavelength 365 nm operated at 5–6 V typically. The LED allows to manipulate the charge carrier concentration as studied in some experiments. Non negligible experimental errors coming at the cost of ease at fabrication and characterization and are discussed in Appendix A.2.

In summary, systematic errors arising from fabrication variations are present and qualitatively slightly higher than typical sensitivity of the measurement setup. Errors on resistivity are negligible compared to errors on mobility in the order of a few percent.

VAN DER PAUW THEORY AND EXPERIMENT

The van der Pauw Hall method allows for a direct measurement of resistivities and Hall voltages and thereby derivation of n and μ for hole-free samples with homogeneous thickness. Mathematically spoken the reciprocity theorem of passive multipoles can be applied to such a hole-free area with small contacts placed at the circumference [194]. Later we will see that specific geometries are useful to increase the robustness to experimental errors i.e. sample shape and placement of ohmic contacts.

Using specific measurement configurations one obtains resistances like $R_{21,43} = (V_4 - V_3)/I_{21}$ for a voltage drop $V_{21,43}$ between contacts 4 and 3 with a current bias applied to contacts 1 and 2, see also Fig. A.2 c). With two independent resistance measurements with different terminal configurations one can derive the bulk resistivity ρ [194]:

$$\rho = f\left(\frac{R_{12,43}}{R_{41,32}}\right)\frac{\pi t}{\ln 2}\,\frac{R_{12,43}+R_{41,32}}{2}. \tag{A.1}$$

Here t denotes the homogeneous thickness of the conducting layer and f is a func-

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[4] Keithley 6220, precision current source, www.tek.com/.../series-6200

[5] Keithley 2182a, nanovoltmeter, www.tek.com/.../nanovoltmeter-model-2182a

[6] Keithley 6487, picoamperemeter/voltage source, www.tek.com/.../series-6400-picoammeters

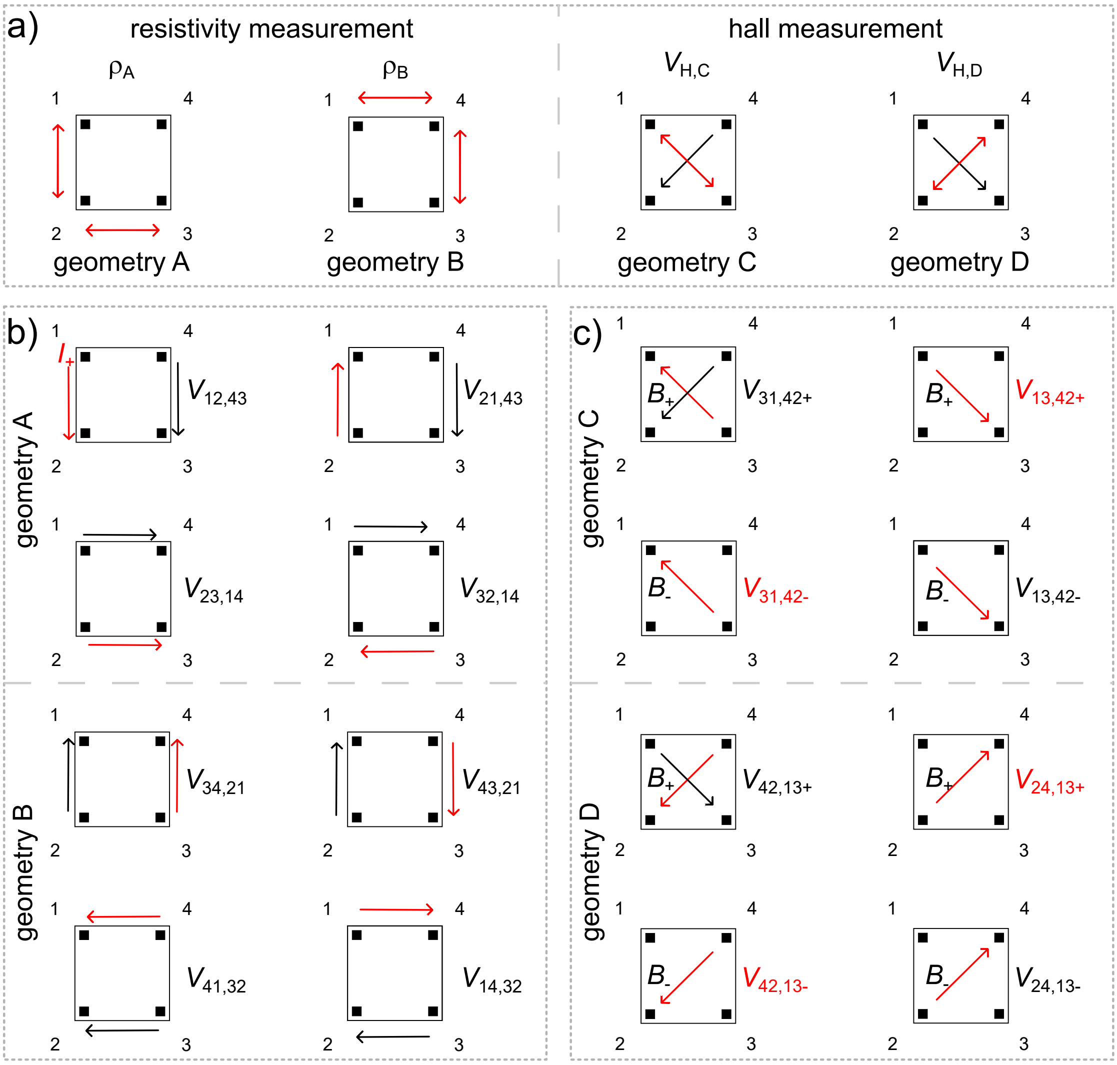

Figure A.3: Measurement configuration for a van der Pauw Hall measurement.
a) The sample is probed in different geometries to average out residual currents or voltages by symmetry operations. Illustration of current and voltage terminals as well as relevant magnetic fields for acquisition of b) resistivity and c) Hall voltage.

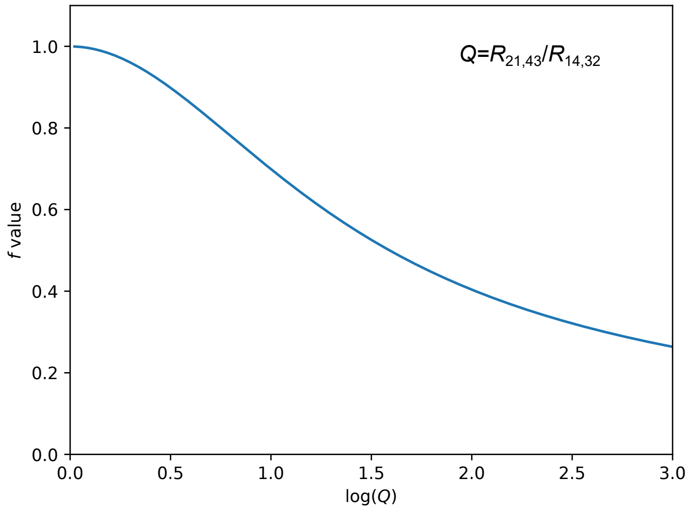

Figure A.4: The correction factor f as a function of resistivity ratio $R_{12,43}$ over $R_{41,32}$ is used for derivation of bulk resistivity.

tion of the resistance ratio $R_{21,43}/R_{14,32}$ defined by [194]

$$\frac{R_{12,43}+R_{41,32}}{R_{12,43}-R_{41,32}} = f \cdot \cosh^{-1}\left(\frac{\mathrm{e}^{\frac{\ln 2}{f}}}{2}\right) \tag{A.2}$$

and can be considered as correction factor for geometric distortions in the plane. The solution of this transcendent equation is given in Fig. A.4.
By application of current reversal and terminal permutation for the resistivity measurements one gets eight voltages $V_1, V_2 ..., V_8$ for a fixed bias current I. These can be interpreted as resistivities when using Ohms law and current reversal which is a sign change for the bias current:

$$R^{\mathrm{CR}}_{12,34} = \frac{1}{2}(V_{21,34} - V_{12,34})/I_{12} \tag{A.3}$$

In this notation with current reversal Eg. A.1 can be rewritten and yields

$$\rho_{\mathrm{A}} = f_{\mathrm{A}}\frac{\pi t}{\ln 2}\left(R^{\mathrm{CR}}_{12,34} + R^{\mathrm{CR}}_{23,14}\right) \tag{A.4}$$

$$\rho_{\mathrm{B}} = f_{\mathrm{B}}\frac{\pi t}{\ln 2}\left(R^{\mathrm{CR}}_{34,21} + R^{\mathrm{CR}}_{41,23}\right). \tag{A.5}$$

where $f_{\mathrm{A,B}}$ are obtained from Eq. A.2 using the measurement geometries A and B, respectively. Finally the resistivity can be obtained from direct measurement values and averaging resistivities from both measurement geometries, see also Fig. A.3:

$$\begin{aligned}\rho_A &= f_A \frac{\pi}{\ln 2} \frac{V_{12,43} - V_{21,43} + V_{23,14} - V_{32,14}}{4I} \\ \rho_B &= f_B \frac{\pi}{\ln 2} \frac{V_{34,21} - V_{43,21} + V_{41,32} - V_{14,32}}{4I} \\ \rho &= \frac{1}{2}(\rho_A + \rho_B).\end{aligned} \tag{A.6}$$

In magnetic fields with magnetic flux density B the resistances change as a consequence of the Hall effect introducing a Hall voltage V_H. Experimentally robustness of the Hall voltage measurement result is enhanced by including field reversal. Hall voltages are measured for both positive and negative magnetic fields, indicated by indices + and -, respectively. The resulting field reversed Hall voltage $V^{FR} = \frac{1}{2}(V_+ - V_-)$ averages both measurements including a sign change for the Hall voltage measured at negative field. Further averaging over the two possible geometries C and D with switched current and voltage terminals, see Fig. A.3 c), yields [195]

$$V_H = \frac{1}{4}\left(V^{FR}_{31,42} - V^{FR}_{13,42} + V^{FR}_{42,13} - V^{FR}_{24,13}\right) \tag{A.7}$$

The sign of V_H represents the type of charge carriers, for negative sign the material is n-type. Finally V_H can be used in the well known equations of the Hall effect for derivation of Hall coefficient R_H, carrier mobility n and electron mobility μ [196]:

$$R_H = \frac{tV_H}{IB} \tag{A.8}$$

$$n = \frac{IBV_H}{te} \tag{A.9}$$

$$\mu_H = \frac{R_H}{\rho} \tag{A.10}$$

$$\tag{A.11}$$

Here e denotes the electron charge. If a free electron gas is assumed for the derivation of the Hall coefficient the simple relation $R_H = \frac{1}{ne}$ is true.

The experimental results of the resistivity, electron mobility and density have to be critically questioned for reliability. Here I will go through the experimental and analytical method to discuss the measurement errors. Van der Pauw made the assumption of samples, i.e. conducting layers homogeneous in thickness. For the samples used this assumption is valid since the thickness deviations on sample scale are a few per mille at maximum deduced from ellipsometry. The assumption of infinitesimally small contacts can not be full filled in the lab. Simultaneously van der Pauw offers correction coefficients that correct for a finite size of contacts and also misplacement at finite distance from the circumference. Typical values for $\partial d/D$ are 5–10 % for the samples studied. The correction factors $\partial\mu/\mu$ or $\partial\rho/\rho$ are linear in d/D for the Hall voltage and quadratic for the resistivity while the prefactors are in the range of 0.1–0.7 [194]. It is to be noted that in general correction factors vary also with Hall angle θ where $\tan(\theta) = B\mu$ but this effect is small compared to the geometric contributions [197]. (if useful: elaborate more on geometry, i.e. using additional figure, introduce d/D. Cite Chwang 1974 [197] who relates geometric variations also to Hall angle). In a worst case approximation the sum of the correction terms for the prefactors is -1.07 for rho and -1.28 for μ on a sample featuring all deviations from perfect geometry. Still the correction terms for resistivity with typically less than 1 % can be neglected while correction can be of importance for mobility results. A full error analysis can be very precise when using the detailed measured on contact geometry and placement on a sample and corrects the mobility down by about $-1.3 \cdot d/D$. However since most of the samples have a ratio d/D of about 0.05 for samples with contacts at the corners on 7x7 mm chips or samples with small contacts close to the corners on 10x10 mm chips the correction terms of about 5 % are not applied. In comparison sensitivity of measurement hardware is below 1 % [198]. Within one temperature measurement series the deviation stays constant since sample geometry does not vary and mobility related changes on the correction terms are negligible. In summary, systematic errors arising from process related variations are present and qualitatively slightly higher than typical measurement sensitivity of the measurement hardware and setup. Errors on resistivity can be neglected compared to errors on mobility in the order of a few percent.

ELECTRICAL TRANSPORT MEASUREMENTS IN THE 4K SETUP

Spin qubits in semiconductors are expected to operate at cryogenic temperatures where thermionic excitation is negligible and less than the level splitting of the qubit. Sufficient suppression of thermal excitation is achieved at temperatures smaller or equal ≈1 K when both the sample environment is cool enough/heating power is big enough [93].[7] Most important the electron temperature needs to be below 1 K. Already wiring with low thermal/electric resistivity can increase electron temperature of the electron temperature in an active device which demands for appropriate choice of wiring and filtering [39, 199]. For the ZnSe project the main focus is on DC electron transport experiments at $T = 4\,\mathrm{K}$ without requiring control pulses or time resolved readout. For the experiments in the dewar setups the timing constants are chosen large (ms to s) to ensure a constant voltage configuration without the need for capacitive corrections. For ohmic contacts the actual device temperature does not strongly influence performance when thermal transport is already suppressed at $T \leq 10\,\mathrm{K}$. These requirements on operation temperature are met by both the 1 K[8] and 4 K system, providing high cooling power and allowing for fast turnaround measurements of the timescale of less than a day. The 1 K system provides about 40 DC lines

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[7] order μW in dilution fridges, orders of magnitude higher in liquid He system(1 K/4 K)

[8] The 1 K system is operated at 4 K and used for the additional features magnet, infrared LED and larger sample space within this project.

of CuNi wires with constant resistance over temperature with 1 kHz filtering and resistance of about 1 kΩ. The 4 K setup supports 24 DC lines consisting of unfiltered Cu wires with R=10 Ω at RT and R=5 Ω at 4 K when the dipstick is inserted. In both setups, the DC lines are unshielded but configured in twisted pairs to reduce inductive coupling. Control hardware used is a combination of SMUs (Keithley 240X) and DC voltage sources (decadacs) built in-house. For experiments at low current levels of <1 nA, lock-in measurements (Stanford Research SR830) allow for improvements of the signal-to-noise ratio.

A.3. OHMIC CONTACTS

COMPARISON OF MODELS FOR EVALUATION OF CONTACT RESISTIVITY

Fig. A.5 provides an overview of available theories to describe and evaluate contact resistivities, developed in the past. A very early simple model by Kennedy and Murley (KM) interprets the contact resistance as a consequence of the resistive substrate below the contact in the limit of negligible specific contact resistivity, i.e. perfect conductivity at the metal-semiconductor interface [94].

We will quantitatively see the differences between TLM and ETLM theory are negligible in the regime of long contacts and relatively high specific contact resistivities. Assumptions of TLM break down for non negligible potential drop in the substrate, which is included in the ETLM model, for which Zhang et al. developed analytical solutions [96]. Still, for a wide parameter space (E)TLM yields good approximations that only slightly (overestimate) underestimate the actual specific contact resistivity, as will be explained in the following:

Fig. A.5 a) displays how in the case of small contacts a/h_b=0.01 the differences of the (E)TLM underestimates (overestimates) ρ_c for low resistivities. Deviations between the models strongly reduce for typical contacts that are at least as wide as the substrate is thick $a/h_\mathrm{b} > 1$ or if ρ_c gets larger. Good agreement with deviations below about ten percent between exact solution and TLM (ETLM) is found for $\rho_\mathrm{c} > 2$ ($\rho_\mathrm{c} > 0.2$ and $a/h_\mathrm{b} > 0.2$) [96]. In the limit of infinitesimally large contacts the contact resistance gets insensitive to specific contact resistivity as the spreading resistance gets dominant.

The special case of vanishing resistance is the KM model. The current is significantly spread across the contact region, not just restricted to the contact edge. Using conformal mapping Hall derived expressions for evaluating the spreading resistance to be $R_\mathrm{c,Hall68} = ln(4)/\pi = 0.441$ [95].[9]

(E)TLM can be applied for large specific normalised contact resistances r_c. ETLM can correctly describe the problem for up to 100 fold lower resistivities whereas the KM model without finite r_c cannot be applied at all [94, 96]. ETLM can correctly describe the problem for up to 100 fold lower r_c compared to TLM. For even lower r_c only the exact solution is a useful model. It is very important to choose the proper model

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[9] In the nomenclature of Ref. [96] R_c is larger by a factor of 2π.

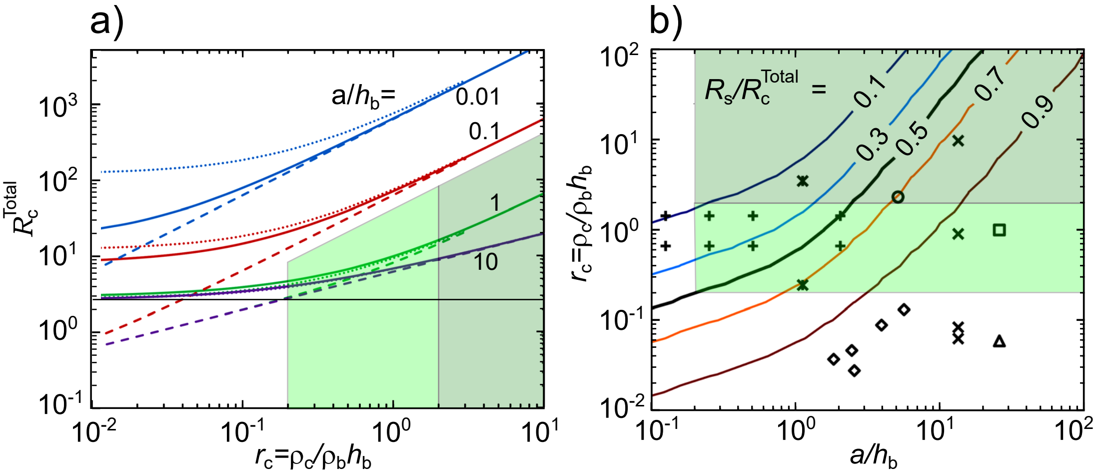


Figure A.5: Comparison of models for assessment of contact resistivity. a) Total contact resistance R_c^{tot} in the parameter space for arbitrary physical (x-axis) and geometrical (a/h_b) configuration. Solutions of the exact model are marked by solid lines and by dashed (dotted) lines for (E)TLM. The KM model is represented by the vertical line. The valid regimes are highlighted in (light) green for the (E)TLM model. b) Projection of panel a) with a highlight on the spreading resistance R_{spread}^{tot} indicated by equipotential lines. Experimental data for different semiconductor materials and contact metals is depicted. Figure adapted from [96].

for determination of the contact resistance. Fig. A.5 b) indicates the parameter range where the spreading resistance is dominating $R_s/R_{c,tot} > 0.5$ and in consequence very likely overestimated by analysis based on the TLM model.

Since the contacts are very large, substantial current spreading occurs (large for large L_t). In other words, the contact length is sufficiently large compared to the transfer length. Differences of TLM and ETLM are negligible in this regime and both models describe the situation correctly, without the need for an exact solution [96]. The contact resistance arises from contributions from the resistive bulk substrate and from the resistance of the interface layer to different degrees.

Applicability of TLM in the simple forms of Eq. 3.2,3.6 has to be ensured. Typically contact resistivities of metal contacts on ZnSe are not lower than $1 \times 10^{-4}\,\Omega\,\mathrm{cm}^2$ [78] on the substrates used (ρ_s=40 Ω/□, h_b=1 µm). The corresponding parameter space ($r_c > 10$ and $a/h_b \approx 100$) is safely covered by TLM as correction terms are negligibly small, see Fig. A.5 a).

ANNEALING OF ION IMPLANTED CONTACTS

After ion implantation, an annealing step was conducted to recover the crystal structure, activate donors and thereby reduce the electrical resistance. Regarding the development of a fabrication technique to contact the 2-DEG in a ZnMgSe/ZnSe/ZnMgSe quantum well (QW) structure, the suitable temperature range of annealing is limited and can lead to degradation of the ZnSe/ZnMgSe interfaces by interdiffusion. Such degradation has been shown by photoluminescence investigations of similar QWs after rapid-thermal annealing for 30 s at about 400 °C [200]. Consequently, we focused our investigations on annealing temperatures around 250 °C to 300 °C according to typical MBE growth conditions of ZnSe. After application of an annealing step for 3 min at 250 °C a substantial improvement of the conductivity was achieved. However, a distinct increase of the resistance in the electrical measurements of the samples B* and C* is observed after a second 3 min long annealing step at 300 °C was applied. Exemplary IV-characteristics of sample C* before (red) and after (green) the second annealing step are shown in Fig. A.6. The IV curves were achieved by two-terminal measurements at a needle probe station under ambient light conditions.

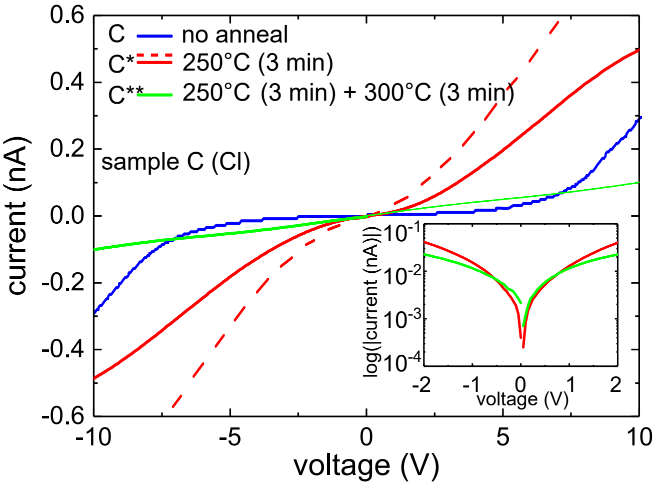


Figure A.6: IV profiles for Cl implanted sample C for different thermal annealing steps. The insert is the logarithmic representation of the absolute current for the low bias voltage range ±2 V. Figure by Johanna Janßen [5].

ANNEALING OF AL IN-SITU CONTACTS ON HETEROSTRUCTURES WITH QW

Further optimization of the Al *in-situ* contact is envisioned for post metal anneal by improvement of the semiconductor-metal interface. Fig. A.9 gives experimental data on the IV profiles of corresponding samples prior and after annealing under optimised conditions. A degradation of contact resistance is observed for samples with both doped and undoped barriers as the IV curve is flattened after annealing, present

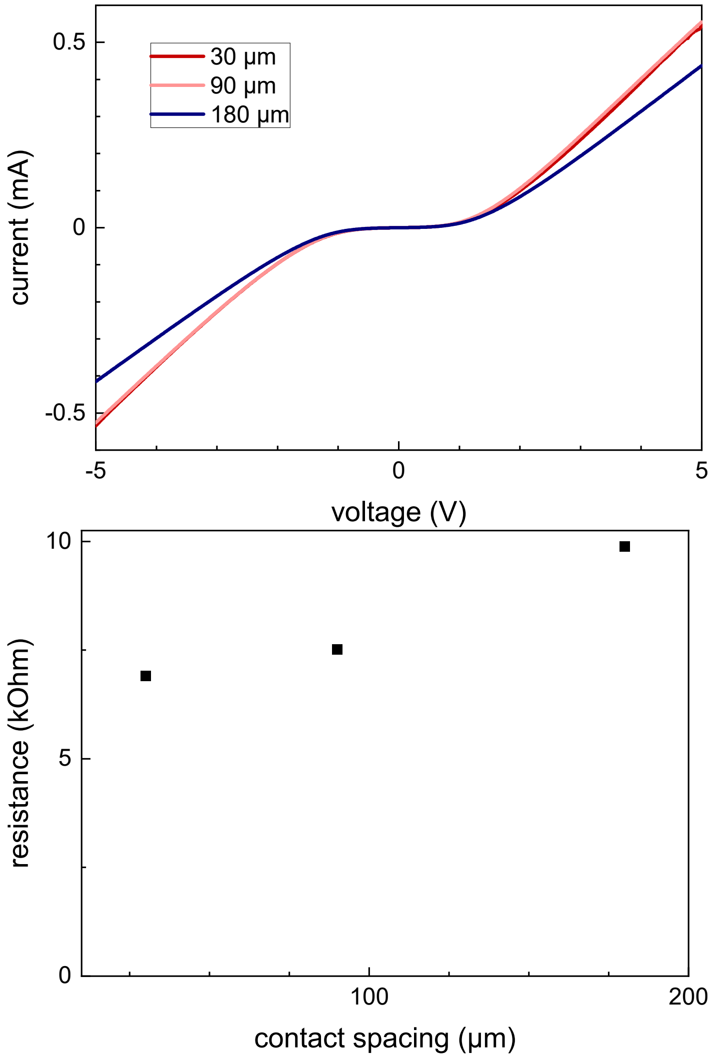


Figure A.7: Electrical characterization of In diffusion contacts after thermal annealing. a) *IV* profiles for a TLM structures annealed twice at 250 °C for one minute. b) $R(d)$ obtained from the differential resistance at 3.5 V. Measurement by Johanna Janßen.

in both samples with doped and undoped barrier, see Fig. A.9 a) and b), respectively. Differential and total resistances are plotted in panels b,c) and e,f) accordingly before and after annealing to highlight the trend. Slightly increased sheet resistance (correlated to the differential resistance for large bias voltage) after annealing can again be attributed to Zn vacancy creation during anneal compensating n. The same effect can increase the contact resistance (differential resistance at zero bias voltage) when the effective doping concentration is lowered and the depletion zone of the junction increases.

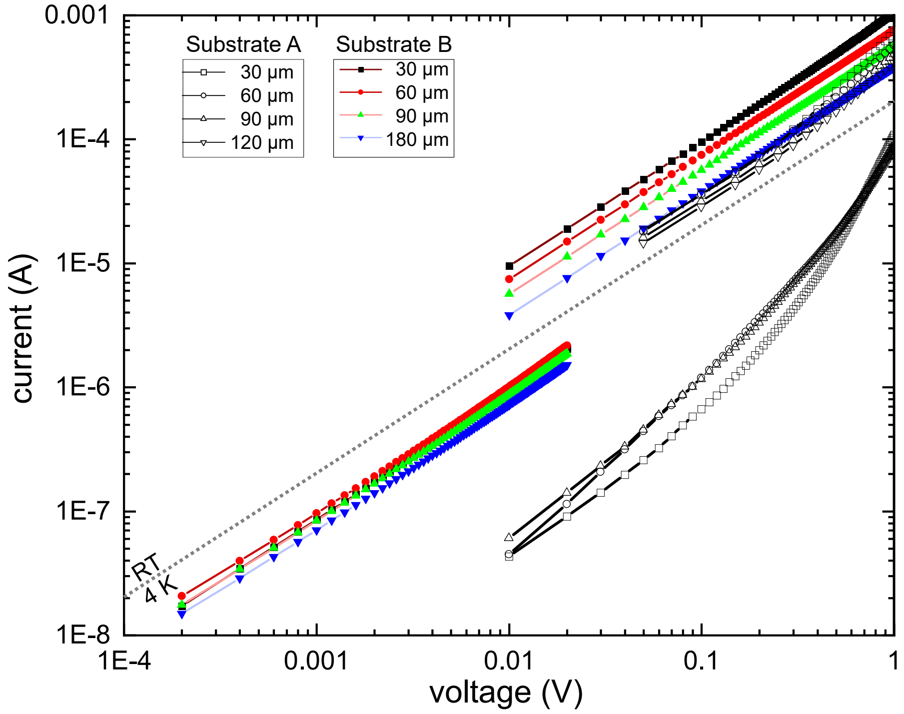


Figure A.8: *In-situ* deposited Al contacts to substrates with ZnSe:Cl QW for different barrier doping. *IV* characteristics of a sample with doping level of 2×10^{18} cm^{-3} (Substrate A) and 5×10^{18} cm^{-3} (Substrate C), respectively. Measurements of TLM devices were performed at RT and LT (4 K. The diagonal dotted line depicts a linear *IV* dependency. Lower current levels correspond to measurements at 4 K. For specifications of the substrates please see Sect. 3.5.

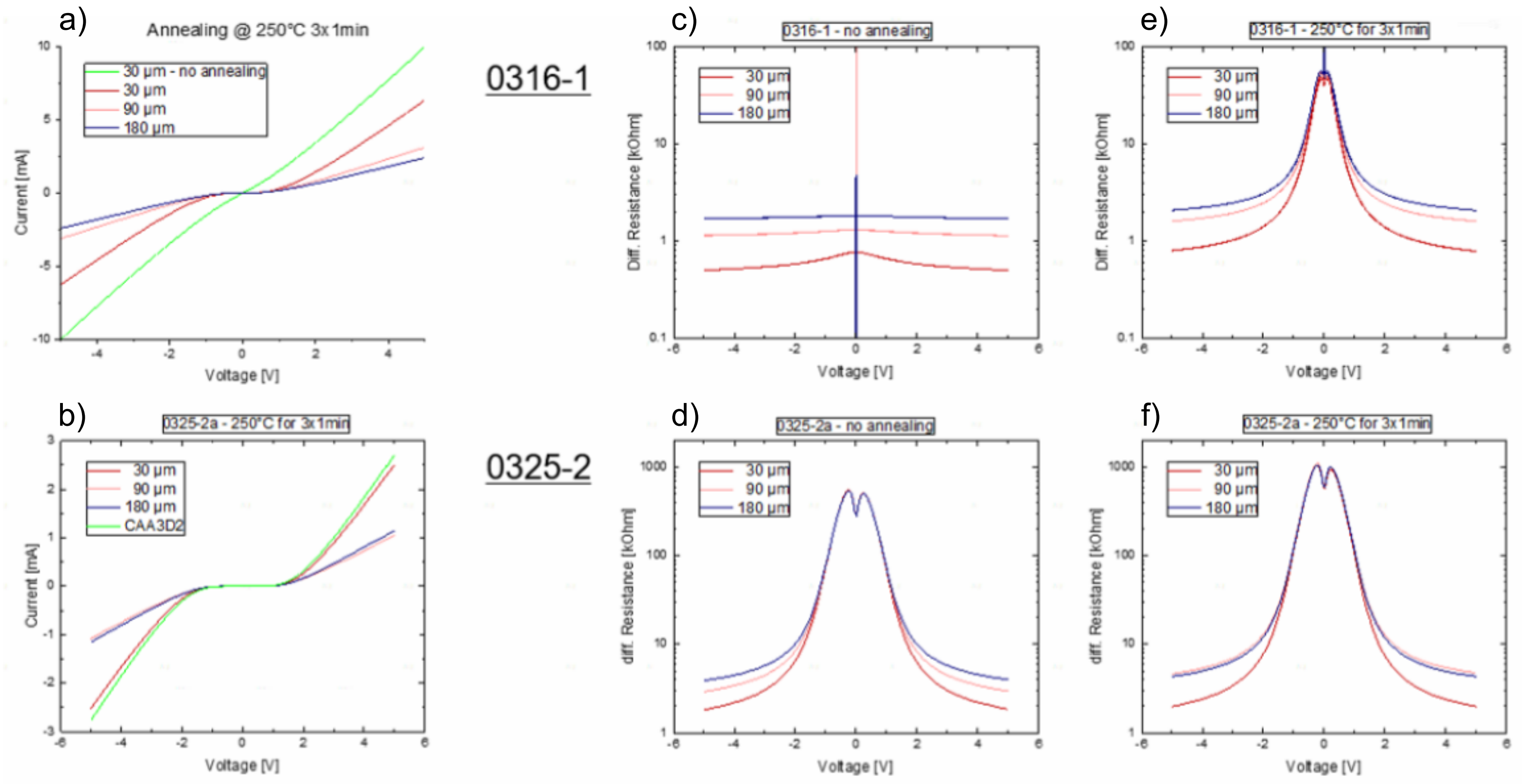


Figure A.9: *In-situ* deposited Al contacts to QW HS, annealed, IV profiling at RT. a (b) IV profiling of QW samples with high (low) carrier concentration before and after annealing three times at 250 °C for 1 min each. The differential resistance is shown for the (un)doped device c(d) before and e(f) after annealing three times at 250 °C for 1 min each. Measurement by Johanna Janßen.

OVERVIEW ON SPECIFIC CONTACT RESISTIVITY TO N-ZNSE FOR VARIOUS FABRICATION TECHNIQUES

					R_c (Ω)	R_s (Ω/□)	ρ_c (Ω cm^2)	L_t (μm)
Tab. 3.2: In, *ex-situ*, diff., HS/QW, (RT)								
metal		T_{ann} (°C)	t (min)	design				
In		175	1	vdP	5×10^7–2×10^9	1×10^4	2×10^4–8×10^5	1×10^4–9×10^4
In		185	1	vdP	1×10^5–2×10^{10}	1×10^4	4×10^1–8×10^6	6×10^2–3×10^5
In		200	1	vdP	3×10^5–1×10^{10}	1×10^4	1.2×10^2–4×10^6	1×10^3–2×10^5
In		250	1	vdP	3×10^5–1×10^6	1×10^4	1.2×10^2–4×10^2	1×10^3–2×10^3
In		300	1	vdP	1×10^9–2×10^9	1×10^4	4×10^5–8×10^5	6×10^4–9×10^4
In		200	120	TLM	3×10^5	1×10^4	4×10^1	6×10^2
In		225	20	TLM	1×10^5	1×10^4	1×10^1	3×10^2
In		250	3	TLM	1×10^5	1×10^4	1×10^1	3×10^2
Tab. 3.4: *ex-situ*, Ar mill, (RT)								
Al		-			0.8×10^2	49	1.1×10^{-2}	1.5×10^2
Ti		-			1.3×10^2	49	1.9×10^{-2}	2.0×10^2
Nb		-			0.6×10^2	49	0.1×10^{-2}	1.4×10^2
Al		0 nm			2.0×10^3	49	0.3	0.8×10^3
Al		5 nm			8.5×10^3	49	1.2	1.6×10^3
Al		10 nm			6.5×10^3	49	0.9	1.4×10^3
Tab. 3.5: Al, *in-situ* (RT)								
Al					1.4	39	2.3×10^{-5}	7.7
Mg					1.5	29	3.7×10^{-5}	11.4
Ti					3.6	27	24×10^{-5}	29.5
Tab. 3.6: Al, *in-situ* (RT/LT)								
	T	mesa			R_c (Ω)	R_s (Ω/□)	ρ_c (Ωcm^2)	L_t (μm)
Al	RT	10 μm			25	44±3	$2.3 \pm 0.9 \times 10^{-5}$	7±2
Al	RT	50 μm			6	45.5±0.7	$6 \pm 2 \times 10^{-5}$	11±2
Al	4 K	10 μm			28	42±3	$4 \pm 2 \times 10^{-5}$	10±2
Al	4 K	50 μm			8	42±3	$17 \pm 3 \times 10^{-5}$	20±2
Tab. 3.7: Al, *in-situ*, regrowth (RT/4 K)								
	sample	T			R_c (Ω)	R_s (kΩ/□)	ρ_c (Ω cm^2)	L_t (μm)
Al	RG	RT			11	0.38±0.05	$1.7 \pm 0.2 \times 10^{-4}$	6.7±0.4
Al	Ref	RT			20	0.36±0.05	$5 \pm 1 \times 10^{-4}$	12±1
Al	RG	4 K			53	1.8±0.2	$1.4 \pm 0.4 \times 10^{-3}$	9±1
Al	Ref	4 K			61	2.0±0.2	$1.0 \pm 0.2 \times 10^{-3}$	7.1±0.7
Tab. 3.8: Al, QW, *in-situ* (RT/LT)								
	sample	T	$c^{SIMS}_{Cl,barrier}$ (cm^{-3})	mesa (μm)	R_c (kΩ)	R_s (kΩ/□)	ρ_c (Ω cm^2)	L_t (μm)
Al	D	RT	2.5×10^{17}	50	350	5.4	5×10^1	1×10^3
Al	A	RT	2×10^{18}	50	1	4.3	1×10^{-3}	6
Al	B	RT	3×10^{18}	190	0.5	3.2	3×10^{-3}	10
Al	C	RT	5×10^{18}	150	0.3	6.8	7×10^{-4}	3
		T			4 K	25 K	4 K	4 K
Al	D	LT	2.5×10^{17}	50	-	8.2	-	-
Al	A	LT	2×10^{18}	50	70	8	1×10^1	4×10^2
Al	B	LT	3×10^{18}	190	7	5	1	23
Al	C	LT	5×10^{18}	150	4	18	3×10^{-3}	4
Tab. 7.2: Al, *in-situ*, shadow mask (RT)								
		x_{Mg} (%)	n_{ZnMgSe} (cm^{-3})	t_{AlOx} (nm)	R_c (kΩ)	R_s (kΩ/□)	ρ_c (Ω cm^2)	L_t (μm)
Al	D	20	-	20	0.30 ± 0.02	1.3 ± 0.3	1.3×10^{-3}	34 (W28-07)
Al	E	20	-	20	0.32 ± 0.02	3.0 ± 0.3	1.6×10^{-3}	15 (W28-05)
Al	F	10	-	20	0.78 ± 0.02	7.3 ± 0.3	3.8×10^{-3}	16 (W28-08)
Al	G	20	5×10^{17}	0	1.00 ± 0.05	9.2 ± 0.5	1.4×10^{-2}	16 (W27-09)

A.4. ELECTRICAL TRANSPORT

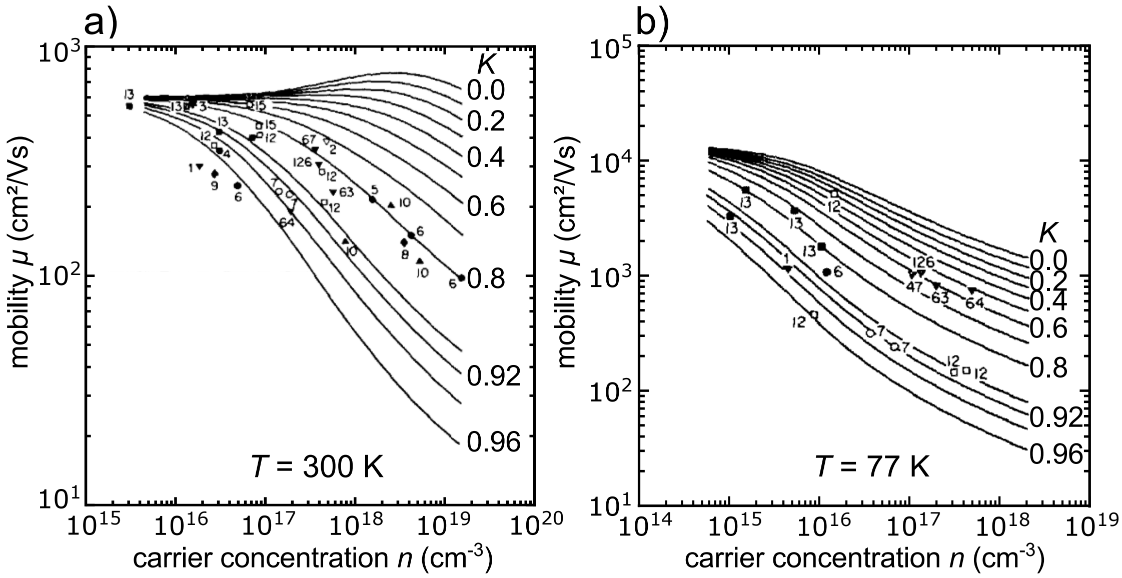


Figure A.10: Experiment and theory for transport in bulk ZnSe. Experimental data and theory including compensation (K) for electrons in ZnSe at a) RT and b) 77 K. Figure adopted from Ref. [118].

Table A.2: Experimental and theoretical material properties for ZnSe

property	unit	experiment	theory
ϵ_r	1	8.6	
m_{eff}	m_e	0.147 [121]	
E_d	meV	25 [138]	27 [118]
E_g	eV	2.82 [121]	
α_{SO}		0.021 [23]	
FLP	eV	0.12 [92]	0.12, 0.13 [92, 201]
n_c	$10^{17}\mathrm{cm}^{-3}$	1.3–6[122], > 5 [142]	4 [140], 4.4 [149], 5.2 [123]

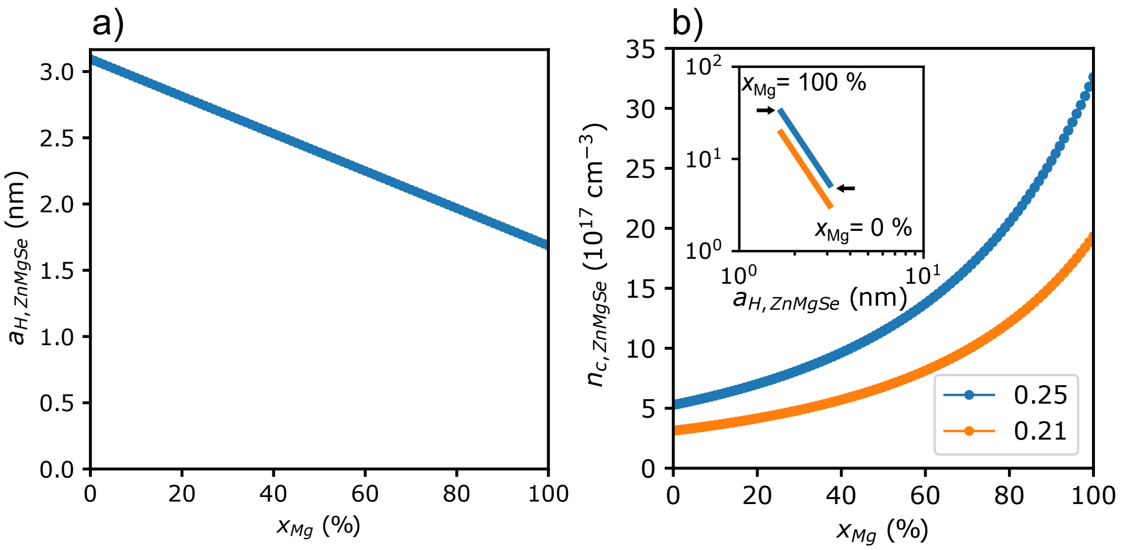


Figure A.11: The Mott criterion for the critical density in $Zn_{1-x}Mg_xSe$. a) Bohr radius of electrons derived by Vegard's law (Eq.4.14) and b) critical density for different x_{Mg} and derived from the Mott criterion (Eq. 4.13). Proportionality constants of the Mott criterion are specified and material constants are taken from Tab. A.2 (ZnSe) and Tab. A.4 (ZnMgSe). The insert provides the power law representation of the critical density on the Bohr radius. Extreme cases for x_{Mg} are indicated by the arrows.

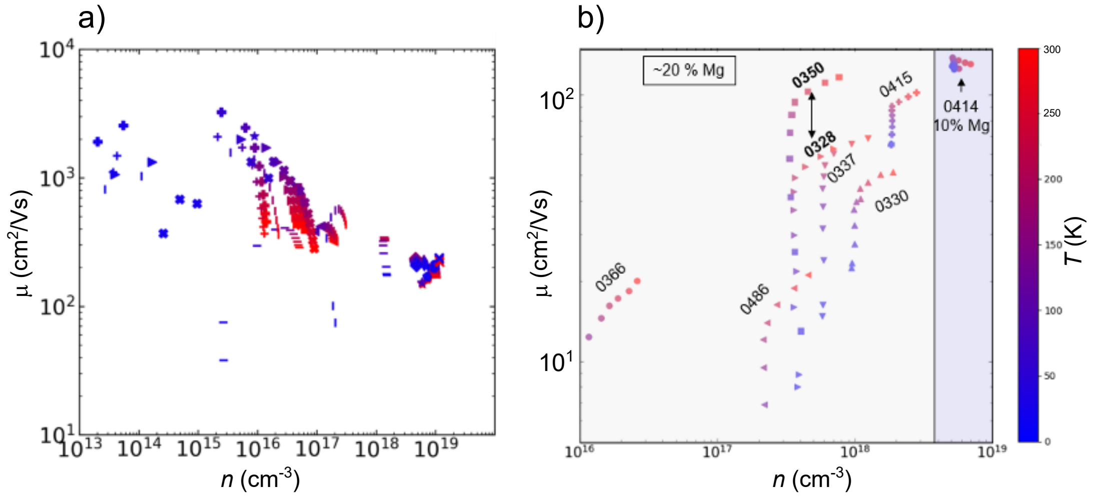


Figure A.12: Temperature dependent transport properties of epitaxially doped ZnSe and ZnMgSe. Electron mobility as a function of electron concentration and temperature determined by van der Pauw Hall measurement of bulk a) ZnSe and b) ZnMgSe with a composition of x_{Mg}=14-21 %. Different samples are represented by individual symbols. Measurement temperature is color coded and ranges from 30–300 K.

A.5. FABRICATION

This section gives supplementary information on all steps required in fabrication to get to the target device architectures. It includes a representation of the designs of the corresponding target devices as implemented as glass mask for mask aligners or jobs at the maskless aligner (MLA100) in HNF. Designs used are the Hall-bar design and DQD device design depicted below.

RUNSHEET HNF CLEANROOM

Runsheet for ZnSe processing in HNF cleanroom and Nanocluster (latest revision by Jürgen Moers, July 2021, 4 pages). The runsheet is based on a joint development together with Johanna Janßen.

July 2021

Run Sheet – Felix Khamphasithivong, QuTech/ JARA

Topic: Realization of metal contacts and fine gates on ZnSe

<u>Sample properties:</u>

- Sample size: about 10x10 mm
- Substrate material: GaAs
- Layer sequence (samples grown in Nanocluster):
    - Sample type A: GaAs/ZnSe
    - Sample type B: GaAs/ZnSe/Al, Mg
    - Layer thicknesses: ZnSe: (70 – 1000) nm, metal: (50 – 100) nm
    - Optional variations:
        - ZnSe -> ZnMgSe/ZnSe/ZnMgSe
        - ZnSe -> ZnSe:Cl (epitaxially chlorine doped)
        - Capping with Al_2O_3 (~15 nm)
- Previous processing (optional): Ion implantation (F, Cl, Al)

<u>Process steps:</u>

A: GaAs/ZnSe	B: GaAs/ZnSe/Metal
1. **Cleaning**: Acetone, IPA, 3 min resp. *(WB 5.1)*	
2. **Optical lithography:** *a.* Resist coating: AZ 5214E, 45 s @ 4000 rpm *(WB 5.3)* *b.* Soft bake: hot plate, 90 °C, 5 min *(WB 5.3)* *c.* Exposure: dose: 75 mJ/cm² *(MA 2/ MA 4/MLA 100)*	
d. Post exposure bake: hot plate, 115°C, 2 min *(WB 5.3)* e. Flood exposure: 350 mJ/cm² *(MA 2/ MA 4)*	--- ---
3. **Development**: AZ 326 MIF, 60 s *(WB 5.2)*	
4a. Metal deposition *(outside cleanroom)*	**4b. Etching of metal layer**: AZ 326 MIF, ~ 5 min *(WB 5.2)*
5a. Lift-off: Acetone, IPA, DI water *(WB 9)*	**5b. Resist removal**: Acetone, IPA, DI water *(WB 5.1 or WB 9)*

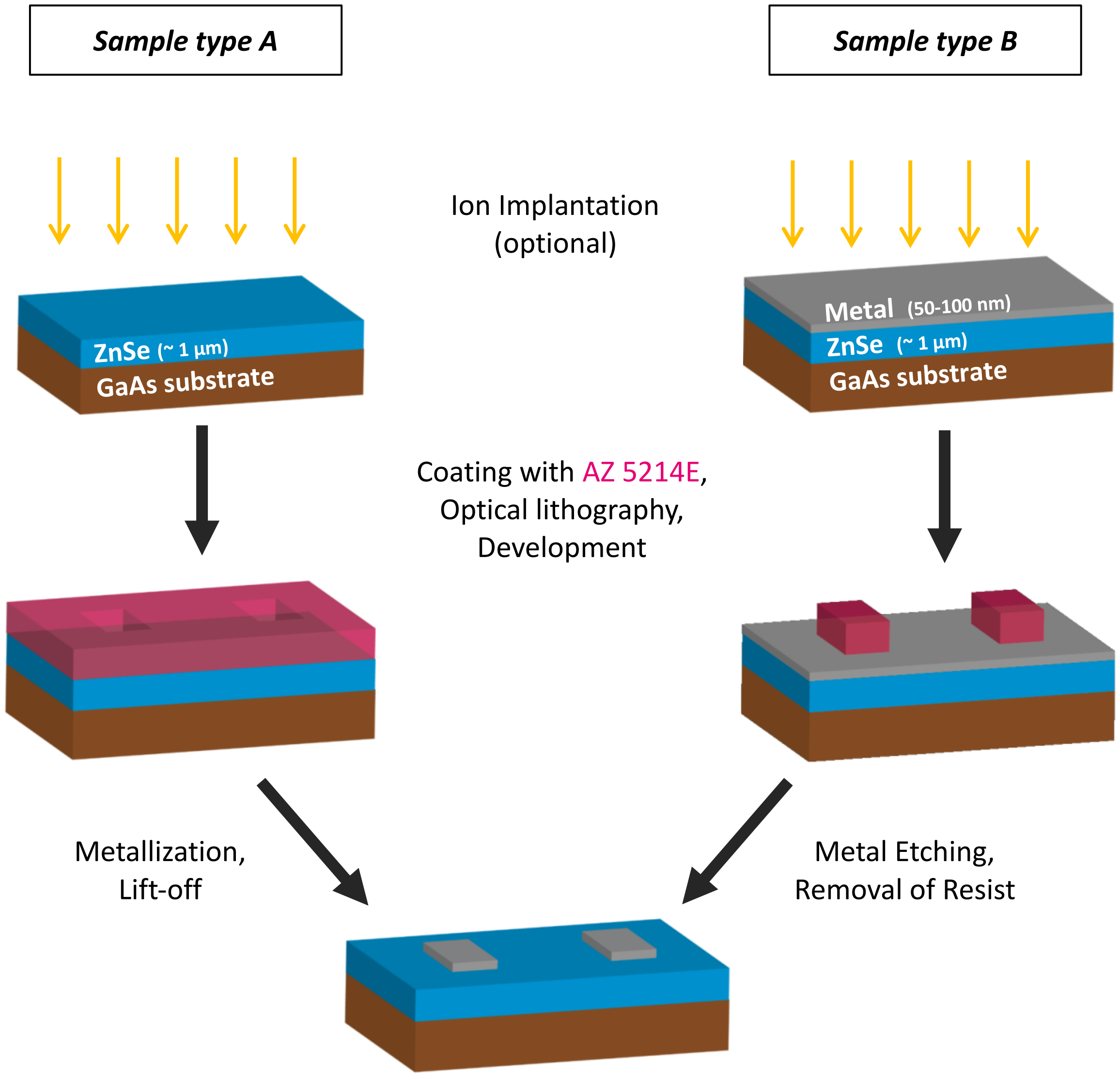
<u>**Optional**</u>: Repetition of the cleaning and lithography steps, followed by:

5. RIE etching (RIE-5, process with CHF_3/O_2 or Cl_2/Ar, including In etching)
6. Deposition of dielectric material (e.g. Al_2O_3 or HfO_2, *Nanocluster*)
7. Wet chemical etching of Al_2O_3 in an alkaline development solution (AZ 326 MIF, *WB 5.2*)
8. Re-growth of ZnSe:Cl in Nanocluster (cf. page 3 for complete process)
9. Wet-chemical etching with $K_2Cr_2O_7$+HBr, NH_3+H_2O_2 or Citric Acid (cf. page 3 for details)

Additional tools that are sometimes used inside the cleanroom for analysis:

- Ellipsometer
- Dektak
- Microscope
- SEM
- AFM
- Probe station
- Scriber
- Gigabatch

Schematic process flow:



Additional processes (possible future projects):

Etching of metal layer:

- Starting sample: ZnSe, capped with Mg/Al (e.g. 50nm/50nm)
- AZ 326 MIF, 60 s, stop in H_2O, >3 min (*WB 5.2*)
- Diluted HCl ($HCl:H_2O$, 1:300), 5 s, stop in H_2O, >3 min *(WB 6)*
- IPA or HF (1-50 %) or BOE for lift-off or oxide etching

Re-growth of ZnSe:

- Starting sample:
  - GaAs substrate
  - Layer sequence: GaAs/ZnSe/ZnMgSe /ZnSe:Cl/ZnMgSe/ dielectric (e.g. Al_2O_3 or HfO_2)
  - Approximate layer thicknesses: Substrate/7 nm/15 nm/70 nm/30 nm/15 nm
  - Sample size: ~ 10 x 10 mm
- Process steps:
  1. Cleaning, optical lithography, development (see table on p.1 , steps 1., 2a.-2e., 3.)
  2. Etching of dielectric: Development solution (AZ 326 MIF, *WB 5.2*) or RIE-5 (CHF_3)
  3. Resist removal (DMSO or Acetone, IPA, DI water *(WB 5.1 or WB 9)*; if necessary ultrasonic or Gigabatch)
  4. Etching of ZnMgSe/ZnSe: RIE-5 (Cl_2/Ar or maybe H_2/Ar)
  5. Wet chemical etching with one of the following solutions (etching at room temperature with magnetic stirring)
     - $C_6H_8O_7$ (citric acid) or $C_6H_8O_7:H_2O_2$ (best ratios have to be determined)
     - or $NH_4OH:H_2O_2$ *(WB 10 or WB 11_1)*
     - or $K_2Cr_2O_7$:HBr *(WB 11_1 or PL Lab Pawlis)*
  6. Regrowth of ZnSe:Cl *(MBE, Nanocluster)*, deposition of Al or Mg/Al *(Nanocluster)*
  7. Cleaning, opt. litho., development, metal etching (see table on p.1, right column)
  8. Etching with $K_2Cr_2O_7$+HBr
- Order of process steps might change
- The sample might be further processed e.g. to fabricate gate structures

Metallization:

- Optionally HF (BOE, 10%, 2%, 1 min) or HCl etch (37%, 10 min) before metallization (*WB 6*)
- Deposition of Ti, Pt, Al, or Nb (*Balzers_PLS_500, Univex 400*)
- Deposition of In (Nanocluster, metal MBE)

E-beam fine gates:

1. **Cleaning**: Acetone, IPA, 3 min resp. (US if no fine gates / low power), N_2 dry *(WB 5.1/ WB 9)*
2. **Coating** *(WB 5.3):*
    a. Dehydration: 180°C, >3 min
    b. Coating: AR 639.04 (50k), 30 s @ 5000 rpm
    c. Bake: hot plate, 180 °C, 15 min
    d. Coating: AR679.02 (950k), 30 s @ 4000 rpm
    e. Bake: hot plate, 180 °C, 5 min
3. **E-beam exposure (100 keV)**
4. **Development** *(WB 5.1 or WB 9):*
    a. IPA, 3 min
    b. H_2O, 15 s
    c. H_2O, 15 s in second beaker
5. **Metal deposition** (e.g. Ti/Pt; *PLS 500, Univex 400, or outside of cleanroom*)
6. **Lift-off:**
    a. Acetone, pipette, optionally US @ level 1
    b. IPA
    c. N_2 dry

- Process might be slightly varied, e.g. additional layer of PMMA, different e-beam resist and development solution, Gigabatch after development …

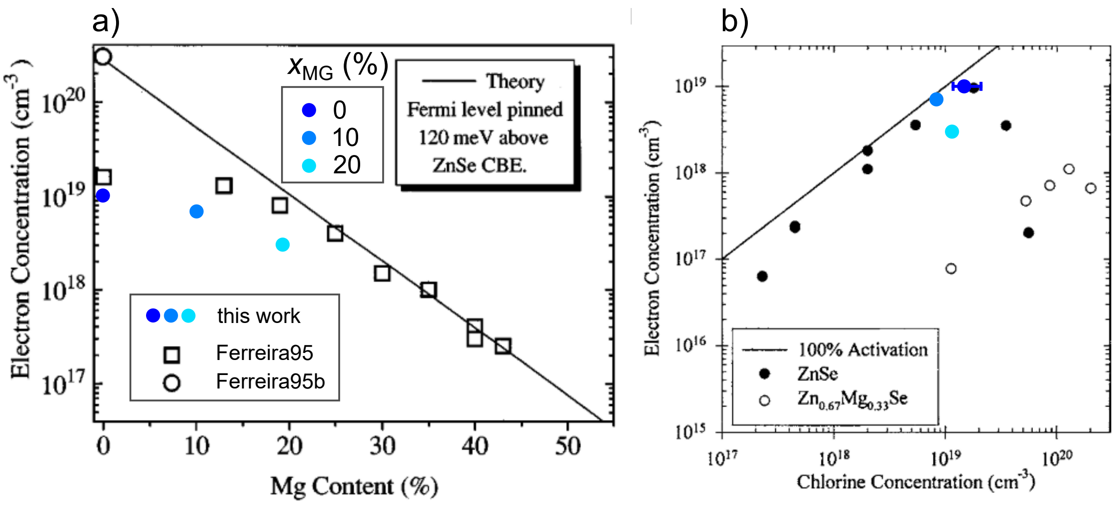


Figure A.13: Experimental study of epitaxial doping of ZnMgSe:Cl. a) Maximal electron concentration at RT in $Zn_{1-x}Mg_xSe$ for different x_{Mg}. The black line denotes the theoretical limit for a Fermi level pinned at 120 meV above the conduction band edge (CBE) [92]. b) Electron concentration versus Cl concentration obtained by SIMS for ZnSe and $Zn_{1-x}Mg_xSe$ (x_{Mg} =0.33) [147]. Panels a) and b) are adapted from [92, 147], respectively.

RECOMMENDATIONS FOR FABRICATION OF II-VI MATERIALS IN HNF

A detail not addressed so far is sample motion during the etch. Inhomogeneous etch profiles have been observed that in some cases with low agitation, see Fig. A.18. Two measures were taken to increase homogeneity and thus reproducibility of the process: Both ultrasonification and manual stirring increase relative motion of etchant versus sample both on micro and macroscale. This observation also underlines the relevance of redeposition in the etch process. Further optimization of the process included adaption of the resist mask covering all Al contacts. Unprotected Al structures were uncontrolled etched by the solution, prevented by a resist pattern overlapping critical structures by 3 µm.

Table A.3: Experimental and theoretical material properties for MgSe

property	unit	experiment	theory
ϵ_r	1		7.3 [202]
m_{eff}	m_e	0.23 [140]	
E_d	meV	25 [138]	27 [118]
E_g	eV	3.74 [130], 4.0 [131]	-
FLP	eV	0.12+X [92]	0.12+X, 0.13+X [92, 201]

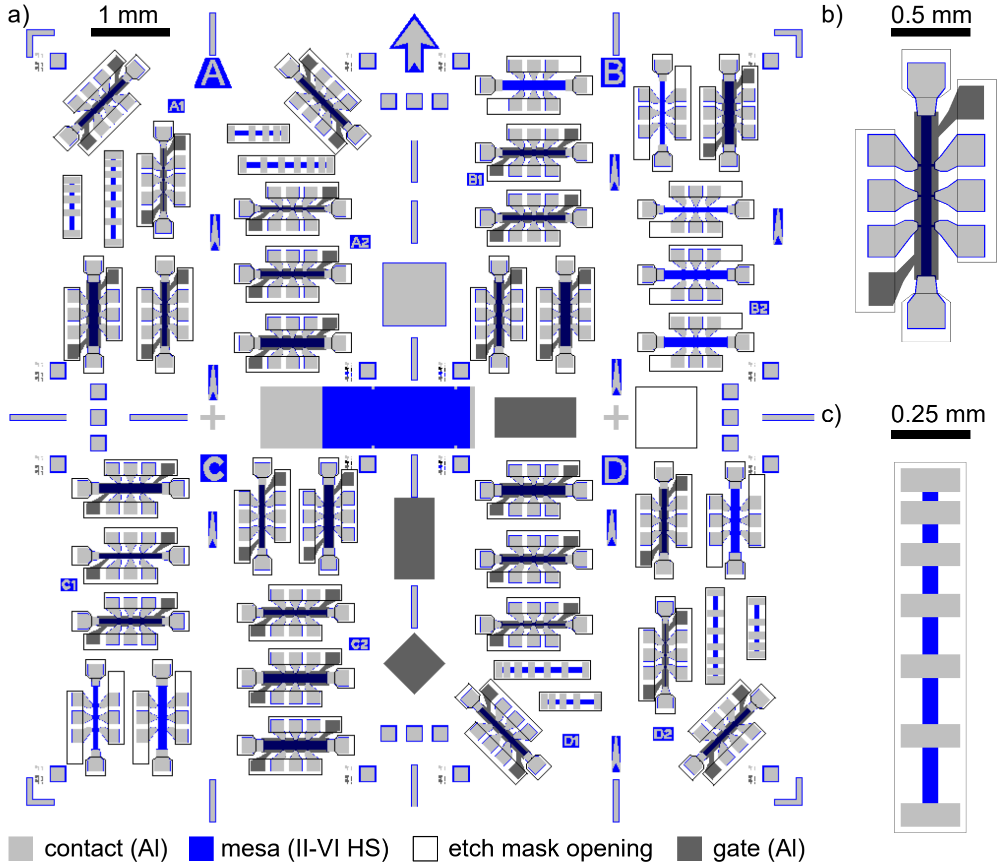


Figure A.14: Gated Hall-bar design. Designs for an a) entire 10x10 mm chip with b) gated Hall-bars orientated in four crystallographic orientations ((011), (01-1), (010), (001)) and c) TLM structures. Layers are color coded according to the description in the bottom line.

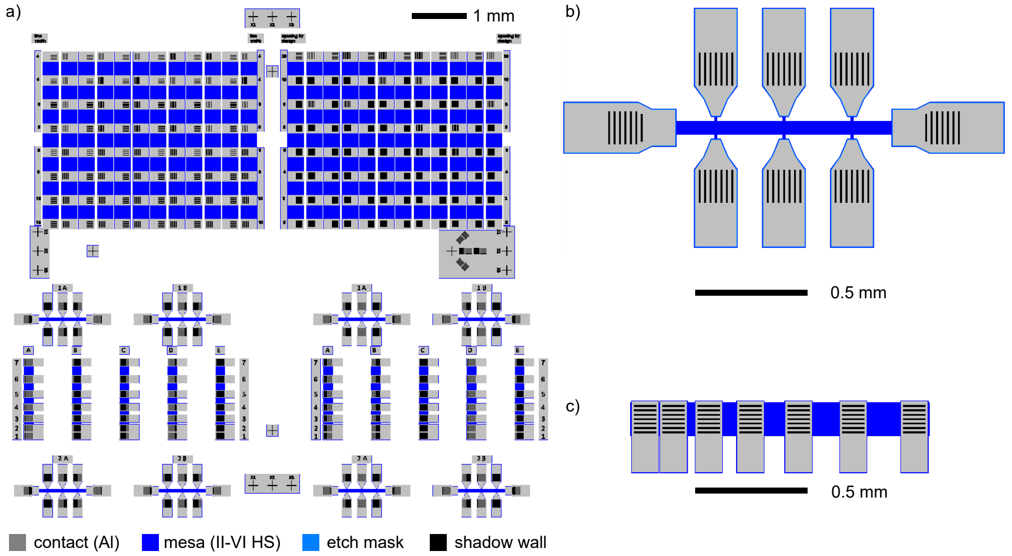


Figure A.15: Shadow mask design. Designs for a) 10x10 mm chip including test structures (upper half), b) gated Hall-bars and c) TLM structures. Layers are color coded according to the description in the bottom line.

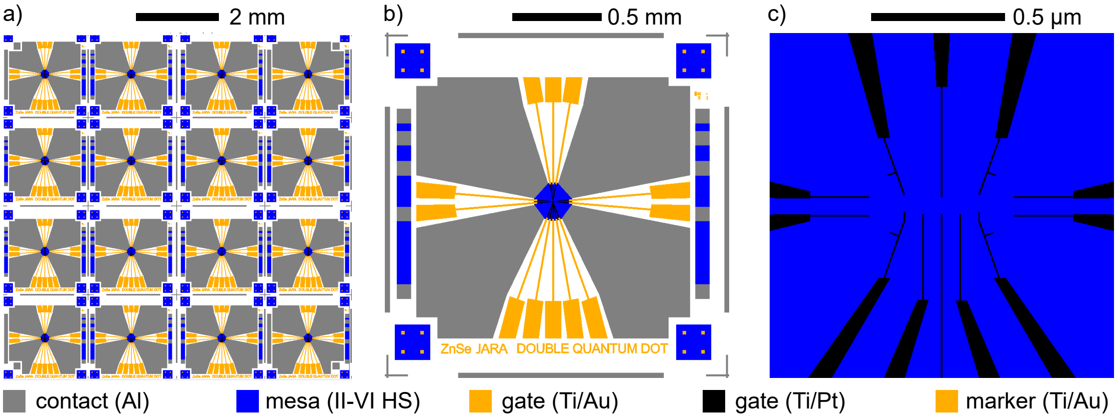
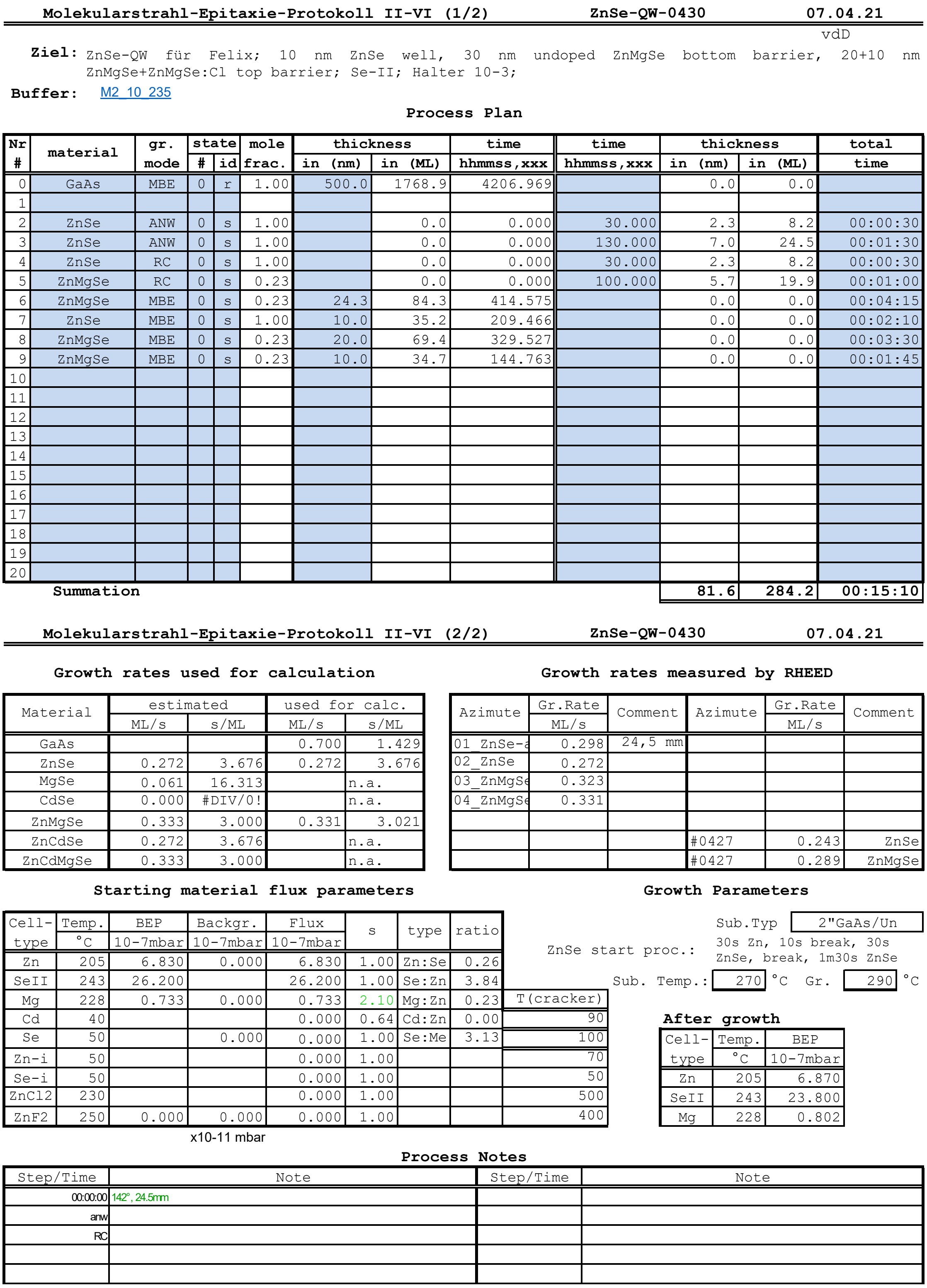


Figure A.16: Layout for EDQD devices. a) Layout for 10x10 mm chip containing 16 uncoupled b) EDQD devices. c) Gate design for the QD region as used for ebeam lithography. Layers are color coded according to the description in the bottom line.



Molekularstrahl-Epitaxie-Protokoll II-VI (1/2) **ZnSe-QW-0430** **07.04.21**

vdD

Ziel: ZnSe-QW für Felix; 10 nm ZnSe well, 30 nm undoped ZnMgSe bottom barrier, 20+10 nm ZnMgSe+ZnMgSe:Cl top barrier; Se-II; Halter 10-3;

Buffer: M2_10_235

Process Plan

Nr	material	gr.	state		mole	thickness		time	time	thickness		total
#		mode	#	id	frac.	in (nm)	in (ML)	hhmmss,xxx	hhmmss,xxx	in (nm)	in (ML)	time
0	GaAs	MBE	0	r	1.00	500.0	1768.9	4206.969		0.0	0.0	
1												
2	ZnSe	ANW	0	s	1.00		0.0	0.000	30.000	2.3	8.2	00:00:30
3	ZnSe	ANW	0	s	1.00		0.0	0.000	130.000	7.0	24.5	00:01:30
4	ZnSe	RC	0	s	1.00		0.0	0.000	30.000	2.3	8.2	00:00:30
5	ZnMgSe	RC	0	s	0.23		0.0	0.000	100.000	5.7	19.9	00:01:00
6	ZnMgSe	MBE	0	s	0.23	24.3	84.3	414.575		0.0	0.0	00:04:15
7	ZnSe	MBE	0	s	1.00	10.0	35.2	209.466		0.0	0.0	00:02:10
8	ZnMgSe	MBE	0	s	0.23	20.0	69.4	329.527		0.0	0.0	00:03:30
9	ZnMgSe	MBE	0	s	0.23	10.0	34.7	144.763		0.0	0.0	00:01:45
10												
11												
12												
13												
14												
15												
16												
17												
18												
19												
20												
	Summation									**81.6**	**284.2**	**00:15:10**

Molekularstrahl-Epitaxie-Protokoll II-VI (2/2) **ZnSe-QW-0430** **07.04.21**

Growth rates used for calculation

Material	estimated		used for calc.	
	ML/s	s/ML	ML/s	s/ML
GaAs			0.700	1.429
ZnSe	0.272	3.676	0.272	3.676
MgSe	0.061	16.313		n.a.
CdSe	0.000	#DIV/0!		n.a.
ZnMgSe	0.333	3.000	0.331	3.021
ZnCdSe	0.272	3.676		n.a.
ZnCdMgSe	0.333	3.000		n.a.

Growth rates measured by RHEED

Azimute	Gr.Rate	Comment	Azimute	Gr.Rate	Comment
	ML/s			ML/s	
01_ZnSe-a	0.298	24,5 mm			
02_ZnSe	0.272				
03_ZnMgSe	0.323				
04_ZnMgSe	0.331				
			#0427	0.243	ZnSe
			#0427	0.289	ZnMgSe

Starting material flux parameters

Cell-type	Temp.	BEP	Backgr.	Flux	s	type	ratio	
	°C	10-7mbar	10-7mbar	10-7mbar				
Zn	205	6.830	0.000	6.830	1.00	Zn:Se	0.26	
SeII	243	26.200		26.200	1.00	Se:Zn	3.84	
Mg	228	0.733	0.000	0.733	2.10	Mg:Zn	0.23	T(cracker)
Cd	40			0.000	0.64	Cd:Zn	0.00	90
Se	50		0.000	0.000	1.00	Se:Me	3.13	100
Zn-i	50			0.000	1.00			70
Se-i	50			0.000	1.00			50
ZnCl2	230			0.000	1.00			500
ZnF2	250	0.000	0.000	0.000	1.00			400

x10-11 mbar

Growth Parameters

Sub.Typ 2"GaAs/Un

ZnSe start proc.: 30s Zn, 10s break, 30s ZnSe, break, 1m30s ZnSe

Sub. Temp.: 270 °C Gr. 290 °C

After growth

Cell-type	Temp.	BEP
	°C	10-7mbar
Zn	205	6.870
SeII	243	23.800
Mg	228	0.802

Process Notes

Step/Time	Note	Step/Time	Note
00:00:00	142°, 24.5mm		
anw			
RC			

Figure A.17: Growth sheet for an exemplary ZnSe/ZnMgSe heterostructure with a ZnSe quantum well. Growth sheet from Nils von den Driesch.

Table A.4: Experimental and theoretical material properties for $Zn_{1-x}Mg_xSe$.

property	unit	experiment	theory
ϵ_r (x=1)	1		7.3 [202]
m_{eff} (x=1)	m_e	0.23 [140]	0.1 [203]
E_g (x=1)	eV	3.74 [130], 4.0 [131]	
FLP	eV	0.12+X [92]	0.12+X, 0.13+X [92, 201]
n_c (x=0.2)	10^{17} cm^{-3}	≥ 5 [150]	7 [123, 140]

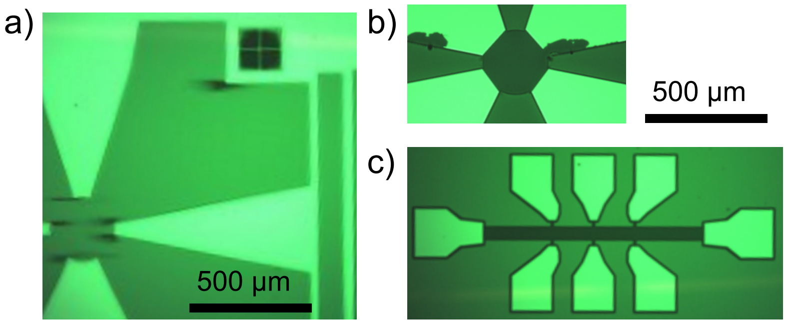


Figure A.18: Possible failure modes by wetchemical etching. a) Low agitation during etch i.e. in absence of ultrasonification leads to inhomogeneous etch result. b) Strong uncontrolled etching of Al is observed at the boundaries of resist protected Al structures without overlap margin. c) Overlap margin of 3 μm sufficiently protects Al from the etchant.

A.6. FINAL DEVICE

Table A.5: Van der Pauw Hall mobility measurement of substrates used for gated Hall-bar devices, see Sect. 6.2.

	SIMS, c_{Cl}			Hall (vdP)			
ID	QW	upper barrier		n_{RT}	μ_{RT}	n_{30K}	μ_{30K}
	c (cm^{-3})	c_{max} (cm^{-3})	c_{min} (cm^{-3})	(cm^{-3})	(cm²/Vs)	(cm^{-3})	(cm²/Vs)
342	2.0E+17	1.0E+19	2.0E+18	2.2E+18	63	1.2E+18	8
344	2.0E+17	4.0E+18	3.0E+18	1.5E+18	140	7.0E+17	9
346	2.0E+17	1.0E+19	5.0E+18	1.5E+18	70	8.0E+17	1
353	2.0E+17	8.0E+18	6.0E+18	2.5E+18	110	1.1E+17	1

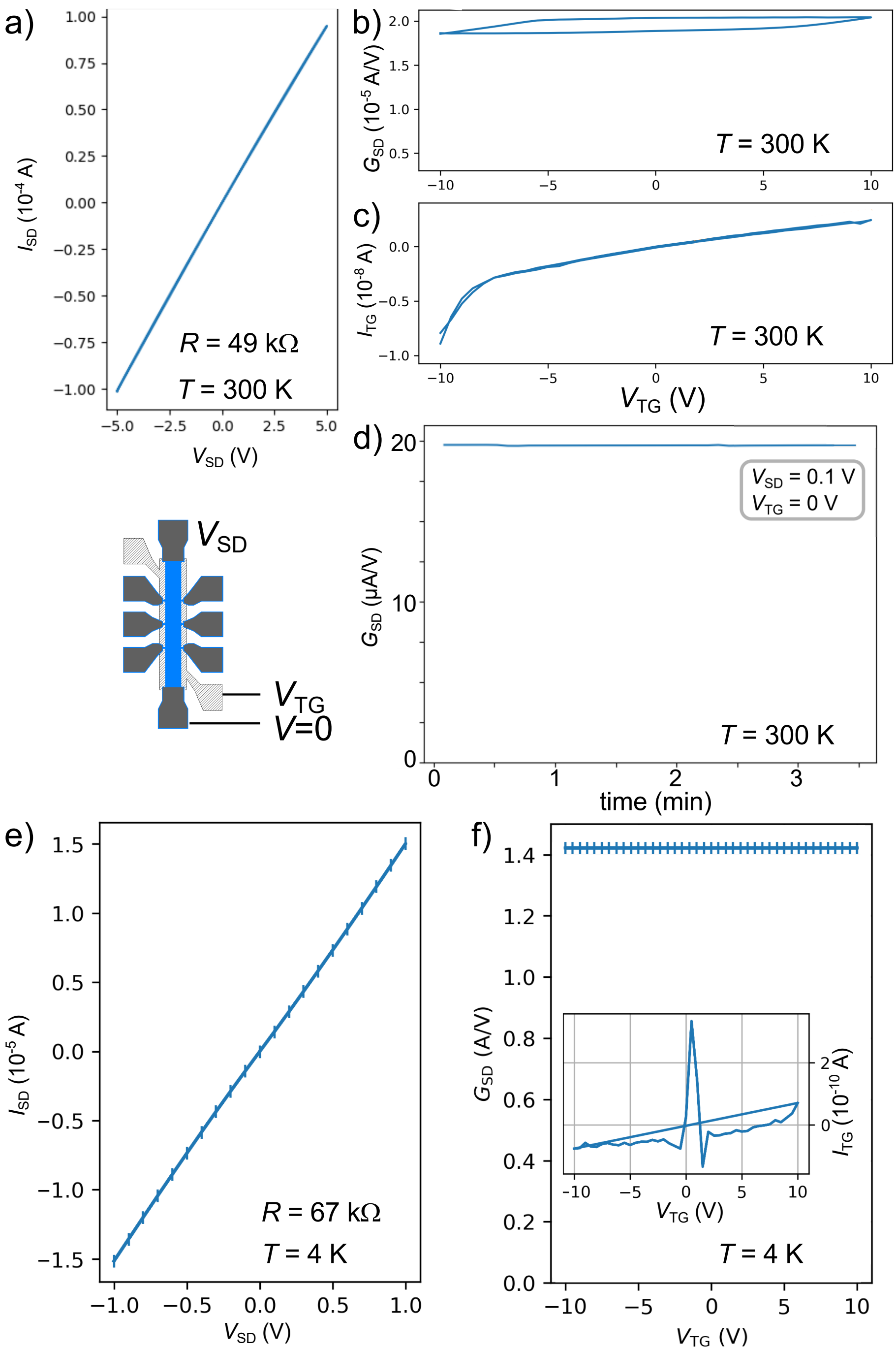


Figure A.19: Electrical characterization at RT and 4 K of a gated Hall-bar fabricated on a ZnSe/ZnMgSe HS with doped QW. a) Linear IV characteristics of the device resistance with a total resistance of 19 kΩ (19 kΩ) at RT at room light. b) G_{SD} vs V_{TG} at RT for $V_{SD} = 0.1$ V (blue curve) and 0.025 V (orange curve). The corresponding leakage current through the gate is depicted in c). d) G_{SD} vs V_{TG} at 4 K. Note, the IV curve shown in panel a) does not correspond to the device characterised in panels b-d). The dimensions of the mesa channel are 50 µm × 800 µm. The sheet resistance determined by van der Pauw Hall on a different piece of this substrate is 3 kΩ/□ (5 kΩ/□) at RT (25 K).

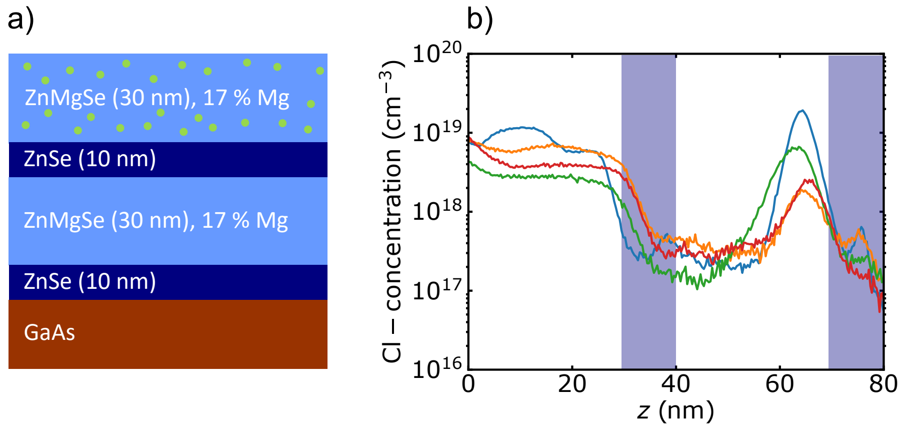


Figure A.20: SIMS characterization of HS with QW used for FETs. a) HS profile and b) Cl concentration determined by SIMS versus penetration depth (z). The surface corresponds to $z = 0$, peaks within the first 5 nm are measurement artefacts. The position of the nominally undoped QW is highlighted in blue, and the signal drop for z close to 80 nm results from probing the II-VI/III-V heterojunction expected there. A FET (hallbar) device built on the substrate corresponding to the green doping profile is electrically characterised, see Sect. 6.2. Figure adopted from Ref. [148].

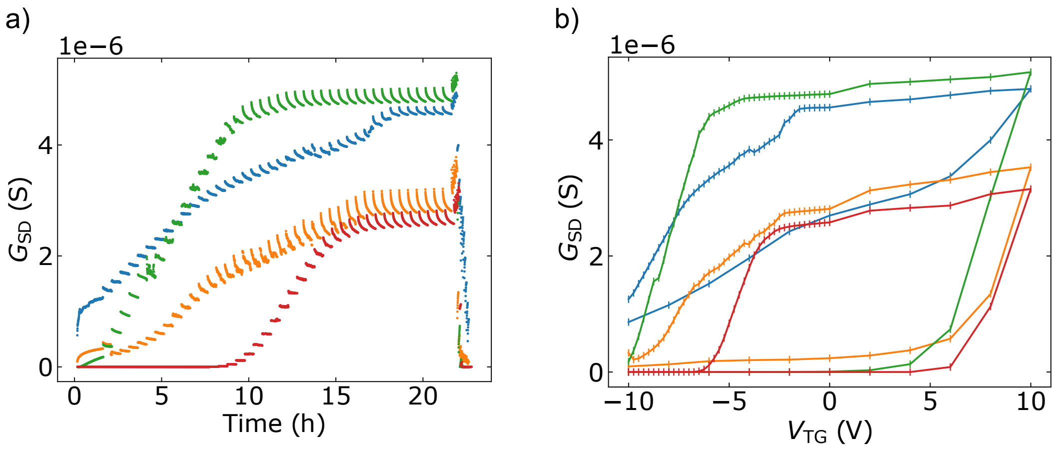


Figure A.21: Characterization of a Field Effect Transistor on a ZnSe/ZnMgSe HS with undoped QW. a) G_{SD} versus measurement time for FETs with gate voltage V_{TG} applied (for details of the measurement protocol see Sect. 6.1). The measurement is performed at room temperature measurement in darkness with V_{SD} of 0.1 V. b) G_{SD} versus V_{TG} for the same measurements as shown in a). Figure adopted from Ref. [148].

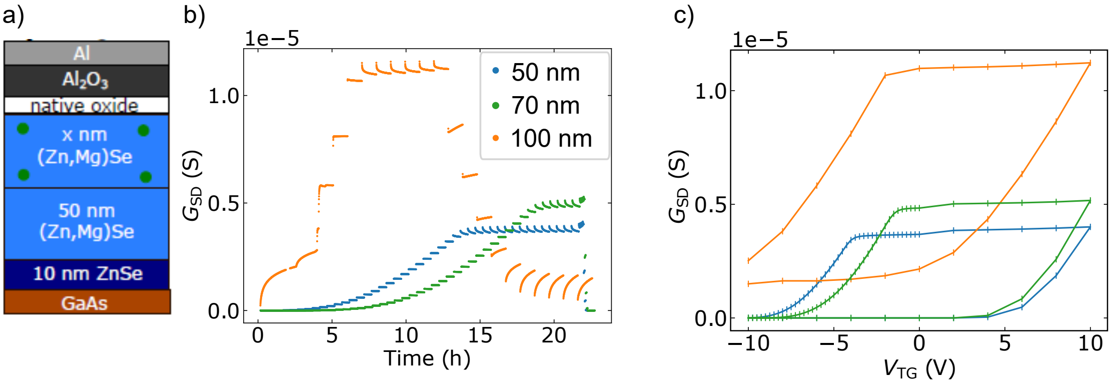


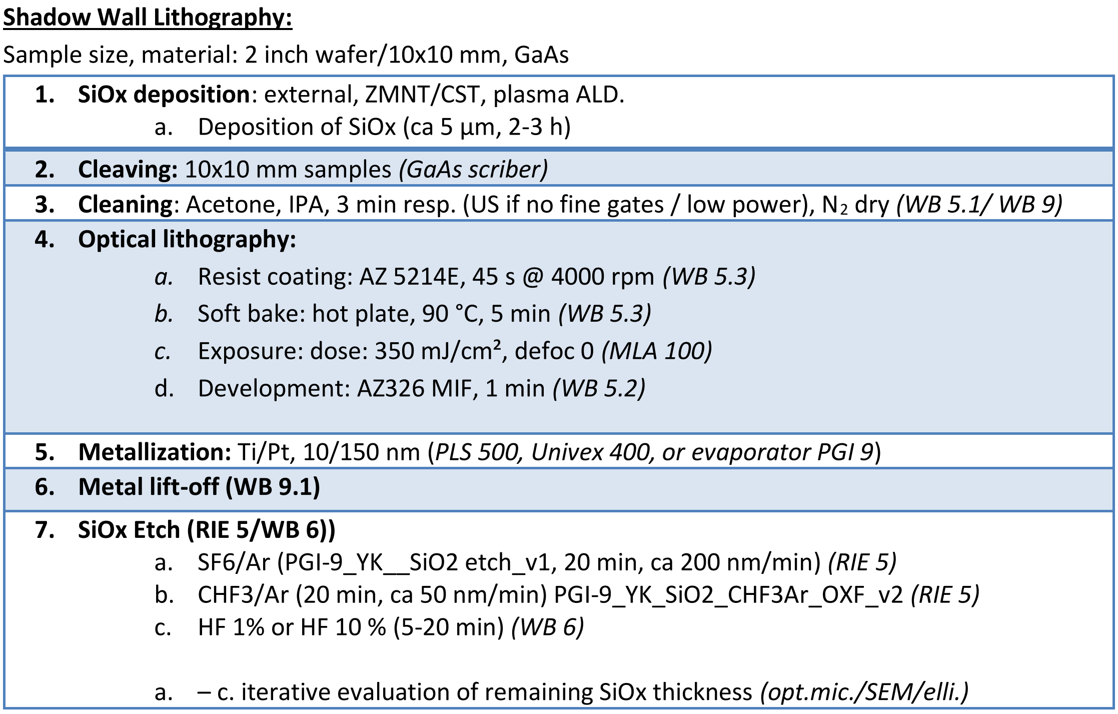
Figure A.22: Characterization of a Field Effect Transistor on a ZnSe/ZnMgSe HS without QW. a) G_{SD} versus measurement time for FETs with gate voltage V_{TG} applied (for details of the measurement protocol see Sect. 6.1). The measurement is performed at room temperature measurement in darkness with V_{SD} of 0.1 V. b) G_{SD} versus V_{TG} for the same measurements as shown in a). Figure adopted from Ref. [148].

A.7. LOCAL OHMIC CONTACTS FABRICATED BY SELECTIVE EPITAXIAL GROWTH

In this thesis, two fabrication processes for local ohmic contacts have been presented and benchmarked. Here I provide a conceptual comparison of the two methods in Tab. A.6. Both processes rely on structuring, selective epitaxial growth and metallization *in-situ*, but also have some significant differences in structuring and contact design. The comparison is based on the processes outlined in Fig. 5.10 and in Fig. 7.3. Results from electrical characterization shown here refer to analysis results of Samples RG and Sample E listed in Tab. 3.7 and Tab. 7.1, respectively.

Table A.6: Comparison of methods for local ohmic contacts to n-ZnSe.

property	regrowth	shadow mask epitaxy
sample	RG (Sect. 3.4.2)	E
metallization	*in-situ*	*in-situ*
limiting factor (contact size)	opt. litho.	wall height, MBE cell angle
fab prior to growth	hard mask (2D)	shadow mask (3D)
surface treatment	RIE (1 step), wet + H etch	RIE (3 steps), wet + H etch
n (cm^{-3})	0.5×10^{19}–2×10^{19}	0.5×10^{19}–2×10^{19}
ρ_c ($\Omega\,cm^2$), measured at 4 K	1×10^{-3}	2.5×10^{-3}
ρ_c ($\Omega\,cm^2$), expected at 4 K	$<1 \times 10^{-3}$	1×10^{-5}



Shadow Wall Lithography:

Sample size, material: 2 inch wafer/10x10 mm, GaAs

1. **SiOx deposition**: external, ZMNT/CST, plasma ALD.
    a. Deposition of SiOx (ca 5 µm, 2-3 h)
2. **Cleaving:** 10x10 mm samples *(GaAs scriber)*
3. **Cleaning**: Acetone, IPA, 3 min resp. (US if no fine gates / low power), N_2 dry *(WB 5.1/ WB 9)*
4. **Optical lithography:**
    a. Resist coating: AZ 5214E, 45 s @ 4000 rpm *(WB 5.3)*
    b. Soft bake: hot plate, 90 °C, 5 min *(WB 5.3)*
    c. Exposure: dose: 350 mJ/cm², defoc 0 *(MLA 100)*
    d. Development: AZ326 MIF, 1 min *(WB 5.2)*
5. **Metallization:** Ti/Pt, 10/150 nm (*PLS 500, Univex 400, or evaporator PGI 9*)
6. **Metal lift-off (WB 9.1)**
7. **SiOx Etch (RIE 5/WB 6))**
    a. SF6/Ar (PGI-9_YK__SiO2 etch_v1, 20 min, ca 200 nm/min) *(RIE 5)*
    b. CHF3/Ar (20 min, ca 50 nm/min) PGI-9_YK_SiO2_CHF3Ar_OXF_v2 *(RIE 5)*
    c. HF 1% or HF 10 % (5-20 min) *(WB 6)*

    a. – c. iterative evaluation of remaining SiOx thickness *(opt.mic./SEM/elli.)*

Figure A.23: Run sheet for prestructuring of shadow walls. Process developed by Yurii Kutovyi.

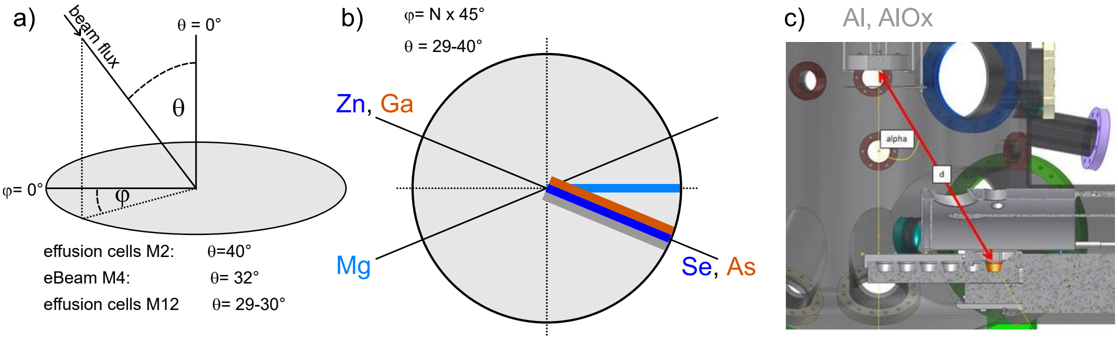


Figure A.24: Cell alignment for growth chambers in Nanocluster. a) Schematic view of cell orientation with respect to wafer orientation in 3D. b) In plane cell alignment for the individual growth chambers highlighted by color: Orange for III-V chamber M2, blue for II-VI chamber M12 and grey for metal (oxide) chamber M4. c) Visualization of the chamber geometry in the case of chamber M4.

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LIST OF PUBLICATIONS

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